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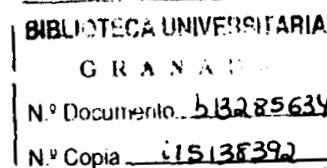
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DESIGN WITH OPERATIONAL AMPLIFIERS AND ANALOG INTEGRATED CIRCUITS

THIRD EDITION

Sergio Franco

San Francisco State University



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Luigia Braidotti and Luigi Franco*

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THIRD EDITION

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CONTENTS

Preface	xi
1 Operational Amplifier Fundamentals	1
1.1 Amplifier Fundamentals	2
1.2 The Operational Amplifier	5
1.3 Basic Op Amp Configurations	8
1.4 Ideal Op Amp Circuit Analysis	15
1.5 Negative Feedback	23
1.6 Feedback in Op Amp Circuits	29
1.7 The Loop Gain	37
1.8 Op Amp Powering	41
Problems	47
Bibliography	58
Appendix 1A Standard Resistor Values	58
2 Circuits with Resistive Feedback	60
2.1 Current-to-Voltage Converters	61
2.2 Voltage-to-Current Converters	63
2.3 Current Amplifiers	71
2.4 Difference Amplifiers	73
2.5 Instrumentation Amplifiers	79
2.6 Instrumentation Applications	86
2.7 Transducer Bridge Amplifiers	91
Problems	98
References	105
3 Active Filters: Part I	106
3.1 The Transfer Function	109
3.2 First-Order Active Filters	115
3.3 Audio Filter Applications	121
3.4 Standard Second-Order Responses	126
3.5 KRC Filters	133
3.6 Multiple-Feedback Filters	141
3.7 State-Variable and Biquad Filters	144
3.8 Sensitivity	150
Problems	153
References	158
4 Active Filters: Part II	160
4.1 Filter Approximations	161
4.2 Cascade Design	166
4.3 Generalized Impedance Converters	175
4.4 Direct Design	181

4.5 The Switched Capacitor	187
4.6 Switched-Capacitor Filters	192
4.7 Universal SC Filters	198
Problems	204
References	210
5 Static Op Amp Limitations	211
5.1 Simplified Op Amp Circuit Diagram	212
5.2 Input Bias and Offset Currents	217
5.3 Low-Input-Bias-Current Op Amps	221
5.4 Input Offset Voltage	225
5.5 Low-Input-Offset-Voltage Op Amps	230
5.6 Input Offset-Error Compensation	235
5.7 Maximum Ratings	240
Problems	244
References	248
Appendix 5A Data Sheets of the $\mu A741$ Op Amp	249
6 Dynamic Op Amp Limitations	258
6.1 Open-Loop Response	259
6.2 Closed-Loop Response	263
6.3 Input and Output Impedances	269
6.4 Transient Response	275
6.5 Effect of Finite GBP on Integrator Circuits	283
6.6 Effect of Finite GBP on Filters	289
6.7 Current-Feedback Amplifiers	293
Problems	303
References	309
7 Noise	311
7.1 Noise Properties	313
7.2 Noise Dynamics	317
7.3 Sources of Noise	322
7.4 Op Amp Noise	328
7.5 Noise in Photodiode Amplifiers	335
7.6 Low-Noise Op Amps	339
Problems	342
References	346
8 Stability	347
8.1 The Stability Problem	348
8.2 Stability in Constant-GBP Op Amp Circuits	356
8.3 Internal Frequency Compensation	365
8.4 External Frequency Compensation	374
8.5 Stability in CFA Circuits	381
8.6 Composite Amplifiers	384
Problems	390
References	396
9 Nonlinear Circuits	398
9.1 Voltage Comparators	399
9.2 Comparator Applications	407

9.3	Schmitt Triggers	416
9.4	Precision Rectifiers	422
9.5	Analog Switches	428
9.6	Peak Detectors	433
9.7	Sample-and-Hold Amplifiers	437
	Problems	443
	References	448
10	Signal Generators	449
10.1	Sine Wave Generators	451
10.2	Multivibrators	457
10.3	Monolithic Timers	465
10.4	Triangular Wave Generators	471
10.5	Sawtooth Wave Generators	476
10.6	Monolithic Waveform Generators	478
10.7	V-F and F-V Converters	486
	Problems	492
	References	497
11	Voltage References and Regulators	499
11.1	Performance Specifications	500
11.2	Voltage References	506
11.3	Voltage-Reference Applications	512
11.4	Linear Regulators	519
11.5	Linear Regulator Applications	527
11.6	Switching Regulators	535
11.7	Monolithic Switching Regulators	544
	Problems	551
	References	557
12	D-A and A-D Converters	559
12.1	Performance Specifications	561
12.2	D-A Conversion Techniques	567
12.3	Multiplying DAC Applications	580
12.4	A-D Conversion Techniques	584
12.5	Oversampling Converters	595
	Problems	603
	References	606
13	Nonlinear Amplifiers and Phase-Locked Loops	607
13.1	Log/Antilog Amplifiers	608
13.2	Analog Multipliers	615
13.3	Operational Transconductance Amplifiers	620
13.4	Phase-Locked Loops	627
13.5	Monolithic PLLs	635
	Problems	642
	References	646
	Index	647

PREFACE

During the last decades much has been prophesized that there will be little need for analog circuitry in the future because digital electronics is taking over. Far from having proven true, this contention has provoked controversial rebuttals, as epitomized by statements such as "If you cannot do it in digital, it's got to be done in analog." Add to this the common misconception that analog design, compared to digital design, seems to be more of a whimsical art than a systematic science, and what is the confused student to make of this controversy? Is it worth pursuing some coursework in analog electronics, or is it better to focus just on digital?

There is no doubt that many functions that were traditionally the domain of analog electronics are nowadays implemented in digital form, a popular example being offered by digital audio. Here, the analog signals produced by microphones and other acoustic transducers are suitably conditioned by means of amplifiers and filters, and are then converted to digital form for further processing, such as mixing, editing, and the creation of special effects, as well as for the more mundane but no less important tasks of transmission, storage, and retrieval. Finally, digital information is converted back to analog signals for playing through loudspeakers. One of the main reasons why it is desirable to perform as many functions as possible digitally is the generally superior reliability and flexibility of digital circuitry. However, *the physical world is inherently analog*, indicating that there will *always* be a need for analog circuitry to condition physical signals such as those associated with transducers, as well as to convert information from analog to digital for processing, and from digital back to analog for reuse in the physical world. Moreover, new applications continue to emerge, where considerations of speed and power make it more advantageous to use analog front ends; wireless communications provide a good example.

Indeed many applications today are best addressed by mixed-mode integrated circuits (mixed-mode ICs) and systems, which rely on analog circuitry to interface with the physical world, and digital circuitry for processing and control. Even though the analog circuitry may constitute only a small portion of the total chip area, it is often the most challenging part to design as well as the limiting factor on the performance of the entire system. In this respect, it is usually the analog designer who is called to devise ingenious solutions to the task of realizing analog functions in decidedly digital technologies; switched-capacitor techniques in filtering and sigma-delta techniques in data conversion are popular examples. In light of the above, the need for competent analog designers will continue to remain very strong. Even purely digital circuits, when pushed to their operational limits, exhibit analog behavior. Consequently, a solid grasp of analog design principles and techniques is a valuable asset in the design of any IC, not just purely digital or purely analog ICs.

THE BOOK

The goal of this book is the illustration of general analog principles and design methodologies using practical devices and applications. The book is intended as a

textbook for undergraduate and graduate courses in design and applications with analog integrated circuits (analog ICs), as well as a reference book for practicing engineers. The reader is expected to have had an introductory course in electronics, to be conversant in frequency-domain analysis techniques, and to possess basic skills in the use of PSpice. Though the book contains enough material for a two-semester course, it can also serve as basis for a one-semester course after suitable selection of topics. The selection process is facilitated by the fact that the book as well as its individual chapters have generally been designed to proceed from the elementary to the complex.

At San Francisco State University we use the book for a sequence of two one-semester courses, one at the senior and the other at the graduate level. In the senior course we cover Chapters 1–3, Chapters 5 and 6, and most of Chapters 9 and 10; in the graduate course we cover all the rest. The senior course is taken concurrently with a course in analog IC fabrication and design. For an effective utilization of analog ICs, it is important that the user be cognizant of their internal workings, at least qualitatively. To serve this need, the book provides intuitive explanations of the technological and circuit factors intervening in a design decision.

The third edition retains the features that distinguished the second edition from the first: namely, considerable pedagogical enhancements, inclusion of PSpice simulations, and expanded subject coverage to include, among others, current-feedback amplifiers, switching regulators, sigma-delta converters, and phase-locked loops. In addition, negative-feedback concepts have been clarified and emphasized further, and the number of end-of-chapter problems has been increased by 10% to achieve a total of 579. Although many readers will undoubtedly prefer to use Windows versions of PSpice, it was decided after much deliberation to retain the netlist version of the second edition because of its pedagogical advantages. However, the interested reader can find Windows versions of the book's netlist examples in the accompanying Website at <http://www.mhhe.com/franco>.

The desire to address general and lasting principles in a manner that transcends the latest technological trend has motivated the choice of well-established and widely documented devices and technologies as vehicles to illustrate such principles. However, whenever necessary, the reader is made aware of more contemporary alternatives, as well as bibliographical sources and where to find them.

THE CONTENTS AT A GLANCE

Although not explicitly indicated, the book consists of three parts. Part I (Chapters 1–4) introduces fundamental concepts and applications based on the op amp as a predominantly ideal device. It is felt that the student needs to develop sufficient confidence with ideal (or near-ideal) op amp situations before tackling and assessing the consequences of practical device limitations. Limitations are the subject of Part II (Chapters 5–8), which covers the topic in more systematic detail than previous editions. Finally, Part III (Chapters 9–13) exploits the maturity and judgment developed by the reader in the first two parts to address a variety of design-oriented applications. Following is a brief chapter-by-chapter description of the material covered.

Chapter 1 reviews basic amplifier concepts, including negative feedback. Much emphasis is placed on the loop gain T as a gauge of circuit performance. The student is introduced to simple PSpice models, which will become more sophisticated as

we progress through the book. Those instructors who find the loop-gain treatment overwhelming this early in the book, may skip it to return to it later, at a more suitable time. Coverage rearrangements of this sort are facilitated by the fact that individual sections and chapters have been designed to be as independent as possible from each other; moreover, the end-of-chapter problems are grouped by section.

Chapter 2 deals with I - V , V - I , and I - I converters, along with various instrumentation and transducer amplifiers. The chapter places much emphasis on feedback topologies and the role of the loop gain T .

Chapter 3 covers first-order filters, audio filters, and popular second-order filters such as the KRC , multiple-feedback, state-variable, and biquad topologies. The chapter emphasizes complex-plane systems concepts, and concludes with filter sensitivities.

The reader who wants to go deeper into the subject of filters will find Chapter 4 useful. This chapter covers higher-order filter synthesis using both the cascade and the direct approaches. Moreover, these approaches are presented for both the case of active RC filters and the case of switched-capacitor (SC) filters.

Chapter 5 addresses input-referrable op amp errors such as V_{OS} , I_B , I_{OS} , CMRR, PSRR, and drift, along with operating limits. The student is introduced to data-sheet interpretation, PSpice macromodels, and also to different technologies and topologies.

Chapter 6 addresses dynamic limitations in both the frequency and time domains, and investigates their effect on the resistive circuits and the filters that were studied in Part I using mainly ideal op amp models. Voltage-feedback and current-feedback are compared in detail, and PSpice is used extensively to visualize both the frequency and transient responses of representative circuit examples. Having mastered the material of the first four chapters using ideal or nearly-ideal op amps, the student is now in a better position to appreciate and evaluate the consequences of practical device limitations.

The subject of ac noise, covered in Chapter 7, follows naturally since it combines the principles learned both in Chapters 5 and 6. Noise calculations and estimation represent another area in which PSpice proves a most useful tool.

Part II concludes with the subject of stability, in Chapter 8. The material has been arranged to facilitate topic selection, and puts much emphasis on a systems-oriented approach. Again, PSpice is used profusely to visualize the effect of the different frequency-compensation techniques presented.

Part III begins with nonlinear applications, in Chapter 9. Here, nonlinear behavior stems from either the lack of feedback (voltage comparators), or the presence of feedback, but of the positive type (Schmitt triggers), or the presence of negative feedback, but using nonlinear elements such as diodes and switches (precision rectifiers, peak detectors, track-and-hold amplifiers).

Chapter 10 covers signal generators, including Wien-bridge and quadrature oscillators, multivibrators, timers, function generators, and V - F and F - V converters.

Chapter 11 addresses regulation. It starts with voltage references, proceeds to linear voltage regulators, and concludes with switching regulators. The last topic has been at the center of much attention and industrial activity since the eighties, and entire books have been written on the subject. Of necessity, this chapter exposes the student only to the fundamentals of this most important area.

Chapter 12 deals with data conversion. Data-converter specifications are treated in systematic fashion, and various applications with multiplying DACs are presented. The chapter concludes with oversampling-conversion principles and sigma-delta

converters. Much has been written also about this subject, so this chapter of necessity exposes the student only to the fundamentals.

Chapter 13 concludes the book with a variety of nonlinear circuits, such as log/antilog amplifiers, analog multipliers, and operational transconductance amplifiers with a brief exposure to g_m - C filters. The chapter culminates with an introduction to phase-locked loops, a subject that combines important materials addressed at various points in the preceding chapters.



THE WEBSITE

The book is accompanied by a website (<http://www.mhhe.com/franco>) containing a variety of Instructor and Student Resources as well as other useful links. A website icon has been placed in the margin in those places in the text where the website resources would prove most useful. The Instructor Resources consist of a Solutions Manual, Downloadable Software, Windows Version of PSpice Examples, and PageOut (a link to McGraw-Hill's course Website Development Tools). The Student Resources consist of Downloadable Software and Windows Version of PSpice Examples. The author welcomes feedback via email, at sfranco@sfsu.edu.

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Some of the changes in the third edition were made in response to feedback received from a number of readers in both industry and academia, and I am grateful to all who took the time to e-mail me. In addition, the following reviewers provided detailed commentaries on the previous edition as well as valuable suggestions for the current revision. All suggestions have been examined in detail, and if only a portion of them has been honored, it was not out of callousness, but because of production constraints or personal philosophy. To all reviewers, my sincere thanks: J. Alvin Connelly, Georgia Institute of Technology; Dragan Maksimovic, University of Colorado-Boulder; Philip C. Munro, Youngstown State University; Thomas G. Owen, University of North Carolina-Charlotte; Dr. Guillermo Rico, New Mexico State University; Mahmoud F. Wagdy, California State University-Long Beach; Subbaraya Yuvarajan, North Dakota State University. Richard C. Jaeger, Auburn University also gave input on the issue of PSpice.

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Sergio Franco
San Francisco, California, 2001

1

OPERATIONAL AMPLIFIER FUNDAMENTALS

- 1.1 Amplifier Fundamentals
- 1.2 The Operational Amplifier
- 1.3 Basic Op Amp Configurations
- 1.4 Ideal Op Amp Circuit Analysis
- 1.5 Negative Feedback
- 1.6 Feedback in Op Amp Circuits
- 1.7 The Loop Gain
- 1.8 Op Amp Powering
 - Problems
 - Bibliography
 - Appendix 1A

The term *operational amplifier*, or *op amp* for short, was coined in 1947 by John R. Ragazzini to denote a special type of amplifier that, by proper selection of its external components, could be configured for a variety of operations such as amplification, addition, subtraction, differentiation, and integration. The first applications of op amps were in analog computers. The ability to perform mathematical operations was the result of combining high gain with negative feedback.

Early op amps were implemented with vacuum tubes, so they were bulky, power-hungry, and expensive. The first dramatic miniaturization of the op amp came with the advent of the bipolar junction transistor (BJT), which led to a whole generation of op amp modules implemented with discrete BJTs. However, the real breakthrough occurred with the development of the integrated circuit (IC) op amp, whose elements are fabricated in monolithic form on a silicon chip the size of a pinhead. The first such device was developed by Robert J. Widlar at Fairchild Semiconductor Corporation in the early 1960s. In 1968 Fairchild introduced the op amp that was to become the industry standard, the popular $\mu A741$. Since then the number of op amp families and manufacturers has swollen considerably. Nevertheless, the 741 remains one of

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13

NONLINEAR AMPLIFIERS AND
PHASE-LOCKED LOOPS

- 13.1 Log/Antilog Amplifiers
- 13.2 Analog Multipliers
- 13.3 Operational Transconductance Amplifiers
- 13.4 Phase-Locked Loops
- 13.5 Monolithic PLLs
- Problems
- References

The highly predictable characteristic of the bipolar junction transistor is exploited in the realization of some very useful nonlinear functions, such as logarithmic conversion and variable transconductance multiplication. These functions, in turn, provide the basis for a variety of other analog operations, such as antilogarithmic amplification, true rms conversion, analog division and square-root computation, various forms of linearization, and voltage-controlled amplification, filtering, and oscillation. These precise building blocks simplify analog design considerably while broadening the scope of practical analog circuits to applications where considerations of speed or cost require implementation in analog rather than digital form.

Another important class of nonlinear circuits is provided by phase-locked loops. Though unrelated to those just mentioned, PLLs encompass many of the important topics that we have studied so far. We thus find it appropriate to conclude the book with this subject.

13.1
LOG/ANTILOG AMPLIFIERS

A logarithmic amplifier—also called *log amp*, or *logger*—is an I - V converter with a transfer characteristic of the type

$$v_O = V_o \log_b \frac{i_I}{I_i} \quad (13.1)$$

where V_o is called the *output scale factor*, I_i the *input reference current*, and b is the *base*, usually 10 or 2. V_o represents the sensitivity of the log amp, in volts per decade (or per octave), and I_i is the value of i_I for which $v_O = 0$. Note that for proper operation we must always have $i_I/I_i > 0$. The quantity

$$\text{DR} = \log_b \frac{|i_I|_{\max}}{|i_I|_{\min}} \quad (13.2)$$

is called the *dynamic range* and is expressed in decades or in octaves, depending on b . For instance, a logger designed to operate over the range $1 \text{ nA} \leq i_I \leq 1 \text{ mA}$ has $\text{DR} = \log_{10}(10^{-3}/10^{-9}) = 6$ decades, or $\text{DR} = \log_2 10^6 \cong 20$ octaves.

Plotting Eq. (13.1) on semilog paper with i_I/I_i on the logarithmic axis and v_O on the linear axis, as in Fig. 13.1a, yields a straight line with a slope of V_o V/dec. Any departure of the actual characteristic from the best-fit straight line is called the *log conformity error* e_O . Though this error can only be observed at the output, it is convenient to refer it to the input because of the unique log-function property that equal percentage errors at the input produce equal incremental errors at the output, regardless of the point on the curve. Indeed, denoting the percentage input error as p , we have $e_O = v_{O(\text{actual})} - v_{O(\text{ideal})} = V_o \log_b[(1+p)(i_I/I_i)] - V_o \log_b[i_I/I_i]$, or

$$e_O = V_o \log_b(1+p) \quad (13.3)$$

For instance, with $b = 10$ and $V_o = 1$ V/dec, a 1% input error corresponds to an output error $e_O = 1 \log_{10}(1+0.01) = 4.32$ mV. Conversely, $e_O = 10$ mV corresponds to a percentage error p such that $10 \text{ mV} = 1 \log_{10}(1+p)$, or $p = 2.33\%$.

The main application of log amps is data compression. As an example, consider the digitization of a photodetector current over the range $10 \text{ nA} \leq i_I \leq 100 \text{ } \mu\text{A}$ with an error of less than 1% of its actual value. Since we have a four-decade range, the required resolution is $0.01/10^4 = 1/10^6$, or 1 ppm. Since $10^6 \cong 2^{20}$, this requires

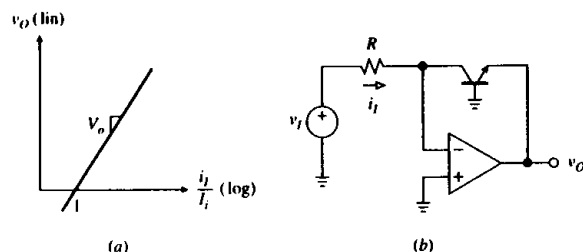


FIGURE 13.1
Logarithmic characteristic and the transdiode configuration.

a 20-bit A/D converter, which can be a challenging and expensive proposition. Consider now the effect of compressing the input with a log amp before digitizing. Letting, for instance, $b = 10$, $V_o = 1$ V/dec, and $I_i = 10$ nA, the current range is now compressed to a 0 to 4-V voltage range. Since a 1% current accuracy corresponds to a 4.32-mV voltage interval, the required resolution is now $(4.32 \times 10^{-3})/4 \cong 1/926 \cong 1/2^{10}$, or 10 bits. This represents a substantial reduction in cost and circuit complexity!

The inverse function of logarithmic compression is exponential expansion. This is provided by the *antilogarithmic amplifier* (antilog amp), whose transfer characteristic is

$$i_O = I_o b^{v_I/V_i} \quad (13.4)$$

where I_o is the *output reference current* and V_i the *input scale factor*, in volts per decade or per octave. The output of an antilog amp can be converted to a voltage by means of an op amp I - V converter. When plotted on semilog paper with v_I on the linear axis and i_O/I_o on the logarithmic axis, Eq. (13.4) also yields a straight line. The above log conformity error considerations still hold, but with the input and output errors interchanged.

The Transdiode Configuration

Log/antilog amplifiers exploit the exponential characteristic of a forward-active BJT. By Eq. (5.3), this characteristic can be written as $v_{BE} = V_T \ln(i_C/I_s)$. Practical logging BJTs conform to this equation remarkably well over a range of at least six decades,¹ typically for $0.1 \text{ nA} \leq i_C \leq 0.1 \text{ mA}$. The heart of log/antilog amps is the circuit of Fig. 13.1b, known as the *transdiode configuration*. The op amp converts v_I to the current $i_I = v_I/R$, and then forces the BJT in its feedback path to respond with a logarithmic base-emitter voltage drop to yield

$$v_O = -V_T \ln \frac{v_I}{R I_s} \quad (13.5)$$

If we take into account also the input bias voltage V_{OS} and bias current I_B , then the collector current becomes $i_C = (v_I - V_{OS})/R - I_B$, so the transfer characteristic takes on the more realistic form

$$v_O = -V_T \ln \frac{v_I - V_{OS} - R I_B}{R I_s} \quad (13.6)$$

The input offset error ($V_{OS} + R I_B$) sets the ultimate limit on the range of inputs that can be processed within a given log conformity error. Wide-dynamic-range loggers use op amps with ultra-low V_{OS} and I_B to approach the ideal characteristic of Eq. (13.5). The ultimate limit is then posed by drift and noise. If the transdiode is driven directly with a current source i_I , Eq. (13.5) reduces to $v_O = -V_T \ln(i_I/I_s)$, and the ultimate limit is now set by the input bias current of the op amp or by the low-end log conformity error of the BJT, whichever is higher. In general, current-driven loggers offer a wider dynamic range than voltage-driven loggers.

Stability Considerations

Transdiode circuits are notorious for their tendency to oscillate due to the presence of an active gain element inside the feedback loop. As shown in Fig. 13.2a, the transdiode is stabilized¹ by using an emitter-degeneration resistance R_E to reduce the feedback factor β , and a feedback capacitance C_f to provide feedback lead. To investigate stability we need to find the feedback factor β . To this end, refer to the ac model of Fig. 13.2b, where the BJT has been replaced by its common-base small-signal model.² The BJT parameters r_e and r_o depend on the operating current I_C as

$$r_e = \frac{\alpha V_T}{I_C} \quad r_o = \frac{V_A}{I_C} \quad (13.7)$$

where V_T is the thermal voltage and V_A is the so-called Early voltage. Typically, $\alpha \cong 1$ and $V_A \cong 100$ V. The base-collector junction capacitance C_μ and the inverting-input stray capacitance C_n are typically on the order of a few picofarads.

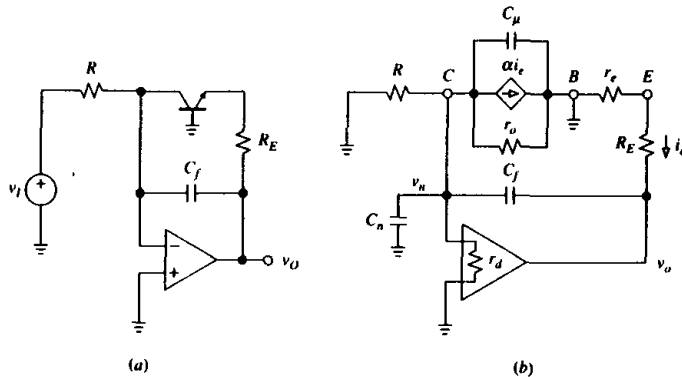


FIGURE 13.2
Transdiode circuit with frequency compensation, and its incremental model.

Circuit analysis is facilitated by the introduction of

$$R_d = R \parallel r_o \parallel r_d \quad R_b = r_e + R_E \quad (13.8)$$

Applying KCL at the summing junction gives

$$v_n[1/R_d + j\omega(C_n + C_\mu)] + \alpha i_e + j\omega C_f(v_n - v_o) = 0$$

Letting $i_e = -v_o/R_b$, rearranging, and solving for $\beta = v_n/v_o$ gives, for $\alpha \cong 1$,

$$\frac{1}{\beta} = \frac{R_b}{R_d} \frac{1 + jf/f_z}{1 + jf/f_p} \quad (13.9)$$

where the zero and pole frequencies are

$$f_z = \frac{1}{2\pi R_d(C_n + C_\mu + C_f)} \quad f_p = \frac{1}{2\pi R_b C_f} \quad (13.10)$$

The $|1/\beta|$ curve has the low-frequency asymptote $1/\beta_0 = R_b/R_d$, the high-frequency asymptote $1/\beta_\infty = 1 + (C_n + C_\mu)/C_f$, and two breakpoints at f_z and f_p . While f_z and $1/\beta_\infty$ are relatively constant, f_p and $1/\beta_0$ depend on the operating current as per Eq. (13.7), so they can vary over a wide range of values, as exemplified in Fig. 13.3. The hardest condition to compensate is when i_C is maximized, since this minimizes $1/\beta_0$ and maximizes f_p , leading to the highest rate of closure. As a rule of thumb,¹ R_E is chosen so that, when i_C is maximized, $1/\beta_0 \cong 0.5$ V/V and $f_p \cong 0.5 f_x$, where f_x is the crossover frequency.

EXAMPLE 13.1. In the circuit of Fig. 13.2a let $R = 10$ k Ω , 1 mV $< v_i < 10$ V, $C_n + C_\mu = 20$ pF, $V_A = 100$ V, $r_d = 2$ M Ω , and $f_i = 1$ MHz. Find suitable values for R_E and C_f .

Solution. At the upper end of the range, where $i_C = (10 \text{ V})/(10 \text{ k}\Omega) = 1$ mA, we have $r_e \cong 26 \Omega$, $r_o = 100$ k Ω , and $R_d \cong 9$ k Ω . Imposing $(26 + R_E)/9000 = 0.5$ gives $R_E = 4.47$ k Ω (use 4.3 k Ω).

Next, find f_x using the definition $|a(jf_x)| \times \beta_\infty = 1$. Letting $|a(jf_x)| \cong f_i/f_x$ and using $1/\beta_\infty = 1 + (C_n + C_\mu)/C_f$ we get $f_x = f_i/[1 + (C_n + C_\mu)/C_f]$. Imposing $f_p = 0.5 f_x$ and simplifying, we finally obtain

$$C_f = \frac{1 + (C_n + C_\mu)/C_f}{\pi R_b f_i}$$

Substituting the given parameter values, along with $R_b \cong 4.3$ k Ω , gives $C_f = 90$ pF (use 100 pF).

Figure 13.3 indicates that at low values of v_i the response is dominated by f_p , thus resulting in slow dynamics. This is not surprising, since at low current levels it takes longer to charge or discharge the various capacitances. At low currents we have $r_e \gg R_E$, so $f_p \cong 1/2\pi r_e C_f$, indicating a time constant $\tau \cong r_e C_f \cong (V_T/I_C)C_f = (V_T/v_i)RC_f$. For instance, with $C_f = 100$ pF, at $I_C = 1$ nA we have $\tau \cong (0.026/10^{-9})10^{-10} = 2.6$ ms, so we must be prepared for slow dynamics near the low end of the range.

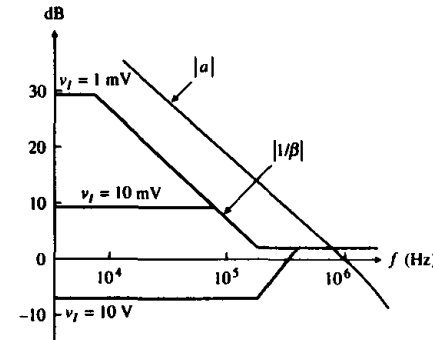


FIGURE 13.3
Bode plots for the transdiode circuit of Example 13.1.

Practical Log/Antilog Circuits³

Both the output scale factor and the input reference term in Eq. (13.5) depend on temperature. The circuit of Fig. 13.4 overcomes this serious drawback by using a matched BJT pair to eliminate I_s , and a temperature-sensitive voltage divider to compensate for $TC(V_T)$. The op amps force the BJTs to develop $v_{BE1} = V_T \ln(i_I/I_{s1})$ and $v_{BE2} = V_T \ln(I_{REF}/I_{s2})$, where $I_{REF} = V_{REF}/R_r$. By the voltage divider formula, $v_{B2} = v_O/(1 + R_2/R_1)$. But, by KVL, $v_{B2} = v_{BE2} - v_{BE1} = V_T \ln[(I_{REF}/I_{s2})(I_{s1}/i_I)]$. Eliminating v_{B2} and using the property $\ln x = 2.303 \log_{10} x$, we get

$$v_O = V_o \log_{10} \frac{i_I}{I_i} \quad (13.11)$$

$$V_o = -2.303 \frac{R_1(T) + R_2}{R_1(T)} V_T \quad I_i = \frac{V_{REF}}{R_r} \times \frac{I_{s2}}{I_{s1}} \quad (13.12)$$

For matched BJTs $I_{s2}/I_{s1} = 1$, so we get the temperature-independent expression $I_i = V_{REF}/R_r$. Moreover, for $R_2 \gg R_1$, we can approximate $V_o \cong -2.303 R_2 V_T / R_1(T)$, indicating that V_o can be thermally stabilized by using a resistance $R_1(T)$ with $TC(R_1) = TC(V_T) = 1/T = 3660 \text{ ppm}/^\circ\text{C}$. A suitable resistor is the Q81 (Tel Labs), which must be mounted in close thermal coupling with the BJT pair. The function of D_1 is to protect the BJTs against inadvertent reverse bias. The use of the LT1012 picoampere-input-current, microvolt-offset, low-noise op amp (Linear Technology) allows for a voltage-logging range of $4\frac{1}{2}$ decades. With the given component values, $V_o = -1 \text{ V/dec}$ and $I_i = 10 \mu\text{A}$, so $v_O = -(1 \text{ V/dec}) \log_{10}[v_I/(0.1 \text{ V})]$. V_o and I_i are calibrated via R_2 and R_r .

If the input reference current I_i is allowed to vary, the log amp is called a *log ratio amplifier* and finds application in wide-dynamic-range ratiometric measurements where the unknown signal is measured against a reference signal that is itself variable. Typical examples are absorbance measurements in medicine and pollution control, where light transmitted through a specimen is measured against incident light, and the result must be independent of incident light intensity. This application is illustrated

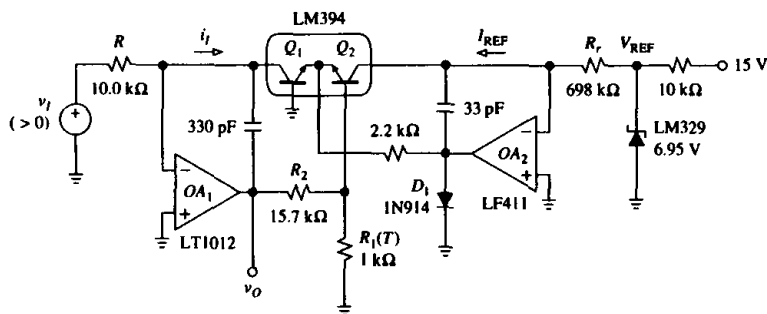


FIGURE 13.4
Logarithmic amplifier.

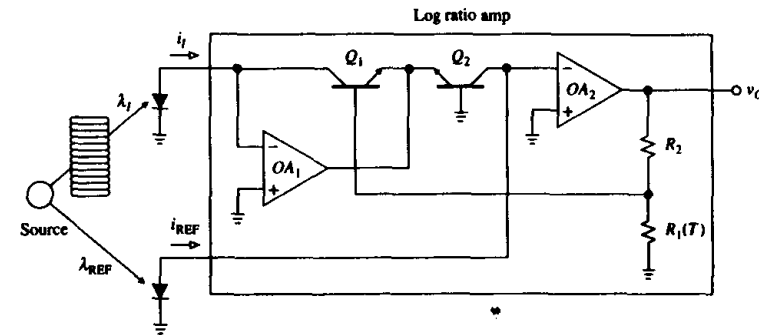


FIGURE 13.5
Log ratio amplifier for absorbance measurements.

in Fig. 13.5, where frequency compensation and reverse-bias protection have been omitted for simplicity. The transmitted light λ_I and the incident light λ_{REF} are converted to the proportional currents i_I and i_{REF} by a pair of matched photodiodes operating in the photovoltaic mode. Then, the circuit computes the log ratio $v_O = V_o \log_{10}(i_I/i_{REF}) = V_o \log_{10}(\lambda_I/\lambda_{REF})$, where V_o is given by Eq. (13.12).

Figure 13.6 shows how the log amp can be rearranged to implement an exponential amp. It is left as an exercise for the reader (see Problem 13.4) to prove that the circuit gives

$$i_O = I_o 10^{v_I/V_i} \quad (13.13)$$

$$I_o = \frac{V_{REF}}{R_r} \times \frac{I_{s2}}{I_{s1}} \quad V_i = -2.303 \frac{R_1(T) + R_2}{R_1(T)} V_T \quad (13.14)$$

With the given component values, $I_o = 0.1 \text{ mA}$ and $V_i = -1 \text{ V/dec}$. It is important that the collector of Q_2 be returned to a 0-V node, such as the virtual-ground node of the I - V converter OA_2 , in order to nullify the collector-base leakage current of Q_2 . Otherwise, this current may degrade log conformity at the low end of the range.

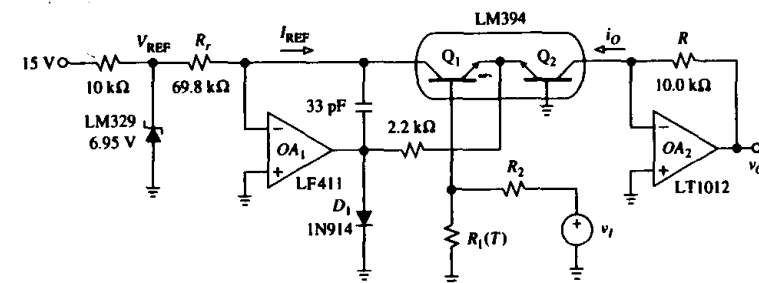


FIGURE 13.6
Antilog amplifier.

Log, log-ratio, and antilog amplifiers are available in IC form from various manufacturers (Analog Devices, Burr-Brown, Harris). These devices usually work over a six-decade current range (1 nA to 1 mA) and a four-decade voltage range (1 mV to 10 V).

True rms-to-dc Converters

The logarithmic characteristics of BJTs are also exploited to perform a variety of slide-rule-like analog computations. A popular example is *true rms-to-dc conversion*, defined as

$$V_{rms} = \left(\frac{1}{T} \int_0^T v^2(t) dt \right)^{1/2} \quad (13.15)$$

V_{rms} gives a measure of the energy content of $v(t)$, so it provides the basis for accurate and consistent measurements, especially in the case of ill-defined waveforms, such as noise (electronic noise, switch contact noise, acoustical noise), mechanical transducer outputs (stress, vibration, shock, bearing noise), SCR waveforms, low-repetition-rate pulse trains, and other waveforms carrying information on the average energy generated, transmitted, or dissipated.

Equation (13.15) can be mechanized by performing the operations of squaring, averaging, and square rooting. Referred to as *explicit rms computation*, this scheme places severe demands on the dynamic output range of the squarer, which must be twice as wide as the input range. This drawback is overcome by *implicit rms computation*, in which the gain of the squarer is made inversely proportional to V_{rms} to make the output dynamic range comparable to the input range.

A common implementation of this principle is shown in Fig. 13.7, where frequency compensation and reverse-bias protection have been omitted for simplicity.

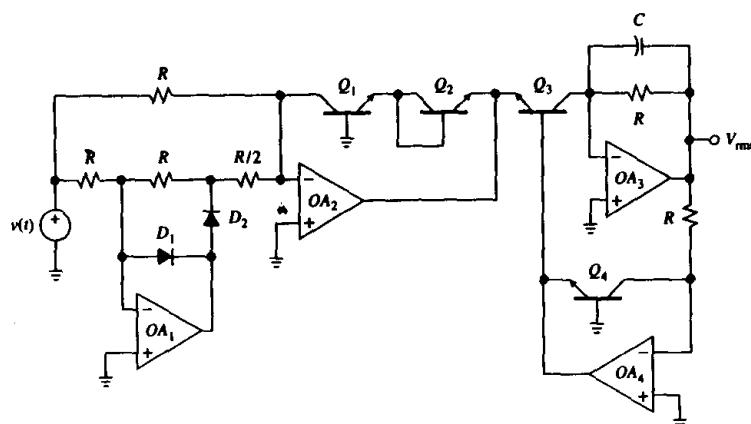


FIGURE 13.7
True rms converter.

OA_1 and the associated circuitry convert $v(t)$ to a full-wave rectified current $i_{C1} = |v|/R$ flowing into Q_1 . By KVL, $v_{BE3} + v_{BE4} = v_{BE1} + v_{BE2}$, or $V_T \ln[(i_{C3}/I_{s3}) \times (i_{C4}/I_{s4})] = V_T \ln[(i_{C1}/I_{s1}) \times (i_{C2}/I_{s2})]$. Assuming pairwise matched BJTs and ignoring base currents so that $i_{C2} = i_{C1}$, we get

$$i_{C3} = \frac{i_{C1}^2}{i_{C4}}$$

Substituting $i_{C1}^2 = v^2/R^2$ and $i_{C4} = V_{rms}/R$ gives

$$i_{C3} = \frac{v^2}{RV_{rms}}$$

indicating that the scale factor of the squaring function is controlled by V_{rms} , as expected of implicit computation.

OA_3 forms a low-pass filter with cutoff frequency $f_0 = 1/2\pi RC$. For signal frequencies sufficiently higher than f_0 , OA_3 will provide the running average of i_{C3} as $V_{rms} \cong \overline{Ri_{C3}} = v^2/V_{rms}$. Making the approximation $\overline{V_{rms}} \cong V_{rms}$, we can write $V_{rms}^2 = v^2$, or

$$V_{rms} = (v^2)^{1/2} \quad (13.16)$$

As a consequence of the approximations made, V_{rms} of Eq. (13.16) will differ from the ideal V_{rms} of Eq. (13.15) by an average (or dc) error as well as an ac (or ripple) error. Both errors can be kept below a specified limit by using a suitably large capacitance.⁴ However, too large a capacitance will increase the response time of the circuit, so a compromise must be reached. An effective way of reducing ripple without unduly lengthening the response is to use a *post filter*, such as a low-pass KRC type.

The structure of Fig. 13.7 (or improved variations thereof) is available in IC form from various manufacturers. Consult the literature⁴ for useful application tips.

13.2 ANALOG MULTIPLIERS

A multiplier produces an output v_O proportional to the product of two inputs v_X and v_Y ,

$$v_O = kv_X v_Y \quad (13.17)$$

where k is a scale factor, usually $1/10 \text{ V}^{-1}$. A multiplier that accepts inputs of either polarity and preserves the correct polarity relationship at the output is referred to as a *four-quadrant multiplier*. Both the input and output ranges are usually from -10 V to $+10 \text{ V}$. By contrast, a *two-quadrant multiplier* requires that one of its inputs be unipolar, and a *one-quadrant multiplier* requires that both inputs be unipolar.

Multiplier performance is specified in terms of *accuracy* and *nonlinearity*. Accuracy represents the maximum deviation of the actual output from the ideal value predicted by Eq. (13.17); this deviation is also referred to as the *total error*. Nonlinearity, also referred to as *linearity error*, represents the maximum output deviation from the best-fit straight line for the case where one input is varied from end to

end while the other is kept fixed, usually at +10 V or -10 V. Both accuracy and nonlinearity are expressed as a percentage of the full-scale output.

Multiplier dynamics are specified in terms of the *small-signal bandwidth*, representing the frequency where the output is 3 dB below its low-frequency value, and the *1% absolute-error bandwidth*, representing the frequency where the output magnitude starts to deviate from its low-frequency value by 1%.

Variable-Transconductance Multipliers

Monolithic four-quadrant multipliers utilize the *variable-transconductance principle*⁵ to achieve errors of fractions of 1% over small-signal bandwidths extending well into the megahertz range. This principle is illustrated in Fig. 13.8a. The block uses the differential pair Q_3 - Q_4 to provide variable transconductance, and the diode-connected pair Q_1 - Q_2 to provide the proper base drive for the former. The following analysis assumes matched BJTs and negligible base currents.

By KVL, $v_{BE1} + v_{BE4} - v_{BE3} - v_{BE2} = 0$, or $v_{BE3} - v_{BE4} = v_{BE1} - v_{BE2}$. Using the logarithmic v - i characteristics of the BJTs, this can be expressed as $V_T \ln(i_3/i_4) = V_T \ln(i_1/i_2)$, or

$$\frac{i_3}{i_4} = \frac{i_1}{i_2}$$

Rewriting as $(i_3 - i_4)/(i_3 + i_4) = (i_1 - i_2)/(i_1 + i_2)$ gives

$$i_3 - i_4 = \frac{(i_1 - i_2) \times (i_3 + i_4)}{i_1 + i_2} \quad (13.18)$$

indicating the circuit's ability to multiply the current difference $(i_1 - i_2)$ by the total emitter current $(i_3 + i_4)$.

To be of practical use, the circuit requires two V - I converters to synthesize the terms $(i_1 - i_2)$ and $(i_3 + i_4)$ from the input voltages v_X and v_Y , and an I - V converter to convert $(i_3 - i_4)$ to the output voltage v_O . Moreover, provisions must be made to

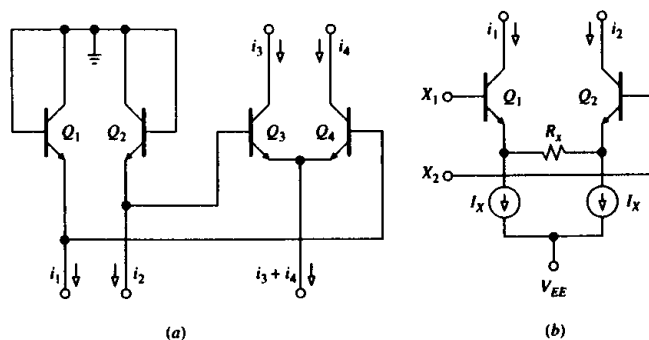


FIGURE 13.8
Linearized transconductance block, and differential V - I converter.

ensure four-quadrant operation; as is, the circuit is only two-quadrant because the current $(i_3 + i_4)$ must always flow out of the emitters.

Figure 13.8b shows the circuit used to provide V - I conversion. By KCL, $i_1 = I_x + i_{R_x}$ and $i_2 = I_x - i_{R_x}$, where $i_{R_x} = (v_{E1} - v_{E2})/R_x$ is the current through R_x , assumed to flow from left to right. Consequently,

$$i_1 - i_2 = 2 \frac{v_{E1} - v_{E2}}{R_x}$$

By KVL, $v_{E1} - v_{E2} = (v_{X1} - v_{BE1}) - (v_{X2} - v_{BE2}) = (v_{X1} - v_{X2}) - (v_{BE1} - v_{BE2})$, or

$$v_{E1} - v_{E2} = v_{X1} - v_{X2} - V_T \ln \frac{i_1}{i_2}$$

Combining the two equations gives

$$i_1 - i_2 = \frac{2}{R_x} (v_{X1} - v_{X2}) - \frac{2V_T}{R_x} \ln \frac{i_1}{i_2} \quad (13.19)$$

In a well-designed multiplier the last term is on the order of 1% of the other two, so we can ignore it and approximate

$$i_1 - i_2 = \frac{2}{R_x} (v_{X1} - v_{X2}) \quad (13.20)$$

indicating the circuit's ability to provide differential V - I conversion.

Figure 13.9 shows the complete multiplier. Four-quadrant operation is achieved by using two transconductance pairs with the bases driven in antiphase and the

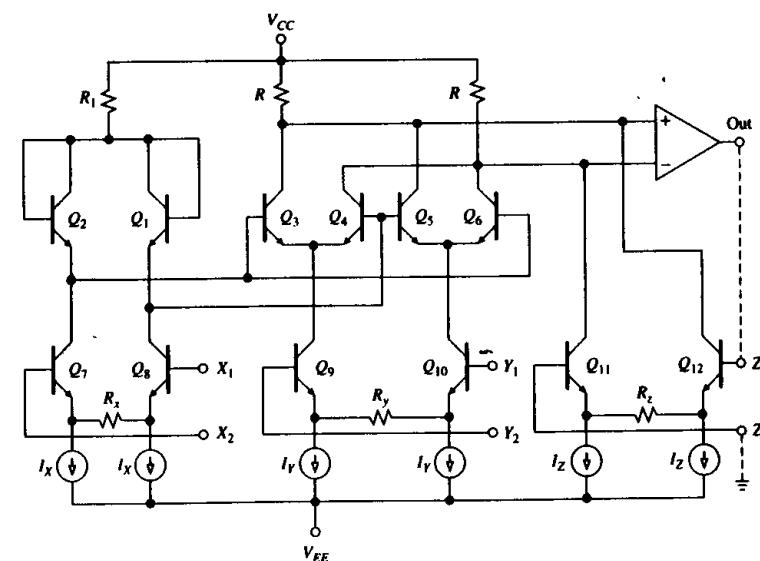


FIGURE 13.9
Four-quadrant analog multiplier.

emitters driven by a second V - I converter. Substituting Eq. (13.20) into Eq. (13.18) and using the identities $i_1 + i_2 = 2I_X$ and $i_3 + i_4 = i_9$, we obtain

$$i_3 - i_4 = \frac{v_{X_1} - v_{X_2}}{R_X I_X} i_9$$

Likewise, using the identity $i_5 + i_6 = i_{10}$, we obtain

$$i_6 - i_5 = \frac{v_{X_1} - v_{X_2}}{R_X I_X} i_{10}$$

Subtracting the first equation from the second pairwise and using $i_{10} - i_9 = (2/R_Y)(v_{Y_1} - v_{Y_2})$, we obtain

$$(i_4 + i_6) - (i_3 + i_5) = \frac{(v_{X_1} - v_{X_2})(v_{Y_1} - v_{Y_2})}{R_X R_Y I_X / 2}$$

The output I - V converter is made up of the op amp and a third V - I converter in its feedback path, namely, Q_{11} - Q_{12} . By KVL, the voltages at the inverting and noninverting inputs are $v_N = V_{CC} - R(i_4 + i_6 + i_{11})$ and $v_P = V_{CC} - R(i_3 + i_5 + i_{12})$. The op amp will provide Q_{12} with whatever drive it takes to make $v_N = v_P$, or $i_4 + i_6 + i_{11} = i_3 + i_5 + i_{12}$, that is,

$$(i_4 + i_6) - (i_3 + i_5) = i_{12} - i_{11} = \frac{2}{R_Z}(v_{Z_1} - v_{Z_2})$$

Combining the last two equations, we finally obtain

$$v_{Z_1} - v_{Z_2} = k(v_{X_1} - v_{X_2})(v_{Y_1} - v_{Y_2}) \quad (13.21)$$

$$k = \frac{R_Z}{R_X R_Y I_X} \quad (13.22)$$

Most multipliers are designed for $k = 1/(10 \text{ V})$. Letting $v_O = v_{Z_1} - v_{Z_2}$, $v_X = v_{X_1} - v_{X_2}$, and $v_Y = v_{Y_1} - v_{Y_2}$ gives Eq. (13.17).

One of the main causes of linearity error is the logarithmic term of Eq. (13.19). This error is, to a first approximation, compensated for by introducing an equal but opposite nonlinearity term via the V - I converter Q_{11} - Q_{12} inside the feedback path. The architecture of Fig. 13.9 forms the basis of a variety of monolithic multipliers. Two of the earliest and most popular examples are the AD534 (Analog Devices) and MPY100 (Burr-Brown). The AD534L version has a maximum pretrimmed total error of 0.25%, a maximum linearity error of 0.12%, a typical small-signal bandwidth of 1 MHz, and a typical 1% amplitude error bandwidth of 50 kHz.

Multiplier Applications

Analog multipliers find application in signal modulation/demodulation, analog computation, curve fitting, transducer linearization, CRT distortion compensation, and a variety of voltage-controlled functions.^{1,6}

Figure 13.10 shows the basic connection for signal multiplication, or $v_O = v_1 v_2 / 10$. As such, it forms the basis of amplitude modulation and voltage-controlled amplification. When either input is zero, v_O should also be zero, regardless of the other input. In practice, because of slight component mismatches, a small fraction

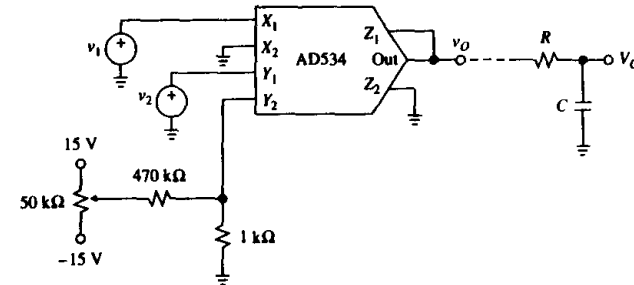


FIGURE 13.10
Basic multiplier connection for $v_O = v_1 v_2 / 10$. If followed by a low-pass filter, it can be used for phase detection.

of the nonzero input will feed through to the output, causing an error. In critical applications such as suppressed-carrier modulation, this error can be minimized by applying an external trim voltage (± 30 -mV range required) to the X_2 or the Y_2 input.

Of particular interest is the case in which the inputs are ac signals, or $v_1 = V_1 \cos(\omega_1 t + \theta_1)$ and $v_2 = V_2 \cos(\omega_2 t + \theta_2)$, for then their product is, by a well-known trigonometric identity

$$v_O = \frac{V_1 V_2}{20} \{ \cos[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)] + \cos[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)] \}$$

indicating that v_O consists of two components, with frequencies equal to the sum and the difference of the input frequencies. If the input frequencies are the same and the high-frequency component is suppressed with a low-pass filter, as shown, then we get

$$v_O = \frac{V_1 V_2}{20} \cos(\theta_1 - \theta_2) \quad (13.23)$$

In this capacity, the circuit can be used in ac power measurements or as a phase detector in phase-locked-loop circuits.

Figure 13.11 shows how a multiplier can be configured for two other popular functions, namely, *analog division* and *square-root extraction*. In Fig. 13.11a we

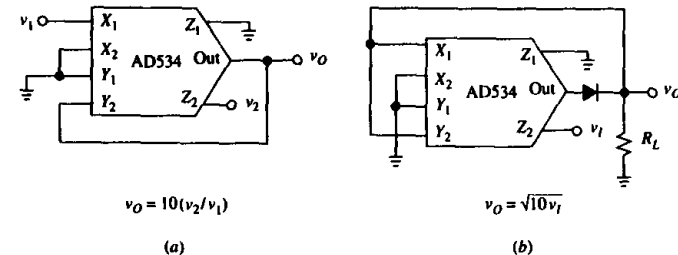


FIGURE 13.11
Analog divider and square-rooter.

have, by Eq. (13.21), $0 - v_2 = (v_1 - 0)(0 - v_O)/10$, or $v_O = 10(v_2/v_1)$. To maximize the denominator range, return the X_2 input to a trimmable voltage (± 3 -mV range required).

In Fig. 13.11b we have $0 - v_1 = (v_O - 0)(0 - v_O)/10$, or $v_O = \sqrt{10v_1}$. The function of the diode is to prevent a latching condition, which could arise in the event of the input inadvertently changing polarity. Additional applications are discussed in the end-of-chapter problems.

13.3 OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

An operational transconductance amplifier (OTA) is a voltage-input, current-output amplifier. Its circuit model is shown in Fig. 13.12a. To avoid loading effects both at the input and at the output, an OTA should have $z_d = z_o = \infty$. The ideal OTA, whose circuit symbol is shown in Fig. 13.12b, gives $i_O = g_m v_D$, or

$$i_O = g_m(v_P - v_N) \quad (13.24)$$

where g_m is the *unloaded transconductance gain*, in amperes per volt.

In its simplest form, an OTA consists of a differential transistor pair with a current-mirror load.⁷ We have encountered this configuration when studying op amp input stages, in Chapter 5. In the bipolar example of Fig. 5.1 the OTA consists of the Q_1 - Q_2 pair and the Q_3 - Q_4 mirror; in the MOS example of Fig. 5.8 it consists of the M_1 - M_2 pair and the M_3 - M_4 mirror.

Besides serving as building blocks for other amplifiers, OTAs find application in their own right. Since it can be realized with just one stage and it operates on the principle of processing currents rather than voltages, the OTA is an inherently fast device.⁸ Moreover, g_m can be varied by changing the bias current of the differential transistor pair, making OTAs suited to electronically programmable functions.

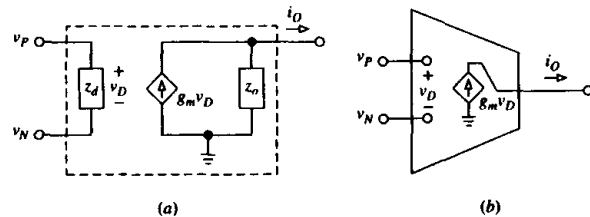


FIGURE 13.12
Operational transconductance amplifier: (a) equivalent circuit and (b) ideal model.

g_m -C Filters

A popular OTA application is the realization of fully integrated continuous-time filters, where OTAs have emerged as viable alternatives to traditional op amps.⁷⁻⁹ OTA-based filters are referred to as g_m -C filters because they use OTAs and capacitors, but no resistors and no inductors. A popular g_m -C filter example is shown in Fig. 13.13a. Its analysis proceeds as follows.

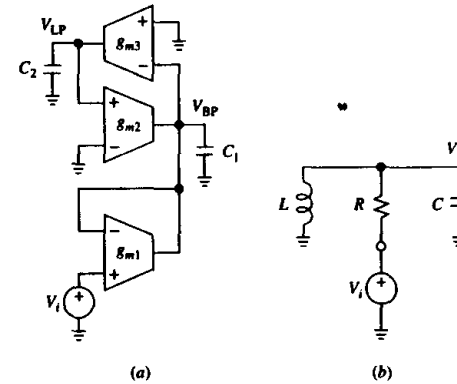


FIGURE 13.13
Second-order g_m -C filter and its RLC equivalent.

By Eq. (13.24), $I_1 = g_{m1}(V_i - V_{BP})$, $I_2 = g_{m2}V_{LP}$, and $I_3 = -g_{m3}V_{BP}$. By Ohm's law, $V_{LP} = (1/sC_2)I_3$ and $V_{BP} = (1/sC_1)(I_1 + I_2)$. Combining, we get

$$\frac{V_{BP}}{V_i} = \frac{sC_2g_{m1}/g_{m2}g_{m3}}{s^2C_1C_2/g_{m2}g_{m3} + sC_2g_{m1}/g_{m2}g_{m3} + 1} \quad (13.25)$$

It is readily seen that this transfer function is the same as that of the RLC equivalent of Fig. 13.13b, provided $C = C_1$, $R = 1/g_{m1}$, and $L = C_2/g_{m2}g_{m3}$. Evidently, g_{m1} simulates a resistance, whereas the combination g_{m2} - g_{m3} - C_2 simulates an inductance. Moreover, the circuit provides V_{BP} and V_{LP} simultaneously, a feature not available in its RLC counterpart. What is even more important is that we can automatically tune f_0 by varying g_{m2} and g_{m3} , and tune Q by varying g_{m1} .

EXAMPLE 13.2. (a) In the filter of Fig. 13.13a find g_{m1} and $g_{m2} = g_{m3}$ for $\omega_0 = 10^5$ rad/s and $Q = 5$ with $C_1 = C_2 = 100$ pF. (b) What are the values of the simulated resistance and the simulated inductance? (c) The sensitivities of the filter?

Solution.

- (a) By inspection, $\omega_0 = \sqrt{g_{m2}g_{m3}/C_1C_2}$ and $Q = \sqrt{C_1/C_2} \times \sqrt{g_{m2}g_{m3}/g_{m1}}$. Substituting the given data, we get $g_{m2} = g_{m3} = 10 \mu\text{A/V}$ and $g_{m1} = 2 \mu\text{A/V}$.
(b) $R = 500 \text{ k}\Omega$, and $L = 1 \text{ H}$.
(c) The sensitivity of Q with respect to g_{m1} is -1 ; all other sensitivities are either $\frac{1}{2}$ or $-\frac{1}{2}$, which are fairly low.

Off-the-Shelf OTAs

Figure 13.14 shows a popular OTA available as an off-the-shelf IC. Its heart is the linearized transconductance multiplier made up of D_1 - D_2 and Q_3 - Q_4 . The remaining blocks, each consisting of a BJT pair and a diode, are high-output-impedance current mirrors of the Wilson type. Denoting the collector current of transistor Q_k as i_k and ignoring base currents, we can describe circuit operation as follows.

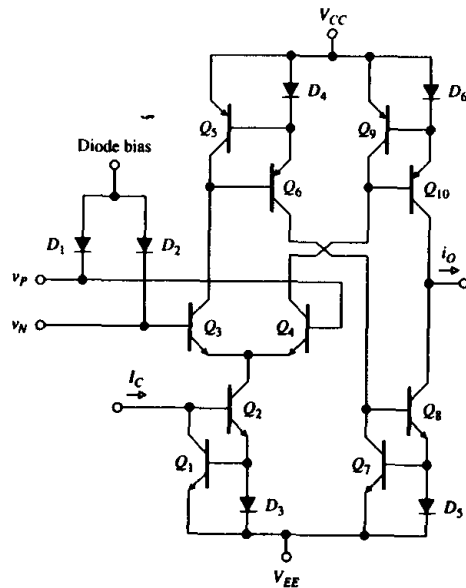


FIGURE 13.14
Bipolar OTA.

The mirror Q_1 - D_3 - Q_2 accepts the external control current I_C and duplicates it at the emitters of the Q_3 - Q_4 pair to give

$$i_3 + i_4 = I_C$$

The mirror Q_5 - D_4 - Q_6 duplicates i_3 to yield $i_6 = i_3$, and the mirror Q_7 - D_5 - Q_8 duplicates i_6 to yield $i_8 = i_6$, so $i_8 = i_3$. Likewise, the mirror Q_9 - D_6 - Q_{10} duplicates i_4 to yield $i_{10} = i_4$. Consequently, KCL gives $i_O = i_{10} - i_8$, or

$$i_O = i_4 - i_3$$

Retracing the reasoning of Section 5.1, we can write

$$i_O = I_C \tanh \frac{v_P - v_N}{2V_T}$$

where V_T is the thermal voltage. As we know, this is a nonlinear characteristic,

which, for $|v_P - v_N| \ll 2V_T$, can be approximated as

$$i_O = \frac{I_C}{2V_T}(v_P - v_N) \quad (13.26)$$

indicating that $g_m = I_C/2V_T$.

To accommodate applications requiring a wider linear range at the input, the linearizing diode network of Fig. 13.15 is used. Applying Eq. (13.18), we can write

$$i_O = i_4 - i_3 = \frac{i_2 - i_1}{i_2 + i_1} I_C$$

With $v_1 = v_2$, the bias current provided by R_3 splits evenly between D_1 and D_2 , giving $i_2 - i_1 = 0$. Moreover, we can write $i_2 + i_1 = I_{R_3} = (V_{CC} - V_D)/(R_3 + (R_1 \parallel R_2)/2) \cong 1.08 \text{ mA}$, where we have assumed $V_D \cong 0.7 \text{ V}$. Making $v_1 \neq v_2$ will unbalance the two halves of the input network and divert a greater portion of I_{R_3} to either D_2 or D_1 , depending on the imbalance direction. The voltage variation at the anodes is designed to be negligible compared to V_{CC} over an input range of more than 10 V, so $i_2 + i_1$ can be assumed to be constant. Using simple KCL reasoning, we find that I_{R_3} is completely diverted from one diode to the other when $|v_1 - v_2| \cong (R_1 + R_2)I_{R_3} \cong 11.3 \text{ V}$. Consequently, for $|v_1 - v_2| \leq 11.3 \text{ V}$ we have $i_2 - i_1 = (v_1 - v_2)/(11.3 \text{ k}\Omega)$. Substituting into the above equation, along with $i_2 + i_1 \cong 1.08 \text{ mA}$, we obtain

$$i_O = g_m(v_1 - v_2) \quad (13.27a)$$

$$g_m \cong \frac{I_C}{12.2 \text{ V}} \quad (13.27b)$$

The scale factor of approximately $1/(12.2 \text{ V})$ allows for operation over the range $-10 \text{ V} < (v_1 - v_2) < 10 \text{ V}$ with negligible linearity error and no fear of saturation. Popular OTAs of the type shown are the LM13600 (National Semiconductor) and NE5517 (Signetics). The CA3080 (Harris) comes without the input diodes.

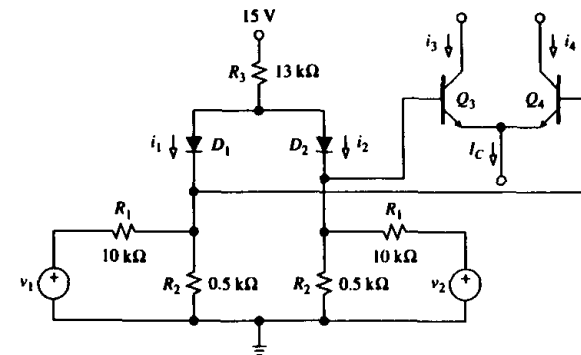


FIGURE 13.15
Input linearization network.

Applications with Off-the-Shelf OTAs

Though OTA data sheets propose quite a variety of useful applications, we shall examine a few representative ones, namely, voltage-controlled amplifiers, filters, and oscillators (VCAs, VCFs, and VCOs).

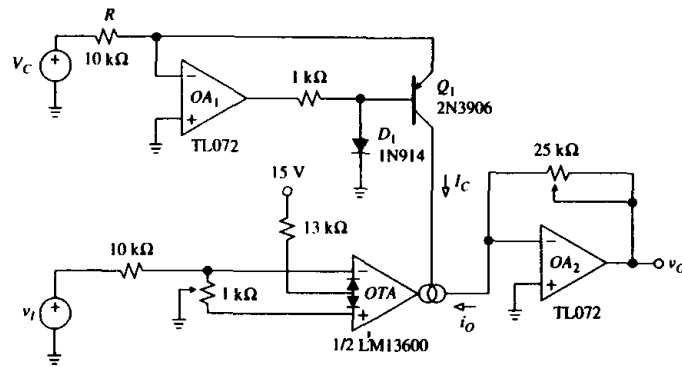


FIGURE 13.16
Voltage-controlled amplifier with linear control.

Figure 13.16 shows a basic VCA (note the alternative symbol for the OTA). Here OA_1 and Q_1 form a $V-I$ converter to provide $I_C = V_C/R$, where we are assuming the base current of Q_1 to be negligible. OA_2 converts i_O to a voltage v_O , and since i_O is proportional to the product $I_C \times v_I$, the final result is $v_O = A v_I$,

$$A = k V_C \quad (13.28)$$

where k is a suitable proportionality constant, in V^{-1} . The 1-k Ω pot is used for offset nulling, and the 25-k Ω pot for the calibration of k . By Eq. (13.27), adjusting the 25-k Ω pot near 12.2 k Ω yields $k = 1/(10 V)$, indicating that varying V_C from 0 to 10 V will change A from 0 to 1 V/V. The circuit is calibrated as follows: (a) with $v_I = 0$, sweep V_C from 0 to 10 V, and adjust the 1-k Ω pot for the minimum deviation of v_O from 0 V; (b) with $V_C = 10 V$, adjust the 25-k Ω pot so that $v_O = 10 V$ for $v_I = 10 V$.

The circuit of Fig. 13.16 provides linear gain control. Audio applications often call for exponential control, or

$$A = A_0 b^{k V_C} \quad (13.29)$$

where b is usually either 10 or 2, k is a proportionality constant in decades or octaves per volt, and A_0 is the gain for $V_C = 0$. Exponential control is readily achieved by generating I_C with an antilog converter, as shown in Fig. 13.17. Since I_C must be sourced to the OTA, the BJTs must be of the pnp type. With $V_C = 0$, the circuit gives $I_C = 1 mA$; increasing V_C decreases I_C exponentially with a sensitivity of k dec/V or k oct/V, with k being set by R_2 .

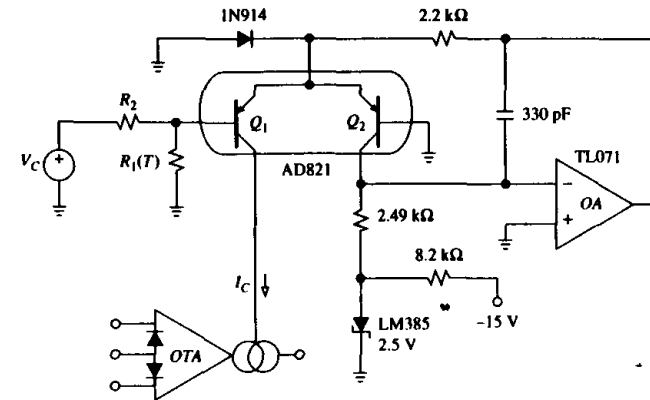


FIGURE 13.17
OTA with exponential control.

OTA-based VCFs and VCOs rely on the integration of the OTA's output current using a capacitor. The example of Fig. 13.18 uses also an op amp to provide low output impedance. Writing $V_o = (-1/sC) I_o = (-1/sC) \times [I_C/(12.2 V)] \times (V_2 - V_1)$, and letting $s = j2\pi f$, we obtain

$$V_o = \frac{1}{jf/f_0} (V_1 - V_2) \quad f_0 = \frac{I_C}{2\pi(12.2 V)C} \quad (13.30)$$

The circuit integrates the difference $V_1 - V_2$ with a programmable unity-gain frequency f_0 . For instance, varying I_C from 1 μA to 1 mA with $C = 652$ pF will sweep f_0 over the entire audio range, from 20 Hz to 20 kHz. I_C can be generated either with a linear $V-I$ converter, as in Fig. 13.16, or with an exponential converter, as in Fig. 13.17.

The circuit of Fig. 13.19 uses two OTA-based integrators to implement a state-variable topology of the type of Fig. 4.37. The output current of the $V-I$ converter, which can be controlled either linearly or exponentially, is split between the two OTAs by the suitably biased AD821 matched BJT pair.

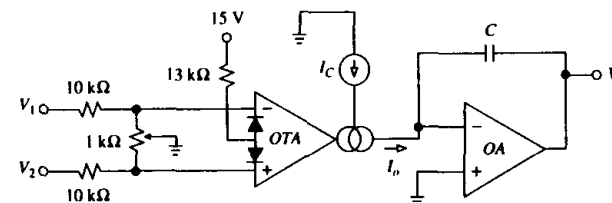


FIGURE 13.18
Current-controlled integrator.

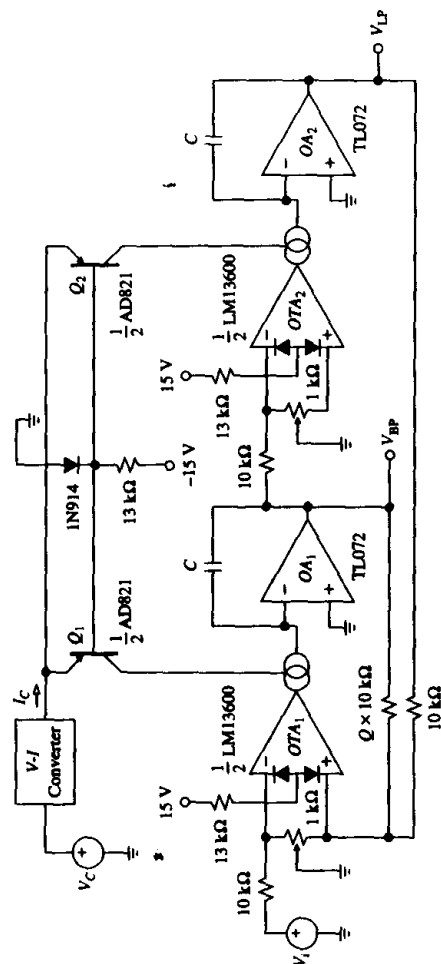


FIGURE 13.19
Voltage-controlled state-variable filter.

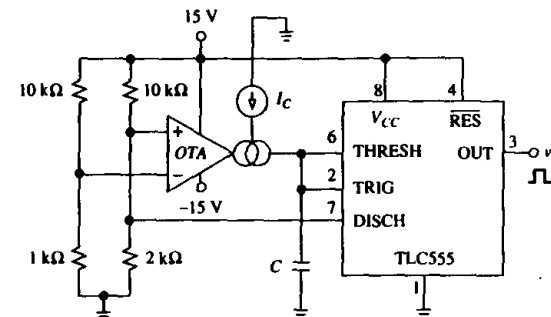


FIGURE 13.20
Current-controlled relaxation oscillator.

Applying Eq. (13.30), we get $V_{BP} = (V_i - V_{BP}/Q - V_{LP})/(jf/f_0)$ and $V_{LP} = V_{BP}/(jf/f_0)$. Combining, we obtain

$$\frac{V_{BP}}{V_i} = QH_{BP} \quad \frac{V_{LP}}{V_i} = H_{LP} \quad (13.31)$$

where H_{BP} and H_{LP} are the standard second-order band-pass and low-pass functions defined in Section 3.4, and

$$f_0 = \frac{I_C}{4\pi(12.2 \text{ V})C}$$

If a resonance gain of unity is desired, then increase the 10-kΩ input resistance by a factor of Q . To reduce Q -enhancement effects, follow the directions of Section 6.5 and use a small phase-lead capacitor in parallel with the 10-kΩ interstage resistance.

In the circuit of Fig. 13.20 the OTA is used to source/sink a current of value I_C , and thus charge/discharge C at a programmable rate. The resulting triangle waveform alternates between 5 V and 10 V, the thresholds of the high-input-impedance CMOS timer. The frequency of oscillation is (see Problem 13.16),

$$f_0 = \frac{I_C}{10C} \quad (13.32)$$

As usual, I_C can be controlled either linearly or exponentially. If the triangular wave is used, a buffer amplifier may be required.

13.4 PHASE-LOCKED LOOPS

A *phase-locked loop* (PLL) is a frequency-selective circuit designed to synchronize with an incoming signal and maintain synchronization in spite of noise or variations in the incoming signal frequency. As depicted in Fig. 13.21, the basic PLL system comprises a *phase detector*, a *loop filter*, and a *voltage-controlled oscillator* (VCO).

The phase detector compares the phase θ_I of the incoming signal v_I against the phase θ_O of the VCO output v_O , and develops a voltage v_D proportional to the difference $\theta_I - \theta_O$. This voltage is sent through a low-pass filter to suppress

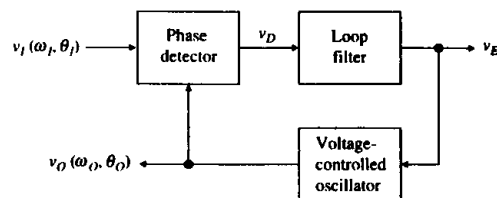


FIGURE 13.21
Basic phase-locked loop.

high-frequency ripple and noise, and the result, called the *error voltage* v_E , is applied to the control input of the VCO to adjust its frequency ω_O .

The VCO is designed so that with $v_E = 0$ it is oscillating at some initial frequency ω_0 called the *free-running frequency*, so its characteristic is

$$\omega_O(t) = \omega_0 + K_O v_E(t) \quad (13.33)$$

where K_O is the *sensitivity* of the VCO, in radians-per-second per volt. If a periodic input is applied to the PLL with frequency ω_I sufficiently close to the free-running frequency ω_0 , an error voltage v_E will develop, which will adjust ω_O until v_E becomes synchronized with v_I , that is, until *for every input cycle there is one, and only one, VCO cycle*. At this point the PLL is said to be *locked* on the incoming signal, and it gives $\omega_O = \omega_I$ exactly.

Should ω_I change, the phase shift between v_O and v_I will start to increase, changing v_D and, hence, the control voltage v_E . This change in v_E is designed to adjust the VCO until ω_O is brought back to the same value as ω_I . This self-adjusting ability by the feedback loop allows the PLL, once locked, to track input frequency changes. Since a change in ω_I is ultimately reflected by a change in v_E , we use v_E as the output of the PLL whenever we wish to detect changes in ω_I , as in FM and FSK demodulation.

A PLL can be designed to lock on the incoming signal in spite of noise that might afflict such a signal. A noisy input will generally cause the phase-detector output v_D to jitter around some average value. However, if the filter cutoff frequency is low enough to suppress this jitter, v_E will emerge as a clean signal, in turn resulting in a stable VCO frequency and phase. We thus use ω_O as the output of the PLL whenever we wish to recover a signal buried in noise, and also in frequency-related applications such as frequency synthesis and synchronization.

Lock and Capture

To develop a concrete understanding of PLL operation, consider the case of phase detection being accomplished with a balanced mixer of the type discussed in Section 13.2. As we know, the mixer output contains the sum and difference frequencies $\omega_I \pm \omega_O$. When the loop is locked, the sum is twice ω_I and the difference is zero, or dc. The low-pass filter suppresses the sum but passes the dc component, which thus keeps the loop in lock.

If the loop is not locked, and if the difference frequency falls above the cutoff frequency of the filter, it will be suppressed along with the sum frequency, leaving the loop unlocked and oscillating at its free-running frequency. However, if ω_O is sufficiently close to ω_I to make the difference frequency approach the filter band edge, part of this component is passed, tending to drive ω_O toward ω_I . As the difference $\omega_O - \omega_I$ is reduced, more error signal is transmitted to the VCO, resulting in a constructive effect that ultimately brings the PLL in lock.

The *capture range* is the frequency range $\pm \Delta\omega_C$, centered about ω_0 , over which the loop can acquire lock. This range is affected by the filter characteristics, and gives an indication of how close ω_I must be to ω_0 to acquire lock. The *lock range* is the frequency range $\pm \Delta\omega_L$, also centered about ω_0 , over which the loop can track the input once lock has been established. The lock range is affected by the operating range of the phase detector and the VCO. The capture process is a complex phenomenon, and the capture range is never greater than the lock range.

The time it takes for a PLL to capture the incoming signal is called the *capture time* or *pull-in time*. This time depends on the initial frequency and phase differences between v_I and v_O , as well as the filter and other loop characteristics. In general, it can be said that reducing the filter bandwidth has the following effects: (a) it slows down the capture process, (b) it increases the pull-in time, (c) it decreases the capture range, and (d) it increases the interference-rejection capabilities of the loop.

The PLL in the Locked Condition

When in the locked condition, a PLL can be modeled¹⁰⁻¹² as in Fig. 13.22. This diagram is similar to that of Fig. 13.21, except that we are now working with Laplace transforms of *signal changes* (symbolized by lowercase letters with lowercase subscripts) about some operating point, and *operations* on these changes, both of which are generally functions of the complex frequency s . The phase detector develops the voltage change

$$v_d(s) = K_d \theta_d(s) \quad (13.34a)$$

$$\theta_d(s) = \theta_i(s) - \theta_o(s) \quad (13.34b)$$

where K_d is the phase-detector *sensitivity*, in volts per radian. This voltage is sent through the loop filter, whose transfer function is denoted as $F(s)$, and possibly

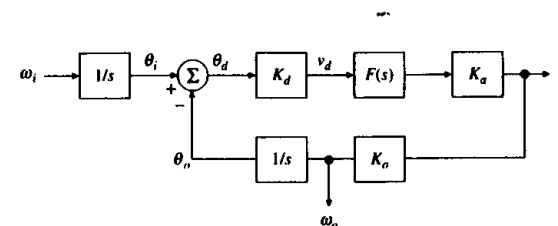


FIGURE 13.22
Block diagram of the basic PLL system in the locked condition.

an amplifier with gain K_a , in volts per volt, to produce the error-voltage variation $v_e(s)$. This, in turn, is converted to the frequency variation $\omega_o(s) = K_o v_e(s)$, by Eq. (13.33).

Since the phase detector processes phase, we need a means for converting from frequency to phase. Considering that frequency represents the rate of change of phase with time, or $\omega = d\theta(t)/dt$, we have

$$\theta(t) = \theta(0) + \int_0^t \omega(\xi) d\xi \quad (13.35)$$

indicating that frequency-to-phase conversion is inherently an operation of integration. Exploiting the well-known Laplace transform property that integration in the time domain corresponds to division by s in the frequency domain, we use the $1/s$ blocks shown.

If we were to open the loop at the inverting input of the phase comparator, the overall gain experienced by $\theta_i(s)$ in going around the path and emerging as $\theta_o(s)$ is $K_d \times F(s) \times K_a \times K_o \times 1/s$, or

$$T(s) = K_v \frac{F(s)}{s} \quad (13.36)$$

$$K_v = K_d K_a K_o \quad (13.37)$$

where $T(s)$ is the *open-loop gain*, in radians per radian, and K_v is called the *gain factor*, in s^{-1} . With the loop closed, we readily find

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{T(s)}{1 + T(s)} = \frac{K_v F(s)}{s + K_v F(s)} \quad (13.38)$$

Other transfer functions may be of interest, depending on what we consider as input and output. For instance, substituting $\theta_i(s) = \omega_i(s)/s$ and $\theta_o = (K_o/s)v_e(s)$, we readily get

$$\frac{v_e(s)}{\omega_i(s)} = \frac{1}{K_o} H(s) \quad (13.39)$$

which allows us to find the voltage change $v_e(s)$ in response to an input frequency change $\omega_i(s)$, as in FM and FSK demodulation.

Comparing Fig. 13.22 with Fig. 1.21, we observe that a PLL is a negative-feedback system with $x_i = \theta_i$, $x_f = \theta_o$, and $a\beta = T = K_v F(s)/s$, indicating that the open-loop gain T plays also the role of the *loop gain* of the system. Further, even though we are more attuned to frequency, we must recognize that the natural input of a PLL is phase. Since $T \rightarrow \infty$ as $s \rightarrow 0$, the PLL will force θ_o to track θ_i , just as an op amp voltage follower forces v_o to track v_i . In this respect, it pays to view a PLL as a *phase follower*. The fact that it also forces ω_o to track ω_i is a consequence of this phase-follower action, along with the phase-frequency relationship $\omega = d\theta/dt$.

As seen in Chapter 8, the loop gain T affects both the dynamics and the stability of the PLL. In turn, $T(s)$ is strongly influenced by $F(s)$. We make the following observations: (a) The number of poles of $H(s)$ defines the *order* of the loop; (b) the number of $1/s$ terms (or integrations) present within the loop defines the *type* of a

loop. Because of the $1/s$ function associated with the VCO, a PLL is at least Type I, and its order equals the order of the filter plus 1.

First-Order Loop

Consider the instructive case in which there is no loop filter, or $F(s) = 1$. The result is a *first-order loop*, and the above equations simplify, after the substitution $s \rightarrow j\omega$, as

$$T(j\omega) = \frac{1}{j\omega/K_v} \quad (13.40)$$

$$\frac{v_e(j\omega)}{\omega_i(j\omega)} = \frac{1/K_o}{1 + j\omega/K_v} \quad (13.41)$$

Equation (13.40) indicates a *Type I* loop with crossover frequency $\omega_x = K_v$ and phase margin $\phi_m = 90^\circ$. Equation (13.41) indicates that the loop inherently provides a first-order low-pass response with a dc gain of $1/K_o$ V/(rad/s) and a cutoff frequency of K_v rad/s.

If $\omega_i(t)$ is a step change, the resulting change $v_e(t)$ will be an exponential transient governed by the time constant $\tau = 1/K_v$. If $\omega_i(t)$ is varied sinusoidally with a modulating frequency ω_m , $v_e(t)$ will also vary sinusoidally with the same frequency ω_m ; its amplitude is $|v_e| = (1/K_o)|\omega_i|$ at low frequencies, and rolls off with ω_m at the rate of -1 dec/dec past K_v .

EXAMPLE 13.3. A first-order PLL with $K_v = 10^4 s^{-1}$ uses a VCO with a free-running frequency of 10 kHz and a sensitivity of 5 kHz/V. (a) What is the control voltage needed to lock the PLL on a 20-kHz input signal? On a 5-kHz input signal? (b) Find the response $v_e(t)$ if the input frequency is changed stepwise as $f_i = [10 + u(t)]$ kHz, where $u(t) = 0$ for $t < 0$ and $u(t) = 1$ for $t > 0$. (c) Repeat if the input frequency is modulated as $f_i = 10(1 + 0.1 \cos 2\pi f_m t)$ kHz, $f_m = 2.5$ kHz.

Solution.

- (a) By Eq. (13.33), $v_E = (\omega_o - \omega_0)/K_o$, where $\omega_0 = 2\pi 10^4$ rad/s and $K_o = 2\pi \times 5 \times 10^3 = \pi 10^4$ (rad/s)/V. For $\omega_o = 2\pi \times 20 \times 10^3$ rad/s we get $v_E = 2$ V, and for $\omega_o = 2\pi \times 5 \times 10^3$ rad/s we get $v_E = -1$ V.
- (b) The response to a step increase $\omega_i(t) = 2\pi u(t)$ krad/s is an exponential transient with amplitude $|\omega_i(t)|/K_o = 2\pi 10^3/10^4\pi = 0.2$ V, and time constant $1/K_v = 1/10^4 = 100$ μ s, so

$$v_e(t) = 0.2[1 - e^{-t/(100 \mu s)}]u(t) \text{ V}$$

- (c) Now $\omega_i(t) = 2\pi \times 10^4 \times 0.1 \cos 2\pi f_m t = 2\pi 10^3 \cos 2\pi 2500t$ rad/s. Calculating Eq. (13.41) at $j\omega = j\omega_m = j2\pi 2500$ rad/s gives

$$\frac{v_e(j\omega_m)}{\omega_i(j\omega_m)} = \frac{1/10^4\pi}{1 + j2\pi 2500/10^4} = \frac{0.5370}{10^4\pi} \angle -57.52^\circ \text{ V/(rad/s)}$$

Letting $\omega_i(j\omega_m) = 2\pi 10^3 \angle 0^\circ$ rad/s gives $v_e(j\omega_m) = 0.1074 \angle -57.52^\circ$ V, so

$$v_e(t) = 0.1074 \cos(2\pi 2500t - 57.52^\circ) \text{ V}$$

The absence of a loop filter drastically limits the selectivity and noise-suppression capabilities of a PLL, so first-order loops are seldom used in practice.

Second-Order Loops

Most PLLs utilize a one-pole low-pass filter and are thus *second-order loops*. Such a filter provides a flywheel-like function that allows the VCO to smooth over noise and jumps in the input frequency. As seen in Chapter 8, the presence of a second pole within the loop erodes the phase margin, so care must be exercised to avoid instability. Second-order loops are stabilized by introducing also a filter zero to counterbalance the phase lag due to the filter pole.

A popular loop filter is shown in Fig. 13.23a. Called a *passive lag-lead filter*, it provides the transfer function

$$F(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p} \quad (13.42)$$

where $\omega_z = 1/R_2C$ and $\omega_p = 1/(R_1 + R_2)C$. By Eq. (13.36), the loop gain is now

$$T(j\omega) = \frac{1 + j\omega/\omega_z}{(j\omega/K_v)(1 + j\omega/\omega_p)} \quad (13.43)$$

indicating a *second-order, Type I loop*. This gain is plotted in Fig. 13.23b for the case in which ω_z is positioned at the geometric mean of ω_p and K_v , or $\omega_z = \sqrt{\omega_p K_v}$. The crossover frequency is then ω_z itself, and the phase margin is 45° . Also shown for comparison is the loop gain of the first-order loop, or $F(s) = 1$.

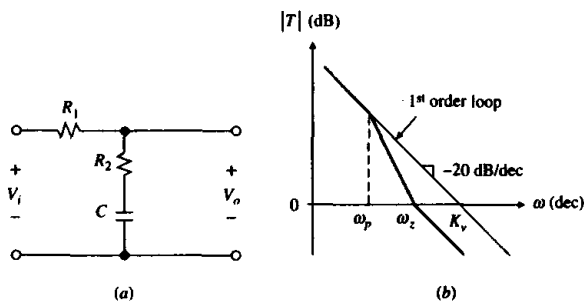


FIGURE 13.23
Passive lag-lead filter, and magnitude plot of the loop gain T .

EXAMPLE 13.4. (a) Given a PLL system with $K_v = 10^4 \text{ s}^{-1}$, specify a passive lag-lead filter for a crossover frequency $\omega_x = 10^3 \text{ rad/s}$ and a phase margin $\phi_m = 45^\circ$. (b) What are the actual values of ω_x and ϕ_m ?

Solution.

- (a) For $\phi_m \cong 45^\circ$ we want $\omega_z = \omega_x = 10^3 \text{ rad/s}$, so $\omega_p = \omega_z^2/K_v = 10^6/10^4 = 100 \text{ rad/s}$. Let $C = 0.1 \mu\text{F}$. Then, $R_2 = 1/\omega_z C = 10 \text{ k}\Omega$, and $R_1 = 1/\omega_p C - R_2 = 90 \text{ k}\Omega$ (use $91 \text{ k}\Omega$).
- (b) Using Eq. (13.43), along with the trial-and-error technique of Example 8.1, we find the actual values $\omega_x = 1.27 \text{ krad/s}$, and $\phi_m = 180^\circ + \angle T(j1.27 \times 10^3) = 56^\circ$.

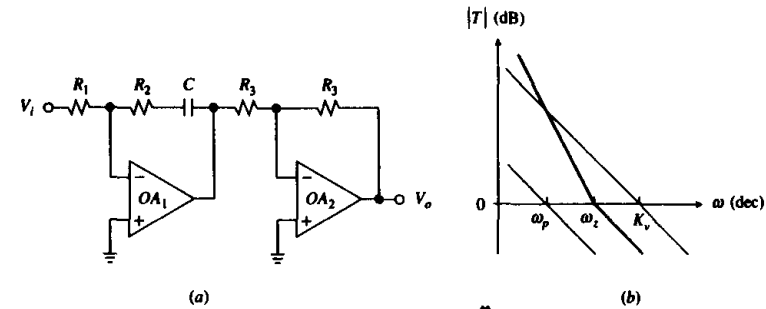


FIGURE 13.24
Active PI filter, and magnitude plot of the loop gain T .

Another popular loop filter is the *active PI filter* of Fig. 13.24a, so called because its output is proportional to the input as well as to the integral of the input. The inverting stage OA_2 can be omitted by interchanging the phase-detector inputs, if needed. Assuming ideal op amps, the filter gives

$$F(s) = \frac{1 + s/\omega_z}{s/\omega_p} \quad (13.44)$$

where $\omega_z = 1/R_2C$ and $\omega_p = 1/R_1C$. The corresponding loop gain is

$$T(j\omega) = \frac{1 + j\omega/\omega_z}{(j\omega/K_v)(j\omega/\omega_p)} \quad (13.45)$$

indicating a *second-order, Type II loop*. As shown in Fig. 13.24b, the slope is -40 dB/dec below ω_z , and -20 dB/dec above ω_z . Imposing again $\omega_z = \sqrt{\omega_p K_v}$ gives $\omega_x \cong \omega_z$ and $\phi_m \cong 45^\circ$.

Compared to the passive filter, whose dc gain is $F(0) = 1$, the active filter gives $F(0) = \infty$, indicating that the phase error θ_D needed to sustain the control voltage v_E approaches zero when the PI filter is used. In practice, $F(0)$ is limited by the finite dc gain of OA_1 ; even so, θ_D will still be vanishingly small, implying $\theta_O \cong \theta_I$, or phase coherence at the detector input. The use of the active filter also avoids possible loading effects at the output.

Damping Characteristics

Additional insight is gained by substituting Eqs. (13.42) and (13.44) into Eq. (13.38), and then expressing the latter in the standard form of Eq. (3.40). The results (see Problem 13.20) are

$$H(s) = \frac{(2\zeta - \omega_n/K_v)(s/\omega_n) + 1}{(s/\omega_n)^2 + 2\zeta(s/\omega_n) + 1} \quad (13.46a)$$

$$\omega_n = \sqrt{\omega_p K_v} \quad \zeta = \frac{\omega_n}{2\omega_z} \left(1 + \frac{\omega_z}{K_v}\right) \quad (13.46b)$$

for the passive lag-lead filter, and

$$H(s) = \frac{2\zeta(s/\omega_n) + 1}{(s/\omega_n)^2 + 2\zeta(s/\omega_n) + 1} \quad (13.47a)$$

$$\omega_n = \sqrt{\omega_p K_v} \quad \zeta = \frac{\omega_n}{2\omega_z} \quad (13.47b)$$

for the active PI filter. As we know, ω_n is the *undamped natural frequency*, and ζ is the *damping ratio*. If $\omega_n \ll K_v$, as is predominantly the case, Eq. (13.46) reduces to Eq. (13.47) and the PLL with the passive lag-lead filter is said to be a *high-gain loop*. We observe that $H(s)$ is in both cases a combination of the band-pass response H_{BP} and the low-pass response H_{LP} . At low frequencies $H \rightarrow H_{LP}$, but at high frequencies $H \rightarrow H_{BP}$.

Recall that for $\zeta < 1$ the step response exhibits overshoot. To keep the latter within reason, it is customary to design for $0.5 \leq \zeta \leq 1$. Under this condition, the time constant governing the loop response to small phase or frequency changes is roughly⁷

$$\tau \cong \frac{1}{\omega_n} \quad (13.48)$$

and the loop bandwidth, obtained by imposing $|H(j\omega)| = 1/\sqrt{2}$, is¹³

$$\omega_{-3 \text{ dB}} = \omega_n [1 \pm 2\zeta^2 + \sqrt{1 + (1 \pm 2\zeta^2)^2}]^{1/2} \quad (13.49)$$

where the plus (minus) sign holds for high-gain (low-gain) loops.

EXAMPLE 13.5. (a) Find ζ , τ , and $\omega_{-3 \text{ dB}}$ for the PLL of Example 13.4. (b) Find the response $v_e(t)$ to small input changes of the type $\omega_i = |\omega_i|u(t)$ and $\omega_i = |\omega_i|\cos\omega_m t$, $\omega_m = 1 \text{ krad/s}$.

Solution.

(a) By Eq. (13.46b), $\omega_n = \sqrt{10^3 \times 10^4} = 1 \text{ krad/s}$ and $\zeta = [10^3/(2 \times 10^3)](1 + 10^3/10^4) = 0.55$. Using Eq. (13.49) for the high-gain loop case gives $\omega_{-3 \text{ dB}} \cong 1.9\omega_n = 1.9 \text{ krad/s}$. By Eq. (13.48), $\tau \cong 1/10^3 = 1 \text{ ms}$.

(b) Substituting the above data into Eq. (13.46a) gives

$$H(s) = \frac{s/10^3 + 1}{(s/10^3)^2 + 1.1(s/10^3) + 1}$$

This function has a complex pole pair at $s = -550 \pm j835 \text{ complex Np/s}$, indicating a step response of the type

$$v_e(t) = \frac{|\omega_i|}{K_o} [1 - Ae^{-550t} \cos(835t + \phi)]$$

with A and ϕ suitable constants. Calculating $H(s)$ at $s = j\omega_m$ as in Example 13.3, we find the ac response as

$$v_e(t) = \frac{|\omega_i|}{K_o} 1.286 \cos(10^3 t - 45^\circ)$$

Filter Design Criteria

In general, ω_n is chosen high enough to ensure satisfactory dynamics, yet low enough to provide sufficient flywheel action for smoothing over undesired frequency jumps or noise. A typical design process proceeds as follows: (a) first, choose ω_n to achieve either the desired $\omega_{-3 \text{ dB}}$ or the desired τ , depending on the application; (b) next, using Eq. (13.46b) or (13.47b), specify ω_p for the chosen ω_n ; (c) finally, specify ω_z for the desired ζ .

We observe that because of the filter zero, a second-order PLL acts as a first-order loop at high frequencies, indicating a reduced ability to suppress ripple and noise. This drawback can be overcome by adding a capacitance $C_2 \ll C$ in parallel with R_2 in either of the above filters. This creates an additional high-frequency pole and turns the loop into a *third-order loop*. To avoid perturbing the existing values of ω_x and ϕ_m significantly, this pole is positioned about a decade above ω_x by imposing $1/R_2 C_2 \cong 10\omega_x$.

EXAMPLE 13.6. Redesign the filter of Example 13.4 for $\omega_{-3 \text{ dB}} = 1 \text{ krad/s}$ and $\zeta = 1/\sqrt{2}$. What are the new values of τ and ϕ_m ? What value of C_2 would yield a third-order loop without reducing ϕ_m too much?

Solution. With $\zeta = 1/\sqrt{2}$ we get $\omega_n \cong \omega_{-3 \text{ dB}}/2 = 10^3/2.0 = 500 \text{ rad/s}$, so $\tau \cong 2 \text{ ms}$. Equation (13.46b) gives $\omega_p = 25 \text{ rad/s}$ and $\omega_z = 366 \text{ rad/s}$, which can be realized with $C = 1 \mu\text{F}$, $R_1 = 39 \text{ k}\Omega$, and $R_2 = 2.7 \text{ k}\Omega$. Proceeding as in Example 13.4, we find $\omega_x \cong 757 \text{ rad/s}$, and $\phi_m \cong 66^\circ$. Use $C_2 \cong C/10 = 0.1 \mu\text{F}$.

13.5 MONOLITHIC PLLS

Monolithic PLLs are available in various technologies and in a wide range of performance specifications.¹² In the following we discuss the popular 4046 CMOS PLL as a representative example.

The 74HC(T)4046A CMOS PLL

Originally developed by RCA, the 4046 family of CMOS PLLs has gone through a series of improvements, and presently includes the 74HC(T)4046A, the 74HC(T)7046A, and the 74HC(T)9046A (Philips).¹³ We select the 4046A version, shown in simplified form in Fig. 13.25, because it includes the three most common phase detector types, known as *Type I* (PC_1), *Type II* (PC_2), and *Type III* (PC_3) *phase comparators*. Since the circuit is powered from a single supply (typically $V_{SS} = 0 \text{ V}$ and $V_{DD} = 5 \text{ V}$), all analog signals are referenced to $V_{DD}/2$, or 2.5 V .

The VCO

The VCO, whose details^{7,13} are omitted for brevity, is a current-controlled multivibrator operating on a principle similar to that of the emitter-coupled VCO of

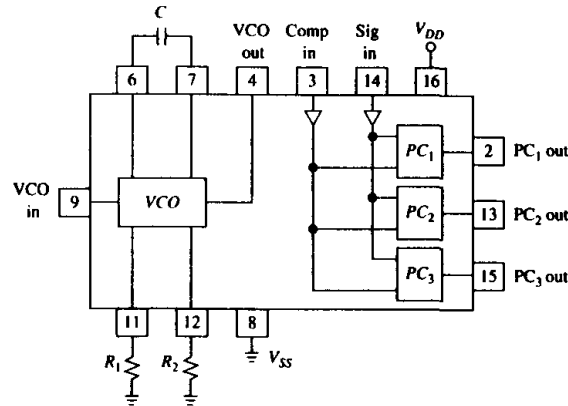


FIGURE 13.25
Simplified block diagram of the 4046A CMOS PLL.

Fig. 10.30. The current for the capacitor is obtained from the control voltage v_E via a $V-I$ converter whose sensitivity is set by R_1 and whose output is offset by R_2 . The VCO characteristic is of the type

$$f_O = \frac{k_1}{R_1 C} v_E + \frac{k_2}{R_2 C} \quad (13.50)$$

where k_1 and k_2 are suitable circuit constants. As shown in Fig. 13.26, the value of f_O corresponding to $v_E = V_{DD}/2$ is called the *center frequency* f_0 . It is apparent that if R_2 is omitted ($R_2 = \infty$), the *frequency offset* $f_{O(\text{off})} = k_2/R_2 C$ becomes zero. The maximum VCO frequency of CMOS PLLs is typically on the order of 10 MHz.

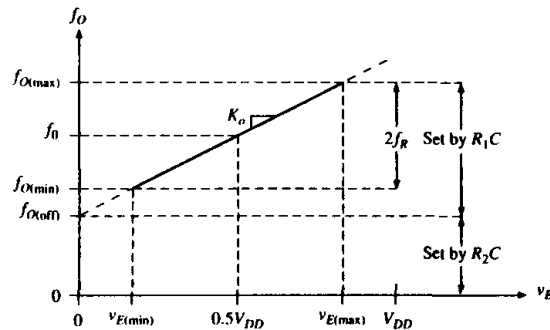


FIGURE 13.26
VCO characteristic and terminology.

The VCO characteristic of Eq. (13.50) holds only as long as v_E is confined within the range $v_{E(\text{min})} \leq v_E \leq v_{E(\text{max})}$. For a 4046A PLL with $V_{DD} = 5$ V, this range is typically¹³ $1.1 \text{ V} \leq v_E \leq 3.9 \text{ V}$. The frequency range corresponding to the permissible range of v_E is called the *VCO frequency range* $2f_R$. Outside this range the VCO characteristic depends on the particular 4046 version, and it can be found in the data sheets.

The VCO sensitivity is $K_O = 2f_R/[v_{E(\text{max})} - v_{E(\text{min})}]$. In FM applications it is usually required that the $V-F$ characteristic of the VCO be highly linear in order to minimize distortion. However, in such applications as frequency synchronization, synthesis, and reconstruction the linearity requirements are less stringent.

The Type I Phase Comparator

The Type I phase comparator, depicted in Fig. 13.27a, is an exclusive-OR (XOR) gate. This gate outputs $v_D = V_{DD} = 5$ V whenever its input levels disagree with each other, and $v_D = V_{SS} = 0$ whenever they agree. This is exemplified in the timing diagram of Fig. 13.28, where the waveforms have been plotted as a function of $\omega_1 t$. It is apparent that if we average out $v_D(t)$ by means of a low-pass filter, the result is $V_D = D V_{DD}$, where D is the duty cycle of v_D . D is minimized when the inputs

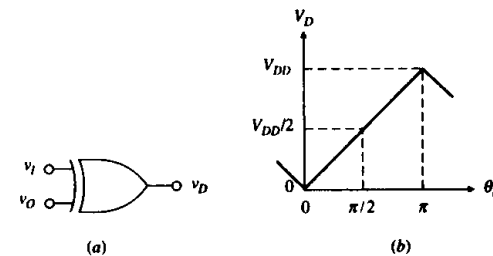


FIGURE 13.27
Type I phase comparator, and its output average V_D as a function of the input phase difference.

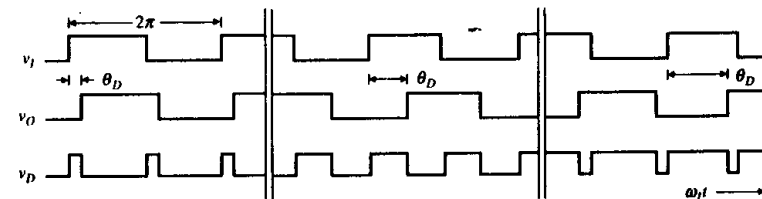


FIGURE 13.28
Typical waveforms for the Type I phase comparator in the locked condition: $\theta_D = \pi/6$ (left), $\theta_D = \pi/2$ (center), and $\theta_D = (5/6)\pi$ (right).

are in phase with each other, and maximized when they are in antiphase. If both input waveforms have 50% duty cycles, as shown, then $0 \leq D \leq 1$. Consequently, PC_1 will exhibit the characteristic of Fig. 13.27b, and $K_d = V_{DD}/\pi = 5/\pi = 1.59$ V/rad.

An alternative implementation of the Type I comparator, especially in bipolar PLLs designed to work with low-amplitude inputs, is a four-quadrant multiplier, as discussed in Section 13.2. Also called a *balanced modulator*, the multiplier is implemented with a scale factor high enough to ensure that v_I will typically overdrive the multiplier and thus render the sensitivity K_d independent of the amplitude of v_I .¹⁰

The Type I comparator requires that both inputs have 50% duty cycles; if at least one input is asymmetrical (see Problem 13.23), the characteristic will generally be clipped, reducing the lock range. Another notorious feature of the Type I comparator is that it may allow the PLL to lock on harmonics of the input signal. Note that if v_I is absent, v_D oscillates at the same frequency as v_O , so the average of v_D is $V_D = 0.5V_{DD}$, and $\omega_O = \omega_I$.

The Type III Phase Comparator

The Type III comparator, shown in simplified form in Fig. 13.29a, overcomes both of the above limitations by using an edge-triggered set-reset (SR) flip-flop. As depicted in Fig. 13.30, v_D now responds only to the rising edges of v_I and v_O , regardless of the duty cycles. It is readily seen that the phase range of PC_3 is twice as large as that of PC_1 , so the characteristic is as in Fig. 13.29b, and $K_d = V_{DD}/2\pi = 0.796$ V/rad.

The advantages of edge-triggering operation come at the price of higher sensitivity to noise. An input noise spike may falsely toggle the flip-flop and cause unacceptable output errors. By contrast, with a Type I comparator, an input spike is merely transmitted to the output, where it is suppressed by the loop filter.

We observe that in the locked condition the output frequency is $\omega_D = 2\omega_I$ for PC_1 , and $\omega_D = \omega_I$ for PC_3 , so the ripple at the output of the loop filter is generally higher with PC_3 than with PC_1 . Note that with v_I absent, PC_3 will drive ω_O as low as it can.

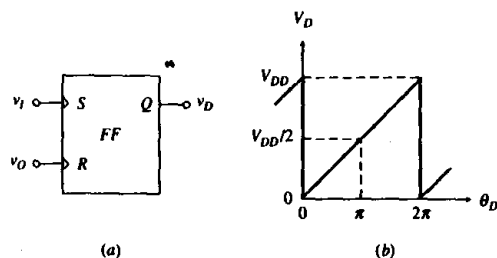


FIGURE 13.29

Type III phase comparator, and its output average V_D as a function of the input phase difference.

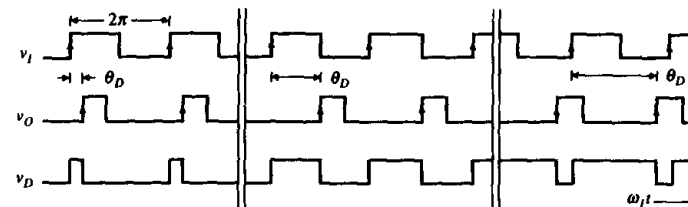


FIGURE 13.30

Typical waveforms for the Type III phase comparator in the locked condition: $\theta_D = \pi/4$ (left), $\theta_D = \pi$ (center), and $\theta_D = (7/4)\pi$ (right).

The Type II Phase Comparator

The Type II comparator differs from PC_1 and PC_3 because its output depends not only on the phase error $\theta_I - \theta_O$, but also on the frequency error $\omega_I - \omega_O$ when the loop has not yet acquired lock. Also called a *phase-frequency detector* (PFD), the circuit is shown in simplified form in Fig. 13.31a.

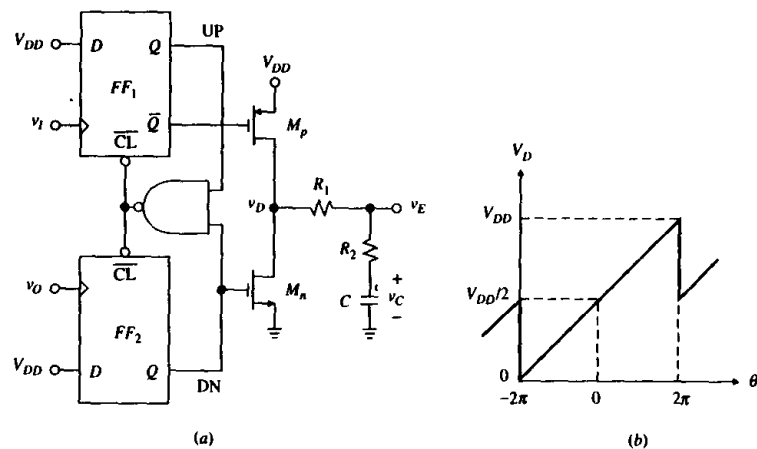


FIGURE 13.31

Type II phase comparator, and its output average V_D as a function of the input phase difference.

With reference to Fig. 13.32, we observe that PC_3 produces UP pulses when the rising edge of v_I leads that of v_O , DN pulses when the rising edge of v_I lags that of v_O , and no pulses when the leading edges are aligned. An UP pulse closes the MOSFET switch M_P and causes the filter capacitance C to charge toward V_{DD} via the series $R_1 + R_2$. A DN pulse closes switch M_N and discharges C toward $V_{SS} = 0$ V. Between pulses, both M_P and M_N are off, providing a high-impedance state to the filter. When PC_2 is in this state, C acts as an analog memory, retaining whatever charge it had accumulated at the end of the last UP or DN pulse.

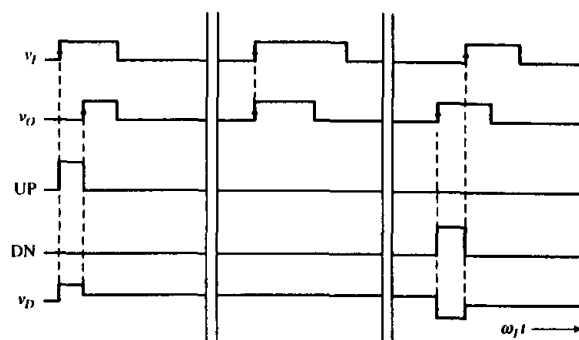


FIGURE 13.32
Typical waveforms for the Type II phase comparator for $\omega_O = \omega_I$: v_O lags v_I (left), v_O is in phase with v_I (center), and v_O leads v_I (right).

Clearly, we now have $v_D = v_E = v_C$. The characteristic is as in Fig. 13.31b, with $K_d = V_{DD}/4\pi = 0.398$ V/rad. For obvious reasons, PC_2 is also called a *charge-pump phase comparator*.

To appreciate its operation, suppose we initially have $\omega_I > \omega_O$. Since v_I generates more rising edges per unit time than v_O , UP will be high most of the time, pumping charge into C and thus raising ω_O . Conversely, when $\omega_I < \omega_O$, DN is high most of the time, pumping charge out of C and lowering ω_O . In either case, PC_2 will keep pumping charge until the inputs become equal both in frequency and in phase, or $\omega_O = \omega_I$ and $\theta_O = \theta_I$. We conclude that PC_2 approaches *ideal-integrator* behavior.

It is apparent that a PLL with a Type II comparator will lock under any condition, and that it drives the input-phase error to zero over the full frequency range of the VCO. Moreover, since the UP and DN pulses disappear entirely once the loop is locked, v_E will exhibit no ripple, so there are no unwanted phase modulation effects. The main drawback of PC_2 is its susceptibility to noise spikes, just like PC_3 . Even so, PC_2 is the most popular of the three PCs. Note that with v_I absent, PC_2 will drive ω_O as low as it can.

Designing with PLLs

The design process of a PLL-based system involves a number of decisions¹² dictated by the performance specifications of the given application, along with considerations of circuit simplicity and cost. For 4046 PLLs, this process requires (a) the specification of the VCO parameters f_0 and $2f_R$, the choice of (b) the phase-detector type and (c) the filter type, and (d) the specification of the filter parameters ω_p and ω_z .

To simplify the process, computer programs are available that accept specifications by the user and translate them into actual resistance and capacitance values to meet the VCO and filter requirements. An example is the *HCMOS Phase-Locked Loop Program*, by Philips Semiconductors (check our Web site at <http://www.mhhe.com/franco> to find how to download this program), which also provides important

data about the loop dynamics and displays the frequency response via Bode plots. Once a PLL system has been designed, it can be simulated by computer,^{7,12} for instance, using suitable SPICE macromodels.¹⁴ However, the designer still needs a sound understanding of PLL theory to judge the results of any simulation!

Popular PLL applications¹⁰ include FM, PM, AM, and FSK modulation/demodulation, frequency synchronization and synthesis, clock reconstruction, and motor speed control. Here we discuss two examples, FM demodulation and frequency synthesis. Other examples can be found in the end-of-chapter problems.

EXAMPLE 13.7. An FM signal is being modulated over the range of $1 \text{ MHz} \pm 10 \text{ kHz}$ with a modulating frequency of 1 kHz . Using a 4046A PLL, design a circuit to demodulate such a signal.

Solution. For the VCO we let $f_0 = 1 \text{ MHz}$, and choose $2f_R$ wide enough to accommodate parameter spread. Thus, let $2f_R = 0.5 \text{ MHz}$. This gives $K_o = 2\pi \times 0.5 \times 10^6 / 2.8 = 1.122 \times 10^6$ (rad/s)/V. Using the data sheets or the aforementioned PLL program, we find that a suitable set of VCO components is $R_1 = 95.3 \text{ k}\Omega$, $R_2 = 130 \text{ k}\Omega$, and $C = 100 \text{ pF}$.

Next, anticipating a noisy input signal, we choose PC_1 , so $K_d = 5/\pi$ V/rad and $K_v = K_d K_o = 1.786 \times 10^6 \text{ s}^{-1}$. To allow for the possibility of a weak input, we take advantage of the fact that the detector input buffers are self-biased near $V_{DD}/2$, where gain is maximized. Consequently, the input signal is ac coupled, as shown in Fig. 13.33.

Finally, to minimize cost, we use a passive lag-lead filter. Impose $\zeta = 0.707$ and choose $f_{-3 \text{ dB}} > f_m$, say, $f_{-3 \text{ dB}} = 10 \text{ kHz}$. Proceeding as in Example 13.6, we find $\omega_p = 553 \text{ rad/s}$ and $\omega_z = 22.5 \text{ krad/s}$, which can be met with the filter components shown in the figure.

Just as inserting a voltage divider within the feedback loop of an op amp increases the output voltage swing, inserting a frequency divider inside the PLL loop downstream of the VCO increases the VCO frequency. A frequency divider is implemented with a counter, and the VCO output frequency becomes $\omega_O = N\omega_I$, where N is the counter modulus. Making the counter programmable allows the synthesis of variable frequencies that are integral multiples of ω_I .

The PLL formalism still holds, but with K_o replaced by K_o/N . We observe that varying N varies also the gain factor K_v , so care must be exercised to ensure that stability and dynamics are maintained over the full range of values of N .

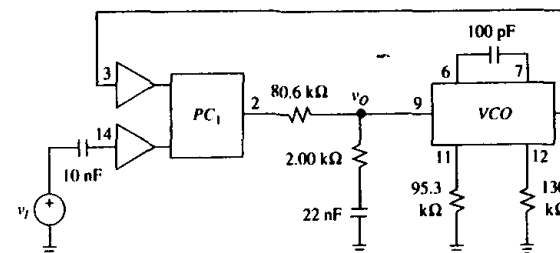


FIGURE 13.33
FM demodulator using the 4046A PLL.

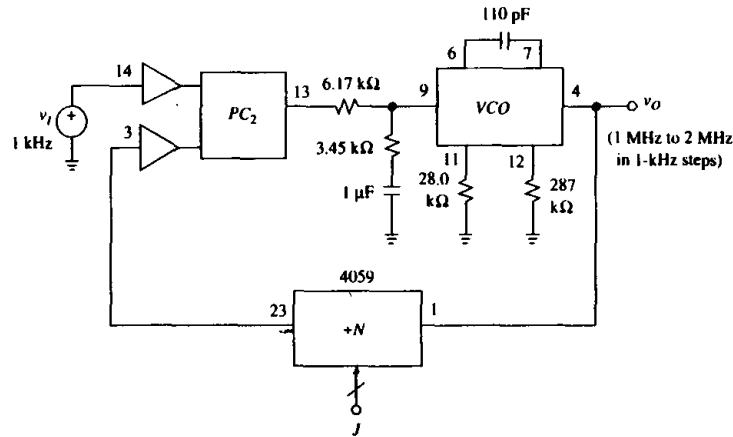


FIGURE 13.34
Frequency synthesizer using the 4046A PLL.

EXAMPLE 13.8. Using a 4046A PLL, design a circuit that accepts a 1-kHz reference frequency and synthesizes all frequencies between 1 MHz and 2 MHz in 1-kHz steps.

Solution. To span the given range, we need a programmable counter between $N_{\min} = 10^6/10^3 = 1000$ and $N_{\max} = 2000$. Choose, for instance, a 4059 counter, which allows for N to be programmed anywhere from 3 to 15,999 via a set of inputs referred to as the *jam inputs* J in the data sheets.

For the VCO, specify f_0 halfway between the extremes, or $f_0 = 1.5$ MHz, and again choose $2f_R$ wide enough, say, $2f_R = 1.5$ MHz. This gives $K_v = 3.366 \times 10^6$ (rad/s)/V. Using the data sheets or the aforementioned PLL program, we find the VCO component values $R_1 = 28.0$ kΩ, $R_2 = 287$ kΩ, and $C = 110$ pF.

Anticipating relatively clean on-board signals, we choose PC_2 , so $K_d = 5/4\pi$ V/rad. Since N is variable, a reasonable approach¹² is to design for the geometric mean of the extremes, or for $N_{\text{mean}} = \sqrt{N_{\min}N_{\max}} = 1414$. The corresponding gain factor is then $K_{v(\text{mean})} = K_d K_v / N_{\text{mean}} = 947$ s⁻¹.

We again use a passive lag-lead filter. Imposing $\zeta = 0.707$ and arbitrarily choosing $\omega_n = \omega_i/20 = 2\pi \cdot 10^3/20 = \pi \cdot 100$ rad/s, we obtain $\omega_p = 104$ rad/s and $\omega_z = 290$ rad/s. These parameters are met with the filter components shown in Fig. 13.34, where the wiring details of the 4059 counter have been omitted for simplicity.

Using Eq. (13.46b), we find $\zeta = 0.78$ for $N = 1000$, and $\zeta = 0.65$ for $N = 2000$, both of which are fairly reasonable values.

PROBLEMS

13.1 Log/antilog amplifiers

13.1 In the transdiode of Fig. 13.2a let $R = 10$ kΩ, $C_n + C_\mu = 20$ pF, $V_A = 100$ V, $r_d = 2$ MΩ, and $f_i = 1$ MHz. If $R_E = 4.3$ kΩ and $C_f = 100$ pF, calculate $1/\beta_0$,

$1/\beta_\infty$, f_z , and f_p for $v_i = 1$ mV, 10 mV, and 10 V; hence, confirm the linearized plots of Fig. 13.3.

13.2 Find the phase margin of the circuit of Example 13.1.

13.3 Modify the circuit of Fig. 13.4 to yield $v_o = -(2 \text{ V/dec}) \log_{10}[v_i/(1 \text{ V})]$.

13.4 (a) Derive Eqs. (13.13) and (13.14). (b) Design a circuit that accepts an input voltage $-5 \text{ V} \leq v_i \leq +5 \text{ V}$, and gives $i_O = (10 \mu\text{A})2^{-v_i/(1 \text{ V})}$; this circuit is useful in electronic music. (c) Modify the above circuit so that it gives the same output range, but for $0 \text{ V} \leq v_i \leq 10 \text{ V}$.

13.5 The log conformity error at the upper end of the current range is due primarily to the bulk resistance of the emitter region, which can be modeled with a small resistance r_s in series with the emitter itself. (a) Recompute the transfer characteristic of the transdiode of Fig. 13.1b, but with r_s in place. If $r_s = 1$ Ω, what is the log conformity error at $i_i = 1$ mA? At $i_i = 0.1$ mA? (b) The effect of r_s can be compensated by feeding a small portion of v_i to the base of the BJT. This is achieved by lifting the base off ground, returning it to ground via a resistance R_x , and connecting a second resistance R_y between the source v_i and the base of the BJT. Sketch the modified circuit, and show that choosing $R_y/R_x = R/r_s - 1$ will eliminate the error due to r_s .

13.6 In the log amp of Fig. 13.4 the bulk-resistance error (see Problem 13.5) can be compensated by connecting a suitable network between the base of Q_2 and the output of OA_2 . Such a network consists of a resistance R_c in series with a diode D_c (cathode at the output of OA_2). In the antilog amp of Fig. 13.6 the compensation network is connected between the base of Q_1 and the output of OA_1 (cathode at the output of OA_1). Show that the error is nulled when $R_c = (R_1 \parallel R_2)(2.2 \text{ kΩ})/r_s$. What is the required R_c , given that the LM394 has $r_s = 0.5$ Ω?

13.2 Analog multipliers

13.7 A popular multiplier application is *frequency doubling*. One way of configuring the AD534 for this operation is as follows:⁶ connect X_2 and Y_1 to ground, connect X_1 and Y_2 together and drive them with a source $v_i = 10 \cos \omega t$ V, connect the Out pin to Z_1 via a 10-kΩ resistor, connect Z_1 to Z_2 via another 10-kΩ resistor, and drive Z_2 with a 10-V reference voltage. (a) Sketch the circuit; then, using the identity $\cos^2 \alpha = (1 + \cos 2\alpha)/2$ obtain an expression for the output v_o . (b) Assuming well-regulated ± 15 -V supplies, design a circuit to generate the 10-V reference for Z_2 .

13.8 The AD534 multiplier can be made to approximate the *sine function* within 0.5% of full scale as follows:⁶ connect Y_2 to ground, connect Y_1 and Z_2 together and drive them with a source v_i , connect Y_1 to X_2 via a 10-kΩ resistor, connect X_2 to ground via an 18-kΩ resistor, connect the Out pin to Z_1 via a 4.7-kΩ resistor, connect Z_1 to X_1 via a 4.3-kΩ resistor, and connect X_1 to ground via a 3-kΩ resistor. (a) Sketch the circuit, derive an expression for the output v_o as a function of v_i , and calculate v_o at some significant points to verify that the circuit approximates the function $v_o = 10 \sin[(v_i/10)90^\circ]$ V. (b) Using additional components as needed, design a circuit that accepts a triangular wave with peak values of ± 5 V and gives a sine wave with the same frequency and peak values as the input.

- 13.9 The AD534 multiplier can be configured to yield the percentage deviation between two signals v_1 and v_2 as follows: connect X_1 and Z_1 together and drive them with v_1 , connect X_2 and Y_1 to ground, drive Z_2 with v_2 , connect the Out pin to Y_2 via a resistance R_1 , and connect Y_2 to ground via a resistance R_2 . Develop an expression for the output v_O , and specify R_1 and R_2 for $v_O = 100(v_2 - v_1)/v_1$.

- 13.10 Figure P13.10 shows a transducer-response linearization technique using a four-quadrant multiplier. Derive an expression for V_O as a function of δ and verify that it is linearly proportional to δ in spite of the fact that the voltage across the transducer is a nonlinear function of δ .

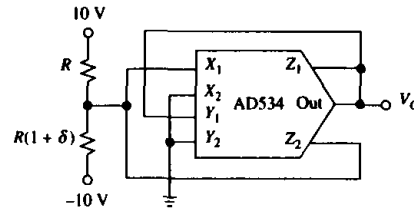


FIGURE P13.10

- 13.11 Using the AD534 as a voltage-controlled attenuator, design a programmable first-order low-pass filter with a dc gain of 20 dB and $f_0 = kV_C$, $0.1 \text{ V} \leq V_C \leq 10 \text{ V}$ and $k = 100 \text{ Hz/V}$. Hint: See Problem 12.11.

13.3 Operational transconductance amplifiers

- 13.12 Find the transfer function of the g_m -C filter of Fig. P13.12.

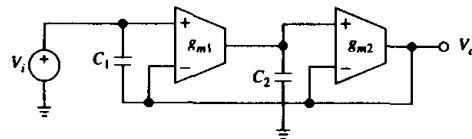


FIGURE P13.12

- 13.13 Design an exponential VCA such that $A = 2^{-V_C/(1 \text{ V})} \text{ V/V}$, $0 \leq V_C \leq 10 \text{ V}$. Hence, outline its calibration procedure.
- 13.14 Design a programmable state-variable filter with $Q = 10$, $H_{\text{BP}} = 1$, and f_0 variable over the audio range by means of control voltage V_C as $f_0 = (20 \text{ kHz})2^{-V_C/(1 \text{ V})}$, $0 \leq V_C \leq 10 \text{ V}$.
- 13.15 The VCA610 (Burr-Brown) is a wideband VCA that accepts two signal inputs v_P and v_N and a control input V_C , and gives $v_O = A(v_P - v_N)$, where $A = 0.01 \times 10^{-V_C/(0.5 \text{ V})} \text{ V/V}$ for $-2 \text{ V} \leq V_C \leq 0$. Using a VCA610 and an OPA620 wideband precision op amp, design a first-order low-pass filter with unity dc gain and programmable cutoff frequency from 100 Hz to 1 MHz.

- 13.16 (a) Sketch and label all relevant waveforms in the CCO of Fig. 13.20, and derive Eq. (13.32). (b) Find C so that $f_0 = 100 \text{ kHz}$ for $I_C = 1 \text{ mA}$; next, using this CCO as basis, design a VCO such that $f_0 = (100 \text{ kHz})10^{-V_C/(2 \text{ V})}$, $0 \leq V_C \leq 10 \text{ V}$. Outline its calibration procedure.

13.4 Phase-locked loops

- 13.17 Find the phase response $\theta_d(t)$, in degrees, in parts (a) and (b) of Example 13.3.

- 13.18 If we let $R_2 = 0$ in Fig. 13.23a, the zero is moved to infinity, resulting in a *passive lag filter*. Such a filter finds limited use because it does not allow for ω_x to be specified independently of K_v . (a) Verify that if we let $R_2 = 0$ in the filter of Example 13.4, the phase margin is inadequate. (b) Specify a new set of values for R_1 and C to ensure $\phi_m \cong 45^\circ$ with $R_2 = 0$. What is the corresponding value of ω_x ?

- 13.19 Repeat Example 13.4, but using an active PI filter.

- 13.20 Prove Eqs. (13.46) through (13.47).

- 13.21 A PLL has $\omega_0 = 2\pi 10^6 \text{ rad/s}$, $K_d = 0.2 \text{ V/rad}$, $K_a = 1 \text{ V/V}$, and $K_o = \pi 10^6 \text{ (rad/s)/V}$. Design an active PI filter for a loop time-constant of approximately 100 periods of the free-running frequency and $Q = 0.5$.

- 13.22 If a $0.1\text{-}\mu\text{F}$ capacitance is connected in parallel with R_2 in the loop filter of Example 13.6, find how it affects ω_x and ϕ_m .

13.5 Monolithic PLLs

- 13.23 (a) Sketch and label the average V_D versus θ_D for a Type I phase comparator if the duty cycles of v_I and v_O are $D_I = \frac{1}{2}$ and $D_O = \frac{1}{3}$. (b) Repeat, but with $D_I = \frac{1}{3}$ and $D_O = \frac{1}{2}$. Comment.

- 13.24 Sketch v_I , v_O , UP, DN, and v_D for a Type II detector if (a) ω_I is slightly higher than ω_O , (b) ω_I is slightly lower than ω_O , (c) $\omega_I \gg \omega_O$, and (d) $\omega_I \ll \omega_O$.

- 13.25 A certain CMOS PLL is powered between 5 V and 0 V, and uses a Type I phase comparator and a VCO with $K_o = 5 \text{ MHz/V}$ and $f_0 = 10 \text{ MHz}$ for $v_E = 2.5 \text{ V}$. (a) Design a passive lag-lead filter for $\omega_n = 2\pi 5 \text{ krad/s}$ and $Q = 0.5$. (b) Sketch v_I , v_O , v_D , and v_E for the case in which the loop is locked to an input frequency of 7.5 MHz.

- 13.26 Find $v_e(t)$ in the FM demodulator of Example 13.7.

- 13.27 Dual-slope ADCs are clocked at a frequency that is locked to the ac line frequency f_{line} in order to reject line-induced noise. Using a 4046A PLL, design a circuit that accepts f_{line} (either 60 Hz or 50 Hz) and gives $f_{\text{CK}} = 2^{16} \times f_{\text{line}}$. Specify as many parameters and components as you can in your circuit.

- 13.28 Using a 4046A for phase detection and an 8038 as VCO, design a circuit that generates a 1-kHz sine wave synchronized on a 1-MHz crystal oscillator.

- 13.29 An FSK signal v_I alternates between $f_L = 1200 \text{ Hz}$ (logic 0) and $f_H = 2400 \text{ Hz}$ (logic 1). One way¹³ to decode this signal with a 4046A PLL is to use PC_3 , a loop

filter consisting of a plain RC stage with $1/2\pi RC = f_H$, the VCO with $f_0 = (f_L + f_H)/2 = 1.8$ kHz and $2f_R = 2$ kHz, and a positive edge-triggered latch flip-flop of the type of Fig. 13.31, with v_I as the D input and the VCO output v_O as the clock; the $\bar{Q}$ output of the flip-flop is the FSK decoder output. Draw the circuit; then sketch and label v_I , the average of v_E , v_O , and $\bar{Q}$ both for $f_I = f_L$ and $f_I = f_H$. What is the distinguishing feature of PC_3 that makes it attractive in this application?

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INDEX

- A**
- $\mu A78G$, 524
 - $\mu A79G$, 524
 - $\mu A741$ op amp, 1, 2, 212, 215, 216, 249–257, 340
 - $\mu A7800$ series, 523–525, 530
 - $\mu A7805$ regulator, 525, 527
 - $\mu A7900$ series, 523, 530
 - Absolute accuracy, 562
 - Absolute maximum ratings, 241
 - Absolute-value circuit, 422
 - ac-dc converters, 426–428
 - ac noise. *See* Noise
 - Acquisition time, 439
 - Active compensation of integrators, 285
 - Active filters, 106–210
 - all-pass filters. *See* All-pass filters
 - audio filter applications, 121–126. *See also* Audio filter applications
 - band-pass filters. *See* Band-pass filters
 - band-reject filters. *See* Band-reject filters
 - biquad filters, 147, 148
 - common frequency responses, 106–108
 - first-order filters, 115–121. *See also* First-order active filters
 - GBP, and, 289–293
 - higher-order filters, 160–210. *See also* Higher-order active filters
 - high-pass filters. *See* High-pass filters
 - KRC filters, 133–141. *See also* KRC filters
 - limitation, 109
 - low-pass filters. *See* Low-pass filters
 - multiple-feedback filters, 141–144
 - nature of, 109
 - RLC filters, 109
 - SC filters. *See* SC filters
 - second-order filters, 126–133. *See also* Second-order filters
 - sensitivity, 150–152
 - SV filters, 144–147
 - transfer function, 109–114
 - universal filters, 144–150
 - Active guard drive, 86, 87
 - Active PI filter, 633
 - Active tone control, 123–125
 - AD522, 81
 - AD534, 618
 - AD537 V-F converter, 484
 - AD537 voltage-to-frequency converter, 487–489
 - AD549, 222
 - AD590 IPTAT, 518
 - AD590 two-terminal temperature transducer, 512
 - AD594/5/6/7 series, 519
 - AD817, 364
 - AD7846 16-bit segmented DAC, 577
 - A-D converters, 559–606. *See also* D-A converters
 - CR ADC, 588–590
 - DAC-based A-D conversion, 584, 585
 - errors, 566
 - flash converters, 590, 591
 - INL/DNL, 566
 - integrating-type converters, 592–595
 - performance specifications, 564, 565
 - pipelined converters, 592
 - SA ADC, 586–588
 - subranging converters, 591, 592
 - ADCs. *See* A-D converters
 - Aliasing, 596
 - All-pass filters
 - all-pass response, 107, 108
 - second-order filters, 132
 - All-pole ladder, 182
 - Alternative D -element realization, 178
 - Amount of feedback, 24
 - AMP-01, 83–85
 - Amplifier
 - bridge, 57. *See also* Transducer bridge amplifiers
 - CFAs, 293–303. *See also* Current-feedback amplifiers (CFAs)
 - composite, 384–390
 - current, 71, 72
 - difference, 19, 20, 73–79. *See also* Difference amplifiers
 - fundamentals, 2–5
 - 1As, 79–91. *See also* Instrumentation amplifiers
 - inverting, 12–15, 266–268
 - linear, 3
 - log/antilog, 608–615
 - main, 234
 - noninverting, 8–12, 262–264
 - nonlinear. *See* Nonlinear amplifiers
 - nulling, 234
 - op amp. *See* Op amp
 - OTA, 620–627
 - photodetector, 63
 - SHAs, 437–443
 - THAs, 437–443
 - transconductance, 63–71. *See also* Voltage-to-current converters
 - transducer bridge, 91–97
 - transimpedance, 61, 294
 - transresistance, 5, 61–63
 - VFAs, 293, 300–303
 - voltage, 3
 - Analog division, 619, 620
 - Analog ground-switch, 430
 - Analog multipliers, 615–620
 - Analog switches, 428–433
 - Analog to digital converters. *See* A-D converters
 - Angular frequency, 109, 258
 - Antilogarithmic amplifier, 609, 613
 - Aperture jitter, 439
 - Aperture time, 439
 - Aperture uncertainty, 439
 - Astable multivibrator, 457
 - Audio filter applications, 121–126
 - active tone control, 123–125
 - graphic equalizers, 125, 126
 - phono preamplifier, 122
 - tape preamplifier, 123
 - Autozero mode, 235
 - Autozero phase, 594
 - Autozero (AZ) technique, 234
 - Avalanche breakdown, 507