IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

BISHOP DISPLAY TECH LLC, Plaintiff, v. BOE TECHNOLOGY GROUP CO., LTD., Defendant.	Civil Action No. 2:25-CV-310-JRG (Lead Case) Civil Action No. 2:25-CV-309-JRG

DEFENDANT'S INVALIDITY CONTENTIONS AND
P.R. 3-3 AND 3-4 DISCLOSURES

Pursuant to Local Patent Rules ("P.R.") 3-3 and 3-4 and the Court's Docket Control Order (Dkt. No. 37 in the -310 case and Dkt. No. 38 in the -309 case),[1] Defendant BOE Technology Group Co., Ltd., ("Defendant" or "BOE") provides its Invalidity Contentions concerning U.S. Patent No. 6,525,798 (the "'798 patent"); U.S. Patent No. 6,787,829 (the "'829 patent"); U.S. Patent No. 6,801,293 (the "'293 patent"); U.S. Patent No. 6,816,208 (the "'208 patent"); U.S. Patent No. 6,850,303 (the "'303 patent"); U.S. Patent No. 6,906,769 (the "'769 patent"); U.S. Patent No. 7,414,682 (the "'682 patent"); U.S. Patent No. 7,583,347 (the "'347 patent"); U.S. Patent No. 7,995,047 (the "'047 patent"); and U.S. Patent No. 8,093,830 (the "'830 patent") (together, the "Asserted Patents"). These contentions set forth Defendant's preliminary Invalidity Contentions with respect to the claims that were identified by Plaintiff Bishop Display Tech LLC ("Plaintiff" or "Bishop Display") in its P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions, served July 30, 2025 ("Infringement Contentions").

[1] Unless otherwise specified, references to the docket numbers will be to the -310 lead case.

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Defendant is also producing, concurrently with these Invalidity Contentions, documents required by P.R. 3-4, including copies of prior art references required by P.R. 3-4(b).

I. INTRODUCTORY STATEMENT

Plaintiff has asserted the following claims against Defendant, consolidated in Civil Action No. 2:25-cv-310-JRG (E.D. Tex.):

U.S. Patent No.	Asserted Claims
6,525,798	1, 2, 4, 5, and 6
6,787,829	1, 2, 5, 6, 10, 11, 18, 19, 29, 30
6,801,293	1
6,816,208	1, 3
6,850,303	1, 4
6,906,769	1, 4, 5, 6, 7, 9, and 14
7,414,682	7, 9
7,583,347	1
7,995,047	1
8,093,830	1

(*See* Plaintiff's Disclosure of Asserted Claims and Infringement Contentions (P.R. 3-1).) These claims are collectively referred to as "the Asserted Claims." The Asserted Claims of the '798, '829, '293, '208, '303, '769, '682, '347, '047, and '830 patents, however, are neither novel nor non-obvious in view of the state of the prior art and the understanding of a person of ordinary skill in the art at the time of the alleged inventions ("POSITA"). The Asserted Claims are also invalid for lack of written description, lack of enablement, and/or indefiniteness under 35 U.S.C. § 112, as explained herein.

In accordance with P.R. 3-3(a)–(d), Defendant hereby: (a) identifies each currently known item of prior art that either anticipates or renders obvious each asserted claim; (b) specifies (i) whether each such item of prior art anticipates each asserted claim and/or renders it obvious, and (ii) if a combination of items of prior art renders a claim obvious, identifies each such combination and the motivation to combine such items; (c) submit a chart identifying where each element in

each asserted claim is disclosed, described, or taught in the prior art, and the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function in the case of means-plus-function elements under 35 U.S.C. § 112, ¶ 6; and (d) identifies the grounds for invalidating the Asserted Claims based upon indefiniteness under 35 U.S.C. § 112, ¶ 2 or enablement or written description under 35 U.S.C. § 112, ¶ 1, with respect to each asserted claim and based upon Defendant's investigation to date.

The initial Invalidity Contentions provided herein by Defendant are preliminary and subject to revision as provided in the Local Rules, the Federal Rules of Civil Procedure, and/or any Order of this Court. For example, these Invalidity Contentions are based on Defendant's current knowledge, understanding, and belief as to the facts and information available at this time. Defendant has not yet completed its investigation, collection of information, discovery, or analysis relating to this action, and additional facts and information may require Defendant to supplement or modify these Invalidity Contentions.

Invalidity Contentions, as required by the P.R. 3-4, typically follow a plaintiff's production of conception and reduction to practice, design and development documents as well as documents evidencing disclosures or offers to sell the patented invention prior to the date of application for the patents-in-suit, as required by P.R. 3-2. To date, however, Bishop Display has not produced any such documentation, stating that "[it] is not presently aware of any non-privileged documents sufficient to evidence discussion with, disclosure to, or other manner of providing to a third party, or sale of or offer to sell, the claimed inventions prior to the date of application for the patents-in-suit" and that "[it] is not presently aware of any non-privileged documents that evidence conception, reduction to practice, design, and development of each claimed invention that were created on or before the above referenced dates for each of the patents-in-suit." (Infringement

Contentions at 20). Accordingly, Defendant has proceeded with its Invalidity Contentions by relying on Plaintiff's representations that it cannot establish an earlier conception or reduction to practice date for any Asserted Claim of the Asserted Patents. Defendant reserves its right to amend and/or supplement these Invalidity Contentions in view of any late identification of evidence of purported earlier conception or reduction to practice.

In addition, Bishop Display's Infringement Contentions are deficient in multiple respects and do not provide Defendant with sufficient information to understand the bases for Bishop Display's infringement allegations or the alleged scope of the claims as Bishop Display is applying them in making such allegations. Indeed, Plaintiff accuses more than 800 products but fails to identify how any representative group of products allegedly infringes the patents-in-suit. Bishop Display's infringement contentions suffer from various deficiencies, including its failure to provide contentions to demonstrate that certain accused products are representative of other accused products, and various deficiencies in the infringement contention charts and the cited evidence that Plaintiff attempts to point to for various claim limitations of the Asserted Patents. Defendant's Invalidity Contentions are therefore based on Defendant's best understanding of Plaintiff's apparent constructions of the Asserted Claims and Plaintiff's theories of infringement.

Furthermore, Defendant intends to diligently seek documents from third parties in discovery to demonstrate such third parties' earlier dates of invention under 35 U.S.C. § 102(g) and/or prior art offers for sale and public uses of products embodying the claimed invention under 35 U.S.C. § 102(b) or under 35 U.S.C. § 102(a). Defendant therefore reserves the right to supplement these Invalidity Contentions with further information and documentation, if and when it becomes available.

Defendant also reserves its right to supplement and/or amend these Invalidity Contentions after the Court has construed disputed claim terms. Defendant's contentions concerning the validity of the Asserted Claims may change based upon the Court's construction of the claims or positions that Bishop Display takes concerning infringement or validity issues after such construction. Moreover, given the inadequacies in Bishop Display's Infringement Contentions, Defendant has used its best efforts to understand how Bishop Display is construing the Asserted Claims for purposes of identifying invalidating prior art. Nothing contained in these Invalidity Contentions or any accompanying Exhibits, however, should be understood or deemed to be an express or implied admission or contention with respect to the proper construction or scope of any terms in the Asserted Claims, nor should they be understood to adopt Bishop Display's stated claim construction or its proposed scope of the Asserted Claims. Defendant's Invalidity Contentions merely consider Bishop Display's apparent application of the Asserted Claims to the accused products under the principle that the scope of the claim must be the same for invalidity as it is for infringement.

Defendant provides the information below and in the attached charts and document production in order to comply with P.R. 3-3 and 3-4. Defendant reserves the right to prove the invalidity or unenforceability of the Asserted Claims on bases other than those required to be disclosed in these Invalidity Contentions pursuant to P.R. 3-3. The production of documents that have been identified in these Invalidity Contentions shall not be deemed an admission that such documents are admissible or that Defendant has waived any objections regarding the admissibility of such documents.

Pursuant to the provisions of P.R. 3-3, Defendant identifies specific portions of prior art references that disclose the elements of the Asserted Claims. Although Defendant has identified

exemplary disclosures for each reference, each and every disclosure in the reference is not necessarily identified. The lack of a citation for an element should not be deemed an admission that the element is not disclosed or is not inherent in the reference. In an effort to focus the issues, Defendant identifies only exemplary portions of cited references. It should be recognized that persons of ordinary skill in the art generally read a prior art reference as a whole and in the context of other publications and literature and in light of the knowledge of one of ordinary skill in the art. To understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their scientific or engineering knowledge. Defendant consequently reserves the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony as to the knowledge of a person of ordinary skill in the art to provide context, and as aids to understanding and interpreting the portions of that art identified. Defendant also reserves the right to rely on other portions of the prior art references, other publications, and the testimony of experts to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain of the cited references so as to render the claims obvious. Further, where Defendant identifies a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure and any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure, the identification should be understood to include the figure as well. Defendant further reserves the right to rely upon any applicable industry standards and prior art cited to the patent office as invalidating references or to show the state of the art.

Prior art not included in these Invalidity Contentions, whether known or unknown to Defendant, may become relevant based on subsequent events. In particular, Defendant is currently

unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Defendant. To the extent that such an issue arises, Defendant reserves the right to identify other known references that would disclose or render obvious the allegedly missing limitation(s) of the Asserted Claims.

Defendant further intends to rely on inventor and Bishop Display admissions concerning the prior art relevant to the Asserted Patent found in, *inter alia*: the Asserted Patents, the patent prosecution histories for the Asserted Patents and related patents and/or patent applications; any deposition testimony of the named inventors on the Asserted Patents; and the papers filed and any evidence submitted by Plaintiff in connection with this litigation or other of its past, current, or future litigations or administrative proceedings concerning or relating to one or more of the Asserted Patents.

Because Defendant is continuing its search for and analysis of relevant prior art, Defendant reserves the right to seek to amend or supplement the information provided herein, including identifying, charting, or relying upon additional prior art references, relevant disclosures, and bases for Invalidity Contentions. Additional prior art and disclosures, whether or not cited in this disclosure and whether known or not known to Defendant, may become relevant as investigation, analysis, and discovery continue. Defendant incorporates by reference, and intend to rely on, each reference, disclosure, or argument served in any prior or concurrent matter involving the same patents but not yet produced to Defendant by Plaintiff.

Additionally, because fact discovery has not yet commenced, Defendant reserves the right to present additional prior art references or disclosures under 35 U.S.C. §§ 102(a), (b), (e), (f), or (g), or § 103, located during the course of discovery or further investigation, and to assert invalidity

under 35 U.S.C. §§ 102(c), (d), or (f), if future discovery or investigation yields information that supports additional bases of invalidity.

1. Incorporation of IPRs and Prior Invalidity Contentions

Defendant hereby incorporates by reference, as if fully set forth herein, the following IPRs concerning the Asserted Patents (collectively, the "Asserted Patent IPRs"):

IPR Proceeding Caption	Asserted Patent No.
Samsung Display Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00505 (PTAB)	U.S. Patent No. 7,414,682
Samsung Display Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00504 (PTAB)	U.S. Patent No. 7,583,347
BOE Technology Group Co., Ltd. v. Bishop Display Tech LLC, IPR2025-01330 (PTAB)	U.S. Patent No. 7,995,047
Samsung Electronics Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00501 (PTAB)	U.S. Patent No. 7,995,047
Samsung Electronics Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00503 (PTAB)	U.S. Patent No. 8,093,830
BOE Technology Group Co., Ltd. v. Bishop Display Tech LLC, IPR2025-01331 (PTAB)	U.S. Patent No. 8,093,830
Samsung Display Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00507 (PTAB)	U.S. Patent No. 6,525,798
Samsung Display Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00508 (PTAB)	U.S. Patent No. 6,787,829
Samsung Display Co., Ltd. v. Bishop Display Tech LLC, IPR2022-00564 (PTAB)	U.S. Patent No. 6,906,769

The Asserted Patent IPRs also includes any forthcoming materials submitted in these IPRs, and any other IPRs, reexaminations, foreign patent office proceedings, International Search Reports, or foreign opposition proceedings related to the Asserted Patents or any family members thereof.

Defendant also incorporates by reference, as if fully set forth herein, all prior and future invalidity contentions served by Defendant or any other party, including without limitation the invalidity contentions served by the following parties in the following litigations (collectively, "Other Invalidity Contentions"):

Case Caption
Bishop Display Tech LLC v. LG Electronics Inc., No. 2:24-cv-00084 (E.D. Tex.)
Bishop Display Tech LLC v. LG Electronics Inc., No. 2:24-cv-00085 (E.D. Tex.)
Bishop Display Tech LLC v. Heesung Electronics Ltd., No. 2:24-cv-00086 (E.D. Tex.)
Bishop Display Tech LLC v. Heesung Electronics Ltd., No. 2:24-cv-00087 (E.D. Tex.)
Bishop Display Tech LLC v. Innolux Corporation, No. 2:22-cv-00385 (E.D. Tex.)
Bishop Display Tech LLC v. Innolux Corporation, No. 2:22-cv-00384 (E.D. Tex.)
Bishop Display LLC v. Samsung Electronics Co., Ltd., No. 2:21-cv-00136 (E.D. Tex.)
Bishop Display LLC v. Samsung Electronics Co., Ltd., No. 2:21-cv-00136 (E.D. Tex.)

Other Invalidity Contentions also includes any forthcoming materials served or filed in any other prior or future proceeding concerning the Asserted Patents.

II. INVALIDITY CONTENTIONS—P.R. 3-3

A. Identity of Each Item of Prior Art—P.R. 3-3(a)

Under P.R. 3-3(a), and subject to Defendant's reservation of rights as articulated above, Defendant identifies each item of prior art that anticipates or renders obvious one or more of the Asserted Claims in the attached Prior Art Index submitted herewith. *See* Section V below. For references listed in Section V that are not identified as items of prior art that anticipate or render obvious an Asserted Claim, Defendant intends to rely on these references as *inter alia* background and evidence of the state of the art at the time of Plaintiff's alleged inventions and the level of skill and knowledge of a person of ordinary skill in the art at that time. *See Koninklijke Philips N.V. v.*

Google LLC, 948 F. 3d 1330, 1347 (Fed. Cir. 2020) ("Regardless of the tribunal, the inquiry into whether any 'differences' between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge.").

Additionally, the prior art references cited by Defendant includes references that are related patent applications and issued patents that contain substantially the same subject matter (*e.g.*, published U.S. patent applications, issued U.S. patents, foreign applications, or foreign issued patents). Any citation to or quotation from any of these patent applications or patents, therefore, encompasses any parallel citation to the same subject matter in other related or corresponding applications or patents. For example, where a claim chart cites a published patent application that ultimately issued as a patent with substantially the same written description, Defendant may rely upon the published patent application or the issued patent as prior art.

Defendant also reserves the right to later rely upon all references or portions of references provided in Section V to supplement or amend these disclosures. Defendant incorporates by reference (1) any and all prior art contained or identified in documents produced thus far by Plaintiff in this or any other proceeding, (2) any and all additional materials regarding or bearing upon invalidity in Plaintiff's possession or control that have not been produced to date, if any exist, and any and all prior art cited by or invalidity contentions served by Defendant in any prior case or concurrent case.

Each disclosed item of prior art describing a product, system, or other implementation made in the United States is evidence of a prior invention by another under 35 U.S.C. § 102(g), as evidenced by the named inventors, authors, organizations, and publishers involved with each of these references. Defendant further intends to rely on admissions of the named inventors concerning the prior art, including statements found in the Asserted Patents, their prosecution

histories, related patents or patent applications, any deposition testimony, and the papers filed and any evidence submitted by Plaintiff in conjunction with this litigation.

Defendant also incorporates by reference, as if fully set forth herein, the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions.

B. Whether Prior Art Anticipates or Renders Obvious—P.R. 3-3(b)

Pursuant to P.R. 3.3(b), and subject to Defendant's reservations of rights, Defendant identifies in the attached Exhibits A-01 through G-12 and J-01 through L19 prior art references that anticipate the Asserted Claims under at least one or more of 35 U.S.C. §§ 102(a), (b), (e), and (g), either expressly or inherently, and/or render obvious the Asserted Claims under 35 U.S.C. § 103 either alone or in combination with other references identified herein. Each Asserted Claim is anticipated by, or obvious in view of, one or more items of prior art identified in these disclosures, alone or in combination. A table identifying ways in which the prior art references cited herein anticipate or render obvious the Asserted Claims is provided in Section II. B. 2 below.

Much of the art identified in the attached Exhibits (i.e., claim charts) reflects common knowledge to persons of ordinary skill in the art and the state of the relevant art at the time of the earliest filing date of each Asserted Patent. Defendant may rely on additional citations, references, expert testimony, and other material to provide context or to aid in understanding the cited portions of the references or cited features of the systems. Defendant may also rely on expert testimony explaining relevant portions of references, relevant hardware or software products or systems, and other discovery regarding these subject matters. Additionally, Defendant may rely on other portions of any prior art reference for purposes of explaining the background and general technical subject area of the reference.

Where an individual reference is cited with respect to all limitations of an Asserted Claim, Defendant contends that the reference anticipates the claim under one or more of 35 U.S.C. §§

102(a), (b), (e), or (g) and also renders obvious the claim under 35 U.S.C. § 103, both by itself in view of the knowledge of a person of ordinary skill in the relevant art and in combination with the other cited references to the extent the reference is not found to disclose one or more claim limitations. A single prior art reference, for example, can establish obviousness where the differences between the disclosures within the reference and the claimed invention would have been obvious to one of ordinary skilled in the art. For example, "[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness." *Boston Scientific Scimed, Inc. v. Cordis Corp*., 554 F.3d 982, 991 (Fed. Cir. 2009). If Plaintiff contends that an embodiment within a particular item of prior art does not fully disclose all limitations of a claim, Defendant reserves the right to rely on other embodiments in that prior art reference, or other information, including, for example, to show single reference obviousness under 35 U.S.C. § 103(a).

Where an individual reference is cited with respect to fewer than all limitations of an Asserted Claim, Defendant contends that the reference renders obvious the claim under 35 U.S.C. § 103(a) by itself in view of the knowledge of a person of ordinary skill in the relevant art or in view of admitted prior art in the Asserted Patents and further in view of each other reference and combination of references that discloses the remaining claim limitation(s), as indicated in the claim charts submitted herewith. "Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined." *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 406 (2007) (quoting *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 (1966)). Exemplary motivations to combine references are discussed below in Section II. B. 3. Defendant reserves the

right to rely upon any references or assertions identified herein in connection with Defendant's contention that each Asserted Claim is invalid under 35 U.S.C. § 103 and to rely upon expert testimony addressing these references and assertions. The fact that prior art is identified to anticipate the Asserted Claims does not prevent Defendant from also relying on the same reference as rendering the Asserted Claims invalid as obvious. *Realtime Data, LLC v. Iancu*, 912 F. 3d 1368, 1373 ("anticipation is the epitome of obviousness"). If any cited prior art item does not fully disclose a limitation of an Asserted Claim or is alleged by Plaintiff to not disclose a limitation, the limitation is present and identified in another prior art item, or is admitted prior art by the Asserted Patents, as shown in the attached claim charts. In addition, the art in section V herein, whether charted or not, shows the "scope and content" under § 103 and the *Graham* factors.

Many of the cited references cite or relate to additional references or products, services, or projects. Many of the cited references also cite hardware or systems. Defendant may rely upon these cited additional references and copies or exemplars of the cited hardware or systems. Defendant will produce or make available for inspection any of these cited references, hardware, or systems that they intend to rely upon. Defendant may also rely upon the disclosures of the references cited or discussed during the prosecution of the Asserted Patents or the assertions presented by the inventor about those references.

Defendant also incorporates by reference, as if fully set forth herein, the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions, as well as the anticipation and obviousness arguments contained therein. Defendant also intends to rely upon the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions in combination with the prior art disclosed herein.

Defendant reserves the right to reduce the number of anticipation or obviousness references relied upon with respect to a given Asserted Claim and to exchange or otherwise modify the specific references relied upon for anticipation and within each obviousness combination for each Asserted Claim.

Discovery is at an early stage and Plaintiff has not provided any contentions or documentation with respect to any alleged pre-filing invention dates or with respect to claim limitations that are allegedly lacking in the prior art or not obvious over the prior art. Each limitation of the Asserted Claims was well known to those of ordinary skill in the art before the relevant priority date for each Asserted Claim, as detailed below.

1. Priority

Plaintiff's P.R. 3-1(e) disclosures allege that the claimed inventions are entitled to the following priority dates:

U.S. Patent No.	Priority Date
6,525,798	October 21, 1999
6,787,829	April 5, 2000
6,801,293	October 6, 1999
6,816,208	July 24, 2000
6,850,303	September 27, 2000
6,906,769	August 30, 2000
7,414,682	July 31, 2000
7,583,347	July 31, 2000
7,995,047	December 13, 2006
8,093,830	July 3, 2008

Defendant's analysis and selection of prior art is based on, and assumes *arguendo*, the above priority dates. Defendant notes that Bishop Display has provided no evidence to support its contentions that the Asserted Claims are entitled to claim priority back to these dates, a number of which rely on foreign application priority dates, and Defendant therefore reserves the right to argue that a later priority date is appropriate based on any findings as to the priority date of the Asserted

Claims by the Court, information learned through discovery, or otherwise. Should Bishop Display fail to establish that any Asserted Claim is entitled to the above priority dates or should Bishop Display improperly later assert a different invention or priority date, Defendant reserves the right to add additional prior art references to these Invalidity Contentions.

2. Application of the Prior Art to the Claims

The charts below identify references or exemplary combinations of references that either anticipate or render obvious the Asserted Claims. The discussion below sets forth rationales and motivations for combining the respective references with respect to the claimed features they disclose. For each of the Asserted Patents, Defendant may rely on "admitted prior art," which include statements in the specification or during prosecution identifying the work of others as "prior art" are admissions that can be relied on for anticipation and obviousness purposes. *See Riverwood Int'l Corp. v. R. A. Jones & Co.,* 324 F. 3d 1346, 1354 (Fed. Cir. 2003).

	Asserted Claims of the '798 Patent				
Prior Art	**1**	**2**	**4**	**5**	**6**
JP H07-128683 ("Fujii") (102/103)	**X**	**X**	**X**	**X**	**X**
US 6,337,726 ("Kawano") (102/103)	**X**	**X**	**X**	**X**	**X**
WO 98/47044 ("Ohta '044") (102/103)	**X**	**X**	**X**	**X**	**X**
WO 98/27454 ("Ohta '454") (102/103)	**X**	**X**	**X**	**X**	**X**
JP H09-073101 ("Ohta '101") (102/103)	**X**	**X**	**X**	**X**	**X**
US 5,886,762 ("Lee") (102/103)	**X**	**X**	**X**	**X**	**X**
US 6,452,656 ("Niwano") (102/103)	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii	**X**	**X**	**X**	**X**	**X**
Ohta '044 + Kawano	**X**	**X**	**X**	**X**	**X**
Ohta '454 + Kawano	**X**	**X**	**X**	**X**	**X**
Ohta '101 + Kawano	**X**	**X**	**X**	**X**	**X**
Product prior art (102/103)	**X**	**X**	**X**	**X**	**X**
JP H1-130784 ("Aratani") (102/103)	**X**	**X**	**X**	**X**	**X**
JP H0-829812A ("Satou") (102/103)	**X**	**X**	**X**	**X**	**X**
US5499123A ("Mikoshiba") (102/103)	**X**	**X**	**X**	**X**	**X**
Ohta '454 + Mikoshiba	**X**	**X**	**X**	**X**	**X**
Aratani + Satou	**X**	**X**	**X**	**X**	**X**
Fujii + Kawano + US 6,400,440 ("Colgan") + US 5,745,207 ("Asada")	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’798 Patent				
Prior Art	**1**	**2**	**4**	**5**	**6**
Fujii + Kawano + Colgan + US 6,266,116 (“Ohta ’116”)	**X**	**X**	**X**	**X**	**X**
Fujii + Kawano + Colgan + US 6,288,763 (“Hirota”)	**X**	**X**	**X**	**X**	**X**
Fujii + Kawano + Colgan + US 6,342,937 (“Hiroshi”)	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii+ Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Ohta ’044 + Kawano + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Ohta ’044 + Kawano + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Ohta ’044 + Kawano + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Ohta ’044 + Kawano + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Ohta ’454 + Kawano + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Ohta ’454 + Kawano + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Ohta ’454 + Kawano + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Ohta ’454 + Kawano + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Kawano + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Kawano + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Kawano + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Kawano + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Niwano + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Niwano + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Niwano + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Niwano + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Lee + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Lee + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Lee + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Lee + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Aratani + Colgan + Asada	**X**	**X**	**X**	**X**	**X**
Aratani + Colgan + Ohta ’116	**X**	**X**	**X**	**X**	**X**
Aratani + Colgan + Hirota	**X**	**X**	**X**	**X**	**X**
Aratani + Colgan + Hiroshi	**X**	**X**	**X**	**X**	**X**
Fujii + Kawano, Ohta ’044, Ohta ’454, Ohta ’101, Lee, Niwano, Prior Art Products, Aratani, Satou, Colgan, US 5,434,690 (“Hisatake”), Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Kawano + Fujii, Ohta ’044, Ohta ’454, Ohta ’101, Lee, Niwano, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’798 Patent				
Prior Art	**1**	**2**	**4**	**5**	**6**
Ohta ’044 + Fujii, Kawano, Ohta ’454, Ohta ’101, Lee, Niwano, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Ohta ’454 + Fujii, Kawano, Ohta ’044, Ohta ’101, Lee, Niwano, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Fujii, Kawano, Ohta ’044, Ohta ’454, Lee, Niwano, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Lee + Fujii, Kawano, Ohta ’044, Ohta ’454, Ohta ’101, Niwano, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Niwano + Fujii, Kawano, Ohta ’044, Ohta ’454, Ohta ’101, Lee, Prior Art Products, Aratani, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Aratani + Fujii, Kawano, Ohta ’044, Ohta ’454, Ohta ’101, Lee, Niwano, Product Prior Art, Satou, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**
Satou + Fujii, Kawano, Ohta ’044, Ohta ’454, Ohta ’101, Lee, Niwano, Product Prior Art, Aratani, Colgan, Hisatake, Asada, Ohta ’116, Hirota, Hiroshi, and/or Mikoshiba	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’829 Patent									
Prior Art	**1**	**2**	**5**	**6**	**10**	**11**	**18**	**19**	**29**	**30**
US 6,337,726 (“Kawano”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
WO 98/27454 (“Ohta ’454”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 6,452,656 (“Niwano”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 5,995,187 (“Wakagi”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
JP H09-073101 (“Ohta ’101”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 6,222,599 (“Yoshida”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Niwano + Kawano	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Niwano + Ohta ’454	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Niwano + Ohta ’101	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Niwano + Wakagi	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Yoshida + Kawano	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Yoshida + Ohta ’454	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’829 Patent									
Prior Art	**1**	**2**	**5**	**6**	**10**	**11**	**18**	**19**	**29**	**30**
Yoshida + Ohta ’101	X	X	X	X	X	X	X	X	X	X
Yoshida + Wakagi	X	X	X	X	X	X	X	X	X	X
Product prior art (102/103)	X	X	X	X	X	X	X	X	X	X
Kawano + US 5,907,379 (“Kim”)	X	X	X	X	X	X	X	X	X	X
Ohta 454 + Kim	X	X	X	X	X	X	X	X	X	X
Niwano + Kim	X	X	X	X	X	X	X	X	X	X
Yoshida + Kim	X	X	X	X	X	X	X	X	X	X
Wakagi + Kim	X	X	X	X	X	X	X	X	X	X
Ohta 101 + Kim	X	X	X	X	X	X	X	X	X	X
Kawano + JP H11-174490 (“Jun”)	X	X	X	X	X	X	X	X	X	X
Ohta 454 + Jun	X	X	X	X	X	X	X	X	X	X
Niwano + Jun	X	X	X	X	X	X	X	X	X	X
Yoshida + Jun	X	X	X	X	X	X	X	X	X	X
Wakagi + Jun	X	X	X	X	X	X	X	X	X	X
Ohta 101 + Jun	X	X	X	X	X	X	X	X	X	X
Niwano + Kawano + Kim	X	X	X	X	X	X	X	X	X	X
Niwano + Ohta ’454 + Kim	X	X	X	X	X	X	X	X	X	X
Niwano + Ohta ’101 + Kim	X	X	X	X	X	X	X	X	X	X
Niwano + Wakagi + Kim	X	X	X	X	X	X	X	X	X	X
Yoshida + Kawano + Kim	X	X	X	X	X	X	X	X	X	X
Yoshida + Ohta ’454 + Kim	X	X	X	X	X	X	X	X	X	X
Yoshida + Ohta ’101 + Kim	X	X	X	X	X	X	X	X	X	X
Yoshida + Wakagi+ Kim	X	X	X	X	X	X	X	X	X	X
Kawano + Ohta ’454, Niwano, Yoshida, Wakagi, Ohta ’101, Prior Art Products, Kim, US 5,723,878 (“Yanai”), US 6,532,053 (“Ohta ’053”), Jun, JP H11-352514 (“Yamada”), and/or JP H04-104227 (“Matsui”).	X	X	X	X	X	X	X	X	X	X
Ohta ’454 + Kawano, Niwano, Yoshida, Wakagi, Ohta ’101, Prior Art Products, Kim, Yanai, Ohta ’053, Jun, Yamada, and/or Matsui.	X	X	X	X	X	X	X	X	X	X
Niwano + Kawano, Ohta ’454, Yoshida, Wakagi, Ohta ’101, Prior Art Products, Kim, Yanai, Ohta ’053, Jun, Yamada, and/or Matsui.	X	X	X	X	X	X	X	X	X	X
Yoshida + Kawano, Ohta ’454, Niwano, Wakagi, Ohta ’101, Prior Art Products, Kim, Yanai, Ohta ’053, Jun, Yamada, and/or Matsui.	X	X	X	X	X	X	X	X	X	X

	Asserted Claims of the ’829 Patent									
Prior Art	**1**	**2**	**5**	**6**	**10**	**11**	**18**	**19**	**29**	**30**
Wakagi + Kawano, Ohta, Niwano, Yoshida, Ohta ’101, Prior Art Products, Kim, Yanai, Ohta ’053, Jun, Yamada, and/or Matsui.	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Ohta ’101 + Kawano, Ohta ’454, Niwano, Yoshida, Wakagi, Prior Art Products, Kim, Yanai, Ohta ’053, Jun, Yamada, and/or Matsui.	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’293 Patent
Prior Art	**1**
US 5,949,509 (“Ohe”) (102/103)	**X**
JPH9-274190 (“Nishikawa 1997”) (102/103)	**X**
JPH7-248478 (“Hideaki”) (102/103)	**X**
Product prior art (102/103)	**X**
JPH10-213802 (“Tsumura”) (102/103)	**X**
JPH0-588180 (“Sawatsubashi”) (102/103)	**X**
JPH5-142542 (“Ichikawa”) (102/103)	**X**
JPH11-202334 (“Yamada”) (102/103)	**X**
US 6,341,003 (“Ashizawa”) (102/103)	**X**
US 6,839,113 (“Watanabe”) (102/103)	**X**
JPH10-148834 (“Minhara”) (102/103)	**X**
JPH0996818A (“Mori”)	**X**
Ohe + Nishikawa	**X**
Ashizawa + Nishikawa	**X**
Minhara + Nishikawa	**X**
Mori + Nishikawa	**X**
Ashizawa + Tsumura	**X**
Watanabe + Tsumura	**X**
Watanabe + Tsumura and Yamada	**X**
Ohe + Tsumura	**X**
Minhara + Tsumura	**X**
Mori + Tsumara	**X**
Ohe + Minhara	**X**
Ohe + Mori	**X**
Ashizawa + Minhara	**X**
Ashizawa + Mori	**X**
Wantanabe + Minhara	**X**
Wantanabe + Mori	**X**
Ashizawa + Tsumura, Sawatsubashi, Ichikawa, Minhara, Mori, and/or Product prior art	**X**

	Asserted Claims of the ’293 Patent
Prior Art	**1**
Watanabe + Tsumura, Yamada, Ichikawa, Sawatsubashi, Minhara, Mori, and/or Product prior art	**X**
Ohe + Tsumura, Sawatsubashi, Ichikawa, Minhara, Mori, and/or Product prior art	**X**
Nishikawa 1997 + Tsumura, Sawatsubashi, Ichikawa, Minhara, Mori, and/or Product prior art	**X**
Hideaki + Tsumura, Sawatsubashi, Ichikawa, Minhara, Mori and/or Product prior art	**X**
Minhara + Tsumura, Sawatsubashi, Yamada, Ichikawa, and/or Product prior art	**X**
Mori + Tsumura, Sawatsubashi, Yamada, Ichikawa, and/or Product prior art	**X**

	Asserted Claims of the ’208 Patent	
Prior Art	**1**	**3**
US 6,028,650 (“Kuroha”) (102/103)	**X**	**X**
JPH05-232509 (“Nishikawa 1993”) (102/103)	**X**	**X**
US 6,020,214 (“Watanabe ’214”) (102/103)	**X**	**X**
KR2000-0003113 (“Yoo”) (102/103)	**X**	**X**
JPH07-029535 (“Yamada 1995”) (102/103)	**X**	**X**
JP2000-56322 (“Yamada 2000”) (102/103)	**X**	**X**
US 5,459,596 (“Ueda”) (102/103)	**X**	**X**
Ueda + US 6,249,325 (“Ohkawara”)	**X**	**X**
Ueda + Yoo	**X**	**X**
Ueda + Yamada 1995	**X**	**X**
Ueda + Yamada 2000	**X**	**X**
Kuroha + Yoo	**X**	**X**
Kuroha + Yamada 1995	**X**	**X**
Kuroha + Yamada 2000	**X**	**X**
Nishikawa 1993 + Yoo	**X**	**X**
Nishikawa 1993 + Yamada 1995	**X**	**X**
Nishikawa 1993 + Yamada 2000	**X**	**X**
Watanabe ’214 + Yoo	**X**	**X**
Watanabe ’214 + Yamada 1995	**X**	**X**
Watanabe ’214 + Yamada 2000	**X**	**X**
Yoo + Yamada 1995	**X**	**X**
Yoo + Yamada 2000	**X**	**X**
Product prior art (102/103)	**X**	**X**
Kuroha in view of Watanabe ’214, Nishikawa 1993, Yamada 1995, Yamada 2000, Yoo and/or Ueda	**X**	**X**

	Asserted Claims of the ’208 Patent	
Prior Art	**1**	**3**
Watanabe ’214 in view of Kuroha, Nishikawa 1993, Yamada 1995, Yamada 2000, Yoo and/or Ueda	**X**	**X**
Nishikawa 1993 in view of Watanabe ’214, Kuroha, Yamada 1995, Yamada 2000, Yoo and/or Ueda	**X**	**X**
Yamada 1995 in view of Watanabe ’214, Kuroha, Nishikawa 1993, Yamada 2000, Yoo and/or Ueda	**X**	**X**
Yamada 2000 in view of Watanabe ’214, Kuroha, Nishikawa 1993, Yamada 1995, Yoo and/or Ueda	**X**	**X**
Yoo in view of Watanabe ’214, Kuroha, Nishikawa 1993, Yamada 2000, Yamada 1995 and/or Ueda	**X**	**X**
Ueda in view of Watanabe ’214, Kuroha, Nishikawa 1993, Yamada	**X**	**X**
2000, Yamada 1995 and/or Yoo		

	Asserted Claims of the ’303 Patent	
Prior Art	**1**	**4**
JP H09-236820 (“Nakagawa”) (102/103)	**X**	**X**
JP P2000-98420 (“Iizuka”) (102/103)	**X**	**X**
US 6,812,975 (“Nagahiro”) (102/103)	**X**	**X**
US 5,182,661 (“Ikeda”) (102/103)	**X**	**X**
US 5,852,485 (“Shimada”) + Iizuka	**X**	**X**
JP3096394 (“Fujiwara")	**X**	**X**
Shimada + Nagahiro	**X**	**X**
Shimada + Ikeda	**X**	**X**
Nakagawa + Iizuka	**X**	**X**
Nakagawa + Nagahiro	**X**	**X**
Nakagawa + Ikeda	**X**	**X**
Fujiwara + Nagahiro	**X**	**X**
Fujiwara + Ikeda	**X**	**X**
Fujiwara + Iizuka	**X**	**X**
Product prior art (102/103)	**X**	**X**
US 6,335,770 (“Komatsu”) (102/103)	**X**	**X**
EP 1,037,093 (“Tanaka”) (102/103)	**X**	**X**
US 6,590,227 (“Ishikawa”) (102/103)	**X**	**X**
US 6,281,957 (“Young”) (102/103)	**X**	**X**
US 6,771,342 (“Hirakata”) (102/103)	**X**	**X**
US 6,445,435 (“Seo”) (102/103)	**X**	**X**
US 6,259,502 (“Komatsu ’502”) (102/103)	**X**	**X**

	Asserted Claims of the ’303 Patent	
Prior Art	**1**	**4**
Komatsu + Ishikawa	**X**	**X**
Komatsu + Tanaka	**X**	**X**
Hirakata + Tanaka	**X**	**X**
Seo + Tanaka	**X**	**X**
Komatsu + Tanaka	**X**	**X**
Komatsu + Young	**X**	**X**
Young + Tanaka	**X**	**X**
Young + Nagahiro	**X**	**X**
Fujiwara + Tanaka	**X**	**X**
Fujiwara + Nagahiro	**X**	**X**
KR0144233 (“Lee”) (102/103)	**X**	**X**
KR2000-0009305 (“Kim”) (102/103)	**X**	**X**
US 5,734,448 (“Cheng”) (102/103)	**X**	**X**
US 5,923,390 (“Mok”) (102/103)	**X**	**X**
US 6,326,641 (“Choi”) (102/103)	**X**	**X**
US 2003/0071930 Al (“Nagahiro ’930”) (102/103)	**X**	**X**
Nakagawa + Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Iizuka + Nakagawa, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Nagahiro + Nakagawa, Iizuka, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Shimada + Nakagawa, Iizuka, Nagahiro, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Ikeda + Nakagawa, Iizuka, Nagahiro, Shimada, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**

	Asserted Claims of the ’303 Patent	
Prior Art	**1**	**4**
Komatsu + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Tanaka + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Ishikawa + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Oh + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Hirakata + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Seo + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Komatsu ’502 + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Lee, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Lee + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Kim, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**

	Asserted Claims of the ’303 Patent	
Prior Art	**1**	**4**
Kim + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Cheng, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Cheng + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Mok, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Mok + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Choi, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Choi + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu, Lee, Kim, Cheng, Mok, Nagahiro ’930, and/or Fujiwara	**X**	**X**
Nagahiro ’930 + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, and/or Fujiwara	**X**	**X**
Fujiwara + Nakagawa, Iizuka, Nagahiro, Shimada, Ikeda, Product Prior Art, Komatsu, Tanaka, Ishikawa, Oh, Hirakata, Seo, Komatsu ’502, Lee, Kim, Cheng, Mok, Choi, and/or Nagahiro ’930	**X**	**X**

	Asserted Claims of the ’769 Patent						
Prior Art	**1**	**4**	**5**	**6**	**7**	**9**	**14**
US 6,335,770 (“Komatsu”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
JPH8-95075 (“Shimada”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
JP H10-186407 (“SakamotoJP407”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 6,069,678 (“SakamotoUS678”)	**X**	**X**	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’769 Patent						
Prior Art	**1**	**4**	**5**	**6**	**7**	**9**	**14**
JPH9-96794 (“Watanabe JP ’794”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 4,909,602 (“Kaneko”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
US 6,005,543 (“Kimura”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
JPH6-202127 to Ota (“OtaJP127”) (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Watanabe JP ’794	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kaneko	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Shimada + Watanabe JP ’794	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Shimada + Kaneko	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Shimada + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Shimada + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoJP407 + Watanabe JP ’794	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoJP407 + Kaneko	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoJP407 + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoJP407 + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoUS678 + Kaneko	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoUS678 + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoUS678 + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Watanabe JP ’794 + Kaneko	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Watanabe JP ’794 + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Watanabe JP ’794 + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kaneko + SakamotoUS678/ SakamotoJP407	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kaneko + Shimada	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kaneko + Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Komatsu + Kaneko + OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Product prior art (102/103)	**X**	**X**	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’769 Patent						
Prior Art	**1**	**4**	**5**	**6**	**7**	**9**	**14**
Komatsu in view of Kaneko, Shimada, SakamotoJP407, SakamotoUS678, Watanabe, Kimura, and/or OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Shimada in view of Kaneko, Komatsu, SakamotoJP407, SakamotoUS678, Watanabe, Kimura, and/or OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
SakamotoJP407 in view of Kaneko, Komatsu, Shimada, SakamotoUS678, Watanabe, Kimura, and/or OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Sakamoto US678 in view of Kaneko, Komatsu, Shimada, Sakamoto JP407, Watanabe, Kimura, and/or OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
Kimura in view of Kaneko, Komatsu, Shimada, Sakamoto JP407, Watanabe, Sakamoto US678, and/or OtaJP127	**X**	**X**	**X**	**X**	**X**	**X**	**X**
OtaJP127 in view of Kaneko, Komatsu, Shimada, Sakamoto JP407, Watanabe, Sakamoto US678, and/or Kimura	**X**	**X**	**X**	**X**	**X**	**X**	**X**

	Asserted Claims of the ’682 Patent	
Prior Art	**7**	**9**
JPH09-269508 (“Matsumoto”) (102/103)	**X**	**X**
WO98/27454 (“Ohta ’454”) (102/103)	**X**	**X**
JP2000-98404 (“Kubota”) (102/103)	**X**	
US 5,907,379 (“Kim”) (103)	**X**	**X**
JPH10-301141 (“Asada”) (103)	**X**	**X**

	Asserted Claims of the ’682 Patent	
Prior Art	**7**	**9**
Kubota + Matsumoto	**X**	**X**
Kubota + Ohta ’454	**X**	**X**
Kubota + Kim	**X**	**X**
Kubota + Asada	**X**	**X**
WO1999045430A1 (“Ota5430”)	**X**	**X**
Kubota + Ota5430	**X**	**X**
US 6,563,561 (“Ota561”) (103)	**X**	**X**
Kubtota + Ota561	**X**	**X**
Kim + Matsumoto	**X**	**X**
Kim + Ohta ’454	**X**	**X**
Asada + Matsumoto	**X**	**X**
Asada + Ohta ’454	**X**	**X**
US 6,452,656 (“Niwano”) (103)	**X**	**X**
US 5,969,782 (“Seung Hee Lee”) (103)	**X**	**X**
Niwano + Matsumoto	**X**	**X**
Niwano + Ohta ’454	**X**	**X**
Niwano + Kubota	**X**	**X**
Seung Hee Lee + Matsumoto	**X**	**X**
Seung Hee Lee + Ohta ’454	**X**	**X**
Seung Hee Lee + Kubota	**X**	**X**
Product prior art (102/103)	**X**	**X**
US 5,852,485 (“Shimada”) (102/103)	**X**	**X**
JPH07199169A (“Yamaji”) (102/103)	**X**	**X**
Kubota + Yamaji	**X**	**X**
Shimada + Yamaji	**X**	**X**
Shimada + Ota561	**X**	**X**
Matsumoto + Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Ohta ’454 + Matsumoto, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**

	Asserted Claims of the ’682 Patent	
Prior Art	**7**	**9**
Kubota + Matsumoto, Ohta ’454, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Kim + Matsumoto, Ohta ’454, Kubota, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Asada + Matsumoto, Ohta ’454, Kubota, Kim, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Niwano + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Seung Hee Lee + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Prior Art Products, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Prior Art Products + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Ota5430, Yamaji, Ota561, and/or Shimada	**X**	**X**
Ota5430 + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Yamaji, Ota561, and/or Shimada	**X**	**X**
Yamaji + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Ota561, and/or Shimada	**X**	**X**

	Asserted Claims of the ’682 Patent	
Prior Art	**7**	**9**
Ota561 + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, and/or Shimada	**X**	**X**
Shimada + Matsumoto, Ohta ’454, Kubota, Kim, Asada, Niwano, Seung Hee Lee, Prior Art Products, Ota5430, Yamaji, and/or Ota561	**X**	**X**

	Asserted Claims of the ’347 Patent
Prior Art	**1**
US 5,949,509 (“Ohe”) (102/103)	**X**
WO98/27454 (“Ohta ’454”) (102/103)	**X**
US 6,351,300 (“Park”) (102/103)	**X**
JPH10-301141 (“Asada”) (103)	**X**
Asada + Ohe	**X**
Asada + Ohta ’454	**X**
Asada + Park	**X**
Asada + JPH09-269508 (“Matsumoto”) + JPH10-170916 (“Hiyama”)	**X**
Asada + Matsumoto + SID Seminar Note (May 14, 2000) (“Sang Soo Kim”)	**X**
US 6,452,656 (“Niwano”) (103)	**X**
US 5,969,782 (“Seung Hee Lee”) (103)	**X**
Niwano + Hiyama	**X**
Niwano + Sang Soo Kim	**X**
Seung Hee Lee + Hiyama	**X**
Seung Hee Lee + Sang Soo Kim	**X**
Product prior art (102/103)	**X**
KR100341123B1 (“Lee”) (102/103)	**X**
JP2000091592A (“Yamazaki”) (102/103)	**X**
US 5,995,187 (“Wakagi”)	**X**
US 5,978,059 (“Ohta059”)	**X**
KR19990088122A (“Ashizawa”)	**X**
Wakagi + Ohta059	**X**
Asada + Lee	**X**
Asada + Yamazaki	**X**
Asada + Wakagi	**X**
Wakagi + Lee	**X**
Asada + Wakagi + Ohta059	**X**

	Asserted Claims of the ’347 Patent
Prior Art	**1**
Ohe + Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Ohta ’454 + Ohe, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Park + Ohe, Ohta ’454, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Asada + Ohe, Ohta ’454, Park, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Matsumoto + Ohe, Ohta ’454, Park, Asada, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Hiyama + Ohe, Ohta ’454, Park, Asada, Matsumoto, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Sang Soo Kim + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Niwano + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Seung Hee Lee + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Prior Art Products, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Prior Art Products + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Lee, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**
Lee + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Yamazaki, Wakagi, Ohta059, and/or Ashizawa	**X**

	Asserted Claims of the ’347 Patent
Prior Art	**1**
Yamazaki + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Wakagi, Ohta059, and/or Ashizawa	**X**
Wakagi + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Ohta059, and/or Ashizawa	**X**
Ohta059 + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, and/or Ashizawa	**X**
Ashizawa + Ohe, Ohta ’454, Park, Asada, Matsumoto, Hiyama, Sang Soo Kim, Niwano, Seung Hee Lee, Prior Art Products, Lee, Yamazaki, Wakagi, and/or Ohta059	**X**

	Asserted Claims of the ’047 Patent
Prior Art	**1**
Prior Art admitted in the specification of the ’047 Patent (’047 APA)	**X**
US 7,760,161 or USP 2005/0017765 (“Sasaki”) (102/103)	**X**
US 6,870,192 (“Yamazaki”) (102/103)	**X**
US 7,760,163 or USP 2006/0158396 (“Jo”) (102/103)	**X**
US 7,268,717 or USP 2006/0170629 (“Baek”) (102/103)	**X**
US 7,859,489 (“Furuichi”) (102/103)	**X**
US 7,679,586 (“Stewart”) (102/103)	**X**
US 7,304,621 or US 2004/0201556 (“Oomori”) (102/103)	**X**
US 7,626,565 or US 2006/023612 (“Tsuge”) (102/103)	**X**
US 8,044,892 OR US 2006/0118700 (“Chaussy”) (102/103)	**X**
US 7,397,449 OR US 2005/0140601 (“Kasai”) (102/103)	**X**
US 8,325,111 or USP 2007/0126664 (“Kimura”) (102/103)	**X**

	Asserted Claims of the ’047 Patent
Prior Art	**1**
Jane Woo Ryu, “A Design of AM-OLED Source Driver with reduced Programming Time for a Large Scale Display Panel” (“Ryu”) (102/103)	**X**
M. Shimoda, “An integrated poly-Si TFT current data driver with a data-line pre-charge function. Journal of the Society for Information Display” (“Shimoda”) (102/103)	**X**
J.H. Baek, “A Current- Mode Display Driver IC Using Sample-and-Hold Scheme for QVGA Full- Color AMOLED Displays” (“Baek Dec. Publication”) (102/103)	**X**
M. Liu, “A Single Driver Chip for Gray Scale Passive-Matrix OLED” (“Liu”) (102/103)	**X**
S. Alexander, “Pixel circuits and drive schemes for glass and elastic AMOLED displays” (“Alexander”) (102/103)	**X**
J.H. Baek, “A Current Driver IC using a S/H for QVGA Full-Color Active- Matrix Organic LED Mobile Displays” (“Baek Feb. Publication”) (102/103)	**X**
’047 APA + Baek	**X**
’047 APA + Ryu	**X**
’047 APA + Kimura	**X**
’047 APA + Shimoda	**X**
’047 APA + Liu	**X**
’047 APA + Alexander	**X**
Shimoda + Jo	**X**
Shimoda + Sasaki	**X**
Shimoda + Kasai	**X**
Shimoda + Oomori	**X**
Baek + Jo	**X**
Baek + Sasaki	**X**
Baek + Kasai	**X**
Baek + Oomori	**X**
Ryu + Jo	**X**
Ryu + Sasaki	**X**
Ryu + Kasai	**X**
Ryu + Oomori	**X**
Kimura + Jo	**X**
Kimura + Sasaki	**X**
Kimura + Kasai	**X**
Kimura + Oomori	**X**

	Asserted Claims of the ’047 Patent
Prior Art	**1**
Liu + Jo	**X**
Liu + Sasaki	**X**
Liu + Kasai	**X**
Liu + Oomori	**X**
Alexander + Jo	**X**
Alexander + Sasaki	**X**
Alexander + Kasai	**X**
Alexander + Oomori	**X**
Baek Dec. Publication + Jo	**X**
Baek Dec. Publication + Sasaki	**X**
Baek Dec. Publication + Kasai	**X**
Baek Dec. Publication + Oomori	**X**
Baek Dec. Publication + Baek Feb. Publication + Jo	**X**
Baek Dec. Publication + Baek Feb. Publication + Sasaki	**X**
Baek Dec. Publication + Baek Feb. Publication + Kasai	**X**
Baek Dec. Publication + Baek Feb. Publication + Oomori	**X**
Prior Art Products (102/103)	**X**
Sasaki + Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Yamazaki + Sasaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Jo + Sasaki, Yamazaki, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Baek + Sasaki, Yamazaki, Jo, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**

	Asserted Claims of the ’047 Patent
Prior Art	**1**
Furuichi + Sasaki, Yamazaki, Jo, Baek, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Stewart + Sasaki, Yamazaki, Jo, Baek, Furuichi, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Oomori + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Tsuge + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Chaussy + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Kasai + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Kimura + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Ryu + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Shimoda, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**

	Asserted Claims of the ’047 Patent
Prior Art	**1**
Shimoda + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Baek Dec. Publication, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Baek Dec. Publication + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Liu, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Liu + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Alexander, Baek Feb. Publication, and/or Prior Art Products	**X**
Alexander + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Baek Feb. Publication, and/or Prior Art Products	**X**
Baek Feb. Publication + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, and/or Prior Art Products	**X**
Prior Art Products + Sasaki, Yamazaki, Jo, Baek, Furuichi, Stewart, Oomori, Tsuge, Chaussy, Kasai, Kimura, Ryu, Shimoda, Baek Dec. Publication, Liu, Alexander, and/or Baek Feb. Publication	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
Prior Art admitted in the specification of the ’830 Patent (“’830 APA”) (102/103)	**X**
US 7,262,559 (“Tripathi ’559”) (102/103)	**X**
US 7,332,699 (“Nishimura) (102/103)	**X**
US 7,202,608 (“Robinson”) (102/103)	**X**
JP 2006-210271 (“Nagase”) (102/103)	**X**
WO 2005/079121 (“Bhagat”) (102/103)	**X**
JP 2006-303093 (“Matsuda”) (102/103)	**X**
US 6,577,512 (“Tripathi 512”) (102/103)	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
US 7,391,335 or USP 2007/0040696 (“Mubaslat”) (102/103)	**X**
US 7,276,861 (“Shteynberg”) (102/103)	**X**
US 8,242,787 (“Hente”) (102/103)	**X**
US 6,285,139 (“Ghanem”) (102/103)	**X**
US 8,111,014 or WO2008/001246 (“Van Erp”) (102/103)	**X**
US 7,492,108 or US 2007/0035538 (“Garcia”) (102/103)	**X**
US 6,747,420 (“Barth”) (102/103)	**X**
US 7,471,287 or USP 2008/0100234 (“Chen”) (102/103)	**X**
JP 2004-327152 (“Shimizu”) (102/103)	**X**
’830 Prior Art Products (102/103)	**X**
U.S. 2007/0170876 (“Ito”) (102/103)	**X**
’830 APA + Hente	**X**
’830 APA + Nishimura	**X**
’830 APA + Chen	**X**
’830 APA + Ito	
’830 APA + Hente + Shimizu	**X**
’830 APA + Nishimura + Shimizu	**X**
’830 APA + Chen + Shimizu	**X**
Shimizu + Hente	**X**
Shimizu + Hente + Barth	**X**
Shimizu + Nishimura	**X**
Shimizu + Nisimura + Barth	**X**
Shimizu + Chen	**X**
Shimizu + Chen + Barth	**X**
Shimizu + Ito	**X**
Shimizu + Ito + Barth	**X**
Shimizu + ’830 APA	**X**
Shimizu + ’830 APA + Ito	**X**
Tripathi ’559 + Hente	**X**
Tripathi ’559 + Hente + Barth	**X**
Tripathi ’559 + Nishimura	**X**
Tripathi ’559 + Nisimura + Barth	**X**
Tripathi ’559 + Chen	**X**
Tripathi ’559 + Chen + Barth	**X**
Tripathi 559 + Ito	**X**
Tripathi ’559 + Ito + Barth	**X**
Tripathi ’559 + ’830 APA	**X**
Tripathi ’559 + ’830 APA + Hente	**X**
Tripathi ’559 + ’830 APA + Nishimura	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
Tripathi ’559 + ’830 APA + Chen	**X**
Tripathi ’559 + ’830 APA + Ito	**X**
Tripathi ’559 + Nishimura	**X**
Tripathi ’512 + Hente	**X**
Tripathi ’512 + Hente + Barth	**X**
Tripathi ’512 + Nishimura	**X**
Tripathi ’512 + Nisimura + Barth	**X**
Tripathi ’512 + Chen	**X**
Tripathi ’512 + Chen + Barth	**X**
Tripathi ’512 + Ito	**X**
Tripathi ’512 + Ito + Barth	**X**
Tripathi ’512 + ’830 APA	**X**
Tripathi ’512 + ’830 APA + Hente	**X**
Tripathi ’512 + ’830 APA + Nishimura	**X**
Tripathi ’512 + ’830 APA + Chen	**X**
Tripathi ’512 + ’830 APA + Ito	**X**
Ghanem + Nishimura	
Bhagat + Hente	**X**
Bhagat + Hente + Barth	**X**
Bhagat + Nishimura	**X**
Bhagat + Nisimura + Barth	**X**
Bhagat + Chen	**X**
Bhagat + Chen + Barth	**X**
Bhagat + Ito	**X**
Bhagat + Ito + Barth	**X**
Bhagat + ’830 APA	**X**
Bhagat + ’830 APA + Hente	**X**
Bhagat + ’830 APA + Nishimura	**X**
Bhagat + ’830 APA + Chen	**X**
Bhagat + ’830 APA + Ito	**X**
Nagase + Hente	**X**
Nagase + Hente + Barth	**X**
Nagase + Nishimura	**X**
Nagase + Nisimura + Barth	**X**
Nagase + Chen	**X**
Nagase + Chen + Barth	**X**
Nagase + Ito	**X**
Nagase + Ito + Barth	**X**
Nagase + ’830 APA	**X**
Nagase + ’830 APA + Hente	**X**
Nagase + ’830 APA + Nishimura	**X**
Nagase + ’830 APA + Chen	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
Nagase + ’830 APA + Ito	**X**
Mubaslat + Hente	**X**
Mubaslat + Hente + Barth	**X**
Mubaslat + Nishimura	**X**
Mubaslat + Nisimura + Barth	**X**
Mubaslat + Chen	**X**
Mubaslat + Chen + Barth	**X**
Mubaslat + Ito	**X**
Mubaslat + Ito + Barth	**X**
Mubaslat + ’830 APA	**X**
Mubaslat + ’830 APA + Hente	**X**
Mubaslat + ’830 APA + Nishimura	**X**
Mubaslat + ’830 APA + Chen	**X**
Mubaslat + ’830 APA + Ito	**X**
Robinson + Hente	**X**
Robinson + Hente + Barth	**X**
Robinson + Nishimura	**X**
Robinson + Nisimura + Barth	**X**
Robinson + Chen	**X**
Robinson + Chen + Barth	**X**
Robinson + Ito	**X**
Robinson + Ito + Barth	**X**
Robinson + ’830 APA	**X**
Robinson + ’830 APA + Hente	**X**
Robinson + ’830 APA + Nishimura	**X**
Robinson + ’830 APA + Chen	**X**
Robinson + ’830 APA + Ito	**X**
’830 APA + Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Shimizu + ’830 APA, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Nishimura + ’830 APA, Shimizu, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
Hente + ’830 APA, Shimizu, Nishimura, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Chen + ’830 APA, Shimizu, Nishimura, Hente, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Tripathi ’559 + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Tripathi ’512 + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Bhagat + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Mubaslat + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Nagase + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Robinson + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**

	Asserted Claims of the ’830 Patent
Prior Art	**1**
Ghanem + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Matsuda, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Matsuda + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Shteynberg, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Shteynberg + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Van Erp, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Van Erp + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Barth, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Barth + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Garcia, ’830 Prior Art Products, and/or Ito	**X**
Garcia + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, ’830 Prior Art Products, and/or Ito	**X**
’830 Prior Art Products + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, and/or Ito	**X**
Ito + ’830 APA, Shimizu, Nishimura, Hente, Chen, Tripathi ’559, Tripathi ’512, Bhagat, Mubaslat, Nagase, Robinson, Ghanem, Matsuda, Shteynberg, Van Erp, Barth, Garcia, and/or ’830 Prior Art Products	**X**

Defendant also incorporates by reference, as if fully set forth herein, the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions, as well as the anticipation and

obviousness arguments contained therein. Defendant also intends to rely upon the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions in combination with the prior art disclosed herein.

3. Obviousness and Motivations to Combine

As shown in the prior art matrices above, each cited prior art reference may be combined with one or more other prior art references to render obvious the Asserted Claims in combination, as explained in more detail below. The disclosures of these references may also be combined with information known to persons skilled in the art at the time of the alleged inventions, and understood and supplemented in view of the common sense of persons skilled in the art at the time of the alleged inventions, including any statements in the intrinsic records of the Asserted Patents and related applications.

A person of ordinary skill would have been motivated to combine the prior art cited in the Exhibits based on the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. The identified prior art references for each of the Asserted Patents, including portions cited in attached Exhibits A-01 through G-12 and J-01 through L19 address the same or similar technical issues and suggest the same or similar solutions to those issues as the Asserted Claims. On such bases, on a limitation-by-limitation basis, Defendant expressly intends to combine one or more prior art items identified in the Exhibits with each other to address any further contention from Plaintiff that a particular prior art item supposedly lacks one or more limitations of an Asserted Claim. In other words, Defendant contends that each charted prior art item can be combined with other charted prior art items when a particular prior art item lacks or does not explicitly disclose a limitation or feature of an Asserted Claim. The suggested obviousness combinations described below are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, if Plaintiff

contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendant reserves the right to identify other prior art references that, when combined with the anticipatory prior art, would render the Asserted Claims obvious despite an allegedly missing limitation. Defendant will further specify the motivations to combine the prior art, including through reliance on expert testimony, at the appropriate later stage of this lawsuit.

A person of skill in the art would have been motivated to combine the identified prior art items. As the United States Supreme Court held in *KSR*, 550 U.S. at 416: "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." The Supreme Court further held that, "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id*. at 417.

The Supreme Court has further held that "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420. It is sufficient that a combination of limitations was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 421. "In that instance the fact that a combination was obvious to try might show that it was obvious under § 103." *Id*. Finally, the

Supreme Court recognized that "[g]ranting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known limitations, deprive prior inventions of their value or utility." *Id*. at 419. All of the following rationales recognized in *KSR* support a finding of obviousness with respect to each of the obviousness combinations disclosed herein:

(1) Combining prior art limitations according to known methods to yield predictable results;

(2) Simple substitution of one known limitation for another to obtain predictable results;

(3) Use of known technique to improve similar devices (methods, or products) in the same way;

(4) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(5) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(6) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

(7) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Certain of these rationales are discussed with greater specificity below, but all apply, and the lack of a more specific discussion of some should not be taken to imply or admit that others do

not also apply as the discussion below is intended to provide further explanation regarding certain of the specific rationales. As Plaintiff's positions regarding claim construction, specific prior art, specific combinations and/or the state of the art at the time of invention have not yet been disclosed, additional explanation regarding obviousness and/or motivation to combine specific references and knowledge may become relevant and appropriate. Accordingly, Defendant reserves the right to further identify and explain motivations to combine as the need arises based on positions taken by Plaintiff and/or rulings issued by the Court.

Defendant further contends that the prior art identified in these Invalidity Contentions is evidence of simultaneous or near-simultaneous independent invention by others of the alleged invention as recited in one or more of the Asserted Claims. Defendant reserves the right to rely on the simultaneous or near-simultaneous independent invention by others as further evidence of the obviousness of the Asserted Claims.

Each limitation of the Asserted Claims was well known to those of ordinary skill in the art before the priority date, as detailed below. The limitations recited in the Asserted Claims are mere combinations and modifications of these well-known limitations. A person of ordinary skill in the art would be able, and motivated, to improve the existing technology in the same or similar manner by combining or modifying the individual limitations that were already known in the art to yield predictable results.

Defendant also incorporates by reference, as if fully set forth herein, the motivations to combine identified in the Asserted Patent IPRs and Other Invalidity Contentions. Defendant also intends to rely upon the prior art identified in the Asserted Patent IPRs and Other Invalidity Contentions in combination with the prior art disclosed herein.

Subject to the foregoing, Defendant identifies the following exemplary reasons that skilled artisans would have combined limitations of the prior art to render obvious the Asserted Claims. The fact that others are not discussed more specifically should not be interpreted as an admission or concession that it does not apply. To the contrary, the discussion below simply provides more explanation of these specific rationales.

b) Motivations Identified During Prosecution

Defendant hereby expressly incorporates by reference any statements and reasons set forth by the Examiner during prosecution of the Asserted Patents and related patent applications, as to why it would have been obvious to modify or combine references to achieve the limitations of the Asserted Claims.

c) Combinations of Related References

In some instances, multiple prior art publications and/or physical references discuss or address the same or substantially similar underlying system or other project, such as multiple patents or publications discussing the same subject matter. Where multiple references discuss or relate to the same or related underlying projects, systems, or other subject matter, it would have been obvious to combine the discussions and disclosures of the references as they would be understood to describe features or potential features of the underlying project, system, or subject matter. Similarly, where one reference cites or discusses other references or their teachings, or references have one or more authors in common and a related area of subject matter, or have a common assignee, it would have been obvious to consider the teachings of the references in combination with each other due to the express relationships and commonalities between the references.

d) Specific Motivations to Combine and Additional Obviousness Considerations

(1) U.S. Patent No. 6,525,798

The asserted claim of the ’798 patent is directed to a liquid crystal display unit where “each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes” and “at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode.” ’798 patent, 15:55–16:12. Figures 13a and 13b illustrate this pixel structure:

FIG. 13a

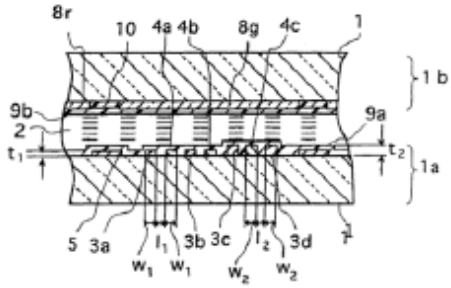
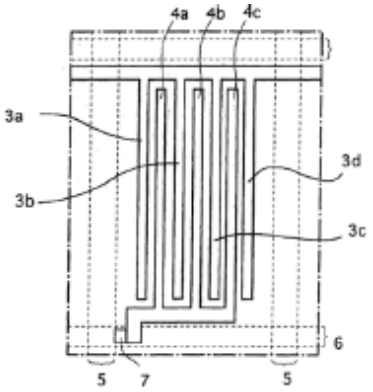


FIG. 13b



According to the specification of the ’798 patent, conventional in-plane switching (“IPS”) type displays had certain problems, including “coloring,” occurrence of “after image,” difficulty with controlling the tone, and low “light use efficiency.” *See id.,* 1:46–2:21. The ’798 patent seeks to address these problems and “provide a liquid crystal display unit with fast-response, a high light use efficiency, little image retention, and a wider viewing angle.” 2:24–27. The purported invention of the ’798 patent is an “IPS type liquid crystal display unit,” where “the common electrodes and pixel electrodes are alternately arranged in a row on the same substrate” and “the electrode pairs different in geometrical shape from other electrode pairs, or the electrodes different in geometrical shape from other electrodes” are used. *Id.,* 2:28–50. More specifically, the ’798 patent states that using different geometrical shapes for electrode pairs within the same pixel can

result in various benefits, including suppressing image retention, canceling coloring, widening the viewing angle, increasing the response time, and improving the tone. *See id.,* 3:1–4:56; *see also id.,* 12:66–13:29 (describing improved viewing angles and faster response times when using electrodes of different thicknesses).

However, the ’798 patent’s claimed structure was well-known in the art. Numerous other LCD prior art references, including, for example, Ohta ’044, Ohta ’454, Ohta ’101, Fujii, and Kawano, already disclosed the pixel structure claimed in the ’798 patent. For example, the prior art was replete with teachings of pixel structures where each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes, and at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode.

For example, Ohta ’044 discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode. *See, e.g.,* Ex. A-03 (Ohta ’044 claim chart). As another example, Ohta ’454 discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode. *See, e.g.,* Ex. A-04 (Ohta ’454 claim chart). As another example, Ohta ’101 discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode. *See, e.g.,* Ex. A-05 (Ohta ’101 claim chart). As another example, Fujii also discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the

electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode. *See, e.g.,* Ex. A-01 (Fujii claim chart). And as yet another example, Kawano also discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode. *See, e.g.,* Ex. A-02 (Kawano claim chart).

Further, under Bishop Display's apparent interpretation of claim 1, the '798 patent's claimed structure was well-known in the art. Numerous other LCD prior art references, including, for example, Lee and Niwano, already disclosed the pixel structure claimed in the '798 patent. For example, the prior art was replete with teachings of pixel structures where each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes, and at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode, under Bishop Display's apparent interpretation of "thickness."

For example, Lee discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a "thickness" of its common electrode or a "thickness" of its pixel electrode (as interpreted by Bishop Display). *See*, *e.g.*, Ex. A-06 (Lee claim chart). As another example, Niwano discloses an IPS-type pixel having a plurality of pairs of common electrodes and adjacent pixel electrodes, where at least one of the electrode pairs differs from other electrode pairs in a "thickness" of its common electrode or a "thickness" of its pixel electrode (as interpreted by Bishop Display) than other common electrodes. *See*, *e.g.*, Ex. A-07 (Niwano claim chart).

Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00507.

The asserted claims of the ’798 patent also would have been obvious to a POSITA in view of the following combinations as well as those identified in IPR2022-00507.

Ohta ’044 in view of Kawano

Ohta ’044 discloses several types of IPS-type pixel structures with a plurality of pairs of pixel electrodes and common electrodes. *See*, *e.g.,* Ohta ’044, [0049]–[0201], Figs. 1, 2, 20, 21, 22, 23.

Kawano, for example, discloses an electrode for light shielding that is opaque, parallel and adjacent to the image signal lines, and electrically connected to the common wiring. *See*, *e.g.*, Kawano, 14:14–15:44.

A POSITA would have recognized that Kawano’s light-shielding electrode could be incorporated into the IPS pixel structures disclosed in Ohta ’044. This would have constituted nothing more than “application of a known technique,” *i.e.*, the addition of a light-shielding electrode adjacent to and parallel to the image signal line, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Kawano’s light-shielding electrode for light shielding would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including improvements in display quality without increasing power consumption. This combination of Ohta ’044 and Kawano could have been done according to known methods to achieve these predictable results.

Kawano itself also provides a specific teaching, suggestion, or motivation for such combination. For example, because Kawano's light-shielding electrode can cover the gaps near the image signal lines, "the width of the light shielding region 94 can be enlarged without lowering the aperture ratio of the pixel region." Kawano, 15:8–16. Further, even if there is misalignment of the array and opposite substrates when they are attached to each other, the opening of the pixel region can be more or less unaffected (i.e. the liquid crystal display unit has greater manufacturing tolerance), and as a result, "neither the aperture ratio nor the luminance of the liquid crystal display element" is lowered. *Id.*, 15:16–26. There is also no need to increase the power consumption of the backlight, and leakage of light due to positional offset can be prevented. *Id.*, 15:23–26; *see also* 2:11-17. A POSITA would thus have recognized that using Kawano's light-shielding electrode would yield the predictable result of a liquid crystal display element with "excellent display quality." *Id.*, 15:26–27.

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing the leakage of light, thus further improving the aperture ratio and luminance of the display. *See, e.g.,* Ohta '044, [0090]–[0095]. A POSITA would also have been motivated to use Kawano's structure of a light-shielding electrode that is connected to the common wiring, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. A POSITA would also have recognized that forming the light shielding electrode of an opaque metal like the Mo–W as disclosed by Kawano would further improve light shielding ability and minimize crosstalk due to the signal lines. A POSITA would also have recognized that forming the light shielding electrode adjacent to the image signal line and electrically connected to the common electrode would further reduce

leakage of the electric field, improve the shielding effect, and reduce crosstalk. *See, e.g.,* Ohta ’044, [0202]–[0207].

In addition, a POSITA would have recognized that Ohta ’044 and Kawano both concern improving image display in an IPS mode liquid crystal display, *see, e.g.,* Ohta ’044, [0005]–[0024]; Kawano, 9:15–26, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Ohta ’044 and Kawano are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See, e.g.,* Ohta ’044, [0009]–[0010], [0020], [0093]–[0095], [0098]–[0104], [0176]–[0177], [0181], [0207]; Kawano, 1:5–18, 2:55–3:9.

Ohta ’454 in view of Kawano

Ohta ’454 discloses several types of IPS-type pixel structures with a plurality of pairs of pixel electrodes and common electrodes. *See, e.g.,* Ohta ’454, 46–51; Figs. 20, 21, 22, 24C.

Kawano discloses an electrode for light shielding that is opaque, parallel and adjacent to the image signal lines, and electrically connected to the common wiring. *See, e.g.,* Kawano, 14:14-15:44.

A POSITA would have recognized that Kawano’s light-shielding electrode could be incorporated into the IPS pixel structures disclosed in Ohta ’454. This would have constituted nothing more than “application of a known technique,” *i.e.,* the addition of a light-shielding electrode adjacent to and parallel to the image signal line, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Kawano’s light-shielding electrode for light shielding would

have been nothing more than a simple substitution of one known element for another to obtain predictable results, including improvements in display quality without increasing power consumption. This combination of Ohta ’454 and Kawano could have been done according to known methods to achieve these predictable results.

Kawano itself also provides a specific teaching, suggestion, or motivation for such combination. For example, because Kawano’s light-shielding electrode can cover the gaps near the image signal lines, “the width of the light shielding region 94 can be enlarged without lowering the aperture ratio of the pixel region.” Kawano, 15:8–16. Further, even if there is misalignment of the array and opposite substrates when they are attached to each other, the opening of the pixel region can be more or less unaffected (i.e. the liquid crystal display unit has greater manufacturing tolerance), and as a result, “neither the aperture ratio nor the luminance of the liquid crystal display element” is lowered. *Id.,* 15:16–26. There is also no need to increase the power consumption of the backlight, and leakage of light due to positional offset can be prevented. *Id.,* 15:23–26; *see also* 2:11-17. A POSITA would thus have recognized that using Kawano’s light-shielding electrode would yield the predictable result of a liquid crystal display element with “excellent display quality.” *Id.,* 15:26–27.

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing the leakage of light, thus further improving the aperture ratio and luminance of the display. *See, e.g.,* Ohta ’454, 1–2, 8, 26, 46–50. A POSITA would also have been motivated to use Kawano’s structure of a light-shielding electrode that is connected to the common wiring, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. *See, e.g.,* Ohta ’454, 19–20, 23–24. A

POSITA would also have recognized that forming the light shielding electrode of an opaque metal like the Mo–W as disclosed by Kawano would further improve light shielding ability and minimize crosstalk due to the signal lines. *See, e.g.,* Ohta ’454, 7, 19–20, 23, 38, 41, 49, 50.

In addition, a POSITA would have recognized that Ohta ’454 and Kawano both concern improving image display in an IPS mode liquid crystal display, *see, e.g.,* Ohta ’454, Abstract; Kawano, 9:15–26, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Ohta ’454 and Kawano are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See, e.g.,* Ohta ’454, 1–2, 7, 19–20, 28–29, 50; Kawano, 1:5–18, 2:55–3:9.

Ohta ’101 in view of Kawano

Ohta ’101 discloses several types of IPS-type pixel structures with a plurality of pairs of pixel electrodes and common electrodes. *See, e.g.,* Ohta ’101, [0119]–[0147]; Figs. 20, 21, 22, 24.

Kawano discloses an electrode for light shielding that is opaque, parallel and adjacent to the image signal lines, and electrically connected to the common wiring. *See, e.g.,* Kawano, 14:14–15:44.

A POSITA would have recognized that Kawano’s light-shielding electrode could be incorporated into the IPS pixel structures disclosed in Ohta ’101. This would have constituted nothing more than “application of a known technique,” *i.e.*, the addition of a light-shielding electrode adjacent to and parallel to the image signal line, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Kawano’s light-shielding electrode for light shielding would

have been nothing more than a simple substitution of one known element for another to obtain predictable results, including improvements in display quality without increasing power consumption. This combination of Ohta '101 and Kawano could have been done according to known methods to achieve these predictable results.

Kawano itself also provides a specific teaching, suggestion, or motivation for such combination. For example, because Kawano's light-shielding electrode can cover the gaps near the image signal lines, "the width of the light shielding region 94 can be enlarged without lowering the aperture ratio of the pixel region." Kawano, 15:8–16. Further, even if there is misalignment of the array and opposite substrates when they are attached to each other, the opening of the pixel region can be more or less unaffected (i.e. the liquid crystal display unit has greater manufacturing tolerance), and as a result, "neither the aperture ratio nor the luminance of the liquid crystal display element" is lowered. *Id.,* 15:16–26. There is also no need to increase the power consumption of the backlight, and leakage of light due to positional offset can be prevented. *Id.,* 15:23–26; *see also* 2:11-17. A POSITA would thus have recognized that using Kawano's light-shielding electrode would yield the predictable result of a liquid crystal display element with "excellent display quality." *Id.,* 15:26–27.

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing the leakage of light, thus further improving the aperture ratio and luminance of the display. *See, e.g.,* Ohta '101, [0007]–[0020], [0046]–[0050], [0119]–[0138]. A POSITA would also have been motivated to use Kawano's structure of a light-shielding electrode that is connected to the common wiring, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines.

See, e.g., Ohta ’101, [0025], [0036]–[0037]. A POSITA would also have recognized that forming the light shielding electrode of an opaque metal like the Mo—W as disclosed by Kawano would further improve light shielding ability and minimize crosstalk due to the signal lines. *See, e.g.,* Ohta ’101, [0025], [0034], [0098], [0135], [0139]–[0142].

In addition, a POSITA would have recognized that Ohta ’101 and Kawano both concern improving image display in an IPS mode liquid crystal display, *see, e.g.,* Ohta ’101, [0001]; Kawano, 9:15–26, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Ohta ’101 and Kawano are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See, e.g.,* Ohta ’101, [0007]–[0020], [0025]–[0026], [0056]–[0059], [0139]–[0142]; Kawano, 1:5–18, 2:55–3:9.

Kawano in view of Fujii

Kawano discloses several types of IPS-type pixel structures with a plurality of pairs of pixel electrodes and common electrodes. *See, e.g.,* Kawano, Figs. 2, 4, 11, 12.

Fujii discloses forming one of the common electrodes at one metal layer (*e.g.* a source/drain layer), and another one of the common electrodes at a different metal layer (*e.g.* a gate layer). *See, e.g.,* Fujii, Figs. 5, 10. Fujii also teaches that its embodiments may be modified to have the pixel and common electrodes in the reverse order. *See, e.g.,* Fujii, [0049], Figs. 11, 12.

A POSITA would have recognized that Fujii’s technique of forming a set of electrodes at two different metal layers could be incorporated into the IPS pixel structures disclosed in Kawano. This would have constituted nothing more than “application of a known technique,” *i.e.,* forming a set of electrodes at two different metal layers, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to

improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that incorporating Fujii's electrodes formed at different metal layers would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including the creation of multiple sub-pixels with different voltage characteristics, such that viewing angles are improved, thus improving display quality. This combination of Kawano and Fujii could have been done according to known methods to achieve these predictable results. Fujii itself also provides a specific teaching, suggestion, or motivation for such combination. For example, by forming electrodes at different metal layers within the same pixel, multiple sub-pixels can be created within the pixel, each with different voltage versus transmittance characteristics (*e.g.* creates multiple domains). Fujii, [0028], [0029]. The use of subpixels with different threshold voltages in turn results in improved viewing angle characteristics of the LCD, due to the "synthesis effect," or "multi-gradation". Fujii, [0028], [0029], [0058].

In addition, a POSITA would have recognized that Kawano and Fujii both concern improving image display in an IPS mode liquid crystal display, *see, e.g.,* Kawano, 9:15–26; Fujii, [0005], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Kawano and Fujii both appreciate the benefits and importance of increased viewing angles. *See, e.g.,* Kawano, 1:10–35; Fujii, [0005]–[0009], [0028], [0029], [0048], [0052], [0058].

(2) U.S. Patent No. 6,787,829

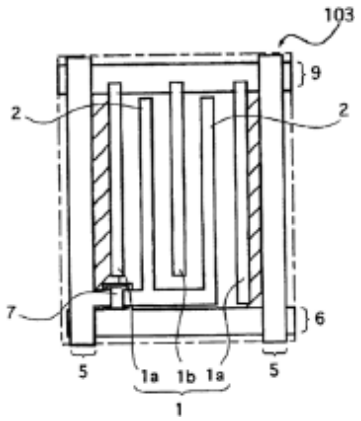
Independent claim 1 of the '829 patent is directed to a liquid crystal display panel where each of the pixel regions include a "line-shaped pixel electrode" that is "parallel to the image signal lines or to the scanning signal lines" and a "common electrode" that is "parallel to the pixel electrode." '829 patent, 11:30–60. Claim 1 further requires that, "of the pixel electrode and the

common electrode, the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines comprises an opaque conductor, and at least one of the other electrodes comprises a transparent conductor." *Id.*

Independent claim 29 of the '829 patent is similarly directed to a liquid crystal display panel where each of the pixel regions include a "line-shaped pixel electrode" that is "parallel to the image signal lines or to the scanning signal lines" and a "common electrode" that is "parallel to the pixel electrode." '829 patent, 14:22–50. Claim 29 further includes a "a light shielding member covering a region between the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines and one of the image signal lines or one of the scanning signal lines." *Id.*

Pixel electrodes having line-shaped pixel electrodes parallel to image signal lines or scanning signal lines, and common electrodes parallel to line-shaped pixel electrodes were well-known in the prior art. Indeed, the applicant admitted that the prior art IPS mode liquid crystal display panels included these structures, as shown in Figure 14 below. *See id.,* 1:11–2:64.

Fig. 14



The additional feature of independent claim 1 was also well-known in the prior art. Numerous other LCD prior art references, including, for example, Kawano, Ohta '454, Niwano, Wakagi, and Ohta '101, disclosed the claimed pixel structure, including the only limitation not

admitted to be in the prior art by the ’829 patent itself: “wherein, of the pixel electrode and the common electrode, the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines comprises an opaque conductor, and at least one of the other electrodes comprises a transparent conductor.” *See, e.g.,* Exs. B-01 (Kawano claim chart); B-02 (Ohta ’454 claim chart); B-03 (Niwano claim chart); B-05 (Wakagi claim chart); B-06 (Ohta ’101 claim chart).

Similarly, the additional feature of independent claim 29 was also well-known in the prior art. Numerous other LCD prior art references, including, for example, Kawano, Ohta ’454, Niwano, Yoshida, Wakagi, and Ohta ’101, disclosed the claimed pixel structure, including the only limitation not admitted to be in the prior art by the ’829 patent itself: “a light shielding member covering a region between the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines and one of the image signal lines or one of the scanning signal lines.” *See, e.g.,* Exs. B-01 (Kawano claim chart); B-02 (Ohta ’454 claim chart); B-03 (Niwano claim chart); B-04 (Yoshida claim chart); B-05 (Wakagi claim chart); B-06 (Ohta ’101 claim chart).

Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00508.

The asserted claims of the ’829 patent also would have been obvious to a POSITA in view of the following combinations as well as those identified in IPR2022-00508.

Niwano in view of Kawano

Niwano discloses that its pixel electrodes and common electrodes may be formed of a variety of different types of materials, including opaque and transparent materials, or multi-layered constructions thereof. *See, e.g.,* Niwano, 9:54–10:26 (“any one of Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of

such as ITO or the like or their laminated construction or their laminated construction including them"). *See also*, *e.g.*, *id.*, 8:65–9:18; 9:34–41 (for scanning lines and signal lines).

Kawano discloses an electrode for light shielding that is opaque, parallel and adjacent to the image signal lines, and electrically connected to the common wiring. *See, e.g.,* Kawano, 14:14–15:44. Kawano further discloses the use of "transparent electrodes such as ITO" for the pixel electrodes and other common electrodes. *See*, *e.g.*, *id.* 15:38–44.

A POSITA would have recognized that Kawano's light-shielding electrode could be incorporated into the IPS pixel structures disclosed in Niwano. This would have constituted nothing more than "application of a known technique," *i.e.*, the addition of a light-shielding electrode adjacent to and parallel to the image signal line, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Kawano's light-shielding electrode for light shielding would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including improving display quality without increasing power consumption. This combination of Niwano and Kawano could have been done according to known methods to achieve these predictable results.

Kawano itself also provides a specific teaching, suggestion, or motivation for such combination. For example, because Kawano's light-shielding electrode can cover the gaps near the image signal lines, "the width of the light shielding region 94 can be enlarged without lowering the aperture ratio of the pixel region." Kawano, 15:8–16. Further, even if there is misalignment of the array and opposite substrates when they are attached to each other, the opening of the pixel

region can be more or less unaffected (i.e. the liquid crystal display unit has greater manufacturing tolerance), and as a result, "neither the aperture ratio nor the luminance of the liquid crystal display element" is lowered. *Id.*, 15:16–26. There is also no need to increase the power consumption of the backlight, and leakage of light due to positional offset can be prevented. *Id.*, 15:23–26; *see also* 2:11-17. A POSITA would thus have recognized that using Kawano's light-shielding electrode would yield the predictable result of a liquid crystal display element with "excellent display quality." *Id.*, 15:26–27.

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing the leakage of light, thus further improving the aperture ratio and luminance of the display. A POSITA would also have been motivated to use Kawano's structure of a light-shielding electrode that is connected to the common wiring, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. A POSITA would also have recognized that forming the light shielding electrode of an opaque metal like the Mo—W as disclosed by Kawano would further improve light shielding ability and minimize crosstalk due to the signal lines.

In addition, a POSITA would have recognized that Niwano and Kawano both concern improving image display in an IPS mode liquid crystal display, *see*, *e.g.*, Niwano, Abstract; Kawano, 9:15–26, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Niwano and Kawano are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See, e.g.,* Niwano, 1:8–15; 3:58–4:56; Kawano, 1:5–18, 2:55–3:9.

Niwano in view of Ohta ’454 or Ohta ’101

Niwano discloses that its pixel electrodes and common electrodes may be formed of a variety of different types of materials, including opaque and transparent materials, or multi-layered constructions thereof. *See*, *e.g.*, Niwano, 9:54–10:26 (“any one of Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of such as ITO or the like or their laminated construction or their laminated construction including them”). *See also*, *e.g.*, *id.*, 8:65–9:18; 9:34–41 (for scanning lines and signal lines).

Ohta ’454 discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for the other electrodes in the pixel. *See*, *e.g.*, Ohta ’454, 26, 50, Fig. 23. Ohta ’101 similarly discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for the other electrodes in the pixel. *See*, *e.g.*, Ohta ’101, [0046]–[0050], [0139]–[0142], Fig. 23.

A POSITA would have recognized that Ohta ’454 or Ohta ’101’s technique of using an opaque conductor for electrodes adjacent to the image signal lines could be incorporated into the IPS pixel structures disclosed in Niwano. This would have constituted nothing more than “application of a known technique,” *i.e.*, using an opaque conductor for electrodes adjacent to the image signal lines, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ohta ’454 or Ohta ’101’s opaque conductors would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including minimizing crosstalk and improving display quality. This combination of Niwano and Ohta ’454 or Ohta ’101 could have been done according to known methods to achieve these predictable results.

Ohta ’454 and Ohta ’101 themselves also provide a specific teaching, suggestion, or motivation for such combination. For example, crosstalk due to electric flux lines from the image signal line results in poor image quality, and allowing the electrode adjacent to the image signal line to be opaque can help suppress the crosstalk associated with the image signal lines, thus improving image quality. Ohta ’454, 7, 19–20, 50; Ohta ’101, [0025], [0139]–[0142]. Ohta ’454 and Ohta ’101 also teach that this crosstalk shielding effect is further improved if the adjacent electrode performing the shielding function is the common electrode, because the voltage potential for the common electrodes is stable. Ohta ’454, 19–20, 23–24; Ohta ’101, [0025], [0036]–[0037].

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing crosstalk, thus further improving the aperture ratio and luminance of the display. *See, e.g.,* Ohta ’454, 1–2, 8, 26, 46–50; Ohta ’101, [0002]–[0019], [0046]–[0050], [0119]–[0142].

A POSITA would also have been motivated to use Ohta ’454 or Ohta ’101’s technique of making opaque the common electrodes adjacent to the image signal lines, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. *See*, *e.g.*, Ohta ’454, 19–20, 23–24; Ohta ’101, [0025], [0036]–[0037]. A POSITA would also have recognized that forming the common electrodes adjacent to the image signal lines of an opaque metal as disclosed by Ohta ’454 or Ohta ’101 would further improve light shielding ability and minimize crosstalk due to the signal lines. *See*, *e.g.*, Ohta ’454, 7, 19–20, 23, 38, 41, 49, 50; Ohta ’101, [0025], [0036], [0134]–[0138], [0139]–[0142].

In addition, a POSITA would have recognized that Niwano and Ohta ’454 and Ohta ’101 all concern improving image display in an IPS mode liquid crystal display, *see*, *e.g.*, Niwano, Abstract; Ohta ’454, Abstract; Ohta ’101, [0002]–[0019], and that the improvements in one could

readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, each of Niwano and Ohta ’454 and Ohta ’101 are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See*, *e.g.*, Niwano, 1:8–15; 3:58–4:56; Ohta ’454, 1–2, 7, 19–20, 28–29, 50; Ohta ’101, [0002]–[0019], [0025], [0056]–[0059], [0139]–[0142].

Niwano in view of Wakagi

Niwano discloses that its pixel electrodes and common electrodes may be formed of a variety of different types of materials, including opaque and transparent materials, or multi-layered constructions thereof. *See, e.g.,* Niwano, 9:54–10:26 (“any one of Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of such as ITO or the like or their laminated construction or their laminated construction including them”). *See also*, *e.g.*, *id.*, 8:65–9:18; 9:34–41 (for scanning lines and signal lines).

Wakagi discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for other electrodes in the pixel. *See*, *e.g.*, Wakagi Figs. 11, 12. Wakagi also discloses using two-layered electrodes formed of both opaque and transparent conductors as the common or pixel electrodes. *See*, *e.g.*, Wakagi Figs. 5, 6, 7, 8, 17.

A POSITA would have recognized that Wakagi’s techniques of using an opaque conductor for electrodes adjacent to the image signal lines, or using two-layered conductors, could be incorporated into the IPS pixel structures disclosed in Niwano. This would have constituted nothing more than “application of a known technique,” *i.e.*, using an opaque conductor for electrodes adjacent to the image signal lines, or using two-layered conductors, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to

implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Wakagi's electrode structures would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including reducing the driving voltage, reducing degradation of the electrodes, and improving aperture ratio. This combination of Niwano and Wakagi could have been done according to known methods to achieve these predictable results.

Wakagi itself also provides a specific teaching, suggestion, or motivation for such combination. For example, when conventional electrodes are formed below insulating films, the electric field applied to the liquid crystal layer is weakened, and a larger driving voltage becomes necessary, and responsiveness of the liquid crystals is limited. Further, metal electrodes can be degraded by contact with liquid crystals. *See*, *e.g.*, Wakagi, 1:37–2:2. Wakagi teaches that its electrode structures would limit the loss in electric field strength, thus allowing smaller driving voltages and lower power consumption; increase display responsiveness; prevent degradation of electrodes through use of ITO; and increase the aperture ratio, resulting in a bright display. *See*, *e.g.*, Wakagi, 3:54–4:67, 5:20–48, 6:40–47, 7:26–34, 7:51–8:8, 8:60–63, 9:65–10:11.

In addition, a POSITA would have recognized that Niwano and Wakagi both concern improving image display in an IPS mode liquid crystal display, *see*, *e.g.*, Niwano, Abstract; Wakagi, 1:7–2:23, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Yoshida in view of Kawano

Yoshida discloses an IPS-type pixel structure where the pixel electrodes and common electrodes are parallel to each other and the image signal lines. *See, e.g.,* Yoshida, Figs. 14–17, 9:22–39, 9:40–47.

Kawano discloses an electrode for light shielding that is opaque, parallel and adjacent to the image signal lines, and electrically connected to the common wiring. *See, e.g.,* Kawano, 14:14–15:44. Kawano further discloses the use of "transparent electrodes such as ITO" for the pixel electrodes and other common electrodes. *See, e.g., id.* 15:38–44.

A POSITA would have recognized that Kawano's light-shielding electrode could be incorporated into the IPS pixel structures disclosed in Yoshida. This would have constituted nothing more than "application of a known technique," *i.e.*, the addition of a light-shielding electrode adjacent to and parallel to the image signal line, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Kawano's light-shielding electrode for light shielding would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including improving display quality without increasing power consumption. This combination of Yoshida and Kawano could have been done according to known methods to achieve these predictable results.

Kawano itself also provides a specific teaching, suggestion, or motivation for such combination. For example, because Kawano's light-shielding electrode can cover the gaps near the image signal lines, "the width of the light shielding region 94 can be enlarged without lowering the aperture ratio of the pixel region." Kawano, 15:8–16. Further, even if there is misalignment of the array and opposite substrates when they are attached to each other, the opening of the pixel region can be more or less unaffected (i.e. the liquid crystal display unit has greater manufacturing tolerance), and as a result, "neither the aperture ratio nor the luminance of the liquid crystal display

element" is lowered. *Id*., 15:16–26. There is also no need to increase the power consumption of the backlight, and leakage of light due to positional offset can be prevented. *Id*., 15:23–26 *see also* 2:11-17. A POSITA would thus have recognized that using Kawano's light-shielding electrode would yield the predictable result of a liquid crystal display element with "excellent display quality." *Id.*, 15:26–27.

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing the leakage of light, thus further improving the aperture ratio and luminance of the display. A POSITA would also have been motivated to use Kawano's structure of a light-

shielding electrode that is connected to the common wiring, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. A POSITA would also have recognized that forming the light shielding electrode of an opaque metal like the Mo—W as disclosed by Kawano would further improve light shielding ability and minimize crosstalk due to the signal lines.

In addition, a POSITA would have recognized that Yoshida and Kawano both concern improving image display in an IPS mode liquid crystal display, *see*, *e.g.*, Yoshida, Abstract; Kawano, 9:15–26, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Yoshida and Kawano are concerned with improving the display by reducing leakage of electric field from the signal line while maximizing aperture and minimizing crosstalk. *See*, *e.g.*, Yoshida, 8:32–42, 9:21–64; Kawano, 1:5–18, 2:55–3:9.

Yoshida in view of Ohta ’454 or Ohta ’101

Yoshida discloses an IPS-type pixel structure where the pixel electrodes and common electrodes are parallel to each other and the image signal lines. *See*, *e.g.*, Yoshida, Figs. 14–17, 9:22–39, 9:40–47.

Ohta ’454 discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for the other electrodes in the pixel. *See*, *e.g.*, Ohta ’454, 26, 50, Fig. 23. Ohta ’101 similarly discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for the other electrodes in the pixel. *See*, *e.g.*, Ohta ’101, [0046]–[0050], [0139]–[0142], Fig. 23. A POSITA would have recognized that Ohta ’454 or Ohta ’101’s technique of using an opaque conductor for electrodes adjacent to the image signal lines could be incorporated into the IPS pixel structures disclosed in Yoshida. This would have constituted nothing more than “application of a known technique,” *i.e.*, using an opaque conductor for electrodes adjacent to the image signal lines, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ohta ’454 or Ohta ’101’s opaque conductors would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including minimizing crosstalk and improving display quality. This combination of Yoshida and Ohta ’454 or Ohta ’101 could have been done according to known methods to achieve these predictable results.

Ohta ’454 and Ohta ’101 themselves also provide a specific teaching, suggestion, or motivation for such combination. For example, crosstalk due to electric flux lines from the image signal line results in poor image quality, and allowing the electrode adjacent to the image signal

line to be opaque can help suppress the crosstalk associated with the image signal lines, thus improving image quality. Ohta ’454, 7, 19–20, 50; Ohta ’101, [0025], [0139]–[0142]. Ohta ’454 also teaches that this crosstalk shielding effect is further improved if the adjacent electrode performing the shielding function is the common electrode, because the voltage potential for the common electrodes is stable. Ohta ’454, 19–20, 23–24; Ohta ’101, [0025], [0036]–[0037].

A POSITA would further have been motivated to make this combination because it would allow the use of ITO—which is optically transparent—for the other electrodes in the pixel while still minimizing crosstalk, thus further improving the aperture ratio and luminance of the display. *See, e.g.,* Ohta ’454, 1–2, 8, 26, 46–50; Ohta ’101, [0002]–[0019], [0046]–[0050], [0119]–[0142].

A POSITA would also have been motivated to use Ohta ’454 or Ohta ’101’s technique of making opaque the common electrodes adjacent to the image signal lines, because the voltage on the common wiring is stable; this improves the ability of the electrode to shield light and minimize crosstalk from the signal lines. *See, e.g.,* Ohta ’454, 19–20, 23–24; Ohta ’101, [0025], [0036]–[0037]. A POSITA would also have recognized that forming the common electrodes adjacent to the image signal lines of an opaque metal as disclosed by Ohta ’454 or Ohta ’101 would further improve light shielding ability and minimize crosstalk due to the signal lines. *See*, *e.g.*, Ohta ’454, 7, 19–20, 23, 38, 41, 49, 50; Ohta ’101, [0025], [0036], [0134]–[0138], [0139]–[0142].

In addition, a POSITA would have recognized that Yoshida and Ohta ’454 and Ohta ’101 all concern improving image display in an IPS mode liquid crystal display, *see, e.g.,* Yoshida, Abstract; Ohta ’454, Abstract; Ohta ’101, [0002]–[0019], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Still further, both Yoshida and Ohta ’454 and Ohta ’101 are concerned with improving the display by reducing leakage of electric field from the

signal line while maximizing aperture and minimizing crosstalk. *See*, *e.g.*, Yoshida, 8:32–42, 9:21–64; Ohta '454, 1–2, 7, 19–20, 28–29, 50; Ohta '101, [0002]–[0019], [0025], [0056]–[0059], [0139]–[0142].

Yoshida in view of Wakagi

Yoshida discloses an IPS-type pixel structure where the pixel electrodes and common electrodes are parallel to each other and the image signal lines. *See, e.g.,* Yoshida, Figs. 14–17, 9:22–39, 9:40–47.

Wakagi discloses using an opaque conductor for the common electrodes parallel and adjacent to the image signal lines, and a transparent conductor for other electrodes in the pixel. *See*, *e.g.*, Wakagi Figs. 11, 12. Wakagi also discloses using two-layered electrodes formed of both opaque and transparent conductors as the common or pixel electrodes. *See*, *e.g.*, Wakagi Figs. 5, 6, 7, 8, 17.

A POSITA would have recognized that Wakagi's techniques of using an opaque conductor for electrodes adjacent to the image signal lines, or using two-layered conductors, could be incorporated into the IPS pixel structures disclosed in Yoshida. This would have constituted nothing more than "application of a known technique," *i.e.*, using an opaque conductor for electrodes adjacent to the image signal lines, or using two-layered conductors, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Wakagi's electrode structures would have been nothing more than a simple substitution of one known element for another to obtain predictable results, including reducing the driving voltage, reducing degradation of the electrodes,

and improving aperture ratio. This combination of Yoshida and Wakagi could have been done according to known methods to achieve these predictable results.

Wakagi itself also provides a specific teaching, suggestion, or motivation for such combination. For example, when conventional electrodes are formed below insulating films, the electric field applied to the liquid crystal layer is weakened, and a larger driving voltage becomes necessary, and responsiveness of the liquid crystals is limited. Further, metal electrodes can be degraded by contact with liquid crystals. *See, e.g.*, Wakagi, 1:37–2:2. Wakagi teaches that its electrode structures would limit the loss in electric field strength, thus allowing smaller driving voltages and lower power consumption; increase display responsiveness; prevent degradation of electrodes through use of ITO; and increase the aperture ratio, resulting in a bright display. *See, e.g.*, Wakagi, 3:54–4:67, 5:20–48, 6:40–47, 7:26–34, 7:51–8:8, 8:60–63, 9:65–10:11.

In addition, a POSITA would have recognized that Yoshida and Wakagi both concern improving image display in an IPS mode liquid crystal display, *see*, *e.g.*, Yoshida, Abstract; Wakagi, 1:7–2:23, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

(3) U.S. Patent No. 6,801,293

The asserted claim of the ’293 patent is directed to a method for “manufacturing an in-plane electric field mode liquid crystal element having a pair of substrates including, on at least one of the substrates, pixel electrodes for generating an in-plane electric field, common electrodes, and an insulating film for insulating these electrodes from one another, orientation films provided on the inner side of one or both of the substrates and a liquid crystal layer sandwiched between the substrates.” ’293 patent, Claim 1. The method for manufacturing further comprises “a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates.” ’293 patent, Claim 1.

Limitations of the ’293 patent were well-known in the prior art and can be grouped generally into structural references and/or rubbing/stripping by rubbing references. For example, in-plane electric fields were known in the prior art.

Structural References: Each of the structural components of a liquid crystal element were well-known before the priority date of the ’293 patent, such as a pair of substrates, pixel electrodes for generating an in-plane electric field, and common electrodes, and an insulating film for insulating electrodes from one another (e.g., Nishikawa 1997, [0002], [0052], [0058], [0072], [0074]; Ohe, Abstract, 1:8-17, 1:21-31, 1:42-51, 2:66-3:4, 7:34-8:13, 8:29-34, 9:40-10:24, Figs. 1, 2, 5, 6A-C; Hideaki, [0001], [0002], [0004], [0018], Fig. 2; Tsumura, [0012], [0014], [0010], [0017], [0024], Figs. 3, 6, 17; Sawatsubashi, Abstract, [0001], [0012], [0013], [0015], [0016], [0017], [0022], Figs. 1, 3; Ichikawa, Abstract, [0028], [0042], Fig. 1; Yamada, Abstract, [0001], [0023], [0024], [0026], [0027], [0032], Figs. 1, 2; Ashizawa, Abstract, 1:40-49, 4:32-39, 8:49-9:6, 11:37-47, 12:19-29, 14:8-12, 14:54-62, 17:50-61, 19:44-63, 20:19-28, Figs. 2, 4, 10, 11, 12; Watanabe, Abstract, 4:50-5:6, 6:16-27, 9:64-10:11, 10:18-20, 13:26-33, Figs. 7, 8; Mihara, [0005], [0006], [0009], [0018], [0021], Figs. 1, 2, Cls. 7-9; Mori, [0014], [0019], [0020], [0021], [0022], [0032], Fig. 5) and orientation films provided on the inner side of one or both of the substrates (e.g., Nishikawa 1997, [0002], [0058], [0061]; Ohe, Abstract, 1:8-17, 1:52-58, 3:11-37, 7:53-8:13, 8:29-34, Figs. 1, 2, 5; Hideaki, [0004], [0006], Figs. 2, 3; Tsumura, [0012], [0014], [0010], [0017], [0024], Figs. 3, 6, 17; Sawatsubashi, Abstract, [0001], [0012], [0013], [0015], [0016], [0017], [0022], Figs. 1, 3; Ichikawa, Abstract, [0028], [0042], Fig. 1; Yamada, Abstract, [0001], [0023], [0024], [0026], [0027], [0032], Figs. 1, 2; Ashizawa, Abstract, 1:40-49, 4:32-39, 8:49-9:6, 11:37-47, 12:19-29, 14:8-12, 14:54-62, 17:50-61, 19:44-63, 20:19-28, Figs. 2, 4, 10, 11, 12; Watanabe, Abstract, 4:50-5:6, 6:16-27, 9:64-10:11, 10:18-20, 13:26-33, Figs. 7, 8; Mihara, Abstract, [0006],

[0021], [0022], Fig. 1; Mori, [0006], [0014], [0016], [0019], [0020], [0021], [0025], [0027], [0029], [0032], [0033], [0034], [0035], Fig. 5).

Rubbing/Stripping References: Additionally, well-known manufacturing steps for fabricating a liquid crystal element included rubbing/stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates (e.g., Nishikawa 1997, [0005], [0061]; Ohe, Abstract, 1:8-17, 1:21-31, 1:42-58, 2:39-56, 2:66-3:4, 3:11-37, 5:21-32, 7:42-52; Hideaki, [0001], [0002], [0004], [0006], [0007], [0009], [0018], [0020], Figs. 2, 3; Tsumura, [0004], [0014], [0021], [0022], Fig. 3; Sawatsubashi, Abstract, [0012], [0016], [0017], [0018], [0024], Fig. 1; Ichikawa, [0018], [0028], [0032], [0033], Fig. 1; Yamada, Abstract, [0024], [0025], [0031], Figs. 1-2; Ashizawa, 14:8-12, 20:18-29, 28:36-50, Fig. 4, 14A, 31A; Watanabe, 12:43-48, 14:44-48, 14:64-15:5, 15:12-15, Figs. 13A-C; Mihara, [0002], [0006], [0007], [0008], [0009], [0010], [0015] [0023], [0025], [0026], Figs. 1, 2, 5; Mori, Abstract, [0027], [0028], [0035], [0035], [0037], [0042]).

Structural References and Rubbing/Stripping References provide teachings or suggestions that would lead a POSITA to combine their respective elements, either within each group or across both groups of references (i.e., the teachings in the Structural References may complement or enhance the teachings in the Rubbing/Stripping References, or vice versa). This explicit indication of compatibility makes it clear that the combination of the teachings from these two groups of references would be an obvious next step for a POSITA.

The combination of Structural References and Rubbing/Stripping References yields predictable results, which is a key factor in determining obviousness. References in both groups of references provide detailed, well-documented information that enables a POSITA to understand

how the elements from each reference would work together. This predictability indicates that the combinations would have been apparent to a POSITA at the time of the invention.

Combining Structural References and Rubbing/Stripping References involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two groups of references, further supporting the argument that the combination is obvious.

References in the Structural References and Rubbing/Stripping References groups are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to one or more additional references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references from the Structural References and Rubbing/Stripping References is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Exemplary two-reference combinations are discussed further below, and such combinations would similarly apply to larger sets of combinations using the same references.

Ohe in view of Nishikawa

References Ohe and Nishikawa both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ohe may complement or enhance the teachings in Nishikawa, or vice versa. This explicit indication of compatibility

makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ohe and Nishikawa yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ohe and Nishikawa involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ohe and Nishikawa are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ohe and Nishikawa is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ashizawa in view of Nishikawa

References Ashizawa and Nishikawa both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ashizawa may complement or enhance the teachings in Nishikawa, or vice versa. This explicit indication of

compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ashizawa and Nishikawa yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ashizawa and Nishikawa involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ashizawa and Nishikawa are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ashizawa and Nishikawa is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Minhara in view of Nishikawa

References Minhara and Nishikawa both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Minhara may complement or enhance the teachings in Nishikawa, or vice versa. This explicit indication of

compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Minhara and Nishikawa yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together.

This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Minhara and Nishikawa involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Minhara and Nishikawa are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Minhara and Nishikawa is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Mori in view of Nishikawa

References Mori and Nishikawa both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Mori may complement or enhance the teachings in Nishikawa, or vice versa. This explicit indication of compatibility

makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Mori and Nishikawa yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together.

This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Mori and Nishikawa involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Mori and Nishikawa are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Mori and Nishikawa is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ashizawa in view of Tsumura

References Ashizawa and Tsumura both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ashizawa may

complement or enhance the teachings in Tsumura, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ashizawa and Tsumura yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ashizawa and Tsumura involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ashizawa and Tsumura are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ashizawa and Tsumura is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Watanabe in view of Tsumura

References Watanabe and Tsumura both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Watanabe may complement or enhance the teachings in Tsumura, or vice versa. This explicit indication of

compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Watanabe and Tsumura yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Watanabe and Tsumura involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. Watanabe and Tsumura are both related to a method to prevent display failure from alignment issue of a liquid crystal display to enhance image quality. For example, Watanabe describes, "It is an object of the present invention to provide an IPS (In-Plane Switching) liquid crystal display that is free of display defects such as vertical crosstalk and stepping non-uniformity even when the display screen is viewed from the side horizontally, that maintains good display uniformity and high aperture ratio, and that has high product yield during fabrication." Watanabe, 4:39-56. Tsumura describes "[t]he boundary between the reverse tilt region and the normal alignment region is called a disclination line 19, which causes light leakage and causes image quality failure." Tsumura, 3:21-25. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Watanabe and Tsumura are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would

look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Watanabe and Tsumura is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ohe in view of Tsumura

References Ohe and Tsumura both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ohe may complement or enhance the teachings in Tsumura, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ohe and Tsumura yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together.

This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ohe and Tsumura involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ohe and Tsumura are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ohe and Tsumura is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Minhara in view of Tsumura

References Minhara and Tsumura both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Minhara may complement or enhance the teachings in Tsumura, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Minhara and Tsumura yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together.

This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Minhara and Tsumura involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Minhara and Tsumura are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Minhara and Tsumura is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Mori in view of Tsumura

References Mori and Tsumura both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Mori may complement or enhance the teachings in Tsumura, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Mori and Tsumura yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together.

This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Mori and Tsumura involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Mori and Tsumura are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Mori and Tsumura is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable

results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ohe in view of Minhara

References Ohe and Minhara both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ohe may complement or enhance the teachings in reference Minhara, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ohe and Minhara yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ohe and Minhara involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ohe and Minhara are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ohe and Minhara is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable

results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ohe in view of Mori

References Ohe and Mori both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ohe may complement or enhance the teachings in reference Mori, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ohe and Mori yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ohe and Mori involves the application of known problem- solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ohe and Mori are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ohe and Mori is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ashizawa in view of Minhara

References Ashizawa and Minhara both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ashizawa may complement or enhance the teachings in reference Minhara, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ashizawa and Minhara yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ashizawa and Minhara involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ashizawa and Minhara are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ashizawa and Minhara is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Ashizawa in view of Mori

References Ashizawa and Mori both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Ashizawa may complement or enhance the teachings in reference Mori, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Ashizawa and Mori yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Ashizawa and Mori involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Ashizawa and Mori are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Ashizawa and Mori is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Wantanabe in view of Minhara

References Wantanabe and Minhara both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Wantanabe may complement or enhance the teachings in reference Minhara, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Wantanabe and Minhara yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Wantanabe and Minhara involves the application of known problem- solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Wantanabe and Minhara are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Wantanabe and Minhara is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

Wantanabe in view of Minhara

References Wantanabe and Mori both provide teachings or suggestions that would lead a POSITA to combine their respective elements. The teachings in reference Wantanabe may complement or enhance the teachings in reference Mori, or vice versa. This explicit indication of compatibility makes it clear that the combination of the two references would be an obvious next step for a POSITA.

The combination of references Wantanabe and Mori yields predictable results, which is a key factor in determining obviousness. Both references provide detailed, well-documented information that enables a POSITA to understand how the elements from each reference would work together. This predictability indicates that the combination would have been apparent to a POSITA at the time of the invention.

Combining references Wantanabe and Mori involves the application of known problem-solving techniques that were well-established in the relevant field at the time of the invention. A POSITA would recognize the utility of applying these techniques to combine the teachings of the two references, further supporting the argument that the combination is obvious.

References Wantanabe and Mori are considered analogous art, meaning that they are from the same field or address similar problems. This makes it more likely that a POSITA would look to both references when seeking a solution to a particular problem, and therefore strengthens the argument that the combination is obvious under the KSR standard.

In conclusion, the combination of references Wantanabe and Mori is obvious under the KSR standard based on the explicit teachings or suggestions within the references, the predictable results that arise from the combination, the application of known problem-solving techniques and the fact that the references are considered analogous art.

(4) U.S. Patent No. 6,816,208

The claims of the ’208 patent are directed to an active matrix LCD device having a “capacitive accumulation portion” formed by overlapping a pixel electrode, an insulating layer, and a common electrode, where the storage capacitance in the “capacitive accumulation portion” is varied from one pixel to an adjacent pixel by varying “an aperture in the common electrode” from one pixel to an adjacent pixel. ’208 patent, 22:38-52. For example, Figures 1A and 1B of the ’208 patent (below) depict this LCD device structure:

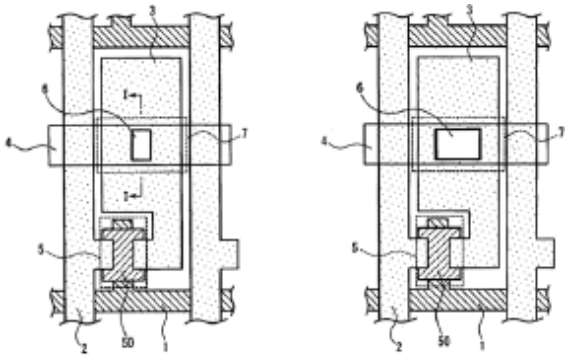


FIG. 1A FIG. 1B

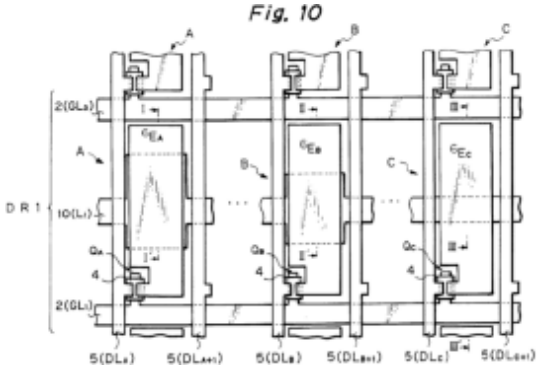
According to the specification of the ’208 patent, this structure is directed to addressing an alleged “display unevenness” problem with LCD devices at the time of the alleged invention caused by a deformation or collapse in the waveform of the scanning voltage pulse as it departs the feeding side of the display. ’208 patent, 1:9–25. The ’208 patent alleges that forming an “aperture in the common electrode” that varies from one pixel to another, where each pixel contains a “capacitive accumulation portion,” solved these problems. In particular, the ’208 patent asserts that the claimed structure allows “the aperture ratio and the electric fields in the vicinity of the [LCD] area [to] be maintained substantially constant independently of the pixel,” leading to “a uniform display . . . from the termination side to the feeding side” of the LCD. ’208 patent, 2:25–30.

However, the ’208 patent’s claimed structure was well-known in the prior art. Numerous other LCD prior art references, including, for example, Kuroha, Watanabe ’214, Nishikawa 1993, and Ueda (in view of Ohkawara) already disclosed the pixel structure claimed in the ’208 patent. For example, the prior art was replete with teachings of a capacitive accumulation portion formed by overlapping a pixel electrode, an insulating layer and a common electrode for each pixel area; a non-electrode area in a part of the pixel area which is not covered with a pixel electrode; wherein a peripheral shape of said capacitive accumulation portion on a side contacting said non-electrode area is substantially the same between respective pixels; and a value of a storage capacity in said capacitive accumulation portion of one pixel at a signal feeding side is larger than that of an adjacent pixel at a termination side.

For example, the ’208 patent itself describes a prior art technique using storage capacitors formed by overlapping portions of an “auxiliary capacity line [] disposed under an interlayer insulating and a pixel electrode,” where the overlapping portions that form the storage capacitors are gradually made smaller from one pixel to the next, such that “the difference in the field-through-voltage accompanied by a deformation or a collapse of the scanning voltage waveform can be eliminated.” ’208 patent, 1:26-47.

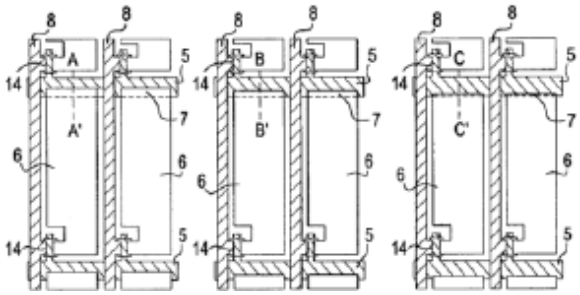
Likewise, as depicted in exemplary Figure 10 below, Kuroha teaches forming “storage capacitors SC_A, SC_B and SC_C” by overlapping storage electrodes, an insulating layer, and pixel electrodes, where the storage capacitances are gradually reduced as the “overlapped areas . . . are gradually reduced.” *See*, *e.g.*, Kuroha, 5:10–37.

Fig. 10

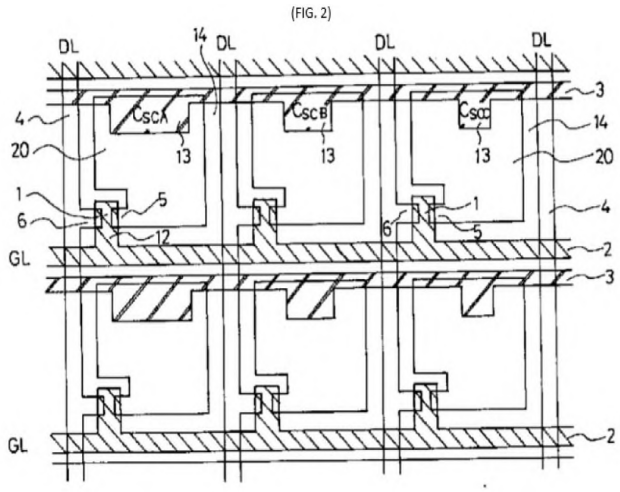


Watanabe ’214 also teaches a pixel structure containing, as depicted in exemplary Figures 4A–4C below, an “overlap portion 7” formed by overlapping a pixel electrode 6 and another electrode through an interlayer insulation film 12 so that the capacitance formed in the overlap portion “decreases stepwise” as the distance from the signal feeding side increases. *See*, *e.g.*, Watanabe ’214, 5:29–39.

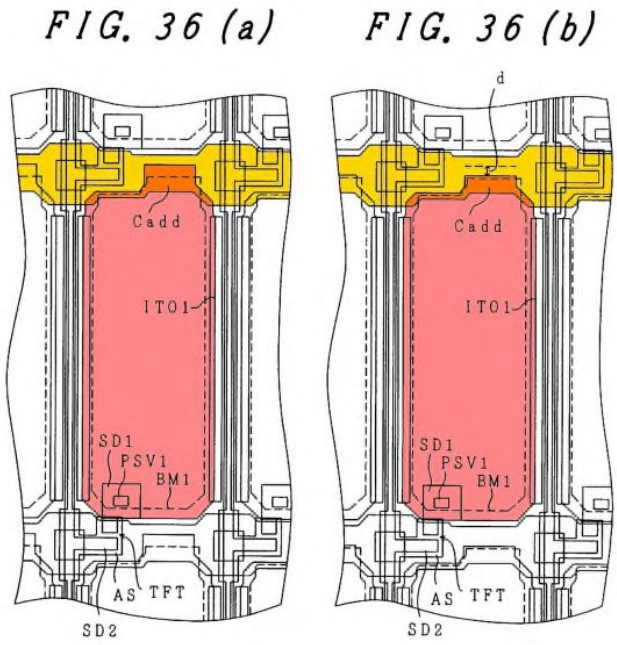
FIG. 4A FIG. 4B FIG. 4C



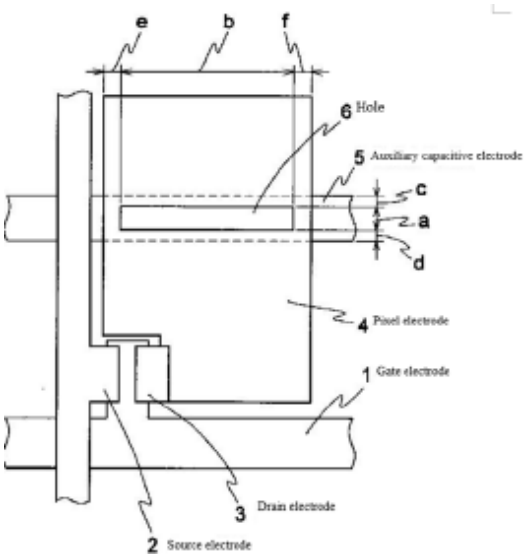
As depicted below in exemplary Figure 2, Nishikawa 1993 similarly teaches, as an example, forming capacitors at the “overlapping portion of the pixel electrode (20) and the auxiliary capacitor electrode (13)” where the capacitance “grow[s] smaller along the way from the input side and [is] smallest at the far end,” “progressively decreas[ing] with each pixel.” *See, e.g.,* Nishikawa 1993, (0018).



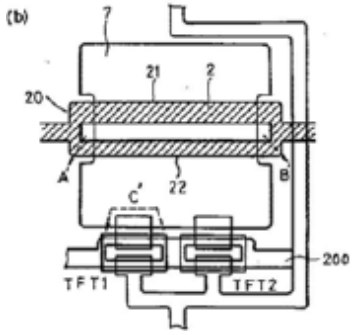
Indeed, by the time of the alleged invention, numerous LCD prior art references had already recognized that it was desirable to gradually adjust the capacitance formed by the overlap between the pixel electrode, insulating layer, and another electrode in order to address the problems discussed in the ’208 patent’s specification, and to improve the LCD display’s picture quality and uniformity. *See, e.g.,* Kuroha, 5:46–48; Watanabe ’214, 7:30–8:3; Nishikawa 1993, (0020); *see also* Ohkawara, 31:2-11 (“In order to decrease the difference in the potential drop component ΔV of the pixel electrode caused by a distortion in the waveform of a scanning signal by adjusting the holding capacity Cadd shown in FIGS. 36(a) and 36(b), the area where the gate signal line GL is superposed on the pixel electrode ITO1 should be decreased by a predetermined amount d starting from the pixels on the side close to the input terminal and going toward the pixels remote from the input terminal thereby to decrease the holding capacity Cadd.”), Figs. 36(a) and 36(b) (reproduced below annotated).



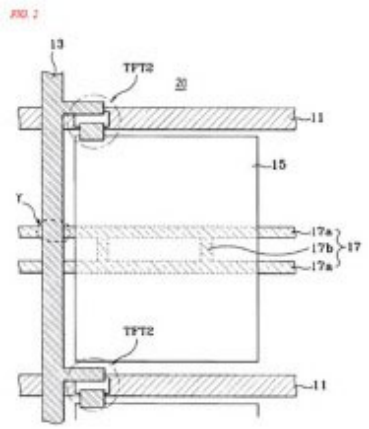
Varying an aperture in the common electrode from one pixel to an adjacent pixel to adjust the capacitor storage capacity in the capacitive accumulation portion was similarly well-known at the time of the purported invention of the ’208 patent. Numerous other LCD prior art references, including, for example, Yamada 2000, Yamada 1995, and Yoo, already disclosed the “aperture” structure claimed in the ’208 patent. For example, Yamada 2000 teaches that the capacitance of an “auxiliary capacitance forming portion, [i.e.,] an overlapping portion between the pixel electrode and an auxiliary capacitance electrode” can be adjusted “by forming a hole in the pixel electrode,” as depicted in exemplary Figure 1 below:



Likewise, as another example, Yamada 1995 discloses a display (pixel) electrode 7, an auxiliary capacitive electrode 22, an insulating film 9 "sandwiched between both electrodes," wherein the auxiliary capacitive electrode contains an aperture, as depicted in exemplary Figure 1(b) below:



And as depicted in exemplary Figure 2 below, Yoo similarly teaches a pixel electrode 15 that overlaps a storage electrode 17 wherein the storage electrode contains an aperture.



Thus, by the time of the alleged invention, numerous LCD prior art references had already recognized that it was desirable to use an aperture, and to vary the size of that aperture, in order to adjust the capacitance formed by the overlap between two electrodes and an insulating layer, in order to address the problems discussed in the ’208 patent’s specification, and to improve the LCD display’s picture quality and prevent display failure. *See, e.g.,* Yamada 2000, [0007]–[0010]; Yamada 1995, [0017]; Yoo at 1–3.

The remaining limitations of the asserted claims of the ’208 patent were similarly well-known, and generally relate to common elements of LCD displays. For example, active matrix LCD devices, including lateral electric field type active matrix LCD devices and twisted nematic (TN) type active matrix LCD devices were well-known in the art. *See, e.g.,* U.S. Patent No. 5,852,485 (“Shimada”); U.S. Patent No. 5,886,762 (“Lee”); U.S. Patent No. 5,907,379 (“Kim”); U.S. Patent No. 5,926,244 (“Takeda”); U.S. Patent No. 6,001,277 (“Ichimura”); U.S. Patent No. 6,028,653 (“Nishida”); Active-Matrix Thin-Film Transistor Liquid-Crystal Displays (Advances in Electronics and Electron Physics Vol. 77); Flat Panel Displays Using Amorphous and Microcrystalline Semiconductor Devices (Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices); Liquid Crystal Displays Using Nematic Liquid Crystals (Flat Panel Displays); Microelectronics in Active-Matrix LCDs and Image Sensors (Electro-Optical

Displays); Fundamentals of Active-Matrix Liquid-Crystal Displays; An Amorphous-Si TFT Addressed 3. 2-in. Full-Color LCD (SID International Symposium Digest of Technical Papers); Active-Matrix-Addressed Color LCDs for Avionics Application (SID International Symposium Digest of Technical Papers); Optics of liquid crystal displays (Pochi).

A POSITA would also have found it obvious to combine Kuroha, Watanabe ’214, or Nishikawa 1993 with other references as shown below.

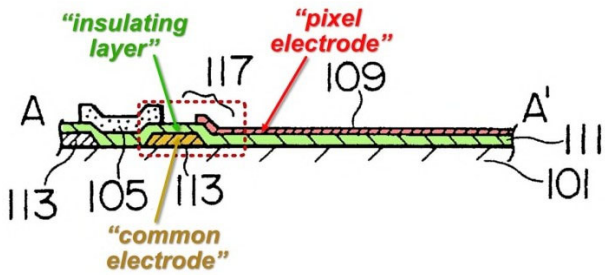
Kuroha, Watanabe ’214, Nishikawa 1993, or Ueda in view of Yamada 2000, Yamada 1995, or Yoo

It would have been obvious to a person of ordinary skill at the time of the invention to incorporate into the LCD display devices taught by Kuroha, Watanabe ’214, Nishikawa 1993, and/or Ueda the aperture structure taught by Yamada 2000, Yamada 1995, and/or Yoo. *See also* Ohkawara, 31:2-11, Figs. 36(a) and 36(b).

As discussed above, Kuroha teaches forming “storage capacitors SC*A*, SC*B* and SC*C*” by overlapping storage electrodes, an insulating layer, and pixel electrodes, where the storage capacitances are gradually reduced as the “overlapped areas . . . are gradually reduced.” *See, e.g.,* Kuroha, 5:10–37. Similarly, Watanabe ’214 teaches a pixel structure containing a storage capacitor formed by overlapping a pixel electrode and another electrode through an interlayer insulation film so that the capacitance formed in the overlap portion “decreases stepwise” as the distance from the signal feeding side increases. *See, e.g.,* Watanabe ’214, 5:29–39. Likewise, Nishikawa 1993 teaches forming capacitors at the “overlapping portion of the pixel electrode (20) and the auxiliary capacitor electrode (13)” where the capacitance “grow[s] smaller along the way from the input side and [is] smallest at the far end,” “progressively decreas[ing] with each pixel.” *See, e.g.,* Nishikawa 1993, (0018). *See also* Ueda at 1:44-56, 9:38-45 (“Moreover, the storage capacitor 117 is formed through the gate insulation layer 111 at the portion where the shield electrode 113 is

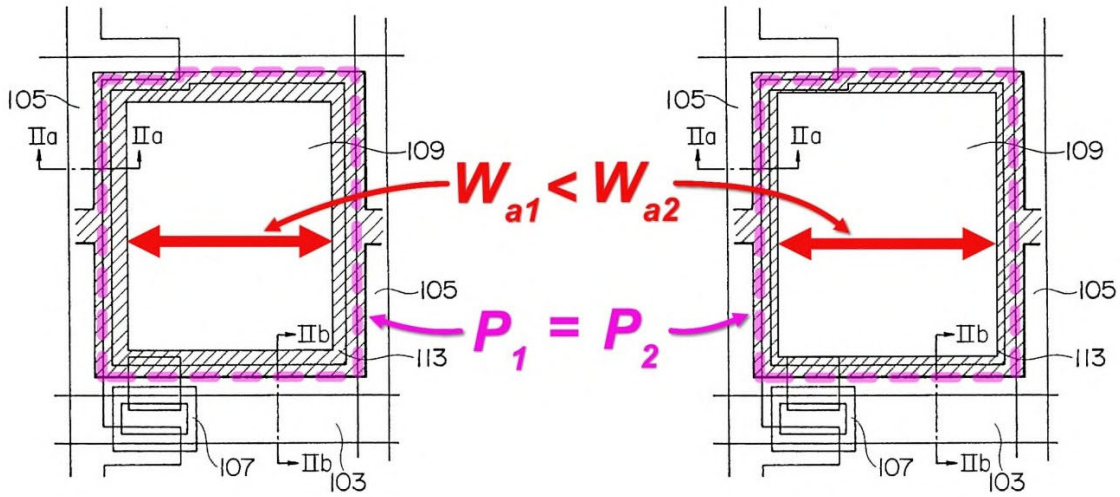
overlaid with the pixel electrode 109. In other words, since the shield electrode 113 is used in common with the storage capacitor electrode of the storage capacitor 117, the construction and production process is simpler than the construction with necessity of an extra storage capacitor electrode."), Fig. 2(a) (reproduced below, annotated.

FIG. 2(a)



A POSITA would have found obvious and known that it was advantageous to modify any of Kuroha, Watanabe '214, Nishikawa 1993, or Ueda to form apertures of increasing size to gradually decrease the storage capacitances across pixels, as taught by Yamada 2000, Yamada 1995, and Yoo. This is consistent, for example, with the object of the invention of Kuroha, *see, e.g.,* Kuroha, 1:59–61 ("capacitance of the storage capacitor is changed in accordance with a distance between the pixel"); *id*., 1:47–50 ("object of the invention [is] to provide an LCD apparatus capable of suppresing the fluctuation of feed-through voltage"); the object of the invention of Watanabe '214, *see, e.g.,* Watanabe '214, 5:29–39 ("an auxiliary capacity formed in the overlap portion . . . can be varied . . . in such a manner that the auxiliary capacity decreases stepwise"); and the object of the invention of Nishikawa 1993, *see, e.g.,* Nishikawa 1993, (0018) ("the auxiliary capacitors formed at the overlapping portion of the pixel electrode (20) and the auxiliary capacitor electrode (13) are formed with the relationship $C_{SCA} > C_{SCB} > C_{SCC}$"); *id*., (0011) ("[B]y changing the size of the auxiliary capacitor electrodes on the input side and the far end of the gate signal, a liquid crystal display device was achieved with greatly improved charging

characteristics"). A POSITA would have found it obvious to form apertures, as taught by, for example, Yamada 2000, Yamada 1995, and Yoo, to modify the storage capacitance, as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results. Similarly, it would have been obvious to change the width of the aperture of Ueda's pixels to adjust the capacitance as taught by Ohkawara.



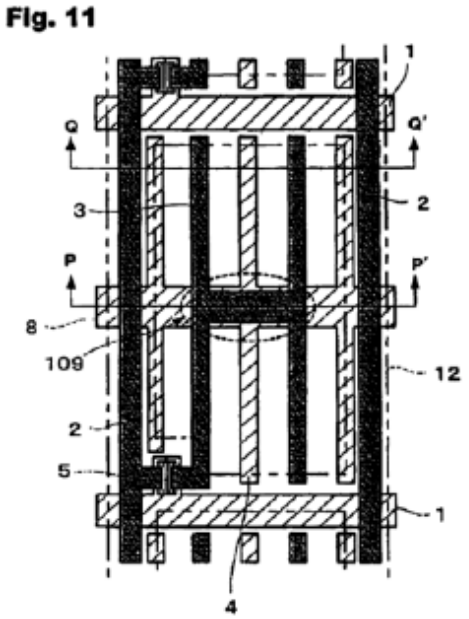
Moreover, the abovementioned modification would have constituted nothing more than the "application of a known technique," *e.g.*, forming holes or apertures in an electrode layer as disclosed by, for example, Yamada 2000, Yamada 1995, and/or Yoo "to a piece of prior art ready for the improvement," *e.g.*, the pixel structure disclosed by, for example, Kuroha, Watanabe '214, Nishikawa 1993, and/or Ueda, particularly given a POSITA's general knowledge and understanding that storage capacitance is directly related to the area of overlap between two electrodes (*e.g.*, pixel electrode and common electrode). *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so).

It would have been straightforward for a POSITA, and well within the ability of a POSITA, to modify the pixel structures of Kuroha, Watanabe ’214, Nishikawa 1993, and/or Ueda in this manner. A POSITA would have understood that as exemplary prior art references Yamada 2000, Yamada 1995, and Yoo are directed to display devices (and specifically, LCD display devices), the improvements described therein could be readily implemented in the LCD display devices taught by, for example, Kuroha, Watanabe ’214, and Nishikawa 1993. A person of ordinary skill in the art would have been motivated to apply a known improvement (as taught, for example, in Yamada 2000, Yamada 1995, and Yoo) to a known LCD display ready for improvement in this manner to yield predictable results. It would have been obvious for a person of ordinary skill in the art to try the combination with a reasonable expectation of success given the design need and market pressure to improve LCD displays.

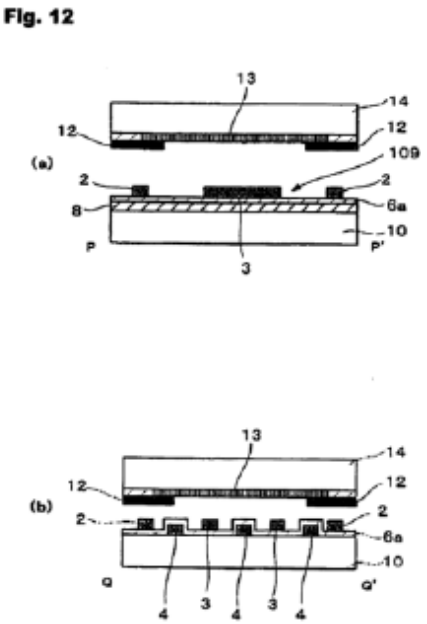
(5) U.S. Patent No. 6,850,303

The asserted claims of the ’303 patent relate to a liquid crystal display device structure, where “a pixel electrode disposed in a region defined by two adjacent gate wirings and two adjacent source wiring,” a “common wiring” is “formed between the two adjacent gate wirings,” a “storage capacity electrode” is “electrically connected to the pixel electrode,” and “the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer.” ’303 patent, 13:14–41.

Pixel regions being defined by adjacent gate wirings and source wirings, and pixel electrodes, common wirings, and storage capacity electrodes connected to pixel electrodes being disposed in pixel regions, were very well-known in the prior art. Indeed, the applicant admitted that the prior art IPS mode liquid crystal display devices included these structures, as shown in Figures 11 and 12 below. *See id.,* 1:38–2:46.



PRIOR ART



PRIOR ART

The additional feature of independent claim 1 was also well-known in the prior art. Numerous other LCD prior art references, including, for example, Iizuka, Nagahiro, and Ikeda, disclosed layering of a pixel electrode, a storage capacity electrode, and a common wiring, including the only limitation not admitted to be in the prior art by the ’303 patent itself: “wherein the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer.” *See, e.g.,* Exs. E-02 (Iizuka claim chart); E-03 (Nagahiro claim chart); E-05 (Ikeda claim chart).

Additionally, under Bishop Display’s interpretation of claim 1, ’303 patent’s claimed structure was also taught or suggested by numerous other LCD prior art references, including, for example, Iizuka, Nagahiro, Nakagawa, Ikeda, and Fujiwara. For example, the prior art was replete with teachings of pixel structures where the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer, under Bishop Display’s apparent interpretation of the terms in claim 1, including “common

wiring," "common electrode," "storage capacity electrode," and "layered so as to hold . . . in between . . ."

The asserted claims of the '303 patent also would have been obvious to a POSITA in view of the following combinations.

Shimada in view of Iizuka

Shimada discloses several types of IPS-type pixel structures with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See, e.g.,* Shimada, Figs. 1, 11, 15, 17.

Iizuka discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See, e.g.,* Iizuka, Fig. 3.

A POSITA would have recognized that Iizuka's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS pixel structures disclosed in Shimada. This would have constituted nothing more than "application of a known technique," *i.e.,* overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Iizuka's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain predictable results. Specifically, a POSITA would have recognized that incorporating Iizuka's electrodes formed at different metal layers would have predictable results, including the creation of additional

storage capacitance, such that the potential of the pixel electrode would not fluctuate due to parasitic capacitance or off-leak current from the TFT, or crosstalk due to an adjacent signal line, thus improving display quality. This combination of Shimada and Iizuka could have been done according to known methods to achieve these predictable results.

Iizuka itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate during a non-selection period due to parasitic capacitance or off-leak current from a TFT, or crosstalk due to an adjacent signal line. Iizuka, [0004]. Thus, it is common to form auxiliary capacitance in parallel with a pixel electrode to suppress the decrease in contrast ratio and deterioration in image quality due to these effects. *Id.* By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio or increase in pixel defects, also resulting in increased manufacturing yield. *Id.,* [0013]–[0016], [0048]–[0052], [0069].

In addition, a POSITA would have recognized that Shimada and Iizuka both concern improving image display in active-matrix type liquid crystal displays, *see, e.g.,* Shimada, Abstract; Iizuka, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Shimada in view of Nagahiro

Shimada discloses several types of IPS-type pixel structures with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See, e.g.,* Shimada, Figs. 1, 11, 15, 17.

Nagahiro discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode

for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See*, *e.g.*, Nagahiro, Figs 1, 3.

A POSITA would have recognized that Nagahiro's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS pixel structures disclosed in Shimada. This would have constituted nothing more than "application of a known technique," *i.e.,* overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Nagahiro's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain predictable results. Specifically, a POSITA would have recognized that incorporating Nagahiro's electrodes formed at different metal layers would have predictable results, including the creation of additional storage capacitance, such that the potential of the pixel electrode would not fluctuate due to parasitic capacitance or off-leak current from the TFT, or crosstalk due to an adjacent signal line, thus improving display quality. This combination of Shimada and Nagahiro could have been done according to known methods to achieve these predictable results.

Nagahiro itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate during a non-selection period due to parasitic capacitance or off-leak current from a TFT, or crosstalk due to an adjacent signal line. Thus, it is common to form auxiliary capacitance in parallel with a pixel electrode to suppress the decrease

in contrast ratio and deterioration in image quality due to these effects. By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio or increase in pixel defects, also resulting in increased manufacturing yield. Nagahiro, 3:11–63, 6:19–39, 7:44–65.

In addition, a POSITA would have recognized that Shimada and Nagahiro both concern improving image display in active-matrix type liquid crystal displays, *see*, *e.g.*, Shimada, Abstract; Nagahiro, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Shimada in view of Ikeda

Shimada discloses several types of IPS-type pixel structures with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See*, *e.g.*, Shimada, Figs. 1, 11, 15, 17.

Ikeda discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See*, *e.g.*, Ikeda, Figs 3B, 4B.

A POSITA would have recognized that Ikeda's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS pixel structures disclosed in Shimada. This would have constituted nothing more than "application of a known technique," *i.e.*, overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways

to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ikeda's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain predictable results. Specifically, a POSITA would have recognized that incorporating Ikeda's electrodes formed at different metal layers would have predictable results, including the creation of additional storage capacitance such that flicker and crosstalk can be eliminated while maintaining high aperture ratio, thus improving display quality. This combination of Shimada and Ikeda could have been done according to known methods to achieve these predictable results.

Ikeda itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate. To prevent flicker or crosstalk, it is necessary to provide as large a storage capacitance as possible. But as the storage capacitance area gets larger, the aperture ratio decreases. By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio, resulting in a high picture quality. *See*, *e.g.*, Ikeda, 1:46–68, 4:3–13, 5:41–49, 5:66–6:13, 8:1–8.

In addition, a POSITA would have recognized that Shimada and Ikeda both concern improving image display in active-matrix type liquid crystal displays, *see*, *e.g.*, Shimada, Abstract; Ikeda, Abstract, 1:58–2:23, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Nakagawa in view of Iizuka

Nakagawa discloses an IPS-type pixel structure with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See*, *e.g.*, Nakagawa, Figs. 1, 2.

Iizuka discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See*, *e.g.*, Iizuka, Fig. 3.

A POSITA would have recognized that Iizuka's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS pixel structures disclosed in Nakagawa. This would have constituted nothing more than "application of a known technique," *i.e.*, overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Iizuka's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain predictable results. Specifically, a POSITA would have recognized that incorporating Iizuka's electrodes formed at different metal layers would have predictable results, including the creation of additional storage capacitance, such that the potential of the pixel electrode would not fluctuate due to parasitic capacitance or off-leak current from the TFT, or crosstalk due to an adjacent signal line, thus improving display quality. This combination of Shimada and Iizuka could have been done according to known methods to achieve these predictable results.

Iizuka itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate during a non-selection period due to parasitic capacitance or off-leak current from a TFT, or crosstalk due to an adjacent signal line. Iizuka, [0004]. Thus, it is common to form auxiliary capacitance in parallel with a pixel electrode to suppress the decrease in contrast ratio and deterioration in image quality due to these effects. *Id.* By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio or increase in pixel defects, also resulting in increased manufacturing yield. *Id.,* [0013]–[0016], [0048]–[0052], [0069].

In addition, a POSITA would have recognized that Nakagawa and Iizuka both concern improving image display in active-matrix type liquid crystal displays, *see, e.g.,* Nakagawa, [0016]–[0018]; Iizuka, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Nakagawa in view of Nagahiro

Nakagawa discloses an IPS-type pixel structure with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See*, *e.g.*, Nakagawa, Figs. 1, 2.

Nagahiro discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See*, *e.g.*, Nagahiro, Figs 1, 3.

A POSITA would have recognized that Nagahiro's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS

pixel structures disclosed in Nakagawa. This would have constituted nothing more than "application of a known technique," *i.e.*, overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Nagahiro's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain predictable results. Specifically, a POSITA would have recognized that incorporating Nagahiro's electrodes formed at different metal layers would have predictable results, including the creation of additional storage capacitance, such that the potential of the pixel electrode would not fluctuate due to parasitic capacitance or off-leak current from the TFT, or crosstalk due to an adjacent signal line, thus improving display quality. This combination of Nakagawa and Nagahiro could have been done according to known methods to achieve these predictable results.

Nagahiro itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate during a non-selection period due to parasitic capacitance or off-leak current from a TFT, or crosstalk due to an adjacent signal line. Thus, it is common to form auxiliary capacitance in parallel with a pixel electrode to suppress the decrease in contrast ratio and deterioration in image quality due to these effects. By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio or

increase in pixel defects, also resulting in increased manufacturing yield. Nagahiro, 3:11–63, 6:19–39, 7:44–65.

In addition, a POSITA would have recognized that Nakagawa and Nagahiro both concern improving image display in active-matrix type liquid crystal displays, *see, e.g.,* Nakagawa, [0016]–[0018]; Nagahiro, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Nakagawa in view of Ikeda

Nakagawa discloses an IPS-type pixel structure with pixel electrodes, common wiring, and storage capacity electrodes within the pixel region. *See*, *e.g.*, Nakagawa, Figs. 1, 2.

Ikeda discloses a multi-layer structure of electrodes, including a pixel electrode in one metal layer, an electrode for generating storage capacitance in a lower metal layer, and an electrode for generating additional capacitance in a yet lower metal layer, where the pixel electrode is electrically connected to the additional capacitance electrode. *See*, *e.g.*, Ikeda, Figs 3B, 4B.

A POSITA would have recognized that Ikeda's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance could be incorporated into the IPS pixel structures disclosed in Nakagawa. This would have constituted nothing more than "application of a known technique," *i.e.*, overlapping a set of electrodes at three different metal layers, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ikeda's technique of forming a set of electrodes at three different metal layers for increasing storage capacitance would have been nothing more than a simple substitution of one known element for another to obtain

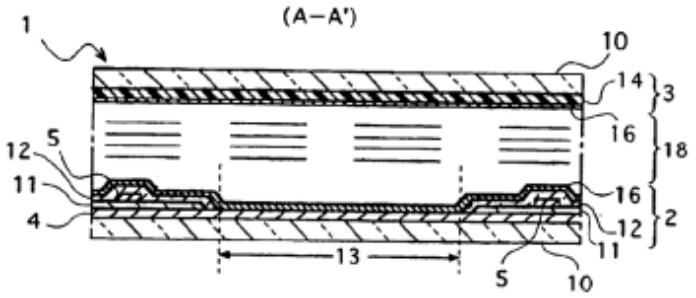
predictable results. Specifically, a POSITA would have recognized that incorporating Ikeda's electrodes formed at different metal layers would have predictable results, including the creation of additional storage capacitance such that flicker and crosstalk can be eliminated while maintaining high aperture ratio, thus improving display quality. This combination of Nakagawa and Ikeda could have been done according to known methods to achieve these predictable results. Ikeda itself also provides a specific teaching, suggestion, or motivation for such combination. For example, in an active matrix type LCD device, the potential written to a pixel electrode during a selection period may fluctuate. To prevent flicker or crosstalk, it is necessary to provide as large a storage capacitance as possible. But as the storage capacitance area gets larger, the aperture ratio decreases. By using a three-layered structure, sufficient auxiliary capacitance can be generated without increasing the area of overlap in the pixel electrodes, resulting in increased capacitance without a decrease in aperture ratio, resulting in a high picture quality. *See*, *e.g.*, Ikeda, 1:46–68, 4:3–13, 5:41–49, 5:66–6:13, 8:1–8.

In addition, a POSITA would have recognized that Nakagawa and Ikeda both concern improving image display in active-matrix type liquid crystal displays, *see, e.g.,* Nakagawa, [0016]–[0018]; Ikeda, Abstract, 1:58–2:23, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

(6) U.S. Patent No. 6,906,769

The '769 patent relates to an active matrix liquid crystal display (LCD) capable of "restraining occurrence of display unevenness." '769 patent, Abstract, 1:5–8. The claims are directed to a LCD in which gate signal lines (acting as a "first conductive member") are formed so as to be "in partial contact with [an] alignment layer and to which a negative voltage is applied."

Id., cl. 1. Figure 2, shown below, shows an LCD structure having a region (13) where the gate signal line 4 is in contact with the alignment layer 16.



'769 Patent, Fig. 2. The specification states that applying a negative voltage to the gate signal line will "generate ions within the liquid crystal layers," thereby "restraining display unevenness attributable to ions which have been locally generated with the liquid crystal layer." According to the patent, the more even distribution of ions in the liquid crystal display that results from this approach reduces "display unevenness," thereby "displaying satisfactory images for a long time." *Id.,* 3:36–40, 4:5–11.

However, the '769 patent's claimed structure was well-known in the prior art. During prosecution, the Examiner found that the prior art taught an LCD with a first conductive member formed so as to be in partial contact with alignment layer, as claimed. '769 File History, 50 (December 31, 2003 Rejection at 3). The Examiner further found that "it would have been obvious ... to apply a negative voltage to the Fukami et al. first conductive member as shown by Tanuma et al. in order to prevent the display unevenness and image persistence by long-term use (*see* abstract)." *Id.*, 50–51 (December 31, 2003 Rejection at 3–4). The applicants did not contest these findings. Instead, they amended the claims to require that the first conductive member must be (1) gate signal lines, (2) formed on a first insulating substrate, and (3) interposed between that substrate and a corresponding alignment layer. *Id*., 34 (March 29, 2004 Amendment at 2). With these additional limitations, the claims were allowed.

However, prior art that was not before the patent office discloses an LCD having the same structural arrangement as specified by the allowed claims.

For example, Komatsu teaches such an LCD having gate signal lines (blue) that are formed between a first insulating substrate (green) and a corresponding alignment layer (red), and that are in partial contact with the alignment layer. *See* Komatsu, Figs. 11b and 11c (reproduced below, annotated).

FIG.11b

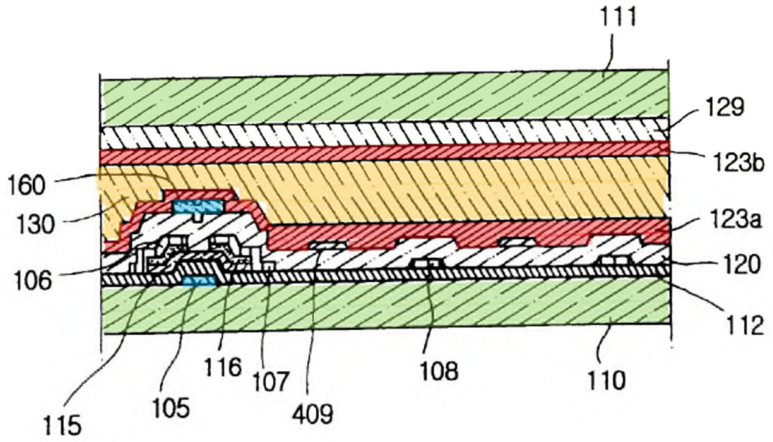
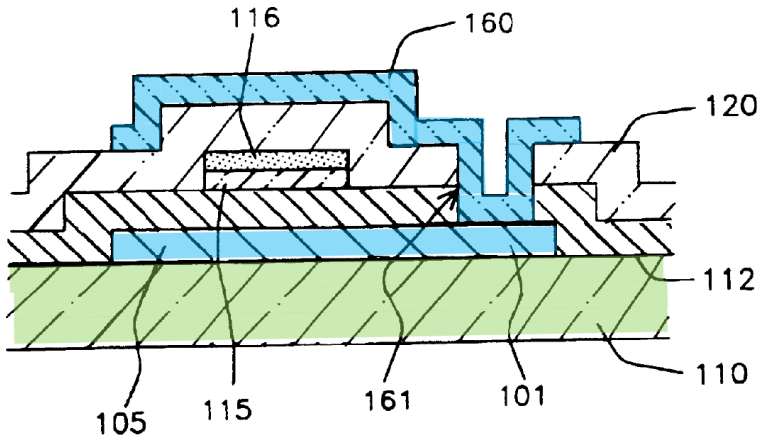


FIG.11c



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Bishop Display's Exhibit 2007
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Similarly, Shimada also teaches such an LCD having gate signal lines that are formed between a first insulating substrate and a corresponding alignment layer, and that are in partial contact with the alignment layer. *See* Shimada, Figs. 1(b), 3(b).

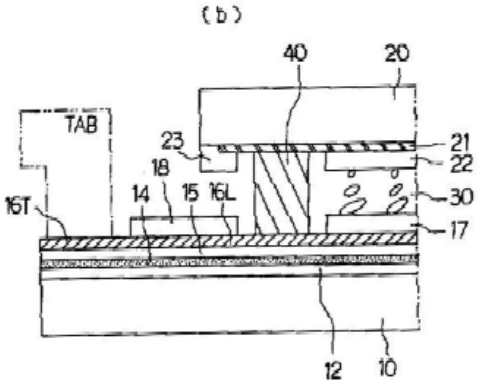


Fig. 1

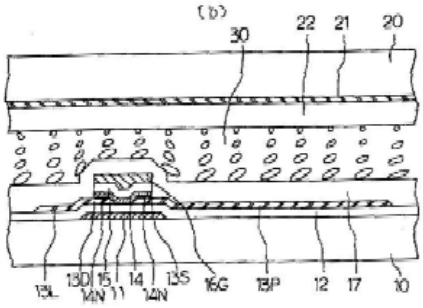


Fig. 3

SakamotoJP407 and SakamotoUS678 also disclose this claimed LCD structure—having gate signal lines that are formed between a first insulating substrate and a corresponding alignment layer, and that are in partial contact with the alignment layer. *See, e.g.,* SakamotoJP407, Figs. 1–3, 11.

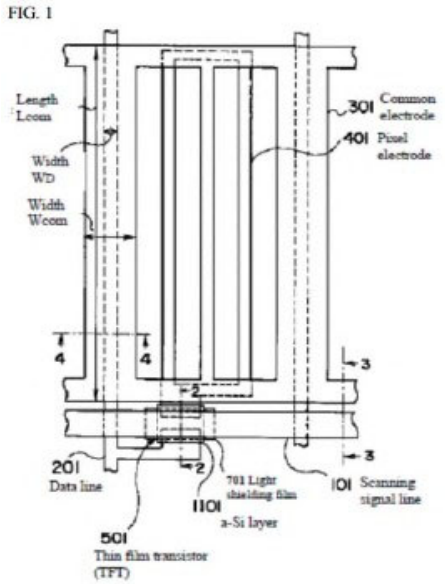


Fig. 1

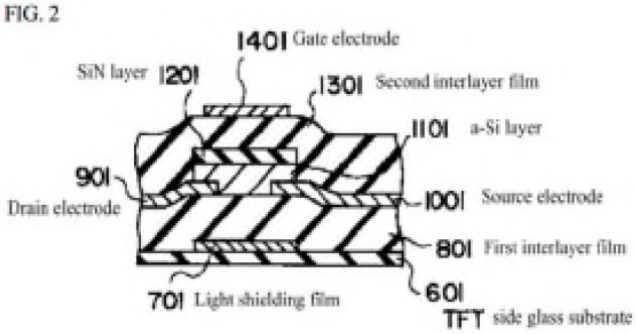


Fig. 2

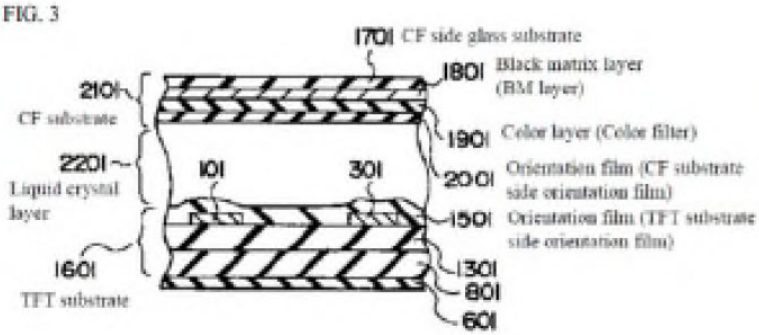


Fig. 3

【図１１】

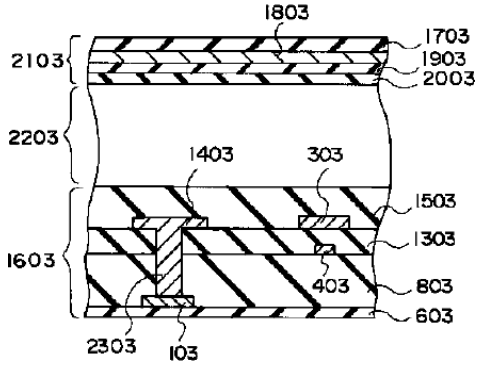


Fig. 11

OtaJP127 also discloses this LCD structure, with gate signal lines that are formed between a first insulating substrate and a corresponding alignment layer, and that are in partial contact with the alignment layer. *See, e.g.,* OtaJP127 Figs. 1– 3, 7-8.

図 1

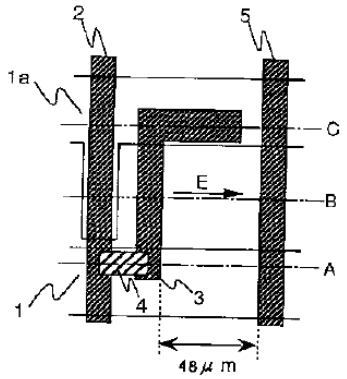


Fig. 1

図 2

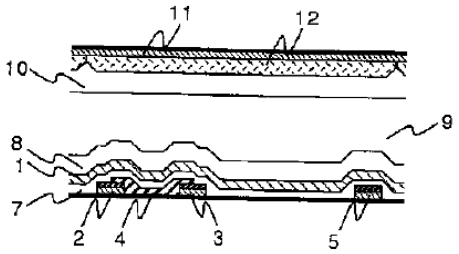


Fig. 2

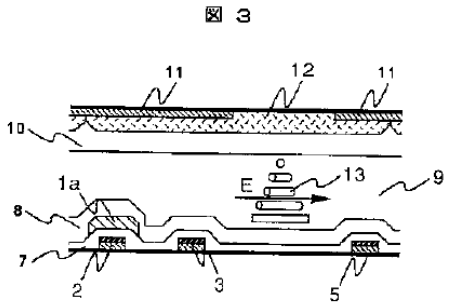


Fig. 3

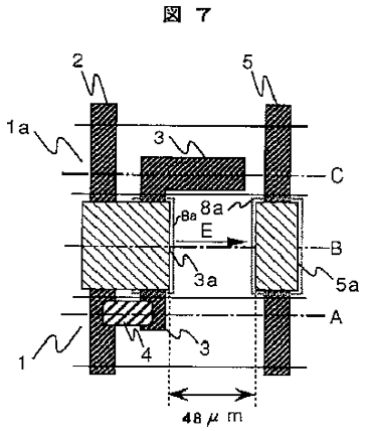


Fig. 7

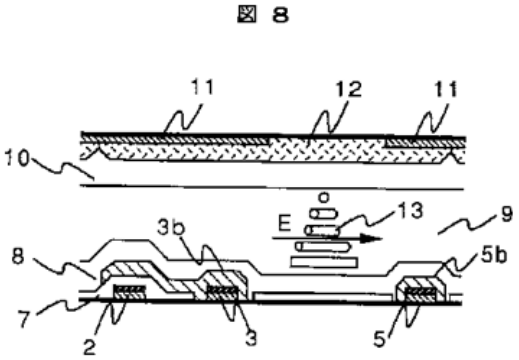


Fig. 8

As shown above and in further detail in the corresponding claim charts, the structures of Komatsu, Shimada, SakamotoJP407/US678, and OtaJP127 likewise teach limitations of dependents claims 4, 5-7, 9 and 14, including a light blocking layer formed on a first or second

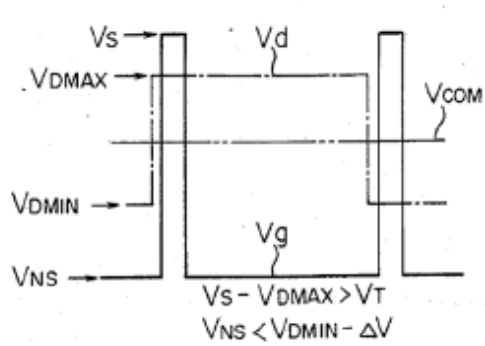
insulating substrate and overlapping with the first conductive member/gate signal lines in a plan view.

Applying a negative voltage to the gate signal lines of transistors, including TFTs used in these types of structures, was well-known and recognized as a beneficial way to operate such an LCD.

Configuring a field effect transistor such that its gate has a negative voltage has been known in the art since at least the 1980s. *See*, *e.g.*, Ralph J. Smith, Electronics: Circuits and Devices 2d ed. 1980) at 147, Fig. 6. 2.

This approach was also known in the art for TFTs in LCDs having structures like those taught by Komatsu, Shimada, SakamotoJP407/US678, and OtaJP127. Kaneko, for instance, teaches a similar structure in which a negative voltage is applied to the gate of the TFT during its off state to improve the image quality of the display. *See* Kaneko, 2:65–3:2 (teaching that if "the relation of $V_{NS} < V_{DMIN} - \Delta V$ is satisfied, the source voltage of the TFT can be prevented from lowering than the gate voltage, thereby realizing a sufficient signal holding without any erroneous turn-on of the TFT.").

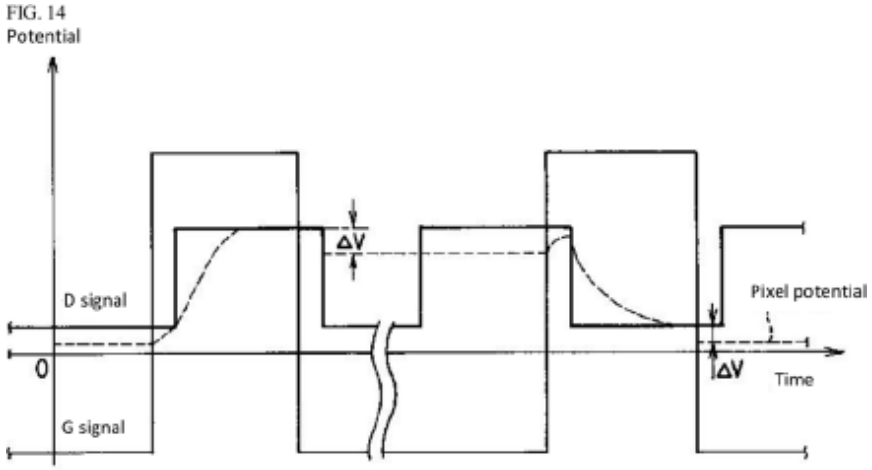
FIG. 3



Id., Fig. 3. Figs. 9A–9C. Exemplary Figures 3 and 9 disclose embodiments in which the gate voltage in the OFF state is lower than the lowest value of the drain and source voltages and

lower than VCOM, which, as the specification of Kaneko further teaches, can be assumed to be 0V. *See id.* at 1:29–30.

Watanabe JP ’794 further illustrates applying a negative voltage to the TFT that it was common to implement Kaneko’s voltage scheme using a negative Gate off voltage. *See* Watanabe JP ’794, [0035] (disclosing that the gate off voltage in Fig. 14 is -10 to -15 V), Fig. 14 (showing gate signal in the OFF state being negative and lower than the lowest value of the data signal or pixel potential).



Similarly, Kimura further illustrates applying a negative voltage to the TFT, and the use of a negative voltage applied to gate electrodes. *See, e.g.*, Kimura, 5:26-39 (gate electrodes are constructed from scanning lines), 6:44-60 (“scanning line voltage Vg” has values ranging -9.4V to -14.0V in the off state), Fig. 4 (showing Vg in the OFF state being negative and lower than the lowest value of the data signal or pixel potential).

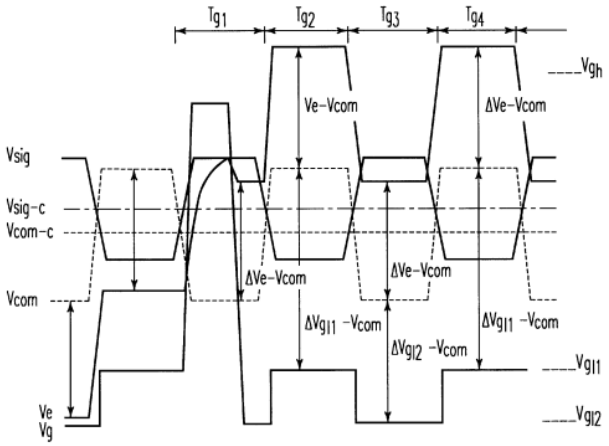


FIG. 4

It also would have been obvious at the time of the alleged invention of the ’769 Patent to implement the LCD displays having the operating voltages of Kaneko, Watanabe, or Kimura using a structure where a gate signal line are in partial contact with an alignment layer—as shown, for example, in Shimada and Sakamoto.

Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine and combinations in IPR2022-00564.

Komatsu, Shimada, SakamotoJP407/US678 or OtaJP127, alone or in view of Kaneko, Watanabe, and/or Kimura

A POSITA would have found it obvious and known that it was advantageous to apply the gate signal lines of Komatsu, Shimada, SakamotoJP407/US678, or OtaJP127 with a negative voltage. *First*, doing so would have constituted one of a finite number of options (i.e., as operating voltage for the gate TFT of an LCD display) that it would have been obvious to try with a reasonable expectation of success in producing an effective and reliably functioning LCD display.

Second, a POSITA would have been motivated to apply to the gate signal lines of Shimada or Sakamoto with a “negative voltage,” as taught in Kaneko, Watanabe, or Kimura, because doing so “prevent[s] ... cross-talk resulting from erroneous turn-on of the TFT ... thereby further

improving the image quality of the display." *See* Kaneko, 4:39–37; *see also id*., 2:65–3:2. Accordingly, applying the gate signal lines of Komatsu, Shimada, SakamotoJP407/US678, or OtaJP127 with a "negative voltage" would have constituted nothing more than the "application of a known technique" (*i.e.,* operating the TFT of an LCD display using a negative gate off voltage) to a known device (*i.e.,* the LCD display of Komatsu, Shimada or SakamotoJP407/US678) to achieve predictable results (improved image quality for the LCD display). *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so).

A POSITA also would have known that implementing the above-described voltage scheme by applying a negative voltage to the gate in the OFF state, would have provided further desirable advantages. A POSITA would have known, for example, that for a given range of voltage values for the drain, gate, and source, a negative gate OFF state voltage would have allowed the other operating voltages of the TFT to be kept lower, thereby making the device more efficient in operation. Alternatively, a POSITA would have known that, keeping other operating voltages the same, lowering the gate OFF state voltage to a negative voltage would have provided further assurances of preventing cross-talk and erroneously turning on the TFT. In this regard, applying a negative voltage to the TFT gate in the OFF state would have involved the use of a known technique to improve an active LCD in the same way as had been done with TFTs in the past. In addition, a POSITA would have appreciated that applying a negative voltage as the gate OFF voltage could counteract undesirable electrochemical corrosion of the metal wiring due to a battery reaction. *See e.g.*, Shimada, [0009]–[0010]. Applying a "negative voltage" also would have been an approach that was obvious to try, in that it would have involved nothing more than a choice

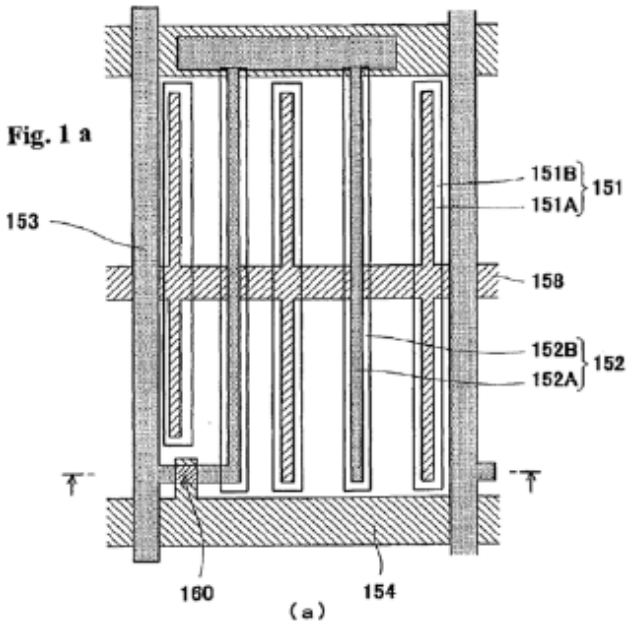
from among a finite number of identified, predictable solutions, with a reasonable expectation of success. It would have been also obvious to implement the same general LCD display of Kaneko, Watanabe, or Kimura with operating voltages disclosed therein, with a "top-gate" TFT structure, as shown in Komatsu, Shimada, SakamotoJP407/US678, or OtaJP127 which results in the gate signal lines being in partial contact with the alignment layer. *First*, top-gate TFT structures were a well-known LCD design implementation at the time of the alleged invention. In fact, transistors with gates on the top layer had been known since at least the 1980s. *See* Smith at 146, Fig. 6. 1. Indeed, top-gate structures and bottom-gate structures were recognized as alternative methods for implementing LCD TFTs. *Compare* SakamotoJP407, [0048] ("The gate electrode 1401 is formed on the second interlayer film 1301 so as to be positioned above the channel, and is electrically connected to the scanning signal line 101. Note that as understood from FIG. 2, the TFT 501 in the present embodiment has a top gate structure, and thus is generally referred to as a positive staggered type.") *with id.*, [0120] (disclosing an alternative embodiment of "an inversely staggered type having a bottom gate structure."). Accordingly, implementing the same general LCD display of Kaneko, Watanabe, or Kimura using a "top-gate" TFT structure would have been obvious to try. A top gate is also one of a finite number of options (*e.g.*, having the gate on the top or the bottom of the TFT of an LCD display) that would have been obvious to try with a reasonable expectation of success in achieving an effectively functioning and efficiently manufactured device.

Furthermore, a POSITA would have been motivated to implement the same general LCD display of Kaneko, Watanabe, or Kimura with the operating voltages disclosed therein, using a "top-gate" TFT structure as disclosed in Komatsu, Shimada, SakamotoJP407/US678, or OtaJP127 in order to lower the manufacturing cost associated with the display. *See e.g.,* Shimada, [0004] ("When positive staggered TFTs with the gate on the upper layer is used, the TFT substrate can be

manufactured with only three masks, resulting in low cost."). Accordingly, implementing the LCD display of Kaneko, Watanabe, or Kimura with a "top-gate" TFT structure would have constituted nothing more than the "application of a known technique" (*i.e.,* manufacturing the TFT of an LCD display to have a top-gate structure) to a known device ready for improvement (*i.e.,* the LCD display of either Kaneko, Watanabe, or Kimura, having the operating voltages disclosed therein) to achieve predictable results (lower manufacturing costs). *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so).

(7) U.S. Patent No. 7,414,682

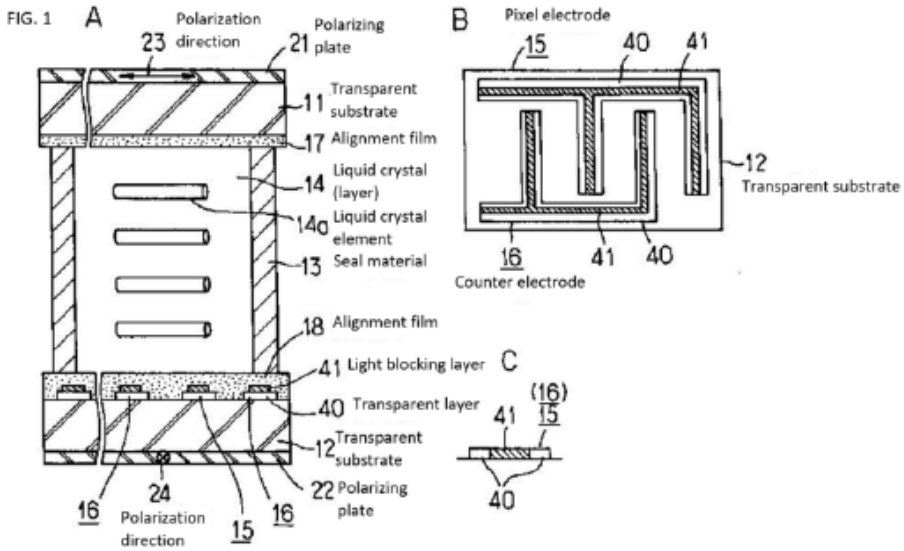
The asserted claims of the '682 patent are directed to a liquid crystal display where "at least one of the scanning signal lines, the video signal lines, the pixel electrode, or the common electrode is at least partially constituted by a light-transmitting conductive layer and a light-non-transmitting conductive layer" and "a width of the light-transmitting conductive layer is wider than a width of the light-non-transmitting layer." '682 Patent, Claim 7. Figure 1 depicts this structure:



The ’682 patent states that a “counter electrode 151 is constituted by two layers including a non-transparent conductive layer 151A . . . and a transparent conductive layer 151B constituted by a transparent electric conductor, for example, ITO.” ’682 patent, 11:37–42. The ’682 patent further states that “the counter electrode 151, when seen in a plan view, an edge portion thereof is constituted by the transparent conductive layer 151B, and a central portion thereof is constituted by the non-transparent conductive layer 151A.” *Id.*, 11:47–52. The ’682 patent states that a pixel electrode may also have “a two-layer structure including a non-transparent conductive layer 152A and a transparent conductive layer 152B.” *Id.*, 13:60–65. According to the ’682 patent, forming an electrode in this manner with both non-transparent and transparent layers allegedly improves luminance, light recycling efficiency of the backlight, and an average contrast of the display. *Id.*, 13:19–30.

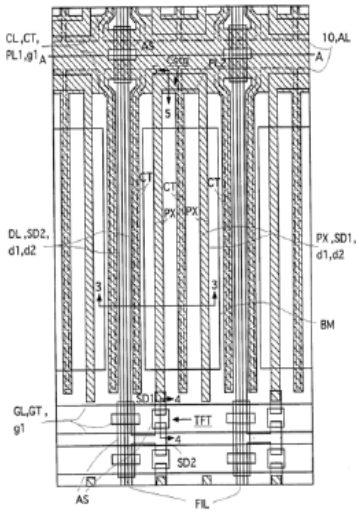
However, the ’682 patent’s claimed structure was well-known in the prior art. Numerous prior art references, including, for example, Matsumoto, Ohta ’454, Kubota, Yamaji, and Shimada already disclosed forming electrodes with both a non-transparent layer and a transparent layer. For example, exemplary Figure 1 of Matsumoto depicts a pixel electrode 15 and a counter electrode

16 that "have a two-layered structure with a light blocking layer 41 overlapping on a transparent layer 40." Matsumoto, [0014].

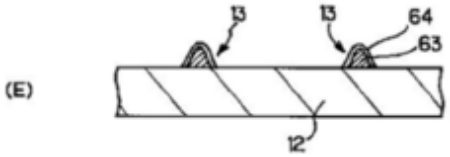


Similarly, exemplary Figure 24C of Ohta '454 depicts a counter electrode CT that is "constituted from of double wiring, in this example, a wire of an ITO film 11 is formed covering the wiring of the Al layer 10." Ohta '454, 51.

FIG.24C

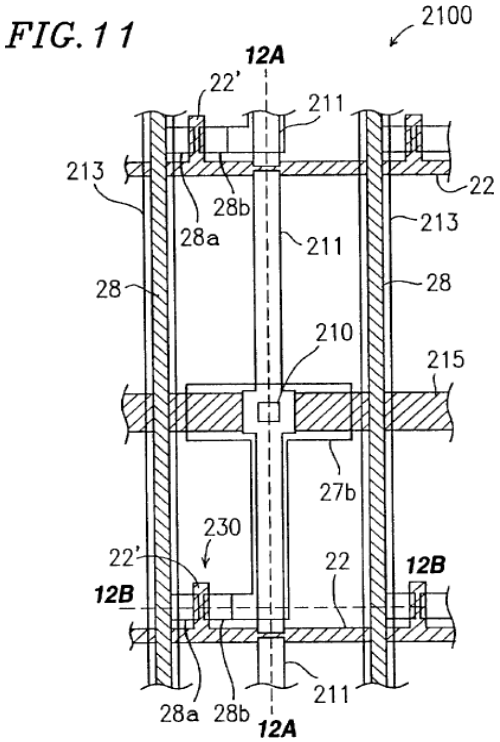


Similarly, exemplary Figure 4 of Kubota depicts a common electrode 13 that formed of a "metal thin film" covered by "a transparent thin film such as indium tin oxide (ITO)." Kubota, [0018].



Similarly, Yamaji describes "[t]he pixel electrode 66 has a light shielding layer 66a formed of a conductive material having a large absorbance at the center, and a transparent layer 66b formed of a transparent conductive material such as ITO at the periphery."

Similarly, exemplary Figure 11 of Shimada discloses a "transparent conductive film 27b" and "picture element electrode 211 [which] is electronically connected to the transparent conductive film 27b…" Shimada, 21:66-22:6.



The remaining limitations of the asserted claims of the ’682 patent were similarly well-known, and generally relate to common elements of LCD displays.

Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00505.

A POSITA would have found the asserted claims obvious in view of the combinations discussed below as well as those in IPR2022-00505.

Kubota in view of Matsumoto

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a “metal thin film.” *See*, *e.g*., Kubota, [0018]; *see also* Figs. 1, 4. Kubota further discloses that a pixel electrode 17 is formed in the same manner. *See*, *e.g.*, Kubota, [0021].

Matsumoto discloses using “chromium or chromium oxide,” along with ITO, for a counter electrode and a pixel electrode. *See*, *e.g.*, Matsumoto, [0017].

A POSITA would have understood that the “chromium or chromium oxide” disclosed in Matsumoto could have been used as the “metal thin film” disclosed in Kubota. This would have constituted nothing more than the “application of a known technique,” *i.e.,* the use of chromium or chromium oxide for an electrode, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). A POSITA would have found it obvious to use chromium or chromium oxide as a “metal thin film,” as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Kubota and Matsumoto are directed to improving image display in an in-plane switching (IPS) mode liquid crystal display,

see, e.g., Kubota, [0004]–[0005]; Matsumoto, [0017], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Kubota in view of Ohta '454

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a "metal thin film." *See*, *e.g.*, Kubota, [0018]; *see also* Figs. 1, 4. Kubota disclose that a pixel electrode 17 is formed in the same manner. *See*, *e.g.*, Kubota, [0021].

Ohta '454 discloses using AL (aluminum) layer 10, along with an ITO film 11, for a counter electrode. *See*, *e.g.*, Ohta '454, 50–51.

A POSITA would have understood that the aluminum disclosed in Ohta '454 could have been used as the "metal thin film" disclosed in Kubota. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of aluminum for an electrode, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). A POSITA would have found it obvious to use aluminum as a "metal thin film," as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Kubota and Ohta '454 are directed to improving image display in an in-plane switching (IPS) mode liquid crystal display*, see, e.g.,* Kubota, [0004]–[0005]; Ohta '454, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Kubota in view of Kim

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a "metal thin film." *See, e.g.,* Kubota, [0018]; *see also* Figs. 1, 4. Kubota further discloses that a pixel electrode 17 is formed in the same manner. *See*, *e.g.*, Kubota, [0021].

Kim discloses a pixel electrode and a data line with "a double-layered structure including a bottom metal layer [and] a top ITO layer." *See*, *e.g.*, Kim, 4:16–20; *see also* Kim, Figs. 5–6. Kim discloses that the bottom metal layer is "made of Cr or Mo." Kim, 4:20.

A POSITA would have understood that the Cr (chromium) or Mo (molybdenum) disclosed in Kim could have been used as the "metal thin film" disclosed in Kubota. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of Cr (chromium) or Mo (molybdenum) for an electrode, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). A POSITA would have found it obvious to use Cr (chromium) or Mo (molybdenum) as a "metal thin film," as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Kubota and Kim are directed to improving image display in an in-plane switching (IPS) mode liquid crystal display*, see*, *e.g.*, Kubota, [0004]–[0005]; Kim, 2:54–55, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Kubota in view of Asada, Ota5430, Ota561, or Yamaji

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a "metal thin film." *See*, *e.g.*, Kubota, [0018]; *see also* Figs. 1, 4. Kubota disclose that a pixel electrode 17 is formed in the same manner. *See*, *e.g.*, Kubota, [0021].

Asada discloses a scanning electrode and a common electrode formed by depositing a "metal thin film having aluminum as a main component." Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada also discloses a signal electrode, a pixel electrode, and common electrode formed by two layers of aluminum/titanium. *See*, *e.g.*, Asada, [0023].

Ota5430 discloses, "The counter electrode terminal C T M has a structure in which the transparent conductive layer i1 is laminated on the conductive layer g 3. This transparent conductive film i1 uses a transparent conductive film ITO as with other terminals." *See* Ohta5430.

Ota561 discloses, "…it is not necessary that the pixel electrode 3 is limited to have transparency (for example, transparent electrode such as ITO)." *See* Ota561 6:64-67 & 7:1-5.

Yamaji discloses "[a] transparent common electrode 65 made of ITO or the like, a pixel electrode 66 provided corresponding to each display pixel on the inner surface side of the other substrate 62, a transparent insulating film 64b covering the pixel electrode 66, and the insulation Transparent alignment films 68 and 69 such as polyimide covering the film 64 b and the common electrode 65…" *See* Yamaji. A POSITA would have understood that the aluminum-based metal thin film or electrode disclosed in Asada could have been used as the "metal thin film" disclosed in Kubota. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of aluminum in an electrode, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some

teaching, suggestion, or motivation exists to do so). A POSITA would have found it obvious to use aluminum as a main component of a "metal thin film," as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Kubota, Asada, Ota5430, Ota561, and Yamaji are directed to improving image display in an in-plane switching (IPS) mode liquid crystal display*, see*, *e.g.*, Kubota, [0004]–[0005]; Asada, [0013]; *see generally* Ota5430, Ota561, and Yamaji, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results. Kim in view of Matsumoto Kim discloses a pixel electrode and a data line with "a double-layered structure including a bottom metal layer [and] a top ITO layer." *See*, *e.g.*, Kim, 4:16–20; *see also* Kim, Figs. 5–6. Kim discloses that the bottom metal layer is "made of Cr or Mo." Kim, 4:20.

Matsumoto discloses a pixel electrode and a counter electrode having "a two-layered structure with a light blocking layer 41 overlapping on a transparent layer 40, and the width of the light blocking layer 41 is selected to be in the range of 25 to 75% of the width of the electrode." Matsumoto, [0014]; *see also* Matsumoto, Figs. 1–2. Matsumoto teaches that using the two-layered structure helps achieve the right balance among white luminance, black luminance, and contrast, compared to using either a transparent layer or light blocking layer alone. *See, e.g.,* Matsumoto, [0015]–[0017], Fig. 2.

Given the benefits taught in Matsumoto, a POSITA would have been motivated to apply the two-layered structure of Matsumoto to the electrodes of Kim. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of a two-layered structure, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–

19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Kim and Matsumoto are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Kim, 2:54–55; Matsumoto, [0017], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Kim in view of Ohta '454

Kim discloses a pixel electrode and a data line with "a double-layered structure including a bottom metal layer [and] a top ITO layer." *See*, *e.g.*, Kim, 4:16–20; *see also* Kim, Figs. 5–6. Kim discloses that the bottom metal layer is "made of Cr or Mo." Kim, 4:20.

Ohta '454 discloses a counter electrode made of a "double wiring," where a narrower aluminum layer is covered by a wider ITO layer. *See*, *e.g.*, Ohta '454, 50–51, Figs. 24A–C. Ohta '454 teaches that the use of the double wiring helps reduce resistivity of the electrodes, while preventing electrical short circuiting. *See*, *e.g.*, Ohta '454, 51. Ohta '454 also teaches that "[b]ecause the vicinity of the center line of such wiring is low in transmissivity even where a voltage is applied between electrodes, aperture ratio reduction will hardly occur even where a non-transparent metal wire is disposed as in this example [of double wiring]." Ohta '454, 51.

Given the benefits taught in Ohta '454, a POSITA would have been motivated to apply the "double wiring" of Ohta '454 to the electrodes of Kim. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a double wiring, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to

implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Kim and Ohta '454 are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Kim, 2:54–55; Ohta '454, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Kim in view of Kubota

Kim discloses a pixel electrode and a data line with "a double-layered structure including a bottom metal layer [and] a top ITO layer." *See*, *e.g.*, Kim, 4:16–20; *see also* Kim, Figs. 5–6. Kim discloses that the bottom metal layer is "made of Cr or Mo." Kim, 4:20.

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a "metal thin film." *See*, *e.g.*, Kubota, [0018]; *see also* Figs. 1, 4. Kubota discloses that the width of the light-transmitting conductive layer is wider than the width of the metal thin film. *See*, *e.g.*, Kubota, [0018], Fig. 4. Kubota discloses that a pixel electrode 17 is formed in the same way. *See*, *e.g.*, Kubota, [0021]. Kubota teaches that using its structure, "a liquid crystal display device having wide viewing angle properties and capable of favorable image display without display unevenness can be obtained." Kubota, [0040].

Given the benefits taught in Kubota, a POSITA would have been motivated to apply the double-layered structure of Kubota to the electrodes of Kim. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of a double-layered structure, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19

(obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Kim and Kubota are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Kim, 2:54–55; Kubota, [0004]–[0005], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Asada, Niwano, or Seung Hee Lee in view of Matsumoto

Asada discloses a scanning electrode and a common electrode formed by depositing a "metal thin film having aluminum as a main component." Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada also discloses a signal electrode, a pixel electrode, and common electrode formed by two layers of aluminum/titanium. *See*, *e.g.*, Asada, [0023].

Niwano discloses a scanning line 2 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W, or of their alloy, transparent materials such as ITO (Indium Tin Oxide) or the like or the laminated thereof." *See, e.g.*, Niwano, 9:7–13. Niwano also discloses a signal line 3 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly made of them, or alloy made chiefly of them, or a transparent material of such as ITO or the like or their laminated construction." *See, e.g.*, *id.*, 9:36–41. Niwano also discloses a driving electrode 5 and an opposite electrode 6 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of such as ITO or the like or their laminated construction or their laminated construction including them." *See*, *e.g.*, *id.*, 9:54–61.

Seung Hee Lee discloses that "the pixel electrode and the second counter electrode are made of transparent metal, specifically Indium Tin Oxide (ITO) or the like, but is not limited to the ITO." *See*, *e.g.*, *id.*, 2:35–38.

Matsumoto discloses a pixel electrode and a counter electrode having "a two-layered structure with a light blocking layer 41 overlapping on a transparent layer 40, and the width of the light blocking layer 41 is selected to be in the range of 25 to 75% of the width of the electrode." Matsumoto, [0014]; *see also* Matsumoto, Figs. 1–2. Matsumoto teaches that using the two-layered structure helps achieve the right balance among white luminance, black luminance, and contrast, compared to using just a transparent layer or just a light blocking layer. *See*, *e.g.*, Matsumoto, [0015]–[0017], Fig. 2. Matsumoto also discloses using "chromium or chromium oxide," along with ITO, for a counter electrode and a pixel electrode. *See, e.g.,* Matsumoto, [0017].

Given the benefits taught in Matsumoto, a POSITA would have been motivated to apply the two-layered structure of Matsumoto to the electrodes of Asada, Niwano, and Seung Hee Lee. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a two-layered structure, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Asada, Niwano, Seung Hee Lee, and Matsumoto are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Asada, [0013]; Niwano, 1:7–15; Seung Hee Lee, 4:26–28; Matsumoto, [0017], and that the improvements in

Matsumoto could readily be implemented in the other references to improve their liquid crystal displays with a reasonable expectation of success and predictable results.

Asada, Niwano, or Seung Hee Lee in view of Ohta '454

Asada discloses a scanning electrode and a common electrode formed by depositing a "metal thin film having aluminum as a main component." Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada also discloses a signal electrode, a pixel electrode, and common electrode formed by two layers of aluminum/titanium. *See*, *e.g.*, Asada, [0023].

Niwano discloses a scanning line 2 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W, or of their alloy, transparent materials such as ITO (Indium Tin Oxide) or the like or the laminated thereof." *See*, *e.g.*, Niwano, 9:7–13. Niwano also discloses a signal line 3 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly made of them, or alloy made chiefly of them, or a transparent material of such as ITO or the like or their laminated construction." *See*, *e.g.*, *Id.*, 9:36–41. Niwano also discloses a driving electrode 5 and an opposite electrode 6 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of such as ITO or the like or their laminated construction or their laminated construction including them." *See*, *e.g.*, *Id.*, 9:54–61.

Seung Hee Lee discloses that "the pixel electrode and the second counter electrode are made of transparent metal, specifically Indium Tin Oxide (ITO) or the like, but is not limited to the ITO." *See*, *e.g.*, *Id.*, 2:35–38.Ohta discloses a counter electrode made of a "double wiring," where a narrower aluminum layer is covered by a wider ITO layer. *See*, *e.g.*, Ohta '454, 50–51, Figs. 24A–C. Ohta '454 teaches that the use of the double wiring helps reduce resistivity of the electrodes, while preventing electrical short circuiting. *See, e.g.,* Ohta '454, 51. Ohta '454 also teaches that "[b]ecause the vicinity of the center line of such wiring is low in transmissivity even where a voltage is applied between electrodes, aperture ratio reduction will hardly occur even

where a non-transparent metal wire is disposed as in this example [of double wiring]." Ohta '454, 51.

Given the benefits taught in Ohta '454, a POSITA would have been motivated to apply the "double wiring" of Ohta '454 to the electrodes of Asada, Niwano, and Seung Hee Lee. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a double wiring, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Asada, Niwano, Seung Hee Lee, and as well as Ohta '454 are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Asada, [0013]; Niwano, 1:7–15; Seung Hee Lee, 4:26–28; Ohta '454, Abstract, and that the improvements in Ohta '454 could readily be implemented in the other references to improve their liquid crystal displays with a reasonable expectation of success and predictable results.

Asada, Niwano, or Seung Hee Lee in view of Kubota

Asada discloses a scanning electrode and a common electrode formed by depositing a "metal thin film having aluminum as a main component." Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada also discloses a signal electrode, a pixel electrode, and common electrode formed by two layers of aluminum/titanium. *See*, *e.g.*, Asada, [0023].

Niwano discloses a scanning line 2 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W, or of their alloy, transparent materials such as ITO (Indium Tin Oxide) or the like or the laminated thereof." *See*, *e.g.*, Niwano, 9:7–13. Niwano also discloses a signal line 3 formed of "Cr,

Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly made of them, or alloy made chiefly of them, or a transparent material of such as ITO or the like or their laminated construction." *See*, *e.g.*, *id.*, 9:36–41. Niwano also discloses a driving electrode 5 and an opposite electrode 6 formed of "Cr, Al, Mo, Ta, Cu, Al—Cu, Al—Si—Cu, Ti, W or alloy mainly composed of at least two thereof, or a transparent material of such as ITO or the like or their laminated construction or their laminated construction including them." *See*, *e.g.*, *id.*, 9:54–61.

Seung Hee Lee discloses that "the pixel electrode and the second counter electrode are made of transparent metal, specifically Indium Tin Oxide (ITO) or the like, but is not limited to the ITO." *See, e.g.*, Seung Hee Lee, 2:35–38. Seung Hee Lee states that "[t]he first counter electrode is made of opaque metal such as MoW, Mo/Al or Al Nd but is not limited." *See*, *e.g.*, *id.*, 2:38–40.

Kubota discloses a common electrode 13 that is partially constituted by a light-transmitting conductive layer made of indium in oxide (ITO) and a "metal thin film." *See*, *e.g.*, Kubota, [0018]; *see also* Figs. 1, 4. Kubota discloses that the width of the light-transmitting conductive layer is wider than the width of the metal thin film. *See*, *e.g.*, Kubota, [0018], Fig. 4. Kubota discloses that a pixel electrode 17 is formed in the same manner. *See*, *e.g.*, Kubota, [0021]. Kubota further teaches that using its structure, "a liquid crystal display device having wide viewing angle properties and capable of favorable image display without display unevenness can be obtained." Kubota, [0040].

Given the benefits taught in Kubota, a POSITA would have been motivated to apply the double-layered structure of Kubota to the electrodes of Asada, Niwano, and Seung Hee Lee. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a double-layered structure, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S.

at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, it would have been a simple substitution of one known limitation for another to obtain predictable results, as well as the use of known technique to improve similar devices in the same way. In addition, a POSITA would have recognized that Asada, Niwano, Seung Hee Lee, and Kubota are directed to improvements improving image display in an in-plane switching (IPS) mode liquid crystal display, *see*, *e.g.*, Asada, [0013]; Niwano, 1:7–15; Seung Hee Lee, 4:26–28; Kubota, [0004]–[0005], and that the improvements in Kubota could readily be implemented in the other references to improve their liquid crystal displays with a reasonable expectation of success and predictable results.

Sequential Signaling in a Matrix of Pixels

It would have been within the knowledge of a POSITA that it was common in conventional liquid crystal displays to use a matrix of pixels, where "an image is displayed on the liquid crystal panel by inputting a video signal from the video signal line into the pixel electrode while sequentially selecting the pixel through the scanning signal line." For example, in addition to the references discussed above, at least the following references demonstrate that sequentially selecting rows of pixels in a matrix display well was a well-known technique at the time of the alleged invention:

- "Active-Matrix Thin-Film Transistor Liquid-Crystal Displays (Advances in Electronics and Electron Physics Vol. 77)," 18–21, 47–53, 64–65, 100;
- US 6,392,627, 3:24–59;
- "Flat Panel Displays Using Amorphous and Microcrystalline Semiconductor Devices (Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices)", 102–03;
- "Microelectronics in Active-Matrix LCDs and Image Sensors (Electro-Optical Displays)," 72, 78;

- "Liquid Crystal Flat Panel Displays: Manufacturing Science & Technology," 22;
- "SID Asia Display '95 (October 16–18, 1995): Principles and Characteristics of Electro-Optical Behaviour with IPS Mode";
- "SID Asia Display '95 (October 16–18, 1995): Development of Super-TFT-LCDs with IPS Display Mode";
- US 6,067,067;
- US 6,091,393;
- US 6,677,925;
- US 6,049,369;
- US 6,014,190;
- US 5,852,485;
- US 5,831,707;
- US 5,786,876;
- US 5,754,266;
- US 5,734,451;
- US 5,600,464;
- US 5,598,285;
- US 4,345,249;
- UK 2,332,769;
- EP 0588568A2;
- EP 0667555A1;
- EP 0673986A2; and
- EP 0732612A1.

A POSITA would have understood that it would have been obvious to implement a method of sequentially selecting rows of pixels in the displays described in any of Matsumoto, Ohta '454,

Kubota, Kim, Asada, Niwano, and/or Seung Hee Lee. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of sequentially selecting rows of pixels in a matrix display, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). A POSITA would have found it obvious to use a method of sequentially selecting rows of pixels in a matrix display as this would have been one of a finite number of predictable solutions and a simple substitution of one known limitation for another to obtain predictable results.

Conductivity

A POSITA would have understood that electrical conductivity is a known property of a material, and that certain metals that are typically used for electrodes in conventional liquid crystal displays, *e.g.,* aluminum, chromium, and titanium, have a higher conductivity than that of ITO. This is evidenced by at least the following references:

- "Liquid Crystal Flat Panel Displays: Manufacturing Science & Technology," 35 (disclosing, among others, aluminum Al, chromium Cr, and titanium Ti), 115 (disclosing ITO);
- Flat Panel Manufacturing, 202 (disclosing, among others, Al, Mo, Ti, and Cr), 207 (disclosing ITO), 222 (disclosing, among others, Al, Mo, Ti, and Cr);
- Sputtering Materials for VLSI and Thin Film Devices, 427 (disclosing, among others, Al, ITO, Mo, Cr);
- US 5,400,157, 4:15–19 (disclosing chromium and ITO);
- JP2000-206550, [0007] (disclosing ITO);
- "CRC Handbook of Chemistry and Physics (67th Edition)" (disclosing, among others, aluminum), E-91; and
- "Elements of Material Science: An Introductory Text for Engineering Students (Second Edition)", appendix e (disclosing, among others, aluminum).

(8) U.S. Patent No. 7,583,347

The asserted claim of the ’347 patent is directed to a liquid crystal display where “at least one electrode of the common electrode and the pixel electrode is constituted by an electrode portion and a wiring portion” and “the electrode portion is at least partially constituted by a transparent electric conductor.” ’347 patent, Claim 1. The electrode portion and the wiring portion are formed in different layers: “the electrode portion is formed in a layer separated by an insulating layer from a layer in which the scanning signal line is formed, and the wiring portion is formed in the layer in which the scanning signal line is formed.” ’347 patent, Claim 1. Figure 16a depicts an exemplary structure:

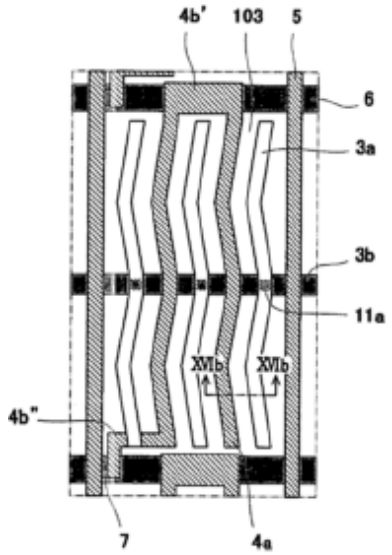
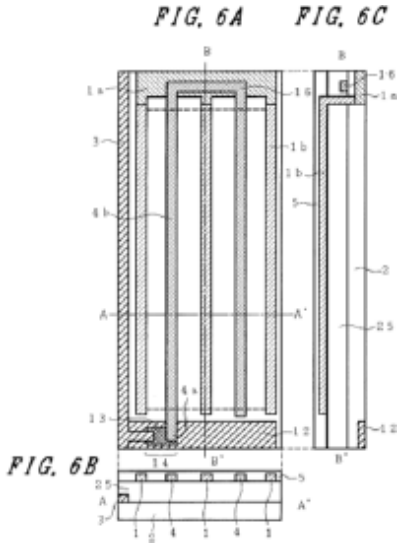


Fig. 16a

The ’347 patent states that a common electrode 3 is constituted by a wiring portion 3b “made of metallic material having a high reflectance” and an electrode portion 3a “constituted by [a] transparent electric conductor.” ’347 patent, 23:21–25. Wiring portion 3b is formed in the same layer as scanning line 6. *Id*., 23:30–37. Electrode portion 3a is formed in a layer separated from scanning line 6 and wiring portion 3b by an insulating layer, and is connected to wiring portion 3b through a contact hole 11a. *Id*., 23:25–30.

According to the ’347 patent, the purported benefits of such a structure are twofold: (1) “since the electrode portion is at least partially constituted by a transparent electric conductor, the luminance is improved,” and (2) “since the electrode portion of the electrode is separated by the insulating layer from the scanning signal line, short-circuit can be prevented.” ’347 patent, 5:39–43.

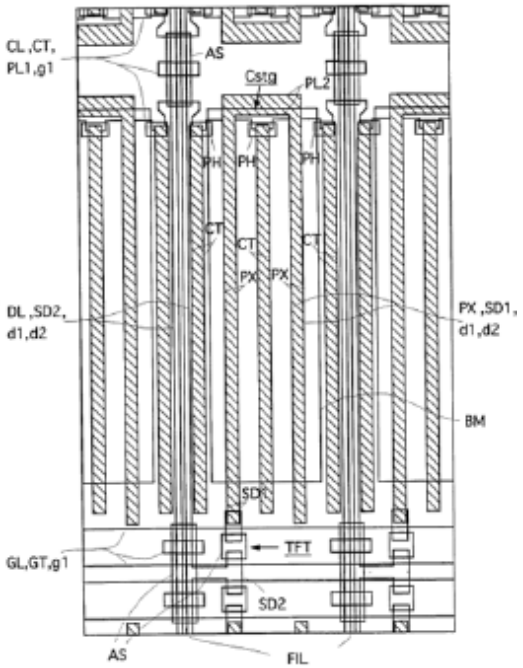
However, the ’347 patent’s claimed structure was well known in the prior art. Numerous prior art references, including for example, Ohe, Ohta ’454, and Park, already disclosed such a structure. For example, exemplary Figure 6 of Ohe depicts a wiring portion 1a of a common electrode 1 formed in the same layer as a scanning electrode 12. *See*, *e.g.*, Ohe, 9:49–52. Exemplary Figure 6 of Ohe further depicts an electrode portion 1b of the common electrode 1 that is formed in a different layer separated by an insulating layer. *See*, *e.g.*, *id.*, 9:53–55. The electrode portion 1b of the common electrode 1 is made of transparent ITO. *See*, *e.g.*, *id.*, 9:58–59.



Similarly, exemplary Figure 22 of Ohta ’454 depicts a wiring portion CL of a counter electrode formed in the same layer as a scanning signal line GL. *See, e.g.*, Ohta ’454, 23. Figure 22 of Ohta ’454 further depicts an electrode portion CT of a counter electrode formed in a different

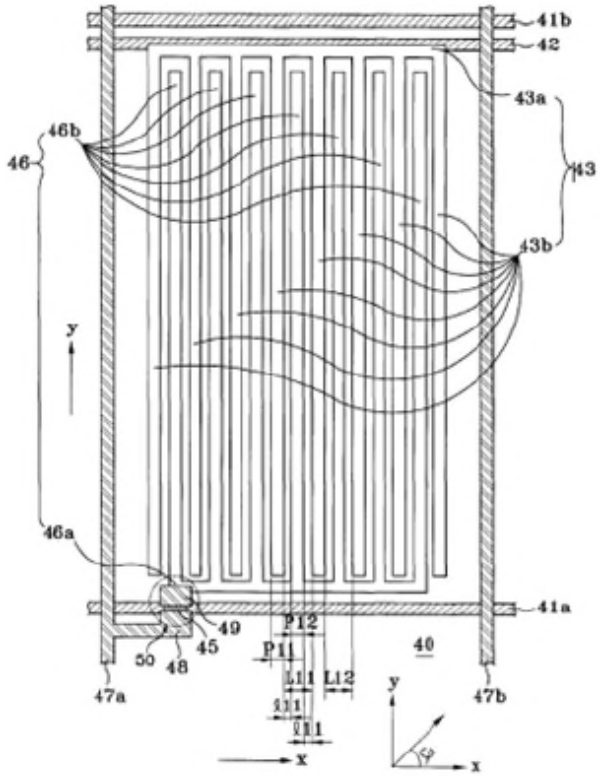
layer separated by an insulating layer. *See, e.g.*, *id.*, 48–49. The electrode portion CT of the counter electrode is made of transparent ITO. *See, e.g.*, *id.*

FIG.22



Similarly, exemplary Figure 2 of Park depicts a wiring portion 42 of a common electrode formed in the same layer as gate bus lines 41a and 41b. *See, e.g.*, Park, 4:31–33. Exemplary Figure 2 of Park further depicts an electrode portion 43b of the common electrode formed in a different layer separated by an insulating layer. *See, e.g.*, *id.*, 4:48–66. The electrode portion 43b of the common electrode is made of transparent ITO. *See, e.g.*, *id.*, 4:59–66.

FIG.2



Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00504.

A POSITA would have found the asserted claims obvious in view of the combinations discussed below as well as those in IPR2022-00504.

Asada in view of Ohe

Asada discloses a liquid crystal panel with a scanning electrode and a wiring portion 103 of a common electrode formed in the same layer by depositing a "metal thin film having aluminum as a main component." *See, e.g.*, Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada further discloses an electrode portion 106 of the common electrode formed in a different layer separated by an insulating layer. *See, e.g., id.*, [0022]–[0023]. The electrode portion

106 of the common electrode is made of two layers of aluminum/titanium (Al/Ti). *See, e.g.*, *id.*, [0023].

Ohe discloses an electrode portion of a common electrode and an electrode portion of a pixel electrode that are formed of ITO, a transparent electric conductor. *See, e.g.,* Ohe, 9:46–59, Fig. 6. Ohe also discloses a reflecting face formed below a liquid crystal panel. *See, e.g.,* Ohe, 11:64–12:24, Fig. 10. A POSITA would have understood that the use of ITO and the use of a reflecting face allow more light to pass through the display, increasing luminance.

Given the benefits, a POSITA would have been motivated to use ITO and a reflecting face of Ohe for the liquid crystal panel disclosed in Asada. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of ITO and a reflecting face, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ohe's ITO and reflecting face would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Asada and Ohe both concern improving image display in an in-plane switching (IPS) mode liquid crystal display*, see, e.g.,* Asada, [0013]; Ohe, 2:66–3:4, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Asada in view of Ohta '454

Asada discloses a liquid crystal panel with a scanning electrode and a wiring portion 103 of a common electrode formed in the same layer by depositing a "metal thin film having aluminum as a main component." *See, e.g.,* Asada, [0022]. Asada discloses that a "multi-layer film" can also

be used. Asada further discloses an electrode portion 106 of the common electrode formed in a different layer separated by an insulating layer. *See, e.g., id.*, [0022]–[0023]. The electrode portion 106 of the common electrode is made of two layers of aluminum/titanium (Al/Ti). *See, e.g.*, *id.*, [0023].

Ohta '454 discloses a counter electrode made of a "double wiring," where a narrower aluminum layer is covered by a wider ITO layer. *See*, *e.g.*, Ohta '454, 50–51, Figs. 24A–C. Ohta '454 teaches that the use of the double wiring helps reduce resistivity of the electrodes, while preventing electrical short circuiting. *See*, *e.g.*, Ohta '454, 51. Ohta '454 also teaches that "[b]ecause the vicinity of the center line of such wiring is low in transmissivity even where a voltage is applied between electrodes, aperture ratio reduction will hardly occur even where a non-transparent metal wire is disposed as in this example [of double wiring]." Ohta '454, 51. Ohta '454 also discloses a reflecting face formed below a liquid crystal panel. *See, e.g.,* Ohta '454, 46, Fig. 18. A POSITA would have understood that the use of ITO and the use of a reflecting face would allow more light to pass through the display, increasing luminance.

Given the benefits, a POSITA would have been motivated to apply the ITO and the reflecting face disclosed in Ohta '454 to the liquid crystal panel disclosed in Asada. This would have constituted nothing more than the "application of a known technique," *i.e.,* the use of ITO and a reflecting face, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ohta '454's ITO and reflecting face would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have

recognized that Asada and Ohta ’454 both concern improving image display in an in-plane switching (IPS) mode liquid crystal display*, see, e.g.,* Asada, [0013]; Ohta ’454, Abstract, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Asada in view of Park

Asada discloses a liquid crystal panel with a scanning electrode and a wiring portion 103 of a common electrode formed in the same layer by depositing a “metal thin film having aluminum as a main component.” *See*, *e.g.*, Asada, [0022]. Asada discloses that a “multi-layer film” can also be used. Asada further discloses an electrode portion 106 of the common electrode formed in a different layer separated by an insulating layer. *See*, *e.g.*, *id.*, [0022]–[0023]. The electrode portion 106 of the common electrode is made of two layers of aluminum/titanium (Al/Ti). *See*, *e.g.*, *id.*, [0023].

Park discloses an electrode portion of a common electrode and an electrode portion of a pixel electrode that are formed of ITO, a transparent electric conductor. *See*, *e.g.,* Park, 4:53–61, Fig. 2. Park also discloses a reflecting face formed below a liquid crystal panel. *See*, *e.g.*, Park, 6:4–17, Fig. 4. A POSITA would have understood that the use of ITO and the use of a reflecting face would allow more light to pass through the display, increasing luminance.

Given the benefits, a POSITA would have been motivated to apply the ITO and the reflecting face disclosed in Park to the liquid crystal panel disclosed in Asada. This would have constituted nothing more than the “application of a known technique,” *i.e.,* the use of ITO and a reflecting face, “to a piece of prior art ready for the improvement.” *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Park’s ITO

and reflecting face would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Asada and Park both concern improving image display in an in-plane switching (IPS) mode liquid crystal display*, see*, *e.g.*, Asada, [0013]; Park, 2:52–59, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Asada in view of Matsumoto and Hiyama or Sang Soo Kim

Asada discloses a liquid crystal panel with a scanning electrode and a wiring portion 103 of a common electrode formed in the same layer by depositing a "metal thin film having aluminum as a main component." *See*, *e.g.*, Asada, [0022]. Asada discloses that a "multi-layer film" can also be used. Asada further discloses an electrode portion 106 of the common electrode formed in a different layer separated by an insulating layer. *See*, *e.g.*, *id.*, [0022]–[0023]. The electrode portion 106 of the common electrode is made of two layers of aluminum/titanium (Al/Ti). *See*, *e.g.*, *id.*, [0023].

Matsumoto discloses a pixel electrode and a counter electrode having "a two-layered structure with a light blocking layer 41 overlapping on a transparent layer 40." Matsumoto, [0014]; *see also* Matsumoto, Figs. 1–2. Matsumoto teaches that using the two-layered structure helps achieve the right balance among white luminance, black luminance, and contrast, compared to using either a transparent layer or light blocking layer alone. *See*, *e.g.*, Matsumoto, [0015]–[0017], Fig. 2.

Hiyama discloses a reflector that increases the efficiency of the display by optimizing the amount of light from the light source that is output through the display. *See*, *e.g.*, Hiyama, [0062]–[0063], [Fig. 1]. Hiyama teaches that use of the reflector allows Hiyama's liquid crystal display

element to "achieve the same brightness as a liquid crystal display element having an aperture ratio 1.5 times greater." *See*, *e.g.*, *id.*, [0063].

Similarly, Sang Soo Kim discloses a reflector. *See*, *e.g.*, Sang Soo Kim, Figs. 20–22. Sang Soo Kim teaches that the reflector "should be optimized to improve the light utilization efficiency and the illumination uniformity." *See*, *e.g.*, *id.*, 8.

Hiyama's and Sang Soo Kim's teaching is consistent with how a reflector was well known in the art. *See*, *e.g.*, U.S. Patent No. 5,739,880, Fig. 3, 5:29.

A POSITA would have understood that the use of Matsumoto's two-layered structure including a transparent layer could have been used with the liquid crystal panel disclosed in Asada. Indeed, a POSITA would have been motivated to do so, given Matsumoto's teaching regarding the benefits of a two-layered structure. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a two-layered structure including a transparent layer, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Matsumoto's two-layered structure including a transparent layer would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Asada and Matsumoto both concern improving image display in an in-plane switching (IPS) mode liquid crystal display*, see*, *e.g*., Asada, [0013]; Matsumoto, [0017], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

A POSITA would have also understood that a conventional liquid crystal display typically included a reflecting plate in order to increase the efficiency of its backlight unit. A POSITA would also have been motivated to use either of Hiyama's or Sang Soo Kim's reflecting plate, given their teachings about the benefits of such a reflecting plate. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a reflecting plate, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Hiyama's or Sang Soo Kim's reflecting plate would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Asada, Hiyama, and Sang Soo Kim all concern improving image display in a liquid crystal display*, see*, *e.g.*, Asada, [0013]; Hiyama, [0063]; Sang Soo Kim, 8, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Niwano or Seung Hee Lee in view of Hiyama or Sang Soo Kim

Niwano discloses a liquid crystal panel with a scanning electrode and a wiring portion 8 of a common electrode formed in the same layer. *See*, *e.g.*, Niwano, 11:51–52 ("the common line 8 is formed on the same layer as that of the scanning line 2"). Niwano further discloses an electrode portion 6 of the common electrode formed in a different layer separated by an insulating layer. *See, e.g.*, *id.*, 11:60–62 ("The opposite electrode 6 is connected with the common line 8 through the through-hole 18."). The electrode portion 6 of the common electrode is made of ITO. *See*, *e.g.*, *id.*, 9:54–61.

Seung Hee Lee discloses a liquid crystal panel with a scanning line and a wiring portion 3 of a common electrode formed in the same layer. *See*, *e.g.*, Seung Hee Lee, 5:32–33. Seung Hee Lee further discloses an electrode portion 8 of the common electrode formed in a different layer separated by an insulating layer. *See*, *e.g.*, *id.*, Figs. 3–4, 5:18–25.

Hiyama discloses a reflector that increases the efficiency of the display by optimizing the amount of light from the light source that is output through the display. *See*, *e.g.*, Hiyama, [0062]–[0063], [Fig. 1]. Hiyama teaches that use of the reflector allows Hiyama's liquid crystal display element to "achieve the same brightness as a liquid crystal display element having an aperture ratio 1.5 times greater." *See*, *e.g.*, *id.*, [0063].

Similarly, Sang Soo Kim discloses a reflector. *See*, *e.g.*, Sang Soo Kim, Figs. 20–22. Sang Soo Kim teaches that the reflector "should be optimized to improve the light utilization efficiency and the illumination uniformity." *See*, *e.g.*, *id.*, 8.

Hiyama's and Sang Soo Kim's teaching is consistent with how a reflector was well known in the art. *See*, *e.g.*, U.S. Patent No. 5,739,880, Fig. 3, 5:29.

A POSITA would have also understood that a conventional liquid crystal display typically included a reflecting plate in order to increase the efficiency of its backlight unit. A POSITA would also have been motivated to use either of Hiyama's or Sang Soo Kim's reflecting plate, given their teachings about the benefits of such a reflecting plate. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a reflecting plate, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Hiyama's or Sang Soo Kim's reflecting plate

would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Niwano, Seung Hee Lee, Hiyama, and Sang Soo Kim all concern improving image display in a liquid crystal display, *see*, *e.g.*, Niwano, 1:11–15; Seung Hee Lee; 1:51–54; Hiyama, [0063]; Sang Soo Kim, 8, and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

Wakagi in view of Ohta059

Wakagi discloses a "liquid crystal display device [comprising] plural gate electric wiring, plural drain electric wiring intersecting therewith in a matrix state, plural thin film transistors formed opposite to each intersection of the gate and drain electric wiring, and plural common electric wiring extending in the same direction as the gate electric wiring are provided on one of a pair of substrates." Wakagi, 2:3-9. Further, Wakagi describes as desirable, "…a bright display panel is obtained, and the power consumption of the backlight may be made small." Wakagi, 5:32-34.

Ohta059, which discloses "a liquid crystal display device," also discloses a reflector face, describing "[l]ight emitted from the backlight fluorescent tube BL disposed on one side of the light conductor LCB is rendered backlight which is uniform on the display surface through the light conductor LCB, reflector plate RM and light diffusion plate SPB, and is emitted to the side of the liquid crystal display panel PNL." Ohta059, 3:37-42 and 33:11-16. Further, Ohta059 describes as desirable "As a result, the counter voltage signal line CL has a decreased resistance, the common signals are smoothly propagated, the picture quality is improved, and the common signal generator unit consumes a reduced amount of electric power." Ohta059, 13:3-7.

A POSITA would have also understood that a conventional liquid crystal display typically included a reflecting plate in order to increase the efficiency of its backlight unit. A POSITA would

also have been motivated to use Ohta059, given their teachings about the benefits of such a reflecting plate. This would have constituted nothing more than the "application of a known technique," *i.e.*, the use of a reflecting plate, "to a piece of prior art ready for the improvement." *See KSR*, 550 U.S. at 417; *see also id.* at 415–19 (obvious to implement known techniques to improve similar devices and methods in known ways to yield predictable results, especially where some teaching, suggestion, or motivation exists to do so). Further, a POSITA would have recognized that using Ohta059's reflecting plate would have been nothing more than a simple substitution of one known limitation for another to obtain predictable results. In addition, a POSITA would have recognized that Wakagi and Ohta059 concern improving image display and reducing power consumption in a liquid crystal display, *see*, *e.g.*, Wakagi [5:27-34]; Ohta059 [13:3-7], and that the improvements in one could readily be implemented in the other to improve the liquid crystal display with a reasonable expectation of success and predictable results.

(9) U.S. Patent No. 7,995,047

The core concepts of the alleged invention were known in the art. To the extent the claims are supported by the specification, and to the extent Bishop's infringement theories can be credited, the elements of the claims, including their relative arrangement, were all well-known components of prior art long before the alleged priority date of the '047 patent. Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00501 and IPR2025-01330 concerning U.S. Patent No. 7,995,047.

Current Driving Device

Claim 1 recites "[a] current driving device, comprising: a first voltage supply source for supplying a first voltage; a first current supply source for supplying a first electric current; a plurality of output terminals." A current driving comprising voltage supply and current supply was well-known in the art long before the '047 patent. For example, it was well known to use a voltage

supply and a current supply in order to supply controlled current to display components, such as light-emitting diodes (LED), organic light-emitting diodes (OLED), or segments of a liquid crystals display (LCD). Shimoda, § 1; *see also*, Baek, ¶¶ [0003], [0036]; Figs. 3, 5. It was also known to have multiple output terminals connected to multiple display components of a display panel, so that the display components could form pixels of an image. Shimoda, § 1. Other references also disclose the similar configuration. *See*, *e.g.,* Baek, ¶¶ [0003], [0036], Figs. 3, 5; Sasaki, 11:15–34; Kimura, 8:43–60; Jo, 12:59–13:3. Further, the '047 patent admitted that a driving device with a current supply source and a plurality of output terminals was known to the art. *See*, *e.g.*, the '047 patent, Figs. 6A, 6B.

A plurality of current output circuits

Claim 1 recites "a plurality of current output circuits for outputting an electric current in accordance with said first electric current, each of said current output circuits comprising a current-voltage converting circuit, a voltage-current converting circuit, a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal." The '047 patent admitted that an output circuit comprising a voltage-current converting circuit, a current-voltage converting circuit, and a voltage holding circuit is known to the art. *See*, *e.g.*, the '047 patent, Figs. 6A, 6B. Further, other references also disclose this configuration. For example, it was known to supply multiple pixels with multiple current output circuits so that each pixel could function independently. Shimoda, § 1. It was also known in the art to connect a voltage holding circuit (*e.g.*, a capacitor) to a reference source via a current-voltage converting circuit and output a current via a voltage-current converting circuit. Shimoda, § 3.1, Fig. 6. Numerous other references also disclose a current supply model. *See*, *e.g.*, Baek, ¶ [0055], Fig. 5; Kimura, Fig. 1, 8:43–60; Sasaki, 15:48–67; Figs. 3, 6, 7. In addition to the reasons discussed above, a POSITA would have been motivated to combine the current output circuits in

any of these references in order to supply an accurate current output to multiple display components.

Voltage supply mode

Claim 1 recites "under said voltage supply mode, each of said current output circuits receives said first voltage from said first voltage supply source, and the first voltage is supplied to another terminal of said voltage holding circuit." A voltage supply mode was well-known in the art long before the '047 Patent. For example, it was known to apply a voltage to a voltage holding circuit (*i.e.*, a voltage supply mode) in order to ensure the voltage holding circuit to be charged before the current output period. Shimoda, § 1. Some other references also disclose using a voltage supply period to reset the current output circuits or to erase data previously stored in the voltage holding circuit. Kimura, 9:23–33, Fig. 2. Numerous other references also disclose a voltage supply mode. *See, e.g.,* Baek, ¶ [0062]; Sasaki, 1:65–2:13, 8:19–45, Fig. 5; Kimura, Figs. 2, 3A–3D; 9:23–33. In addition to the reasons discussed above, a POSITA would have been motivated to combine the current supply model in any of these references in order to reduce the time required to charge the holding circuit or to erase data previously stored.

Current supply mode

Claim 1 recites "under said current supply mode, each of said current output circuits receives said first current from said first current supply source, and generates a second voltage by said current-voltage converting circuit, and the first current is supplied to said another terminal of said voltage holding circuit." A current supply mode was well-known in the art long before the '047 Patent. For example, Baek discloses supplying current to a voltage holding circuit to charge the voltage holding circuit to a desirable level. Baek, ¶ [0056]. During the current supply period, a current is directly supplied to the voltage holding circuit to calibrate the voltage of the voltage holding circuit to a desired level. Baek, Fig. 5, ¶ [0056]. Numerous other references also

disclose a current supply mode. *See*, *e.g.*, Shimoda, § 3. 2; Sasaki, Fig 1, 8:19–45; Kimura, Figs. 2, 3A–3D, 9:23–33. In addition to the reasons discussed above, a POSITA would have been motivated to combine the current supply model in any of these references in order to calibrate the voltage held in the voltage holding circuit.

Current output mode

Claim 1 recites "under said current output mode, each of said current output circuits outputs an output current according to said voltage held in said voltage holding circuit by said voltage-current converting circuit." The current output mode was well-known in the art long before the '047 Patent. The '047 patent admitted that a current output mode is known in the art. *See* the '047 patent, 2:41–58. Further, other references also suggest it was known to use a current output mode, outputting a current programmed in accordance with the voltage level of the voltage holding circuit to obtain an accurate brightness. Shimoda, § 3.2. Numerous other references also disclose a current supply model. *See, e.g.,* Sasaki, Fig. 1, 37:30–34; Kimura, Figs. 2, 3A–3D, 9:23–33. In addition to the reasons discussed above, a POSITA would have been motivated to combine the current supply model in any of these references in order to accurately activate the display components.

(10) U.S. Patent No. 8,093,830

The core concepts of the alleged invention were known in the art. To the extent the claims are supported by the specification, and to the extent Bishop's infringement theories can be credited, the elements of the claims, including their relative arrangement, were all well-known components of prior art long before the alleged priority date of the '830 patent. Defendant additionally incorporates by reference, as if fully stated herein, the motivations to combine in IPR2022-00503 and IPR2025-01331 concerning U.S. Patent No. 8,093,830.

Admitted prior art in the ’830 patent (’830 APA)

The ’830 patent discusses prior art and knowledge of persons skilled in the art that the applicant admitted were “conventional” and “well-known” in the art before the alleged invention of the ’830 patent. *See, e.g.,* ’830 patent, 1:22–5:67 and Figs. 1, 2, 3A, 3B, 3C, and 4. The applicant admitted that “FIG. 1 [shown below] is a block diagram showing a configuration example of ***a conventional semiconductor light source driving apparatus***” and that “FIG. 2 [also shown below] is a block diagram showing ***another*** configuration example of ***a conventional semiconductor light source driving apparatus***[.]” *Id*., 5:54–59 (emphasis added).

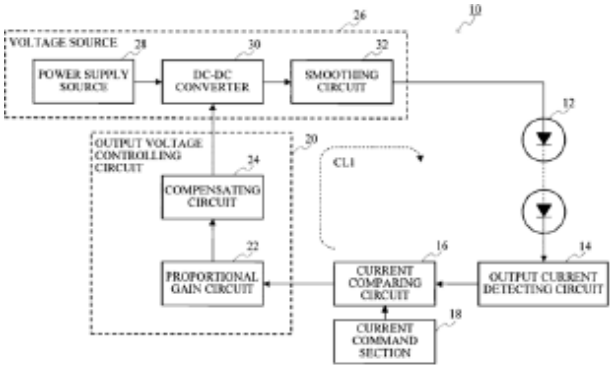


FIG.1

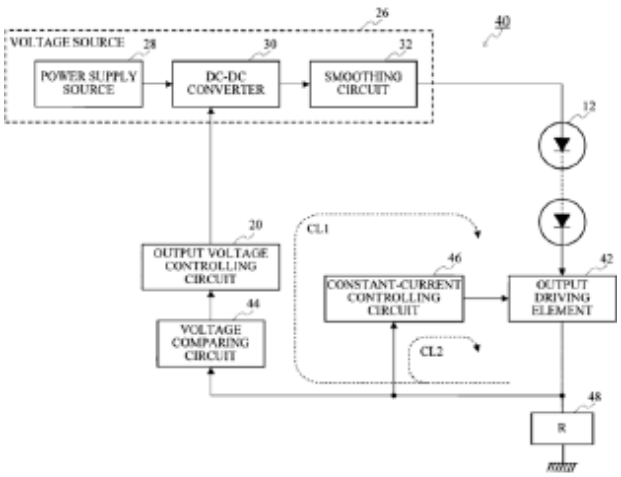


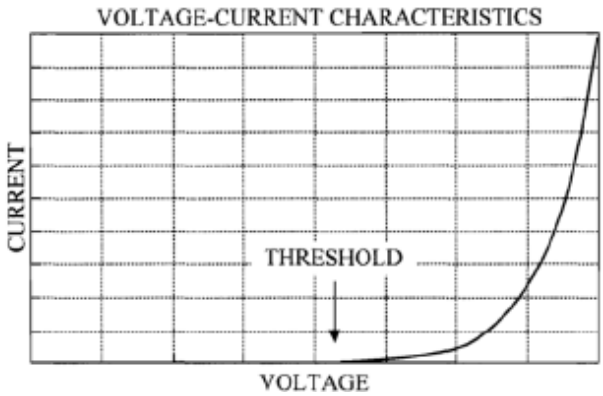
FIG.2

’830 patent, Figs. 1 and 2. As such, the applicant of the ’830 patent admitted that, prior to the alleged invention of the ’830 patent, it was already “conventional” to control an output voltage of

a semiconductor light source driving apparatus based on detected output current (as shown in Fig. 1) or detected output voltage (as shown in Fig. 2). *Id*.

The applicant of the ’830 patent further admitted that “a semiconductor light source has electrical characteristics that equal the characteristics of a diode” and that “the ***well-known*** voltage-current characteristics of a diode is shown in FIG. 3A.” ’830 patent, 3:29–32.

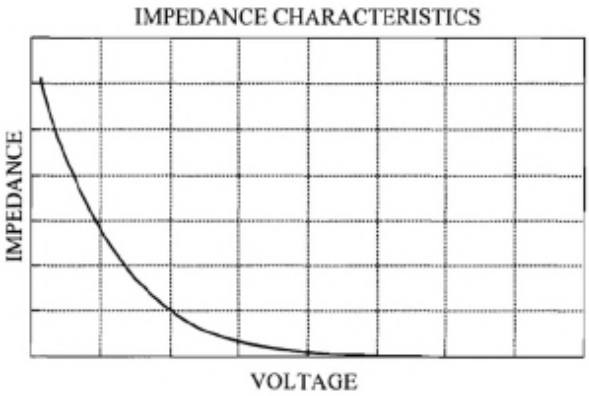
FIG.3A



Id., Fig. 3A. The applicant of the ’830 patent explained the “well-known voltage-current characteristics” as: “[W]hen a voltage is applied little current flows until the voltage generally referred to as a ‘threshold’ and current starts flowing slowly after the voltage exceeds the threshold. Afterwards, the ratio of the increasing in the current with respect to the increase in the voltage becomes higher, so that the current increases abruptly even when the voltage changes a little.” *Id*., 3:32–38.

The applicant continued: “[t]o view this from another point of view, as shown in Fig. 3B, the impedance of a diode decreases following the increase in the applied voltage.” *Id*., 3:32–41.

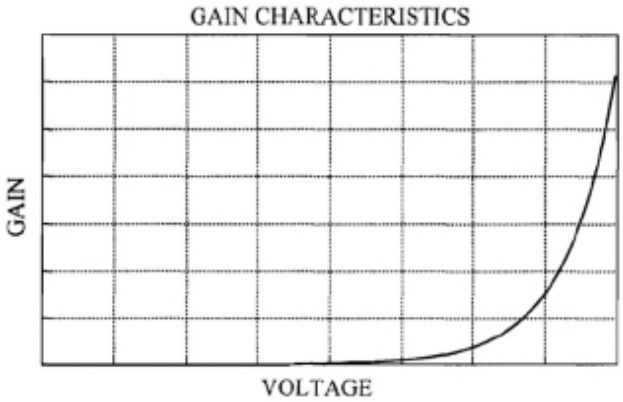
FIG.3B



Id., Fig. 3B.

"Further, assuming that a diode is a functional element that receives a voltage as input and outputs a current, as shown in Fig. 3C, its gain is not constant with respect to the input voltage and increases following the increase in the input voltage." *Id*., 3:41–45.

FIG.3C



Id., Fig. 3C. Accordingly, the applicant of the '830 patent admitted the diode characteristics of Figs. 3A–C were "well-known" before the alleged invention of the '830 patent.

The lone asserted claim of the '830 patent is claim 1, which recites:

> A semiconductor light source driving apparatus comprising: a semiconductor light source that is driven by a current;
>
> a voltage source that drives the semiconductor light source;
>
> an output voltage controlling section that controls a drive current value for driving the semiconductor light source by controlling an output voltage of the voltage source;

> an output current detecting section that detects an output current of the semiconductor light source;
>
> a current command section that specifies a reference value of a drive current which is applied to the semiconductor light source;
>
> a current comparing section that compares the output current detected by the output current detecting section and the reference value specified by the current command section; and
>
> an impedance detecting section that detects an impedance of the semiconductor light source, wherein the output voltage controlling section controls the output voltage of the voltage source based on an output of the current comparing section and an output of the impedance detecting section.

The admitted prior art of the ’830 patent (hereinafter ’830 APA) explicitly recognizes that at least the following from claim 1 was “conventional” in the art before the alleged invention of the ’830 patent:

“[a] semiconductor light source driving apparatus” (*e.g.*, the “[s]emiconductor light source driving apparatus 10 shown in FIG. 1” that “is a constant current driving circuit using a current control loop”). *Id.*, Fig. 1 and 1:39–41.

“a semiconductor light source that is driven by a current” (*e.g.*, the “semiconductor light source 12” of Figure 1). *Id.*, Fig. 1 and 1:41–48.

“a voltage source that drives the semiconductor light source” (*e.g.*, the “voltage source 26” of Figure 1). *Id.*, Fig. 1 and 1:45–52.

“an output voltage controlling section that controls a drive current value for driving the semiconductor light source by controlling an output voltage of the voltage source” (*e.g.*, “output voltage controlling circuit 20” of Figure 1 that “performs a pulse width control in voltage source 26”). *Id.*, Fig. 1 and 1:49–52.

"an output current detecting section that detects an output current of the semiconductor light source" (*e.g.*, the "output current detecting circuit 14" of Figure 1 that "detects the current applied to [the] semiconductor light source 12"). *Id*., Fig. 1 and 1:41–44.

"a current command section that specifies a reference value of a drive current which is applied to the semiconductor light source" (*e.g.*, "current command section 18" that provides "a current command value" to "current comparing circuit 16"). *Id*., Fig. 1 and 1:45–49.

"a current comparing section that compares the output current detected by the output current detecting section and the reference value specified by the current command section" (*e.g.*, the "current comparing circuit 16" that "compare[s]" the "output of output current detecting circuit 14" with "a current command value from current command section 18."). *Id*., Fig. 1 and 1:45–49. "wherein the output voltage controlling section controls the output voltage of the voltage source based on an output of the current comparing section" (*e.g.*, "output voltage controlling circuit 20" that "controls DC-DC converter 30 according to the comparison result in current comparing circuit 16.") *Id*., Fig. 1 and 1:56–59.

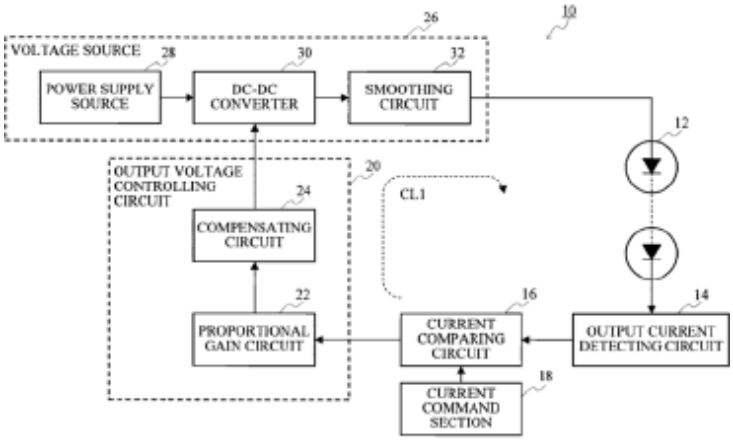


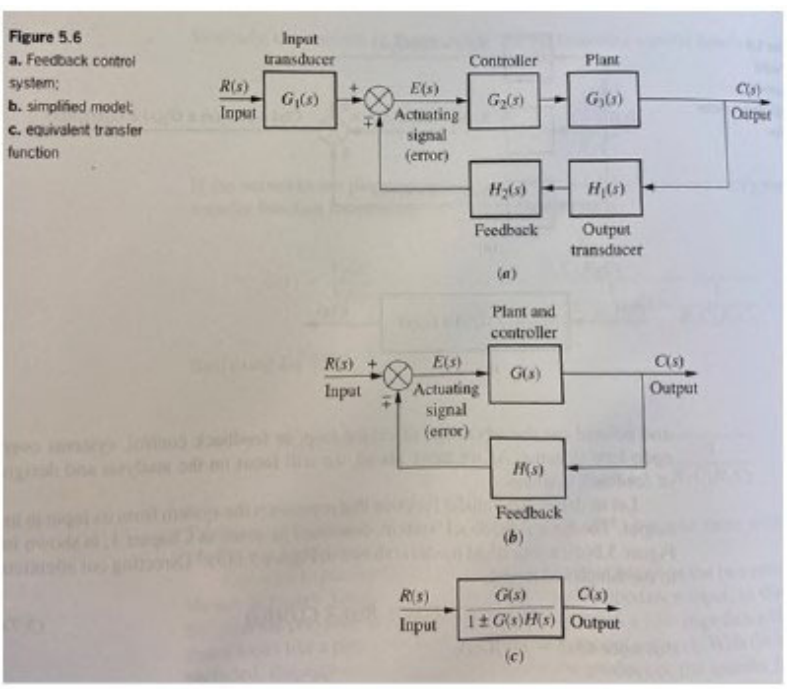
FIG.1

'830 patent, Fig. 1; *see also* '830 APA Claim Chart L-01.

Drive circuits relying on feedback for current control

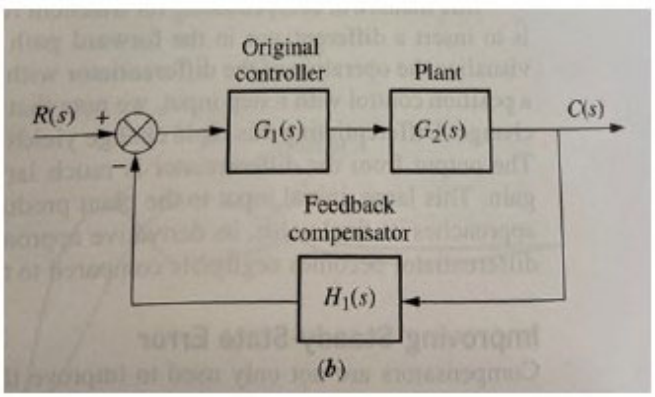
As discussed above, the ’830 APA describes “a configuration of a conventional semiconductor light source driving apparatus that is generally used to perform a constant-current control of a semiconductor light source” prior to the alleged invention of the ’830 patent. *See* ’830 patent, Fig. 1 and 1:22–2:19. Other prior art references confirm that these types of circuits were well-known in the prior art before the earliest priority date of the ’830 patent.

Control circuits, and in particular closed-loop feedback control circuits, were well-known in the art before the alleged invention of the ’830 patent. *See*, *e.g.,* Norman S. Nise, CONTROL SYSTEMS ENGINEERING (4th ed. 2004), Chapters 1, 2, 5, 7–9, and 11; John A. Camara, PE, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, (6th ed. 2002), Chapters 43–45 and 63. “The feedback system forms the basis for our study of control systems engineering” where “Figure 5. 6” shows “a. Feedback control system; b. simplified model; c. equivalent transfer function”:



Norman S. Nise, CONTROL SYSTEMS ENGINEERING (4th ed. 2004), 257–58; *see also* John A. Camara, PE, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, (6th ed. 2002), 63-4 – 63-5 ("Feedback Theory: The output signal is returned as input in a feedback loop (feedback system) where "[a] basic feedback system consists of two black box units (a dynamic unit and a feedback unit), a pick-off point (take-off point), and a summing point (comparator or summer" and "[t]he incoming signal , Vi, is combined with the feed back signal, Vf, to give the error (error signal), e.").

It was well-known that feedback could be used as a compensator in control circuits. An example of a feedback compensator is shown below:



Id., 502; *see also id*. at 500–571. "Ideal Integral Compensation (PI)" was further well-known in the art. *See id*., 504–515. "[W]e call the ideal integral compensator a proportional-plus-integral (PI) controller, since the implementation . . . consists of feeding the error (proportional) plus the integral of the error forward to the plant" and this type of feedback control system was known to be effective for addressing "steady-state error." *Id*., 503–504.

The prior art—including the '830 APA—is replete with drive circuits relying feedback control systems that utilize one or more of: reference voltage(s), reference current(s), reference

resistance(s), detected voltage(s), detected current(s), and detected resistance(s)—including detected impedance(s).

Tripathi ’559 describes to a “power supply (20) for LEDs” that “provides power to a LED light source 10 having a variable number of LEDs[.]” Tripathi ’559, Abstract. “Sensed LED current ISE and sensed LED voltage VSE as well as a voltage reference VREF are fed to feedback controller 125” which “maintains an accurate voltage feedback VFB to thereby avoid large errors in LED current flowing through LED light source 110.” *Id*. 3:52–56; *see also* Tripathi ’512, Abstract and 3:43–59 (describing a “power supply for LEDs” that “uses current feedback to adjust power the LEDs” where “[t]he sensed current signal and reference current signal are compared at current controller 130” that “maintains an accurate current feedback signal, thereby avoiding large errors in LED current.”)

Bhagat describes “[a] lighting controller arranged to drive one or more light emitting semiconductors, the controller comprising a current source and/or a voltage source and a current and/or voltage sensor[.]” Bhagat, Abstract. Bhagat discloses that “[a]s LED lighting heats up, the effective impedance goes down” and “with a constant voltage source the current goes up, or with a constant current source the required voltage goes down[.]” *Id*. at 14:22–15:8. For example, “[i]f the voltage falls below a preset value . . . appropriate action can be taken; i.e. the current is reduced[.]” *Id*.

Barth describes “a control circuit for at least one light-emitting diode (1) for adjusting the current and/or the voltage of the light-emitting diode (1) to a desired value adjusted by means of a controller (3), the current, the voltage, and/or the luminescence of the light-emitting diode (1) being detectable and comparable with the desired value.” Barth, Abstract. Barth discloses that “[t]o regulate the current through the light emitting diodes 1, the voltage drop across the measuring

shunt 6 is determined and fed to the switched-mode regulator 4 as measured signal UMEAS" and "[i]n the switched-mode regulator, the current through the light-emitting diodes determined from said measured signal UMEAS is compared with setpoint value of the current through the light-emitting diodes supplied by the microcontroller 3 and the current ILED is regulated accordingly." *Id*., 3:54–65.

Garcia describes a "[s]witch current regulator" that "controls a current provided to a light-emitting diode based upon a magnitude of a voltage on the current control signal input." Garcia, ¶ 0007. "The circuit also includes a switching voltage regulator connected to the switch current regulator and the LED" where "[t]he switching voltage regulator provides current to the LED." *Id*. Garcia discloses that "[t]he circuit further includes a sensor connected to the switch current regulator, the LED, and a signal feedback circuit" where "[t]he sensor measures status information about the switch current regulator and the LED and provides the status information to a controller via the signal feedback circuit" so "[a]t the controller, the status information can be used to adjust the voltage on the current control signal input." *Id*. "A sensor (or sensors) 310 can be used to detect Voltage and current magnitudes, temperatures, and so forth of the LED 110, the drive current, driver circuitry, or so on, and feed the information back to the LED driver circuit 305 which can make necessary adjustments to the drive current to optimize the operation of the LED 110." *Id.*, ¶ 0025. Garcia discloses that "[t]he feedback information from the sensor 310 can be used directly by the LED driver circuit 305 or be provided to the controller 120, which can issue additional LED instructions to the LED driver circuit 305 to make the necessary adjustments to the drive current." *Id*.

Shimizu (JP2004327152) describes an "LED lighting device . . . to output a target current flowing in an LED." Shimizu, Abstract. Shimizu discloses a "PWM circuit 13 performs the

switching operation of field effect transistor FET1 on the basis of the multiplied signal output from multiplier circuit 12" which "multiplies the error from the error amplifier 9 by the voltage between both ends of resistor R3 [*e.g.*, a reference voltage]," where the "voltage between both ends of the resistor R1 detected by the LED current detection circuit 4 is input to one input terminal of the error amplifier 9" and "error amplifier 9 outputs an effective value of the voltage between both ends of the resistor R3 and the resistor R1 to the multiplier circuit 12." *Id.*, ¶ 0023. Shimizu recognized that "a target current flows through the LED load 2 as a result of the effective value output from the effective value detection circuit 5 matching (substantially matching) the voltage between both ends of the resistor R1 detected by the LED current detection circuit 4" and "[i]n other words, the current flowing in the LED load 2 becomes a current value (target current) in accordance with the effective value detected by the effective value detection circuit 5." *Id*. Shimizu disclosed that "the current waveform of the input current of the boost chopper circuit 11, that is, the current waveform of the DC current of the rectifier circuit 3, is substantially similar to the voltage waveform of the DC voltage of the rectifier circuit 3, and the input current of the boost chopper circuit 11 is controlled in proportion to the multiplication signal (output signal) of the multiplier circuit 12" so "[t]he target current (effective value of the voltage between both ends of the resistor R3) output from the effective value detection circuit 5 matches (substantially matches) the current flowing in the LED load 2 (voltage between both ends of the resistor R1)." *Id*.

Nagase describes "an LED driving device which lights an LED stably" that includes "a voltage detection circuit . . . which detects a voltage applied to the LED light source . . . ; and a current detecting resistor R0 which detects ad current I flowing in the LED light source 6." Nagase, Abstract. "[T]he drive control unit 3 performs on / off control of the switching element S0 while monitoring the output of the lighting circuit unit 2 by the voltage detection circuit unite 5 and the

current detection resistor R0, and controls the switching element S0 on / off" and "the output voltage V is adjusted so that the current I flowing through the LED light source 6 becomes a set value." *Id*. at p. 3.

Shteynberg describes "a system" that "drives one or plurality of LEDs regulating their brightness by controlling LEDs average current or voltage" and "relates generally to power conversion, and more specifically, to a system and method for driving LEDs, and particularly to integrated LED drivers with digital controllers." Shteynberg, Abstract and 1:12–15. Shteynberg recognizes that "[a]n LED, having a diode type volt amp characteristic, presents a very difficult load for a voltage type regulators" and "[t]hat's why all up to date LED drivers are constructed as a regulated current source[.]" *Id*., 1:27–67. "The current regulator . . . includes feedback, which is created as a voltage signal proportional to the average LED current." *Id*. Shteynberg discloses that "a digital PI or PID regulator" is "capable to drive one or a plurality of LEDS with the continuous current in the switching converter" based on an LED current. *Id*., 9:31–63.

Robinson is related to "the field of driver circuits, and more particularly, to driver circuits that provide switched constant current sources for electronic devices such as light-emitting elements." Robinson, 1:15–18. Robinson discloses that "[l]ight-emitting diodes are current driven devices, meaning that the amount of current passing through an LED controls its brightness." *Id*., 1:31–33. Robinson includes "a temperature sensitive device that changes the resistance of [a] resistor divider feedback look as the light-emitting element junction temperature changes" to allow for "temperature-based correction." *Id*., 13:12–25. "The feedback means is used to maintain the desired current level flowing through the electronic devices" and "[v]oltage converter 12 . . . adjusts its output voltage to provide a constant current to the light-emitting element load." *Id*., 10:22–38.

Mubaslat describes "[a] system (10) and method for monitoring the . . . performance of one or more light-emitting diodes (LEDs) (20) based on sensed parameters[.]" Mubaslat, Abstract. "LED performance may include . . . measuring operational characteristics of an LED when it is activated (turned on)." *Id.*, 2:55–62. "LED voltage and current measurements may even be used to indirectly monitor the diode junction temperature while the LED bank 20 is activated[.]" *Id.*, 11:16–19. "LED power control and operations monitoring subsystem 10 may be configured to control power dissipation and light intensity of the LED bank 20 during operation according to a PWM and/or PAM technique[.]" *Id.*, 3:66–4:10.

Impedance detection

It was well-known prior to the alleged invention of the '830 patent that "voltage, current, and resistance are related by Ohm's law," which relates voltage (V) with current (I) and resistance (R) as: V = I * R. John A. Camara, PE, ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM, (6th ed. 2002), 26–3. "Electrical impedance . . . is the total opposition a circuit presents to alternating current" and is "analogous to Ohm's law[.]" *Id.*, 27–3. Impedance is the "complex sum of a circuit's resistive (R) and reactive (X) components" and is shown by Z (impedance) = R (resistive) + jX (reactive) where R = Z cos ϕ and X = Z sin ϕ. *Id.* Ignoring the reactive component, Z (impedance) = R (resistance). *Id.* Further, it was also well-known that semiconductor devices, such as LEDs, typically have non-linear impedance. STEVE WINDER, POWER SUPPLIES FOR LED DRIVING, § 2.4 (2008).

Nishimura describes "control circuitry" for an "LED's [light emitting diode] operating current" and recognizes that "[i]t is known that the voltage at which an LED starts to conduct appreciable current (*i.e.,* its turn-on voltage), as well as the LED's dynamic impedance, are functions of the LED's junction temperature and aging effects[.]" Nishimura, 4:59–67, Fig. 5, and 2:22–25. Nishimura discloses that "[c]omputation of the dynamic impedance comprises dividing

the amplitude of the recovered voltage component by the amplitude of the operating current" and that the dynamic impedance can be used "to set a desired light intensity of the LED" (*e.g.*, by modifying the drive current). *Id*., 3:61–65 and 6:10–19; *see also id*. at 2:60–3:5.

Hente describes a "driver circuit for supplying power to [] LED/OLED device[.]" Hente, 1:23–24. Hente discloses that "[p]rior art techniques have utilized simple static measurements delivering only one parameter for determining a status or condition of a LED/OLED device for compensating aging, etc." and that "[t]his parameter is, for example, forward voltage or slope of the IV [current-voltage] curve or an impedance value." *Id*., 1:32–36. Hente further discloses "determining impedance values of said device" and "matching the impedance values to . . . an equivalent circuit network . . ., such that the impedance of the circuit network corresponds to the determined impedance value" (*id*., 2:59–64) and "can be used by an OLED driver controller" to "adapt the driver operation[.]" *Id*., 8:56–67.

Chen describes "[a] light source driving circuit" with "a feedback circuit" that and "comprises an impedance detection circuit and a feedback voltage control circuit" where "[t]he level of output by the detection terminal of the impedance detection circuit is determined according to the impedance between the first terminal and the second terminal" and "[t]he input terminal of the feedback voltage control circuit is coupled to the detection terminal of the impedance detection circuit and controls the voltage value of the feedback signal output by the output terminal according to the level output by the detection terminal of the impedance detection circuit." Chen, 2:40–58.

Ito describes "a lighting control apparatus and a method of lighting control for a vehicle lighting device and, in particular, relates to a lighting control apparatus and method of lighting control for a vehicle lighting device which is configured to control the lighting of a semiconductor

light source constituted by a semiconductor light emitting element." Ito, 1:7-12. Ito recognizes that "leak failure of an LED is considered as another abnormality and, in this case, the LED has a certain impedance" such that "when leak failure occurs in an LED, a forward voltage Vf according to the impedance is generated when the LED is supplied with a current" and "[t]he forward voltage Vf is lower than a forward voltage in the normal state." *Id.*, 2:60-39. "A microcomputer compares a forward voltage generated from the semiconductor light source during the current restriction period with an abnormality determination value to determine whether or not an abnormality occurs due to a change of the forward voltage of the semiconductor light source." *Id.*, Abstract.

As recognized by the '830 APA, the "voltage-current characteristics of a diode" (*e.g.*, a light-emitting diode or LED) were "well-known" before the alleged invention of the '830 patent and are described in Fig. 3A. '830, Fig. 3A, 3:27–54. The corresponding impedance characteristics are shown in Fig. 3B and the corresponding gain characteristics are shown in Fig. 3C. *Id.*, Figs. 3B–C and 3:27–54. Because the "well known voltage-current characteristics of a diode" (including LEDs) include a non-linear increase in current in response to an increase in voltage (*see* Fig. 1), and accordingly that the impedance of the diode decreases non-linearly with increased voltage (*see* Fig. 2), it was well understood that voltage control circuits could use feedback (*e.g.*, current, voltage, temperature, etc.) to control a current applied to an LED. Similarly, it was well known that the impedance of a circuit could be measured and used as feedback to control a drive current to an LED. As such, it would have been obvious to a person of ordinary skill in the art at the time of the earliest priority date of the '830 patent to combine one or more of the impedance- detection references discussed above (*e.g.*, Nishimura, Hente, Chen, and Ito) with one or more of the references discussed above disclosing drive circuits for semiconductor light sources (*e.g.*, '830

APA, Shimizu, Robinson, Nagase, Tripathi ’559, Tripathi ’512, Bhagat, Barth, Garcia, Shteynberg, and Mubaslat).

C. Claim Charts—P.R. 3-3(c)

Pursuant to P.R. 3-3(c), and subject to Defendant’s reservation of rights, claim charts providing a limitation-by-limitation analysis of where specifically, in each prior art item, each limitation of the Asserted Claims of the Asserted Patents are attached in Exhibits A-01 through G-12 and J-01 through L19. Some of the claim charts for foreign language references may include quotations and citations to machine translations. Defendant reserves the right to obtain and rely on a certified translation for each of the foreign language references relied upon in these invalidity contentions.

Defendant further incorporates by reference, as if fully set forth herein, the claim charts in the Asserted Patent IPRs and Other Invalidity Contentions.

1. Claim Charts for U.S. Patent No. 6,525,798

Exhibit	Prior Art Reference
Exhibit A-01	JP H07-128683 (“Fujii”)
Exhibit A-02	US 6,337,726 (“Kawano”)
Exhibit A-03	WO 98/47044 (“Ohta ’044”)
Exhibit A-04	WO 98/27454 (“Ohta ’454”)
Exhibit A-05	JP H09-73101 (“Ohta ’101”)
Exhibit A-06	US 5,886,762 (“Lee”)
Exhibit A-07	US 6,452,656 (“Niwano”)
Exhibit A-08	Prior Art Products
Exhibit A-09	JP H11-30784 (“Aratani”)
Exhibit A-10	JP H08-29812A (“Satou”)
Exhibit A-11	US 6,400,440 (“Colgan”)
Exhibit A-12	US 5,434,690 (“Hisatake”)
Exhibit A-13	US 5,745,207 (“Asada”)
Exhibit A-14	US 6,266,116 (“Ohta ’116”)
Exhibit A-15	US 6,288,763 (“Hirota”)
Exhibit A-16	US 6,342,937 (“Hiroshi”)
Exhibit A-17	US 5,499,123 (“Mikoshiba”)

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Bishop Display's Exhibit 2007
Ex. 2007, Page 171

2. Claim Charts for U.S. Patent No. 6,787,829

Exhibit	Prior Art Reference
Exhibit B-01	US 6,337,726 ("Kawano")
Exhibit B-02	WO 98/27454 ("Ohta '454")
Exhibit B-03	US 6,452,656 ("Niwano")
Exhibit B-04	US 6,222,599 ("Yoshida")
Exhibit B-05	US 5,995,187 ("Wakagi")
Exhibit B-06	JP H09-73101 ("Ohta '101")
Exhibit B-07	Prior Art Products
Exhibit B-08	US 5,907,379 ("Kim")
Exhibit B-09	US 5,723,878 ("Yanai")
Exhibit B-10	US 6,532,053 ("Ohta '053")
Exhibit B-11	JP H11-174490 ("Jun")
Exhibit B-12	JP H11-352514 ("Yamada")
Exhibit B-13	JP H04-104227 ("Matsui")

3. Claim Charts for U.S. Patent No. 6,801,293

Exhibit	Prior Art Reference
Exhibit C-01	JPH9-274190 ("Nishikawa 1997")
Exhibit C-02	US 5,949,509 ("Ohe")
Exhibit C-03	JPH7-248478 ("Hideaki")
Exhibit C-04	Prior Art Products
Exhibit C-05	JPH10-213802 ("Tsumura")
Exhibit C-06	JPH0-588180 ("Sawatsubashi")
Exhibit C-07	JPH5-142542 ("Ichikawa")
Exhibit C-08	JPH11-202334 ("Yamada")
Exhibit C-09	US 6,341,003 ("Ashizawa")
Exhibit C-10	US 6,839,113 ("Watanabe")
Exhibit C-11	JPH10-148834 ("Minhara")
Exhibit C-12	JPH09-96818A ("Mori")

4. Claim Charts for U.S. Patent No. 6,816,208

Exhibit	Prior Art Reference
Exhibit D-01	US 6,028,650 ("Kuroha")
Exhibit D-02	JPH05-232509 ("Nishikawa 1993")
Exhibit D-03	US 6,020,214 ("Watanabe '214")
Exhibit D-04	KR2000-0003113 ("Yoo")
Exhibit D-05	JPH07-029535 ("Yamada 1995")
Exhibit D-06	JP2000-56322 ("Yamada 2000")
Exhibit D-07	Prior Art Products
Exhibit D-08	US 5,459,596 ("Ueda")

5. Claim Charts for U.S. Patent No. 6,850,303

Exhibit	Prior Art Reference
Exhibit E-01	JP H09-236820 (“Nakagawa”)
Exhibit E-02	JP P2000-98420 (“Iizuka”)
Exhibit E-03	US 6,812,975 (“Nagahiro”)
Exhibit E-04	US 5,852,485 (“Shimada”)
Exhibit E-05	US 5,182,661 (“Ikeda”)
Exhibit E-06	Prior Art Products
Exhibit E-07	US 6,335,770 (“Komatsu”)
Exhibit E-08	EP 1,037,093 (“Tanaka”)
Exhibit E-09	US 6,590,227 (“Ishikawa”)
Exhibit E-10	US 6,281,957 (“Young”)
Exhibit E-11	US 6,771,342 (“Hirakata”)
Exhibit E-12	US 6,445,435 (“Seo”)
Exhibit E-13	US 6,259,502 (“Komatsu ’502”)
Exhibit E-14	KR0144233 (“Lee”)
Exhibit E-15	KR2000-0009305 (“Kim”)
Exhibit E-16	US 5,734,448 (“Cheng”)
Exhibit E-17	US 5,923,390 (“Mok”)
Exhibit E-18	US 6,326,641 (“Choi”)
Exhibit E-19	US 2003/0071930 Al (“Nagahiro ’930”)
Exhibit E-20	JP 3096394 (“Fujiwara”)

6. Claim Charts for U.S. Patent No. 6,906,769

Exhibit	Prior Art Reference
Exhibit F-01	US 6,335,770 (“Komatsu”)
Exhibit F-02	US 4,909,602 (“Kaneko”)
Exhibit F-03	JPH8-95075 (“Shimada”)
Exhibit F-04	JPH10-186407 (“SakamotoJP407”)
Exhibit F-05	US 6,069,678 (“SakamotoUS678”)
Exhibit F-06	JPH9-96794 (“Watanabe JP ’794”)
Exhibit F-07	Prior Art Products
Exhibit F-08	US 6,005,543 (“Kimura”)
Exhibit F-09	JPH6-202127 (“OtaJP127”)

7. Claim Charts for U.S. Patent No. 7,414,682

Exhibit	Prior Art Reference
Exhibit G-01	JPH09-269508 (“Matsumoto”)
Exhibit G-02	WO98/27454 (“Ohta ’454”)
Exhibit G-03	JP2000-98404 (“Kubota”)
Exhibit G-04	US 5,907,379 (“Kim”)
Exhibit G-05	JPH10-301141 (“Asada”)
Exhibit G-06	U.S. Patent No. 6,452,656 (“Niwano”)

Exhibit G-07	U.S. Patent No. 5,969,782 (“Seung Hee Lee”)
Exhibit G-08	Prior Art Products
Exhibit G-09	WO1999045430A1 (“Ota5430”)
Exhibit G-10	JPH07199169A (“Yamaji”)
Exhibit G-11	U.S. Patent No. 6,563,561 (“Ota561”)
Exhibit G-12	U.S. Patent No. 5,852,485 (“Shimada”)

8. Claim Charts for U.S. Patent No. 7,583,347

Exhibit	Prior Art Reference
Exhibit J-01	US 5,949,509 (“Ohe”)
Exhibit J-02	WO98/27454 (“Ohta ’454”)
Exhibit J-03	US 6,351,300 (“Park”)
Exhibit J-04	JPH10-301141 (“Asada”)
Exhibit J-05	JPH09-269508 (“Matsumoto”)
Exhibit J-06	JPH10-170916 (“Hiyama”)
Exhibit J-07	SID Seminar Note (May 14, 2000) (“Sang Soo Kim”)
Exhibit J-08	U.S. Patent No. 6,452,656 (“Niwano”)
Exhibit J-09	U.S. Patent No. 5,969,782 (“Seung Hee Lee”)
Exhibit J-10	Prior Art Products
Exhibit J-11	KR100341123B1 (“Lee”)
Exhibit J-12	JP2000091592A (“Yamazaki”)
Exhibit J-13	U.S. Patent No. 5,995,187 (“Wakagi”)
Exhibit J-14	U.S. Patent No. 5,978,059 (“Ohta059”)
Exhibit J-15	KR19990088122A (“Ashizawa”)

9. Claim Charts for U.S. Patent No. 7,995,047

Exhibit	Prior Art Reference
Exhibit K-01	US 7,760,161 or USP 2005/0017765 (“Sasaki”)
Exhibit K-02	US 6,870,192 (“Yamazaki”)
Exhibit K-03	US 7,760,163 or USP 2006/0158396 (“Jo”)
Exhibit K-04	US 7,268,717 or USP 2006/0170629 (“Baek”)
Exhibit K-05	US 7,859,489 (“Furuichi”)
Exhibit K-06	US 7,679,586 (“Stewart”)
Exhibit K-07	US 7,304,621 or US 2004/0201556 (“Oomori”)
Exhibit K-08	US 7,626,565 or US 2006/0232612 (“Tsuge”)
Exhibit K-09	US 8,044,892 or US 2006/0118700 (“Chaussy”)
Exhibit K-10	US 2005/0140601 (“Kasai”)
Exhibit K-11	US 8,325,111 or USP 2007/0126664 (“Kimura”)
Exhibit K-12	Jane Woo Ryu, “A Design of AM-OLED Source Driver with reduced Programming Time for a Large Scale Display Panel” (“Ryu”)
Exhibit K-13	M. Shimoda, “An integrated poly-Si TFT current data driver with a data- line pre-charge function. Journal of the Society for Information Display” (“Shimoda”)

Exhibit K-14	J.H. Baek, "A Current-Mode Display Driver IC Using Sample-and-Hold Scheme for QVGA Full-Color AMOLED Displays" ("Baek Dec. Publication")
Exhibit K-15	M. Liu, "A Single Driver Chip for Gray Scale Passive-Matrix OLED" ("Liu"
Exhibit K-16	S. Alexander, "Pixel circuits and drive schemes for glass and elastic AMOLED displays" ("Alexander")
Exhibit K-17	J.H. Baek, "A Current Driver IC using a S/H for QVGA Full-Color Active-Matrix Organic LED Mobile Displays" (Baek Feb. Publication")
Exhibit K-18	Prior Art Products

10. Claim Charts for U.S. Patent No. 8,093,830

Exhibit	Prior Art Reference
Exhibit L-01	Admitted prior art ("APA") disclosed in U.S. Patent No. 8,093,830 ('830 APA)
Exhibit L-02	JP Pat. Pub. No. 2004-327152 to Shimizu et al. ("Shimizu")
Exhibit L-03	U.S. Pat. No. 7,332,699 to Nishimura et al. ("Nishimura")
Exhibit L-04	U.S. Pat. No. 8,242,787 to Hente et al. ("Hente")
Exhibit L-05	U.S. Pat. No. 7,471,287 to Chen et al. ("Chen")
Exhibit L-06	U.S. Pat. No. 7,262,559 to Tripathi et al. ("Tripathi '559")
Exhibit L-07	U.S. Pat. No. 6,577,512 to Tripathi et al. ("Tripathi '512")
Exhibit L-08	WO Pat. Pub. No. WO 2005/079121 to Bhagat et al. ("Bhagat")
Exhibit L-09	U.S. Pat. No. 7,391,335 to Mubaslat et al. ("Mubaslat")
Exhibit L-10	JP. Pat. Pub. No. 2006-210271 to Nagase et al. ("Nagase")
Exhibit L-11	U.S. Pat. No. 7,202,608 to Robinson et al. ("Robinson")
Exhibit L-12	U.S. Pat. No. 6,285,139 to Ghanem et al. ("Ghanem")
Exhibit L-13	J.P. Pat. Pub. No. 2006-303093 to Matsuda et al. ("Matsuda")
Exhibit L-14	U.S. Pat. No. 7,276,861 to Shteynberg et al. ("Shteynberg")
Exhibit L-15	U.S. Pat. No. 8,111,014 to Van Erp et al. ("Van Erp")
Exhibit L-16	U.S. Pat. No. 6,747,420 to Barth et al. ("Barth")
Exhibit L-17	U.S. Pat. No. 7,492,108 to Garcia et al. ("Garcia")
Exhibit L-18	'830 Prior Art Products
Exhibit L-19	U.S. Pat. App. 2007/0170876 to Ito et al. ("Ito")

D. Invalidity Under 35 U.S.C. § 112—P.R. 3-3(d)

Pursuant to P.R. 3-3(d), and subject to Defendant's reservation of rights, Defendant contends that the Asserted Claims of the Asserted Patents are invalid under 35 U.S.C. § 112 because (1) the claims are indefinite, (2) the claims lack adequate written description; and/or (3) the claims are not enabled. Defendant's contentions that the following claims are invalid under 35 U.S.C. § 112 are made in the alternative and do not constitute, and should not be interpreted as,

admissions regarding the construction or scope of the claims of the Asserted Patents, or that any of the claims of the Asserted Patents are not anticipated or rendered obvious by prior art.

The disclosures below do not attempt to identify all recitations of a given term or phrase in each claim. Where Defendant has identified an instance of a term or limitation in a particular claim that renders the claim invalid under Section 112, Defendant contends that every instance of the challenged term or limitation, or similar term or limitation, in the claim renders the claim invalid for the same reasons. The following contentions are subject to revision and amendment under Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter where appropriate in light of further investigation and discovery regarding the defenses below, the Court's construction of the claims at issue, or the review and analysis of expert witnesses. Defendant offers these contentions in response to Plaintiff's apparent interpretation of the Asserted Claims and Infringement Contentions, which remain insufficient under the Patent Rules, including for failure to provide a "chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality" as required by P.R. 3-1(c), as well as the reasons articulated in Defendant LG Display Co, Ltd.'s July 31, 2024, letter to Plaintiff.

1. Lack of Enablement and Written Description

One or more Asserted Claims of the patents-in-suit are invalid under § 112, ¶ 1 for failing to particularly point out and distinctly claim the subject matter which the patentee regards as its alleged invention such that one skilled in the relevant art would be reasonably apprised of the bounds of the asserted claims when read in light of the specification. Section 112, paragraph 1 requires that the specification contain a written description of the invention. "[T]he hallmark of written description is disclosure." *Boston Scientific Corp. v. Johnson & Johnson*, 647 F. 3d 1353, 1361-62 (Fed. Cir. 2011) (citation omitted). The test for whether a specification adequately describes an invention is "whether the disclosure of the application relied upon reasonably conveys

to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date [T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art [It] is a question of fact." *Ariad Pharms., Inc. v. Eli Lilly and Co.,* 598 F. 3d 1336, 1351 (Fed. Cir. 2010) (*en banc*); *Boston Scientific*, 647 F. 3d at 1362.

Section 112, paragraph 1 also requires that the patent specification enable "those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'" *Genentech, Inc. v. Novo Nordisk A/S*, 108 F. 3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wright*, 999 F. 2d 1557, 1561 (Fed. Cir. 1993)). "[T]he scope of the claims must be less than or equal to the scope of the enablement." *Nat'l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.,* 166 F. 3d 1190, 1196 (Fed. Cir. 1999).

Subject to Defendant's reservation of rights, Defendant identifies the following written description and enablement grounds with respect to the following asserted claims. The following does not purport to list every claim limitation to the foregoing disclosed grounds. Where a particular claim term or limitation is identified, Defendant contends that the identified term or limitation, as well as the surrounding claim language in context as recited in the applicable claim, suffer from the identified Section 112 defect. Furthermore, where a particular claim term or limitation is identified with respect to one or more particular claims, Defendant contends that each other Asserted Claim that recites the same claim term or limitation, or similar claim term or limitation, is subject to the same Section 112 defect. Defendant also reserves the right to assert additional Section 112 defenses as discovery progresses.

The Asserted Claims fail to meet the requirements of 35 U.S.C. § 112, ¶ 1 because the specifications of the Asserted Patents do not contain a written description of the alleged invention

and do not enable a person skilled in the art to make and use the alleged invention. In particular, at least the following limitations of the Asserted Claims are not enabled and/or lack written description support:

'798 Patent

- The asserted claims of the '798 patent lacks adequate written description because the specification of the '798 patent fails to convey to a POSITA that the inventor had possession of the claimed invention as of the filing date. Moreover, claim 1 of the '798 patent is not enabled because the specification of the '798 patent does not teach a POSITA how to make and use the full scope of claim 1 without undue experimentation. For example, to the extent claim 1 of the '798 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the '798 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (e.g., VA-mode, TN-mode).

- If the limitation of the asserted claims, "each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes" encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the claim is not enabled and lacks written description support, particularly with respect to the terms "pair" or "pairs" and "adjacent."

- If the limitation of the asserted claim, "at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode" encompasses the alternative theories identified by Plaintiff in its infringement contention claim charts, then the claim is not enabled and lacks written description support, particularly with respect to the term "thickness."

- If the term "common electrode" or "common electrodes" in asserted claim 1 encompass the structure in the accused products that Plaintiff points to in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the term "electrode pair" or "electrode pairs" in asserted claim 1 encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the term "adjacent" in the asserted claims encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the term "thickness" in the asserted claims encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the claim is not enabled and lacks written description support.

'829 Patent

- The asserted claims of the '829 patent lack adequate written description because the specification of the '829 patent fails to convey to a POSITA that the inventor had possession of the claimed inventions as of the filing date. Moreover, the asserted claims of the '829 patent are not enabled because the specification of the '829 patent does not teach a POSITA how to make and use the full scope of the asserted claims without undue experimentation. For example, to the extent the asserted claims of the '829 patent were read to encompass displays other than in- plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the '829 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (*e.g.*, VA-mode, TN-mode).

- All asserted claims are not enabled and lack written description support due to the limitation of independent claims 1 and 29: "a plurality of image signal lines located over the surface of the array substrate that is in contact with the liquid crystal layer, the image signal lines being aligned in a same direction," and in particular, the requirement of "in contact with" as used in this limitation.

- If the limitation of asserted claims 1 and 29, "a line-shaped pixel electrode located in each of pixel regions of the array substrate that is surrounded by the image signal lines and the scanning signal lines, the pixel electrode located parallel to the image signal lines or to the scanning signal lines," encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support, particularly with respect to the "parallel" requirement.

- If the limitation of asserted claims 1 and 29, "a common electrode located in each of the pixel regions and located parallel to the pixel electrode," encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support, particularly with respect to the "parallel" requirement.

- If the limitation of asserted claims 1 and 29, "wherein, of the pixel electrode and the common electrode, the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines comprises an opaque conductor, and at least one of the other electrodes comprises a transparent conductor," encompasses the structure in the accused products that Plaintiff points to in its

infringement contentions, then the asserted claims are not enabled and lack written description support, particularly with respect to the "parallel" requirement.

- If the term "common electrode" in asserted claims 1 and 29 encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the claims are not enabled and lack written description support.

'293 Patent

- Claim 1 of the '293 patent lacks adequate written description because the specification of the '293 patent fails to convey to a POSITA that the inventor had possession of the claimed invention as of the filing date. Moreover, claim 1 of the '293 patent is not enabled because the specification of the '293 patent does not teach a POSITA how to make and use the full scope of claim 1 without undue experimentation. For example, the specification of the '293 patent fails to adequately disclose how to manufacture a liquid crystal display device with "a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates" without undue experimentation. The specification further fails to convey to a POSITA that the inventor had possession of the claimed manufacturing step of "a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates." As another example, to the extent claim 1 of the '293 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the '293 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (*e.g.*, VA-mode, TN-mode).

- If the limitation of asserted claim 1, "a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates," encompasses the method used to manufacture the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

'208 Patent

- Claim 1 of the '208 patent lacks adequate written description because the specification of the '208 patent fails to convey to a POSITA that the inventor had possession of the claimed invention as of the filing date. Moreover, claim 1 of the '208 patent is not enabled because the specification of the '208 patent does not teach a POSITA how to make and use the full scope of claim 1 without undue experimentation. For example, the specification of the '208 patent fails to adequately disclose how to make and use a liquid crystal display device "wherein the value of the storage capacity in said

capacitive accumulation portion of the one pixel is different from that of the adjacent pixel by varying an aperture in the common electrode of the adjacent pixel with respect to the aperture of the one pixel." The specification further fails to convey to a POSITA that the inventor had possession of the claimed structure: "wherein the value of the storage capacity in said capacitive accumulation portion of the one pixel is different from that of the adjacent pixel by varying an aperture in the common electrode of the adjacent pixel with respect to the aperture of the one pixel."

- To the extent claim 3 of the '208 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the '208 patent fails to disclose how to make and use such a device without undue experimentation. A POSITA would understand that there are differences in the design, structure, and operation of in- plane switching displays from the design, structure, and operation of other types of displays (*e.g.*, VA-mode).

- If the limitation of asserted claim 1, "a capacitive accumulation portion formed by overlapping a pixel electrode, an insulating layer and a common electrode for each pixel area," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "and a non-electrode area in a part of the pixel area which is not covered with a pixel electrode," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "wherein a peripheral shape of said capacitive accumulation portion on a side contacting said non-electrode area is substantially the same between respective pixels," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "a value of a storage capacity in said capacitive accumulation portion of one pixel at a signal feeding side is larger than that of an adjacent pixel at a termination side," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "wherein the value of the storage capacity in said capacitive accumulation portion of the one pixel is different from that of the adjacent pixel by varying an aperture in the common electrode of the adjacent pixel with respect to the aperture of the one pixel," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

’303 Patent

- The asserted claims of the ’303 patent lack adequate written description because the specification of the ’303 patent fails to convey to a POSITA that the inventor had possession of the claimed inventions as of the filing date. Moreover, the asserted claims of the ’303 patent are not enabled because the specification of the ’303 patent does not teach a POSITA how to make and use the full scope of the asserted claims without undue experimentation. For example, to the extent the asserted claims of the ’303 patent were read to encompass displays other than in- plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the ’303 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (*e.g.*, VA-mode, TN-mode).

- If the limitation of asserted claim 1, “a common electrode being electrically connected to the common wiring and generating an electric field between the common electrode and the pixel electrode creating a voltage for driving the liquid crystal,” encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support, in particular the requirement of “generating an electric field between the common electrode and the pixel electrode creating a voltage for driving the liquid crystal.”

- If the limitation of asserted claim 1, “wherein the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer” encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support.

- If the limitation “a storage capacity electrode electrically connected to the pixel electrode” in asserted claim 1 encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support.

- If the term “common wiring” in asserted claim 1 encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support.

- If the term “common electrode” in asserted claim 1 encompasses the structure in the accused products that Plaintiff points to in its infringement contentions, then the asserted claims are not enabled and lack written description support.

’769 Patent

- To the extent claim 1 of the ’769 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the ’769 patent fails to disclose how to make and use such a device without undue experimentation. A POSITA would understand that there are differences in the design, structure, and operation of in- plane switching displays from the design, structure, and operation of other types of displays (*e.g.*, VA-mode).

- If the limitation of asserted claim 1, “a first conductive member which is formed on the first insulating substrate and interposed between the first insulating substrate and its corresponding alignment layer ... the first conductive member being gate signal lines,” encompasses the structure of the accused products that Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, “a first conductive member ... being in partial contact with the alignment layer ... the first conductive member being gate signal lines,” encompasses the structure of the accused products that Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, “a first conductive member ... to which a negative voltage is applied, the first conductive member being gate signal lines,” encompasses the structure of the accused products that Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

’682 Patent

- Claims 7 and 9 of the ’682 patent lack adequate written description because the specification of the ’682 patent fails to convey to a POSITA that the inventor had possession of the claimed invention as of the filing date. Moreover, claims 7 and 9 of the ’682 patent are not enabled because the specification of the ’682 patent does not teach a POSITA how to make and use the full scope of claims 7 and 9 without undue experimentation. For example, to the extent claims 7 and 9 of the ’682 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the ’682 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (*e.g.*, VA-mode, TN-mode).

- If the preamble of asserted claim 7, “[a] liquid crystal display of transversal electric field type,” encompasses the structure of the accused products, as Plaintiff appears to

assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 7, "a plurality of scanning signal lines and a plurality of video signal lines formed so as to define a plurality of pixels in a matrix on an inner surface of one of the pair of substrates," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 7, "a pixel electrode and a common electrode formed opposite to each other in each pixel in a plan view," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 7, "an image is displayed on the liquid crystal panel by inputting a video signal from the video signal line into the pixel electrode while sequentially selecting the pixel through the scanning signal line," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

'347 Patent

- Claim 1 of the '347 patent lacks adequate written description because the specification of the '347 patent fails to convey to a POSITA that the inventor had possession of the claimed invention as of the filing date. Moreover, claim 1 of the '347 patent are not enabled because the specification of the '347 patent does not teach a POSITA how to make and use the full scope of claim 1 without undue experimentation. For example, to the extent claim 1 of the '347 patent were read to encompass displays other than in-plane switching (IPS, lateral electric type, or transversal electric field type) liquid crystal displays, the specification of the '347 patent fails to disclose how to make and use such a device without undue experimentation, and fails to convey that the alleged inventors had possession of such a device at the timing of the filing of the patent. A POSITA would understand that there are differences in the design, structure, and operation of in-plane switching devices from the design, structure, and operation of other types of displays (*e.g.*, VA-mode, TN-mode).

- If the limitation of asserted claim 1, "an array substrate having an upper surface on which a common electrode, a pixel electrode, a scanning signal line, a video signal line, and a semiconductor switching device are formed," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "an opposing substrate disposed so as to be opposite to the upper surface of the array substrate," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "at least one electrode of the common electrode and the pixel electrode is constituted by an electrode portion and a wiring portion," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "the electrode portion is at least partially constituted by a transparent electric conductor," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "the electrode portion is formed in a layer separated by an insulating layer from a layer in which the scanning signal line is formed," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

- If the limitation of asserted claim 1, "the wiring portion is formed in the layer in which the scanning signal line is formed," encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim is not enabled and lacks written description support.

'047 Patent

- Claim 1 of the '047 Patent is invalid for lacking written description. The '047 Patent was filed in the United States on December 12, 2007. On December 8, 2010, the USPTO Examiner issued an office action, finding claims 1-10 anticipated by the prior art. On March 7, 2011, the applicants responded to the office action by amending claim 1 to recite, *inter alia*, a voltage holding "circuit having a terminal being connected to a reference voltage different from the first voltage." The amendments to claim 1 are shown below:

1. (Currently Amended) A current driving device, comprising:

a first voltage supply [[part]] source for supplying a first voltage;

a first current supply [[part]] source for supplying a first electric current;

a plurality of output terminals; and

a plurality of current output [[parts]] circuits for outputting an electric current in accordance with said first electric current, each of said current output [[parts]] circuits comprising a current-voltage converting ~~function~~ circuit, a voltage-current converting ~~function~~ circuit, a voltage holding [[part]] circuit having a terminal being connected to a reference voltage different from the first voltage, and at least one current output terminal, wherein:

each of said current output ~~part takes~~ circuits operates in three operation modes [[, i.e.]] including a voltage supply mode, a current supply mode, and a current output mode,

under said voltage supply mode, each of said current output [[part]] circuits receives said first voltage from said first voltage supply [[part]] source, and ~~holds said voltage in~~ the first voltage is supplied to another terminal of said voltage holding [[part]] circuit,

under said current supply mode, each of said current output [[part]] circuits receives said first current from said first current supply [[part]] source, and generates a second voltage by said current-voltage converting ~~function~~ circuit, and ~~holds said voltage in~~ the first current is supplied to said another terminal of said voltage holding [[part]] circuit, and

under said current output mode, each of said current output [[part]] circuits outputs an output current according to said voltage held in said voltage holding [[part]] circuit by said voltage-current converting ~~function~~ circuit.

- As of the filing date of the ’047 Patent (December 12, 2007), there was no support in the specification for this limitation.

’830 Patent

- If the following from claim 1, “an impedance detecting section that detects an impedance of the semiconductor light source” and “the output voltage controlling section controls the output voltage of the voltage source based on an output of the current comparing section and an output of the impedance detecting section” encompasses the structure of the accused products, as Plaintiff appears to assert in its infringement contentions, then the claim lacks written description support.

- For example, the only “impedance detecting section” disclosed by the ’830 patent is “impedance detecting circuit 150” that “is constituted by divider 152” which “finds the impedance of semiconductor light source 110 (strictly speaking, a value corresponding to the impedance of semiconductor light source 110, hereinafter “impedance equivalent value”) by diving the output voltage of voltage source 170 supplied to semiconductor light source 110 by the output current of semiconductor light source 110 detected by output current detecting circuit 120” such that “[b]y this means, it is possible to find an

impedance equivalent value which corresponds to the characteristics in FIG. 3B showing the impedance characteristics of semiconductor light source 110, in a state in which semiconductor light source 110 is actually driven." '830 patent, 7:32–47.

- As another example, the only disclosure of "the output voltage controlling section controls the output voltage of the voltage source based on an output of the current comparing section and an output of the impedance detecting section" is "Gain circuit 162" that "multiplies, at multiplier 163, the output of current comparing circuit 140 (i.e. the difference between the current command value and the drive current detecting value of semiconductor light source 110), by the impedance equivalent value of semiconductor light source 110 detected by impedance detecting circuit 150" such that "[b]y this means, gain circuit 162 of output voltage controlling circuit 160 has gain characteristics proportional to the impedance characteristics of semiconductor light source 110." *Id*. 7:54–62. "That is, gain circuit 162 multiplies the output of current comparing circuit 140 and the impedance equivalent value of semiconductor light source 110 detected by impedance detecting circuit 150, to prevent the gain of the control loop from changing even when the impedance of semiconductor light source 110 changes, that is, automatically adjusts the characteristics of the current control loop, to the optimal value according to the detected impedance equivalent value. Gain circuit 162 is one of the characteristic components of the present invention." *Id*., 7:62–8:4.

2. Indefiniteness

As detailed below, the Asserted Claims are indefinite under 35 U.S.C. § 112, ¶ 2 at least under Plaintiff's apparent constructions of the Asserted Claims. Claims are indefinite under 35 U.S.C. § 112, ¶ 2 when they "fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.,* 134 S. Ct. 2120, 2124 (2014).

Defendant notes that the Court's Docket Control Order contemplates that all indefiniteness issues be brought to the Court's attention through the *Markman* briefing process (*see* Dkt. No. 50 at 6 in the -084 case), which has not yet begun. Defendant's detailed arguments as to indefiniteness will be presented at that time, through the *Markman* meet and confer and briefing process.

Subject to Defendant's reservation of rights, and based on Defendant's present understanding of Bishop Display's Infringement Contentions, at least one or more of these claim terms/phrases/limitations are indefinite because they, read in light of the specifications and the prosecution histories, fail to inform with reasonable certainty those skilled in the art about the

scope of the invention, and are therefore invalid for indefiniteness under 35 U.S.C. § 112 ¶ 2. *See Nautilus, Inc. v. Biosig Instruments, Inc.,* 134 S. Ct. 2120 (2012). Although the question of whether a given claim term is indefinite may turn on claim construction positions (including claim construction positions advocated by Bishop Display), Defendant alleges that at least the following claims of the Asserted Patents, at least under Plaintiff's apparent constructions, are invalid because they include limitations and/or claim terms that fail to satisfy the definiteness requirement of 35 U.S.C. § 112 ¶ 2:

'798 Patent

- "each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes" (Claim 1)
- "at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode" (Claim 1)
- "common electrode" / "common electrodes" (Claim 1)
- "electrode pair" / "electrode pairs" (Claim 1)
- "adjacent" (Claim 1)
- "each of the pixels includes a plurality of electrode pairs, each electrode pair comprising one of the common electrodes and an adjacent one of the pixel electrodes" (Claim 1)
- "at least one of the electrode pairs differs from other electrode pairs in a thickness of its common electrode or a thickness of its pixel electrode" (Claim 1)

'829 Patent

- "a plurality of image signal lines located over the surface of the array substrate that is in contact with the liquid crystal layer, the image signal lines being aligned in a same direction" (Claims 1, 29)
- "a line-shaped pixel electrode located in each of pixel regions of the array substrate that is surrounded by the image signal lines and the scanning signal lines, the pixel electrode located parallel to the image signal lines or to the scanning signal lines" (Claims 1, 29)

- "a common electrode located in each of the pixel regions and located parallel to the pixel electrode" (Claims 1, 29)

- "wherein, of the pixel electrode and the common electrode, the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines comprises an opaque conductor, and at least one of the other electrodes comprises a transparent conductor" (Claims 1, 29)

- "common electrode" (Claims 1, 29)

- "the line shaped common electrode" (Claim 5)

- "line-shaped" (Claims 1, 5, 6, 29)

- "wherein, of the pixel electrode and the common electrode, the electrode that is located adjacent to and parallel to one of the image signal lines or one of the scanning signal lines comprises an opaque conductor, and at least one of the other electrodes comprises a transparent conductor" (Claim 1)

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- "a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates" (Claim 1)

- "a stripping step of stripping, by rubbing, a predetermined portion of the orientation film on the electrodes or lines once formed on the inner side of one or both of the substrates" (Claim 1)

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- "a capacitive accumulation portion formed by overlapping a pixel electrode, an insulating layer and a common electrode for each pixel area" (Claim 1)

- "a non-electrode area in a part of the pixel area which is not covered with a pixel electrode" (Claim 1)

- "wherein a peripheral shape of said capacitive accumulation portion on a side contacting said non-electrode area is substantially the same between respective pixels" (Claim 1)

- "a value of a storage capacity in said capacitive accumulation portion of one pixel at a signal feeding side is larger than that of an adjacent pixel at a termination side" (Claim 1)

- "wherein the value of the storage capacity in said capacitive accumulation portion of the one pixel is different from that of the adjacent pixel by varying an aperture in the

common electrode of the adjacent pixel with respect to the aperture of the one pixel" (Claim 1)

- "a capacitive accumulation portion formed by overlapping a pixel electrode, an insulating layer and a common electrode for each pixel area" (Claim 1)

- "a non-electrode area in a part of the pixel area which is not covered with a pixel electrode" (Claim 1)

- "wherein a peripheral shape of said capacitive accumulation portion on a side contacting said non-electrode area is substantially the same between respective pixels" (Claim 1)

- "a value of a storage capacity in said capacitive accumulation portion of one pixel at a signal feeding side is larger than that of an adjacent pixel at a termination side" (Claim 1)

- "wherein the value of the storage capacity in said capacitive accumulation portion of the one pixel is different from that of the adjacent pixel by varying an aperture in the common electrode of the adjacent pixel with respect to the aperture of the one pixel" (Claim 1)

'303 Patent

- "a common electrode being electrically connected to the common wiring and generating an electric field between the common electrode and the pixel electrode creating a voltage for driving the liquid crystal" (Claim 1)

- "wherein the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer" (Claim 1)

- "a storage capacity electrode electrically connected to the pixel electrode" (Claim 1)

- "common wiring" (Claim 1)

- "common electrode" (Claim 1)

- "a plurality of gate wirings and a plurality of source wirings intersecting each other" (Claim 1)

- "a switching element for switching a voltage applied to the pixel electrode from the source wiring based on a signal voltage fed from the gate wiring" (Claim 1)

- "wherein the pixel electrode and the storage capacity electrode are layered so as to hold at least some part of the common wiring in between through an insulating layer" (Claim 1).

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- “a first conductive member ... to which a negative voltage is applied, the first conductive member being gate signal lines” (Claim 1)

- “a first conductive member ... being in partial contact with the alignment layer ... the first conductive member being gate signal lines” (Claim 1)

- “a first conductive member which is formed on the first insulating substrate and interposed between the first insulating substrate and its corresponding alignment layer, being in partial contact with the alignment layer and to which a negative voltage is applied, the first conductive member being gate signal lines” (Claim 1)

- “wherein the first conductive member is formed so as to overlap with the light blocking layer in a plan view of the display” (Claim 5)

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- “[a] liquid crystal display of transversal electric field type” (Claim 7)

- “a plurality of scanning signal lines and a plurality of video signal lines formed so as to define a plurality of pixels in a matrix on an inner surface of one of the pair of substrates” (Claim 7)

- “a pixel electrode and a common electrode formed opposite to each other in each pixel in a plan view” (Claim 7)

- “an image is displayed on the liquid crystal panel by inputting a video signal from the video signal line into the pixel electrode while sequentially selecting the pixel through the scanning signal line” (Claim 7)

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- “an array substrate having an upper surface on which a common electrode, a pixel electrode, a scanning signal line, a video signal line, and a semiconductor switching device are formed” (Claim 1)

- “an opposing substrate disposed so as to be opposite to the upper surface of the array substrate” (Claim 1)

- “at least one electrode of the common electrode and the pixel electrode is constituted by an electrode portion and a wiring portion” (Claim 1)

- “the electrode portion is at least partially constituted by a transparent electric conductor” (Claim 1)

- “the electrode portion is formed in a layer separated by an insulating layer from a layer in which the scanning signal line is formed” (Claim 1)

- "the wiring portion is formed in the layer in which the scanning signal line is formed" (Claim 1)

'047 Patent

- "a first voltage supply source for supplying a first voltage . . . [and] a voltage holding circuit having a terminal being connected to a reference voltage different from the first voltage" (Claim 1)

E. Other Grounds of Invalidity

Defendant reserves the right to assert that the Asserted Claims are invalid under 35 U.S.C. §102(a), (b), (f) and/or (g) in the event Defendant obtains evidence (i) concerning prior art publications and systems through on-going discovery, including that which is subject to any third-party subpoenas, such as, for example, Panasonic Corporation (formerly, Matsushita Electric Industrial Co., Ltd.), Godo Kaisha IP Bridge 1, Parkside IP LLC, IP EDGE LLC, Lillian Woung, Gautham Bodepudi, Sanjay Pant, Hitachi, Sharp, Samsung Display, Sanyo Electric, Motorola, Fujitsu, Sony, Seiko Epson, or Citizen Watch; (ii) concerning any on-sale or public use bars, or any products or devices offered for sale or sold that render one or more of the Asserted Claims obvious; or (iii) that the named inventors of the patents-in-suit, did not invent (either alone or in conjunction with other parties) or first conceive of the subject matter claimed in the patents-in-suit. Should Defendant obtain such evidence of the latter, it will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived, and/or the circumstances surrounding the conception of the invention before the patent application.

Defendant reserves the right to supplement these disclosures based on further investigation and discovery.

III. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS—P.R. 3-4

Pursuant to P.R. 3-4 and the Docket Control Order (Dkt. No. 37 in the -310 case), and based on its investigation to date and understanding of Plaintiff's Infringement Contentions,

Defendant is producing, concurrently with these Invalidity Contentions, documents required by P.R. 3-4, including copies of prior art references required by P.R. 3-4(b). Defendant has produced herewith copies of each of the Asserted Patent IPRs. Plaintiff is already in possession of the Other Invalidity Contentions by virtue of these contentions having been served on Plaintiff in the context of litigation.

IV. OTHER PRIOR ART

In addition to the prior art references that Defendant has specifically discussed in these Invalidity Contentions, Defendant identifies each reference produced and cited in the accompanying document production of the same date. All of these references are relevant prior art, and Defendant reserves the right to rely on them based on its continuing research and analysis of the Asserted Claims, accused instrumentalities, and the prior art.

Further, Defendant contends that one or more claims of the patents-in-suit may be invalid due to derivation under 35 U.S.C. § 102(f). It is plain from the specifications and the prosecution histories that the named inventors "stood on the shoulders of others" at best and likely had access to numerous highly-pertinent prior art references in connection with their work and related documentation and communications.

Defendant further reserves the right to supplement these Invalidity Contentions once discovery into the original assignees, named inventors, and other third parties can take place, including as to the full scope of the named inventors.

In addition, until all prior art references available to the named inventors are identified or produced and they are deposed, it is impossible to know all aspects of what the named inventors learned from prior art sources (or from collaborations with others) and what they independently

contributed to the claimed subject matter. Defendant will supplement these Invalidity Contentions if and when more information becomes available.

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Defendants incorporate by reference, as if fully set forth herein, the Asserted Patent IPRs and Other Invalidity Contentions.

V. PRIOR ART INDEX

A. U.S. Patent No. 6,525,798

1. Patents & Published Patent Applications

U.S. Patent No. 6,525,798				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H07-128683 ("Fujii")	102(a) & (b)	Japan	November 4, 1993	May 19, 1995
U.S. Patent No. 6,337,726 ("Kawano")	102(e)	United States	February 23, 1999	January 8, 2002
WO (PCT) Patent Application Publication No. 98/47044 ("Ohta '044")	102(a) & (b)	World Intellectual Property Organization	April 1, 1998	October 22, 1998
WO (PCT) Patent Application Publication No. 98/27454 ("Ohta '454")	102(a) & (b)	World Intellectual Property Organization	December 18, 1996	June 25, 1998
Japanese Patent Application Publication No. H09-73101 ("Ohta '101")	102(a) & (b)	Japan	September 6, 1995	March 18, 1997
U.S. Patent No. 5,886,762 ("Lee")	102(a), (b) & (e)	United States	November 19, 1997	March 23, 1999
U.S. Patent No. 6,452,656 ("Niwano")	102(e)	United States	July 2, 1998	September 17, 2002

U.S. Patent No. 6,525,798				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H08-220518 (“Araya”)	102(a) & (b)	Japan	February 15, 1995	August 30, 1996
Japanese Patent Application Publication No. H09-80383 (“Kondo”)	102(a) & (b)	Japan	September 11, 1995	March 28, 1997
Japanese Patent Application Publication No. H09-90410 (“Ota”)	102(a) & (b)	Japan	September 20, 1995	April 4, 1997
Japanese Patent Application Publication No. H09-258242 (“Yamada”)	102(a) & (b)	Japan	March 18, 1996	October 3, 1997
Japanese Patent Application Publication No. H11-231344 (“Sunada”)	102(a) & (b)	Japan	February 18, 1998	August 27, 1999
Korean Patent Application Publication No. 101998-0083634 (“Kim”)	102(a) & (b)	Korea	May 16, 1997	December 5, 1998
U.S. Patent No. 5,754,266 (“Ohta ’266”)	102(a), (b) & (e)	United States	March 4, 1996	May 19, 1998
U.S. Patent No. 5,852,485 (“Shimada”)	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 5,907,379 (“Kim”)	102(a), (b) & (e)	United States	October 21, 1997	May 25, 1999
U.S. Patent No. 6,266,116 (“Ohta ’116”)	102(a), (b) & (e)	United States	September 26, 1996	July 24, 2001

U.S. Patent No. 6,525,798				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H11-119237 (“Niwano JP”)	102(a), (b)	Japan	October 16, 1997	April 30, 1999
U.S. Patent No. 6,208,399 (“Ohta ’399”)	102(e)	United States	October 8, 1999	March 27, 2001
JPH1130784 (“Aratani”)	102(a), (b) & (e)	Japan	July 11, 1997	February 2, 1999
JPH0829812A (“Satou”)	102(a), (b) & (e)	Japan	July 19, 1994	February 2, 1996
US6400440 (“Colgan”)	102(a), (b) & (e)	United States	June 23, 1999	June 4, 2002
US5434690 (“Hisatake”)	102(a), (b) & (e)	United States	July 26, 1994	July 18, 1995
US5745207 (“Asada”)	102(a), (b) & (e)	United States	November 27, 1996	April 28, 1998
US6288763 (“Hirota”)	102(a), (b) & (e)	United States	April 15, 1997	September 11, 2001
US6342937 (“Hiroshi”)	102(a), (b) & (e)	United States	January 24, 2001	January 29, 2001
JP2000206550	102(a)	Japan	January 13, 1999	July 28, 2000
JPH07-191336	102(a) & (b)	Japan	December 23, 1993	July 28, 1995
JPH07-199205	102(a) & (b)	Japan	December 28, 1993	August 4, 1995
JPH-07-234414	102(a) & (b)	Japan	July 25, 1994	September 5, 1995
JPH08-29812	102(a) & (b)	Japan	July 19, 1994	February 2, 1996
JPH08-262445	102(a) & (b)	Japan	March 23, 1995	October 11, 1996
JPH09-5764	102(a) & (b)	Japan	June 20, 1995	January 10, 1997
JPH09-105908	102(a) & (b)	Japan	October 9, 1995	April 22, 1997
JPH09-160061	102(a) & (b)	Japan	December 8, 1995	June 20, 1997
JPH09-258269	102(a) & (b)	Japan	March 27, 1996	October 3, 1997
JPH10-10556	102(a) & (b)	Japan	June 26, 1996	January 16, 1998
JPH10-68955	102(a) & (b)	Japan	August 29, 1996	March 10, 1998
JPH10-148826	102(a) & (b)	Japan	November 22, 1996	June 2, 1998
JPH10-186407	102(a) & (b)	Japan	October 29, 1997	July 14, 1998
JPH10-206866	102(a) & (b)	Japan	January 23, 1997	August 7, 1998
JPH11-2836	102(a) & (b)	Japan	June 10, 1997	January 6, 1999
JPH11-30784	102(a) & (b)	Japan	July 11, 1997	February 2, 1999
JPH11-119252	102(a) & (b)	Japan	October 16, 1997	April 30, 1999
US5434690	102(a), (b) & (e)	United States	July 26, 1994	February 1, 1995

U.S. Patent No. 6,525,798				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US5499123	102(a), (b) & (e)	United States	October 27, 1992	May 20, 1994
US5600464	102(a), (b) & (e)	United States	September 15, 1994	March 21, 1995
US5745207	102(a), (b) & (e)	United States	November 22, 1996	June 24, 1997
US5831701	102(a), (b) & (e)	United States	July 27, 1995	December 18, 1996
US5886762	102(a), (b) & (e)	United States	November 29, 1996	August 17, 1998
US5946066	102(a) & (e)	United States	June 27, 1997	January 15, 1999
US6078375	102(a) & (e)	United States	September 17, 1997	March 24, 1999
US6104450	102(a), (b) & (e)	United States	November 7, 1996	May 29, 1998
US6208399	102(a) & (e)	United States	April 1, 1998	October 22, 1998
US6256081	102(a) & (e)	United States	May 29, 1998	December 15, 1999
US6266116	102(a), (b) & (e)	United States	October 4, 1995	April 15, 1997
US6335770	102(a) & (e)	United States	July 17, 1998	December 27, 2001
US6452656	102(a) & (e)	United States	October 16, 1997	April 30, 1999
US6538713	102(a) & (e)	United States	April 16, 1999	November 2, 2000
US6583839	102(a) & (e)	United States	April 28, 1997	May 13, 1998
US6724452	102(a), (b) & (e)	United States	June 11, 1998	December 16, 1998
WO1998008134	102(a) & (b)	Japan	August 18, 1997	February 26, 1998

2. Publications

U.S. Patent No. 6,525,798			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of Liquid Crystal Displays	102(a)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999

B. U.S. Patent No. 6,787,829

1. Patents & Published Patent Applications

U.S. Patent No. 6,787,829				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,337,726 ("Kawano")	102(e)	United States	February 23, 1999	January 8, 2002
WO (PCT) Patent Application Publication No. 98/27454 ("Ohta '454")	102(a) & (b)	World Intellectual Property Organization	December 18, 1996	June 25, 1998

U.S. Patent No. 6,787,829				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,452,656 (“Niwano”)	102(e)	United States	July 2, 1998	September 17, 2002
U.S. Patent No. 6,222,599 (“Yoshida”)	102(e)	United States	March 31, 1999	April 24, 2001
U.S. Patent No. 5,995,187 (“Wakagi”)	102(a), (b) & (e)	United States	August 5, 1997	November 30, 1999
U.S. Patent No. 5,808,706 (“Bae”)	102(a), (b) & (e)	United States	March 19, 1997	September 15, 1998
Japanese Patent Application Publication No. H09-73101 (“Ohta ’101”)	102(a) & (b)	Japan	September 6, 1995	March 18, 1997
WO (PCT) Patent Application Publication No. 99/32924 (“Ohta ’924”)	102(a) & (b)	World Intellectual Property Organization	December 19, 1997	July 1, 1999
U.S. Patent No. 6,429,918 (“Choi”)	102(e)	United States	October 27, 1999	August 6, 2002
Korean Patent Application Publication No. 2000-0027768 (“Choi KR”)	102(a)	Korea	October 29, 1998	May 15, 2000
Korean Patent Application Publication No. 1999-0012988 (“Park”)	102(a) & (b)	Korea	July 31, 1997	February 25, 1999
Korean Patent Application Publication No. 1999-0085022 (“Bae KR”)	102(a) & (b)	Korea	May 13, 1998	December 6, 1999
Japanese Patent Application No. Publication No. H11-311808 (“Kawano JP”)	102(a) & (b)	Japan	February 9, 1999	November 9, 1999

U.S. Patent No. 6,787,829				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H11-119237 ("Niwano JP")	102(a) & (b)	Japan	October 16, 1997	April 30, 1999
Japanese Patent Application Publication No. P2000-081641 ("Yoshida JP")	102(a) & (b)	Japan	December 28, 1998	March 21, 2000
Japanese Patent Application Publication No. P2000-056324 ("Shiga")	102(a) & (b)	Japan	August 12, 1998	February 25, 2000
Japanese Patent Application Publication No. H08-50269 ("Kenmochi")	102(a) & (b)	Japan	August 5, 1994	February 20, 1996
Japanese Patent Application Publication No. H09-15650 ("Ota")	102(a) & (b)	Japan	January 25, 1996	January 17, 1997
U.S. Patent No. 5,852,485 ("Shimada")	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 6,028,653 ("Nishida")	102(a), (b) & (e)	United States	June 19, 1997	February 22, 2000
U.S. Patent No. 6,335,770 ("Komatsu")	102(e)	United States	July 17, 1998	January 1, 2002
U.S. Patent No. 6,476,783 ("Matthies")	102(e)	United States	February 16, 1999	November 5, 2002
U.S. Patent No. 5,969,782 ("Lee")	102(a), (b) & (e)	United States	June 24, 1998	October 19, 1999
U.S. Patent No. 6,081,308 ("Jeong")	102(e)	United States	February 26, 1998	June 27, 2000
U.S. Patent No. 6,531,392 ("Song")	102(e)	United States	October 15, 1999	March 11, 2003
US5907379 ("Kim")	102(a), (b) & (e)	United States	October 21, 1997	May 25, 1999

U.S. Patent No. 6,787,829				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US5723878 (“Yanai”)	102(a), (b) & (e)	United States	August 26, 1996	March 3,1998
US6532053 (“Ohta ’053”)	102(a), (b) & (e)	United States	December 18, 1996	March 11, 2003
JPH1174490 (“Jun”)	102(a) & (b)	Japan	October 16, 1997	July 2, 1999
JPH11352514 (“Yamada”)	102(a) & (b)	Japan	June 9, 1998	December 24, 1999
JP04104227 (“Matsui”)	102(a) & (b)	Japan	August 24, 1990	April 6, 1992
JP2000206550	102(a)	Japan	January 13, 1999	July 28, 2000
JP2001033814	102(a)	Japan	July 19, 1999	February 9, 2001
JPH07-128683	102(a) & (b)	Japan	November 4, 1993	May 19, 1995
JPH09-105908	102(a) & (b)	Japan	October 9, 1995	April 22, 1997
JPH09-258269	102(a) & (b)	Japan	March 27, 1996	October 3, 1997
JPH09-5764	102(a) & (b)	Japan	June 20, 1995	January 10, 1997
JPH10-10556	102(a) & (b)	Japan	June 26, 1996	January 16, 1998
JPH10-148826	102(a) & (b)	Japan	November 22, 1996	June 2, 1998
JPH10-186407	102(a) & (b)	Japan	October 29, 1997	July 14, 1998
JPH10-206866	102(a) & (b)	Japan	January 23, 1997	August 7, 1998
JPH11-119237	102(a) & (b)	Japan	October 16, 1997	April 30, 1999
JPH11-119252	102(a) & (b)	Japan	October 16, 1997	April 30, 1999
JPH11-2836	102(a) & (b)	Japan	June 10, 1997	January 6, 1999
JPH11-30784	102(a) & (b)	Japan	July 11, 1997	February 2, 1999
US5600464	102(a), (b) & (e)	United States	September 20, 1994	March 21, 1995
US5745207	102(a), (b) & (e)	United States	November 27, 1996	June 24, 1997
US5796448	102(a), (b) & (e)	United States	January 29, 1996	August 17, 1996
US5831701	102(a), (b) & (e)	United States	June 6, 1996	December 18, 1996
US5928733	102(a), (b) & (e)	United States	May 8, 1997	November 12, 1997
US5995187	102(a), (b) & (e)	United States	August 5, 1997	February 20, 1998
US6078375	102(a), (b) & (e)	United States	September 16, 1998	March 24, 1999
US6208399	102(a), (b) & (e)	United States	April 1, 1998	October 22, 1998
US6266116	102(a), (b) & (e)	United States	September 26, 1996	April 15, 1997
US6335770	102(a) & (e)	United States	July 17, 1998	December 27, 2001
US6337726	102(a) & (e)	United States	February 23, 1999	September 27, 1999
US6452656	102(a) & (e)	United States	July 2, 1998	April 30, 1999
US6512565	102(a) & (e)	United States	May 26, 1999	December 15, 1999

U.S. Patent No. 6,787,829				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US6538713	102(a) & (e)	United States	April 12, 2000	November 2, 2000
US6724452	102(a), (b) & (e)	United States	June 12, 1998	December 16, 1998
US6741310	102(a) & (e)	United States	November 12, 1999	May 26, 2000
WO1998008134	102(a) & (b)	Japan	August 18, 1997	February 26, 1998
WO1998027454	102(a) & (b)	Japan	December 18, 1996	June 25, 1998

2. Publications

U.S. Patent No. 6,787,829			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of Liquid Crystal Displays	102(a) & (b)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999
Optical properties of Al, Fe, Ti, Ta, W, and Mo at submillimeter wavelengths (Applied Optics, vol. 27 no. 6)	102(a) & (b)	Mark A. Ordal, Robert J. Bell, Ralph W. Alexander, Jr., Lawrence A. Newquist, and Marvin R. Querry (Optical Society of America)	March 15, 1988

C. U.S. Patent No. 6,801,293

1. Patents & Published Patent Applications

U.S. Patent No. 6,801,293				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H9-274190 ("Nishikawa 1997")	102(a) & (b)	Japan	April 3, 1996	October 21, 1997
U.S. Patent No. 5,949,509 ("Ohe")	102(a) & (e)	United States	May 8, 1998	September 7, 1999
Japanese Patent Application Publication No. H7-248478 ("Hideaki")	102(a) & (b)	Japan	March 14, 1994	September 26, 1995

U.S. Patent No. 6,801,293				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H11-109307 (“Toshihiro”)	102(a) & (b)	Japan	September 30, 1997	April 23, 1999
Japanese Patent Application Publication No. H11-305235 (“Satoru”)	102(a)	Japan	April 20, 1998	November 5, 1999
Korean Patent Application Publication No. 1998-020163 (“Choi”)	102(a) & (b)	Korea	September 5, 1996	June 25, 1998
U.S. Patent No. 4,693,562 (“Hasegawa”)	102(a), (b) & (e)	United States	December 6, 1985	September 15, 1987
Korean Patent Application Publication No. 2000-0021353 (“Lee”)	102(a)	Korea	September 28, 1998	April 25, 2000
Japanese Patent Application Publication No H10-148834 (“Minhara”)	102(a) & (b)	Japan	November 21, 1996	June 2, 1998
JPH07-168182	102(a) & (b)	Japan	December 16, 1993	July 4, 1995
JPH01-120531	102(a) & (b)	Japan	November 4, 1987	May 12, 1989
JPH01-120532	102(a) & (b)	Japan	November 4, 1987	May 12, 1989
JPH01-120533	102(a) & (b)	Japan	November 4, 1987	May 12, 1989
JPH01-210932	102(a) & (b)	Japan	February 18, 1988	August 24, 1989
JPH04-361233	102(a) & (b)	Japan	June 7, 1991	December 14, 1992
JPH05-142515	102(a) & (b)	Japan	November 18, 1991	June 11, 1993
JPH05-142542	102(a) & (b)	Japan	November 20, 1991	June 11, 1993
JPH05-142544	102(a) & (b)	Japan	November 22, 1991	June 11, 1993
JPH05-173143	102(a) & (b)	Japan	December 24, 1991	July 13, 1993
JPH05-75741U	102(a) & (b)	Japan	March 13, 1992	October 15, 1993

U.S. Patent No. 6,801,293				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
JPH05-88180	102(a) & (b)	Japan	September 30, 1991	April 9, 1993
JPH08-22023	102(a) & (b)	Japan	July 5, 1994	January 23, 1996
JPH09-203902	102(a) & (b)	Japan	January 25, 1996	August 5, 1997
JPH09-61822	102(a) & (b)	Japan	August 22, 1995	March 7, 1997
JPH09-96818A	102(a) & (b)	Japan	October 2, 1995	April 8, 1997
JPH10-148834	102(a) & (b)	Japan	November 21, 1996	June 2, 1998
JPH10-186391	102(a) & (b)	Japan	December 27, 1996	July 14, 1998
JPH10-213802	102(a) & (b)	Japan	January 29, 1997	August 11, 1998
JPH10-333150	102(a) & (b)	Japan	May 28, 1997	December 18, 1998
JPH10-96931	102(a) & (b)	Japan	September 24, 1996	April 14, 1998
JPH11-174462	102(a) & (b)	Japan	December 8, 1997	July 2, 1999
JPH11-202334	102(a) & (b)	Japan	January 20, 1998	July 30, 1999
JPS63-217323	102(a) & (b)	Japan	March 6, 1987	September 9, 1988
KR970004881	102(a) & (b)	Korea	July 26, 1996	January 29, 1997
US3967883	102(a), (b), & (e)	United States	May 22, 1975	July 6, 1976
US4232947	102(a), (b), & (e)	United States	July 1, 1975	January 16, 1976
US4247174	102(a), (b), & (e)	United States	May 31, 1979	December 13, 1979
US5042920	102(a), (b), & (e)	United States	November 9, 1989	May 16, 1990
US5128788	102(a), (b), & (e)	United States	September 26, 1990	April 3, 1991
US5305126	102(a), (b), & (e)	United States	November 26, 1991	June 3, 1992
US5416619	102(a), (b), & (e)	United States	December 17, 1992	June 29, 1993
US5438421	102(a), (b), & (e)	United States	February 28, 1994	August 1, 1995
US5504604	102(a), (b), & (e)	United States	August 9, 1994	April 2, 1996
US5552914	102(a), (b), & (e)	United States	May 26, 1995	February 25, 1994
US5559621	102(a), (b), & (e)	United States	July 20, 1994	January 25, 1995
US5627667	102(a), (b), & (e)	United States	May 25, 1995	July 30, 1994
US5657102	102(a), (b), & (e)	United States	January 28, 1994	July 30, 1994
US5694188	102(a), (b), & (e)	United States	September 14, 1995	November 29, 1996
US5712696	102(a), (b), & (e)	United States	February 13, 1995	August 23, 1995
US5725915	102(a), (b), & (e)	United States	September 21, 1995	April 12, 1996
US5739883	102(a), (b), & (e)	United States	August 30, 1996	April 14, 1998
US5786876	102(a), (b), & (e)	United States	June 24, 1994	September 21, 1995

U.S. Patent No. 6,801,293				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US5796458	102(a), (b), & (e)	United States	January 29, 1996	August 18, 1998
US5822031	102(a), (b), & (e)	United States	October 31, 1996	October 29, 1994
US5877836	102(a), (b), & (e)	United States	March 20, 1998	October 3, 1995
US5953091	102(a) &(e)	United States	April 9, 1998	September 14, 1999
US6081313	102(a), (b), & (e)	United States	March 29, 1996	May 28, 1997
US6128058	102(a), (b), & (e)	United States	May 21, 1998	July 16, 1997
US6154266	102(a) & (e)	United States	March 18, 1998	October 13, 1998
US6195140	102(a) & (e)	United States	July 27, 1998	February 25, 1999
US6233031	102(a), (b), & (e)	United States	February 20, 1998	August 26, 1998
US6266116	102(a), (b), & (e)	United States	September 26, 1996	April 15, 1997
US6266117	102(a), (b), & (e)	United States	September 9, 1996	March 20, 1997
US6266121	102(a), (b), & (e)	United States	November 24, 1997	January 28, 1998
US6313898	102(a) & (e)	United States	December 15, 1998	January 14, 2000
US6335775	102(a), (b), & (e)	United States	September 26, 1996	April 2, 1997
US6337728	102(a) & (e)	United States	October 8, 1998	April 30, 1999
US6341003	102(a) & (e)	United States	January 21, 1999	August 25, 1999
US6356329	102(a) & (e)	United States	January 27, 1999	February 2, 1999
US6362863	102(a) & (e)	United States	September 17, 1999	April 25, 2000
US6724452	102(a) & (e)	United States	June 12, 1998	December 16, 1998
US6781657	102(a), (b), & (e)	United States	March 30, 1998	July 1, 1998
US6839113	102(a) & (e)	United States	July 30, 1999	February 1, 2000

2. Publications

U.S. Patent No. 6,801,293			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of Liquid Crystal Displays	102(a)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999
Rubbed polyimide films studied by scanning force microscopy	102(a) & (b)	Y. B. Kim et al. (Applied Physics Letters)	April 24, 1995 (Publication accepted February 10, 1995)

Control of liquid crystal alignment by polyimide surface modification using atomic force microscopy	102(a) & (b)	A. J. Pidduck et al. (Applied Physics Letters)	November 17, 1997 (Publication accepted September 19, 1997)
Liquid crystal alignment by rubbed polymer surfaces	102(a) & (b)	Journal of Electron Spectroscopy and Related Phenomena	January 1, 1999

D. U.S. Patent No. 6,816,208

1. Patents & Published Patent Applications

U.S. Patent No. 6,816,208				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,028,650 ("Kuroha")	102(a), (b) & (e)	United States	July 18, 1997	February 22, 2000
U.S. Patent No. 6,020,214 ("Watanabe '214")	102(a), (b) & (e)	United States	July 16, 1998	February 1, 2000
Japanese Patent Application Publication No. H5-232509 ("Nishikawa 1993")	102(a) & (b)	Japan	February 21, 1992	September 10, 1993
Japanese Patent Application Publication No. H07-029535 ("Yamada 1995")	102(a) & (b)	Japan	July 31, 1989	June 2, 1995
Japanese Patent Application Publication No. JP2000-56322 ("Yamada 2000")	102(a) & (b)	Japan	August 7, 1998	February 25, 2000
Korean Patent Application Publication No. 2000-0003113 ("Yoo")	102(a) & (b)	Korea	June 25, 1998	January 15, 2000
U.S. Patent No. 5,459,596 ("Ueda")	102(a), (b) & (e)	United States	March 29, 1993	October 17, 1995
U.S. Patent No. 5,852,485 ("Shimada")	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998

U.S. Patent No. 6,816,208				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 5,886,762 (“Lee”)	102(a), (b) & (e)	United States	November 19, 1997	March 23, 1999
U.S. Patent No. 5,907,379 (“Kim”)	102(a), (b) & (e)	United States	October 21, 1997	May 25, 1999
U.S. Patent No. 5,926,244 (“Takeda”)	102(a), (b) & (e)	United States	July 17, 1997	July 20, 1999
U.S. Patent No. 6,001,277 (“Ichimura”)	102(a), (b) & (e)	United States	(PCT Date) May 25, 1996 (371 Date) July 16, 1998	December 14, 1999
U.S. Patent No. 6,028,653 (“Nishida”)	102(a), (b) & (e)	United States	June 19, 1997	February 22, 2000
U.S. Patent No. 6,249,325 (“Ohkawara”)	102(a) & (e)	United States	July 10, 1998	June 19, 2001
U.S. Patent No. 5,724,112 (“Yoshida ’112")	102(a), (b) & (e)	United States	June 16, 1995	March 3, 1998
Japanese Patent Application Publication No. H11-271791 (“Katsusato”)	102(a) & (b)	Japan	March 26, 1998	October 8, 1999
Japanese Patent Application Publication No. JP2000-056322 (“Kenichiro”)	102(a) & (b)	Japan	August 7, 1998	February 25, 2000
Korean Patent Application Publication No. 1999-0052414 (“Lee”)	102(a) & (b)	Korea	December 22, 1997	July 5, 1999
Korean Patent Application Publication No. 2000-0014694 (“Son”)	102(a) & (b)	Korea	August 24, 1998	March 15, 2000
U.S. Patent No. 6,760,081 (“Takagi”)	102(e)	United States	May 23, 2000	July 6, 2004
Japanese Patent Application Publication No. H05-297412 (“Yasumitsu”)	102(a) & (b)	Japan	April 22, 1992	November 12, 1993
JP2000056322A	102(a) & (b)	Japan	August 7, 1998	February 25, 2000

U.S. Patent No. 6,816,208				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
JP2000155343A	102(a) & (b)	Japan	December 28, 1999	June 6, 2000
JPH1-1311808	102(a) & (b)	Japan	February 9, 1999	April 4, 2000
JP3029426	102(a) & (b)	Japan	February 9, 1999	November 9, 1999
KR1019970048779	102(a) & (b)	Korea	December 30, 1995	July 29, 1997
US5459596	102(a), (b), & (e)	United States	March 29, 1993	August 13, 1993
US5517342	102(a), (b), & (e)	United States	March 4, 1994	April 20, 1994
US5880798	102(a), (b), & (e)	United States	June 24, 1997	August 28, 1996
US6249325	102(a), (b), & (e)	United States	July 10, 1998	February 25, 1999
US6690031	102(a) & (e)	United States	April 20, 1999	November 9, 1999
US6771342	102(a), (b), & (e)	United States	March 4, 1997	October 13, 1997
US6809787	102(e)	United States	February 24, 1999	May 8, 2003

2. Publications

U.S. Patent No. 6,816,208			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of Liquid Crystal Displays	102(a) & (b)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999
Active-Matrix Thin- Film Transistor Liquid-Crystal Displays (Advances in Electronics and Electron Physics Vol. 77)	102(a) & (b)	Shinji Morozumi; edited by Peter W. Hawkes (Academic Press, Inc.)	1990
Flat Panel Displays Using Amorphous and Microcrystalline Semiconductor Devices (Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices)	102(a) & (b)	Kouji Suzuki; edited by Jerzy Kanicki (Artech House, Inc.)	1991
Liquid Crystal Displays Using Nematic Liquid Crystals (Flat Panel Displays)	102(a)	S. M. Kelly (The Royal Society of Chemistry)	2000
Microelectronics in Active-Matrix LCDs and Image Sensors (Electro-Optical Displays)	102(a) & (b)	William den Boer et al.; edited by Mohammad A. Karim (Marcel Dekker, Inc.)	1992

Fundamentals of Active-Matrix Liquid- Crystal Displays	102(a) & (b)	Sang Soo Kim (Society for Information Display)	May 14, 2000
An Amorphous-Si TFT Addressed 3. 2-in. Full-Color LCD (SID International Symposium Digest of Technical Papers)	102(a) & (b)	F. Funada et al. (Society for Information Display)	May 1986
Active-Matrix-Addressed Color LCDs for Avionics Application (SID International Symposium Digest of Technical Papers)	102(a) & (b)	Kazuhisa Katoh et al. (Society for Information Display)	May 1988
A Novel Backlighting Unit with Ultra-High Luminance for Monitor Applications (SID International Symposium Digest of Technical Papers)	102(a) & (b)	H. Sasaki et al. (Society for Information Display)	May 1999
A Late-News Paper: A Novel Protective Diffuser for Backlit LCDs (SID International Symposium Digest of Technical Papers)	102(a) & (b)	Masakazu Uekita et al. (Society for Information Display)	May 2000

E. U.S. Patent No. 6,850,303

1. Patents & Published Patent Applications

U.S. Patent No. 6,850,303				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H09-236820 (“Nakagawa”)	102(a) & (b)	Japan	February 29, 1996	September 9, 1997
Japanese Patent Application Publication No. P2000-98420 (“Iizuka”)	102(a) & (b)	Japan	September 22, 1998	April 7, 2000

U.S. Patent No. 6,850,303				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,812,975 (“Nagahiro”)	102(e)	United States	April 18, 2000	November 2, 2004
U.S. Patent No. 5,852,485 (“Shimada”)	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 5,734,449 (“Jang”)	102(a), (b) & (e)	United States	June 13, 1995	March 31, 1998
U.S. Patent No. 5,182,661 (“Ikeda”)	102(a), (b) & (e)	United States	June 25, 1991	January 26, 1993
U.S. Patent No. 6,292,245 (“Lee”)	102(e)	United States	November 24, 1998	September 18, 2001
U.S. Patent No. 6,335,770 (“Komatsu 770”)	102(e)	United States	July 17, 1998	January 1, 2002
U.S. Patent No. 6,259,502 (“Komatsu 502”)	102(e)	United States	July 10, 1998	July 10, 2001
U.S. Patent No. 6,281,957 (“Oh”)	102(e)	United States	May 15, 1998	August 28, 2001
U.S. Patent No. 5,734,451 (“Yanagawa 451”)	102(a), (b) & (e)	United States	December 3, 1996	March 31, 1998
U.S. Patent No. 6,049,369 (“Yanagawa 369”)	102(a), (b) & (e)	United States	September 9, 1996	April 11, 2000
Japanese Patent Application Publication No. P2000-155337 (“Yanagawa 337”)	102(a) & (b)	Japan	November 24, 1998	June 6, 2000
Japanese Patent Application Publication No. H05-2189 (“Ogawa”)	102(a) & (b)	Japan	June 26, 1991	January 8, 1993
Japanese Patent Application Publication No. H07-72506 (“Teruhira”)	102(a) & (b)	Japan	June 14, 1993	March 17, 1995
Japanese Patent Application Publication No. H09-101543 (“Nakazato”)	102(a) & (b)	Japan	October 5, 1995	April 15, 1997

U.S. Patent No. 6,850,303				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H10-39328 ("Kuroba")	102(a) & (b)	Japan	July 19, 1996	February 13, 1998
Japanese Patent Application Publication No. H09-230380 ("Shimada 380")	102(a) & (b)	Japan	February 27, 1996	September 5, 1997
Japanese Patent Application Publication No. H11-271804 ("Onozuka")	102(a) & (b)	Japan	March 20, 1998	October 8, 1999
Japanese Patent No. JP3096394 ("Fujiwara")	102(a)	Japan	December 27, 1994	October 10, 2000
JPH08-179375	102(a) & (b)	Japan	December 27, 1994	July 12, 1996
JPH11-2836	102(a) & (b)	Japan	June 10, 1997	January 6, 1999
JPH05-216067	102(a) & (b)	Japan	February 4, 1992	August 27, 1993
JPH07-72506	102(a) & (b)	Japan	June 14, 1993	March 17, 1995
JPH08-234239	102(a) & (b)	Japan	February 28, 1995	September 13, 1996
JPH09-22024	102(a) & (b)	Japan	July 7, 1995	January 21, 1997
JPH09-26601	102(a) & (b)	Japan	July 13, 1995	January 28, 1997
JPH11-119237	102(a) & (b)	Japan	October 16, 1997	April 30, 1999
JPH11-24107	102(a) & (b)	Japan	July 7, 1997	January 29, 1999
JPS57-20778	102(a) & (b)	Japan	July 11, 1980	February 3, 1982
JPS62-36687	102(a) & (b)	Japan	August 12, 1985	February 17, 1987
US20010046018	102(a) &(e)	United States	August 14, 1998	November 29, 2001
US4983022	102(a), (b), & (e)	United States	March 29, 1988	May 20, 1987
US5182661	102(a), (b), & (e)	United States	June 25, 1991	January 8, 1992
US5321535	102(a), (b), & (e)	United States	May 27, 1993	January 29, 1992
US5598285	102(a), (b), & (e)	United States	September 20, 1993	March 23, 1994
US5644370	102(a), (b), & (e)	United States	July 5, 1996	August 4, 1993
US5659375	102(a), (b), & (e)	United States	June 2, 1995	January 4, 1996
US5734449	102(a), (b), & (e)	United States	June 13, 1995	January 25, 1996
US5745207	102(a), (b), & (e)	United States	November 27, 1996	June 24, 1997
US5754266	102(a), (b), & (e)	United States	March 4, 1996	September 18, 1996
US5760856	102(a), (b), & (e)	United States	August 16, 1996	March 28, 1997
US5774099	102(a), (b), & (e)	United States	April 10, 1996	November 12, 1996

U.S. Patent No. 6,850,303				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US5781261	102(a), (b), & (e)	United States	July 8, 1996	February 7, 1997
US5786876	102(a), (b), & (e)	United States	June 24, 1994	September 21, 1995
US5905556	102(a), (b), & (e)	United States	July 11, 1997	January 27, 1998
US5917563	102(a), (b), & (e)	United States	September 13, 1996	June 20, 1997
US5926161	102(a), (b), & (e)	United States	February 1, 1996	August 20, 1996
US5942310	102(a), (b), & (e)	United States	September 11, 1996	April 28, 1997
US5956103	102(a), (b), & (e)	United States	June 17, 1997	January 16, 1998
US5982460	102(a), (b), & (e)	United States	June 24, 1997	January 16, 1998
US5986735	102(a), (b), & (e)	United States	September 22, 1997	July 6, 1998
US5995187	102(a), (b), & (e)	United States	August 5, 1997	February 20, 1998
US6049365	102(a) &(e)	United States	November 27, 1998	April 11, 2000
US6088071	102(a), (b), & (e)	United States	February 19, 1998	September 11, 1998
US6091473	102(a), (b), & (e)	United States	May 21, 1998	December 4, 1998
US6108066	102(a), (b), & (e)	United States	January 12, 2000	April 22, 1997
US6111626	102(a), (b), & (e)	United States	October 9, 1998	April 30, 1999
US6127998	102(a), (b), & (e)	United States	October 17, 1997	April 22, 1998
US6181398	102(a) &(e)	United States	September 3, 1998	March 31, 2000
US6184961	102(a) &(e)	United States	July 7, 1998	February 6, 2001
US6271903	102(a), (b), & (e)	United States	January 22, 1998	July 29, 1998
US6281957	102(a), (b), & (e)	United States	May 15, 1998	December 5, 1998
US6335770	102(a) &(e)	United States	July 17, 1998	December 27, 2001
US6337728	102(a), (b), & (e)	United States	October 8, 1998	April 30, 1999
US6445435	102(a), (b), & (e)	United States	January 21, 1999	August 16, 1999
US6493046	102(a) &(e)	United States	June 27, 2000	January 19, 2001
US6529256	102(a), (b), & (e)	United States	August 25, 2000	December 5, 1998
US6556265	102(a), (b), & (e)	United States	March 19, 1999	September 23, 1999
US6583828	102(a) &(e)	United States	August 21, 2000	March 15, 2001
US6697136	102(a) &(e)	United States	September 26, 2000	April 16, 2001
US6771342	102(a), (b), & (e)	United States	March 4, 1997	October 13, 1997
US6784979	102(a) &(e)	United States	May 22, 2003	December 25, 2003
US6812975	102(a) &(e)	United States	April 18, 2000	November 30, 2000
US6812985	102(a) &(e)	United States	March 28, 2000	November 2, 2004
US6856360	102(a), (b), & (e)	United States	November 24, 1998	June 18, 1999
US7192865	102(a), (b), & (e)	United States	April 17, 2000	June 18, 1999

U.S. Patent No. 6,850,303				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
US7202497	102(a), (b), & (e)	United States	November 23, 1998	June 18, 1999
WO1998027454	102(a) & (b)	Japan	December 18, 1996	June 25, 1998
US 6,335,770	102(a), (b), & (e)	United States	July 7, 1998	January 1, 2002
EP 1,037,093	102(a) & (b)	Europe	November 30, 1998	September 20, 2000
US 6,590,227	102(a), (b), & (e)	United States	December 27, 2000	June 28, 2001
KR0144233	102(a) & (b)	Korea	June 29, 1995	January 24, 1997
KR2000-0009305	102(a) & (b)	Korea	July 23, 1998	February 15, 2000
US5734448	102(a), (b), & (e)	United States	February 18, 1997	March 31, 1998
US5923390	102(a), (b), & (e)	United States	June 25, 1998	July 13, 1999
US6326641	102(a) &(e)	United States	November 24, 1999	December 4, 2001
US 2003/0071930 Al	102(a) &(e)	United States	April 18, 2000	April 17, 2003

2. Publications

U.S. Patent No. 6,850,303			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of Liquid Crystal Displays	102(a) & (b)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999

F. U.S. Patent No. 6,906,769

1. Patents & Published Patent Applications

U.S. Patent No. 6,906,769				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,335,770 (“Komatsu”)	102(e)	United States	July 17, 1998	Jan. 1, 2002
U.S. Patent No. 6,069,678 (SakamotoUS678)	102(a) & (e)	United States	October 29, 1997	May 30, 2000
Japanese Patent Application Publication No. H10-186407 (“SakamotoJP407”)	102(a) & (b)	Japan	October 29, 1997	July 14, 1998

U.S. Patent No. 6,906,769				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H9-96794 ("Watanabe JP '794")	102(a) & (b)	Japan	September 28, 1995	April 8, 1997
Japanese Patent Application Publication No. H8-95075 ("Shimada")	102(a) & (b)	Japan	September 26, 1994	April 12, 1996
U.S. Patent No. 4,909,602 ("Kaneko")	102(a), (b) & (e)	United States	April 19, 1988	March 20, 1990
Japanese Patent Application Publication No. H10-123526 ("Tanuma")	102(a) & (b)	Japan	October 24, 1996	May 15, 1998
Japanese Patent Application Publication No. H03-137619 ("Fukami")	102(a) & (b)	Japan	October 23, 1989	June 12, 1991
Japanese Patent Application Publication No. H06-202127 ("OtaJP127")	102(a) & (b)	Japan	December 28, 1992	July 22, 1994
U.S. Patent No. 5,398,043 ("Takeda")	102(a), (b) & (e)	United States	October 8, 1992	March 14, 1995
U.S. Patent No. 6,005,542 ("Yoon")	102(a), (b) & (e)	United States	October 31, 1996	December 21, 1999
Japanese Patent Publication No. 2000-267082 ("Takaomi JP '082")	102(a)	Japan	March 18, 1999	September 29, 2000
U.S. Patent No. 5,852,485 ("Shimada")	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 5,928,733	102(a), (b) & (e)	United States	May 8, 1997	July 27, 1999
U.S. Patent No. 5,990,987 ("Tanaka")	102(a), (b) & (e)	United States	November 17, 1998	November 23, 1999
U.S. Patent No. 6,005,543 ("Kimura")	102(a), (b) & (e)	United States	February 13, 1998	December 21, 1999
U.S. Patent No. 6,208,399 ("Ohta")	102(a) & (e)	United States	April 1, 1998	March 27, 2001

U.S. Patent No. 6,906,769				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,233,034	102(a) & (e)	United States	May 29, 1998	May 15, 2001
U.S. Patent No. 6,271,903 ("Shin")	102(a) & (e)	United States	January 22, 1998	August 7, 2001
U.S. Patent No. 6,281,957 ("Oh")	102(a) & (e)	United States	May 15, 1998	August 28, 2001
U.S. Patent No. 6,346,932 ("Maeda")	102(a) & (e)	United States	March 13, 1997	February 12, 2002
U.S. Patent No. 6,429,918 ("Choi")	102(e)	United States	October 27, 1999	August 6, 2002
U.S. Patent No. 6,445,435 ("Seo")	102(e)	United States	January, 1999	September 3, 2002
U.S. Patent No. 6,704,083 ("Kim")	102(e)	United States	November 17, 1997	March 9, 2004
U.S. Patent No. 6,781,657	102(e)	United States	March 30, 1997	August 24, 2004
U.S. Patent No. 7,561,238 ("Sakamoto")	102(e)	United States	July 29, 1999	July 14, 2009
U.S. Patent Application Publication No. US 2001/0011981 ("Yamamoto")	102(e)	United States	December 24, 1997	August 9, 2001
U.S. Patent No. 6,690,445 ("Matsumoto")	102(e)	United States	April 20, 2001	February 10, 2004
Japanese Patent Publication No. 2000-267113 ("Takaomi JP '113")	102(a)	Japan	March 18, 1999	September 29, 2000
Japanese Patent Application Publication No. H08-095078 ("Shimada JP '078")	102(a) & (b)	Japan	September 26, 1994	April 12, 1996
Japanese Patent Application Publication No. H08-082805 ("Shimada JP '805")	102(a) & (b)	Japan	September 9, 1994	March 26, 1996
U.S. Patent No. 6,704,084 ("Kodate")	102(e)	United States	March 9, 2001	March 9, 2004

U.S. Patent No. 6,906,769				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 5,359,206 (Yamamoto)	102(a), (b) & (e)	United States	(PCT Date) August 13, 1990 (371 Date) April 15, 1991	October 25, 1994
Japanese Patent Publication No. 2001-188233 ("Jun")	102(a)	Japan	December 27, 1999	July 10, 2001
Japanese Patent Application Publication No. H09-236822 ("Junji")	102(a) & (b)	Japan	March 1, 1996	September 9, 1997
JPH10-133205	102(a) & (b)	Japan	November 5, 1996	May 22, 1998
JPH10-186391	102(a) & (b)	Japan	December 27, 1996	July 14, 1998
JPH11-174493	102(a) & (b)	Japan	December 17,1997	July 2, 1999
EP1008896A1	102(a)	Europe	April 1, 1998	September 14, 2000
JPH10-96950	102(a) & (b)	Japan	September 20, 1996	April 14, 1998
JPH10-123526	102(a) & (b)	Japan	October 24, 1996	May 15, 1998
JP10-133205	102(a) & (b)	Japan	November 5, 1996	May 22, 1998
JP10-170923	102(a) & (b)	Japan	May 8, 1997	June 26, 1998
US5928733	102(a), (b), & (e)	United States	May 8, 1997	July 27, 1999
JP10-186391	102(a) & (b)	Japan	December 27, 1996	July 14, 1998
JP11-024068	102(a) & (b)	Japan	March 30, 1998	January 29, 1999
US6781657	102(e)	United States	March 30, 1998	August 24, 2004
JP11-174493	102(a) & (b)	Japan	December 17, 1997	July 2, 1999
JP11-202356	102(a) & (b)	Japan	May 29, 1998	July 30, 1999
US6233034	102(a) & (e)	United States	May 29, 1998	May 15, 2001
JP1989086113A	102(a) & (b)	Japan	September 29, 1987	March 30, 1989
JP1990039029A	102(a) & (b)	Japan	July 28, 1988	February 8, 1990
JP1992242223A	102(a) & (b)	Japan	January 16, 1991	August 28, 1992
JP1994012387B	102(a) & (b)	Japan	December 17, 1985	February 16, 1994
JP1997113930	102(a) & (b)	Japan	October 16, 1996	May 2, 1997
JP1997325363A	102(a) & (b)	Japan	June 5, 1997	December 16, 1997
JP1999038444A	102(a) & (b)	Japan	July 18, 1997	February 12, 1999

U.S. Patent No. 6,906,769				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
JP1999109321A	102(a) & (b)	Japan	October 2, 1997	April 23, 1999
JPH10186407A	102(a) & (b)	Japan	October 29, 1997	July 14, 1998
US6069678	102(a), (b), & (e)	United States	October 29, 1997	May 30, 2000
JPH8-95075	102(a) & (b)	Japan	September 26, 1994	April 12, 1996
JPH9-96794	102(a) & (b)	Japan	September 28, 1995	April 8, 1997
KR1019970004144	102(a) & (b)	Korea	February 12, 1997	October 15, 1998
KR1019970053872	102(a) & (b)	Korea	October 21, 1997	May 15, 1999
KR1019970066154	102(a) & (b)	Korea	December 5, 1997	July 5, 1999
KR1019980034015	102(a) & (b)	Korea	August 21, 1998	March 15, 2000
KR1019980035143	102(a) & (b)	Korea	August 28, 1998	March 15, 2000
US20010011981	102(a)	Korea	April 16, 2001	August 9, 2001
US3647280	102(a), (b), & (e)	United States	November 6, 1969	May 19, 1971
US3703329	102(a), (b), & (e)	United States	December 29, 1969	July 8, 1971
US4644338	102(a), (b), & (e)	United States	July 1, 1983	August 10, 1983
US4909602	102(a), (b), & (e)	United States	April 19, 1988	October 26, 1988
US5431773	102(a), (b), & (e)	United States	December 17, 1992	June 23, 1993
US5793460	102(a), (b), & (e)	United States	August 22, 1996	March 29, 1997
US5835177	102(a), (b), & (e)	United States	October 4, 1996	May 30, 1997
US5852485	102(a), (b), & (e)	United States	February 26, 1997	September 5, 1997
US5990987	102(a), (b), & (e)	United States	November 17, 1998	June 2, 1999
US6069678	102(a), (b), & (e)	United States	October 29, 1997	July 14, 1998
US6208399	102(a), (b), & (e)	United States	April 1, 1998	October 22, 1998
US6271903	102(a), (b), & (e)	United States	January 22, 1998	July 29, 1998
US6281957	102(a), (b), & (e)	United States	May 15, 1998	December 5, 1998
US6335770	102(a) & (e)	United States	July 17, 1998	December 27, 2001
US6346932	102(a), (b), & (e)	United States	March 13, 1997	September 18, 1997
US6429918	102(a) & (e)	United States	October 27, 1999	May 15, 2000
US6445435	102(a), (b), & (e)	United States	January 21, 1999	August 16, 1999
US6704083	102(e)	United States	November 17, 1997	March 9, 2004
US7561238	102(a), (b), & (e)	United States	April 13, 2007	March 25, 2000

2. Publications

U.S. Patent No. 6,906,769			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
"Electronics Circuits and Devices"	102(a) & (b)	Ralph J. Smith (John Wiley and Sons, Inc.)	January 1, 1980
"Compensative Addressing for Switching Distortion in a-Si TFTLCD"	102(a) & (b)	Suzuki, Toshiba R&D Center, Eurodisplay '87, Proceedings of the Conference, The Institute of Physics and The Society for Information Display.	September 15–17, 1987
"Amorphous Silicon Shows Promise for Flat-Panel T.V. Display"	102(a) & (b)	Smith, The International Magazine of Electronics Technology, vol. 52, No. 13	June 21, 1979
"Compensation of the Display Electrode Voltage Distortion"	102(a) & (b)	Yanagisawa et al., Toshiba Corp. Electron Device Engineering Laboratory, Proceedings of the SID, vol. 29, No. 1	1988
"A 220 x 240 Pixel a- Si TFT Matrix Transmission LCD"	102(a) & (b)	Suzuki et al., Toshiba Corp. R&D Center, Proceedings of the Society for Information Display, vol. 25, No. 1	June 19, 1984
"A New Address Scheme to Improve the Display Quality of a-Si TFT/LCD Panels	102(a) & (b)	Kaneko et al., IEEE Transactions on Electron Devices, vol. 36, No. 12	December 1989
"Analysis of Liquid Crystal Orientation at Interface between Liquid Crystal and Alignment Film by Total Reflection Ellipsometry"	102(a) & (b)	Okutani et al., Jpn. J. Appl. Phys. Vol. 37 (1998) pp. L600–L602 Part 2, No. 5B	May 1998
"Advantageous voltage-holding ratio characteristics induced by in-plane electric® elds, and the optimization concept of liquid crystals for an in-plane switching electro-optical effect"	102(a) & (b)	Oh-e et al., Liquid Crystals, 1998, Vol. 25, No. 6, 699-709	1998

U.S. Patent No. 6,906,769			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
"Super High Quality MVA-TFT Liquid Crystal Displays"	102(a) & (b)	Koike et al., FUJITSU Sci. Tech. J., 35, 2, pp.221-228	December 1999
"Wide Viewing Angle Technologies of TFT-LCDs"	102(a) & (b)	Koden, Ecological Technology Development Center Corporate Research and Development Group	1999
"Comb-on-plane switching electrodes for liquid-crystal displays"	102(a) & (b)	Journal of the SID, Vol. 8, Issue 2, pp.139-145	June 2000

G. U.S. Patent No. 7,414,682

1. Patents & Published Patent Applications

U.S. Patent No. 7,414,682				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. H09-269508 ("Matsumoto")	102(a) & (b)	Japan	March 29, 1996	October 14, 1997
WO (PCT) Patent Application Publication No. 98/27454 ("Ohta '454")	102(a) & (b)	World Intellectual Property Organization	December 18, 1996	June 25, 1998
Japanese Patent Application Publication No. 2000-98404 ("Kubota")	102(a) & (b)	Japan	September 28, 1998	April 7, 2000
U.S. Patent No. 5,907,379 ("Kim")	102(a), (b) & (e)	United States	October 21, 1997	May 25, 1999
Japanese Patent Application Publication No. H10-301141 ("Asada")	102(a) & (b)	Japan	April 25, 1997	November 13, 1998
Japanese Patent Application Publication No. 2001-092379	102(a)	Japan	September 27, 1999	April 6, 2001

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U.S. Patent No. 7,414,682				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Japanese Patent Application Publication No. 2001-142056	102(a)	Japan	November 10, 1999	May 25, 2001
Japanese Patent Application Publication No. H7-036058	102(a) & (b)	Japan	July 20, 1993	February 7, 1995
Japanese Patent Application Publication No. H7-239480	102(a) & (b)	Japan	March 1, 1994	September 12, 1995
Japanese Patent Application Publication No. H11-024095	102(a) & (b)	Japan	July 2, 1997	January 29, 1999
Japanese Patent Application Publication No. 2000-047202	102(a) & (b)	Japan	July 31, 1998	February 18, 2000
Japanese Patent Application Publication No. 2000-206550	102(a) & (b)	Japan	January 13, 1999	July 28, 2000
Japanese Patent Application Publication No. 2000-250059	102(a)	Japan	March 2, 1999	September 14, 2000
Japanese Patent Application Publication No. 2001-091974	102(a)	Japan	July 19, 1999	April 6, 2001
Korean Patent Application Publication No. 2000-032042	102(a) & (b)	Korea	November 12, 1998	June 5, 2000
U.S. Patent No. 5,400,157	102(a), (b) & (e)	United States	November 17, 1993	March 21, 1995
U.S. Patent No. 5,995,187	102(a), (b) & (e)	United States	August 5, 1997	November 30, 1999
U.S. Patent No. 6,067,067	102(a), (b) & (e)	United States	December 23, 1997	May 23, 2000

U.S. Patent No. 7,414,682				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 6,091,393	102(a), (b) & (e)	United States	December 23, 1997	July 18, 2000
U.S. Patent No. 6,108,064	102(a), & (e)	United States	November 6, 1998	August 22, 2000
U.S. Patent No. 6,128,061	102(a), & (e)	United States	December 8, 1998	October 3, 2000
U.S. Patent No. 6,262,784	102(a), & (e)	United States	June 30, 1997	July 17, 2001
U.S. Patent No. 6,392,627	102(e)	United States	February 22, 1999	May 21, 2002
U.S. Patent No. 6,512,565	102(e)	United States	May 26, 1999	January 28, 2003
U.S. Patent No. 6,642,984	102(e)	United States	December 7, 1999	November 4, 2003
U.S. Patent No. 6,677,925	102(e)	United States	September 6, 2000	January 13, 2004
U.S. Patent No. 4,345,249	102(a), (b) & (e)	United States	December 12, 1980	August 17, 1982
U.S. Patent No. 5,598,285	102(a), (b) & (e)	United States	September 20, 1993	January 28, 1997
U.S. Patent No. 5,600,464	102(a), (b) & (e)	United States	September 20, 1994	February 4, 1997
U.S. Patent No. 5,734,451	102(a), (b) & (e)	United States	December 3, 1996	March 31, 1998
U.S. Patent No. 5,754,266	102(a), (b) & (e)	United States	March 4, 1996	May 19, 1998
U.S. Patent No. 5,786,876	102(a), (b) & (e)	United States	(PCT Date) June 24, 1994 (371 Date) January 13, 1995	July 28, 1998
U.S. Patent No. 5,831,707	102(a), (b) & (e)	United States	August 24, 1995	November 3, 1998
U.S. Patent No. 5,852,485	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 6,014,190	102(a), (b) & (e)	United States	December 2, 1996	January 11, 2000
U.S. Patent No. 6,049,369	102(a), (b) & (e)	United States	September 9, 1996	April 11, 2000
U.K. Patent Application Publication No. 2,332,769	102(a) & (b)	United Kingdom	May 29, 1998	June 30, 1999

U.S. Patent No. 7,414,682				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
European Patent Application Publication No. 0588568A2	102(a) & (b)	Europe	September 10, 1993	March 23, 1994
European Patent Application Publication No. 0673986A2	102(a) & (b)	Europe	March 17, 1995	September 27, 1995
European Patent Application Publication No. 0732612A1	102(a) & (b)	Europe	March 15, 1996	September 18, 1996
U.S. Patent No. 6,452,656 ("Niwano")	102(e)	United States	July 2, 1998	September 17, 2002
U.S. Patent No. 5,969,782 ("Seung Hee Lee")	102(a), (b) & (e)	United States	June 24, 1998	October 19, 1999
WO (PCT) Patent Application Publication No. WO1999045430A1 ("Ota")	102(a) & (b)	Japan	June 30, 1998	September 10, 1999
Yamaji JPH07199169A	102(a) & (b)	Japan	December 28, 1993	August 4, 1995
U.S. Patent No. 6,563,561 ("Ota561")	102(a) & (e)	United States	February 9, 2000	May 13, 2003
U.S. Patent No. 5,852,485 ("Shimada")	102(a), (b) & (e)	United States	February 26, 1997	September 5, 1997
JPH09-269508	102(a) & (b)	Japan	March 29, 1996	October 14, 1997
US5852485	102(a), (b) & (e)	United States	February 26, 1997	September 5, 1997
US5995187	102(a), (b) & (e)	United States	August 5, 1997	February 20, 1998
WO98/27454	102(a) & (b)	Japan	December 18, 1996	June 25, 1998

2. Publications

U.S. Patent No. 7,414,682			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of liquid crystal displays	102(a) & (b)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999

U.S. Patent No. 7,414,682			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Active-Matrix Thin- Film Transistor Liquid-Crystal Displays (Advances in Electronics and Electron Physics Vol. 77)	102(a) & (b)	Shinji Morozumi; edited by Peter W. Hawkes (Academic Press, Inc.)	1990
Flat Panel Displays Using Amorphous and Microcrystalline Semiconductor Devices (Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices)	102(a) & (b)	Kouji Suzuki; edited by Jerzy Kanicki (Artech House, Inc.)	1991
Liquid Crystal Displays Using Nematic Liquid Crystals (Flat Panel Displays)	102(a) & (b)	S. M. Kelly (The Royal Society of Chemistry)	2000
Microelectronics in Active-Matrix LCDs and Image Sensors (Electro-Optical Displays)	102(a) & (b)	William den Boer et al. ; edited by Mohammad A. Karim (Marcel Dekker, Inc.)	1992
Fundamentals of Active-Matrix Liquid- Crystal Displays	102(a) & (b)	Sang Soo Kim (Society for Information Display)	May 14, 2000
An Amorphous-Si TFT Addressed 3. 2-in. Full-Color LCD (SID International Symposium Digest of Technical Papers)	102(a) & (b)	F. Funada et al. (Society for Information Display)	May 1986
Active-Matrix-Addressed Color LCDs for Avionics Application (SID International Symposium Digest of Technical Papers)	102(a) & (b)	Kazuhisa Katoh et al. (Society for Information Display)	May 1988

U.S. Patent No. 7,414,682			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
A Novel Backlighting Unit with Ultra-High Luminance for Monitor Applications (SID International Symposium Digest of Technical Papers)	102(a) & (b)	H. Sasaki et al. (Society for Information Display)	May 1999
A Late-News Paper: A Novel Protective Diffuser for Backlit LCDs (SID International Symposium Digest of Technical Papers)	102(a) & (b)	Masakazu Uekita et al. (Society for Information Display)	May 2000
Liquid Crystal Flat Panel Displays: Manufacturing Science & Technology	102(a) & (b)	William C. O'Mara (Van Nostrand Reinhold)	1993
CRC Handbook of Chemistry and Physics (67th Edition)	102(a) & (b)	Robert C. Weast (CRC Press, Inc.)	1986
Elements of Material Science: An Introductory Text for Engineering Students (Second Edition)	102(a) & (b)	Lawrence H. Van Vlack	April 1967
Development of Super-TFT-LCDs with IPS Display Mode (Ohta - Asia Display 95)	102(a) & (b)	Ohta et al. (Asia Display '95, Proceedings of the 15th International Display Research Conference, The Institute of Television Engineers of Japan and The Society for Information Display)	October 16–18, 1995
Flat Panel Manufacturing		Hyun Eok Shin, Tetsuhiro Ohno et al.; edited by Jun Souk et al. (John Wiley and Sons Ltd)	2018

U.S. Patent No. 7,414,682			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Principles and Characteristics of Electro-Optical Behaviour with IPS Mode	102(a) & (b)	Ohe et al. (Asia Display '95, Proceedings of the 15th International Display Research Conference, The Institute of Television Engineers of Japan and The Society for Information Display)	October 16–18, 1995
Sputtering Materials for VLSI and Thin Film Devices		Jaydeep Sarkar (Elsevier Inc.)	2014

H. U.S. Patent No. 7,583,347

1. Patents & Published Patent Applications

U.S. Patent No. 7,583,347				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 5,949,509 ("Ohe")	102(a), (b) & (e)	United States	May 8, 1998	September 7, 1999
WO (PCT) Patent Application Publication No. 98/27454 ("Ohta '454")	102(a) & (b)	World Intellectual Property Organization	December 18, 1996	June 25, 1998
U.S. Patent No. 6,351,300 ("Park")	102(e)	United States	August 23, 1999	February 26, 2002
Japanese Patent Application Publication No. H10-301141 ("Asada")	102(a) & (b)	Japan	April 25, 1997	November 13, 1998
Japanese Patent Application Publication No. H09-269508 ("Matsumoto")	102(a) & (b)	Japan	March 29, 1996	October 14, 1997
Japanese Patent Application Publication No. H10-170916 ("Hiyama")	102(a) & (b)	Japan	December 12, 1996	June 26, 1998

WO (PCT) Patent Application Publication No. 99/32924	102(a) & (b)	World Intellectual Property Organization	December 19, 1997	July 1, 1999
Korean Patent Application Publication No. 1999-009891	102(a) & (b)	Korea	July 12, 1997	February 5, 1999
Korean Patent Application Publication No. 1999-0062389	102(a) & (b)	Korea	March 18, 1998	July 26, 1999
Korean Patent Application Publication No. 2000-0004372	102(a) & (b)	Korea	June 30, 1998	January 25, 2000
Japanese Patent Application Publication No. H10-319371	102(a) & (b)	Japan	May 22, 1997	December 4, 1998
Japanese Patent Application Publication No. H10-301141	102(a) & (b)	Japan	April 25, 1997	November 13, 1998
Japanese Patent Application Publication No. H10-010556	102(a) & (b)	Japan	June 26, 1996	January 16, 1998
Japanese Patent Application Publication No. H09-269508	102(a) & (b)	Japan	March 29, 1996	October 14, 1997
Japanese Patent Application Publication No. H09-073101	102(a) & (b)	Japan	September 6, 1995	March 18, 1997
Japanese Patent Application Publication No. H09-061842	102(a) & (b)	Japan	August 21, 1995	March 7, 1997
Japanese Patent Application Publication No. H07-128683	102(a) & (b)	Japan	November 4, 1993	May 19, 1995
Japanese Patent Application Publication No. H06-051311	102(a) & (b)	Japan	August 3, 1992	February 25, 1994
Japanese Patent Application Publication No. 2000-057832	102(a) & (b)	Japan	July 31, 1998	February 25, 2000
U.S. Patent No. 6,266,118	102(e)	United States	May 26, 1999	July 24, 2001
U.S. Patent No. 6,233,034	102(a) & (e)	United States	May 29, 1998	May 15, 2001

U.S. Patent No. 5,969,782 ("Seung Hee Lee")	102(a), (b) & (e)	United States	June 24, 1998	October 19, 1999
U.S. Patent No. 5,886,762	102(a), (b) & (e)	United States	November 19, 1997	March 23, 1999
U.S. Patent No. 6,281,957	102(e)	United States	May 15, 1998	August 28, 2001
U.S. Patent No. 4,345,249	102(a), (b) & (e)	United States	December 12, 1980	August 17, 1982
U.S. Patent No. 5,598,285	102(a), (b) & (e)	United States	September 20, 1993	January 28, 1997
U.S. Patent No. 5,600,464	102(a), (b) & (e)	United States	September 20, 1994	February 4, 1997
U.S. Patent No. 5,734,451	102(a), (b) & (e)	United States	December 3, 1996	March 31, 1998
U.S. Patent No. 5,754,266	102(a), (b) & (e)	United States	March 4, 1996	May 19, 1998
U.S. Patent No. 5,786,876	102(a), (b) & (e)	United States	(PCT Date) June 24, 1994 (371 Date) January 13, 1995	July 28, 1998
U.S. Patent No. 5,831,707	102(a), (b) & (e)	United States	August 24, 1995	November 3, 1998
U.S. Patent No. 5,852,485	102(a), (b) & (e)	United States	February 26, 1997	December 22, 1998
U.S. Patent No. 6,014,190	102(a), (b) & (e)	United States	December 2, 1996	January 11, 2000
U.S. Patent No. 6,049,369	102(a), (b) & (e)	United States	September 9, 1996	April 11, 2000
U.K. Patent Application Publication No. 2,332,769	102(a) & (b)	United Kingdom	May 29, 1998	June 30, 1999
European Patent Application Publication No. 0588568A2	102(a) & (b)	Europe	September 10, 1993	March 23, 1994
European Patent Application Publication No. 0667555A1	102(a) & (b)	Europe	February 13, 1995	August 16, 1995
European Patent Application Publication No. 0673986A2	102(a) & (b)	Europe	March 17, 1995	September 27, 1995
European Patent Application Publication No. 0732612A1	102(a) & (b)	Europe	March 15, 1996	September 18, 1996
U.S. Patent No. 6,452,656 ("Niwano")	102(e)	United States	July 2, 1998	September 17, 2002

U.S. Patent No. 5,739,880	102(a), (b) & (e)	United States	Nov. 29, 1996	April 14, 1998
JP2000091592A (“Yamazaki”)	102(a) & (b)	Japan	August 18, 1999	March 31, 2000
U.S. Patent No. 5,995,187 (“Wakagi”)	102(a), (b), & (e)	United States	August 5, 1997	February 20, 1998
U.S. Patent No. 5,978,059 (“Ohta059”)	102(a), (b), & (e)	United States	May 15, 1998	September 18, 1996
KR19990088122A (“Ashizawa”)	102(a) & (b)	Korea	May 7, 1999	December 27, 1999

2. Publications

U.S. Patent No. 7,583,347			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Optics of liquid crystal displays	102(a) & (b)	Pochi Yeh, Claire Gu (John Wiley & Sons, Inc.)	1999
Active-Matrix Thin- Film Transistor Liquid-Crystal Displays (Advances in Electronics and Electron Physics Vol. 77)	102(a) & (b)	Shinji Morozumi; edited by Peter W. Hawkes (Academic Press, Inc.)	1990
Flat Panel Displays Using Amorphous and Microcrystalline Semiconductor Devices (Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices)	102(a) & (b)	Kouji Suzuki; edited by Jerzy Kanicki (Artech House, Inc.)	1991
Liquid Crystal Displays Using Nematic Liquid Crystals (Flat Panel Displays)	102(a)	S. M. Kelly (The Royal Society of Chemistry)	2000
Microelectronics in Active-Matrix LCDs and Image Sensors (Electro-Optical Displays)	102(a) & (b)	William den Boer et al. ; edited by Mohammad A. Karim (Marcel Dekker, Inc.)	1992
SID Seminar Note (May 14, 2000): Fundamentals of Active-Matrix Liquid-Crystal Displays (“Sang Soo Kim”)	102(a) & (b)	Sang Soo Kim (Society for Information Display)	May 14, 2000

U.S. Patent No. 7,583,347			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
An Amorphous-Si TFT Addressed 3. 2-in. Full-Color LCD (SID International Symposium Digest of Technical Papers)	102(a) & (b)	F. Funada et al. (Society for Information Display)	May 1986
Active-Matrix-Addressed Color LCDs for Avionics Application (SID International Symposium Digest of Technical Papers)	102(a) & (b)	Kazuhisa Katoh et al. (Society for Information Display)	May 1988
A Novel Backlighting Unit with Ultra-High Luminance for Monitor Applications (SID International Symposium Digest of Technical Papers)	102(a) & (b)	H. Sasaki et al. (Society for Information Display)	May 1999
A Late-News Paper: A Novel Protective Diffuser for Backlit LCDs (SID International Symposium Digest of Technical Papers)	102(a)	Masakazu Uekita et al. (Society for Information Display)	May 2000
Liquid Crystal Flat Panel Displays: Manufacturing Science & Technology	102(a) & (b)	William C. O'Mara (Van Nostrand Reinhold)	1993
CRC Handbook of Chemistry and Physics (67th Edition)	102(a) & (b)	Robert C. Weast (CRC Press, Inc.)	1986
Elements of Material Science: An Introductory Text for Engineering Students (Second Edition)	102(a) & (b)	Lawrence H. Van Vlack	April 1967

U.S. Patent No. 7,583,347			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
Development of Super-TFT-LCDs with IPS Display Mode (Ohta - Asia Display 95)	102(a) & (b)	Ohta et al. (Asia Display '95, Proceedings of the 15th International Display Research Conference, The Institute of Television Engineers of Japan and The Society for Information Display)	October 16-18, 1995
Flat Panel Manufacturing		Hyun Eok Shin, Tetsuhiro Ohno et al.; edited by Jun Souk et al. (John Wiley and Sons Ltd)	2018
Principles and Characteristics of Electro-Optical Behaviour with IPS Mode	102(a) & (b)	Ohe et al. (Asia Display '95, Proceedings of the 15th International Display Research Conference, The Institute of Television Engineers of Japan and The Society for Information Display)	October 16-18, 1995
Sputtering Materials for VLSI and Thin Film Devices		Jaydeep Sarkar (Elsevier Inc.)	2014

I. U.S. Patent No. 7,995,047

1. Patents & Published Patent Applications

U.S. Patent No. 7,995,047				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 7,760,161 ("Sasaki")	102(e)	United States	July 14, 2004	July 20, 2010
U.S. Patent Application Publication No. 2005/0017765 ("Sasaki")	102(a), (b) & (e)	United States	July 14, 2004	January 27, 2005
U.S. Patent No. 6,870,192 ("Yamazaki")	102(a), (b) & (e)	United States	September 20, 2002	March 22, 2005
U.S. Patent No. 7,760,163 ("Jo")	102(e)	United States	January 10, 2006	July 20, 2010

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U.S. Patent No. 7,995,047				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent Application Publication No. 2006/0158396 ("Jo")	102(a), (b) & (e)	United States	January 10, 2006	July 20, 2006
U.S. Patent No. 7,268,717 ("Baek")	102(a) & (e)	United States	January 27, 2006	September 11, 2007
U.S. Patent Application Publication No. 2006/0170629 ("Baek")	102(a), (b) & (e)	United States	January 27, 2006	August 3, 2006
U.S. Patent No. 7,859,489 ("Furuichi")	102(e)	United States	December 27, 2006	December 28, 2010
U.S. Patent No. 7,679,586 ("Stewart")	102(e) & (g)	United States	June 7, 2007	March 16, 2010
U.S. Patent No. 7,304,621 ("Oomori")	102(a) & (e)	United States	March 16, 2004	December 4, 2007
U.S. Patent Application Publication No. 2004/0201556 ("Oomori")	102(a), (b) & (e)	United States	March 16, 2004	October 14, 2004
U.S. Patent No. 7,626,565 ("Tsuge")	102(e)	United States	February 28, 2006	December 1, 2009
U.S. Patent Application Publication No. 2006/0232612 ("Tsuge")	102(a), (b) & (e)	United States	February 28, 2006	October 19, 2006
U.S. Patent No. 8,044,892 ("Chaussy)	102(e)	United States	December 6, 2005	October 25, 2011
U.S. Patent Application Publication No. 2006/0118700 ("Chaussy")	102(a), (b) & (e)	United States	December 6, 2005	June 8, 2006
US 7,397,449 ("Kasai")	102(e)	United States	June 30, 2005	July 8, 2008

U.S. Patent No. 7,995,047				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent Application Publication No. 2005/0140601 ("Kasai")	102(a), (b) & (e)	United States	September 1, 2004	June 30, 2005
U.S. Patent No. 8,325,111 ("Kimura")	102(e)	United States	November 22, 2006	December 4, 2012
U.S. Patent Application Publication No. 2007/0126664 ("Kimura")	102(a), (b) & (e)	United States	November 22, 2006	June 7, 2007

2. Publications

U.S. Patent No. 7,995,047			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
"A Design of AM-OLED Source Driver with reduced Programming Time for a Large Scale Display Panel"	102(a) & (b)	Jane Woo Ryu et al., *2005 IEEE Conference on Electron Devices and Solid-State Circuits*, p. 475–477	Dec. 19–21, 2005
"An integrated poly-Si TFT current data driver with a data-line pre-charge function. Journal of the Society for Information Display"	102(a) & (b)	M. Shimoda et al., *Journal of the Society for Information Display* vol. 11 no. 3, p. 461–466	2003
"A Current-Mode Display Driver IC Using Sample-and- Hold Scheme for QVGA Full-Color AMOLED Displays"	102(a)	J. H. Baek et al., *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, p. 2974–2982	Dec. 2006
"A Single Driver Chip for Gray Scale Passive-Matrix OLED"	102(a) & (b)	M. Liu et al., Int'l Conf. on Commn's, Circuits & Systems, p. 2193–2196	June 25–28, 2006
"Pixel circuits and drive schemes for glass and elastic AMOLED displays"	102(a) & (b)	S. Alexander et al., Journal of the Society for Information Display 13(7) p. 587–595	July 2005

U.S. Patent No. 7,995,047			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
"A Current Driver IC using a S/H for QVGA Full-Color Active-Matrix Organic LED Mobile Displays"	102(a) & (b)	J. H. Baek et al., 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, p. 609–618	Feb. 6–9, 2006

J. U.S. Patent No. 8,093,830

1. Patents & Published Patent Applications

U.S. Patent No. 8,093,830				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
Admitted Prior Art ("APA") in US 8,093,830 ("'830 APA")	102(a), (b) & (g)(2)	United States Japan	July 1, 2009	January 10, 2012
Japanese Patent Application Publication No. 2004-327152 ("Shimizu")	102(a) & (b)	Japan	April 23, 2003	November 18, 2004
U.S. Patent No. 7,332,699 ("Nishimura")	102(a), (b) & (e)	United States	July 23, 2004	February 19, 2008
U.S. Patent No. 8,242,787 ("Hente")	102(e)	United States	March 27, 2008	August 14, 2012
U.S. Patent No. 7,471,287 ("Chen")	102(e)	United States	December 29, 2006	December 30, 2008
U.S. Patent No. 2008/0100234 ("Chen")	102(a), (b) & (e)	United States	December 29, 2006	May 1, 2008
U.S. Patent No. 7,262,559 ("Tripathi 559")	102(a), (b) & (e)	United States	December 11, 2003	August 28, 2007
U.S. Patent No. 6,577,512 ("Tripathi 512")	102(a), (b) & (e)	United States	May 25, 2001	June 10, 2003
WO (PCT) Patent Application Publication No. 2005/079121 ("Bhagat")	102(a), (b) & (e)	World Intellectual Property Organization	February 11, 2005	August 25, 2005

U.S. Patent No. 8,093,830				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
U.S. Patent No. 7,391,335 ("Mubaslat")	102(a), (b) & (e)	United States	August 18, 2005	June 24, 2008
U.S. Patent Application Publication No. 2007/0040696 ("Mubaslat")	102(a), (b) & (e)	United States	August 18, 2005	February 22, 2007
Japanese Patent Application Publication No. 2006-210271 ("Nagase")	102(a) & (b)	Japan	January 31, 2005	August 10, 2006
U.S. Patent No. 7,202,608 ("Robinson")	102(a), (b) & (e)	United States	April 6, 2005	April 10, 2007
U.S. Patent No. 6,285,139 ("Ghanem")	102(a), (b) & (e)	United States	December 23, 1999	September 4, 2001
Japanese Patent Application Publication No. 2006-303093 ("Matsuda")	102(a) & (b)	Japan	April 19, 2005	November 2, 2006
U.S. Patent No. 7,276,861 ("Shteynberg")	102(e)	United States	January 19, 2007	February 2, 2010
U.S. Patent No. 8,111,014 ("Van Erp")	102(e)	United States	June 7, 2007	February 7, 2012
WO (PCT) Patent Application Publication No. 2008/001246 ("Van Erp")	102(a), (b) & (e)	World Intellectual Property Organization	June 7, 2007	January 3, 2008
U.S. Patent No. 6,747,420 ("Barth")	102(a), (b) & (e)	United States	September 13, 2002	June 8, 2004
U.S. Patent No. 7,492,108 ("Garcia")	102(a) & (e)	United States	August 11, 2005	February 17, 2009
U.S. Patent Application Publication No. 2007/0035538 ("Garcia")	102(a), (b) & (e)	United States	August 11, 2005	February 15, 2007

U.S. Patent No. 8,093,830				
Patent or Patent Publication Number	**Prior Art Provision**	**Country of Origin**	**Filing Date**	**Issuance or Publication Date**
’830 Prior Art Products	102(a), (b) & (g)(2)	United States	N/A	N/A
U.S. 2007/0170876 (“Ito”)	102(a), (b) & (e)	United States	January 23, 2007	July 26, 2007
JP2008130523A	102(a) & (b)	Japan	November 24, 2006	June 5, 2008
US6285139	102(a), (b), & (e)	United States	December 23, 1999	July 5, 2001
US7262559	102(a), (b), & (e)	United States	December 11, 2003	July 8, 2004
US7332699	102(a), (b), & (e)	United States	July 23, 2004	January 26, 2006
WO2008050679A1	102(a) & (b)	Japan	October 19, 2007	May 2, 2008

2. Publications

U.S. Patent No. 8,093,830			
Title	**Prior Art Provision**	**Author and Publisher**	**Date of Publication**
CONTROL SYSTEMS ENGINEERING	102(a), (b) & (f)	Norman S. Nise (Jon Wiley & Sons, Inc.)	2004
ELECTRICAL ENGINEERING REFERENCE MANUAL FOR THE ELECTRICAL AND COMPUTER PE EXAM	102(a), (b) & (f)	John A. Camara (PE Professional Publications, Inc.)	2002
AN INTRODUCTION TO CONTROL SYSTEMS, 2 ED., Vol. 8	102(a) & (b)	Kevin Warwick, ADVANCED SERIES IN ELECTRICAL AND COMPUTER ENGINEERING (WORLD SCIENTIFIC PUBLISHING CO. PTC LTD: 1989)	January 1, 1996
THE ART OF ELECTRONICS, 2nd Ed.	102(a) & (b)	Paul Horowitz et al. (Cambridge University Press: 1989)	July 28, 1989
POWER SUPPLIES FOR LED DRIVING, 1st Ed.	102(a) & (b)	Steve Winder (Newnes: 2008)	April 1, 2008

K. Products and Systems

Defendant is diligently seeking and will continue to diligently seek documents from third parties in discovery to demonstrate such third parties' earlier dates of invention under 35 U.S.C. § 102(g) and/or prior art offers for sale and public uses of products embodying the claimed invention under 35 U.S.C. § 102(b) or under 35 U.S.C. § 102(a). On information and belief, electronic devices, including LCDs, made by Hitachi, Sharp, Samsung Display, Sanyo Electric, Motorola, Fujitsu, Sony, Seiko Epson, Matsushita, Panasonic, or Citizen Watch, anticipate or render obvious the asserted claims of the patents in suit. Defendant therefore reserves the right to supplement these Invalidity Contentions with further information and documentation, if and when it becomes available.

L. Section 101

Defendant reserves the right to assert 101 defenses based on Plaintiff's claim construction positions, infringement theories, and other information that may be obtained through the discovery process.

M. Secondary Considerations of Non-Obviousness

Plaintiff cannot show secondary considerations of non-obviousness and is unable to establish a nexus between any asserted claim and objective evidence. For example, plaintiff cannot show any long-felt need, as demonstrated by the plethora of prior art shown in section V herein. For the same reason, plaintiff is unable to show failure of others. Plaintiff has not shown (and cannot show) any of the secondary considerations (such as commercial success, long-felt but unsolved needs, failure of others, unexpected results, copying, licensing, and praise) to be met, and Defendant reserves the right to rebut any evidence related to secondary considerations later identified by plaintiff.

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VI. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

As required by P.R. 3-4(a), BOE has previously produced documents labeled BOE-BDT_0000001 through BOE-BDT_0004012, and is concurrently making design files for the accused products available for inspection, as documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by Bishop in its P.R. 3-1(c) charts, to the extent such documents are within BOE's possession, custody, or control and were able to be located after a reasonable search. BOE has identified additional documents for which it owes a third party a confidentiality obligation and is presently in the process of complying with any applicable notice and/or consent provisions concerning additional documents that are subject to such restrictions. BOE will produce those documents once it has complied with the applicable provisions.

Pursuant to P.R. 3-4(b), BOE is producing each item of prior art identified pursuant to P.R. 3-3(a) which does not appear in the file history of the Asserted Patents. Due to the transition of outside counsel to a new firm, BOE is concurrently serving this prior art as native files and will separately provide production versions once the production database is available to run the production.

Subject to all reservation of rights and objections set forth herein, and/or after Bishop's identification of all accused devices with specificity, BOE further reserves the right to supplement its document production pursuant to the Scheduling Order and Federal Rules of Civil Procedure.

Dated: September 24, 2025

Respectfully submitted,

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Counsel for Defendant
BOE Technology Group Co., Ltd.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that counsel of record who are deemed to have consented to electronic service are being served today, September 24, 2025, with a copy of this document via electronic mail.

/s/ *Matthew R. Shapiro*
Matthew R. Shapiro