

EXHIBIT 20
UNITED STATES PATENT NO. 9,036,701
CLAIM CHART FOR INFRINGEMENT OF CLAIMS 1, 8, AND 15 BY HISENSE ACCUSED PRODUCTS

As demonstrated in the chart below, The Hisense Respondents. (“Hisense”) directly and indirectly infringe the asserted claims of US 9,036,701 (the “’701 Patent”). Hisense directly infringes, contributes to the infringement of, and/or induces infringement of the ’701 Patent by making, using, selling, offering for sale, and/or importing into the United States the Accused Products that are covered by one or more claims of the ’701 Patent. The Accused Products are devices that decode H.265-compliant video. For example, the Hisense 43A7N is a representative product for other Hisense devices that decode H.265-compliant video.

The Hisense 43A7N contains at least one video decoder that helps decode H.265-compliant video.¹ While evidence from the Hisense 43A7N is specifically charted herein, the evidence and contentions charted herein apply equally to the other Hisense Accused Products that decode H.265-compliant video. The example ’701 Patent Accused Products are listed in NOK1448_00002051. The ’701 Accused Products are also identified in Hisense’s Response to Interrogatory No. 1 and all supplements thereto.

No part of this exemplary chart construes, or is intended to construe, the specification, file history, or claims of the ’701 Patent. Moreover, this exemplary chart does not limit, and is not intended to limit, Nokia’s infringement positions or contentions.

The following infringement chart includes exemplary citations to ITU-T Rec. H.265 (12/2016) High efficiency video coding (available at NOK1448_00002414) (the “H.265 Standard”). The cited functionality has been included in editions of the H.265 Standard since April 2013 and remains in current editions of the H.265 Standard. Any Hisense device that decodes H.265-compliant video practices the claims of the ’701 Patent. Thus, the Accused Products each practice the H.265 Standard and are covered by claims of the ’701 Patent.

Nokia contends each of the following limitations is met literally, and, to the extent a limitation is not met literally, it is met under the doctrine of equivalents.²

¹ See, e.g., Ex. 92, Hisense 43A7N User Manual, available at <https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n>.

² This claim chart is based on the information currently available to Nokia and is intended to be exemplary in nature. Nokia reserves all rights to update and elaborate its infringement positions, including as Nokia obtains additional information during the course of discovery.

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1. Claim 1

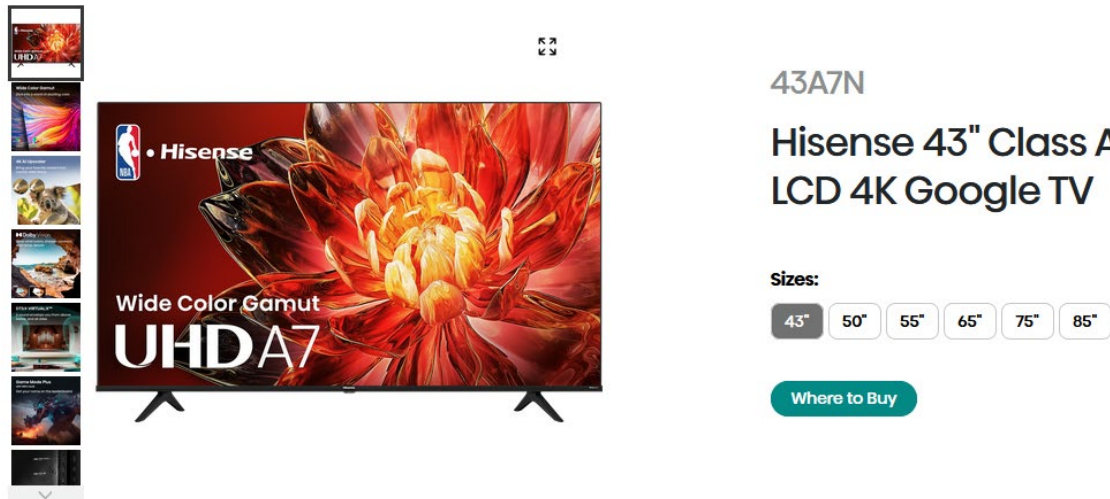
U.S. PATENT NO. 9,036,701	HISENSE ACCUSED PRODUCTS
<p>1. [Pre] A method comprising:</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method comprising the limitations below.</p> <p>For example, and without limitation, the Hisense 43A7N uses hardware-accelerated video decoding and includes Mediatek MT9602 Processor.</p> <div data-bbox="619 560 1722 1055">  </div> <p>https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).</p>

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	<div data-bbox="638 451 1178 797">  </div> <div data-bbox="1209 354 1743 634"> <p>Display: 42.5 in, VA, Direct LED, 3840 x 2160 pixels Viewing angles (H/V): 178 ° / 178 ° Brightness: 275 cd/m² Static contrast: 4000 : 1 Refresh rate: 50 Hz / 60 Hz Frame interpolation: 120 MR (Motion Rate) TV tuner: Analog (NTSC/PAL/SECAM), ATSC, Clear QAM SoC: MediaTek MT9602 CPU: ARM Cortex-A53, 1500 MHz, Cores: 4 Dimensions: 963 x 560 x 74 mm Weight: 6.8 kg</p> </div> <div data-bbox="1218 659 1690 706"> <div>Add to compare</div> <div>Suggest an edit</div> </div> <div data-bbox="619 911 1331 941"> https://www.displayspecifications.com/en/model/234a3f3b </div>

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	Video Format			
	MPEG program stream	MPEG1/2	.DAT, .VOB, .MPG, .MPEG	1920 x 1080 @ 60fps
		MPEG4		
		H.264		3840 x 2160 @ 60fps
	MPEG transport stream	HEVC/H.265	.ts, .trp, .tp	3840 x 2160 @ 60fps
		MPEG4		1920 x 1080 @ 60fps
		H.264		3840 x 2160 @ 60fps
		VC1		1920 x 1080 @ 60fps

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	Container	Video Codec	File Extension Name	Resolution and Frame Rate
		MPEG1/2		1920 x 1080 @ 60fps
		AVS		
		AVS+		
		AVS2		3840 x 2160 @ 60fps
	MP4	VP8	.mp4, .mov	1920 x 1080 @ 60fps
		AV1		3840 x 2160 @ 60fps
		HEVC/H.265		
		MPEG1/2		1920 x 1080 @ 60fps
		MPEG4		
		H.263		
		H.264		3840 x 2160 @ 60fps
		WMV3		1920 x 1080 @ 60fps
		VC1		
		Motion JPEG		1920 x 1080 @ 30fps
	Source: Hisense 43A7N User Manual, at 45-46. Downloaded from https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).			
For example, a Hisense 43A7N was used to playback an H.265-compliant video.				

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	<div data-bbox="646 280 1822 1162"><p>Acer-AV16-HEVC-Main10-Encode-QSV.mp4</p><p>hevc aac</p></div> <p data-bbox="646 1166 1507 1198">Source: Picture of H.265-complaint video playback on Hisense 43A7N</p>

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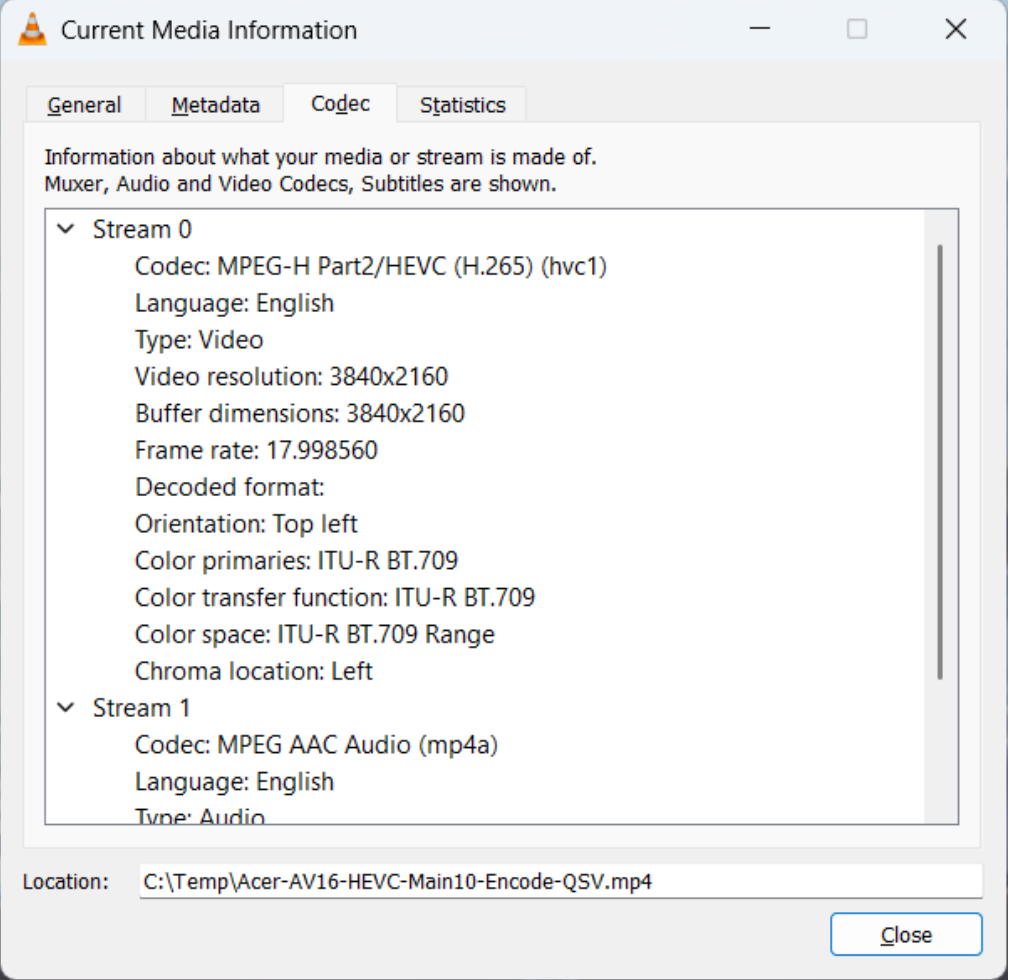
U.S. PATENT NO. 9,036,701	HISENSE ACCUSED PRODUCTS
	 <p>Source: Media Information for video decoded by Hisense 43A7N.</p>

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	<p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising the limitations below.</p> <p>3 Definitions</p> <p>For the purposes of this Recommendation International Standard, the following definitions apply.</p> <p>...</p> <p>3.12 bitstream: A sequence of bits, . . . , that forms the representation of <i>coded pictures</i> and associated data forming one or more coded video sequences (<i>CVSs</i>).</p> <p>...</p> <p>3.25 coded picture: A <i>coded representation</i> of a <i>picture</i> . . .</p> <p>...</p> <p>3.44 decoding process: The process specified in this Specification that reads a <i>bitstream</i> and derives <i>decoded pictures</i> from it.</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 4 – 7.</p>
<p>[a] determining a frequency of occurrence threshold based on an expected frequency of occurrence of syntax elements in a bit stream;</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method comprising determining a frequency of occurrence threshold based on an expected frequency of occurrence of syntax elements in a bit stream.</p> <p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising determining a frequency of occurrence threshold based on an expected frequency of occurrence of syntax elements in a bit stream.</p>

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	<p>The following specifications provide further evidence of how each of the Accused Products operates:</p> <p>3 Definitions</p> <p>For the purposes of this Recommendation International Standard, the following definitions apply. ... </p> <p>3.153 syntax element: <i>An element of data represented in the bitstream.</i> ... </p> <p>3.166 transform coefficient: A Scalar quantity, considered to be in a frequency domain, that is associated with a particular one-dimensional or two-dimensional <i>frequency index</i> in a <i>transform</i> in the <i>decoding process</i>.</p> <p>3.167 transform coefficient level: <i>An integer quantity representing the value associated with a particular two-dimensional frequency index in the decoding process prior to scaling for computation of a transform coefficient value.</i></p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 12.</p> <p>7.3.8.11 Residual coding syntax</p> <table border="1" data-bbox="690 1099 1864 1203"> <tr> <td data-bbox="690 1099 1713 1138">residual_coding(x0, y0, log2TrafoSize, cIdx) {</td><td data-bbox="1713 1099 1864 1138">Descriptor</td></tr> <tr> <td data-bbox="690 1138 1713 1203">if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))</td><td data-bbox="1713 1138 1864 1203"></td></tr> </table> <p>...</p>	residual_coding(x0, y0, log2TrafoSize, cIdx) {	Descriptor	if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))	
residual_coding(x0, y0, log2TrafoSize, cIdx) {	Descriptor				
if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))					

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	numGreater1Flag = 0	
	lastGreater1ScanPos = -1	
	for(n = 15; n >= 0; n--) {	
	xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]	
	yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]	
	if(sig_coeff_flag[xC][yC]) {	
	if(numGreater1Flag < 8) {	
	coeff_abs_level_greater1_flag[n]	ae(v)
	numGreater1Flag++	
	if(coeff_abs_level_greater1_flag[n] && lastGreater1ScanPos == -1)	
	lastGreater1ScanPos = n	
	else if(coeff_abs_level_greater1_flag[n])	
	escapeDataPresent = 1	
	} else	
	...	
ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 58-59.		
Additionally, the video played back on the Hisense 43A7N was analyzed to confirm that the video contained transform units with more than eight non-zero transform coefficients according to the H.265 Standard.		
For example, NAL 46, IDR Frame 18, at CTB [38,15], CU [2432,976] is an 8x8 coded block broken up into 4x4 sub-blocks.		

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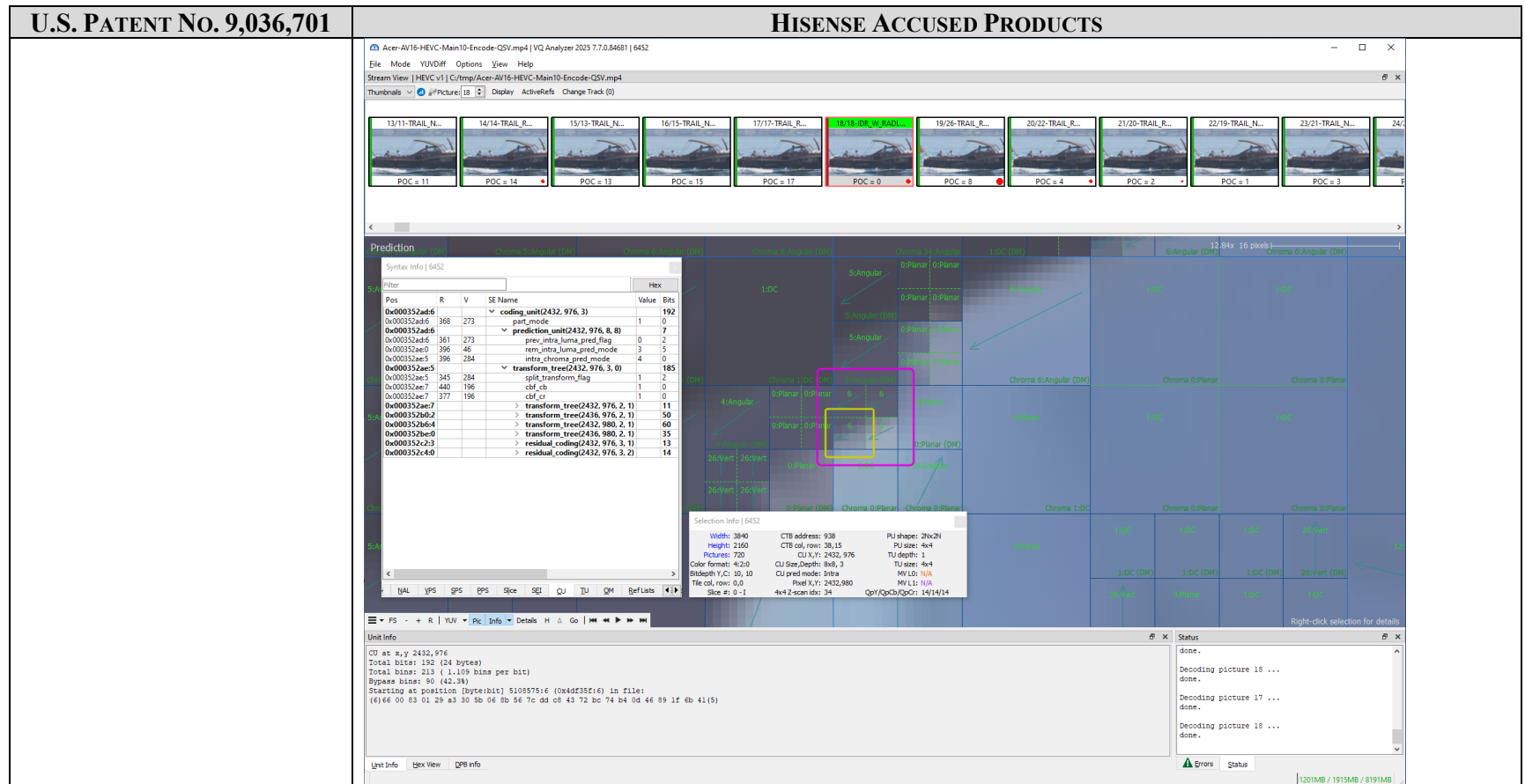


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Syntax Info | 6452

Pos	R	V	SE Name	Value	Bits	Bits, %	D
0x000352b6:4	336	40	cbf_luma	1	0	0.00	AI
0x000352b6:4			transform_unit(2432, 980, 2, 1)	60	100.00		
0x000352b6:4			residual_coding(2432, 980, 2, 0)	60	100.00		
0x000352b6:4	329	40	transform_skip_flag	0	0	0.00	AI
0x000352b6:4	322	40	last_sig_coeff_x_prefix	1	2	3.33	AI
0x000352b6:6	328	162	last_sig_coeff_y_prefix	3	3	5.00	AI
0x000352b7:1	256	70	sig_coeff_flag	0	1	1.67	AI
0x000352b7:2	280	141	sig_coeff_flag	0	1	1.67	AI
0x000352b7:3	370	282	sig_coeff_flag	1	2	3.33	AI
0x000352b7:5	440	90	sig_coeff_flag	1	1	1.67	AI
0x000352b7:6	464	181	sig_coeff_flag	1	1	1.67	AI
0x000352b7:7	474	363	sig_coeff_flag	1	1	1.67	AI
0x000352b8:0	284	62	sig_coeff_flag	1	1	1.67	AI
0x000352b8:1	312	124	sig_coeff_flag	1	1	1.67	AI
0x000352b8:2	444	249	sig_coeff_flag	1	0	0.00	AI
0x000352b8:2	307	249	sig_coeff_flag	1	2	3.33	AI
0x000352b8:4	380	151	sig_coeff_flag	1	1	1.67	AI
0x000352b8:5	460	303	sig_coeff_flag	1	0	0.00	AI
0x000352b8:5	366	303	sig_coeff_flag	1	0	0.00	AI
0x000352b8:5	339	303	coeff_abs_level_greater1_flag	1	3	5.00	AI
0x000352b9:0	384	100	coeff_abs_level_greater1_flag	1	1	1.67	AI
0x000352b9:1	394	201	coeff_abs_level_greater1_flag	1	1	1.67	AI
0x000352b9:2	432	403	coeff_abs_level_greater1_flag	0	1	1.67	AI
0x000352b9:3	338	280	coeff_abs_level_greater1_flag	0	1	1.67	AI
0x000352b9:4	316	201	coeff_abs_level_greater1_flag	0	1	1.67	AI
0x000352b9:5	256	27	coeff_abs_level_greater1_flag	1	1	1.67	AI

Selection Info | 6452

Width: 3840	CTB address: 938	PU shape: 2Nx2N
Height: 2160	CTB col, row: 38, 15	PU size: N/A
Pictures: 720	CU X,Y: 2432, 976	TU depth: 1
Color format: 4:2:0	CU Size, Depth: 8x8, 3	TU size: 4x4
Bitdepth Y,C: 10, 10	CU pred mode: Intra	MV L0: N/A
Tile col, row: 0,0	Pixel X,Y: 2432,980	MV L1: N/A
Slice #: 0 - I	4x4 Z-scan idx: 34	QpY/QpCb/QpCr: 14/14/14

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

CU [2432,976] includes transform block [2432,980], which has 12 non-zero transform coefficients.

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

CU [2432,976] includes transform block [2432,980], which has 12 non-zero transform coefficients.

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Transform block (2432,980) details

Syntax Info | 6452

Filter								Hex
Pos	R	V	SE Name	Value	Bits	Bits, %	Decoding type	Ctx Idx
0x000352b6:4	336	40	cbf_luma	1	0	0.00	Arithmetic	0
0x000352b6:4			transform_unit(2432, 980, 2, 1)		60	100.00		
0x000352b6:4			residual_coding(2432, 980, 2, 0)		60	100.00		
0x000352b6:4	329	40	transform_skip_flag	0	0	0.00	Arithmetic	0
0x000352b6:4	322	40	last_sig_coeff_x_prefix	1	2	3.33	Arithmetic	0
0x000352b6:6	328	162	last_sig_coeff_y_prefix	3	3	5.00	Arithmetic	0
0x000352b7:1	256	70	sig_coeff_flag	0	1	1.67	Arithmetic	5
0x000352b7:2	280	141	sig_coeff_flag	0	1	1.67	Arithmetic	8
0x000352b7:3	370	282	sig_coeff_flag	1	2	3.33	Arithmetic	8
0x000352b7:5	440	90	sig_coeff_flag	1	1	1.67	Arithmetic	4
0x000352b7:6	464	181	sig_coeff_flag	1	1	1.67	Arithmetic	4
0x000352b7:7	474	363	sig_coeff_flag	1	1	1.67	Arithmetic	7
0x000352b8:0	284	62	sig_coeff_flag	1	1	1.67	Arithmetic	6
0x000352b8:1	312	124	sig_coeff_flag	1	1	1.67	Arithmetic	3
0x000352b8:2	444	249	sig_coeff_flag	1	0	0.00	Arithmetic	1
0x000352b8:2	307	249	sig_coeff_flag	1	2	3.33	Arithmetic	7
0x000352b8:4	380	151	sig_coeff_flag	1	1	1.67	Arithmetic	6
0x000352b8:5	460	303	sig_coeff_flag	1	0	0.00	Arithmetic	2
0x000352b8:5	366	303	sig_coeff_flag	1	0	0.00	Arithmetic	0
0x000352b8:5	339	303	coeff_abs_level_greater1_flag	1	3	5.00	Arithmetic	1
0x000352b9:0	384	100	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0
0x000352b9:1	394	201	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0
0x000352b9:2	432	403	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0
0x000352b9:3	338	280	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0
0x000352b9:4	316	201	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0
0x000352b9:5	256	27	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0
0x000352b9:6	256	55	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0
0x000352b9:7	256	110	coeff_abs_level_greater2_flag	0	1	1.67	Arithmetic	0
0x000352ba:0	366	221	coeff_sign_flag	1	1	1.67	Bypass	
0x000352ba:1	366	77	coeff_sign_flag	0	1	1.67	Bypass	

MP4NALVPSSPSPSSliceSEICUQUQMRef ListsStatsHRD

Y Levels (2432,980)

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

The first 8 non-zero transform coefficient values are coded using the coeff_abs_level_greater1_flag, which is arithmetic coded using context updating. The remaining non-zero transform coefficient values are coded using coeff_abs_level_remaining, which is bypass coded.

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Transform block (2432,980) details

Syntax Info | 6452

Filter

Hex

Pos	R	V	SE Name	Value	Bits	Bits, %	Decoding type	Ctx Idx	↵	^
0x000352b6:4	336	40	cbf_luma	1	0	0.00	Arithmetic	0	6	
0x000352b6:4			transform_unit(2432, 980, 2, 1)		60	100.00				
0x000352b6:4			residual_coding(2432, 980, 2, 0)		60	100.00				
0x000352b6:4	329	40	transform_skip_flag	0	0	0.00	Arithmetic	0	6	
0x000352b6:4	322	40	last_sig_coeff_x_prefix	1	2	3.33	Arithmetic	0	0	
0x000352b6:6	328	162	last_sig_coeff_y_prefix	3	3	5.00	Arithmetic	0	4	
0x000352b7:1	256	70	sig_coeff_flag	0	1	1.67	Arithmetic	5	4	
0x000352b7:2	280	141	sig_coeff_flag	0	1	1.67	Arithmetic	8	8	
0x000352b7:3	370	282	sig_coeff_flag	1	2	3.33	Arithmetic	8	9	
0x000352b7:5	440	90	sig_coeff_flag	1	1	1.67	Arithmetic	4	0	
0x000352b7:6	464	181	sig_coeff_flag	1	1	1.67	Arithmetic	4	1	
0x000352b7:7	474	363	sig_coeff_flag	1	1	1.67	Arithmetic	7	1	
0x000352b8:0	284	62	sig_coeff_flag	1	1	1.67	Arithmetic	6	2	
0x000352b8:1	312	124	sig_coeff_flag	1	1	1.67	Arithmetic	3	9	
0x000352b8:2	444	249	sig_coeff_flag	1	0	0.00	Arithmetic	1	8	
0x000352b8:2	307	249	sig_coeff_flag	1	2	3.33	Arithmetic	7	8	
0x000352b8:4	380	151	sig_coeff_flag	1	1	1.67	Arithmetic	6	3	
0x000352b8:5	460	303	sig_coeff_flag	1	0	0.00	Arithmetic	2	1	
0x000352b8:5	366	303	sig_coeff_flag	1	0	0.00	Arithmetic	0	3	
0x000352b8:5	339	303	coeff_abs_level_greater1_flag	1	3	5.00	Arithmetic	1	2	
0x000352b9:0	384	100	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0	2	
0x000352b9:1	394	201	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0	3	
0x000352b9:2	432	403	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0	4	
0x000352b9:3	338	280	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0	2	
0x000352b9:4	316	201	coeff_abs_level_greater1_flag	0	1	1.67	Arithmetic	0	1	
0x000352b9:5	256	27	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0	0	
0x000352b9:6	256	55	coeff_abs_level_greater1_flag	1	1	1.67	Arithmetic	0	1	
0x000352b9:7	256	110	coeff_abs_level_greater2_flag	0	1	1.67	Arithmetic	0	1	
0x000352ba:0	366	221	coeff_sign_flag	1	1	1.67	Bypass			
0x000352ba:1	366	77	coeff_sign_flag	0	1	1.67	Bypass			

MP4NALVPSSPSPSSliceSEIQUITUQMRefListsStatsHRD

Y Levels (2432,980)

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

As another example, NAL 46, IDR Frame 18, CTB [37,15] CU[2424,976] is an 8x8 intra-coded block broken up into 4x4 sub-blocks.

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Snap - Exhibit 1021
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CLAIM CHART FOR INFRINGEMENT OF CLAIMS 1, 8, AND 15 BY HISENSE ACCUSED PRODUCTS

U.S. PATENT NO. 9,036,701	HISENSE ACCUSED PRODUCTS																																																																																																																																																									
	<div style="border: 1px solid #ccc; padding: 5px;"><div style="font-size: 0.8em; margin-bottom: 5px;">Acer-AV16-HEVC-Main10-Encode-QSV.mp4 VQ Analyzer 2025 7.7.0.84681 616</div><div style="margin-bottom: 5px;">File Mode YUVDiff Options View Help</div><div style="margin-bottom: 5px;">Stream View HEVC v1 C:\tmp\Acer-AV16-HEVC-Main10-Encode-QSV.mp4</div><div style="margin-bottom: 5px;">Thumbnails ▾ a/Picture: 18 ▾ Display ActiveRefs Change Track (0)</div><div style="display: flex; justify-content: space-around; align-items: center; margin-bottom: 10px;"><div></div><div></div><div></div><div></div><div></div><div style="border: 2px solid red; padding: 2px;"></div><div></div><div></div><div></div><div></div><div></div></div><div style="margin-bottom: 10px;">Prediction <div style="font-size: 0.7em; margin-bottom: 5px;">Syntax info 616</div><table border="1" style="width: 100%; border-collapse: collapse; font-size: 0.7em;"><thead><tr><th>Filter</th><th>Pos</th><th>R</th><th>V</th><th>SE Name</th><th>Value</th><th>Bits</th><th>Bits %</th><th>Decoding t</th></tr></thead><tbody><tr><td colspan="9">0x0003517b:4 coding_unit(2424, 976, 3) 76 100.00</td></tr><tr><td>0x0003517b:4</td><td>508</td><td>320</td><td></td><td>part_mode</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td></tr><tr><td colspan="9">0x0003517b:4 prediction_unit(2424, 976, 8, 8) 2 2.63</td></tr><tr><td>0x0003517b:4</td><td>499</td><td>320</td><td></td><td>prev_intra_luma_pred_flag</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td></tr><tr><td>0x0003517b:4</td><td>341</td><td>320</td><td></td><td>mpm_idx</td><td>2</td><td>2</td><td>100.00</td><td>Bypass</td></tr><tr><td>0x0003517b:6</td><td>341</td><td>259</td><td></td><td>intra_chroma_pred_mode</td><td>4</td><td>0</td><td>0.00</td><td>Arithmetic</td></tr><tr><td colspan="9">0x0003517b:6 split_transform_flag 74 97.37</td></tr><tr><td>0x0003517b:6</td><td>334</td><td>259</td><td></td><td>split_transform_flag</td><td>1</td><td>2</td><td>2.70</td><td>Arithmetic</td></tr><tr><td>0x0003517c:0</td><td>376</td><td>78</td><td></td><td>cbf_cb</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td></tr><tr><td>0x0003517c:0</td><td>307</td><td>78</td><td></td><td>cbf_cr</td><td>1</td><td>1</td><td>1.35</td><td>Arithmetic</td></tr><tr><td colspan="9">0x0003517c:1 transform_tree(2424, 976, 2, 1) 10 13.51</td></tr><tr><td>0x0003517d:3</td><td></td><td></td><td></td><td>transform_tree(2428, 976, 2, 1)</td><td>4</td><td>5.41</td><td></td><td></td></tr><tr><td>0x0003517d:7</td><td></td><td></td><td></td><td>transform_tree(2424, 980, 2, 1)</td><td>11</td><td>14.86</td><td></td><td></td></tr><tr><td>0x0003517f:2</td><td></td><td></td><td></td><td>transform_tree(2428, 980, 2, 1)</td><td>38</td><td>51.35</td><td></td><td></td></tr><tr><td colspan="9">0x0003518d:0 residual_coding(2424, 976, 3, 1) 3 4.05</td></tr><tr><td colspan="9">0x0003518d:3 residual_coding(2424, 976, 3, 2) 5 6.76</td></tr></tbody></table></div><div style="margin-bottom: 10px;">Selection info 616 <div style="font-size: 0.7em; margin-bottom: 5px;">Width: 3840 CTB address: 937 PU shape: 2Nx2N Height: 2160 CTB col, row: 37,15 PU size: 4x4 Pictures: 720 CU x/y: 2424, 976 TU depth: 1 Color format: 4:2:0 CU Size/Depth: 8x8, 3 TU size: 4x4 Bisdepth Y,C: 10, 10 CU pred mode: Intra MV L0: N/A Tile col, row: 0,0 Pixel x/y: 2424, 976 MV L1: N/A Slice #: 0-1 4x4 2-scan idx: 116 QpT/QpCb/QpCr: 14/14/14</div></div><div style="margin-bottom: 10px;"><div style="display: flex; justify-content: space-between; font-size: 0.7em;">MP4 NAL VPS SPS PPS Slice SEI CU TU QM Ref/Lists Stats HRDRight-click selection for details</div><div style="font-size: 0.7em; margin-top: 5px;">Unit Info CU at x,y 2424, 976 Total bits: 76 (10 bytes) Total bins: 96 (1.263 bins per bit) Bypass bins: 33 (34.4%) Starting at position [byte:bits] 5108269:4 (0x4df22d:4) in file: (4) 8a 3e 56 1b ca f5 ee dd 01 ea (7)</div><div style="display: flex; justify-content: space-between; font-size: 0.7em; margin-top: 5px;">Unit Info Hex View QP8 infoStatus</div><div style="font-size: 0.7em; margin-top: 5px;"><div>done. Decoding picture 23 ... done. Decoding picture 22 ... done. Decoding picture 18 ... done.</div><div style="font-size: 0.6em; margin-top: 5px;">Errors Status</div></div><div style="font-size: 0.7em; margin-top: 5px; text-align: right;">1151MB / 2257MB / 8191MB</div></div></div>	Filter	Pos	R	V	SE Name	Value	Bits	Bits %	Decoding t	0x0003517b:4 coding_unit(2424, 976, 3) 76 100.00									0x0003517b:4	508	320		part_mode	1	0	0.00	Arithmetic	0x0003517b:4 prediction_unit(2424, 976, 8, 8) 2 2.63									0x0003517b:4	499	320		prev_intra_luma_pred_flag	1	0	0.00	Arithmetic	0x0003517b:4	341	320		mpm_idx	2	2	100.00	Bypass	0x0003517b:6	341	259		intra_chroma_pred_mode	4	0	0.00	Arithmetic	0x0003517b:6 split_transform_flag 74 97.37									0x0003517b:6	334	259		split_transform_flag	1	2	2.70	Arithmetic	0x0003517c:0	376	78		cbf_cb	1	0	0.00	Arithmetic	0x0003517c:0	307	78		cbf_cr	1	1	1.35	Arithmetic	0x0003517c:1 transform_tree(2424, 976, 2, 1) 10 13.51									0x0003517d:3				transform_tree(2428, 976, 2, 1)	4	5.41			0x0003517d:7				transform_tree(2424, 980, 2, 1)	11	14.86			0x0003517f:2				transform_tree(2428, 980, 2, 1)	38	51.35			0x0003518d:0 residual_coding(2424, 976, 3, 1) 3 4.05									0x0003518d:3 residual_coding(2424, 976, 3, 2) 5 6.76								
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EXHIBIT 20
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U.S. PATENT NO. 9,036,701

HISENSE ACCUSED PRODUCTS

Syntax Info | 616

Pos	R	V	SE Name	Value	Bits	Bits, %	Decoding type	Ctx Idx
0x0003517c:1	508	156	cbf_luma	1	0	0.00	Arithmetic	0
0x0003517c:1			transform_unit(2424, 976, 2, 1)	10	100.00			
0x0003517c:1			> delta_qp0	0	0.00			
0x0003517c:1			residual_coding(2424, 976, 2, 0)	10	100.00			
0x0003517c:1	490	156	transform_skip_flag	0	0	0.00	Arithmetic	0
0x0003517c:1	481	156	last_sig_coeff_x_prefix	1	2	20.00	Arithmetic	0
0x0003517c:3	480	141	last_sig_coeff_y_prefix	1	1	10.00	Arithmetic	0
0x0003517c:4	334	283	sig_coeff_flag	0	2	20.00	Arithmetic	6
0x0003517c:6	488	287	sig_coeff_flag	0	1	10.00	Arithmetic	1
0x0003517c:7	432	31	sig_coeff_flag	1	0	0.00	Arithmetic	2
0x0003517c:7	337	31	sig_coeff_flag	1	0	0.00	Arithmetic	0
0x0003517c:7	261	31	coeff_abs_level_greater1_flag	0	1	10.00	Arithmetic	1
0x0003517d:0	440	62	coeff_abs_level_greater1_flag	0	0	0.00	Arithmetic	2
0x0003517d:0	359	62	coeff_abs_level_greater1_flag	0	0	0.00	Arithmetic	3
0x0003517d:0	279	62	coeff_sign_flag	0	1	10.00	Bypass	
0x0003517d:1	279	124	coeff_sign_flag	0	1	10.00	Bypass	
0x0003517d:2	279	249	coeff_sign_flag	1	1	10.00	Bypass	

Selection Info | 616

Width: 3840	CTB address: 937	PU shape: 2Nx2N
Height: 2160	CTB col, row: 37,15	PU size: N/A
Pictures: 720	CU X,Y: 2424, 976	TU depth: 1
Color format: 4:2:0	CU Size,Depth: 8x8, 3	TU size: 4x4
Bitdepth Y,C: 10, 10	CU pred mode: Intra	MV L0: N/A
Tile col, row: 0,0	Pixel X,Y: 2424,976	MV L1: N/A
Slice #: 0 - 1	4x4 Z-scan idx: 116	QpY/QpCb/QpCr: 14/14/14

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

CU [2424,976] includes transform block [2424,976], which has 3 non-zero transform coefficients.

Source: Screenshot of VQ Analyzer software analyzing video played back on Hisense 43A7N.

CU [2424,976] includes transform block [2424,976], which has 3 non-zero transform coefficients.

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	<div><div>Transform block (2424,976) details</div><div><div>Syntax Info 616</div><div><div>Filter</div><div>Hex</div><table><tr><th>Pos</th><th>R</th><th>V</th><th>SE Name</th><th>Value</th><th>Bits</th><th>Bits, %</th><th>Decoding type</th><th>Ctx Idx</th></tr><tr><td>0x0003517c:1</td><td>508</td><td>156</td><td>cbf_luma</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>0</td></tr><tr><td>0x0003517c:1</td><td></td><td></td><td>transform_unit(2424, 976, 2, 1)</td><td>10</td><td>100.00</td><td></td><td></td><td></td></tr><tr><td>0x0003517c:1</td><td></td><td></td><td>> delta_qp0</td><td>0</td><td>0.00</td><td></td><td></td><td></td></tr><tr><td>0x0003517c:1</td><td></td><td></td><td>residual_coding(2424, 976, 2, 0)</td><td>10</td><td>100.00</td><td></td><td></td><td></td></tr><tr><td>0x0003517c:1</td><td>490</td><td>156</td><td>transform_skip_flag</td><td>0</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>0</td></tr><tr><td>0x0003517c:1</td><td>481</td><td>156</td><td>last_sig_coeff_x_prefix</td><td>1</td><td>2</td><td>20.00</td><td>Arithmetic</td><td>0</td></tr><tr><td>0x0003517c:3</td><td>480</td><td>141</td><td>last_sig_coeff_y_prefix</td><td>1</td><td>1</td><td>10.00</td><td>Arithmetic</td><td>0</td></tr><tr><td>0x0003517c:4</td><td>334</td><td>283</td><td>sig_coeff_flag</td><td>0</td><td>2</td><td>20.00</td><td>Arithmetic</td><td>6</td></tr><tr><td>0x0003517c:6</td><td>488</td><td>287</td><td>sig_coeff_flag</td><td>0</td><td>1</td><td>10.00</td><td>Arithmetic</td><td>1</td></tr><tr><td>0x0003517c:7</td><td>432</td><td>31</td><td>sig_coeff_flag</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>2</td></tr><tr><td>0x0003517c:7</td><td>337</td><td>31</td><td>sig_coeff_flag</td><td>1</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>0</td></tr><tr><td>0x0003517c:7</td><td>261</td><td>31</td><td>coeff_abs_level_greater1_flag</td><td>0</td><td>1</td><td>10.00</td><td>Arithmetic</td><td>1</td></tr><tr><td>0x0003517d:0</td><td>440</td><td>62</td><td>coeff_abs_level_greater1_flag</td><td>0</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>2</td></tr><tr><td>0x0003517d:0</td><td>359</td><td>62</td><td>coeff_abs_level_greater1_flag</td><td>0</td><td>0</td><td>0.00</td><td>Arithmetic</td><td>3</td></tr><tr><td>0x0003517d:0</td><td>279</td><td>62</td><td>coeff_sign_flag</td><td>0</td><td>1</td><td>10.00</td><td>Bypass</td><td></td></tr><tr><td>0x0003517d:1</td><td>279</td><td>124</td><td>coeff_sign_flag</td><td>0</td><td>1</td><td>10.00</td><td>Bypass</td><td></td></tr><tr><td>0x0003517d:2</td><td>279</td><td>249</td><td>coeff_sign_flag</td><td>1</td><td>1</td><td>10.00</td><td>Bypass</td><td></td></tr></table></div></div></div>	Pos	R	V	SE Name	Value	Bits	Bits, %	Decoding type	Ctx Idx	0x0003517c:1	508	156	cbf_luma	1	0	0.00	Arithmetic	0	0x0003517c:1			transform_unit(2424, 976, 2, 1)	10	100.00				0x0003517c:1			> delta_qp0	0	0.00				0x0003517c:1			residual_coding(2424, 976, 2, 0)	10	100.00				0x0003517c:1	490	156	transform_skip_flag	0	0	0.00	Arithmetic	0	0x0003517c:1	481	156	last_sig_coeff_x_prefix	1	2	20.00	Arithmetic	0	0x0003517c:3	480	141	last_sig_coeff_y_prefix	1	1	10.00	Arithmetic	0	0x0003517c:4	334	283	sig_coeff_flag	0	2	20.00	Arithmetic	6	0x0003517c:6	488	287	sig_coeff_flag	0	1	10.00	Arithmetic	1	0x0003517c:7	432	31	sig_coeff_flag	1	0	0.00	Arithmetic	2	0x0003517c:7	337	31	sig_coeff_flag	1	0	0.00	Arithmetic	0	0x0003517c:7	261	31	coeff_abs_level_greater1_flag	0	1	10.00	Arithmetic	1	0x0003517d:0	440	62	coeff_abs_level_greater1_flag	0	0	0.00	Arithmetic	2	0x0003517d:0	359	62	coeff_abs_level_greater1_flag	0	0	0.00	Arithmetic	3	0x0003517d:0	279	62	coeff_sign_flag	0	1	10.00	Bypass		0x0003517d:1	279	124	coeff_sign_flag	0	1	10.00	Bypass		0x0003517d:2	279	249	coeff_sign_flag	1	1	10.00	Bypass		<div>Y Levels (2424,976)</div> <div></div>
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<div>[b] categorizing a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold, wherein syntax elements which occur greater</div>	<div>Each of the Accused Products, such as the Hisense 43A7N, performs a method comprising categorizing a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category.</div> <div>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising</div>																																																																																																																																																																			

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than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category;	<p>categorizing a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category.</p> <p>The following specifications provide further evidence of how each of the Accused Products operates:</p>

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	<p>7.3.8.11 Residual coding syntax</p> <table border="1"> <thead> <tr> <th></th><th>Descriptor</th></tr> </thead> <tbody> <tr> <td>residual_coding(x0, y0, log2TrafoSize, cIdx) {</td><td></td></tr> <tr> <td>if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))</td><td></td></tr> <tr> <td>transform_skip_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>if(CuPredMode[x0][y0] == MODE_INTER && explicit_rdpem_enabled_flag && (transform_skip_flag[x0][y0][cIdx] cu_transquant_bypass_flag)) {</td><td></td></tr> <tr> <td>explicit_rdpem_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>if(explicit_rdpem_flag[x0][y0][cIdx])</td><td></td></tr> <tr> <td>explicit_rdpem_dir_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>}</td><td></td></tr> <tr> <td>last_sig_coeff_x_prefix</td><td>ae(v)</td></tr> <tr> <td>last_sig_coeff_y_prefix</td><td>ae(v)</td></tr> <tr> <td>if(last_sig_coeff_x_prefix > 3)</td><td></td></tr> <tr> <td>last_sig_coeff_x_suffix</td><td>ae(v)</td></tr> <tr> <td>if(last_sig_coeff_y_prefix > 3)</td><td></td></tr> <tr> <td>last_sig_coeff_y_suffix</td><td>ae(v)</td></tr> <tr> <td>lastScanPos = 16</td><td></td></tr> <tr> <td>lastSubBlock = (1 << (log2TrafoSize - 2)) * (1 << (log2TrafoSize - 2)) - 1</td><td></td></tr> <tr> <td>do {</td><td></td></tr> <tr> <td>if(lastScanPos == 0) {</td><td></td></tr> </tbody> </table>		Descriptor	residual_coding(x0, y0, log2TrafoSize, cIdx) {		if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))		transform_skip_flag [x0][y0][cIdx]	ae(v)	if(CuPredMode[x0][y0] == MODE_INTER && explicit_rdpem_enabled_flag && (transform_skip_flag[x0][y0][cIdx] cu_transquant_bypass_flag)) {		explicit_rdpem_flag [x0][y0][cIdx]	ae(v)	if(explicit_rdpem_flag[x0][y0][cIdx])		explicit_rdpem_dir_flag [x0][y0][cIdx]	ae(v)	}		last_sig_coeff_x_prefix	ae(v)	last_sig_coeff_y_prefix	ae(v)	if(last_sig_coeff_x_prefix > 3)		last_sig_coeff_x_suffix	ae(v)	if(last_sig_coeff_y_prefix > 3)		last_sig_coeff_y_suffix	ae(v)	lastScanPos = 16		lastSubBlock = (1 << (log2TrafoSize - 2)) * (1 << (log2TrafoSize - 2)) - 1		do {		if(lastScanPos == 0) {	
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	lastScanPos = 16	
	lastSubBlock--	
	}	
	lastScanPos--	
	xS = ScanOrder[log2TrafoSize - 2][scanIdx][lastSubBlock][0]	
	yS = ScanOrder[log2TrafoSize - 2][scanIdx][lastSubBlock][1]	
	xC = (xS << 2) + ScanOrder[2][scanIdx][lastScanPos][0]	
	yC = (yS << 2) + ScanOrder[2][scanIdx][lastScanPos][1]	
	} while((xC != LastSignificantCoeffX) (yC != LastSignificantCoeffY))	
	for(i = lastSubBlock; i >= 0; i--) {	
	xS = ScanOrder[log2TrafoSize - 2][scanIdx][i][0]	
	yS = ScanOrder[log2TrafoSize - 2][scanIdx][i][1]	
	escapeDataPresent = 0	
	inferSbDcSigCoeffFlag = 0	
	if((i < lastSubBlock) && (i > 0)) {	
	coded_sub_block_flag [xS][yS]	ae(v)
	inferSbDcSigCoeffFlag = 1	
	}	
	for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {	
	xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]	
	yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]	
	if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {	
	sig_coeff_flag [xC][yC]	ae(v)
	if(sig_coeff_flag[xC][yC])	
	inferSbDcSigCoeffFlag = 0	
	}	

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	<table> <tr><td>}</td><td></td><td></td></tr> <tr><td>firstSigScanPos = 16</td><td></td><td></td></tr> <tr><td>lastSigScanPos = -1</td><td></td><td></td></tr> <tr><td>numGreater1Flag = 0</td><td></td><td></td></tr> <tr><td>lastGreater1ScanPos = -1</td><td></td><td></td></tr> <tr><td>for(n = 15; n >= 0; n--) {</td><td></td><td></td></tr> <tr><td> xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]</td><td></td><td></td></tr> <tr><td> yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]</td><td></td><td></td></tr> <tr><td> if(sig_coeff_flag[xC][yC]) {</td><td></td><td></td></tr> <tr><td> if(numGreater1Flag < 8) {</td><td></td><td></td></tr> <tr><td> coeff_abs_level_greater1_flag[n]</td><td></td><td>ae(v)</td></tr> <tr><td> numGreater1Flag++</td><td></td><td></td></tr> <tr><td> if(coeff_abs_level_greater1_flag[n] && lastGreater1ScanPos == -1)</td><td></td><td></td></tr> <tr><td> lastGreater1ScanPos = n</td><td></td><td></td></tr> <tr><td> else if(coeff_abs_level_greater1_flag[n])</td><td></td><td></td></tr> <tr><td> escapeDataPresent = 1</td><td></td><td></td></tr> <tr><td> } else</td><td></td><td></td></tr> <tr><td> escapeDataPresent = 1</td><td></td><td></td></tr> </table>		}			firstSigScanPos = 16			lastSigScanPos = -1			numGreater1Flag = 0			lastGreater1ScanPos = -1			for(n = 15; n >= 0; n--) {			xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]			yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]			if(sig_coeff_flag[xC][yC]) {			if(numGreater1Flag < 8) {			coeff_abs_level_greater1_flag[n]		ae(v)	numGreater1Flag++			if(coeff_abs_level_greater1_flag[n] && lastGreater1ScanPos == -1)			lastGreater1ScanPos = n			else if(coeff_abs_level_greater1_flag[n])			escapeDataPresent = 1			} else			escapeDataPresent = 1		
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	if(lastSigScanPos == -1)	
	lastSigScanPos = n	
	firstSigScanPos = n	
	}	
	}	
	if(cu_transquant_bypass_flag (CuPredMode[x0][y0] == MODE_INTRA && implicit_rdpdm_enabled_flag && transform_skip_flag[x0][y0][cIdx] && (predModeIntra == 10 predModeIntra == 26)) explicit_rdpdm_flag[x0][y0][cIdx])	
	signHidden = 0	
	else	
	signHidden = lastSigScanPos – firstSigScanPos > 3	
	if(lastGreater1ScanPos != -1) {	
	coeff_abs_level_greater2_flag[lastGreater1ScanPos]	ae(v)
	if(coeff_abs_level_greater2_flag[lastGreater1ScanPos])	
	escapeDataPresent = 1	
	}	

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		for(n = 15; n >= 0; n--) {	
		xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]	
		yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]	
		if(sig_coeff_flag[xC][yC] && (!sign_data_hiding_enabled_flag !signHidden (n != firstSigScanPos)))	
		coeff_sign_flag[n]	ae(v)
		}	

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	<pre> numSigCoeff = 0 sumAbsLevel = 0 for(n = 15; n >= 0; n--) { xC = (xS << 2) + ScanOrder[2][scanIdx][n][0] yC = (yS << 2) + ScanOrder[2][scanIdx][n][1] if(sig_coeff_flag[xC][yC]) { baseLevel = 1 + coeff_abs_level_greater1_flag[n] + coeff_abs_level_greater2_flag[n] if(baseLevel == ((numSigCoeff < 8) ? ((n == lastGreater1ScanPos) ? 3 : 2) : 1)) coeff_abs_level_remaining[n] TransCoeffLevel[x0][y0][cIdx][xC][yC] = (coeff_abs_level_remaining[n] + baseLevel) * (1 - 2 * coeff_sign_flag[n]) if(sign_data_hiding_enabled_flag && signHidden) { sumAbsLevel += (coeff_abs_level_remaining[n] + baseLevel) if((n == firstSigScanPos) && ((sumAbsLevel % 2) == 1)) TransCoeffLevel[x0][y0][cIdx][xC][yC] = -TransCoeffLevel[x0][y0][cIdx][xC][yC] } } numSigCoeff++ } } } } } </pre>
	<p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 58-60.</p> <p>As set out in the Residual Coding Syntax in section 7.3.8.11, an H.265 compliant decoder parses <i>sig_coeff_flags</i> from the bit stream according to the logic reproduced below.</p>

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	<table> <tr> <td>for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {</td><td></td></tr> <tr> <td>xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]</td><td></td></tr> <tr> <td>yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]</td><td></td></tr> <tr> <td>if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {</td><td></td></tr> <tr> <td>sig_coeff_flag[xC][yC]</td><td>ae(v)</td></tr> <tr> <td>if(sig_coeff_flag[xC][yC])</td><td></td></tr> <tr> <td>inferSbDcSigCoeffFlag = 0</td><td></td></tr> <tr> <td>}</td><td></td></tr> </table> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 59.</p> <p>7.4.9.11 Residual coding semantics</p> <p>...</p> <p>sig_coeff_flag[xC][yC] specifies for the transform coefficient location (xC, yC) within the current transform block whether the corresponding transform coefficient level at the location (xC, yC) is non-zero as follows:</p> <ul style="list-style-type: none"> – If sig_coeff_flag[xC][yC] is equal to 0, the transform coefficient level at the location (xC, yC) is set equal to 0. – Otherwise (sig_coeff_flag[xC][yC] is equal to 1), the transform coefficient level at the location (xC, yC) has a non-zero value. <p>When sig_coeff_flag[xC][yC] is not present, it is inferred as follows:</p> <ul style="list-style-type: none"> – If (xC, yC) is the last significant location (LastSignificantCoeffX, LastSignificantCoeffY) in scan order or all of the following conditions are true, sig_coeff_flag[xC][yC] is inferred to be equal to 1: <ul style="list-style-type: none"> – (xC & 3, yC & 3) is equal to (0, 0). – inferSbDcSigCoeffFlag is equal to 1. 	for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {		xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]		yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]		if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {		sig_coeff_flag[xC][yC]	ae(v)	if(sig_coeff_flag[xC][yC])		inferSbDcSigCoeffFlag = 0		}	
for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {																	
xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]																	
yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]																	
if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {																	
sig_coeff_flag[xC][yC]	ae(v)																
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inferSbDcSigCoeffFlag = 0																	
}																	

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	<ul style="list-style-type: none"> – coded_sub_block_flag[xS][yS] is equal to 1. – Otherwise, sig_coeff_flag[xC][yC] is inferred to be equal to 0. ... <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 111.</p> <p>9.3.4.2 Derivation process for ctxTable, ctxIdx and bypassFlag</p> <p>9.3.4.2.1 General</p> <p>Input to this process is the position of the current bin within the bin string, binIdx.</p> <p>Outputs of this process are ctxTable, ctxIdx and bypassFlag.</p> <p>The values of ctxTable, ctxIdx and bypassFlag are derived as follows based on the entries for binIdx of the corresponding syntax element in Table 9-48:</p> <ul style="list-style-type: none"> – If the entry in Table 9-48 is not equal to "bypass", "terminate" or "na", the values of binIdx are decoded by invoking the DecodeDecision process as specified in clause 9.3.4.3.2 and the following applies: <ul style="list-style-type: none"> – ctxTable is specified in Table 9-4. – The variable ctxInc is specified by the corresponding entry in Table 9-48 and when more than one value is listed in Table 9-48 for a binIdx, the assignment process for ctxInc for that binIdx is further specified in the clauses given in parenthesis. – The variable ctxIdxOffset is specified by the lowest value of ctxIdx in Table 9-4 depending on the current value of initType. – ctxIdx is set equal to the sum of ctxInc and ctxIdxOffset. – bypassFlag is set equal to 0. – Otherwise, if the entry in Table 9-48 is equal to "bypass", the values of binIdx are decoded by invoking the DecodeBypass process as specified in clause 9.3.4.3.4 and the following applies:

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	<ul style="list-style-type: none">– ctxTable is set equal to 0.– ctxIdx is set equal to 0.– bypassFlag is set equal to 1.																																																
	ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 225.																																																
	Table 9-48 – Assignment of ctxInc to syntax elements with context coded bins																																																
	<table><tr><th rowspan="2">Syntax element</th><th colspan="6">binIdx</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>>= 5</th></tr><tr><td>...</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>sig_coeff_flag[][]</td><td>0..43 (clause 9.3.4.2.5)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater1_flag[]</td><td>0..23 (clause 9.3.4.2.6)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater2_flag[]</td><td>0..5 (clause 9.3.4.2.7)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_remaining[]</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td></tr></table>	Syntax element	binIdx						0	1	2	3	4	>= 5	...							sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na	coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na	coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na	coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass
	Syntax element		binIdx																																														
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...																																																	
sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na																																											
coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na																																											
coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na																																											
coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass																																											
	ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 225-227.																																																
[c] entropy coding symbols that correspond to the first category of syntax elements and that have been subjected to a context update; and	Each of the Accused Products, such as the Hisense 43A7N, performs a method comprising entropy coding symbols that correspond to the first category of syntax elements and that have been subjected to a context update.																																																

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	<p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising entropy coding symbols that correspond to the first category of syntax elements and that have been subjected to a context update.</p> <p>The following specifications provide further evidence of how each of the Accused Products operates:</p> <p>9.3.4.2 Derivation process for ctxTable, ctxIdx and bypassFlag</p> <p>9.3.4.2.1 General</p> <p>Input to this process is the position of the current bin within the bin string, binIdx.</p> <p>Outputs of this process are ctxTable, ctxIdx and bypassFlag.</p> <p>The values of ctxTable, ctxIdx and bypassFlag are derived as follows based on the entries for binIdx of the corresponding syntax element in Table 9-48:</p> <ul style="list-style-type: none"> – If the entry in Table 9-48 is not equal to "bypass", "terminate" or "na", the values of binIdx are decoded by invoking the DecodeDecision process as specified in clause 9.3.4.3.2 and the following applies: <ul style="list-style-type: none"> – ctxTable is specified in Table 9-4. – The variable ctxInc is specified by the corresponding entry in Table 9-48 and when more than one value is listed in Table 9-48 for a binIdx, the assignment process for ctxInc for that binIdx is further specified in the clauses given in parenthesis. – The variable ctxIdxOffset is specified by the lowest value of ctxIdx in Table 9-4 depending on the current value of initType. – ctxIdx is set equal to the sum of ctxInc and ctxIdxOffset. – bypassFlag is set equal to 0. ... <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 225.</p>

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	<p>9.3.4.3 Arithmetic decoding process</p> <p>9.3.4.3.1 General</p> <p>Inputs to this process are ctxTable, ctxIdx and bypassFlag, as derived in clause 9.3.4.2, and the state variables ivlCurrRange and ivlOffset of the arithmetic decoding engine.</p> <p>Output of this process is the value of the bin.</p> <p>Figure 9-5 illustrates the whole arithmetic decoding process for a single bin. For decoding the value of a bin, the context index table ctxTable and the ctxIdx are passed to the arithmetic decoding process DecodeBin(ctxTable, ctxIdx), which is specified as follows:</p> <ul style="list-style-type: none"> – If bypassFlag is equal to 1, DecodeBypass() as specified in clause 9.3.4.3.4 is invoked. – Otherwise, if bypassFlag is equal to 0, ctxTable is equal to 0 and ctxIdx is equal to 0, DecodeTerminate() as specified in clause 9.3.4.3.5 is invoked. – Otherwise (bypassFlag is equal to 0 and ctxTable is not equal to 0), DecodeDecision() as specified in clause 9.3.4.3.2 is invoked. <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 232.</p> <p>9.3.4.2.6 Derivation process of ctxInc for the syntax element coeff_abs_level_greater1_flag</p> <p>Inputs to this process are the colour component index cIdx, the current sub-block scan index i and the current coefficient scan index n within the current sub-block.</p> <p>Output of this process is the variable ctxInc.</p> <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p 231.</p> <p>9.3.4.2.7 Derivation process of ctxInc for the syntax element coeff_abs_level_greater2_flag</p>

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	<p>Inputs to this process are the colour component index cldx, the current sub-block scan index i and the current coefficient scan index n within the current sub-block.</p> <p>Output of this process is the variable ctxInc.</p> <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 232.</p> <p>For example, the symbols that correspond to the first category of syntax elements and that have been subjected to a context update are the coeff_abs_level_greater1_flag, and coeff_abs_level_greater2_flag that are used to represent, at least in part, the <i>non-zero transform coefficient levels</i> in the first category, as shown in Table 9-48 and described in section 9.3.2.5 of the H.265 Standard reproduced below, in which the process for calculating the context for each of coeff_abs_level_greater1_flag and coeff_abs_level_greater2_flag is provided.</p> <p style="text-align: center;">Table 9-48 – Assignment of ctxInc to syntax elements with context coded bins</p> <table><tr><th rowspan="2">Syntax element</th><th colspan="6">binIdx</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>>= 5</th></tr><tr><td>...</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>sig_coeff_flag[][]</td><td>0..43 (clause 9.3.4.2.5)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater1_flag[]</td><td>0..23 (clause 9.3.4.2.6)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater2_flag[]</td><td>0..5 (clause 9.3.4.2.7)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_remaining[]</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td></tr></table> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 225-227.</p>	Syntax element	binIdx						0	1	2	3	4	>= 5	...							sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na	coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na	coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na	coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass
Syntax element	binIdx																																																
	0	1	2	3	4	>= 5																																											
...																																																	
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coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na																																											
coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass																																											

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	<p>9.3.2.5 Synchronization process for context variables, Rice parameter initialization states, and palette predictor variables</p> <p>Inputs to this process are:</p> <ul style="list-style-type: none"> – The variables tableStateSync and tableMPSSync containing the values of the variables pStateIdx and valMps used in the storage process of context variables that are assigned to all syntax elements in clauses 7.3.8.1 through 7.3.8.12, except end_of_slice_segment_flag, end_of_subset_one_bit and pcm_flag. – The variable tableStatCoeffSync containing the values of the variables StatCoeff[k] used in the storage process of context variables and Rice parameter initialization states. – The variables PredictorPaletteSizeSync and tablePredictorPaletteEntriesSync containing the values used in the storage process of palette predictor variables. <p>Outputs of this process are:</p> <ul style="list-style-type: none"> – The initialized CABAC context variables indexed by ctxTable and ctxIdx. – The initialized Rice parameter initialization states StatCoeff indexed by k. – The palette predictor variables, PredictorPaletteSize and PredictorPaletteEntries. <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 215.</p>
<p>[d] entropy coding symbols that correspond to the second category of syntax elements and that have bypassed context updating.</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method comprising entropy coding symbols that correspond to the second category of syntax elements and that have bypassed context updating.</p> <p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising entropy coding symbols that correspond to the second category of syntax elements and that have bypassed context updating.</p>

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	<p>The following specifications provide further evidence of how each of the Accused Products operates:</p> <p>9.3.4.2 Derivation process for ctxTable, ctxIdx and bypassFlag</p> <p>9.3.4.2.1 General</p> <p>Input to this process is the position of the current bin within the bin string, binIdx.</p> <p>Outputs of this process are ctxTable, ctxIdx and bypassFlag.</p> <p>The values of ctxTable, ctxIdx and bypassFlag are derived as follows based on the entries for binIdx of the corresponding syntax element in Table 9-48:</p> <p>...</p> <ul style="list-style-type: none">– Otherwise, if the entry in Table 9-48 is equal to "bypass", the values of binIdx are decoded by invoking the DecodeBypass process as specified in clause 9.3.4.3.4 and the following applies:<ul style="list-style-type: none">– ctxTable is set equal to 0.– ctxIdx is set equal to 0.– bypassFlag is set equal to 1. <p>...</p> <p style="text-align: center;">Table 9-48 – Assignment of ctxInc to syntax elements with context coded bins</p> <table><tr><th rowspan="2">Syntax element</th><th colspan="6">binIdx</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>>= 5</th></tr><tr><td>...</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>...</p>	Syntax element	binIdx						0	1	2	3	4	>= 5	...						
Syntax element	binIdx																				
	0	1	2	3	4	>= 5															
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	sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na
	coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na
	coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na
	coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass
<p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 225-227.</p> <p>9.3.4.3 Arithmetic decoding process</p> <p>9.3.4.3.1 General</p> <p>Inputs to this process are ctxTable, ctxIdx and bypassFlag, as derived in clause 9.3.4.2, and the state variables ivlCurrRange and ivlOffset of the arithmetic decoding engine.</p> <p>Output of this process is the value of the bin.</p> <p>Figure 9-5 illustrates the whole arithmetic decoding process for a single bin. For decoding the value of a bin, the context index table ctxTable and the ctxIdx are passed to the arithmetic decoding process DecodeBin(ctxTable, ctxIdx), which is specified as follows:</p> <ul style="list-style-type: none"> – If bypassFlag is equal to 1, DecodeBypass() as specified in clause 9.3.4.3.4 is invoked. – Otherwise, if bypassFlag is equal to 0, ctxTable is equal to 0 and ctxIdx is equal to 0, DecodeTerminate() as specified in clause 9.3.4.3.5 is invoked. – Otherwise (bypassFlag is equal to 0 and ctxTable is not equal to 0), DecodeDecision() as specified in clause 9.3.4.3.2 is invoked. <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 232.</p>							

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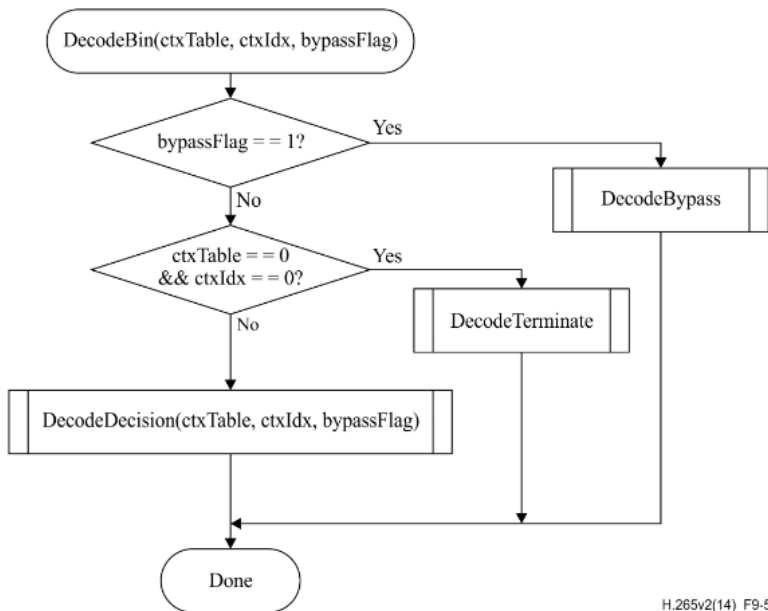
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	 <pre> graph TD Start([DecodeBin(ctxTable, ctxIdx, bypassFlag)]) --> D1{bypassFlag == 1?} D1 -- Yes --> DB[DecodeBypass] D1 -- No --> D2{ctxTable == 0 && ctxIdx == 0?} D2 -- Yes --> DT[DecodeTerminate] D2 -- No --> DD[DecodeDecision(ctxTable, ctxIdx, bypassFlag)] DB --> Done([Done]) DT --> Done DD --> Done </pre> <p style="text-align: right; font-size: small;">H.265v2(14)_F9-5</p> <p>Figure 9-5 – Overview of the arithmetic decoding process for a single bin (informative)</p> <p>NOTE – Arithmetic coding is based on the principle of recursive interval subdivision. Given a probability estimation $p(0)$ and $p(1) = 1 - p(0)$ of a binary decision $(0, 1)$, an initially given code sub-interval with the range $ivlCurrRange$ will be subdivided into two sub-intervals having range $p(0) * ivlCurrRange$ and $ivlCurrRange - p(0) * ivlCurrRange$, respectively. Depending on the decision, which has been observed, the corresponding sub-interval will be chosen as the new code interval, and a binary code string pointing into that interval will represent the sequence of observed binary decisions. It is useful to distinguish between the most probable symbol (MPS) and the least probable symbol (LPS), so that binary decisions have to be identified as either MPS or LPS, rather than 0 or 1. Given this terminology, each context is specified by the probability $pLPS$ of the LPS and the value of MPS ($valMps$), which is either 0 or 1. The arithmetic core engine in this Specification has three distinct properties:</p>

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	<ul style="list-style-type: none"> – The probability estimation is performed by means of a finite-state machine with a table-based transition process between 64 different representative probability states $\{ pLPS(pStateIdx) \mid 0 \leq pStateIdx < 64 \}$ for the LPS probability pLPS. The numbering of the states is arranged in such a way that the probability state with index $pStateIdx = 0$ corresponds to an LPS probability value of 0.5, with decreasing LPS probability towards higher state indices. – The range $ivlCurrRange$ representing the state of the coding engine is quantized to a small set $\{Q1,...,Q4\}$ of pre-set quantization values prior to the calculation of the new interval range. Storing a table containing all 64×4 pre-computed product values of $Q_i * pLPS(pStateIdx)$ allows a multiplication-free approximation of the product $ivlCurrRange * pLPS(pStateIdx)$. – For syntax elements or parts thereof for which an approximately uniform probability distribution is assumed to be given a separate simplified encoding and decoding bypass process is used. <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 233.</p>

2. Claim 3

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3. Pre A method according to claim 1 further comprising	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1.</p> <p>The evidence cited for Claim 1 applies to this claim limitation.</p>
[a] performing binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1 further comprising performing binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating.</p> <p>The evidence cited for Claim 1 applies to this claim limitation.</p>

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	<p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method according to claim 1 further comprising performing binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating.</p> <p>The following specifications provide further evidence of how each of the Accused Products operates:</p> <p>9.3 CABAC parsing for slice segment data</p> <p>9.3.1 General</p> <p>This process is invoked when parsing syntax elements with descriptor ae(v) in clauses 7.3.8.1 through 7.3.8.12.</p> <p>Inputs to this process are a request for a value of a syntax element and value of prior parsed syntax elements.</p> <p>Outputs of this process is the value of the syntax element</p> <p>...</p> <p>For each requested value of a syntax element a binarization is derived as specified in clause 9.3.3.</p> <p>The binarization for the syntax element and the sequence of parsed bins determines the decoding process flow as described in clause 9.3.4.</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 201.</p> <p>9.3.3 Binarization process</p> <p>9.3.3.1 General</p> <p>Inputs to this process is a request for syntax element.</p> <p>Output of this process is the binarization of the syntax element.</p>

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	<p>Table 9-43 specifies the type of binarization process associated with each syntax element and corresponding inputs.</p> <p>The specification of the truncated Rice (TR) binarization process, the k-th order Exp-Golomb (EGk) binarization process, limited k-th order Exp-Golomb (EGk) binarization process, the fixed-length (FL) binarization process, and the truncated binary binarization process are given in clauses 9.3.3.2 through 9.3.3.6, respectively. Other binarizations are specified in clauses 9.3.3.7 through 9.3.3.14.</p> <p>...</p>

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	Table 9-43 – Syntax elements and associated binarizations		
	Syntax structure	Syntax element	<div>Binarization</div> <div><div>Process</div><div>Input parameters</div></div>
	cross_comp_pred()	log2_res_scale_abs_plus1	TR cMax = 4, cRiceParam = 0
		res_scale_sign_flag	FL cMax = 1
	residual_coding()	transform_skip_flag[][]	FL cMax = 1
		explicit_rdpem_flag[][]	FL cMax = 1
		explicit_rdpem_dir_flag[][]	FL cMax = 1
		last_sig_coeff_x_prefix	TR cMax = (log2TrafoSize << 1) - 1, cRiceParam = 0
		last_sig_coeff_y_prefix	TR cMax = (log2TrafoSize << 1) - 1, cRiceParam = 0
		last_sig_coeff_x_suffix	FL cMax = (1 << ((last_sig_coeff_x_prefix >> 1) - 1) - 1)
		last_sig_coeff_y_suffix	FL cMax = (1 << ((last_sig_coeff_y_prefix >> 1) - 1) - 1)
		coded_sub_block_flag[][]	FL cMax = 1
		sig_coeff_flag[][]	FL cMax = 1
		coeff_abs_level_greater1_flag[]	FL cMax = 1
		coeff_abs_level_greater2_flag[]	FL cMax = 1
		coeff_abs_level_remaining[]	9.3.3.11 current sub-block scan index i, baseLevel
		coeff_sign_flag[]	FL cMax = 1

ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 216-218.

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	<p>9.3.4 Decoding process flow</p> <p>9.3.4.1 General</p> <p>Inputs to this process are all bin strings of the binarization of the requested syntax element as specified in clause 9.3.3.</p> <p>Output of this process is the value of the syntax element.</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 225.</p>

3. Claim 4

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4. Pre A method according to claim 3	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 3.</p> <p>The evidence cited for claims 1 and 3 applies to this limitation.</p>
[a] wherein performing binarization comprises performing binarization so as to target a predetermined probability.	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 3 wherein performing binarization comprises performing binarization so as to target a predetermined probability.</p> <p>The evidence cited for Claim 1 applies to this claim limitation.</p> <p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method according to claim 3 wherein performing binarization comprises performing binarization so as to target a predetermined probability.</p> <p>The following specifications provide further evidence of how each of the Accused Products operates:</p>

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	<p>9.3.3.11 Binarization process for coeff_abs_level_remaining[]</p> <p>Input to this process is a request for a binarization for the syntax element coeff_abs_level_remaining[n], the current sub-block scan index i, baseLevel, the colour component cIdx and the luma location (x0, y0) specifying the top-left sample of the current luma transform block relative to the top-left luma sample of the picture.</p> <p>Output of this process is the binarization of the syntax element.</p>

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	<p>The variables cLastAbsLevel and cLastRiceParam are derived as follows:</p> <ul style="list-style-type: none"> – If this process is invoked for the first time for the current sub-block scan index i, cLastAbsLevel is set equal to 0 and cLastRiceParam is set equal to initRiceValue. – Otherwise (this process is not invoked for the first time for the current sub-block scan index i), cLastAbsLevel and cLastRiceParam are set equal to the values of cAbsLevel and cRiceParam, respectively, that have been derived during the last invocation of the binarization process for the syntax element coeff_abs_level_remaining[n] as specified in this clause. <p>The variable cAbsLevel is set equal to baseLevel + coeff_abs_level_remaining[n].</p> <p>The variable cRiceParam is derived from cLastAbsLevel and cLastRiceParam as follows:</p> <ul style="list-style-type: none"> – If persistent_rice_adaptation_enabled_flag is equal to 0, the following applies: $cRiceParam = \text{Min}(cLastRiceParam + (cLastAbsLevel > (3 * (1 \ll cLastRiceParam)) ? 1 : 0), 4) \quad (9-24)$ – Otherwise (persistent_rice_adaptation_enabled_flag is equal to 1), the following applies: $cRiceParam = cLastRiceParam + (cLastAbsLevel > (3 * (1 \ll cLastRiceParam)) ? 1 : 0) \quad (9-25)$ <p>The variable cMax is derived from cRiceParam as:</p> $cMax = 4 \ll cRiceParam \quad (9-26)$ <p>The binarization of the syntax element coeff_abs_level_remaining[n] is a concatenation of a prefix bin string and (when present) a suffix bin string.</p> <p>For the derivation of the prefix bin string, the following applies:</p> <ul style="list-style-type: none"> – The prefix value of coeff_abs_level_remaining[n], prefixVal, is derived as follows: $\text{prefixVal} = \text{Min}(cMax, \text{coeff_abs_level_remaining}[n]) \quad (9-27)$ – The prefix bin string is specified by invoking the TR binarization process as specified in clause 9.3.3.2 for prefixVal with the variables cMax and cRiceParam as inputs.

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	<p>When the prefix bin string is equal to the bit string of length 4 with all bits equal to 1, the suffix bin string is present and it is derived as follows:</p> <ul style="list-style-type: none"> – The suffix value of <code>coeff_abs_level_remaining[n]</code>, <code>suffixVal</code>, is derived as follows: <div style="text-align: right;"> $\text{suffixVal} = \text{coeff_abs_level_remaining}[n] - \text{cMax} \quad (9-28)$ </div> – If <code>extended_precision_processing_flag</code> is equal to 0, the suffix bin string is specified by invoking the k-th order EGk binarization process as specified in clause 9.3.3.3 for the binarization of <code>suffixVal</code> with the Exp-Golomb order k set equal to <code>cRiceParam + 1</code>. – Otherwise (<code>extended_precision_processing_flag</code> is equal to 1), the suffix bin string is specified by invoking the limited k-th order EGk binarization process as specified in clause 9.3.3.4 for the binarization of <code>suffixVal</code> with the variable <code>riceParam</code> set equal to <code>cRiceParam + 1</code> and the colour component <code>cIdx</code>. <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 222-224.</p> <p>9.3.4.2 Derivation process for <code>ctxTable</code>, <code>ctxIdx</code> and <code>bypassFlag</code></p> <p>9.3.4.2.1 General</p> <p>Input to this process is the position of the current bin within the bin string, <code>binIdx</code>.</p> <p>Outputs of this process are <code>ctxTable</code>, <code>ctxIdx</code> and <code>bypassFlag</code>.</p> <p>The values of <code>ctxTable</code>, <code>ctxIdx</code> and <code>bypassFlag</code> are derived as follows based on the entries for <code>binIdx</code> of the corresponding syntax element in Table 9-48:</p> <p>...</p> <ul style="list-style-type: none"> – Otherwise, if the entry in Table 9-48 is equal to "bypass", the values of <code>binIdx</code> are decoded by invoking the <code>DecodeBypass</code> process as specified in clause 9.3.4.3.4 and the following applies: <ul style="list-style-type: none"> – <code>ctxTable</code> is set equal to 0. – <code>ctxIdx</code> is set equal to 0. – <code>bypassFlag</code> is set equal to 1.

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	<p>...</p> <p style="text-align: center;">Table 9-48 – Assignment of ctxInc to syntax elements with context coded bins</p> <table><tr><th rowspan="2">Syntax element</th><th colspan="6">binIdx</th></tr><tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>>= 5</th></tr><tr><td>...</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>sig_coeff_flag[][]</td><td>0..43 (clause 9.3.4.2.5)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater1_flag[]</td><td>0..23 (clause 9.3.4.2.6)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_greater2_flag[]</td><td>0..5 (clause 9.3.4.2.7)</td><td>na</td><td>na</td><td>na</td><td>na</td><td>na</td></tr><tr><td>coeff_abs_level_remaining[]</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td><td>bypass</td></tr></table> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 225-227.</p> <p>9.3.4.3 Arithmetic decoding process</p> <p>9.3.4.3.1 General</p> <p>Inputs to this process are ctxTable, ctxIdx and bypassFlag, as derived in clause 9.3.4.2, and the state variables ivlCurrRange and ivlOffset of the arithmetic decoding engine.</p> <p>Output of this process is the value of the bin.</p> <p>Figure 9-5 illustrates the whole arithmetic decoding process for a single bin. For decoding the value of a bin, the context index table ctxTable and the ctxIdx are passed to the arithmetic decoding process DecodeBin(ctxTable, ctxIdx), which is specified as follows:</p> <ul style="list-style-type: none">– If bypassFlag is equal to 1, DecodeBypass() as specified in clause 9.3.4.3.4 is invoked.– Otherwise, if bypassFlag is equal to 0, ctxTable is equal to 0 and ctxIdx is equal to 0,	Syntax element	binIdx						0	1	2	3	4	>= 5	...							sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na	coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na	coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na	coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass
Syntax element	binIdx																																																
	0	1	2	3	4	>= 5																																											
...																																																	
sig_coeff_flag[][]	0..43 (clause 9.3.4.2.5)	na	na	na	na	na																																											
coeff_abs_level_greater1_flag[]	0..23 (clause 9.3.4.2.6)	na	na	na	na	na																																											
coeff_abs_level_greater2_flag[]	0..5 (clause 9.3.4.2.7)	na	na	na	na	na																																											
coeff_abs_level_remaining[]	bypass	bypass	bypass	bypass	bypass	bypass																																											

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	<p>DecodeTerminate() as specified in clause 9.3.4.3.5 is invoked.</p> <p>– Otherwise (bypassFlag is equal to 0 and ctxTable is not equal to 0), DecodeDecision() as specified in clause 9.3.4.3.2 is invoked.</p> <p>...</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 232.</p> <div data-bbox="898 578 1652 1185" data-label="Diagram"> <pre> graph TD Start([DecodeBin(ctxTable, ctxIdx, bypassFlag)]) --> D1{bypassFlag == 1?} D1 -- Yes --> DB[DecodeBypass] D1 -- No --> D2{ctxTable == 0 && ctxIdx == 0?} D2 -- Yes --> DT[DecodeTerminate] D2 -- No --> DD[DecodeDecision(ctxTable, ctxIdx, bypassFlag)] DB --> Done([Done]) DT --> Done DD --> Done </pre> <p style="text-align: right; font-size: small;">H.265v2(14)_F9-5</p> </div> <p style="text-align: center;">Figure 9-5 – Overview of the arithmetic decoding process for a single bin (informative)</p> <p>NOTE – Arithmetic coding is based on the principle of recursive interval subdivision. Given a probability estimation $p(0)$ and $p(1) = 1 - p(0)$ of a binary decision $(0, 1)$, an initially given code sub-interval with</p>

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	<p>the range $ivlCurrRange$ will be subdivided into two sub-intervals having range $p(0) * ivlCurrRange$ and $ivlCurrRange - p(0) * ivlCurrRange$, respectively. Depending on the decision, which has been observed, the corresponding sub-interval will be chosen as the new code interval, and a binary code string pointing into that interval will represent the sequence of observed binary decisions. It is useful to distinguish between the most probable symbol (MPS) and the least probable symbol (LPS), so that binary decisions have to be identified as either MPS or LPS, rather than 0 or 1. Given this terminology, each context is specified by the probability $pLPS$ of the LPS and the value of MPS ($valMps$), which is either 0 or 1. The arithmetic core engine in this Specification has three distinct properties:</p> <ul style="list-style-type: none"> – The probability estimation is performed by means of a finite-state machine with a table-based transition process between 64 different representative probability states $\{ pLPS(pStateIdx) \mid 0 \leq pStateIdx < 64 \}$ for the LPS probability $pLPS$. The numbering of the states is arranged in such a way that the probability state with index $pStateIdx = 0$ corresponds to an LPS probability value of 0.5, with decreasing LPS probability towards higher state indices. – The range $ivlCurrRange$ representing the state of the coding engine is quantized to a small set $\{Q1, \dots, Q4\}$ of pre-set quantization values prior to the calculation of the new interval range. Storing a table containing all 64×4 pre-computed product values of $Q_i * pLPS(pStateIdx)$ allows a multiplication-free approximation of the product $ivlCurrRange * pLPS(pStateIdx)$. – For syntax elements or parts thereof for which an approximately uniform probability distribution is assumed to be given a separate simplified encoding and decoding bypass process is used. <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 233.</p>

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9.3.4.3.4 Bypass decoding process for binary decisions

Inputs to this process are bits from slice segment data and the variables `ivlCurrRange` and `ivlOffset`.

Outputs of this process are the updated variable `ivlOffset` and the decoded value `binVal`.

The bypass decoding process is invoked when `bypassFlag` is equal to 1. Figure 9-8 shows a flowchart of the corresponding process.

First, the value of `ivlOffset` is doubled, i.e., left-shifted by 1 and a single bit is shifted into `ivlOffset` by using `read_bits( 1 )`. Then, the value of `ivlOffset` is compared to the value of `ivlCurrRange` and then the following applies:

- If `ivlOffset` is greater than or equal to `ivlCurrRange`, the variable `binVal` is set equal to 1 and `ivlOffset` is decremented by `ivlCurrRange`.
- Otherwise (`ivlOffset` is less than `ivlCurrRange`), the variable `binVal` is set equal to 0.

The bitstream shall not contain data that result in a value of `ivlOffset` being greater than or equal to `ivlCurrRange` upon completion of this process.

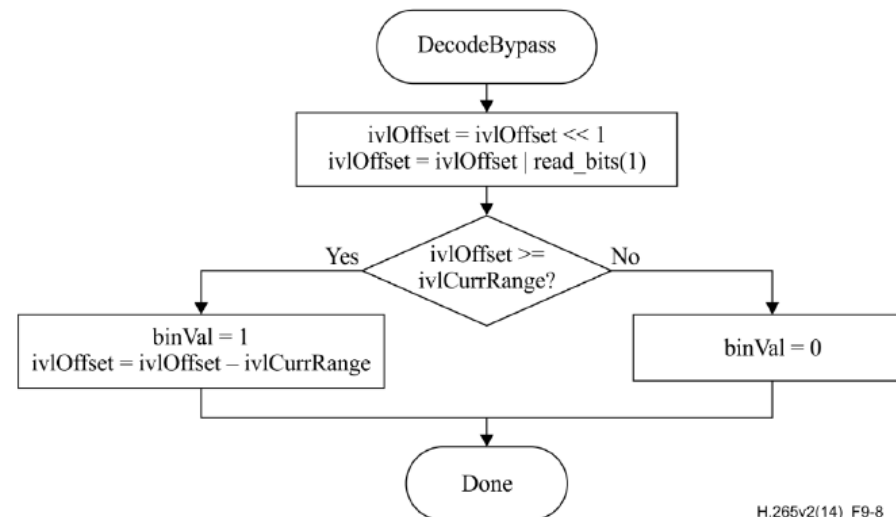


Figure 9-8 – Flowchart of bypass decoding process

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	ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 237.

4. Claim 6

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6. Pre A method according to claim 1	Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1 The evidence cited for Claim 1 applies to this claim limitation.
wherein categorizing the plurality of syntax elements comprises categorizing the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold.	Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1 wherein categorizing the plurality of syntax elements comprises categorizing the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold. The evidence cited for Claim 1 applies to this claim limitation. For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method according to claim 1 wherein categorizing the plurality of syntax elements comprises categorizing the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold. The following specifications provide further evidence of how each of the Accused Products operates:

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	<p>7.3.8.11 Residual coding syntax</p> <table border="1"> <thead> <tr> <th></th><th>Descriptor</th></tr> </thead> <tbody> <tr> <td>residual_coding(x0, y0, log2TrafoSize, cIdx) {</td><td></td></tr> <tr> <td>if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))</td><td></td></tr> <tr> <td>transform_skip_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>if(CuPredMode[x0][y0] == MODE_INTER && explicit_rdpem_enabled_flag && (transform_skip_flag[x0][y0][cIdx] cu_transquant_bypass_flag)) {</td><td></td></tr> <tr> <td>explicit_rdpem_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>if(explicit_rdpem_flag[x0][y0][cIdx])</td><td></td></tr> <tr> <td>explicit_rdpem_dir_flag[x0][y0][cIdx]</td><td>ae(v)</td></tr> <tr> <td>}</td><td></td></tr> <tr> <td>last_sig_coeff_x_prefix</td><td>ae(v)</td></tr> <tr> <td>last_sig_coeff_y_prefix</td><td>ae(v)</td></tr> <tr> <td>if(last_sig_coeff_x_prefix > 3)</td><td></td></tr> <tr> <td>last_sig_coeff_x_suffix</td><td>ae(v)</td></tr> <tr> <td>if(last_sig_coeff_y_prefix > 3)</td><td></td></tr> <tr> <td>last_sig_coeff_y_suffix</td><td>ae(v)</td></tr> <tr> <td>lastScanPos = 16</td><td></td></tr> <tr> <td>lastSubBlock = (1 << (log2TrafoSize - 2)) * (1 << (log2TrafoSize - 2)) - 1</td><td></td></tr> <tr> <td>do {</td><td></td></tr> <tr> <td>if(lastScanPos == 0) {</td><td></td></tr> </tbody> </table>		Descriptor	residual_coding(x0, y0, log2TrafoSize, cIdx) {		if(transform_skip_enabled_flag && !cu_transquant_bypass_flag && (log2TrafoSize <= Log2MaxTransformSkipSize))		transform_skip_flag[x0][y0][cIdx]	ae(v)	if(CuPredMode[x0][y0] == MODE_INTER && explicit_rdpem_enabled_flag && (transform_skip_flag[x0][y0][cIdx] cu_transquant_bypass_flag)) {		explicit_rdpem_flag[x0][y0][cIdx]	ae(v)	if(explicit_rdpem_flag[x0][y0][cIdx])		explicit_rdpem_dir_flag[x0][y0][cIdx]	ae(v)	}		last_sig_coeff_x_prefix	ae(v)	last_sig_coeff_y_prefix	ae(v)	if(last_sig_coeff_x_prefix > 3)		last_sig_coeff_x_suffix	ae(v)	if(last_sig_coeff_y_prefix > 3)		last_sig_coeff_y_suffix	ae(v)	lastScanPos = 16		lastSubBlock = (1 << (log2TrafoSize - 2)) * (1 << (log2TrafoSize - 2)) - 1		do {		if(lastScanPos == 0) {	
	Descriptor																																						
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explicit_rdpem_dir_flag[x0][y0][cIdx]	ae(v)																																						
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last_sig_coeff_x_prefix	ae(v)																																						
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do {																																							
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	lastScanPos = 16	
	lastSubBlock--	
	}	
	lastScanPos--	
	xS = ScanOrder[log2TrafoSize - 2][scanIdx][lastSubBlock][0]	
	yS = ScanOrder[log2TrafoSize - 2][scanIdx][lastSubBlock][1]	
	xC = (xS << 2) + ScanOrder[2][scanIdx][lastScanPos][0]	
	yC = (yS << 2) + ScanOrder[2][scanIdx][lastScanPos][1]	
	} while((xC != LastSignificantCoeffX) (yC != LastSignificantCoeffY))	
	for(i = lastSubBlock; i >= 0; i--) {	
	xS = ScanOrder[log2TrafoSize - 2][scanIdx][i][0]	
	yS = ScanOrder[log2TrafoSize - 2][scanIdx][i][1]	
	escapeDataPresent = 0	
	inferSbDcSigCoeffFlag = 0	
	if((i < lastSubBlock) && (i > 0)) {	
	coded_sub_block_flag [xS][yS]	ae(v)
	inferSbDcSigCoeffFlag = 1	
	}	
	for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {	
	xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]	
	yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]	
	if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {	
	sig_coeff_flag [xC][yC]	ae(v)
	if(sig_coeff_flag[xC][yC])	
	inferSbDcSigCoeffFlag = 0	
	}	

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	<table> <tr><td>}</td><td></td><td></td></tr> <tr><td>firstSigScanPos = 16</td><td></td><td></td></tr> <tr><td>lastSigScanPos = -1</td><td></td><td></td></tr> <tr><td>numGreater1Flag = 0</td><td></td><td></td></tr> <tr><td>lastGreater1ScanPos = -1</td><td></td><td></td></tr> <tr><td>for(n = 15; n >= 0; n--) {</td><td></td><td></td></tr> <tr><td>xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]</td><td></td><td></td></tr> <tr><td>yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]</td><td></td><td></td></tr> <tr><td>if(sig_coeff_flag[xC][yC]) {</td><td></td><td></td></tr> <tr><td>if(numGreater1Flag < 8) {</td><td></td><td></td></tr> <tr><td>coeff_abs_level_greater1_flag[n]</td><td></td><td>ae(v)</td></tr> <tr><td>numGreater1Flag++</td><td></td><td></td></tr> <tr><td>if(coeff_abs_level_greater1_flag[n] && lastGreater1ScanPos == -1)</td><td></td><td></td></tr> <tr><td>lastGreater1ScanPos = n</td><td></td><td></td></tr> <tr><td>else if(coeff_abs_level_greater1_flag[n])</td><td></td><td></td></tr> <tr><td>escapeDataPresent = 1</td><td></td><td></td></tr> <tr><td>} else</td><td></td><td></td></tr> <tr><td>escapeDataPresent = 1</td><td></td><td></td></tr> </table>		}			firstSigScanPos = 16			lastSigScanPos = -1			numGreater1Flag = 0			lastGreater1ScanPos = -1			for(n = 15; n >= 0; n--) {			xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]			yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]			if(sig_coeff_flag[xC][yC]) {			if(numGreater1Flag < 8) {			coeff_abs_level_greater1_flag[n]		ae(v)	numGreater1Flag++			if(coeff_abs_level_greater1_flag[n] && lastGreater1ScanPos == -1)			lastGreater1ScanPos = n			else if(coeff_abs_level_greater1_flag[n])			escapeDataPresent = 1			} else			escapeDataPresent = 1		
}																																																								
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	if(lastSigScanPos == -1)	
	lastSigScanPos = n	
	firstSigScanPos = n	
	}	
	}	
	if(cu_transquant_bypass_flag (CuPredMode[x0][y0] == MODE_INTRA && implicit_rdpkm_enabled_flag && transform_skip_flag[x0][y0][cIdx] && (predModeIntra == 10 predModeIntra == 26)) explicit_rdpkm_flag[x0][y0][cIdx])	
	signHidden = 0	
	else	
	signHidden = lastSigScanPos - firstSigScanPos > 3	
	if(lastGreater1ScanPos != -1) {	
	coeff_abs_level_greater2_flag[lastGreater1ScanPos]	ae(v)
	if(coeff_abs_level_greater2_flag[lastGreater1ScanPos])	
	escapeDataPresent = 1	
	}	

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		for(n = 15; n >= 0; n--) {	
		xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]	
		yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]	
		if(sig_coeff_flag[xC][yC] && (!sign_data_hiding_enabled_flag !signHidden (n != firstSigScanPos)))	
		coeff_sign_flag[n]	ae(v)
		}	

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	<pre> numSigCoeff = 0 sumAbsLevel = 0 for(n = 15; n >= 0; n--) { xC = (xS << 2) + ScanOrder[2][scanIdx][n][0] yC = (yS << 2) + ScanOrder[2][scanIdx][n][1] if(sig_coeff_flag[xC][yC]) { baseLevel = 1 + coeff_abs_level_greater1_flag[n] + coeff_abs_level_greater2_flag[n] if(baseLevel == ((numSigCoeff < 8) ? ((n == lastGreater1ScanPos) ? 3 : 2) : 1)) coeff_abs_level_remaining[n] TransCoeffLevel[x0][y0][cIdx][xC][yC] = (coeff_abs_level_remaining[n] + baseLevel) * (1 - 2 * coeff_sign_flag[n]) if(sign_data_hiding_enabled_flag && signHidden) { sumAbsLevel += (coeff_abs_level_remaining[n] + baseLevel) if((n == firstSigScanPos) && ((sumAbsLevel % 2) == 1)) TransCoeffLevel[x0][y0][cIdx][xC][yC] = -TransCoeffLevel[x0][y0][cIdx][xC][yC] } } numSigCoeff++ } } } } } </pre>
	<p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 58-60.</p> <p>As set out in the Residual Coding Syntax in section 7.3.8.11, an H.265 compliant decoder parses <i>sig_coeff_flags</i> from the bit stream according to the logic reproduced below.</p>

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	<table border="1"> <tr> <td>for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {</td><td></td></tr> <tr> <td>xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]</td><td></td></tr> <tr> <td>yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]</td><td></td></tr> <tr> <td>if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {</td><td></td></tr> <tr> <td>sig_coeff_flag[xC][yC]</td><td>ae(v)</td></tr> <tr> <td>if(sig_coeff_flag[xC][yC])</td><td></td></tr> <tr> <td>inferSbDcSigCoeffFlag = 0</td><td></td></tr> <tr> <td>}</td><td></td></tr> </table>	for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {		xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]		yC = (yS << 2) + ScanOrder[2][scanIdx][n][1]		if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {		sig_coeff_flag[xC][yC]	ae(v)	if(sig_coeff_flag[xC][yC])		inferSbDcSigCoeffFlag = 0		}	
for(n = (i == lastSubBlock) ? lastScanPos - 1 : 15; n >= 0; n--) {																	
xC = (xS << 2) + ScanOrder[2][scanIdx][n][0]																	
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if(coded_sub_block_flag[xS][yS] && (n > 0 !inferSbDcSigCoeffFlag)) {																	
sig_coeff_flag[xC][yC]	ae(v)																
if(sig_coeff_flag[xC][yC])																	
inferSbDcSigCoeffFlag = 0																	
}																	
	<p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 59.</p> <p>7.4.9.11 Residual coding semantics</p> <p>...</p> <p>sig_coeff_flag[xC][yC] specifies for the transform coefficient location (xC, yC) within the current transform block whether the corresponding transform coefficient level at the location (xC, yC) is non-zero as follows:</p> <ul style="list-style-type: none"> – If sig_coeff_flag[xC][yC] is equal to 0, the transform coefficient level at the location (xC, yC) is set equal to 0. – Otherwise (sig_coeff_flag[xC][yC] is equal to 1), the transform coefficient level at the location (xC, yC) has a non-zero value. <p>When sig_coeff_flag[xC][yC] is not present, it is inferred as follows:</p> <ul style="list-style-type: none"> – If (xC, yC) is the last significant location (LastSignificantCoeffX, LastSignificantCoeffY) in scan order or all of the following conditions are true, sig_coeff_flag[xC][yC] is inferred to be equal to 1: <ul style="list-style-type: none"> – (xC & 3, yC & 3) is equal to (0, 0). – inferSbDcSigCoeffFlag is equal to 1. 																

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	<ul style="list-style-type: none"> – coded_sub_block_flag[xS][yS] is equal to 1. – Otherwise, sig_coeff_flag[xC][yC] is inferred to be equal to 0. ... <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 111.</p> <p>9.3.4.2 Derivation process for ctxTable, ctxIdx and bypassFlag</p> <p>9.3.4.2.1 General</p> <p>Input to this process is the position of the current bin within the bin string, binIdx.</p> <p>Outputs of this process are ctxTable, ctxIdx and bypassFlag.</p> <p>The values of ctxTable, ctxIdx and bypassFlag are derived as follows based on the entries for binIdx of the corresponding syntax element in Table 9-48:</p> <ul style="list-style-type: none"> – If the entry in Table 9-48 is not equal to "bypass", "terminate" or "na", the values of binIdx are decoded by invoking the DecodeDecision process as specified in clause 9.3.4.3.2 and the following applies: <ul style="list-style-type: none"> – ctxTable is specified in Table 9-4. – The variable ctxInc is specified by the corresponding entry in Table 9-48 and when more than one value is listed in Table 9-48 for a binIdx, the assignment process for ctxInc for that binIdx is further specified in the clauses given in parenthesis. – The variable ctxIdxOffset is specified by the lowest value of ctxIdx in Table 9-4 depending on the current value of initType. – ctxIdx is set equal to the sum of ctxInc and ctxIdxOffset. – bypassFlag is set equal to 0. – Otherwise, if the entry in Table 9-48 is equal to "bypass", the values of binIdx are decoded by invoking the DecodeBypass process as specified in clause 9.3.4.3.4 and the following applies:

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5. Claim 7

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<p>7. Pre A method according to claim 1</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1.</p> <p>The evidence cited for Claim 1 applies to this claim limitation.</p>
<p>[a] further comprising performing binarization of the symbols that correspond to the first category of syntax elements prior to entropy coding the symbols that correspond to the first category of syntax elements.</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, performs a method according to claim 1 further comprising performing binarization of the symbols that correspond to the first category of syntax elements prior to entropy coding the symbols that correspond to the first category of syntax elements.</p> <p>The evidence cited for Claim 1 applies to this claim limitation.</p> <p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method according to claim 1 further comprising performing binarization of the symbols that correspond to the first category of syntax elements prior to entropy coding the symbols that correspond to the first category of syntax elements.</p> <p>The following specifications provide further evidence of how each of the Accused Products operates:</p> <p>9.3 CABAC parsing for slice segment data</p> <p>9.3.1 General</p> <p>This process is invoked when parsing syntax elements with descriptor ae(v) in clauses 7.3.8.1 through 7.3.8.12.</p> <p>Inputs to this process are a request for a value of a syntax element and value of prior parsed syntax elements.</p> <p>Outputs of this process is the value of the syntax element</p> <p>...</p> <p>For each requested value of a syntax element a binarization is derived as specified in clause 9.3.3.</p>

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	<p>The binarization for the syntax element and the sequence of parsed bins determines the decoding process flow as described in clause 9.3.4.</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 201.</p> <p>9.3.3 Binarization process</p> <p>9.3.3.1 General</p> <p>Inputs to this process is a request for syntax element.</p> <p>Output of this process is the binarization of the syntax element.</p> <p>Table 9-43 specifies the type of binarization process associated with each syntax element and corresponding inputs.</p> <p>The specification of the truncated Rice (TR) binarization process, the k-th order Exp-Golomb (EGk) binarization process, limited k-th order Exp-Golomb (EGk) binarization process, the fixed-length (FL) binarization process, and the truncated binary binarization process are given in clauses 9.3.3.2 through 9.3.3.6, respectively. Other binarizations are specified in clauses 9.3.3.7 through 9.3.3.14.</p> <p>...</p>

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	Table 9-43 – Syntax elements and associated binarizations			
	Syntax structure	Syntax element	Binarization	
			Process	Input parameters
	cross_comp_pred()	log2_res_scale_abs_plus1	TR	cMax = 4, cRiceParam = 0
		res_scale_sign_flag	FL	cMax = 1
	residual_coding()	transform_skip_flag[][]	FL	cMax = 1
		explicit_rdpem_flag[][]	FL	cMax = 1
		explicit_rdpem_dir_flag[][]	FL	cMax = 1
		last_sig_coeff_x_prefix	TR	cMax = (log2TrafoSize << 1) - 1, cRiceParam = 0
		last_sig_coeff_y_prefix	TR	cMax = (log2TrafoSize << 1) - 1, cRiceParam = 0
		last_sig_coeff_x_suffix	FL	cMax = (1 << ((last_sig_coeff_x_prefix >> 1) - 1) - 1)
		last_sig_coeff_y_suffix	FL	cMax = (1 << ((last_sig_coeff_y_prefix >> 1) - 1) - 1)
		coded_sub_block_flag[][]	FL	cMax = 1
		sig_coeff_flag[][]	FL	cMax = 1
		coeff_abs_level_greater1_flag[]	FL	cMax = 1
		coeff_abs_level_greater2_flag[]	FL	cMax = 1
		coeff_abs_level_remaining[]	9.3.3.11	current sub-block scan index i, baseLevel
coeff_sign_flag[]	FL	cMax = 1		
ITU-T Rec. H.265 (12/2016) High efficiency video coding at pp. 216-218.				

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	<p>9.3.4 Decoding process flow</p> <p>9.3.4.1 General</p> <p>Inputs to this process are all bin strings of the binarization of the requested syntax element as specified in clause 9.3.3.</p> <p>Output of this process is the value of the syntax element.</p> <p>ITU-T Rec. H.265 (12/2016) High efficiency video coding at p. 225.</p>

6. Claim 8

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<p>8. [Pre] An apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, cause the apparatus to at least:</p>	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises an apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, cause the apparatus to satisfy the limitations below.</p> <p>For example, and without limitation, the Hisense 43A7N uses hardware-accelerated video decoding and includes Mediatek MT9602 Processor with onboard memory.</p>

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	<div></div> <p>https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).</p>

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	<div data-bbox="638 451 1178 797">  </div> <div data-bbox="1207 354 1743 634"> <p>Display: 42.5 in, VA, Direct LED, 3840 x 2160 pixels Viewing angles (H/V): 178 ° / 178 ° Brightness: 275 cd/m² Static contrast: 4000 : 1 Refresh rate: 50 Hz / 60 Hz Frame interpolation: 120 MR (Motion Rate) TV tuner: Analog (NTSC/PAL/SECAM), ATSC, Clear QAM SoC: MediaTek MT9602 CPU: ARM Cortex-A53, 1500 MHz, Cores: 4 Dimensions: 963 x 560 x 74 mm Weight: 6.8 kg</p> </div> <div data-bbox="1218 659 1690 704"> <div>Add to compare</div> <div>Suggest an edit</div> </div> <p>https://www.displayspecifications.com/en/model/234a3f3b</p>

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	<div data-bbox="638 297 1010 354">Specifications</div> <hr/> <table> <tr> <td data-bbox="638 488 863 529" rowspan="8">Processors</td><td data-bbox="989 488 1142 529">CPU Type</td><td data-bbox="1379 488 1549 513">Arm Cortex-A53</td></tr> <tr> <td data-bbox="989 602 1113 634">CPU Bit</td><td data-bbox="1379 602 1451 626">64-bit</td></tr> <tr> <td data-bbox="989 716 1157 748">CPU Cores</td><td data-bbox="1379 716 1472 740">Quad (4)</td></tr> <tr> <td data-bbox="989 829 1304 862">Max CPU Frequency</td><td data-bbox="1379 829 1451 854">1.5GHz</td></tr> <tr> <td data-bbox="989 943 1142 976">GPU Type</td><td data-bbox="1379 943 1619 967">Arm Mali-G52 2EE MC1</td></tr> <tr> <td data-bbox="989 1057 1121 1089">Memory</td><td data-bbox="1379 1057 1486 1081">48b DDR3</td></tr> <tr> <td data-bbox="989 1170 1192 1203">Max Memory</td><td data-bbox="1379 1170 1430 1195">2GB</td></tr> <tr> <td colspan="2">Source: https://www.mediatek.com/products/pentonic/mt9602. (Last accessed March 29, 2025).</td></tr> </table>		Processors	CPU Type	Arm Cortex-A53	CPU Bit	64-bit	CPU Cores	Quad (4)	Max CPU Frequency	1.5GHz	GPU Type	Arm Mali-G52 2EE MC1	Memory	48b DDR3	Max Memory	2GB	Source: https://www.mediatek.com/products/pentonic/mt9602 . (Last accessed March 29, 2025).	
Processors	CPU Type	Arm Cortex-A53																	
	CPU Bit	64-bit																	
	CPU Cores	Quad (4)																	
	Max CPU Frequency	1.5GHz																	
	GPU Type	Arm Mali-G52 2EE MC1																	
	Memory	48b DDR3																	
	Max Memory	2GB																	
	Source: https://www.mediatek.com/products/pentonic/mt9602 . (Last accessed March 29, 2025).																		

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	Video Format			
	MPEG program stream	MPEG1/2	.DAT, .VOB, .MPG, .MPEG	1920 x 1080 @ 60fps
		MPEG4		
		H.264		3840 x 2160 @ 60fps
	MPEG transport stream	HEVC/H.265	.ts, .trp, .tp	3840 x 2160 @ 60fps
		MPEG4		1920 x 1080 @ 60fps
		H.264		3840 x 2160 @ 60fps
		VC1		1920 x 1080 @ 60fps

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<div></div>	Container	Video Codec	File Extension Name	Resolution and Frame Rate
		MPEG1/2		1920 x 1080 @ 60fps
		AVS		
		AVS+		
		AVS2		
	MP4	VP8	.mp4, .mov	1920 x 1080 @ 60fps
		AV1		3840 x 2160 @ 60fps
		HEVC/H.265		1920 x 1080 @ 60fps
		MPEG1/2		
		MPEG4		
		H.263		
		H.264		3840 x 2160 @ 60fps
		WMV3		1920 x 1080 @ 60fps
		VC1		1920 x 1080 @ 30fps
		Motion JPEG		
Source: Hisense 43A7N User Manual, at 45-46. Downloaded from https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).				
The evidence cited for the claim limitation of claim 1[A] applies to this claim limitation.				
[a] determine a frequency occurrence threshold based on an expected frequency of	Each of the Accused Products, such as the Hisense 43A7N, comprises an apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, determine a frequency occurrence threshold based on an expected frequency of occurrence of syntax elements in a bit stream.			

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CLAIM CHART FOR INFRINGEMENT OF CLAIMS 1, 8, AND 15 BY HISENSE ACCUSED PRODUCTS

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occurrence of syntax elements in a bit stream;	The evidence cited for the claim limitations of claim 1[a] applies to this claim limitation.
[b] categorize a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category;	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises an apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, categorize a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category.</p> <p>The evidence cited for the claim limitations of claim 1[b] applies to this claim limitation.</p>
[c] entropy code symbols that correspond to the first category of syntax elements and that have been subjected to a context update; and	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises an apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, entropy code symbols that correspond to the first category of syntax elements and that have been subjected to a context update.</p> <p>The evidence cited for the claim limitations of claim 1[c] applies to this claim limitation.</p>
[d] entropy code symbols that correspond to the second category of syntax elements	Each of the Accused Products, such as the Hisense 43A7N, comprises an apparatus comprising at least one processor and at least one memory including computer program code, the at least one memory and the computer program code configured to, with the processor, entropy code symbols that correspond to the second category of syntax elements and that have bypassed context updating.

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and that have bypassed context updating.	The evidence cited for the claim limitations of claim 1[d] applies to this claim limitation.

7. Claim 10

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10. Pre An apparatus according to claim 8	<p>Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8.</p> <p>The evidence cited for Claim 8 applies to this claim limitation.</p> <p>For example, and without limitation, the H.265 Standard specifies the following regarding the decoding process. Each of the Accused Products performs a method comprising entropy coding symbols that correspond to the second category of syntax elements and that have bypassed context updating.</p>
[a] wherein the at least one memory and the computer program code are further configured to, with the processor, cause the apparatus to perform binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating.	<p>Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8 wherein the at least one memory and the computer program code are further configured to, with the processor, cause the apparatus to perform binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating.</p> <p>The evidence cited for Claims 3 and 8 applies to this claim limitation.</p>

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8. Claim 11

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11. Pre An apparatus according to claim 10	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 10. The evidence cited for Claim 10 applies to this claim limitation.
wherein the at least one memory and the computer program code are configured to, with the processor, cause the apparatus to perform binarization by performing binarization so as to target a predetermined probability.	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 10 wherein the at least one memory and the computer program code are configured to, with the processor, cause the apparatus to perform binarization by performing binarization so as to target a predetermined probability. The evidence cited for Claims 4 and 10 applies to this claim limitation.

9. Claim 13

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13. Pre An apparatus according to claim 8	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8. The evidence cited for Claim 8 applies to this claim limitation.

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[a] wherein the at least one memory and the computer program code are configured to, with the processor, cause the apparatus to categorize the plurality of syntax elements by categorizing the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold.	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8 wherein the at least one memory and the computer program code are configured to, with the processor, cause the apparatus to categorize the plurality of syntax elements by categorizing the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold. The evidence cited for Claims 6 and 8 applies to this claim limitation.

10. Claim 14

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14. Pre An apparatus according to claim 8	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8. The evidence cited for Claim 8 applies to this claim limitation.
[a] wherein the at least one memory and the computer program code are further configured to, with the processor, cause the	Each of the Accused Products, such as the Hisense 43A7N, comprise an apparatus according to claim 8 wherein the at least one memory and the computer program code are further configured to, with the processor, cause the apparatus to perform binarization of the symbols that correspond to the first category of syntax elements prior to entropy coding the symbols that correspond to the first category of syntax elements.

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apparatus to perform binarization of the symbols that correspond to the first category of syntax elements prior to entropy coding the symbols that correspond to the first category of syntax elements.	The evidence cited for Claims 7 and 8 applies to this claim limitation.

11. Claim 15

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15. [Pre] A computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising program code instructions to:	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises a computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising program code instructions to satisfy the limitations below.</p> <p>For example, and without limitation, the Hisense 43A7N uses hardware-accelerated video decoding and includes Mediatek MT9602 Processor.</p>

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	<div data-bbox="625 293 699 784"></div> <div data-bbox="709 386 1215 708"></div> <div data-bbox="1381 350 1871 496"><p>43A7N</p><p>Hisense 43" Class A7 Series LCD 4K Google TV</p></div> <div data-bbox="1381 553 1724 623"><p>Sizes:</p><div>43" 50" 55" 65" 75" 85"</div></div> <div data-bbox="1381 664 1528 699"><p>Where to Buy</p></div> <p>https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).</p>

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	<div data-bbox="638 451 1178 797">  </div> <div data-bbox="1207 354 1743 634"> <p>Display: 42.5 in, VA, Direct LED, 3840 x 2160 pixels Viewing angles (H/V): 178 ° / 178 ° Brightness: 275 cd/m² Static contrast: 4000 : 1 Refresh rate: 50 Hz / 60 Hz Frame interpolation: 120 MR (Motion Rate) TV tuner: Analog (NTSC/PAL/SECAM), ATSC, Clear QAM SoC: MediaTek MT9602 CPU: ARM Cortex-A53, 1500 MHz, Cores: 4 Dimensions: 963 x 560 x 74 mm Weight: 6.8 kg</p> </div> <div data-bbox="1218 659 1690 704"> <div>Add to compare</div> <div>Suggest an edit</div> </div> <div data-bbox="619 911 1331 941"> https://www.displayspecifications.com/en/model/234a3f3b </div>

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	Video Format			
	Container	Video Codec	File Extension Name	Resolution and Frame Rate
	MPEG program stream	MPEG1/2	.DAT, .VOB, .MPG, .MPEG	1920 x 1080 @ 60fps
		MPEG4		
		H.264		3840 x 2160 @ 60fps
	MPEG transport stream	HEVC/H.265	.ts, .trp, .tp	3840 x 2160 @ 60fps
		MPEG4		1920 x 1080 @ 60fps
		H.264		3840 x 2160 @ 60fps
		VC1		1920 x 1080 @ 60fps

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	Container	Video Codec	File Extension Name	Resolution and Frame Rate
		MPEG1/2		1920 x 1080 @ 60fps
		AVS		
		AVS+		
		AVS2		
	MP4	VP8	.mp4, .mov	1920 x 1080 @ 60fps
		AV1		3840 x 2160 @ 60fps
		HEVC/H.265		1920 x 1080 @ 60fps
		MPEG1/2		
		MPEG4		
		H.263		
		H.264		3840 x 2160 @ 60fps
		WMV3		1920 x 1080 @ 60fps
		VC1		1920 x 1080 @ 30fps
		Motion JPEG		
Source: Hisense 43A7N User Manual, at 45-46. Downloaded from https://www.hisense-usa.com/televisions/hisense-43-class-a7-series-4k-wide-color-gamut-google-tv-43a7n (last accessed March 29, 2025).				
The evidence cited for the claim limitation of claim 1[A] applies to this claim limitation.				
[a] determine a frequency of occurrence threshold based on an expected frequency of	Each of the Accused Products, such as the Hisense 43A7N, comprises a computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising			

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occurrence of syntax elements in a bit stream;	<p>program code instructions to determine a frequency of occurrence threshold based on an expected frequency of occurrence of syntax elements in a bit stream.</p> <p>The evidence cited for the claim limitations of claim 1[a] applies to this claim limitation.</p>
[b] categorize a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category;	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises a computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising program code instructions to categorize a plurality of syntax elements of video content into first and second categories based on the frequency of occurrence threshold, wherein syntax elements which occur greater than the frequency of occurrence threshold are categorized into the second category and syntax elements which occur less than the frequency of occurrence are categorized into the first category.</p> <p>The evidence cited for the claim limitations of claim 1[b] applies to this claim limitation.</p>
[c] entropy code symbols that correspond to the first category of syntax elements and that have been subjected to a context update; and	<p>Each of the Accused Products, such as the Hisense 43A7N, comprises a computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising program code instructions to entropy code symbols that correspond to the first category of syntax elements and that have been subjected to a context update.</p> <p>The evidence cited for the claim limitations of claim 1[c] applies to this claim limitation.</p>

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[d] entropy code symbols that correspond to the second category of syntax elements and that have bypassed context updating.	Each of the Accused Products, such as the Hisense 43A7N, comprises a computer program product comprising at least one non-transitory computer-readable storage medium having computer-executable program code instructions stored therein, the computer-executable program code instructions comprising program code instructions to entropy code symbols that correspond to the second category of syntax elements and that have bypassed context updating. The evidence cited for the claim limitations of claim 1[d] applies to this claim limitation.

12. Claim 17

U.S. PATENT NO. 9,036,701	HISENSE ACCUSED PRODUCTS
17. Pre A computer program product according to claim 15	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 15. The evidence cited for Claim 15 applies to this claim limitation.
[a] wherein the computer-executable program code instructions further comprise program code instructions to perform binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 15 wherein the computer-executable program code instructions further comprise program code instructions to perform binarization of the symbols that correspond to the second category of syntax elements prior to bypassing the context updating. The evidence cited for Claims 3 and 15 applies to this claim limitation.

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13. Claim 18

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3. A computer program product according to claim 17	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 17. The evidence cited for Claim 17 applies to this claim limitation.
[a] wherein the comprise program code instructions to perform binarization comprise program code instructions to perform binarization so as to target a predetermined probability.	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 17 wherein the comprise program code instructions to perform binarization comprise program code instructions to perform binarization so as to target a predetermined probability. The evidence cited for Claims 4 and 17 applies to this claim limitation.

14. Claim 20

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20. Pre A computer program product according to claim 15	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 15. The evidence cited for Claim 15 applies to this claim limitation.
[a] comprise the program code instructions to categorize the plurality of	Each of the Accused Products, such as the Hisense 43A7N, comprise a computer program product according to claim 15 comprise the program code instructions to categorize the plurality of syntax

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syntax elements comprise program code instructions to categorize the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold.	<p>elements comprise program code instructions to categorize the plurality of syntax elements based on a relationship of the frequency of occurrence of the syntax elements to a predefined threshold.</p> <p>The evidence cited for Claims 6 and 15 applies to this claim limitation.</p>