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Patent

Address to:
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Patent Number	11347657
Issue Date	05/31/2022
Application Number	17/479475
Filing Date	09/20/2021
First Named Inventor	Robert LERCARI
Attorney Docket Number	RMS-08BC2 / 821Z

Please change the Correspondence Address for the above-identified patent to:

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☒ **Firm *or* Individual Name** Radian Memory Systems, LLC

6275 West Plano Parkway, Suite 500

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Country

Telephone | **Email**

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I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 35675.

Signature /Marc P. Schuyler/

Typed or Printed Name Marc P. Schuyler

Date 11/22/2024 | Telephone

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/479,475	**11/22/2024 08:40:24 PM Z ET**	**2021051 / RMS08BC2**

Title of Invention

ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11347657
CONFIRMATION #	7676	FILED BY	Marc Schuyler
PATENT CENTER #	68096749	FILING DATE	09/20/2021
CUSTOMER #	73091	FIRST NAMED INVENTOR	Robert Lercari
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
sb0123_fill-821Z-17479475.pdf	2	Change of Address	68 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
sb0123_fill-821Z-17479475.pdf	8327A6B32DEAAB1047D110F7720C5EC79F68E40693C389050E38D61C8BDBE25E55E23E9A0FCA5CA0043CB187A402065CA3921D8A3D302B4FF283A48A982CC6D7

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ACKNOWLEDGEMENT OF LOSS OF ENTITLEMENT TO ENTITY STATUS DISCOUNT

APPLICATION #	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET #	REQUEST ID
17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	216404

The entity status change request below filed through Patent Center on 05/17/2024 has been accepted.

Certifications

APPLICANT CHANGING TO REGULAR UNDISCOUNTED FEE STATUS

Signature

I certify, in accordance with 37 CFR 1.4(d)(4), that I am one of the signatories making the entity status change.

Signature	Name	Registration #
/Marc P. Schuyler/	Marc Schuyler	35675

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/479,475	05/31/2022	11347657	2021051 / RMS08BC2	7676

73091 7590 05/11/2022

Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Robert Lercari, Thousand Oaks, CA;
Alan Chen, Simi Valley, CA;
Mike Jadon, Manhattan Beach, CA;
Craig Robertson, Simi Valley, CA;
Andrey V. Kuzmin, Moscow, RUSSIAN FEDERATION;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Radian Memory Systems, Inc., Manhattan Beach, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Robert Lercari
Art Unit	
Examiner Name	unknown
Attorney Docket Number	2021051 / RMS-08BC2

	20	8065471	B2	2011-11-22	Yano et al.	
	21	9229854	B2	2016-01-05	Kuzmin et al.	
	22	5860082	A	1999-01-12	Smith et al.	
	23	7339823	B2	2008-03-04	Nakayama et al.	
	24	7581078	B2	2009-08-25	Ware	
	25	7710777	B1	2010-05-04	Mintierth	
	26	8055833	B2	2011-11-08	Danilak et al.	
	27	8068365	B2	2011-11-29	Kim	
	28	9542118	B1	2017-01-10	Lercari et al.	
	29	9400749	B1	2016-07-26	Kuzmin et al.	
Change(s) applied to document, /P.H./ 4/29/2022	30	9519578	B1	~~8216-12-13~~ 12/2016	Kuzmin et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.W/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number:	17/479475
Confirmation Number:	7676
First Named Inventor:	Robert Lercari
Title:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
Filing Date:	09/20/2021
Attorney Docket:	2021051 / RMS08BC2

COMMENT ON STATEMENT OF REASONS FOR ALLOWANCE

In connection with the reasons for allowance, as stated in the Notice of Allowance mailed on April 20, 2022, the Examiner provided a statement of reasons for allowance (hereinafter referred to as the "Reasons"). Applicant believes that the Reasons, to the extent understood, may be misconstrued and, as such, are incomplete. Applicant does not acquiesce to the Examiner's characterization/construction of the references cited, or that limitations referenced and/or highlighted and/or emboldened or otherwise emphasized by the Examiner are the "only" or "primary" grounds of distinguishing cited art, or that the art "teaches" subject matter as advocated by the Examiner, or that art is or is not "close." Applicant submits that indeed, the claims as a whole of the instant application, individually or in combination with other claims (via dependency), describe the patentable subject matter of Applicant's invention, and that claims are to be construed as provided by statute (i.e., by a court). Applicant reserves the right to assert that other limitations not listed by the Examiner also differentiate the cited art, and/or that cited references are not prior art to the present application, and/or that the cited art should be interpreted differently than as characterized by the Examiner. Accordingly, the Reasons in no way bind or affect the interpretation, infringement, validity and/or enforceability of any claim(s) or patent(s) resulting from, or relating to this application.

Respectfully submitted,
/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35,675

Electronic Patent Application Fee Transmittal

Application Number:	17479475
Filing Date:	20-Sep-2021
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2021051 / RMS08BC2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	600	600

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt

EFS ID:	45601122
Application Number:	17479475
International Application Number:	
Confirmation Number:	7676
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Customer Number:	73091
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2021051 / RMS08BC2
Receipt Date:	29-APR-2022
Filing Date:	20-SEP-2021
Time Stamp:	16:02:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E20224SG02423192
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	00-ptol85b-RMS-8BC2.pdf	272310 a30859a6669d4bfce9c063c0d324f1decbdbb3ac	no	2
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	00-2022-04-29-COSORFA-RMS-08BC2.pdf	43849 f823fb9278da1b7dd0f9a3443851dbe47b72aeeb	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	38255 faec688883e119e77d5fd68669ad98538c1234cd	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	354414		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B – FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
17/479475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

TITLE OF INVENTION:

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	600	0	0	600	07/20/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Marc P. Schuyler
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Radian Memory Systems, Inc.

(B) RESIDENCE: (CITY and STATE or COUNTRY): Manhattan Beach, California (USA)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☑ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (*Please first reapply any previously paid fee shown above*):

☑ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change of Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29. NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27. NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status. NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Marc P. Schuyler/ Date 29 April 2022

Typed or printed name Marc P. Schuyler Registration No. 35675

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

73091 7590 04/20/2022

Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

EXAMINER
WU, STEPHANIE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/20/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

TITLE OF INVENTION: ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/20/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73091 7590 04/20/2022

Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

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17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

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nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/20/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
WU, STEPHANIE	2133	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

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73091 7590 04/20/2022

Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

EXAMINER	
WU, STEPHANIE	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/20/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Samsung Ex. 1002, Page 17 of 249

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/479,475	Applicant(s) Lercari et al.	
	Examiner STEPHANIE WU	Art Unit 2133	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 3/30/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-18 and 20-23 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/STEPHANIE WU/
Examiner, Art Unit 2133

REASONS FOR ALLOWANCE

1. **Claims 1-18 and 20-23** are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claim 1 recites the limitation "flash memory comprising erase units; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address portion and a second address portion,

identify an addressed block device from the first address portion,

use a first division operation on the second address portion, to identify an addressed segment within the addressed block device, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, identify from the first division operation a third address portion, and use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a storage location within the selected one of the erase units"

Said limitation is taught by the specification of the instant application as originally filed at least at [P. 0057-58, 0063 and FIGs. 7 & 8 and incorporated specification 14/880529 P. 0057]. Said limitations, in combination with the other recited limitations of claim 1, are not taught or suggested by the prior art of record.

The closest prior art of record includes:

Coffin et al. (U.S. PGPub No. 2017/0192901) which teaches translating a virtual address into a physical address identifying a port associated with a cluster, an address field subdivided

into a base address identifying a memory block and an offset identifying a location within the block but does not teach the base address identifying a segment within the cluster, and performing further division on the base address to obtain numbers corresponding to: a memory block within the segment, and a storage location within the memory block.

Ravimohan et al. (U.S. PGPub No. 2017/0199703) which teaches memory organized as metaplanes, virtual dies and metablocks, virtual blocks and determining a die number during address translation by performing modulo on a metablock address but does not teach deriving first and second address portions from the metablock address, the first address portion identifying a metaplane, dividing the second address portion to identify a virtual die within the metaplane and a third address portion, dividing the third address portion to identify a virtual block and storage location within the virtual block.

Shaharabany et al. (U.S. PGPub No. 2017/0109078) which teaches dividing a logical block address by a size of a portion of an address map, then dividing the resulting quotient by a total number of dies to obtain a die number, which corresponds to the die storing the portion of the address map containing the logical block address but does not teach a portion of the logical block address identifying a block device, the resulting quotient identifying an addressed segment within the block device, and the result of the further division identifying an erase unit and storage location.

Claims 2-18 and 23 depend from claim 1, and are considered allowable for at least the same reasons as claim 1. **Claims 20-22** contain similar limitations to claim 1, and are considered allowable for at least the same reasons as claim 1

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments, see page 12-13, filed 3/30/2022, with respect to claim 20 have been fully considered and are persuasive. The objection of claim 20 has been withdrawn.

4. Applicant's arguments, see page 13, filed 3/30/2022, with respect to claim 1 have been fully considered and are persuasive. The 112(b) rejection of claim 1 has been withdrawn.

5. Applicant's arguments, see page 13, filed 3/30/2022, with respect to claim 2 have been fully considered and are persuasive. The 112(b) rejection of claim 2 has been withdrawn.

6. Applicant's arguments, see page 14, filed 3/30/2022, with respect to claim 5 have been fully considered and are persuasive. The 112(b) rejection of claim 5 has been withdrawn.

7. Applicant's arguments, see page 14-15, filed 3/30/2022, with respect to claim 14 have been fully considered and are persuasive. The 112(b) rejection of claim 14 has been withdrawn.

8. Applicant's arguments, see page 15, filed 3/30/2022, with respect to claim 2 have been fully considered and are persuasive. The 101 rejection of claim 2 has been withdrawn.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHANIE WU whose telephone number is (571)272-0257. The examiner can normally be reached 11a-8p.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/STEPHANIE WU/
Examiner, Art Unit 2133

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	**Art Unit**
	STEPHANIE WU	2133

CPC						
Symbol					**Type**	**Version**
G06F	/	12	/	1009	F	2013-01-01
G06F	/	12	/	109	I	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	3	/	0688	I	2013-01-01
G06F	/	3	/	0616	I	2013-01-01
G06F	/	3	/	064	I	2013-01-01
G06F	/	2212	/	7202	A	2013-01-01
G06F	/	3	/	0662	A	2013-01-01
G06F	/	2212	/	7205	A	2013-01-01
G06F	/	2212	/	7201	A	2013-01-01
G06F	/	3	/	0659	A	2013-01-01
G06F	/	2212	/	1016	A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/STEPHANIE WU/ Examiner, Art Unit 2133	15 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

U.S. Patent and Trademark Office

Part of Paper No.: 20220414

Samsung Ex. 1002, Page 24 of 249

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	**Art Unit**
	STEPHANIE WU	2133

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F12/1009	/	12	/	1009	
G06F3/06	/	3	/	06	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
711	103

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/STEPHANIE WU/ Examiner, Art Unit 2133	15 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
	STEPHANIE WU	2133

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10		19										
2	2	11	11	19	20										
3	3	12	12	20	21										
4	4	13	13	21	22										
5	5	14	14	22	23										
6	6	15	15												
7	7	16	16												
8	8	17	17												
9	9	18	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/STEPHANIE WU/ Examiner, Art Unit 2133	15 April 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	Art Unit
	STEPHANIE WU	2133

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F12/all, 109, 1036 (text limited)	12/29/2021	SW
G06F3/06xxxxxx, 0688 (text limited)	12/29/2021	SW
G06F2212/all (text limited)	12/30/2021	SW

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Inventor search in PALM	12/27/2021	SW
Assignee search in SEARCH	12/27/2021	SW
Searched PE2E SEARCH, see attached history	12/27/2021	SW
Searched Google Patents + Scholar for "divide address channel plane die"	12/29/2021	SW
Refreshed search in PE2E SEARCH, see attached history	04/14/2022	SW

/STEPHANIE WU/ Examiner, Art Unit 2133	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	Art Unit
	STEPHANIE WU	2133

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F3	0688, 06XX (text limited)	04/14/2022	SW
G06F12	all (text limited)	04/14/2022	SW
G06F2212	all (text limited)	04/14/2022	SW

/STEPHANIE WU/ Examiner, Art Unit 2133	

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	336	("10445229"|"10552058"|"10552085"|"10838853"|"20030028733"|"20030065866"|"20050073844"|"20050144413"|"20060022171"|"20070046681"|"20070058431"|"20070143569"|"20070233939"|"20070260811"|"20070283428"|"20080034153"|"20080082596"|"20080126720"|"20080147964"|"20080155204"|"20080189485"|"20080320476"|"20090036163"|"20090046533"|"20090083478"|"20090089482"|"20090089490"|"20090138671"|"20090172219"|"20090172246"|"20090172250"|"20090172257"|"20090172499"|"20090198946"|"20090254705"|"20090271562"|"20090292839"|"20090300015"|"20090327602"|"20100042655"|"20100115172"|"20100161882"|"20100162012"|"20100182838"|"20100191779"|"20100211737"|"20100241866"|"20100262761"|"20100262762"|"20100262765"|"20100262773"|"20100281230"|"20100287217"|"20100287327"|"20100287332"|"20100329011"|"20110033548"|"20110055445"|"20110066792"|"20110125956"|"20110153817"|"20110153911"|"20110161784"|"20110197023"|"20110238943"|"20110276756"|"20110296089"|"20110296133"|"20110314209"|"20120033519"|"20120054419"|"20120059972"|"20120066441"|"20120079174"|"20120131270"|"20120131381"|"20120159039"|"20120198129"|"2012	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:19 PM

		0204079"|"2013000734 3"|"20130013852"|"201 30019062"|"201300738 16"|"20130111295"|"20 130111298"|"20130124 793"|"20130138868"|"2 0130145111"|"2013016 6825"|"20130242425"|" 20130282955"|"201302 90619"|"20130297852"| "20130332656"|"20130 339580"|"20140101371 "|"20140122781"|"2014 0189207"|"2014018920 9"|"20140208004"|"201 40208062"|"201402151 29"|"20140237168"|"20 140297949"|"20150067 297"|"20150113203"|"2 0150134930"|"2015014 9789"|"20150193148"|" 20150212938"|"201502 61456"|"20150263978"| "20150309734"|"20150 324264"|"20150347041 "|"20150347296"|"2015 0355965"|"2015037861 3"|"20150378886"|"201 60018998"|"201600191 59"|"20160026564"|"20 160092116"|"20160179 664"|"20160202910"|"2 0160342509"|"2016035 7462"|"20160364179"|" 20170031699"|"201701 39838"|"20170220287"| "20170364445"|"55684 23"|"5652857"|"586008 2"|"6134631"|"7096378" |"7339823"|"7404031"|" 7406563"|"7581078"|"7 702846"|"7710777"|"77 52381"|"7801561"|"780 9900"|"7818489"|"7836 244"|"7861122"|"78775 40"|"7904619"|"794169 2"|"7970983"|"7991944" |"8001318"|"8024545"|" 8046524"|"8055833"|"8 065471"|"8065473"|"80 68365"|"8069284"|"807 2463"|"8074022"|"8082 389"|"8086790"|"80996 32"|"8285918"|"834704 2"|"8539197"|"8572331" |"8645634"|"9063844"|" 9176864"|"9229854"|"9 335939"|"9400749"|"95				

		19578"|"9542118"|"9588904"|"9652376"|"9696917"|"9710377"|"9727454"|"9785572"|"9846541").PN.					
L2	147	L1 AND (divid$4 division sub$1divid$4 sub$1divis$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:20 PM
L3	108	L1 NOT (radian).as. AND (divid$4 division sub$1divid$4 sub$1divis$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:21 PM
L4	36	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location))))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 12:29 AM
L5	43	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location))))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 12:29 AM
L20	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2	(US-PGPUB; USPAT)	OR	ON	ON	2021/12/29 01:04 AM

		(address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT ("radian").as,ASNM,AS TX,ASNP.					
L22	208	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:04 AM
L23	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:05 AM
L24	208	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:05 AM

		vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L25	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM
L26	17	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM
L27	24	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4) near6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM

		(address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L30	1	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 04:09 PM
L31	463	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 04:10 PM
L32	24	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 05:31 PM

		(address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L34	1	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4 divisor) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 05:32 PM
L38	110	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit) hierarch$8 tier level)) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:12 PM
L39	43	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:12 PM

		location))))					
L40	70	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! hierarch$5 (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:13 PM
L41	676	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:08 PM
L42	206	(hierarch$5 tier$3 level tuple) same2 (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:09 PM

		virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.					
L43	322	((hierarch$5 tier$3 level tuple) WITH (plane chip die channel bank eu! (erase NEAR unit))) AND (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:09 PM
L44	163	((hierarch$5 tier$3 level tuple) WITH (plane chip die channel bank eu! (erase NEAR unit))) AND (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:10 PM

		g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.					

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	174	((hierarch$5 tier$3 level tuple) WITH (plane chip die channel bank eu! (erase NEAR unit))) AND (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.	(US-PGPUB; USPAT)	OR	ON	ON	2022/04/14 12:41 AM
N2	75	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! hierarch$5 (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT)	OR	ON	ON	2022/04/14 12:41 AM

Bibliographic Data

Application No: 17/479,475

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /STEPHANIE WU/ Examiner's Signature | Initials

Title: ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/20/2021	711	2133	2021051 / RMS08BC2
RULE			

APPLICANTS

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INVENTORS

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Alan Chen, Simi Valley, CA, UNITED STATES

Mike Jadon, Manhattan Beach, CA, UNITED STATES

Craig Robertson, Simi Valley, CA, UNITED STATES

Andrey V. Kuzmin, Moscow, RUSSIAN FEDERATION

CONTINUING DATA

This application is a CON of 16808304 03/03/2020 PAT 11221959

16808304 is a CON of 15690006 08/29/2017 PAT 10642748

15690006 is a CON of 15074778 03/18/2016 PAT 9785572

15074778 is a CON of 14880529 10/12/2015 PAT 9542118

14880529 is a CIP of 14848273 09/08/2015 PAT 10642505

14880529 has PRO of 62199969 07/31/2015

14880529 has PRO of 62194172 07/17/2015

14880529 has PRO of 62063357 10/13/2014

14848273 has PRO of 62048162 09/09/2014

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

09/28/2021

**** SMALL ENTITY ****

STATE OR COUNTRY

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FILING FEE RECEIVED

$3,340

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

73091 7590 04/01/2022

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EXAMINER	
WU, STEPHANIE	

ART UNIT	PAPER NUMBER
2133	

MAIL DATE	DELIVERY MODE
04/01/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	**Application No.** 17/479,475	**Applicant(s)** Lercari et al.		
	Examiner STEPHANIE WU	**Art Unit** 2133	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
STEPHANIE WU	Primary Examiner	Telephonic
Marc Schuyler	Attorney	

Date of Interview: 30 March 2022

Issues Discussed:

Proposed Amendment(s)

Discussed applicant proposed amendments, which appear to overcome objections, 112(b) and 101 rejections, with the exception of claim 14. For claim 14, applicant encouraged to provide support from specification on how a single value, representing a time since a segment was last programmed, is determined in the case where multiple erase units are within a single segment.

☑ Attachment

/STEPHANIE WU/ Examiner, Art Unit 2133	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number:	17/479475
Confirmation Number:	7676
First Named Inventor:	Robert Lercari
Title:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
Filing Date:	09/20/2021
Attorney Docket:	2021051 / RMS08BC2

APPLICANT RESPONSE TO 1/04/2022 NONFINAL OFFICE ACTION

DRAFT**

In The Claims.

Please amend the claims as set forth below. This listing replaces all prior listings.

1. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address portion and a second address portion

identify an addressed block device from the first address portion,

use a first division operation on the second address portion, to identify an addressed segment within the addressed block device, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, identify from the first division operation a third address portion, and [[]] use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests; and

wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

2. (Currently Amended) The storage device of claim 1 wherein:

said circuitry comprises at least one processor; and

the storage device further comprises instructions stored on at least one physical storage medium, said instructions when executed to control the at least one processor .

3. (Currently Amended) The storage device of claim 1 wherein:

said circuitry can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and is to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host;

the request from the host to copy is to designate destination address information corresponding to the second physical storage location; and

the circuitry is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.

4. (Currently Amended) The storage device of claim 3 wherein the circuitry is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit.

5. (Currently Amended) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage device is to store the values representing a time since data was programmed on a basis that is respective to each structure of the number of structures, wherein each structure comprises at least one of a page or a unit of memory comprising one or more erase units of the flash memory, and wherein each value represents time since data was programmed into the respective structure.

6. (Currently Amended) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the circuitry is to fulfill the at least one of the incoming requests by issuing commands to the flash memory for which a quantum of flash memory selected by the commands which are issued in response to the at least one request is dependent on the information transmitted to the host identifying the number of structures.

7. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit to a host information that identifies an amount of flash memory that is to be erased as a unit.

8. (Currently Amended) The storage device of claim 1 wherein the third address portion specifies a location within a sequential range of locations that correspond to the erase units in the subset.

9. (Currently Amended) The storage device of claim 1 wherein the first division operation and the second division operation each subdivide a value obtained from the incoming address information accompanying each of the write requests into respective bitfields.

10. (Original) The storage device of claim 1 wherein:

the storage device is to store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

the storage device is to compare the values representing time since data was programmed to at least one threshold;

upon detection that a specific one of the values has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit; and

the storage device is to remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit.

11. (Currently Amended) The storage device of claim 10 wherein:

the flash memory is to have block devices, one of the block devices being the addressed block device; and

the storage device is to identify, for the data being copied, an address of a logical erase unit, the logical erase unit being associated with the addressed block device to the exclusion of each other one of the block devices; and

the storage device is to remap a correspondence between the address of the logical erase unit and the first physical erase unit to instead be between the address of the logical erase unit and the second physical erase unit.

12. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device is to store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory space;

the storage device is to compare the metadata to at least one threshold;

upon detection that specific metadata has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific metadata from a first physical erase unit to a second physical erase unit; and

the storage device is to remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit.

13. (Currently Amended) The storage device of claim 1 wherein:

the erase units of the flash memory are physical erase units;

the circuitry is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units; and

the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests.

14. (Currently Amended) The storage device of claim 1 wherein the storage device is to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold; and

responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values.

15. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device is further to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices,

receive a query, issued by a host, directed to a specific one of the block devices, and

responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted

information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

16. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device is further to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space, and

receive a query, issued by a host, wherein said query is specific to one of the block devices, and responsive to the query, identify specific metadata, associated with the specified one of the block devices, and transmit information to the host that conveys the specific metadata.

17. (Currently Amended) The storage device of claim 1 wherein the storage device is further to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space;

compare the metadata to at least one threshold; and

responsive to detection that specific metadata has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

18. (Currently Amended) The storage device of claim 1 wherein:

the flash memory comprises multiple planes; and

the circuitry is to, for each one of a set of the data write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page.

19. (Canceled)

20. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address portion and a second address portion,

identify an addressed block device from the first address portion,

use a first operation on the second address portion to subdivide the incoming address information into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second one of the first bit fields as a third address portion and use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields and to identify a storage location within the selected one of the erase units from a second one of the second bit fields;

wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests;

wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

21. (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of incoming requests:

derive a first address portion and a second address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the second address portion into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields, and to identify a third address portion from a second one of the first bit fields , wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields, and to identify a storage location within the selected one of the erase units from a second one of the second bit fields;

wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests;

wherein said circuitry is also to

execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

22. (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

Samsung Ex. 1002, Page 50 of 249

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address portion and a second address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the second address portion into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields and a third address portion from a second one of the first bit fields, , wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify, from a first one of the second bit fields, an address value to select one of the erase units and, from a second one of the second bit fields a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the incoming data write requests; and

wherein said circuitry is also to execute each one of incoming erase requests by controlling erasure in the flash memory of the one or more erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

23. (New) The storage device of claim 1 wherein the second address portion comprises a first set of bits and a second set of bits, the bits of the first set of bits being mutually-exclusive to the bits of the second set of bits, wherein the first division operation is to separate the first set of bits from the second set of bits, and the circuitry is to identify the addressed segment from the first set of bits.

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Samsung Ex. 1002, Page 51 of 249

REMARKS

In the Office Action mailed February 1, 2022, the Examiner issued a number of objections, a rejection under 35 USC 101 and a rejection under 35 USC 112, second paragraph.

Applicant respectfully requests reconsideration in view of the amendments set forth above.

In an attempt to facilitate ease of discussing each position of the Office Action, Applicant sequentially addresses each of the Examiner's positions below using numbered paragraphs.

1. Objection, claims 1, 20-22. At pages 2-3 of the Office Action, the Examiner objects to each independent claim and requires Applicant to add a second and/or third colon to each claim. Applicant disagrees with the Examiner's position, but has added extra colons as 'required' by the Examiner.[1] It is therefore respectfully requested that this objection be withdrawn.

2. Objection, claim 11. At page 3 of the Office Action, the Examiner objects to use of the term "and other of the block devices" and asserts that this term is grammatically incorrect. It is believed that the amendment set forth above moots this objection, and therefore, reconsideration and withdrawal of this objection is therefore respectfully requested.

3. Objection, claim 20. At page 3 of the Office Action, the Examiner objects to claim 20 and asserts that the term "second operation" should be "second division operation" to be consistent with the other independent claims. Applicant does not agree and respectfully requests reconsideration. In this regard, claim 1 simply refers to first and second division operations, whereas the other independent claims refer to first and second "operations" "to subdivide." The language is slightly different but is submitted to refer to the same feature, i.e., an operation "to subdivide" clearly also divides. Applicant has therefore not made the change requested by the Examiner and asserts that this claim feature is already consistent with the "division operations" referred to be the first claim set. Therefore, reconsideration is respectfully requested.

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[1]The Examiner appears to be focusing on her own grammatical stylistic preferences rather than a clarity issue. In this regard, a claim is a sentence, and there are many who believe that proper English grammar admits of only one colon per claim, e.g., to demark a subordinate clause or separate a list from a primary sentence topic. See, https://www.wipo.int/edocs/mdocs/aspac/en/wipo_ip_phl_16/wipo_ip_phl_16_t5.pdf (a patent claim is a single sentence with a colon separating a transitional phrase from the claim body, see, e.g., p. 24). Applicant also refers the Examiner to MPEP 608.01(m), which states that "there is no set statutory form for claims," "the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," and "[w]here a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation." Thus, the PTO Rules suggest that the primary way to clearly separate respective elements is by line indentation, not by inserting colons at multiple places within a claim. Thus, Applicant disagrees with the Examiner that colons are needed as implied by the Office Action. As noted however, in order to advance prosecution, Applicant has complied with the Examiner's request, by adding the requested colons.

4. Rejection, 35 USC 112(b), claim 1. At pages 3-4 of the Office Action, the Examiner rejects claims 1-22 asserting that use of "a first address portion" to refer to a portion of incoming address information for write requests, and use of "a first address portion" to refer to a portion of incoming address information for erase requests is unclear, and states an indefiniteness issue. Applicant does not agree, but to advance prosecution, has amended the claims in a manner that should moot this rejection. The Examiner also rejected these claims because the claims stated that the recited "storage drive" processes erase request address information without specifying whether "the circuitry" used to process address information used to process write request addresses is the same. Here also, this is not a 112 issue, i.e., it can be, or in other embodiments, it doesn't have to be - this does not raise a clarity issue. Nevertheless, to advance prosecution, Applicant has amended the claims in a manner that should moot this rejection. Therefore, reconsideration is respectfully requested.

5. Rejection, 35 USC 112(b), claim 2. At pages 4-5 of the Office Action, the Examiner rejects claim 2 as allegedly indefinite, because it is not clear to the Examiner whether the recited instructions control all of or part of the circuitry of claim 1. This rejection is traversed; ALL integrated circuits are made up of combinations and permutations of transistors, gates, and other structures. Similarly, all microprocessors feature "some" circuit elements (e.g., an ESD structure on an input pin) that are not configured by software. In this regard, claim 2 simply recites that the circuitry of claim 1 can, in some embodiments, be implemented to include software and processor or other hardware that is configured by the software. This is what the term "comprises" means, e.g., as contrasted with "consists of." It is respectfully submitted that claim 2 would be readily understood by those having skill in the art simply to say that the "circuitry" of claim 1 can, within the more detailed subject matter circumscribed by claim 2, include a processor/configurable hardware and instructions (e.g., software) that configured that processor/configurable hardware. With all due respect, there will always, in any implementation, be "some" circuitry (e.g., a ground pin) not configured by software/instructions, and one having skill in the art would not be confused by this claim vernacular, i.e., the claim unambiguously recites that some portion of "the circuitry" of claim 1 is embodies as a combination of general purpose circuitry and instructions/firmware/software. So as to hopefully clarify the meaning of this language in the Examiner's eyes, Applicant has made some minor amendments to claim 2 to delete second usage of the term "circuitry." Based on the foregoing, reconsideration of this ground of rejection is respectfully requested.

6. Rejection, 35 USC 112(b), claim 5. Applicant has corrected the term "drive" to instead refer to "device," as was originally intended. Also, the Examiner rejected this claim based on her reasoning that "it is unclear if the 'structure' in claim 5 is the same as an erase unit." This latter rejection, once again, does not state a 112 issue or any problem with clarity; that is, as would be well-known to those having skill in the art, time since data was programmed could be stored at a granularity of each page, or of each erase unit (e.g., the oldest data in that erase unit), or one some other basis. This claim is not rendered vague by specifying the

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granularity at which metadata is stored. Nevertheless, to advance prosecution, Applicant has amended the claim in a manner calculated to moot this ground of rejection, and reconsideration is respectfully requested.

7. Rejection, 35 USC 112(b), claim 6. Applicant has amended the claim in question in a manner that should moot this rejection, and therefore, reconsideration is therefore here also requested.

8. Rejection, 35 USC 112(b), claim 11. Applicant has amended the claim in question in a manner that should moot this rejection, and therefore, reconsideration is therefore here also requested.

9. Rejection, 35 USC 112(b), claims 12 and 15-17. Applicant has amended the claims in question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

10. Rejection, 35 USC 112(b), claim 13. Applicant has amended the claim in a question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

11. Rejection, 35 USC 112(b), claim 14. At page 7 of the Office Action, the Examiner rejected this claim saying that it is not clear whether the metadata represents a time since data was programmed in a particular erase unit or a time since data was programmed in a segment having such an erase unit. Applicant traverses this rejection, i.e., if a segment hypothetically has two erase units, and time since programming is stored for each erase unit, it is also stored for the segment, no? Consider for example a memory controller that stores a hypothetical age value of "5 minutes ago" for "erase unit 1" and of "6 minutes ago" for "erase unit 2," and that "segment A" corresponds to "erase units 1 and 2;" does not this memory controller NECESSARILY also store data for "segment A" indicating (the oldest) age of data in "segment A" (i.e., "6 minutes ago" in this hypothetical). Applicant does not see any lack of clarity at all, notwithstanding the Examiner's remarks, and respectfully requests reconsideration. It is additionally noted for the Examiner's convenience that "a time" will typically be embodied as the oldest age in a particular erase unit or group of erase units, i.e., evicting 'write cold data' and recycling each underlying erase unit promotes wear leveling by catching and forcing erasure of erase units that may evade garbage collection operations because associated data is only infrequently deallocated (i.e., these erase units continue to stay full and are not released, so they are not recycled by garbage collection processes which look for mostly-released erase units). It is submitted that there is no lack of clarity in this claim, i.e., this claim says that a time since data was programmed is stored for a segment (and since in described embodiments it can be stored for each erase unit that is part of a segment, it is also necessarily stored by these embodiments for each segment).

12. Rejection, 35 USC 112(b), claims 18-22. Applicant has amended the claims in question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

13. Rejection, 35 USC 101, claim 2. At page 7 of the Office Action, the Examiner rejected claim 2 as allegedly constituting nonstatutory subject matter. Applicant notes that this issue has been thoroughly discussed in the sister applications and need not be discussed again herein in detail - a claim is not "directed" to nonstatutory subject matter unless a claim as a whole is determined to be so directed, which cannot be

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the case for a dependent claim only (i.e., which inherits structure, including without limitation, all statutory subject matter structure, from one or more claims on which it dependents); furthermore, "nontransitory" is expressly defined in the specification so as to refer exclusively to physical media. Nevertheless, to advance prosecution, Applicant has changed the language in question to refer to at least one PHYSICAL storage medium. It is respectfully submitted that this change should moot the issue the Examiner has, and therefore reconsideration and withdrawal of this rejection is respectfully requested.

CONCLUSION.

For the various reasons set forth above, Applicant respectfully requests reconsideration, with a favorable eye toward allowance. As this particular application has track one status, it is respectfully requested that if the Examiner still has issues (e.g., objections to claim language or rejections based on language or otherwise), the Examiner telephone the undersigned so as to discuss by interview, e.g., so that this application can be prosecuted in a streamlined manner.

Consequently, if PTO personnel have any questions or concerns regarding the foregoing, they are requested to telephone or email Applicant's attorney using the contact information set forth below.

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Electronic Acknowledgement Receipt

EFS ID:	45357544
Application Number:	17479475
International Application Number:	
Confirmation Number:	7676
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Customer Number:	73091
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2021051 / RMS08BC2
Receipt Date:	30-MAR-2022
Filing Date:	20-SEP-2021
Time Stamp:	16:42:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Request for Reconsideration-After Non-Final Rejection	2022-03-30-Resp2OA-RMS08-BC2-INT.pdf	124842 065502dce66dc0ff9adee9e6ca4c3f1c6c1e310b	no	16

Warnings:

Information:	
Total Files Size (in bytes):	124842

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number:	17/479475
Confirmation Number:	7676
First Named Inventor:	Robert Lercari
Title:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
Filing Date:	09/20/2021
Attorney Docket:	2021051 / RMS08BC2

APPLICANT RESPONSE TO 1/04/2022 NONFINAL OFFICE ACTION

Samsung Ex. 1002, Page 58 of 249

In The Claims.

Please amend the claims as set forth below. This listing replaces all prior listings.

1. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of the incoming ~~data write requests,~~requests:

derive, from the accompanying incoming address information, a first address ~~portion,~~ portion and a second address portion ~~and a third address portion,~~

identify an addressed block device from the first address portion,

use a first division operation on ~~to derive~~ the second address portion, to identify an addressed segment within the addressed block device, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, identify from the first division operation ~~and use the first division operation to derive a~~the third address portion, and [[-]] use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the ~~incoming~~ data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests~~of the selected one of the erase units which was selected from the address value that was identified by the second division operation for the one of the incoming data write requests~~; and

wherein said circuitry is also to ~~the storage device is to, for each one of incoming erase requests received from a host,~~

~~derive a first address portion that identifies a host-selected block device,~~

~~derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and~~execute ~~the one~~ each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset ~~that correspond~~ corresponding to the ~~host-selected~~addressed segment that

was identified from the incoming address information accompanying the one of the incoming erase requests.

2. (Currently Amended) The storage device of claim 1 wherein:

said circuitry comprises at least one processor; and

the storage device further comprises instructions stored on at least one ~~non-transitory~~physical storage medium, said instructions when executed to control the at least one processor ~~so as to operate as special purpose circuitry~~.

3. (Currently Amended) The storage device of claim 1 wherein:

~~the storage device~~ said circuitry can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and is ~~the storage device comprises circuitry~~ to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host;

the request from the host to copy is to designate destination address information corresponding to the second physical storage location; and

the ~~storage device~~ circuitry is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.

4. (Currently Amended) The storage device of claim 3 wherein the ~~storage device~~ circuitry is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit.

5. (Currently Amended) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage ~~drive~~ device is to store the values representing a time since data was programmed on a basis that is respective to each structure of the number of structures, wherein each structure comprises at least one of a page or a unit of memory comprising one or more erase units of the flash memory, and wherein each value represents time since data was programmed into the respective structure.

6. (Currently Amended) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the ~~storage device comprises~~ circuitry is to fulfill the at least one ~~request~~ of the incoming requests by issuing commands to the flash memory for which a quantum of flash memory selected by the commands which are issued in response to the at least one request is dependent on the information transmitted to the host identifying the number of structures.

7. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit to a host information that identifies an amount of flash memory that is to be erased as a unit.

8. (Currently Amended) The storage device of claim 1 wherein ~~the addressed segment corresponds to an integer number of erase units, and~~ the third address portion specifies a location within a sequential range of locations that correspond to the ~~integer number of~~ erase units in the subset.

9. (Currently Amended) The storage device of claim 1 wherein the first division operation and the second division operation each subdivide a value obtained from ~~an~~ the incoming address information accompanying each of the write requests into respective bitfields.

10. (Currently Amended) The storage device of claim 1 wherein ~~the storage device further comprises circuitry to~~:

the storage device is to store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

the storage device is to compare the values representing time since data was programmed to at least one threshold;

upon detection that a specific one of the values has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit; and

the storage device is to remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit.

11. (Currently Amended) The storage device of claim 10 wherein:

the flash memory is to have block devices, one of the block devices being the addressed block device; and

the storage device is to identify, for the data being copied, an address of a logical erase unit ~~address~~, the logical erase unit being associated with the addressed block device to the exclusion of each other one of the block devices; and

the storage device is to remap a correspondence between the ~~logical erase unit~~ address of the logical erase unit and ~~from~~ the first physical erase unit to instead be between the address of the logical erase unit and the second physical erase unit.

12. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

~~the storage device further comprises circuitry to~~

the storage device is to store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory ~~space,~~ space;

the storage device is to compare the metadata to at least one ~~threshold,~~ threshold;

upon detection that specific metadata has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific metadata from a first physical erase unit to a second physical erase ~~unit,~~ unit; and

the storage device is to remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit.

13. (Currently Amended) The storage device of claim 1 wherein:

the erase units of the flash memory are physical erase units;

the ~~storage device~~ circuitry is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units; and

the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests.

14. (Currently Amended) The storage device of claim 1 wherein the storage device ~~further comprises circuitry~~is to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold; and

responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values.

15. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device is further ~~comprises circuitry to~~ to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices,

receive a query, issued by a host, directed to a specific one of the block devices, and

responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

16. (Currently Amended) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device is further ~~comprises circuitry to~~ to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space, and

receive a query, issued by a host, wherein said query is specific to one of the block devices, and responsive to the query, identify specific metadata, associated with the specified one of the block devices, and transmit information to the host that conveys the specific metadata.

17. (Currently Amended) The storage device of claim 1 wherein the storage device is further ~~comprises circuitry~~ to:

store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space;

compare the metadata to at least one threshold; and

responsive to detection that specific metadata has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

18. (Currently Amended) The storage device of claim 1 wherein:

~~the data access requests comprise write requests;~~

the flash memory comprises multiple planes; and

the ~~storage device~~ circuitry is to, for each one of a set of the data write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page.

19. (Canceled)

20. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information; ~~for each of incoming data write requests,~~

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address ~~portion,~~ portion and a second address portion ~~and a third address portion~~,

identify an addressed block device from the first address portion,

use a first operation on the second address portion to subdivide the incoming address information into first ~~respective~~ bit fields, ~~including the second address portion and the third address portion,~~ and to identify an addressed segment within the addressed block device ~~from the second address portion~~ from a first one of the first bit fields,

wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second one of the first bit fields as a ~~use a second operation to subdivide the~~ third address portion and use a second operation to subdivide the third address portion into second bit fields, to ~~respectively~~ identify an address value to select one of the erase units from a first one of the second bit fields and to identify a storage location within the selected one of the erase units from a second one of the second bit fields;

wherein said circuitry is to execute each one of the ~~incoming~~ data write requests by programming accompanying data into the storage location ~~of the selected one of the erase units which was selected from the address value~~ that was identified for that one of the ~~by the second division operation for the one of the incoming~~ data write requests;

wherein said circuitry is also to execute ~~the storage device is to, for~~ each one of the incoming erase requests ~~received from a host,~~

~~derive a first address portion that identifies a host-selected block device,~~

~~derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and~~

~~execute the one of the incoming erase requests~~ by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding ~~that correspond~~ to the ~~host-selected~~addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

21. (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of incoming ~~data write requests,~~ requests:

derive a first address ~~portion,~~ portion and a second address portion ~~and a third address portion~~,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the second address portion ~~incoming address information~~ into ~~respective~~ first bit fields, ~~including the second address portion and the third address portion,~~ and to identify an addressed segment within the addressed block device from a first one of the first bit fields, and to identify a third address portion from a second one of the first bit fields ~~the second address portion,~~ , wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to ~~respectively~~ identify an address value to select one of the erase units from a first one of the second bit fields, and to identify a storage location within the selected one of the erase units from a second one of the second bit fields;

wherein said circuitry is to execute each one of the ~~incoming~~ data write requests by programming accompanying data into the storage location ~~of the selected one of the erase units which was selected from the address value~~ that was identified for that one of the ~~by the second division operation for the one of the incoming~~ data write requests;

wherein said circuitry is also to ~~the storage device is to, for each one of incoming erase requests received from a host,~~

~~derive a first address portion that identifies a host-selected block device,~~

~~derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and~~

execute ~~the one~~ each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding ~~that correspond~~ to the addressed ~~host-selected~~ segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

22. (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level,

each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to receive from a host, and control execution of, incoming requests including ~~, for each of incoming~~ data write ~~requests,~~ requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;

wherein said circuitry is to, for each of the incoming requests:

derive, from the accompanying incoming address information, a first address ~~portion,~~ portion and a second address portion ~~and a third address portion~~,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the second address portion ~~incoming address information~~ into first ~~respective~~ bit fields, ~~including the second address portion and the third address portion,~~ and to identify an addressed segment within the addressed block device from a first one of the first bit fields and a third address portion from a second one of the first bit fields~~the second address portion~~, , wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and

for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to ~~respectively~~ identify, from a first one of the second bit fields, an address value to select one of the erase units and, from a second one of the second bit fields ~~to identify~~ a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the ~~incoming~~ data write requests by programming accompanying data into the storage location ~~of the selected one of the erase units which was selected from the address value~~ that was identified for that ~~by the second division operation for the~~ one of the incoming data write requests; and

wherein ~~the storage device~~said circuitry is also to execute, ~~for~~ each one of incoming erase requests ~~received from a host,~~

~~derive a first address portion that identifies a host-selected block device,~~

~~use the first division operation to derive a second address portion, to identify an addressed one of the segments within the addressed block device, and use the first division operation to derive address information for one or more erase units within the one of the segments addressed by the one of the incoming erase requests, and~~

~~execute the one of the incoming erase requests~~ by controlling erasure in the flash memory of the one or more erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.

23. (New) The storage device of claim 1 wherein the second address portion comprises a first set of bits and a second set of bits, the bits of the first set of bits being mutually-exclusive to the bits of the second set of bits, wherein the first division operation is to separate the first set of bits from the second set of bits, and the circuitry is to identify the addressed segment from the first set of bits.

REMARKS

In the Office Action mailed February 1, 2022, the Examiner issued a number of objections, a rejection under 35 USC 101 and a rejection under 35 USC 112, second paragraph.

Applicant respectfully requests reconsideration in view of the amendments set forth above.

Preliminarily, Applicant would like to thank the Examiner for an interview with the undersigned held on March 30, 2022, at 1130 Pacific time. At that interview, the undersigned discussed the changes effectuated by this amendment, as a draft, and it is believed that the Examiner agreed that these amendments would overcome the objections and rejections of record and lead to allowance. The Examiner is respectfully requested, should any issues remain, to telephone the undersigned using the contact information set forth below, to effectuate compact resolution of any such issue.

In an attempt to facilitate ease of discussing each position of the Office Action, Applicant sequentially addresses each of the Examiner's positions below using numbered paragraphs.

1. Objection, claims 1, 20-22. At pages 2-3 of the Office Action, the Examiner objects to each independent claim and requires Applicant to add a second and/or third colon to each claim. Applicant disagrees with the Examiner's position, but has added extra colons as 'required' by the Examiner.[1] It is therefore respectfully requested that this objection be withdrawn.

2. Objection, claim 11. At page 3 of the Office Action, the Examiner objects to use of the term "and other of the block devices" and asserts that this term is grammatically incorrect. It is believed that the amendment set forth above moots this objection, and therefore, reconsideration and withdrawal of this objection is therefore respectfully requested.

3. Objection, claim 20. At page 3 of the Office Action, the Examiner objects to claim 20 and asserts that the term "second operation" should be "second division operation" to be consistent with the other

[1]The Examiner appears to be focusing on her own grammatical stylistic preferences rather than a clarity issue. In this regard, a claim is a sentence, and there are many who believe that proper English grammar admits of only one colon per claim, e.g., to demark a subordinate clause or separate a list from a primary sentence topic. See, https://www.wipo.int/edocs/mdocs/aspac/en/wipo_ip_phl_16/wipo_ip_phl_16_t5.pdf (a patent claim is a single sentence with a colon separating a transitional phrase from the claim body, see, e.g., p. 24). Applicant also refers the Examiner to MPEP 608.01(m), which states that "there is no set statutory form for claims," "the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," and "[w]here a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation." Thus, the PTO Rules suggest that the primary way to clearly separate respective elements is by line indentation, not by inserting colons at multiple places within a claim. Thus, Applicant disagrees with the Examiner that colons are needed as implied by the Office Action. As noted however, in order to advance prosecution, Applicant has complied with the Examiner's request, by adding the requested colons.

independent claims. Applicant does not agree and respectfully requests reconsideration. In this regard, claim 1 simply refers to first and second division operations, whereas the other independent claims refer to first and second "operations" "to subdivide." The language is slightly different but is submitted to refer to the same feature, i.e., an operation "to subdivide" clearly also divides. Applicant has therefore not made the change requested by the Examiner and asserts that this claim feature is already consistent with the "division operations" referred to be the first claim set. Therefore, reconsideration is respectfully requested.

4. Rejection, 35 USC 112(b), claim 1. At pages 3-4 of the Office Action, the Examiner rejects claims 1-22 asserting that use of "a first address portion" to refer to a portion of incoming address information for write requests, and use of "a first address portion" to refer to a portion of incoming address information for erase requests is unclear, and states an indefiniteness issue. Applicant does not agree, but to advance prosecution, has amended the claims in a manner that should moot this rejection. The Examiner also rejected these claims because the claims stated that the recited "storage drive" processes erase request address information without specifying whether "the circuitry" used to process address information used to process write request addresses is the same. Here also, this is not a 112 issue, i.e., it can be, or in other embodiments, it doesn't have to be - this does not raise a clarity issue. Nevertheless, to advance prosecution, Applicant has amended the claims in a manner that should moot this rejection. Therefore, reconsideration is respectfully requested.

5. Rejection, 35 USC 112(b), claim 2. At pages 4-5 of the Office Action, the Examiner rejects claim 2 as allegedly indefinite, because it is not clear to the Examiner whether the recited instructions control all of or part of the circuitry of claim 1. This rejection is traversed; ALL integrated circuits are made up of combinations and permutations of transistors, gates, and other structures. Similarly, all microprocessors feature "some" circuit elements (e.g., an ESD structure on an input pin) that are not configured by software. In this regard, claim 2 simply recites that the circuitry of claim 1 can, in some embodiments, be implemented to include software and processor or other hardware that is configured by the software. This is what the term "comprises" means, e.g., as contrasted with "consists of." It is respectfully submitted that claim 2 would be readily understood by those having skill in the art simply to say that the "circuitry" of claim 1 can, within the more detailed subject matter circumscribed by claim 2, include a processor/configurable hardware and instructions (e.g., software) that configured that processor/configurable hardware. With all due respect, there will always, in any implementation, be "some" circuitry (e.g., a ground pin) not configured by software/instructions, and one having skill in the art would not be confused by this claim vernacular, i.e., the claim unambiguously recites that some portion of "the circuitry" of claim 1 is embodies as a combination of general purpose circuitry and instructions/firmware/software. So as to hopefully clarify the meaning of this language in the Examiner's eyes, Applicant has made some minor amendments to claim 2 to delete second

usage of the term "circuitry." Based on the foregoing, reconsideration of this ground of rejection is respectfully requested.

6. Rejection, 35 USC 112(b), claim 5. Applicant has corrected the term "drive" to instead refer to "device," as was originally intended. Also, the Examiner rejected this claim based on her reasoning that "it is unclear if the 'structure' in claim 5 is the same as an erase unit." This latter rejection, once again, does not state a 112 issue or any problem with clarity; that is, as would be well-known to those having skill in the art, time since data was programmed could be stored at a granularity of each page, or of each erase unit (e.g., the oldest data in that erase unit), or one some other basis. This claim is not rendered vague by specifying the granularity at which metadata is stored. Nevertheless, to advance prosecution, Applicant has amended the claim in a manner calculated to moot this ground of rejection, and reconsideration is respectfully requested.

7. Rejection, 35 USC 112(b), claim 6. Applicant has amended the claim in question in a manner that should moot this rejection, and therefore, reconsideration is therefore here also requested.

8. Rejection, 35 USC 112(b), claim 11. Applicant has amended the claim in question in a manner that should moot this rejection, and therefore, reconsideration is therefore here also requested.

9. Rejection, 35 USC 112(b), claims 12 and 15-17. Applicant has amended the claims in question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

10. Rejection, 35 USC 112(b), claim 13. Applicant has amended the claim in a question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

11. Rejection, 35 USC 112(b), claim 14. At page 7 of the Office Action, the Examiner rejected this claim saying that it is not clear whether the metadata represents a time since data was programmed in a particular erase unit or a time since data was programmed in a segment having such an erase unit. Applicant traverses this rejection, i.e., if a segment hypothetically has two erase units, and time since programming is stored for each erase unit, it is also stored for the segment, no? Consider for example a memory controller that stores a hypothetical age value of "5 minutes ago" for "erase unit 1" and of "6 minutes ago" for "erase unit 2," and that "segment A" corresponds to "erase units 1 and 2;" does not this memory controller NECESSARILY also store data for "segment A" indicating (the oldest) age of data in "segment A" (i.e., "6 minutes ago" in this hypothetical). Applicant does not see any lack of clarity at all, notwithstanding the Examiner's remarks, and respectfully requests reconsideration. It is additionally noted for the Examiner's convenience that "a time" will typically be embodied as the oldest age in a particular erase unit or group of erase units, i.e., evicting 'write cold data' and recycling each underlying erase unit promotes wear leveling by catching and forcing erasure of erase units that may evade garbage collection operations because associated data is only infrequently deallocated (i.e., these erase units continue to stay full and are not released, so they are not recycled by garbage collection processes which look for mostly-released erase units). It is submitted that

there is no lack of clarity in this claim, i.e., this claim says that a time since data was programmed is stored for a segment (and since in described embodiments it can be stored for each erase unit that is part of a segment, it is also necessarily stored by these embodiments for each segment).[2]

12. Rejection, 35 USC 112(b), claims 18-22. Applicant has amended the claims in question in a manner that should moot these rejections, and therefore, reconsideration is therefore here also requested.

13. Rejection, 35 USC 101, claim 2. At page 7 of the Office Action, the Examiner rejected claim 2 as allegedly constituting nonstatutory subject matter. Applicant notes that this issue has been thoroughly discussed in the sister applications and need not be discussed again herein in detail - a claim is not "directed" to nonstatutory subject matter unless a claim as a whole is determined to be so directed, which cannot be the case for a dependent claim only (i.e., which inherits structure, including without limitation, all statutory subject matter structure, from one or more claims on which it dependents); furthermore, "nontransitory" is expressly defined in the specification so as to refer exclusively to physical media. Nevertheless, to advance prosecution, Applicant has changed the language in question to refer to at least one PHYSICAL storage medium. It is respectfully submitted that this change should moot the issue the Examiner has, and therefore reconsideration and withdrawal of this rejection is respectfully requested.

CONCLUSION.

For the various reasons set forth above, Applicant respectfully requests reconsideration, with a favorable eye toward allowance. As this particular application has track one status, it is respectfully requested that if the Examiner still has issues (e.g., objections to claim language or rejections based on language or otherwise), the Examiner telephone the undersigned so as to discuss by interview, e.g., so that this application can be prosecuted in a streamlined manner.

Consequently, if PTO personnel have any questions or concerns regarding the foregoing, they are requested to telephone or email Applicant's attorney using the contact information set forth below.

Consequently, if PTO personnel have any questions are concerns regarding the foregoing, they are requested to telephone or email Applicant's attorney using the contact information set forth below.

[2]During the interview referenced above, the Examiner requested citation to some exemplary support for the position that a storage device can store metadata by EU or at other levels of granularity, such as by segment; Applicant notes that ample support exists for such operations, e.g., see the last sentence of paragraph 56 and incorporated by reference documents USPB 20140215129 and USPT 10642545 (USSN 14/848273, "Techniques for Data Migration Based On Per-Data Metrics and Memory Degradation"), e.g., especially col. 13, lines 15 et seq. of the latter. As stated by these documents, metadata including age metadata can be stored for any granularity of subdivision; as stated at col. 27, line 34, for example, each subdivision can be one *or more* erase units, and information can be filtered, e.g., the oldest age of any data in a subdivision. These support citations are exemplary.

Samsung Ex. 1002, Page 72 of 249

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/479,475	Filing Date 09/20/2021	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/30/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EFREM WARREN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

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EXAMINER	
WU, STEPHANIE	

ART UNIT	PAPER NUMBER
2133	

MAIL DATE	DELIVERY MODE
01/04/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 17/479,475	Applicant(s) Lercari et al.	
	Examiner STEPHANIE WU	Art Unit 2133	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 9/20/2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-22 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-22 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 9/20/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending in this application.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 9/20/2021 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

4. **Claims 1, 11, 20-22** are objected to because of the following informalities:

Claim 1 states "*[…] circuitry to, for each of incoming data write requests, derive a first address portion, a second address portion and a third address portion, identify an addressed block device […] wherein the storage device is to, for each one of incoming erase requests received from a host, derive a first address portion that identifies a host-selected block device […]*" it appears different derive and identify steps occur for incoming data write requests and incoming erase requests. It is suggested to amend to "*[…] circuitry to, for each of incoming data write requests[[,]]: derive a first address portion, a second address portion and a third address portion, identify an addressed block device […] wherein the storage device is to, for each one of incoming erase requests received from a host[[,]]: derive a first address portion that identifies a host-selected block device […]*"". This reduces any confusion over what steps are performed for specific types of requests, instead of general operation of the storage device. **Claims 20-22** contain similar limitations to claim 1, and require the same corrections.

Claim 11 states "*[…] the logical erase unit being associated with the addressed block device to the exclusion of each other of the block devices [...]*". The underlined portion of the claim is grammatically incorrect.

Claim 20 states "*[…] use a second operation to subdivide the third address portion […] the address value that was identified by the second division operation*", it appears the second operation was meant to state ""second division operation" to be consistent with later limitations.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1-22** are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

Claim 1 states "*[…] circuitry to, for each of incoming data write requests,*

derive a first address portion, a second address portion and a third address portion, […]

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and […]". The claims mention two different instances of a "first address portion" and a "second address portion", but each instance

is associated with a different type of request (write requests and erase requests). It is unclear if 1) the applicant intends both instances of "first address portion" to be the same address portion despite being part of different types of requests, 2) or if both instances of a "first address portion" are meant to be related (e.g. derived using the same technique), 3) or if neither instance of a "first address portion" are related at all. If the applicant intends to claim 3) it is suggested one of the instances of "first address portion" be renamed. The same issues apply for each instance of "second address portion". It is necessary to determine if there is any relationship between the different instances of first/second address portions, in order to determine the metes and bounds of the claim.

Additionally, the functions related to "incoming erase requests received from a host" are not associated with any type of circuitry, controller or other functional unit within the storage device. The applicant's specification gives multiple examples of how techniques are implemented in 0018 (controller, flash memory device, software), but only one embodiment can be claimed. It is requested the applicant clarifies how the functions related to "incoming erase requests received from a host" are carried out by the storage device. **Claims 2-19** depend from claim 1, and are rejected for at least the same reasons as claim 1. **Claims 20-22** contain similar limitations to claim 1, and are rejected for at least the same reasons as claim 1.

Claim 2 states "*The storage device of claim 1 wherein:*

said circuitry comprises at least one processor; and

the storage device further comprises instructions stored on at least one non-transitory storage medium, said instructions when executed to control the at least one processor so as to operate as special purpose circuitry." It is unclear how the special purpose circuitry is incorporated with the other circuitry mentioned in parent claim 1, and if the special purpose circuitry is supposed to perform the functions of the other circuitry (i.e. deriving a first address portion for incoming write requests) or other functions mentioned in parent claim 1 (i.e. deriving address portions for incoming erase requests received from a host). If the special purpose

circuitry is intended to perform the functions of the other circuitry, it is unclear if this special purpose circuitry is meant to replace the circuitry mentioned in parent 1 or operate in conjunction with said circuitry. It is necessary to define what functions each component in the storage device performs, in order to determine the metes and bounds of the claim.

Claim 3 states "*The storage device of claim 1 wherein: the storage device can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, […] and the storage device is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.*" Parent claim 1 states the first division operation is performed by an instance of "circuitry", but claim 3 does not associate using "the first division operation on the designated destination address information" with the aforementioned circuitry or with a new and different instance of circuitry. It is necessary to define what functions each component in the storage device performs, in order to determine the metes and bounds of the claim.

Claim 5 recites the limitation "the storage drive" in line 3. There is insufficient antecedent basis for this limitation in the claim. Additionally, claim 5 states "wherein each value represents time since data was programmed into the respective structure", however parent claim 1 states "programming accompanying data into the storage location of the selected one of the erase units". It is unclear if the "structure" in claim 5 is the same as an "erase unit", or if the programming data into erase units affects the "value" in claim 5 is affected by programming data into erase units. It is necessary to determine if there is any relationship between the programming of data in erase units and programming of data in structures, in order to determine the metes and bounds of the claim.

Claim 6 states "*[…] wherein the storage device comprises circuitry to fulfill the at least one request by issuing commands to the flash memory […]*'. Parent claim 1 mentions both "incoming data write requests" and "incoming erase requests", but claim 6 does not specify if

"the at least one request" refers to an erase request or write request (or both). The examiner suggests amending to "*[…] wherein the storage device comprises circuitry to fulfill ~~the at least one~~ each of the incoming data write requests and each of the incoming erase requests by issuing commands to the flash memory […]*". Additionally, it is unclear if the circuitry cited in claim 6 is associated with "said circuitry is to execute each one of the incoming data write requests" in parent claim 1, or the circuitry of claim 6 is a new and different instance of circuitry. It is necessary to define what functions each component in the storage device performs, in order to determine the metes and bounds of the claim.

Claim 11 states "*The storage device of claim 10 wherein: the storage device is to identify, for the data being copied, a logical erase unit address, the logical erase unit being associated with the addressed block device to the exclusion of each other of the block devices […]*". The limitation "the logical erase unit" in line 2 has insufficient antecedent basis.

Claim 12 states "*The storage device of claim 1 wherein: the flash memory is to have block devices[1], including the addressed block device; and the storage device further comprises circuitry to store metadata on an independent basis for flash memory[2] associated with each one of the block devices […]*". It is unclear how metadata is stored for independently for flash memory in [2] when claim 12 previously established the flash memory has multiple block devices at [1]. All stored metadata for a plurality of block devices in a single flash memory would be equivalent, as a single flash memory contains multiple block devices and the metadata is stored for "flash memory associated with each one of the block devices". It is suggested to amend the claims to state "*the storage device further comprises circuitry to store metadata on an independent basis for portions of flash memory associated with each one of the block devices […]*", if the intention was to claim portions (or subsets) of flash memory associated with each of the block devices to have corresponding stored metadata. **Claims 15-17** contain similar limitations, and are rejected for at least the same reasons as claim 12.

Claim 13 states "*The storage device of claim 1 wherein: the erase units are physical erase units; the storage device is to use the second division operation to identify a logical erase unit*", however parent claim 1 states the "second division operation" is performed by specific circuitry in response to incoming data write requests. It is unclear if said circuitry is performing the second division operation in claim 13, or with a new and different instance of circuitry. It is necessary to define what functions each component in the storage device performs, in order to determine the metes and bounds of the claim.

Claim 14 states "*The storage device of claim 1 wherein the storage device further comprises circuitry to: store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed […]*". It is unclear if the value represents a time since the valid data in a particular erase unit of a segment was programmed, or if the value represents a time since the most recent program operation occurred in the segment (i.e. the last time since any erase unit in the segment was programmed). The specification (particularly, incorporated spec 62/194,172 paragraph 0250) did not make the distinction.

Claim 18 states "*the data access requests*" in line 2, there is insufficient antecedent basis for this limitation.

Claim 19 states "*the storage drive*" in lines 1-2, there is insufficient antecedent basis for this limitation.

Claim 20 states "*the incoming address information*" in line 6, there is insufficient antecedent basis for this limitation. **Claims 21-22** contain similar limitations and are rejected for at least the same reasons as claim 20.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 2 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim(s) does/do not fall within at least one of the four categories of patent eligible subject matter because claim 2 states "*The storage device of claim 1 wherein: said circuitry comprises at least one processor; and the storage device further comprises instructions stored on at least one non-transitory storage medium*", however the applicants specification 0001 (between 0070 and 0071) defines non-transitory machine-readable media "as used herein means any tangible (i.e., physical) storage medium, irrespective of how data on that medium is stored". Paragraph 0001 also provides an example of non-transitory storage medium as stored on a distributed basis using servers, which would include transmission of data using signals. Signals are not within one of the four statutory categories.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Coffin et al. (U.S. PGPub No. 2017/0192901) teaches subdividing a physical address into to identify a physical address location at different physical memory tiers.

Ravimohan et al. (U.S. PGPub No. 2017/0199703) teaches dividing a metablock address to obtain die number and block number pairs

Shaharabany et al. (U.S. PGPub No. 2017/0109078) teaches dividing a logical block address

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHANIE WU whose telephone number is (571)272-0257. The examiner can normally be reached 11a-8p.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/STEPHANIE WU/
Examiner, Art Unit 2133

Notice of References Cited	Application/Control No. 17/479,475	Applicant(s)/Patent Under Reexamination Lercari et al.	
	Examiner STEPHANIE WU	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20170192901-A1	07-2017	Coffin; Jerome Vincent	G06F12/10	1/1
*	B	US-20170199703-A1	07-2017	Ravimohan; Narendhiran Chinnaanangur	G06F3/0659	1/1
*	C	US-20170109078-A1	04-2017	Shaharabany; Amir	G06F3/0613	1/1
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	Art Unit
	STEPHANIE WU	2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/30/2021								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	13	✓								
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	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	Art Unit
	STEPHANIE WU	2133

CPC - Searched*		
Symbol	Date	Examiner
G06F12/all, 109, 1036 (text limited)	12/29/2021	SW
G06F3/06xxxxxx, 0688 (text limited)	12/29/2021	SW
G06F2212/all (text limited)	12/30/2021	SW

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor search in PALM	12/27/2021	SW
Assignee search in SEARCH	12/27/2021	SW
Searched PE2E SEARCH, see attached history	12/27/2021	SW
Searched Google Patents + Scholar for "divide address channel plane die"	12/29/2021	SW

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/STEPHANIE WU/ Examiner, Art Unit 2133	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/479,475	Lercari et al.
	Examiner	Art Unit
	STEPHANIE WU	2133

/STEPHANIE WU/ Examiner, Art Unit 2133	

Bibliographic Data

Application No: 17/479,475

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /STEPHANIE WU/ Examiner's Signature | Initials

Title: ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/20/2021	711	2133	2021051 / RMS08BC2
RULE			

APPLICANTS

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INVENTORS

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Alan Chen, Simi Valley, CA, UNITED STATES

Mike Jadon, Manhattan Beach, CA, UNITED STATES

Craig Robertson, Simi Valley, CA, UNITED STATES

Andrey V. Kuzmin, Moscow, RUSSIAN FEDERATION

CONTINUING DATA

This application is a CON of 16808304 03/03/2020 PAT 11221959

16808304 is a CON of 15690006 08/29/2017 PAT 10642748

15690006 is a CON of 15074778 03/18/2016 PAT 9785572

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14880529 is a CIP of 14848273 09/08/2015 PAT 10642505

14880529 has PRO of 62199969 07/31/2015

14880529 has PRO of 62194172 07/17/2015

14880529 has PRO of 62063357 10/13/2014

14848273 has PRO of 62048162 09/09/2014

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

09/28/2021

**** SMALL ENTITY ****

STATE OR COUNTRY

UNITED STATES

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Saratoga, CA 95070
UNITED STATES

FILING FEE RECEIVED

$3,340

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Robert Lercari
Art Unit	
Examiner Name	unknown
Attorney Docket Number	2021051 / RMS-08BC2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	6134631	A	2000-10-17	Jennings III	
	3	7861122	B2	2010-12-28	Cornwell et al.	
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	7	7702846	B2	2010-04-20	Nakanishi et al.	
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.W/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Robert Lercari
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	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Attorney Docket Number	2021051 / RMS-08BC2

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	29	9400749	B1	2016-07-26	Kuzmin et al.	
	30	9519578	B1	0216-12-13	Kuzmin et al.	

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	First Named Inventor	Robert Lercari
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	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
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	Art Unit	
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	Art Unit	
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	Attorney Docket Number	2021051 / RMS-08BC2

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	Art Unit	
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	Art Unit	
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Signature	/Marc P. Schuyler/	Date (YYYY-MM-DD)	2021-09-20
Name/Print	Marc P. Schuyler	Registration Number	35675

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.W/

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	336	("10445229"|"10552058"|"10552085"|"10838853"|"20030028733"|"20030065866"|"20050073844"|"20050144413"|"20060022171"|"20070046681"|"20070058431"|"20070143569"|"20070233939"|"20070260811"|"20070283428"|"20080034153"|"20080082596"|"20080126720"|"20080147964"|"20080155204"|"20080189485"|"20080320476"|"20090036163"|"20090046533"|"20090083478"|"20090089482"|"20090089490"|"20090138671"|"20090172219"|"20090172246"|"20090172250"|"20090172257"|"20090172499"|"20090198946"|"20090254705"|"20090271562"|"20090292839"|"20090300015"|"20090327602"|"20100042655"|"20100115172"|"20100161882"|"20100162012"|"20100182838"|"20100191779"|"20100211737"|"20100241866"|"20100262761"|"20100262762"|"20100262765"|"20100262773"|"20100281230"|"20100287217"|"20100287327"|"20100287332"|"20100329011"|"20110033548"|"20110055445"|"20110066792"|"20110125956"|"20110153817"|"20110153911"|"20110161784"|"20110197023"|"20110238943"|"20110276756"|"20110296089"|"20110296133"|"20110314209"|"20120033519"|"20120054419"|"20120059972"|"20120066441"|"20120079174"|"20120131270"|"20120131381"|"20120159039"|"20120198129"|"2012	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:19 PM

		0204079"|"2013000734 3"|"20130013852"|"201 30019062"|"201300738 16"|"20130111295"|"20 130111298"|"20130124 793"|"20130138868"|"2 0130145111"|"2013016 6825"|"20130242425"|" 20130282955"|"201302 90619"|"20130297852"| "20130332656"|"20130 339580"|"20140101371 "|"20140122781"|"2014 0189207"|"2014018920 9"|"20140208004"|"201 40208062"|"201402151 29"|"20140237168"|"20 140297949"|"20150067 297"|"20150113203"|"2 0150134930"|"2015014 9789"|"20150193148"|" 20150212938"|"201502 61456"|"20150263978"| "20150309734"|"20150 324264"|"20150347041 "|"20150347296"|"2015 0355965"|"2015037861 3"|"20150378886"|"201 60018998"|"201600191 59"|"20160026564"|"20 160092116"|"20160179 664"|"20160202910"|"2 0160342509"|"2016035 7462"|"20160364179"|" 20170031699"|"201701 39838"|"20170220287"| "20170364445"|"55684 23"|"5652857"|"586008 2"|"6134631"|"7096378" |"7339823"|"7404031"|" 7406563"|"7581078"|"7 702846"|"7710777"|"77 52381"|"7801561"|"780 9900"|"7818489"|"7836 244"|"7861122"|"78775 40"|"7904619"|"794169 2"|"7970983"|"7991944" |"8001318"|"8024545"|" 8046524"|"8055833"|"8 065471"|"8065473"|"80 68365"|"8069284"|"807 2463"|"8074022"|"8082 389"|"8086790"|"80996 32"|"8285918"|"834704 2"|"8539197"|"8572331" |"8645634"|"9063844"|" 9176864"|"9229854"|"9 335939"|"9400749"|"95				

		19578"|"9542118"|"9588904"|"9652376"|"9696917"|"9710377"|"9727454"|"9785572"|"9846541").PN.					
L2	147	L1 AND (divid$4 division sub$1divid$4 sub$1divis$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:20 PM
L3	108	L1 NOT (radian).as. AND (divid$4 division sub$1divid$4 sub$1divis$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/27 11:21 PM
L4	36	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location))))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 12:29 AM
L5	43	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location))))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 12:29 AM
L20	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2	(US-PGPUB; USPAT)	OR	ON	ON	2021/12/29 01:04 AM

		(address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT ("radian").as,ASNM,AS TX,ASNP.					
L22	208	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:04 AM
L23	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:05 AM
L24	208	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:05 AM

		vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L25	2	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06F2212/7201 OR G06F2212/7208).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM
L26	17	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM
L27	24	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4) near6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 01:06 AM

		(address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L30	1	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 04:09 PM
L31	463	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/29 04:10 PM
L32	24	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 05:31 PM

		(address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.					
L34	1	((map$5 correspond$4 respectiv$4 associat$5) WITH (divid$4 division sub$1divid$4 sub$1divis$4 divisor) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 05:32 PM
L38	110	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit) hierarch$8 tier level)) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/109 OR G06F12/1036).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:12 PM
L39	43	L1 NOT (radian).as. AND ((divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) WITH (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:12 PM

		location))))					
L40	70	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! hierarch$5 (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor quotient) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06f3/0688).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 06:13 PM
L41	676	(((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:08 PM
L42	206	(hierarch$5 tier$3 level tuple) same2 (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:09 PM

		virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.					
L43	322	((hierarch$5 tier$3 level tuple) WITH (plane chip die channel bank eu! (erase NEAR unit))) AND (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME2 (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:09 PM
L44	163	((hierarch$5 tier$3 level tuple) WITH (plane chip die channel bank eu! (erase NEAR unit))) AND (((map$5 correspond$4 respectiv$4 associat$5) near5 (plane chip die channel bank eu! (erase NEAR unit))) SAME (divid$4 division sub$1divid$4 sub$1divis$4 divisor) near6 (address lba$1 lbn$1 lpa$1 lpn$1 lsn$1 lsa$1 la! vba$1 vbn$1 vpa$1 vpn$1 vsn$1 vsa$1 va! ((logical virtual) near2 (address$4 identif$9 number sequence location)))) AND (G06F12/$6 OR	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; IBM_TDB)	OR	ON	ON	2021/12/30 10:10 PM

		g06f3/06$5 OR G06F2212/$6).cpc. NOT (radian).as.					

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/479,475	09/20/2021	Robert Lercari	2021051 / RMS08BC2	7676

73091 7590 12/09/2021

Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

EXAMINER	
CENTRAL, DOCKET	
ART UNIT	**PAPER NUMBER**
OPAP	
MAIL DATE	**DELIVERY MODE**
12/09/2021	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/479,475	**Applicant(s)** Lercari et al.	
	Examiner CHERYL P GIBSON BAYLOR	**Art Unit** OPET	**AIA (FITF) Status** Yes

1. THE REQUEST FILED 20 September 2021 IS **GRANTED** .

   The above-identified application has met the requirements for prioritized examination
   - A. ☑ for an original nonprovisional application (Track I).
   - B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:
   - A. filing a **petition for extension of time** to extend the time period for filing a reply;
   - B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;
   - C. filing a **request for continued examination** ;
   - D. filing a notice of appeal;
   - E. filing a request for suspension of action;
   - F. mailing of a notice of allowance;
   - G. mailing of a final Office action;
   - H. completion of examination as defined in 37 CFR 41.102; or
   - I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to CHERYL GIBSON BAYLOR at (571)272-3213. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

Electronic Acknowledgement Receipt

EFS ID:	43974065
Application Number:	17479475
International Application Number:	
Confirmation Number:	7676
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Customer Number:	73091
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2021051 / RMS08BC2
Receipt Date:	07-OCT-2021
Filing Date:	20-SEP-2021
Time Stamp:	14:10:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	2021-10-07-PAM-RMS-08BC2.pdf	80420 44d087e9ee919b5254213c4f0df028d6890e3a44	no	10

Warnings:

Information:	
Total Files Size (in bytes):	80420

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number:	17/479475
Confirmation Number:	7676
First Named Inventor:	Robert Lercari
Title:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
Filing Date:	09/20/2021
Attorney Docket:	2021051 / RMS-08BC2

PRELIMINARY AMENDMENT

In The Claims.

Please amend the claims as set forth below. This listing replaces all prior listings.

1. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed block device from the first address portion,

use a first division operation to derive the second address portion, to identify an addressed segment within the addressed block device, and use the first division operation to derive the third address portion, and

use a second division operation ~~on the third address portion,~~ to identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation ~~of the third address portion within the selected one of the erase units identified~~ for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

2. (Original) The storage device of claim 1 wherein:

said circuitry comprises at least one processor; and

the storage device further comprises instructions stored on at least one non-transitory storage medium, said instructions when executed to control the at least one processor so as to operate as special purpose circuitry.

3. (Original) The storage device of claim 1 wherein:

the storage device can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and the storage device comprises circuitry to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host;

the request from the host to copy is to designate destination address information corresponding to the second physical storage location; and

the storage device is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.

4. (Original) The storage device of claim 3 wherein the storage device is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit.

5. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage drive is to store the values representing a time since data was programmed on a basis that is respective to each structure of the number of structures, wherein each value represents time since data was programmed into the respective structure.

6. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage device comprises circuitry to fulfill the at least one request by issuing commands to the flash memory for which a quantum of flash memory selected by the commands which are issued in response to the at least one request is dependent on the information transmitted to the host identifying the number of structures.

7. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit to a host information that identifies an amount of flash memory that is to be erased as a unit.

8. (Original) The storage device of claim 1 wherein the addressed segment corresponds to an integer number of erase units, and the third address portion specifies a location within a sequential range of locations that correspond to the integer number of erase units.

9. (Original) The storage device of claim 1 wherein the first division operation and the second division operation each subdivide a value obtained from an incoming address into respective bitfields.

10. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold;

upon detection that a specific one of the values has satisfied the one or more thresholds, copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit; and

remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit.

11. (Original) The storage device of claim 10 wherein:

the storage device is to identify, for the data being copied, a logical erase unit address, the logical erase unit being associated with the addressed block device to the exclusion of each other of the block devices; and

the storage device is to remap the logical erase unit address from the first physical erase unit to the second physical erase unit.

12. (Original) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory space,

compare the metadata to at least one threshold,

upon detection that specific metadata has satisfied the one or more thresholds, copy data stored at one or more physical storage locations associated with the specific metadata from a first physical erase unit to a second physical erase unit, and

remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit.

13. (Original) The storage device of claim 1 wherein:

the erase units are physical erase units;

the storage device is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units; and

the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests.

14. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold; and

responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values.

15. (Original) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices,

receive a query, issued by a host, directed to a specific one of the block devices, and

responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

16. (Original) The storage device of claim 1 wherein:

Samsung Ex. 1002, Page 132 of 249

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space, and

receive a query, issued by a host, wherein said query is specific to one of the block devices, and responsive to the query, identify specific metadata, associated with the specified one of the block devices, and transmit information to the host that conveys the specific metadata.

17. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space;

compare the metadata to at least one threshold; and

responsive to detection that specific metadata has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

18. (Original) The storage device of claim 1 wherein:

the data access requests comprise write requests;

the flash memory comprises multiple planes; and

the storage device is to, for each one of the write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page.

19. (Original) The storage device of claim 1 wherein for each one of the incoming erase requests, the storage drive is to perform a division operation to subdivide incoming address information accompanying the one of the erase requests, to identify a bit field that identifies an address-delimited subset of the host-selected segment for erasure.

20. (Currently Amended) A storage device comprising:

flash memory comprising erase units; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed block device from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation ~~of the third address portion within the selected one of the erase units identified~~ for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

21. (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an

addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation ~~of the third address portion within the selected one of the erase units identified~~ for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

22 (Currently Amended) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation ~~of the third address portion within the selected one of the erase units identified~~ for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

use the first division operation to derive a second address portion, to identify an addressed one of the segments within the addressed block device, and use the first division operation to derive address information for one or more erase units within the one of the segments addressed by the one of the incoming erase requests, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of the one or more erase units.

REMARKS

This preliminary amendment is being submitted prior to a first office action on the merits and is therefore believed to be submitted as a matter of right.

If the Examiner has any questions, or if it would be helpful for the Examiner to discuss this case or any particulars, or to achieve compact prosecution, the Examiner is respectfully requested to call the undersigned using the contact information presented below.

Respectfully submitted,

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35675
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Samsung Ex. 1002, Page 137 of 249

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/479,475	Filing Date 09/20/2021	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	10/07/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LDRC
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EVA V GILLIS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/479,475	09/20/2021	2139	1170	2021051 / RMS08BC2	22	4

CONFIRMATION NO. 7676

73091
Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

FILING RECEIPT

OC000000128743290

Date Mailed: 09/29/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

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Alan Chen, Simi Valley, CA;
Mike Jadon, Manhattan Beach, CA;
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Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 73091

Domestic Priority data as claimed by applicant

This application is a CON of 16/808,304 03/03/2020
which is a CON of 15/690,006 08/29/2017 PAT 10642748
which is a CON of 15/074,778 03/18/2016 PAT 9785572
which is a CON of 14/880,529 10/12/2015 PAT 9542118
which claims benefit of 62/199,969 07/31/2015
and claims benefit of 62/194,172 07/17/2015
and claims benefit of 62/063,357 10/13/2014
and is a CIP of 14/848,273 09/08/2015 PAT 10642505
which claims benefit of 62/048,162 09/09/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/28/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/479,475**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
**** SMALL ENTITY ****
Title

ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/479,475

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	22 minus 20 =	* 2	x 50 =	100	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1	x 240 =	240			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1170		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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First Named Inventor	Robert Lercari
Art Unit	
Examiner Name	unknown
Attorney Docket Number	2021051 / RMS-08BC2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
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	Examiner Name	unknown
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	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
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	First Named Inventor	Robert Lercari
	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Art Unit	
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	Art Unit	
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	Art Unit	
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	Application Number	
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	Art Unit	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Robert Lercari
	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Application Number	
	Filing Date	
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	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

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	Attorney Docket Number	2021051 / RMS-08BC2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Robert Lercari
	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

	10	Open NAND Flash Interface (ONFI), specification, version 3.1, 296 pages 09-19-2012	
	11	NVM Express, V. 1.2.1, 217 pages, 06/03/2016	
	12	Garth Gibson, Greg Ganger, "Principles of Operation for Shingled Disk Devices," Canregie Mellon Parallel Data Laboratory, CMU-PDL-11-107, April 2011, 9 pages	
	13	Li-Pin Chang, "Hybrid Solid State Disks: Combining Heterogeneous NAND Flash in Large SSDs," National Chiao-Tung University, Taiwan, ASPDAC 2008, 26 pages	
	14	Hua Wangx, Ping Huangxz, Shuang Hex, Ke Zhoux, Chunhua Lix, and Xubin He, "A Novel I/O Scheduler for SSD with Improved Performance and Lifetime," Mass Storage Systems and Technologies (MSST), 2013 IEEE 29th Symposium on, 6-10 May 2013, 5 pages.	
	15	Altera Corp. et al., "Hybrid Memory Cube" specification, 2012, 122 pages.	
	16	JEDEC Standard, JESD229, Wide IO, December 2011, 74 pages.	
	17	Li-Pin Chang, "Hybrid Solid State Disks: Combining Heterogeneous NAND Flash in Large SSDs," National Chiao-Tung University, Taiwan, 978-1-4244-1922-7/08, 2008 IEEE, 6 pages	
	18	Optimizing NAND Flash Performance, Flash Memory Summit, Santa Clara, CA USA August 2008, Ryan Fisher, pp. 1-23.	
	19	High-Speed NAND Flash: Design Considerations to Maximize Performance, Flash Memory Summit, Santa Clara, CA USA August 11,2009, , Robert Pierce, pp. 1-19.	
	20	NAND 201: An Update on the Continued Evolution of NAND Flash, Jim Cooke, Micron White Paper, September 6, 2011, pp. 1-10.	

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	Application Number	
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	First Named Inventor	Robert Lercari
	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

	21	Spansion SLC NAND Flash Memory for Embedded, data sheet, S34ML01G1, S34ML02G1, S34ML04G1, Sept. 6, 2012, pp. 1-73.	
	22	Wang et al., "An Efficient Design and Implementation of LSM-Tree based Key-Value Store on Open Channel SSD,"EuroSys '14 Proceedings of the Ninth European Conference on Computer Systems, Article No. 16, 2014-04-14, 14 pages.	
	23	Ouyang et al., "SDF: Software-defined flash for web-scale internet storage systems," Computer Architecture News - ASPLOS '14, Volume 42 Issue 1, March 2014, 14 pages.	
	24	Macko et al., "Tracking Back References in a Write-Anywhere File System,"FAST'10 Proceedings of the 8th USENIX conference on File and storage technologies, 14 pages, 2-23-2010	
	25	Ohad, Rodeh, "IBM Research Report Defragmentation Mechanisms for Copy-on-Write File-systems," IBM white paper, April 26, 2010, 10 pages, available at domino.watson.ibm.com/library/CyberDig.nsf/papers/298A0EF3C2CDB17B852577070056B41F/$File/rj10465.pdf	
	26	Michael Cornwell, "Anatomy of a solid-state drive," October 17, 2012, pages 1-13, https://queue.acm.org/detail.cfm?id=2385276.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Robert Lercari
	Art Unit	
	Examiner Name	unknown
	Attorney Docket Number	2021051 / RMS-08BC2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Marc P. Schuyler/	Date (YYYY-MM-DD)	2021-09-20
Name/Print	Marc P. Schuyler	Registration Number	35675

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2021051 / RMS-08BC2

Filed as Small Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
REQUEST FOR PRIORITIZED EXAMINATION	2817	1	2100	2100
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	2	50	100
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	1	240	240

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous-Filing:				
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**3340**

Electronic Acknowledgement Receipt

EFS ID:	43810763
Application Number:	17479475
International Application Number:	
Confirmation Number:	7676
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE
First Named Inventor/Applicant Name:	Robert Lercari
Customer Number:	73091
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2021051 / RMS-08BC2
Receipt Date:	20-SEP-2021
Filing Date:	
Time Stamp:	15:42:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$3340
RAM confirmation Number	E20219JF43302605
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	TrackOne Request	0-aia0424-prioritized.pdf	114577 9d69066c930067cb8f4c1517af0ed7b47f6f4ed2	no	2
Warnings:					
Information:					
2	Application Data Sheet	1-aia0014-ADS.pdf	1397391 d3fd2214aff042bde2910a3bc27e1225c5d95fe0	no	7
Warnings:					
Information:					
3		2-RMS-08BC2-Specification-FIN-2021-09-20.pdf	315666 4bf95a298ede86cf7f81ae995f42730484b6a60f	yes	42

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	32
Claims	33	41
Abstract	42	42

Warnings:					
Information:					
4	Drawings-only black and white line drawings	3-Visio-RMS-08-Drawings-2020-01-23-Generic.pdf	329016 63d9043d7ed06a89ac5a3f7e885c386e215b9cf5	no	10
Warnings:					
Information:					
5	Oath or Declaration filed	4-Robert-Declaration.pdf	935485 0c5bcfaabf76b7c9e66b1e052f9d0e73b61999f3	no	2

Warnings:					
Information:					
6	Oath or Declaration filed	5-aia0001-Declaration-AC-signed.pdf	652738 ff6a4b9924af00b08e16284553d69b96242dc184	no	2
Warnings:					
Information:					
7	Oath or Declaration filed	6-CR-Decl-efmc-cer.pdf	652701 fcd8176b3dc337bdcb7678811a14765290a18d6e	no	2
Warnings:					
Information:					
8	Oath or Declaration filed	7-MJadonExpositive.pdf	843399 512502d0821285ec293fb733a838069774c48410	no	2
Warnings:					
Information:					
9	Oath or Declaration filed	8-Andrey-Decl.pdf	1173656 7490c733d554fd6bd148f41662db8d266537a93a	no	2
Warnings:					
Information:					
10	Assignee showing of ownership per 37 CFR 3.73	9A-aia0096-AssnStatement-2021-09-20.pdf	120754 b1147d7f41a387083fa948a743be1f5ba5f8f3be	no	3
Warnings:					
Information:					
11	Power of Attorney	9B-aia0080-POA-2016-11-08-s.pdf	44477 2ad25a7b24c7336c2ae33911996154b407397931	no	1
Warnings:					
Information:					
12	Miscellaneous Incoming Letter	9C-IDS-cover.pdf	37892 a63faac281b7ce73d73cf02bcfd3493b71d7b108	no	1
Warnings:					
Information:					

13	Information Disclosure Statement (IDS) Form (SB08)	9D-2021-07-08-Updated-IDS.pdf	619879 4ae0b922c9c263922386f27eb6803f3a685ba07d	no	23
Warnings:					
Information:					
14	Fee Worksheet (SB06)	fee-info.pdf	55181 574c400f4092d4856e327b7649a3ff46f3870c0c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	7292812	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 73091

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 73091

OR

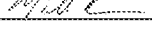
☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: Radian Memory Systems, Inc., 5010 N. Parkway Calabasas Unit 205, Calabasas, CA 91302

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	
Name	Mike Jadon	Telephone	
Title	Officer, Radian Memory Systems, Inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, and in compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, applicant submits attached Form PTO/SB/08a (EFS-Web) for consideration and request the references cited therein be made of record by the U.S. Patent and Trademark Office in the above-captioned application.

Applicant respectfully points out that the submission of the listed references in this Information Disclosure Statement is not an admission that they are prior art or that they are material to patentability of any claims of the application. Also, the submission of this Information Disclosure Statement is not an indication that a search has been made by Applicant.

It is respectfully submitted that copies of all cited materials (and translations, as appropriate) have already been cited in one or more parent applications relied upon for priority, in a manner compliant with 37 C.F.R. §1.98(a-c); these one or more applications are identified below -

USSN 16/808304, 15/690006, USSN 15/074778, USSN 14/880529 and/or USSN 14/848273

Accordingly, per the provisions of 37 C.F.R. §1.98(d), copies of such materials which were previously provided and are not again being provided herewith. To the extent not already submitted in connection with the referenced parent application, NPLs and Foreign References (and translations thereof, as appropriate) are being furnished herewith. Consideration of the foregoing plus the prompt return of a copy of the enclosed Form SB/08A with the Examiner's initials in the left column in accordance with MPEP §609 are respectfully requested.

Respectfully submitted,

September 10, 2021

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35,675
Attorney for Applicant

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Robert Lercari	Nonprovisional Application Number (if known):	
Title of Invention:	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Marc P. Schuyler/	Date 20 September 2021
Name (Print/Typed) Marc P. Schuyler	Practitioner Registration Number 35675

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2021051 / RMS08BC2
	Application Number	
Title of Invention	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2021051 / RMS08BC2
	Application Number	
Title of Invention	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2021051 / RMS08BC2
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Title of Invention	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE	

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Title of the Invention	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE		
Attorney Docket Number	2021051 / RMS08BC2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	16/808304	2020-03-03

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2021051 / RMS08BC2
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Title of Invention	ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE	

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/808304	Continuation of	15/690006	2017-08-29	10642748	2020-05-05

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/690006	Continuation of	15/074778	2016-03-18	9785572	2017-10-10

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/074778	Continuation of	14/880529	2015-10-12	9542118	2017-01-10

Prior Application Status: Expired — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/880529	non provisional of	62/199969	2015-07-31

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/880529	non provisional of	62/194172	2015-07-17

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/880529	non provisional of	62/063357	2014-10-13

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/880529	Continuation in part of	14/848273	2015-09-08	10642505	2020-05-05

Prior Application Status: Expired — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14/848273	non provisional of	62/048162	2014-09-09

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Application Number	Country	Filing Date (YYYY-MM-DD)	Priority Claimed
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ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

PRIORITY/INCORPORATION BY REFERENCE

[0001] This document is a continuation of US Utility Patent Application No. 16/808304, filed on March 3, 2020, on behalf of first-named inventor Robert Lercari for "Nonvolatile memory controller supporting variable configurability and forward compatibility," which in turn is a continuation of US Utility Patent Application No. 15/690006, filed on August 29, 2017, on behalf of first-named inventor Robert Lercari for "Memory Controller with multimodal control over memory dies" (issued on May 5, 2020, as US Patent 10642748), which in turn is a continuation of US Utility Patent Application No. 15/074778, filed on March 18, 2016, on behalf of first-named inventor Robert Lercari for "Expositive Flash Memory Control" (issued on October 10, 2017, as US Patent 9785572). US Utility Patent Application No. 15/074778, in turn, is a continuation of US Utility Patent Application No. 14/880529, filed on October 12, 2015, on behalf of first-named inventor Robert Lercari for "Expositive Flash Memory Control" (issued on January 10, 2017, as US Patent No. 9542118). US Utility Patent Application No. 14/880529 in turn claims the benefit of: U.S. Provisional Patent Application No. 62/199969, filed on July 31, 2015, on behalf of first-named inventor Robert Lercari for "Expositive Flash Memory Control;" U.S. Provisional Patent Application No. 62/194172, filed on July 17, 2015, on behalf of first-named inventor Robert Lercari for "Techniques for Memory Controller Configuration;" and U.S. Provisional Patent Application No. 62/063357, filed on October 13, 2014, on behalf of first-named inventor Robert Lercari for "Techniques for Memory Controller Configuration." US Utility Patent Application No. 14/880529 is also a continuation in-part of U.S. Utility Patent Application No. 14/848273, filed on September 8, 2015, on behalf of first-named inventor Andrey V. Kuzmin for "Techniques for Data Migration Based On Per-Data Metrics and Memory Degradation," which in turn claims the benefit of U.S. Provisional Patent Application No. 62/048162, filed on September 9, 2014, on behalf of first-named inventor Andrey V. Kuzmin for "Techniques for Data Migration Based On Per-Data Metrics and Memory Degradation." The foregoing patent applications are each hereby incorporated by reference, as are U.S. Patent Publication 2014/0215129, for "Cooperative Flash Memory Control," and U.S. Utility Patent Application No. 14/047193, filed on October 7, 2013, on behalf of first-named inventor Andrey V. Kuzmin for "Multi-Array Operation Support And Related Devices, Systems And Software."

TECHNICAL FIELD

[0002] The disclosure herein relates to non-volatile data storage and retrieval within semiconductor memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

[0004] Figure 1 illustrates an embodiment of a multi-modal flash memory device and its interconnection to a host system.

[0005] Figure 2 illustrates an exemplary application and configuration of a flash device having a pseudo-expositive memory controller within a host system.

[0006] Figure 3 illustrates an exemplary flash memory device in which discrete block devices may be configured and allocated as described in Figure 2.

[0007] Figure 4 illustrates an exemplary block device allocation and configuration within the flash device of Figure 3 effected using the block device allocator described in reference to Figure 2.

[0008] Figure 5 illustrates a host perspective of the exemplary block device allocations and configurations presented in Figure 4.

[0009] Figure 6 illustrates an exemplary pair of block device configurations.

[0010] Figure 7 illustrates exemplary generation of a physical block address in response to an incoming LBA.

[0011] Figure 8 illustrates a conceptual implementation of an address generation module.

[0012] Figure 9 illustrates exemplary virtualization of erase units within a four-die block device.

[0013] Figure 10 demonstrates an exemplary sequence of operations coordinated between a pseudo-expositive flash memory controller and a host file server.

[0014] Figure 11 illustrates forward (and reverse) compatibility between successive flash generations enable by a pseudo-expositive flash architecture provided by the teachings herein.

[0015] Figure 12 illustrates detail regarding pseudo-physical geometry export options within a flash device having multi-plane flash dies.

[0016] Figure 13 illustrates additional operations that may be managed by embodiments of pseudo-exposition.

[0017] Figure 14 illustrates a memory controller integrated circuit (IC).

[0018] The subject matter defined by the enumerated claims may be better understood by referring to the following detailed description, which should be read in conjunction with the accompanying drawings. This description of one or more particular embodiments, set out below to enable one to build and use various implementations of the technology set forth by the claims, is not intended to limit the enumerated claims, but to exemplify their application to certain methods and devices. The description set out below exemplifies addressing schemes and supporting, methods, devices, structures and systems. Such techniques can be practiced in one embodiment by a host, in another embodiment by a memory controller (e.g., within a single drive or across multiple drives), in another embodiment by a flash memory device (e.g., die or integrated circuit) and in yet another embodiment by a host or memory controller cooperating with one or more other circuits. This disclosure also provides improved designs for a memory controller, host, memory devices, a memory system, a subsystem (such as a drive, e.g., a solid state drive or "SSD"), and associated circuitry, firmware and addressing methodology. The disclosed techniques can also be implemented in software or instructions for fabricating an integrated circuit (e.g., a circuit design file or field programmable gate array or "FPGA" configuration). While the specific examples are presented, particularly in the context of flash memory, the principles described herein may also be applied to other methods, devices and systems as well.

DETAILED DESCRIPTION

[0019] A memory controller that subdivides an incoming memory address into multiple discrete address fields corresponding to respective hierarchical groups of structural elements within a target nonvolatile semiconductor memory system and in which at least one of the discrete address fields constitutes a virtual address for the corresponding physical element within the structural hierarchy is disclosed in various embodiments. Through this hierarchical subdivision, the virtual address portion of the incoming memory address is ensured to resolve to an element within the physical bounds of a larger (hierarchically-superior) structure, but may be freely mapped to any of the constituent physical elements of that larger structure. Accordingly, a host requestor may issue logical memory addresses with address fields purposefully specified to direct read, write and maintenance operations to physically distinct structures within the memory system in a manner that limits performance-degrading conflicts while the memory controller remains free, by virtue of one or more virtualized address fields within the incoming logical addresses, to virtualize localized groups of physical structures and thus mask defective structural elements and swap operational structural elements into and out of service, for example, as they wear or otherwise require maintenance.

[0020] In other embodiments presented herein, the net storage volume of a nonvolatile semiconductor memory system is subdivided into discrete performance-isolated storage regions based on specified system requirements and underlying memory system geometry and performance characteristics, with each such storage region being mapped by an independent linear range of logical addresses. Accordingly, each performance-isolated storage region may be presented to one or more host access requestors as an independent block device (i.e., mass storage unit having a continuously mapped logical address space) so that the nonvolatile memory system may be perceived by that host as being constituted by multiple discrete block devices, each having its own performance characteristics and address space. Moreover, the mapping of the logical address space within a given block device, referred to herein as "address space layout," may vary from one block device to another (e.g., sequential addresses within logical address ranges of respective block devices may be distributed within the structural hierarchy of the memory system in different order) to yield configurable and varied block device characteristics in terms of endurance and I/O bandwidth. Further, multiple different address space layouts may be applied within different "subspaces" of a given block device (i.e., discrete portions of the block device's address range) with, for example, addresses in one subspace being sequentially applied to structural elements at different hierarchical levels of the memory system in a different order

than in another subspace. Also, in a number of embodiments, system requirements specified (e.g., by a user/system designer) in terms of block device capacity and performance metrics including, without limitation, read and write bandwidth requirements and minimum data transfer size required by the block device, are automatically translated into corresponding configuration and allocation of structural elements as necessary to meet the high-level requirements, with such configuration and allocation optionally being programmed directly into the nonvolatile memory subsystem and/or corresponding block device definition reported to a host access requestor. By this approach, a system designer may configure and allocate block devices according to performance requirements of the application at hand without having to resort to the complex and error-prone task of allocating and configuring numerous physical resources within the nonvolatile memory system individually. Moreover, in a number of embodiments, high-level performance requirements specified to configure and allocate block devices within a given memory subsystem may be used to enable forward-compatible allocation and configuration of like-performance block devices within next-generation memory subsystems and thus enable seamless memory subsystem replacement (with or without data migration) and/or supplement with next-generation technologies. These and other embodiments, features and benefits are described in greater detail below in reference to exemplary drawing figures.

[0021] The nonvolatile memory subsystem in which a number of embodiments are detailed herein is presented as a flash memory device forming in whole or part a solid state disk drive (SSD); the flash memory device can be hierarchically arranged in multiple wired signaling channels each coupled to multiple flash memory dies, with each die including numerous individually erasable storage units ("erase units" or erase blocks or flash blocks) distributed in one or more access planes, and with each erase unit including numerous pages constituted by a predetermined number of single-bit or multi-bit nonvolatile storage cells (i.e., channels, dies, erase units and pages constitute, for example and without limitation, respective hierarchical physical elements within the flash memory device). For example, in one embodiment, a memory controller within the flash memory system (e.g., within the drive or SSD) subdivides each incoming "logical block address" (LBA) into respective channel, die, erase unit and page address fields, any or all of which may be virtual addresses, and resolves a commanded read or write access to a specific channel indicated by the channel address field, a specific die indicated by the die address field, a specific erase unit indicated by the erase unit field (including possible resolution to two or more erase units in the case of multi-plane command sequences) and a specific page indicated by the page address field (including possible resolution to two or more pages in the case of a multi-page operation).

[0022] Numerous specific details relating to flash memory device technology including, for example and without limitation, erase granularity limited to whole erase units (a fundamental characteristic of flash memory), usage-induced storage cell wear (i.e., as program and erase cycles involve destructive charge-carrier passage through isolating oxide layers) and finite storage cell retention times (largely due to leakage from floating storage cells which increases as feature sizes shrink in successive device generations) and disparate data write (or "program") timing and read timing constraints, bears on implementation and/or operational details of a number of embodiments presented below. In all cases, such details may change or be omitted when not required by the underlying memory technology. Thus, while the various embodiments presented herein are described in the context of flash memory devices, the structures and techniques disclosed are not so limited and may be applied with respect to any underlying memory technology wherever beneficial including both nonvolatile and volatile memory technologies.

[0023] Figure 1 illustrates an embodiment of a multi-modal flash memory device ("flash device") and its interconnection to a host system or device, referred to herein as the "host." As shown, the flash device includes multiple flash memory dies coupled to a multi-modal flash memory controller (MC). It should be understood that the memory controller is depicted in multiple locations within the figure, to illustrate different modes of operation; the memory controller itself includes a mode register or other configuration circuit which, when programmed by the host or pre-programmed during or after flash device production, enables the flash device to be selectively operated in any one of at least four different memory control modes including a physical access mode 112, a linearly virtualized mode 114, a cooperative management mode 116, and a hierarchically virtualized mode 118.

[0024] In physical access mode, shown generally at 112, the flash device takes little or no autonomous action and instead merely executes read, write and erase requests at the direction of the host. Thus, the host is fully aware of the underlying flash device geometry (shown, in this conceptual example, as three flash memory dies each having five erase units) and issues a physical block address (PBA) with each read/write request – that is a memory address having a fixed, one-for-one correspondence to a logical storage block (e.g., smallest addressable unit of data storage) within the collective storage space formed by the constituent flash dies of the flash device. An address received by the memory controller from the host is substantially identical to the address transmitted from the memory controller to memory; that is, the physical access mode enables executions of flash memory input/output operations (IOPs) with theoretically minimal latency (i.e., no address translation is needed

and the host can schedule IOPs in a manner that avoids resource conflicts due to full awareness of the underlying physical hardware and limitations thereof). In this mode, however, the host is burdened with numerous complex and hardware-specific media management tasks, including discovery and avoidance of failed structural elements (especially erase units and dies), leveling otherwise disparate wear between different erase units ("wear leveling"), reducing storage fragmentation ("garbage collection") as the ratio of partially filled erase units to available continuous storage space rises, and refreshing (i.e., re-writing in a new location) data nearing its retention time limit ("scrubbing" aged data). Thus design and implementation of a host system needed to interact with and manage the flash memory in physical access mode can become tremendously complex and, making matters worse, may require substantial and expensive re-design as new generations of flash memory devices become available.

[0025] Still referring to Figure 1, if physical access mode represents an extreme burdening of the host in return for potentially minimized IOP latency, the linearly virtualized mode shown at 114 represents the opposite extreme. In linearly virtualized mode, a flash translation layer (FTL) and media management engine are enabled within the memory controller to present the aggregate storage of the flash device (i.e., collective storage area within the three flash memory dies) to the host as a simple linear address range in which all media management operations are executed transparently (i.e., without host visibility or responsibility). While the FTL and under-hood media management tremendously simplifies host design and implementation, the cost of that simplicity is a substantial degradation of flash device performance and capacity. For example, because every logical block address issued by the host (e.g., LBA i-1, LBA i, LBA i+1, LBA i+2 as shown in Figure 1) may map to any storage location within the flash device (e.g., any page within any erase unit within any die on any signaling channel within the flash device), translation time tends to be substantial and increases exponentially as flash capacity grows (i.e., in new generations of flash devices). Worse, because the mapping of logical block addresses to underlying storage locations is invisible to the host, the host is unable to avoid sequential issuance of logical block addresses that resolve to the same flash die, meaning that resource conflicts may arise at random. From the host perspective, the I/O latency (i.e., time required to complete an I/O) is simply unpredictable and may, at any instant, grow many times beyond the native operational time imposed by the underlying flash die hardware. This unpredictable latency is made even worse by the memory controller's autonomous scheduling of flash maintenance operations (i.e., garbage collection, wear-leveling, data scrubbing) each of which tends to involve numerous memory-controller-initiated write operations followed by one or more relatively slow erase operations and thus may dramatically increase the I/O latency perceived by the host.

[0026] Continuing with the linearly virtualized controller mode 114, the memory controller's responsibility for flash maintenance requires that it keep substantial storage regions in reserve. Even more space is typically reserved to reduce the probability of worst-case resource conflict scenarios (i.e., limit occurrence of system-buckling long-latency I/O events). As a result, the overall flash memory capacity made available to the host in linearly-virtualized mode (i.e., the space encompassed by the linear LBA range) is generally substantially less than the physical capacity of the device. This "overprovisioning" of the physical storage space to meet a host-desired capacity and performance is exacerbated by the need for nonvolatile storage of the ever-growing FTL translation table (i.e., growing as the flash device capacity is consumed, and growing with new generations of more capacious flash devices) within the nonvolatile flash storage itself.

[0027] Still referring to Figure 1, the cooperative management mode shown at 116 achieves the performance advantages of physical access mode by exposing the underlying flash geometry to the host, but limits the host's flash management burden by gathering statistics needed to manage flash maintenance operations and by notifying the host when maintenance is required. The general approach is enumerated in the detail view of cooperative management mode and in which the host (1) requests and receives a physical geometry description from the memory controller (referred to herein as a "geometry export") and then (2) defines an address assignment in which the linear block address range of the host file system is mapped directly onto the physical block address within the underlying flash storage. In the particular example shown, a defective and unavailable erase unit marked by 'B' is reported to the host by the memory controller and noted within the LBA-to-PBA address map.

[0028] Hierarchically virtualized mode, shown for example at 118, takes cooperative management mode a significant step forward by presenting to the host an idealized view of underlying physical structures within the flash memory device. That is, as in cooperative management mode, the host requests a physical geometry description from the memory controller, but the memory controller returns, instead of a true physical description with all attendant details regarding defective storage and other realities, an idealized or pseudo-physical description of the underlying geometry that enables abstraction of the underlying flash memory structures without loss of coherence with respect to boundaries between hierarchical structures. Thus, in the hierarchically-virtualized example shown, the memory controller informs the host that the aggregate flash storage is subdivided among three flash dies and that four erase units are available within each flash die, holding in reserve some number of erase units (or dies or any other resource likely to fail over time) as necessary to maintain a static

idealized perspective of the underlying flash geometry for the host. Accordingly, despite the defective erase unit ('B') within the center flash die or even run-time detected failure of erase units within the other two flash dies, the host perceives a defect free set of physically extant dies and erase units therein. This pseudo-physical host perspective may be appreciated by comparing the host-perceived flash device architecture (three defect-free dies, each having four erase units) shown by the LBA to pseudo-physical block address (PPBA) mapping at 121 with the memory controller mapping of the LBAs to underlying physical block addresses (PBAs) as shown at 123. Whereas the host perceives a linear address mapping to the idealized physical storage (i.e., pseudo-physical storage), the memory controller maps the LBAs discontiguously, skipping over reserved and defective erase units, and thus virtualizing the pool of erase units within each individual flash die while maintaining the physical boundary between dies as reported to the host. Contrasting the cooperative management and hierarchically virtualized operating modes shown in Figure 1, the controller fully exposes the physical flash hardware in the cooperative management mode and exposes a pseudo-physical hardware set in the hierarchically virtualized mode and is thus referred to herein alternately as an expositive or pseudo-expositive memory controller when operating in those respective modes, with the pseudo-expositive memory controller being a specialized instance of the more general expositive memory controller.

[0029] Note that in the cooperative management mode 116 and the hierarchically virtualized mode 118, some limited amount of address translation can be performed at the memory controller, e.g., by translating the address of one block in the hierarchy (e.g., erase unit) while preserving logical location level at other address levels (e.g., preserving page ordering within a remapped erase unit); in the cooperative management mode 116, such remapping can be temporary (e.g., with the host ultimately being informed for example of bad block remappings, for example), and in the hierarchically virtualized mode 118, such remapping can be transparent, with a memory controller deriving for example, any of erase unit, page, die, plane, device, channel or other hierarchical address distinctions while preserving address-space division (e.g., logical order) at other levels. Among other advantages, this architecture provides for greatly simplified address translation (e.g., which can optionally be implemented entirely in hardware), and facilitates configurable and predictable I/O latency, and greatly shortens address translation time and associated complexity.

[0030] Figure 2 illustrates an exemplary application and configuration of a flash device having a pseudo-expositive memory controller (i.e., multi-mode memory controller operating in a pseudo-expositive mode, or memory controller having only a pseudo-expositive operating mode) within a host

system. In the particular embodiment shown, an interactive block-device designer/allocator is executed within either the flash device, host system and/or separate computing device to obtain flash device geometry and performance characteristics and interact with a system designer (i.e., user, system architect or other human operator or programmed intelligence) to define and allocate one or more discrete performance-isolated storage regions within the flash device. The block device designer/allocator ("block device allocator" for short) supplies parameterized descriptions of each allocated flash storage region to a host file system (i.e., one or more threads or processes executed on a host computing system to carry out file storage, retrieval and maintenance operations with respect to files and other data objects) which, accordingly perceives each such flash storage region as a linear range of logical block addresses and thus as an independent block device.

[0031] Still referring to Figure 2, and more specifically to the exemplary operational flow at 151, the block device allocator initially requests and receives geometry and performance data from the flash device and/or a device library at 155. In the embodiment shown and a number of embodiments described below, the geometry information includes hierarchical topology information including, for example and without limitation, (1) the number of independent flash-die access channels (also referred to herein as "signaling channels" or simply "channels") coupled to or otherwise accessible by the memory controller, (2) the number of discrete flash dies coupled to each access channel, (3) the number of erase-unit planes (or "planes" for short) within each flash die, (4) the number of erase units within each plane, (5) the number of pages per erase unit and (6) the storage capacity of each page. In general, each of the device geometry parameters may be a physical (i.e., actual) or pseudo-physical representation of the corresponding underlying hierarchical structure (e.g., channels, dies, planes, erase units or pages). Performance data, which may be viewed as part of the geometry export, may include for example and without limitation, (a) the nominal programming time of a physical page within the erase unit of a flash die (i.e., "t_{PROG}" also referred to herein as the page write time), (b) the nominal read time of the physical page (t_{READ}), (c) the nominal time required to erase contents within an erase unit (t_{ERASE}), (d) the data transfer bandwidth over an individual access channel (Chan BW), (e) the data transfer bandwidth of the host interface (H-Intf BW), (f) various performance enhancement/optimization functions that may be available (e.g., multi-page functionality, read caching, write caching, etc.), and so forth.

[0032] At 157, the block device allocator determines the available block device profiles (i.e., physical and performance characteristics of different configurations of physical resources within the

flash device) accounting for any pre-existing allocations. Assuming that no block devices have been allocated at this point and thus that resources sufficient for further block device definition remain within the flash device (i.e., negative determination at decision 159), then the block device allocator displays (e.g., in a visible display or other user interface of the computing device in which the block device allocator is instantiated) available block device profiles and the allocable quantities of each as shown at 161, prompting the user/designer to select one or more block device profiles and their desired allocation quantities. Upon receiving user input specifying a quantity of block devices having a given profile (and possibly multiple different profiles and respective quantities) at 163, the block device allocator prompts the user/designer to specify, for each block device to be allocated, whether the LBA range of the block device is to be uniformly sequenced among the hierarchical structures of the flash storage region to be allocated (e.g., channels, dies, erase units, pages) thus establishing a uniform address space layout (ASL) for the block device, or whether the address space layout is to be varied within one or more "subspaces" of the block device (i.e., "sub-ranges" of the overall LBA range for the block device). If subspace ASL is desired (affirmative determination at 165), the user is prompted to specify one or more specialized LBA ranges (i.e., LBA ranges having ASLs different from the otherwise uniform ASL corresponding to the block device profile). After receiving subspace ASL specifications, if any, for each user-requested block device, the block device allocator programs block device configuration registers 169 within the flash device (thereby allocating individually configured block devices within the flash device) and notifies the host file system of the block device allocation, supplying, for example a parameterized description of each block device that informs the host file system of the block device capacity (thus establishing the LBA range of the block device for a given LBA granularity), write bandwidth, read bandwidth and minimum data transfer size.

[0033] Note that the LBA granularity (i.e., size of a logical block of data – not to be confused with a block device which will typically hold millions of logical blocks of data each having a respective LBA) may be programmed within the block device configuration registers or other configuration storage of the flash device to enable a variable user-specified number of LBAs to span each physical page of storage within the flash device. Similarly, as discussed in greater detail below, the size of a logical quantum of data, referred to herein as a "host data segment" or "segment" and that constitutes a fundamental unit of storage allocation operated upon by the host file system, may be programmed within the block device configuration register to enable the memory controller to associate discrete sets of physical storage structures (e.g., an integer number of erase units within a given block device) with respective segments and thereby facilitate coordinated file-system and flash device management operations.

[0034] Continuing with the block device allocator flow, after programming the block device configuration registers and exporting corresponding block device parameters to the host file system at 169, the block device allocator returns to the space availability evaluation at 157, and determines the block device profiles and quantities thereof that remain available for allocation after accounting for any prior allocations at 169. If all available block devices are determined to have been allocated (i.e., all resources reported to be available by the flash memory device and/or library description of the flash memory device have been allocated in a block device definition or respective block device definitions), then the block device design/allocation operation is deemed complete and the block device allocator terminates. Though not specifically shown, the designer/user of the block device allocator may also terminate the block device allocation sequence without allocating all flash resources.

[0035] Reflecting on the block device allocation sequence shown in Figure 2, it should be noted that numerous additional provisions and or options may be implemented in various embodiments. For example, instead of executing the flash memory/file system configuration operation at 169 in each loop iteration, the block device allocator may accumulate an internal set of flash device and flash memory configuration parameters in each loop iteration, prompting the user/designer to review a comprehensive allocation plan before proceeding with flash device programming and/or file system notification. Also, instead of issuing configuration commands/parameters to the flash memory device and/or host file system, the block device allocator may write configuration information to one or more configuration files (or other data objects) for later delivery to actual flash memory devices or host file systems. Further, instead of iteratively prompting a user to select from among available block device profiles (which selection constitutes an implied or explicit user/designer specification of block device characteristics, including logical block size, read bandwidth, write bandwidth, capacity, transfer size, endurance metric, etc.), the block device allocator may initially receive desired block device performance parameters from a user/designer and thus proceed from the user's initial performance specification to resolve block device allocations. In yet other embodiments, the quantity of block devices and/or their individual characteristics may be determined in whole or part by user/designer specification of aggregate read or write bandwidth within the flash device as a whole (together with other "overall device" requirements, such as a minimum segment size, logical block size and/or transfer size), with the block device allocator allocating and configuring, for example, a minimum or maximum number of block devices as necessary to meet those aggregate requirements. Accordingly, the iterative block device allocation sequence shown in Figure 2 should be understood as but one of many possible block device allocation schemes which may be deployed in different embodiments or configurations.

[0036] Figure 3 illustrates an exemplary flash memory device in which discrete block devices may be configured and allocated as described in Figure 2. For purposes of explanation and understanding only, a specific flash device geometry and set of performance metrics are shown in Figure 3 and carried forward in a number of embodiments described in reference to following figures of the drawing. In all such cases, the specific geometries (e.g., numbers of physical elements at each hierarchy within the flash device structure including, without limitation, access channels, flash dies per channel, planes per flash die, erase units per plane, pages per erase unit, page size, page read and write times (t_{READ} and t_{PROG}), channel bandwidth and host interface bandwidth, number of host interfaces, etc.) may be different from those shown in Figure 3.

[0037] With that understanding, it can be seen that the exemplary flash device in Figure 3 includes a memory controller coupled to 16 access channels (ch0....ch16), with each access channel coupled to eight flash dies, each flash die having two planes, and each plane containing 1124 erase units (2248 erase units per die), and each erase unit containing 256 pages each containing a number of flash memory cells (e.g., NAND memory cells, though NOR or flash memory cell configurations may be deployed in alternative embodiments) sufficient to store 16kilobytes (kB) of data. As an aside, references to volumes of data herein are generally intended to mean a power of two quantity so that KB, MB, GB, TB, etc. refer respectively to 2^{10}, 2^{20}, 2^{30}, 2^{40}, etc. byte of data (sometimes designated by KiB, MiB, GiB, TiB and so forth).

[0038] Continuing with the flash memory embodiment shown in Figure 3, for purposes of example, it is assumed that the geometry exported to the block device allocator accurately reflects the underlying structural/physical hierarchy in all aspects but one – that the number of erase units per plane is reported pseudo-physically as 1024 (i.e., 2^{10} and thus 2^{11} or 2048 erase units per die) instead of 1124, meaning that 100 erase units per plane and thus 200 erase units per die are held in reserve. As explained below, this erase unit reservation or "spare pool" enables the memory controller to virtualize the available erase units within each die and thus mask defective erase units from host visibility and swap erase units into and out of service as storage for respective LBA ranges of an allocated block device without impacting the host perspective of the block device or the flash device as a whole. Also, it bears emphasis that each virtualized collection of erase units is confined to the individual flash die (or even the individual planes, depending on block device configuration) containing the corresponding physical erase units. That is, while a given LBA that resolves to a flash die may include a virtualized erase-unit address field (an example of a discrete address field within the LBA corresponding to a group of physical

elements within a structural hierarchy – erase units in this case), the LBA is nonetheless guaranteed by design to resolve to a physical erase unit with the LBA-specified physical die on the LBA-specified physical channel. More generally, as discussed in greater detail below, while any address fields (i.e., contiguous or discontiguous ranges of bits within an incoming LBA) corresponding to a hierarchical group of structures (e.g., channels, dies, erase units, pages) may be virtualized such that one or more of the corresponding hierarchical structures may be held in reserve, the address-space division between the hierarchical structures is maintained. Thus, once the channel field of an LBA is resolved to a particular channel, it is assured that, despite possible virtualization of the sub-hierarchical fields (i.e., die field, erase unit field and/or page field within the LBA), the LBA will ultimately resolve to a physical page on a physical die on that particular channel. This principle holds true for each level of the structural hierarchy so that once the LBA is resolved to a particular die, it is assured that the remaining erase unit and page fields, even if one or both are virtualized, will resolve to a physical page within that die, and likewise an LBA resolved to a particular erase unit is assured to specify a physical page within that erase unit, despite possible virtualization of the LBA's page field. Through this arrangement, it becomes possible to virtualize physical structures at each hierarchical level within the flash device while guaranteeing access to discrete subdivisions of the flash storage and thereby permitting, for example, specification of discrete subsets of dies and channels (or even finer-grained hierarchical elements where it makes sense to do so) to respective block devices specified within the block device configuration storage.

[0039] Figure 4 illustrates an exemplary (and not necessarily complete) block device allocation and configuration within the flash device of Figure 3 effected, for example, using the block device allocator described in reference to Figure 2. As shown, five block devices, BD0-BD4, are allocated, with each block device being constituted by one or more flash dies that are collectively associated with one or more memory channels (i.e., in this example, the smallest allocable block device is a single flash device). The block device configuration storage (BD Config) includes a block device lookup table (BD LUT) that is indexed by a block device identifier (BDid which may be, for example, a namespace or other handle or identifier) and holds, for example and without limitation, a specification of the one or more channels spanned by the block device (i.e., "constituent channels") and the one or more dies on the constituent channels. For instance, block device 0 (BD0) spans channels 0 and 1, and includes dies 0 and 1 on the constituent channels and thus includes four flash dies in all. Block device 1 is similarly defined as encompassing a 2x2 set of flash dies, but spans channels 2 and 3 instead of 0 and 1 and thus forms an entirely discrete storage area (i.e., no physical overlap) with respect to block device 0. Block device 2

spans a single channel (channel 0) and flash dies 2-5 on that channel, and thus also constitutes a four-die block device, but without the channel parallelism of block devices 0 and 1 (i.e., a 1x4 block device instead of a 2x2 block device). Block device 3 is also a four-die 1x4 block device, but is constituted by allocation of dies 2-5 on channel 1 instead of channel 0. Lastly, block device 4 is a 16-die block device that includes a single die (die 6) all 16 channels – that is, a 16x1 block device. Thus, of the overall set of five allocated block devices, four block devices (BD0-BD3) include discrete sets of four constituent dies and thus have a 32GB pseudo-physical storage capacity (i.e., each die includes a pseudo physical count of 2048 erase units, each containing 256 16KB pages and thus $2^{11}*2^{8}*2^{14}$ bytes or 8GB) and the fifth block device (BD4) includes a discrete set of sixteen dies and thus a 128 GB pseudo physical storage capacity. Also, in this particular example, the channel and die identifiers recorded within the block device lookup table correspond one-for-one with underlying physical channels and dies within the flash device as neither of those elements of the structural hierarchy are virtualized. In alternative embodiments or configurations of the flash device, either or both of those elements may be virtualized.

[0040] Continuing with Figure 4, each entry within the block device lookup table additionally includes an index to a respective set of one or more entries within an ASL lookup table (ASL LUT), with each ASL lookup table entry including ASL (address space layout) parameterizations and feature control settings for the complete or partial LBA range of the corresponding block device. In the particular example shown, ASL/feature-control parameter settings for three different block devices are illustrated, including a uniform ASL/feature-control parameterization within block device 0 (i.e., parameterization applies uniformly to the entire LBA range of the block device – there are no subspace definitions), another uniform ASL/feature- control parameterization with block device 2, and another multi-subspace ASL/feature-control parameterization within block device 4, with separate ASLs defined for each of multiple LBA ranges within the block device, only two of which are shown. Entries for block devices 1 and 3 are also present in the ASL lookup table, but not specifically shown in Figure 4.

[0041] As discussed above, the ASL parameters define the manner in which sequential LBAs are distributed within the structural hierarchy of the block device and thus indicate the number of pages within the same erase unit (i.e., "seqPg") to which sequential LBAs apply before progressing to page(s) in the next erase unit, and then the number of erase units to be sequentially accessed within a given die ("seqEU") before progressing to the next die, and then the number of dies to be accessed on a given channel ("seqDie") before progressing to the next channel. The feature control parameters include, for example and without limitation, whether read caching and write caching are to be enabled

(independently settable via the rdC and wrC fields of the ASL lookup table entry) for the block device or subspace thereof, the number of pages that may be simultaneously or concurrently written to or read from within the same erase unit (nPa), and the number of erase-unit planes to be concurrently accessed in a given write or read command sequence (nPl). In general, read caching is a double-buffering construct that enables data retrieved from an address-selected storage page and stored within the flash die's page register (i.e., a buffer element that temporarily holds outbound page-read data and inbound page-write data) to be output from the flash die concurrently with transfer of subsequently selected storage-page data to the page register, and write caching is a similar double-buffering arrangement that enables concurrency during page-write operations. Thus, the read and write page caching features, when enabled, reduce net latency of a sequence of read or write operations, respectively. In general, page caching scales (e.g., multiples according to cache depth) the effective size of the page register and thus correspondingly raises the minimum data transfer size imposed on the host in a given page read or write operation. For simplicity of understanding, page caching in both the read and write directions is disabled (i.e., "off") within the exemplary ASL lookup table entries shown. Multi-page operation (i.e., nPA set to a value greater than one) and multi-plane operation (nPl set to a value greater than 1) likewise raise the minimum data transfer size between the host and memory controller. In the specific examples shown in the ASL lookup table of Figure 4, multi-page operation is disabled at least within block devices 0, 2 and 4, and multi-plane operation is disabled at least within block devices 2 and 4. By contrast, dual-plane operation (nPl=2) is specified for block device 0, thus doubling the number of concurrently written pages (a block device characteristic referred to herein as a "stripe size" or "frontier width") as compared to a physically-comparable block device (e.g., block device 1) configured for single-plane operation.

[0042] Still referring to Figure 4, the singular values ('1') recorded for the LBA-sequencing ASL parameters within the ASL lookup table entry for block device 0 dictate that LBAs are to be distributed widely through the structural hierarchy of the flash device with, for example, each page of a sequentially addressed set of four pages (and thus a sequential range of 16 LBAs given the sLB=4KB logical block size setting) being read or written within a different one of the four constituent dies of the block device, thus effecting 4x ("multiplied-by-four") parallelism in the page read or write operation and thus approximately a 4x bandwidth increase over a configuration that directs four sequential page read or write accesses to the same erase unit within a given die. In actuality, the dual plane setting within block device 0 doubles the number of concurrently accessed pages within each of the four constituent flash memory dies of block device 0, thus establishing an 8-page stripe size and thus read and write

bandwidths that are approximately eight times the baseline single page read and write bandwidths of a given flash die. By contrast, block device 1 which otherwise constitutes the same 2x2 die-layout as block device 0, is configured with a deep (rather than wide) address space layout and with only single-plane access throughout its LBA range. Thus, pages falling within a sequential LBA range of block device 1 are mapped to physical pages within an erase unit until the end of that erase unit is reached (i.e., "Pg/EU"), with the LBA range thereafter continuing through the physical pages of a next erase unit and then the next until the final erase unit (EU/Die) within the die has been traversed, with the LBA range thereafter continuing through the pages and erase units of the next die on the same channel before carrying over to EUs and dies on an adjacent channel. In general because the stripe size is very narrow (i.e., a single page and thus as narrow as possible in the exemplary flash memory die shown), only a single erase unit is impacted by each page write operation and thus, despite the relatively low write bandwidth (i.e., $16KB/t_{PROG}$ in contrast to the $8*16KB/t_{PROG}$ bandwidth achieved by the 8x wider stripe size in block device 0), write-induced wear resulting from, for example, storage of a 16MB host segment, will occur in only a relatively small number of erase units and dies – four 4MB erase units within the same die in this example – in contrast to the storage of each of the 1024 16KB pages within a respective one of the 1024 erase units of block device 0 (i.e., each of the 256 erase units within each of the four dies is written to and thus worn to some degree). Conceptually, while the total page wear is equivalent in both block die configurations (the same number of pages is written), the wear within narrower-stripe-size (i.e., deeper, but lower bandwidth) block device 1 is concentrated within a much smaller number dies (and potentially erase units as well), simplifying wear-leveling operations and thus raising endurance of the block device as compared to wider, higher-bandwidth block device 0. In general, all these considerations are made available to the user/system designer in configuring the block devices, as the designer is able to directly, or with the aid of the block device allocator, specify ASL and feature-control parameters that strike a design balance between endurance and bandwidth requirements of a given application, potentially configuring block devices having widely varying performance characteristics within the same flash memory device, as illustrated by block devices 0-4 in Figure 4.

[0043] Concluding with Figure 4, the ASL lookup table includes multiple entries (and thus multiple subspace definitions) for block device 4, with an initial entry specifying a 4K LBA range (0-4095) mapped for high I/O bandwidth (i.e., 16-page stripe size as the write frontier spans all sixteen of the flash dies within the block device) and another entry specifying a subsequent 4K LBA range mapped for endurance (single-page stripe size). One or more other subspace definitions (not shown) complete the LBA range mapping of block device 4.

[0044] Figure 5 illustrates a host perspective of the exemplary block device allocations and configurations presented in Figure 4, showing relative block device capacities by the area/footprint of the block devices (as will be the case within the physical flash storage media) and illustrating relative block device bandwidths according to block device width (left-to-right across the drawing figure). Thus, block devices 0-3 all have the same four-die, 32GB capacity and thus have the same footprint (i.e., spanning an equivalent area within the figure), while block device 4, encompassing four times as many flash dies as each of the other block devices has a correspondingly larger 128GB capacity. Also, block devices 0, 1, 2, 3 and 4 are depicted with respective widths according to their nominal maximum I/O bandwidths of 8x, 1x, 1x, 2x and 16x, respectively, where each non-unity multiplier scales the baseline read and write bandwidths (i.e., $1/t_{READ}$ and $1/t_{PROG}$). As shown in detail view 251, the signaling bandwidth of block device 4 varies according to subspace, having a high (16x) bandwidth in the initial LBA range, and a 1x bandwidth in the LBA range that follows (i.e., in accordance with the respective subspace stripe sizes of 256KB and 16KB). Note also that actual block device bandwidths may be constrained by peak channel and/or host interface signaling rates, particularly in the case of memory read operations. For example, because the host interface is shared between all block devices (at least in the single host-interface embodiment shown in Figures 3 and 4) and individual access channels may be shared by as many as eight block devices (or more or fewer according to the number of flash dies per channel), operations executed in one block device may cut into the signaling bandwidth needed for peak-rate operation within another block device, particularly where numerous high-bandwidth block devices share the same signaling access channel or a large number of block devices are allocated within the flash device (which may saturate the host interface during occasional concurrent read access within a threshold number of block devices).

[0045] Figure 5 also presents a non-exhaustive list of flash device performance characteristics and features enabled by hierarchical address virtualization within the memory controller and configurable block device allocation, including (i) a configurable and predictable I/O latency, (ii) brief or otherwise negligible logical-to-physical ("L2P") address translation time (or at least dramatically reduced L2P time relative to operating modes that invoke a flash translation layer), (iii) allocation of discrete defect-free block devices in user-specified quantities and capacities, (iv) host-scheduled maintenance of flash-device-identified segments (or other logical units of storage), and (v) forward compatibility/ease of migration as flash device capacities and feature sets expand in successive device generations. Each of these characteristics/features is discussed in greater detail below.

[0046] Figure 6 illustrates an exemplary pair of block device configurations that demonstrate the configurable and predictable I/O latency enabled by the pseudo-expositive flash device described above (i.e., flash device having a pseudo-expositive memory controller) and the user-configurable block device allocation therein. These configurations will be respectively referred to as "configuration A" and "configuration B," with it being understood that a device may be reconfigured dynamically or otherwise as desired, as indicated by the presence of a migration arrow separating these two configurations. As shown, each of the block configurations features a 2x2 disposition of four dies (i.e., two dies coupled to channel 0 and two dies coupled to channel 1) and two planes of erase units within each die. That is, the block device configurations represent physically identical geometry and capability. However, by programming a wide and shallow ASL (i.e., ASL parameters set to distribute sequential LBAs through a minimum number of physical structures at each level of the structural hierarchy) and enabling dual-plane operation, an 8-page I/O stripe width is implemented with block configuration A and thus an 8 page/t_{PROG} write bandwidth and 8 page/t_{READ} read bandwidth, assuming sufficient overhead within the host-interface and flash-die access channels (as indicated by the 8 EU's in bold in the left-most grouping of 4 dies in figure 6). By contrast, block device configuration B features a narrow and deep ASL (i.e., ASL parameters set to distribute sequential LBAs through a maximum number of physical (or pseudo-physical) structures at each level of the structural hierarchy) and for single-plane operation, so that a single-page stripe size is established and thus write and read bandwidths of only 1 page/t_{PROG} and 1 page/t_{READ}, respectively. As explained above, the sequencing of LBAs through all the physical (or pseudo-physical) structures of a given die before proceeding to the next die increases endurance of the block device relative to its wider-stripe-width counterpart. Accordingly, the ASL of a given block device within the pseudo-expositive flash device may be tuned to meet endurance and bandwidth targets of a given application.

[0047] Figure 7 illustrates an exemplary generation of a physical block address in response to an incoming LBA (i.e., logical block address provided by host in connection/association with a memory access or maintenance operation) and block device ID (BDid). As shown, the block device ID is applied to a block device lookup table (e.g., as described in reference to Figure 4) to retrieve information identifying the channels and dies that constitute the block device (i.e., allocated to the block device) and thus, base die and base channel values that specify starting boundaries within a physical or pseudo-physical die matrix, together with parameters that indicate a number of channels and dies per channel spanned by the block device (Chans, Dies/Chan). In other embodiments, the constituent dies and

channels of the block device may be specified in other ways (e.g., list of specifically identifiable dies, starting channel/ending channel together with starting die/ending die, etc.).

[0048] In the implementation shown, the block device lookup table also outputs an ASL lookup address to the ASL lookup table. The ASL lookup table, in turn, outputs the recorded ASL parameters (including logical block size if implemented as a variable parameter) to an ASL generation logic block which in turn outputs an address-space-layout value that enables the incoming LBA to be decomposed into a set of hierarchical "sub-address" values, one sub-address for the group of elements at each respective level of the structural hierarchy within the flash device (e.g., channel sub-address, die sub-address, erase-unit sub-address, page sub-address).

[0049] This LBA decomposition into sub-addresses is easiest understood by considering the special case in which each sub-address maps to a power-of-two number of corresponding hierarchical elements (e.g., 2^4 channels, 2^3 dies per channel, 2^{11} erase units per die, 2^8 pages per erase unit) as, in that case, the ASL indicates, in effect, the location of discrete bit fields within the incoming LBA that correspond to respective levels of the structural hierarchy. Moreover, as shown in the shaded examples of ASLs for block devices 0-4 (BD0-BD4) at, the ASL also identifies the position of each discrete bit field within the ASL – a consequence of the sequential LBA assignment parameters described above in reference to Figures 4 and 5. Considering the ASL for block device 0, for example, it can be seen that, except for the page offset fixed at the lowest bits of the incoming LBA, the channel sub-address field constitutes the least significant field of the BD0 ASL, followed by the die sub-address field, the erase-unit sub-address field and then the page-address sub-address field. Accordingly, assuming for example that the page offset is a two-bit field such that four logical blocks are stored within each flash page, then every fourth LBA in a linear sequence of LBAs will be written within a die on a different channel with modulo wrap around to an initial channel after a die on the final channel has been written. By contrast, the sub-address (or field) order in the block 1 ASL is exactly the opposite that of block device 0 (excepting the least-significant page offset field), such that pages are sequenced first, then erase-units, then dies, and then channels at the end.

[0050] Continuing with Figure 7, as the ASL indicates how the individual hierarchical sub-address fields have been packed or encoded within the incoming logical block address, that value is supplied to pseudo-physical address generator and used therein to extract (or unpack or decode) or otherwise recover the individual hierarchical sub-addresses. In the particular example shown, the erase-unit sub-address (EUvirt) is assumed to be a virtual address (e.g., resolving between 2048 possible erase units

within a die having, in actuality, some larger number of erase units) which is therefore supplied to a sub-address translation table (or lookup table) for un-mapping to the physical address of the erase unit to be accessed. In the particular example shown, the remaining sub-address fields are assumed to be physical addresses corresponding to respective levels of the structural hierarchy so that those sub-address fields, together with the output of the translated erase-unit address (EUphys) constitute a physical block address that may be supplied to address decoding logic to issue the necessary control and enable signals to effect access to the specified page of flash storage (at the offset specified by the page offset).

[0051] In an alternative embodiment, the channel, die, page and page-offset sub-addresses (or any subset thereof) recovered from the LBA are also virtual addresses and thus supplied to respective sub-address translation or lookup tables (Ch LUT, Die LUT, Pg LUT, PO LUT) to obtain or generate the corresponding physical sub-addresses. More generally, any or all of the sub-address fields (including the page offset) recovered from the inbound LBA may be virtual addresses that are converted to physical addresses through translation/lookup operations. Also, two or more of the lookup tables for different hierarchical levels may be merged or combined. For example, the channel and die lookup tables may be merged to enable a two-dimensional lookup, thus virtualizing the die array as a whole and enabling any die on any channel to be interchanged (i.e., through virtual-to-physical address translation) with any other die on the same channel or any other channel.

[0052] A conceptual view of an erase-unit virtual-to-physical (V2P) translation table implementation is shown conceptually in the bottom portion of Figure 7 to demonstrate that a channel and die, selected by one of numerous constituent erase-unit lookup tables (or translation tables) is selected to yield the physical erase-unit address (i.e., to provide for independent erase-unit mapping from die to die). Various other implementations may be deployed in alternative embodiments.

[0053] A number of points bear emphasis in view of Figure 7. First, as the individual sub-address fields are, by virtue of block device and ASL programming, modulo-encoded into the incoming logical block address (e.g., as respective bit-fields in the power-of-two example shown), the sub-address values may be deterministically (e.g., algorithmically) recovered from the logical block address extremely quickly and efficiently, avoiding altogether the generally enormous translation data storage (e.g., trie structures and the like) and extensive translation times required for FTL operating modes or implementations. Moreover, the very presence of the sub-address values within the logical block address (i.e., the logical block address may be viewed as a tuple of the hierarchical sub-address values made possible by the pseudo-physical specification of the block device and in which the sub-address

values that form the tuple may be re-ordered in a variety of ways and even fragmented in accordance with the user-specified address space layout for a block device or subspace therein) effects an assurance to the host that LBAs containing the same sub-addresses down to a given hierarchical level will resolve to the same physical resource. For example, LBAs containing the same channel sub-address are ensured to access a die on the sub-address-identified channel. Similarly, LBAs containing the same channel and die sub-addresses are ensured to access an erase unit within the same die, and so forth. Moreover, any of the sub-addresses may be encoded into the LBA as a virtual address – that is a sub-address value that virtualizes the corresponding (and compartmentalized) physical resource. Thus, even though a given LBA may be assured to resolve to a desired die (virtual or physical), a virtualized erase-unit sub-address enables the underlying physical resources within that die to be swapped in and out of service as necessary, all without impacting the linear address space and performance perceived by the host.

[0054] Also note that the depicted architecture permits address translation to be reduced to relatively simple operations that can be implemented using logic gates and lookup tables, that is, in a manner that can be performed extremely fast, e.g., on an intra-cycle basis (i.e., in less than a clock cycle) or at most using only a handful of clock cycles. For example, as will be discussed below, a memory controller can offload address translation to a set of logic gates and prepopulated lookup tables, which can perform address translation without requiring processor clock cycles. On-board logic can then update the lookup tables and/or metadata as appropriate, in a manner that does not encumber I/O latency. By contradistinction, conventional flash memory tables which map a logical page address to potentially any wordline in flash memory device typically require gigabit-size translation tables, with translation only being performed using a substantial number of using processor cycles. This architecture, once again, helps streamline I/O latency, rendering it far more predictable, and reduces address translation time to a negligible quantity.

[0055] As discussed above, the exemplary ASL bit-field maps shown in Figure 7 for the different block devices assume a power-of-two quantity of physical resources at each hierarchical level in the flash. In the more general case, the resources at any or all physical levels may not be power-of-two quantities and thus complicate the picture of sub-address encoding. For example, assuming a 3-channel, 5-die block device allocation in which each die contains 2000 pseudo-physical erase units and 400 pages per erase unit, the total LBA range (assuming four LBAs per page) will span from 0 to 3*5*2000*400*4 (where '*' denotes multiplication) and thus from 0 to 48,000,000-1 and thus only part of the range represented by the smallest sufficient binary address size 2^26. Moreover, because each

element of the tuple that constitutes a given logical block address ranges between 0 and a non-power-of-2 maximum (i.e., magnitude of individual tuple elements are not, in all cases, power of 2 numbers), the sub-addresses of different hierarchical groups of structures (i.e., channels, dies, erase units, pages, etc.) do not fall within discrete bit fields. Said another way, the power-of-two ASL examples shown in Figure 7 are a special case of a more general solution in which sub-address fields are recovered using modulo arithmetic that reflects the tuple composition of the logical block address. Once again, as depicted, such an architecture can be easily implemented entirely or primarily in hardware, thus reducing translation times to negligible levels.

[0056] Figure 8 illustrates a conceptual implementation of an address generation module that may be used to extract (or recover) sub-address values from an inbound LBA regardless of whether the magnitude of individual tuple elements (i.e., number of channels, number of dies/channel, number of erase units/die, number of pages/erase unit) are power-of-two numbers or not. As in Figure 7, any or all of the hierarchical sub-address values, once recovered, may be converted from virtual to physical sub-addresses to collectively form an inbound physical block address (PBA), adding offsets to reflect the base channel and base die of the block device. For reasons discussed in further detail below, the address generator is implemented bi-directionally. That is, essentially the same operations executed to yield a PBA from an inbound LBA may be executed in reverse to produce an outbound LBA from a physical block address, thus enabling status regarding a given physical resource within the flash device to be reported to the host in terms of the LBA mapping that the host understands. Note that this information can be used to provide context to a host in order for a host to schedule maintenance or data movement (e.g., data migration or garbage collection) to preselected locations (e.g., where the logical address locations corresponding to the data are matched to the wear of a destination physical location, or where logical address locations having similar age, write frequency and/or read frequency characteristics are grouped together), as discussed in the copending application "Techniques for Data Migration Based On Per-Data Metrics and Memory Degradation" which as been incorporated by reference, as noted earlier.

[0057] Referring first to the inbound LBA path, an ASL value (e.g., generated per the ASL lookup table entry as discussed in reference to Figure 7) that describes the order of tuple elements within the inbound LBA is supplied to a pair of steering circuits that yield a set of divisors -- products of individual tuple elements. More specifically, a magnitude steering circuit selects, as magnitudes of the three least significant tuple elements within the inbound LBA (a four-tuple LBA is assumed in this example, having as tuple elements, a channel sub-address, die sub-address erase-unit sub-address, and page sub-address

in any order), from among the block device configuration settings for structural element quantities (i.e, number of allocated channels, number of allocated dies, number of allocated erase units, number of allocated pages) to produce divisor values that reflect strides within the LBA (after scaling to account for the page offset -- the "scaled LBA" or "offset-scaled LBA") at which boundaries between different members of the same structural group occur. Thus, in the 3-channel, 5-die, 2000 erase-unit, 400 page example above, if the tuple elements are ordered from most to least significant as channel sub-address, die sub-address, erase-unit sub-address, page sub-address, then the tuple element magnitudes will be 400, 2000, and 5, for elements 0, 1 and 2, respectively. Accordingly, the divisors supplied to the divisor steering logic will be DM1=200, DM2=400*2000=800,000 and DM3=400*2000*5=4,000,000. The divisor steering logic serves to route the divisors to the appropriate sub-address generation paths according to the tuple order specified in the ASL value and thus, continuing with the 3 channel, 5 die, 2000 erase unit, 400 page example (i.e., in tuple notation: "(3,5, 2000, 400)"), the channel sub-address path will receive the 400*2000*5 divisor (reflecting that a different channel is specified at each 4,000,000 increment in the scaled LBA), the die sub-address path will receive the 400*2000 divisor (reflecting that a different die is specified at each 800,000 increment in the scaled LBA) and the erase-unit sub-address path will receive the 400 divisor (reflecting that a different erase unit is specified at each 400 increment in the scaled LBA). The sub-address path for the least significant tuple element will receive a unity divisor (i.e., '1'), reflecting that a different page is specified at each increment of the scaled LBA.

[0058] Still referring to the inbound LBA path of Figure 8, after divisors have been applied to the scaled LBA (i.e., integer division as reflected by the '/' operator in divider logic elements), the results (integer-valued quotients) are subject to modulo operations (i.e., modulo 400, 2000, 5 and 3 for the respective sub-addresses) within the "mod" logic elements to yield sub-address values which, in the example shown, are assumed to be virtual sub-address values. As shown, the virtual sub-addresses are supplied to respective (or joint) lookup/translation modules to generate physical sub-address counterparts generally as described above in reference to Figure 7. Any or all of the modulo logic outputs may be physical sub-address values in alternative embodiments.

[0059] Still referring to Figure 8, the outbound PBA/LBA path is essentially the reverse of the inbound path, converting physical sub-address into virtual sub-addresses as necessary, multiplying by the steered divisor value (now a multiplier and hence a "divisor-multiplier"), and then summing the multiplied sub-address values to form the four-tuple LBA output (merging in the page offset to yield the full-range rather than offset-scaled LBA).

[0060] Figure 9 illustrates an exemplary virtualization of erase units within a four-die (2 dies by 2 channels) block device that demonstrate the discrete defect-free block device exposition enabled by the various pseudo-expositive flash device embodiments described above. In the example shown, the ASL is configured similarly to that of block device in the left-most portion of Figure 6, but with only single-plane operation, thus establishing a four-page stripe width. For purposes of example the erase units into which the first sixteen pages of data are enumerated within the erase-unit elements themselves. Further, it is assumed that the erase unit population is larger than the virtual erase unit address field within each incoming LBA such that some number of spare erase units is available within each die. Accordingly, upon determining that the erase unit shown at the bottom right corner of the fourth die is defective, the pseudo-expositive memory controller remaps the LBA that would otherwise resolve to the defective erase unit to a spare erase unit within the same die. That is, the fifth page of data that might otherwise be written to the defective erase unit is, through translation of the virtual address field within the incoming LBA to a physical address field as discussed above, re-directed to the spare page entirely transparently to the host write requestor. Impending run-time detected erase-unit failures in dies marked 'X' result in similar re-mapping and data move operations (i.e., prior to complete failure of the suspect erase units) again permitting the host to perceive the block device as a discrete defect-free storage entity. As discussed above, any other resources within the structural hierarchy of the flash device (including particularly those most likely to fail), such as dies, planes, pages or even channels may be virtualized and pseudo-exposed to the host in a manner that preserves one or more spares. In all such cases, the host may configure the number of structural elements reserved as spares on a flash-device-wide or block-device basis, for example, after requesting and receiving a physical geometry description from the flash device, including a reporting of the number of failed or suspect elements at each level of the structural hierarchy. Such spare-setting (or reserve pool specification) may be carried out, for example, in connection with block device programming within the block device allocator described above in reference to Figure 2 (e.g., programming the number of spares to be reserved, percentage of spares to be reserved, size of virtual address field and thus the allocable number of structural elements, etc.) and may be assisted by receiving a default reserve pool recommendation from the memory controller (which default may be applied to allocated block devices absent host programming of a different setting.

[0061] Still referring to Figure 9, the pseudo-physical host perspective of block device remains static and defect free, despite ongoing failure events (and/or removal of erase units or other virtualized structural elements from service for wear leveling, garbage collection, scrubbing or other maintenance

or operational reasons). The remapping of address information by the memory controller using the identified translation scheme once again helps streamline I/O latency, as discussed earlier.

[0062] Figure 10 demonstrates an exemplary sequence of operations coordinated between the pseudo-expositive flash memory controller and host file server to enable host-scheduled maintenance of flash-device-identified units of data, and more specifically segments in this example. The device tracks statistics and environmental status of the memory looking for indications that a portion of the data needs maintenance driven by a physical resource. An example of a maintenance operation might be that data has resided on a given EU for a time long enough to approach a maximum estimated safe retention time. An event could be set to trigger at a threshold of safety previously selected by to host and communicated to the device. Once that event has been triggered, the device translates the physical location though the previous block device and ASL map structures in order to identify the segment as a host LBA in which the physical resource resides. When the host has received the notification of the event, along with the associated segment LBA address, length, and event type, the host may elect to handle that event in a number of ways. Host issued instructions may garbage collect, copy, move, or discard data in manner the best benefits the overall efficiency of the system. Those instructions may be mixed into the overall system scheduling. Note that in contradistinction to conventional approaches (e.g., where an entire address space is garbage collected, in a device-wide operation delegated to a memory controller) that this approach permits the host to command specific maintenance operations to specific hierarchies, for example, by command to perform maintenance on a specific EU; to this effect, the host transmits a maintenance command with a specific block address, which the memory controller uses to perform maintenance on a host-selected or host-specified address range, conveyed by or in connection the maintenance command. Once data has been relocated or discarded, a segment of interest may be erased.

[0063] Figure 11 illustrates a forward (and reverse) compatibility between successive flash generations that is enabled by the pseudo-expositive flash device in combination with the block device allocator discussed above in reference to Figure 2. Assume, for example, that the block device allocator was initially executed in connection with a generation 'A' flash device having a page size 'K', to configure a block device having a four-page stripe size. For ease of illustration, the K-sized pages are assumed sufficiently large that each erase unit contains only two pages, and that each host segment spans four erase units. Thus, a first host segment ("Seg0") is striped across the four dies of the block device and fills erase unit 0 within each die, being stored in eight pages total (pages 0-7), while a second host

segment ("Seg1") is stored within erase unit 1 of the four dies and thus in pages 8-15. Assume as a forward-compatibility example, that a next generation "GenB" flash device is to be deployed in combination with or in place of a "GenA" flash device, and that page size has doubled to 2K so that the overall flash device capacity has doubled in GenB (i.e., there are the same number of pages per erase unit, erase units per die, dies per channel and channels as in the GenA device so that the doubled page size doubles the capacity of every element in the structural hierarchy). In this case, assuming further that the page read and write times (t_{READ} and t_{PROG}) have also doubled between the two flash device generations, then the user/designer may re-run the block device allocator with an unchanged set of block device specifications (i.e., in terms of read and write bandwidth, at least) to yield a block device allocation and ASL within the GenB device that matches the performance characteristics of the counterpart block device within the GenA flash device, albeit at double capacity. For example, as shown in Figure 11, the block device allocator may define the ASL such that the stripe width still spans four pages (i.e., a page within each of the four allocated dies) so that the reduced write bandwidth (due to the 2x higher GenB tProg) is offset by the doubled page size. Thus, the two segments previously stored within the GenA drive may be written to the GenB drive with the same bandwidth, but now occupy only half the number of erase units (as their capacity has doubled) as in the GenA storage. Note that Seg1 may, through different ASL specification, be stored within dies 0 and 1of the GenB flash device instead of dies 2 and 3, thus raising endurance of the flash device at the cost of reduced write bandwidth. Changing the example so that the tPROG and tREAD times remain unchanged in the GenB device, then the alternative segment 1 storage destination (i.e., alternative ASL specification) within dies 0 and 1 may be preferable, as the two-die stripe size in the GenB device would yield the same write bandwidth as the four-die stripe size in the GenA device. That is, sequencing more narrowly through dies 0 and 1 (instead of more broadly across all four dies) will yield a higher endurance result with approximately the same read/write bandwidth. As discussed above, the ASL may be further tuned to yield a desired balance between endurance and I/O bandwidth.

[0064] Figure 12 illustrates more detail regarding pseudo-physical geometry export options within a flash device having multi-plane flash dies. In the particular example shown, it is assumed that each die within the flash device, exemplified by "Die 0" includes N erase units distributed evenly between even and odd erase-unit planes (i.e., N/2 erase units per plane). In general, the die may be switched on the fly, according to incoming command sequences, between single-plane and multi-plane operation. Once again, therefore, the same die ("Die 0") is illustrated in duplicate to discuss multiple alternate configurations; the pseudo-expositive memory controller may operate the die in one of several different

pseudo-physical modes including, an opportunistic single-plane mode, an exclusively multi-plane mode, and a range-split hybrid mode in which a portion of the pseudo-physical or physical erase units within the die are operated in opportunistic single-plane mode and another portion of the erase units are operated in exclusively multi-plane mode. In each of the pseudo-physical operating modes, the erase unit field of an incoming LBA resolves to fewer than N erase units. For example, the erase unit field resolves to any one of M erase units in single-plane mode, to any one of M/2 double-width erase units (i.e., logical combination of paired erase units drawn respectively from the odd and even planes) in dual plane mode and any one of K single-plane erase units or J double-width erase units in the hybrid split-range mode, where M<N and K+2J<N.

[0065] In opportunistic single-plane mode, the flash die is generally accessed one erase-unit at a time (or more accurately one page within one erase unit at a time, for reads and writes), occasionally executing a dual-plane command where a pair of successive accesses are directed respectively to erase units within the odd and even planes. By contrast, when configured for dual plane mode, each host requested memory access is translated by the memory controller into a dual plane command sequence that accesses a matched pair of erase units within each of the odd and even planes (i.e., one odd-plane erase unit and a counterpart even-plane erase unit). Accordingly, the page registers and erase units are viewed, from a pseudo-physical perspective, as double-width elements as compared to individual page registers and erase units in single-plane mode. Moreover, the total number of erase units is halved (by the effective merging of the two planes) so that the pseudo physical address range is reconfigured to account for half the number of virtually addressable erase units within the die, and double the number of logical blocks per page.

[0066] Still referring to Figure 12, the split-range hybrid mode, due to its dual range-divided configuration, permits single-plane commands and opportunistic multi-plane command sequences within the single-plane address range (i.e., logical addresses that resolve to erase units below pseudo-physical erase unit K), and requires exclusively multi-plane command sequences within the dual-plane address range. In alternative embodiments, the ordering of the dual-plane and single-plane ranges may be reversed (i.e., dual-plane at lower rather than higher-ordered addresses) and the total number of different ranges may be greater than the two shown.

[0067] Figure 13 illustrates additional operations that may be managed by embodiments of the pseudo-exposition. Once again, "Die 0" is shown in multiple, alternate configurations. A defective erase unit detected within a given plane of a multi-plane capable die may be mapped (logically replaced) by an

otherwise reserved erase unit within the same plane as shown in the two pseudo-physical views of die zero. This enables opportunistic multi-plane operations to continue when the die is configured for single-plane operation, and permits multi-plane operations to proceed entirely transparently to the host.

[0068] Figure 14 illustrates one embodiment of various techniques illustrated above, implemented as a memory controller integrated circuit (IC). As noted by the figure, in one version, such an IC can be implemented as a field-programmable gate array (FPGA) having logic gates and lookup tables (e.g., circuitry) configured to provide fast address translation as discussed above; this is not required for all embodiments, and in other contemplated embodiments, a memory controller can be implemented as a special purpose processor or other preconfigured integrated circuit, with or without the use of support software (e.g., firmware). As depicted by the figure, the IC includes a host interface, which for example, uses a standard communication interface framework (e.g., non-volatile memory express, or NVME or Serial ATA) for packetized communications, where packets comprise commands, address and data, as appropriate; note that this interface can be shared for commands directed to different channels or devices, i.e., the commands and data to respective channels and/or dies are typically MUX'ed over this channel for exchange between the memory controller IC and the host. Similarly, as discussed earlier, the memory controller features a flash interface, whereby one or more channels are used to communication with one or more memory devices. Each channel can consist of a set of links for address and/or data (e.g., for packetized communication of address and data over a set of eight links), or can feature separated address and databusses (as depicted by the optional, dashed-line links designated for "data"). The memory controller IC also features hardware translation circuitry as mentioned (e.g., with ASL parameters being used to configure address wrapping and distinction between hierarchical levels and with LUTs used for address mapping at selected or predetermined levels of the hierarchy) and buffers for buffering commands and/or data transfer as appropriate. In addition, the memory controller IC in this embodiment can include supervisory logic (e.g., for responding to host queries, performing LUT updates, and configuring parameters as appropriate, as well as for controlling sequencing and maintenance operations in memory), a block-device designer and allocator section as discussed earlier in connection with FIG. 2, and block device configuration elements, as appropriate. In one embodiment, some or all of these functions can be implemented in the form of instructions stored on non-transitory machine-readable media (e.g., firmware or software, for controlling one or more cores or processors).

[0069] It should be noted that, as a step in their fabrication or other reification, the various circuits disclosed herein may be described using computer aided design tools and expressed (or represented) as data and/or instructions embodied in various computer-readable media, in terms of their behavioral, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to, formats supporting behavioral languages such as C, Verilog, and VHDL, formats supporting register level description languages like RTL, and formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, computer storage media in various forms (e.g., optical, magnetic or semiconductor storage media, whether independently distributed in that manner, or stored "in situ" in an operating system).

[0070] When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process. Any of the various methods and operational sequences herein may likewise be recorded as one or more sequences of instructions on a computer-readable medium and may be executed on a computing device to effectuate the disclosed method and/or operational sequence.

[0001] Also, as noted, many of the techniques described herein can be employed in an apparatus, a method, an integrated circuit, a system on-chip, a memory device, a memory controller, a host processor, as a circuit description (i.e., that contains data structures defining fabrication parameters for a processor, integrated circuit, device, or components of any of these things), as instructions stored on machine-readable media (e.g., firmware or software intended for execution on one or more general purpose machines), or as combinations of these things. In the case of software or other instructional logic, the instructions are typically written or designed in a manner that has certain structure (architectural features) such that, when they are ultimately executed, they cause the one or more general purpose machines or hardware to behave as special purpose machines, having structure

configured by the instructions to necessarily perform certain described tasks. "Non-transitory machine-readable media" as used herein means any tangible (i.e., physical) storage medium, irrespective of how data on that medium is stored, including without limitation, random access memory, hard disk memory, optical memory, a floppy disk or CD, server storage, volatile memory and other tangible mechanisms where instructions may subsequently be retrieved by a machine. The machine-readable media can be in standalone form (e.g., a program disk) or embodied as part of a larger mechanism, for example, a storage drive, CPU, laptop computer, portable or mobile device, server, data center, "blade" device, subsystem, electronics "card," storage device, network, or other set of one or more other forms of devices. The instructions can be implemented in different formats, for example, as metadata that when called is effective to invoke a certain action, as Java code or scripting, as code written in a specific programming language (e.g., as C++ code), as a processor-specific instruction set, or in some other form; the instructions can also be executed by the same processor or different processors, depending on embodiment. For example, in one implementation, instructions on non-transitory machine-readable media can be executed by a single computer and, in other cases as noted, can be stored and/or executed on a distributed basis, e.g., using one or more servers, web clients, or application-specific devices. Each function mentioned in the disclosure or FIGS. can be implemented as part of a combined program or as a standalone module, either stored together on a single media expression (e.g., single floppy disk) or on multiple, separate storage devices. The same is also true for a circuit description for fabricating cores, processors, devices or circuits described herein, i.e., the result of creating a design can be stored in non-transitory machine-readable media for temporary or permanent use, either on the same machine or for use on one or more other machines; for example, a circuit description or software can be generated using a first machine, and then stored for transfer to a printer or manufacturing device, e.g., for download via the internet (or another network) or for manual transport (e.g., via a transport media such as a DVD) for use on another machine. Throughout this disclosure, various processes will be described, any of which can generally be implemented as instructional logic (instructions stored on non-transitory machine-readable media), as hardware logic, or as a combination of these things. Depending on product design, such products can be fabricated to be in saleable form, or as a preparatory step for other processing that will ultimately create finished products for sale, distribution, exportation or importation.

[0071] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice

the invention. For example, any of the specific numbers of bits, signal path widths, signaling or operating frequencies, device geometries and numbers of hierarchical structural elements (e.g., channels, dies, planes, erase units, pages, etc.), component circuits or devices and the like may be different from those described above in alternative embodiments. Additionally, links or other interconnection between integrated circuit devices or internal circuit elements or blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be a single signal line, and each of the single signal lines may alternatively be buses. Signals and signaling links, however shown or described, may be single-ended or differential. A signal driving circuit is said to "output" a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. The term "coupled" is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Device "programming" may include, for example and without limitation, loading a control value into a register or other storage circuit within an integrated circuit device in response to a host instruction (and thus controlling an operational aspect of the device and/or establishing a device configuration) or through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device. The terms "exemplary" and "embodiment" are used to express an example, not a preference or requirement.

[0072] While the invention has been described with reference to specific embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope. For example, features or aspects of any of the embodiments may be applied in combination with any other of the embodiments disclosed herein and/or in materials incorporated by reference or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. (Original) A storage device comprising:

flash memory comprising erase units; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed block device from the first address portion,

use a first division operation to derive the second address portion, to identify an addressed segment within the addressed block device, and use the first division operation to derive the third address portion, and

use a second division operation on the third address portion, to identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation of the third address portion within the selected one of the erase units identified for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

2. (Original) The storage device of claim 1 wherein:

said circuitry comprises at least one processor; and

the storage device further comprises instructions stored on at least one non-transitory storage medium, said instructions when executed to control the at least one processor so as to operate as special purpose circuitry.

3. (Original) The storage device of claim 1 wherein:

the storage device can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and the storage device comprises circuitry to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host;

the request from the host to copy is to designate destination address information corresponding to the second physical storage location; and

the storage device is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.

4. (Original) The storage device of claim 3 wherein the storage device is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit.

5. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage drive is to store the values representing a time since data was programmed on a basis that is respective to each structure of the number of structures, wherein each value represents time since data was programmed into the respective structure.

6. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit the information identifying the number of structures to a host, and wherein the storage device comprises circuitry to fulfill the at least one request by issuing commands to the flash memory for which a quantum of flash memory selected by the commands which are issued in response to the at least one request is dependent on the information transmitted to the host identifying the number of structures.

7. (Original) The storage device of claim 1 wherein the storage device is to store information identifying a number of structures in the flash memory and is to transmit to a host information that identifies an amount of flash memory that is to be erased as a unit.

8. (Original) The storage device of claim 1 wherein the addressed segment corresponds to an integer number of erase units, and the third address portion specifies a location within a sequential range of locations that correspond to the integer number of erase units.

9. (Original) The storage device of claim 1 wherein the first division operation and the second division operation each subdivide a value obtained from an incoming address into respective bitfields.

10. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold;

upon detection that a specific one of the values has satisfied the one or more thresholds, copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit; and

remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit.

11. (Original) The storage device of claim 10 wherein:

the storage device is to identify, for the data being copied, a logical erase unit address, the logical erase unit being associated with the addressed block device to the exclusion of each other of the block devices; and

the storage device is to remap the logical erase unit address from the first physical erase unit to the second physical erase unit.

12. (Original) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory space,

compare the metadata to at least one threshold,

upon detection that specific metadata has satisfied the one or more thresholds, copy data stored at one or more physical storage locations associated with the

specific metadata from a first physical erase unit to a second physical erase unit, and

remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit.

13. (Original) The storage device of claim 1 wherein:

the erase units are physical erase units;

the storage device is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units; and

the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests.

14. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;

compare the values representing time since data was programmed to at least one threshold; and

responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values.

15. (Original) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices,

receive a query, issued by a host, directed to a specific one of the block devices, and

responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

16. (Original) The storage device of claim 1 wherein:

the flash memory is to have block devices, including the addressed block device; and

the storage device further comprises circuitry to

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space, and

receive a query, issued by a host, wherein said query is specific to one of the block devices, and responsive to the query, identify specific metadata, associated with the specified one of the block devices, and transmit information to the host that conveys the specific metadata.

17. (Original) The storage device of claim 1 wherein the storage device further comprises circuitry to:

store metadata on an independent basis for flash memory associated with each one of the block devices, wherein the stored metadata represents an erase count of associated physical memory space;

compare the metadata to at least one threshold; and

responsive to detection that specific metadata has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.

18. (Original) The storage device of claim 1 wherein:

the data access requests comprise write requests;

the flash memory comprises multiple planes; and

the storage device is to, for each one of the write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page.

19. (Original) The storage device of claim 1 wherein for each one of the incoming erase requests, the storage drive is to perform a division operation to subdivide incoming address information accompanying the one of the erase requests, to identify a bit field that identifies an address-delimited subset of the host-selected segment for erasure.

20. (Original) A storage device comprising:

flash memory comprising erase units; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed block device from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation of the third address portion within the selected one of the erase units identified for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

21. (Original) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation of the third address portion within the selected one of the erase units identified for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

derive a second address portion and identify from the second address portion a host-selected segment within the host-selected block device, and

execute the one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units that correspond to the host-selected segment.

22 (Original) A storage device comprising:

flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-

inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and

circuitry to, for each of incoming data write requests,

derive a first address portion, a second address portion and a third address portion,

identify an addressed one of the block devices from the first address portion,

use a first operation to subdivide the incoming address information into respective bit fields, including the second address portion and the third address portion, to identify an addressed segment within the addressed block device from the second address portion, and

use a second operation to subdivide the third address portion into bit fields, to respectively identify an address value to select one of the erase units and to identify a storage location within the selected one of the erase units;

wherein said circuitry is to execute each one of the incoming data write requests by programming accompanying data into the storage location of the selected one of the erase units which was selected from the address value that was identified by the second division operation of the third address portion within the selected one of the erase units identified for the one of the incoming data write requests;

wherein the storage device is to, for each one of incoming erase requests received from a host,

derive a first address portion that identifies a host-selected block device,

use the first division operation to derive a second address portion, to identify an addressed one of the segments within the addressed block device, and use the first division operation to derive address information for one or more erase units within the one of the segments addressed by the one of the incoming erase requests, and

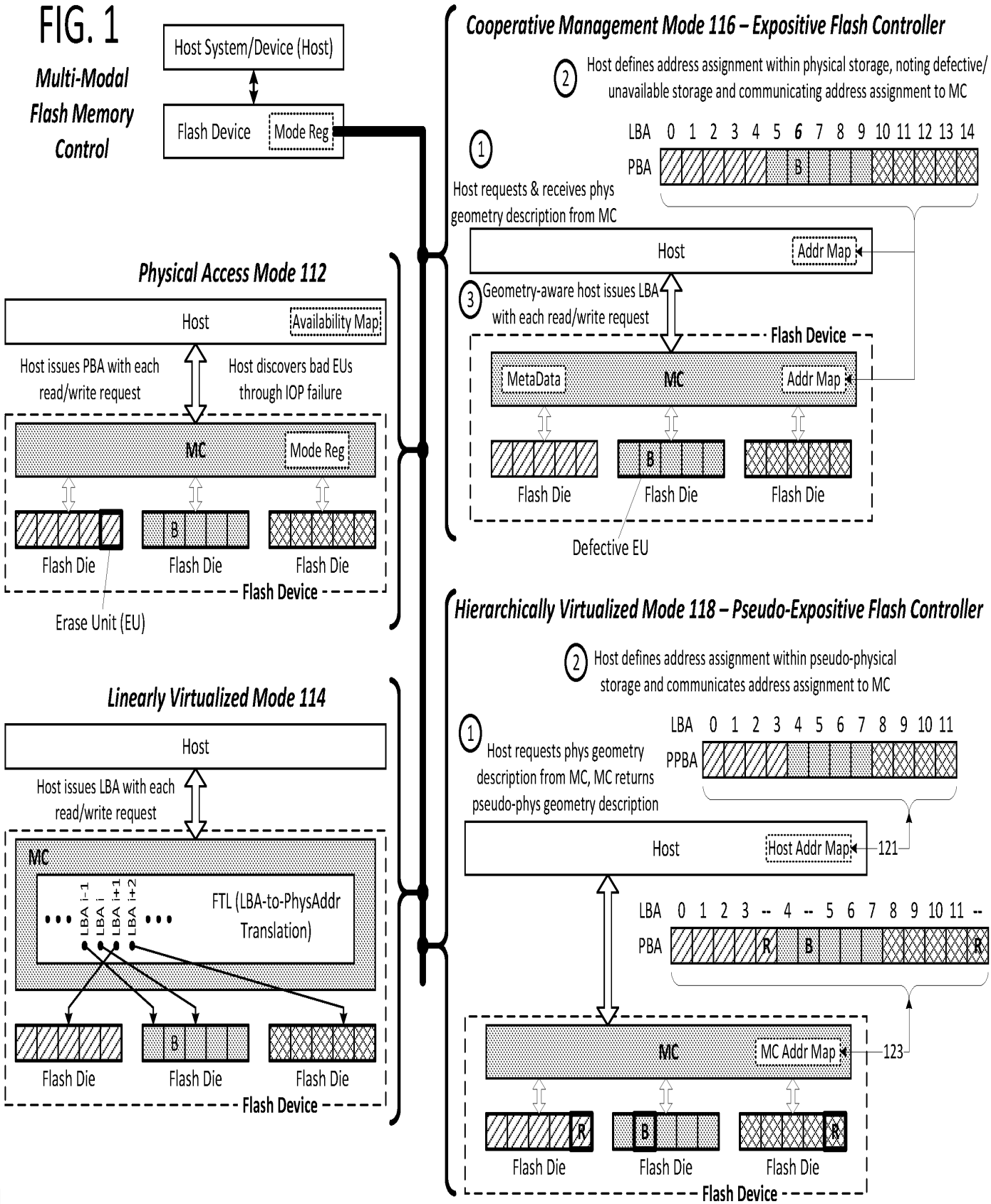
execute the one of the incoming erase requests by controlling erasure in the flash memory of the one or more erase units.

ABSTRACT

This disclosure provides techniques hierarchical address virtualization within a memory controller and configurable block device allocation. By performing address translation only at select hierarchical levels, a memory controller can be designed to have predictable I/O latency, with brief or otherwise negligible logical-to-physical address translation time. In one embodiment, address transition may be implemented entirely with logical gates and look-up tables of a memory controller integrated circuit, without requiring processor cycles. The disclosed virtualization scheme also provides for flexibility in customizing the configuration of virtual storage devices, to present nearly any desired configuration to a host or client.

FIG. 1

Multi-Modal Flash Memory Control



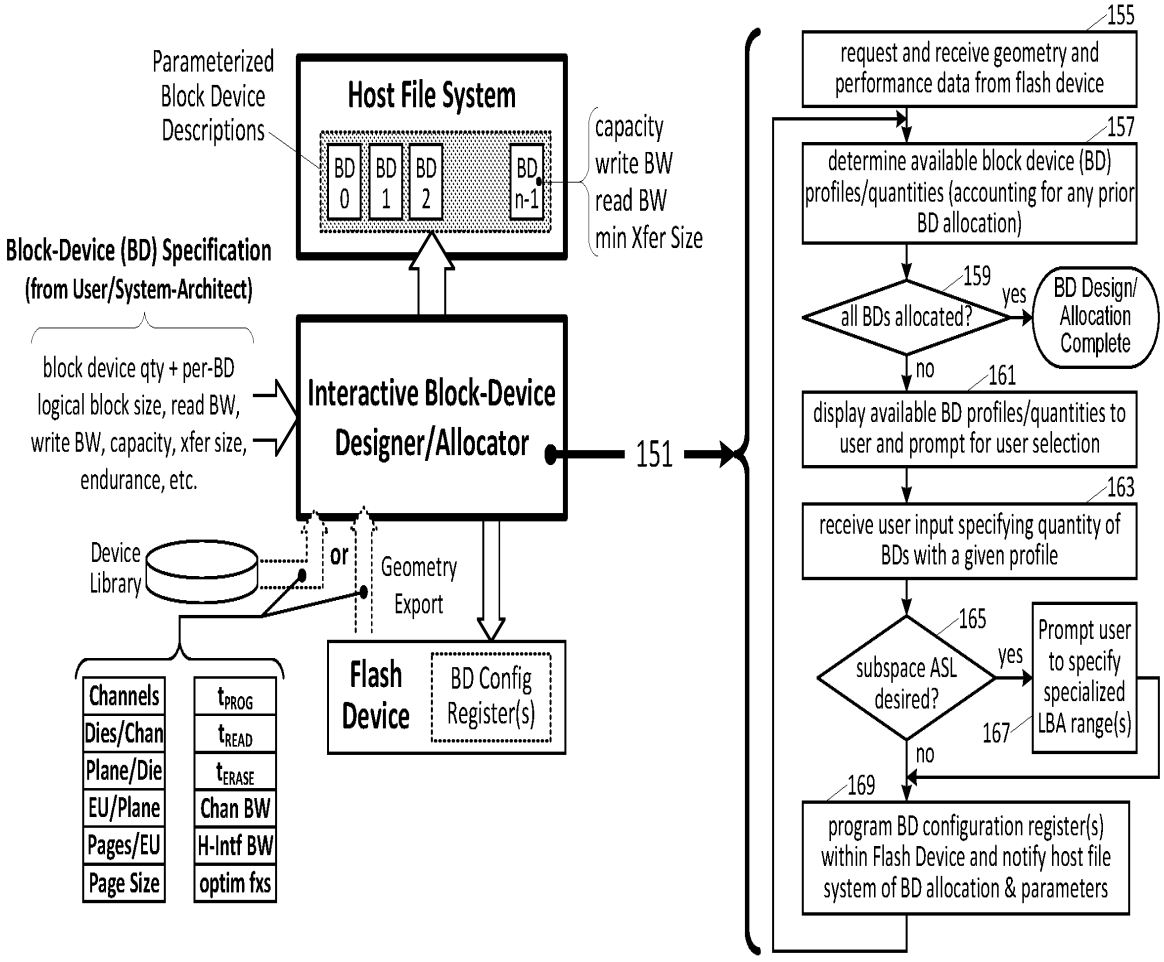

Parameterized Block Device Descriptions
Host File System
BD 0
BD 1
BD 2
BD n-1
capacity
write BW
read BW
min Xfer Size
Block-Device (BD) Specification (from User/System-Architect)
block device qty + per-BD logical block size, read BW, write BW, capacity, xfer size, endurance, etc.
Interactive Block-Device Designer/Allocator
151
Device Library
or
Geometry Export
Flash Device
BD Config Register(s)
Channels
Dies/Chan
Plane/Die
EU/Plane
Pages/EU
Page Size
t_{PROG}
t_{READ}
t_{ERASE}
Chan BW
H-Intf BW
optim fxs
155
request and receive geometry and performance data from flash device
157
determine available block device (BD) profiles/quantities (accounting for any prior BD allocation)
159
all BDs allocated?
yes
BD Design/ Allocation Complete
no
161
display available BD profiles/quantities to user and prompt for user selection
163
receive user input specifying quantity of BDs with a given profile
165
subspace ASL desired?
yes
Prompt user to specify specialized LBA range(s)
167
no
169
program BD configuration register(s) within Flash Device and notify host file system of BD allocation & parameters

FIG. 2

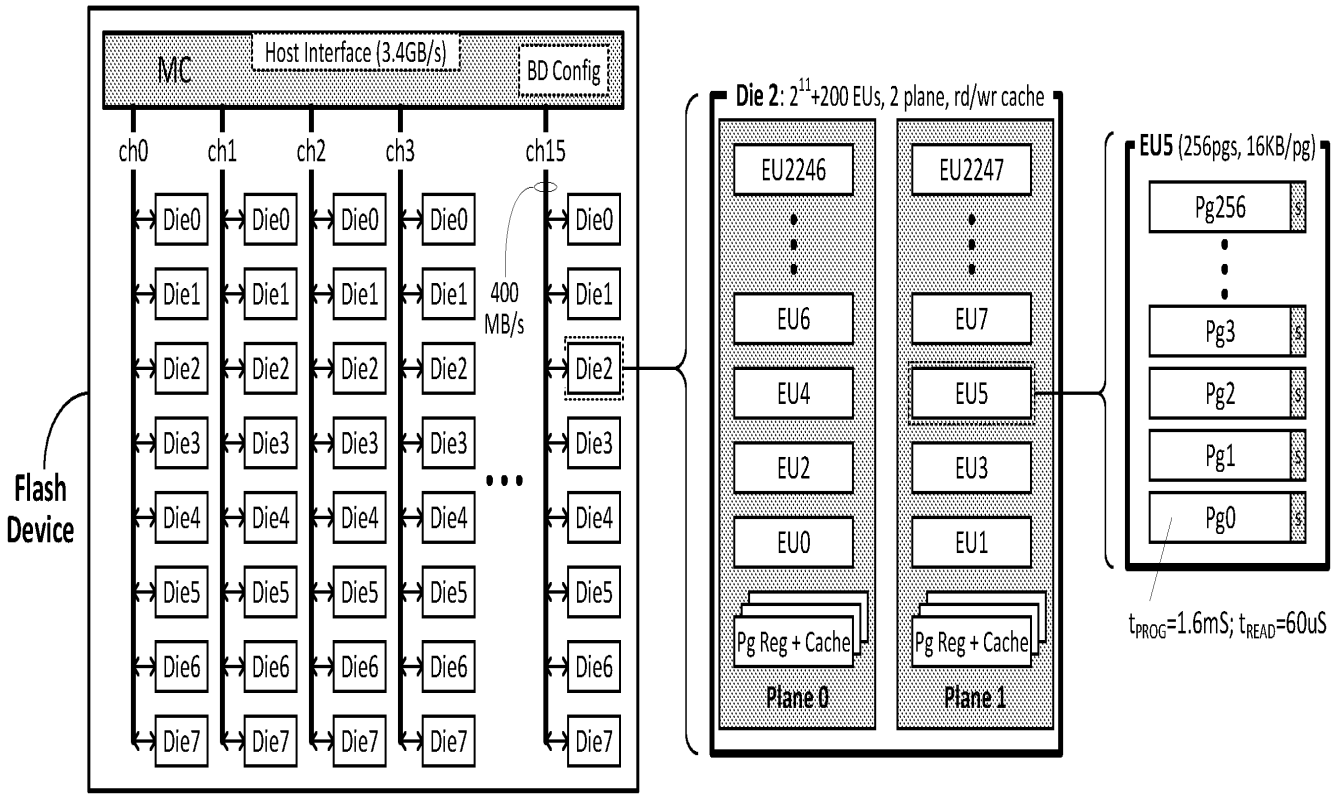
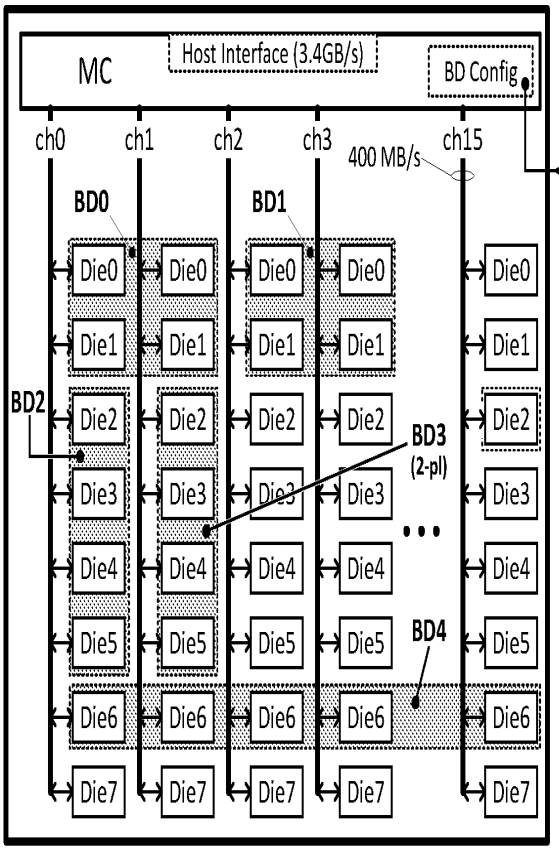

MC
Host Interface (3.4GB/s)
BD Config
ch0
ch1
ch2
ch3
ch15
Die0
Die1
Die2
Die3
Die4
Die5
Die6
Die7
400 MB/s
Flash Device
Die 2: 2^11+200 EUs, 2 plane, rd/wr cache
EU2246
EU2247
EU6
EU7
EU4
EU5
EU2
EU3
EU0
EU1
Pg Reg + Cache
Plane 0
Plane 1
EU5 (256pgs, 16KB/pg)
Pg256
Pg3
Pg2
Pg1
Pg0
tPROG=1.6mS; tREAD=60uS

FIG. 3

FIG. 4



BDid	Chans	Dies	ASL
0	0-1	0-1	map 0
1	2-3	0-1	map 1
2	0	2-5	map 2
3	1	2-5	map 3
4	0-15	6	map 4

BD LUT

ASL LUT

uniformly mapped for I/O parallelism

	ASL Parameters					feature control			
LBA Range	seqCh	seqDie	seqEU	seqPg	sLB	rdC	wrC	nPa	nPl
0-nLB_{BD}	1	1	1	1	4KB	off	off	1	2

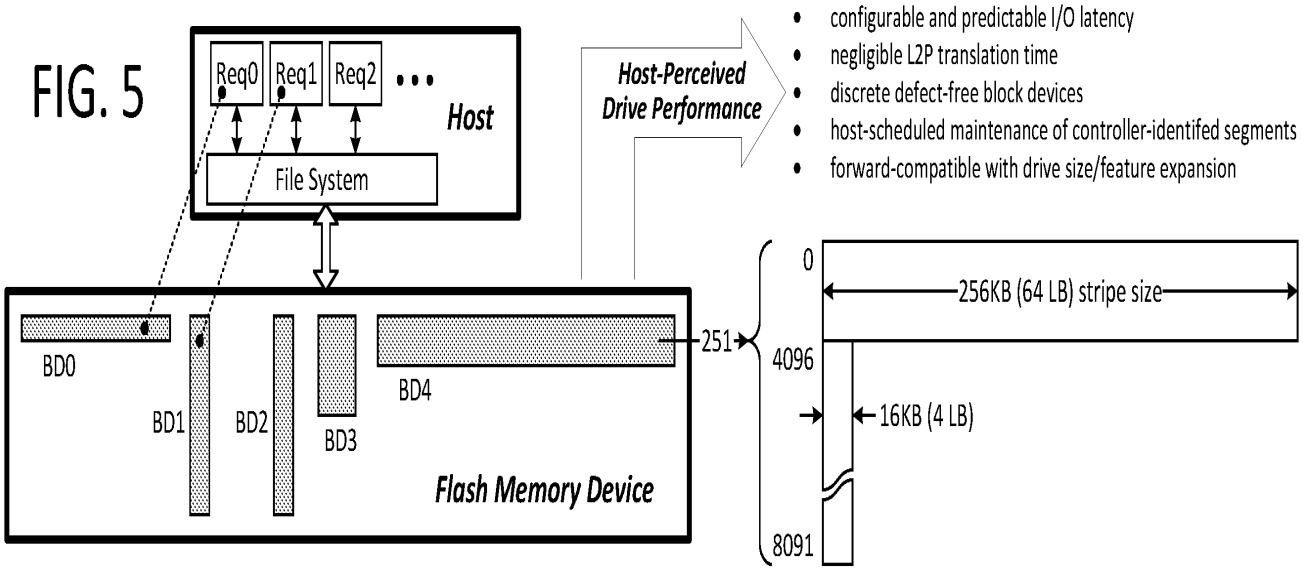
uniformly mapped for endurance

	ASL Parameters					feature control			
LBA Range	seqCh	seqDie	seqEU	seqPg	sLB	rdC	wrC	nPa	nPl
0-nLB_{BD}	nCH_{BD}	Die/CH_{BD}	EU/Die	Pg/EU	4KB	off	off	1	1

non-uniform subspace mapping

	ASL Parameters					feature control			
LBA Range	seqCh	seqDie	seqEU	seqPg	sLB	rdC	wrC	nPa	nPl
0-4095	1	1	1	1	4KB	off	off	1	1
4096-8091	nCH_{BD}	Die/CH_{BD}	EU/Die_{BD}	Pg/EU	4KB	off	off	1	1

FIG. 5



- configurable and predictable I/O latency
- negligible L2P translation time
- discrete defect-free block devices
- host-scheduled maintenance of controller-identifed segments
- forward-compatible with drive size/feature expansion

FIG. 6

Configurable and predictable I/O latency

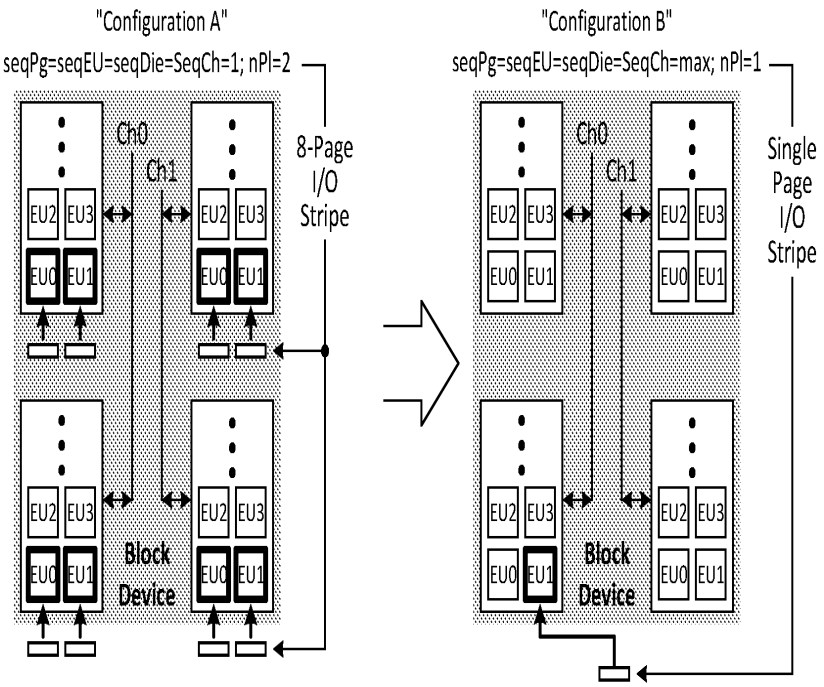


FIG. 7

Negligible L2P translation time

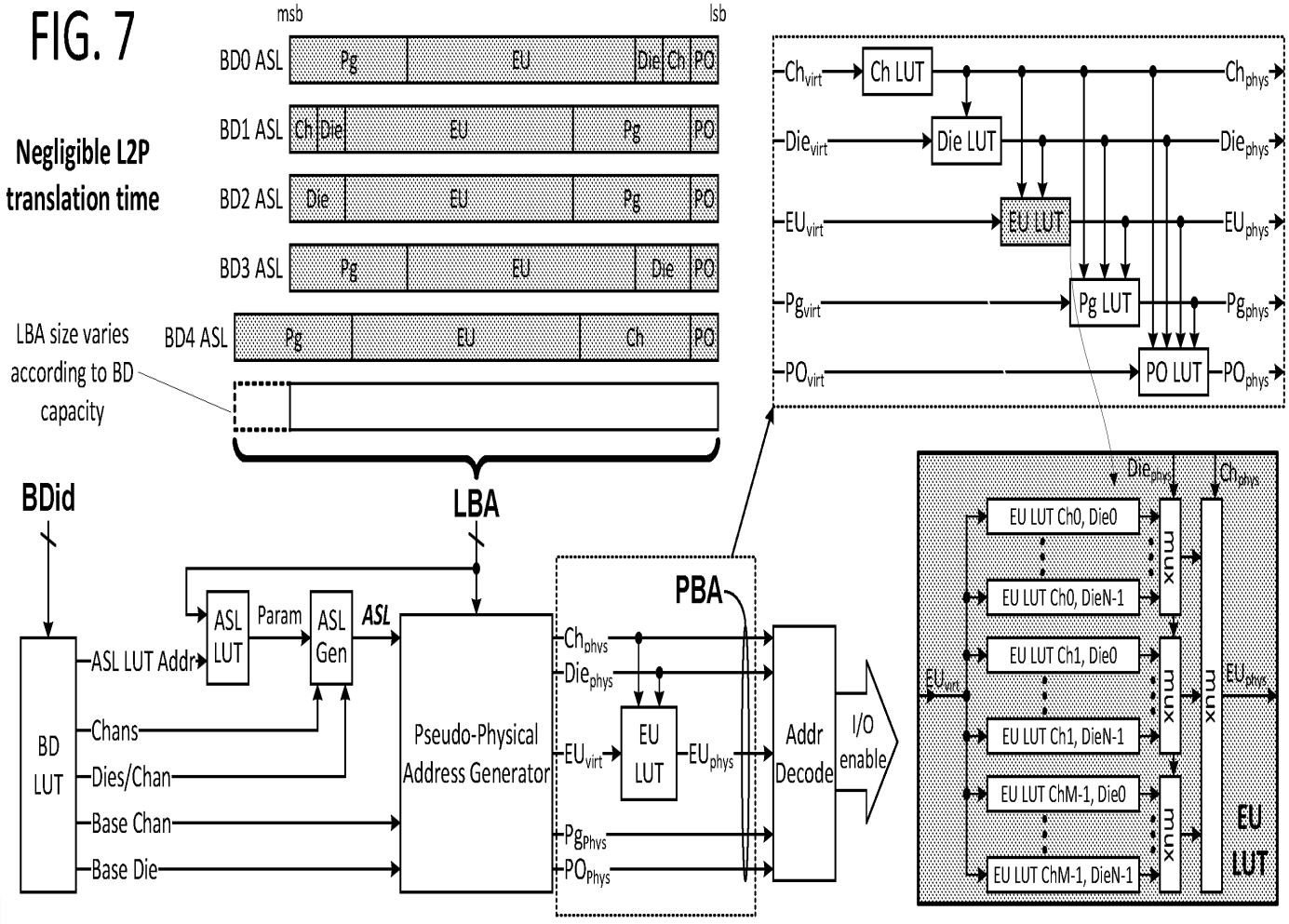


FIG. 8

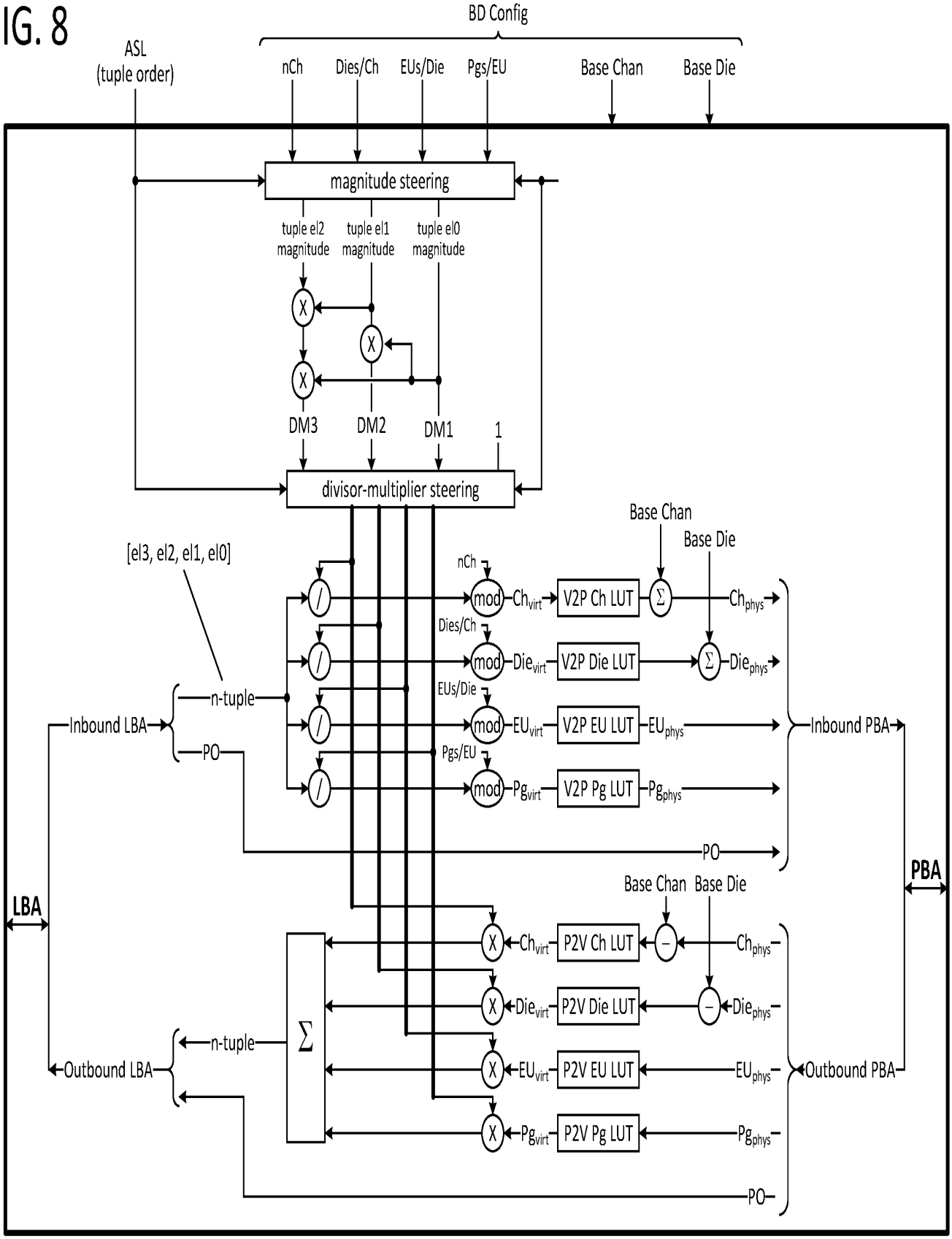

BD Config
ASL
(tuple order)
nCh
Dies/Ch
EUs/Die
Pgs/EU
Base Chan
Base Die
magnitude steering
tuple el2 magnitude
tuple el1 magnitude
tuple el0 magnitude
DM3
DM2
DM1
1
divisor-multiplier steering
[el3, el2, el1, el0]
n-tuple
Inbound LBA
PO
mod
Ch_virt
V2P Ch LUT
Ch_phys
Die_virt
V2P Die LUT
Die_phys
EU_virt
V2P EU LUT
EU_phys
Pg_virt
V2P Pg LUT
Pg_phys
Inbound PBA
LBA
PBA
P2V Ch LUT
P2V Die LUT
P2V EU LUT
P2V Pg LUT
Outbound LBA
Outbound PBA

FIG. 9

Discrete defect-free block devices

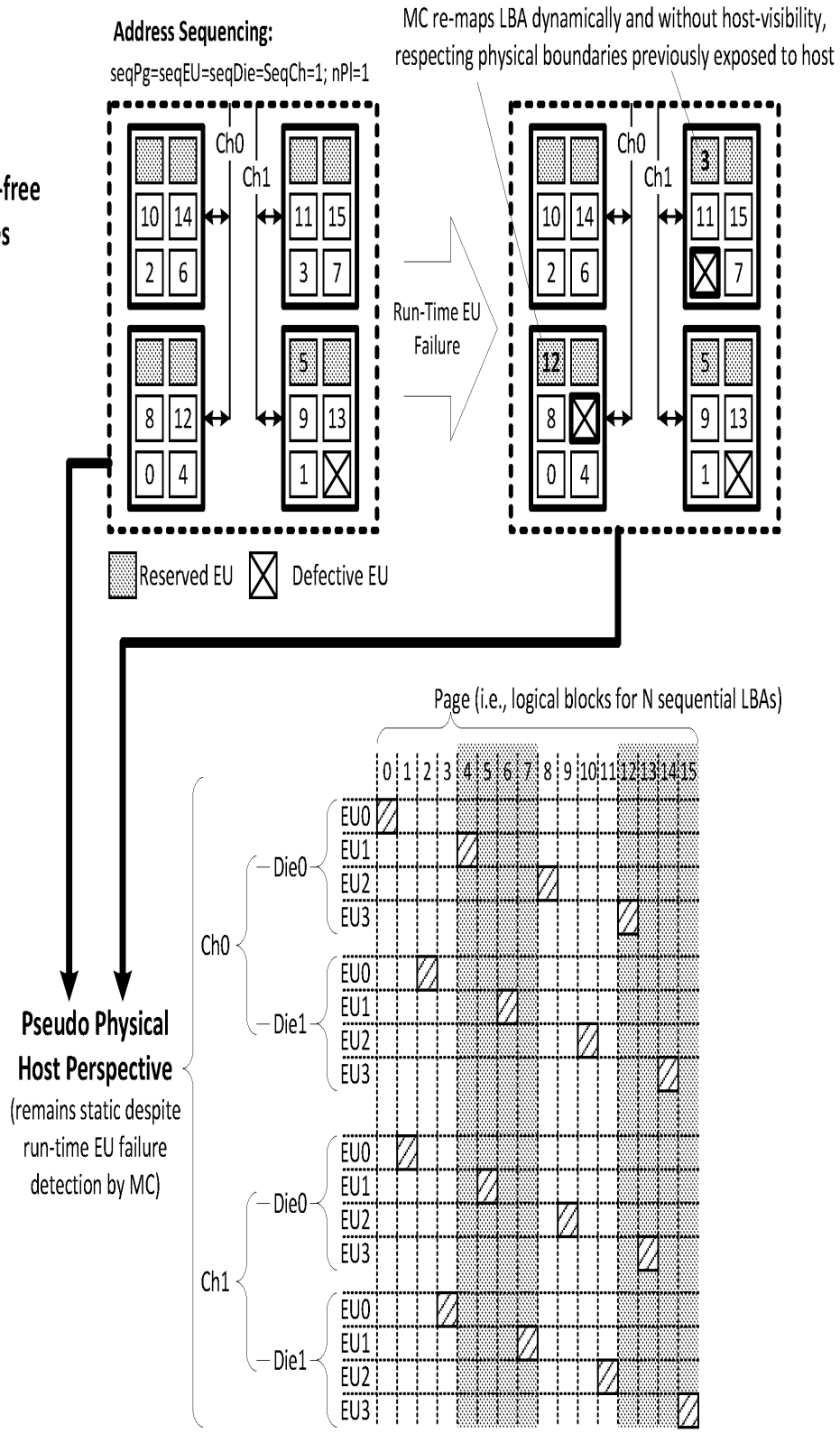


FIG. 10

Host-scheduled Flash maintenance of controller identified segments

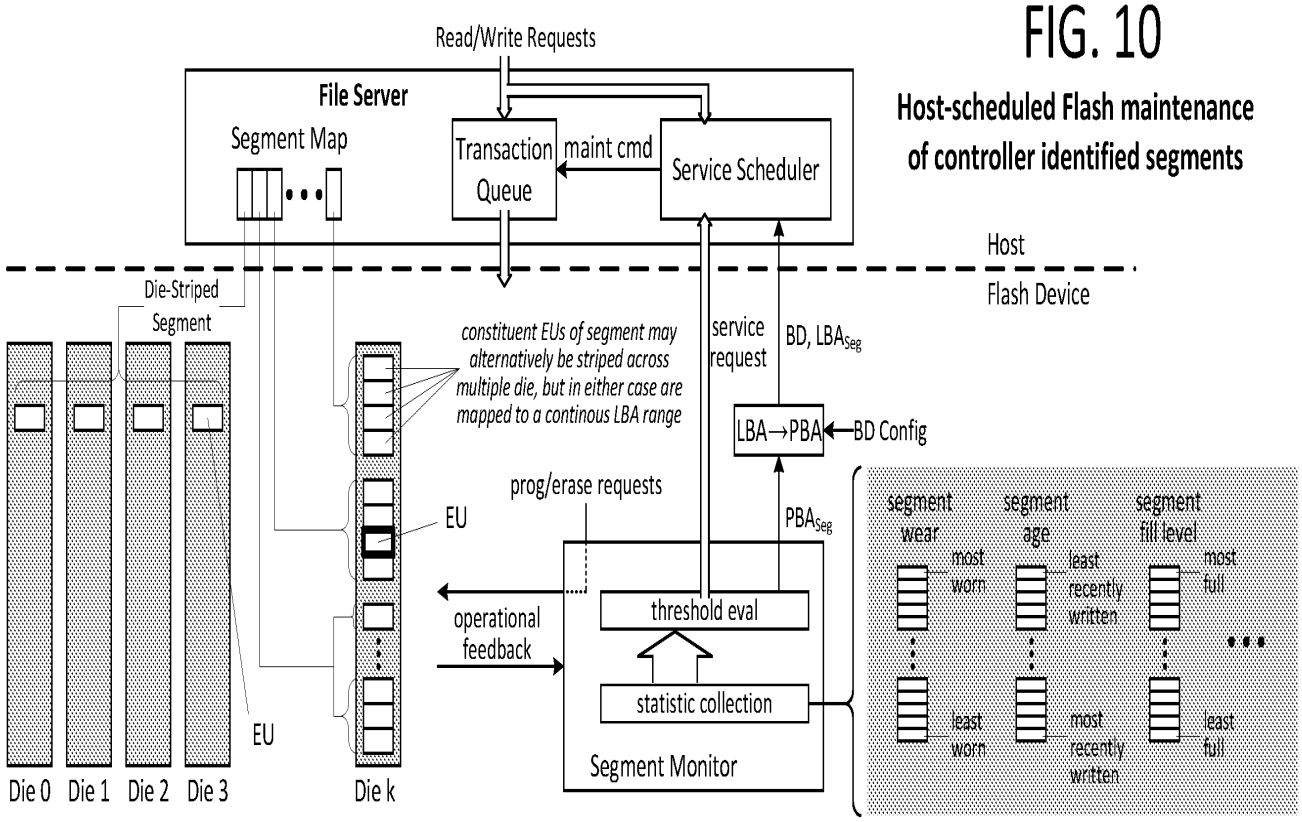


FIG. 11

Forward-compatible with drive size/feature expansion

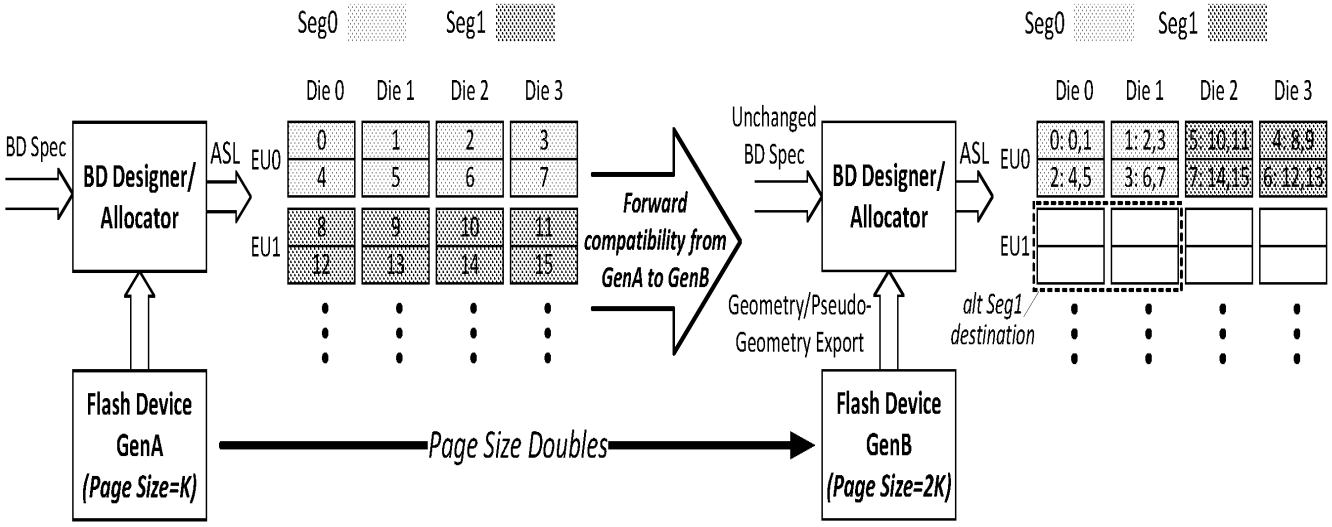


FIG. 12

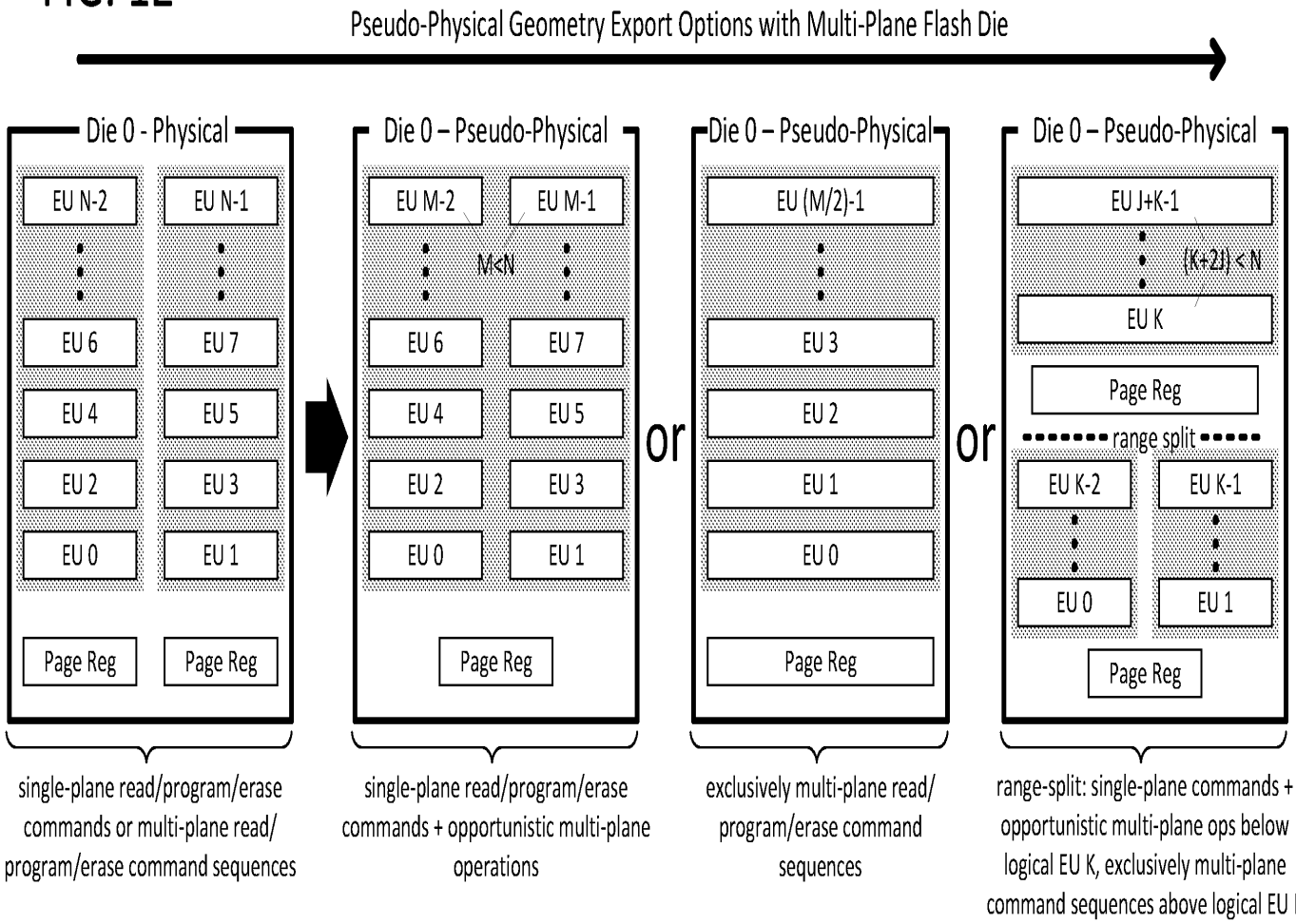
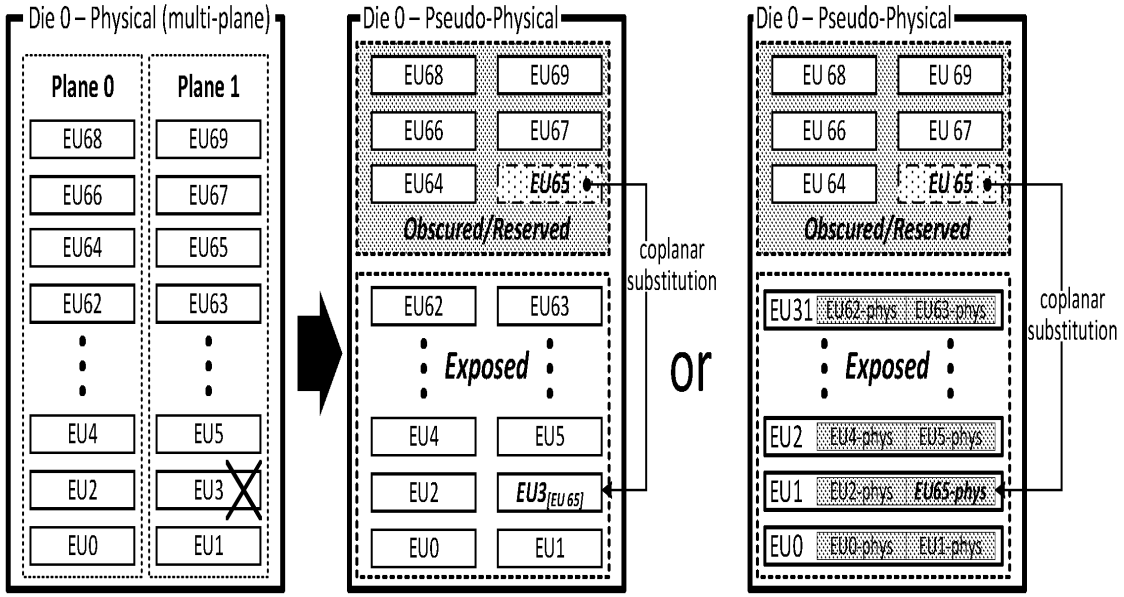

Pseudo-Physical Geometry Export Options with Multi-Plane Flash Die
Die 0 - Physical
EU N-2
EU N-1
EU 6
EU 7
EU 4
EU 5
EU 2
EU 3
EU 0
EU 1
Page Reg
Page Reg
Die 0 – Pseudo-Physical
EU M-2
EU M-1
M<N
EU 6
EU 7
EU 4
EU 5
EU 2
EU 3
EU 0
EU 1
Page Reg
or
Die 0 – Pseudo-Physical
EU (M/2)-1
EU 3
EU 2
EU 1
EU 0
Page Reg
or
Die 0 – Pseudo-Physical
EU J+K-1
(K+2J) < N
EU K
Page Reg
range split
EU K-2
EU K-1
EU 0
EU 1
Page Reg
single-plane read/program/erase commands or multi-plane read/ program/erase command sequences
single-plane read/program/erase commands + opportunistic multi-plane operations
exclusively multi-plane read/ program/erase command sequences
range-split: single-plane commands + opportunistic multi-plane ops below logical EU K, exclusively multi-plane command sequences above logical EU K

FIG. 13


Die 0 – Physical (multi-plane)
Plane 0
Plane 1
EU68
EU69
EU66
EU67
EU64
EU65
EU62
EU63
EU4
EU5
EU2
EU3
EU0
EU1
Die 0 – Pseudo-Physical
EU68
EU69
EU66
EU67
EU64
EU65
Obscured/Reserved
EU62
EU63
Exposed
EU4
EU5
EU2
EU3[EU 65]
EU0
EU1
coplanar substitution
or
Die 0 – Pseudo-Physical
EU 68
EU 69
EU 66
EU 67
EU 64
EU 65
Obscured/Reserved
EU31
EU62-phys
EU63-phys
Exposed
EU2
EU4-phys
EU5-phys
EU1
EU2-phys
EU65-phys
EU0
EU0-phys
EU1-phys
coplanar substitution

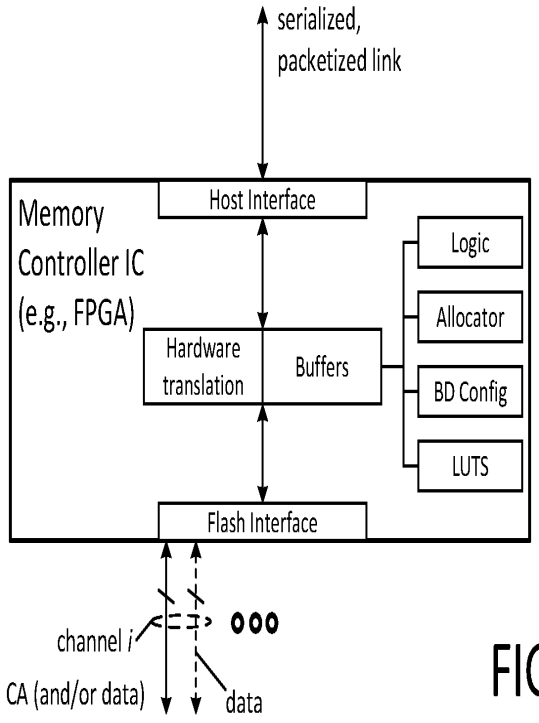

serialized,
packetized link
Memory
Controller IC
(e.g., FPGA)
Host Interface
Hardware
translation
Buffers
Logic
Allocator
BD Config
LUTS
Flash Interface
channel i
CA (and/or data)
data

FIG. 14

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Title of Invention	Expositive Flash Memory Control

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This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Robert Lercari Date (Optional) : _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Alan Chen Date (Optional): 12/2005

Signature: _____

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LEGAL NAME OF INVENTOR

Inventor: Craig Robertson Date (Optional): 10/7/15

Signature: Craig Robertson

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LEGAL NAME OF INVENTOR

Inventor: Mike Jadon Date (Optional): 10/9/15

Signature: _____

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Expositive Flash Memory Control

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Andrey V. Kuzmin Date (Optional): 10/10/2015

Signature: Andrey Kuzmin

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Radian Memory Systems, Inc.

Application No./Patent No.: herewith (con of 16808304) Filed/Issue Date: herewith

Titled: ADDRESSING TECHNIQUES FOR WRITE AND ERASE OPERATIONS IN A NON-VOLATILE STORAGE DEVICE

Radian Memory Systems, Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: all inventors To: Radian Memory Systems, LLC

   The document was recorded in the United States Patent and Trademark Office at
   Reel 038037, Frame 0234, or for which a copy thereof is attached.

2. From: Radian Memory Systems, LLC To: Radian Memory Systems, Inc.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 040579, Frame 0405, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Marc P. Schuyler/	20 September 2021
Signature	Date
Marc P. Schuyler	35675
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 17479475 Document Date: 09/20/2021

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