

Exhibit F-5
Invalidity Chart for U.S. Patent No. 11,347,657 In View of SCSI Zoned Block Commands Standard

Working Draft Revision 1 of the Small Computer System Interface (“SCSI”) Zoned Block Commands standard (“ZBC”) was published, and therefore qualifies as prior art under at least 35 U.S.C. § 102(a)(1) as to the asserted claims of U.S. Pat. No. 11,347,657 (“the ’657 Patent”). ZBC also incorporates by reference, or otherwise relies on or includes, other SCSI standards including SCSI Block Commands – 4 (“SBC-4”) and SCSI Primary Commands – 4 (“SPC-4”). SBC-4 and SPC-4 were published on August 27, 2014 and July 29, 2008, respectively, and there qualify as prior art under at least 35 U.S.C. § 102(a)(1). ZBC, including SBC-4, SPC-4, and any other material incorporated by reference, anticipates or renders obvious claims 1-4, 8-15, 18-22 of the ’657 Patent under 35 U.S.C. § 102 and/or 35 U.S.C. § 103, alone or based on the state of the art and/or in combination with one or more other references identified in Exs. F1-F4, Cover Pleading, and Ex. F-Obviousness Chart.¹

To the extent Plaintiff alleges that the ZBC, SBC-4, and SPC-4 (collectively, “SCSI Standard”) references do not disclose any particular limitation of the Asserted Claims of the ’657 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’657 Patent to modify the SCSI Standard reference and/or to combine the teachings of the SCSI Standard reference with other prior art references, including but not limited to the present prior art references found in Exs. F1-F4, Cover Pleading, and Ex. F-Obviousness Chart, and the corresponding section(s) of charts for other prior art references for the ’657 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

With respect to the obviousness of the Asserted Claims under 35 U.S.C. § 103, one or more of the principles enumerated by the United States Supreme Court in *KSR v. Teleflex*, 550 U.S. 398 (2007) apply, including: (a) combining various claimed elements known in the prior art according to known methods to yield a predictable result; and/or (b) making a simple substitution of one or more known elements for another to obtain a predictable result; and/or (c) using a known technique to improve a similar device or method in the same way; and/or (d) applying a known technique to a known device or method ready for improvement to yield a predictable result; and/or (e) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success or, in other words, the solution was one which was “obvious to try”; and/or (f) a known work in one field of endeavor prompting variations of it for use either in the same field or a different field based on given design incentives or other market forces in which the variations were predictable to one of ordinary skill in the art; and/or (g) a teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine the teachings of various prior art

¹ Samsung notes that Plaintiff appears in many instances to be pursuing overly broad constructions of various limitations of the asserted claims of the ’657 Patent in an effort to piece together an infringement claim where none exists and to accuse a product that does not practice the claims. This claim chart may take into account Plaintiff’s overly broad constructions of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper.

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references to arrive at the claimed invention. It therefore would have been obvious to one of ordinary skill in the art to combine the disclosures of these references in accordance with the principles and rationales set forth above.

The citations to portions of any reference in this chart are exemplary only. For example, a citation that refers to or discusses a figure or figure item should be understood to also incorporate by reference that figure and any additional descriptions of that figure as if set forth fully therein. Samsung reserves the right to rely on the entirety of the references cited in this chart to show that the Asserted Claims are invalid. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends. Samsung also reserves the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Plaintiff's infringement contentions, and/or information obtained during discovery as the case progresses.

Claim	'657 Patent	Exemplary Disclosure
1[pre]	A storage device comprising:	To the extent the preamble is limiting, ZBC discloses or at least renders obvious a storage device. <i>See e.g.</i>: This purpose of this standard is to define the model and command set extensions to be used in conjunction with the SCSI Primary Command Set standard —4 (SPC-4) and the SCSI Block Commands - 3 (SBC-3) to facilitate operation of SCSI zoned block devices. ZBC, Foreword. This standard defines the command set extensions to facilitate operation of SCSI zoned block devices. ZBC, Section 1. 3.1.5 host aware zoned block device SCSI target device with the PERIPHERAL DEVICE TYPE field set to 00h (i.e., direct access block device) and the HAW_ZBC bit set to one in the Block Device Characteristics VPD page (see SBC-4)

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		Note 1 to entry: See 4.2.2. ZBC, Section 3.1.5. 3.1.6 host managed zoned block device SCSI target device with the PERIPHERAL DEVICE TYPE field set to 14h (i.e., host managed zoned block device) Note 1 to entry: See 4.2.3. ZBC, Section 3.1.6. 3.1.19 zoned block device either a host aware zoned block device or a host managed zoned block device ZBC, Section 3.1.19.
1[a]	flash memory comprising erase units; and	ZBC discloses or at least renders obvious flash memory having physical erase units. <i>See, e.g.:</i> This purpose of this standard is to define the model and command set extensions to be used in conjunction with the SCSI Primary Command Set standard —4 (SPC-4) and the SCSI Block Commands - 3 (SBC-3) to facilitate operation of SCSI zoned block devices. ZBC, Foreword. This standard defines the command set extensions to facilitate operation of SCSI zoned block devices. ZBC, Section 1. 3.1.5 host aware zoned block device SCSI target device with the PERIPHERAL DEVICE TYPE field set to 00h (i.e., direct access block

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		device) and the HAW_ZBC bit set to one in the Block Device Characteristics VPD page (see SBC-4) Note 1 to entry: See 4.2.2. ZBC, Sections 3.1.5. 3.1.6 host managed zoned block device SCSI target device with the PERIPHERAL DEVICE TYPE field set to 14h (i.e., host managed zoned block device) Note 1 to entry: See 4.2.3. ZBC, Section 3.1.6. 3.1.19 zoned block device either a host aware zoned block device or a host managed zoned block device ZBC, Section 3.1.19.
1[b]	circuitry to receive from a host, and control execution of, incoming requests including data write request and erase requests, wherein each of the incoming requests is accompanied by incoming address information;	ZBC discloses or at least renders obvious circuitry to receive from a host, and control execution of, incoming requests including data write request and erase requests, wherein each of the incoming requests is accompanied by incoming address information. <i>See, e.g.:</i>

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Table 67 — WRITE (32) command								
Byte/Bit	7	6	5	4	3	2	1	0
0	OPERATION CODE (7Fh)							
1	CONTROL							
2	Reserved							
5								
6	Reserved			GROUP NUMBER				
7	ADDITIONAL CDB LENGTH (18h)							
8	SERVICE ACTION (000Bh)							
9								
10	WRPROTECT			DPO	FUA	Reserved	FUA_NV	Reserved
11	Reserved							
12	LOGICAL BLOCK ADDRESS							
19								
20	EXPECTED INITIAL LOGICAL BLOCK REFERENCE TAG							
23								
24	EXPECTED LOGICAL BLOCK APPLICATION TAG							
25								
26	LOGICAL BLOCK APPLICATION TAG MASK							
27								
28	TRANSFER LENGTH							
31								

SBC-3, Table 67.

4.3.5.3 Logical block address

The logical block addresses on a logical unit or within a volume or partition shall begin with block zero and be contiguous up to the last logical block of that logical unit or within that volume or partition.

SPC-4, Section 4.3.5.3.

This purpose of this standard is to define the model and command set extensions to be used in conjunction with the SCSI Primary Command

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		Set standard —4 (SPC-4) and the SCSI Block Commands - 3 (SBC-3) to facilitate operation of SCSI zoned block devices. ZBC, Foreword. 3.1.15 write operation process by which a device server performs operations (e.g., write cache operations (see SBC-4) and write medium operations (see SBC-4)) as described in SBC-4 ZBC, Section 3.1.15. 3.1.8 logical block address (LBA) value used to reference a logical block ZBC, Section 3.1.8. 3.1.11 reset write pointer operation process by which a device server sets a write pointer to the lowest LBA of a write pointer zone ZBC, Section 3.1.11. A write pointer zone is a type of zone that has a write pointer that indicates a location within that zone. Each write pointer zone has one write pointer. That write pointer indicates the LBA that the application client should specify in the LOGICAL BLOCK ADDRESS field of a subsequent write command for that write pointer zone. ZBC, Section 4.3.3.1.
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		A read operation on an LBA that has been written since the last reset write pointer operation in that sequential write preferred zone shall return the last written data. A read operation on an LBA that has not been written since the last reset write pointer operation in that sequential write preferred zone shall return user data set to the last initialization pattern that was set by: a) the manufacturer's default initialization pattern; b) the initialization pattern set by the last FORMAT UNIT command (see SBC-4), if any; or c) the initialization pattern set by the last SANITIZE command with the service action set to OVERWRITE (see SBC-4), if any. ZBC, Section 4.3.3.2. The ZONE ID field specifies the zone start LBA, if any, of the write pointer zone on which the device server shall perform a reset write pointer operation (see 4.3.3.1). ZBC, Section 5.3.
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		Table 16 — RESET WRITE POINTER command <table><tr><th>Bit Byte</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td colspan="8">OPERATION CODE (9Fh)</td></tr><tr><td>1</td><td colspan="3">Reserved</td><td colspan="5">SERVICE ACTION (14h)</td></tr><tr><td>3</td><td colspan="8">(MSB)</td></tr><tr><td>...</td><td colspan="8">ZONE ID</td></tr><tr><td>9</td><td colspan="8">(LSB)</td></tr><tr><td>10</td><td colspan="8" rowspan="3">Reserved</td></tr><tr><td>...</td></tr><tr><td>13</td></tr><tr><td>14</td><td colspan="7">Reserved</td><td>RESET ALL</td></tr><tr><td>15</td><td colspan="8">CONTROL</td></tr></table> ZBC, Table 16.	Bit Byte	7	6	5	4	3	2	1	0	0	OPERATION CODE (9Fh)								1	Reserved			SERVICE ACTION (14h)					3	(MSB)								...	ZONE ID								9	(LSB)								10	Reserved								...	13	14	Reserved							RESET ALL	15	CONTROL							
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1[c]	wherein said circuitry is to, for each of the incoming requests:	ZBC discloses or at least renders obvious said circuitry is to, for each of the incoming requests. <i>See, e.g.:</i> 1[d]-[g].																																																																																			
1[d]	derive, from the accompanying incoming address information, a first address portion and a second address portion,	ZBC discloses or at least renders obvious derive, from the accompanying incoming address information, a first address portion and a second address portion. <i>See, e.g.:</i> 4.3.5.3 Logical block address The logical block addresses on a logical unit or within a volume or partition shall begin with block zero and be contiguous up to the last logical block of that logical unit or within that volume or partition. SPC-4, Section 4.3.5.3. 3.1.8 logical block address (LBA)																																																																																			

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		value used to reference a logical block ZBC, Section, 3.1.8 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard: a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where LBA 0 is the lowest LBA of zone 0 and LBA m—1 is the highest LBA of zone n—1. ZBC, Section 4.2.1.
1[e]	identify an addressed block device from the first address portion,	ZBC discloses or at least renders obvious identify an addressed block device from the first address portion. <i>See, e.g.:</i> 4.3.5.3 Logical block address The logical block addresses on a logical unit or within a volume or partition shall begin with block zero and be contiguous up to the last logical block of that logical unit or within that volume or partition. SPC-4, Section 4.3.5.3.
1[f]	use a first division operation on the second address portion, to	ZBC discloses or at least renders obvious use a first division operation on the second address portion, to identify an addressed segment within the addressed block device,

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	identify an addressed segment within the addressed block device, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and	wherein the addressed segment corresponds to a subset of the erase units of the flash memory. <i>See, e.g.:</i> 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard: a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where LBA 0 is the lowest LBA of zone 0 and LBA m—1 is the highest LBA of zone n—1. ZBC, Section 4.2.1. If the device server processes a write command with: a) the starting LBA equal to the write pointer; b) the ending LBA is in the same sequential write required zone; and c) an ending LBA that is equal to the last logical block within a physical block, then the device server shall perform write operations for that command. ZBC, Section 4.3.3.3.
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		The ZONE ID field specifies the zone start LBA, if any, of the write pointer zone on which the device server shall perform a reset write pointer operation (see 4.3.3.1). ZBC, Section 5.3. Table 16 — RESET WRITE POINTER command <table><tr><th>Bit Byte</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td colspan="8">OPERATION CODE (9Fh)</td></tr><tr><td>1</td><td colspan="3">Reserved</td><td colspan="5">SERVICE ACTION (14h)</td></tr><tr><td>3</td><td colspan="8">(MSB)</td></tr><tr><td>...</td><td colspan="8">ZONE ID</td></tr><tr><td>9</td><td colspan="8">(LSB)</td></tr><tr><td>10</td><td colspan="8" rowspan="2">Reserved</td></tr><tr><td>...</td></tr><tr><td>13</td><td colspan="8">Reserved</td></tr><tr><td>14</td><td colspan="7">Reserved</td><td>RESET ALL</td></tr><tr><td>15</td><td colspan="8">CONTROL</td></tr></table> ZBC, Table 16.	Bit Byte	7	6	5	4	3	2	1	0	0	OPERATION CODE (9Fh)								1	Reserved			SERVICE ACTION (14h)					3	(MSB)								...	ZONE ID								9	(LSB)								10	Reserved								...	13	Reserved								14	Reserved							RESET ALL	15	CONTROL							
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1[g]	for each of the data write requests, identify from the first division operation a third address portion, and use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a	ZBC discloses or at least renders obvious for each of the data write requests, identify from the first division operation a third address portion, and use a second division operation on the third address portion to identify an address value to select one of the erase units from the subset which corresponds to the addressed segment and to identify a storage location within the selected one of the erase units. <i>See, e.g.:</i> 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard:																																																																																											

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	storage location within the selected one of the erase units;	a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where LBA 0 is the lowest LBA of zone 0 and LBA m—1 is the highest LBA of zone n—1. ZBC, Section 4.2.1. If the device server processes a write command with: a) the starting LBA equal to the write pointer; b) the ending LBA is in the same sequential write required zone; and c) an ending LBA that is equal to the last logical block within a physical block, then the device server shall perform write operations for that command. ZBC, Section 4.3.3.3.
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1[h]	wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests; and	ZBC discloses or at least renders obvious said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests. <i>See, e.g.:</i> 3.1.15 write operation process by which a device server performs operations (e.g., write cache operations (see SBC-4) and write medium operations (see SBC-4)) as described in SBC-4																																																																																																												

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		ZBC, Section 3.1.15.
1[i]	wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.	ZBC discloses or at least renders obvious said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests. <i>See, e.g.:</i> 3.1.11 reset write pointer operation process by which a device server sets a write pointer to the lowest LBA of a write pointer zone ZBC, Section 3.1.11. A write pointer zone is a type of zone that has a write pointer that indicates a location within that zone. Each write pointer zone has one write pointer. That write pointer indicates the LBA that the application client should specify in the LOGICAL BLOCK ADDRESS field of a subsequent write command for that write pointer zone. ZBC, Section 4.3.3.1. A read operation on an LBA that has been written since the last reset write pointer operation in that sequential write preferred zone shall return the last written data. A read operation on an LBA that has not been written since the last reset write pointer operation in that sequential write preferred zone shall return user data set to the last initialization pattern that was set by: a) the manufacturer's default initialization pattern;

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		b) the initialization pattern set by the last FORMAT UNIT command (see SBC-4), if any; or c) the initialization pattern set by the last SANITIZE command with the service action set to OVERWRITE (see SBC-4), if any. ZBC, Section 4.3.3.2.
2[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
2[b]	said circuitry comprises at least one processor; and	ZBC discloses or at least renders obvious said circuitry comprises at least one processor. <i>See, e.g.:</i> 3.1.11 reset write pointer operation process by which a device server sets a write pointer to the lowest LBA of a write pointer zone ZBC, Setion 3.1.11. A write pointer zone is a type of zone that has a write pointer that indicates a location within that zone. Each write pointer zone has one write pointer. That write pointer indicates the LBA that the application client should specify in the LOGICAL BLOCK ADDRESS field of a subsequent write command for that write pointer zone. ZBC, Section 4.3.3.1. A read operation on an LBA that has been written since the last reset write pointer operation in that sequential write preferred zone shall return the last written data. A read operation on an LBA that has not been written since the last reset write pointer operation in that sequential

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		write preferred zone shall return user data set to the last initialization pattern that was set by: a) the manufacturer's default initialization pattern; b) the initialization pattern set by the last FORMAT UNIT command (see SBC-4), if any; or c) the initialization pattern set by the last SANITIZE command with the service action set to OVERWRITE (see SBC-4), if any. ZBC, Section 4.3.3.2.
2[c]	the storage device further comprises instructions stored on at least one physical storage medium, said instructions when executed to control the at least one processor.	ZBC discloses or at least renders obvious the storage device further comprises instructions stored on at least one physical storage medium, said instructions when executed to control the at least one processor. <i>See, e.g.:</i> The clauses in this standard, implemented in conjunction with the applicable clauses of SPC-4 and SBC-3, specify the standard command set for SCSI zoned block devices. The objectives of this standard are to: a) permit an application client to communicate over a SCSI service delivery subsystem (see SAM-5) with a logical unit that declares itself to be a zoned block device in the PERIPHERAL DEVICE TYPE field of the standard INQUIRY data (see SPC-4); and b) define commands and parameters unique to the zoned block device type. ZBC, Section 1.

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		3.1.5 host aware zoned block device SCSI target device with the PERIPHERAL DEVICE TYPE field set to 00h (i.e., direct access block device) and the HAW_ZBC bit set to one in the Block Device Characteristics VPD page (see SBC-4) Note 1 to entry: See 4.2.2. ZBC, Section 3.1.5. 3.1.6 host managed zoned block device SCSI target device with the PERIPHERALDEVICE TYPE field set to 14h (i.e., host managed zoned block device) Note 1 to entry: See 4.2.3. ZBC, Section 3.1.6.
3[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
3[b]	said circuitry can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and is to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory	ZBC discloses or at least renders obvious said circuitry can receive a request from a host to copy host-selected data from one storage location in flash memory to another storage location in the flash memory, and is to issue commands to the flash memory, in response to the request from the host to copy, to read the host-selected data from a first physical storage location in the flash memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host. <i>See, e.g.:</i> 6.3.1 EXTENDED COPY command introduction The EXTENDED COPY command (see table 99) provides a means to copy data from one set of logical units to another set of logical units or

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	memory and write the host-selected data to a second physical storage location in the flash memory without sending the data being copied to the host;	to the same set of logical units. The entity within a SCSI device that receives and performs the EXTENDED COPY command is called the copy manager. The copy manager is responsible for copying data from the source devices to the destination devices. The copy source and destination devices are logical units that may reside in different SCSI devices or the same SCSI device. It is possible that the copy source device, copy destination device, and the copy manager are the same logical unit. SPC-4, Section 6.3.1. The application client clears the insufficient resources condition by sending a RESET WRITE POINTER command that specifies the affected zone to the device server. Before sending the RESET WRITE POINTER command, the application client may copy the logical block data in the affected zone to another location. ZBC, Section 4.4.1.
3[c]	the request from the host to copy is to designate destination address information corresponding to the second physical storage location; and	ZBC discloses or at least renders obvious the request from the host to copy is to designate destination address information corresponding to the second physical storage location. <i>See, e.g.:</i> 6.3.1 EXTENDED COPY command introduction The EXTENDED COPY command (see table 99) provides a means to copy data from one set of logical units to another set of logical units or to the same set of logical units. The entity within a SCSI device that receives and performs the EXTENDED COPY command is called the copy manager. The copy manager is responsible for copying data from the source devices to the destination devices. The copy source and destination devices are logical units that may reside in different SCSI devices or the same SCSI device. It is possible that the copy source

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		device, copy destination device, and the copy manager are the same logical unit. SPC-4, Section 6.3.1.
3[d]	the circuitry is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device.	ZBC discloses or at least renders obvious the circuitry is to use the first division operation on the designated destination address information to identify a destination segment within a destination block device. <i>See, e.g.:</i> 1[f].
4[a]	The storage device of claim 3 wherein	ZBC discloses or at least renders obvious the storage device of claim 3. <i>See, e.g.:</i> 3[a]-[d].
4[b]	the circuitry is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit.	ZBC discloses or at least renders obvious the circuitry is to identify from the destination address information a destination logical erase unit and is to select the second physical storage location to be within a physical erase unit that is already mapped to the destination logical erase unit. <i>See, e.g.:</i> 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard: a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where

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		LBA 0 is the lowest LBA of zone 0 and LBA m—1 is the highest LBA of zone n—1. ZBC, Section 4.2.1. If the device server processes a write command with: a) the starting LBA equal to the write pointer; b) the ending LBA is in the same sequential write required zone; and c) an ending LBA that is equal to the last logical block within a physical block, then the device server shall perform write operations for that command. ZBC, Section 4.3.3.3. The ZONE ID field specifies the zone start LBA, if any, of the write pointer zone on which the device server shall perform a reset write pointer operation (see 4.3.3.1). ZBC, Section 5.3.
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		Table 16 — RESET WRITE POINTER command <table><tr><th>Bit Byte</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td colspan="8">OPERATION CODE (9Fh)</td></tr><tr><td>1</td><td colspan="3">Reserved</td><td colspan="5">SERVICE ACTION (14h)</td></tr><tr><td>3</td><td colspan="8">(MSB)</td></tr><tr><td>...</td><td colspan="8">ZONE ID</td></tr><tr><td>9</td><td colspan="8">(LSB)</td></tr><tr><td>10</td><td colspan="8">Reserved</td></tr><tr><td>...</td><td colspan="8">Reserved</td></tr><tr><td>13</td><td colspan="8">Reserved</td></tr><tr><td>14</td><td colspan="7">Reserved</td><td>RESET ALL</td></tr><tr><td>15</td><td colspan="8">CONTROL</td></tr></table> ZBC, Table 16.	Bit Byte	7	6	5	4	3	2	1	0	0	OPERATION CODE (9Fh)								1	Reserved			SERVICE ACTION (14h)					3	(MSB)								...	ZONE ID								9	(LSB)								10	Reserved								...	Reserved								13	Reserved								14	Reserved							RESET ALL	15	CONTROL							
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8[a]	The storage device of claim 1 wherein	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].																																																																																																			
8[b]	the third address portion specifies a location within a sequential range of locations that correspond to the erase units in the subset.	ZBC discloses or at least renders obvious the third address portion specifies a location within a sequential range of locations that correspond to the erase units in the subset. <i>See, e.g.:</i> 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard: a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block																																																																																																			

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		device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where LBA 0 is the lowest LBA of zone 0 and LBA m—1 is the highest LBA of zone n—1. ZBC, Section 4.2.
9[a]	The storage device of claim 1 wherein	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
9[b]	the first division operation and the second division operation each subdivide a value obtained from the incoming address information accompanying each of the write requests into respective bitfields.	ZBC discloses or at least renders obvious the first division operation and the second division operation each subdivide a value obtained from the incoming address information accompanying each of the write requests into respective bitfields. <i>See, e.g.:</i> 4.3.5.3 Logical block address The logical block addresses on a logical unit or within a volume or partition shall begin with block zero and be contiguous up to the last logical block of that logical unit or within that volume or partition. SPC-4, Section 4.3.5.3.

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		<table><tr><th colspan="10">Table 63 — READ (32) command</th></tr><tr><th>Byte</th><th>Bit</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td></td><td colspan="8">OPERATION CODE (7Fh)</td></tr><tr><td>1</td><td></td><td colspan="8">CONTROL</td></tr><tr><td>2</td><td></td><td colspan="8" rowspan="3">Reserved</td></tr><tr><td>...</td><td></td></tr><tr><td>5</td><td></td></tr><tr><td>6</td><td></td><td colspan="3">Reserved</td><td colspan="5">GROUP NUMBER</td></tr><tr><td>7</td><td></td><td colspan="8">ADDITIONAL CDB LENGTH (18h)</td></tr><tr><td>8</td><td>(MSB)</td><td colspan="8">SERVICE ACTION (0009h)</td></tr><tr><td>9</td><td></td><td colspan="7"></td><td>(LSB)</td></tr><tr><td>10</td><td></td><td colspan="3">RDPROTECT</td><td>DPO</td><td>FUA</td><td>RARC</td><td>Obsolete</td><td>Reserved</td></tr><tr><td>11</td><td></td><td colspan="8">Reserved</td></tr><tr><td>12</td><td>(MSB)</td><td colspan="8" rowspan="2">LOGICAL BLOCK ADDRESS</td></tr><tr><td>...</td><td></td></tr><tr><td>19</td><td></td><td colspan="8">(LSB)</td></tr><tr><td>20</td><td>(MSB)</td><td colspan="8" rowspan="2">EXPECTED INITIAL LOGICAL BLOCK REFERENCE TAG</td></tr><tr><td>...</td><td></td></tr><tr><td>23</td><td></td><td colspan="8">(LSB)</td></tr><tr><td>24</td><td>(MSB)</td><td colspan="8">EXPECTED LOGICAL BLOCK APPLICATION TAG</td></tr><tr><td>25</td><td></td><td colspan="8">(LSB)</td></tr><tr><td>26</td><td>(MSB)</td><td colspan="8">LOGICAL BLOCK APPLICATION TAG MASK</td></tr><tr><td>27</td><td></td><td colspan="8">(LSB)</td></tr><tr><td>28</td><td>(MSB)</td><td colspan="8" rowspan="2">TRANSFER LENGTH</td></tr><tr><td>...</td><td></td></tr><tr><td>31</td><td></td><td colspan="8">(LSB)</td></tr></table>	Table 63 — READ (32) command										Byte	Bit	7	6	5	4	3	2	1	0	0		OPERATION CODE (7Fh)								1		CONTROL								2		Reserved								...		5		6		Reserved			GROUP NUMBER					7		ADDITIONAL CDB LENGTH (18h)								8	(MSB)	SERVICE ACTION (0009h)								9									(LSB)	10		RDPROTECT			DPO	FUA	RARC	Obsolete	Reserved	11		Reserved								12	(MSB)	LOGICAL BLOCK ADDRESS								...		19		(LSB)								20	(MSB)	EXPECTED INITIAL LOGICAL BLOCK REFERENCE TAG								...		23		(LSB)								24	(MSB)	EXPECTED LOGICAL BLOCK APPLICATION TAG								25		(LSB)								26	(MSB)	LOGICAL BLOCK APPLICATION TAG MASK								27		(LSB)								28	(MSB)	TRANSFER LENGTH								...		31		(LSB)							
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10[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.</i> : 1[pre]-[i].																																																																																																																																																																																																																												
10[b]	the storage device is to store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;	ZBC discloses or at least renders obvious the storage device is to store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed. <i>See, e.g.</i> : [NA]																																																																																																																																																																																																																												

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10[c]	the storage device is to compare the values representing time since data was programmed to at least one threshold;	ZBC discloses or at least renders obvious the storage device is to compare the values representing time since data was programmed to at least one threshold. <i>See, e.g.:</i> [NA]
10[d]	upon detection that a specific one of the values has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit; and	ZBC discloses or at least renders obvious upon detection that a specific one of the values has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific one of the values from a first physical erase unit to a second physical erase unit. <i>See, e.g.:</i> [NA]
10[e]	the storage device is to remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit.	ZBC discloses or at least renders obvious the storage device is to remap a logical address for the data being copied from the first physical erase unit to the second physical erase unit. <i>See, e.g.:</i> [NA]
11[a]	The storage device of claim 10 wherein:	ZBC discloses or at least renders obvious the storage device of claim 10. <i>See, e.g.:</i> 10[a]-[e].
11[b]	the flash memory is to have block devices, one of the block devices being the addressed block device; and	ZBC discloses or at least renders obvious the flash memory is to have block devices, one of the block devices being the addressed block device. <i>See, e.g.:</i> 4.3.5.3 Logical block address The logical block addresses on a logical unit or within a volume or partition shall begin with block zero and be contiguous up to the last logical block of that logical unit or within that volume or partition.

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		SPC-4, Section 4.3.5.3.
11[c]	the storage device is to identify, for the data being copied, an address of a logical erase unit, the logical erase unit being associated with the addressed block device to the exclusion of each other one of the block devices; and	ZBC discloses or at least renders obvious the storage device is to identify, for the data being copied, an address of a logical erase unit, the logical erase unit being associated with the addressed block device to the exclusion of each other one of the block devices. <i>See, e.g.:</i> 6.3.1 EXTENDED COPY command introduction The EXTENDED COPY command (see table 99) provides a means to copy data from one set of logical units to another set of logical units or to the same set of logical units. The entity within a SCSI device that receives and performs the EXTENDED COPY command is called the copy manager. The copy manager is responsible for copying data from the source devices to the destination devices. The copy source and destination devices are logical units that may reside in different SCSI devices or the same SCSI device. It is possible that the copy source device, copy destination device, and the copy manager are the same logical unit. SPC-4, Section 6.3.1.
11[d]	the storage device is to remap a correspondence between the address of the logical erase unit and the first physical erase unit to instead be between the address of the logical erase unit and the second physical erase unit.	ZBC discloses or at least renders obvious the storage device is to remap a correspondence between the address of the logical erase unit and the first physical erase unit to instead be between the address of the logical erase unit and the second physical erase unit. <i>See, e.g.:</i> The REASSIGN BLOCKS command (see table 77) requests that the device server perform a reassign operation on one or more LBAs (e.g., LBAs referencing logical blocks on which unrecovered read errors occurred) to another area on the medium set aside for this purpose and to add the physical blocks containing those logical blocks to the GLIST. This command shall not alter the contents of the PLIST (see 4.13).

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		SBC-4, Section 5.21.1.
12[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.</i> : 1[pre]-[i].
12[b]	the flash memory is to have block devices, including the addressed block device; and	ZBC discloses or at least renders obvious the flash memory is to have block devices, including the addressed block device. <i>See, e.g.</i> : 11[b].
12[c]	the storage device is to store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory space;	ZBC discloses or at least renders obvious the storage device is to store metadata on an independent basis for portions of flash memory associated with each one of the block devices, wherein the stored metadata is dependent on an erase count of associated physical memory space. <i>See, e.g.</i> : [NA]
12[d]	the storage device is to compare the metadata to at least one threshold;	ZBC discloses or at least renders obvious the storage device is to compare the metadata to at least one threshold. <i>See, e.g.</i> : [NA]
12[e]	upon detection that specific metadata has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific metadata from a first physical erase unit to a second physical erase unit; and	ZBC discloses or at least renders obvious upon detection that specific metadata has satisfied the one or more thresholds, the circuitry is to copy data stored at one or more physical storage locations associated with the specific metadata from a first physical erase unit to a second physical erase unit. <i>See, e.g.</i> : 10[d].

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12[h]	the storage device is to remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit.	ZBC discloses or at least renders obvious the storage device is to remap a logical erase unit value associated with the third address portion from the first physical erase unit to the second physical erase unit. <i>See, e.g.:</i> 10[e].
13[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
13[b]	the erase units of the flash memory are physical erase units;	ZBC discloses or at least renders obvious the erase units of the flash memory are physical erase units. <i>See, e.g.:</i> 1[a], 1[g].
13[c]	the circuitry is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units; and	ZBC discloses or at least renders obvious the circuitry is to use the second division operation to identify a logical erase unit, wherein each logical erase unit is mapped to one of the physical erase units. <i>See, e.g.:</i> The REASSIGN BLOCKS command (see table 77) requests that the device server perform a reassign operation on one or more LBAs (e.g., LBAs referencing logical blocks on which unrecovered read errors occurred) to another area on the medium set aside for this purpose and to add the physical blocks containing those logical blocks to the GLIST. This command shall not alter the contents of the PLIST (see 4.13). SBC-4, Section 5.21.1. 3.1.8 logical block address (LBA) value used to reference a logical block ZBC, Section 3.1.8.

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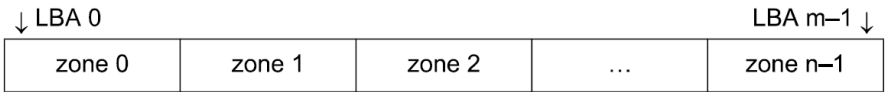
		4.2 Zoned Block Device access models 4.2.1 Zoned Block Device access models overview These are the zoned block device models described in this standard: a) host aware zoned block device; and b) host managed zoned block device. Zoned block devices are accessed using LBAs. The LBAs are divided into ranges called zones (see 4.3). The entire capacity of a zoned block device is organized into a set of contiguous, non-overlapping zones. Figure 1 shows a zoned block device with n zones and m LBAs where LBA 0 is the lowest LBA of zone 0 and LBA m-1 is the highest LBA of zone n-1. ZBC, Section 4.2.1.  Figure 1 — Zones in a zoned block device ZBC, Section 4.2.1.
13[d]	the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for	ZBC discloses or at least renders obvious the storage device is to detect a failure condition of the physical erase units and is to remap each logical erase unit which corresponds to one of the physical erase units for which the failure condition is detected to instead correspond to one of the physical erase units for which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests. <i>See, e.g.:</i> The REASSIGN BLOCKS command (see table 77) requests that the device server perform a reassign operation on one or more LBAs (e.g.,

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	which the failure condition has not been detected and is to utilize the remapped correspondence to service one or more of the incoming data access requests.	LBAs referencing logical blocks on which unrecovered read errors occurred) to another area on the medium set aside for this purpose and to add the physical blocks containing those logical blocks to the GLIST. This command shall not alter the contents of the PLIST (see 4.13). SBC-4, Section 5.21.1. 4.4.3 Media failure Failures may cause some or all of the host managed zoned block device media to become inaccessible. If host managed zoned block device media is still available to be used after a failure, then the media may continue to work properly. ZBC, Section 4.4.3.
14[a]	The storage device of claim 1 wherein the storage device is to:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
14[b]	store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed;	ZBC discloses or at least renders obvious store, for each segment having an erase unit which stores valid data, a value representing a time since data was programmed. <i>See, e.g.:</i> [NA]
14[c]	compare the values representing time since data was programmed to at least one threshold; and	ZBC discloses or at least renders obvious compare the values representing time since data was programmed to at least one threshold. <i>See, e.g.:</i> [NA]
14[d]	responsive to detection of a condition that a specific one of the values representing time	ZBC discloses or at least renders obvious responsive to detection of a condition that a specific one of the values representing time since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted

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	since data was programmed has satisfied the one or more thresholds, transmit information to a host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values.	information conveys address information for data stored at one or more physical storage locations associated with the specific one of the values. <i>See, e.g.:</i> [NA]
15[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
15[b]	the flash memory is to have block devices, including the addressed block device; and	ZBC discloses or at least renders obvious the flash memory is to have block devices, including the addressed block device. <i>See, e.g.:</i> 11[b].
15[c]	the storage device is further to:	ZBC discloses or at least renders obvious the storage device is further to. <i>See, e.g.:</i> 15[d]-[f].
15[d]	store metadata on an independent basis for portions of flash memory associated with each one of the block devices,	ZBC discloses or at least renders obvious store metadata on an independent basis for portions of flash memory associated with each one of the block devices. <i>See, e.g.:</i> 12[c].
15[e]	receive a query, issued by a host, directed to a specific one of the block devices, and	ZBC discloses or at least renders obvious receive a query, issued by a host, directed to a specific one of the block devices. <i>See, e.g.:</i> ZBC, Section 3.1.6. 5.2 REPORT ZONES command

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		5.2.1 REPORT ZONES command introduction The REPORT ZONES command (see table 10) requests that the device server return the zone structure of the zoned block device. ZBC, Section 5.2.1.
15[f]	responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata.	ZBC discloses or at least renders obvious responsive to the query, compare the metadata to at least one threshold, to identify specific metadata, and transmit information to the host wherein such transmitted information conveys address information for data stored at one or more physical storage locations associated with the specific metadata. <i>See, e.g.:</i> A RESET bit set to zero indicates that the device server has sufficient resources to maintain the zone described by this zone descriptor. A RESET bit set to one indicates that the application client should send a RESET WRITE POINTER command (see 5.3) that specifies the zone described by this zone descriptor as described in 4.4.1. If the zone type is conventional or sequential write preferred (see table 14), then the device server shall not set the RESET bit to one. The device server shall set the RESET bit to zero for conventional zones. ZBC, Section 5.2.2.

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		Table 12 — REPORT ZONES parameter data							
Bit Byte	7	6	5	4	3	2	1	0	
1	(MSB)								
...	ZONE LIST LENGTH (n-63)								
3	(LSB)								
4	Reserved							SAME	
5	Reserved								
...									
63									
Zone descriptors list									
64	Zone descriptor [first]								
...									
127									
	⋮								
n-63	Zone descriptor [last]								
...									
n									

ZBC, Section 5.2.2.

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		<table><tr><th colspan="9">Table 13 — Zone descriptor format</th></tr><tr><th>Bit Byte</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td colspan="4">Reserved</td><td colspan="4">ZONE TYPE</td></tr><tr><td>1</td><td colspan="4">ZONE CONDITION</td><td colspan="3">Reserved</td><td>RESET</td></tr><tr><td>2</td><td colspan="8" rowspan="3">Reserved</td></tr><tr><td>...</td></tr><tr><td>7</td></tr><tr><td>8</td><td>(MSB)</td><td colspan="7" rowspan="3">ZONE LENGTH</td></tr><tr><td>...</td></tr><tr><td>15</td><td>(LSB)</td></tr><tr><td>16</td><td>(MSB)</td><td colspan="7" rowspan="3">ZONE START LBA</td></tr><tr><td>...</td></tr><tr><td>23</td><td>(LSB)</td></tr><tr><td>24</td><td>(MSB)</td><td colspan="7" rowspan="3">WRITE POINTER LBA</td></tr><tr><td>...</td></tr><tr><td>31</td><td>(LSB)</td></tr><tr><td>32</td><td colspan="8" rowspan="3">Reserved</td></tr><tr><td>...</td></tr><tr><td>63</td></tr></table>	Table 13 — Zone descriptor format									Bit Byte	7	6	5	4	3	2	1	0	0	Reserved				ZONE TYPE				1	ZONE CONDITION				Reserved			RESET	2	Reserved								...	7	8	(MSB)	ZONE LENGTH							...	15	(LSB)	16	(MSB)	ZONE START LBA							...	23	(LSB)	24	(MSB)	WRITE POINTER LBA							...	31	(LSB)	32	Reserved								...	63
Table 13 — Zone descriptor format																																																																																																
Bit Byte	7	6	5	4	3	2	1	0																																																																																								
0	Reserved				ZONE TYPE																																																																																											
1	ZONE CONDITION				Reserved			RESET																																																																																								
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8	(MSB)	ZONE LENGTH																																																																																														
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16	(MSB)	ZONE START LBA																																																																																														
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23	(LSB)																																																																																															
24	(MSB)	WRITE POINTER LBA																																																																																														
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31	(LSB)																																																																																															
32	Reserved																																																																																															
...																																																																																																
63																																																																																																
		ZBC, Section 5.2.2.																																																																																														
18[a]	The storage device of claim 1 wherein:	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].																																																																																														
18[b]	the flash memory comprises multiple planes; and	ZBC discloses or at least renders obvious the flash memory comprises multiple planes. <i>See, e.g.:</i> This purpose of this standard is to define the model and command set extensions to be used in conjunction with the SCSI Primary Command Set standard —4 (SPC-4) and the SCSI Block Commands - 3 (SBC-3) to facilitate operation of SCSI zoned block devices.																																																																																														

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		ZBC, Foreword. This standard defines the command set extensions to facilitate operation of SCSI zoned block devices. ZBC, Section 1.
18[c]	the circuitry is to, for each one of a set of the data write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page.	ZBC discloses or at least renders obvious the circuitry is to, for each one of a set of the data write requests having sequential addressing, identify a commonly addressed page and concurrently write data accompanying the set of write requests into respective ones of the multiple planes in a manner corresponding to the commonly addressed page. <i>See, e.g.:</i>

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Table 63 — READ (32) command									
Byte	Bit	7	6	5	4	3	2	1	0
0		OPERATION CODE (7Fh)							
1		CONTROL							
2		Reserved							
...									
5									
6		Reserved			GROUP NUMBER				
7		ADDITIONAL CDB LENGTH (18h)							
8	(MSB)	SERVICE ACTION (0009h)							
9									
10		RDPROTECT			DPO	FUA	RARC	Obsolete	Reserved
11		Reserved							
12	(MSB)	LOGICAL BLOCK ADDRESS							
...									
19		(LSB)							
20	(MSB)	EXPECTED INITIAL LOGICAL BLOCK REFERENCE TAG							
...									
23		(LSB)							
24	(MSB)	EXPECTED LOGICAL BLOCK APPLICATION TAG							
25		(LSB)							
26	(MSB)	LOGICAL BLOCK APPLICATION TAG MASK							
27		(LSB)							
28	(MSB)	TRANSFER LENGTH							
...									
31		(LSB)							

SBC-4, Table 63.

3.1.13 sequential write required zone

write pointer zone in which the device server requires that write operations specify a first LBA that is equal to that zone’s write pointer

ZBC, Section 3.1.13.

Figure 3 shows a write pointer zone where LBAs have been written since the last reset write pointer operation for that zone (i.e., LBAs less

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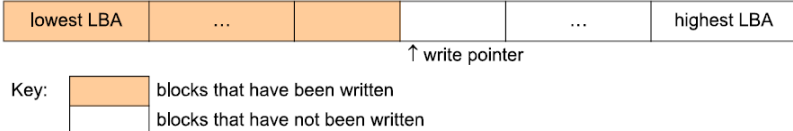
		than the write pointer value) and LBAs have not been written since the last reset write pointer operation for that zone (i.e., LBAs greater than or equal to the write pointer value). ZBC, Section 4.3.3.1.  Figure 3 — Write pointer zone and write pointer ZBC, Figure 3.
19[pre]	A storage device comprising:	ZBC discloses or at least renders obvious a storage device. <i>See, e.g.:</i> 1[pre].
19[a]	flash memory comprising erase units; and	ZBC discloses or at least renders obvious flash memory comprising erase units. <i>See, e.g.:</i> 1[a].
19[b]	circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;	ZBC discloses or at least renders obvious circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information. <i>See, e.g.:</i> 1[b].
19[c]	wherein said circuitry is to, for each of the incoming requests:	ZBC discloses or at least renders obvious said circuitry is to, for each of the incoming requests. <i>See, e.g.:</i> 1[c].

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19[d]	derive, from the accompanying incoming address information, a first address portion and a second address portion,	ZBC discloses or at least renders obvious derive, from the accompanying incoming address information, a first address portion and a second address portion. <i>See, e.g.:</i> 1[d].
19[e]	identify an addressed block device from the first address portion,	ZBC discloses or at least renders obvious identify an addressed block device from the first address portion. <i>See, e.g.:</i> 1[e].
19[f]	use a first operation on the second address portion to subdivide the incoming address information into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and	ZBC discloses or at least renders obvious use a first operation on the second address portion to subdivide the incoming address information into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory. <i>See, e.g.:</i> 1[f], 9[b].
19[g]	for each of the data write requests, use a second one of the first bit fields as a third address portion and use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields and to identify a storage location within the selected one of the	ZBC discloses or at least renders obvious for each of the data write requests, use a second one of the first bit fields as a third address portion and use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields and to identify a storage location within the selected one of the erase units from a second one of the second bit fields. <i>See, e.g.:</i> 1[g], 9[b].

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	erase units from a second one of the second bit fields;	
19[h]	wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests;	ZBC discloses or at least renders obvious said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests. <i>See, e.g.</i> : 1[h].
19[i]	wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.	ZBC discloses or at least renders obvious said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests. <i>See, e.g.</i> : 1[i].
20[pre]	A storage device comprising:	ZBC discloses or at least renders obvious a storage device. <i>See, e.g.</i> : 1[pre].
20[a]	flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate	ZBC discloses or at least renders obvious flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each

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	level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments; and	segment being associated with only one of the block devices, each erase unit being associated with only one of the segments. <i>See, e.g.</i> : 1[a], 1[e]-[g].
20[b]	circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;	ZBC discloses or at least renders obvious circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information. <i>See, e.g.</i> : 1[b].
20[c]	wherein said circuitry is to, for each of incoming requests:	ZBC discloses or at least renders obvious derive a first address portion and a second address portion. <i>See, e.g.</i> : 1[c].
20[d]	derive a first address portion and a second address portion,	ZBC discloses or at least renders obvious derive a first address portion and a second address portion. <i>See, e.g.</i> : 1[d].
20[e]	identify an addressed one of the block devices from the first address portion,	ZBC discloses or at least renders obvious identify an addressed one of the block devices from the first address portion. <i>See, e.g.</i> : 1[e].
20[f]	use a first operation to subdivide the second address	ZBC discloses or at least renders obvious use a first operation to subdivide the second address portion into first bit fields, and to identify an addressed segment within the

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	portion into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields, and to identify a third address portion from a second one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and	addressed block device from a first one of the first bit fields, and to identify a third address portion from a second one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory. <i>See, e.g.</i> : 1[f], 9[b].
20[g]	for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields, and to identify a storage location within the selected one of the erase units from a second one of the second bit fields;	ZBC discloses or at least renders obvious for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify an address value to select one of the erase units from a first one of the second bit fields, and to identify a storage location within the selected one of the erase units from a second one of the second bit fields. <i>See, e.g.</i> : 1[g], 9[b].
20[h]	wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests;	ZBC discloses or at least renders obvious said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the data write requests. <i>See, e.g.</i> : 1[h].

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20[i]	wherein said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.	ZBC discloses or at least renders obvious said circuitry is also to execute each one of the incoming erase requests by controlling erasure in the flash memory of one or more of the erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests. <i>See, e.g.</i> : 1[i].
21[pre]	A storage device comprising:	ZBC discloses or at least renders obvious a storage device. <i>See, e.g.</i> : 1[pre].
21[a]	flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase	ZBC discloses or at least renders obvious flash memory, the flash memory to have one or more block devices at a hierarchically-superior level, segments within each of the block devices at a hierarchically-intermediate level, and addressable storage locations within each of the segments at a hierarchically-inferior level, each segment corresponding to a respective, mutually exclusive set of one or more erase units, each segment being associated with only one of the block devices, each erase unit being associated with only one of the segments. <i>See, e.g.</i> : 1[a], 1[e]-[g].

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	unit being associated with only one of the segments; and	
21[b]	circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information;	ZBC discloses or at least renders obvious circuitry to receive from a host, and control execution of, incoming requests including data write requests and erase requests, wherein each of the incoming requests is accompanied by incoming address information. <i>See, e.g.:</i> 1[b].
21[c]	wherein said circuitry is to, for each of the incoming requests:	ZBC discloses or at least renders obvious derive, from the accompanying incoming address information, a first address portion and a second address portion. <i>See, e.g.:</i> 1[c].
21[d]	derive, from the accompanying incoming address information, a first address portion and a second address portion,	ZBC discloses or at least renders obvious derive, from the accompanying incoming address information, a first address portion and a second address portion. <i>See, e.g.:</i> 1[d].
21[e]	identify an addressed one of the block devices from the first address portion,	ZBC discloses or at least renders obvious identify an addressed one of the block devices from the first address portion. <i>See, e.g.:</i> 1[e].
21[f]	use a first operation to subdivide the second address portion into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields and a third address portion from a second	ZBC discloses or at least renders obvious use a first operation to subdivide the second address portion into first bit fields, and to identify an addressed segment within the addressed block device from a first one of the first bit fields and a third address portion from a second one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory. <i>See, e.g.:</i> 1[f], 9[b].

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	one of the first bit fields, wherein the addressed segment corresponds to a subset of the erase units of the flash memory, and	
21[g]	for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify, from a first one of the second bit fields, an address value to select one of the erase units and, from a second one of the second bit fields a storage location within the selected one of the erase units;	ZBC discloses or at least renders obvious for each of the data write requests, use a second operation to subdivide the third address portion into second bit fields, to identify, from a first one of the second bit fields, an address value to select one of the erase units and, from a second one of the second bit fields a storage location within the selected one of the erase units. <i>See, e.g.: 1[g], 9[b].</i>
21[h]	wherein said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the incoming data write requests; and	ZBC discloses or at least renders obvious said circuitry is to execute each one of the data write requests by programming accompanying data into the storage location that was identified for that one of the incoming data write requests. <i>See, e.g.: 1[h].</i>
21[i]	wherein said circuitry is also to execute each one of incoming erase requests by controlling erasure in the flash memory of the one or more erase units in the subset corresponding to the	ZBC discloses or at least renders obvious said circuitry is also to execute each one of incoming erase requests by controlling erasure in the flash memory of the one or more erase units in the subset corresponding to the addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests. <i>See, e.g.: 1[i].</i>

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	addressed segment that was identified from the incoming address information accompanying the one of the incoming erase requests.	
22[a]	The storage device of claim 1 wherein	ZBC discloses or at least renders obvious the storage device of claim 1. <i>See, e.g.:</i> 1[pre]-[i].
22[b]	the second address portion comprises a first set of bits and a second set of bits, the bits of the first set of bits being mutually-exclusive to the bits of the second set of bits, wherein the first division operation is to separate the first set of bits from the second set of bits, and the circuitry is to identify the addressed segment from the first set of bits.	ZBC discloses or at least renders obvious the second address portion comprises a first set of bits and a second set of bits, the bits of the first set of bits being mutually-exclusive to the bits of the second set of bits, wherein the first division operation is to separate the first set of bits from the second set of bits, and the circuitry is to identify the addressed segment from the first set of bits. <i>See, e.g.:</i> 1[f], 9[b].