# SFP-DD MSA

## SFP-DD Hardware Specification

## for

## SFP DOUBLE DENSITY 2X PLUGGABLE TRANSCEIVER

Rev 3.0 April 10, 2019

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable SFP Double Density (SFP-DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Change History:

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| | | |
|---|---|---|
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| 2.3 | February 16 2019 | Added SN and MDC optical connectors |
| 3.0 | April 10 2019 | Added SN, MDC connectors to Table 9.<br>Deleted requirement that host shall not change the state of LPMode when module is present (4.1.1.7).<br>Added 'Latch disengaged to first four entries in Table 8 |

**Foreword**

The development work on this specification was done by the SFP-DD MSA, an industry group. The membership of the committee since its formation in May 2017 has included a mix of companies which are leaders across the industry.

The members of the SFP-DD MSA would like to acknowledge the contributions of Edmund Poh. He was an excellent engineer; his technical skills and collaborative attitude will be missed.

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# SFP-DD 2X Pluggable Transceiver

## 1. Scope

The scope of this specification is the definition of a high density 2-channel module, cage and connector system. SFP-DD supports up to 100 Gb/s in aggregate over a 2 x 50Gb/s electrical interface. The cage and connector design provides backwards compatibility to SFP28 modules which can be inserted into a SFP-DD cage and connector using 1 of the electrical channels.

### 1.1 Description of Sections

Section 1 Scope and Purpose

Section 2 Referenced and Related Standards and SFF Specifications

Section 3 Introduction

Section 4 Electrical specifications

Section 5 Mechanical specifications, printed circuit board recommendations, labeling, color code recommendations and optical interface examples.

Section 6 Environmental and thermal considerations

Section 7 Management Interface Timing

## 2. References

### 2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- IEEE Std 802.3
- IEEE Std 802.3by
- IEEE Std 802.3bs
- IEEE Std 802.3cd
- InfiniBand Architecture Specifications
- FC-PI-7
- OIF CEI-56G-VSR-PAM4
- SFP-DD Management Interface

SFF Specifications

- INF-8438 QSFP (Quad SFP) 4 Gbps 4X Transceiver
- SFF-8636 Shielded Cables Common Management Interface
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8661 QSFP+ 4X Pluggable Module
- SFF-8679 QSFP28 4X Base Electrical Specification
- SFF-8402 SFP28 1x Pluggable Module
- SFF-8071 SFP+ 1x0.8mm Card Edge Connector
- SFF-8432 SFP+ Module and Cage

## 2.2 Sources

This document can be obtained via the www.SFP-DD.com web site.

# 3 Introduction

This Specification covers the following items:

- Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

- Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified.

- Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

- Thermal requirements

- Management Interface Timing requirements

- Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

- Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

- Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

- Management Registers

## 3.1 Objectives

Electrical signal contact and channel assignments, electrical and power requirements defined in Section 4 and optical lane assignments defined in Section 5 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Section 5 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

## 3.2 Applications

This specification defines a connector, cage and module for single or double lane applications at up to 58 Gb/s per lane. Intended applications include but are not limited to Ethernet and/or InfiniBand and/or Fibre Channel. The SFP-DD interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.
An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the SFP-DD module.

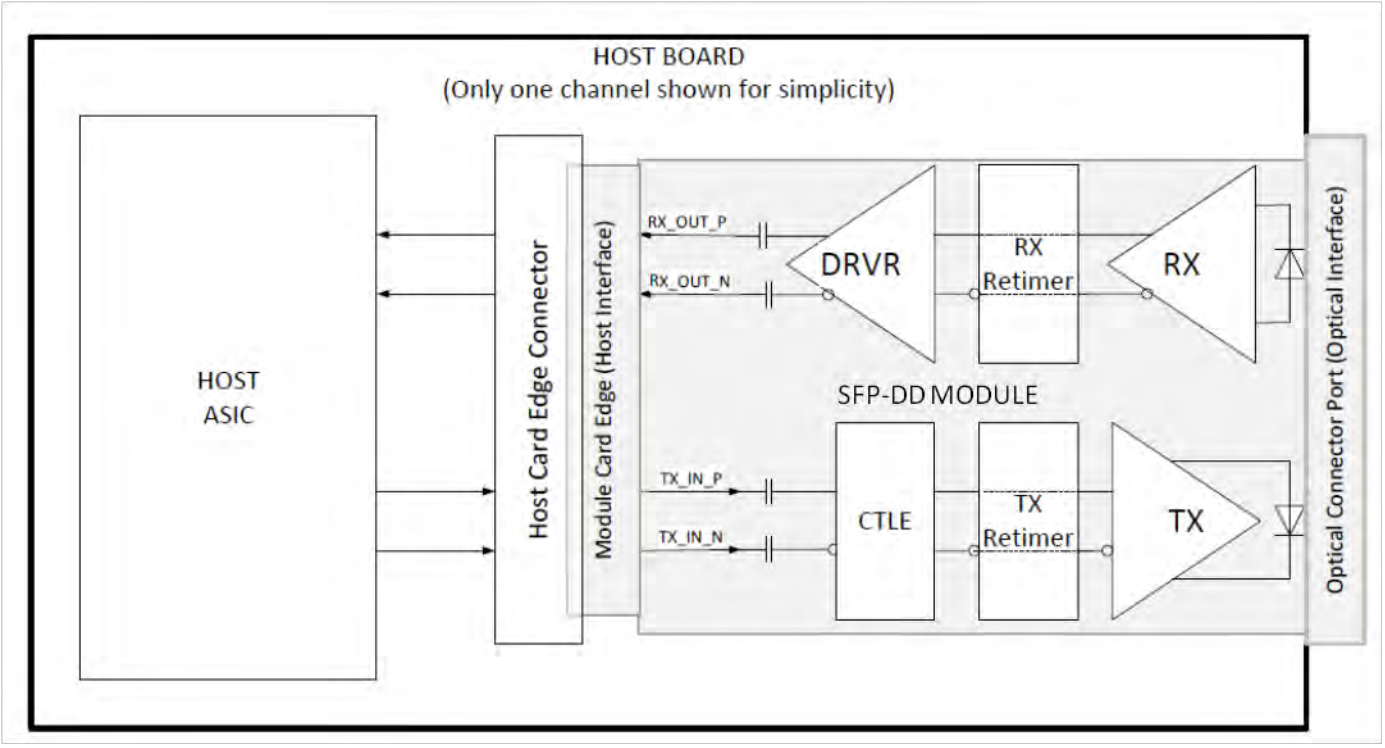


**Figure 1: Application Reference Model**

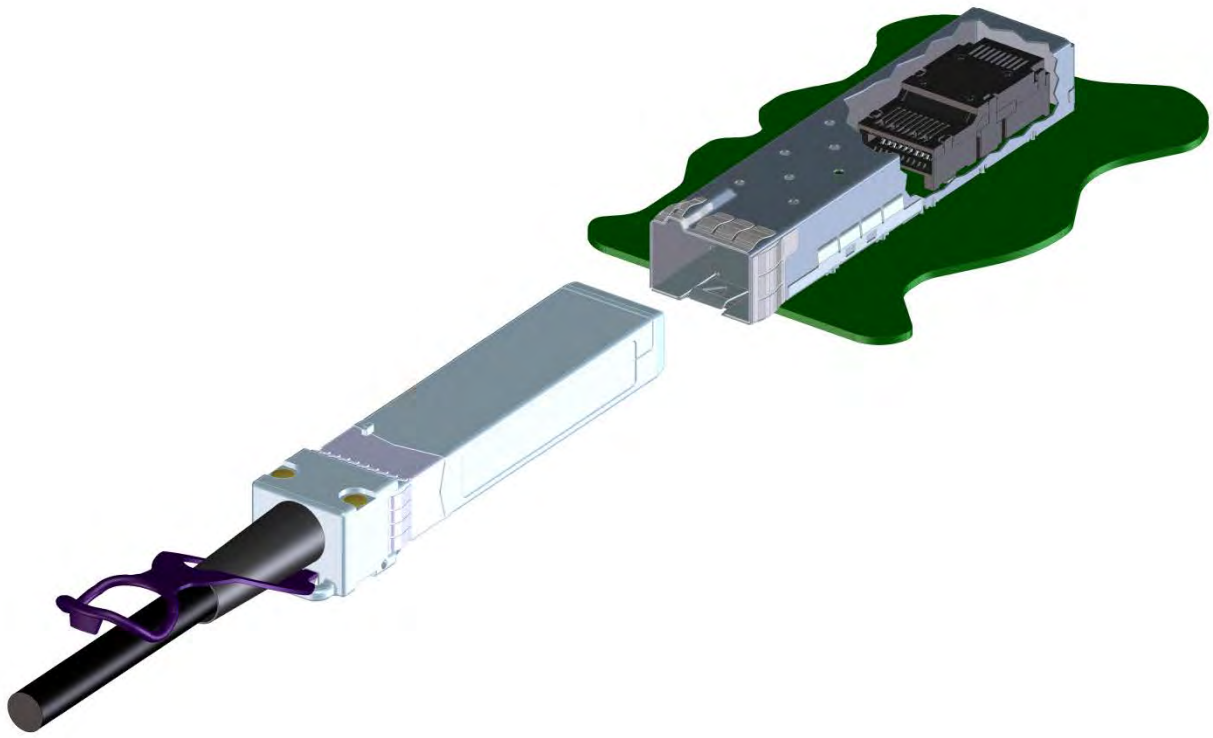

**Figure 2: SFP-DD Cage, Connector and Module**

# 4 Electrical Specification

This section contains signal definitions and requirements that are specific to the SFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

## 4.1 Electrical Connector

The SFP-DD module edge connector consists of a single paddle card with 20 pads on the top and 20 pads on the bottom of the paddle card for a total of 40 pads. The pads positions are defined to allow insertion of either an SFP-DD module or an SFP28 into the SFP-DD receptacle. The legacy/channel 0 signal locations are deeper on the paddlecard, so that legacy/channel 0 SFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins open circuited in a SFP application.

The pads are designed for a sequenced mating:

First mate – ground pads
Second mate – power pads
Third mate – signal pads

Figure 3 shows the signal symbols and pad numbering for the SFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 40 pads intended for high speed signals, low speed signals, power and ground connections. Table 1 provides more information about each of the 40 pads. Figure 14 and Figure 15 show pad dimensions.

For EMI protection the signals from the host connector should be shut off when the SFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the SFP-DD module should be isolated from the module’s

circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

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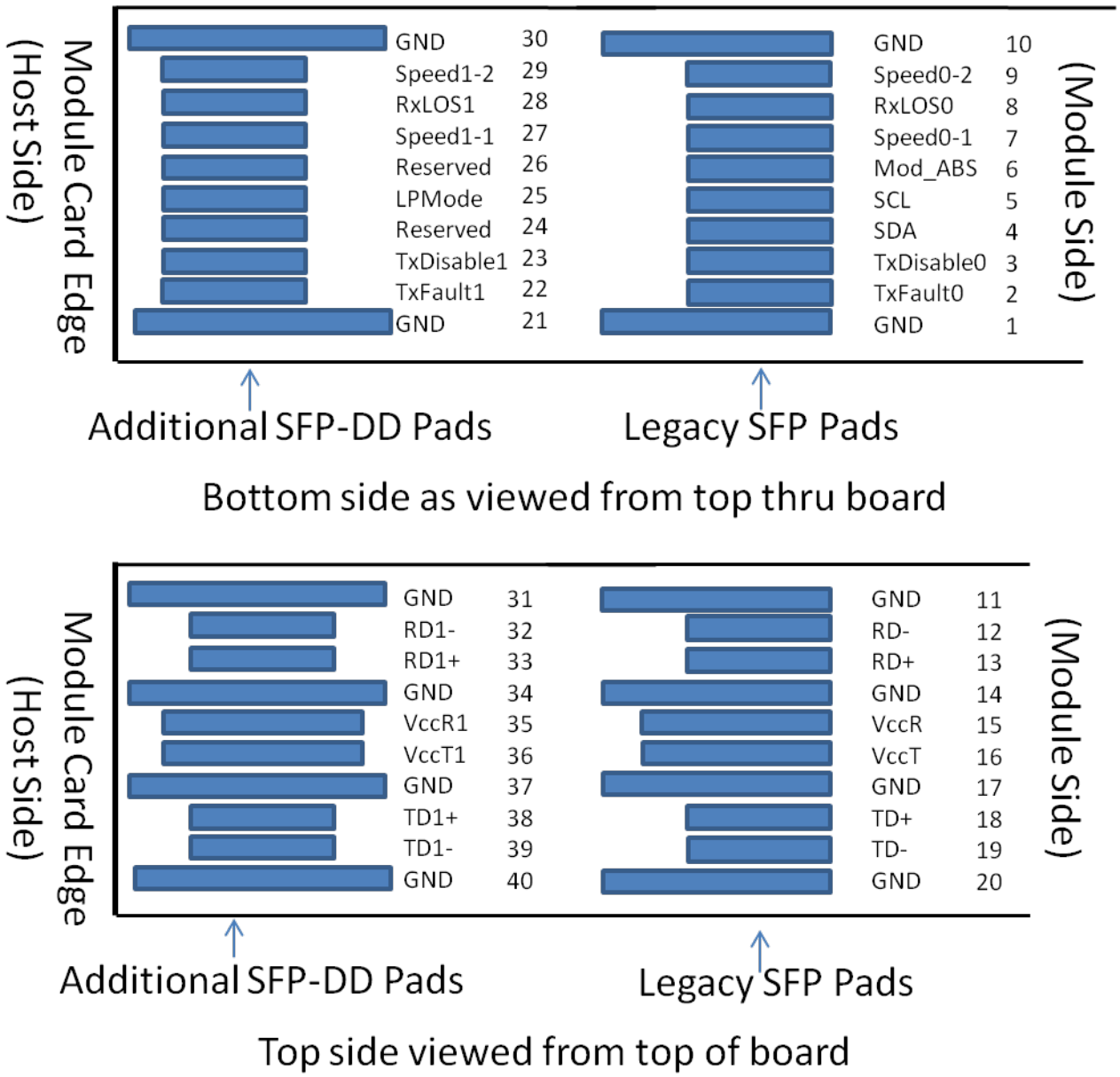



**Figure 3: Module pad layout**

Because the SFP-DD module has 2 rows of pads, the additional SFP-DD pads will have an intermittent connection with the legacy SFP pins in the connector during the module insertion and removal. The 'legacy' SFP pads have a 'channel 0' label shown in Table 1 to designate them as the second row of module pads to contact the SFP-DD connector. The additional SFP-DD pads have an 'channel 1' label in Table 1 to designate them as the first row of module pads to contact the SFP-DD connector. The additional SFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy SFP pads and the respective additional SFP-DD pads are simultaneous.

For a reliable interconnect, a sufficient contact wipe of the connector pins sliding over the module gold pads is required. In the past, long signal pads have been used to provide the mechanical wipe. As operating speeds were relatively slow, the electrical stub was not an issue with signal integrity.

As operating speeds have increased, signal pad lengths have become shorter and shorter to reduce electrical stubs, however this caused insufficient mechanical wipe. A solution is to add a small separation of the signal pad such that there is a passive 'pre-wipe" pad and an active signal pad. In SFP-DD, there are also long pre-wipe pads between the additional SFP-DD pads and the legacy SFP pads. This provides connector pins a gold platted pad surface to slide between rows.

**Table 1- Pad Function Definition**

| Pad | Logic | Symbol | Module Pad Descriptions | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1A | 1 |
| 2 | LVTTL-O | Tx Fault0 | Transmitter Fault Indication for channel 0 | 3A | |
| 3 | LVTTL-I | TxDisable0 | Transmitter Disable for channel 0 | 3A | |
| 4 | LVCMOS-I/O | SDA | Management I/F data line | 3A | |
| 5 | LVCMOS-I/O | SCL | Management I/F clock | 3A | |
| 6 | LVTTL-O | Mod_ABS | Module Absent | 3A | |
| 7 | LVTTL-I | Speed0-1 | Rx Rate Select for channel 0 | 3A | |
| 8 | LVTTL-O | RxLOS0 | Rx Loss of Signal for channel 0 | 3A | |
| 9 | LVTTL-I | Speed0-2 | Tx Rate Select for channel 0 | 3A | |
| 10 | | GND | Ground | 1A | 1 |
| 11 | | GND | Ground | 1A | 1 |
| 12 | CML-O | RD0- | Inverse Received Data Out for channel 0 | 3A | |
| 13 | CML-O | RD0+ | Received Data Out for channel 0 | 3A | |
| 14 | | GND | Ground | 1A | 1 |
| 15 | | VccR0 | Receiver Power | 2A | 2 |
| 16 | | VccT0 | Transmitter Power | 2A | 2 |
| 17 | | GND | Ground | 1A | 1 |
| 18 | CML-I | TD0+ | Transmit Data In for channel 0 | 3A | |
| 19 | CML-I | TD0- | Inverse Transmit Data In for channel 0 | 3A | |
| 20 | | GND | Ground | 1A | 1 |
| 21 | | GND | Ground | 1B | 1 |
| 22 | LVTTL-O | TxFault1 | Transmitter Fault Indication/Interrupt for channel 1 | 3B | |
| 23 | LVTTL-I | TxDisable1 | Transmitter Disable for channel 1 | 3B | |
| 24 | | Reserved | Reserved for future use | 3B | |
| 25 | LVTTL-I | LPMode | Low Power Mode Control | 3B | |
| 26 | | Reserved | Reserved for Future Use | 3B | 3 |
| 27 | LVTTL-I | Speed1-1 | Rx Rate Select for channel 1 | 3B | |
| 28 | LVTTL-O | RxLOS1 | Loss of Signal for channel 1 | 3B | |
| 29 | LVTTL-I | Speed1-2 | Tx Rate Select for channel 1 | 3B | |
| 30 | | GND | Ground | 1B | 1 |
| 31 | | GND | Ground | 1B | 1 |
| 32 | CML-O | RD1- | Inverse Received Data Out for channel 1 | 3B | |
| 33 | CML-O | RD1+ | Received Data Out for channel 1 | 3B | |
| 34 | | GND | Ground | 1B | 1 |
| 35 | | VccR1 | Receiver Power for channel 1 | 2B | 2 |
| 36 | | VccT1 | Transmitter Power for channel 1 | 2B | 2 |
| 37 | | GND | Ground | 1B | 1 |
| 38 | CML-I | TD1+ | Transmit Data In for channel 1 | 3B | |
| 39 | CML-I | TD1- | Inverse Transmit Data In for channel 1 | 3B | |
| 40 | | GND | Ground | 1B | 1 |

| |
|---|
| Note 1: SFP-DD uses common ground (GND)for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. |
| Note 2: VccR0, VccT0 shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 5. VccR0, VccT0, VccR1, VccT1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA. |
| Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Vendor specific and Reserved pads shall have an impedance to GND looking into the module, of greater than 10 kOhms and less than 100 pF. |
| Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional SFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B. |

Figure 4, Figure 5 and Figure 6 show examples of SFP-DD host PCB schematics with connections to CDR and control ICs. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

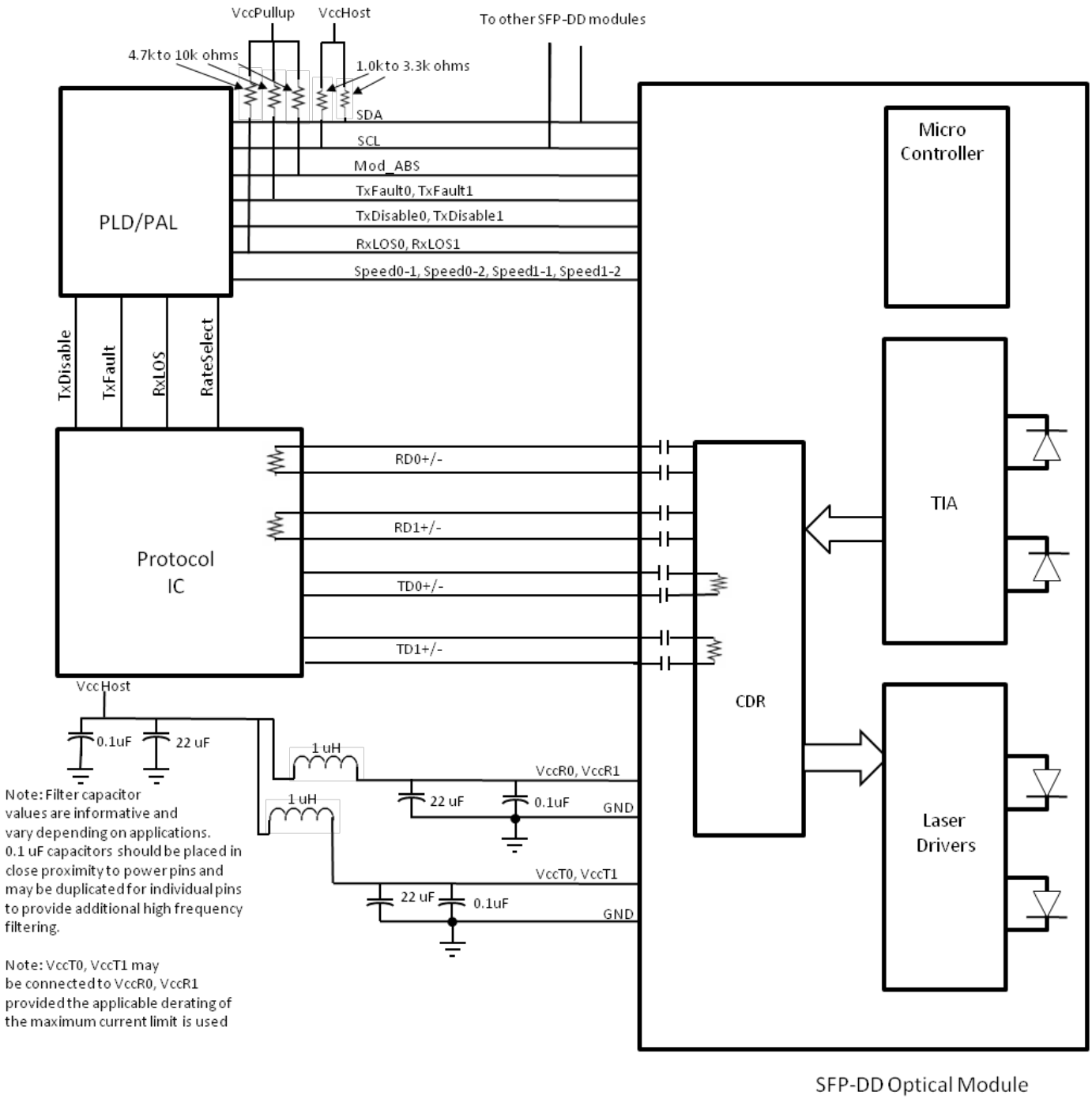



**Figure 4: Example SFP-DD Host Board Schematic For Optical Modules**

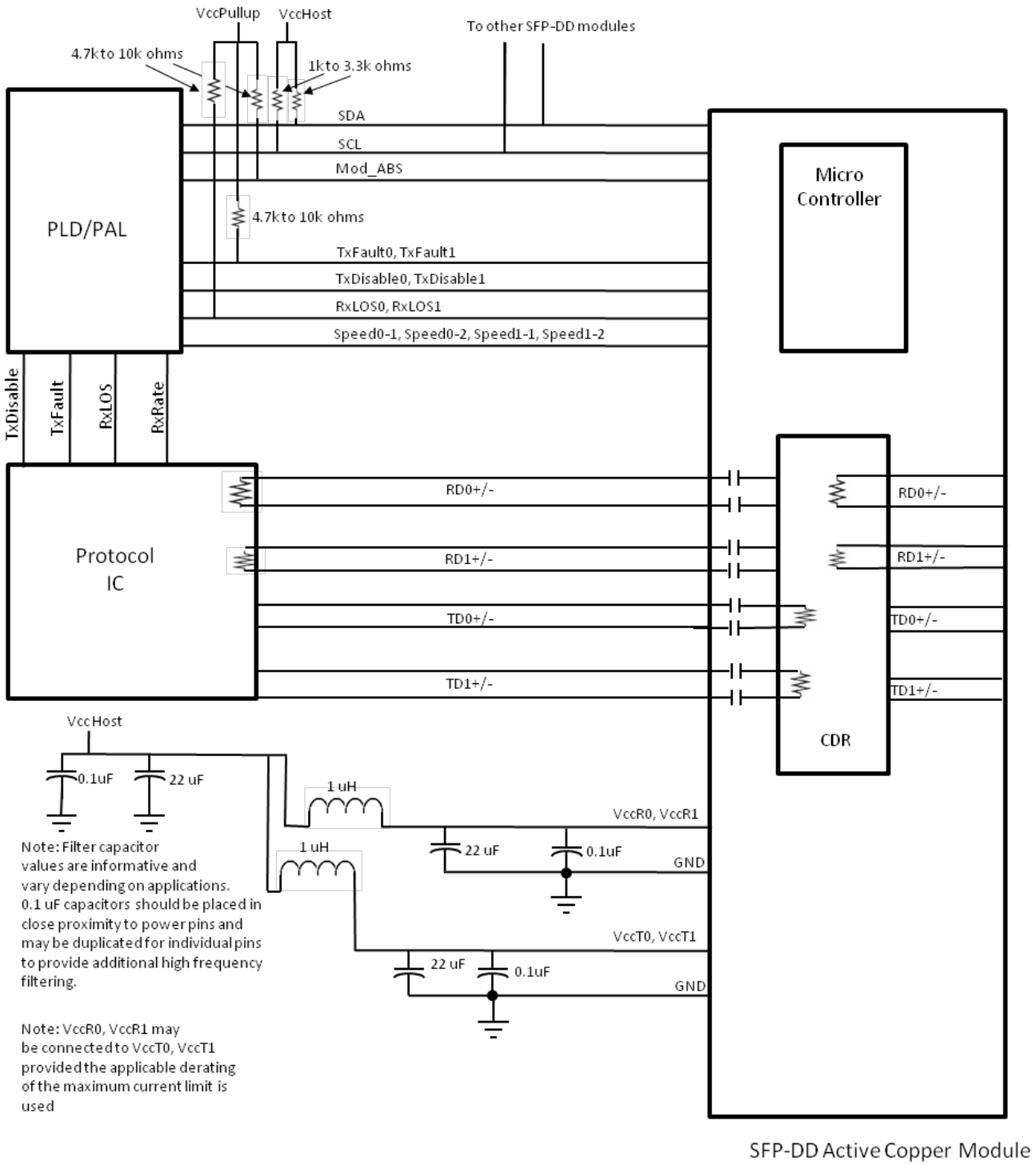



**Figure 5: Example SFP-DD Host Board Schematic for active copper cables**

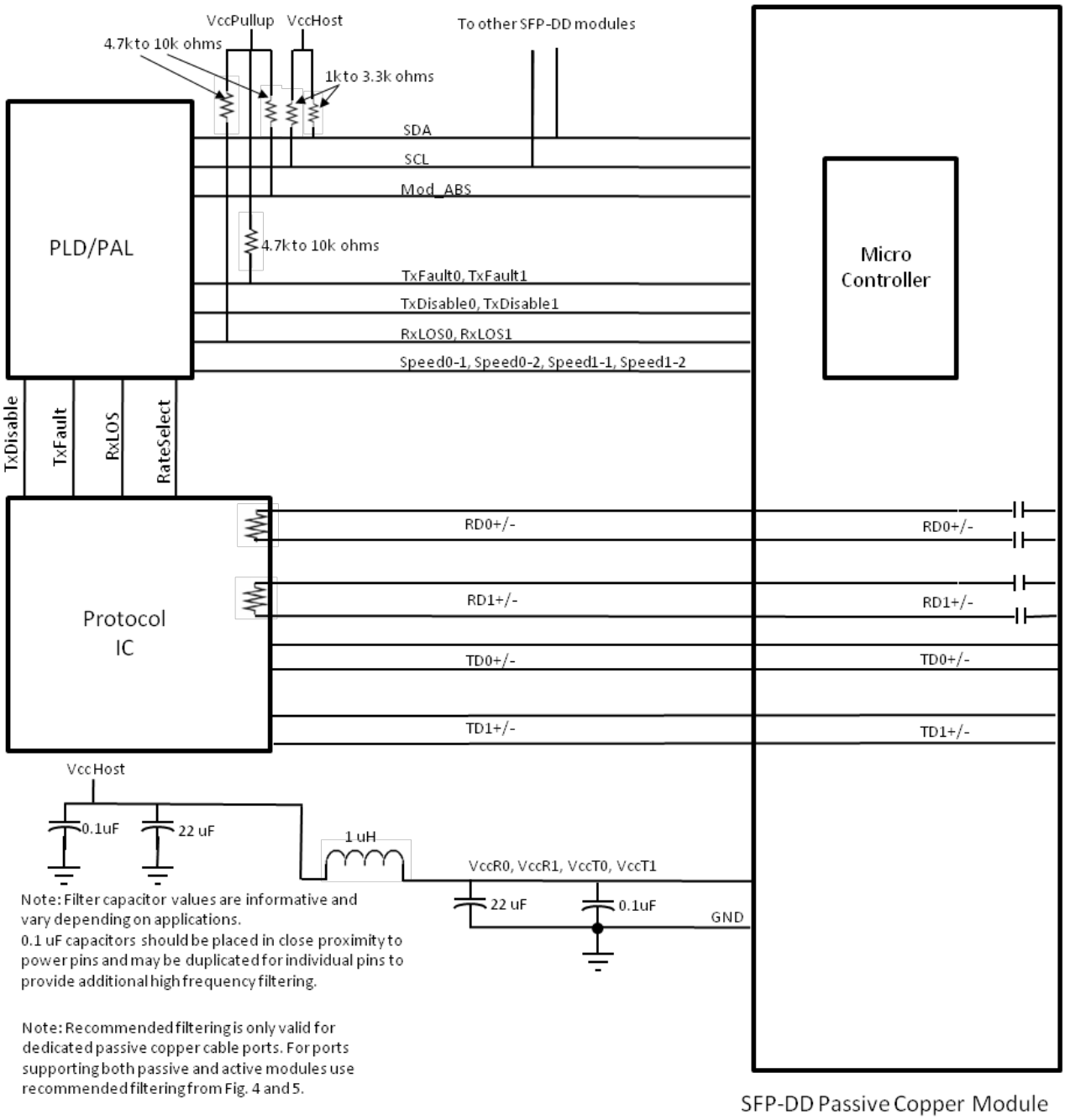



**Figure 6: Example SFP-DD Host Board Schematic for passive copper cables**

### 4.1.1 Low Speed Electrical Hardware Signals

The module has the following low speed signals for control, status and management by the host:

TxFault0, TxFault1
TxDisable0, TxDisable1
SDA
SCL
Mod_ABS
Speed0-1, Speed0-2, Speed1-1, Speed1-2
RxLOS0, RxLOS1
LPMode

#### 4.1.1.1 TxFault0, TxFault1

Tx_Fault0 and TxFault1 are module outputs that when high, indicate that the module transmitter has detected a fault/flag/warning condition for the appropriate channel. If Tx_Fault0 and/or TxFault1 are not implemented, the contact signal shall be held low by the module and may be connected to GND within the module. The Tx_Fault0 and TxFault1 outputs are open drain/collector and shall be pulled up to the Vcc_Host in the host with a resistor in the range 4.7 kOhms to 10 kOhms, or with an active termination according to Table 2.

#### 4.1.1.2 TxDisable0, TxDisable1

When TxDisable0 or TxDisable1 are asserted high or left open, the appropriate SFP-DD module transmitter output shall be turned off unless the module is a passive cable assembly in which case this signal may be ignored. This contact shall be pulled up to VccT in modules and cable assemblies. Tx_Disable0 and TxDisable1 are module input contacts. When TxDisable0 or TxDisable1 are asserted low or grounded the module transmitter is operating normally.

#### 4.1.1.3 Speed0-1, Speed0-2, Speed1-1, Speed1-2

Speed0-1, Speed0-2, Speed1-1 and Speed1-2 are module inputs and are pulled low to GND with >30 kOhms resistors in the module. Speed0-1 optionally selects the optical receive signaling rate for channel 0. Speed1-1 optionally selects the optical receive signaling rate for channel 1. Speed0-2 optionally selects the optical transmit signaling rate for the channel 0. Speed1-2 optionally selects the optical transmit signaling rate for channel 1. For logical definitions of Speed0-1, Speed0-2, Speed1-1, Speed1-2 see Section 4.2.

#### 4.1.1.4 Mod_ABS

Mod_ABS must be pulled up to Vcc Host on the host board and pulled low in the module (see Table 2). The Mod_ABS is asserted “Low” when the module is inserted. The Mod_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

#### 4.1.1.5 SCL, SDA

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to Vcc_Host by resistors in the host. For full specifications see Section 7 Management Interface Timing.

#### 4.1.1.6 RxLOS0, RxLOS1

Rx Loss of Signal indication. When high indicates an optical signal level below that specified in the relevant standard. LOS is an open drain/collector output with a resistive pull up to Vcc_Host as specified in Table 2.

LOS may be an optional function depending on the supported standard. If the LOS function is not implemented, or is reported via the two-wire interface only, the RxLOS contact shall be held low by the module and may be connected to GND within the module.

RxLOS0, RxLOS1 assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of LOS a minimum hysteresis of 0.5 dBo is recommended.

#### 4.1.1.7 LPMode

LPMode is an input signal from the host operating with active high logic. The LPMode signal must be pulled up to Vcc in the SFP-DD module. The LPMode signal allows the host to define whether the SFP-DD module will remain in Low Power Mode until software enables the transition to High Power Mode as defined in the SFP-DD management specification. In Low Power Mode (LPMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

### 4.1.2 Low Speed Electrical Specification

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at a module supply Vcc of 3.3V +/- 5% and with a host supply Vcc_Host range of 2.38 to 3.46V. Vcc refers to the generic supply voltages of VccTx, VccRx, VccPullup or Vcc1.

### 4.1.3 2 Wire Management Interface Specification

The 2-wire interface protocol and timing specifications are defined in SFF-8472. Editors note: This reference is still in development.

The SFP-DD low speed electrical specifications are given in Table 2. This specification ensures compatibility between host bus masters and the 2-wire interface.

**Table 2- Low Speed Control and Sense Signals**

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| SCL and SDA | VOL | 0 | 0.4 | V | Iout=3.0mA for fast mode, 20ma for fast-mode plus |
| | VOH | | | | |
| SCL and SDA | VIL | -0.3 | Vcc*0.3 | V | |
| | VIH | Vcc*0.7 | Vcc+0.5 | V | |
| Capacitance for SCL and SDA I/O signal | Ci | | 14 | pF | |
| Total bus capacitive load for SCL and SDA | Cb | | 100 | pF | For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure x. |
| | | | 200 | pF | For 400kHz clock rate use 1.6 k Ohms pullup resistor max. For 1000kHz clock rate refer to Figure x. |
| TxDisable, LPMode, Speed | VIL | -0.3 | 0.8 | V | \|Iin\|<=360 uA for 0V<Vin,Vcc |
| | VIH | 2 | Vcc+0.3 | V | |
| Mod_ABS | VOL | 0 | 0.4 | V | IOL=2.0ma |
| | VOH | | | | Mod_ABS can be implemented as a short-circuit to GND on the module |
| RxLOS, TxFault | VOL | -0.3 | 0.40 | V | 4.7k Ohm Pullup resistor to Vcc_Host where Vcc_Host_min<Vcc_Host<Vcc_Host_max |
| | IOH | -50 | 37.5 | uA | |

### 4.1.4 High Speed Electrical Specification

For detailed electrical specifications see the appropriate specification, e.g. 802.3ba Annex 86A, 802.3bs Annex 120E, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification.

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.1.4.1 and 4.1.4.2 may be used.

#### 4.1.4.1 RD0+, RD0-, RD1+, RD1-

RD(n)+/- are SFP-DD module receiver data outputs. Rx(n)+/- are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the SFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Section 5.10.5. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

#### 4.1.4.2 TD0+, TD0-, TD1+, TD1-

TD(n)+/- are SFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the SFP-DD optical module. The AC coupling is implemented inside the SFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter TX Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where TX Squelch is implemented, the default case has TX Squelch active. TX Squelch can be deactivated using TX Squelch Disable through the 2-wire serial interface. TX Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

## 4.2 Rate Select Hardware Control

The module provides 4 inputs Speed0-1, Speed0-2, Speed1-1 and Speed1-2 that can optionally be used for rate selection as defined in Table 3. Speed0-1, Speed1-1 specifies the highest rate advertised by the channel. Speed0-2, Speed1-2 specifies a lower speed for each channel. Speed0-1 controls the receive path signaling rate capability for the channel 0 receive path. Speed1-1 controls the receive path signaling rate capability for the channel 1 receive path. Similarly, Speed0-2 controls the transmit path signaling rate capability for channel 0 and Speed1-2 controls the transmit path signaling rate capability for the channel 1 transmit path.

The rate select functionality can also be controlled by software as defined by the SFP-DD management specification.

The Rate select Hardware Control is intended to be compatible with Fibre Channel 64GFC rate select methodology.

**Table 3- Rate Select Hardware Control**

| Parameter | State | Conditions |
|---|---|---|
| Speed0-1, Speed1-1 | Low | RX signaling rate of 14Gbaud |
| | High | RX signaling rate of 28Gbaud |
| Speed0-2, Speed1-2 | Low | TX signaling rate of 14Gbaud |
| | High | TX signaling rate of 28Gbaud |

## 4.3 Power Requirements

The power supply has four designated pins, VccT0, VccT1 VccR0, VccR1 in the connector. Power is applied concurrently to VccT0, VccR0 in the row for channel 0 and concurrently to VccT1, VccR1 in the row for channel 1.

A host board together with the SFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 5 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

### 4.3.1 Power Classes and Maximum Power Consumption

There are multiple power classes as defined in Table 4. Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host identify the power class of the module before allowing the module to go into high power mode.

Power levels associated with classifications of modules are shown in Table 4.

**Table 4- Power Classification**

| Power Class | Max Power (W) |
|---|---|
| 1 | 1.0 |
| 2 | 1.5 |
| 3 | 2.0 |
| 4 | 3.5 |
| 5 | 5.0 |
| 6 | reserved |
| 7 | reserved |
| 8 | See management register for maximum power consumption |

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

### 4.3.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 7.

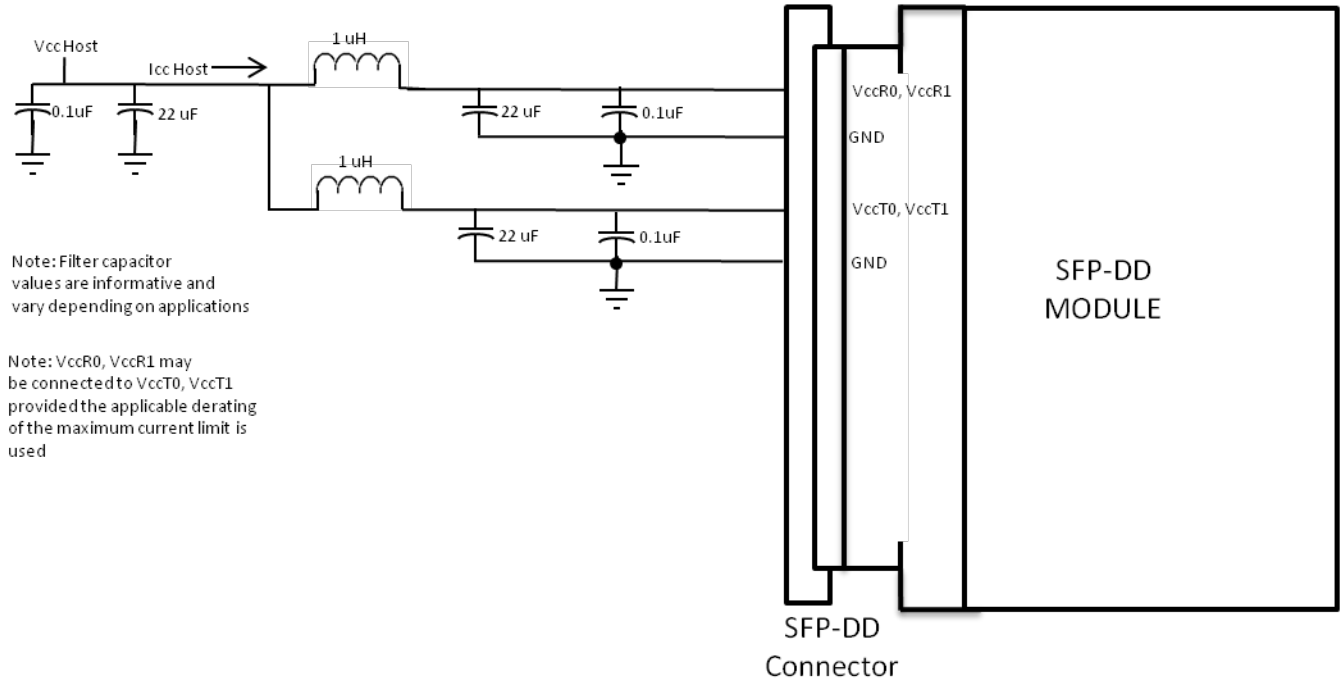



**Figure 7: Recommended Host Board Power Supply Filtering**

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 ohm.

The specifications for the power supply are shown in Table 5. The limits in Table 5 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 7). The test method for measuring inrush current can be found in Keysight Technologies application brief 5991-2778EN.pdf.

### 4.3.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all SFP-DD modules shall power up in Low Power Mode if InitMode is asserted. If InitMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 8 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 5.

**Table 5- Power Supply specifications, Instantaneous, sustained and steady state current limits**

| Parameter | Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltages VccTx0, VccTx1, VccRx0, VccRx1 including ripple, droop and noise below 100kHz[1] | | 3.135 | 3.3 | 3.465 | V |
| Host RMS noise output 10 Hz-10 MHz | | | | 25 | mV |
| Module RMS noise output 10 Hz - 10 MHz | | | | 15 | mV |
| Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak) | $PSNR_{mod}$ | | | 66 | mV |
| Module inrush - instantaneous peak duration | T_ip | | | 50 | µs |
| Module inrush - initialization time | T_init | | | 500 | ms |
| Low Power Mode[2] | | | | | |
| Power Consumption | P_lp | | .5 | | W |
| Instantaneous peak current at hot plug | Icc_ip_lp | - | 200 | | mA |
| Sustained peak current at hot plug | Icc_sp_lp | - | 165 | | mA |
| Steady state current | Icc_lp | See Note 4 | | | mA |
| High Power Class 1 module | | | | | |
| Power Consumption | P_1 | | 1.0 | | W |
| Instantaneous peak current | Icc_ip_1 | - | 400 | | mA |
| Sustained peak current | Icc_sp_1 | - | 330 | | mA |
| Steady state current | Icc_1 | See Note 4 | | | mA |
| High Power Class 2 module | | | | | |
| Power Consumption | P_2 | | 1.5 | | W |
| Instantaneous peak current | Icc_ip_2 | - | 600 | | mA |
| Sustained peak current | Icc_sp_2 | - | 495 | | mA |
| Steady state current | Icc_2 | See Note 4 | | | mA |
| High Power Class 3 module | | | | | |
| Power Consumption | P_3 | | 2.0 | | W |
| Instantaneous peak current | Icc_ip_3 | - | 800 | | mA |
| Sustained peak current | Icc_sp_3 | - | 660 | | mA |
| Steady state current | Icc_3 | See Note 4 | | | mA |
| High Power Class 4 module | | | | | |
| Power Consumption | P_4 | | 3.5 | | W |
| Instantaneous peak current | Icc_ip_4 | - | 1400 | | mA |
| Sustained peak current | Icc_sp_4 | - | 1155 | | mA |
| Steady state current | Icc_4 | See Note 4 | | | mA |
| High Power Class 5 module | | | | | |
| Power Consumption | P_5 | | 5.0 | | W |
| Instantaneous peak current | Icc_ip_5 | - | 2000 | | mA |
| Sustained peak current | Icc_sp_5 | - | 1650 | | mA |
| Steady state current | Icc_5 | See Note 4 | | | mA |
| High Power Class 8 module | | | | | |
| Power Consumption | P_8[3] | | | | W |
| Instantaneous peak current | Icc_ip_8 | - | - | P_8/2.5 | A |
| Sustained peak current | Icc_sp_8 | - | - | P_8/3.03 | A |
| Steady state current | Icc_8 | - | - | 4 | A |

Note 1: Measured at VccT, VccR
Note 2: Host designers are responsible for handling 1.5W Low Power Mode SFP legacy modules as appropriate in their system.
Note 3: User must read management register for maximum power consumption
Note 4: The module must stay within its declared power class.

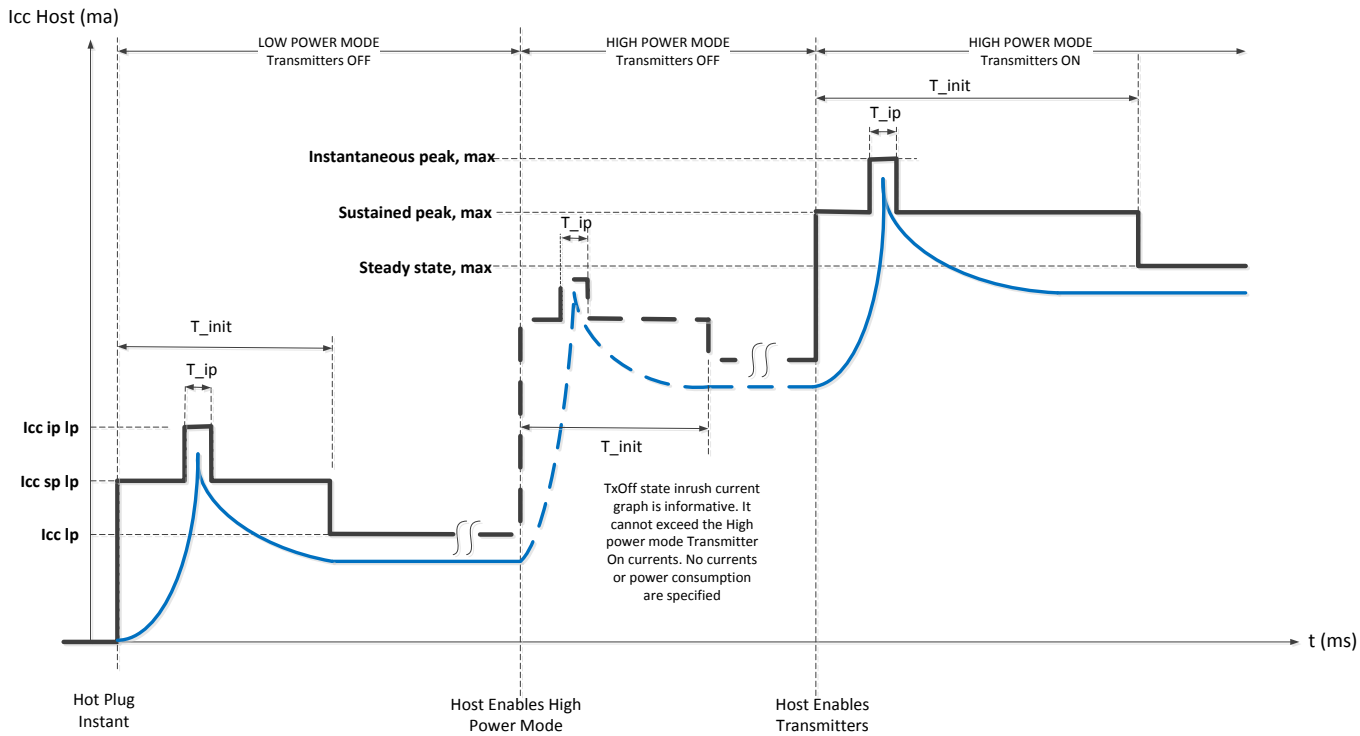



**Figure 8: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)**

### 4.3.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 5 when tested by the methods of SFF-8419, section A.1.1.

### 4.3.5 Module Power Supply Noise Output

The SFP-DD module shall generate less than the value in Table 5 when tested by the methods of SFF-8419, section A.1.1. Note: The series resister value may need to be reduced for high power modules.

### 4.3.6 Module Power Supply Noise Tolerance

The SFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 5, swept from 10 Hz to 10 MHz according to the methods of SFF-8419, section A.1.1. This emulates the worst case noise output of the host.

## 4.4 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the SFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the SFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

# 5 Mechanical and Board Definition

## 5.1 Introduction

The cages and modules defined in this section are illustrated in Figure 9 (press fit cage) and Figure 10 (pluggable module). All Pluggable modules and direct attach cable plugs must mate to the connectors and cages defined in this specification. (See SFF-8432 for details) Heat sink/clip thermal designs are application specific and not specifically defined by this specification. The SFP-DD module and cage support both a pull tab and a bail latch solution. Details on bail latch retention and extraction specifications can be found in SFF-8432.

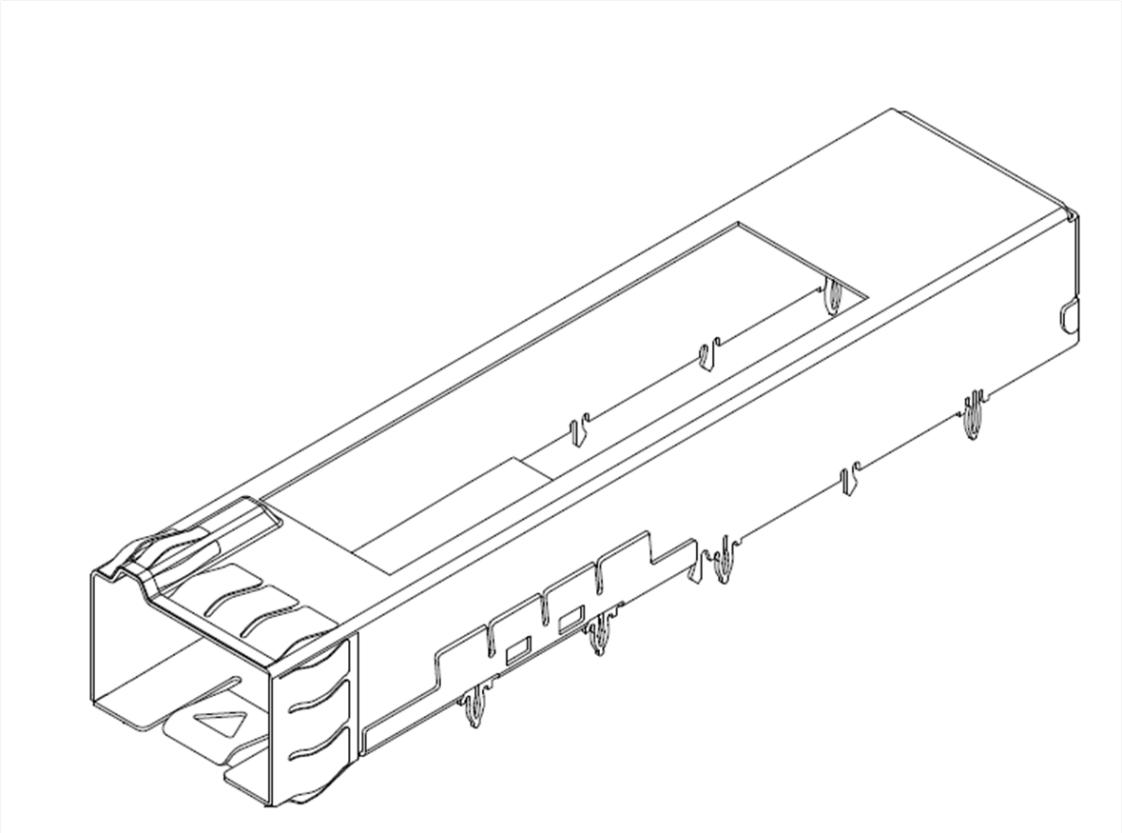
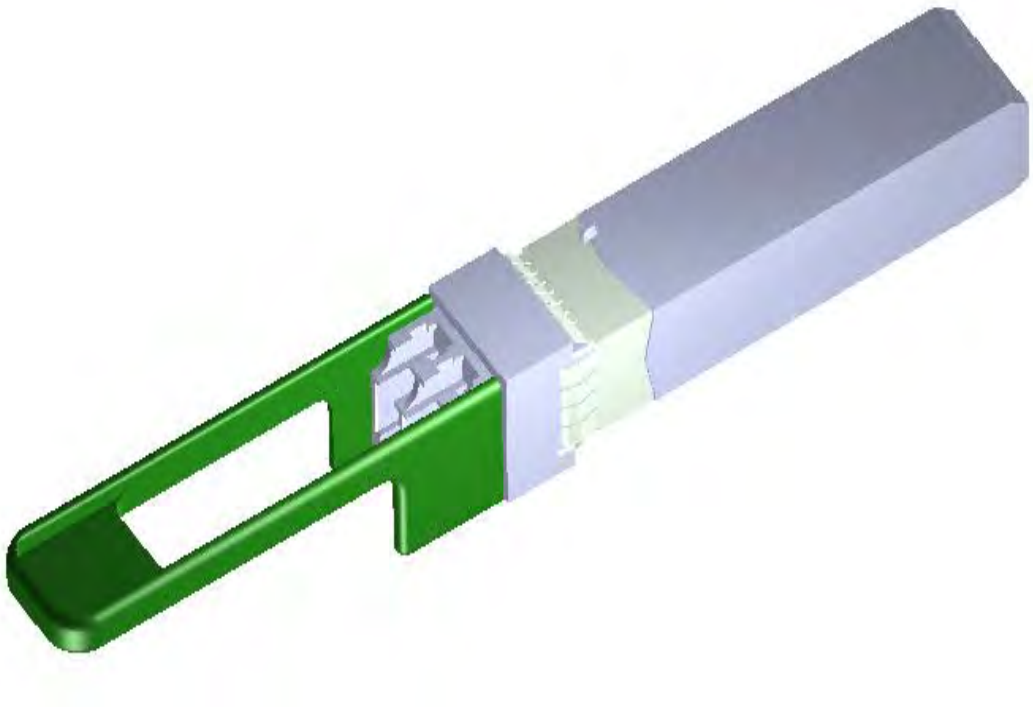
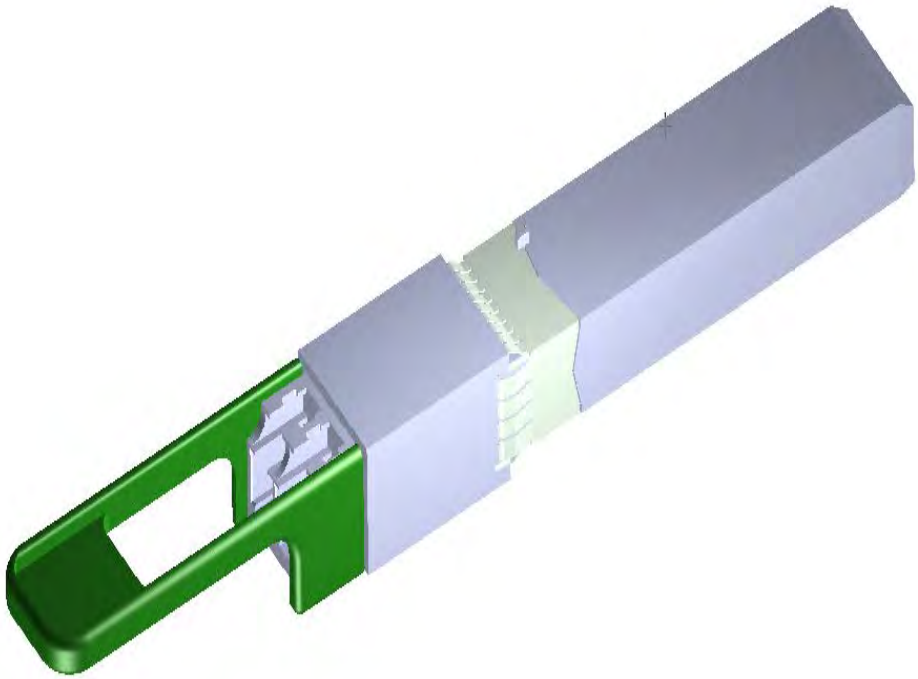


**Figure 9: Press fit cage**



**Type 1 module**



**Type 2 module**

**Figure 10: Modules**

**Table 6- Datum Description**

| Datum | Description |
|---|---|
| A | Width Of module |
| B | Bottom surface of module |
| C | Leading edge of signal contact pads on module paddle card |
| D | Hard stop on module |
| E | Host board thru hole to accept primary cage press fit pin |
| F | Hard stop on cage |
| G | Bottom surface of bezel cutout |
| K | Host board thru hole #1 to accept connector guide post |
| L | Host board thru hole #2 to accept connector guide post |
| P | Vertical center line of internal surface of cage |
| S | Seating plane of cage on host board |
| Z | Top surface of host board |
| AA | Center line of module paddle card width |
| BB | Top surface of module paddle card |
| CC | Center line of connector slot width |
| DD | Seating plane of connector on host board |

## 5.2 Cage, Connector, Module Alignment

The alignment of the cage, connector and module are shown in Figure **11**.

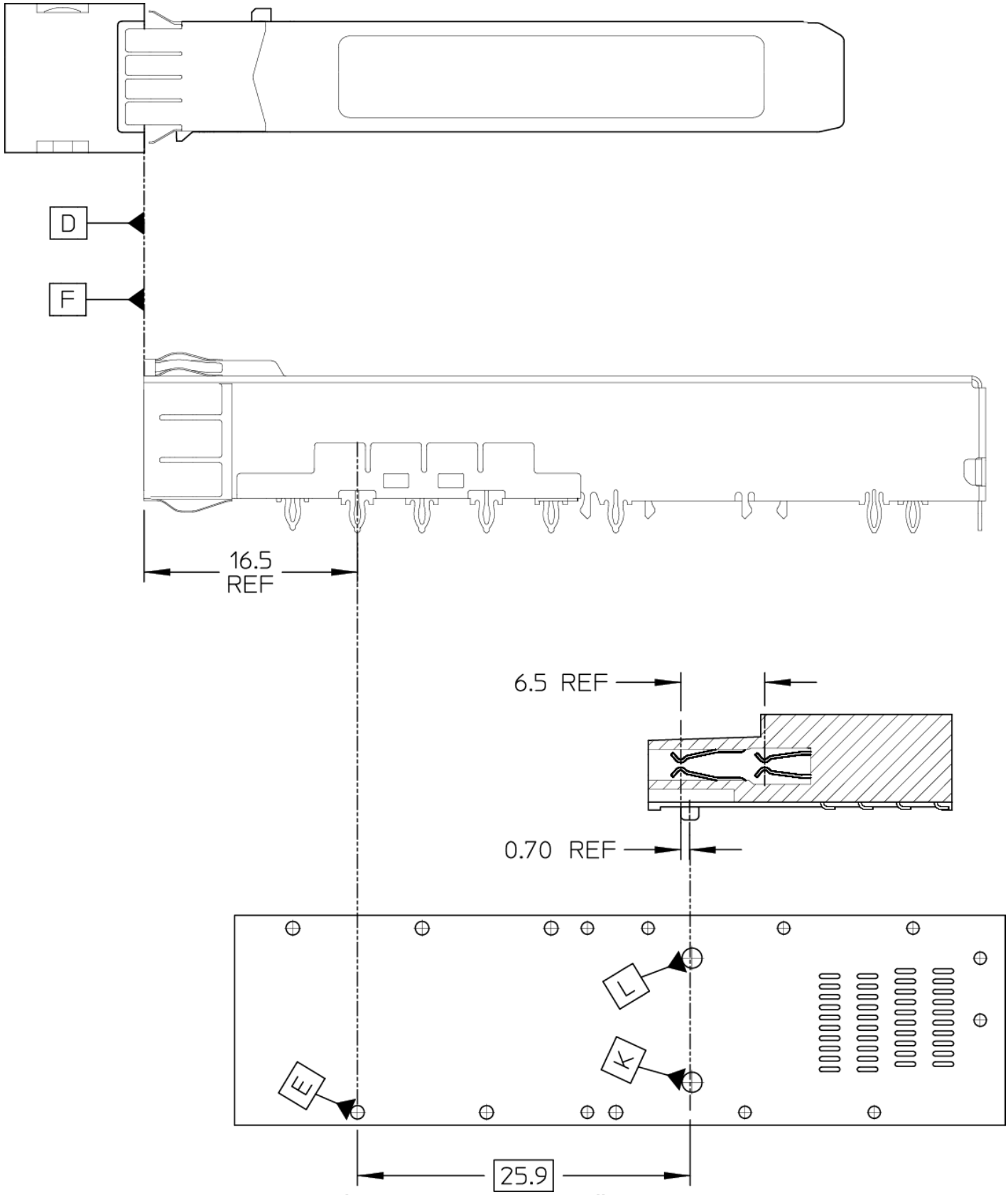
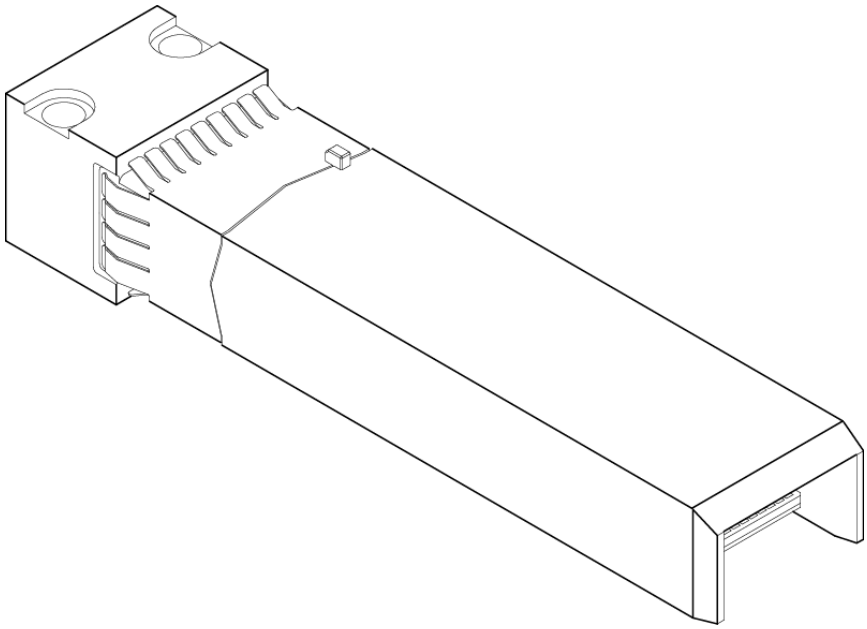


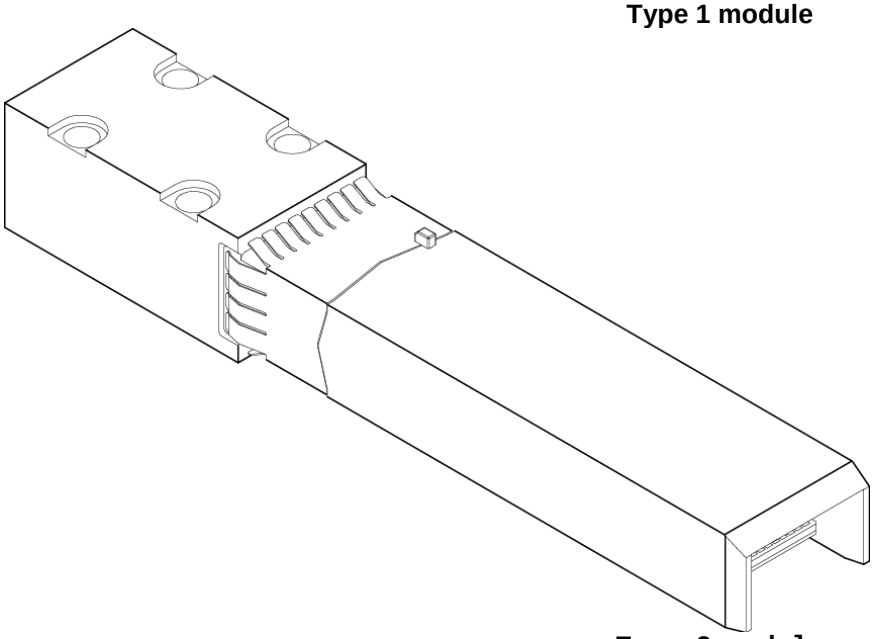

**Figure 11: Cage, Connector alignment**

## 5.3 Module Mechanical Dimensions

The mechanical outline for the SFP-DD module and direct attach cables is shown in Figure 12. The module shall provide a means to self-lock with the cage upon insertion. The module package dimensions are defined in Figure 13. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 13.



**Type 1 module**



**Type 2 module**

**Figure 12: Type 1 and Type 2 Modules**

NOTES APPLY TO MODULE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS.

3. RECOMMENDED MAXIMUM. MODULE LENGTH EXTENDING OUTSIDE OF CAGE. OTHER LENGTHS ARE APPLICATION SPECIFIC.

4. INDICATED OUTLINE DEFINES MAXIMUM ENVELOP OUTSIDE THE CAGE. THE SURFACES OF THE MAXIMUM ENVELOP MAY BE CONTACTED BY AN ADJACENT MODULE EMI SPRINGS DURING INSERTION AND EXTRACTION OF THE MODULE FROM THE CAGE. THE SURFACES SHALL NOT HAVE ANY SHAPES OR MATERIALS THAT CAN DAMAGE THE ADJACENT MODULE EMI SPRINGS OR BE DAMAGED THEMSELVES BY THE SPRINGS.

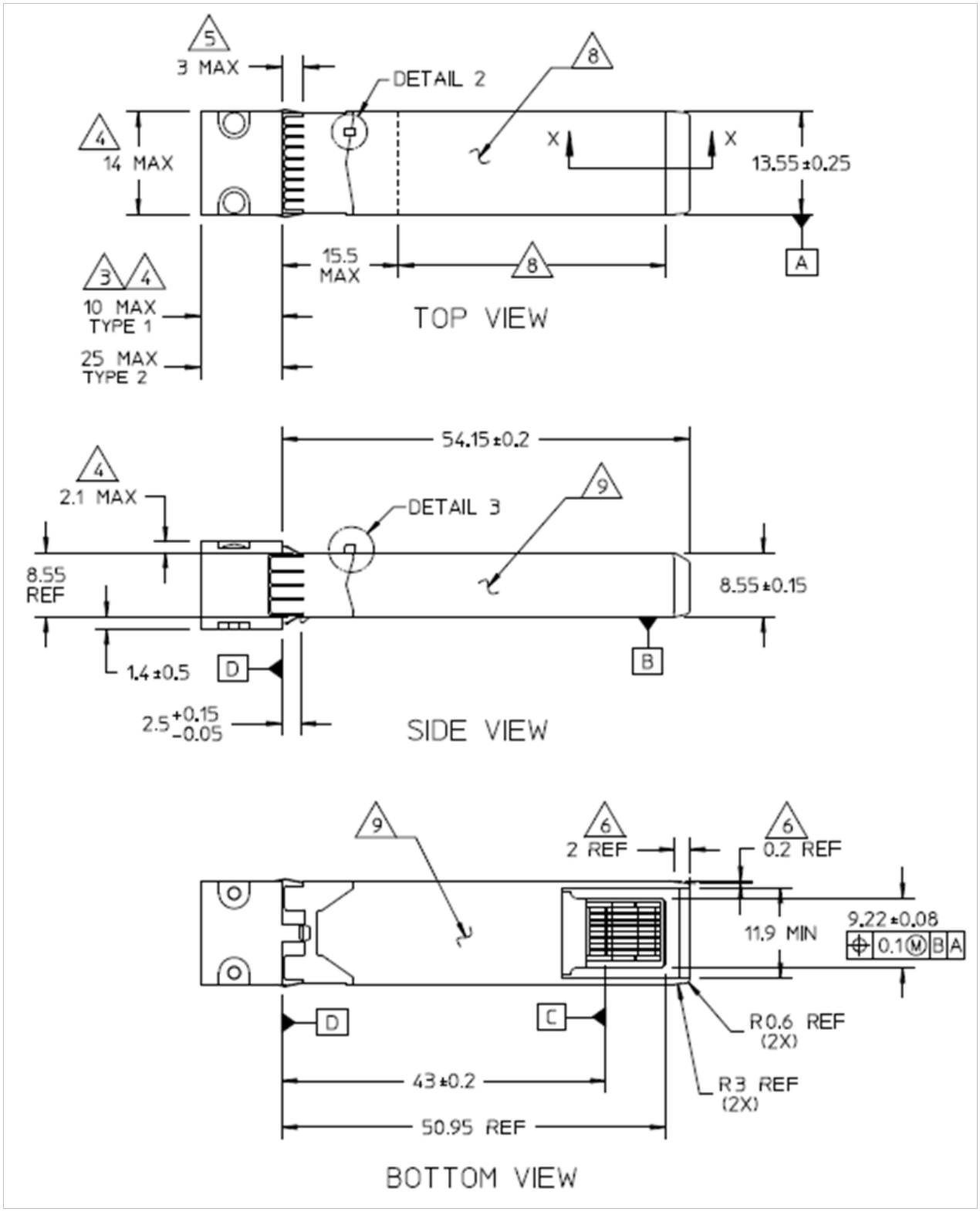
5. DIMENSIONS DEFINES EMI SPRING CONTACT POINT WITH MODULE CAGE.

6. LEAD-IN CHAMFER DIMENSION MEASURED FROM TSC (THEORETICAL SHARP CORNER).

7. BLOCKING RIB FEATURE TO PREVENT SFP-DD MODULE FROM MATING INTO LEGACY SFP CONNECTOR.

8. FLATNESS SPECIFICATION APPLIES OVER THE ENTIRE HEAT SINK AREA. REFER TO SECTION 5.4 TABLE 7 FOR FLATNESS REQUIREMENTS.

9. PRODUCT LABEL ON BOTTOM AND/OR SIDES TO BE FLUSHED OR RECESSED BELOW EXTERNAL SURFACES. LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMC PROPERTIES.


5
3 MAX
DETAIL 2
8
4
14 MAX
X
X
13.55±0.25
15.5
MAX
8
A
3 4
10 MAX
TYPE 1
25 MAX
TYPE 2
TOP VIEW
54.15±0.2
4
2.1 MAX
DETAIL 3
9
8.55
REF
8.55±0.15
1.4±0.5
D
B
2.5 +0.15 -0.05
SIDE VIEW
9
6
2 REF
6
0.2 REF
11.9 MIN
9.22±0.08
0.1 M B A
D
C
R0.6 REF
(2X)
43±0.2
R3 REF
(2X)
50.95 REF
BOTTOM VIEW

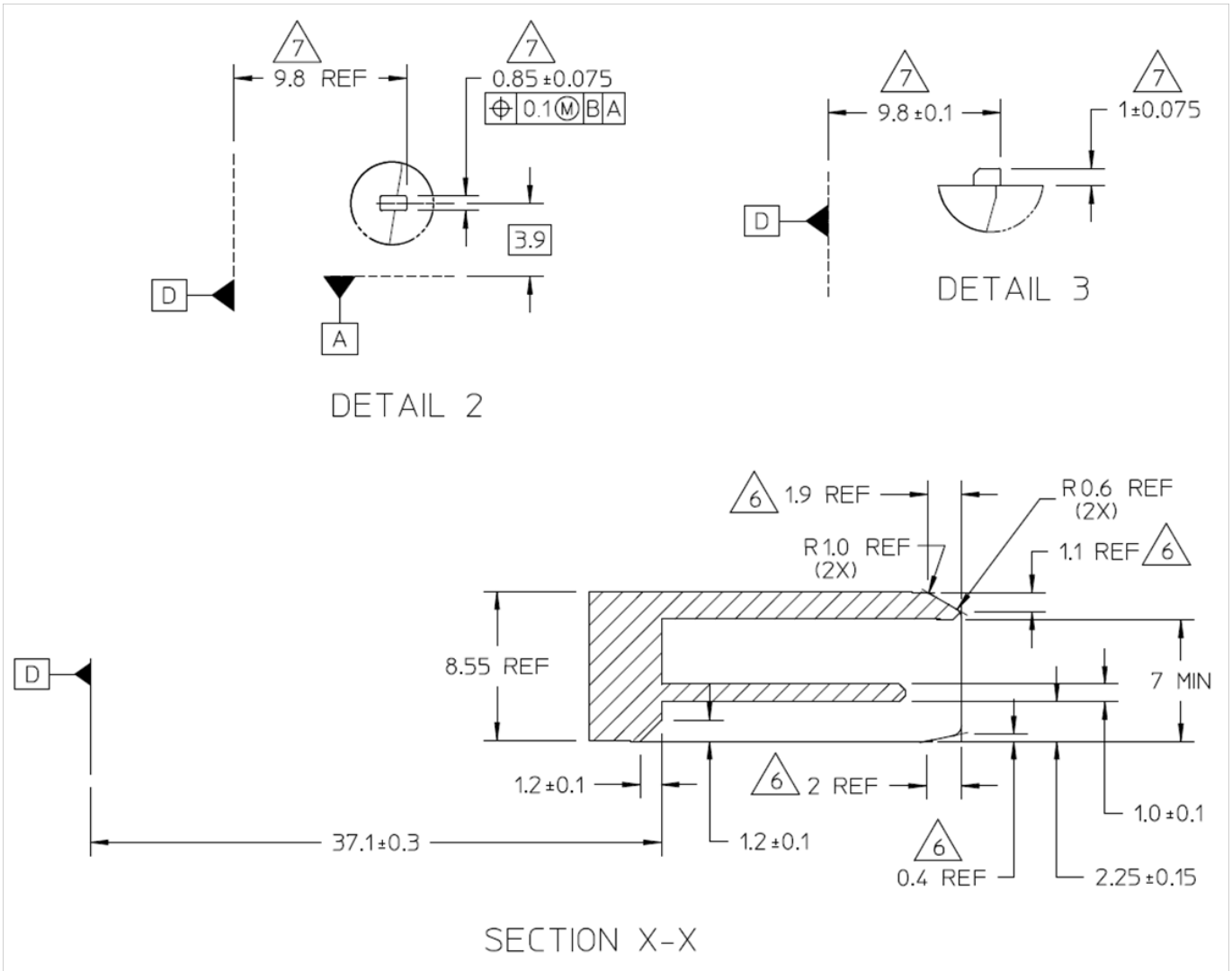



**Figure 13: Detailed dimensions of module**

## 5.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 13.
Specifications for Module flatness and surface roughness are shown in Table 7.

**Table 7- Module flatness specifications**

| Power Class | Module Flatness (mm) | Surface Roughness (Ra,µm) |
|---|---|---|
| 1 | 0.075 | 1.6 |
| 2 | 0.075 | 1.6 |
| 3 | 0.075 | 1.6 |
| 4 | 0.075 | 1.6 |
| 5 | 0.050 | 0.8 |
| 6 | reserved | reserved |
| 7 | reserved | reserved |
| 8 | 0.050 | 0.8 |

## 5.5 Module paddle card dimensions

NOTES APPLY TO MODULE PADDLE CARD :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD

5 DATUM C IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTER MOST SIGNAL CONTACTS PADS TO BE RE-ESTABLISHED ON EACH SIDE

6 DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS

7 DIMENSION AND TOLERANCE APPLIES TO ALL PADS ON BOTH TOP AND BOTTOM SIDE OF THE PADDLE CARD

8 A ZERO GAP IS ALLOWED FOR A CONTINUOUS PAD OPTION

9 APPLIES TO ALL SIGNAL PAD TO PRE-WIPE PAD SPACING

10 PRE-WIPE PADS (SHADED AREA) ON MODULE CARD HOST SIDE ARE OPTIONAL

11 PRE-WIPE PADS (UNSHADED AREA) ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND PAD DESIGNS

12 PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE

13 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS

14 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS

15 COMPONENT KEEP OUT AREA MEASURED FROM DATUM C

16 A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED, THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OF 0.13 ± 0.05

17. PRE-WIPE PADS ENSURE ADEQUATE WIPE REQUIRED TO PROVIDE A RELIABLE ELECTRICAL INTERCONNECT WHILE MINIMIZING SIGNAL INTEGRITY STUB EFFECTS

18. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1.27 MICROMETERS MINIMUM NICKEL

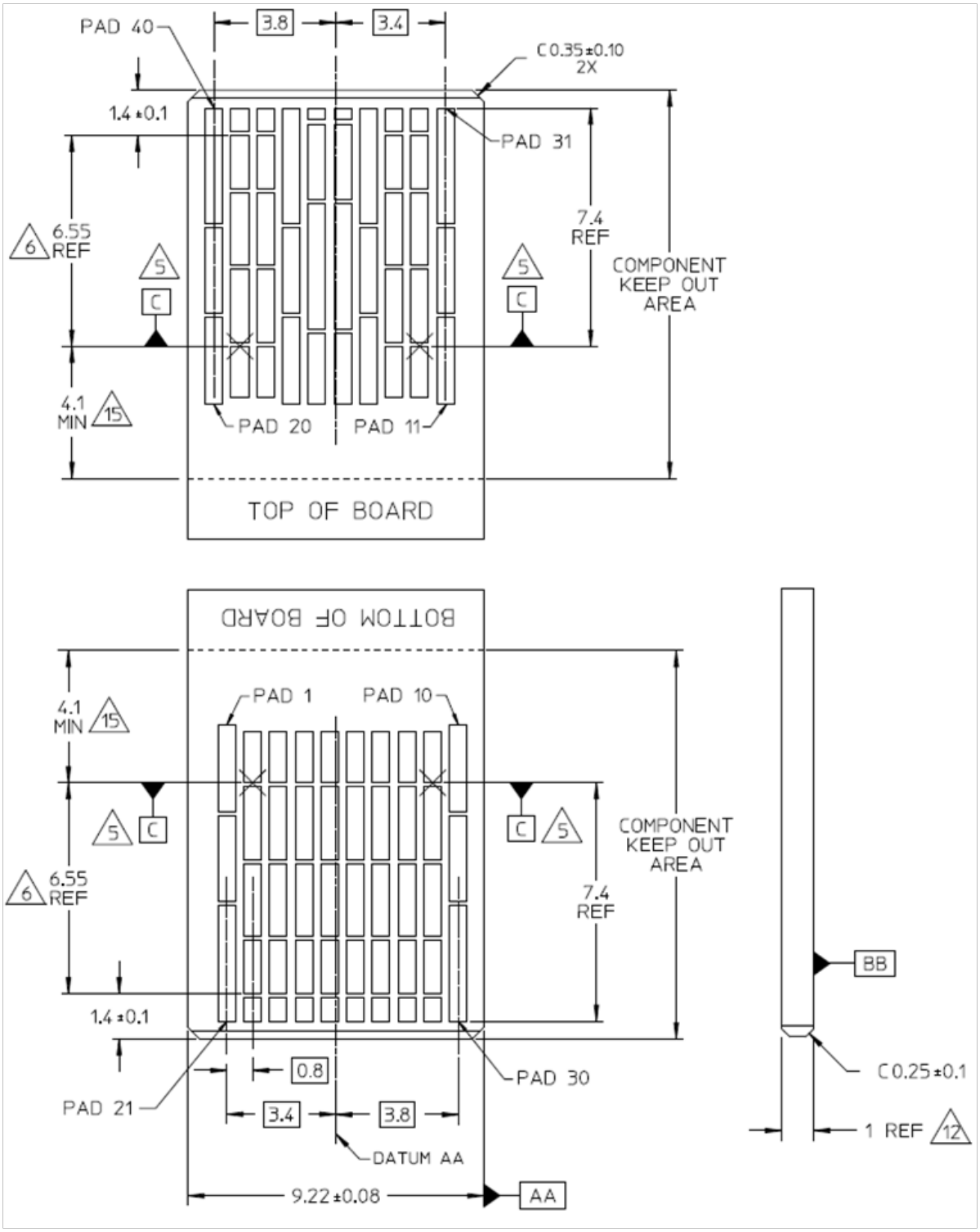



**Figure 14: Module paddle card dimensions**

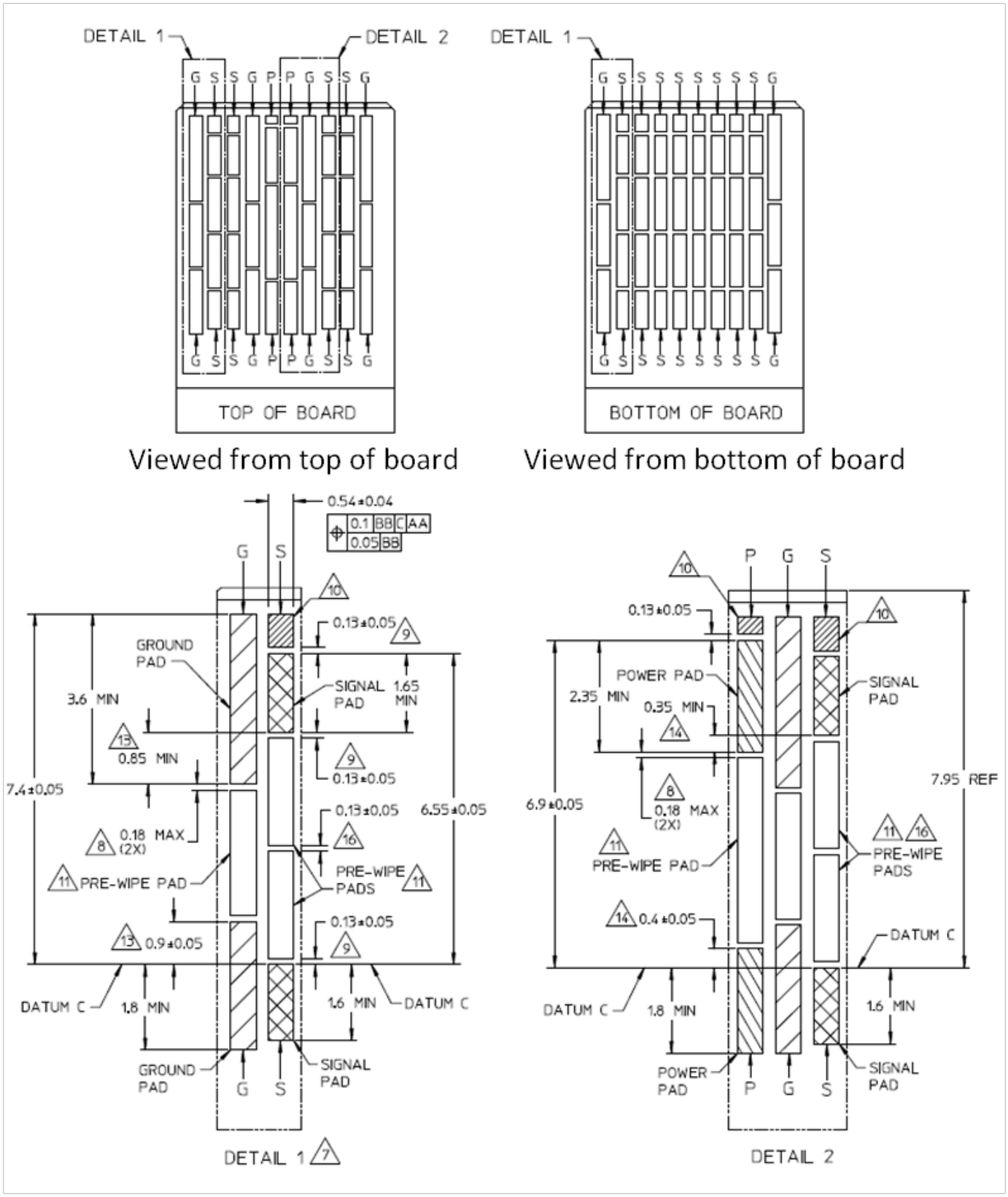



**Figure 15: Module pad dimensions**

## 5.6 Module Extraction and Retention Forces

**The requirements for insertion forces, extraction forces and retention forces are specified in Table 8. The SFP-DD cage and module are designed to ensure that excessive force applied to a cable does not damage the SFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. Examples of module retention mechanisms are found in SFF-8432 Figures 4-4 through 4-7. The contact pad plating shall meet the requirements of Section 5.5.**

**Table 8- Insertion, Extraction and Retention Forces**

| Measurement | Min | Max | Units | Comments |
|---|---|---|---|---|
| SFP module insertion | 0 | 18 | N | Condition: EIA-364-13<br>12.7mm/min Max cycle rate<br>Latch disengaged<br>Failure Criteria: Force not to exceed max stated value. No damage to module, cage or connector |
| SFP-DD module insertion | 0 | 40 | N | |
| SFP module extraction | 0 | 12.5 | N | |
| SFP-DD module extraction | 0 | 30 | N | |
| SFP module retention | 90 | N/A | N | Condition: EIA-364-35<br>12.7mm/min Max cycle rate<br>Latch engaged<br>Failure Criteria: Force without separation must be greater than the min stated value. No damage to module, cage or connector |
| SFP-DD module retention | 90 | N/A | N | |
| Cage retention in Host Board | 100 | N/A | N | Condition: Pull cage in a direction perpendicular to the board at a rate of 25.4mm/min to the specified force.<br>Tested with module, module analog, or fixture mated to cage.<br>Failure Criteria: Cage shall not separate from the board. |
| Insertion / removal cycles, connector / cage | 100 | N/A | Cycles | Condition: EIA-364-09<br>12.7mm/min Max mating rate<br>Tested with multiple modules<br>Failure Criteria: EIA-364-23 LLCR-20mohms Max change from baseline, no physical damage to cage or connector |
| Insertion / removal cycles, SFP-DD module | 50 | N/A | Cycles | |
| Note: Insertion, Extraction and Retention forces are absolute values. (must comply with or without a riding heat sink) | | | | |

## 5.7 Press fit Cage Mechanical

The SFP-DD Cage is shown in Figure 16 with detailed drawings in Figure 17. Recommendations for the cage bezel opening are shown in Figure 19.

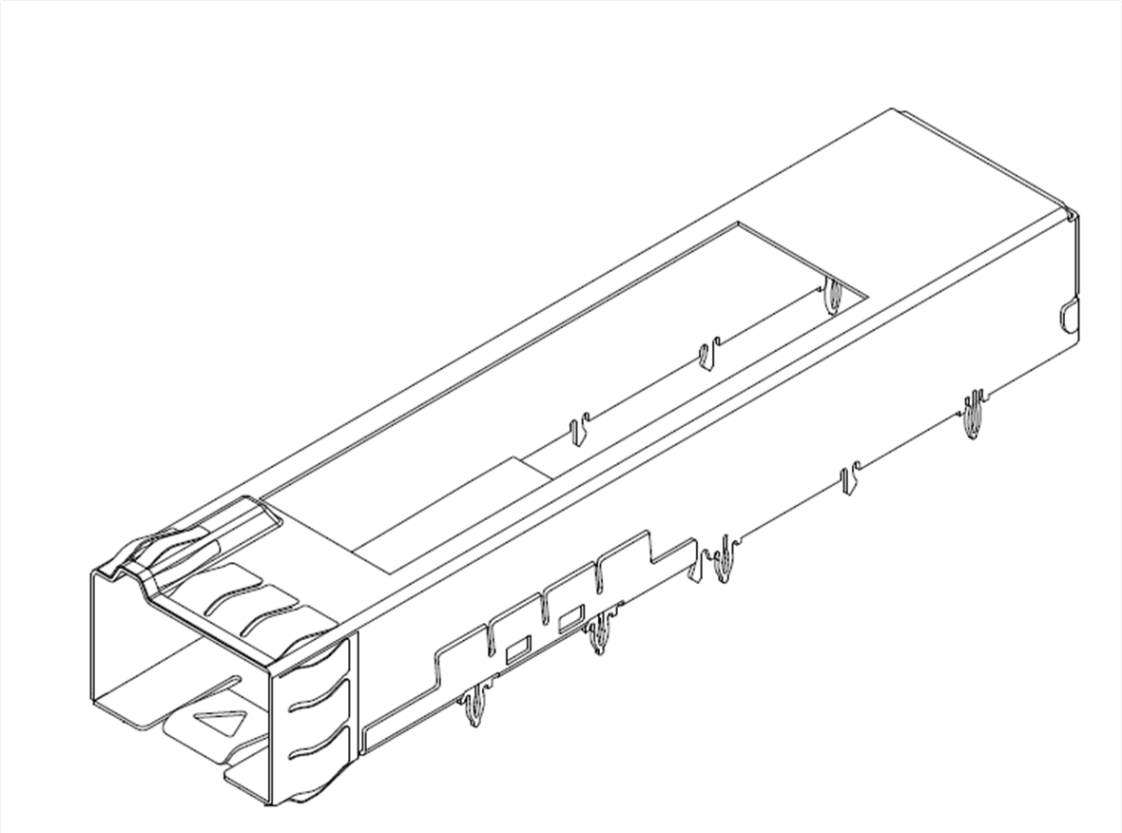


**Figure 16: Press Fit 1x1 Cage**

NOTES APPLY TO 1 X N CAGE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. DATUM S IS DEFINED BY THE SEATING SURFACE ON THE HOST BOARD

3. DIMENSIONS FROM INSIDE SURFACES OF CAGE

4. SIZE AND SHAPE OF CAGE PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

5. APPLIES TO 1.05 MM PCB HOLE DIAMETER

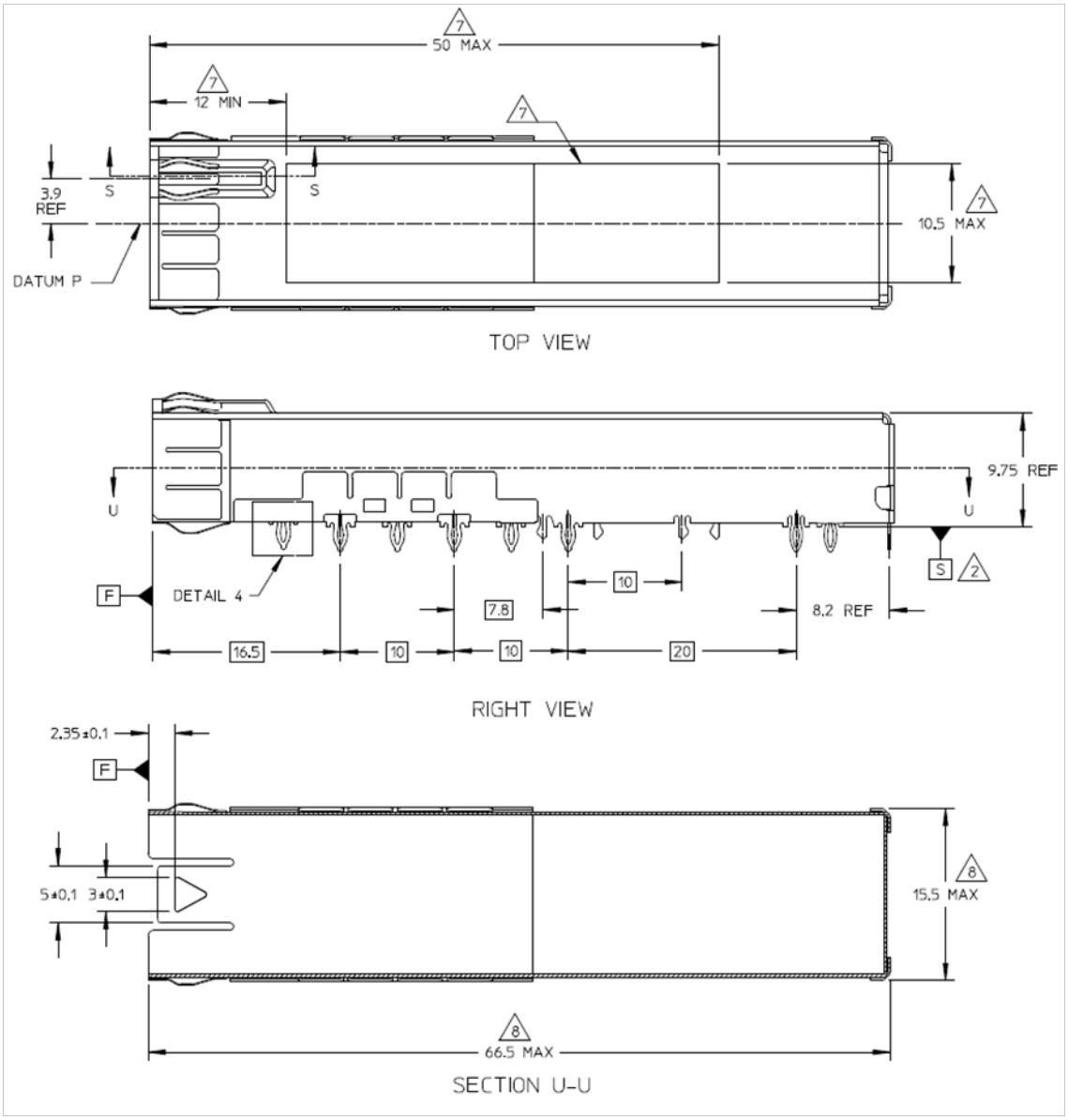
6. APPLIES TO 0.95 MM PCB HOLE DIAMETER

7. CUTOUT OPENING FOR HEAT SINK IS OPTIONAL

8. MAXIMUM ENVELOPE DIMENSION INCLUDES BACK COVER FOLDING TABS AND BOTTOM COVER ATTACHMENT FEATURES

9. APPLIES TO ALL RADAII SURFACES BETWEEN POINTS A AND B

10. APPLIES TO ALL FLAT SURFACES BETWEEN POINTS A AND B


7
50 MAX
7
12 MIN
7
3.9
REF
S
S
7
10.5 MAX
DATUM P
TOP VIEW
9.75 REF
U
U
S
2
F
DETAIL 4
10
7.8
8.2 REF
16.5
10
10
20
RIGHT VIEW
2.35±0.1
F
5±0.1
3±0.1
8
15.5 MAX
8
66.5 MAX
SECTION U-U

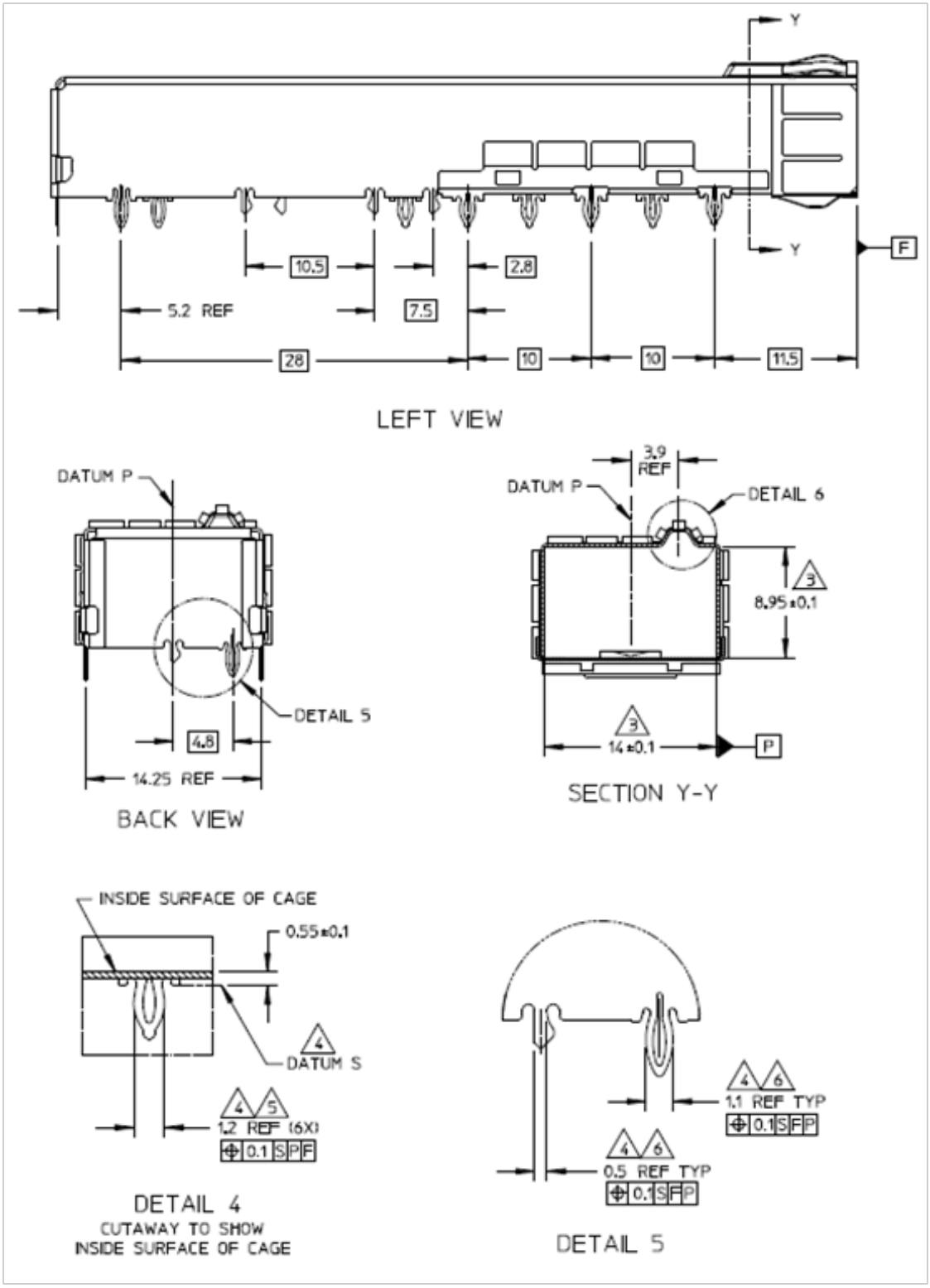



**Figure 17: Press Fit 1x1 Cage Design**

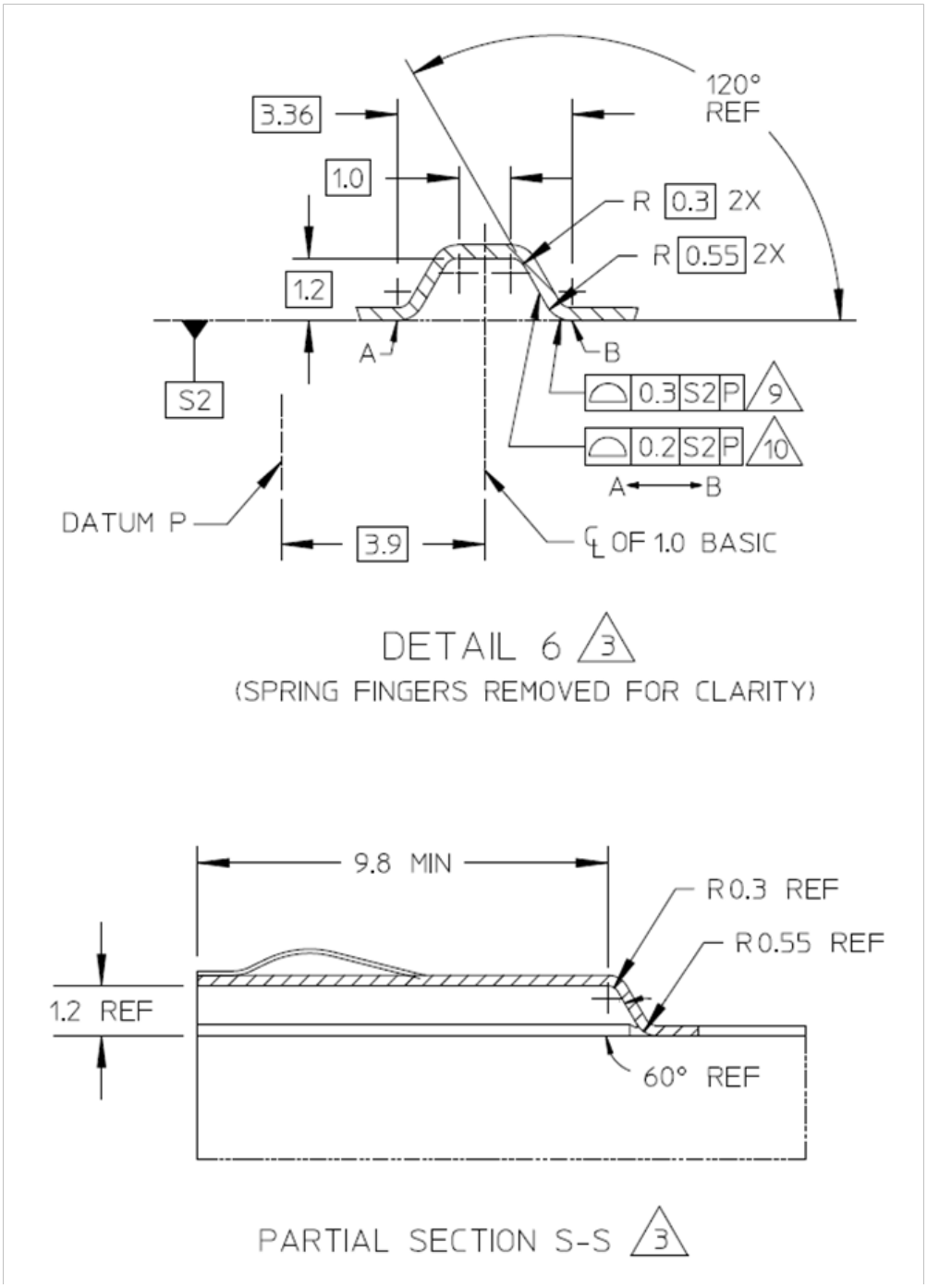



**Figure 18: Press Fit Cage Detail**

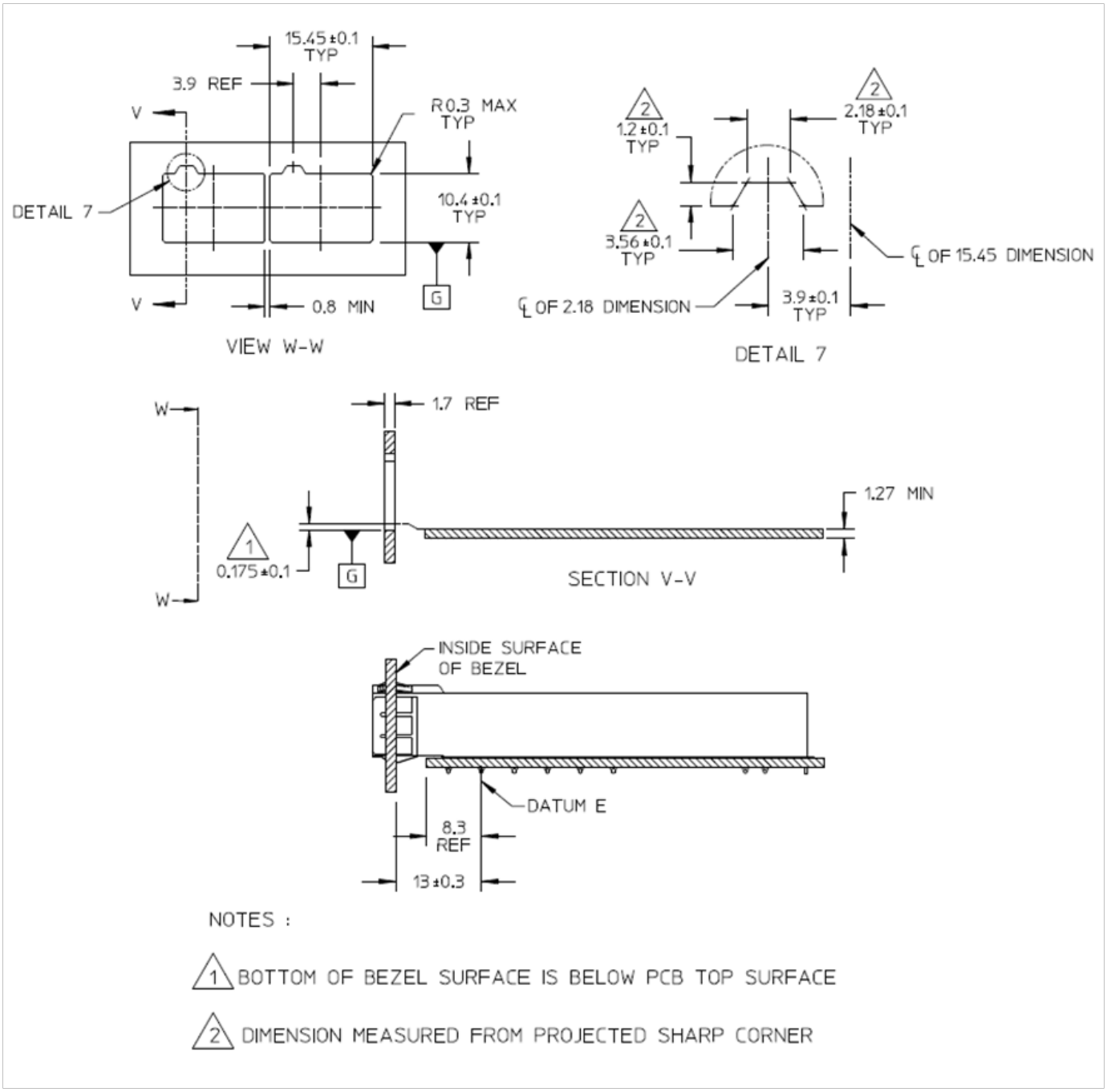



**Figure 19: 1 x n bezel opening**

## 5.8 SMT Electrical Connector Mechanical

The SFP-DD Connector is a 40-contact, right angle connector. The SMT connector is shown in Figure 20 with detailed drawings in Figure 21.

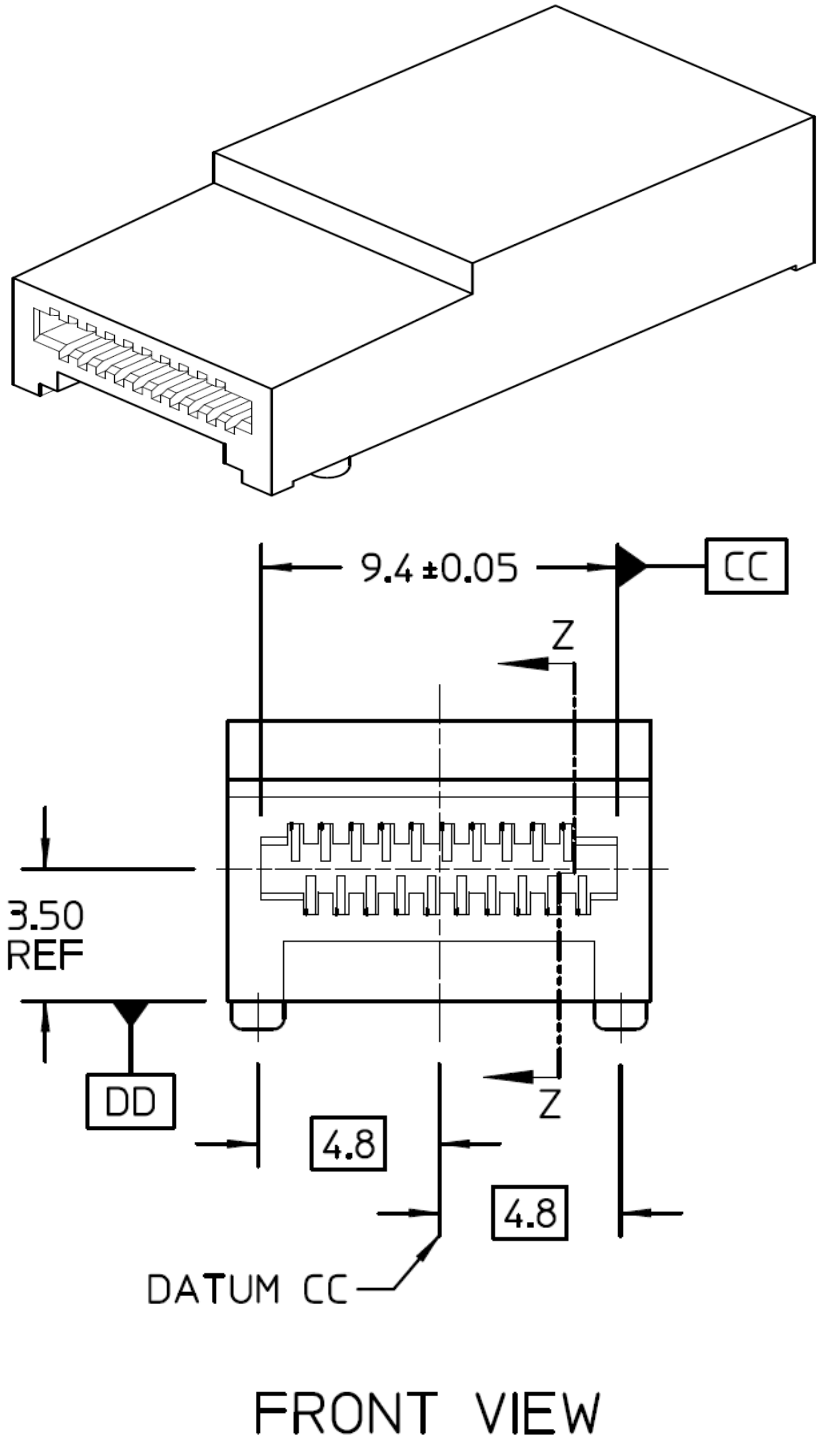
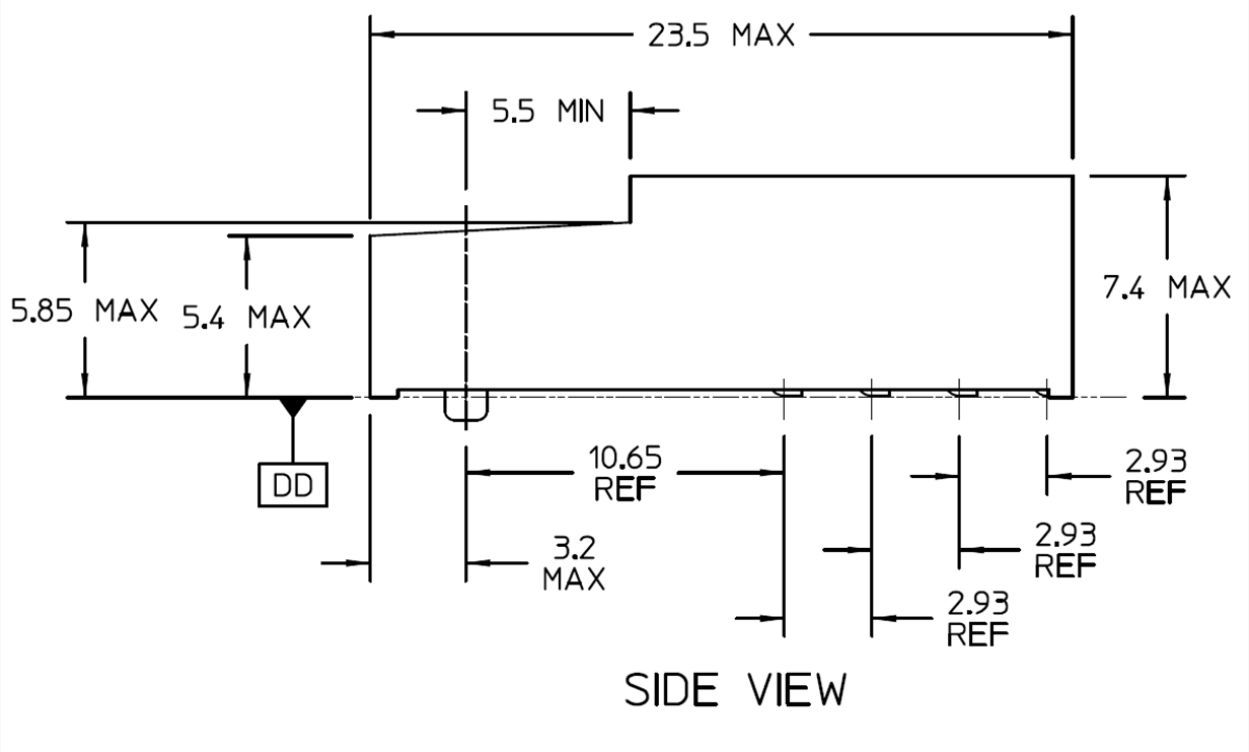
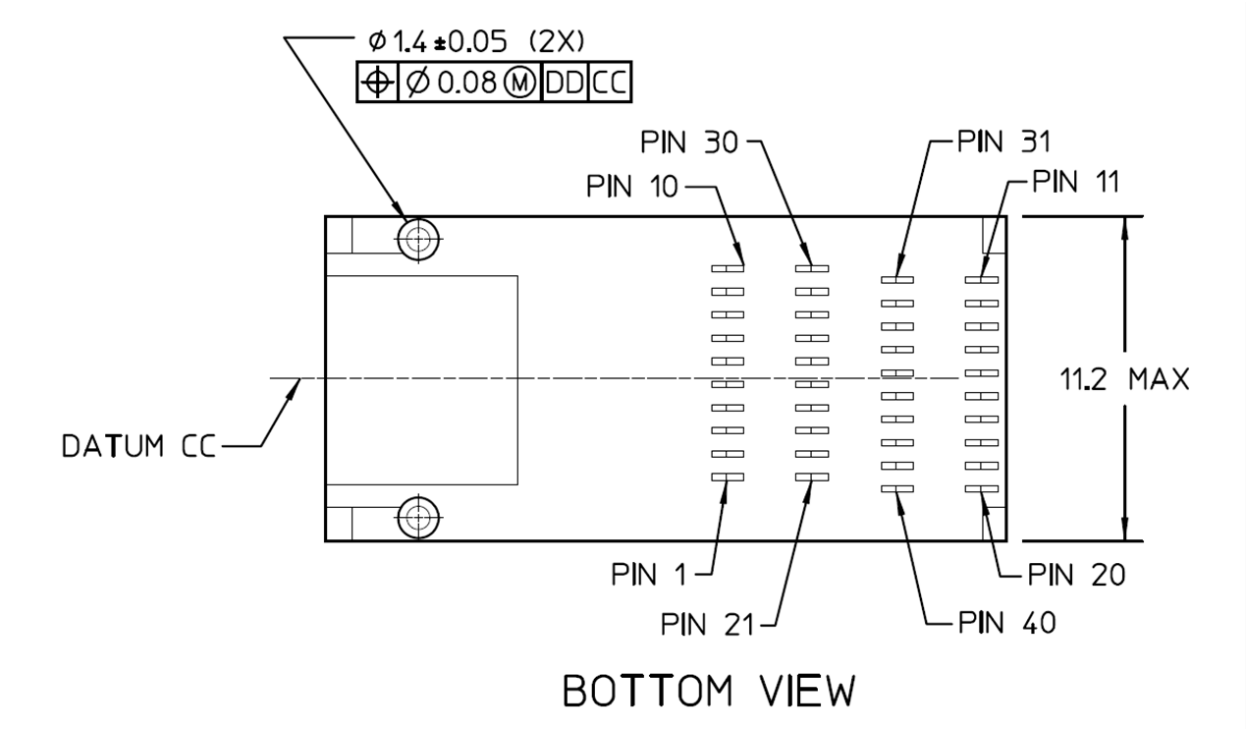



**Figure 20: SMT connector**


23.5 MAX
5.5 MIN
5.85 MAX
5.4 MAX
7.4 MAX
DD
10.65 REF
3.2 MAX
2.93 REF
2.93 REF
2.93 REF
SIDE VIEW


Ø1.4 ±0.05 (2X)
Ø 0.08 M DD CC
PIN 30
PIN 31
PIN 10
PIN 11
11.2 MAX
DATUM CC
PIN 1
PIN 20
PIN 21
PIN 40
BOTTOM VIEW

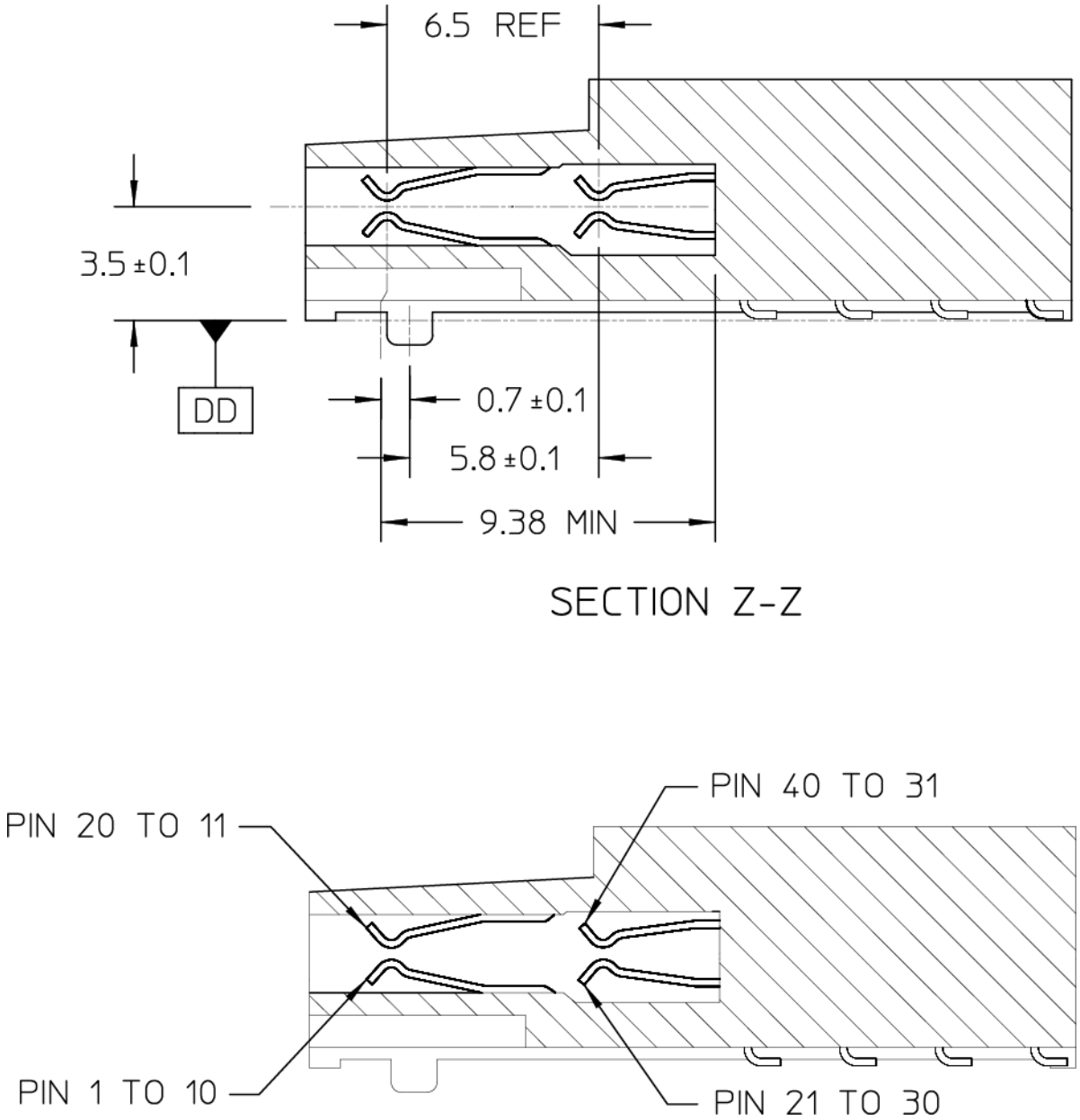
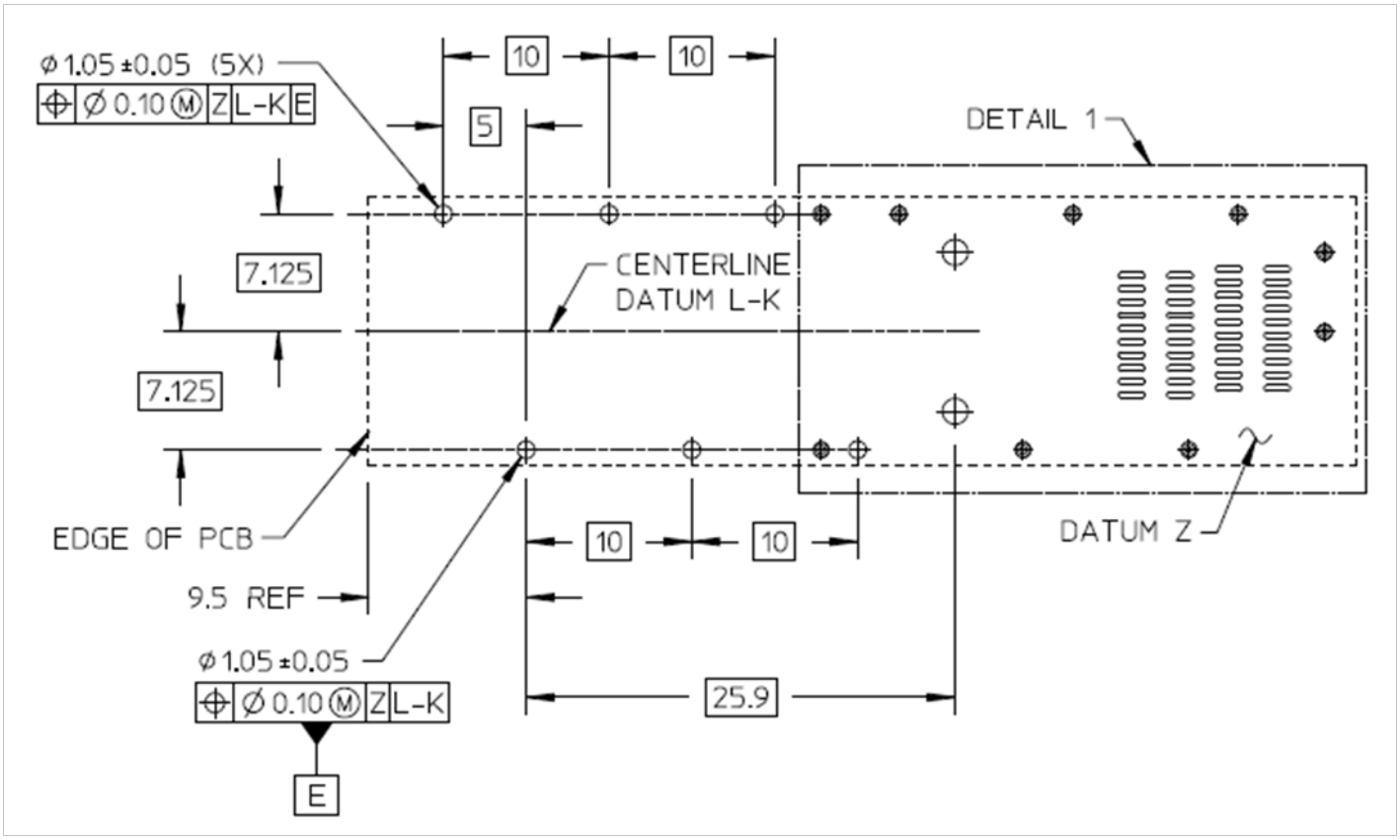


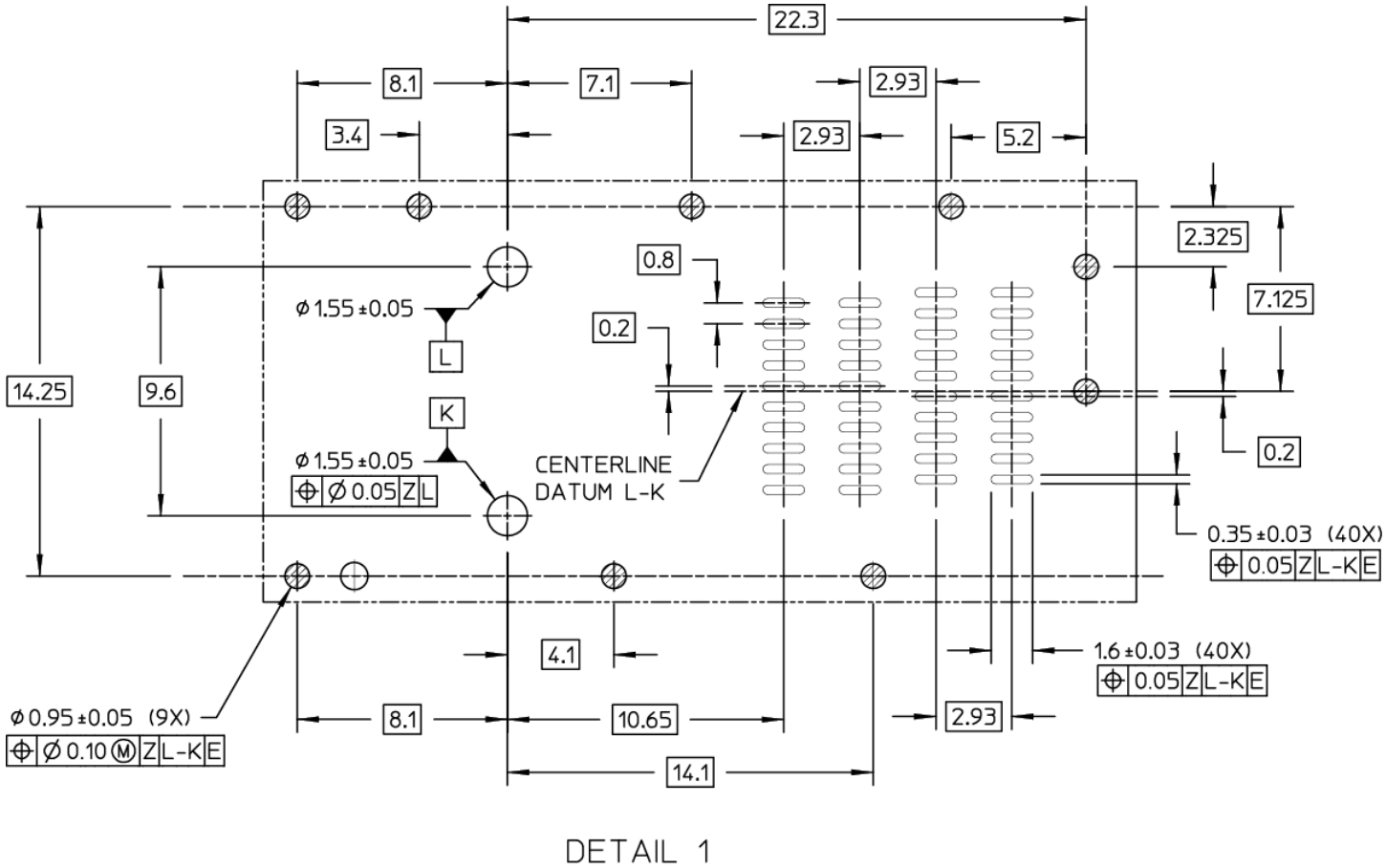

**Figure 21: 1x1 Connector Design and Host PCB Pin Numbers**

### 5.8.1 SMT connector and cage host PCB layout

A typical host board mechanical layout for attaching the SFP-DD SMT Connector and press fit Cage System is shown in Figure 22. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.






DETAIL 1

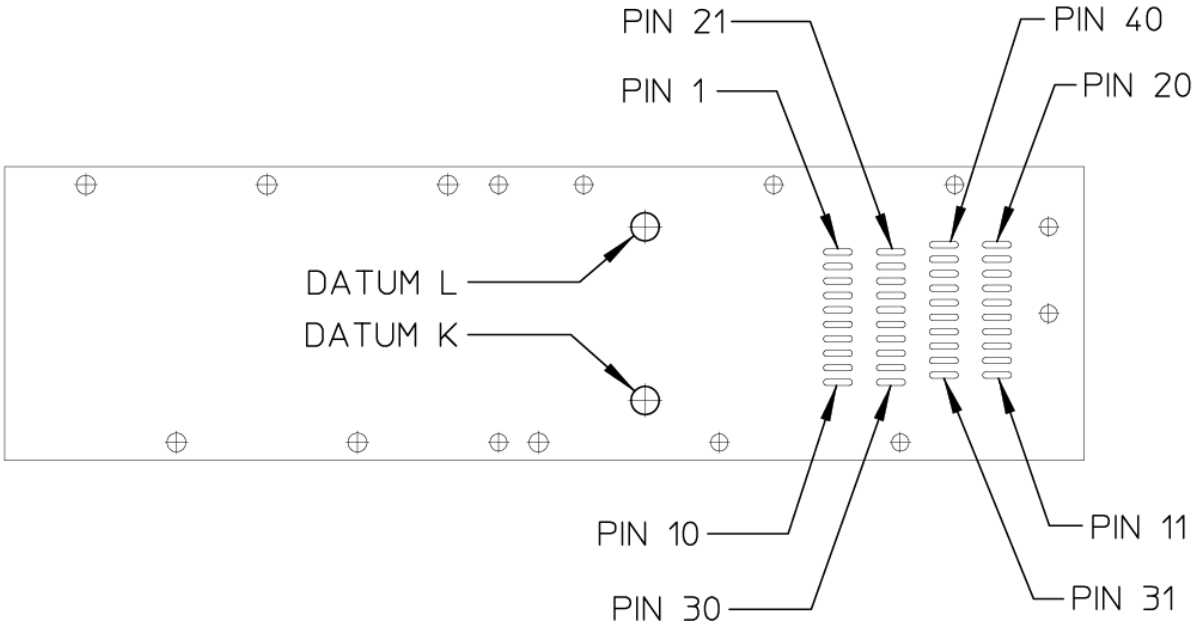



**Figure 22: Host PCB Mechanical Layout**

## 5.9 Module Color Coding and Labeling

If provided, color coding shall be on an exposed feature of the SFP-DD module (a feature or surface extending outside of the bezel). Color code are outside the scope of this specification.

Each SFP-DD module shall be clearly labeled. The complete labeling need not be visible when the SFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

## 5.10 Optical Interface

Four examples of the SFP-DD optical interface port are a male MPO receptacle (see Figure 24), a dual LC (see Figure 25), a SN receptacle (see Figure 26), or a MDC receptacle (see Figure 27). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 23.

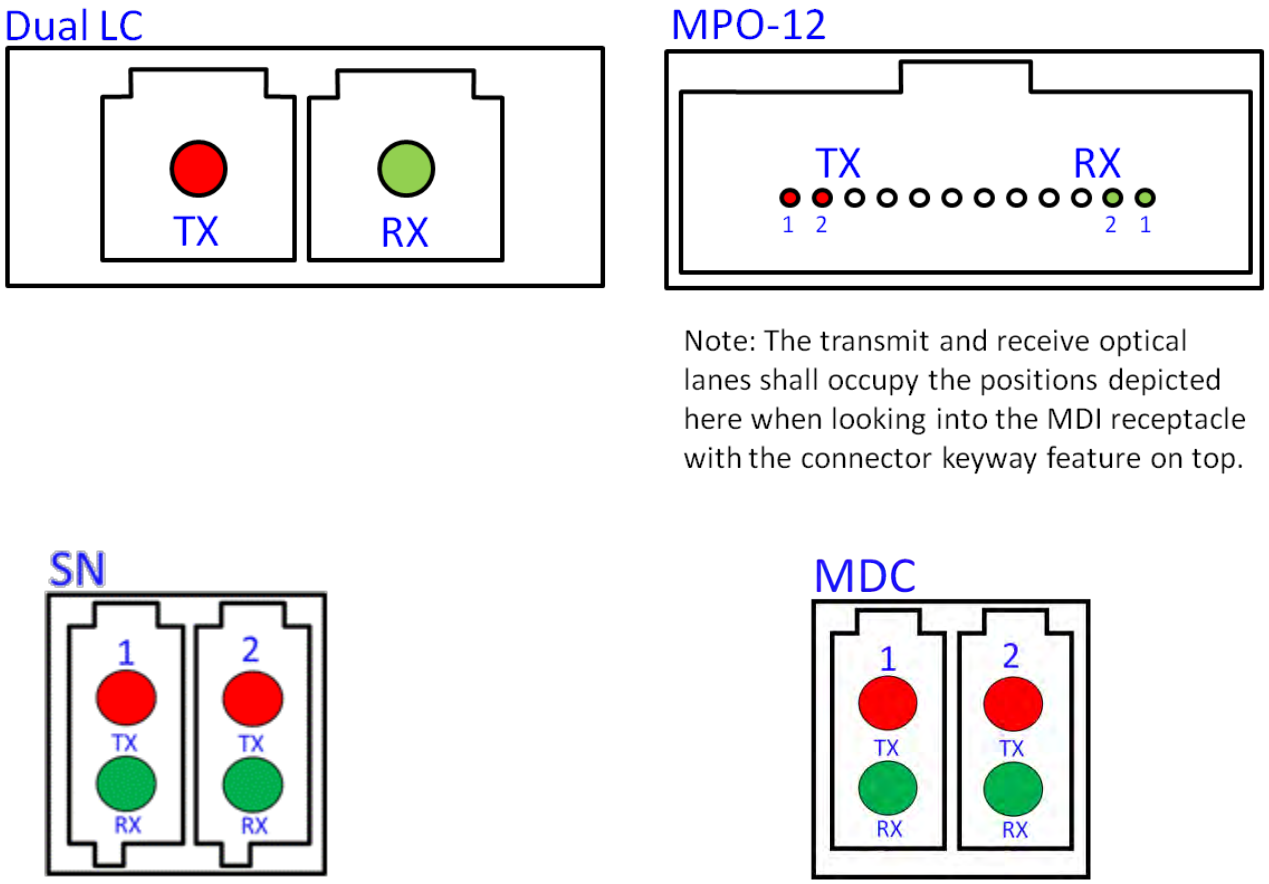



**Figure 23: Optical Media Dependent Interface port assignments**

### 5.10.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5, IEC 61754-7 and shown in Figure 24 (MPO-12). Note: Two alignment pins are present in each receptacle.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

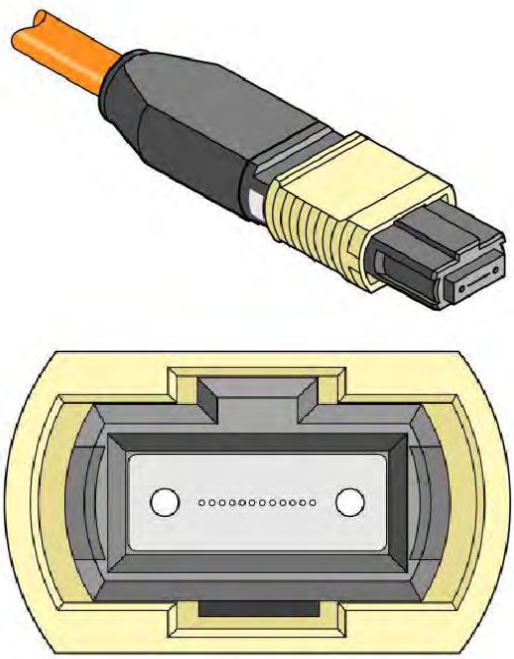


**Figure 24: MPO-12 Single Row optical patch cord and module receptacle**

### 5.10.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10, IEC 61754-20 and shown in Figure 25.

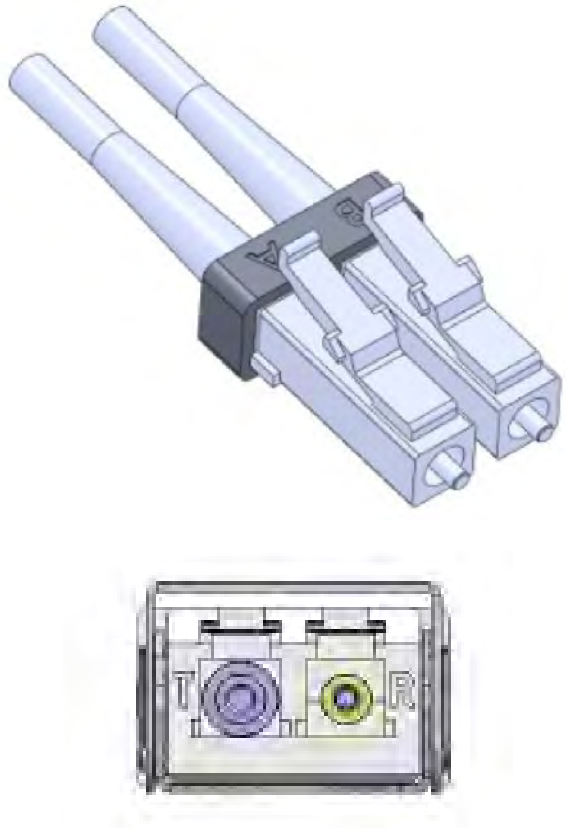



**Figure 25: Dual LC optical patchcord and module receptacle**

### 5.10.3 SN Optical Cable connections

The SN optical connector and receptacle for SFP-DD module is specified in SN-60092019 and shown in Figure 26. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

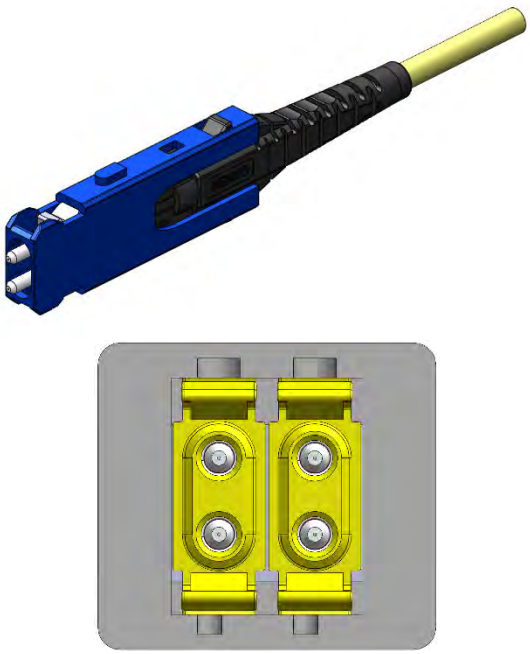


**Figure 26: SN optical connector plug and two-port module receptacle**

### 5.10.4 MDC Optical Cable connections

The MDC optical plug and receptacle for a SFP-DD module is specified in USC-11383001 and shown in Figure 27. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

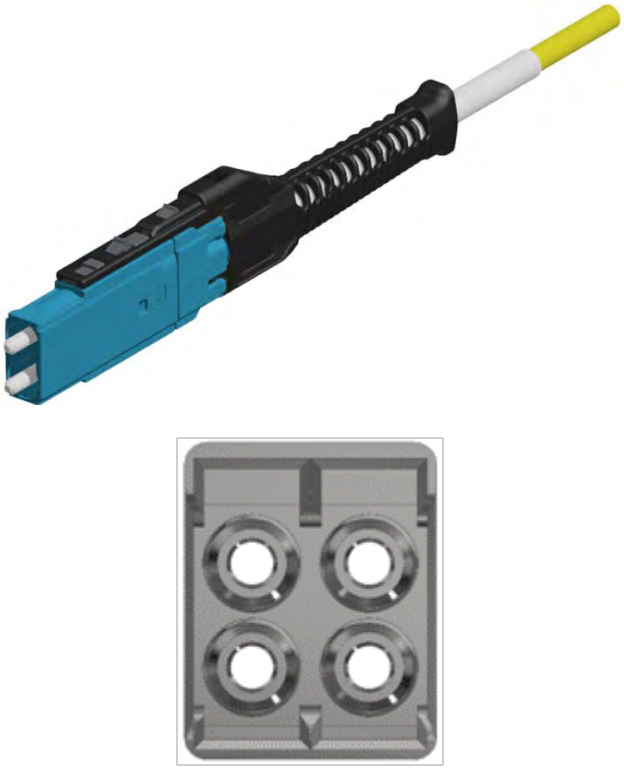


**Figure 27: MDC optical connector plug and two-port module receptacle**

### 5.10.5 Electrical data input/output to optical port mapping

Table 9 defines the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

**Table 9- Electrical data input to Optical Port Mapping**

| Electrical Data Input Reference | LC, SN, MDC | SN, MDC, MPO-12 |
|---|---|---|
| | 1 TX fiber | 2 TX fibers |
| TD0+/- | TX-1 | TX-1 |
| TD1+/- | | TX-2 |

# 6 Environmental and Thermal

## 6.1 Thermal Requirements

The SFP-DD module shall operate within one or more of the case temperatures ranges defined in Table 10. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

**Table 10- Temperature Range Class of operation**

| **Class** | **Case Temperature Range** |
|---|---|
| Standard | 0°C through 70°C |
| Extended | -5°C through 85°C |
| Industrial | -40°C through 85°C |

SFP-DD is designed to allow for up to 48 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

# 7 Management Interface Timing

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is required in order to enable flexible use of the module by the user. (See SFP-DD Management Interface Specification) Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the SFP-DD memory map rather than the SFP memory map. When a legacy SFP28 module is inserted into a SFP-DD port the legacy SFP memory map (i.e. SFF-8472) must be used. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

## 7.1 SCL and SDA Timing Specification

### 7.1.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in SFF-8419 Subsection 5.2.

### 7.1.2 Management Interface Timing Specification

The timing requirements are shown in Figure 28 and specified in Table 11.
SFP-DD is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This subsection closely follows the QSFP SFF-8636 specification.

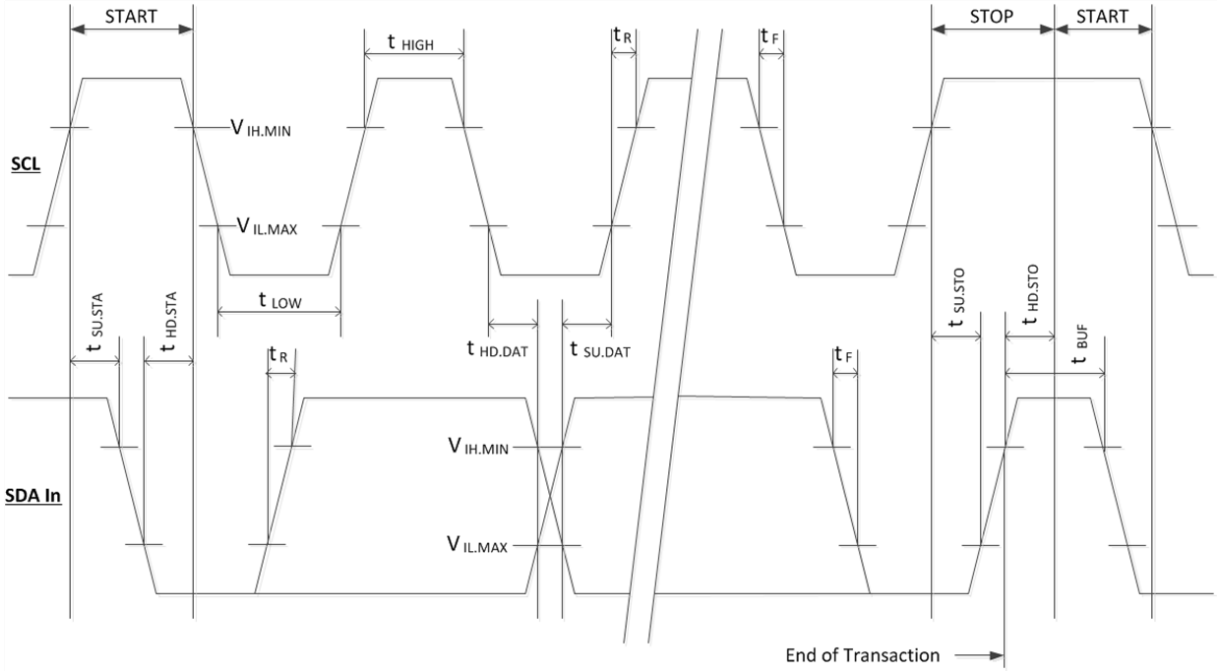



**Figure 28: SFP-DD Two Wire Interface Timing**

## 7.2 Serial Interface Protocol

### 7.2.1 Management Timing Parameters

The timing parameters for the 2-Wire interface to the SFP-DD module and the SFP-DD memory transaction timings are shown in Table 11. Tradeoffs between Pull up resistor values, bus capacitance and rise time are shown in Figure 29.

**Table 11- Management Interface timing parameters**

| | | Fast Mode (400 KHz) | | Fast Mode Plus (1 MHz) | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Unit | Conditions |
| Clock Frequency | fSCL | 0 | 400 | 0 | 1000 | KHz | |
| Clock Pulse Width Low | tLOW | 1.3 | | 0.50 | | µs | |
| Clock Pulse Width High | tHIGH | 0.6 | | 0.26 | | µs | |
| Time bus free before new transmission can start | tBUF | 20 | | 1 | | µs | Between STOP and START and between ACK and ReStart |
| START Hold Time | tHD.STA | 0.6 | | 0.26 | | µs | The delay required between SDA becoming low and SCL starting to go low in a START |
| START Setup Time | tSU.STA | 0.6 | | 0.26 | | µs | The delay required between SCL becoming high and SDA starting to go low in a START |
| Data In Hold Time | tHD.DAT | 0 | | 0 | | µs | |
| Data In Setup Time | tSU.DAT | 0.1 | | 0.1 | | µs | |
| Input Rise Time (400kHz) | tR.400 | | 300 | | 120 | ns | From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc) |
| Input Fall Time (400kHz) | tF.400 | | 300 | | 120 | ns | From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc) |
| STOP Setup Time | tSU.STO | 0.6 | | 0.6 | | µs | |
| STOP Hold Time | tHD.STO | 0.6 | | 0.26 | | us | |
| Aborted sequence – bus release | Deselect _Abort | 2 | | 2 | | ms | Delay from a host de-asserting Mod_ABS (at any point in a bus sequence) to the SFP-DD module releasing SCL and SDA |
| Serial Interface Clock Holdoff “Clock Stretching” | T_clock_hold | | 500 | | 500 | us | Maximum time the SFP-DD module may hold the SCL line low before continuing with a read or write operation. |
| Complete Single or Sequential Write | tWR | | 40 | | 40 | ms | Complete (up to) 4 Byte Write |
| Endurance (Write Cycles) | | 50K | | | 50k | cycles | Module Case Temperature = $70^0$ C |

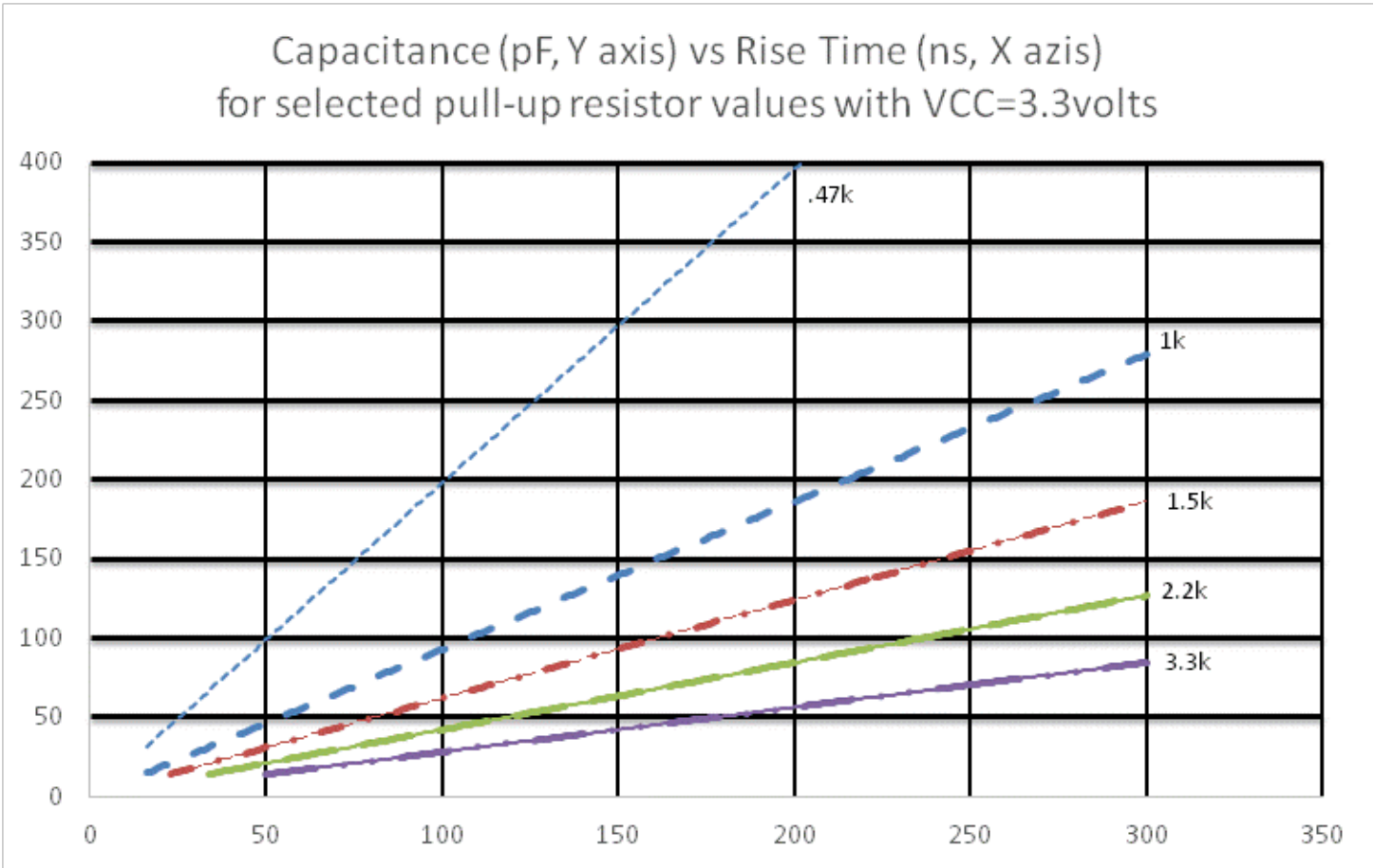



**Figure 29: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times**

## 7.3 Timing for Soft Control and Status Functions

Timing for SFP-DD soft control and status functions are described in Table 12.

**Table 12- Timing for SFP-DD soft control and status functions**

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| ResetL Assert Time | t_reset_init | 10 | | µs | Minimum pulse time on the ResetL signal to initiate a module reset. |
| TxFault Assert Time | ton_Int | | 200 | ms | Time from occurrence of condition triggering TxFault until Vout:TxFault=Voh |
| TxFault Deassert Time | toff_Int | | 500 | µs | Time from clear on read[3] operation of associated flag until Vout:Int=Vol. This includes deassert times for Rx LOS, TxFault and other flag bits. |
| Note 1. Measured from the rising edge of SDA in the stop bit of the write transaction | | | | | |
| Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 5. | | | | | |
| Note 3. Measured from the rising edge of SDA in the stop bit of the read transaction | | | | | |

# End of Document