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EXHIBIT B

https://web.archive.org/web/20170306001105/http://www.ti.com/lit/ds/symlink/ds125df1610.pdf

DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer

1 Features

- Pin-Compatible Family
  - DS150DF1610: 12.5 to 15 G
  - DS125DF1610: 9.8 to 12.5 G
  - DS110DF1610: 8.5 to 11.3 G
- 4x4 Analog Cross Point Switch for Each Quad
- Fully Adaptive CTLE
- Self tuning DFE, with Optional Continuous Adaption
- Configurable VGA
- Adjustable Transmit V_{OD}
- Adjustable 3-tap Transmit FIR Filter
- On-chip AC Coupling on Receive Inputs
- Locks to Half/Quarter/Eighth Data Rates for Legacy Support
- On-chip Eye Monitor(EOM), PRBS Checker, Pattern Generator
- Supports JTAG Boundary Scan
- Programmable Output Polarity Inversion
- Input Signal Detection, CDR Lock Detection
- Single 2.5 V ±5% Power Supply
- SMBus Based Register Configuration
- Optional EEPROM Configuration
- 15 mm × 15 mm, 196-pin FCBGA Package
- Operating Temp Range : –40°C to +85°C

2 Applications

- SFF-8431
- CPRI
- 10G/40G Ethernet
- Backplanes

3 Description

The DS125DF1610 is a sixteen-channel multi-rate retimer with integrated signal conditioning features. The device includes a fully adaptive Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), clock and data recovery (CDR), and a transmit FIR filter to enhance the reach and robustness over long, lossy, crosstalk impaired high speed serial links to achieve BER < 1×10^{-15}.

Each channel of the DS125DF1610 independently locks to serial data at 9.8 to 12.5 Gbps and the divide by 2, 4 and 8 sub-multiples. A simple external oscillator (±100ppm) that is synchronous or asynchronous with the incoming data stream is used as a reference clock. Integrated 4x4 cross point switches allow for full non-blocking routing or broadcasting within each quad of the DS125DF1610.

Programmable transmit FIR filter offers control of the pre-cursor, main tap and post-cursor for transmit equalization. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnects and backplanes with multiple connectors.

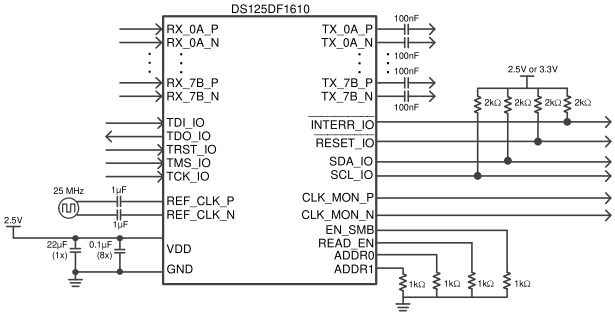
A non-disruptive mission mode eye-monitor feature allows link monitoring internal to the receiver. The built-in PRBS generator and checker compliment the internal diagnostic features to complete standalone BERT measurements. Built-in JTAG enables manufacturing tests.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE NOM
DS125DF1610	FCBGA (196)	15.00 mm x 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 8
6.1 Absolute Maximum Ratings ... 8
6.2 Handling Ratings ... 8
6.3 Recommended Operating Conditions ... 8
6.4 Thermal Information ... 8
6.5 Additional Thermal Information ... 8
6.6 Electrical Characteristics ... 9
7 Detailed Description ... 13
7.1 Overview ... 13
7.2 Functional Block Diagram ... 13
7.3 Feature Description ... 14
7.4 Device Functional Modes ... 24
7.5 Programming ... 26
8 Applications and Implementation ... 69
8.1 Application Information ... 69
8.2 Typical Applications ... 70
8.3 Initialization Setup ... 73
9 Power Supply Recommendations ... 75
9.1 Power Supply Filtering ... 75
10 Layout ... 75
10.1 Layout Guidelines ... 75
10.2 Layout Example ... 76
11 Device and Documentation Support ... 77
11.1 Device Support ... 77
11.2 Documentation Support ... 77
11.3 Receiving Notification of Documentation Updates 77
11.4 Community Resources ... 77
11.5 Trademarks ... 77
11.6 Electrostatic Discharge Caution ... 77
11.7 Glossary ... 77
12 Mechanical, Packaging, and Orderable Information ... 77

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2015) to Revision B	Page
• Changed the minimum temperature from -20°C to -40°C	1
• Changed the minimum temperature from -20°C to -40°C	8

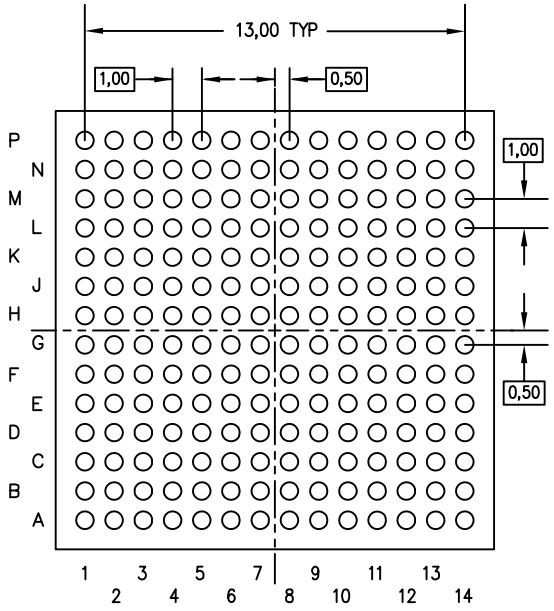
Changes from Original (April 2014) to Revision A	Page
• Added full datasheet	1

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5 Pin Configuration and Functions

Plastic Ball Grid Array
196 Balls
Bottom View



	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
01	TX_6B_N	TX_6B_P	GND	GND	TX_4B_N	TX_4B_P	GND	GND	TX_3A_N	TX_3A_P	GND	GND	TX_1A_N	TX_1A_P	01
02	GND	GND	TX_5B_N	TX_5B_P	GND	GND	TX_4A_N	TX_4A_P	GND	GND	TX_2A_N	TX_2A_P	GND	GND	02
03	TX_7A_N	TX_7A_P	GND	GND	TX_5A_N	TX_5A_P	GND	GND	TX_2B_N	TX_2B_P	GND	GND	TX_0B_N	TX_0B_P	03
04	GND	GND	TX_6A_N	TX_6A_P	GND	GND	TX_3B_N	TX_3B_P	GND	GND	TX_1B_N	TX_1B_P	GND	GND	04
05	TX_7B_N	TX_7B_P	GND	ALL_DONE	VDD	VDD	GND	READ_EN	VDD	VDD	ADDR1	GND	TX_0A_N	TX_0A_P	05
06	GND	GND	N/C	SCL_IO	VDD	GND	VDD	GND	VDD	GND	TCK_IO	N/C	ADDR0	GND	06
07	REF_CLK_P	N/C	SDA_IO	N/C	GND	VDD	GND	VDD	GND	VDD	TDI_IO	TDO_IO	TMS_IO	CLK_MON_P	07
08	REF_CLK_N	EN_SMB	INTERR#_IO	RESET#_IO	VDD	GND	VDD	GND	VDD	GND	N/C	TRST_IO	N/C	CLK_MON_N	08
09	GND	GND	N/C	N/C	GND	VDD	GND	VDD	GND	VDD	N/C	N/C	GND	GND	09
10	RX_7B_N	RX_7B_P	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	RX_0A_N	RX_0A_P	10
11	GND	GND	RX_6A_N	RX_6A_P	GND	GND	RX_3B_N	RX_3B_P	GND	GND	RX_1B_N	RX_1B_P	GND	GND	11
12	RX_7A_N	RX_7A_P	GND	GND	RX_5A_N	RX_5A_P	GND	GND	RX_2B_N	RX_2B_P	GND	GND	RX_0B_N	RX_0B_P	12
13	GND	GND	RX_5B_N	RX_5B_P	GND	GND	RX_4A_N	RX_4A_P	GND	GND	RX_2A_N	RX_2A_P	GND	GND	13
14	RX_6B_N	RX_6B_P	GND	GND	RX_4B_N	RX_4B_P	GND	GND	RX_3A_N	RX_3A_P	GND	GND	RX_1A_N	RX_1A_P	14
	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

(TOP VIEW)

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Pin Functions

DS110DF1610, DS125DF1610 PIN NAME	DS150DF1610 PIN NAME	PIN	I/O	DESCRIPTION
HIGH SPEED DIFFERENTIAL I/O				
RX_1A_P RX_1A_N	RX_0_0P RX_0_0N	A14 B14	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_0B_P Rx_0B_N	RX_0_1P RX_0_1N	A12 B12	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_0A_P RX_0A_N	RX_0_2P RX_0_2N	A10 B10	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_2A_P RX_2A_N	RX_0_3P RX_0_3N	C13 D13	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_1B_P RX_1B_N	RX_0_4P RX_0_4N	C11 D11	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_3A_P RX_3A_N	RX_0_5P RX_0_5N	E14 F14	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_2B_P RX_2B_N	RX_0_6P RX_0_6N	E12 F12	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_4A_P RX_4A_N	RX_0_7P RX_0_7N	G13 H13	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_3B_P RX_3B_N	RX_1_0P RX_1_0N	G11 H11	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_4B_P Rx_4B_N	RX_1_1P RX_1_1N	J14 K14	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_5A_P RX_5A_N	RX_1_2P RX_1_2N	J12 K12	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_5B_P RX_5B_N	RX_1_3P RX_1_3N	L13 M13	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_6A_P RX_6A_N	RX_1_4P RX_1_4N	L11 M11	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_6B_P RX_6B_N	RX_1_5P RX_1_5N	N14 P14	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_7A_P RX_7A_N	RX_1_6P RX_1_6N	N12 P12	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
RX_7B_P RX_7B_N	RX_1_7P RX_1_7N	N10 P10	I, CML	Inverting and non-inverting CML-compatible, AC coupled differential inputs. An on-chip 100 Ohm differential termination resistor connects these inputs.
TX_1A_P TX_1A_N	TX_0_0P TX_0_0N	A1 B1	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_0B_P TX_0B_N	TX_0_1P TX_0_1N	A3 B3	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_0A_P TX_0A_N	TX_0_2P TX_0_2N	A5 B5	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.

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Pin Functions (continued)

DS110DF1610, DS125DF1610 PIN NAME	DS150DF1610 PIN NAME	PIN	I/O	DESCRIPTION
TX_2A_P TX_2A_N	TX_0_3P TX_0_3N	C2 D2	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_1B_P TX_1B_N	TX_0_4P TX_0_4N	C4 D4	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_3A_P TX_3A_N	TX_0_5P TX_0_5N	E1 F1	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_2B_P TX_2B_N	TX_0_6P TX_0_6N	E3 F3	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_4A_P TX_4A_N	TX_0_7P TX_0_7N	G2 H2	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_3B_P TX_3B_N	TX_1_0P TX_1_0N	G4 H4	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_4B_P TX_4B_N	TX_1_1P TX_1_1N	J1 K1	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_5A_P TX_5A_N	TX_1_2P TX_1_2N	J3 K3	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_5B_P TX_5B_N	TX_1_3P TX_1_3N	L2 M2	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_6A_P TX_6A_N	TX_1_4P TX_1_4N	L4 M4	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_6B_P TX_6B_N	TX_1_5P TX_1_5N	N1 P1	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_7A_P TX_7A_N	TX_1_6P TX_1_6N	N3 P3	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
TX_7B_P TX_7B_N	TX_1_7P TX_1_7N	N5 P5	O, CML	Inverting and non-inverting CML-compatible differential outputs. Driver presents an output impedance of 100 ohms between these outputs when switching.
CLOCK PINS				
REF_CLK_P REF_CLK_N		P7 P8	I, LVDS/ LVCMOS	Inverting and non-inverting CML-compatible differential inputs for 25 MHz, 125 MHz, or 312.5 MHz clock. These differential signals are typically AC coupled with 1 µF capacitors When configured for single-ended input operation, apply LVCMOS ref clock to REF_CLK_P and float REF_CLK_N. Single-ended signals should be DC coupled.
CLK_MON_P CLK_MON_N		A7 A8	O, LVDS	Inverting and non-inverting CML-compatible differential outputs to monitor system differential clock. When daisy chaining to another retimer the output frequency should be set to 25 MHz.
SMBUS INTERFACE				
SDA_IO		M7	I/O, Open Drain	Data Input / Open Drain Output External pull-up resistor is required, typically in the 2kΩ to 5kΩ range. Pull-up value should be selected according to system implementation. Pin is 3.3 V LVCMOS tolerant.

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Pin Functions (continued)

DS110DF1610, DS125DF1610 PIN NAME	DS150DF1610 PIN NAME	PIN	I/O	DESCRIPTION
SCL_IO		L6	I/O, Open Drain	Clock input/output External pull-up resistor is required, typically in the 2kΩ to 5kΩ range. Pull-up value should be selected according to system implementation. Pin is 3.3 V LVCMOS tolerant EEPROM configuration (SMBus Master mode)
JTAG INTERFACE(1)				
TMS_IO		B7	I, LVCMOS	JTAG Test Mode Select, internal pull-up
TDO_IO		C7	O, LVCMOS	JTAG Test Data Out
TRST_IO		C8	I, LVCMOS	JTAG Test Reset, internal pull-up
TCK_IO		D6	I, LVCMOS	JTAG Test clock, internal pull-up
TDI_IO		D7	I, LVCMOS	JTAG Test Data Input, internal pull-up
OTHER PINS				
$\overline{\text{RESET\_IO}}$		L8	I, LVCMOS	Resets registers and state machines on rising edge. Pulse LOW for minimum of 10µs to perform reset. Pin should be pulled HIGH during power on.
$\overline{\text{INTERR\_IO}}$		M8	O, Open Drain	Active Low interrupt signal. Pin goes low when an interrupt event occurs. Interrupts must be enabled via SMBus.
ADDR0		B6	I, LVCMOS	4 level input strap pin for SMBus address code LSB. Standard LVCMOS output.
ADDR1		D5	I, LVCMOS	4 level input strap pin for SMBus address code MSB. Standard LVCMOS output.
READ_EN		G5	I, LVCMOS	Tie LOW for SMBus slave mode normal operation. Pin has internal pull down. In SMBus slave mode, tie HIGH to force SMBus address = 0x30.
ALL_DONE		L5	O, LVCMOS	EEPROM load status. Pin goes LOW when EEPROM load is complete.
EN_SMB		N8	I, LVCMOS	Connect to GND through ≤1kΩ resistor for SMBus slave operation. Connect to VDD through ≤1kΩ resistor for EEPROM configuration
POWER				
VDD		E5, E7, E9, E10, F5, F6, F8, F10, G7, G9, H6, H8, J5, J7, J9, J10, K5, K6, K8, K10	Power	VDD = 2.5 V +/- 5%

(1) Refer to the DS125DF1610 Programming Guide for additional information

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Pin Functions (continued)

DS110DF1610, DS125DF1610 PIN NAME	DS150DF1610 PIN NAME	PIN	I/O	DESCRIPTION
GND		A2, A4, A6, A9, A11, A13, B2, B4, B9, B11, B13, C1, C3, C5, C10, C12, C14, D1, D3, D10, D12, D14, E2, E4, E6, E8, E11, E13, F2, F4, F7, F9, F11, F13, G1, G3, G6, G8, G10, G12, G14, H1, H3, H5, H7, H9, H10, H12, H14, J2, J4, J6, J8, J11, J13, K2, K4, K7, K9, K11, K13, L1, L3, L10, L12, L14, M1, M3, M5, M10, M12, M14, N2, N4, N6, N9, N11, N13, P2, P4, P6, P9, P11, P13	Power	Ground reference
N/C		B8, C6, C9, D8, D9, L7, L9, M6, M9, N7		No Connect, leave floating

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6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (VDD)	–0.5	2.75	V
LVCMOS Input/Output Voltage	–0.5	2.75	V
Open Drain I/O Supply Voltage	–0.5	4.0	V
CML Input Voltage	–0.5	(VDD + 0.5)	V
CML Input Current	–30	30	mA
Storage temperature range, T_{stg}	-40	150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications

6.2 Handling Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4,000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1,000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply Voltage	2.375	2.5	2.625	V
Ambient Temperature	–40	25	85	°C
SMBus (SDA, SCL), INTERR_IO		2.5	3.6	V
Maximum Continuous Junction Temperature while Device is Operational			115	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		DS125DF1610 FCBGA ABB (196) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	18.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	5.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal model available upon request

6.5 Additional Thermal Information

BOARD	θ_{JC} (°C / W)	θ_{JA} (°C / W)	ψ_{JT}(°C / W)	ψ_{JB}(°C / W)
JEDEC 4 layer board, no airflow	0.7	18.2	0.8	5.3
8x6 inches 10 layer, no airflow	0.7	7.2	0.3	3.2
8x6 inches 20 layer, no airflow	0.7	6.4	0.3	3.2
8x6 inches 30 layer, no airflow	0.7	6.3	0.3	3.2

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6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
R_baud	Input Data Rate	Full Rate	9.8		12.5	Gbps
		Half Rate	4.9		6.25	Gbps
		Quarter Rate	2.45		3.125	Gbps
		Eighth Rate	1.225		1.5625	Gbps
POWER SUPPLY						
W	Power Consumption per Active Channel	CTLE only, 800mVp-p VOD, per channel, CDR locked		175		mW
		CDR Locking with CTLE only, 800mVp-p VOD, per channel		325		mW
		CTLE and DFE, 800mVp-p VOD, per channel, CDR locked		200	323	mW
		CDR Locking with CTLE and DFE, 800mVp-p VOD		350	535.5	mW
		PRBS Checker		100		mW
		PRBS Generator		105		mW
W_{STATIC}	Device Static Power Consumption	Power Applied to Device, No Signals Present		325	1325	mW
NT_{PS}	Power Supply Noise Tolerance	50 Hz to 100 Hz		100		mV_{PP}
		100 Hz to 10 MHz		40		
		10 MHz to 5.0 GHz		10		
LVCMOS						
V_{IH}	High level input voltage		1.75		VDD	V
V_{IL}	Low level input voltage		GND		0.7	V
V_{OH}	High level output voltage	IOH = 4mA	2			V
V_{OL}	Low level output voltage	IOL = -4mA			0.4	V
I_{IH}	Input High Leakage current	Vinput = VDD, Open Drain terminals			30	µA
		Vinput = VDD, JTAG terminals, Ref_CLK terminals			25	µA
		Vinput = VDD, ADDR, READ_EN, ALL_DONE terminals, EN_SMB terminal			75	µA
I_{IL}	Input Low Leakage current	Vinput = 0V, Open drain terminals	-15			µA
		Vinput = 0V, JTAG terminals, Ref_CLK terminals	-45			µA
		Vinput = 0V, ADDR, READ_EN, ALL_DONE terminals, EN_SMB terminal	-120			µA

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RX INPUTS						
R_{RD}	DC Input Resistance		80	100	120	Ω
V_{RX-IN}	Input Differential Voltage	Differential voltage seen at the high speed input terminals (1)			1600	mV_{PP}
V_{SDAT}	Signal Detect Assert Threshold	Default setting 1T pattern, 12.5 Gbps		110		mV_{PP}
		Default setting PRBS-31, 12.5 Gbps		24		
V_{SDDT}	Signal Detect De-Assert Threshold	Default setting 1T pattern, 12.5 Gbps		70		mV_{PP}
		Default setting PRBS-31, 12.5 Gbps		21		
V_{cm-RX}	Input common mode	Internal coupling cap	V_{RX-IN} / 4		VDD - (V_{RX-IN}/ 4)	V
TX OUTPUTS						
V_{OD}	Output Differential Voltage	drv_sel_vod[5:0] = 31, DEM, FIR = default	725	935	1135	mV_{PP}
		drv_sel_vod[5:0] = 15, DEM, FIR = default	350	470	595	
ΔV_{OD}	Step Size for drv_sel_vod Control	Default DEM, and FIR settings		50		mV_{PP}
ΔV_{ODVT}	Change in Output Differential Voltage due to Change in Temperature and Voltage			<15		mV_{PP}
T_{Rd}	Output Differential Resistance			100		Ω
t_r, t_f	Output Rise/Fall Time	20% - 80% using 8T Pattern, fir_sel_edge = default		35		ps
I_{OS}	Output Short Circuit Current	Differential Driver Output Pin Short to GND		-16		mA

(1) Parameter is not tested at final production

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RETIMER JITTER SPECS						
J_{TJ}	Total Output Jitter	PRBS-15 pattern, measured to 1e-12 10.3125 Gbps		0.08		UI
J_{RJ}	Output Random Jitter	PRBS-15 pattern, measured to 1e-12 10.3125 Gbps		3.6		mUI_{RMS}
J_{DJ}	Output Deterministic Jitter	PRBS-15 10.3125 Gbps		0.03		UI
J_{PEAK}	Jitter Peaking	Data Rate = 9.8 Gbps, Peaking Frequency = 1 - 3 MHz		<1		dB
		Data Rate = 12.5 Gbps Peaking Frequency = 3 - 8 MHz		<1		
BW_{PLL}	PLL Bandwidth at -3 dB	Data Rate = 9.8 Gbps		5		MHz
		Data Rate = 12.5 Gbps		10		
J_{TOL}	Input Jitter Tolerance	Jitter per SFF-8431 Appendix D.11 Combination of D_J P_J and R_J		>0.7		UI
RETIMER TIMING SPECS						
t_D	Propagation Delay from Rx inputs to Tx outputs	No Cross Point		3UI + 220ps		ps
		Cross Point enabled		3UI + 230ps		
t_{SK}	Channel To Channel Skew			<80		ps
RECOMMENDED REFERENCE CLOCK SPECS						
REF_f	Input Reference Clock Frequency			25		MHz
				125		
				312.5		
REF_{PPM}	Reference Clock PPM Tolerance	REF_f = 25 MHz (2)	-100		100	PPM
REF_{IDC}	Input Reference Clock Duty Cycle	REF_f = 25 MHz (2)	40%	50%	60%	
REF_{ODC}	Intrinsic Reference Clock Duty Cycle Distortion	Intrinsic Duty Cycle Distortion of the reference clock output from the CLK_MON pins		±1%		
REF_{VID}	Reference Clock Input Differential Voltage	Differential mode (2)	200		1200	mV_{PP}
REF_{VIH}	Reference Clock Signle-Ended Input High Threshold	Single-ended mode. Signal DC coupled to REF_CLK_P, REF_CLK_N is float		1.75		V
REF_{VIL}	Reference Clock Single-Ended Input Low Threshold	Single-ended mode. Signal DC coupled to REF_CLK_P, REF_CLK_N is float		0.7		V

(2) Parameter is specified by design and not tested at final production

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SMBus ELECTRICAL CHARACTERISTICS (SLAVE MODE)						
V_{IH}	Input High Level Voltage	SDA and SCL	1.75		3.6	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.8	V
C_{IN}	Input Pin Capacitance			<5		pF
V_{OL}	Low Level Output Voltage	SDA or SCL IOL = 1.25 mA			0.4	V
I_{IN}	Input Current	SDA or SCL, V_{INPUT} = V_{IN}, V_{DD}, GND	-15		15	µA
T_R	SDA Rise Time Read Operation	SDA, pullup resistor = 1 kΩ, Cb = 50pF		150		ns
T_F	SDA Fall Time Read Operation	SDA, pullup resistor = 1 kΩ, Cb = 50pF		4.5		ns
RECOMMENDED SMBus SWITCHING CHARACTERISTICS (SLAVE MODE)						
f_{SCL}	SCL Clock Frequency		10	100	400	kHz
$t_{HD:DAT}$	Data Hold Time			0.75		ns
$t_{SU:DAT}$	Data Setup Time			100		ns
RECOMMENDED SMBus SWITCHING CHARACTERISTICS (MASTER MODE)						
F_{SCL}	SCL Clock Frequency			400		kHz
T_{LOW}	SCL Low Period			1.25		µs
T_{HIGH}	SCL High Period			1.25		µs
$T_{HD:STA}$	Hold Time Start Operation			0.6		µs
$T_{SU:STA}$	Setup Time Start Operation			0.6		µs
$T_{HD:DAT}$	Data Hold Time			0.9		µs
$T_{SD:DAT}$	Data Setup Time			0.1		µs
$T_{SU:STO}$	Stop Condition Setup Time			0.6		µs
T_{BUF}	Bus Free Time between Stop-Start			1.3		µs
T_R	SCL and SDA Rise Time			300		ns
T_F	SCL and SDA Fall Time			300		ns
RECOMMENDED JTAG SWITCHING CHARACTERISTICS						
t_{TCK}	TCK Clock Period			100		ns
t_{SU}	TDI, TMI Setup Time to TCK			50		ns
t_{HD}	TDI, TMS Hold Time to TCK			50		ns
t_{DLY}	TCK Falling Edge to TDO			50		ns

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7 Detailed Description

7.1 Overview

The DS125DF1610 is a multi-rate, 16-channel retimer with integrated 4x4 cross point switches and receiver AC coupling capacitors. There is 1 cross point switch per 4 channels (quad). Each channel in the DS125DF1610 operates independently even if the cross point switch routing is enabled. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Variable Gain Amplifier (VGA), Clock and Data Recovery circuit (CDR) and a differential driver with a 3-tap transmit Finite Impulse Response (FIR) filter. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern checker and pattern generator that can be used for debug purposes.

The DS125DF1610 also supports JTAG boundary scan. The DS125DF1610 is configurable through a single SMBus port. The DS125DF1610 can also act as an SMBus master to configure itself from an EEPROM.

The sections below describe the functionality of the various circuits and features within the DS125DF1610. For more information about how to program or operate these features please consult the DS125DF1610 Programming Guide.

7.2 Functional Block Diagram

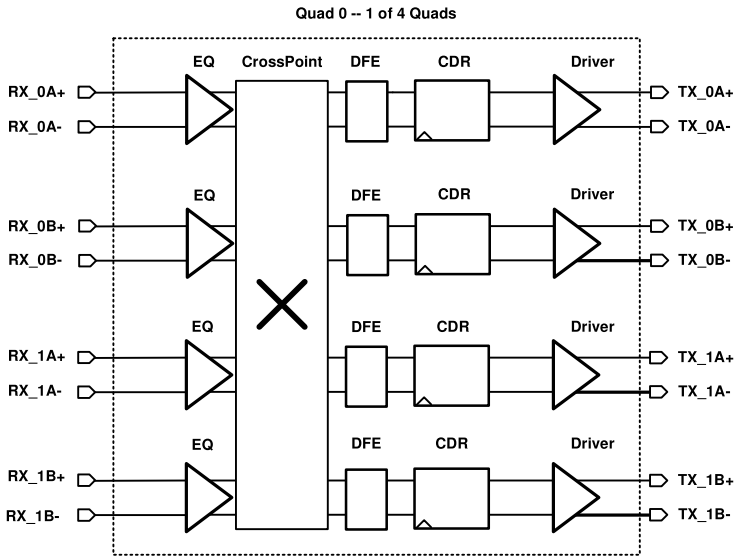


Figure 1. DS125DF1610 Simplified Cross Point Diagram

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Functional Block Diagram (continued)

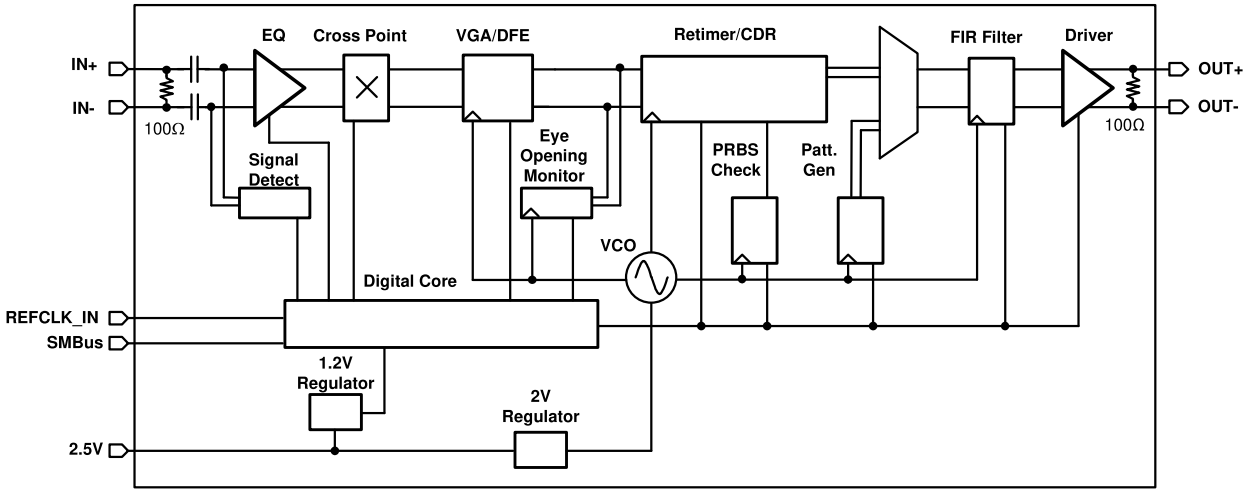


Figure 2. DS125DF1610 Simplified Data Path Diagram

7.3 Feature Description

7.3.1 Device Data Path Operation

The DS125DF1610 data path consists of several key blocks as shown in Figure 2. These key circuits are:

- AC-coupled Receiver with Signal Detect
- CTLE
- Cross Point Switch
- DFE with VGA
- CDR
- Differential Driver with FIR Filter

7.3.2 AC-Coupled Receiver with Signal Detect

The differential receiver for each DS125DF1610 channel contains on chip AC coupling capacitors. The minimum bandwidth for this AC coupled receiver is 16kHz. The receiver also contains a signal detect circuit.

The signal detect circuit monitors the energy level on the receiver inputs and powers on or off the rest of the high speed data path if a signal is detected or not. By default, each channel allows the signal detect circuit to automatically power on or off the rest of the high speed data path depending on if a signal is present. The signal detect block can be manually controlled in the SMBus channel registers. This can be useful if it is desired manually force channels to be disabled. For information on how to manually operate the signal detect circuit please see the DS125DF1610 Programming Guide and channel register 0x14 information.

7.3.3 CTLE

The CTLE in the DS125DF1610 is a fully adaptive equalizer with adjustable bandwidth and optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically re-adapted by resetting the CDR, set and then clear channel register 0x0A[3:2].

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Feature Description (continued)

The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. Users also have the option of limiting the EQ table length to any value between a minimum value of 1 and a maximum value of 32.

CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The boost levels can be set between 0 dB and 31 dB.

The CTLE bandwidth can be adjusted through SMBus control to 3 different levels:

Table 1. CTLE Bandwidth Settings

CTLE BANDWIDTH SETTING	BANDWDITH (GHz) (TYP)
Full Rate (default)	9
Mid Rate	7
Half Rate	5

The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE.

7.3.4 Cross Point Switch

Each quad has a 4x4 non-blocking analog cross point switch. This allows for full switching or broadcasting of data between any input within the quad to any output within the quad. Since the cross point switch is an analog implementation, all of the channels are allowed to operate asynchronously. The analog implementation also minimizes added latency through the device.

As shown in Figure 3, the cross point switch connections for each quad are located between CTLE and DFE in each channel.

The cross point switch consists of 4 sets of MUXs and buffers. In each channel there is a local buffer and a multi-drive buffer. The local buffer transmits data from the CTLE to the DFE of the same channel. The multi drive buffer transmits data from the CTLE to the DFE(s) of other channels within the quad. Each channel has two MUXs:

1. Data path mux – Selects whether to get data from the local buffer or from the other channel's multi-driver buffer
2. Control bus mux – Selects where the signal detect and EQ control bus should be connected. This setting should mirror the data path mux setting. Note, when an EQ is connected to another channel's CDR the EQ becomes associated with that CDR's register set. For example, if the cross point was configured to do point to point switching from the inputs of channel 0 to the output of channel 1 and the inputs of channel 1 to the outputs of channel 0, the EQ physically located at the pins for inputs of channel 0 would be accessible through the register set of channel 1.

A simplified diagram of the cross point switch is shown in Figure 3.

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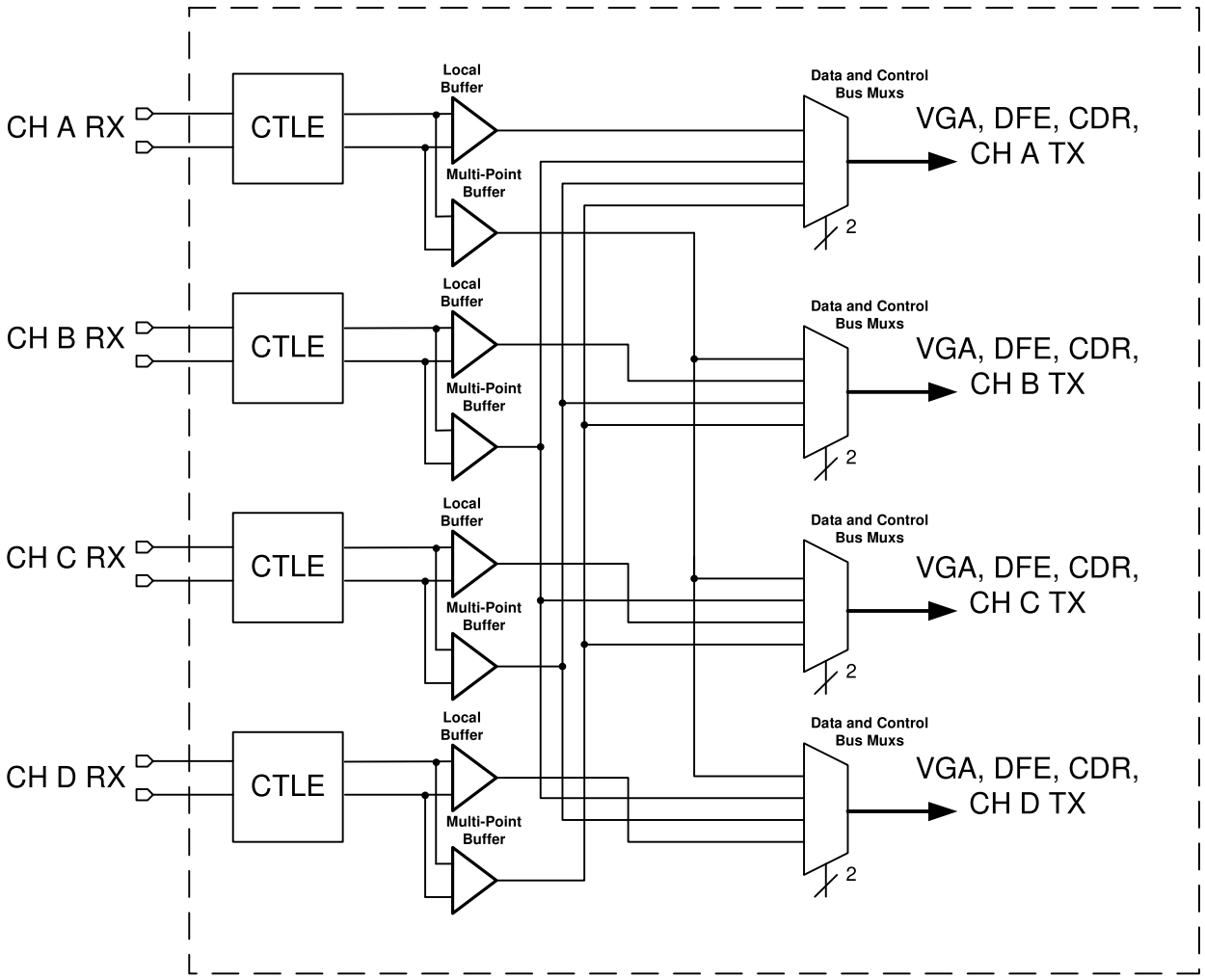


Figure 3. Cross Point Switch Diagram

Table 2. Cross Point Switch Channel Map

QUAD	Ch A	Ch B	Ch C	Ch D
0	TX/RX_0A	TX/RX_0B	TX/RX_1A	TX/RX_1B
1	TX/RX_2A	TX/RX_2B	TX/RX_3A	TX/RX_3B
2	TX/RX_4A	TX/RX_4B	TX/RX_5A	TX/RX_5B
3	TX/RX_6A	TX/RX_6B	TX/RX_7A	TX/RX_7B

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In a typical point-to-point switching application users must configure the following for each channel:

1. Control bus mux setting (ch reg 0x9B)
2. Data path mux setting (ch reg 0x96)
3. Enabling/Disabling the local or multi-drive buffers for each channel (ch reg 0x96)
4. Cross point enable bit (ch reg 0x96)
5. Perform a CDR reset and reset release (ch reg 0x0A)

Note, when using the cross point switch the local and multi-drive buffer should both be enabled regardless of the desired configuration.

The cross point switch can also be used to replicate data or perform a broadcast function. The options for this type of configuration include:

- 1:2 – any channel input to any 2 channels output
- 1:3 – any channel input to any 3 channels output
- 1:4 – any channel input to all 4 channels output

When the cross point switch is configured to replicate/broadcast data a master must be assigned during the cross point configuration. The master channel will have control over the CTLE adaption. All of the slave channels will be able to adapt their own DFE, but will not have control to adapt the CTLE. In this type of configuration there must be 1 channel assigned as a master. All other channels in the broadcast network must be assigned as slaves. There cannot be more than one master channel in a broadcast network. In a broadcast configuration, the straight through path connecting the broadcasting input to its own output needs to be enabled and set to have master control.

In a typical data replication/broadcast application users must configure the following for each channel:

1. Control bus mux setting (ch reg 0x9B)
2. Data path mux setting (ch reg 0x96)
3. Enabling/Disabling the local or multi-drive buffers for each channel (ch reg 0x96)
4. Master/Slave assignment (ch reg 0x96) -- master/slave bit set to master, master function assigned by mux setting
5. Cross point enable bit (ch reg 0x96)
6. Perform a CDR reset and reset release (ch reg 0x0A)

7.3.5 DFE with VGA

A 5-tap DFE with a VGA can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. Once the DFE has been enabled it can be configured to adapt only during lock acquisition or to adapt continuously. The DFE can also be manually configured to specified tap polarities and tap weights. However, when the DFE is configured manually the DFE auto-adaption should be disabled.

The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit.

Table 3. DFE Tap Weights

DFE Parameter	VALUE (mV) (TYP)
Tap 1 Weight Range	0 - 224
Tap 2-5 Weight Range	0 - 112
Tap Weight Step Size	7
Polarity	+ (positive): Signal is attenuated by the tap weight, register bit = 0 - (negative): Signal is boosted by the tap weight, register bit = 1

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The VGA is located within the DFE block. The VGA has 2-bit control and allows for 3 levels of boost. The VGA can be used to assist in the recovery of extremely small signals. Note that the default VGA should be used for most applications.

Table 4. VGA Boost Settings

VGA BOOST Setting (CH REG 0x8E[1:0])	BOOST (dB) (TYP)
00 (default)	0
01	6
10	6
11	12

7.3.6 Clock and Data Recovery

The CDR block consists of a Phase Locked Loop (PLL), reference clock based PPM counter, Input and Output Data Multiplexers (mux) and circuits to monitor single bit transitions and detect false locking. The CDR sampling position is fixed at the 0.5UI location for each bit.

By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.

The CDR requires the following in order to be properly configured:

- Input reference clock with proper reference clock divider setting to run the PPM counter.
- Expected data rates must be programmed into the CDR either through the rate/sub-rate Table 18 or entered manually with the corrected divider settings.

7.3.7 Reference Clock

The reference clock is not part of the CDR's PLL. The reference clock is connected only to the PPM counter for each CDR. The PPM counter constrains the allowable lock ranges of the CDR according to the programmed values in the rate/sub-rate Table 18 or the manually entered data rates.

The reference clock can be set to any of the 3 allowable frequencies independent of the data rate of the high speed channel. The input reference clock can be single-ended or differential for the 25 MHz or 125 MHz settings. If the 312.5 MHz setting is used, the input signaling type should be differential. The reference clock can be output through the CLK_MON pins for observation or daisy chaining the reference clock to the next device. If the CLK_MON port is used for daisy chaining then the output frequency should be set to 25 MHz.

If the reference clock port is configured to operate in single-ended mode, the 2.5V LVCMOS clock signal should be applied to the REF_CLK_P pin. In this configuration the REF_CLK_N pin should be floated (N/C). In this case the LVCMOS clock signal should be DC coupled into the REF_CLK_P pin. If the reference clock port is configured for differential mode, it is recommended to AC couple the clock signal into the DS125DF1610 device.

Configuring the reference clock frequency is done in share register 0x02[6:5]. Configuring the reference clock input port for single-ended or differential mode operation is done in share register 0x0B[4]. Enabling or disabling the CLK_MON port is done in share reg 0x0A[0]. Selecting the CLK_MON outputs to transmit the divided (25 MHz) or undivided (input frequency) clock frequency is done in share register 0x04[7].

Table 5. REF_CLK and CLK_MON Configurations

INPUT FREQUENCE	INPUT CONFIGURATION	DEFAULT CLK_MON FREQUENCY	RECOMMENDED CLK_MON OUTPUT FREQUENCY FOR DAISY CHAINING
25 MHz	Single-ended or Differential	25 MHz	25 MHz
125 MHz	Single-ended or Differential	125 MHz	25 MHz
312.5 MHz	Differential	312.5 MHz	25 MHz

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7.3.8 Differential Driver with FIR Filter

The DS125DF1610 uses a 3-tap FIR filter to assist with transmit equalization. The FIR filter consists of a pre cursor tap, a main cursor tap and a post cursor tap. Each tap has a polarity bit and 64 available levels. By default, the main cursor tap is set to a positive polarity, while the pre cursor and post cursor taps are set to a negative polarity. Users can invert the polarity of all 3 FIR taps to invert the polarity of the output data.

The DS125DF1610 output driver can be manually powered off through SMBus register control.

7.3.9 Setting the Output V_{OD}

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the drv_sel_vod bits, DEM bits, and FIR main cursor tap. The Table 6 below shows various settings for V_{OD} settings ranging from 150mV_{PP} to 1200 mV_{PP}. Using the FIR, DEM and drv_sel_vod bits is the recommended method for configuring the output V_{OD} for the best signal integrity.

Table 6. Typical V_{OD} Settings

V_{OD} (mV_{PP})	DEM SETTING	drv_sel_vod SETTING	FIR		
			PRE	MAIN	POST
1200	0	31	0	56	-4
1150	0	31	0	52	-4
1100	0	31	0	49	-4
1050	0	31	0	45	-4
1000	2	31	0	54	-3
950	3	31	0	56	-2
900	3	31	0	52	-2
850	3	31	0	46	-1
800	3	31	0	42	-1
750	3	25	0	56	-3
700	3	25	0	46	-2
650	3	25	0	40	-1
600	3	21	0	50	-2
550	3	19	0	50	-3
500	3	17	0	52	-3
450	3	15	0	50	-3
400	3	13	0	52	-3
350	3	12	0	51	-3
300	3	10	0	51	-3
250	3	8	0	55	-3
200	3	6	0	56	-3
150	3	4	0	57	-3

7.3.10 Output Driver Polarity Inversion

In some applications it may be necessary to invert the polarity of the data transmitted from the retimer. To invert the polarity of the data read back the FIR polarity settings for the pre, main and post cursor taps and then invert these bits.

7.3.11 Driver Output Rise/Fall Time

In some applications, a longer rise/fall time for the output signal is desired. This can reduce electromagnetic interference (EMI) generated by fast switching waveforms. This is necessary in some applications for regulatory compliance. In others, it can reduce the crosstalk in the system.

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The DS125DF1610 can be configured to operate with a nominal rise/fall time corresponding to the maximum slew rate of the output drivers into the load capacitance. Alternatively, the DS125DF1610 can be configured to operate with a slightly greater rise/fall time if desired. By default the DS125DF1610 is configured to use the fastest edge rate.

Table 7. Differential Driver Edge Rate Settings

EDGE RATE SETTING (CH REG 0x8E[4:2])	20-80 TYPICAL EDGE RATE (ps) (TYP)
111 (Default)	35
110	40
101	45
100	50
011	55
010	60
001	65
000	70

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7.3.12 Debug Features

7.3.12.1 Pattern Generator

Each channel in the DS125DF1610 can be configured to generate a 16-bit user defined data pattern or a pseudo random bit sequence (PRBS). The user defined pattern can also be set to automatically invert every other 16-bit symbol for DC balancing purposes. The DS125DF1610 pattern generator supports the following PRBS sequences:

- PRBS – 2^7 - 1
- PRBS – 2^9 - 1
- PRBS – 2^{15} - 1
- PRBS – 2^{31} - 1

7.3.12.2 Pattern Checker

The pattern checker can be manually set to look for specific PRBS sequences and polarities or it can be set to automatically detect the incoming pattern and polarity.

The pattern checker consists of a 47-bit word counter and an 11-bit error counter. The pattern checker uses 32-bit words.

In order to read out the bit and error counters, the pattern checker must first be frozen. Continuous operation with simultaneous read out of the bit and error counters is not supported in this implementation.

7.3.12.3 Eye Opening Monitor

The DS125DF1610's Eye Opening Monitor (EOM) measures the internal data eye at the input of the CDR and can be used for 2 functions:

1. Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) measurement
2. Full Eye Diagram Capture

The HEO measurement is made at the 0V crossing and is read in channel register 0x27. The VEO measurement is made at the 0.5 UI mark and is read in channel register 0x28. The HEO and VEO registers can be read from channel registers 0x27 and 0x28 at any time while the CDR is locked. The following equations are used to convert the contents of channel registers 0x27 and 0x28 into their appropriate units:

- HEO [UI] = ch reg 0x27 ÷ 64
- VEO [mV] = ch reg 0x28 x 3.125

A full eye diagram capture can be performed when the CDR is locked. The eye diagram is constructed within a 64 x 64 array, where each cell in the matrix consists of an 16-bit word. Users can manually adjust the vertical scaling of the EOM or allow the state machine to control the scaling which is the default option. The horizontal scaling controlled by the state machine and is always directly proportional to the data rate.

When a full eye diagram plot is captured, the retimer will shift out 4 16-bit words of junk data that should be discarded followed by 4096 16-bit words that make up the 64 x 64 eye plot. The first actual word of the eye plot from the retimer is for (X, Y) position (0,0). Each time the eye plot data is read out the voltage position is incremented. Once the voltage position has incremented to position 63, the next read will cause the voltage position to reset to 0 and the phase position to increment. This process will continue until the entire 64 x 64 matrix is read out. Figure 4 shows the EOM read out sequence overlaid on top of a simple eye opening plot. In this plot any hits are shown in green. This type of plot is helpful for quickly visualizing the HEO and VEO. Users can apply different algorithms to the output data to plot density or color gradients to the output data.

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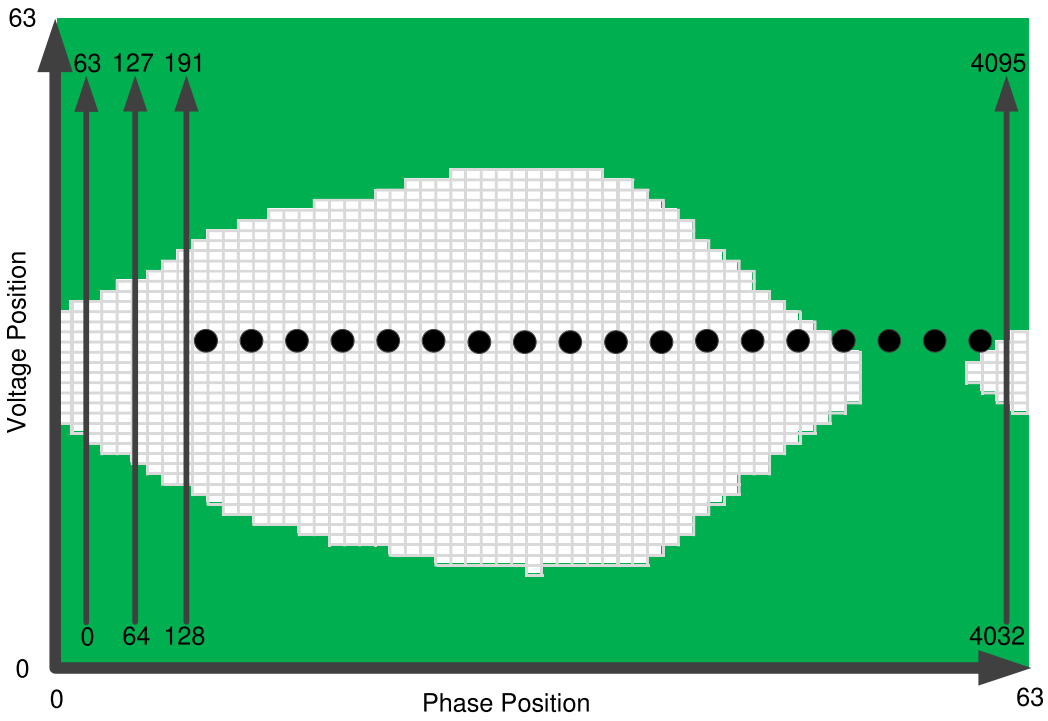


Figure 4. EOM Full Eye Capture Readout

To manually control the EOM vertical range, remove scaling control from the state machine then select the desired range:

1. Channel Reg 0x2C[6] → 0
2. See Table 8

Table 8. Eye Opening Monitor Vertical Range Settings

CH REG 0x11[7:6] VALUE	EOM VERTICAL RANGE [mV]
2'b00	±100
2'b01	±200
2'b10	±300
2'b11	±400

The EOM operates as an under-sampled circuit. This allows the EOM to be useful in identifying over equalization, ringing and other gross signal conditioning issues. However, the EOM cannot be correlated to a bit error rate.

The EOM can be accessed in two ways to read out the entire eye plot:

- Multi-byte reads can be used such that data is repeatedly latched out from channel register 0x25.
- Or single byte reads. With single byte reads, the MSB are located in register 0x25 and the LSB are located in register 0x26. In this mode, the device must be addressed each time a new byte is read.

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To perform a full eye capture with the EOM, follow these steps within the desired channel register set:

Table 9. Eye Opening Monitor Full Eye Capture Instructions

STEP	REGISTER [bits]	VALUE	DESCRIPTION
1	0x67[5]	0	Disable lock EOM lock monitoring
2	0x2C[6] 0x11[7:6]	0 2'b--	Set the desired EOM vertical range
3	0x11[5]	0	Power on the EOM
4	0x24[7]	1	Enable fast EOM
5	0x24[0] 0x25 0x26	1	Begin read out of the 64 x 64 array, discard first 4 words Ch reg 0x24[0] is self clearing. 0x25 is the MSB of the 16-bit word 0x26 is the LSB of the 16-bit word
6	0x25 0x26		Continue reading information until the 64 x 64 array is complete.
7	0x67[5] 0x2C[6] 0x11[5] 0x24[7,1]	1 1 1 0	Return the EOM to its original state. Undo steps 1-4

7.3.13 Interrupt Signals

The DS125DF1610 can be configured to report different events as interrupt signals. These interrupt signals do not impact the operation of the device, but merely report that the selected event has occurred. The interrupt bits in the register sets are all sticky bits. This means that when an event triggers an interrupt the status bit for that interrupt is set to logic HIGH. This interrupt status bit will remain at logic HIGH until the bit has been read. Once the bit has been read it will be automatically cleared, which allows for new interrupts to be detected. The DS125DF1610 will report the occurrence of an interrupt through the INTERR_IO pin. The INTERR_IO pin is an open drain output that will pull the line low when an interrupt signal is triggered.

Note that all available interrupts are disabled by default. Users must activate the various interrupts before they can be used.

The interrupts available in the DS125DF1610 are:

- CDR loss of lock
- CDR locked
- Signal detect loss
- Signal detected
- PRBS pattern checker bit error detected
- HEO/VEO threshold violation

When an interrupt occurs, share register 0x08 and 0x09 report which channel generated the interrupt request. Users can then select the channel(s) that generated the interrupt request and service the interrupt by reading the appropriate interrupt status bits in the corresponding channel registers.

7.3.14 Other Features

7.3.14.1 Lock Sequencer

A channel will temporarily consume a higher amount of power while its CDR is attempting to lock, compared to when the CDR is locked. In order to reduce the impact of a power consumption spike when data is transmitted to a DS125DF1610, the internal lock sequencer will limit the number of active channels that are simultaneously allowed to attempt to lock.

The lock sequencer grants tokens to various channels that have detected a signal at the input to the CTLE. Once a channel has achieved CDR lock, it returns its token to the lock sequencer. The lock sequencer will distribute any available tokens on a first come first serve basis to any channel that is allowed to attempt lock and that has detected a valid signal.

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The lock sequencer is configurable in the share registers. Users can control which channels are allowed to attempt lock when a signal is present by configuring share registers 0x0F and 0x10. Users can also limit the number of channels that are allowed to simultaneously attempt to lock by configuring share register 0x05.

7.3.14.2 $\overline{\text{RESET\_IO}}$ Pin

The $\overline{\text{RESET\_IO}}$ pin in the DS125DF1610 emulates a power on reset (POR). This type of reset re-initializes the entire device including the SMBus address strap settings and restores both share and channel register defaults.

The $\overline{\text{RESET\_IO}}$ pin triggers a reset on the rising edge of the signal. It is not recommended to hold the $\overline{\text{RESET\_IO}}$ terminal at a logic LOW state for an extended period of time. $\overline{\text{RESET\_IO}}$ should be held at logic HIGH during power on. After power on, the $\overline{\text{RESET\_IO}}$ terminal should be pulsed low for a minimum of 10 µs to perform a reset. After power on, the $\overline{\text{RESET\_IO}}$ terminal can be held low longer than 10µs, but the device will only be in a partial reset state for the during this time. Note, reset and partial reset states are not sleep or power down states.

7.4 Device Functional Modes

7.4.1 SMBus Master Mode

SMBus master mode allows the DS125DF1610 to program itself by reading directly from an external EEPROM. When using the SMBus master mode, the DS125DF1610 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines:

- Maximum EEPROM size is 2048 Bytes
- Minimum EEPROM size for a single DS125DF1610 with individual channel configuration is 1417 Bytes (3 base header bytes + 3 address map bytes + 16 x 88 channel register bytes + 3 share register bytes; bytes are defined to be 8-bits)
- Set ENSMB = VDD through 1kΩ resistor, enable SMBus master mode
- The external EEPROM device address byte must be 0xA0
- The external EEPROM device must support 400kHz operation at 2.5V supply
- Set the SMBus address of the DS125DF1610 by configuring the ADDR0 and ADDR1 terminals.

When loading multiple DS125DF1610 devices from the same EEPROM, use these guidelines to configure the devices:

- Configure the SMBus addresses for each DS125DF1610 to be sequential. The first device in the sequence must have an address of 0x30.
- Daisy chain READEN and ALL_DONE from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
- All DS125DF1610 devices sharing the same EEPROM must be configured with the common channel bit set to 1. With common channel configuration enabled, each DS125DF1610 device will configure all 16 channels with the same settings.

When loading a single DS125DF1610 from an EEPROM, use these guidelines to configure the device:

- Set the common channel bit to 0 to allow for individual channel configuration. Or set the common channel bit to 1 to load the same configuration settings to all channels.
- When configuring individual channels, a 2048 Byte EEPROM must be used.
- If there are multiple DS125DF1610 devices on a PCB that require individual channel configuration, then each device must have its own EEPROM.

7.4.2 SMBus Slave Mode

7.4.2.1 SDA and SDC

In both SMBus master and SMBus slave mode, the DS125DF1610 is configured using the SMBus. The SMBus consists of two lines, the SDA or serial data line and the SCL or serial clock line. In the DS125DF1610 these pins are 3.3V tolerant. The SDA and SCL lines are both open-drain. They require a pull-up resistor to a supply voltage, which may be either 2.5V or 3.3V. A pull-up resistor in the 2kΩ to 5kΩ range will provide reliable SMBus operation.

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Device Functional Modes (continued)

7.4.2.2 SMBus Address Configuration

In either SMBus mode the DS125DF1610 must be assigned a unique SMBus address.

The DS125DF1610 can be configured to respond to one of the sixteen SMBus addresses listed in the Table 10 below. GPIO1 and GPIO0 are configured to be four level inputs immediately after the device powers on. Logic 0 can be set by tying the pin to ground through a ≤1kΩ resistor. Logic R is set by tying the pin to ground through a 20kΩ resistor. Logic F is set by floating the pin. Logic 1 is set by tying the pin to VCC = 2.5V through a ≤1kΩ resistor.

Table 10. SMBus Address Configuration

ADDR1(GPIO1) (pin D5)	ADDR0(GPIO0) (pin B6)	7-BIT ADDRESS	8-BIT WRITE ADDRESS
0	0	7'h18	0x30
0	R	7'h19	0x32
0	F	7'h1A	0x34
0	1	7'h1B	0x36
R	0	7'h1C	0x38
R	R	7'h1D	0x3A
R	F	7'h1E	0x3C
R	1	7'h1F	0x3E
F	0	7'h20	0x40
F	R	7'h21	0x42
F	F	7'h22	0x44
F	1	7'h23	0x46
1	0	7'h24	0x48
1	R	7'h25	0x4A
1	F	7'h26	0x4C
1	1	7'h27	0x4E

When an SMBus device is addressed for reading or writing a bit is appended to the address a the least significant bit space. This bit is set to 0 for a write or to 1 for a read.

7.4.3 Device Configuration in SMBus Slave Mode

The configurable settings of the DS125DF1610 may be set independently for each channel at any time after power up using the SMBus. A register write is accomplished when the controller sends a START condition on the SMBus followed by the Write address of the DS125DF1610 to be configured. After sending the Write address of the DS125DF1610, the controller sends the register address byte followed by the register data byte. The DS125DF1610 acknowledges each byte written to the controller according to the data link protocol of the SMBus Version 2.0 Specification. See this specification for additional information on the operation of the SMBus.

There are 3 types of device registers in the DS125DF1610. These are the global registers, shared registers and the channel registers. The global registers are programmed to access the various channel registers or the shared registers. The shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF1610 at the greater device level.

The channel registers are used to set all the configuration settings of the DS125DF1610. They provide independent control for each channel of the DS125DF1610 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF1610 on a channel-by-channel basis.

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7.5 Programming

7.5.1 Bit Fields in the Register Set

Many of the registers in the DS125DF1610 are divided into bit fields. This allows a single register to serve multiple purposes, which may be unrelated. Often configuring the DS125DF1610 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged.

The procedure for accomplishing this is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all the register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.

Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions. Register bits can have the following interface constraints:

- R - Read only
- RW - Read/Write
- RWSC - Read/Write, self clearing
- W - Write only

7.5.2 Writing to and Reading from the Global/Shared/Channel Registers

Global registers can be accessed from the shared register page and also the channel register pages. There are three global registers in the DS125DF1610:

1. Register 0xFC
2. Register 0xFD
3. Register 0xFF

Registers 0xFC and 0xFD are used to select the channel registers to be written to. To select a channel write a 1 to its corresponding bit in these global registers. Note more than one channel may be written to by setting multiple bits in registers 0xFC and 0xFD. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0x00.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in the 0xFC or 0xFD registers. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value.

Table 11. Channel Select Global Registers

GLOBAL REGISTER	BIT	DESCRIPTION	CDR/TX PIN ASSIGNMENT
0xFD	7	Channel 15– Quad 3 Channel 3 – Cross Point Ch D	TX_7B
	6	Channel 14– Quad 3 Channel 2 – Cross Point Ch C	TX_7A
	5	Channel 13– Quad 3 Channel 1 – Cross Point Ch B	TX_6B
	4	Channel 12– Quad 3 Channel 0 – Cross Point Ch A	TX_6A
	3	Channel 11– Quad 2 Channel 3 – Cross Point Ch D	TX_5B
	2	Channel 10– Quad 2 Channel 2 – Cross Point Ch C	TX_5A
	1	Channel 9– Quad 2 Channel 1 – Cross Point Ch B	TX_4B
	0	Channel 8– Quad 2 Channel 0 – Cross Point Ch A	TX_4A

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Programming (continued)

Table 11. Channel Select Global Registers (continued)

GLOBAL REGISTER	BIT	DESCRIPTION	CDR/TX PIN ASSIGNMENT
0xFC	7	Channel 7– Quad 1 Channel 3 – Cross Point Ch D	TX_3B
	6	Channel 6– Quad 1 Channel 2 – Cross Point Ch C	TX_3A
	5	Channel 5– Quad 1 Channel 1 – Cross Point Ch B	TX_2B
	4	Channel 4– Quad 1 Channel 0 – Cross Point Ch A	TX_2A
	3	Channel 3– Quad 0 Channel 3 – Cross Point Ch D	TX_1B
	2	Channel 2– Quad 0 Channel 2 – Cross Point Ch C	TX_1A
	1	Channel 1– Quad 0 Channel 1 – Cross Point Ch B	TX_0B
	0	Channel 0 – Quad 0 Channel 0 – Cross Point Ch A	TX_0A

Table 12. Shared-Channel Select Global Register

GLOBAL REGISTER	BIT	DESCRIPTION
0xFF	7:2	These bits are not used and default to 0
	1	1: Broadcast write to all channels, 0xFF[0] must be set to 1. 0: Normal operation, select channel register as defined in 0xFC and 0xFD
	0	1: Select Channel Registers 0: Select Share Registers

Table 13. Shared Registers

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
0	7	0	R	N	SMBus_Addr3	SMBus Address Strapped 7-bit addres is 0x18 + SMBus_Addr[3:0]
	6	0	R	N	SMBus_Addr2	
	5	0	R	N	SMBus_Addr1	
	4	0	R	N	SMBus_Addr0	
	3	0	R	Y	RESERVED	
	2:0	0	R	N	RESERVED	
1	7	0	R	N	Version2	Device version
	6	1	R	N	Version1	
	5	1	R	N	Version0	
	4	1	R	N	Device_ID4	Device ID code for DS125DF1610
	3	0	R	N	Device_ID3	
	2	0	R	N	Device_ID2	
	1	0	R	N	Device_ID1	
	0	1	R	N	Device_ID0	
2	7	0	RW	N	RESERVED	
	6	0	RW	Y	REFCLK_SEL1	Sets the REFCLK input frequency 00: 25 MHz 01: 125 MHz 10: 312.5MHz 11: Reserved
	5	0	RW	Y	REFCLK_SEL0	
	4:0	0	RW	N	RESERVED	
3	7:3	0	R	N	RESERVED	
	2	0	R	Y	RESERVED	
	1:0	0	R	N	RESERVED	

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Table 13. Shared Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
4	7	0	RW	N	SEL_REF_CLK_DIG_OUT_ANA	1: Selects the divided clock 0: Selects the undivided clock
	6	0	RWSC	N	RST_SMB_REGS	1: Resets share registers
	5	0	RWSC	N	RST_SMB_MAS	1: Resets SMBus Master controller
	4	0	RW	N	RESERVED	
	3	0	RW	N	MR_DIS_LOCK_SEQR	1: Disables the lock sequencer circuit 0: Normal operation, lock sequencer is enabled
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	1	RW	N	RESERVED	
5	7	0	RW	N	RESERVED	
	6	0	RW	N	CRC_EN	1: Slave CRC Trigger
	5	0	RW	N	RESERVED	
	4	1	R	N	EEPROM_READ_DONE	This bit is set to 1 when read from EEPROM is done
	3	1	RW	N	LIMIT_CONC_LOCKS3	Sets max number of channels that can lock at any given time, defaults to 8 channels.
	2	0	RW	N	LIMIT_CONC_LOCKS2	
	1	0	RW	N	LIMIT_CONC_LOCKS1	
	0	0	RW	N	LIMIT_CONC_LOCKS0	
6	7:0	0	RW	N	RESERVED	
7	7:0	0	RW	N	RESERVED	
8	7	0	R	N	INT_Q1C3	Interrupt from quad 1, ch 3
	6	0	R	N	INT_Q1C2	Interrupt from quad 1, ch 2
	5	0	R	N	INT_Q1C1	Interrupt from quad 1, ch 1
	4	0	R	N	INT_Q1C0	Interrupt from quad 1, ch 0
	3	0	R	N	INT_Q0C3	Interrupt from quad 0, ch 3
	2	0	R	N	INT_Q0C2	Interrupt from quad 0, ch 2
	1	0	R	N	INT_Q0C1	Interrupt from quad 0, ch 1
	0	0	R	N	INT_Q0C0	Interrupt from quad 0, ch 0
9	7	0	R	N	INT_Q3C3	Interrupt from quad 3, ch 3
	6	0	R	N	INT_Q3C2	Interrupt from quad 3, ch 2
	5	0	R	N	INT_Q3C1	Interrupt from quad 3, ch 1
	4	0	R	N	INT_Q3C0	Interrupt from quad 3, ch 0
	3	0	R	N	INT_Q2C3	Interrupt from quad 2, ch 3
	2	0	R	N	INT_Q2C2	Interrupt from quad 2, ch 2
	1	0	R	N	INT_Q2C1	Interrupt from quad 2, ch 1
	0	0	R	N	INT_Q2C0	Interrupt from quad 2, ch 0

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Table 13. Shared Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
A	7	0	RW	N	SEL_CLK_FROM_DIG	1: selects ref clk from digital to transmit out 0: selects ref clk from analog loop chain to transmit out. All channels' analog blocks must have ref clk loop through enabled to transmit ref clk out of device
	6	0	RW	N	SEL_REFCLK_TX_VCM1	Sets the output common-mode voltage: 00: 800mV 01: 1000mV 10: 1200mV 11: Tracks VCC, bias at 1.2V
	5	0	RW	N	SEL_REFCLK_TX_VCM0	
	4	0	RW	N	SEL_REFCLK_TX_VOD1	Sets the output differential peak-to-peak voltage: 00: 400mV 01: 533mV 10: 667mV 11: 800mV
	3	0	RW	N	SEL_REFCLK_TX_VOD0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	SEL_REFCLK_TX_SCP	1:disable 0:Ref-clk TX short-circuit protection
	0	1	RW	Y	DIS_REFCLK_OUT	1: Disable REFCLK_OUT (TRI-STATE) 0: Enable REFCLK_OUT
B	7	0	RW	N	RESERVED	
	6	0	R	N	REFCLK_DET	This bit is set to 1 when refclk has been detected
	5	0	RW	N	RESERVED	
	4	0	RW	N	REFCLK_SINGLE_END	1: Reference clock input port configured as single-ended input 0: Normal operation, reference clock input port configured as differential input
	3:0	0	RW	N	RESERVED	
C	7:3	0	RW	N	RESERVED	
	2	0	RW	N	SAR_ADC_RST	Resets SAR ADC
	1	0	RW	N	SAR_ADC_EN	Enables SAR ADC
	0	0	RW	N	RESERVED	
D	7	0	RW	N	SAR_ADC_OUT7	10-bit SAR ADC Output[7:0]
	6	0	RW	N	SAR_ADC_OUT6	
	5	0	RW	N	SAR_ADC_OUT5	
	4	0	RW	N	SAR_ADC_OUT4	
	3	0	RW	N	SAR_ADC_OUT3	
	2	0	RW	N	SAR_ADC_OUT2	
	1	0	RW	N	SAR_ADC_OUT1	
	0	0	RW	N	SAR_ADC_OUT0	
E	7:2	0	RW	N	RESERVED	
	1	0	R	N	SAR_ADC_OUT9	10-bit SAR ADC Output[9:8]
	0	0	R	N	SAR_ADC_OUT8	

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Table 13. Shared Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
F	7	1	RW	Y	EN_CH_LOCK15	1: Allows channel to lock 0: Channel not allowed to lock
	6	1	RW	Y	EN_CH_LOCK14	1: Allows channel to lock 0: Channel not allowed to lock
	5	1	RW	Y	EN_CH_LOCK13	1: Allows channel to lock 0: Channel not allowed to lock
	4	1	RW	Y	EN_CH_LOCK12	1: Allows channel to lock 0: Channel not allowed to lock
	3	1	RW	Y	EN_CH_LOCK11	1: Allows channel to lock 0: Channel not allowed to lock
	2	1	RW	Y	EN_CH_LOCK10	1: Allows channel to lock 0: Channel not allowed to lock
	1	1	RW	Y	EN_CH_LOCK9	1: Allows channel to lock 0: Channel not allowed to lock
	0	1	RW	Y	EN_CH_LOCK8	1: Allows channel to lock 0: Channel not allowed to lock
10	7	1	RW	Y	EN_CH_LOCK7	1: Allows channel to lock 0: Channel not allowed to lock
	6	1	RW	Y	EN_CH_LOCK6	1: Allows channel to lock 0: Channel not allowed to lock
	5	1	RW	Y	EN_CH_LOCK5	1: Allows channel to lock 0: Channel not allowed to lock
	4	1	RW	Y	EN_CH_LOCK4	1: Allows channel to lock 0: Channel not allowed to lock
	3	1	RW	Y	EN_CH_LOCK3	1: Allows channel to lock 0: Channel not allowed to lock
	2	1	RW	Y	EN_CH_LOCK2	1: Allows channel to lock 0: Channel not allowed to lock
	1	1	RW	Y	EN_CH_LOCK1	1: Allows channel to lock 0: Channel not allowed to lock
	0	1	RW	Y	EN_CH_LOCK0	1: Allows channel to lock 0: Channel not allowed to lock
11	7:6	0	R	N	EEPRM_LOAD_STATUS	11: Not valid 10: EEPROM load completed successfully 01: EEPROM load failed after 64 attempts 00: EEPROM load in progress
	5	0	R	N	EEPRM_ATMPT5	Number of attempts made to load EEPROM image
	4	0	R	N	EEPRM_ATMPT4	
	3	0	R	N	EEPRM_ATMPT3	
	2	0	R	N	EEPRM_ATMPT2	
	1	0	R	N	EEPRM_ATMPT1	
	0	0	R	N	EEPRM_ATMPT0	

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Table 13. Shared Registers (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
FC	7	0	RW	N	Channel 7– Quad 1 Channel 3	1: Enables SMBus access to channel 7
	6	0	RW	N	Channel 6– Quad 1 Channel 2	1: Enables SMBus access to channel 6
	5	0	RW	N	Channel 5– Quad 1 Channel 1	1: Enables SMBus access to channel 5
	4	0	RW	N	Channel 4– Quad 1 Channel 0	1: Enables SMBus access to channel 4
	3	0	RW	N	Channel 3– Quad 0 Channel 3	1: Enables SMBus access to channel 3
	2	0	RW	N	Channel 2– Quad 0 Channel 2	1: Enables SMBus access to channel 2
	1	0	RW	N	Channel 1– Quad 0 Channel 1	1: Enables SMBus access to channel 1
	0	0	RW	N	Channel 0– Quad 0 Channel 0	1: Enables SMBus access to channel 0
FD	7	0	RW	N	Channel 15– Quad 3 Channel 3	1: Enables SMBus access to channel 15
	6	0	RW	N	Channel 14– Quad 3 Channel 2	1: Enables SMBus access to channel 14
	5	0	RW	N	Channel 13– Quad 3 Channel 1	1: Enables SMBus access to channel 13
	4	0	RW	N	Channel 12– Quad 3 Channel 0	1: Enables SMBus access to channel 12
	3	0	RW	N	Channel 11– Quad 2 Channel 3	1: Enables SMBus access to channel 11
	2	0	RW	N	Channel 10– Quad 2 Channel 2	1: Enables SMBus access to channel 10
	1	0	RW	N	Channel 9– Quad 2 Channel 1	1: Enables SMBus access to channel 9
	0	0	RW	N	Channel 8– Quad 2 Channel 0	1: Enables SMBus access to channel 8
FE	7	0	R	N	VENDOR_ID7	
	6	0	R	N	VENDOR_ID6	
	5	0	R	N	VENDOR_ID5	
	4	0	R	N	VENDOR_ID4	
	3	0	R	N	VENDOR_ID3	
	2	0	R	N	VENDOR_ID2	
	1	1	R	N	VENDOR_ID1	
	0	1	R	N	VENDOR_ID0	
FF	7:2	0	RW	N	RESERVED	
	1	0	RW	N	WRITE_ALL_CH	1: Write to all channels as if they are the same, but only allows to read back from a single channel specified in 0xFC and 0xFD. Note: EN_CH_SMB must be set to 1, or else this function is invalid.
	0	0	RW	N	EN_CH_SMB	1: Enables SMBus access to the channels specified in 0xFC and 0xFD. 0: Enables SMBus access to the shared registers

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Table 14. Channel Registers, 0 to 1F

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
0	7	0	RW	N	CLK_CORE_DIS	1: Disables the primary digital clock, resets all state machines 0: Normal operation
	6:4	0	RW	N	RESERVED	
	3	0	RW	N	RST_CORE	1: Reset core state machine 0: Normal Operation
	2	0	RW	N	RST_REGS	1: Resets channel registers, restores default values 0: Normal Operation
	1	0	RW	N	RST_VCO	1: Resets PPM counter, EOM counter, FLD counter, SBT counter 0: Normal Operation
	0	0	RW	N	RST_REFCLK	1: Reset PPM counter 0: Normal Operation
1	7	0	R	N	SIG_DET	1: Signal is present on high speed inputs 0: No signal is detected on high speed inputs
	6	0	R	N	POL_INV_DET	1: PRBS checker detected polarity inversion 0: No pattern inversion detected
	5	0	R	N	CDR_LOCK_LOSS_INT	1: indicates loss of CDR lock after having acquired it. Bit clears on read.
	4	0	R	N	PRBS_SEQ_DET3	1: Indicates if the PRBS-31 sequence is locked
	3	0	R	N	PRBS_SEQ_DET2	1: Indicates if the PRBS-15 sequence is locked
	2	0	R	N	PRBS_SEQ_DET1	1: Indicates if the PRBS-9 sequence is locked
	1	0	R	N	PRBS_SEQ_DET0	1: Indicates if the PRBS-7 sequence is locked
	0	0	R	N	SIG_DET_LOSS_INT	Loss of signal indicator. Bit is set once signal is acquired and then lost.
2	7:0	0	R	N	MULTI_PURP_STATUS	Register configured by setting channel register 0x0C[7:4]
3	7	0	RW	Y	EQ_BST0[1]	This register can be used to force an EQ boost setting if used in conjuntion with channel register 0x2D[3]
	6	0	RW	Y	EQ_BST0[0]	
	5	0	RW	Y	EQ_BST1[1]	
	4	0	RW	Y	EQ_BST1[0]	
	3	0	RW	Y	EQ_BST2[1]	
	2	0	RW	Y	EQ_BST2[0]	
	1	0	RW	Y	EQ_BST3[1]	
	0	0	RW	Y	EQ_BST3[0]	
4	7:4	0	RW	N	RESERVED	
	3	0	RW	Y	RESERVED	
	2:0	0x01	RW	N	RESERVED	
5	7:0	0x01	RW	N	RESERVED	
6	7:0	0x01	RW	N	RESERVED	
7	7:0	0x01	RW	N	RESERVED	

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Table 14. Channel Registers, 0 to 1F (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
8	7	0	RW	Y	RESERVED	
	6	1	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	RESERVED	
	0	0	RW	Y	RESERVED	
9	7	0	RW	Y	DIVSEL_VCO_CAP_OV	Enable bit to override cap_cnt with value in register 0x0B[4:0]
	6	0	RW	Y	SET_CP_LVL_LPF_OV	Enable bit to override lpf_dac_val with value in register 0x1F[4:0]
	5	0	RW	Y	BYPASS_PFD_OV	Enable bit to override sel_retimed_loopthru and sel_raw_loopthru with values in reg 0x1E[7:5]
	4	0	RW	Y	EN_FD_PD_VCO_PDIQ_OV	Enable bit to override en_fd, pd_pd, pd_vco, pd_pdiq with reg 0x1E[0], reg 0x1E[2], reg 0x1C[0], reg 0x1C[1]
	3	0	RW	Y	EN_PD_CP_OV	Enable bit to override pd_fd_cp and pd_pd_cp with value in reg 0x1B[1:0]
	2	0	RW	Y	DIVSEL_OV	Enable bit to override divsel with value in reg 0x18[6:4] 1: Override enable 0: Normal operation
	1	0	RW	Y	EN_FLD_OV	Enable to override pd_fld with value in reg 0x1E[1]
	0	0	RW	Y	PFD_LOCK_ MODE_SM	Enable FD in lock state
A	7	0	RW	Y	SBT_EN	Enable bit to override sbt_en with value in reg 0x1D[7]
	6	1	RW	Y	EN_IDAC_PD_CP_OV EN_IDAC_FD_CP_OV	Enable bit to overridephase detector charge pump settings with reg 0x1C[7:5] Enable bit to override frequency detector charge pump settings with reg 0x1C[4:2]
	5	0	RW	Y	DAC_LPF_HIGH_ PHASE_OV DAC_LPF_LOW_ PHASE_OV	Enable bit to override loop filter comparator trip voltage with reg 0x16[7:0]
	4	1	RW	Y	EN150_LPF_OV	Enable bit to override en150_lpf with value in reg 0x1F[6]
	3	0	RW	N	CDR_RESET_OV	Enable bit to override CDR reset with reg 0x0A[2]
	2	0	RW	N	CDR_RESET_SM	1: CDR is put into reset 0: normal CDR operation
	1	0	RW	N	CDR_LOCK_OV	Enable CDR lock signal override with reg 0x0A[0]
	0	0	RW	N	CDR_LOCK	CDR lock signal override bit

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Table 14. Channel Registers, 0 to 1F (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
B	7	0	RW	Y	RESERVED	
	6	1	RW	Y	RESERVED	
	5	1	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	1	RW	Y	RESERVED	
	2	1	RW	Y	RESERVED	
	1	1	RW	Y	RESERVED	
	0	1	RW	Y	RESERVED	
C	7:4	0	RW	N	STATUS_CONTROL	These bits repurpose channel register 0x02 to report different status signals
	3	1	RW	Y	SINGLE_BIT_LIMIT_CHECK_ON	1: Normal operation, device checks for single bit transitions as a gate to achieving CDR lock
	2	0	RW	N	RESERVED	
	1	0	RW	Y	EN_IDAC_FD_CP3	Frequency detector charge pump setting bit 3 (MSB) LSB located in channel register 0x1C
	0	0	RW	Y	EN_IDAC_PD_CP3	Phase detector charge pump setting bit 3 (MSB) LSB located in channel register 0x1C
D	7	1	RW	N	DES_PD	1: Deserializer is powered down 0: Deserializer is enabled
	6	0	RW	N	RESERVED	
	5	1	RW	Y	DRV_SEL_VOD4	Used in conjunction with 0x2D[2:0] to control the VOD levels of the high speed drivers
	4	1	RW	Y	DRV_SEL_VOD3	
	3	0	RW	Y	FIR_RLOAD_MAX	
	2	1	RW	Y	FIR_SEL_NEG_GM	
	1:0	0	RW	N	RESERVED	
E	7:0	0x93	RW	N	RESERVED	
F	7:0	0x69	RW	N	RESERVED	
10	7:0	0x3A	RW	Y	RESERVED	

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Table 14. Channel Registers, 0 to 1F (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
11	7	0	RW	Y	EOM_SEL_VRANGE1	Manually set the EOM vertical range, used with channel register 0x2C[6] 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE1	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	SD_SEL_MUTEZ	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	
13	7	1	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	N	RESERVED	
	4	1	RW	Y	EQ_EN_DC_OFF	1: Normal operation
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	EQ_LIMIT_EN	1: Configures the final stage of the equalizer to be a limiting stage. 0: Normal operation, final stage of the equalizer is configured to be a linear stage.
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Table 14. Channel Registers, 0 to 1F (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
14	7	0	RW	Y	EQ_SD_PRESET	1: Forces signal detect HIGH, and force enables the channel. Should not be set if bit 6 is set. 0: Normal Operation.
	6	0	RW	Y	EQ_SD_RESET	1: Forces signal detect LOW and force disables the channel. Should not be set if bit 7 is set. 0: Normal Operation.
	5	0	RW	Y	EQ_REFA_SEL1	Controls the signal detect assert levels.
	4	0	RW	Y	EQ_REFA_SEL0	
	3	0	RW	Y	EQ_REFD_SEL1	Controls the signal detect de-assert levels.
	2	0	RW	Y	EQ_REFD_SEL0	
	1:0	0	RW	N	RESERVED	
15	7	0	RW	Y	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	RESERVED	
	1	1	RW	Y	DRV_DEM1	Degenerates the pre-driver degeneration 00: 0 dB 01: 1 dB 10: 2 dB 11: 3 dB
	0	0	RW	Y	DRV_DEM0	
16	7:0	0x7A	RW	Y	RESERVED	
17	7:0	0x25	RW	Y	RESERVED	
18	7	0	RW	N	RESERVED	
	6	1	RW	Y	PDIQ_SEL_DIV2	These bits will force the divider setting if 0x09[2] is set. 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 All other values are reserved.
	5	0	RW	Y	PDIQ_SEL_DIV1	
	4	0	RW	Y	PDIQ_SEL_DIV0	
	3	0	RW	N	RESERVED	
	2	0	RW	N	DRV_PD_R_EN	1: Enables the shut down termination resistor to be present when the driver is powered down with channel register 0x15[3] 0: Normal operation, resistor is disconnected from output for propper driver operation
	1:0	0	RW	N	RESERVED	
19	7:6	0x20	RW	N	RESERVED	
	5:0		RW	Y	RESERVED	
1A	7:4	0xA	RW	Y	RESERVED	
	3	0	RW	Y	DRV_SEL_VCM1	This feature is reserved for future use.
	2	0	RW	Y	DRV_SEL_VCM0	
	1:0	0	RW	N	RESERVED	

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Table 14. Channel Registers, 0 to 1F (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
1B	7:2	0	RW	N	RESERVED	
	1	1	RW	Y	CP_EN_CP_PD	1: Normal operation
	0	1	RW	Y	CP_EN_CP_FD	1: Normal operation
1C	7	1	RW	Y	EN_IDAC_PD_CP2	Phase detector charge pump setting MSB located in channel register 0x0C[0] Override bit required for these bits to take effect
	6	0	RW	Y	EN_IDAC_PD_CP1	
	5	0	RW	Y	EN_IDAC_PD_CP0	
	4	1	RW	Y	EN_IDAC_FD_CP2	Frequency detector charge pump setting MSB located in channel register 0x0C[1] Override bit required for these bits to take effect
	3	0	RW	Y	EN_IDAC_FD_CP1	
	2	0	RW	Y	EN_IDAC_FD_CP0	
	1:0	0	RW	N	RESERVED	
1D	7	0	RW	Y	SBT_EN	SBT enable override 0: Normal operation
	6:0	0	RW	N	RESERVED	
1E	7	1	RW	Y	PFD_SEL_DATA_MUX2	For these values to take effect, register 0x09[5] must be set to 1. 000: Raw Data* 001: Retimed Data 100: Pattern Generator 111: Mute All other values are reserved. *Note in this mode the FIR filter will not function. Data is routed only through the pre cursor tap. See Functional Description section for more information.
	6	1	RW	Y	PFD_SEL_DATA_MUX1	
	5	1	RW	Y	PFD_SEL_DATA_MUX0	
	4	0	RW	N	SER_EN	1: Enables the serializer for pattern generation 0: Disables the serializer
	3	1	RW	Y	DFE_PD	This bit must be cleared for the DFE to be functional in any adapt mode. 0: DFE enabled 1: DFE disabled
	2	0	RW	Y	PFD_PD_PD	PFD phasee detector power down override
	1	0	RW	Y	PFD_EN_FLD	PFD enable FLD override
	0	1	RW	Y	PFD_EN_FD	PFD enable frequency detector override
1F	7:6	0x55	RW	Y	RESERVED	
	5:0		RW	Y	RESERVED	

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Table 15. Channel Registers, 20 to 39

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	
22	7	0	RW	N	EOM_OV	1: Override enable for EOM manual control 0: Normal operation
	6	0	RW	N	EOM_SEL_RATE_OV	1: Override enable for EOM rate selection 0: Normal operation
	5:0	0	RW	N	RESERVED	
23	7	0	RW	N	EOM_GET_HEO_VEO_OV	1: Override enable for manual control of the HEO/VEO trigger 0: Normal operation
	6	1	RW	Y	DFE_OV	1: Normal operation, DFE must be enabled in channel register 0x1E[3]
	5:0	0	RW	N	RESERVED	

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
24	7	0	RW	N	FAST_EOM	1: Enables fast EOM mode for fully eye capture. In this mode the phase DAC and voltage DAC of the EOM are automatically incremented through a 64 x 64 matrix. Values for each point are stored in channel registers 25 and 26.
	6	0	R	N	DFE_EQ_ERROR_NO_LOCK	DFE/CTLE SM quit due to loss of lock
	5	0	R	N	GET_HEO_VEO_ERROR_ NO_HITS	GET_HEO_VEO sees no hits at zero crossing
	4	0	R	N	GET_HEO_VEO_ERROR_ NO_OPENING	GET_HEO_VEO cannot see a vertical eye opening
	3	0	RW	N	RESERVED	
	2	0	RWSC	N	DFE_ADAPT	1: Manually start DFE adaption, self clearing. 0: Normal operation
	1	0	RWSC	N	EOM_GET_HEO_VEO	1: Manually triggers a HEO/VEO measurement. Must be enabled with channel register 0x23[7].
	0	0	RWSC	N	EOM_START	1: Starts EOM counter, self clearing
25	7	0	R	N	EOM_COUNT15	MSBs of EOM counter
	6	0	R	N	EOM_COUNT14	
	5	0	R	N	EOM_COUNT13	
	4	0	R	N	EOM_COUNT12	
	3	0	R	N	EOM_COUNT11	
	2	0	R	N	EOM_COUNT10	
	1	0	R	N	EOM_COUNT9	
	0	0	R	N	EOM_COUNT8	
26	7	0	R	N	EOM_COUNT7	LSBs of EOM counter
	6	0	R	N	EOM_COUNT6	
	5	0	R	N	EOM_COUNT5	
	4	0	R	N	EOM_COUNT4	
	3	0	R	N	EOM_COUNT3	
	2	0	R	N	EOM_COUNT2	
	1	0	R	N	EOM_COUNT1	
	0	0	R	N	EOM_COUNT0	
27	7	0	R	N	HEO7	HEO value, requires CDR to be locked for valid measurement
	6	0	R	N	HEO6	
	5	0	R	N	HEO5	
	4	0	R	N	HEO4	
	3	0	R	N	HEO3	
	2	0	R	N	HEO2	
	1	0	R	N	HEO1	
	0	0	R	N	HEO0	

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
28	7	0	R	N	VEO7	VEO value, requires CDR to be locked for valid measurement
	6	0	R	N	VEO6	
	5	0	R	N	VEO5	
	4	0	R	N	VEO4	
	3	0	R	N	VEO3	
	2	0	R	N	VEO2	
	1	0	R	N	VEO1	
	0	0	R	N	VEO0	
29	7	0	RW	N	RESERVED	
	6	0	R	N	EOM_VRANGE_SETTING1	Use these bits to read back the EOM voltage range setting 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	5	0	R	N	EOM_VRANGE_SETTING0	
	4	0	RW	N	EN_FOM_RESET	1: Enables resetting the FOM before issuing a manual adaption
	3	0	RW	N	VEO_MIN_HITS_1	These bits set the number of hits for a particular phase and voltage location in the EOM before the EOM will indicate a hit has occured. This filtering only affects the VEO measurement. Filter thresholds: 00: 0 hits 01: 15 hits 10, 11: 255 hits
	2	0	RW	N	VEO_MIN_HITS_0	
	1:0	0	RW	N	RESERVED	
2A	7	0	RW	Y	EOM_TIMER_THR7	Controls the amount of time the EOM samples each point in the eye for. The total counter bit width is 16-bits, this register is the upper 8-bits. The counter counts in 32-bit words, therefore, the total number of bits counted is 32 times this value.
	6	0	RW	Y	EOM_TIMER_THR6	
	5	1	RW	Y	EOM_TIMER_THR5	
	4	1	RW	Y	EOM_TIMER_THR4	
	3	0	RW	Y	EOM_TIMER_THR3	
	2	0	RW	Y	EOM_TIMER_THR2	
	1	0	RW	Y	EOM_TIMER_THR1	
	0	0	RW	Y	EOM_TIMER_THR0	
2B	7:6	0	RW	N	RESERVED	
	5:4	0	RW	Y	RESERVED	
	3	1	RW	Y	EOM_MIN_REQ_HITS3	These bits set the number of hits for a particular phase and voltage location in the EOM before the EOM will indicate a hit has occured. This filtering only affects the HEO measurement. Filter threshold ranges from 0 to 15 hits.
	2	1	RW	Y	EOM_MIN_REQ_HITS2	
	1	1	RW	Y	EOM_MIN_REQ_HITS1	
	0	1	RW	Y	EOM_MIN_REQ_HITS0	

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
2C	7	1	RW	N	RELOAD_DFE_TAPS	1: Reload DFE taps from last adapted value
	6	1	RW	Y	VEO_SCALE	1: Scale VEO based on EOM vertical range 0: Manual control of vertical range
	5	1	RW	Y	DFE_SM_FOM1	00: not valid 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO
	4	1	RW	Y	DFE_SM_FOM0	
	3	0	RW	Y	DFE_ADAPT_COUNTER3	DFE look-beyond count.
	2	0	RW	Y	DFE_ADAPT_COUNTER2	
	1	1	RW	Y	DFE_ADAPT_COUNTER1	
	0	0	RW	Y	DFE_ADAPT_COUNTER0	
2D	7	0	RW	Y	PD_SCP	1: Power down the short circuit protection for the high speed driver outputs 0: Normal operation, short circuit protection is enabled for the high speed driver outputs
	6	0	RW	Y	SD_EN_FAST_OOB	Feature is reserved for future use.
	5	0	RW	Y	SD_REF_HIGH	Feature is reserved for future use.
	4	0	RW	Y	SD_GAIN	Feature is reserved for future use.
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	1	RW	Y	DRV_SEL_VOD2	Used in conjunction with 0x0D[5:4] to control the VOD levels of the high speed drivers
	1	1	RW	Y	DRV_SEL_VOD1	
	0	1	RW	Y	DRV_SEL_VOD0	
2E	7:0	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. 0x6: 11.5 Gbps 0x7: 12.5, 6.5, 3.125 Gbps 0x8: 9.8304, 4.9152, 2.4576 Gbps 0x9: 6.144, 3.072 Gbps 0xA: 10, 5, 2.5 Gbps 0xB: 10.3125, 1.25
	6	0	RW	Y	RATE0	
	5	1	RW	Y	SUBRATE1	
	4	1	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	1: False lock detector is used as a qualifier when performing lock detect
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self clearing

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
30	7	0	RW	N	FREEZE_PPM_CNT	1: Freeze PPM counter to allow safe read asynchronously
	6	0	RW	Y	EQ_SEARCH_OV_EN	Enables the EQ search bit to be force by channel register 0x13[2]
	5	0	RW	N	EN_PATT_INV	1: Enables automatic pattern inversion of successive 16-bit words when using the user defined pattern generator option.
	4	0	RW	N	RELOAD_PRBS_CHKR	Feature is reserved for future use.
	3	0	RW	N	PRBS_EN_DIG_CLK	This bit enables the clock to operate the PRBS generator and/or the PRBS checker. Toggling this bit is the primary method to reset the PRBS pattern generator and PRBS checker.
	2	0	RW	N	PRBS_PROGPATT_EN	1: Enable a fixed user defined pattern. Requires that the pattern generator be configured properly to be enabled
	1	0	RW	N	PRBS_PATTERN_SEL1	Selects the PRBS generator pattern to output. Requires that the pattern generator be configured properly. 00: PRBS-7 01: PRBS-9 10: PRBS-15 11: PRBS-31
	0	0	RW	N	PRBS_PATTERN_SEL0	
31	7	0	RW	N	PRBS_INT_EN	1: Enables interrupt for detection of PRBS errors. The PRBS checker must be properly configured for this feature to work
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until HEO/VEO threshold in reg 0x33 are met, then DFE, then EQ until optimal
	5	0	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	Sets the desired FoM for EQ adaption 00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	CDR_LOCK_LOSS_INT_EN	1: enables loss of CDR lock interrupt
	0	0	RW	N	SIG_DET_LOSS_INT_EN	1: enable loss of signal detect interrupt

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
32	7	0	RW	Y	HEO_INT_THRESH3	These bits set the threshold for the HEO and VEO interrupt. Each threshold bit represents 8 counts of HEO or VEO.
	6	0	RW	Y	HEO_INT_THRESH2	
	5	0	RW	Y	HEO_INT_THRESH1	
	4	1	RW	Y	HEO_INT_THRESH0	
	3	0	RW	Y	VEO_INT_THRESH3	
	2	0	RW	Y	VEO_INT_THRESH2	
	1	0	RW	Y	VEO_INT_THRESH1	
	0	1	RW	Y	VEO_INT_THRESH0	
33	7	1	RW	Y	HEO_THRESH3	In adapt mode 3, this register sets the minimum HEO and VEO required for CTLE adaption, before starting DFE adaption. This can be a max of 15
	6	0	RW	Y	HEO_THRESH2	
	5	0	RW	Y	HEO_THRESH1	
	4	0	RW	Y	HEO_THRESH0	
	3	1	RW	Y	VEO_THRESH3	
	2	0	RW	Y	VEO_THRESH2	
	1	0	RW	Y	VEO_THRESH1	
	0	0	RW	Y	VEO_THRESH0	
34	7	0	RW	N	PPM_ERR_RDY	1: Indicates that a PPM error count is read to be read from channel register 0x3B and 0x3C
	6	0	RW	Y	LOW_POWER_MODE_DISABLE	By default, all blocks (except signal detect) power down after 100ms after signal detect goes low.
	5	1	RW	Y	LOCK_COUNTER1	After achieving lock, the CDR continues to monitor the lock criteria.If the lock criteria fail, the lock is checked for a total of N number of times before declaring an out of lock condition, where N is set by this the value in these registers, with a max value of +3, for a total of 4. If during the N lock checks, lock is regained, then the lock condition is left HI, and the counter is reset back to zero.
	4	1	RW	Y	LOCK_COUNTER0	
	3	1	RW	Y	DFE_MAX_TAP2_5[3]	These 4 bits are used to set the maximum value by which DFE taps 2-5 are able to adapt with each subsequent adaptation. Same used for both polarities.
	2	1	RW	Y	DFE_MAX_TAP2_5[2]	
	1	1	RW	Y	DFE_MAX_TAP2_5[1]	
	0	1	RW	Y	DFE_MAX_TAP2_5[0]	

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
35	7	0	RW	Y	DATA_LOCK_PPM1	Modifies the value of the ppm delta tolerance from channel register 0x64 00 - ppm_delta[7:0] =1 x ppm_delta[7:0] 01 - ppm_delta[7:0] =1 x ppm_delta[7:0] + ppm_delta[3:1] 10 - ppm_delta[7:0] =2 x ppm_delta[7:0] 11 - ppm_delta[7:0] =2 x ppm_delta[7:0] + ppm_delta[3:1]
	6	0	RW	Y	DATA_LOCK_PPM0	
	5	0	RW	N	GET_PPM_ERROR	Get ppm error from ppm_count - clears when done. Normally updates continuously, but can be manually triggered with read value from channel register 0x3B and 0x3C
	4	1	RW	Y	DFE_MAX_TAP1[4]	Determines max tap limit for DFE tap 1
	3	1	RW	Y	DFE_MAX_TAP1[3]	
	2	1	RW	Y	DFE_MAX_TAP1[2]	
	1	1	RW	Y	DFE_MAX_TAP1[1]	
	0	1	RW	Y	DFE_MAX_TAP1[0]	
36	7	0	RW	N	UNCORR_ERR_INT_EN	Feature is reserved for future use.
	6	0	RW	N	HEO_VEO_INT_EN	1: Enable HEO/VEO interrupt capability
	5	1	RW	Y	REF_MODE1	11: Fast_lock all cap dac ref clock enabled (recommended) 10: Reserved 01: Reserved 00: referenceless all cap dac, for debug use only
	4	1	RW	Y	REF_MODE0	
	3	0	RW	Y	EN_6466B_LOCK_GATE	Feautre is reserved for future use.
	2	0	RW	Y	CDR_CAP_DAC_RNG_OV	Override enable for cap dac range
	1	0	RW	N	EN_6466B_RESTART	Feature is reserved for future use.
	0	0	RW	N	K28P5_6466_INT_EN	Feature is reserved for future use.
37	7	0	R	N	CTLE_STATUS7	Feature is reserved for future use.
	6	0	R	N	CTLE_STATUS6	
	5	0	R	N	CTLE_STATUS5	
	4	0	R	N	CTLE_STATUS4	
	3	0	R	N	CTLE_STATUS3	
	2	0	R	N	CTLE_STATUS2	
	1	0	R	N	CTLE_STATUS1	
	0	0	R	N	CTLE_STATUS0	

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Table 15. Channel Registers, 20 to 39 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
38	7	0	R	N	DFE_STATUS7	Feature is reserved for future use.
	6	0	R	N	DFE_STATUS6	
	5	0	R	N	DFE_STATUS5	
	4	0	R	N	DFE_STATUS4	
	3	0	R	N	DFE_STATUS3	
	2	0	R	N	DFE_STATUS2	
	1	0	R	N	DFE_STATUS1	
	0	0	R	N	DFE_STATUS0	
39	7	0	RW	N	PRELOCK_COMPARATOR_ ABRT_MODE	Feature is reserved for future use.
	6	0	RW	Y	EOM_RATE1	With eom_ov=1, these bits control the Eye Monitor Rate. 11: Use for Full Rate, Fastest 10 : Use for 1/2 Rate 01: Use for 1/4 Rate 00: Use for 1/8 Rate, Slowest
	5	0	RW	Y	EOM_RATE0	
	4	0	RW	Y	START_INDEX4	Start index for EQ adaptation
	3	0	RW	Y	START_INDEX3	
	2	0	RW	Y	START_INDEX2	
	1	0	RW	Y	START_INDEX1	
	0	0	RW	Y	START_INDEX0	

Table 16. Channel Registers, 3A to 59

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
3A	7	0	RW	Y	FIXED_EQ_BST0[1]	During adaptation, if the divider setting is >2, then a fixed EQ setting from this register will be used. However, if channel register 0x6F[7] is enabled, then an EQ adaptation will be performed instead.
	6	0	RW	Y	FIXED_EQ_BST0[0]	
	5	0	RW	Y	FIXED_EQ_BST1[1]	
	4	0	RW	Y	FIXED_EQ_BST1[0]	
	3	0	RW	Y	FIXED_EQ_BST2[1]	
	2	0	RW	Y	FIXED_EQ_BST2[0]	
	1	0	RW	Y	FIXED_EQ_BST3[1]	
	0	0	RW	Y	FIXED_EQ_BST3[0]	
3B	7	0	R	N	PPM_COUNT15	PPM count MSB
	6	0	R	N	PPM_COUNT14	
	5	0	R	N	PPM_COUNT13	
	4	0	R	N	PPM_COUNT12	
	3	0	R	N	PPM_COUNT11	
	2	0	R	N	PPM_COUNT10	
	1	0	R	N	PPM_COUNT9	
	0	0	R	N	PPM_COUNT8	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
3C	7	0	R	N	PPM_COUNT7	PPM count LSB
	6	0	R	N	PPM_COUNT6	
	5	0	R	N	PPM_COUNT5	
	4	0	R	N	PPM_COUNT4	
	3	0	R	N	PPM_COUNT3	
	2	0	R	N	PPM_COUNT2	
	1	0	R	N	PPM_COUNT1	
	0	0	R	N	PPM_COUNT0	
3D	7	0	RW	Y	FIR_PD_pd	
	6	0	RW	Y	FIR_C0_SGN	FIR main cursor polarity 1: negative 0: positive
	5	1	RW	Y	FIR_C0[5]	FIR main cursor setting
	4	1	RW	Y	FIR_C0[4]	
	3	0	RW	Y	FIR_C0[3]	
	2	1	RW	Y	FIR_C0[2]	
	1	0	RW	Y	FIR_C0[1]	
	0	1	RW	Y	FIR_C0[0]	
3E	7	0	RW	Y	FIR_PD_TX	
	6	1	RW	Y	FIR_CN1_SGN	FIR pre cursor polarity 1: negative 0: positive
	5	0	RW	Y	FIR_CN1[5]	FIR pre cursor setting
	4	0	RW	Y	FIR_CN1[4]	
	3	0	RW	Y	FIR_CN1[3]	
	2	0	RW	Y	FIR_CN1[2]	
	1	1	RW	Y	FIR_CN1[1]	
	0	1	RW	Y	FIR_CN1[0]	
3F	7	1	RW	Y	FIR_SEL_I_MAX	
	6	1	RW	Y	FIR_CP1_SGN	FIR post cursor polarity 1: negative 0: positive
	5	0	RW	Y	FIR_CP1[5]	FIR post cursor setting
	4	0	RW	Y	FIR_CP1[4]	
	3	0	RW	Y	FIR_CP1[3]	
	2	1	RW	Y	FIR_CP1[2]	
	1	1	RW	Y	FIR_CP1[1]	
	0	1	RW	Y	FIR_CP1[0]	
40	7	0	RW	Y	EQ_ARRAY_INDEX_0_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_0_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_0_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_0_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_0_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_0_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_0_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_0_BST3[0]	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
41	7	0	RW	Y	EQ_ARRAY_INDEX_1_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_1_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_1_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_1_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_1_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_1_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_1_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_1_BST3[0]	
42	7	0	RW	Y	EQ_ARRAY_INDEX_2_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_2_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_2_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_2_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_2_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_2_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_2_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_2_BST3[0]	
43	7	0	RW	Y	EQ_ARRAY_INDEX_3_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_3_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_3_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_3_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_3_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_3_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_3_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_3_BST3[0]	
44	7	0	RW	Y	EQ_ARRAY_INDEX_4_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_4_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_4_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_4_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_4_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_4_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_4_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_4_BST3[0]	
45	7	0	RW	Y	EQ_ARRAY_INDEX_5_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_5_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_5_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_5_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_5_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_5_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_5_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_5_BST3[0]	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
46	7	0	RW	Y	EQ_ARRAY_INDEX_6_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_6_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_6_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_6_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_6_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_6_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_6_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_6_BST3[0]	
47	7	1	RW	Y	EQ_ARRAY_INDEX_7_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_7_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_7_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_7_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_7_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_7_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_7_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_7_BST3[0]	
48	7	0	RW	Y	EQ_ARRAY_INDEX_8_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_8_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_8_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_8_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_8_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_8_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_8_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_8_BST3[0]	
49	7	0	RW	Y	EQ_ARRAY_INDEX_9_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_9_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_9_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_9_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_9_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_9_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_9_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_9_BST3[0]	
4A	7	0	RW	Y	EQ_ARRAY_INDEX_10_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_10_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_10_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_10_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_10_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_10_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_10_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_10_BST3[0]	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
4B	7	0	RW	Y	EQ_ARRAY_INDEX_11_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_11_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_11_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_11_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_11_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_11_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_11_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_11_BST3[0]	
4C	7	0	RW	Y	EQ_ARRAY_INDEX_12_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_12_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_12_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_12_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_12_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_12_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_12_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_12_BST3[0]	
4D	7	1	RW	Y	EQ_ARRAY_INDEX_13_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_13_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_13_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_13_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_13_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_13_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_13_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_13_BST3[0]	
4E	7	0	RW	Y	EQ_ARRAY_INDEX_14_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_14_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_14_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_14_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_14_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_14_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_14_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_14_BST3[0]	
4F	7	1	RW	Y	EQ_ARRAY_INDEX_15_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_15_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_15_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_15_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_15_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_15_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_15_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_15_BST3[0]	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
50	7	1	RW	Y	EQ_ARRAY_INDEX_16_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_16_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_16_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_16_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_16_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_16_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_16_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_16_BST3[0]	
51	7	1	RW	Y	EQ_ARRAY_INDEX_17_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_17_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_17_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_17_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_17_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_17_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_17_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_17_BST3[0]	
52	7	1	RW	Y	EQ_ARRAY_INDEX_18_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_18_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_18_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_18_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_18_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_18_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_18_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_18_BST3[0]	
53	7	0	RW	Y	EQ_ARRAY_INDEX_19_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_19_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_19_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_19_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_19_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_19_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_19_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_19_BST3[0]	
54	7	0	RW	Y	EQ_ARRAY_INDEX_20_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_20_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_20_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_20_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_20_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_20_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_20_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_20_BST3[0]	

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Table 16. Channel Registers, 3A to 59 (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
55	7	1	RW	Y	EQ_ARRAY_INDEX_21_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_21_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_21_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_21_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_21_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_21_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_21_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_21_BST3[0]	
56	7	1	RW	Y	EQ_ARRAY_INDEX_22_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_22_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_22_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_22_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_22_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_22_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_22_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_22_BST3[0]	
57	7	1	RW	Y	EQ_ARRAY_INDEX_23_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_23_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_23_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_23_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_23_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_23_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_23_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_23_BST3[0]	
58	7	0	RW	Y	EQ_ARRAY_INDEX_24_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_24_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_24_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_24_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_24_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_24_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_24_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_24_BST3[0]	
59	7	0	RW	Y	EQ_ARRAY_INDEX_25_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_25_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_25_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_25_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_25_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_25_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_25_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_25_BST3[0]	

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Table 17. Channel Registers, 5A to 9B

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
5A	7	0	RW	Y	EQ_ARRAY_INDEX_26_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_26_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_26_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_26_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_26_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_26_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_26_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_26_BST3[0]	
5B	7	0	RW	Y	EQ_ARRAY_INDEX_27_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_27_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_27_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_27_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_27_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_27_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_27_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_27_BST3[0]	
5C	7	1	RW	Y	EQ_ARRAY_INDEX_28_BST0[1]	
	6	1	RW	Y	EQ_ARRAY_INDEX_28_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_28_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_28_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_28_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_28_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_28_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_28_BST3[0]	
5D	7	1	RW	Y	EQ_ARRAY_INDEX_29_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_29_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_29_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_29_BST1[0]	
	3	1	RW	Y	EQ_ARRAY_INDEX_29_BST2[1]	
	2	0	RW	Y	EQ_ARRAY_INDEX_29_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_29_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_29_BST3[0]	
5E	7	1	RW	Y	EQ_ARRAY_INDEX_30_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_30_BST0[0]	
	5	0	RW	Y	EQ_ARRAY_INDEX_30_BST1[1]	
	4	1	RW	Y	EQ_ARRAY_INDEX_30_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_30_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_30_BST2[0]	
	1	1	RW	Y	EQ_ARRAY_INDEX_30_BST3[1]	
	0	0	RW	Y	EQ_ARRAY_INDEX_30_BST3[0]	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
5F	7	1	RW	Y	EQ_ARRAY_INDEX_31_BST0[1]	
	6	0	RW	Y	EQ_ARRAY_INDEX_31_BST0[0]	
	5	1	RW	Y	EQ_ARRAY_INDEX_31_BST1[1]	
	4	0	RW	Y	EQ_ARRAY_INDEX_31_BST1[0]	
	3	0	RW	Y	EQ_ARRAY_INDEX_31_BST2[1]	
	2	1	RW	Y	EQ_ARRAY_INDEX_31_BST2[0]	
	1	0	RW	Y	EQ_ARRAY_INDEX_31_BST3[1]	
	0	1	RW	Y	EQ_ARRAY_INDEX_31_BST3[0]	
60	7	0	RW	Y	GRP0_OV_CNT7	Group 0 count LSB
	6	0	RW	Y	GRP0_OV_CNT6	
	5	0	RW	Y	GRP0_OV_CNT5	
	4	0	RW	Y	GRP0_OV_CNT4	
	3	0	RW	Y	GRP0_OV_CNT3	
	2	0	RW	Y	GRP0_OV_CNT2	
	1	0	RW	Y	GRP0_OV_CNT1	
	0	0	RW	Y	GRP0_OV_CNT0	
61	7	0	RW	Y	CNT_DLTA_OV_0	Override enable for group 0 manual data rate selection
	6	0	RW	Y	GRP0_OV_CNT14	Group 0 count MSB
	5	0	RW	Y	GRP0_OV_CNT13	
	4	0	RW	Y	GRP0_OV_CNT12	
	3	0	RW	Y	GRP0_OV_CNT11	
	2	0	RW	Y	GRP0_OV_CNT10	
	1	0	RW	Y	GRP0_OV_CNT9	
	0	0	RW	Y	GRP0_OV_CNT8	
62	7	0	RW	Y	GRP1_OV_CNT7	Group 1 count LSB
	6	0	RW	Y	GRP1_OV_CNT6	
	5	0	RW	Y	GRP1_OV_CNT5	
	4	0	RW	Y	GRP1_OV_CNT4	
	3	0	RW	Y	GRP1_OV_CNT3	
	2	0	RW	Y	GRP1_OV_CNT2	
	1	0	RW	Y	GRP1_OV_CNT1	
	0	0	RW	Y	GRP1_OV_CNT0	
63	7	0	RW	Y	CNT_DLTA_OV_1	Override enable for group 1 manual data rate selection
	6	0	RW	Y	GRP1_OV_CNT14	Group 1 count MSB
	5	0	RW	Y	GRP1_OV_CNT13	
	4	0	RW	Y	GRP1_OV_CNT12	
	3	0	RW	Y	GRP1_OV_CNT11	
	2	0	RW	Y	GRP1_OV_CNT10	
	1	0	RW	Y	GRP1_OV_CNT9	
	0	0	RW	Y	GRP1_OV_CNT8	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
64	7	0	RW	Y	GRP0_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 0. Must also program channel register 0x67[7].
	6	0	RW	Y	GRP0_OV_DLTA2	
	5	0	RW	Y	GRP0_OV_DLTA1	
	4	0	RW	Y	GRP0_OV_DLTA0	
	3	0	RW	Y	GRP1_OV_DLTA3	Sets the PPM delta tolerance for the PPM counter lock check for group 1. Must also program channel register 0x67[6].
	2	0	RW	Y	GRP1_OV_DLTA2	
	1	0	RW	Y	GRP1_OV_DLTA1	
	0	0	RW	Y	GRP1_OV_DLTA0	
65	7:0	0	RW	N	RESERVED	
66	7:00	0	RW	N	RESERVED	
67	7	0	RW	Y	GRP0_OV_DLTA4	
	6	0	RW	Y	GRP1_OV_DLTA4	
	5	1	RW	Y	HV_LOCKMON_EN	1: Normal operation, HEO/VEO measurements are used for lock monitoring
	4:1	0	RW	N	RESERVED	
	0	0	RW	N	LOCKMON_FRC_EN	This feature is reserved for future use.
68	7:5	0	RW	N	RESERVED	
	4	0	RW	N	ADPT_FRC_EN	This feature is reserved for future use.
	3	0	RW	N	SCN_OBS_CTRL3	This feature is reserved for future use.
	2	0	RW	N	SCN_OBS_CTRL2	
	1	0	RW	N	SCN_OBS_CTRL1	
	0	0	RW	N	SCN_OBS_CTRL0	
69	7:5	0	RW	N	RESERVED	
	4	0	RW	N	CTLE_ADPT_FRC_EN	This feature is reserved for future use.
	3	1	RW	Y	HV_LCKMON_CNT_MS3	This feature is reserved for future use.
	2	0	RW	Y	HV_LCKMON_CNT_MS2	
	1	1	RW	Y	HV_LCKMON_CNT_MS1	
	0	0	RW	Y	HV_LCKMON_CNT_MS0	
6A	7	0	RW	Y	VEO_LCK_THRSH3	VEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO.
	6	0	RW	Y	VEO_LCK_THRSH2	
	5	1	RW	Y	VEO_LCK_THRSH1	
	4	0	RW	Y	VEO_LCK_THRSH0	
	3	0	RW	Y	HEO_LCK_THRSH3	HEO threshold to meet before lock is established. The LSB step size is 4 counts of HEO.
	2	0	RW	Y	HEO_LCK_THRSH2	
	1	1	RW	Y	HEO_LCK_THRSH1	
	0	0	RW	Y	HEO_LCK_THRSH0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
6B	7	0	RW	Y	FOM_A7	Alternate Figure of Merit variable A Max value for this register is 128, do not use the MSB
	6	1	RW	Y	FOM_A6	
	5	0	RW	Y	FOM_A5	
	4	0	RW	Y	FOM_A4	
	3	0	RW	Y	FOM_A3	
	2	0	RW	Y	FOM_A2	
	1	0	RW	Y	FOM_A1	
	0	0	RW	Y	FOM_A0	
6C	7	0	RW	Y	FOM_B7	HEO adjustment for Alternate FoM, variable B
	6	1	RW	Y	FOM_B6	
	5	0	RW	Y	FOM_B5	
	4	0	RW	Y	FOM_B4	
	3	0	RW	Y	FOM_B3	
	2	0	RW	Y	FOM_B2	
	1	0	RW	Y	FOM_B1	
	0	0	RW	Y	FOM_B0	
6D	7	0	RW	Y	FOM_C7	VEO adjustment for alternate FoM, variable C
	6	1	RW	Y	FOM_C6	
	5	0	RW	Y	FOM_C5	
	4	0	RW	Y	FOM_C4	
	3	0	RW	Y	FOM_C3	
	2	0	RW	Y	FOM_C2	
	1	0	RW	Y	FOM_C1	
	0	0	RW	Y	FOM_C0	
6E	7	0	RW	Y	EN_NEW_FOM_CTLE	1: CTLE adaption state machine will use the alternate FoM HEO_ALT = (HEO-B)*A*2 VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128 The Alternate FoM = (HEO-B)*A*2 + (VEO-C)*(1-A)*2
	6	0	RW	Y	EN_NEW_FOM_DFE	1: DFE adaption state machine will use the alternate FoM HEO_ALT = (HEO-B)*A*2 VEO_ALT = (VEO-C)*(1-A)*2 The values of A,B,C are set in channel register 0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128 The Alternate FoM = (HEO-B)*A*2 + (VEO-C)*(1-A)*2
	5:1	0	RW	N	RESERVED	
	0	0	RW	N	GET_HV_ST_FRC_EN	This feature is reserved for future use.

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
6F	7	0	RW	Y	EN_LOW_DIVSEL_EQ	1: EQ adaption will be performed for all divider settings 0: EQ adaption will only be performed for dividers of 1 and 2
	6:5	0	RW	Y	RESERVED	
	4:0	0	RW	N	RESERVED	
70	7:4	0	RW	N	RESERVED	
	3	0	RW	Y	RESERVED	
	2	0	RW	Y	EQ_LB_CNT2	CTLE look beyond count for adaption.
	1	1	RW	Y	EQ_LB_CNT1	
	0	1	RW	Y	EQ_LB_CNT0	
71	7	0	R	N	PRBS_INT	1: Indicates that a PRBS error has been detected. Requires the PRBS checker to be properly configured. This bit will stay set until it has been cleared by being read. This bit will clear after reading
	6	0	R	N	K28P5_6466_COND_MET_INT	This feature is reserved for future use.
	5	0	R	N	DFE_POL_1_OBS	Primary observation point for DFE tap 1 polarity
	4	0	R	N	DFE_WT1_OBS4	Primary observation point for DFE tap 1 weight
	3	0	R	N	DFE_WT1_OBS3	
	2	0	R	N	DFE_WT1_OBS2	
	1	0	R	N	DFE_WT1_OBS1	
	0	0	R	N	DFE_WT1_OBS0	
72	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_2_OBS	Primary observation point for DFE tap 2 polarity
	3	0	R	N	DFE_WT2_OBS3	Primary observation point for DFE tap 2 weight
	2	0	R	N	DFE_WT2_OBS2	
	1	0	R	N	DFE_WT2_OBS1	
	0	0	R	N	DFE_WT2_OBS0	
73	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_3_OBS	Primary observation point for DFE tap 3 polarity
	3	0	R	N	DFE_WT3_OBS3	Primary observation point for DFE tap 3 weight
	2	0	R	N	DFE_WT3_OBS2	
	1	0	R	N	DFE_WT3_OBS1	
	0	0	R	N	DFE_WT3_OBS0	
74	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_4_OBS	Primary observation point for DFE tap 4 polarity
	3	0	R	N	DFE_WT4_OBS3	Primary observation point for DFE tap 4 weight
	2	0	R	N	DFE_WT4_OBS2	
	1	0	R	N	DFE_WT4_OBS1	
	0	0	R	N	DFE_WT4_OBS0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
75	7:5	0	RW	N	RESERVED	
	4	0	R	N	DFE_POL_5_OBS	Primary observation point for DFE tap 5 polarity
	3	0	R	N	DFE_WT5_OBS3	Primary observation point for DFE tap 5 weight
	2	0	R	N	DFE_WT5_OBS2	
	1	0	R	N	DFE_WT5_OBS1	
	0	0	R	N	DFE_WT5_OBS0	
76	7	0	RW	Y	POST_LOCK_VEO_THR3	VEO threshold after lock is established. The LSB step size is 4 counts of VEO.
	6	0	RW	Y	POST_LOCK_VEO_THR2	
	5	1	RW	Y	POST_LOCK_VEO_THR1	
	4	0	RW	Y	POST_LOCK_VEO_THR0	
	3	0	RW	Y	POST_LOCK_HEO_THR3	HEO threshold after lock is established. The LSB step size is 4 counts of HEO.
	2	0	RW	Y	POST_LOCK_HEO_THR2	
	1	1	RW	Y	POST_LOCK_HEO_THR1	
	0	0	RW	Y	POST_LOCK_HEO_THR0	
77	7	0	RW	N	PRBS_GEN_POL_EN	This feature is reserved for future use. To invert the polarity of the PRBS data use the normal method of inverting of the sign bits for the FIR taps.
	6	0	RW	Y	CDR_CAP_DAC_START1[5]	This feature is reserved for future use
	5	0	RW	Y	CDR_CAP_DAC_START0[5]	
	4	1	RW	Y	POST_LOCK_SBTTHR4	SBT threshold after lock is established.
	3	1	RW	Y	POST_LOCK_SBTTHR3	
	2	0	RW	Y	POST_LOCK_SBTTHR2	
	1	1	RW	Y	POST_LOCK_SBTTHR1	
	0	0	RW	Y	POST_LOCK_SBTTHR0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
78	7	0	R	N	UNCORR_ERR_INT	This feature is reserved for future use.
	6	0	R	N	PRBS_LOCKUP_STATUS	This feature is reserved for future use.
	5	0	R	N	SD_STATUS	Primary observation point for signal detect status
	4	0	R	N	CDR_LOCK_STATUS	Primary observation point for CDR lock status
	3	0	R	N	CDR_LOCK_INT	Requires that channel register 0x79[1] be set. 1: Indicates CDR has achieved lock, lock goes from LOW to HIGH. This bit is cleared after reading. This bit will stay set until it has been cleared by reading.
	2	0	R	N	SD_INT	Requires that channel register 0x79[0] be set. 1: Indicates signal detect status has changed. This will trigger when signal detect goes from LOW to HIGH or HIGH to LOW. This bit is cleared after reading. This bit will stay set until it has been cleared by reading.
	1	0	R	N	EOM_VRANGE_LIMIT_ERROR	This feature is reserved for future use.
	0	0	R	N	HEO_VEO_INT	Requires that channel register 0x36[6] be set. 1: Indicates that HEO/VEO dropped below the limits set in channel register 0x76 This bit is cleared after reading. This bit will stay set until it has been cleared by reading.

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
79	7	0	R	N	PWDN_SD	This feature is reserved for future use.
	6	0	R	N	PRBS_CHKR_EN	1: Enable the PRBS checker. 0: Disable the PRBS checker
	5	0	R	N	PRBS_GEN_EN	1: Enable the pattern generator 0: Disable the pattern generator
	4	1	RW	N	PRBS_LCKUP_EXIT_EN	This feature is reserved for future use.
	3	0	R	Y	EN_K285	1: Enables K28.5 checking as a requirement for lock 0: Normal operation
	2	0	R	Y	CAL_OVERRIDE	This feature is reserved for future use.
	1	0	R	N	CDR_LOCK_INT_EN	1: Enable CDR lock interrupt, observable in channel register 0x78[3] 0: Disable CDR lock interrupt
	0	0	R	N	SD_INT_EN	1: Enable signal detect interrupt, observable in channel register 0x78[3] 0: Disable signal detect interrupt
7A	7	0	RW	N	SEL_A7	This feature is reserved for future use.
	6	0	RW	N	SEL_A6	
	5	0	RW	N	SEL_A5	
	4	0	RW	N	SEL_A4	
	3	0	RW	N	SEL_A3	
	2	0	RW	N	SEL_A2	
	1	0	RW	N	SEL_A1	
	0	0	RW	N	SEL_A0	
7B	7	0	RW	N	SEL_D7	This feature is reserved for future use.
	6	0	RW	N	SEL_D6	
	5	0	RW	N	SEL_D5	
	4	0	RW	N	SEL_D4	
	3	0	RW	N	SEL_D3	
	2	0	RW	N	SEL_D2	
	1	0	RW	N	SEL_D1	
	0	0	RW	N	SEL_D0	
7C	7	0	W	N	PRBS_FIXED7	Pattern generator user defined pattern LSB. MSB located at channel register 0x97.
	6	0	W	N	PRBS_FIXED6	
	5	0	W	N	PRBS_FIXED5	
	4	0	W	N	PRBS_FIXED4	
	3	0	W	N	PRBS_FIXED3	
	2	0	W	N	PRBS_FIXED2	
	1	0	W	N	PRBS_FIXED1	
	0	0	W	N	PRBS_FIXED0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
7D	7	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS3	Limit for HEO change before triggering a DFE adaption while continous DFE adaption is enabled.
	6	1	RW	Y	CONT_ADAPT_HEO_CHNG_THRS2	
	5	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS1	
	4	0	RW	Y	CONT_ADAPT_HEO_CHNG_THRS0	
	3	1	RW	Y	CONT_ADAPT_VEO_CHNG_THRS3	Limit for VEO change before triggering a DFE adaption while continous DFE adaption is enabled.
	2	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS2	
	1	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS1	
	0	0	RW	Y	CONT_ADAPT_VEO_CHNG_THRS0	
7E	7	0	RW	Y	CONT_ADPT_TAP_INCR3	Limit of allowable DFE tap weight change from the previous base point
	6	0	RW	Y	CONT_ADPT_TAP_INCR2	
	5	0	RW	Y	CONT_ADPT_TAP_INCR1	
	4	1	RW	Y	CONT_ADPT_TAP_INCR0	
	3	0	RW	Y	CONT_ADPT_FOM_CHNG_THRS3	This feature is reserved for future use.
	2	0	RW	Y	CONT_ADPT_FOM_CHNG_THRS2	
	1	1	RW	Y	CONT_ADPT_FOM_CHNG_THRS1	
	0	1	RW	Y	CONT_ADPT_FOM_CHNG_THRS0	
7F	7	0	RW	N	EN_OBS_ALT_FOM	1: Allows for alternate FoM calculation to be shown in channel registers 0x27, 0x28 and 0x29 instead of HEO and VEO
	6	0	RW	N	RESERVED	
	5	1	RW	Y	DIS_HV_CHK_FOR_CONT_ADAPT	1: Ignore HEO/VEO lock condition checks during continous adaption. Normal operation for continous DFE adaption
	4	1	RW	Y	EN_DFE_CONT_ADAPT	1: Continous DFE adaption is enabled 0: DFE adapts only during lock and then freezes
	3	1	RW	Y	CONT_ADPT_CMP_BOTH	1: If continous DFE adaption is enabled, a DFE adaption will trigger if either HEO or VEO degrades
	2	0	RW	Y	CONT_ADPT_COUNT2	Limit for number of weights the DFE can look ahead in continous adaption
	1	1	RW	Y	CONT_ADPT_COUNT1	
	0	0	RW	Y	CONT_ADPT_COUNT0	
80	7	0	R	N	HEO_CENTER7	This feature is reserved for future use.
	6	0	R	N	HEO_CENTER6	
	5	0	R	N	HEO_CENTER5	
	4	0	R	N	HEO_CENTER4	
	3	0	R	N	HEO_CENTER3	
	2	0	R	N	HEO_CENTER2	
	1	0	R	N	HEO_CENTER1	
	0	0	R	N	HEO_CENTER0	
81	7:0	0	R	N	RESERVED	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
82	7	0	RW	N	FREEZE_PRBS_CNTR	1: Freeze the PRBS bit and error counts to allow for read back 0: Normal operation. Both bit and error counters are allowed to increment if the PRBS checker is properly configured.
	6	0	RW	N	RST_PRBS_CNTS	1: Reset PRBS bit and error counts 0: Normal operation, counters are released from reset
	5	0	RW	N	RESERVED	
	4	0	RW	N	PRBS_PATT_OV	1: Override PRBS pattern auto detection. Forces the pattern checker to only lock onto the pattern defined in bits 3 and 2 of this register. 0: Normal operation, pattern checker will automatically detect the PRBS pattern
	3	0	RW	N	PRBS_PATT1	Usage is enabled with channel reg 0x82[4] Select PRBS pattern to be checked 00: PRBS-7 01: PRBS-9 10: PRBS-15 11: PRBS-31
	2	0	RW	N	PRBS_PATT0	
	1	0	RW	N	PRBS_POL_OV	1: Override PRBS pattern auto polarity detection. Forces the pattern checker to only lock onto the polarity defined in bit 0 of this register. 0: Normal operation, pattern checker will automatically detect the PRBS pattern polarity
	0	0	RW	N	PRBS_POL	Usage is enabled with channel register 0x82[1] 0: Forced polarity = true 1 - Forced polarity = inverted
83	7:3	0	R	N	RESERVED	
	2	0	R	N	PRBS_ERR_CNT10	PRBS error count MSB
	1	0	R	N	PRBS_ERR_CNT9	
	0	0	R	N	PRBS_ERR_CNT8	
84	7	0	R	N	PRBS_ERR_CNT7	PRBS error count LSB
	6	0	R	N	PRBS_ERR_CNT6	
	5	0	R	N	PRBS_ERR_CNT5	
	4	0	R	N	PRBS_ERR_CNT4	
	3	0	R	N	PRBS_ERR_CNT3	
	2	0	R	N	PRBS_ERR_CNT2	
	1	0	R	N	PRBS_ERR_CNT1	
	0	0	R	N	PRBS_ERR_CNT0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
85	7	0	R	N	RESERVED	
	6	0	R	N	PRBS_DATA_CNT46	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	5	0	R	N	PRBS_DATA_CNT45	
	4	0	R	N	PRBS_DATA_CNT44	
	3	0	R	N	PRBS_DATA_CNT43	
	2	0	R	N	PRBS_DATA_CNT42	
	1	0	R	N	PRBS_DATA_CNT41	
	0	0	R	N	PRBS_DATA_CNT40	
86	7	0	R	N	PRBS_DATA_CNT39	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	6	0	R	N	PRBS_DATA_CNT38	
	5	0	R	N	PRBS_DATA_CNT37	
	4	0	R	N	PRBS_DATA_CNT36	
	3	0	R	N	PRBS_DATA_CNT35	
	2	0	R	N	PRBS_DATA_CNT34	
	1	0	R	N	PRBS_DATA_CNT33	
	0	0	R	N	PRBS_DATA_CNT32	
87	7	0	R	N	PRBS_DATA_CNT31	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	6	0	R	N	PRBS_DATA_CNT30	
	5	0	R	N	PRBS_DATA_CNT29	
	4	0	R	N	PRBS_DATA_CNT28	
	3	0	R	N	PRBS_DATA_CNT27	
	2	0	R	N	PRBS_DATA_CNT26	
	1	0	R	N	PRBS_DATA_CNT25	
	0	0	R	N	PRBS_DATA_CNT24	
88	7	0	R	N	PRBS_DATA_CNT23	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	6	0	R	N	PRBS_DATA_CNT22	
	5	0	R	N	PRBS_DATA_CNT21	
	4	0	R	N	PRBS_DATA_CNT20	
	3	0	R	N	PRBS_DATA_CNT19	
	2	0	R	N	PRBS_DATA_CNT18	
	1	0	R	N	PRBS_DATA_CNT17	
	0	0	R	N	PRBS_DATA_CNT16	
89	7	0	R	N	PRBS_DATA_CNT15	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	6	0	R	N	PRBS_DATA_CNT14	
	5	0	R	N	PRBS_DATA_CNT13	
	4	0	R	N	PRBS_DATA_CNT12	
	3	0	R	N	PRBS_DATA_CNT11	
	2	0	R	N	PRBS_DATA_CNT10	
	1	0	R	N	PRBS_DATA_CNT9	
	0	0	R	N	PRBS_DATA_CNT8	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
8A	7	0	R	N	PRBS_DATA_CNT7	PRBS bit count, 47-bit word from channel registers 0x85 to 0x8A
	6	0	R	N	PRBS_DATA_CNT6	
	5	0	R	N	PRBS_DATA_CNT5	
	4	0	R	N	PRBS_DATA_CNT4	
	3	0	R	N	PRBS_DATA_CNT3	
	2	0	R	N	PRBS_DATA_CNT2	
	1	0	R	N	PRBS_DATA_CNT1	
	0	0	R	N	PRBS_DATA_CNT0	
8B	7	0	RW	N	UNCORR_ERR_PATT15	This feature is reserved for future use.
	6	0	RW	N	UNCORR_ERR_PATT14	
	5	0	RW	N	UNCORR_ERR_PATT13	
	4	0	RW	N	UNCORR_ERR_PATT12	
	3	0	RW	N	UNCORR_ERR_PATT11	
	2	0	RW	N	UNCORR_ERR_PATT10	
	1	0	RW	N	UNCORR_ERR_PATT9	
	0	0	RW	N	UNCORR_ERR_PATT8	
8C	7	0	RW	N	UNCORR_ERR_PATT7	This feature is reserved for future use.
	6	0	RW	N	UNCORR_ERR_PATT6	
	5	0	RW	N	UNCORR_ERR_PATT5	
	4	0	RW	N	UNCORR_ERR_PATT4	
	3	0	RW	N	UNCORR_ERR_PATT3	
	2	0	RW	N	UNCORR_ERR_PATT2	
	1	0	RW	N	UNCORR_ERR_PATT1	
	0	0	RW	N	UNCORR_ERR_PATT0	
8D	7	0	RW	N	RESERVED	
	6	0	RW	Y	EQ_EN_HR_MODE	Used with bit 2 to set Full rate, Mid rate or Half rate EQ bandwidth. Bit 6 is MSB. Bit 2 is LSB. 00: Full rate 01: Mid rate 11: Half rate
	5	0	RW	Y	PFD_EN_HR_MODE	
	4	0	RW	Y	DIV_EN_HR_MODE	
	3	0	RW	Y	DIV_EN_HR_MODE	
	2	1	RW	Y	EQ_EN_MR_MODE	Used with bit 6 to set Full rate, Mid rate or Half rate EQ bandwidth. Bit 6 is MSB. Bit 2 is LSB. 00: Full rate 01: Mid rate 10: Alternate mid rate 11: Half rate
	1	1	RW	Y	SD_DC_EN	This feature is reserved for future use.
	0	0	RW	Y	EQ_SEL_LOOP_OUT	This feature is reserved for future use.

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
8E	7	0	RW	N	SD_CAL_RESET_LV	This feature is reserved for future use.
	6	0	RW	N	SEL_DIV48_LV	Output reference clock selection 1: Selects reference clock from in channel digital 0: Selects reference clock from adjacent channel output
	5	0	RW	Y	EN_CLK_LOOPTHRU_LV	1: Enable the reference clock loop through mux
	4	1	RW	Y	FIR_SEL_EDGE2	Edge rate (slew rate) control
	3	1	RW	Y	FIR_SEL_EDGE1	
	2	1	RW	Y	FIR_SEL_EDGE0	
	1	0	RW	Y	DFE_SEL_GAIN1	VGA gain control
	0	0	RW	Y	DFE_SEL_GAIN0	
8F	7	0	R	N	EQ_BST_TO_ANA7	Primary observation point for the EQ boost setting.
	6	0	R	N	EQ_BST_TO_ANA6	
	5	0	R	N	EQ_BST_TO_ANA5	
	4	0	R	N	EQ_BST_TO_ANA4	
	3	0	R	N	EQ_BST_TO_ANA3	
	2	0	R	N	EQ_BST_TO_ANA2	
	1	0	R	N	EQ_BST_TO_ANA1	
	0	0	R	N	EQ_BST_TO_ANA0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
90	7	0	RW	Y	K28P5_COMPR_PERIOD3	Used when one of these modes are enabled, k28.5 lock check(channel register 0x79[5]), 64b66b lock check(channel register 0x36[3]), k28.5 or 64b66b Interrupt(register 0x36[0]) k28.5_compr_period defines period within which k28.5 is expected to be seen. Also used for expected frequency of 64B66B transitions The number of bits to check is equal to 2^(min_k28.5_reqd[11:0]) * 32 Enable K28.5 checking with reg_79[3]
	6	0	RW	Y	K28P5_COMPR_PERIOD2	
	5	0	RW	Y	K28P5_COMPR_PERIOD1	
	4	0	RW	Y	K28P5_COMPR_PERIOD0	
	3	0	RW	Y	MIN_K28P5_REQD11	Used when one of these modes are enabled, k28.5 lock check(channel register 0x79[5]), 64b66b lock check(channel register 0x36[3]), k28.5 or 64b66b Interrupt(register 0x36[0]) Channel register 0x90[3:0] together with channel register 0x91[7:0] defines number of k28.5+ patterns that need to be detected in the number of bits checked(set by channel register 0x90[7:4] Also used for expected frequency of 64B66B transitions Enable k28.5 checking with channel register 0x79[3]
	2	0	RW	Y	MIN_K28P5_REQD10	
	1	0	RW	Y	MIN_K28P5_REQD9	
	0	0	RW	Y	MIN_K28P5_REQD8	
91	7	0	RW	Y	MIN_K28P5_REQD7	See channel register 0x90[3:0]
	6	0	RW	Y	MIN_K28P5_REQD6	
	5	0	RW	Y	MIN_K28P5_REQD5	
	4	0	RW	Y	MIN_K28P5_REQD4	
	3	0	RW	Y	MIN_K28P5_REQD3	
	2	0	RW	Y	MIN_K28P5_REQD2	
	1	0	RW	Y	MIN_K28P5_REQD1	
	0	0	RW	Y	MIN_K28P5_REQD0	
92	7:0	0	RW	N	RESERVED	
93	7:0	0	RW	N	RESERVED	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
94	7	0	RW	N	DFE_EN	This feature is reserved for future use.
	6	0	RW	N	DFE_DIS	This feature is reserved for future use.
	5	0	RW	N	EOM_EN	This feature is reserved for future use.
	4	0	RW	N	EOM_DIS	This feature is reserved for future use.
	3	0	RW	N	DRV_EN	This feature is reserved for future use.
	2	0	RW	N	DRV_DIS	This feature is reserved for future use.
	1	0	RW	N	PEAK_DET_EN	This feature is reserved for future use.
	0	0	RW	N	PEAK_DET_DIS	This feature is reserved for future use.
95	7	0	RW	N	SD_EN	This feature is reserved for future use.
	6	0	RW	N	SD_DIS	This feature is reserved for future use.
	5	0	RW	N	DC_OFF_EN	This feature is reserved for future use.
	4	0	RW	N	DC_OFF_DIS	This feature is reserved for future use.
	3	0	RW	N	EQ_EN	This feature is reserved for future use.
	2	0	RW	N	EQ_DIS	This feature is reserved for future use.
	1	0	RW	N	COMP_EN	This feature is reserved for future use.
	0	0	RW	N	COMP_DIS	This feature is reserved for future use.

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
96	7	0	RW	N	RESERVED	
	6	0	RW	N	RESERVED	
	5	0	RW	Y	XPNT_SLAVE	Always configure this bit to be master. Master control is assigned by mux selection 1: Channel is a slave 0: Channel is a master (recommended)
	4	0	RW	Y	XPNT_EN	1: Cross Point is enabled 0: Cross Point is disabled
	3	0	RW	Y	EQ_BUFFER_EN[1]	Enable EQ output buffers: 00: Neither buffer in ON (not recommended) 01: Only local buffer is ON 10: Only multi-drive buffer is ON 11: Both buffers are ON
	2	1	RW	Y	EQ_BUFFER_EN[0]	
	1	0	RW	Y	EQ_DATA_MUX_IN[1]	Select EQ data and signal detect bus from one channel: 00: channel A 01: Channel B 10: Channel C 11: Channel D Channel A = 0,4,8,12 Channel B = 1,5,9,13 Channel C = 2,6,10,14 Channel D = 3,7,11,15
	0	0	RW	Y	EQ_DATA_MUX_IN[0]	
97	7	0	W	N	PRBS_FIXED15	Pattern generator user defined pattern MSB. LSB located at channel register 0x7C.
	6	0	W	N	PRBS_FIXED14	
	5	0	W	N	PRBS_FIXED13	
	4	0	W	N	PRBS_FIXED12	
	3	0	W	N	PRBS_FIXED11	
	2	0	W	N	PRBS_FIXED10	
	1	0	W	N	PRBS_FIXED9	
	0	0	W	N	PRBS_FIXED8	
98	7:6	0	RW	N	RESERVED	
	5:0	0x0C0	RW	Y	RESERVED	
99	7	0	RW	Y	DIVSEL_START1_OV	This feature is reserved for future use.
	6	0	RW	Y	DIVSEL_STOP1_OV	
	5	1	RW	Y	DIVSEL_START2	This feature is reserved for future use.
	4	1	RW	Y	DIVSEL_START1	
	3	1	RW	Y	DIVSEL_START0	
	2	1	RW	Y	DIVSEL_STOP2	This feature is reserved for future use.
	1	1	RW	Y	DIVSEL_STOP1	
	0	1	RW	Y	DIVSEL_STOP0	

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Table 17. Channel Registers, 5A to 9B (continued)

Address (Hex)	Bits	Default Value (Hex)	Mode	EEPROM	Field Name	Description
9A	7	0	RW	Y	DIVSEL_START0_OV	This feature is reserved for future use.
	6	0	RW	Y	DIVSEL_STOP0_OV	This feature is reserved for future use.
	5	1	RW	Y	DIVSEL_START0[2]	This feature is reserved for future use.
	4	1	RW	Y	DIVSEL_START0[1]	
	3	1	RW	Y	DIVSEL_START0[0]	
	2	1	RW	Y	DIVSEL_STOP0[2]	This feature is reserved for future use.
	1	1	RW	Y	DIVSEL_STOP0[1]	
	0	1	RW	Y	DIVSEL_STOP0[0]	
9B	7:3	0	RW	N	RESERVED	
	2	0	RW	Y	RESERVED	
	1	0	RW	Y	EQ_CTRL_MUX_IN[1]	Select EQ control bus from one channel: 00: channel A 01: Channel B 10: Channel C 11: Channel D Channel A = 0,4,8,12 Channel B = 1,5,9,13 Channel C = 2,6,10,14 Channel D = 3,7,11,15
	0	0	RW	Y	EQ_CTRL_MUX_IN[0]	

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS125DF1610 is a 16 channel retimer that support many different data rates and application spaces. The following sections describe the typical use cases and common implementation practices.

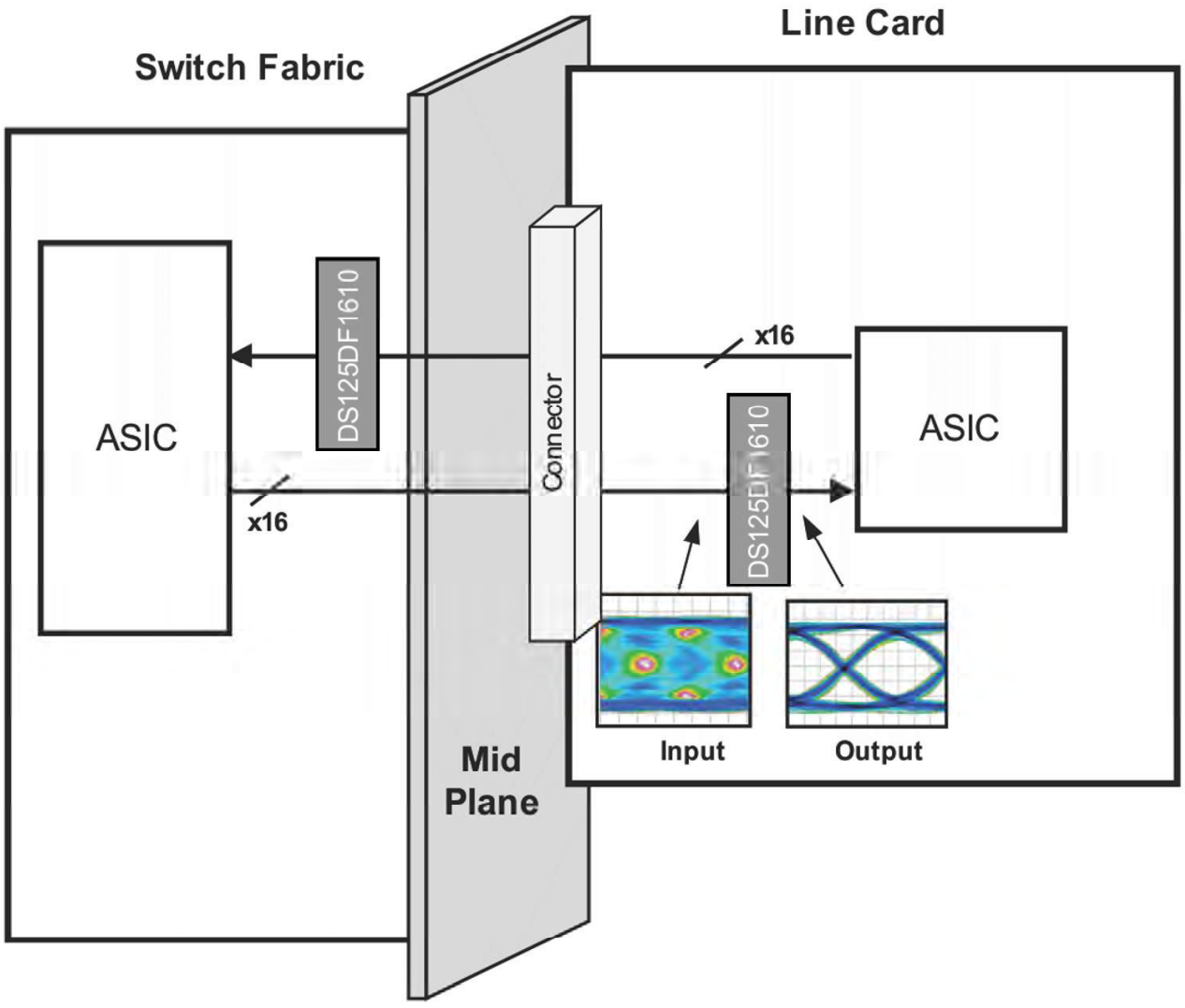


Figure 5. DS125DF1610 Example Application

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8.2 Typical Applications

Figure 5 shows a typical implementation for the DS125DF1610 in a back plane application. The DS125DF1610 can also be used for front port applications. The DS125DF1610 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates.

Figure 6 and Figure 7 show a typical application of the DS125DF1610. In these diagrams, the DS125DF1610 is configured for SMBus slave mode programming. Power is supplied to the device through a single 2.5 V plane. The power supply filtering shown in these diagrams may need to be adjusted to accommodate additional system power noise. The SMBus and LVCMOS signals in this example use 2.5 V logic. A differential reference clock for the digital block is applied to the device through 1 µF AC-coupling capacitors. In this example, the high speed signals are connected to the device in groups of four to allow for the system designer to make use of the 4x4 cross point switches. Note that since the device contains AC-coupling capacitors on the high speed receiver inputs, the signals can be directly connected to the device. The transmitter outputs of this device should connect to AC-coupling capacitors placed near the receive inputs of the receiving ASIC.

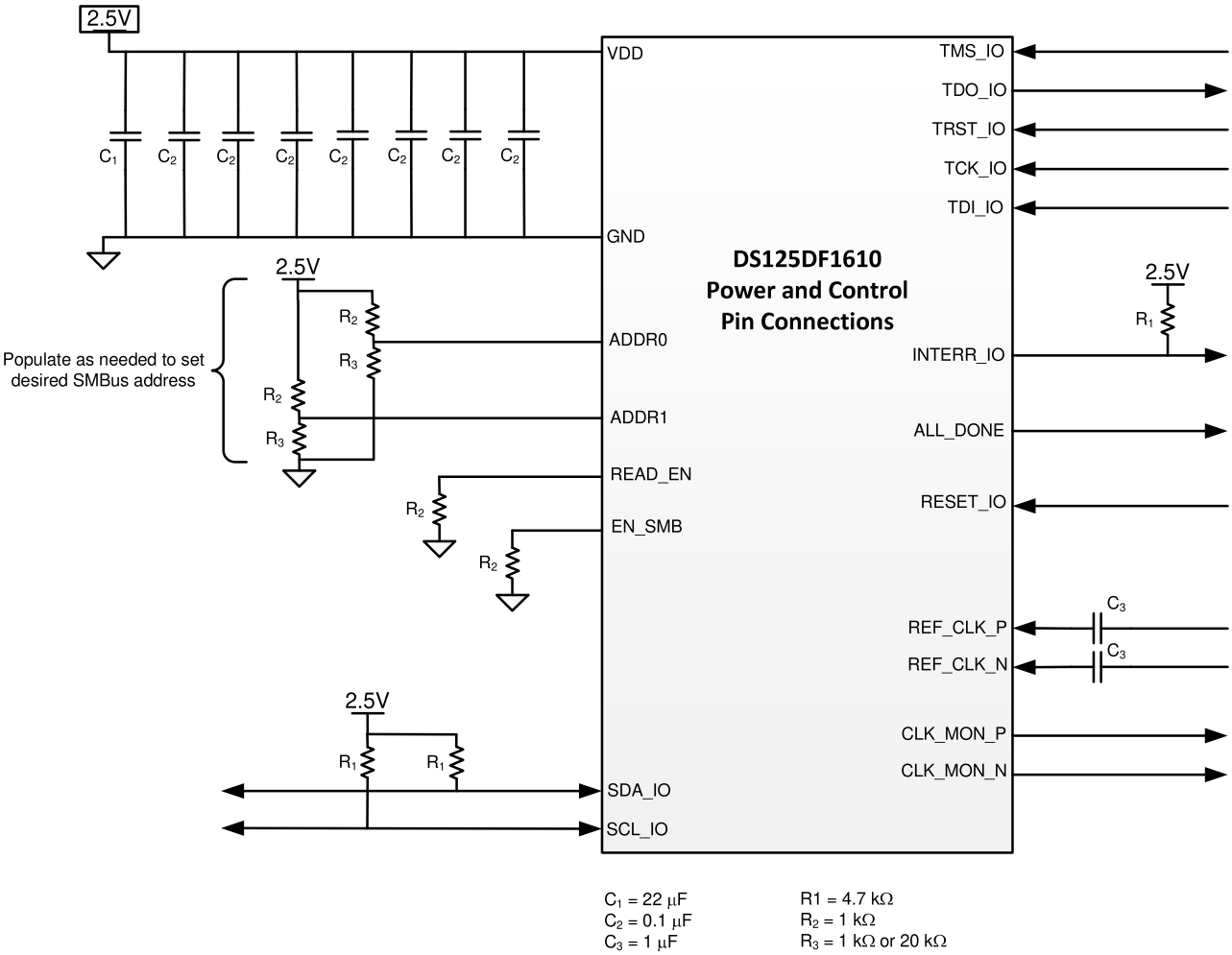


Figure 6. Typical Connection Diagram: Power and Control Pins

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Typical Applications (continued)

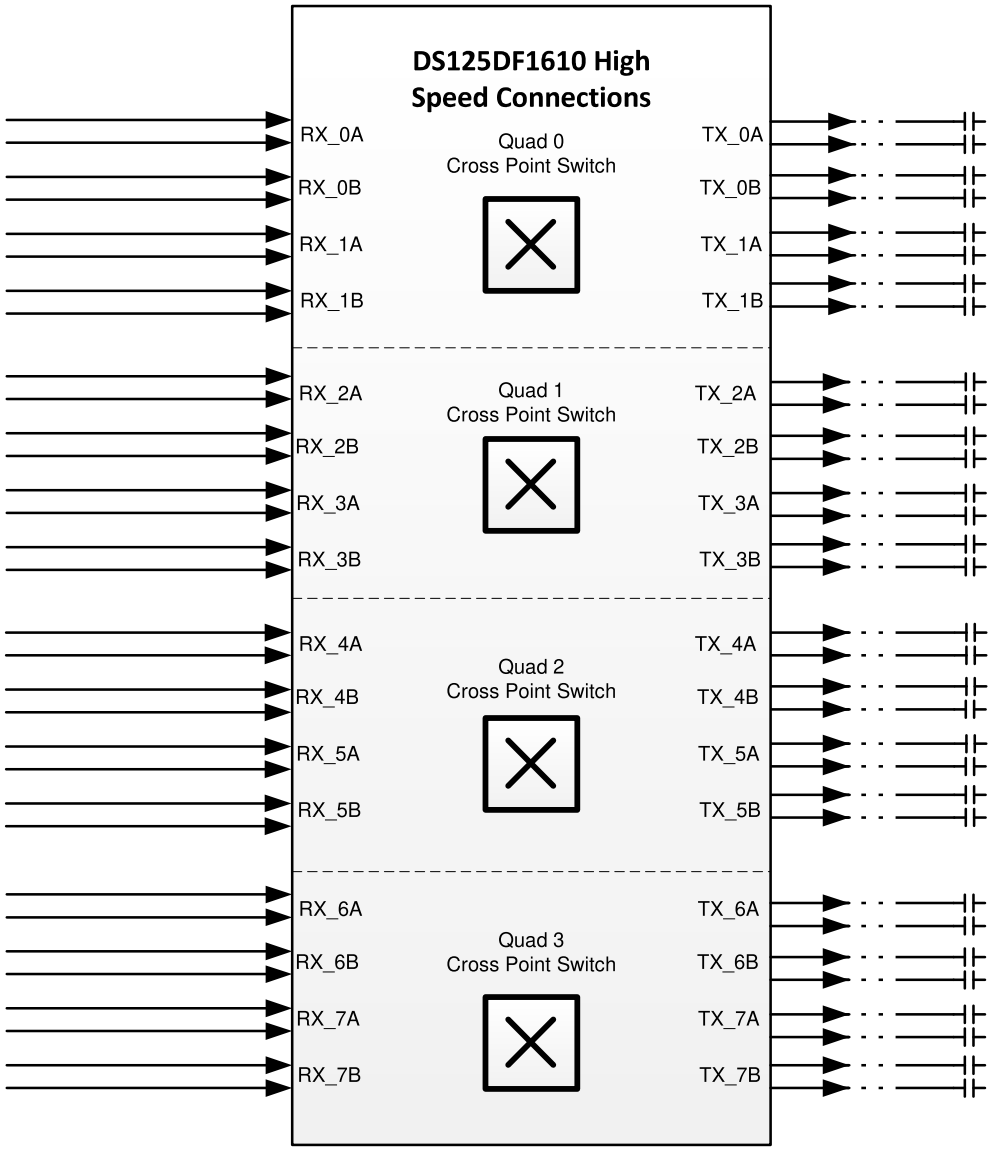


Figure 7. Typical Connection Diagram: High Speed Signals

8.2.1 Design Requirements

This section lists some critical areas for high speed printed circuit board design consideration and study.

- Utilize 100Ω differential impedance traces.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.
- Place AC-Coupling capacitors for the transmitter links near the receiver for that channel.
- The maximum body size for AC-coupling capacitors is 0402.

8.2.2 Detailed Design Procedure

To begin the design process determine the following:

- Maximum power draw for PCB regulator selection. For this calculation use the CDR locking power number

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Typical Applications (continued)

specified in the datasheet, multiplied by the number of channels allowed to lock at a time by the lock sequencer. Then add the static power. The lock sequencer defaults to 8 channels allowed to lock at a time. To ease the peak power draw, the lock sequencer can be set to allow for only 1 channel to lock at a time. The lock time for each channel is typically very short, so this power calculation should not be used for the thermal simulations of the PCB.

- Maximum operational power for thermal calculations. For this calculation use the CDR locked power numbers specified in the datasheet, multiplied by the number of channels that will be active in the device. Then add the static power. If it is desired to use the Pattern Generator or PRBS checker, add these powers per channel. Note that a channel's PRBS Checker and Pattern Generator cannot both be active at the same time. So the total count of active PRBS Checkers and Pattern Generators should not be more than 16 per device.
- Select a reference clock frequency and routing scheme.
- Plan out channel connectivity. Be sure to note any desired cross point routing in the board schematics.
- Ensure that each device has a unique SMBus address if the control bus is shared with other devices or components.
- Use the IBIS-AMI model for simple channel simulations before PCB layout is complete.
- Compare schematic against the typical connection diagrams in the datasheet, Figure 6 and Figure 7

8.2.3 Typical Application Performance Plots

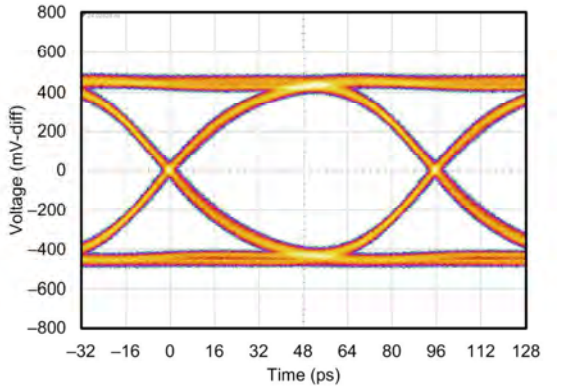


Figure 8. Typical Transmit Eye Diagram, 10.3125 Gbps

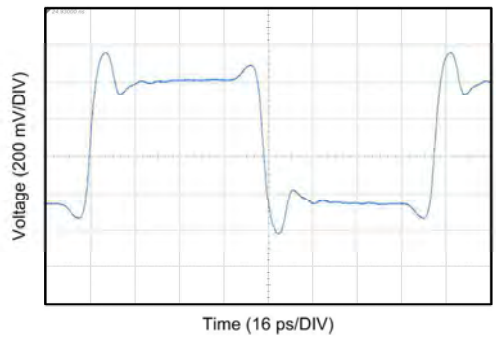


Figure 9. FIR Transmit Equalization Example, 10.3125Gbps

Figure 8 shows a typical output eye diagram for the DS125DF1610 operating at 10.3125 Gbps with the 1V_{PP} V_{OD} settings. All other device settings are left at default.

Figure 9 shows an example of FIR transmit equalization for a DS125DF1610 operating at 10.3125 Gbps. In this example, the high speed output is configured for 1V_{PP} V_{OD}. The FIR filter is then further adjusted such that the pre cursor tap is set to -5, the main cursor tap is set to +42, and the post cursor tap is set to -10. An 8T pattern is used to evaluate the FIR filter, which consists of 0xFF00. All other device settings are left at default.

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8.3 Initialization Setup

The typical device initialization sequence for a DS125DF1610 includes the following:

- Shared Register Configurations:
  - Reference Clock Divider Setting (default is 25MHz)
  - Lock Sequencer Configuration (default is 8 channels allowed lock concurrently)
- Channel Register Configurations repeated for all desired channels:
  - CDR reset
  - Adapt Mode Configuration
  - Data rate selection
  - Output driver VOD and FIR configuration
  - *Optional* Continuous DFE adaption configuration
  - *Optional* Interrupt enable
  - *Optional* Reference clock loop through enable
  - *Optional* Cross point switch configuration
  - CDR reset release

8.3.1 Data Rate Selection (Rate/Sub-Rate Table)

The data rates for the DS125DF1610 must be known and programmed into each desired channel. The DS125DF1610 will only lock to programmed data rates and the programmed divider settings. For ease of use several common data rates have been preprogrammed into the DS125DF1610 along with the associated sub-rates for those various standards. These rate/sub-rate settings comprise the Rate/Sub-rate Table 18. Note that each channel operates independently, so different channels in the DS125DF1610 can operate at different data rates at the same time.

The Rate/Sub-rate Table 18 for the DS125DF1610 shown below includes all of the available preprogrammed data rates and associated divider groupings.

Table 18. Rate/Sub-Rate Options

CHANNEL REGISTER 0x2F[7:4] SETTING	STANDARD	DATA RATES (Gbps)	FIRST GROUP DIVIDER SETTINGS	SECOND GROUP DIVIDER SETTINGS
0x6	Custom	11.5	1	1
0x7	Interlaken	12.5, 6.25, 3.125	1, 2, 4	1, 2, 4
0x8	CPRI 1	9.8304, 4.9152, 2.4576	1, 2, 4	1, 2, 4
0x9	CPRI 2	6.144, 3.072	2, 4	2, 4
0xA	Infiniband	10, 5, 2.5	1, 2, 4	1, 2, 4
0xB	Ethernet	10.3125, 1.25	8	1

8.3.2 Data Rate Selection (Manual Programming)

The DS125DF1610 is capable of supporting any data rate within the specified range of 9.8 Gbps to 12.5 Gbps including the divide by 2, 4, and 8 sub-rates of this range. If it is desired to operate the DS125DF1610 at a data rate or data rate and sub-rate combination that is not available in the Rate/Sub-rate Table 18, then these desired data rates can be programmed into the device manually.

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The following procedure describes how to calculate and manually program data rates into the DS125DF1610.

1. Select a divider grouping from the Rate/Sub-rate Table and program that value to channel register 0x2F. When manually programming the data rate into the device, other rate/sub-rate values may be used to allow for different divider and group combinations. A list of all preprogrammed divider, group combinations is shown in the Table 19 below.

Table 19. Divider Options

CHANNEL REGISTER 0x2F[7:4] SETTING	FIRST GROUP DIVIDER SETTINGS	SECOND GROUP DIVIDER SETTINGS
0x0	2, 4	2, 4
0x1	1	1
0x2	1, 2, 4	1, 2, 4
0x3	1, 2, 4	1, 2, 4
0x4	1	1
0x5	1	1
0x6	1	1
0x7	1, 2, 4	1, 2, 4
0x8	1, 2, 4	1, 2, 4
0x9	2, 4	2, 4
0xA	1, 2, 4	1, 2, 4
0xB	8	1
0xC	8	1
0xD	1, 2, 4	1
0xE	1	1
0xF	1, 2	1, 2

2. Calculate the first group settings:

Table 20. Manual Data Rate Configuration -- 1STGroup Instructions

PARAMETER	VALUE/EQUATION	COMMENT
Reference Clock	F0 = 25e6	Internally the reference clock always operates at 25 MHz
Desired VCO Frequency	F1	F1 is the frequency of the VC0 which is equal to the desired data rate. If the desired data rate uses dividers, be sure to multiply the data rate by the divide setting to get the correct VCO frequency
Number of Reference Clocks	N = 1024	
VCO Freq ÷ 32	F2 = F1 ÷ 32	
Counts of VCO Freq ÷ 32 required	F3 = F2 x N ÷ F0	
Counts of VCO Freq ÷ 32 required rounded	F4	Round F3 to the nearest integer value. Convert this value to binary. Program the upper 8 bits to ch register 0x61 and the lower 8 bits to ch register 0x60. Be sure to set channel register 0x61[7] to 1 to enable the override function for manual programming.
PPM error due to rounding	Err = 1e6 x (F4 – F3) ÷ F3	
Required PPM tolerance	T	Enter the desired PPM tolerance
VCO Freq ÷ 32 +PPM tolerance	F5 = (1+ T÷1e6) * F2	
Rounded Counts of the VCO Freq ÷ 32 +PPM tolerance required	F6 = F5 x N ÷ F0	Round F6 to the nearest integer value
PPM Counts delta	F7 = F6 – F3	Convert this value to binary. Program the most significant bit channel register 0x67[7] and the rest of the bits to channel register 0x64[7:4]

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3. Calculate the second group settings:

Table 21. Manual Data Rate Configuration -- 2nd Group Instructions

PARAMETER	VALUE/EQUATION	COMMENT
Reference Clock	F0 = 25e6	Internally the reference clock always operates at 25 MHz
Desired VCO Frequency	F1	F1 is the frequency of the VC0 which is equal to the desired data rate. If the desired data rate uses dividers, be sure to multiply the data rate by the divide setting to get the correct VCO frequency
Number of Reference Clocks	N = 1024	
VCO Freq ÷ 32	F2 = F1 ÷ 32	
Counts of VCO Freq ÷ 32 required	F3 = F2 x N ÷ F0	
Counts of VCO Freq ÷ 32 required rounded	F4	Round F3 to the nearest integer value. Convert this value to binary. Program the upper 8 bits to ch register 0x63 and the lower 8 bits to ch register 0x62. Be sure to set channel register 0x63[7] to 1 to enable the override function for manual programming.
PPM error due to rounding	Err = 1e6 x (F4 – F3) ÷ F3	
Required PPM tolerance	T	Enter the desired PPM tolerance
VCO Freq ÷ 32 +PPM tolerance	F5 = (1+ T÷1e6) * F2	
Rounded Counts of the VCO Freq ÷ 32 +PPM tolerance required	F6 = F5 x N ÷ F0	Round F6 to the nearest integer value
PPM Counts delta	F7 = F6 – F3	Convert this value to binary. Program the most significant bit channel register 0x67[6] and the rest of the bits to channel register 0x64[3:0]

An example for setting group 0 and group 1 to 11.3 Gbps is shown in the Table 22 below.

Table 22. Manual Data Rate Configuration Example

CHANNEL REGISTER (HEX)	VALUE
0x60	0x80
0x61	0xB8
0x62	0x80
0x63	0xB8
0x64	0xEE
0x67[7:6]	2'b00

9 Power Supply Recommendations

9.1 Power Supply Filtering

The power pins on the DS125DF1610 are all internally shorted together on the BGA substrate. This allows board designers to more easily distribute the bypass capacitors for power supply filtering.

Power supply filtering typically consists of a bulk 22 µF capacitor with an array of 0.1 µF capacitors all placed near the device. Additional bypass capacitors or capacitors of different values may be required depending on system conditions. An example array of power supply filtering capacitors is shown in Figure 6.

10 Layout

10.1 Layout Guidelines

The high speed inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 100Ω. Vias should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board.

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10.2 Layout Example

Common BGA routing techniques such as trace necking, using blind vias and buried vias, are OK as long as the differential traces are balanced in their routing and the signals see few impedance changes. For example, necking lengths should be the same for the differential traces and implemented symmetrically for both traces. Figure 10 shows general Dos and Don'ts for high speed layout, such as differential trace gathering, differential trace necking, and high speed signal and return via implementation.

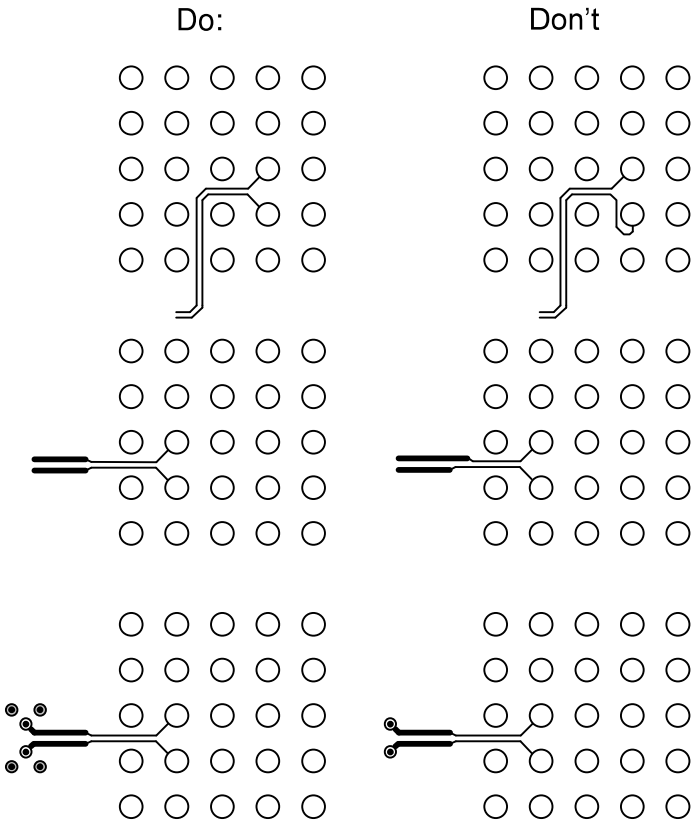


Figure 10. Layout Guidelines

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11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

•
•

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designed devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125DF1610FB/NOPB	ACTIVE	FCBGA	ABB	196	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-245C-72 HR	-40 to 85	DS125 DF1610	Samples
DS125DF1610FBE/NOPB	ACTIVE	FCBGA	ABB	196	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-245C-72 HR	-40 to 85	DS125 DF1610	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

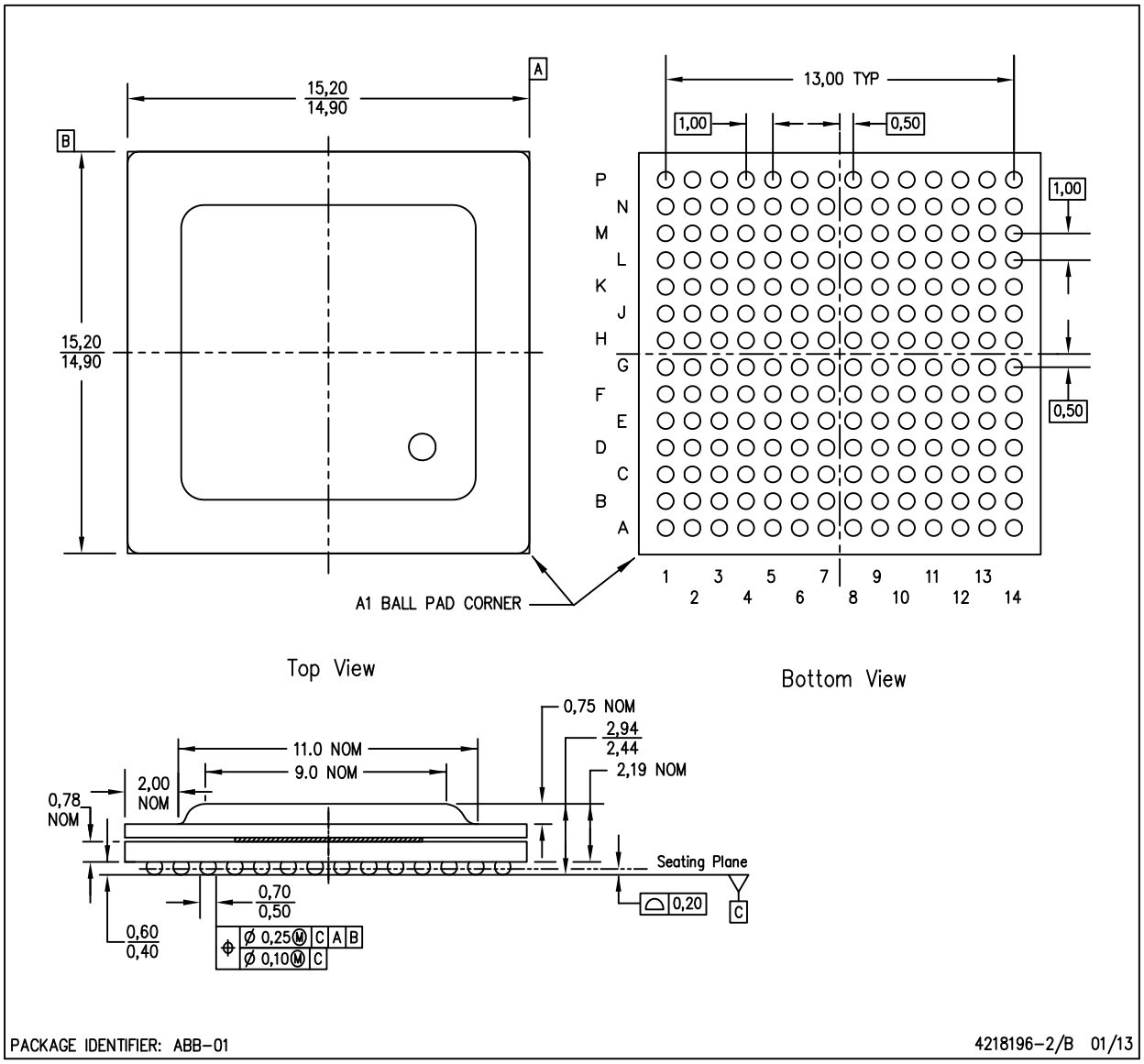
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ABB (S–FCBGA–N196) PLASTIC BALL GRID ARRAY



PACKAGE IDENTIFIER: ABB–01 4218196–2/B 01/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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