UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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AMPHENOL CORP.,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

_____

Case No. IPR2025-00835
Patent No. 10,877,233

_____

DECLARATION OF PAUL S. MIN, Ph.D.
IN SUPPORT OF PETITION FOR
***INTER PARTES* REVIEW OF U.S. PATENT NO. 10,877,233**

Amphenol Exhibit 1003
Amphenol v. Credo

Volex Exhibit 1033
Volex v. Credo

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      [1.b]: a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and 55
      iii. Limitation [1.c]: electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween, ... 64
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      [1.e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port, ... 65
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ii. Limitations [8.a]-[8.c] 81

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[8.b]: connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug; 81

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[8.e]: the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port, ...83

[8.f]: the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.....83

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i. Claim 10: The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. 84

j. Claim 11: The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories. 84

k. Claims 12-13 85

Claim 12: The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. 85

Claim 13: The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.....85

l. Claim 15 86

i. Preamble [15.PRE]: A communications method that comprises: 86

ii. Limitation [15.a]: inserting a first end connector plug of a cable into a first host interface port, the first end

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B. Ground 2: The Combination of Lugthart-706, Gorecki-617, and 802.3 Renders Obvious Claims 7, 14, and 20 89

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I, Paul S. Min, declare:

I. INTRODUCTION

A. Engagement

1. I have been engaged by Amphenol Corp. ("Petitioner" or "Amphenol") as an independent expert on the subject matters in connection with Amphenol's Petition for *Inter Partes* Review ("IPR") of U.S. Patent No. 10,877,233 (the "'233 patent").

2. I understand that the '233 patent is assigned to Credo Technology Group Ltd. ("Patent Owner" or "Credo").

3. This Declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and analysis, which may include a review of documents and information that have not yet been produced, as well as testimony from depositions that have not yet been taken.

4. All of the opinions set forth in this Declaration are based on my own personal knowledge, professional experience, education and judgment, in consideration of the documents, materials and information that I reference.

5. In connection with my work as an expert in this matter, I am being compensated at my standard hourly rate for consulting services, including time spent testifying at any hearing that may be held. I am also being reimbursed for

reasonable and customary expenses associated with my work in this case. I receive no other forms of compensation related to this case. No portion of my compensation is dependent or otherwise contingent upon the results of this proceeding or the specifics of my testimony.

B. Background and Qualifications

6. I am an expert in the field of high speed communication and computing, and the development of electronic devices and software systems and for the related applications. I am currently a Senior Professor in the Department of Electrical and Systems Engineering at Washington University in Saint Louis.

7. I received a B.S. degree in Electrical Engineering in 1982, an M.S. degree in Electrical Engineering in 1984, and a Ph.D. degree in Electrical Engineering in 1987 from the University of Michigan in Ann Arbor. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

8. After receiving my Ph.D., I worked at Bellcore in New Jersey from August 1987 until August 1990. At Bellcore, I was responsible for evolving the public switched telephone network (PSTN) into a multi-services voice and data network that incorporated packet switches, optical technologies, and wireless

technologies. I received an Outstanding Achievement Award for my contributions to Bellcore in 1989.

9. In September 1990, I joined the faculty at Washington University in St. Louis. Upon arriving at Washington University, I developed a communication and computer curricula in the School of Engineering and Applied Science. I regularly teach undergraduate and graduate courses. In July 1996, I was promoted to an Associate Professor of Electrical Engineering with tenure. I am currently a Senior Professor of Electrical and Systems Engineering at Washington University. I have served as the Chair of the Graduate Curriculum (2000–2002) and the Chair of the Undergraduate Curriculum (2011–2014) for the Department of Electrical and Systems Engineering.

10. At Washington University, I have conducted research in communication, computing, and related electronic hardware and software. My research group has pioneered a new paradigm for computing and communication systems that can alleviate the speed and performance mismatch against optical technology. I have received several grants from U.S. Federal Agencies, including the National Science Foundation (NSF), the Defense Advanced Research Project Agency (DARPA), and the Air Force Office of Scientific Research (AFOSR), and numerous contracts from companies and organizations around the world.

11. I have developed and incorporated various types of SerializerDeserializer (in short "SerDes") devices in the electronic circuits. These electronic circuits perform various functions in high speed communication, for which the integrated circuit chips are notoriously input/output (I/O) limited. To overcome the fundamental I/O limitations in the integrated circuit chips I developed, different types of SerDes blocks such as the RapidIO, the LVDS, and the PCIe were utilized.

12. In addition, my research group at Washington University has significantly contributed to development of future generations of wireless technology. We developed methods that enable coordinated transmission and reception of wireless signals among multiple base stations. Previously, radio signals from multiple base stations were considered as interference. Leveraging our research, a cluster of base stations can work together as a single resource enhancing the quality of radio signals across extremely noisy wireless channels.

13. I developed and implemented a number of semiconductor integrated circuit chips. These integrated circuit chips include switch fabrics, processors, high speed interfaces, protocol transposers, controllers, content search engines, look up table processors, and memory cells and arrays.

14. I have researched a variety of technologies for the packet switches and routers including packet scheduler, traffic shaper, traffic policing, buffer

management, and interposer. In addition, I have researched and implemented various look-up table configurations for fast packet processing, which is particularly applicable to the Multi Protocol Label Switching or MPLS. Moreover, since mid-1990s, I have been researching and developing various security technologies such as the deep packet inspection, content searching and matching, regular expression processing, etc.

15. As a faculty member at Washington University, I have taught a number of courses in electronics, communication, and computing at both the undergraduate and graduate levels. For example, I have taught Electronics (Washington University ESE 232), Communication Theory (Washington University ESE 471), Transmission and Multiplexing (Washington University ESE 571), and Signaling and Control of Communication Networks (Washington University ESE 572).

16. I have directly supervised numerous graduate students, a number of whom received a doctoral degree under my guidance. A number of doctoral theses that I have supervised relate specifically to the aforementioned-communication and computing technologies related to this litigation. My students and I have published a number of peer-reviewed articles in these topics.

17. In addition to my responsibilities as a university faculty member, I have founded two companies. In May 1997, I founded MinMax Technologies, Inc.,

a fabless semiconductor company that developed switch fabric integrated circuit chips for the Internet. In March 1999, I founded Erlang Technology, Inc., a fabless semiconductor company that focused on the design and development of integrated circuit chips and software for the Internet. One of Erlang's products received a best product of the year award in 2004 from a major trade journal for the electronics industry.

18. Outside my own start-up companies, I have also served in various technology and business advisor roles for other companies and organizations around the world. I was the main technical author for one of two winning proposals to the Korean government for CDMA wireless service licenses (1996). I was responsible for designing a commercial scale IS-95 CDMA cellular network, which I understand to be one of the earliest such networks deployed in the world. I worked with numerous engineers and scientists around the world to implement this commercial-scale cellular network before IS-95 CDMA was widely accepted. This provided me with extensive insight into various components of commercial-scale communication technology used today. I have also been involved in a semiconductor company that specializes in semiconductor memories, such as flash EEPROMs, as a board member and as a technical advisor (2007–2011).

19. I am a named inventor on eleven U.S. patents. I have authored and co-authored numerous technical papers and memoranda, many of which have

appeared in various peer-reviewed international journals and conferences. I have given more than 100 seminars and invited talks around the world. I have organized several international conferences and served as an international journal editor.

20. I am a member of, and have been actively involved in, a number of professional organizations. I have served as the Chair of the St. Louis Section of the IEEE, which has more than 3,000 members (2014), and a member of the Eta Kappa Nu Honor Society for electrical engineers. I have also been an Ambassador of the McDonnell International Scholars Academy (2007–2013).

21. I was a member of the Presidential Business Advisors Committee (to President George W. Bush) and was named 2002 Businessman of the Year by the Wall Street Journal for the State of Missouri, for my entrepreneurial efforts.

22. I have received multiple awards for my publications and contributions to technical communication systems. In 1988, I received the Best Paper Award at 18th ISATA Award of Technical Excellence in Florence, Italy. I was also a Rockwell Fellow at the University of Michigan in Ann Arbor in 1988 and 1989. I received a Research Initiation Award in 1993 from the Defense Advance Research Project Agency (DARPA). I received the Best Paper Award at MOBILITY 2011 in Barcelona, Spain. In my nearly 40 years of professional experience, I have acquired significant knowledge about telecommunications, computer, and

electronics industry standards and standard setting organizations such as ANSI, IEEE, ITU, IETF, Bellcore, and 3GPP.

23. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my curriculum vitae. *See* EX1004.

24. In forming my opinions, I have relied upon the materials listed below, my education, training, and knowledge of connector technologies, electrical and electronic materials, and related experience.

C. Bases of My Opinions and Materials Considered

25. I have reviewed the ’233 patent, its prosecution history, and the prior art and other documents and materials cited herein. For ease of reference, the full list of documents that I have considered is in the exhibit list below. I have also considered the documents cited and referenced herein, even if not included in the exhibit list below. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent office and/or well-known libraries, conferences, publications, organizations, and websites in the field as further discussed herein.

26. My opinions, as explained below, are based on my years of education, research, experience, and background in the field of microelectronics and

computing systems, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section III below. In forming my opinions, I have studied and considered the materials identified in the list below.

Exhibit	Description
1001	U.S. Patent No. 10,877,233 ("the '233 Patent")
1002	Prosecution History of U.S. Patent No. 10,877,233
1003	*Intentionally left blank*
1004	Curriculum Vitae of Paul S. Min, Ph.D.
1005	U.S. Patent No. 9,882,706 ("Lugthart-706")
1006	U.S. Patent No. 7,233,617 ("Gorecki-617")
1007	IEEE Std. 802.3-2015, Section 1 ("802.3-2015, Section 1")
1008	IEEE Std. 802.3-2015, Section 2 ("802.3-2015, Section 2")
1009	IEEE Std. 802.3-2015, Section 3 ("802.3-2015, Section 3")
1010	IEEE Std. 802.3-2015, Section 4 ("802.3-2015, Section 4")
1011	IEEE Std. 802.3-2015, Section 5 ("802.3-2015, Section 5")
1012	IEEE Std. 802.3-2015, Section 6 ("802.3-2015, Section 6")
1013	U.S. Patent No. 9,172,578 ("Dabiri")
1014	U.S. Patent No. 6,975,140 ("Hsu-140")
1015	U.S. Patent No. 8,990,654 ("Bliss")
1016	U.S. Pub. No. 2013/0195155 ("Pan")
1017	U.S. Patent No. 9,806,812 ("Schmidt")
1018	U.S. Patent No. 9,137,063 ("Zerbe-063")
1019	U.S. Patent No. 9,152,257 ("McCall")
1020	U.S. Pub. No. 2014/0119425 ("Boccaccio")

Exhibit	Description
1021	*Intentionally left blank*
1022	SFP-DD MSA, "SFP-DD Hardware Specification for SFP Double Density 2X Pluggable Transceiver," SFP-DD Rev 3.0 (April 10, 2019) ("SFP-DD-3.0")
1023	SFF-8436 Specification for QSFP+ 4X 10 Gb/s Pluggable Transceiver, Rev. 4.9 (Aug. 31, 2018)
1024	U.S. Patent No. 9,178,542 ("Shimanouchi")
1025	U.S. Pub. No. 2005/0078758 ("Aziz")
1026	U.S. Patent No. 7,570,708 ("Laturell")
1027	"Equalizers for High-Speed Serial Links," Pavan Kumar Hanumolu, et al., International Journal of High Speed Electronics and Systems, Vol. 15, No. 2 (2005), 429-458 ("Hanumolu")
1028	U.S. Pub. No. 2014/0281068 ("Das Sharma")
1029	'233 Patent Claim Limitation Comparison Chart
1030	Affidavit of Tanya Zeif including Exhibit B, DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer Datasheet, SNLS482B, Texas Instruments Incorporated (January 2017) ("TI-Retimer")
1031	U.S. Pub. No. 2014/0075076 ("Pillai")
1032	U.S. Patent No. 8,000,176 ("Bakx")
1033	*Intentionally left blank*
1034	*Intentionally left blank*
1035	*Intentionally left blank*
1036	*Intentionally left blank*
1037	*Intentionally left blank*
1038	*Intentionally left blank*
1039	*Intentionally left blank*
1040	*Intentionally left blank*
1041	*Intentionally left blank*
1042	*Intentionally left blank*

Exhibit	Description
1043	*Intentionally left blank*
1044	U.S. Patent No. 5,452,333 ("Guo")
1045	U.S. Patent No. 7,762,727 ("Aronson")
1046	Proakis, John G., "Digital Communication," 4th Edition, 2000, McGraw-Hill, pp. 583-635 ("Proakis")
1047	U.S. Pub. No. 2005/0013317 ("Lindsay")
1048	Liu, Jin and Xiaofeng Lin, "Equalization in high-speed communication systems." IEEE Circuits and Systems Magazine 4 (2004) pp. 4-17 ("Liu")
1049	Hsieh, Ming-ta and Gerald E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery." IEEE Circuits and Systems Magazine 8 (2008), pp. 45-57 ("Hsieh")
1050	U.S. Patent No. 8,787,430 ("Raghavan")
1051	U.S. Pub. No. 2015/0106536 ("Lauby")

D. My Understanding of Patent Law

27. In developing my opinions, I discussed various relevant legal principles with Petitioner's attorneys. Though I do not purport to have prior knowledge of such principles, I understood them when they were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

28. I understand that "*inter partes* review" (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent's claims based on prior-art patents and printed publications.

29. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the '233 patent are unpatentable by a preponderance of the evidence. I understand that "preponderance of the evidence" means that a fact or conclusion is more likely true than not true.

30. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art ("POSA") in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification's special definition controls. If a claim element is expressed as a "means" for performing a specified function, I understand that it covers the corresponding structure described in the specification and equivalents of the described structure. I have applied these standards in preparing the opinions in this declaration.

31. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the

challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application's filing date. I understand that a disclosure that merely renders the claimed invention obvious is not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

32. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (novel—*i.e.*, not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

1. Anticipation

33. I understand that, for a patent claim to be "anticipated" by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior-art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA's knowledge and experience.

34. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

2. Obviousness

35. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior-art reference or a combination of prior-art references.

36. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

- the scope and content of the prior art;
- the differences between the prior art and the claims at issue;
- the knowledge of a person of ordinary skill in the pertinent art; and
- if present, objective factors indicative of non-obviousness, sometimes referred to as "secondary considerations." To my

knowledge, the Patent Owner has not asserted any such secondary considerations with respect to the ’233 patent.

37. I understand that in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

38. I further understand that in determining whether a prior-art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

- combining prior-art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve similar devices in the same way;
- applying a known technique to a known device ready for improvement to yield predictable results;
- applying a technique or approach that would have been “obvious to try,” *i.e.*, choosing from a finite number of

identified, predictable solutions, with a reasonable expectation of success.

- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine prior-art reference teachings to arrive at the claimed invention. I understand that this teaching, suggestion or motivation may come from a prior-art reference or from the knowledge or common sense of one of ordinary skill in the art.

39. I understand that for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

3. Claim Interpretation

40. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the claim. In this section, I discuss the interpretations I have applied to certain claim terms in my analysis.

41. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (*i.e.*, at the time of the purported invention, or the so called "effective filing date" of the patent application), after reviewing the patent claim language, the specification and the prosecution history (*i.e.*, the intrinsic record).

42. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an

applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

43. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the time of the alleged invention. This can be useful for technical terms whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

44. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Declaration, I apply the above standards to the terms in the challenged claims. The meanings of specific terms are discussed below in connection with evaluating the disclosure in the priority documents.

II. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

45. I have reviewed the ’233 patent (EX1001) and its prosecution history (EX1002).

46. I understand that the ’233 patent issued from U.S. Patent Application No. 16/698,935 (“the ’935 application”), filed on November 27, 2019. EX1001, codes (21), (22).

47. I am informed that the ’935 application relates to Chinese Patent Application No. 201910542576.3, which was filed on July 1, 2019.

48. I have been instructed by counsel to assume the relevant timeframe for my analysis of the prior art in this Declaration is on or before July 1, 2019.

49. Based on my review of this material, I believe that the relevant general field for the purposes of the ’233 patent is digital communication system design.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

50. I have been informed and understand that for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date.

51. I have been informed and understand that various factors may be considered in assessing the level of a POSA, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. I have also been informed and understand that not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. I have further been informed and understand that these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. I have applied this standard throughout my declaration.

52. The ’233 patent involves technology in the field of network communication designs. I have been asked to provide my opinions as to the state of the art in this field on or around July 2019. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the ’233 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the July 2019 timeframe, even if I do not say so specifically in each case.

53. In the context of the ’233 patent and the prior art, it is my opinion that the POSA to whom the patent is addressed, on July 1, 2019, would have had a

Bachelor of Science in Electrical or Computer Engineering with at least three years of experience in digital communication system design. For example, a POSA would have had a working knowledge of assuring the signal integrity over noisy channels and how the signal integrity is affected by PCB and cable designs, and methods for addressing those concerns. More education could substitute for experience, and vice versa. This person would have been capable of understanding and applying the teachings of the ’233 patent and the prior-art references discussed in this declaration.

54. The basis for my familiarity with the level of ordinary skill is my own technical experience and my interaction with students and professionals in the field of Electrical and Computer Engineering who were at this level of skill as of July 1, 2019. I am also very familiar with the professional background of those who worked in the field around the priority date of the ’233 patent as I personally have worked in the industry extensively at the time. I am well aware of the knowledge that a POSA would have had at the time this patent was written as I have been actively consulting, teaching, and carrying out research with such students and/or professionals all through that period.

55. In reaching this opinion as to the hypothetical POSA, I have considered the standard recited above such as types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations

are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field.

56. As summarized above with regard to my qualifications and experience, I possessed at least the level of skill of a person of ordinary skill in the art at the time of the alleged invention of the ’233 patent.

57. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill in and around July 2019. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above.

IV. THE ’233 PATENT

58. The ’233 patent is titled “Active Ethernet Cable with Preset Pre-Equalization.” The ’233 patent states that “[t]his Ethernet standard provides a common media access control specification for local area network (LAN) operations at selected speeds from 1 Mb/s to 100 Gb/s over coaxial cable, twinaxial cable, twisted wire pair cable, fiber optic cable, and electrical backplanes, with various channel signal constellations.” EX1001, 1:10-15. The ’233 patent goes on to state that “[a]s demand continues for ever-higher data rates, the standard is being extended. Such extensions to the standard must account for increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates. It is becoming increasingly difficult to provide

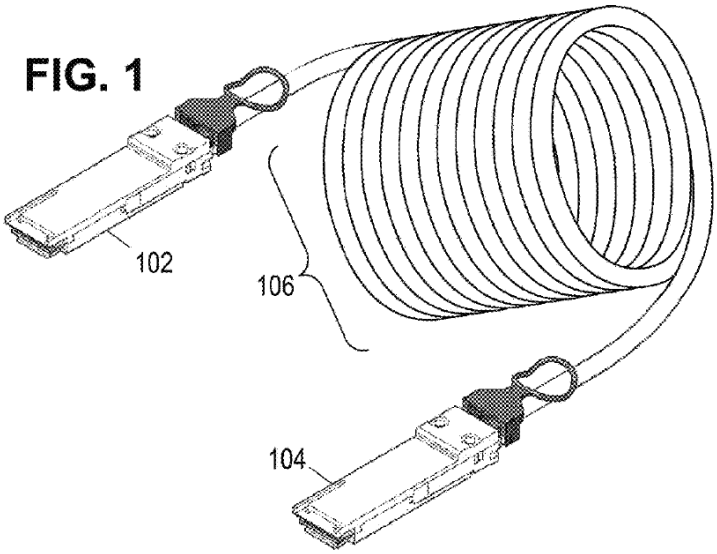
affordable, mass-manufactured network hardware that assures consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps with PAM4 or larger signal constellations." EX1001, 1:15-23.

A. Described Embodiments

59. The '233 Patent describes an active electrical cable (which it calls an "active Ethernet cable" or "AEC"), a cable manufacturing method, and a communications method using a cable, employing preset transmit-side equalization (e.g., pre-equalization or pre-emphasis). EX1001, Abstract, code (54), 1:32-36, 3:8-9. Pre-equalization was a well-known technique wherein transmit filters modify a signal in a way that compensates for the signal distortion that occurs during transmission on a communication path—over a cable, over a backplane—so that on receipt the recovered digital signal closely approximates the digital signal transmitted. The transmit filter behavior is controlled by setting filter coefficients or "taps." EX1001, 5:39-48, 9:11-12, 10:40-44. The '233 Patent describes storing filter coefficients in non-volatile memory, and setting transmit filter coefficients using those stored values. EX1001, 5:3-5, 5:27-35, 11:3-6.

60. The cable has an industry-standard SFP or QSFP connector at each end, wherein the connector comprises a transceiver that the '233 Patent calls a "data recovery and re-modulation (DRR) device." EX1001, Abstract, Fig. 1 (below), 3:49-55 ("[E]ach connector 100, 101 may include a powered transceiver

that performs clock and data recovery (CDR) and re-modulation of data streams, hereafter called a data recovery and re-modulation (DRR) device."), 9:19-22, 10:5-9.



61. Each connector, a pluggable module, mates with a receiving port in a host device, and the AEC provides a communication link between the host devices coupled to each AEC connector according to protocols that "can be found in the current Ethernet standard" and whose implementation details were "well within" the POSA's ordinary skill. EX1001, 7:14-34. "[T]he transceivers perform CDR and re-modulation not only of the inbound data streams to the host interface as they exit the cable, but also of the outbound data streams from the host interface entering the cable." EX1001, 3:55-60. Clock and data recovery (e.g., CDR) was a known process for recovering a data signal from a received signal.

62. The ’233 Patent describes data streams being communicated in lanes, referring to particular signal paths. The ’233 Patent describes re-modulating data streams entering or exiting the DRR device (such as the data streams that the transceiver receives from and transmits to a host device) as met by “format conversion” such as converting “1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa.” EX1001, 4:43-45. PAM-4 and NRZ were known coding schemes used with known standards like Ethernet. EX1015 (“Bliss”), 4:5-13. PAM-4 is four-level pulse amplitude modulation, which encodes two bits per symbol. Bliss, 4:5-13. NRZ is non-return to zero, which encoded one bit per symbol. EX1016 (“Pan”), ¶4. Thus, the ’233 Patent describes the known concepts of a transceiver converting two received NRZ data streams into one transmitted PAM-4 data stream, and vice versa. EX1031 (“Pillai”), ¶[0006].

B. Challenged Claims

63. The ’233 Patent has 20 claims. Claims 1, 8, and 15 are independent. Appendix A provides a claim list labeling limitations (e.g., “[1.a]”).

64. Claim 1 recites an electrical cable connecting a “*data recovery and re-modulation (DRR) device*” at each end. Limitations [1.a]-[1.c]. Each *DRR device* “*exchanges inbound and outbound multi-lane data streams*” with a host device coupled to a respective *DRR device*. Limitations [1.a]-[1.b]. Each *DRR device* “*convert[s]*” between signals received over the cable and the “*multi-lane data*

streams" received from and transmitted to the host. Limitations [1.d]-[1.e]. Each *DRR device* pre-equalizes signal transmitted over the cable "*using transmit filter coefficient values stored in nonvolatile memories*." Limitation [1.f].

65. Claim 8 recites a manufacturing method for claim 1's cable, while claim 15 recites a communication method over a cable.

C. Prosecution History

66. The '233 Patent issued from application no. 16/698,935, filed November 27, 2019. EX1001, code (21), (22). The Examiner allowed all claims in a first action. EX1002, 107. The applicant then requested continued examination (RCE) to consider an Information Disclosure Statement citing Office communications in different cases. EX1002, 134-138. The Examiner thereafter repeated the claim allowance without discussing any art cited in the communications from the unrelated cases. The Examiner stated in the reasons for allowance that the prior art failed to teach limitations [1.f], [8.f], and [15.c], e.g., *the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories*. EX1002, 154.

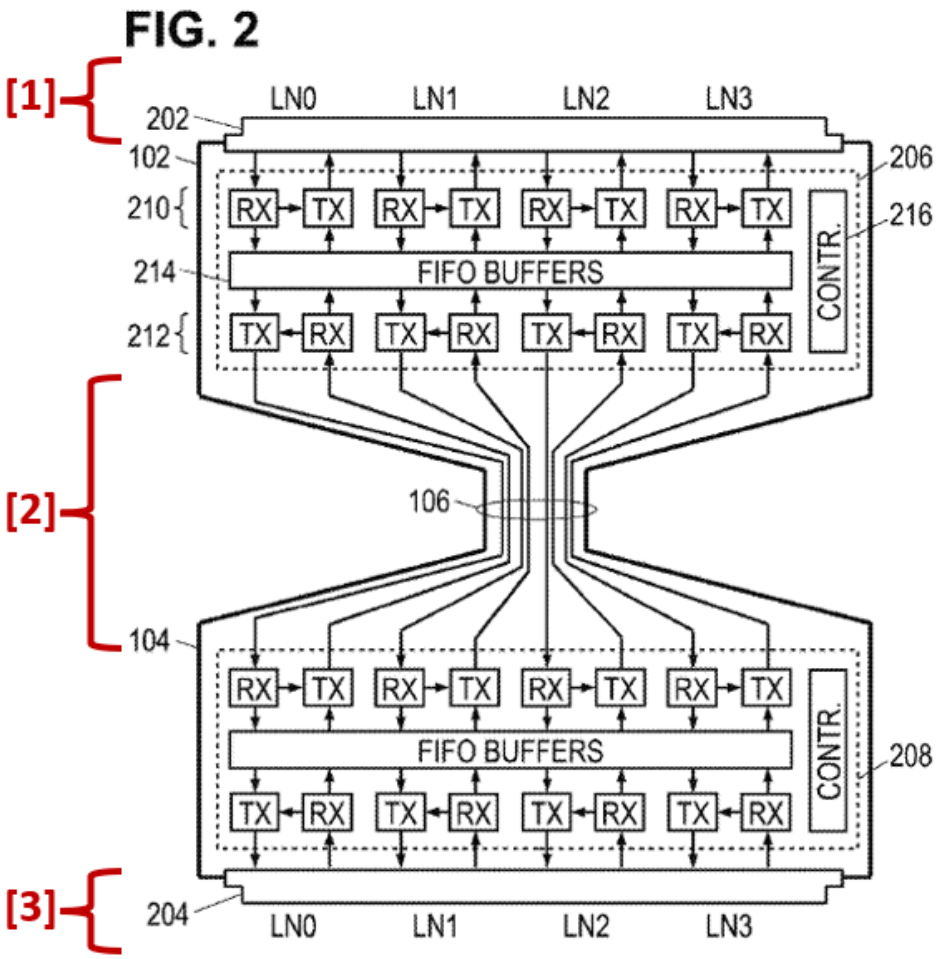
D. Additional Technical Background

67. Below, I will briefly describe technical concepts that are described in the '233 patent and/or the prior art.

1. Active Ethernet Cables

68. The ’233 patent relates to active Ethernet cables that connect two “host devices” (*e.g.*, computers). EX1001, 3:44-48, 1:5-23 (“Ethernet” is an IEEE standard). “Active” cables have powered components that process signals transmitted into and/or out of the cable. EX1005 (“Lugthart-706”), 14:29-31. Active Ethernet cables have “connectors” at their ends to connect to mating ports on host devices and each connector has a transceiver (*i.e.*, a transmitter and receiver) that processes signals transmitted into and out of the cable. EX1001, 1:29-42.

69. The transceivers in each of the connectors split the link between two hosts into three segments–[1] from the first host to the first transceiver (a first host interface), [2] between the first transceiver and the second transceiver (over the cable), and [3] between the second transceiver and the second host (a second host interface).



Each transceiver receives a signal from its host, demodulates, processes, and remodulates it for transmission over the cable. The transceiver at the other end of the cable receives the signal, demodulates, processes, and remodulates it to pass through its host interface. EX1001, 4:4-26. Modulation sets the properties of an analog signal (*e.g.*, its amplitude) to represent digital data, which facilitates transmission over a communication channel. Lugthart-706, 31:23-46. Demodulation reconstructs the digital data from the analog signal. EX1001, 7:3-11; Lugthart-706, 8:56-60.

70. As the analog signal passes over a communication channel, it may be degraded/distorted. EX1001, 4:20-21; Lugthart-706, 6:36-57. The transceivers of the ’233 patent include “clock and data recovery” (CDR) circuits. EX1001, 4:27-43. CDR circuits in a signal’s path will retime and attempt to recreate the signal (as best as it is able to; *see* my discussion of CDR in Section IV.D.4 below), and so degradation/distortion of signals over each segment of the link between hosts to be addressed separately (*i.e.*, degradation/distortion before CDR is separated from degradation/distortion after CDR), rather than addressing a larger aggregate amount of degradation/distortion over the entire link. One form of degradation/distortion is jitter, an unwanted variation in the timing of changes in the analog signal that represents digital data. EX1044 (“Guo”), 1:24-26, 1:58-2:2; EX1045 (Aronson), 11:6-10. A transceiver with CDR can “recover the clock and retime the signal” to compensate for jitter. Aronson, 11:1-6, 11:20-24.

71. Intersymbol interference (ISI) is another form of degradation/distortion, *e.g.*, caused by lossy channels, in which one symbol in a data stream interferes with subsequent symbols. Lugthart-706, 6:41-57. Equalization is signal processing that may be used to compensate for channel losses—and therefore compensate for ISI—so that a received signal approximates the transmitted signal. Lughtart-706, 9:10-25; EX1016, 1:9-12; Aronson, 15:2-4. Equalization can be performed at the transmitter (called pre-equalization) and/or

the receiver. Aronson, 14:19-23, 15:1-8. Equalization was commonly achieved via filters using parameters (*e.g.*, coefficients) controlling the filter's modification of the signal. Lugthart-706, 9:38-51, 22:3-16.

72. Equalization parameters could be fixed, adjustable, or "adaptive" via a process, *e.g.*, during which equalization parameters are modified in response to sending known test signals through the channel using different equalization parameters until the error in the equalized signal at the receiver is low. Aronson, 15:5-8; Mezer-665, 6:36-41, 2:47-50; Das Sharma, [0080]-[0081].

73. I further discuss these concepts, such as ISI, equalization, and CDRs, below.

2. SerDes for Transmission of High-Speed Serial Data

74. In today's environment, many of the specialized integrated chips (or ICs) are in the form of the Application Specific Integrated Chip (or ASIC). In particular, the ASICs used in the communications and computer environments are notoriously input-output (IO) limited.

75. By way of background, some integrated circuit chips are die-limited when the ICs contain large number of complex functional blocks comprising a large number of transistors. For example, certain complex processors may be die-limited as they contain multiple functional blocks such as a large number of processor cores, memory interfaces, off-load engines, security features, IO

interfaces, etc. To implement these functional block takes up large areas of silicon die, and thus the sizes of such ICs are determined by the size of the silicon die, that the IC packages contain.

76. In other cases, some integrated circuit chips are IO limited. The inputs and outputs from an IC must be accessible to the outside of the package containing the IC in the form of IO pins or pads. When there are a large number of inputs and outputs from the IC, the size of the package containing the silicon die of the IC must be increased since the IO pins or pads must be spaced apart to provide proper electrical connectivity of the IC to the printed circuit board. In this case, the size of the IC is determined by the number of input and output pins or pads. Many of the ASICs used in the communication environment are IO limited IC.

77. When the number of IO pins or pads becomes so large, *e.g.*, more than a thousand, in order to provide the IO pins or pads outside the IC package becomes untenable since in this case, the size of the IC package becomes too large for the IC to be mounted on a printed circuit board, which is often crowded with many components necessary to perform the required functions.

78. To cope with the IO limitation in the communication ICs, the electronic industry developed the Serializer/Deserializer (or SerDes). In designing an IO-limited IC, one or more of the SerDes blocks are incorporated as the external interfaces from the IC. For transmission, the serializer portion of the SerDes

combines multiple output data streams into a single data stream via multiplexing these output data streams, which otherwise would be transmitted separately. Then, the serialized data stream is transmitted from the IC to the receiving end, for example, another IC with similar SerDes blocks. The receiving IC then deserializes the received serial data stream by way of the Des portion of the SerDes block, which is embedded in the receiving IC.

79. While the use of the SerDes mitigates or minimizes the IO limitation in the IC design, it creates different challenges, specifically the increase in the transmission rate as the data rate increases according to the number of the data streams combined during the serialization process.

3. Equalization

80. In explaining the basic concept of the equalization, I refer to a widely referenced textbook entitled, "Digital Communication" by John G. Proakis (EX1046; "Proakis"). In addition, I also refer to a tutorial paper entitled, "Equalizers for High-Speed Serial Link" by Pavan K. Hanumolu, G. Y. Wei, and U. K. Moon (EX1027; "Hanumolu"), and a featured article entitled "Equalization in High-Speed Communication Systems" by J. Liu and X. Lin (EX1048; "Liu").

81. Liu describes that "[c]ommunication systems may be described by the block diagram shown in Figure 1. They always involve three basic parts: the transmitter (TX), the channel, and the receiver (RX). The signal, *s(t)*, is the

transmitted signal and the signal, *r(t)*, is the received signal. Non-ideal channel characteristics, for example, limited channel bandwidth and crosstalk noise, often deteriorate the signal quality of the received signal and causes error in data recovery." Liu, page 5. The following is Figure 1 of Liu.

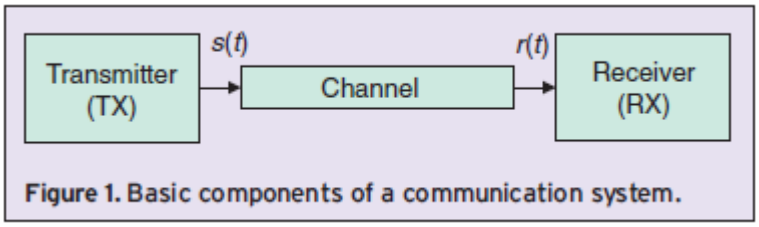


Figure 1. Basic components of a communication system.

82. In high-speed communication systems, for example utilizing the SerDes in the transmitter and the receiver, the channel bandwidth may be limited in comparison to potentially up to hundreds of gigabits per second data rate. In this case, the "deterior[ation of] the signal quality of the received signal" that Liu refers to above requires the use of signal processing techniques known as the equalization.

83. In particular, Liu states that "[t]he term of inter-symbol interference describes the dispersion effect in discrete time domain, where the transmitted data are treated as digital symbols with pulse modulation. Figure 5 shows the communication channel with transmitter pulse modulation and receiver filter. For binary data, which is also known as two level pulse amplitude modulation (2-PAM) shown in Figure 2, the discrete information-bearing symbol $\{I_n\}$ is either

"1" or "0" and the modulation pulse is a square pulse as shown." The following is Figure 5 of Liu.

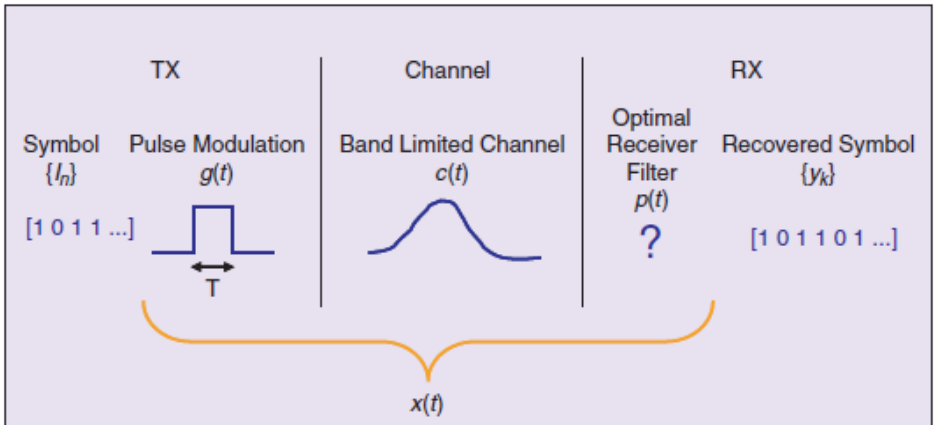


Figure 5. Communication channel with transmitter pulse modulation and receiver filter.

84. As shown in Figure 5 of Liu above, square pulse *g(t)* is transmitted during a time period T from the transmitter TX. Because the channel is bandwidth limited, the transmitted signal *g(t)* cannot maintain its sharp transitions in both leading and trailing edges, making more rounded shape of signal shown in *c(t),* which is received at the receiver RX. Importantly, the received signals *c(t)* has trailing edge lasting longer than the transmission interval T. If the transmitter has more signal to transmit after one transmission interval of T, then by the time the leading edge of the successively transmitted signal arrive at the receiver, the trailing edge of the received signal *c(t)* from the previously transmitted signal is present at the receiver. In other words, the trailing edge of the signal received may overlap with the leading edges of one or more of the signals transmitted successively. This phenomenon is called the intersymbol interference (or ISI).

85. Proakis describes that "[t]he channel distortion results in intersymbol interference, which, if left uncompensated, causes high error rates. The solution to the ISI problem is to design a receiver that employs a means for compensating or reducing the ISI in the received signal. The compensator for the ISI is called an *equalizer*" (Proakis, page 583), and that "[t]he discrete-time white noise linear filter model for the intersymbol interference effects that arise in high-speed digital transmission over nonideal band-limited channels will be used throughout the remainder of this chapter in our discussion of compensation techniques for the interference. In general, the compensation methods are called *equalization techniques* or *equalization algorithms"* (Proakis, page 589).

86. Liu explains that "[t]here are two types of equalization: transmitter pre-emphasis and receiver equalization. Both seek to either emphasize the high-frequency components or to deemphasize the low frequency components of the transmitted or received signal, in order to compensate the effect that the high-frequency components are attenuated more than the low-frequency components through the channel. Using both the transmitter and receiver equalization allows the best system performance in terms of BER." Lui, page 9.

4. Clock and Data Recovery (CDR)

87. In "Architectures for multi-gigabit wire-linked clock and data recovery" by Ming-ta Hsieh and Gerald E. Sobelman (EX1049; "Hsieh"), Hsieh

states that "[a] clock and data recovery (CDR) circuit is an essential block in many high-speed wire-linked data transmission applications such as optical communications systems, backplane data-link routing and chip-to-chip interconnection. The important role of a CDR is to extract the transmitted data sequence from the distorted received signal and to recover the associated clock timing information." Hsieh, page 46.

88. Hsieh further states that "Figure 2 illustrates a simplified functional diagram of clock recovery and data retiming using a CDR circuit. The clock recovery circuit detects the transitions in the received data and generates a periodic clock. The decision circuit often uses D-type Flip-Flops (DFFs) driven by the recovered clock to retime the received data, which samples noisy data and then regenerates it with less jitter and skew." Hsieh, page 46. The following is Figure 2 of Hsieh.

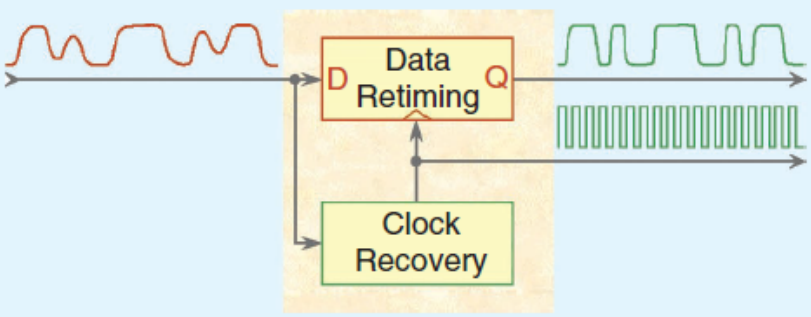


Figure 2. Clock recovery and data retiming for a CDR circuit.

89. The figure above shows that the CDR circuit receives data signals from the channel, which is distorted by, among others, the limited bandwidth of the channel. From the received signal, the clock is recovered, and using the clock, the received signal is sampled and the data is stored in its original form.

90. Hsieh states that "[a] generic block diagram of a high-speed wire-linked data transmission system is shown in Figure 3, where the received data is equalized in the receiver input buffer and retimed in the CDR module before proceeding into the deserializer module." Hsieh, page 46. The following is Figure 3 of Hsieh.

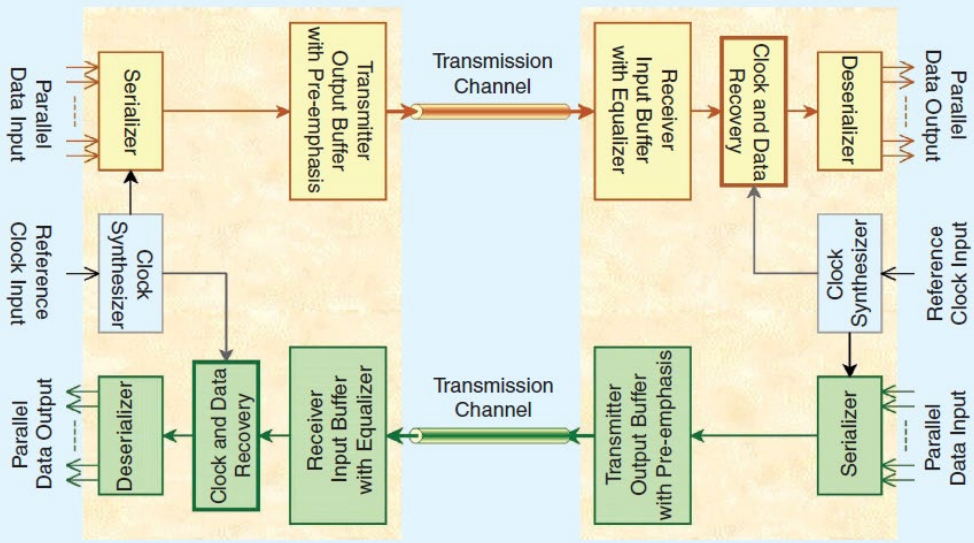


Figure 3. Block diagram of a generic high-speed wire-linked transmission system.

91. With reference to the figure above, the "Parallel Data Input" shown at the top left of the figure enters the "Serializer" block." The signal conveying the "Parallel Data Input" may be in a variety of forms, for example, Non Return to

Zero (NRZ), Pulse Amplitude Modulation 4 (PAM4), BPSK, QPSK, etc. At this point, the signal conveying the "Parallel Data Input" is an analog signal, into which the underlying digital information (*e.g.*, "1" and "0") is modulated. Then, multiple streams of "Parallel Data Input" is multiplexed by the "Serializer" block (at the top left of the figure in yellow), creating a single stream of modulated data.

92. The serialized data stream, which is output from the "Serializer" block, is entered into the "Transmitter Output Buffer with Pre-emphasis" block. The "Transmitter Output Buffer with Pre-emphasis" block then pre-emphasizes the serialized data stream and transmits the pre-emphasized serialized data stream over the "Transmission Channel."

93. At the receiver, the "Receiver Input Buffer with Equalizer" block received the transmitted signal, which is likely to have been distorted by the channel. The "Receiver Input Buffer with Equalizer" block at the receiver equalizes the distortion in the received signal. Then, the Clock and Data Recovery" block attempts to recover the originally transmitted serialized data stream as shown in Figure 2 of Hsieh. The final step in the receive sequence is the "Deserializer" block, which demultiplexes the recovered serialized data stream into multiple parallel data streams for subsequent output as streams of modulated digital data.

94. The block diagram of a generic high-speed wire-linked transmission system shown in Figure 3 of Hsieh describes various processes performed between a pair of transmitter and receiver. This generic block diagram of Hsieh has cross relationship with the embodiment disclosed in the ’233 patent. For example, the following is FIG. 5 of the ’233 patent, which “is a block diagram of a transmitter in an illustrative multi-lane transceiver.” EX1001, 3:27-28.

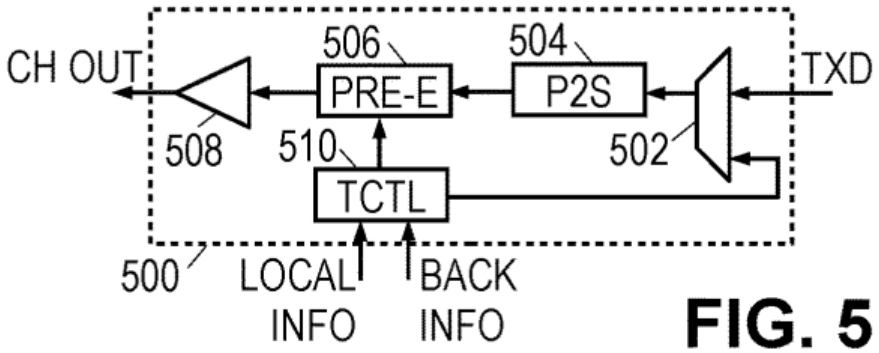
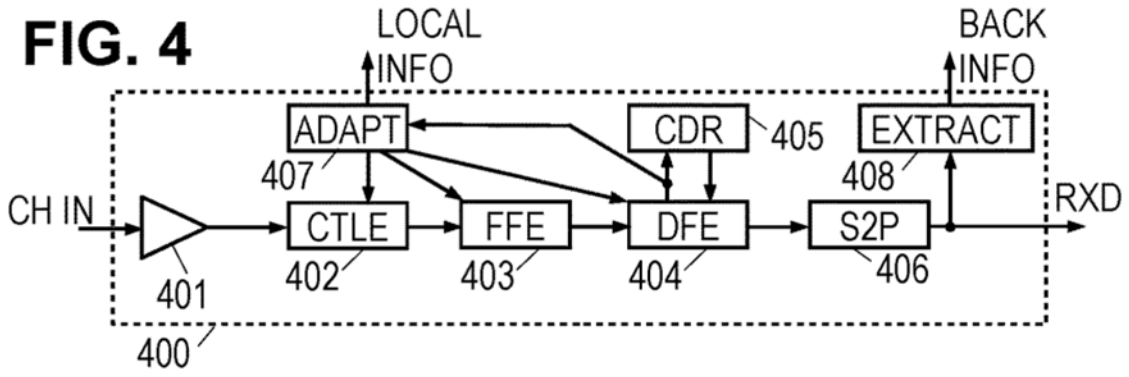


FIG. 5

95. Setting aside the “LOCAL INFO” and “BACK INFO” portions of the block diagram, which are used for configuration of the pre-emphasis function performed by “PRE-E” 506, the “P2S” block 504 performs parallel to serial conversion, which is performed by the “Serializer” block in Figure 3 of Hsieh and the “PRE-E” block 506 perform pre-emphasis function, which is performed by the “Transmitter Output Buffer with Pre-emphasis" block in Figure 3 of Hsieh.

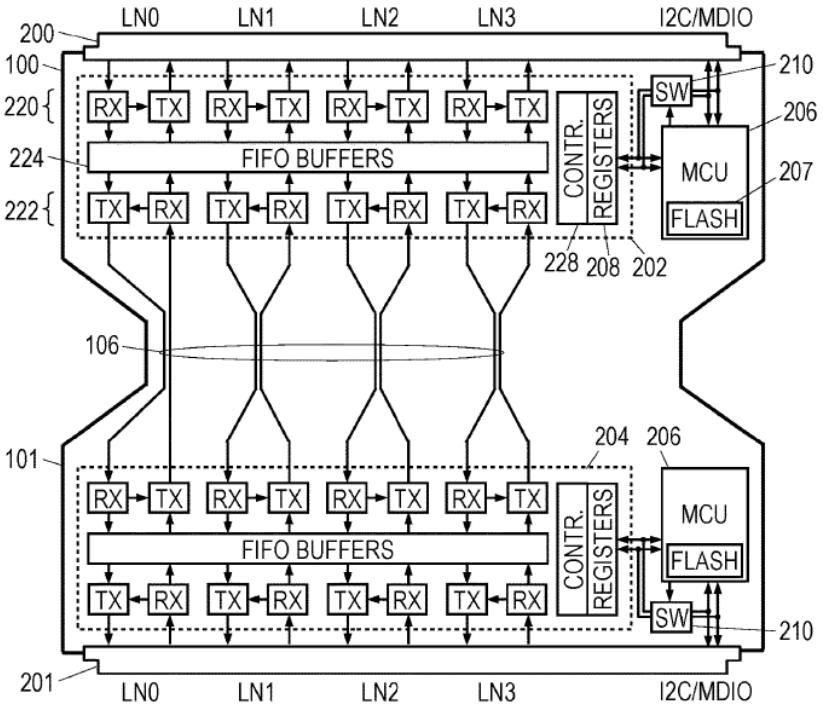
96. Similarly, the following is FIG. 4 of the ’233 patent, which “is a block diagram of a receiver in an illustrative multi-lane transceiver.” (’233 patent, 3:16-17.)



97. Again, setting aside the "LOCAL INFO" and "BACK INFO" portions of the block diagram, which are used for configuration of the equalization functions performed by "CTLE" 404 and DFE 406, the "CDR" block 408 performs clock and data recovery function, which is performed by the "Clock and Data Recovery" block in Figure 3 of Hsieh, and the "CTLE" and "DFE" blocks together perform the equalization function, which is performed by the "Receiver Input Buffer with Equalizer" block in Figure 3 of Hsieh. Finally, the "S2P" block 410 performs the serial to parallel conversion, which is performed by the "Deserializer" block in Figure 3 of Hsieh.

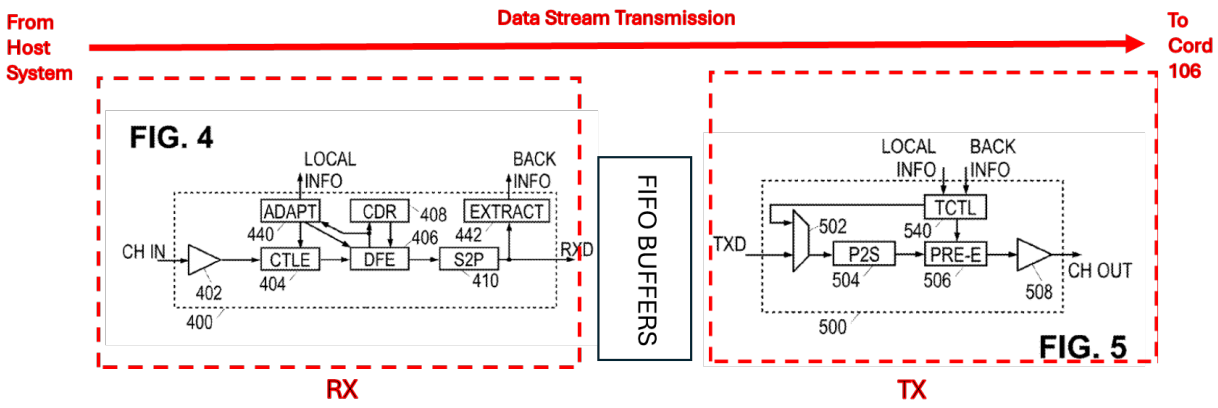
98. The '233 patent discloses an "active Ethernet cable" (EX1001, 3:8-9), as part of the "function-block" diagram of the illustrative cable" (EX1001, 3:10-11), plug 202 "adapted to fit a standard-compliant Ethernet port (EX1001, 4:47-48), as shown in Figure 3A below.

FIG. 3A



99. As shown in the figure above, plug 202 has multiple receivers and transmitters in sets 210 and 212. In particular, when plug 202 receives a data stream on one of the lanes, the data stream goes through one of the receivers and one of the transmitters before the data stream is transmitted onto the cable cord 106. For example, the data stream received on the left most lane, *i.e.*, LN0, it goes through the leftmost RX among the receivers 210 and the leftmost TX among the transmitters 212.

100. In the context of Figures 4 and 5, which respectively illustrates the RX and the TX shown in Figure 2 above, the following figure shows the processes, to which the data stream to be transmitted is subject.



101. In the figure above, the "S2P" block in RX (FIG. 4) and the "P2S" block in TX (FIG.5) negate each other – the serial to parallel conversion by the "S2P" block negates the parallel to serial conversion by the "P2S" block. The center of the overall transmission path shown in the figure above is the "CDR" 408 (FIG. 4), which restores the data stream transmitted from the host system, which is distorted by the channel formed over the path comprising the package of the IC where the data stream is originated, through the electrical trace over the printed circuit board on which the IC is mounted, to the connector on the plug, and to the "CH IN" shown in FIG. 4. Once the data stream is recovered by the "CDR" block 408, the data stream is pre-emphasized by the "PRE-E" block 506 in FIG. 5 in preparation for the transmission over the cord 106.

V. PRIOR-ART REFERENCES

102. I briefly introduce in this section various prior-art references discussed in this declaration.

A. Lugthart-706 (EX1005)

103. Lugthart-706 is titled "High Speed Transceiver." Lugthart-706 is directed to "[s]ystems and methods for high speed communications" that "include innovative transceiver architectures and techniques for re-timing, multiplexing, de-multiplexing and transmitting data." Lugthart-706, Abstract.

104. I have been instructed by Petitioner's counsel to assume that Lugthart-706 qualifies is prior art to every claim in the '233 patent.

B. Gorecki-617 (EX1006)

105. Gorecki-617 is titled "System and Method of Equalization of High Speed Signals." Gorecki-617 is directed to "a technique of, and system for enhancing the performance of high-speed digital communications through a communications channel." Gorecki-617, Abstract.

106. I have been instructed by Petitioner's counsel to assume that Gorecki-617 is prior art to every claim in the '233 patent.

C. IEEE Std. 802.3-2015 (EX1007-EX1012)

107. IEEE Std. 802.3-2015 ("802.3") is the 2015 IEEE Standard for Ethernet. EX1007, 21 (Introduction). 802.3 is a standard that "defines Ethernet local area, access and metropolitan area networks." EX1007, 54 (Scope). 802.3 has six sections, which are provided at EX1007-EX1012.

108. 802.3 is an IEEE Standards Association standard published on March 4, 2016 and is a Revision of IEEE Std. 802.3-2012. I have been instructed by

Petitioner's counsel to assume that 802.3 qualifies as prior art to every claim in the '233 patent.

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE IN LIGHT OF THE PRIOR ART

109. I have been asked to provide my opinion concerning whether claims 1-20 of the '233 patent would have been obvious to a POSA in light of the prior-art references discussed below. For the reasons explained below, it is my opinion that each of claims 1-20 would have been obvious to a POSA. The following table summarizes the Grounds that I discuss in the sections below (independent claims have been indicated in **bold** in the table below):

Ground	Reference(s)	Claims	Basis
1	Lugthart+Gorecki	**1**-6, **8**-13, **15**-19	Obviousness
2	Lugthart+Gorecki+ IEEE Std. 802.3-2015	7, 14, 20	Obviousness

A. <u>Ground 1</u>: Lugthart-706 in view of Gorecki-617 Renders Obvious Claims 1-6, 8-13, and 15-19

110. As explained in this section below, in my opinion claims 1-6, 8-13, and 15-19 of the '233 patent would have been rendered obvious over Lugthart-706 in view of Gorecki-617 (hereinafter "Lugthart+Gorecki").

1. Discussion of Lugthart-706 (EX1005)

111. Lugthart-706 discloses an "active cable" that "includes… first and second transceiver assemblies 105a, 105b positioned at either end of… conductive lines 111." Lugthart-706, 14:30-34, Fig. 2A (below).

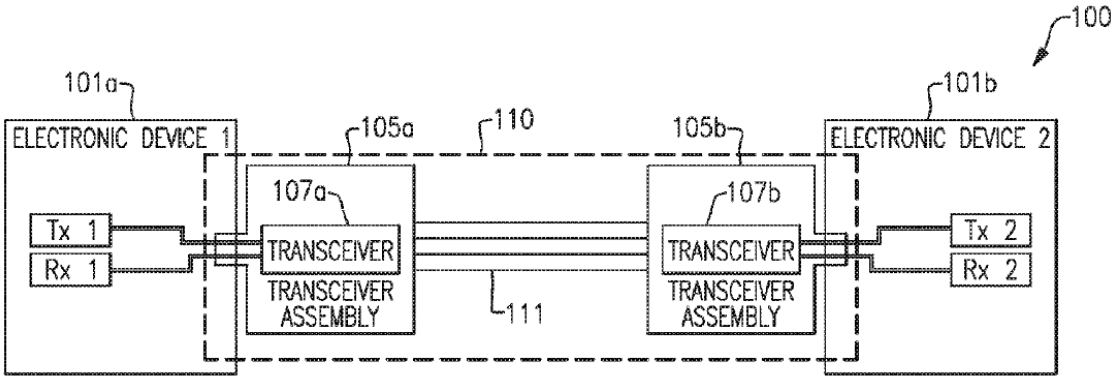
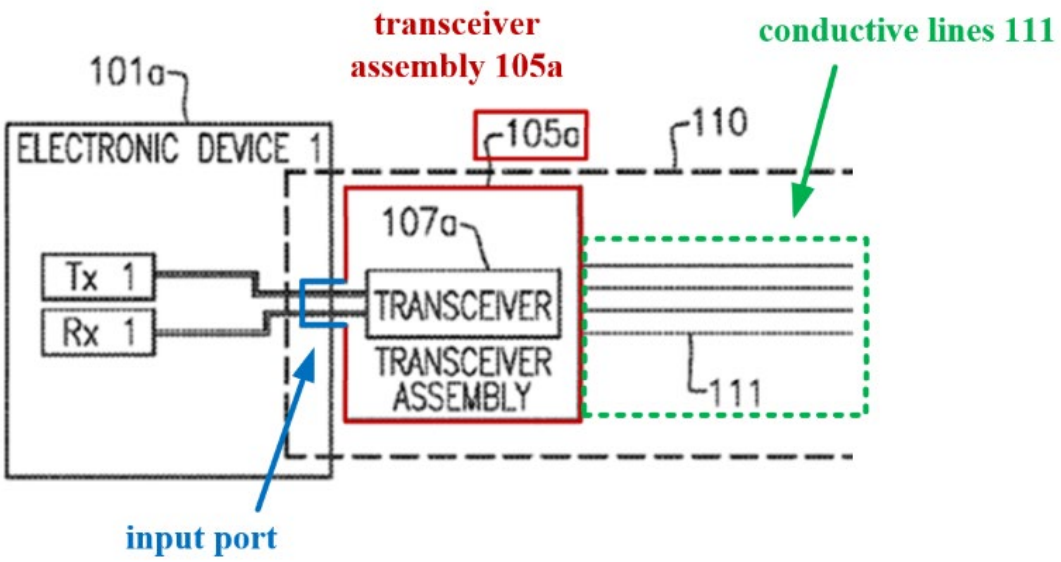


FIG.2A

112. An active cable's electronic components improve signal quality. Lugthart-706, 14:29-31. The transceiver assemblies 105a, 105b include transceivers 107a, 107b, respectively. Lugthart-706, Fig. 2A, 14:47-53. Each transceiver assembly has a "host side" electrically connected to a host (termed an "electronic device") and a "line side" electrically connected to one end of the cable's conductive lines 111. Lugthart-706, 14:34-38, Fig. 2A (annotated detail below).

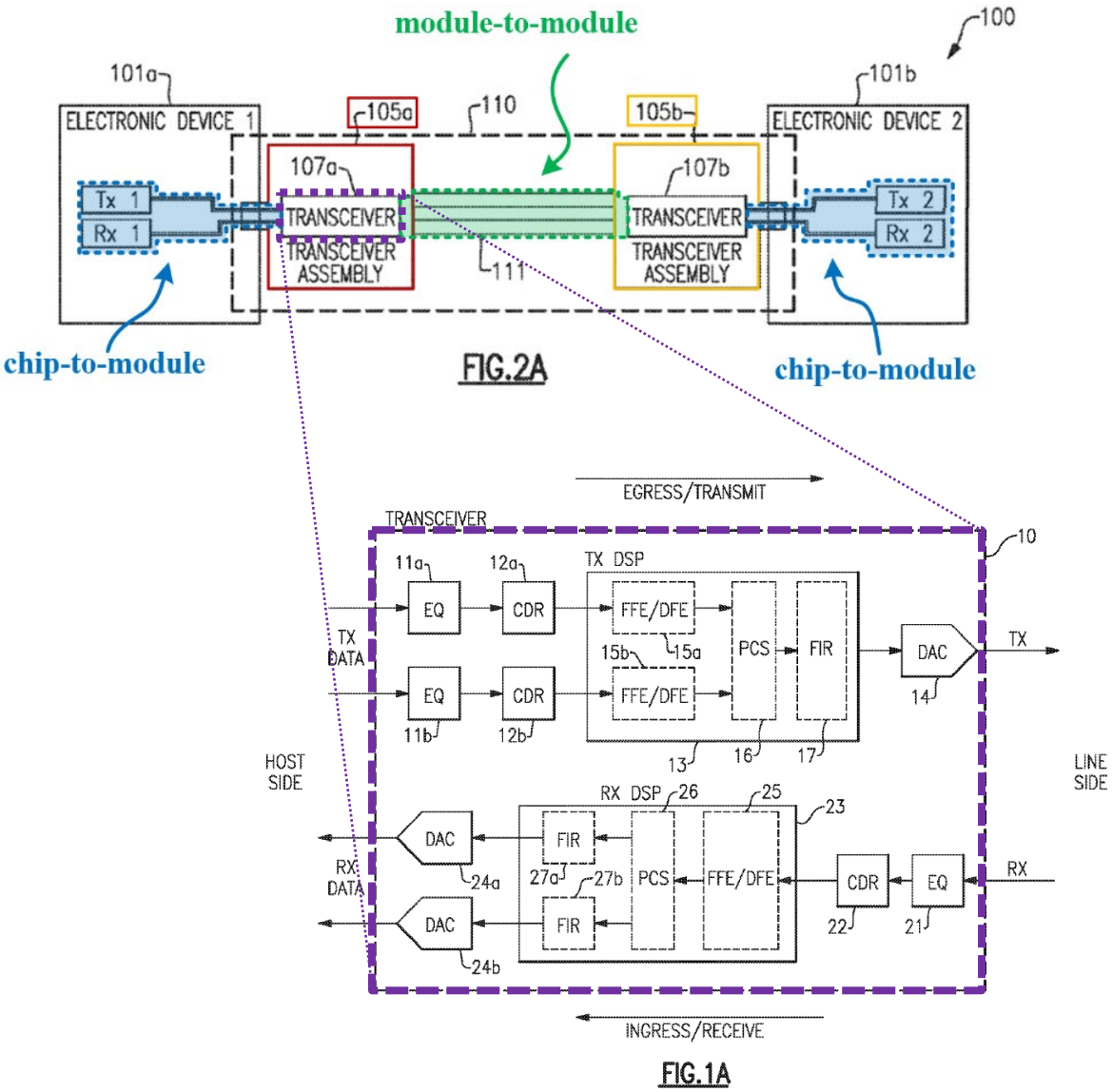


Lugthart-706, Fig. 2A (annotated detail)

113. Each transceiver assembly's input port comprises a connector, such as an industry standard SFP or QSFP connector, that "is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable." Lugthart-706, 15:42-52, Figs. 2A, 17A, 17B, 18.

114. Lugthart-706's transceiver 107a/107b can perform pre-equalization (which Lugthart-706 calls pre-emphasis) on signals transmitted over the cable's conductive lines 111, as well as on signals transmitted to electronic devices 101a/101b. Lugthart-706, 23:62-64, 29:23-28.

115. Figure 1A's transceiver 10 illustrates one embodiment of Figure 2A's pluggable module transceiver 107a/107b. Lugthart-706, 14:47-53.



Lugthart-706, Figs. 1A, 2A (annotated)

116. Transceiver 10's "EGRESS/TRANSMIT" path through DSP 13 performs digital signal processing, including retiming, on the multi-lane TX DATA signal before transmitting the TX signal over conductive lines 111. Lugthart-706, Figs. 1A, 2A, 15:64-16:3, 21:35-38. Finite impulse response (FIR)

filter 17 is a transmit filter that performs pre-emphasis on the re-timed TX signal transmitted over conductive lines 111. Lugthart-706, 16:11-15, 29:23-28.

117. Lugthart-706 configures FIR filters using "tap coefficients," and the filters "perform emphasis on the signal to compensate for channel losses." Lugthart-706, 22:13-16, 23:59-64. "Pre-emphasis" and "pre-equalization" were used interchangeably in the art. EX1050 ("Raghavan"), 2:39-41 (describing a "technique for combating ISI [inter-symbol interference]… known as 'pre-emphasis', or pre-equalization"); EX1017 ("Schmidt"), 7:54-55; EX1018 ("Zerbe-063"), 3:24-27; EX1019 ("McCall"), 5:4-8. The pre-equalization compensates for anticipated channel distortion on a transmitted signal.

118. On the "INGRESS/RECEIVE" path, DSP 23 performs digital signal processing on signal RX received from the cable before that signal is transmitted to the host (electronic device 101a/101b in Figure 2A). Lugthart-706, 8:26-32, 9:38-51, Fig. 1A. DSP 23 includes FIR filters 27a/27b. Lugthart-706, 9:38-46. DSP 23 uses these FIR filters for "adaptive and configurable signal conditioning features such as… output pre-emphasis" on the signal transmitted to the host. Lugthart-706, 9:52-55, 29:23-28. In one embodiment, Lugthart-706 describes a five-tap FIR 17 and 27a/27b. Lugthart-706, 22:12-16.

2. Discussion of Gorecki-617 (EX1006)

119. Gorecki-617 describes systems and methods for transmitter equalization (e.g., "pre-emphasis equalization" or pre-equalization) by FIR transmit filters in high-speed digital communication systems, including cables. Gorecki-617, Abstract, 1:15-17, 1:59-2:11, 19:61-66. Gorecki-617 explains that it was known to digitally equalize data, thus implementing FIR filters in digital signal processing, before converting the equalized signals to analog. Gorecki-617, 16:40-46.

120. Gorecki-617 describes storing FIR filter tap coefficients in non-volatile memory ("NVM") including writable NVM ("ROM, PROM, EPROM, EEPROM or the like"). Gorecki-617, 7:18-43, 10:37-51, 17:41-51. EEPROM is electrically erasable programmable read only memory that is re-writable non-volatile memory ("NVM"). Lauby, [0081] ("nonvolatile memory can include… electrically erasable PROM (EEPROM)"); Bakx, 2:53-54 ("EEPROM is a non-volatile memory"); EX1047 ("Lindsay"), [0012] ("non-volatile memory may include… an EEPROM"). Flash memory was another well-known rewritable non-volatile memory (e.g., "EEPROM or the like") conventionally used with transmit FIR filters. E.g., Hsu-140, 3:42-4:2 ("Any type of NVRAM can be used as the rewritable non-volatile storage, so long as [it] is of the type suitable for integration on an integrated circuit.").

121. Gorecki's FIR filter taps are programmable. Gorecki-617, 3:42-45. "In this way, the transmitter may access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization." Gorecki-617, 7:31-33. Gorecki-617 describes a "controller" that adjusts equalizer tap coefficients by distributing filter coefficient values from NVM (including EEPROM) to a transmitter to implement FIR filter taps "within the equalization circuitry." Gorecki-617, 7:9-17.

122. Gorecki-617 also explains the filter coefficients stored in its non-volatile memory can be "re-programmed." Gorecki-617, 7:18-26, 20:41-43 (claim 2, "pre-programmed [tap] coefficient… is… re-programmed"). The filter coefficients can also be "fine-tuned" using adaptive algorithms. Gorecki-617, 7:50-61, 10:26-51.

3. Discussion of the Lugthart+Gorecki Combination

123. As noted above in Sections VI.A.1-VI.A.2, both Lugthart-706 and Gorecki-617 teach active electrical cables with signal conditioning functions. I further reference this combination as "Lugthart+Gorecki."

a. Reasons to Combine

124. While Lugthart-706 describes multi-tap transmit filters (FIR 17), it does not explain how to set the equalizer or transmit filter coefficients and thus

leaves the implementation details to the POSA. E.g., Lugthart-706, Fig. 2A, 22:12-16 (describing five-tap filter).

125. A POSA would have had reasons to configure the transmit filters of Lugthart-706 based on Gorecki-617's approach of using coefficients stored in nonvolatile memory. Gorecki-617 is directed to "enhancing the performance of high-speed digital communications through a communications channel." Gorecki-617, 1:15-17, 6:4-5, 19:61-66. Gorecki-617 explains that "[t]he extent of equalization introduced by the circuitry, however, may vary between equalization circuitry of each transmitter in the high-speed digital communication system." Gorecki-617, 8:66-9:2. For each transmitter, "the amount of equalization may be adjusted or controlled by… changing the coefficients of the taps[.]" Gorecki-617, 9:37-40. The equalizers are "configured to introduce compensation that is ideally the inverse of the effects caused by the communications channel." Gorecki-617, 9:8-10. Gorecki-617 achieves this result by storing and loading equalization parameters, including transmit filter coefficient values, from "ROM, PROM, EPROM, EEPROM or the like" (i.e., *nonvolatile memory*). Gorecki-617, 7:25. Each of these is an example of non-volatile memory, meaning that the memory retains stored values even when no power is applied.

126. A POSA, therefore, would have understood that "performance of high-speed digital communications" could be enhanced by *using transmit filter coefficient values stored in nonvolatile memories*.

127. Having a transmitter "access the memory" to retrieve the filter coefficient values and program an equalizer (including setting pre-equalizer filter taps) with those values when Lugthart-706's transceiver is powered up, initialized, or re-initialized was a conventional and convenient technique for setting filter coefficients while persisting the coefficient values for use as power to the AEC transceiver was cycled. Gorecki-617, 7:18-42. Cycling AEC power merely means turning off/on and in Gorecki-617's system the coefficient values would remain in NVM after powering the cable transceivers back on.

128. A POSA would have understood that the controller that Gorecki-617 describes distributing filter tap coefficients to a transmitter to set taps by user programming would also have been a conventional way to implement that transmitter's memory access and setting programmable FIR filter taps. Gorecki-617, 7:1-17; EX1014 ("Hsu-140"), 4:25-38, 9:54-62; EX1020 ("Boccaccio"), Fig. 6 (micro-controller 68, EEPROM 70), [0049]-[0050] (programmable equalizer 56 includes on-board microcontroller 68 that sets equalizer parameters after power-up using values stored in non-volatile memory 70).

129. Providing Lugthart-706's transceiver with pre-set filter coefficient values in non-volatile memory would have allowed setting the AEC with initial coefficient values determined at manufacture and/or default pre-set coefficient values for various chip-to-module channel models for host devices that could be used with the AEC.

130. The resulting Lugthart+Gorecki combination would have combined familiar elements (Lugthart-706's equalizer and FIR filters with Gorecki's controller, EEPROM or the like, and techniques for programming filter coefficient values from such memory) according to known methods (as demonstrated by Gorecki-617) yielding no more than predictable results.

131. Lugthart+Gorecki also would have arranged known elements with each performing the same function it had been known to perform.
A POSA would have recognized that Gorecki's coefficient storage and filter programming techniques could improve Lugthart-706's equalization circuitry in the same way that they improved Gorecki-617's equalization circuitry.

b. Reasonable Expectation of Success

132. A POSA would have had a reasonable expectation of success achieving Lugthart+Gorecki because the combination used known components with known filter programming and non-volatile coefficient value storage techniques that were within the POSA's ordinary skill and conventionally used for

pre-equalization. Gorecki-617, 16:40-46 (describing digital pre-equalization); Lugthart-706, 8:33-39, 15:30-52, 22:12-16, 29:6-20; Gorecki, 6:39-67; 7:18-49.

133. As Hsu explains, for example, "[f]lash memory is a non-volatile random access memory (NVRAM) suitable for use as the rewriteable non-volatile storage to store updated control information for operating the FIR transmitter. … Any type of NVRAM can be used as the rewriteable non-volatile storage, so long as such NVRAM is of the type suitable for integration on an integrated circuit chip." Hsu-140, 3:42-4:3.

4. Mapping of Lugthart+Gorecki to claims 1-6, 8-13, and 15-19

a. Claim 1

i. Preamble [1.PRE]: A cable that comprises:

134. Lugthart+Gorecki meets [1.PRE] because Lugthart-706 describes "an electrical cable including one or more pairs of differential micro coaxial cables or conductors" to implement a "high-speed communication link between first and second electronic devices." Lugthart-706, Fig. 2A (cable 110), 6:65-7:20, 14:7-31, 15:42-47.

ii. Limitations [1.a]/[1.b]

[1.a]: a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

[1.b]: a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and

135. Lugthart+Gorecki meets [1.a] and [1.b] as shown below.

(1) *DRR Device*

136. The '233 Patent defines "a data recovery and re-modulation (DRR) device" as "a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams." EX1001, 3:51-55. The transceivers of Lugthart-706 have these characteristics and are *DRR devices*.

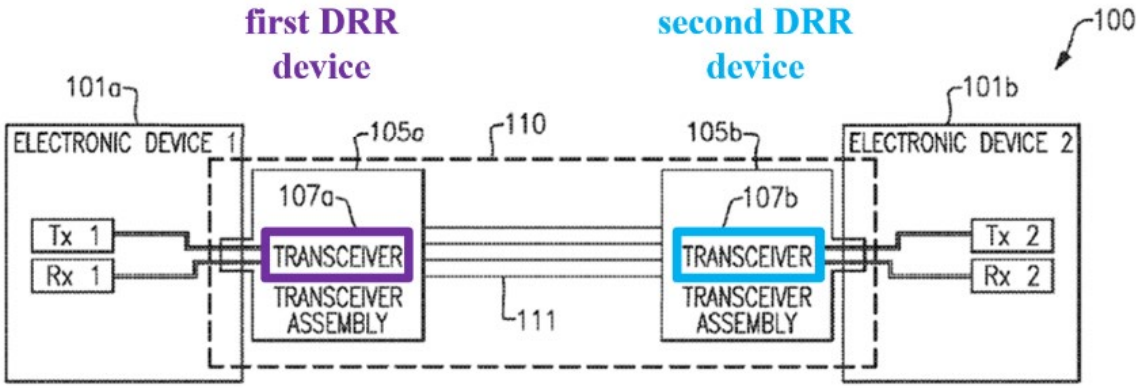
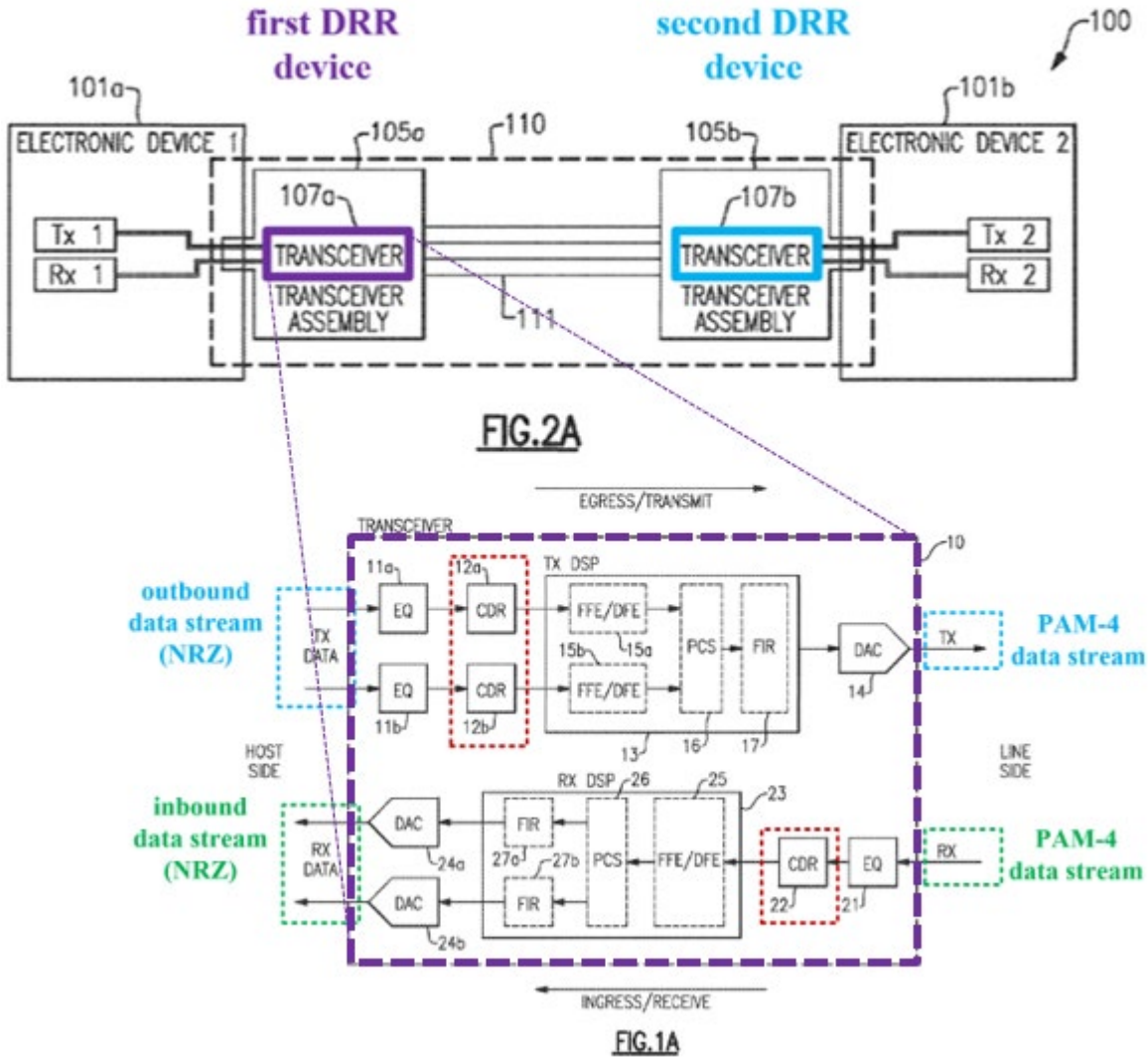


FIG.2A

137. Lugthart-706 discloses *a first DRR device* and *a second DRR device* because its active cable includes "a pair of ***transceivers*** provided at respective ends

of the cable." Lugthart-706, 6:65-67; *id.*, Figs. 1A (transceiver 10), 1B-1C, 2A (annotated above showing transceivers 107a/107b), 8:8-60 (describing transceiver 10). These transceivers are ***powered***. Lugthart-706, 14:7-53 ("cable 110… includ[es] actively powered componentry for improving performance of the cable 110").



138. Lugthart-706's transceiver 10 is an embodiment of transceivers 107a/107b. Lugthart-706, Fig. 1A (annotated above), 8:8-12. CDR 12a/12b and

22 “perform clock and data recovery operations” on respective signals—“TX Data” (outbound data stream) from the host (CDR 12a/12b) and “RX” from the line (CDR 22). Lugthart-706, Figs. 1A (above), 2A, 9:26-37, 33:3-8.

139. As explained below transceiver 10 ***remodulates*** host-side non-return-to-zero (NRZ) “TX Data” (*outbound data stream*) to a four-level pulse amplitude modulation (PAM-4) “TX” data stream for transmission over the cable, and vice-versa. Lugthart-706, 7:8-22, 8:40-60; 13:25-27. A POSA would have understood “remodulation” as including converting data from NRZ to PAM-4. Transceivers 107a and 107b are a *first* and *second DRR device*, respectively.

(2) *inbound and outbound multi-lane data streams*

140. The ’233 Patent defines *inbound* and *outbound* from a ***host’s*** viewpoint, e.g., “***inbound*** data streams ***to the host interface***” and “***outbound*** data streams ***from the host interface***.” EX1001, 3:57-60, 4:47-52. Like the claims, Lugthart-706 defines data streams and communication paths from the ***host’s*** perspective.

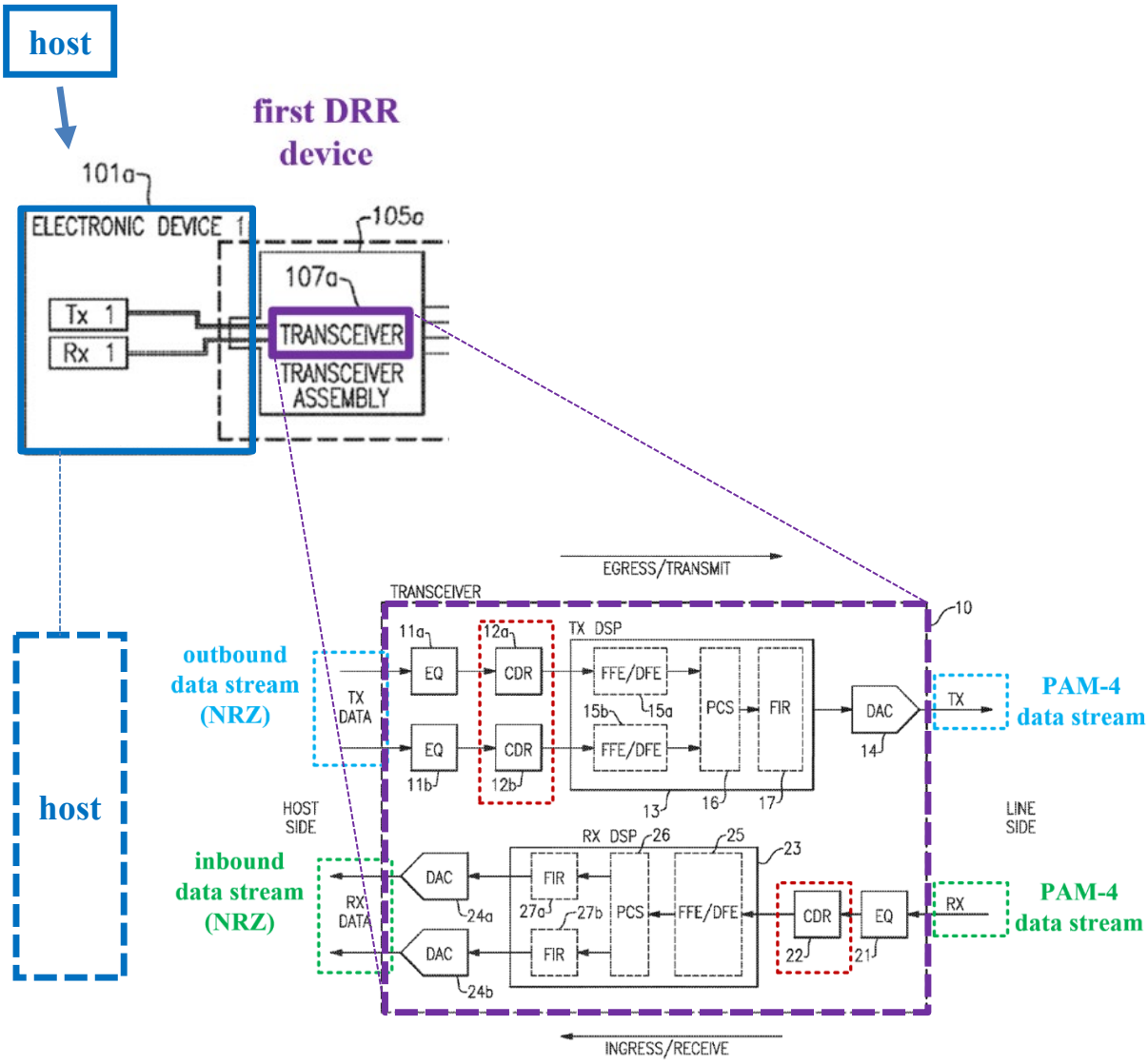


FIG.1A

141. The RX and TX DATA indicated on the host (left) side of Figure 1A are *inbound* and *outbound data streams*.

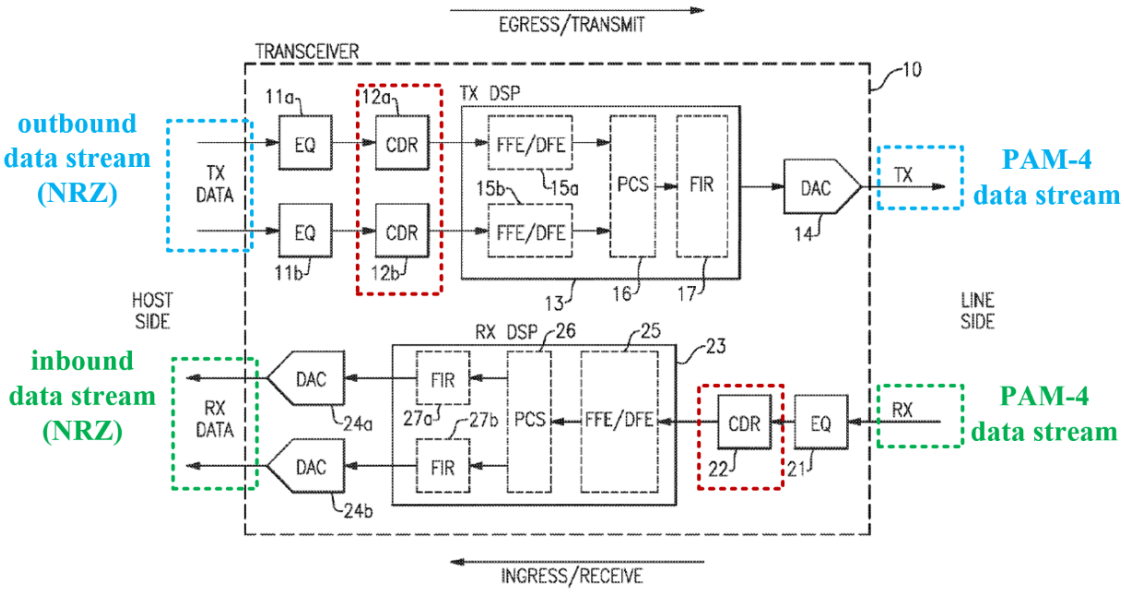


FIG. 1A

142. A POSA would have understood the multiple arrows for each data stream to represent multiple lanes. Lugthart-706 uses the term "lane" in a way that makes clear that the multiple arrows in Fig. 1A indicate multiple lanes. E.g., Lugthart-706, 13:52-57 ("each of the transceivers described above as implementing a multiplexing function in the egress/transmit direction will be capable of performing a corresponding demultiplexing function in the ingress/receive direction to generate the ***appropriate number of host-side lanes***."), Figs. 1A-1D, 13:13-48 (describing configurations with different numbers of lanes at the host-side and/or line-side).

143. This usage is consistent with the Ethernet standard in which a "lane" is a "bundle of signals" that "communicate a quantum of data and/or control

information between two end-points." EX1007, IEEE Std. 802.3-2015, 86 (§1.4.246).

144. This usage is also consistent with the '233 specification, which describes "converting 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa," as is depicted in FIG. 1A of Lugthart-706. *Compare* EX1001, 4:44-45; Lugthart-706, 8:50-60.

145. The '233 specification also refers to a "unidirectional connection" and defines a "***bidirectional*** lane" as "formed by two unidirectional connections" wherein one is for transmit (TX) and the other for receive (RX). EX1001, Fig. 3A, 5:16-24 (bidirectional lanes LN0-LN3). Accordingly, one of the arrows for the TX DATA and one for the RX DATA in Lugthart-706 Fig. 1A represents a bidirectional *lane* as that term is used in the specification.

146. The specification uses a *multi-lane data stream* to describe multiple lanes that each carry a portion of a data stream, as is shown in Lugthart-706 Figure 1A. E.g., EX1001, 2:18-20 (describing "[a DRR] device… converts ***a multi-lane data stream*** from the first host interface port").

147. Lugthart-706 discloses *inbound and outbound multi-lane data streams* because its transceiver receives TX DATA (*outbound data stream*) ***from a host*** in multiple lanes on the "EGRESS/TRANSMIT" path. E.g., Lugthart-706, Figs. 1A (TX data on two lanes), 1C-1D (showing multiple host-side differential TX lanes),

Fig. 2A, 7:24-27, 8:13-32, 13:25-27. Transceiver 10 transmits RX DATA (*inbound data stream*) ***to a host***—on the "INGRESS/RECEIVE" path—in multiple lanes. Lugthart-706, Figs. 1A (RX DATA on two lanes), 1C-1D (showing multiple host-side differential RX lanes), 2A, 7:24-27, 8:13-32, 13:25-27.

(3) *end connector plug*

148. The "end connector plug" is capable of being inserted in a "host interface port." Limitation [15.a]; EX1001, 2:16-17. The '233 specification describes a connector terminating each end of a cable as including a "plug" (e.g., *end connector plug*) adapted to mate with a host device's Ethernet port (e.g., *host interface port*). EX1001, Figs. 2 (connector 100), Fig. 3B (connector 100/101, plug 200/201, host device 302/304), 4:47-54 ("Connector 100 includes a plug 200 adapted to fit a standard-compliant Ethernet port in a first host device 302[.]"), 7:14-15 ("The connectors 100, 101, have plugs 200, 201 that mate with the receptacles 336 of the two host devices 302, 304.").

149. Lugthart-706's cable has transceiver assemblies 105a/105b at respective ends of cable 110. Lugthart-706, 6:65-67, 15:42-47, Fig. 2A (annotated below). "Each of the transceiver assemblies 105a and 105b ***has an input port*** that is ***configured to mechanically and electrically connect***, e.g., in a releasable fashion, ***to a corresponding port***… ***on the respective electronic device*** 101a, 101b[.]" Lugthart-706, 15:42-47.

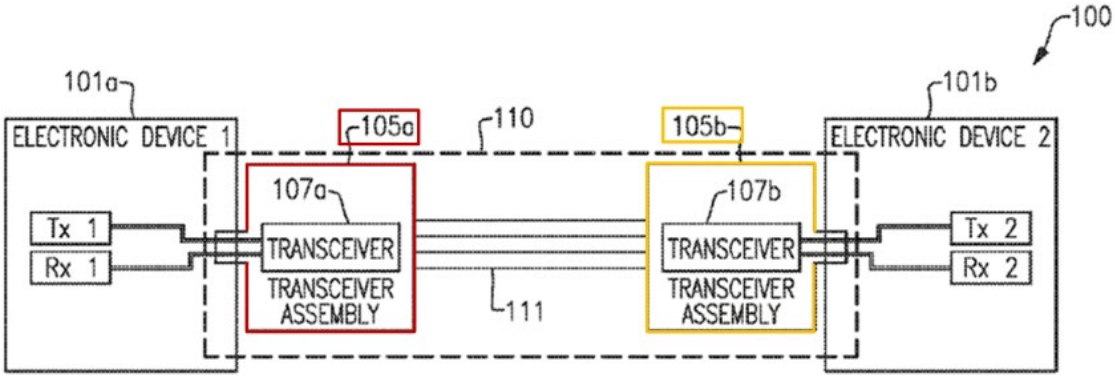


FIG.2A

150. Lugthart-706's input port for each transceiver assembly 105a/105b is a *first/second end connector plug*, respectively, because it mechanically and electrically mates with the corresponding port on an electronic device (e.g., host device) just like plug 200 in the '233 Patent. POSAs also understood that the corresponding port in each electronic device was conventionally a "standard-complaint Ethernet port" (EX1001, 4:47-54) because Lugthart-706 describes the input port as comprising standardized connectors including SFP and QSFP that were typically used for Ethernet-complaint connections and had *plugs* for mating with an electronic device's interface port. Lugthart-706, 15:47-52, 15:59-63; EX1022, 26-27; EX1023("SFF-8436"), 24.

(4) *host interface port*

151. The '233 Patent describes "inserting [an] end connector plug of a cable into a… host interface port[.]" Limitation [15.a]; EX1001, 2:16-17.

152. Lugthart-706's electronic device is a *host* device. Lugthart-706, 14:14-15 ("first and second electronic devices 101a, 101b, which can also be referred to herein as host devices."). The electronic device interface is a *host interface*. Lugthart-706, 3:31-34 ("a communication device includes a host interface"). The transceiver assembly 107a/107b input port "***mechanically and electrically connect[s]***, e.g., in a releasable fashion, ***to a corresponding port***… ***on the respective electronic device*** 101a, 101b[.]" Lugthart-706, 15:42-47. The "corresponding port" on electronic device 101a/101b is the *first/second host interface port*, respectively, because it receives and electrically and mechanically connects the transceiver assembly 107a/107b input port (e.g., *first/second end connector plug*).

153. When used Lugthart-706's transceiver 107a *exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug* because as explained above, e.g., Figure 1A, when connected to a host device the transceiver electrically receives two lanes of TX data (*outbound multi-lane data stream*) from, and transmits two lanes of RX data (*inbound multi-lane data stream*) to, electronic device 101a (host device) through the "corresponding port" (*first host interface port*) that electrically connects the transceiver assembly 107a's input port (*first end connector plug*), meeting [1.a]. Lugthart-706, 8:8-32 (transceiver "receive[s] host side transmit data," DAC

24a/24b "generate host side receive data"), 8:33-39 ("transceiver 10 can be used to support data transfer between various electronic devices"). Transceiver 107b in transceiver assembly 105b provides the same functionality with electronic device 101b, meeting [1.b].

154. Thus, it is my opinion that Lughtart+Gorecki meets Limitations [1.a]-[1.b].

iii. Limitation [1.c]: electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

155. Lugthart+Gorecki meets [1.c] because Lugthart-706 describes cable 110 comprising conductive lines 111 (*electrical conductors*) connecting transceivers 107a/107b. Lugthart-706, Fig. 2A (annotated below), 14:29-42, 16:11-20 (copper conducting lines 111); 19:2-6 (lines 111 can be twinaxial cable providing differential signaling).

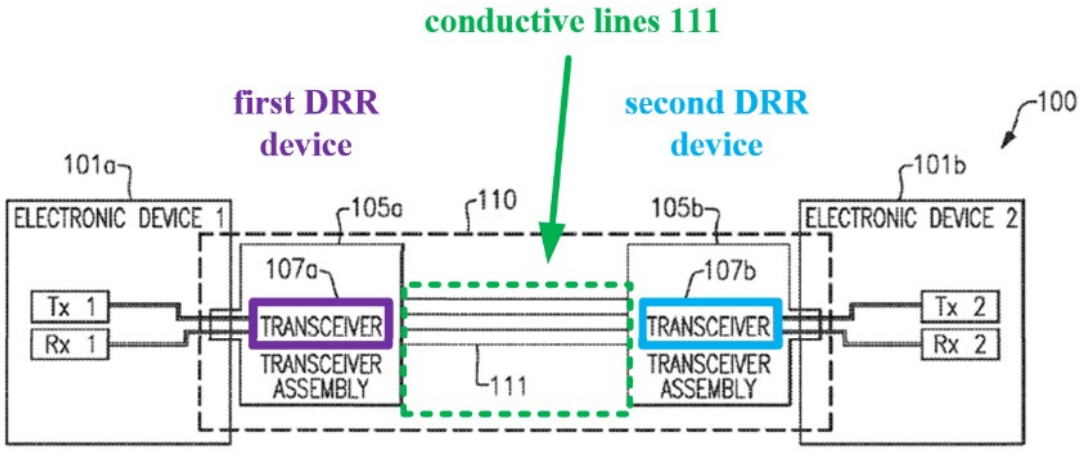


FIG.2A

156. The ’233 Patent describes electrical signals “transiting the cable conductors” as “electrical transit signals.” EX1001, 2:5-7, 4:17-18. Lugthart-706’s conducting lines 111 conduct electrical signals between transceivers 107a and 107b. E.g., Lugthart-706, 14:7-42, 16:11-15 (“electrical conducting lines 111… can transport electrical signals” between electronic devices 101a/b), 19:2-6 (twinax lines 111 support differential signaling).

157. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [1.c].

iv. Limitations [1.d]/[1.e]

[1.d]: the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

[1.e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

158. As explained *supra* §VI.A.4.a.ii (Limitation [1.a]), Lugthart-706 converts multiple NRZ data streams from a host to, e.g., re-timed NRZ or PAM-4 data stream(s) over the cable, and the reverse for RX signal from the cable to RX DATA transmitted to the host device. E.g., Lugthart-706, 8:40-60, 13:13-48. This matches an example of converting in the specification. EX1001, 4:44-45.

159. Lugthart+Gorecki meets [1.d] because—when used—Lugthart-706’s transceiver 107a receives multiple signals from a host device comprising “host side

transmit data (TX DATA)," e.g., *outbound multi-lane data streams*. Lugthart-706, Figs. 1A (annotated below), 6A, 8:13-17, 30:23-25; *supra* §VI.A.4.a.ii (Limitation [1.a]).

160. Transceiver 107a "converts between" the TX DATA from the *first* host (electronic device 101a)—received over the *first host interface port* (*supra* § VI.A.4.a.ii (Limitation [1.a])—and the TX signal (e.g., *electrical transit signal*, (*supra* § VI.A.4.a.iii (Limitation [1.c]) transmitted over the cable by equalizing the TX DATA signal received (equalizers 11a/11b), performing a CDR function (CDR 12a/12b), conditioning and recovering the TX DATA (DSP 13), and multiplexing and remodulating the TX DATA into the TX signal (DSP 13, DAC 14). Lugthart-706, Figs. 1A (annotated below), 2A, 6A, 8:19-22, 9:52-55, 16:11-15, 30:25-55, *generally* 7:66-10:27 (describing transceiver).

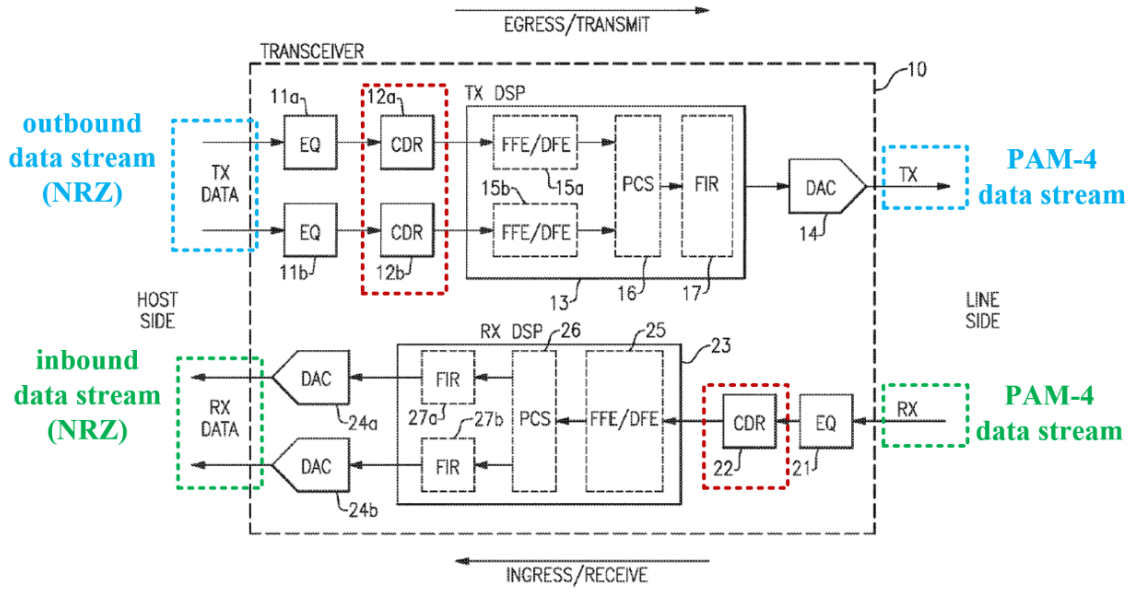


FIG.1A

161. The receive path electronics perform the same operations—in a reverse order—to convert between the RX signal from the cable to the RX DATA signal transmitted to the host device. The transceiver signal conversion is *for the first host interface port* because as explained above transceiver 107a receives TX DATA from, and transmits RX DATA to, electronic device 101a via the *first host interface port*. Lugthart-706, Figs. 1A ("INGRESS/RECEIVE"), 2A, 6A, 9:10-51, *generally* 7:66-10:27 (describing transceiver).

162. Lugthart-706 transceiver 107b provides the same functionality for electronic device 101b, meeting [1.e].

163. Thus, it is my opinion that Lugthart+Gorecki meets Limitations [1.d]-[1.e].

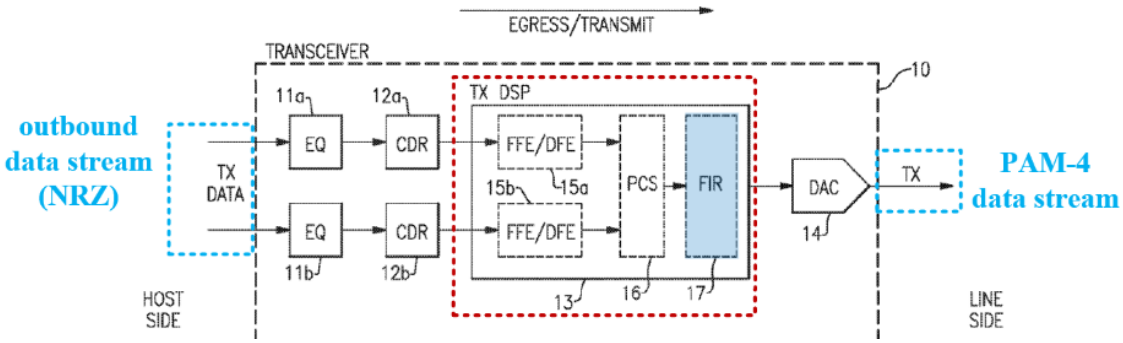
v. Limitation [1.f]: the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

(1) pre-equalization

164. Lugthart+Gorecki meets [1.f] because Lugthart-706's transceivers 107a/b provide "adaptive and configurable signal conditioning features such as… ***output pre-emphasis***" on the TX signals transported by conductive lines 111 (e.g., *electrical transit signals*, *supra* §VI.A.4.a.iii (Limitation [1.c])). Lugthart-706, Figs. 1A, 2A, 16:11-15, 23:59-24:2, 29:23-28. POSAs understood that "pre-

emphasis" and "pre-equalization" have the same meaning. Raghavan, 2:39-41 (describing a "technique for combating ISI… known as 'pre-emphasis', or pre-equalization"); Schmidt, 7:54-55; Zerbe-063, 3:24-27; McCall, 5:4-8.

165. Transceivers 107a/107b provide pre-equalization in DSP 13 using finite impulse response (FIR) filter 17. FIR filter 17 is a *transmit filter* because DAC 14 converts the FIR 17 output to an analog signal that is transmitted on the line side. Lugthart-706, Fig. 1A (annotated detail below), 23:13-17, 23:59-24:2.



166. FIR filter 17 "perform[s] emphasis on the signal to compensate for channel losses," e.g., it *pre-equaliz[es]* the signal that—when transmitted over the cable after DAC 14—is the *electrical transit signal*. Lugthart-706, 23:62-64. FIR filter 17 forwards conditioned signals to DAC 14 for transmission over cable 110 and conductive lines 111. Lugthart-706, Figs. 1A, 2A, 8:19-22, 16:11-15, 23:59-24:2. The TX signals transmitted on the cable's conductive lines are *electrical transit signals*.

167. The filter 17 tap coefficients are *transmit filter coefficient values*. The '233 Patent states that "equalization parameters may include filter coefficient

values for pre-equalizer filters[.]" EX1001, 5:45-48, 8:15-26 (during training adaptation adjusts filter coefficient values). Lugthart-706 explains that FIR filter 17 can be "a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3," Lugthart-706, 22:12-16, while Gorecki-617 provides that "tap weights or coefficients (values) may be determined or controlled[.]" Gorecki-617, 6:56-57.

(2) non-volatile memory

168. Lugthart+Gorecki uses Gorecki-617's teaching to store filter coefficient values in non-volatile memory ("NVM"), which can include EEPROM and the like such as flash memory, and use those values to set filter coefficients to provide pre-equalization. Hsu-140, 3:42-4:2; Gorecki-617, 7:18-33 ("[I]nformation representative of… ***the coefficients of the tap(s)*** may be ***stored*…** ***in… for example… ROM or EEPROM.*** In this way, the transmitter ***may access the memory to retrieve the necessary information*** during start-up/power-up, initialization or re-initialization."); *supra* §VI.A.2 (discussing NVM as described in Gorecki-617). Lugthart+Gorecki uses Gorecki-617's teaching to program filter 17 coefficients using the values stored in NVM to pre-equalize the TX signal in transceiver 107a and 107b, thus meeting [1.f]. *Supra* §VI.A.3 (combination).

169. Thus, it is my opinion that Lugthart+Gorecki meets [1.f].

b. Claim 2: The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

170. Lugthart+Gorecki meets claim 2 because Gorecki-617 teaches "[I]nformation representative of… ***the coefficients of the tap(s)*** may be ***stored*…** ***in… for example… ROM or EEPROM.*** In this way, the transmitter ***may access the memory to retrieve the necessary information*** during start up/power-up," which is *a power-on event*. Gorecki-617, 7:18-33, 16:47-53; *supra* §VI.A.3 (combination). Gorecki-617 describes a "controller" that "distribute[s] to the transmitter" the filter coefficients thereby configuring FIR filter 17 for pre-emphasis at this power-on event. Gorecki-617, 7:4-17; 7:26-33. For transceiver 107a this is a *first controller*, so that Lugthart+Gorecki meets claim 2.

171. Thus, it is my opinion that Lugthart+Gorecki meets claim 2.

c. Claim 3: The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

172. The analysis treats "*transmit coefficient values*" as referring to [1.f] "*transmit filter coefficient values*," as the term otherwise has no antecedent basis.

173. Lugthart+Gorecki meets claim 3 because Lugthart-706's FIR 17 in transceivers 107a and 107b use *transmit filter coefficient values* that have been stored in memory. *Supra* §§VI.A.3 (combination), VI.A.4.a (claim 1).

174. Like the ’233 Patent specification, Gorecki-617refers to storing of values in memory as programming. Gorecki-617, 7:1-33 (“the adjustment or control of the taps of the equalization circuitry may be by the user via ***programming***… coefficients of the tap(s), and/or the pulse durations of the tap(s) may be ***pre-programmed***”); EX1001, 11:3-6 (“the automated tester equipment ‘burns’ the flash memory or otherwise ***programs*** the initial default values of the filter coefficients[.]”).

175. Gorecki-617 teaches that the programmed memory “may reside on the integrated circuit containing the transmitter, receiver or transceiver.” Gorecki-617, 7:43-49. A POSA would have found such an implementation of Lugthart+Gorecki obvious, as Lugthart-706 already includes programmable circuity. Lugthart-706, 30:42-44 (“Programmable chip sets, physical coding sublayer (PCS) blocks, FPGAs, FIR filters can be used to condition and multiplex the digital data signal.”). As the *first and second DRR devices* include the transceivers, a POSA would have understood that Lugthart+Gorecki meets “*the first and second DRR devices are programmed*.”

176. This programming is done *to use the transmit coefficient values* when *power is supplied to the first and second end connector plugs*. In Lugthart+Gorecki, stored FIR filter coefficients are retrieved from the nonvolatile

memory at start-up/power-up as taught in Gorecki-617. Gorecki-617, 7:18-33, *supra* §§VI.A.3 (combination), VI.A.4.b (claim 2).

177. Power-up in Lugthart+Gorecki indicates that *power is supplied to the first and second end connector plugs*. POSAs would have understood that power is supplied from a host device when the enclosing connector's connector plug was electrically connected to the host interface port in a corresponding electronic device 101a/b as described *supra* §VI.A.4.a.ii (Limitation [1.a]) because this was conventionally how standardized connectors like QSFP or SFP worked. *E.g.,* Lugthart-706, 15:36-52 (describing connector formats); EX1023, 21 ("A host board together with the QSFP+ module(s) forms an integrated power system. ***The host supplies stable power to the module***."), 22 Fig. 4 ("Recommended Host Board Power Supply Filtering"). Regardless a POSA would have found implementing Lugthart+Gorecki with QSFP connectors powered by a connected host device conventional and an obvious implementation choice.

178. A POSA would have understood that Lugthart+Gorecki uses the transmit coefficient values stored in memory *each time* power is supplied to the first and second end connector plugs. Gorecki-617 teaches that the programmed values can be stored "permanently, semi-permanently or temporarily[.]" Gorecki-617, 7:21. When stored permanently, a POSA would have understood the filter coefficient values to be used *each time power is supplied to the first and second*

end connector plugs. The transceiver filter 17 would behave the same way, with the same coefficients, at each power-up, until the coefficient values stored in NVM were rewritten.

179. Thus, it is my opinion that Lugthart+Gorecki meets claim 3.

d. Claim 4: The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable .

180. A POSA would have had reasons to implement Lugthart+Gorecki by *determin[ing]* and then storing the transmit filter coefficient values in the nonvolatile memories *after assembly of the cable*. As Gorecki-617 teaches, the values should be selected to offset effects of a communication channel. Gorecki-617, 9:8-10 (The equalizers are "configured to introduce compensation that is ideally the inverse of the effects caused by the communications channel."); *supra* §VI.A.2.

181. In Lugthart+Gorecki the communications channel includes the electrical conductors as connected to the *first and second DRR devices*. That communication channel does not exist until the cable is assembled by attaching the first and second DRR devices to the electrical conductors.

182. Accordingly, a POSA would have found it obvious to determine and then store filter coefficients, such as by measuring the effects in that communication channel *after assembly*. Such an approach was known in the art.

Boccaccio, [0033] ("The programming is preferably performed with the cable installed between the actual source and actual sink it will be connecting.").

183. Additionally, Lugthart+Gorecki meets claim 4 because Gorecki-617 describes "the coefficients of the tap(s)… are adjusted or controlled ***during operation*** of the transmitter, for example using an adaptive algorithm." Gorecki-617, 10:27-51, 6:50-53, 17:41-51. Determining values "during operation" happens after cable assembly. Gorecki-617 teaches that the adaptive algorithm—which *determin[es] transmit filter coefficient values*—is performed "after (or during) the performance of an initialization or re-initialization process." Gorecki-617, 7:50-61.

184. Gorecki-617 describes stored coefficient values can be "fine-tuned to enhance the system performance" (Gorecki-617, 7:51-53), and that the values can be "re-programmed" and, for that reason, are stored in writable NVM. Gorecki-617, 7:18-33, 10:37-51.

185. A POSA would have had reasons to implement Lugthart+Gorecki with writable nonvolatile memory, as Gorecki-617 describes NVM including writable NVM ("ROM, PROM, EPROM, ***EEPROM or the like***"). Gorecki-617, 7:24-25, 10:46-47. As explained above (*supra* §VI.A.2 (discussing Gorecki-617)), EEPROM is electrically erasable programmable read only memory. This means that the EEPROM can be re-written.

186. A POSA would have known that flash memory was another well-known rewritable non-volatile memory (e.g., "EEPROM or the like") conventionally used with transmit FIR filters. E.g., Hsu-140, 3:42-4:2 ("Any type of NVRAM can be used as the rewritable non-volatile storage, so long as [it] is of the type suitable for integration on an integrated circuit."). Gorecki-617 describes functions conventionally implemented with writable and nonvolatile memory. A POSA would have understood such memories would be used when the content of those memories is both re-programmed and preserved through "startup/power-up, initialization or re-initialization," as described in Gorecki-617, 7:18-33.

187. Thus, Lugthart+Gorecki would have included writable nonvolatile memory that could be updated with new coefficient values that fine-tuned pre-equalization or equalization with new coefficient values learned through training at manufacture or during usage with a particular device in a particular environment. Lugthart-706, 48:64-49:12, 49:20-34; Gorecki, 7:50-61, 10:37-51; Hsu-140, 3:42-4:2, 9:21-28.

188. Preserving such adapted pre-equalization filter coefficients in writable non-volatile memory like an EEPROM would have ensured that the fine-tuned coefficients remained available after an AEC transceiver—or the host powering it—was power cycled, initialized, or re-initialized. Gorecki-617, 7:31-33 ("In this

way, the transmitter may access the memory to retrieve the necessary information during start up/power-up, initialization or re-initialization.”).

189. Regardless, POSAs would have known that storing updated filter coefficients in Lugthart+Gorecki’s NVM was conventional and desirable so that the adapted coefficient values would be available after power cycling the AEC transceiver by unplugging it from a host device powering it, or power cycling the host device powering the AEC transceiver. E.g., Hsu-140, Abstract (“[D]ata transmitter includes a rewriteable non-volatile storage, operable to be rewritten with control information representing the values of coefficients updated during operation off the FIR driver.”), 2:46-49 (same), 3:45-52 (“Updated values of the coefficients used in the taps of the FIR transmitter 30 are determined and stored to the flash memory 20 during the operation of the FIR transmitter. ***When the FIR transmitter is powered off and back on again, the coefficient values as last updated are available to be retrieved from the flash memory 20 and applied to the taps of the FIR transmitter again.***”).

190. Thus, it is my opinion that Lugthart+Gorecki meets claim 4.

e. Claim 5: The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

191. The ’233 specification parrots the “receiver-based equalization” claim language but does not give examples or explain what it is. E.g., EX1001, 2:42-45,

2:61-63. Regardless, "receiver-based equalization" meant equalizing a received signal to compensate for distortion incurred during transmission. EX1024 ("Shimanouchi"), 10:22-35; EX1025 ("Aziz"), ¶4; EX1026 ("Laturell"), 2:17-21; EX1027 ("Hanumolu"), p.185 (describing "receive-side equalization" suppressing channel loss).

192. A POSA would have had a reason to implement Lugthart+Gorecki in a way that meets claim 5. Lugthart-706's transceiver equalizes signals received over conductive lines 111 (e.g., *electrical transit signals*) using receive path equalizer 21. Lugthart-706, Fig. 1A, 9:10-25 ("receive path equalizer 21 can be used to provide signal equalization to compensate for transmission line losses on the line side" such as "to compensate for high-frequency signal loss by boosting high frequency components of a signal relative to low frequency components of the signal, thereby improving signal fidelity.").

193. As part of the transceivers, receive path equalizers 21 in transceivers 107a and 107b would be in *the first* and *second DRR devices*, respectively. *Supra* §§VI.A.3 (combination), VI.A.4.a.ii (Limitations [1.a]/[1.b]).

194. Receive path equalizers 21 are performing an equalization function analogous to that performed by transmit filters 17. For the reasons explained *supra* §§VI.A.3 (combination), VI.A.4.a.v (Limitation [1.f]) that it would have been obvious to implement transmit filters 17 in Lugthart+Gorecki using coefficient

values stored in nonvolatile memories, it would have been obvious to implement equalizers 21 with *coefficient values stored in the nonvolatile memories*.

195. Both Lugthart-706 and Gorecki-617 suggest that equalizers 21 are, like filters 17, configured to compensate for signal distortion over the cable. Lugthart-706, 22:43-48 ("The equalizer 21 can be configured to compensate for losses occurring during transmission over the cable…."); Gorecki-617, 1:59-67 ("[C]onventional high speed digital baseband communications systems often employ circuitry, for example, a finite impulse response filter ('FIR filter'), ***in the receiver***…. Such circuitry typically includes one or more taps having fixed or pre-programmed 'positions' and coefficients."), 2:17-21 ("***Regardless of where the equalization circuitry is implemented***, the duration of the equalization signal and the relative position or placement of the tap(s) of the equalization circuitry are selected or designed to avoid interference with the signal representative of the transmitted information.").

196. Equalizer 21's equalization functionality depends on filter coefficient settings like transmit filter 17. Hanumolu, pp. 185-198 (describing different receive-side equalization architectures configured with coefficients [C-1, C0, C1]); EX1028 ("Das Sharma"), ¶69 (describing applying coefficients to a receiver's settings to minimize communication data loss).

197. Though Gorecki-617 describes implementing its equalization structure and techniques at a transmitter "may have an advantage," Gorecki-617, 18:47-53, a POSA would have recognized from this statement that implementation in the receiver was also an option, particularly as Gorecki-617 explains implementation more generally in connection with equalization circuitry more generally. Gorecki-617, 2:17-21, 6:14-23 ("The circuitry and techniques include leading and/or trailing taps to reduce, minimize, mitigate or effectively eliminate precursor and/or post-cursor intersymbol interference due to, for example, bandwidth limitations and reflections in high-speed digital communication systems. In this way, the equalization circuitry and techniques may reduce, minimize or eliminate non optimum (e.g., over-equalization) at the boundaries of the data signal (i.e., the symbol)."). A POSA would have considered such an approach would have been applicable to equalizers 21 as they provide equalization in the same way as transmit filter 17.

198. Additionally, a POSA would have understood that the equalization performed at both transmit filter 17 and receive path equalizer 21 should collectively compensate for the effects introduced the communication channel and would have had a reason to set equalization parameters for both in the same way.

199. As explained *supra* §§VI.A.3 (combination), VI.A.4.a.v (Limitation [1.f]), in Lugthart+Gorecki, transmit filter 17 uses coefficient values stored in nonvolatile memory.

200. Thus, it is my opinion that Lugthart+Gorecki meets claim 5.

f. Claim 6: The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

201. Lugthart+Gorecki meets claim 6 because Lugthart-706's active cable includes at least one twin-axial cable, which includes at least two inner conductors that provide differential signaling. Lugthart-706, 19:2-6 ("a cable can include twinaxial cables ('Twinax'), where each Twinax cable includes two inner conductors… [and] the two inner conductors can be configured to implement differential signaling."). The twin-axial cable's inner conductors are *twin-axial conductors*. EX1013 ("Dabiri"), 3:41-45 ("twinaxial (or 'twinax') cables… can each comprise a full-duplex twinax pair of conductors"). The Twinax conductors transport signals (e.g., *electrical transit signals*) between the ends of the cable.

202. Thus, it is my opinion that Lugthart+Gorecki meets claim 6.

g. Claim 8

203. Claim 8 recites a *cable manufacturing method* for the cable in claim 1, comprising three "connecting" steps (Limitations [8.a], [8.b], [8.c]), while

limitations [8.d]-[8.f] repeat cable component capabilities recited in Limitations [1.d]-[1.f].

i. Preamble [8.PRE]: A cable manufacturing method that comprises:

204. Lugthart+Gorecki renders obvious claim 1. *Supra* §VI.A.4.a (claim 1). As shown *infra* §VI.A.4.g.ii (Limitations [8.a]-[8.c]), POSAs would have found it obvious to manufacture claim 1's cable by "connecting" Lugthart-706's transceiver, at each end of a cable, to standard connectors and conductive lines 111, meeting [8.PRE].

ii. Limitations [8.a]-[8.c]

[8.a]: connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

[8.b]: connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

[8.c]: connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

205. Limitations [8.a]/[8.b] recite *connecting a first/second connector plug* to the *first/second DRR device* recited in [1.a]/[1.b]. EX1029, 1.

206. POSAs would have had reasons to "connect" a "connector plug" to Lugthart-706's transceivers 107a/107b (*first/second DRR device*, respectively)

because as explained *supra* §VI.A.4.a.ii (Limitations [1.a]/[1.b]) Lugthart-706 describes each transceiver having "an input port" comprising the *connector plug*.

207. A POSA would have understood that the input port required electrical connection to a transceiver before it could transport signals between a host transceiver and transceiver 107a/107b, to provide the functionality described in Lugthart-706. *Supra* §VI.A.4.a.ii (Limitations [1.a]/[1.b]); Lugthart-706, Fig. 2A (annotated below).

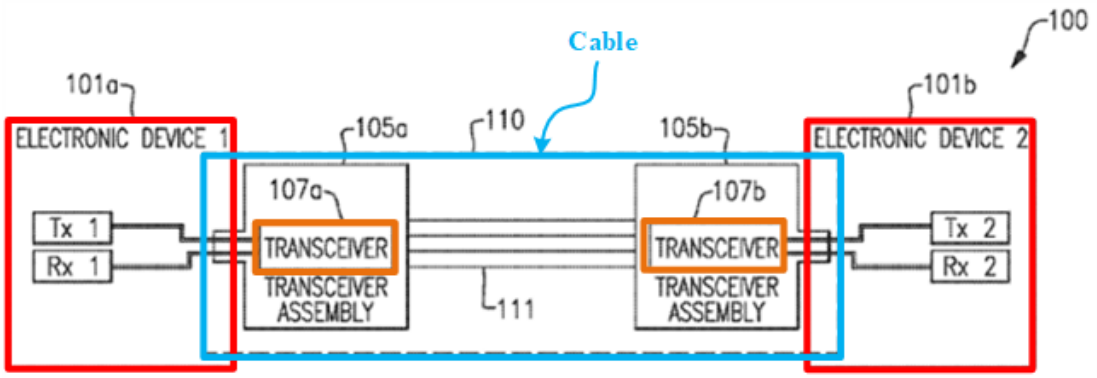


FIG.2A

208. A POSA would have had reasons to "connect" conductive lines 111 to Lugthart-706 transceiver 107a/107b, meeting [8.c], in order to achieve the cable that Lugthart-706 describes wherein lines 111 electrically connect transceivers 107a/107b as explained *supra* §VI.A.4.a.iii (Limitation [1.c]). Lugthart-706, 16:11-15; EX1029, 1.

209. Thus, it is my opinion that Lugthart+Gorecki meets Limitations [8.a]-[8.c].

iii. Limitations [8.d]-[8.f]

[8.d]: the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and

[8.e]: the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,

[8.f]: the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

210. Limitations [8.d]-[8.f] substantively recite the same subject matter as limitations [1.d]-[1.f] in device claim 1. EX1029, 1-2. The [8.d] *multi-lane data streams* are the [1.d] *inbound and outbound multi-lane data streams*. Lugthart+Gorecki meets limitations [8.d]-[8.f] for the same reasons it meets the corresponding limitations below.

Limitation	Corresponding Limitation	Discussion (*supra*)
[8.d]	[1.d]	§VI.A.4.a.iv
[8.e]	[1.e]	§VI.A.4.a.iv
[8.f]	[1.f]	§VI.A.4.a.v

211. Thus, it is my opinion that Lugthart+Gorecki meets Limitations [8.d]-[8.f].

h. Claim 9: The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.

212. Lugthart+Gorecki meets claim 9 for the reasons it meets claim 2. EX1029, 4; *supra* §VI.A.4.b (claim 2). POSAs would have had reasons to "provide" the *first controller* because Gorecki-617 describes a controller that comprises part of Lugthart+Gorecki's cable. Gorecki-617, 7:4-17; 7:26-33; *supra* § VI.A.4.b (claim 2).

213. Thus, it is my opinion that Lugthart+Gorecki meets claim 9.

i. Claim 10: The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

214. Lugthart+Gorecki meets claim 10 for the reasons it meets claim 3 *supra* §VI.A.4.c (claim 3). EX1029, p. 4.

215. Thus, it is my opinion that Lugthart+Gorecki meets claim 10.

j. Claim 11: The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

216. Lugthart+Gorecki meets claim 11 for the reasons it meets claim 4 *supra* §VI.A.4.d (claim 4). EX1029, 4. POSAs would have had reasons to

determine transmit filter 17 coefficient values by training as part of the cable manufacture after connecting transceivers 107a/107b in order to provide the initial pre-set coefficient values that Gorecki-617 describes. Lugthart-706, 4:31-63, 49:3-12, 20-37 (describing training); Gorecki-617, 7:18-33 (describing storing pre-set coefficients); *supra* §VI.A.4.a.v (Limitation [1.f]).

217. As explained *supra* § VI.A.4.a.v (Limitation [1.f]), Lugthart+Gorecki stores preset coefficient values in EEPROM. This renders obvious claim 11.

218. Thus, it is my opinion that Lugthart+Gorecki meets claim 11.

k. Claims 12-13

Claim 12: The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

Claim 13: The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

219. Claims 12-13 recite the same additional limitations as claims 5-6, respectively, and Lugthart+Gorecki meets claims 12-13 for the same reasons. EX1029, 5; *supra* §§VI.A.4.e (claim 5), VI.A.4.f (claim 6).

220. Thus, it is my opinion that Lugthart+Gorecki meets claims 12-13.

l. Claim 15

i. Preamble [15.PRE]: A communications method that comprises:

221. Lugthart+Gorecki meets [15.PRE] because Lugthart-706 describes "methods for high speed communications." Lugthart-706, Abstract, 1:36-37; *see also* Gorecki-617, 1:12-14 ("[T]he invention relates to a system and ***method for providing high-speed digital communications*** through a communications channel.").

ii. Limitation [15.a]: inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

222. Lugthart+Gorecki meets Limitation [15.a] for the reasons it meets Limitations [1.a], [1.c], and [1.d] *supra* §§VI.A.4.a.ii (Limitation [1.a]), VI.A.4.a.iii (Limitation [1.c]), VI.A.4.a.iv (Limitation [1.d]). EX1029, 6. Lugthart-706 describes "Each of the transceiver assemblies 105a and 105b ***has an input port*** that is ***configured to mechanically and electrically connect***, e.g., in a releasable fashion, ***to a corresponding port***… ***on the respective electronic device*** 101a, 101b[.]" Lugthart-706, 15:42-47. POSAs would have had reasons to insert

each input port in a corresponding electronic device's port (*host interface port*) to use the Lugthart+Gorecki cable as shown in Lugthart-706 Figure 2A.

223. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [15.a].

iii. Limitation [15.b]: inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

224. Lugthart+Gorecki meets Limitation [15.b] for the reasons it meets Limitations [1.b], [1.c], and [1.e] *supra* §§ VI.A.4.a.ii-VI.A.4.a.iii (Limitations [1.b]-[1.c]), VI.A.4.a.iv (Limitation [1.e]); EX1029, 6-7. POSAs had reasons to insert transceiver assembly 105b's input port in electronic device 101b's corresponding port (*second host interface port*) for the same reasons described for assembly 105a / electronic device 101a *supra* § VI.A.4.l.ii (Limitation [15.a]).

225. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [15.b].

iv. Limitation [15.c]: the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

226. Lugthart+Gorecki meets Limitation [15.c] for the reasons discussed *supra* § VI.A.4.a.v (Limitation [1.f]); EX1029, 7.

227. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [15.c].

m. Claim 16

i. Limitation [16.a]: The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively,

228. Lugthart+Gorecki meets Limitation [16.a] for the reasons it meets claim 3 *supra* § VI.A.4.c. Each transceiver assembly input port (*connector plug*) is supplied power from the host device that electrically connects to the cable when the input port is coupled to the host device's corresponding receiving port. *Supra* §§VI.A.4.b-VI.A.4.c (claims 2-3). Each transceiver assembly input port (*connector plug*) is connected to the Lugthart+Gorecki controller because as explained for claim 2 *supra* § VI.A.4.b the controller comprises part of the transceiver assembly, which is electrically connected to the input port.

229. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [16.a].

ii. Limitation [16.b]: each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

230. Lugthart+Gorecki Limitation meets [16.b]—for the *first and second controller devices*—for the reasons it meets claim 2 *supra* § VI.A.4.b for the *first controller device*.

231. Thus, it is my opinion that Lugthart+Gorecki meets Limitation [16.b].

n. Claims 17-19

232. Claims 17-19 substantively recite the same subject matter as claims 3-5, respectively. EX1029, 8. Lugthart+Gorecki meets claims 17-19 for the same reasons it meets the corresponding claims below.

Claim	Corresponding Claim	Discussion (*supra*)
17	3	§VI.A.4.c
18	4	§VI.A.4.d
19	5	§VI.A.4.e

233. Thus, it is my opinion that Lugthart+Gorecki meets claims 17-19.

B. Ground 2: The Combination of Lugthart-706, Gorecki-617, and 802.3 Renders Obvious Claims 7, 14, and 20

1. Discussion of IEEE Std. 802.3-2015 (EX1007-EX1012)

234. IEEE Std. 802.3-2015 ("802.3") is the 2015 IEEE Standard for Ethernet and is applicant admitted prior art.[1] EX1001, 1:6-24, 6:33-45; EX1007, 21 (Introduction), 54 ("This standard defines Ethernet local area, access and metropolitan area networks."); EX1001, 1:6-24. IEEE Std. 802.3-2015 was

[1] 802.3-2015 comprises six sections provided as EX1007-EX1012, respectively. EX1007, 21-22 (identifying sections).

adopted on September 3, 2015 and as noted in IEEE Explore it was published March 4, 2016.[2] EX1007; *supra* §V.C.

235. The standard defines a three-tap transmit filter for pre-equalization in electrical backplanes (e.g., 10GBASE-KR). EX1011, Fig. 72-11 ("Transmit equalizer example" with taps c(-1), c(0), and c(1)), 490. 10GBASE-KR is the "IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane." EX1007, 71 (Definitions §1.4.34).

236. The same three-tap transmit filter is used for pre-equalization in a chip-to-module link. EX1012, Fig. 85-3 ("Transmit equalizer functional model" below), 225 ("The 40GBASE-CR4 and 100GBASE-CR10 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. … The requirements for the 40GBASE-CR4 and 100GBASE-CR10 transmit equalizer are intended to be similar to the requirements for 10GBASE-KR specified in 72.7.1.10."); see also Fig. 92-7, 416 (same transmit filter model for 100GBASE-CR4).

[2] *See* https://ieeexplore.ieee.org/servlet/opac?punumber=7428774.

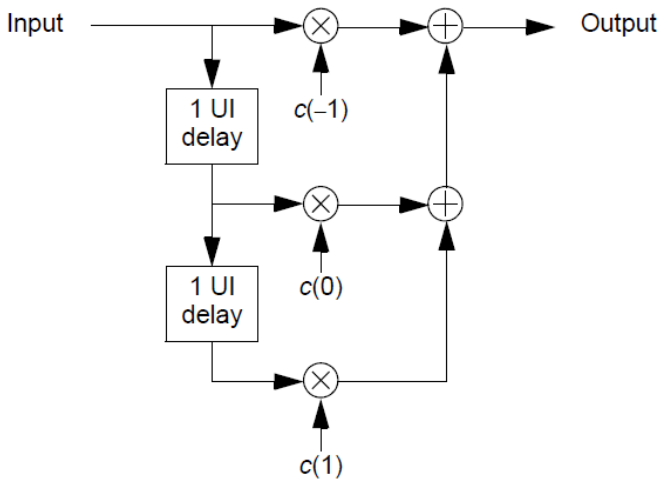


Figure 85–3—Transmit equalizer functional model

802.3, Figure 85-3

237. 40GBASE-CR4, 100GBASE-CR4, and 100GBASE-CR10 are different Ethernet implementations described in the Ethernet Standard. The first number is data rate (40G is 40 Gbps or giga bits per second, also written Gb/s, while 100G is 100 Gbps). The "C" refers to transmission over shielded balanced copper cable, as opposed to transmission over a backplane "K" as specified in 10GBASE-KR (above). The "R" refers to the encoding. The final digit refers to the number of data lanes (e.g., 4 or 10).

238. In particular, 40GBASE-CR4 is the IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of shielded balanced copper cabling. EX1007, 73 (Definitions §1.4.67).

239. 100GBASE-CR4 and 100GBASE-CR10 are the specifications for 100 Gb/s using 100GBASE-R encoding over four (CR4) and ten (CR10) lanes,

respectively, of shielded balanced copper cabling (EX1007, 72 (Definitions "§1.4.53 100GBASE-CR4," "§1.4.54 100GBASE-CR10").

240. Setting the first and third tap coefficient values (e.g., c(-1) and c(1)) to 0, and the second tap coefficient value (e.g., c(0)) to "maximum," passes the input signal without equalization. EX1011, 480 ("If preset is TRUE then the function returns the coefficient value equivalent to no equalization [c(–1) and c(1) coefficients are set to zero, c(0) set to maximum]."). In other words, 802.3 specifically defines transmit filter tap settings that disable pre-equalization.

2. Discussion of the Lugthart+Gorecki+802.3 Combination

241. As noted in Sections VI.B.1-3, Lugthart-706, Gorecki-617, and 802.3 each teach signal processing for network communications.

a. Reasons to Combine Lugthart+Gorecki and 802.3

242. A POSA would have had reasons to use 802.3's teaching to disable transmit equalization in Lugthart+Gorecki (*supra* §VI.A.3) because it was known that disabling filter taps could minimize transceiver power consumption where signal quality was achievable without transmit pre-equalization.

243. Essentially, by disabling the filter tabs, the transmitter transmits each symbol in exactly one symbol time (as opposed to transmitting the delayed versions of the symbol in the successive symbol times), thereby reducing the transmission power.

244. A POSA would have known that disabling a filter tap would have the same effect as setting a filter tap coefficient value to zero as taught in 802.3. For example, Zerbe-063 describes transmit pre-equalization and explains that "the FIRs of the transmitter… can be modified to support modes in which… taps can be disabled if not needed to consume minimum power while satisfying the performance or margin objective…. Through a combination of enabling or disabling Tx and Rx DFE taps… the overall system power can be minimized while maintaining adequate margins." Zerbe-063, 27:15-43.

245. A POSA would have known that disabling transmit pre-equalization was a conventional functionality for a transceiver. EX1030, Ex. B ("TI Retimer"), 37, Table 14 (describing hexadecimal channel register 1E setting for "Raw Data" in which "FIR filter will not function"); Gorecki-617, 18:3-17 (explaining "the leading and/or trailing taps may be 'turned off' or disabled"). And a POSA would have known that Lugthart-706's five-tap transmit filter pre-equalization functionality could be disabled through choice of tap coefficient values in the same manner as the Ethernet Standard taught for its three-tap transmit filter (e.g., by setting certain taps to zero while maximizing the central tap).

246. The resulting Lugthart+Gorecki+802.3 combination provides a mechanism for disabling transmit pre-equalization in FIR 17 and 27a/27b. A POSA would have disabled Lugthart+Gorecki+802.3 pre-equalization in FIR 17

and/or FIR 27a/27b in order to reduce power consumption where pre-equalization was not needed to meet signal quality requirements. Lugthart+Gorecki+802.3 thus would have combined familiar elements according to known methods yielding no more than predictable results. The combinations would have used known methods (disabling FIR filters when pre-equalization was unnecessary) to solve a known problem (reducing power consumption), and would have improved the Lugthart+Gorecki transceivers and system power consumption in the same way that it improved power consumption in Zerbe-063.

b. Reasonable Expectation of Success

247. A POSA would have had a reasonable expectation of success in achieving Lugthart+Gorecki+802.3 because setting filter coefficient values that disabled pre-equalization in transmit filters was known and described in the Ethernet Standard and other prior art discussed above, and—as those same references demonstrate—implementing this functionality was within the POSA's ordinary skill. Disabling pre-equalization was conventional for providing lower power mode in transceiver components.

3. Mapping of Lugthart+Gorecki+802.3 to claims 7, 14, and 20

248. Although claim 7 concerns claim 1's ***cable***, claim 14 concerns claim 14's ***manufacturing method***, and claim 20 concerns claim 15's "***communications*** ***method***, claims 7, 14, and 20 recite the same negative limitation "*wherein the first*

and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports." EX1029, 3.

249. Lugthart+Gorecki+802.3 uses the 802.3 teaching to set transmit filter coefficients to disable pre-equalization. As was known in the art, a POSA would have disabled pre-equalization "if not needed to consume minimum power while satisfying the performance or margin objective" for a system. Zerbe-063, 27:24-37. Thus, for use-cases where signal transmission between host devices using the active cable meets performance objectives ***without*** FIR filters 27a/27b pre-equalizing the RX DATA signal transmitted into electronic device 101a/101b, a user would disable the pre-equalization at filters 27a/27b in Lugthart+Gorecki+802.3. *Supra* §VI.B.2 (combination). This renders obvious claims 7, 14, and 20.

250. Thus, it is my opinion that Lugthart+Gorecki+802.3 meets claims 7, 14, and 20.

VII. DECLARATION

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: April 9, 2025

Paul S. Min, Ph.D.

APPENDIX A: U.S. PATENT NO. 10,877,233 CLAIM LIST

Ref	Limitation
1.PRE	A cable that comprises:
1.a	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
1.b	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and
1.c	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
1.d	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
1.e	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
2	The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.
3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

Ref	Limitation
4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
6	The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
7	The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
8.PRE	A cable manufacturing method that comprises:
8.a	connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;
8.b	connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;
8.c	connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,
8.d	the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and
8.e	the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,

Ref	Limitation
8.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
9	The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.
10	The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
11	The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.
12	The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
13	The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
14	The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
15.PRE	A communications method that comprises:

Ref	Limitation
15.a	inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
15.b	inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,
15.c	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
16.a	The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively,
16.b	each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.
17	The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
18	The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
19	The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

Ref	Limitation
20	The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

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Education

Year	College or University	Degree
1987	The University of Michigan	Ph.D. in Electrical Engineering
1984	The University of Michigan	M.S. in Electrical Engineering
1982	The University of Michigan	B.S. in Electrical Engineering

Professional Experience

From: 1990
To: Present
Organization: Washington University, St. Louis

Summary:

2015 -	Senior Professor - Department of Electrical Systems Engineering
2011 – 2014	Chair – Undergraduate Curriculum, Department of Electrical and Systems Engineering
2000 – 2002	Chair – Graduate Curriculum, Department of Electrical and Systems Engineering
2002 - 2014	Associate Professor - Department of Electrical and Systems Engineering
1997 - 2008	On leave from full-time duty at Washington University – as Presidents of MinMax Technologies and Erlang Technology.)
1996 - 2002	Associate Professor - Department of Electrical Engineering
1996	Promoted with Tenure

Amphenol Exhibit 1004
Amphenol v. Credo

1990 - 1996 Assistant Professor - Department of Electrical Engineering

Teaching Experience

- "Transmission System and Multiplexing," Washington University, ESE 571
- "Electrical Laboratory I," Washington University, EE 250.
- "Communication Theory," Washington University, ESE 471.
- "Reliability and Quality Control," Washington University, ESE 405/505
- "Signaling and Control of Communications Networks," Washington University, ESE 572.
- "Introduction to Electronic Circuits," Washington University, ESE232
- "Queueing Systems and Discrete Stochastic Processes," Washington University, EE 536 / CS 567.
- "Digital Computer," Washington University, EE 260M / CS 260.
- "Data Networks," Washington University, EE 530.
- "Electrical Circuit Analysis," Washington University, ESE 230.
- "Computer/Communications System Analysis I," Washington University, EE 557/ CS 557.
- "Computer/Communications System Analysis II," Washington University, EE558 / CS 558.
- "Digital Systems Laboratory," Washington University, EE 455 / CS 455.

From: 1999
To: 2008
Organization: Erlang Technology, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Up to 70 employees, $40M in total capital raised from 5 VCs and 3 Corporations
Received "Product of Year" Award from Analog Zone Magazine in 2004

From: 1997
To: 1999
Organization: MinMax Technologies, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Fabless semiconductor company, designing high performance switching ASICs

From: September 1987
To: August 1990
Organization: Bellcore, New Jersey
Title: Member of Technical Staff
Summary: Member of New Network Architecture Development Group

From: 1983
To: 1987

Organization: Department of Electrical Engineering, The University of Michigan
Title: Graduate Instructor
Summary: Instructor for senior level Electrical Engineering Laboratory Class. Received a Best "Best Graduate Instructor Award" from the Department of Electrical Engineering

Professional Affiliations, Achievements & Awards

- Technical Program Committee, COMCAS 2021, Tel Aviv, November 2021.
- Technical Program Committee, COMCAS 2019, Tel Aviv, November 2019.
- Technical Program Committee, COMCAS 2017, Tel Aviv, November 2017.
- Technical Program Committee, COMCAS 2015, Tel Aviv, October 2015.
- Past-Chair, Saint Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), 2015.
- Member of Executive Committee, Saint Louis Section of the IEEE, 2010-2015.
- Chair, Saint Louis Section of the IEEE, 2014.
- Technical Program Committee, COMCAS 2013, Tel Aviv, October 2013.
- Vice Chair, Saint Louis Section of the IEEE, 2013
- Treasurer, Saint Louis Section of the IEEE, 2012.
- The Best Paper Award at MOBILITY 2011, October 2011, Barcelona, Spain.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2011.
- Award of Appreciation, Saint Louis Section of the Institute of Electrical and Electronics. Engineers, 2011, for contribution to various activities of the Saint Louis Section the Institute of Electrical and Electronics Engineers.
- Secretary, Saint Louis Section of the IEEE, 2010.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2010.
- Wall Street Journal Businessmen of Year, 2003.
- American Men and Women of Science, listed in 1997.
- Member, Eta Kappa Nu (Honor Society for Electrical Engineers), inducted in 1992
- Outstanding Achievement Award, Bellcore, 1990.
- 18th ISATA Award of Technical Excellence, the best paper award at ISATA 1988.
- Rockwell Fellow, Rockwell International, 1985, 1986.
- Outstanding Graduate Student Award, the University of Michigan, 1985.
- Outstanding Teaching Award, the University of Michigan, 1984, 1986.
- Member of Honor's College, the University of Michigan, 1979, 1980.

- Honor's Convocation, the University of Michigan, 1979.
- Outstanding Freshman Award, the University of Michigan, 1979.
- Woodhaven Rotary Club Scholarship, Woodhaven Rotary Club, 1978.
- Second Place Winner, the State of Michigan Mathematics Prize Competition, 1977.
- International Program Committee, *IASTED International Conference on Communications, Internet and Information Technology (CIIT 2005*), Cambridge, Massachusetts from October 31-November 2, 2005.
- International Program Committee, *IASTED International Conference on Communications 2003*, Scottsdale, Arizona, 2003.
- International Program Committee, *Wireless and Optical Communications 2003*, Banff, Canada, 2003.
- International Program Committee, Session Chair, *Wireless and Optical Communications 2002*, Banff, Canada, 2002.
- Invited participant, *NSF Workshop on Enhancing International Cooperation in CS/CE Research and Education*, Portland, 1997.
- Session Chair, *the 1993 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Member, Board of Editors, *Journal of Network and Systems Management*, 1996-1998.
- Program Committee, *International Symposium on Integrated Network Management*, San Diego, 1997.
- Guest Editor, *Journal of Network and Systems Management, Special Issue on Routing in Broadband Networks*, December 1995 and June 1996.
- Invited participant, *ARPA Workshop on Survivability of Large Scale Systems*, Washington D.C., 1996.
- Special Event Organizer, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Organizing Committee, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Local Arrangements Chair, *IEEE Information Theory Workshop on Information Theory Multiple Access and Queueing*, St. Louis, 1995.
- Chair, *Communications Chapter, St. Louis Section of the IEEE*, 1995.
- Participant, *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing*, St. Louis, 1995.
- Participant, *ARPA/AFOSR Non-Linear Optics and Communication Workshop*, Denver, 1994.
- Participant, *CNRI Giga Bit Network Workshop*, Washington D.C., 1993.
- Participant, *IFIP/IEEE International Workshop on Distributed Systems*, New Jersey, 1993.
- Program Committee, *International Conference on Computer Communications and Networks*, San Diego, 1992.
- Session Chair, *ISMM International Conference*, New Orleans, 1990.
- Senior Member, *IEEE*.

- Member, *IEEE Committee on Network Operations and Management*.
- Member, *IEEE Committee on Computer Communications*.
- Registered Specialist, *Hong Kong Research Grant Council*.
- Reviewer, *IEEE Transactions on Communications*.
- Reviewer, *IEEE Transactions on Networking*.
- Reviewer, *IEEE Journal on Selected Areas in Communications*.
- Reviewer, *Journal of Network and Systems Management*.
- Reviewer, *Telecommunication Systems*.
- Reviewer, Computers and Electrical Engineering.
- Reviewer, *ETRI Journal*.
- Reviewer, *IEEE Transactions on Automatic Control*.
- Reviewer, *IEEE Communications*.
- Book Reviewer, *Prentice Hall*.
- Book Reviewer, *Morgan Kaufmann Publishers, Inc.*
- Book Reviewer, *Irwin Publishing Co.*

University Activities:

- Undergraduate Studies Committee, School of Engineering and Applied Science (2012 – Present)
- Faculty Advisor for IEEE Student Chapter (2009 – Present)
- Ambassador for McDonnell International Scholar Academy (2007 – 2013)
- Web Development Committee (2006 – 2008)
- University Judicial Board (1998 - 2000)
- Resource Generation Committee (1994 - 1995)
- Top 20 Committee (1992 - 1995)
- Telecommunications Committee, Chair (1991 - 1997)
- Library Planning Committee (1991 - 1992)
- Computer Engineering Committee (1990 - 1996)
- Communications Curriculum Committee (1990 - 1992)
- Resources Committee (1990 - 1992)

Patents

Patent No.	Date	Title
10,623,323	04/14/20	Network Devices and a Method for Signature Pattern Detection
10,284,476	05/07/19	Hierarchical Pattern Matching Devices and Methods

7,110,411	09/19/06	Method of and Apparatus for WFQ Scheduling Using a Plurality of Scheduling Queues to Provide Fairness, High Scalability, and Low Computational Complexity
7,106,738	09/12/06	Method of and Apparatus for High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability
6,859,455	02/22/05	Method of and Apparatus for Building and Using Multi-Dimensional Index Trees for Multi-Dimensional Data Objects
6,614,789	09/02/03	Method of and Apparatus for Matching Strings of Different Lengths
6,359,885	3/19/02	Multi-Channel Packet Switching Apparatus Having Traffic Flow Controlling and Checking Functions
6,128,292	10/03/00	Packet Switching Apparatus with Multi-Channel and Multi-Cast Switching Functions and Packet Switching System Using the Same
5,788,161	12/13/98	Network Designer for Communication Networks
5,526,352	06/11/95	Integrable Low Complexity Multi-Channel Switch
5,440,549	08/08/95	Nonblocking Multi-Channel Switching with Multicasting Capability

Publications

- Yu, Qixiang, Luo, Z, and Min, P.S., "Intrusion Detection in Wireless Sensor Networks for Destructive Intruders." Proceedings of the APSIPA 2015 conference. December 16-19, 2015.
- Hung, C.P., and Min, P.S., "Simple Web Application Framework." Submitted for publication in the IEEE Transactions on Cloud Computing.
- Luo, Z., and Min, P.S., "Parallel Implementation of Energy-Based Target Localization Methods in Wireless Sensor Networks." Proceeding of the 2014 IEEE SOUTHEASTCON.
- Yu, Q., Luo, Z., and Min, P.S., "Intrusion Detection in Wireless Sensor Networks for Destructive Intruder." Proceeding of 2014 International Conference on Smart Computing (SMARTCOMP 2014).
- Luo, Z., and Min, P.S., "Survey of Target Localization Methods in Wireless Sensor Networks," 19th IEEE International Conference on Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., "Deriving and Visualizing the Lower Bounds of Information Gain for Prefetch Systems," 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., "Access LUT without CAM - Improved Pearson Hashing for Collision Reduction," 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Luo, Z and Min, P.S., "Target Localization in Wireless Sensor Networks for Industrial Control with Selected Sensors." International Journal of Distributed Sensor Networks, Volume 2013 (2013), Article ID 304631.
- Hung, C.P., and Min, P.S. "Performance Evaluation of Distributed Mobile Application Virtualization Services," International Journal on Advances in Internet Technology, Vol. 5, no. 3&4, 2012, pp. 65-83.

- Hung, C.P. and Min, P.S., "Performance evaluation of distributed application virtualization services using the UMTS mobility model," MOBILITY 2011 The First International Conference on Mobile Services, Resources, and Users, 23-29 Oct. 2011.
- Hung, C.P. and Min, P.S., "Service Area Optimization For Application Virtualization Using UMTS Mobility Model," International Conference on Internet Computing, pp. 128-134, Las Vegas, July 18-21, 2011.
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- Hung, C.P. and Min, P.S., "Infrastructure Arrangement for Application Virtualization Service," the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 78-85, Rio de Janeiro, December 2010.
- Hung, C.P. and Min, P.S., "Probabilistic Approach to Network-Based Virtual Computing," the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 117-124, Rio de Janeiro, December 2010.
- Shiravi, A. and Min, P. S., "On the Latency Bound of Proportional Nested-DRR with Credit Adjusting," *2007 Workshop on High Performance Switching and Routing HPSR 2007*, July 2007.
- Shiravi, A. and Min, P. S., "LOOFA-PB: A Modified LOOFA Scheduler for Variable-Length Packet Switching." *2007 IEEE International Conference on Communications (ICC 2007),* Glasgow, June 2007.
- Shiravi, A., Kim, Y. G., and Min, P. S., "Congestion Prediction of Self-Similar Network through Parameter Estimation," *Proceedings of 2006 IEEE/IFIP Network Operations & Management Symposium*, April 2006, Vancouver.
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Testimony Provided or Expected to Provide as Expert Witness

Matter: Patent Infringement for Wireless Local Area Networks
Law Firm: Quinn Emanuel Urquhard & Sullivan LLP

Case Name: Certain Audio Players and Components thereof (II). U.S.I.T.C. Inv. No. 337-TA-1330.
Testifying Expert for Google Inc.
Completed in June 2023.
(Expert reports submitted and deposed.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Alston & Bird
Case Name: Atlas Global Technologies LLC v. ASUSTek Computers Inc.USDC WD TX Civil Action No. 6:21-cv-820
Testifying Expert for ASUSTek
Completed in November 2023
(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023
(Expert report submitted. Deposed.)

Matter: Patent Infringement for Wireless Communications
Law Firm: LAW OFFICES S. J. CHRISTINE YANG
Case Name: Atlas Global Technologies LLC v. ZyXEL Communications Corp. et al., U.S.D.C., W.D.T.X., W aco Div., Case No. 6:22-cv-00355 Atlas Global Technologies LLC v. D-Link Corp. U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00520
Testifying Expert for ZyXel
Retained in March 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Bell Northern Research v. MeidaTek Inc.
Testifying Expert for MediaTek Inc.
Retained in August 2023.

Matter: Patent Infringement for Home Security System
Law Firm: Foley and Lardner LLP
Case Name: Alarm.com v. Vivint, Inc., AAA Arbitration Case. No. 01-22-0004-5525 and U.S.D.C. Case No. 2:23-cv-00004-JRG-RSP (E.D. Tex.),
Testifying Expert for Vivint, Inc.
Completed in 2023.

Matter: Patent Infringement for Wireless Communications and Electronics

Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023.

Matter: Patent Infringement for Network Switches
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC v. CouldFlare, Inc. U.S.D.C. WD Tx Case No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.
Completed in January 2024.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Security
Law Firm: Fish and Richardson
Case Name: Finjan LLC v. Palo Alto Networks, Inc. – Case No. 4:14-cv-04908-PJH. USDC ND CA, Oakland Division.
Testifying Expert for Finjan LLC.
Retained in September 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Management
Law Firm: Irell & Manella LLP
Case Name: SNMP Research, Inc. & SNMP Research International, Inc. v. Broadcom Inc., Brodcade Communications Systems LLC, & Extreme Networks, Inc. U.S.D.C. E.D. Tennessee at Knoxville Case No. 3:20-CV-451
Testifying Expert for SNMP Research.
Retained in May 2022.

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for MediaTek
Retained in March 2023.

Matter: Patent Infringement for Network Switching
Law Firm: Baker Botts
Case Name: Corrigent Corp. v. Arista Networks, Inc., Case No. 1:22-cv-00497-UNA. USDC Delaware
Testifying Expert for Arista
Retained in October 2022.

Matter: Patent Infringement for Mobile Deives
Law Firm: Fish and Richardson
Case Name: GComm v. Samsung, U.S.D.C. ED. TX. Case No.:2:22-cv-0078-JRG

Testifying Expert for Samsung
Completed in January 2024.

Matter: Patent Infringement for Wireless Networks
Law Firm: McKool Smith
Case Name: Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and Smart Watches with Cellular Connectivity, Components Thereof, and Products Containing Same. U.S.I.T.C. Inv. No. 337-TA-1299
Testifying Expert for Ericsson
Completed in July 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Semiconductor Manufacturing
Law Firm: Kramer Levin
Case Name: Oasis Tooling, Inc. v. Siemens Indus. Software, Inc., 1:22-cv-151 (D. Del.), Oasis Tooling, Inc. v. GlobalFoundries U.S. Inc., 1:22-cv-312 (D. Del.)
Testifying Expert for Oasis Tooling
Retained in June 2022.
(Expert reports submitted.)

Matter: Patent Infringement for Optical Networks
Law Firm: Duane Morris
Case Name: NextGen Innovations, LLC v. Infinera Corporation. U.S.D.C. ED. TX (Marshall) Case No. 2:22-cv-00306-JRG-RSP / IPR
Testifying Expert for Infinera
Retained in April 2023.

Matter: Patent Infringement for Wireless Devices
Law Firm: King and Spalding LLP
Case Name: Intellectual Ventures, et. al. v. General Motors Company and General Company Motors, LLC, Case No. 6:21-CV-1088 pending in the Western District of Texas, Waco Division
Testifying Expert for General Motors
Completed in January 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Devices
Law Firm: Sterne Kessler
Case Name: Neo Wireless LLC v. Volkswagen Group of America, Inc. and Volkswagen Group of America Chattanooga Operations, LLC and related matters
Testifying Expert for Volkswagen
Completed in September 2023.
(Expert report submitted and deposed. IPR declarations submitted)

Matter: Patent Infringement for Wireless Networks
Law Firm: Covington & Burling LLP

Case Name: XR Communications, LLC v. D-Link Systems, Inc., No. 8:17-cv-00596 (Consolidated) (C.D. Cal.)
Testifying Expert for Hewlett Packard Enterprise
Completed
(Expert report submitted and deposed.)

Matter: Patent Infringement for USB Charging System
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Fundamental Innovation Systems International LLC v. TCT Mobile (US), TCT Mobile (US) Holdings, Inc., et al. U.S.D.C. Delaware No. 20-552-RGA-CJB
Testifying Expert for TCL
Completed in June 2022.
(Expert report submitted and deposed.)

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Alston & Bird
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Nokia
Retained in May 2022.
(Expert report submitted.)

Matter: Patent Infringement for Network Management System
Law Firm: Morgan, Lewis & Bockius, LLP
Case Name: Certain Routers, Access Points, Controllers, Network Management Devices, Other Networking Products, and Hardware and Software Components Thereof, U.S.I.T.C. Inv. No. 337-TA-1227
Testifying Expert for Hewlett Packard, Netgear, and CommScope
Completed in August 2021.
(Expert report submitted, deposed, and testified during trial.)

Matter: Contract Dispute
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Allied Telesis, Inc., et al vs. Micron Technology, Inc., Santa Clara County Case No: 2015-1-CV-282977
Testifying Expert for Micron
Retained in 2021. Deposed in October 2021.
Completed in 2022

Matter: Patent Infringement for Security Systems
Law Firm: Forley and Lardner LLP
Case Name: Certain Residential Premises Security Monitoring and Automation Control Panels, and Components Thereof (ITC Inv. No. 337-TA-1273) and ADT LLC et al v. Vivint, Inc., Case No. 6:21-cv-00687 (W.D. Tex.)
Testifying Expert for Vivint, Inc.
Completed in April 2022.
(Expert report submitted, deposed, and testified during trial.)

Matter: Inter Parte Reexamination for Internet Communications
Law Firm: Perkins Coie
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Twitter
Retained in June 2020.
(Expert report submitted.)

Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd. v. Heathco LLC, U.S.D.C. Delaware No. 20-224-LPS
Testifying Expert for Vaxcel
Retained in February 2021.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Communication System
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC, v. ClouFlare, Inc. U.S.D.C. WDTX, Civil Action No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.,
Completed in January 2024.

Matter: Patent Infringement for Mobile Wireless Device
Law Firm: Pearl Cohen
Case Name: In the Matter Of Certain UMTS And LTE Cellular Communications Modules And Products Containing The Same, U.S.I.T.C. Inv. No. 337-TA-1240
Testifying Expert for Telit Wireless Communication, Quectel, and Thales
Completed in March 2023.
(Expert reports submitted and deposed.)

Matter: Transactional Taxes for Internet Application
Law Firm: Ryan Rapp & Underwood, PLC
Case Name: ADP, LLC v. Arizona Department of Revenue (TX2018-000246),
Testifying Expert for ADP, LLC.
Completed in June 2020.
(Expert report submitted.)

Matter: Trade Secret Misappropriation in Digital Electronics
Law Firm: Goodwin Proctor LLP
Case Name: Guzik Technical Enterprises versus Keysight Technologies, Inc. Superior Court of the State of California for the County of Santa Clara, Case No.: 19CV355879
Testifying Expert for Keysignt Technologies, Inc.
Retained in August 2020.

Matter: Patent Infringement for Fiber Optic Devices
Law Firm: Cooley

Case Name: Certain High-Density Fiber Optic Equipment and Components Thereof, U.S.I.T.C. Inv. No. 337-TA-1194
Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and Siemon
Completed in October 2020.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Optical Transport Networks
Law Firm: Venerble
Case Name: Huawei Technologies Co. Ltd v Verizon Communications, Inc., et. al., 2:20-cv-0030
Testifying Expert for Verizon.
Retained in March 2020.
(IPR declarations submitted.)

Matter: Patent Infringement for Lighting System
Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd., v. Jasco Products Company, LLC., (Case No. USDC Western District of Oklahoma, 5:19-CV-00154-JD
Testifying Expert for Vaxcel.
Retained in August 2020.

Matter: Patent Infringement for Wireless Communication
Law Firm: McDermott Will & Emery
Case Name: Bell Northern Research LLC v. ZTE. (Case No. 3:18-cv-01786 - S.D. Cal)
Testifying Expert for ZTE.
Retained in July 2019.
(IPR declarations submitted.)

Matter: Patent Infringement for Wireless Communication
Law Firm: Jones Day
Case Name: Bell Northern Research LLC v. Kyocera Corp. (Case No. 3:18-cv-1785 - S.D. Cal)
Testifying Expert for Kyocera.
Completed in May 2019.
(Claim construction declaration submitted, and deposed.)

Matter: Patent Infringement for Electronic Payment Systems
Law Firm: Paul Hastings
Case Name: ID Tech Corp. v. Samsung Electronics Co., Ltd., et al. (Case No. No. 8:17-cv-1748-DOC-JDE (C.D. Cal))
Testifying Expert for Samsung.
Retained in January 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Internet Switching

Law Firm: Maynard Cooper
Case Name: Parity Networks, LLC v. Juniper Networks, Inc., Case No. 6:17-CV-00495-RWS-KNM (U.S.D.C.E.D. Tx.)
Testifying Expert for Juniper.
Retained in April 2018.
(IPR declarations submitted.)

Matter: Patent Infringement for Internet Switching
Law Firm: Morgan Lewis
Case Name: Parity Networks, LLC v. Hewlett Packard Enterprise Company, Case No. 6:17-CV-00682 (U.S.D.C.E.D. Tx.)
Testifying Expert for Hewlett Packard Enterprise Company.
Retained in September 2018.
(IPR declarations submitted.)

Matter: Inter Parte Rexamination for Covered Business Method
Law Firm: Reed Smith LLP
Case Name: NASDAQ v. Miami International
Expert for Miami International.
Retained in February 2018.
(Expert declarations submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Qualcomm v. Apple, Case No. 3:17-cv-00108-GPC-MDD (U.S.D.C.S.D. Cal.)
Testifying Expert for Qualcomm.
Completed in April 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Devices
Law Firm: Venable
Case Name: Sycamore IP Holdings LLC v. Verizon Communications Inc, Case No. 2:16-cv-591-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Verizon and Level 3.
Completed in September 2017.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Alston Bird
Case Name: Huawei Technologies Co. Ltd. V. Nokia Solutions and Networks, Case No. 2:16-cv-0056-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Nokia.
Completed in December 2017.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Huawei Technologies Co. Ltd. V. Samsung Electronics C. Ltd, Case No. 3:16-cv-02787 (U.S.D.C. N.D. Cal)
Testifying Expert for Samsung.
Completed in March 2019.
(Expert reports submitted, and deposed.)

Matter: Arbitration for Licensing
Law Firm: Alston Bird
Case Name: Nokia v. LG Electronics, International Chamber of Commerce Arb. No. 21326
Testifying Expert for Nokia.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Ropes and Gray
Case Name: Godo Kaisha IP Bridge 1 v. TCL Communication Technology Holdings, Case No. 15-634-SLR-SRF (U.S.D.C.S.D. Delaware.)
Testifying Expert for IP Bridge.
Completed in October 2018.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Paul Hastings
Case Name: Odyssey Wireless, Inc,. v. Samsung Electronics Co., Ltd., et al, Case No. 3:15-cv-1738-H-RBB (U.S.D.C.S.D. Cal.)
Testifying Expert for Samsung.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Greenberg Traurig
Case Name: Mobile Telecommunications Technologies LLC v. Amazon.com, Inc., 2:13-cv-883-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Amazon.
Completed in April 2015.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Mayer Brown
Case Name: Mobile Telecommunications Technologies LLC v. LG Electronics Mobilecomm U.S.A., Inc., 2:13-cv-947-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for LG Electronics Mobilecomm.
Completed in February 2016.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Semiconductor Devices
Law Firm: Mayer Brown
Case Name: Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332
Expert for LG Electronics.
Completed in February 2016.
(Expert declaration submitted, and deposed.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Gardner, Linn, Burkhart & Flory, L.L.P
Case Name: *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:12-cv-00654 (Western District of Michigan), and relating to the action styled *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:13-cv-00324 (Western District of Michigan).
Testifying Expert for Magna Electronics
Completed in February 2016.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement in Electronic Circuits
Law Firm: Ropes and Gray
Case Name: Certain Devices Containing Non-Volatile Memory and Products Containing the Same (USITC Inv. Nos. 337-TA-922)
Testifying Expert for Spansion Inc.
Completed in February 2015.
(Expert reports submitted.)

Matter: Trade Secret Misappropriation in Software Method for Cable Television Advertisement
Law Firm: Brownstein Hyatt Farber Schreck
Case Name: Cross MediaWorks v. EMT Holdings, USDC Southern District of New York, Case No. 1:14-cv-00561-VSB
Testifying Expert for Cross MediaWorks.
Completed in April 2015.
(Testified during injunction hearing.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Steptoe and Johnson
Case Name: Certain Vision-Based river Assistance System Cameras and Components Thereof (USITC Inv. Nos. 337-TA-899 and 907)
Testifying Expert for Magna Electronics
Completed in February 2015.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Vehicular System
Law Firm: Susman Godfrey

Case Name: Eagle Harbor Holdings, LLC, and Mediustech, LLC, v. Ford Motor Company, 3:11-cv-05503-BHS (U.S.D.C. Western District of Washington at Tacoma)
Testifying Expert for Mediustech.
Completed in March 2015.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Communication Networks
Law Firm: Davis Polk & Wardwell LLP
Case Name: Sprint Communications Company L.P., v. Comcast Cable Communications, LLC, Comcast IP Phone, LLC, and Comcast Phone of Kansas, LLC. 2:11-cv-02684-KHV-DJW (U.S.D.C. Kansas)
Testifying Expert for Comcast.
Retained in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Networks
Law Firm: Quinn Emanuel
Case Name: France Telecom S.A. v. Marvell Semiconductor, Inc., 12-Civ-4986 (S.D.N.Y.)
Testifying Expert for Marvell.
Completed in September 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Wireless Image Distribution
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent No. 8,437,797
Expert for Google Inc.
Completed in November 2014.
(Expert declaration submitted.)

Matter: Nonvolatile Semiconductor Memories
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent Nos. 8,301,833 and 8,516,187
Expert for SanDisk.
Completed in May 2014.
(Expert declaration submitted.)

Matter: Communication Protocols for Wireless Device
Law Firm: Dorsey & Whitney, LLP
Case Name: Certain Point-To-Point Network Communication Devices and Products Containing Same (USITC Inv. No. 337-TA-892)
Testifying Expert for Toshiba
Completed in May 2014.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Ropes and Gray

Case Name: In the Matter of Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof (USITC Inv. No. 337-TA-868) InterDigital Comms., Inc. v. Huawei Techs. Co., Ltd., No. 13-00008 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. ZTE Corp., No. 13-00009 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Nokia Corp., No. 1:13-cv-00010 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Samsung Elec. Co., Ltd., No. 13-00011 (D. Del., filed January 2, 2013)
Testifying Expert for Joint Defense Group.
Completed in February 2014.
(Expert reports submitted, deposed, and testified during trials.)

Matter: Patent Infringement for Mobile Communication
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
Case Name: Certain Digital Media Devices, Including Televisions, Blu-Ray Disc Players, Home Theater Systems, Tablets and Mobile Phones, Components Thereof and Associated Software (USITC Inv. No. 337-TA-882)
Testifying Expert for LG Electronics, Inc.
Completed in February 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Vinson & Elkins LLP
Case Name: Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Telefonaktiebolaget LM Ericsson and Ericsson, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23569), Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Alcatel-Lucent USA, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23568-Altonaga/Simonton)
Testifying Expert for Wi-LAN.
Completed in May 2015.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Data Storage
Law Firm: Ropes and Gray, Weil Gotshal
Case Name: Summit Data Systems, LLC v. EMC Corporation., et al. 1:10-cv-00749-GMS (U.S.D.C. Delaware)
Testifying Expert for EMC Corporation and Netapp, Inc.
Completed in December 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Ashurst Australia
Case Name: Samsung v. Apple, Australian Federal Court Proceeding No. NSD 1243 of 2011
Testifying Expert for Samsung Electronics.
Completed in December 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Mobile Devices

Law Firm: Quinn Emanuel
Case Name: Apple Inc. v. Samsung Electronics Co., Ltd., et al., 4:11-cv-01846-LHK (N.D. Cal.) and Samsung Electronics Co., Ltd., et al. v. Apple Inc., 4:11-cv-02079 (N.D. Cal.)
Testifying Expert for Samsung Electronics.
Completed in July 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Quinn Emanuel
Case Name: Certain Electronic Devices, Including Wireless Communication Devices, Portable Music And Data Processing Devices, And Tablet Computer, U.S.I.T.C. Inv. No. 337-TA-794
Testifying Expert for Samsung Electronics.
Completed in June 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Portable Storage Device
Law Firm: White and Case
Case Name: CERTAIN UNIVERSAL SERIAL BUS ("USB") PORTABLE STORAGE DEVICES, INCLUDING USB FLASH DRIVES AND COMPONENTS THEREOF, US International Trade Commission Investigation No. 337-TA-788
Testifying Expert Witness for Trek
Completed in May 2012.
(Expert reports submitted, and deposed.)

Matter: Copyright Infringement for Petroleum Processing Software
Law Firm: Osha Liang LLP
Case Name: Aspen Technology, Inc. v. Tekin A. Kunt and M3 Technology, Inc., Case Number: H-10-1127, US District Court, Texas, Houston Division.
Testifying Expert for M3 Technology, Inc.
Completed in May 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Trade Secret Misappropriation for DC-DC converter
Law Firm: Covington & Burling, Haynes Boone
Case Name: Certain DC—DC Controllers and Products Containing Same, US International Trade Commission Investigation No. 337-TA-698
Testifying Expert for UPI.
Completed in March 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Parallel Processor
Law Firm: Orrick, Herrington, & Sutcliffe. Kirkland and Ellis.
Case Name: BIAX Corporation v. Nvidia and Sony Civil Action No. 09-cv-01257-PAB-MEH
Testifying Expert for Nvidia and Sony

Completed in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Duffy, Sweeney, and Scott. Foley Lardner.
Case Name: Ronald Katz Technology Licensing v. Citizens Financial Group 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for Citizens Financial Group.
Completed in 2011.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Storage Area Network
Law Firm: DLA Piper
Case Name: Network Appliance, Inc., v. Sun Microsystems, Inc., Case Number: C-07-06053 EDL, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Sun Microsystems, Inc.
Completed in 2010.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flat Panel Display Controller
Law Firm: Jones Day
Case Name: Certain Video Displays, Components Thereof, and Products Containing Same, US International Trade Commission Investigation No. 337-TA-687
Testifying Expert for Vizio, Inc.
Completed in 2010.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Foley Lardner
Case Name: Ronald Katz Technology Licensing v. US Bank 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for US Bank
Completed in May 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for USB to VGA Converter
Law Firm: Wang Hartmann, Gibbs, & Cauley, P.C.
Case Name: Displaylink Corporation v. Magic Control Technology Corporation, Case No. 5:07-CV-01998-RMW, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Magic Control Technology Corporation
Completed in 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flash Memory
Law Firm: Jones Day and Wilson Sansini

Case Name: Certain Flash Memory Controllers, Drives, Memory Card, and Media Players and Products Containing Same. US International Trade Commission Investigation No. 337-TA-619
Testifying Expert for SanDisk Corporation.
Completed in 2008.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Semiconductor Packaging
Law Firm: Jones Day
Case Name: Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing the Same. US International Trade Commission Investigation No. 337-TA-605
Testifying Expert for Freescale Semiconductor
Completed in 2008.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Automatic Switching System
Law Firms: Jones Day, and Heller Ehrman, LLP.
Case Name: ATEN International Co., Ltd and ATEN Technology, Inc. v. Belkin Corporation, Belkin Logistics, Inc. and Emine Technology Co., Ltd. US International Trade Commission Investigation No. Ltd 337-TA-589
Testifying Expert for Belkin Corporation, Belkin Logistics, Inc., and Emine Technology Co., Ltd.
Completed in 2007.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Dual Mode Communication
Law Firm: Wilmer Cutler Pickering Hale and Dorr, LLP
Case Name: Broadcom Corporation v. Qualcomm Incorporated SACV05-467-JVS (RNBx)
Testifying Expert Witness for Broadcom Corporation
Completed in 2007.
(Expert reports submitted, deposed, and testified during trial.)