

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VOLEX PLC,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

Case No. IPR2025-01387
Patent No. 11,032,111

**DECLARATION OF AYMAN FAYED, Ph.D.
IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO. 11,032,111**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
A.	Engagement.....	1
B.	Background and Qualifications.....	2
C.	Bases of My Opinions and Materials Considered.....	8
D.	My Understanding of Patent Law	10
1.	Anticipation	12
2.	Obviousness	13
3.	Claim Interpretation	15
II.	DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME	17
III.	PERSON OF ORDINARY SKILL IN THE ART (“POSA”).....	18
IV.	THE ’111 PATENT	22
A.	Background.....	22
B.	Described Embodiments	27
C.	Prosecution History of the ’111 patent.....	30
D.	The Challenged Claims.....	31
V.	CLAIM INTERPRETATION.....	32
VI.	GROUND 1: CLAIMS 1-19 ARE OBVIOUS OVER THE COMBINATION OF LUGTHART, DAS SHARMA, AND MEZER	32
A.	Lugthart-706.....	33
B.	Das Sharma	41
C.	Mezer	43
D.	The Lugthart-Das Sharma-Mezer Combination.....	45
1.	Reasons to Combine with a Reasonable Expectation of Success	45
2.	The Resulting Lugthart-Das Sharma-Mezer Combination	68
E.	Lugthart-Das Sharma-Mezer Meets All Challenged Claims	69
1.	Claim 1.....	69
2.	Claim 2.....	80

3. Claim 3.....	85
4. Claim 4.....	86
5. Claim 5.....	88
6. Claim 6.....	89
7. Claim 7.....	90
8. Claim 8.....	91
9. Claims 9-10.....	100
10. Claim 11.....	100
11. Claims 12-13.....	103
12. Claim 14.....	103
13. Claim 15.....	105
14. Claim 16.....	105
15. Claims 17-19.....	106
VII. DECLARATION	106
APPENDIX A: U.S. PATENT NO. 11,032,111 CLAIM LIST	107

I, Ayman Fayed, Ph.D., make this declaration in connection with IPR2025-01387.

I. INTRODUCTION

A. Engagement

1. I have been engaged by Volex plc (“Petitioner” or “Volex”) as an independent expert on the subject matters in connection with Volex’s Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 11,032,111 (“the ’111 patent”).

2. I understand that the ’111 patent is assigned to Credo Technology Group Ltd. (“Patent Owner” or “Credo”).

3. This Declaration is based on the information currently available to me. If additional relevant information or testimony becomes available, I reserve the right to continue my investigation and analysis based thereon.

4. All of the opinions set forth in this Declaration are based on my own personal knowledge, professional experience, education and judgment, and my consideration of the documents, materials and information that I reference.

5. I am being compensated for my work as an expert at my standard hourly rate for consulting services, including for the time I may spend testifying on deposition or at any hearing. I am also being reimbursed for reasonable and customary expenses associated with my work in this case. I receive no other forms of compensation related to this case. No portion of my compensation is dependent

or otherwise contingent on the results of this proceeding or the specifics of my testimony.

B. Background and Qualifications

6. I have over 26 years of experience in the fields of electrical, computer, and electrical communications engineering. My CV is attached as Exhibit EX1004, and it details my experience relevant to the patents-in-suit.

7. My industry and research experience and expertise specifically relevant to the patents-in-suit includes high-speed wire-line transceiver design for digital communication systems, including adaptive signal drivers/transmitters, adaptive signal receivers/equalizers, adaptive filters, clock and data recovery circuits, and analog and mixed-signal integrated circuits.

8. I earned a Ph.D. in Electrical and Computer Engineering from The Ohio State University in 2004. I also earned a M.Sc. in Electrical and Computer Engineering from The Ohio State University in 2000. I earned a B.Sc. in Electronics and Electrical Communications Engineering from Cairo University in Egypt in 1998.

9. I am currently a Professor in the Department of Electrical and Computer Engineering at The Ohio State University where I lead and direct the Power Management Research Lab.

10. A selected summary of my specific experience relevant to the patents-in-suit includes my experience in the field as an analog, mixed-signal, and power management/electronics IC (integrated circuit) designer for the Connectivity Department at Texas Instruments in 2000 and 2002-2005. In that role, I designed systems and circuits for the front-end receive/transmit paths of several high-speed wire-line transceivers in multiple digital CMOS technology nodes. This included the receive and transmit paths of Universal Serial Bus (USB) 2.0 transceivers in 0.18 μ m/0.13 μ m/90nm processes, the receive path of High-Definition Multi-Media Interface (HDMI) transceivers in 0.13 μ m processes, and the receive path of IEEE 1394b transceivers in 0.18 μ m processes. The designs encompassed a wide variety of circuit techniques for adaptive equalizers, clock and data recovery circuits, high-speed low-jitter receivers, voltage/current signal drivers/transmitters, high-speed signal detectors/rectifiers, automatically-tuned on-chip transmission line terminations, low-voltage voltage-controlled transconductors, adaptive GM-C filters, and voltage/current references.

11. My relevant experience also includes my 2005-2008 role as a member of the technical staff and as an analog, mixed-signal, and power management/electronics IC (integrated circuit) designer for the Wireless Terminal Business Unit at Texas Instruments.

12. In that role, I led the system and circuit design of a wide range of analog, mixed-signal, and power management functions for integrated wireless, RF, and baseband System-on-Chip (SoC) applications in 90nm/65nm/45nm digital CMOS technologies.

13. For example, the design of various classes of delta-sigma data converters including switched-C, continuous-time, and single-amplifier-based architectures for wireless RF CODEC applications for GSM/WCDMA wireless standards, including high-speed sampling/hold networks, quantizers, and clocking schemes; low-noise low-power amplifiers; reference signal buffers; and voltage/current reference generators.

14. Another example of my responsibilities in that role is the design of RF-friendly dc-dc converters, ripple suppression and cancellation techniques, and low-leakage circuit techniques for linear and switching power converters for RF and mixed-signal modules.

15. I have also led the clear spectrum task force at Texas Instruments, where I was responsible for power system architecture, supply domain definition and specifications, noise and power budgeting, as well as the development of design and verification methodology for power management/electronics modules in large mixed-signal System-on-Chip with multi noise-sensitive RF cores, including Cellular, Bluetooth, and Wireless LAN RF transceivers. This

encompassed circuit design, power distribution networks, package and board parasitics modeling, communication across supply domains, and power supply isolation.

16. My relevant experience also includes my role as an assistant professor (2009-2014) and associate professor (2014-2015) at Iowa State University, and as an associate professor (2015-2020) and full professor (2020-present) at The Ohio State University, where I supervised the research of 14 Ph.D. students, over 14 M.Sc. students, who, for example, designed various classes of integrated linear and switching power regulators and battery management systems, low-noise low-EMI power converters for RF circuits, high-frequency switching converters with on-chip outputs, and continuous- and discrete-time signal filters, all in 350nm/65nm/45nm/28nm CMOS technologies.

17. The focus of my professional and research work has been on analog, mixed-signal, and power management/electronics integrated circuits.

18. I have authored or co-authored over 71 technical papers in international journals and conferences and have been an inventor or co-inventor on 8 US and international patents. Much of my published work, including my Master's and Ph.D. research, covers the area of analog, mixed-signal, and power management/electronics integrated circuits.

19. My expertise in, and contributions to, the field of analog, mixed-signal, and power management/electronics integrated circuits have been recognized in many ways.

20. For example, from 2016 to 2023, I served on the editorial board (as an associate editor) of the IEEE Transactions on Circuits and Systems I, which is the leading journal of the IEEE Circuits and Systems Society.

21. I have also been serving as a member of the Technical Program Committee of many leading IEEE international conferences, such as RF Integrated Circuits Symposium (2011-2021), Applied Power Electronics Conference (2018-present), and International Symposium of Circuits and Systems (2012-present).

22. I have also served on the board of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society (Chair of the board 2022-2025, Chair-Elect 2021-2022, and Secretary 2019-2021). I have also received the Best Associate Editor Award from IEEE Transactions on Circuits and Systems–I in 2020, 2021 and 2022, and I have received the 2022 IEEE Circuits and Systems Society Outstanding Technical Committee Award. I have also received the 2021 IEEE Transactions on Power Electronics Second Place Prize Paper Award from the IEEE Power Electronics Society, the 2015 Darlington Best Transactions Paper Award from the IEEE Circuits and System Society, the

National Science Foundation CAREER Award in 2013, and the Northrop Grumman Chair Professorship from Iowa State University in 2013 and 2014.

23. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my curriculum vitae. *See* EX1004.

24. In forming my opinions, I have relied upon the materials listed below, my education, training, and knowledge of connector technologies, electrical and electronic materials, and related experience.

C. Bases of My Opinions and Materials Considered

25. I have reviewed the '111 patent, its prosecution history, and the prior art and other documents and materials cited herein. I have also reviewed the Declaration of Paul S. Min, Ph.D. which—together with Dr. Min's c.v.—from Exhibits 1003 and 1004 in Case No. IPR2025-00699, in which I understand Amphenol Corporation challenges the patentability of the claims of the '111 patent. I was specifically asked by counsel to, in the course of performing my analysis, consider the accuracy and correctness of Dr. Min's declaration. And, in fact, I have found that declaration to be accurate and correct; and—as set forth below—I have largely adopted Dr. Min's declaration, with the exception of some minor edits I found useful for clarity.

26. My opinions, as explained below, are based on my years of education, research, experience, and background in the field of microelectronics and computing systems, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section III below. In forming my opinions, I have studied and considered the materials identified in the list below.

Exhibit	Description
1001	United States Patent No. 11,032,111 (“the ’111 Patent”)
1002	Prosecution History of United States Patent No. 11,032,111
1003	Declaration of Ayman Fayed, Ph.D.
1004	Curriculum Vitae of Ayman Fayed, Ph.D.
1005	United States Patent No. 9,882,706 (“Lugthart-706”)
1006	United States Patent Publication No. 2014/0281067 (“Das Sharma”)
1007	United States Patent No. 7,239,665 (“Mezer”)
1008	United States Patent No. 8,787,430 (“Raghavan”)
1009	United States Patent No. 9,806,812 (“Schmidt”)
1010	United States Patent No. 9,137,063 (“Zerbe-063”)
1011	United States Patent No. 7,308,058 (“Zerbe-058”)
1012	United States Patent No. 8,477,835 (“Zerbe-835”)
1013	United States Patent No. 9,152,257 (“McCall”)
1014	United States Patent No. 9,118,512 (“Gotman”)
1015	United States Patent No. 10,736,201 (“Burchardt”)
1016	United States Patent No. 7,664,171 (“Sun”)
1017	United States Patent No. 6,680,681 (“Hsu”)
1018	United States Patent Publication No. 2013/0223506 (“Kolze”)
1019	United States Patent Publication No. 2010/0232493 (“Thirumoorthy”)
1020	PCT Publication No. 2016/203205 (“Griffin”)
1021	United States Patent No. 9,495,245 (“Peddle”)
1022	United States Patent No. 5,854,921 (“Pickett”)
1023	United States Patent Publication No. 2004/0071203 (“Gorecki”)

Exhibit	Description
1024	IEEE Std. 802.3-2015, “IEEE Standard for Ethernet: Section 5” (“802.3- 2015 Section 5”)
1025	<i>Insertion loss</i> , Newton’s Telecom Dictionary (31st ed. 2018) (“Newton’s”)
1026	<i>Insertion loss, package, loss, dissipation</i> , Oxford – A Dictionary of Electronics and Electrical Engineering (5th ed. 2018) (“Oxford”)
1027	IEEE Std. 802.3bs-2017 “IEEE Standard for Ethernet: Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation” (2017) (“802.3bs”).
1028	Optical Internetworking Forum Implementation Agreement, “Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps,” OIF-CEI-04.0 (Dec. 29, 2017) (“OIF-CEI-04.0”)
1029	United States Patent Publication No. 2015/0189092 (“Thapa”)
1030	United States Patent No. 9,088,336 (“Mani”)
1031	United States Patent No. 9,754,605 (“Chhetri”)
1032	Optical Internetworking Forum, “OIF Next Generation Interconnect Framework,” OIF-FD-Client-400G/1T-01.0 (2013) (“OIF-FD-Client-400G/1T-01.0”)
1033	Declaration of Paul S. Min, Ph.D., together with Dr. Min’s c.v., which are Exhibits 1003 and 1004 in Case No. IPR2025-00699
1034	<i>Intentionally left blank</i>
1035	<i>Intentionally left blank</i>
1036	<i>Intentionally left blank</i>
1037	<i>Intentionally left blank</i>
1038	<i>Intentionally left blank</i>
1039	<i>Intentionally left blank</i>
1040	<i>Intentionally left blank</i>
1041	<i>Intentionally left blank</i>
1042	<i>Intentionally left blank</i>
1043	<i>Intentionally left blank</i>

D. My Understanding of Patent Law

27. In developing my opinions, I discussed various relevant legal principles with Petitioner’s attorneys. I understood those principles when they

were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

28. I understand that “*inter partes* review” (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent’s claims based on prior-art patents and printed publications.

29. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the ’111 patent are unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

30. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSA”) in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification’s special definition controls. If a claim element is expressed as a “means” for performing a specified function, I understand that it covers the corresponding structure described in the specification and equivalents of the described structure. I have applied these standards in preparing the opinions in this declaration.

31. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that, for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application's filing date. I understand that a disclosure that merely renders the claimed invention obvious is not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

32. I understand that, for an invention claimed in a patent to be patentable, it must be, among other things, new (novel—*i.e.*, not anticipated) and not obvious over the prior art. My understanding of these two legal standards is set forth below.

1. Anticipation

33. I understand that, for a patent claim to be “anticipated” by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior-art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the limitation based on inferences that a POSA

would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA's knowledge and experience.

34. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

2. Obviousness

35. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior-art reference or a combination of prior-art references.

36. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

- the scope and content of the prior art;
- the differences between the prior art and the claims at issue;
- the knowledge of a person of ordinary skill in the pertinent art; and

- if present, objective factors indicative of non-obviousness, sometimes referred to as “secondary considerations.” To my knowledge, the Patent Owner has not asserted any such secondary considerations with respect to the ’111 patent.

37. I understand that, in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

38. I further understand that, in determining whether a prior-art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

- combining prior-art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve similar devices in the same way;
- applying a known technique to a known device ready for improvement to yield predictable results;
- applying a technique or approach that would have been “obvious to

try,” *i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.

- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine prior-art reference teachings to arrive at the claimed invention. I understand that this teaching, suggestion or motivation may come from a prior-art reference or from the knowledge or common sense of one of ordinary skill in the art.

39. I understand that, for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

3. Claim Interpretation

40. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the claim. In this section, I discuss the interpretations I have applied to certain claim terms in my analysis.

41. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art at the time of the alleged

invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification and the prosecution history (i.e., the intrinsic record).

42. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that, in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner’s rejection by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

43. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider “extrinsic” evidence, including

expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the time of the alleged invention. This can be useful for technical terms whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

44. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Declaration, I apply the above standards to the terms in the challenged claims. The meanings of specific terms are discussed below in connection with evaluating the disclosure in the priority documents.

II. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

45. I have reviewed the '111 patent (EX1001) and its prosecution history (EX1002).

46. I understand that the '111 patent issued from U.S. Patent Application No. 16/552,927, filed on August 27, 2019. EX1001, codes (21), (22).

47. I understand that the '111 patent claims priority to U.S. Provisional Application No. 62/723,701, filed on August 28, 2018. EX1001, code (60).

48. I have been instructed by counsel to assume the relevant timeframe for my analysis of the prior art in this Declaration is on or before August 28, 2018.

49. Based on my review of this material, I believe that the relevant general field for the purposes of the '111 patent is network communication.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

50. I have been informed and understand that, for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date.

51. I have been informed and understand that various factors may be considered in assessing the level of a POSA, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. I have also been informed and understand that not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. I have further been informed and understand that these factors are not

exhaustive but are merely a guide to determining the level of ordinary skill in the art. I have applied this standard throughout my declaration.

52. The '111 patent involves technology in the field of network communications. I have been asked to provide my opinions as to the state of the art in this field by mid-2018. I use this timeframe because the face of the '111 patent indicates an earliest claimed priority date of August 28, 2018. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '111 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the mid-2018 timeframe, even if I do not say so specifically in each case.

53. In the context of the '111 patent and the prior art, it is my opinion that the POSA to whom the patent is addressed, on August 28, 2018, would have had a Bachelor of Science in electrical or computer engineering with at least three years of experience in digital communication system design. A higher level of education may substitute for less experience. A POSA's level of skill would not have differed materially between the August 28, 2018 date of the provisional to which the '111 Patent purports to claim priority and the August 27, 2019 date when PO filed the utility application that issued as the '111 Patent. This person would have

been capable of understanding and applying the teachings of the '111 patent and the prior-art references discussed in this declaration.

54. The basis for my familiarity with the level of ordinary skill is my own technical experience and my interaction with students and professionals in the field of electrical and computer engineering who were at this level of skill as of August 28, 2018. I am also very familiar with the professional background of those who worked in the field around the priority date of the '111 patent as I personally have worked in the industry extensively. I am well aware of the knowledge that a POSA would have had at the time this patent was written as I have been actively consulting, teaching, and carrying out research with such students and/or professionals all through that period.

55. In reaching this opinion as to the hypothetical POSA, I have considered the standard recited above such as types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field.

56. As summarized above with regards to my qualifications and experience, I possessed at least the level of skill of a person of ordinary skill in the art at the time of the alleged invention of the '111 patent.

57. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill in and around August 2018. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above.

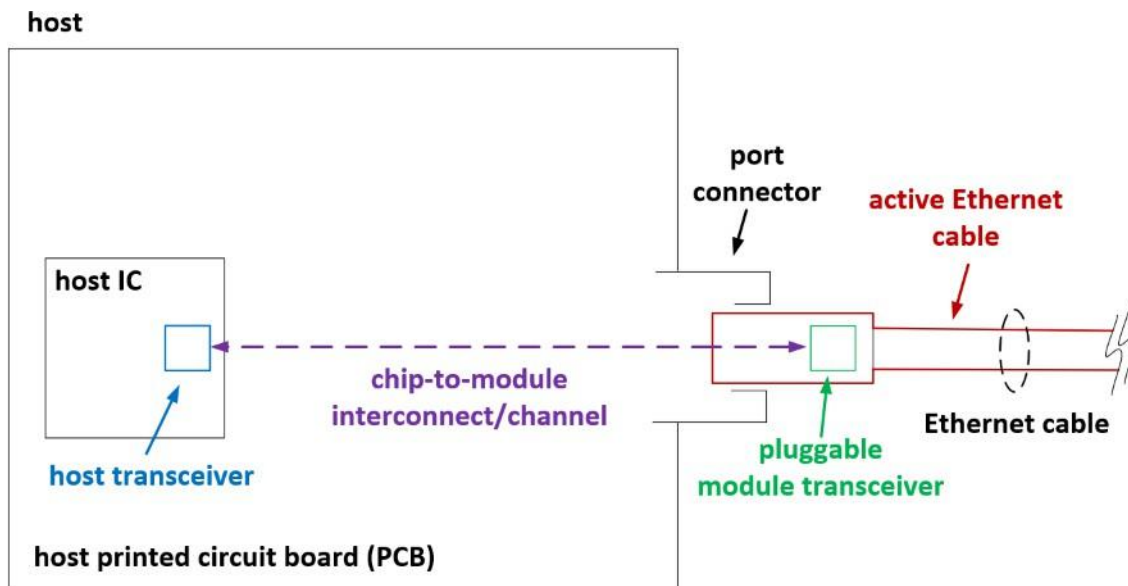
IV. THE '111 PATENT

A. Background

58. The '111 Patent concerns high data-rate communication links connecting local area network (LAN) nodes (e.g., computers). EX1001, 1:19-35, 2:54-67, Fig. 1 (links 110). The '111 Patent describes and claims “chip-to-module” links in such systems and “pluggable modules” used in such links. EX1001, 11:26-31, claims 8, 11, 16. These were known components with a variety of commercially available solutions.

59. A routing network often connects hosts—e.g., switches and routers—with active cables. EX1001, Fig. 1 (routing network 106, equipment items 108), 2:54-67. As the below schematic depicts, each host typically has an integrated circuit (“IC”) comprising a transceiver (“host IC”), and the host IC is typically mounted on a host printed circuit board (“PCB”). A host PCB often electrically connects the host IC with a host’s port connector compatible with an active cable’s “pluggable module.” Plugging the pluggable module into the port provides

electrical connection between the cable and the host IC. EX1001, claim 8; EX1005 (“Lugthart-706”), 15:25-52.



60. The pluggable module has a transceiver (“pluggable module transceiver”) that transmits signals to, and receives signals from, a transceiver (the “host transceiver”) within the host IC. EX1001, 5:10-23, claim 8; Lugthart-706, 10:17-22, 12:1-6, 15:5-10, FIG. 2A. A channel (which includes the port connector) electrically couples the host transceiver to the pluggable module transceiver. EX1001, 5:10-23. That is to say, the “channel” depicted in the figure above comprises the entire transmission medium between the host transceiver and the pluggable module transceiver. The port connector can be implemented in various ways and can be connected to the host transceiver in different ways (*e.g.*, via copper traces of varying length on the PCB. EX1001, 4:52-64, 11:38-46, 12:1-36.

61. The link between a host transceiver and a pluggable module transceiver was known as a “chip-to-module” (“C2M”) communication link. EX1001, 5:24-30; EX1027 (“802.3bs”), §120; EX1028 (“OIF-CEI-04.0”), 309, lines 3-5; EX1032 (“OIF-FD-Client- 400G/1T-01.0”), 15 (§3: Interconnect Applications) (Figure 4 showing chip-to-module communication link for both copper and fiber optic interconnects, below), 17 (§3.4: Chip to module) (Figure 8 “Chip to Module Interconnect Application Space” for fiber optic interconnect, annotated below); *see also* EX1011 (“Zerbe-058”), 1:26-28 (PCI Express could provide host electrical channel in C2M link).

62. Often, the ports on the host systems are exposed externally from the host system such that the pluggable modules with copper cables or optical fibers can reach and mate. At the same time, the locations of the chips with the SerDes transceiver(s) on the printed circuit board are determined based on the functions performed by the chips and surrounding components that work together with the chip with the SerDes transceivers.

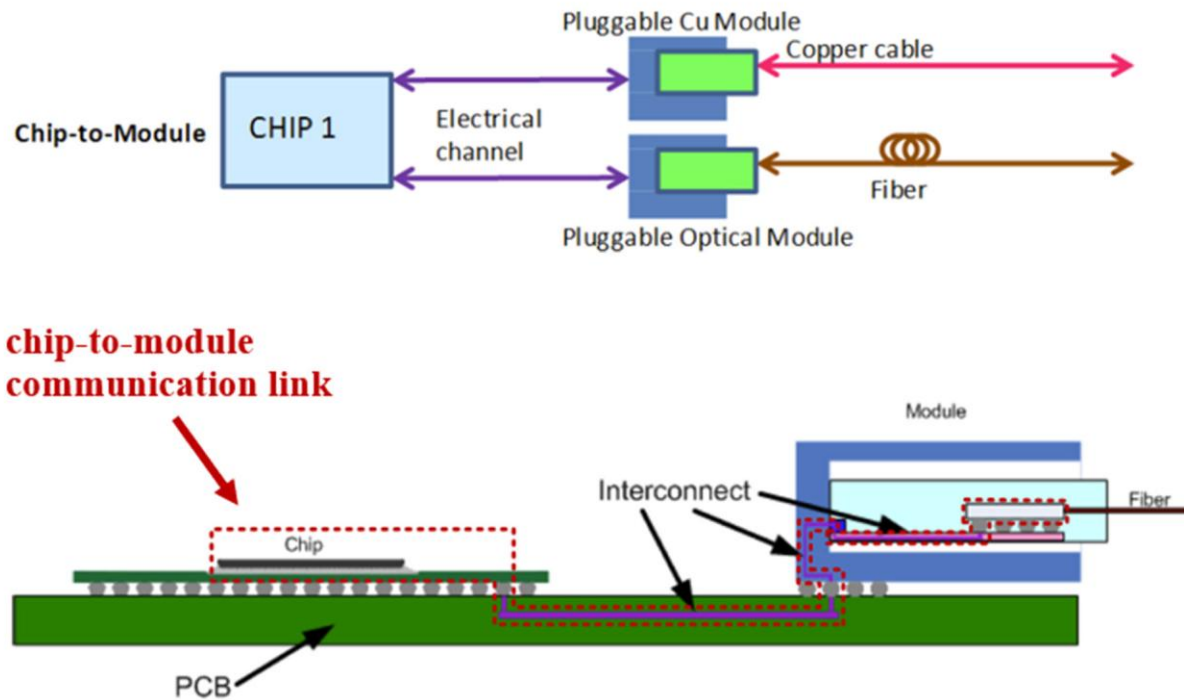


Figure 8 Chip to Module Interconnect Application Space

Depending on the size of the PCB and the size of the host system’s casing, the trace length of the C2M link may vary widely, and as such the C2M link may be either optical or electrical to accommodate the quality and the integrity of the C2M channel.

63. The link is a channel that may distort signals transmitted between the pluggable module transceiver and the host transceiver “due to the physical channel’s introduction of noise, attenuation, and signal dispersion.” EX1001, 5:20-23; EX1008 (“Raghavan”), 2:24-34.

64. A “commonly utilized technique for” mitigating this distortion was “pre-equalization”—also termed “pre-emphasis”—wherein a transmitter pre-

distorts the signal in a manner that compensates for the anticipated channel-induced distortion. Raghavan, 2:39-42; EX1001, 6:40-45. Pre-equalization was implemented by filtering (or modifying) the signal to be transmitted before the transmission. Lugthart-706, 9:38-51; EX1001, claim 8; OIF-CEI-04.0, 310, lines 8-11. By doing so, the pre-equalization can mitigate or minimize potentially non-reversible corruptions of the signal as the signal propagates over the channel. These filters were configured by applying a set of programmable coefficient values specifying the signal modifications that would compensate distortion in the C2M channel / communication link. Lugthart-706, 22:13-17; EX1001, 7:43-59.

65. One known type of pre-equalization was “adaptive.” EX1001, 7:43-59; EX1007 (“Mezer”), 2:47-50; EX1006 (“Das Sharma”), [0080]. *Adaptive* pre-equalization involved adapting (modifying) the coefficients used to perform pre-equalization based on feedback from a receiver. Adaptive pre-equalization involves transmitting signal over a communication channel, and measuring deviation (or “error”) from expected values in the signal received at the far end of the communication channel. Das Sharma, [0081]; EX1001, 7:43-59. Based on the measured deviation, the filter coefficient values in the transceiver that transmitted the signal are adjusted to better compensate for the distortion that resulted in the error in the received signal. Das Sharma, [0081]; EX1001, 7:43-59. Adaptation

can be iterative and repeated until level of the measured error becomes satisfactory, meaning acceptably low. Das Sharma, [0081]; EX1001, 13:46-64.

66. During adaptive training, information about the deviation between the known training signal and the received signal is evaluated. Das Sharma, [0081], FIG. 5. The transmitter learns about the deviation through a “backchannel” communication from the receiver and implements pre-equalization using new (e.g., adaptive) coefficient values that reduce the deviation by more accurately compensating for channel distortion. Das Sharma, [0078], FIG. 5; EX1001, 14:57-65.

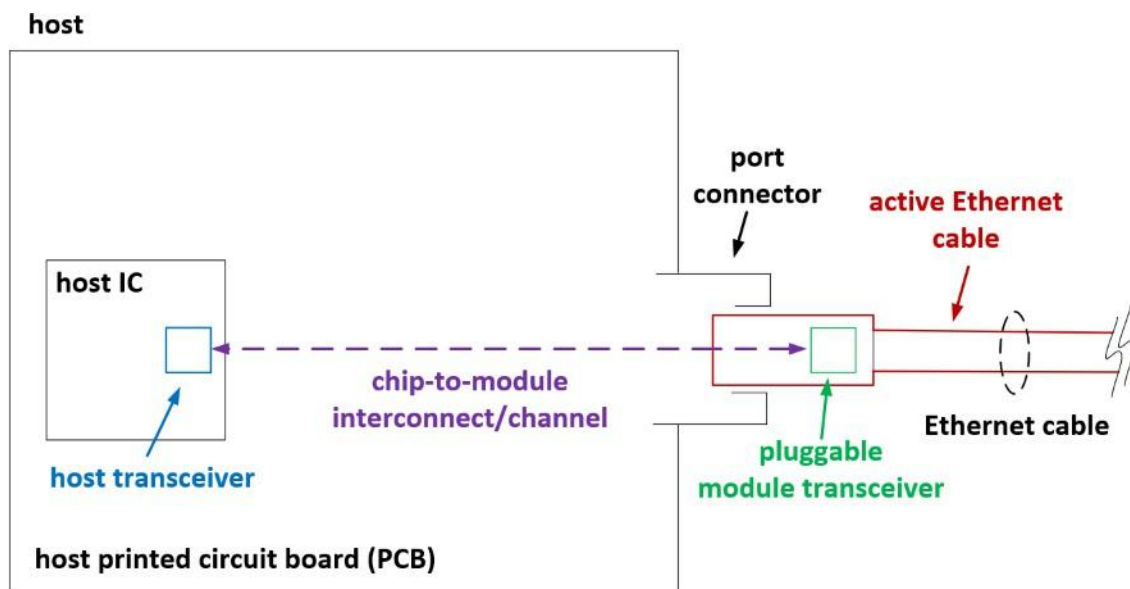
B. Described Embodiments

67. The '111 Patent describes a serializer-deserializer (“SerDes”) architecture. EX1001, 1:39-42. SerDes was a known architecture, in which data is converted between a serial and parallel data stream, and was used by Ethernet and other protocols. Raghavan, 1:33-38; EX1024 (“802.3-2015 Section 5”), 632; EX1001, 1:42-48. Personally, I have designed a variety of different SerDes solutions in my chip designs well before the priority date of the '111 patent. The '111 Patent purports to implement “an efficient adaptation interface for transmitter pre-equalizers” for a C2M link in a SerDes architecture. EX1001, 1:39-42.

68. Again, based on my personal experience, when designing a chip with embedded SerDes interfaces, because it is not possible to know the exact

environments in which the chip would be used, it is necessary to incorporate certain tuning mechanisms for adapting the SerDes in different channel environments. This is what the '111 patent calls the adaptive pre-equalization, which again was a well-known technique before the priority date of the '111 patent.

69. Referring to the simplified figure depicting a C2M link below, the characteristics of the channel between the pluggable module transceiver and the host transceiver can vary widely (e.g., length of the channel, surrounding electronic components that may generate noises and interference), and different channel types can distort the signal transmitted through the channel differently.



70. The '111 Patent describes different channel models for the different types of devices into which a cable's pluggable module can be plugged. EX1001, 11:53-12:15. Different default pre-equalization coefficients for the different

channel models are stored in registers. EX1001, 12:63-13:2, 13:18-24 (“the default coefficient value[s]” are “expected to provide a good starting point for training/adaptation” of the transmit pre-equalizers).

71. The adaptive pre-equalization process is made more efficient by storing these various “channel models” that include different “default [pre-equalization] coefficient values” for different channel types. EX1001, 12:1-58. When a “pluggable module” (*e.g.*, on a cable) is plugged into a device, the appropriate channel model can be selected. EX1001, 14:12-35. The stored equalization coefficients for the selected channel model are used as the initial coefficient values for the adaptive pre-equalization process. EX1001, 13:18-24. This results in a more efficient training process (*e.g.*, requiring fewer iterations) because the initial pre-equalization coefficient values are well suited to compensate for distortion in the type of channel to which the pluggable module has been connected. EX1001, 13:18-26.

72. To be sure, storing one or more default values in non-volatile memories was nothing new around the priority date of the ’111 patent. During the SerDes implementation process, the SerDes design would be tested for different channel models (*e.g.*, types of shielding for cable, different length of cable, chassis backplane/midplane for different trace distances, density of traces on chassis backplane/midplane), and once verified (*e.g.*, seeing the clear and open eyes on

oscilloscope), the parameters used would be stored as the default values for the corresponding channel models. This procedure had been used extensively for many years prior to the priority date of the '111 patent. In fact, the adaptation of the SerDes in different channel environments without a proper starting point (i.e., the default value) would be impractical as performing adaptation process in a brute force manner (i.e., without a proper initial starting point depicted by default values) is prone to error and may not achieve the proper functioning of the SerDes. A POSA would have known this fact.

C. Prosecution History of the '111 patent

73. The '111 Patent issued from application no. 16/552,927 filed with 20 claims. The Examiner rejected all original independent claims as obvious over EX1018 (“Kolze”) and EX1019 (“Thirumoorthy”), and indicated that original dependent claim 2—which recited that “each of the multiple registers” storing initial pre-equalization coefficient values “corresponds to a different channel model”—contained allowable subject matter. EX1002, 88, 94, 212. Applicant incorporated a form of this limitation into each independent claim and the application was allowed.¹

¹ Applicant rewrote original dependent claim 2 as an independent claim that issued as claim 1. EX1002, 77. Applicant amended original independent claim 1 to add

D. The Challenged Claims

74. The '111 Patent has 19 claims, with independent claims 1, 8, 11, and 16.

75. Claim 1 is representative. It recites a communications method performed “*in a transceiver*” that includes three limitations:

- [1.a]: “*selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model*”;
- [1.b]: “*updating the initial pre-equalizer coefficient values during a training phase; and*”
- [1.c]: “*using the updated pre-equalizer coefficient values to convey a transmit data stream.*”

76. Every Challenged Claim requires using a set of initial pre-equalization coefficients selected from among different sets of stored pre-equalization coefficients. That is the reason why the claims were allowed. But, as I have explained above, it is my opinion that this technique was known and widely practiced by POSAs, and that the claims never should have been allowed.

different limitations, EX1002, 77, but later cancelled that claim. EX1002, 36.

V. CLAIM INTERPRETATION

77. As discussed above, I have been informed that, in the present proceeding, claim terms are construed in accordance with the ordinary and customary meaning as understood by a POSA. As discussed variously below, I have applied this standard throughout the analysis presented in this declaration.

78. I have also been informed that the Board need only construe terms to the extent necessary to resolve disputes. It is my opinion that the prior art and combinations discussed below meets the claims under any reasonable interpretation of the claim terms, which I have been informed means that no claim term requires that the Board reach an exact outer boundary construction because the prior art meets the claims under any reasonable interpretation.

VI. GROUND 1: CLAIMS 1-19 ARE OBVIOUS OVER THE COMBINATION OF LUGTHART, DAS SHARMA, AND MEZER

79. I have been asked to provide my opinion concerning whether claims 1-19 of the '111 patent would have been obvious to a POSA in light of the prior art references discussed below. For the reasons explained below, it is my opinion that each of claims 1-19 would have been obvious to a POSA.

A. Lugthart-706

80. Lugthart-706 discloses an “active cable” that “includes ... first and second transceiver assemblies 105a, 105b positioned at either end of [] conductive lines 111.” Lugthart-706, 14:29-34, Fig. 2A (reproduced below). An “active cable” has electronic components that improve the quality of the signal transmitted through the cable, as well as the signals transmitted to, and received from, a host device. Lugthart-706, 14:29-31.

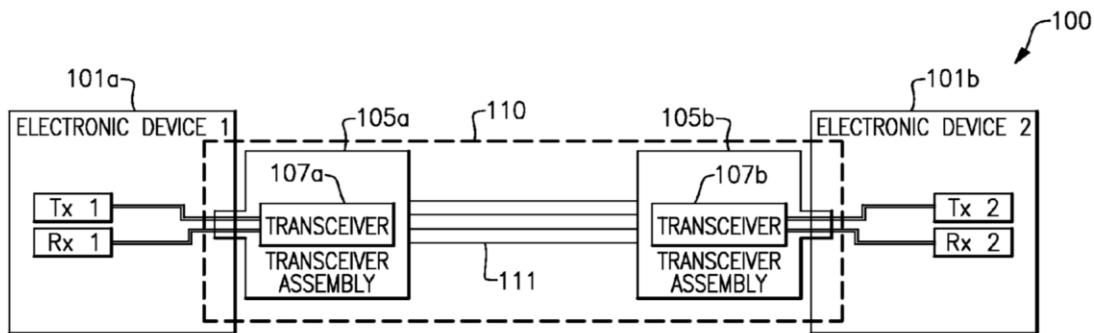
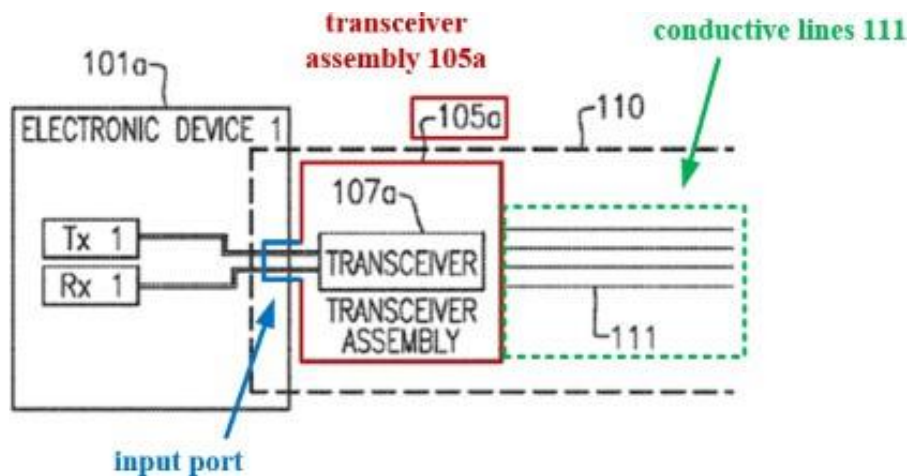


FIG. 2A

81. Focusing on the left-hand side of the cable in Figure 2A for simplicity, “first transceiver assembly 105a” (red below) “includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111” (green). Lugthart-706, 14:34-38, FIG. 2A (partially reproduced and annotated below). “Each transceiver assembl[y] 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding *port* or other interface on the respective electronic device 101a,

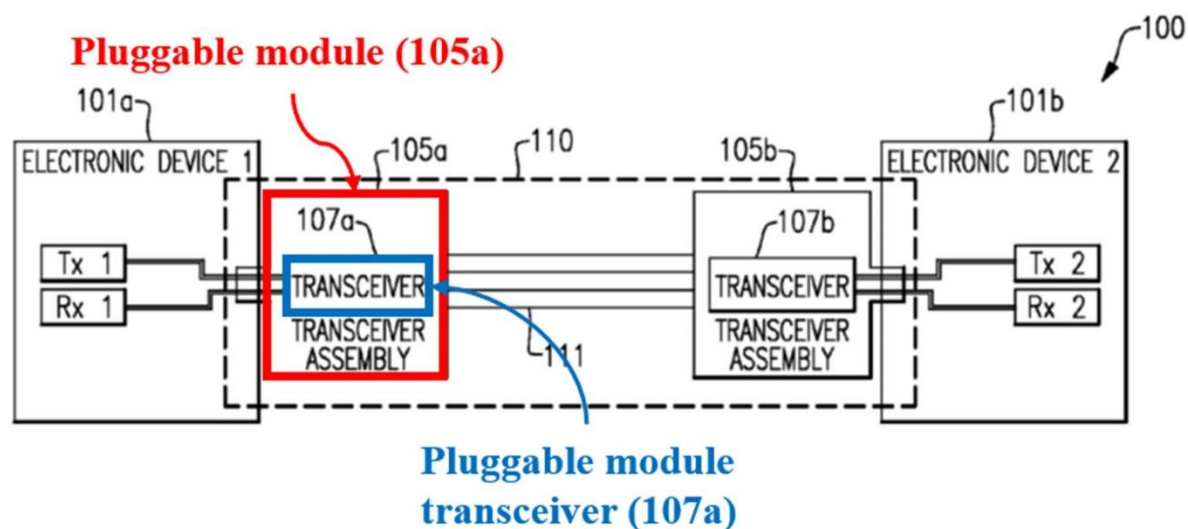
101b, and an output port that is connected to the cable.” Lugthart-706, 15:42-47,

Fig. 2A. The electronic device 101a’s port is indicated in blue below.



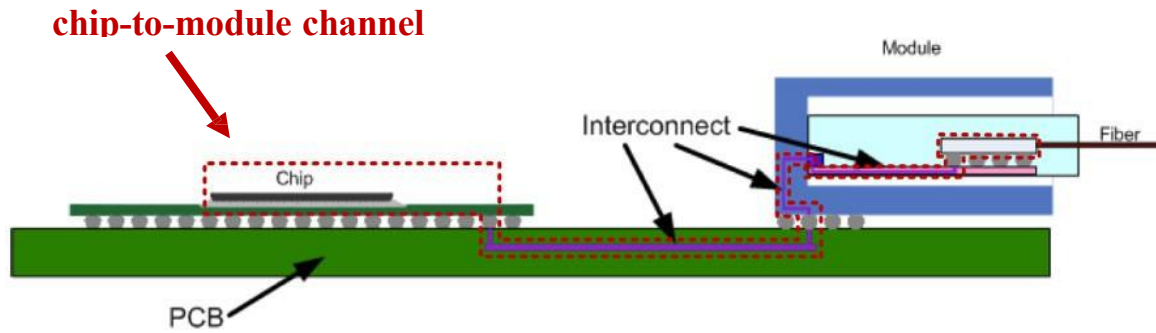
Lugthart-706, Fig. 2A (annotated detail)

82. Each transceiver assembly 105a and 105b can be “releasabl[y]” plugged into the port/interface on the host electronic device, Lugthart-706, 15:42-47, and thus is a “*pluggable module*” with a “*pluggable module transceiver.*”

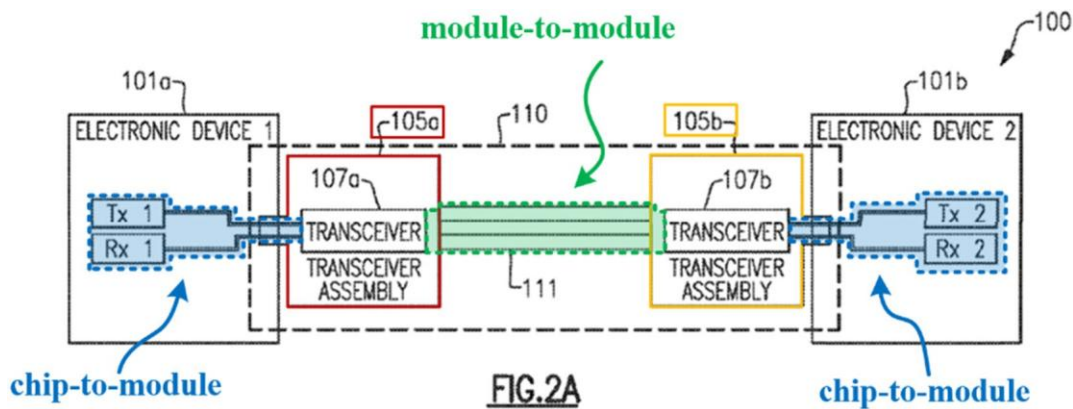


Lugthart-706, Fig. 2A (annotated)

83. Lugthart-706 describes implementing transceivers 107a/b on separate ICs. Lugthart-706, 15:27-36. Lugthart-706 describes transceivers 107a/b providing signals “to one or more additional *transceivers... on the host side*,” so that Lugthart-706 describes electronic device 101a having a host transceiver comprising an IC providing transmit (Tx 1) and receive (Rx 1) functionality. Lugthart-706, 8:61-9:1, 10:17-22. The host transceiver in electronic device 1 transmits signals to, and receives signals from, pluggable module transceiver 107a. Electronic device 101b similarly has a chip comprising a host transceiver that transmits signal Tx 2 and receives signal Rx 2. The communications link between the host IC in electronic device 101a/101b and the transceiver 107a/107b in the cable’s *pluggable module* (i.e., transceiver assembly 105a/105b) is a “*chip-to-module communications link*.” Lugthart-706’s active cable comprises three communication links (depicted below): (1) a C2M channel between electronic device 101a’s host IC and transceiver 107a; (2) another C2M channel for 101b to 107b; and (3) a module-to-module channel comprising transceivers 107a—conductors 111—transceiver 107b.

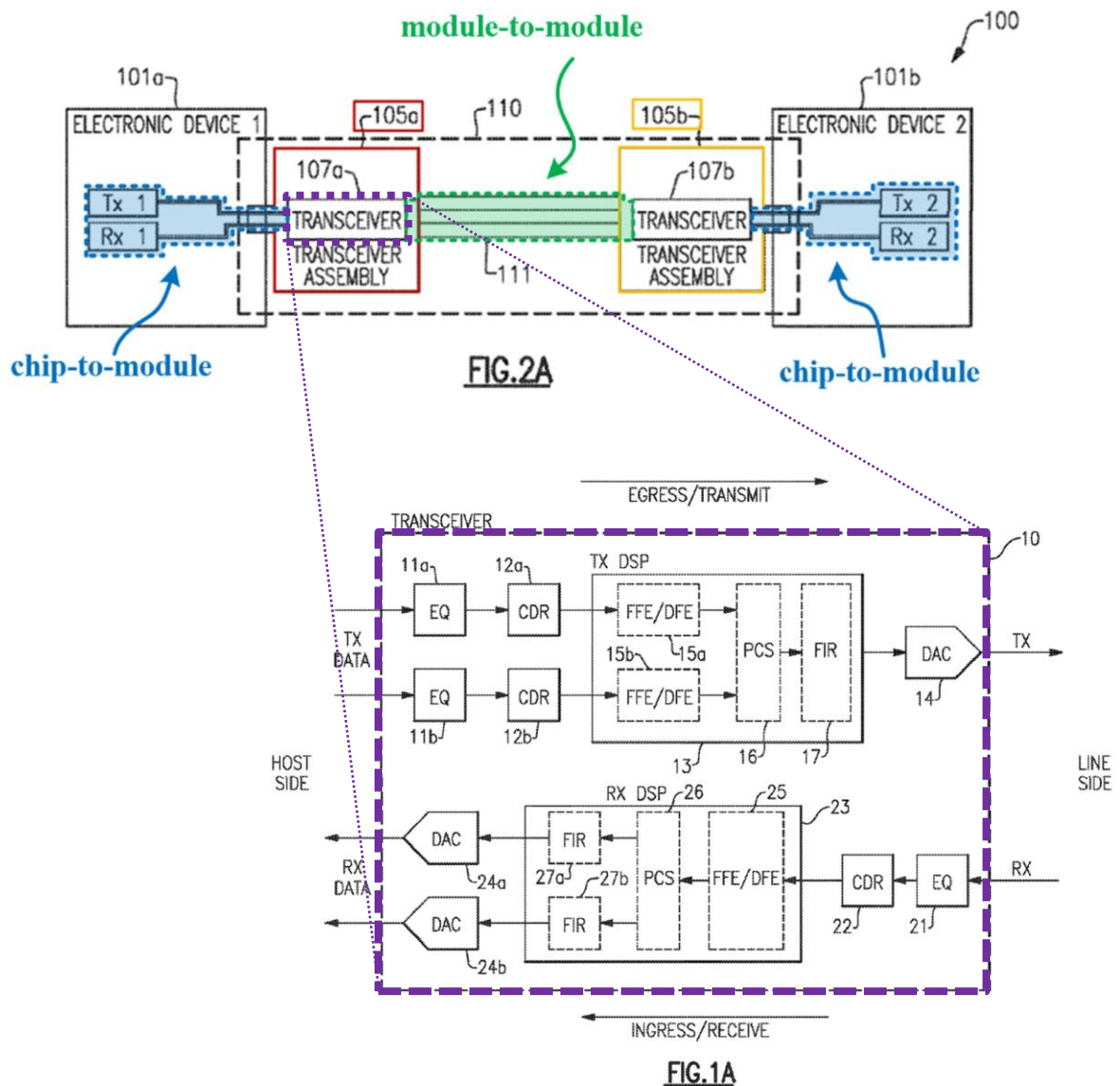


OIF-FD-Client- 400G/1T-01.0,
Fig. 8



Lugthart-706, Fig. 2A (depicting three communication links)

84. As explained below, Lugthart-706's pluggable module transceiver 107a/107b performs pre-equalization (which Lugthart-706 calls pre-emphasis) on signals transmitted to the host IC in the electronics device 101a/101b. Lugthart-706, 29:23-28. Fig. 1A (annotated below) illustrates one embodiment of Fig. 2A's pluggable module transceiver 107a/107b. Lugthart-706, 14:47-53. In other words, transceiver 10 in Figure 1A can be regarded as an exploded view of transceiver 107a in Figure 2A, as depicted below.



85. As seen in Figure 1A, Lugthart-706 labels communication paths and data signals from the host's perspective: for a transceiver 10 the adjacent electronic device (host transceiver) originates the "EGRESS/TRANSMIT" path while it terminates the "INGRESS/RECEIVE" path. Thus, the "EGRESS/TRANSMIT" data path carries data from electronic device 101a/101b (on the pluggable module transceiver's "host side") and transmitted to conductive lines 111 (on the pluggable module transceiver's "line side"), whereas the "INGRESS/RECEIVE" data path

carries data received from conductive lines 111 (on transceiver's "line side") and transmitted to electronic device 101a/101b (on the transceiver's "host" side). Lugthart-706, Fig. 1A, 8:13-32, 8:50-60. The "host side" of the pluggable module transceiver is connected to the host transceiver on the electronic device 101a/101b via a port connector, while the "line side" is connected to the cable's conductive lines 111 in Fig. 2A. Lugthart-706, FIG. 1A, 8:13-32, 14:12-15 ("electronic devices 101a, 101b" are "also be referred to herein as host devices"). The "egress/transmit" data path represents data received from electronic device 101a/101b (on the pluggable module transceiver's "host side") and transmitted to conductive lines 111 (on the pluggable module transceiver's "line side"), whereas the "ingress/receive" data path represents data received from conductive lines 111 (on pluggable module transceiver's "line side") and transmitted to electronic device 101a/101b (on pluggable module transceiver's "host" side). Lugthart-706, FIG. 1A, 8:13-32, 8:50-60.

86. The pluggable module transceiver has a receive path through "RX DSP" 23 that performs digital signal processing on the ingress/receive signal before that signal is transmitted to the host (electronic device 101a/101b in Fig. 2A). Lugthart-706, 8:26-32, 9:38-51, Fig. 1A. RX DSP 23 includes first and second "finite impulse response (FIR) filter[s]" 27a/27b. Lugthart-706, 9:38-46. RX DSP 23 uses these FIR filters to perform "adaptive and configurable signal

conditioning features such as... ***output pre-emphasis***[.]” Lugthart-706, 9:52-55, 29:23-28. “Pre-emphasis” and “pre-equalization” very often have the same meaning and were used interchangeably in the art. Raghavan, 2:39-42 (describing a “technique for combating ISI [inter-symbol interference]... known as ‘pre-emphasis,’ or pre-equalization”); EX1009 (“Schmidt”), 7:50-55; EX1010 (“Zerbe-063”), 3:24-27; EX1013 (“McCall”), 5:4-8. This is because the purpose of the pre-equalization is to compensate for the anticipated distortion occurring while the signals traverse the channel. This anticipated distortion is largely attributed to the limited bandwidth of the channel. In other words, the portion of the signals in the higher frequency range is likely to be attenuated, and the pre-equalization pre-distort the signals, by amplifying the higher frequency portion of the signals. This is what the pre-emphasis does.

87. The manner in which the FIR filters condition the signal to perform “output pre-emphasis” is described in Lugthart-706, Lugthart-706, Fig. 1A, 29:23-28, with respect to operation of FIR filter 17 in the egress/transmit path DSP 13. FIR filter 17 conditions the recovered multiplexed and coded data stream generated by PCS 16 for transmission to the line side. Lugthart-706, Fig. 1A, 29:23-28. Lugthart-706 further explains that the FIR filter is configured using “tap coefficients” and “perform emphasis on the signal to compensate for channel losses,” *i.e.*, FIR filter 17 pre-equalizes the signal transmitted over the line (e.g.,

cable). Lugthart-706, 22:13-17, 23:59-64. FIR filter 17 forwards conditioned signals to DAC 14 for transmission over cable 110 and conductive lines 111. Lugthart-706, Figs. 1A, 2A, 8:19-22, 16:11-15, 23:59-24:2. Lugthart-706 is explicit that the ingress/receive “DSP 23 can include componentry implementing similar functionality to the componentry in the egress path,” thereby indicating that—like the FIR filter 17 in DSP 13—the FIR filters 27a,b in the RX DSP 23 are also configured using “tap coefficients,” and also “perform emphasis,” *i.e.*, pre-equalization, “on the signal to compensate for channel losses,” *i.e.*, it pre-equalizes the signal recovered from the line (e.g., cable) for transmission to the host.

Lugthart-706, 23:18-23, 23:59-66.

88. Lugthart-706 describes a “full speed training phase” during which data is transmitted over the communication channel and “parameters” are “adjusted,” including “operating parameters for the equalizers.” Lugthart-706, 48:65-49:34. In my opinion, POSAs understood that this describes adaptive equalization and adjusting equalization parameters for all of Lugthart-706’s equalizers, including for FIR filters 27a/27b of the RX DSP 23 that performs pre-equalization on signals transmitted to the host transceiver. Lugthart-706, 23:18-23, 23:59-66, 48:65-49:34.

B. Das Sharma

89. Das Sharma discloses *adaptive* pre-equalization to fine-tune pre-equalization coefficients. Das Sharma, [0075], [0080]. Das Sharma stores pre-equalization coefficients in registers on the transmitter side. Das Sharma, [0078], [0106]. Das Sharma uses these adaptive pre-equalization techniques for PCI Express applications, a widely practiced SerDes method and one of the protocols that Lugthart-706 explicitly supports. Das Sharma, [0038]; Lugthart-706, 16:31-36.

90. More specifically, Das Sharma describes “a link training and equalization procedure” in which “a set of coefficients” is “applied to [the] transmission logic” of the transceiver. Das Sharma, [0066]. The set of coefficients is “applied to a finite impulse response (FIR) filter” in transmission logic of the transceiver to apply pre-emphasis before signal transmission. Das Sharma, [0079]. Das Sharma explains that “a lower bit error rate may be achieved in a channel of a communications link... when an optimized set of coefficients are applied to” the “transmission logic” of the transceiver. Das Sharma, [0089].

91. Das Sharma stores “a set of default coefficients located within registers of the transmitter” that “may be applied to the transmission... logic.” Das Sharma, [0078], [0106]. Das Sharma refers to each register storing coefficient data as a “coefficient register table.” Das Sharma, [0078]. During operation, the

default coefficients (also referred to as “pre-sets”) “are requested from the configuration registers” and applied to the transmitter’s pre-emphasis filter. Das Sharma, [0086]-[0088], [0136], [0155].

92. As discussed *supra* §IV.A, adaptive pre-equalization was a well-known process whereby (1) training signal(s) are transmitted to the receiver from the transmitter, (2) the receiver compares the received signal(s) to the known good training signal(s) and determines an error, (3) the equalization coefficients are adapted (i.e., modified), in the receiver or the transmitter, to reduce the error, (4) this continues iteratively until the received signal has an acceptable error, and (5) the adapted coefficients are adopted for use in equalizing signals transmitted over the channel from the transmitter to the receiver. Das Sharma, [0081]; EX1016 (“Sun”), 1:62-2:40 (describing adaptive pre-equalization). Das Sharma teaches that “if the target BER [bit error rate] is 10^{-12} , the error rate of data transmitted is measured..., results... are sent to the remote coefficient generation algorithm module 520 (e.g., path 511), and new coefficients are generated if the target BER is not achieved.” Das Sharma, [0081]. “Once the target BER is achieved, no new coefficients are generated and applied to the transmission... logic[.]” Das Sharma, [0081] (“new set[s] of coefficients are generated” in an iterative training fashion “until the target BER” (bit error rate) “is reached”).

93. Thus, Das Sharma teaches that pre-equalization coefficients may be optimized during a training process during which the settings of “a transmitter or receiver component” are “adjusted, optimized, etc.” to “achieve communication capability... with minimal data loss.” Das Sharma, [0075].

C. Mezer

94. Mezer discloses an equalization process that uses “a set of coefficients” that Mezer also calls “equalizer characteristic[s].” Mezer, 3:64-4:7, 7:11-15 (“‘equalizer characteristic’ shall be understood to include a set of coefficients such as a set of filter coefficients”). “[V]arious types of channels may be tested in advance to determine suitable FFE [Feed-Forward Equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected.” Mezer, 6:53-57; *see also* 3:33-4:42 (describing the process for pre-computing the various sets of coefficients).

95. Mezer explains that “[s]election of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic.” Mezer, 6:62-7:3. A POSA would have understood that this included a chip-to-module communication channel, which was known to

have an impulse response that varied with physical characteristics such as, e.g., length.

96. A POSA would have understood that Mezer's Feed-Forward Equalizer was exemplary and did not limit the use-cases for pre-stored pre-equalization filter coefficients. The Feed-Forward Equalizer, in short, the FFE, refers to a type of pre-equalization methods similar to Lugthart-706's Finite Impulse Response (or the FIR) filter that pre-distort the signal to be transmitted to compensate for the inter-symbol interference (or the ISI). Because all realistic channels have finite bandwidth incurring attenuation and distortion, the symbol(s) transmitted previously may still have non-negligible level of residual signals by the time the subsequent symbols arrive at the receiver. This phenomenon is known as the inter-symbol interference, or the ISI, which is a major challenge in high-speed transceiver designs. The method corrects the residual signal of a symbol appearing at subsequent symbol times, by pre-subtracting the anticipated residual for the symbol before the symbol is transmitted.

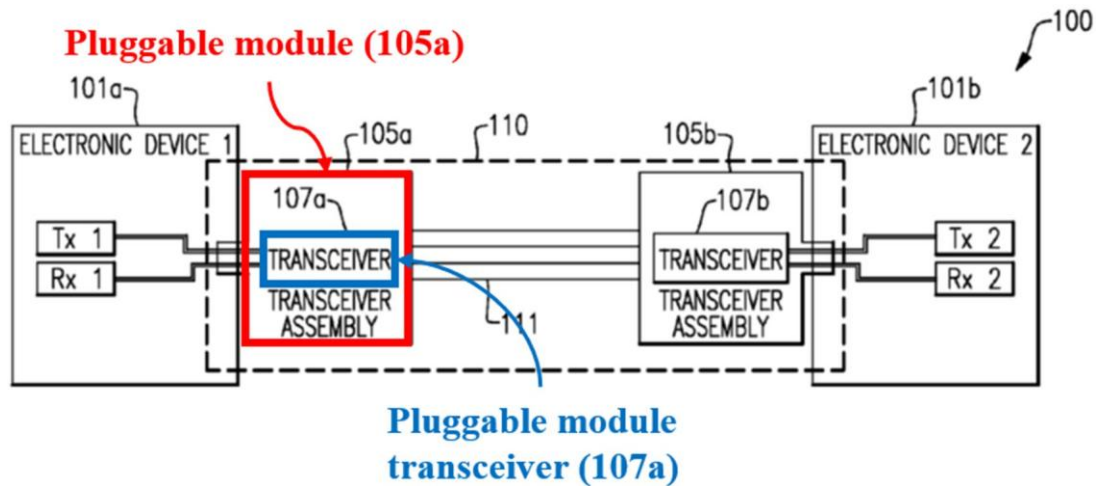
97. POSAs thus would have understood that Mezer's "FFE" performs a type of equalization like Lugthart-706's pre-equalization that uses "equalizer characteristics" (analogous to coefficients used in an adaptive pre-equalization process) to improve communication by compensating for channel distortion, including a chip-to-module channel between a host device (like electronic device

101a's host transceiver in Lugthart-706) and a pluggable module transceiver (like Lugthart-706's transceiver 107a). Raghavan, 17:4-14. Accordingly, POSAs would have recognized Mezer to teach a pre-equalization method where different initial "set[s] of coefficients" can be "pre-computed" for different types of channels and those different sets of coefficients can be "stored in [a] storage unit." Mezer, 4:4-7. In short, a POSA would have understood that Mezer's approach was just as applicable to storing transmit filter coefficients for pre-equalization—as provided by Lugthart-706 FIR filters 27a/27b or 17—as for Mezer's FFE example.

D. The Lugthart-Das Sharma-Mezer Combination

1. Reasons to Combine with a Reasonable Expectation of Success

98. As discussed above, Lugthart-706 discloses an active cable with a transceiver assembly 105a/105b ("*pluggable module*") on each end, including a transceiver 107a/107b in a module that that can be releasably plugged into a port/interface on a host electronic device. *See supra* §VI.A; Lugthart-706, Fig. 2A (annotated below). Lugthart-706's active cable can support a PCI Express link—with a *chip-to-module communications link*. Lugthart-706, 16:31-36; Zerbe-058, 1:25-28.



99. As I explained *supra* §VI.A, Lugthart-706’s pluggable module transceiver 107a/107b performs pre-equalization, e.g., pre-emphasis, on signals transmitted to the host IC in electronics device 101a/101b, respectively. *See supra* §VI.A; Lugthart-706, 29:23-28, Fig. 1A (annotated below). The “ingress/receive” data path in Lugthart-706 Figure 1A represents data received from conductive lines 111 (through pluggable module’s “line side”) and transmitted to the electronic device 101a/101b (through the pluggable module transceiver’s “host side”). *Supra* §VI.A; Lugthart-706, FIG. 1A (annotated below), 8:13-32, 8:50-60.

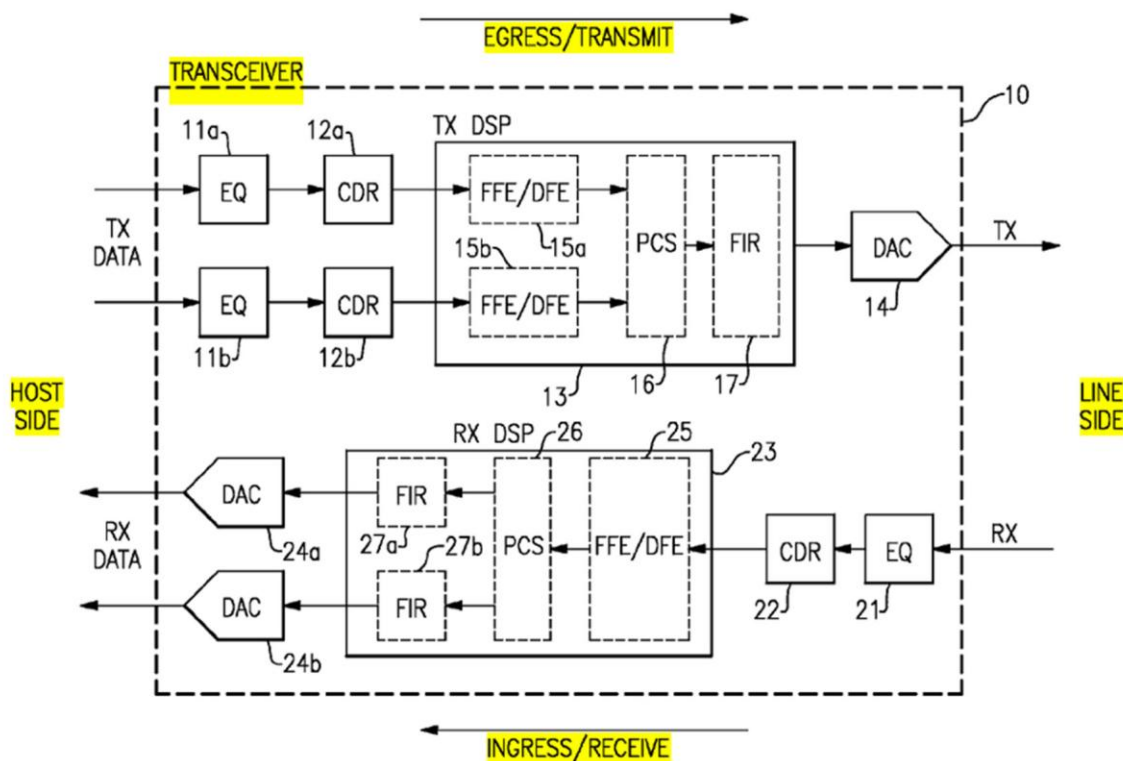


FIG.1A

100. The transceiver's "RX DSP" 23 processes the ingress/receive side signal before it is transmitted to the host IC in an electronic device 101a/101b using FIR filters 27a-b. *Supra* §VI.A; Lugthart-706, 8:26-32, 9:38-51. RX DSP 23 uses FIR filters 27a-b to perform pre-emphasis which a POSA understood is "pre-equalization." *Supra* §VI.A; Lugthart-706, 29:23-28 (describing output pre-emphasis), 23:62-64 (the FIR filters "perform emphasis on the signal to compensate for channel losses"); Raghavan, 2:39-41 (the terms pre-emphasis and pre-equalization were used interchangeably in the art); Schmidt, 7:54-55; Zerbe-

063, 3:24-27; McCall, 5:4-8 The FIR filters use “tap coefficients” to control the pre-emphasis. *See supra* §VI.A; Lugthart-706, 22:13-17, 23:21-23, 23:59-64.

a. Modifying Lugthart-706 to Use an Adaptive Pre-equalization Process With Coefficients Stored in Registers as Taught by Das Sharma

101. Lugthart-706 describes training phases. Lugthart-706, 47:53-49:37. During training, signals are transmitted over the communication channel and “parameters” are “adjusted,” including “operating parameters for the equalizers.” Lugthart-706, 48:65-49:37. In my opinion, POSAs understood that this describes adaptive equalization. While Lugthart-706 is not explicit about which of the equalizers has its parameters “adjusted” during training, POSAs understood that Lugthart-706 describes adjusting the equalization parameters for any or all of Lugthart-706’s equalizers, including FIR filters 27a/27b of RX DSP 23 and FIR filter 17 of TX DSP 13 in Lugthart-706’s transceiver assembly that performs pre-equalization on signals transmitted to the host transceiver and the signals transmitted between transceivers 107a and 107b across the conductive line 111, respectively, as discussed *supra* §VI.A. Lugthart-706, 23:21-23, 23:59-64, 48:65-49:37.

102. To the extent Lugthart-706 is read to not expressly disclose adjusting the “tap coefficients” of FIR filters 27a/27b of RX DSP 23 or FIR filter 17 of TX DSP 13 in Lugthart-706’s transceiver assembly to perform adaptive pre-

equalization, Das Sharma would have motivated a POSA to have implemented Lugthart-706 in that manner. Das Sharma teaches adaptive pre-equalization used in the same type of PCI Express protocol that Lugthart-706 describes. Das Sharma, [0038]; Lugthart-706, 16:31-36. Das Sharma stores an initial set of pre-equalization coefficients in registers of the transceiver on the transmitter side, Das Sharma, [0078], [0106], and performs an adaptive pre-equalization process that optimizes the pre-equalization coefficients during a training process to “achieve communication... with minimal data loss,” Das Sharma, [0075].

103. As shown in FIG. 2A of Lugthart-706, Lugthart-706 specifically contemplates the use of cable/optical fiber 111 connecting a pair of transceiver assemblies 107a and 107b. A POSA would have known that the cable assembly shown as 110 in FIG. 2A of Lugthart-706 would be assembled during the manufacturing process. As such, the characteristics of the channel formed by cable/optical fiber 111 connecting a pair of transceiver assemblies 107a and 107b would be largely determined during the manufacturing process, with some perturbations arising from the surrounding factors such as the interference caused by other cables in the proximity and electrical noises generated by the transceiver, and the changes in the electrical conductivity of the cable due to the variations in the temperature and humidity, etc.

104. A POSA would have known that it is convenient and even essential to store the default values for the pre-equalization parameters determined during the manufacturing process for certain operating environments that made adaptation impractical (e.g., densely packed cable conduits with large number of cable assemblies, placement of cable-assembly in proximity to noisy servers, switches and routers). Further, storing the default values improves the boot-up speed of the cable assembly as the adjustment in the pre-equalization can be done incrementally from the default values. This adjustment needs only to account for the deviations incurred during the actual use of the cable assembly (i.e., after the cable assembly is connected between the systems and booted using the default values for the pre-equalization parameters by, e.g., transmitting the training sequence).

105. It is my opinion that, if Lugthart-706 is not already understood as describing an adaptive pre-equalization process, then nonetheless a POSA would have had multiple reasons to modify Lugthart-706 to make Lugthart-706's pre-equalization process adaptive and to store the initial set of pre-equalization coefficients in a set of registers.

106. **First**, Das Sharma expressly teaches the benefits of using an adaptive pre-equalization process that optimizes the pre-equalization coefficients to the particular channel environment so that communication is achieved “with minimal data loss.” Das Sharma, [0075]. POSAs understood that an adaptive pre-

equalization process, like Das Sharma's, enables optimizing pre-equalization coefficients for the current characteristics of a particular channel, thereby compensating for changes in the operating environment (*e.g.*, temperature) that may alter the channel impairments (*e.g.*, distortion) affecting transmitted signals. EX1012 ("Zerbe- 835"), 3:54-64 (pre-equalization coefficients "can be adapted periodically during system operation to account for changes in the system environment that may impact performance"). Das Sharma also expressly teaches storing initial pre-equalization coefficients in a set of registers. Das Sharma, [0078], [0106].

107. Thus, in my opinion, Das Sharma's express teachings would have motivated a POSA to make Lugthart-706's pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in a set of registers, which are specific memory locations that the processor(s) performing the pre-equalization can access quickly and conveniently.

108. ***Second***, the benefit of adaptive pre-equalization to optimize pre-equalization coefficients and thereby improve data transmission performance was well-known. Das Sharma, [0075], [0089] (optimizing the initial pre-equalizer coefficients based on channel conditions yields "a lower bit error rate" and thus "***increase[d] data transmission performance*** within [the] communication system[.]"); Schmidt, 10:40-11:2; Zerbe-835, 5:34-39; EX1017 ("Hsu"), 2:20-28.

109. Similarly, on-chip registers were a well-known storage medium that POSAs understood were desirable for storing coefficients in a digital signal processor (DSP) because values can be retrieved from registers more quickly than from other types of storage, which may require the specific address locations for access (as opposed to the names typically associated with the registers, to which the software programs can point), thereby increasing the speed and flexibility of DSP operations. EX1021 (“Peddle”), 5:13-22 (registers permit “parallel and ... immediate[e] access and allows “data to be accessed, processed, and transferred more efficiently”); EX1022 (“Pickett”), 1:41-52, 2:8-34 (operations by a processor on data stored in “registers... within the microprocessor” requires fewer clock cycles than operations on data stored in off-chip memory like DRAM).

110. POSAs also would have been motivated to store Mezer’s below-discussed pre-computed sets of coefficients in a coefficient register table as taught by Das Sharma, to reduce the size, cost and complexity of implementing Mezer’s “lookup table.” Hsu, 1:38-41 (the “size, cost and complexity” of storing equalizer coefficients in a “lookup table” in memory may be “unacceptable”), 2:46-52 (addressing these concerns by storing equalizer coefficients in a “register array”); Mezer, 5:13-18; Das Sharma, [0075], [0078], [0106].

111. In my opinion, these well-known benefits of an adaptive pre-equalization process and storing coefficients in registers would have motivated a

POSA to make Lugthart-706's pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in registers.

112. *Third*, making Lugthart-706's pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers, both of which were known from Das Sharma, meets multiple rationales that I have been informed are indicative of obviousness. In my opinion, this combination is a "mere application of a known technique [adaptive pre-equalization using initial coefficients stored in registers as taught by Das Sharma] to a piece of prior art [Lugthart-706] ready for the improvement" because Lugthart-706's system was ready for the improved error rate reduction achieved by Das Sharma's adaptive pre-equalization. *Supra* §§VI.A-B.

113. In my opinion, this combination is also nothing more than combining known elements (Lugthart-706's pluggable module transceiver that performs pre-equalization and Das Sharma's adaptive pre-equalization that uses initial coefficients stored in registers) to perform their same known functions to yield predictable results.

**b. Modifying Lugthart-Das Sharma to Use
Different Coefficients for Different
Channel Models as Taught by Mezer**

114. To the extent Lugthart-706 and Das Sharma do not disclose storing different initial pre-equalization coefficient values for different channel models, that was taught by Mezer.

115. Mezer's equalization process uses "coefficients" that Mezer also calls "equalizer characteristics." *See supra* §VI.C; Mezer, 3:64-4:7, 7:11-15. Mezer teaches that "various types of channels may be tested in advance to determine suitable FFE [Feed-Forward *Equalizer*] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected." Mezer, 6:53-57; *see also* 3:33-4:42 (describing the process for pre-computing the various sets of coefficients). POSAs understood that Mezer's "feed-forward equalizer" were just one type of equalizer that, like others involved in pre-equalization and employing coefficient operating parameters, improved communication by compensating for channel effects, such as distortion and pre- and post-cursor ISI. For example, Lugthart-706, Fig. 1A, 23:38-43 explains the role of FFEs and DFEs ("the FFE/DFE blocks 15a-15b can implement one or more digital filters configured to equalize the incoming signal and compensate for channel effects including pre- and postcursor ISI. The filters can include an FFE and/or a DFE, for example."), and

explains a related role for the FIR 17 in 23:59-64 (“The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses.”) and also explains in 23:14-23 that FIR 27a/27b filters in DSP 23 perform similar functionality to the FIR 17 filter in DSP 13 (“In the illustrated configuration, the DSP 13 of the egress path includes a first feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 15a, a second FFE/DFE block 15b, a PCS block 16, and a finite impulse response (FIR) filter 17. Additionally, in the illustrated configuration, the DSP 23 in the ingress path includes an FFE/DFE block 25, a PCS block 26, a first FIR filter 27a, and a second FIR filter 27b. Thus, the DSP 23 can include componentry implementing similar functionality to the componentry in the egress path.”).

Therefore, a POSA would have understood that the “equalizer characteristics” (coefficients) in Mezer are analogous to coefficients used in an adaptive pre-equalization process and that Mezer’s “pre-computation” teachings for FFEs would be equally applicable to coefficients used in an adaptive pre-equalization process. Raghavan, 17:4-14. Thus, Mezer teaches that different initial “set[s] of coefficients” can be “pre-computed” for different channel types and “stored in [a] storage unit.” Mezer, 4:4-7.

116. In other words, it is my opinion that POSAs would have understood that Mezer's teachings were applicable to the pre-equalization process performed by Lugthart-706 (as modified by Das Sharma in the manner described *supra* §VI.D.1.a). Mezer, in fact, explicitly teaches that "[s]election of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic" and is explicit that this includes Ethernet channels. Mezer, 6:62-7:3. POSAs understood that Lugthart-706's *chip-to-module communications link* between the pluggable module transceiver and the host transceiver, *see supra* §VI.A, is a "communication channel that has an impulse response that varies with a physical characteristic" as described by Mezer, because the signals transmitted through Lugthart-706's *chip-to-module communications link* are distorted in ways that vary with the physical characteristics of the channel as discussed *supra* §VI.A.

117. Mezer's equalizer is on the receiver side of the communication channel rather than the transmitter side as in Lugthart-706 and Das Sharma, so Mezer's equalization is not *pre*-equalization as in Lugthart-706 and Das Sharma. Mezer, 5:25-28; Lugthart-706, 23:21-23, 23:59-64, 48:65-49:34; Das Sharma, [0078], [0081], FIG. 5. However, in my opinion, POSAs understood that the below-discussed benefits Mezer describes of storing different initial equalization

coefficients for different channel types (improved efficiency and/or using less hardware) apply equally to pre-equalization performed on the transmitter side.

Mezer, 5:40-55.

118. Indeed, applying the same type of “lookup table” approach for initial pre-equalizer coefficients on the transmitter side was known. EX1014 (“Gotman”), 12:34-55, 13:56-59 (“a measurement of a channel condition... may be used to index a lookup table and obtain... coefficient[s]” for a transmitter-side pre-equalizer); EX1015 (“Burchardt”), 10:13-52 (initial pre-equalizer coefficients “can be pre-determined and stored in a memory of the driving circuitry,” for example “in a look-up table”); Zerbe-835, 9:67-10:2 (“a simple mapping table, which can be realized through a table-lookup ROM, RAM, or through firmware, can provide the means to set TX equalizer coefficients”); Das Sharma, [0078], [0106].

119. For the foregoing reasons, it is my opinion that POSAs would have understood that Mezer’s teachings regarding equalization are directly applicable to the pre-equalization process performed by Lugthart-706 (as modified by Das Sharma as described *supra* §VI.D.1.a). Indeed, as discussed above, Lugthart-706 explains that both equalization and pre-equalization improve communication by compensating for channel effects, such as distortion and pre- and post-cursor ISI. *See, e.g.*, Lugthart-706, Fig. 1A, 23:39-43, 23:59-64.

120. A POSA would have had multiple reasons to modify the above-discussed combination of Lugthart-706 and Das Sharma to store in Das Sharma's registers different pre-computed pre-equalization coefficients for different channel models.

121. **First**, Mezer expressly teaches the benefits of using different pre-stored pre-computed pre-equalization coefficients for different channel types with different channel characteristics. Mezer, Abstract, 5:40-55. If the adaptive equalizer does not customize the initial coefficients to the channel type, “convergence of the adaptive equalizer may be slower than desirable.” Mezer, 1:12-18. Mezer explains that its use of different pre-computed coefficients for different channel types can be used in an adaptive equalization process that uses “conventional principles” like in Lugthart-706 and Das Sharma, but “because of the relatively high degree of equalization provided by the pre-computed FFE block 48, the adaptive FFE 52 may *converge more rapidly*, and/or may *require less hardware* (e.g., fewer gates) than would be the case” if initial equalization coefficients were used that were not pre-computed for the specific channel type. Mezer, 5:40-55, 2:21-22 (FFE means “feed forward *equalizer*”).

122. Thus, in my opinion, Mezer expressly teaches that using different sets of stored coefficients for different channel types can advantageously provide a more efficient adaptive training process that “converges more rapidly” to

coefficients that yield an acceptable error rate and/or can use less hardware. Mezer, 5:40-55.

123. One example of a channel characteristic Mezer describes is the length of a cable used in the channel, because different cable lengths can distort the signal transmitted through the channel differently. Mezer, 3:32-4:22. POSAs understood that Mezer's techniques are applicable to other variable channel characteristics beyond cable length, such as different lengths of PCB trace between the host transceiver and the pluggable module connector. Mezer, 6:50-53 ("selection of one of a number of stored pre-computed equalizer characteristics may be performed on the basis of a channel characteristic other than cable length"), 6:62-7:3 (Mezer's techniques "may be performed with respect to virtually any **communication channel** that has an impulse response that varies with a physical characteristic").

124. Personally, I have designed a number of SerDes components. Because these chips can be used in various system configurations, one must test and determine various characteristics of the channels that the SerDes may be coupled to. For example, varying length of the trace on the PCB affects the electrical characteristics of the channel formed by the trace, which directly determines the bandwidth and attenuation of the channel.

125. Moreover, the chips with SerDes may be driving signals over the backplane/midplane of a system. The electrical traces on the backplane/midplane are not shielded (as in the case of the cable assemblies). In this scenario, not only may the length of the trace over the backplane/midplane be extended (beyond the typical length of the trace over PCBs), but also the tightly placed traces (among potentially dozens of the SerDes utilizing the same backplane/midplanes) would create hostile channels due to inductive/capacity coupling among the tightly placed traces. As the characteristics of the channels can vary widely, it is typical that the designers of the chips with SerDes characterize multiple different channel models and store the corresponding pre-equalization parameters as potential initial values for the adaptation process.

126. Thus, in my opinion, Mezer's express teachings would have motivated a POSA to modify Lugthart-706 and Das Sharma to store different pre-computed pre-equalization coefficients for different channel models as initial coefficients for use in the adaptive pre-equalization process used by Lugthart-706 as modified by Das Sharma. A POSA would have stored the pre-computed initial pre-equalization coefficients in a set of registers in the same way Das Sharma describes for storing initial pre-equalization coefficients. Das Sharma, [0078].

127. ***Second***, it was well-known that using initial pre-equalization coefficients that accurately estimate the impact of the channel "shorten[s] the

training time” for the pre-equalizer, leading to less costly down time for training. Mezer, 5:40-55 (the adaptive training process converges more rapidly); Sun, 10:30-33, 2:33-40 (“if the initial coefficient value of equalizer is estimated accurately enough, the equalizer will nearly enter into the convergence state before training”), 2:33-40 (describing a “pre-loading technique of equalizer coefficient[s], which first writes a group of initial coefficient value pre-calculated (estimated) into the coefficient register of equalizer before the equalizer starts training process”), 10:47-11:7 (“the effect of equalizer coefficient pre-load of the present invention is much better than the prior art.”); Gotman, 12:34-55, 13:56-59; Burchardt, 10:13-52; Zerbe-835, 9:67-10:3; Das Sharma, [0078], [0082], [0106]; Mezer, 6:27-42.

128. It was also well-known that active cables like Lugthart-706’s could be plugged into different types of electronic devices 101a/101b with different types of communication links between the pluggable module connector and the host transceiver (*see* Fig. 2A of Lugthart-706) and that the *chip-to-module communication link* between the pluggable module’s transceiver and the host device’s transceiver could vary for different electronic devices and distort the signal differently. *Supra* §VI.A; Lugthart-706, 6:22-45.

129. Thus, it is my opinion that a POSA would have understood that storing different initial equalization coefficients for different types of electronic devices that might be used with the cable would increase the likelihood that initial

coefficients would be selected for a particular device that accurately estimate the impact of the chip-to-module channel on the signal and desirably yield an efficient training process.

130. **Third**, modifying the Lugthart-Das Sharma pluggable module transceiver discussed *supra* §VI.D.1.a to store different initial sets of pre-equalization coefficients for different channel models meets multiple rationales that I understand are indicative of obviousness. Modifying the Lugthart-Das Sharma pluggable module transceiver to use different pre-equalization coefficients for different C2M channel models is a “mere application of a known technique [using different initial coefficients for different channel types as taught by Mezer] to a piece of prior art [Lugthart-706 as modified by Das Sharma] ready for the improvement” because the Lugthart-Das Sharma pluggable module transceiver was ready for the improvement of a more efficient pre-equalization training process that results from having different initial coefficients for different channel types. *Supra* §VI.D.1.a.

131. This combination is also nothing more than combining known elements (Lugthart-706’s pluggable module transceiver that performs pre-equalization, Das Sharma’s adaptive pre-equalization that uses initial coefficients stored in registers, and Mezer’s different initial equalization coefficients for

different channel types) to perform their same known functions to yield predictable results.

c. A POSA Would Have Had a Reasonable Expectation of Success in Making the Lugthart-Das Sharma-Mezer Combination

132. In my opinion, a POSA would have reasonably expected success in making Lugthart-706's pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers as taught by Das Sharma. *Supra* §VI.D.1.a. Adaptive pre-equalization was well-known. *See supra* §VI.B; Das Sharma, [0081]; Sun, 1:62-2:40. Based on these teachings in the art, POSAs understood how to use training signals to perform adaptive pre-equalization and to update an initial set of pre-equalization coefficients. *See supra* §VI.B; Das Sharma, [0081]; Sun, 1:62-2:40. A POSA further knew how to store initial and updated pre-equalization coefficients in registers because this was taught by Das Sharma, Das Sharma, [0075]-[0078], and registers were a well-known storage medium for storing data in a digital signal processor like Lugthart-706's RX DSP 23. *See supra* §VI.D.1.a; Peddle, 5:13-22; Pickett, 2:8-34.

133. It is my opinion that a POSA also would have reasonably expected success in further modifying Lugthart-706 and Das Sharma to store different initial pre-equalization coefficients for different channel types as taught by Mezer. Mezer, Abstract, 5:40-55. Mezer teaches that initial equalization coefficients for

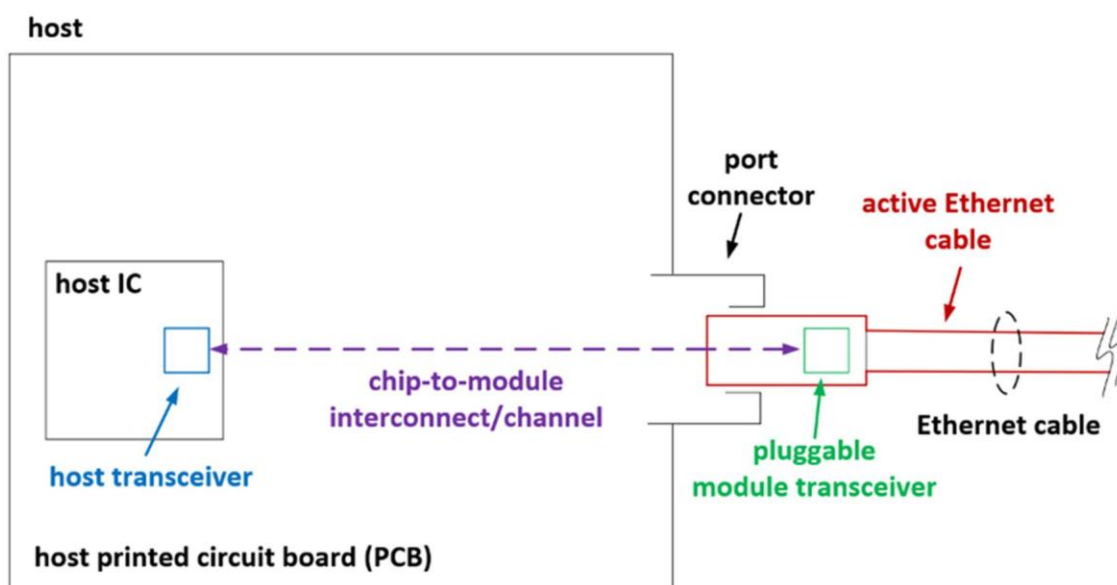
different channel types can be computed and stored in advance. Mezer, 3:32-4:22.

In terms of how the Lugthart-Das Sharma-Mezer transceiver would determine which set of initial coefficients to use when the cable is plugged into a new host device, at least two techniques were known.

134. **First**, Mezer teaches that the pre-computed equalizer characteristics may be selected based on cable length or “*on the basis of a channel characteristic other than cable length.*” Mezer, 6:27-28, 6:50-57. “Selection of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to *virtually any communication channel* that has an impulse response that varies with a physical characteristic.” Mezer, 6:62-7:3. “[W]hen it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected.” Mezer, 6:50-57.

135. Lugthart-706 teaches a “startup-phase” when its active cable is installed between two electronic devices. Lugthart-706, 47:65-48:63, Fig. 2A. “[I]n the start-up phase... [a] basic channel test may be performed... to **determine the channel parameters** such as, for example, loss, noise, dispersion, non-linearity, etc.” Lugthart-706, 48:21-23. To the extent Lugthart-706 suggests that this “channel test” tests the channel between the host transceivers in the electronic devices 101a/101b, POSAs understood that pluggable module transceivers 107a/107b could have been easily adapted to each perform a channel test for the

channel shown in red below between the pluggable module transceiver and its respective host transceiver in the electronic device 101a/101b into which the pluggable module transceiver's assembly is releasably plugged. *Supra* §VI.A (describing Lugthart-706). This would have been well-within the POSA's capabilities as it would have simply involved implementing Lugthart-706's known "basic channel test" capability in the pluggable module transceiver because Lugthart-706's host transceiver already had this "basic channel test" functionality. Lugthart-706, 48:20-23.



136. POSAs understood that Lugthart-706's "basic channel test" that "*determine[s] the channel parameters*" like "loss, noise, dispersion, non-linearity, etc." was a desirable way to select among Mezer's different sets of initial pre-equalization coefficients for different channel types. Lugthart-706, 48:20-23;

Mezer, 6:50-7:3. During Das Sharma's adaptive equalization process, equalization coefficients are adjusted to compensate for these types of "channel parameters" like loss and noise. Das Sharma, [0066], [0075]-[0077], [0087]-[0089].

137. POSAs understood that these same channel parameters used to adapt pre-equalization coefficients to yield suitably low error in the received signal were desirable parameters to use to select an initial set of pre-equalization coefficients that best compensates for the channel's impact on the signal to make the training process "converge more rapidly, and/or... require less hardware." Mezer, 5:40-55, 6:27-33, 6:50-57; Das Sharma, [0081] (describing generating new coefficient values during the adaptive equalization process based on a measured bit error rate for the channel).

138. *Second*, an alternative way to select from among the sets of pre-computed pre-equalization coefficients in Lugthart-Das Sharma-Mezer was to send a known test signal using each set, determine which set produced a received signal that most closely matched the known test signal, and select the set of coefficients that produced that closest matching signal. Mezer, 6:50-57 (selecting set of coefficients when channel type is determined); Das Sharma, [0081] (iteratively cycling through multiple sets of coefficients during the adaptive equalization process and determining a bit error rate for each one). This was well-within the capabilities of a POSA. It simply involves the pluggable module transceiver

sending a known test signal using each set of coefficients, the port transceiver determining which received test signal most closely matches the known test signal using the same error evaluation techniques known for use in adaptive equalization, Das Sharma, [0081], selecting the register with the coefficients that yielded the test signal with lowest error, and the pluggable module transceiver using the set of coefficients selected by the port transceiver.

139. In terms of whether the pluggable module transceiver or the port transceiver makes the selection of the register with the best performing coefficients, as there was backchannel communication between the transceivers, either transceiver could make the choice, and it was a matter of design choice where selection was implemented. A POSA understood that either was a possible obvious design choice.

140. It was well-known to use backchannel communication between transceivers on opposite ends of a communications channel to implement equalization. *See e.g.*, EX1023 (“Gorecki”), [0070]; 802.3-2015 Section 5, 473 (§72.6.10.2.3: Coefficient update field) (“The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer.”). The receiving host transceiver could use a backchannel communication technique to provide error information on each test signal to the transmitting pluggable module transceiver and the pluggable module transceiver

could use that error information to select the register with the coefficients that produced the lowest error. Alternatively, the receiving port transceiver could evaluate the error data and select the register with the coefficients that produced the lowest error and communication that selection to the pluggable module transceiver using backchannel communication.

141. Thus, it is my opinion that a POSA would have had a reasonable expectation of success in implementing Lugthart-706's active cable to perform adaptive pre-equalization, store in Das Sharma's registers different initial pre-equalization coefficients for different channel types as taught by Mezer, and select from among those different coefficients the set best suited to the channel in which the cable is installed because this involved simply using known techniques and was well within a POSA's skill.

2. The Resulting Lugthart-Das Sharma-Mezer Combination

142. The result of modifying Lugthart-706 based on Das Sharma and Mezer in the manner explained *supra* §VI.D.1 is an active cable 110 like the one shown in Lugthart-706's Fig. 2A with transceiver assemblies 105a/105b and conductive lines 111 between them. In the combination, receive path (RX) DSP 23 (Lugthart-706, Fig. 1A) of Lugthart-706's transceiver 107a/107b is modified to store different sets of initial pre-equalization coefficients for different channel types as taught by Mezer, store those initial coefficients in registers as taught by

Das Sharma, and use an adaptive pre-equalization process as taught by Das Sharma. *See supra* §VI.D.1; Das Sharma, [0078], [0106], [0155]; Mezer, 6:53-57. The initial set of coefficients is selected based on channel characteristics, or by using each set of coefficients to send a test signal and selecting the set that produces the best result, as discussed *supra* §VI.B. Updated coefficients generated during the adaptive training process are used as “tap coefficient” values for FIR filters 27a/27b in Lugthart-706’s modified RX DSP 23. *See supra* §§VI.A-C. Lugthart-706, 9:38-51, 22:13-17, 23:17-23, 23:59-64, 29:23-28.

143. The above-described active cable that results from modifying Lugthart-706 based on Das Sharma and Mezer is hereafter referred to as “the Lugthart-Das Sharma-Mezer Combination” or simply “Lugthart-Das Sharma-Mezer.”

E. Lugthart-Das Sharma-Mezer Meets All Challenged Claims

1. Claim 1

a. Preamble

1.PRE	A SerDes communications method that comprises, in a transceiver:
-------	--

144. A “SerDes” communications method is one in which data is converted between serial and parallel data streams. Raghavan, 1:36-38; EX1001, 1:42-48; *supra* § IV.B.

145. Lugthart-Das Sharma-Mezer’s “active cable” provides a “high-speed communication link between first and second electronic devices[.]” Lugthart-706,14:7-28. The cable includes conductive lines 111 extending between transceiver assemblies 105a/105b that include “transceivers 107a, 107b, respectively.” Lugthart-706, 14:29-34, 14:47-53, Fig. 2A. Lugthart-706’s transceivers “implement a serializer/deserializer (SerDes) function” converting between parallel data paths on the host-side and a serial data path on the line side. Lugthart-706, 7:6-20. Thus, the below-described method performed by the transceiver in Lugthart-Das Sharma-Mezer’s active cable, which meets all the steps in claim 1, is a “*SerDes communications method*” performed “*in a transceiver.*”

b. Limitation [1.a]

1.a	selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;
-----	---

146. As discussed *supra* §VI.D (describing the combination), in Lugthart-Das Sharma-Mezer, a step is performed of “*selecting one of multiple registers to specify initial pre-equalizer coefficient values.*” Lugthart-Das Sharma-Mezer’s pluggable module transceiver performs “adaptive and configurable signal conditioning features such as... ***output pre-emphasis.***” Lugthart-706, 29:23-28. POSAs understood that “pre-emphasis” and “pre-equalization” have the same meaning. Raghavan, 2:39-42 (describing a “technique for combating ISI

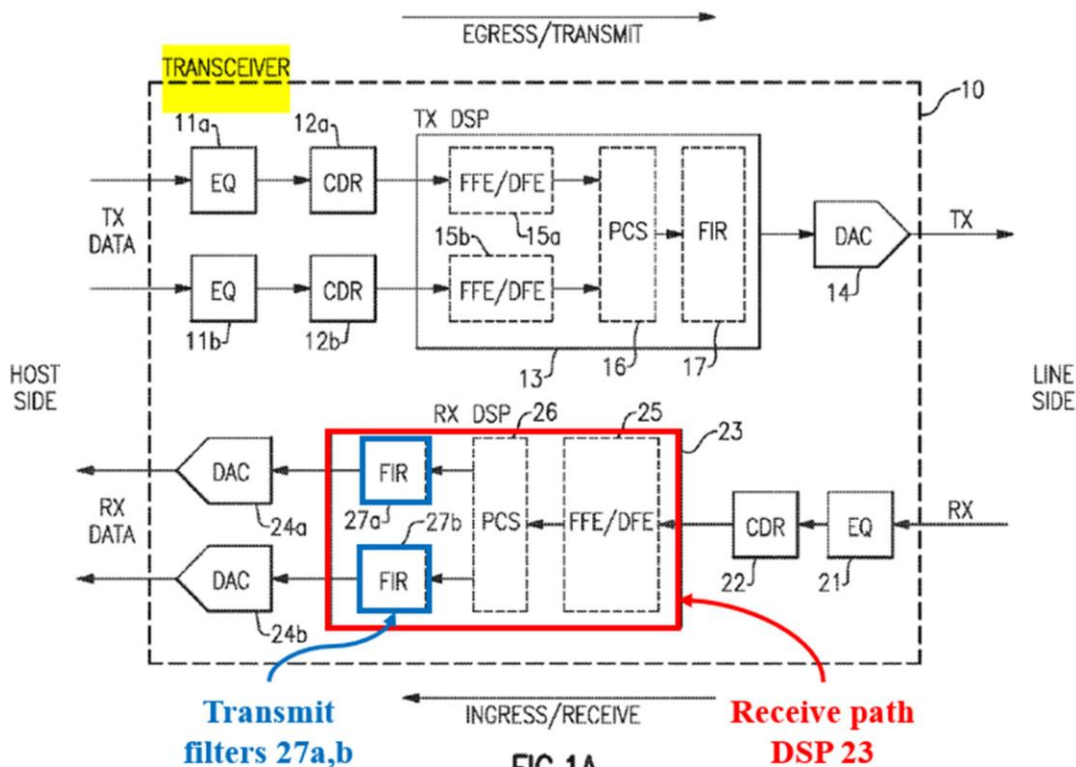
[intersymbol interference]... known as ‘pre-emphasis’, or pre-equalization”); Schmidt, 7:50-57; Zerbe-063, 3:24-27; McCall, 5:4-8.

147. The intersymbol interference, or the ISI, is a phenomenon caused by the bandwidth limitation in the channel. In a symbol period, an electrical signal, which represents one or more bits of information that the symbol carries, is transmitted. A symbol period is time-limited (i.e., the signal corresponding to the symbol must be transmitted within a symbol period) and upon the completion of one symbol period, another symbol period will follow, carrying a different electrical signal carrying one or more bits of information that the next symbol carries. The transition between two successive symbol periods takes place at a specific time instance, at which point, signals must change abruptly from one signal to the next. Since the channel has finite bandwidth, changing one signal from the next signal requires potentially infinite bandwidth in the channel, which is not possible. Thus, the residual signal from one symbol period can carry over the subsequent symbol period(s), causing ISI. In other words, the signal corresponding to one symbol period may have residual signal for the sequent symbol period(s) because turning off the signal at the symbol boundary requires infinite bandwidth of the channel.

148. One widely used technique to mitigate or minimize the ISI is the use of pre-equalization. For example, the finite impulse response (or the FIR) filter can

be used, which modifies the signal to be transmitted in one symbol period into a signal transmitted over multiple symbol periods in anticipation of the fact that there would be residual signal over multiple symbol periods. By adding anticipated residual signal in a reverse polarity to the signal to be transmitted, the receiver receives the modified signal that can negatively combine with the channel generated residual signal. Since the residual signal is generated by the channel due to the limited bandwidth, the modification of the signal transmitted by the FIR filter is essentially pre-emphasizing the signal transmitted at the higher frequency range, thereby the term “pre-emphasis.”

149. Lugthart-Das Sharma-Mezer’s pluggable module transceiver provides pre-equalization functionality in RX DSP 23, which includes FIR filters 27a/27b. Lugthart-706, Fig. 1A (annotated below), 9:38-51.



150. FIR filters 27a/27b condition the signal from the line side and forward conditioned signals to DACs 24a/24b for transmission to the host side. Lugthart-706, 23:3-13. Lugthart-706 is explicit that there are “transmission line losses on the host side” between the pluggable module transceiver and the host transceiver. Lugthart-706, 9:10-15. Lugthart-706 explains that its FIR filter 17 in the egress/transmit path “perform[s] emphasis on the signal to compensate for channel losses,” Lugthart-706, 23:59-64, and notes that the “DSP 23 in the ingress path can include componentry that is similar to the DSP 13 in the egress path.” Lugthart-706, 24:3-4, 24:3-29 (explaining that there are differences in DSPs due to the

serial-to-parallel conversion in DSP 23 versus the parallel-to-serial conversion in DSP 13 but noting no difference in the signal conditioning in the FIR filters).

151. Lugthart-706's transceiver has equalizer 21 that already "compensate[s] for transmission line losses on the line side" in the ingress/receive data path, Lugthart-706, 9:10-115, and Lugthart-706 explains that the pluggable module transceiver performs "*output pre-emphasis*." Lugthart-706, 29:21-28. Thus, POSAs understood that Lugthart-706 describes FIR filters 27a/27b as performing "output pre-emphasis" to compensate for the transmission losses that Lugthart-706 describes on the host side between the pluggable module transceiver and the port transceiver. Lugthart, 29:21-28.

152. To the extent Lugthart-706 is considered to not expressly disclose that the equalization performed by FIR filters 27 in RX DSP 23 is *pre*-equalization to compensate for transmission losses on the host side, that would have been a conventional and obvious way to implement what Lugthart-706 discloses. It was well-known that equalization can be performed on the transmitter side (i.e., pre-equalization) and/or on the receiver side and it was a matter of design choice where to perform equalization. Das Sharma, [0085]; Mezer, 5:41-55; Hsu, 1:9-12, 2:1-7. A provider of an active cable like Lugthart-706's had reason to implement pre-equalization of signals being transmitted from transceiver to host because this ensures good active cable performance irrespective of the host device to which the

cable is attached. OIF-CEI-04.0, 310 (§16.2.2: Transmitter equalizer function) (“Both host and module Tx FIRs are likely to be required to meet [test point 1a] and far-end [test point 4] eye requirements respectively for high loss channels.”).

153. FIR filters 27a/27b use “*tap coefficients*” to control the output pre-emphasis functionality. Lugthart-706, 22:13-17, 23:17-23. In Lugthart-Das Sharma-Mezer, the transceiver’s pre-emphasis coefficients are adjusted during a training phase as taught by both Lugthart-706 (48:65-49:37) and Das Sharma ([0066], [0075]). *See supra* §VI.D (describing the combination). The set of coefficients adjusted during the training phase are applied to FIR filters 27a/27b in the RX DSP’s transceiver. *See supra* §VI.D; Das Sharma, [0079] (FIR filter uses adjusted coefficients).

154. Lugthart-Das Sharma-Mezer stores “a set of default coefficients located within registers” in the pluggable module transceiver as taught by Das Sharma, [0078], [0106]. *See supra* §VI.D. In Lugthart-Das Sharma-Mezer, “various types of channels may be tested in advance to determine suitable FFE [equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, *the suitable FFE characteristic for that type of channel may be selected*” as taught by Mezer. Mezer, 6:53-57, 4:24-26 (teaching “*selecting* one of the pre-computed equalizer characteristics” (*i.e.*, sets of coefficients) “stored in the storage unit,”), 4:32-39 (describing a “*lookup table*”

used “to select one of the pre-computed equalizer characteristics stored in the storage unit 80”), 3:32-4:42 (describing the process for pre-computing the sets of coefficients); *supra* §VI.D. A POSA would have stored each set of coefficients corresponding to a different channel model in a different register so that, once the desired set of coefficients is selected, they can be accessed by simply selecting the corresponding register. The pre-computed pre-equalizer coefficients stored in registers in Lugthart-Das Sharma-Mezer are *initial pre-equalizer coefficient values*.

155. The '111 Patent says that each *channel model* is provided based on assumptions of known or predicted link characteristics and that each channel model stores “default coefficient values” provided by the “the manufacturer of the pluggable module.” EX1001, 12:1-4, 12:54-13:8. That is precisely what the different sets of default coefficients for different channel types are in Lugthart-Das Sharma-Mezer. *See supra* §VI.D; Das Sharma, [0078] (describing default coefficients “provided by manufacturer”). Thus, the different sets of *equalizer coefficient values* stored in different registers in Lugthart-Das Sharma-Mezer for different channel types correspond to “*different channel model[s]*” in Limitation [1.a].

156. When the Lugthart-Das Sharma-Mezer active cable is plugged into a host device, either a channel test is performed to determine parameters of the channel between the cable’s transceiver and the host’s transceiver, or each of the

sets of coefficients is used to send a training signal and a determination is made as to which set performs best. *See supra* §VI.D; Lugthart-706, 48:14-27. The set of default coefficients that correspond to a channel having the parameters detected during the basic channel test, or the set of coefficients that performs best, is *selected* and requested “from the configuration registers,” Das Sharma, [0155], Fig. 15, and then applied to the pre-emphasis FIR filters 27a/27b. *See supra* §VI.D.

157. As discussed *supra* §VI.D, in Lugthart-Das Sharma-Mezer, the selection of one of the registers with the desired initial coefficients can be made by the pluggable module transceiver or the host transceiver as a matter of design choice. Either option meets Limitation [1.a].

158. Accordingly, Lugthart-Das Sharma-Mezer’s pluggable module transceiver or port transceiver “*select[s] one of multiple registers to specify initial pre-equalizer coefficient values*” where each register “*correspond[s] to a different channel model.*”

c. Limitation [1.b]

1.b	updating the initial pre-equalizer coefficient values during a training phase; and
-----	--

159. Lugthart-706 teaches a “training phase” during which “operating parameters for the equalizers” are “adjusted.” Lugthart-706, 48:64-49:19, 49:20-34. Das Sharma also describes a “link ***training*** and equalization procedure,” which is a training phase during which initial coefficients are “***adjusted.***” Das Sharma,

[0066], [0075], [0063] (it is “important to provide the capability to dynamically adjust the transmitter and receiver equalization settings”). “[O]nce the initial coefficients are computed...a new set of coefficients may be computed by *adding a predefined constant or set of predefined constants to the computed set of coefficients*” at each iteration of the training phase. Das Sharma, [0124], [0136] (“multiple iterations may be performed to achieve the optimum link training and equalization transmitter...settings”). “[N]ew set[s] of coefficients” are “generated” and applied in an iterative fashion “until the target BER” (bit error rate) “is reached.” Das Sharma, [0081].

160. In Lugthart-Das Sharma-Mezer, *during a training phase*, as taught by Lugthart-706 and/or Das Sharma, the pluggable module transceiver 107a/107b—that includes the registers storing different pre-equalizer coefficients—*update[es] the initial pre-equalizer coefficients*, selected as discussed in connection with Limitation [1.a], for FIR filters 27a/27b in order to optimize those coefficients and thus reduce the error rate. *Supra* §VI.D; Das Sharma, [0063], [0066], [0075], [0081], [0124], [0136]; Lugthart-706, 9:38-51, 22:13-17, 23:21-23.

d. Limitation [1.c]

1.c	using the updated pre-equalizer coefficient values to convey a transmit data stream.
-----	--

161. In Lugthart-Das Sharma-Mezer, the pluggable module transceiver 107a/107b *us[es] the updated pre-equalizer coefficient values* generated during the training phase by applying them to FIR filters 27a/27b of RX DSP 23 to process the ingress/receive data stream in Lugthart-706 Fig. 1A and *convey a transmit data stream*. See *supra* §VI.D. As I explained above, Lugthart-706 names ***data streams*** and communication paths from the adjacent host’s perspective, but this ***signal naming convention*** is irrelevant to the filter 27a/27b’s function, which is to condition signals ***for transmission*** over the C2M channel ***to the host transceiver***. Min, [0161]. The outputs of FIR filters 27a/27b are connected to DACs 24a/24b, respectively, that “include outputs that generate host side receive data (RX DATA)” which is *a transmit data stream* that is ***transmitted*** to the host device. Lugthart-706, 8:28-32; *supra* §VI.D. Thus, Lugthart-Das Sharma-Mezer’s pluggable module transceiver 107a/107b *us[es] the updated pre-equalizer coefficient values to convey a transmit data stream*.

2. Claim 2

2	The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
---	--

a. “C2M channel”

162. As discussed *supra* §§ IV.A and IV.B, “*chip-to-module (C2M)*” describes a channel between a transceiver on a host IC and the transceiver on a pluggable module that plugs into a port on the device. EX1001, 5:24-30, 11:26-31 (describing the module side of a “C2M link” as implemented in the form of a *pluggable module*” such as a “*QSFP*” interface “that is inserted into a port in a host such as a switch or a router”); OIF-FD-Client- 400G/1T-01.0, Fig. 8 (below), 15 (§3: Interconnect Applications) (Figure 4 showing chip- to-module communication), 17 (§3.4: Chip to module) (Fig. 8 “Chip to Module Interconnect Application Space”).

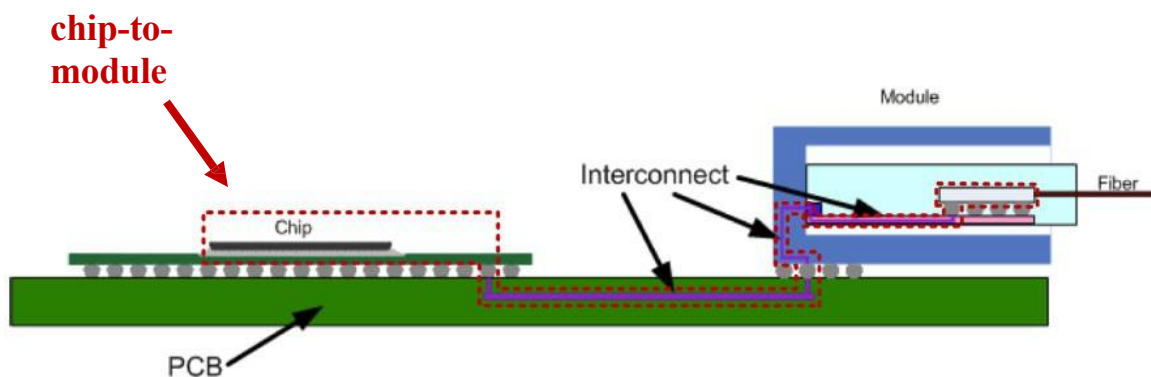


Figure 8 Chip to Module Interconnect Application Space

163. The claimed phrase “insertion loss” describes the loss of signal strength (or quality) incurred when the pluggable module is inserted into a port. The electrical connection between the pluggable module and the port represents a discontinuity of the electrical medium, which causes the loss of signal strength. The claimed phrase “package loss” refers to the loss of signal strength (or quality) while the signal traverses from the transceiver on the silicon die inside the chip, through the bonding wires of the chip, and through the pins exposed externally from the chip. The transceiver, which is located on the silicon die inside the chip, has the pre-emphasis filter, and in characterizing the C2M channel, the “insertion loss and package loss characteristics” would be counted for as the part of the channel.

164. Lugthart-Das Sharma-Mezer meets claim 2 because Lugthart-706 teaches an active cable having a pluggable module that, when the cable is plugged into a host device, forms a *chip-to-module channel* between a host transceiver and the pluggable module transceiver. *Supra* §VI.D. Lugthart-Das Sharma-Mezer’s active cable includes a “**QSFP** interface,” which is a “**pluggable module**” and includes transceivers 107a/b. Lugthart-706, 15:25-52 (describing active cable including the transceivers 107a/b in a connector compatible with a QSFP input port on the host), 50:34-59 (describing an example active cable including the

transceivers in a QSFP interface), 51:64-52:5 (referring to QSFP interface as a “pluggable module”), FIG. 17A.

165. The pluggable module transceivers 107a/b can send electrical signals to “one or more additional *transceivers... on the host side*” (host transceivers) in the electronic devices 101a/b. Lugthart-706, 10:17-22. These signals can be sent “over *high loss PCB channels*” connecting the pluggable module transceivers 107a/b and the host transceivers. Lugthart-706, 29:39-43.

166. Lugthart-706 explains that “transceivers can be a monolithic device including analog and digital components *included in a single integrated circuit (IC)*, for example, or may instead include multiple integrated circuits.” Lugthart-706, 15:31-35. POSAs would have understood that Lugthart-706 described a host transceiver in electronic device 101a/b as comprising an IC, thus providing the “chip” for a C2M channel. Regardless, POSAs would have known that a conventional way to implement the host transceiver was with an IC mounted on the PCB in the host. Thus, in Lugthart-Das Sharma-Mezer, the “high loss PCB channel[]” that connects the host transceiver (an integrated circuit or “*chip*”) to the pluggable *module* transceiver 107a/b is a “*chip-to-module (C2M) channel*.” Lugthart-706, 10:17-22, 15:25-52, 29:39-43, 50:34-59, 51:64-52:5.

167. To the extent “*chip-to-module (C2M) channel*” is interpreted to mean a chip-to-module channel conforming to the 802.3-2015 Ethernet standard

referenced throughout the '111 Patent, Lugthart-Das Sharma-Mezer still meets the claim because Lugthart-706 describes that the communications protocol used over the PCB channel between the pluggable module transceiver 107a/b and the host transceiver can be “*Ethernet*.” Lugthart-706, 48:16-20, 16:19-26 (“conducting lines 111” can “reside on a PCB or other substrate”).

b. “C2M channel insertion/package loss”

168. As explained above, “*insertion loss*” refers to losses in signal strength as the pluggable module is connected to a port. EX1025 (“Newton’s”), 661; EX1026 (“Oxford”), 305. “*Package loss*” refers to loss attributed to the particular “integrated circuit package” or “PCB layout” over which the signals travel. EX1001, 11:55-60; Oxford, 7 (“package” definition), 3 (definition of “dissipation (loss)”), 6 (“loss” definition refers to “dissipation”).

169. While Lugthart-706 does not expressly say that the “high loss PCB channels” on the host side have “*insertion loss*” and “*package loss*,” a POSA understood that this was so because it was well-known that there is *package loss* for signals exiting the pluggable module’s transceiver and entering the host device’s transceiver, as well as *insertion loss* as the signal propagates over the printed circuit board (PCB) between those transceivers. Lugthart-706, 29:21-37 (describing the use of signal conditioning features (e.g., “output pre-emphasis”) to compensate for channel “insertion loss”), 15:25-42 (disclosing that the transceiver

is “enclosed in a packaging” comprising “materials suitable for electronic and computer interfaces”).

170. In view of the foregoing, POSAs understood that the host-side “loss”—that Lugthart-706 describes compensating for using pre-equalization performed by the pluggable module transceiver—includes both *insertion loss* and *packaging loss*. Lugthart-706, 29:21-43.

171. Thus, in Lugthart-Das Sharma-Mezer, the different chip-to-module channel models for which pre-equalizer coefficients are stored in registers include “different channel models [] for chip-to-module (C2M) channels with different insertion loss and package loss characteristics” as in claim 2. *Supra* §VI.D.

172. Alternatively, to the extent Lugthart-706 is considered to not expressly disclose compensating for insertion and package loss, a POSA would have been motivated to have the pre-equalization that Lugthart-Das Sharma-Mezer performs compensate for insertion and package loss, with a reasonable expectation of success, because these were well-known losses in a chip-to-module channel between an active cable’s transceiver and the host device’s transceiver which were routinely compensated for by the type of pre-equalization used in Lugthart-Das Sharma-Mezer. Lugthart-706, 15:25-42, 29:21-37; Kolze, [0060] (describing the use of equalization to compensate for different types of channel loss); Das Sharma, [0075] (same); *supra* §VI.D. Thus, an obvious implementation of Lugthart-Das

Sharma-Mezer stores in its registers “*different channel models [] for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.*” *Supra* §VI.D.

3. Claim 3

3	The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.
---	--

173. Das Sharma’s pre-equalization is performed “on a per ***transmitter-receiver pair basis*** to ensure interoperability” between the transmitter and the receiver in compensating for the channel’s distortion. Das Sharma, [0064].

174. It was well-known that receive equalization influenced the appropriate transmit equalization: “[i]deally, transmit and receive equalization work together to mitigate the degradation imposed by the channel, and thus allow increased data rates and/or reduced probability of communication errors.” Zerbe-835, 1:17-27.

Thus, POSAs understood that, when a particular host-side transceiver compensated for a particular distortion in a received signal, it was unnecessary for the pluggable module transceiver’s pre-equalization to compensate for that same distortion.

Moreover, by avoiding pre-emphasis, the transmitter could operate at lower power.

Conversely, for a different host-side transceiver that was incapable of compensating for that same distortion in a received signal, it would be desirable for the cable-side transceiver’s pre-equalization to do so. POSAs also knew that transmitter pre-emphasis was desirable to compensate channel distortion because it

could mitigate noise enhancement wherein the receiver equalization boosts both received noise and signal.

175. A POSA had reason to implement the Lugthart-Das Sharma-Mezer combination so that *at least some of the different channel models presume different types of receiver equalization* to ensure interoperability between different transmitter-receiver pairs to ensure that they all mitigate degradation imposed by the channel as taught by Das Sharma and Zerbe-835. Das Sharma, [0064]; Zerbe-835, 1:17-27.

176. A POSA would have had a reasonable expectation of success in implementing Lugthart-Das Sharma-Mezer in this manner because it simply required not using pre-equalization coefficients to compensate for some distortion that the host-side transceiver's equalization can compensate for. It was common practice for pluggable modules to be compatible with a range of hosts, such as prior generations or hosts with different performance levels. The proposed combination is an example of that, such that a POSA would have expected success.

4. Claim 4

4	The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.
---	---

177. The antecedent for claim 4 is Limitation [1.a] *selecting one of multiple registers to specify initial pre-equalizer coefficient values...* in claim 1, *supra*

§VI.E.1.b, which recites a method performed *in a transceiver, supra* §VI.E.1.a (Limitation [1.PRE]). The '111 Patent describes testing each set of coefficients and selecting one that performs best based on a performance characteristic such as “an error signal energy” or a “bit error rate.” EX1001, 1:59-2:16, 14:12-43, claims 5-6. The '111 specification's only description supporting claim 4's selection of the register with the best performing coefficients is Figure 8, steps 802-812, and 14:12-15:3.

178. That disclosure describes actions by “training controller link or link controller” that receives test signals (steps 808 and 818) and selects the best performing register on a “**remote** transmitter” that transmitted the test signals. EX1001, 14:12-56. The “**remote** transmitter” is “instructed to use those preset coefficients” from a register selected in step 812 “as a starting point” and “program the pre-equalizer with the preset coefficients from the selected register and transmits a training pattern and/or data.” EX1001, 14:36-43.

179. Accordingly, claim 4 may be met by more than one transceiver, with at least one step (determining a performance characteristic for each register in claim 4) performed by a receive-side transceiver while another step (claim 1's conveying a transmit data stream) is performed by a transmit-side transceiver. Thus, claim 1's method, as modified by claim 4, can be met by some steps

performed by the pluggable module transceiver and others by the port transceiver in the above-discussed obvious implementation of Lugthart-Das Sharma-Mezer.

180. As discussed *supra* §VI.D, in one obvious implementation of Lugthart-Das Sharma-Mezer, a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send different instances of a test signal that were pre-equalized with the different set of coefficients, determining at the port transceiver which set of coefficients had the best performance characteristic (e.g., produced a signal with the smallest error), and then selecting (at either the pluggable module transceiver or the port transceiver) the set of coefficients that performed best. Mezer, 6:50-57 (describing determining a “channel type[]” to select between the different pre-computed channel models associated with different channel types); Das Sharma, [0081] (describing testing multiple different sets of coefficients in an iterative fashion and determining a bit error rate for each). That meets “*wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.*”

5. Claim 5

5	The method of claim 4, wherein the performance characteristic is an error signal energy.
---	--

181. Various performance characteristics were known for comparing a received signal to the known transmitted signal. Mezer “adapt[s]” equalizer

coefficients “on the basis of *an error signal*” that “indicates deviation of the” received training signal “from a pre-determined ideal signal profile.” Mezer, 2:21-50, 2:66-3:7. That meets the claimed “*error signal energy*.” EX1001, 14:26-30 (“measur[ing] error signals” represents “the difference between the equalized receive signals and an idealized receive signal”).

182. Furthermore, it was well-known in the art to use “*error signal energy*” as a performance characteristic for a control system. E.g., EX1029 (“Thapa”), [0160] (computing error signal energy); EX1030 (“Mani”), 11:34-49, claims 2, 5, 14 (same); EX1031 (“Chhetri”), 14:42-53 (same). Thus, an obvious implementation of Lugthart-Das Sharma-Mezer uses *error signal energy* as the performance characteristic to select among the registers storing different sets of pre-computed pre-equalization coefficients. *See supra* §VI.D.

6. Claim 6

6	The method of claim 4, wherein the performance characteristic is a bit error rate.
---	--

183. Another known performance characteristic for comparing a received signal to a known transmitted signal was bit error rate. Das Sharma teaches the use of bit error rate and explains that it may be “the ratio of the number of bits incorrectly received (errors) and the total number of bits received.” Das Sharma, [0076]-[0077]. In another obvious implementation of Lugthart-Das Sharma-

Mezer, the performance characteristic used to make the selection from among the registers storing different sets of pre-computed pre-equalization coefficients, *supra* §VI.D, is *bit error rate* as taught by Das Sharma.

7. Claim 7

7	The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.
---	---

184. As discussed *supra* §VI.E.1.c (Limitation [1.b]), Lugthart-Das Sharma-Mezer implements a training phase, as taught by Lugthart-706 and/or Das Sharma, during which the pluggable module transceiver 107a/107b updates the pre-equalizer coefficient values for FIR filters 27a/27b from the selected register to optimize those coefficient values to reduce the error rate. *See supra* §VI.D; Das Sharma, [0063], [0066], [0075], [0081], [0124], [0136]; Lugthart-706, 9:38-51, 22:13-17, 23:17-23.

185. A POSA had reason to update the coefficient values in the selected register itself. It was known to store initial equalization coefficient values in a storage device and to then update those values directly in the storage medium during a training process. Gorecki, [0069] (the equalizer coefficients are “pre-programmed” and stored in a storage device “until re-programmed” to “be fine-tuned to enhance the system performance”). POSAs understood that using this technique in Lugthart-Das Sharma-Mezer would advantageously result in the coefficients in the selected register that represent a particular chip-to-module

channel being updated to reflect the channel more accurately given the adaptation that occurs during the training process. When Lugthart-Das Sharma-Mezer in this known (as taught by Gorecki) and obvious manner, the pluggable module transceiver *updat[es] the selected register with the updated pre-equalizer coefficient values* as required by claim 7.

8. Claim 8

a. Preamble

8.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
-------	---

186. The '111 Patent uses “*chip-to-module communications link*” consistent with its known meaning—it is a communications link between a host IC transceiver in a host device and a pluggable module transceiver that can be plugged into a port on the host. *See supra* §VI.A; OIF-FD-Client- 400G/1T-01.0, Fig. 8 (below), 15 (§3:Interconnect Applications) (Figure 4 showing chip- to-module communication), 17 (§3.4: Chip to module) (Fig. 8 “Chip to Module Interconnect Application Space”).

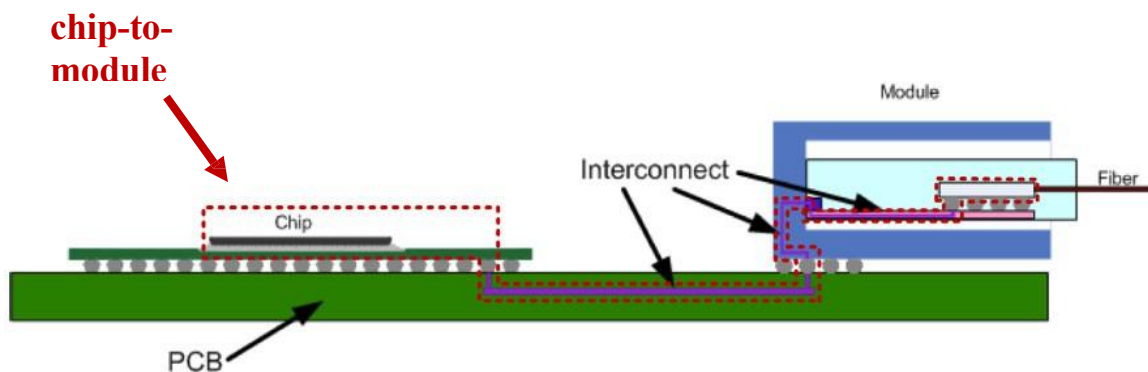
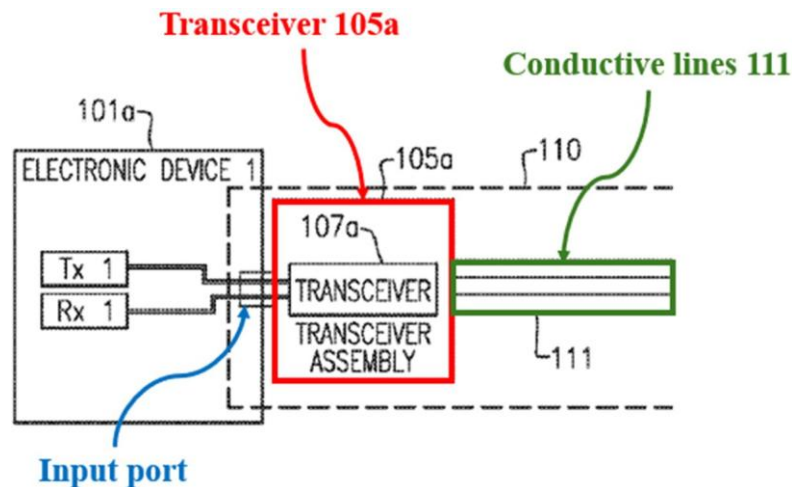


Figure 8 Chip to Module Interconnect Application Space

187. As discussed *supra* §§VI.A and VI.D., Lugthart-Das Sharma-Mezer’s communications link between a host IC transceiver in Lugthart-706’s electronic device 101a/101b and transceiver 107a/107b in the cable’s *pluggable module* (Lugthart-706’s modified transceiver assembly 105a/105b) is a “*chip-to-module communications link*.” *cf. supra* §VI.E.2 (claim 2, “C2M channel”).



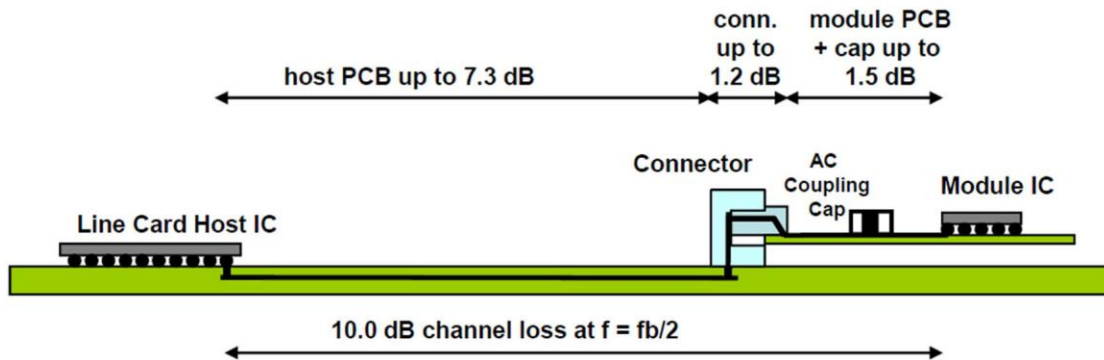
188. Transceiver assembly 105a is a *pluggable module* (red in the annotated figure below) with a port that is releasably coupled to a *port connector* (blue) on the first electronic device 101a. Lugthart-706, 14:29-38, 15:42-47, Fig. 2A (annotated detail above). The host device has a transceiver. Lugthart-706, 10:17-22 (transceiver 105a produces electrical signals that “can be provided to one or more additional *transceivers* electrically coupled to the transceiver... *on the host side*”).

189. The host transceiver is a *port transceiver* as claimed because it is connected to the pluggable module transceiver via a port connector. EX1001,

1:50-51 (“a port connector couples a port transceiver to a pluggable module transceiver”). Transceiver 107a is a *pluggable module transceiver* because it is in transceiver assembly 105a which is a *pluggable module* releasably pluggable into the host device port. Lugthart-706, 4:10-30, 15:42-52, 52:1-5.

190. Regardless, POSAs would have had reasons to implement Lugthart-Das Sharma-Mezer with a reasonable expectation of success so that it complied with the Ethernet standard because Lugthart-706 and Mezer each describe supporting Ethernet, and such standards-compliant implementation was conventional. Lugthart-706, 48:16-20, 53:31-39; Mezer, 4:53-57, 6:62-7:3. This obvious implementation would have met the Ethernet standard’s description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. 802.3bs-2017, 323-30 (Annex 120C), 350-72 (Annex 120E), 350 (“The chip-to-module interface is defined using a specification... that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0”); OIF-CEI-04.0, 334, Fig. 16-15 (below).

Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model



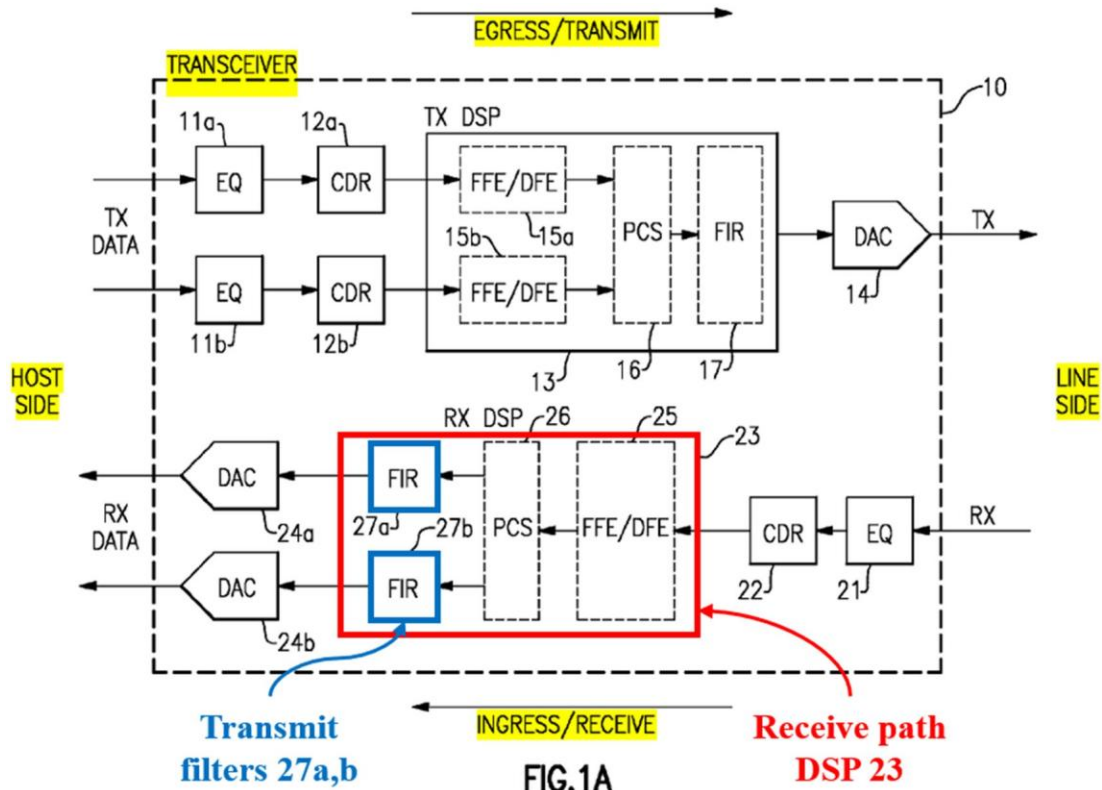
191. In OIF-CEI-04.0 Figure 16-15, the “Line Card Host IC” is the “*port transceiver*,” the “module IC” is the “*pluggable module transceiver*,” and the “Connector” is the “*port connector*,” meeting [8.PRE].

b. Limitation [8.a]

8.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
-----	---

192. Lugthart-Das Sharma-Mezer is an active cable with Lugthart-706’s *pluggable module transceiver* 107a modified as discussed *supra* §VI.D. As shown in Lugthart-706 FIG. 1A, this *pluggable module transceiver* has a “host side” connected to electronic device 101a through the host’s port connector (discussed *supra* [8.PRE]) and a “line side” connected to the cable’s conductive lines 111. Lugthart-706, FIG. 1A, 8:13-32. An “ingress/receive” data path represents data received from conductive lines 111 (“line side”) and transmitted to electronic device 101a (“host side”) after being processed by receive path RX DSP 23.

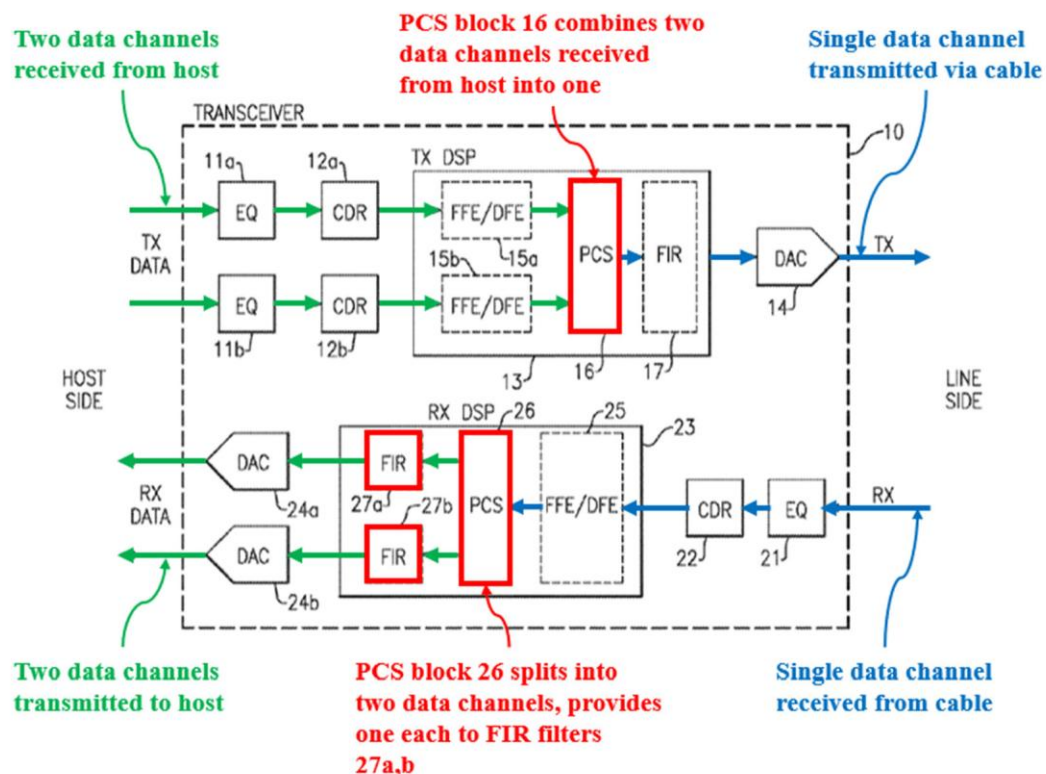
Lugthart-706, FIG. 1A (annotated below), 8:13-32, 8:50-9:9, 9:38-51, 10:17-22, 12:1-5, 15:42-47, FIG. 2A, 8:28-32 (receive path DSP 23's outputs are electrically coupled to DACs 24a/24b which "include outputs that generate host side receive data (RX DATA).")



193. Receive path DSP 23 includes FIR filters 27a/27b, as shown in the detailed view of the transceiver 107a (*the pluggable module transceiver*) in FIG. 1A. Lugthart-706, 9:38-51. FIR filters 27a/27b are *transmit filters* because they process data to be transmitted to the host. As discussed *supra* §VI.E.1.b (Limitation [1.a]), Lugthart-Das Sharma-Mezer's FIR filters 27a/27b pre-equalize the signals transmitted to the host device transceiver. Lugthart-706, 23:18-23,

23:59-66. The host device transceiver is a “*port transceiver*” as discussed *supra* §VI.E.8.a (Limitation [8.PRE]).

194. Lugthart-Das Sharma-Mezer’s FIR filters 27a/27b *each pre-equalize[s] a corresponding serial symbol stream being transmitted to a port transceiver*. Lugthart-706’s transceivers “implement a serializer/deserializer (SerDes) function” converting between multiple signals on the host side and a single signal on the line side. Lugthart-706, 7:6-20, Fig. 1A (annotated below), 24:17-20 (RX DSP 23’s PCS block 26 “de-multiplex[es]” a single line-side signal into multiple signals transmitted to the host).



195. A POSA understood that each of the signals transmitted to the host is a “*serial symbol stream*” as claimed. “Symbol” was a well-known term for a portion of a waveform or a signal state that represents a unit of data. Lugthart-706, 31:39-46. Lugthart-706 notes that “intersymbol interference (ISI)” is “a form of signal distortion in which *a symbol in a digital data stream interferes with subsequent symbols.*” Lugthart-706, 6:36-50. A symbol interfering with “subsequent symbols” transmitted over a data channel confirms that the symbols reside in a *serial symbol stream* are transmitted one after another.

196. Thus, each of FIR filters 27a/27b “*pre-equalize[s] a corresponding serial symbol stream being transmitted to the port transceiver.*”

c. Limitation [8.b]

8.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
-----	---

197. As discussed *supra* §VI.E.1.b (Limitation [1.a]), Lugthart-Das Sharma-Mezer’s pluggable module transceiver (Lugthart-706’s modified transceiver 107a/107b) has multiple registers, each containing a set of initial coefficient values corresponding to a different channel model. *See also supra* §VI.D (the combination uses Mezer’s teaching of different channel models with different initial coefficients and Das Sharma’s teaching to store coefficients in registers). As further discussed *supra* §VI.D (explaining the combination) and

§VI.E.1.b (Limitation [1.a]), Lugthart-Das Sharma-Mezer modifies RX DSP 23 in Lugthart-706's transceiver 107a/107b to have the multiple registers, each storing a different set of coefficient values, and to select from among them the initial coefficient values for FIR filters 27a/27b (transmit filters per Limitation [8.a]) for use in an adaptive pre-equalization training process. Das Sharma, [0078], [0193], FIG. 5; Lugthart-706, 9:38-51, 23:59-64.

198. A POSA would have implemented this functionality in the RX DSP 23 with a controller. Das Sharma teaches that the “coefficient register table” is used by a “coefficient algorithm module” that provides a set of initial coefficients to the transceiver's transmission logic. Das Sharma, [0078], FIG. 5. Das Sharma FIG. 5 (annotated below) shows the coefficient algorithm module (red) and coefficient register table (blue). Das Sharma, [0078] (“coefficient algorithm module 520”). Das Sharma teaches that the coefficient algorithm module can be implemented by a microcontroller that includes the coefficient register table. Das Sharma, [0078], [0193] (Das Sharma's “modules” can each be implemented via a “microcontroller” including “registers”).

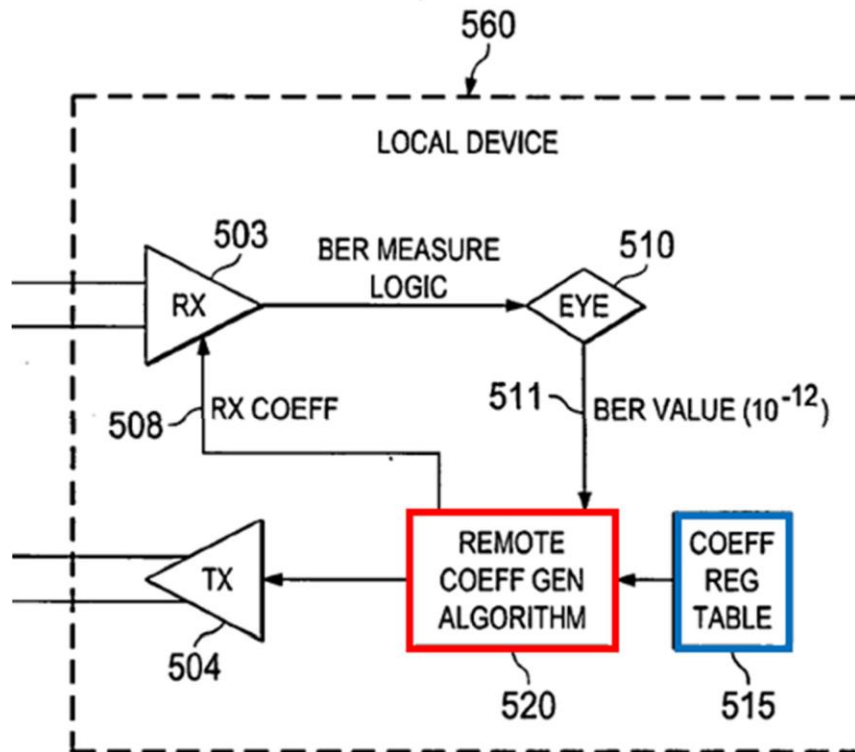


FIG. 5

199. In addition to Das Sharma's teachings, implementing Lugthart-Das Sharma-Mezer's pluggable module transceiver so that the RX DSP 23 functionality that stores initial coefficients in registers and selects an initial set is implemented by a controller including the registers would have been a routine, conventional and obvious way to implement that functionality in RX DSP 23. It was common to implement functionality in a DSP via a controller; and, it was common to include in the controller registers that store data used in implementing the controller's functionality in order to improve performance, given that data can be quickly and efficiently accessed from a local register. Peddle, 5:13-22; Pickett, 2:8-34.

200. Accordingly, an obvious implementation of Lugthart-Das Sharma-Mezer has “*a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.*”

9. Claims 9-10

201. The additional limitations in claims 9 and 10 are identical to those in claims 2 and 3, respectively, and met by Lugthart-Das Sharma-Mezer for the same reasons. *Supra* §§VI.E.2 (claim 2), VI.E.3 (claim 3).

10. Claim 11

202. Limitations [11.PRE] and [11.a] are identical to limitations [8.PRE] and [8.a], respectively, and met by Lugthart-Das Sharma-Mezer for the same reasons. *Supra* §§VI.E.8.a (Limitation [8.PRE]), VI.E.8.b (Limitation [8.a]).

a. Limitation [11.b]

11.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,
------	---

203. Limitation [11.b]’s requirement of “*a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values*” is identical to a requirement in Limitation [8.b] and Lugthart-Das Sharma-

Mezer meets that requirement in [11.b] for the same reasons. *See supra* §VI.E.8.c (Limitation [8.b]).

204. As discussed *supra* §VI.E.4 (claim 4), in one obvious implementation of Lugthart-Das Sharma-Mezer, a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send an instance of a test signal pre-equalized with the set of coefficients stored in each register, and the port transceiver determine which register's coefficients had the best performance characteristic (e.g., produced a signal with the smallest error). The port transceiver is a *port transceiver*. *See supra* §VI.E.8.a (Limitation [8.PRE]). Thus, the port transceiver determining a performance characteristic for each register meets “*each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic*” in [11.b].

b. Limitation [11.c]

11.c	the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.
------	--

205. As discussed *supra* §VI.E.8.c (Limitation [8.b]), Lugthart-Das Sharma-Mezer's modified transceiver 107a/107b has a “controller [that] us[es] one of the registers ... to specify the initial coefficient values for the one or more

transmit filters.” The only additional requirement in limitation [11.c] is that the register is “selected by the port transceiver.”

206. As discussed *supra* §§VI.D (the combination), VI.E.4 (claim 4), and VI.E.10.a (Limitation [11.b]), one obvious implementation of Lugthart-Das Sharma-Mezer chooses the set of initial coefficients by having the pluggable module transceiver send an instance of a test signal pre-equalized with the coefficients in each register, determining at the port (host) transceiver which register’s coefficients had the best performance characteristic and selecting the register with the best-performing characteristics. In Lugthart-Das Sharma-Mezer, the performance characteristic is determined in the port (host) transceiver because that is where the test signal is received and can be best compared against a known error-free version of the test signal. *See supra* §§VI.E.5-6 (claims 5-6).

207. In terms of which side (host/port or cable/pluggable module) of the link selects the register having the coefficients that produced the best performance characteristic, that was a matter of design choice. There were only two options, and a POSA understood that either was a well-known design choice, rendering both obvious. A POSA also understood that the *host/port transceiver* is the desirable design choice to make the selection because the *host/port transceiver* is the one that determines the performance characteristic for each register’s coefficients and can simply select the best performing one and inform the pluggable

module/pluggable module transceiver of that selection. This is analogous to Das Sharma's teaching that, during its training phase, adapted equalization coefficients are determined by the receiving-side transceiver based on the received test signals and the adapted coefficients are then provided to transmitter-side transceiver. Das Sharma, [0078], [0193], FIG. 5.

208. Thus, in the obvious implementation of Lugthart-Das Sharma-Mezer in which the host/*port transceiver* selects the register whose set of coefficients has the best performance characteristics and sends that selection to the cable/pluggable module/transceiver, the *controller* in the pluggable module transceiver "*us[es] one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters*" as required by [11.c].

11. Claims 12-13

209. The additional limitations in claims 12 and 13 are identical to those in claims 5 and 6, respectively, and met by Lugthart-Das Sharma-Mezer for the same reasons. *Supra* §§VI.E.5-6 (claim 5-6).

12. Claim 14

14	The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.
----	---

210. As discussed *supra* §VI.E.7 (claim 7), Lugthart-Das Sharma-Mezer implements an adaptive pre-equalization training process during which *updates* are

generated for the pre-equalization coefficient values of FIR filters 27a/27b meet the claimed *transmit filters*. See *supra* §VI.E.8.b.

211. A conventional and obvious way to implement this adaptive pre-equalization training process in Lugthart-Das Sharma-Mezer was to have the host “*port transceiver generate[] updates*” as required by claim 14. Das Sharma, [0078], [0193], FIG. 5. There were only two options, and a POSA understood that either was a possible design choice and therefore obvious. POSAs also understood that the host/*port transceiver* was a desirable design choice to determine how to adapt the equalization coefficients because the host/*port transceiver* is the one that receives the test signals and can determine how they differ from known good signals and thus how the equalization coefficients should be adapted to reduce error. Additionally, Das Sharma specifically teaches that updated equalization coefficients are determined on the receive side of the channel that receives the training signals and then transferring those updated coefficients to the transmitter side. Das Sharma, [0078], [0193], FIG. 5.

212. Lugthart-Das Sharma-Mezer implemented, as suggested by Das Sharma and as was well-known in the art, to have the host/*port transceiver* determine the updated coefficients during training, meets and renders obvious claim 14.

13. Claim 15

15	The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.
----	---

213. As discussed *supra* §VI.E.7 (claim 7), Lugthart-Das Sharma-Mezer's adaptive pre-equalization training process updates the initial coefficient values and stores the updated coefficients in one of the "multiple registers" in the cable's transceiver. And, as discussed *supra* §VI.E.8.c (Limitation [8.b]), an obvious way to implement Lugthart-Das Sharma-Mezer's adaptive pre-equalization process was via a controller in Lugthart-706's modified RX DSP 23. Das Sharma, [0078], [0193]. Thus, Lugthart-Das Sharma-Mezer meets and renders obvious claim 15.

14. Claim 16

214. Claim 16 is directed to a "*pluggable module transceiver*," rather than a chip-to-module communications link that comprises a pluggable module transceiver as recited in claim 8 (Limitation [16.PRE]), but claim 16 is otherwise identical to claim 8.

215. Limitation [16.PRE] is met because, as discussed *supra* §VI.E.8.a (Limitation [8.PRE]), Lugthart-Das Sharma-Mezer's modified transceiver 107a/107b is a *pluggable module transceiver*. Lugthart-Das Sharma-Mezer meets limitations [16.a]-[16.b] for the same reasons it meets limitations [8.a]-[8.b], respectively. *See supra* §§VI.E.8.b-c(Limitations [8.a]-[8.b]). Thus, Lugthart-Das Sharma-Mezer renders obvious claim 16.

15. Claims 17-19

216. The additional limitations in claims 17, 18, and 19 are substantively identical to those in Limitation [11.b], claim 5, and claim 6, respectively, and are met by Lugthart-Das Sharma-Mezer for the same reasons. *Supra* §§VI.E.10.a (Limitation [11.b] for claim 17), VI.E.5 (claim 5 for claim 18), and VI.E.6 (claim 6 for claim 19).

VII. DECLARATION

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: August 6, 2025



Ayman Fayed, Ph.D.

APPENDIX A: U.S. PATENT NO. 11,032,111 CLAIM LIST

Ref	Limitation
1.PRE	A SerDes communications method that comprises, in a transceiver:
1.a	selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;
1.b	updating the initial pre-equalizer coefficient values during a training phase; and
1.c	using the updated pre-equalizer coefficient values to convey a transmit data stream.
2	The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
3	The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.
4	The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.
5	The method of claim 4, wherein the performance characteristic is an error signal energy.
6	The method of claim 4, wherein the performance characteristic is a bit error rate.
7	The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.

Ref	Limitation
8.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
8.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
8.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
9	The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
10	The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.
11.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
11.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
11.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,
11.c	the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.

Ref	Limitation
12	The communications link of claim 11, wherein the performance characteristic is an error signal energy.
13	The communications link of claim 11, wherein the performance characteristic is a bit error rate.
14	The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.
15	The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.
16.PRE	A pluggable module transceiver including:
16.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and
16.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
17	The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.
18	The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.
19	The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.