

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

PTAB Case No. IPR 2025-01396

Patent No. 7,636,146

**DECLARATION OF RICHARD FLASCK IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF PATENT NO. 7,636,146**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code.

Executed on August 12, 2025 in Sam Ramon, CA

A handwritten signature in blue ink that reads "Richard Flasck". The signature is written in a cursive style with a horizontal line extending from the end of the name.

Richard Flasck

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PETITIONER’S EXHIBIT LIST

Exhibit No.	Document
Ex. 1001	U.S. Pat. No. 7,636,146 (“ 146 patent ”)
Ex. 1002	Declaration and Curriculum Vitae of Richard Flasck (“ Flasck ”)
Ex. 1003	Certified file history of the ’146 patent
Ex. 1004	JP H11282011A & Certified Translation (“ Kitawada ”)
Ex. 1005	JP 2000231115A & Certified Translation (“ Kawaguchi ”)
Ex. 1006	JP H10282516A & Certified Translation (“ Sano ”)
Ex. 1007	JP H03-125334 & Certified Translation (“ Minami ”)
Ex. 1008	<i>Electronic Display Devices</i> , edited by Shoichi Matsumoto, 1990, Chapter 2, Liquid Crystal Displays (LCDs) and Declaration (“ Matsumoto ”)
Ex. 1009	U.S. Publication 2002-0018169A1 (“ Kato ”)
Ex. 1010	JP 2003216064 & Certified Translation (“ Nakanishi ”)
Ex. 1011	U.S. Publication 2003-0001808A1 (“ Sakuma ”)
Ex. 1012	U.S. Pat. No. 5,592,199 (“ Kawaguchi ’199 ”)
Ex. 1013	JP 2000047643A & Certified Translation (“ Shii ”)
Ex. 1014	Wei-Fun Hou, TaiYan Kam, Adam Hsieh, JianCheng Chen, and Shyh-Ming Chang “ <i>Mismatch analysis of TAB-on-glass connection with ACF,</i> ” Proc. SPIE 4079, Display Technologies III and Declaration (“ Mismatch Analysis Report ”)
Ex. 1015	U.S. Publication 2003-0095227 (“ Kohtaka ”)
Ex. 1016	U.S. Pat. No. 3,824,003 (“ Koda ”)
Ex. 1017	<i>Tape-automated Bonding: Materials and Technologies</i> and Declaration (“ Kang ”)

Exhibit No.	Document
Ex. 1018	U.S. Publication 2003-0142905 (“ Yonekubo ”)
Ex. 1019	U.S. Publication 2003-0090500 (“ Yamazaki ”)
Ex. 1020	U.S. Publication 2003-0043105 (“ Hirakata ”)
Ex. 1021	U.S. Pat. No. 7,002,545 (“ Osame ”)
Ex. 1022	“ <i>Liquid Crystal Display Technology</i> ,” with partial translation provided by the patent applicant, cited in September 17, 2008 Response to Office Action.
Ex. 1023	U.S. Pat. No. 5,155,065 (“ Schweiss ”)

CHALLENGED CLAIM LISTING (CLAIMS 1-23)

Claim	Limitation No.	Limitation
1	[1pre]	An electro-optical panel comprising:
	[1a]	a plurality of data lines
	[1b]	a plurality of scanning lines intersecting the plurality of data lines
	[1c]	a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines
	[1d]	a clock signal input terminal supplied with a scanning line clock signal
	[1e]	an image signal input terminal supplied with an image signal
	[1f]	a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals
	[1g]	a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and
	[1h]	a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,
	[1i]	wherein the clock signal input terminal has a larger area than the image signal input terminal, and
	[1j]	wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a

Claim	Limitation No.	Limitation
		plurality of the second image signal input terminals are included
	[1k]	the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and
	[1l]	a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.
2		An electro-optical panel according to claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.
3		An electro-optical panel according to claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.
4		An electro-optical panel according to claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.
5		An electro-optical apparatus comprising: an electro-optical panel set forth in claim 1; power source means for supplying the power source; and signal generation means for supplying the input signals.
6		An electro-optical apparatus comprising: an electro-optical panel set forth in claim 5; an external substrate which includes power source means for supplying the power source and signal generation means for supplying

Claim	Limitation No.	Limitation
		the input signals; and a flexible substrate which connects the external substrate and the electro-optical panel, wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.
	7	An electro-optical apparatus according to claim 6, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.
	8	An electronic system comprising the electro-optical apparatus set forth in claim 1.
	9	The electro-optical panel according to claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.
10	[10pre]	An electro-optical panel comprising:
	[10a]	a first substrate
	[10b]	data lines
	[10c]	scanning lines intersecting the data lines
	[10d]	pixels disposed corresponding to intersections between the data lines and the scanning lines
	[10e]	a clock-signal input terminal supplied with a clock signal and connected to a mounting member through anisotropic conductive film

Claim	Limitation No.	Limitation
	[10f]	image-signal input terminals supplied with image signals and connected to the mounting member through anisotropic conductive film,
	[10g]	the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate,
	[10h]	the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines
	[10i]	and a scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal
	[10j]	wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film.
11		The electro-optical panel according to claim 10, the clock-signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.
12		The electro-optical panel according to claim 10 the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal.
13		The electro-optical panel according to claim 10, the external data line circuit being formed on a second substrate other than the first substrate.

Claim	Limitation No.	Limitation
	14	The electro-optical panel according to claim 10, the clock-signal input terminal being disposed further out on the first substrate relative to a central part of an outer edge of the first substrate than the image signal input terminal.
	15	The electro-optical panel according to claim 10, the pixels arranged on the first substrate.
	16	The electro-optical panel according to claim 10, the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.
	17	The electro-optical panel according to claim 10, wherein each of the first wiring and the second wiring comprise at least one wire.
	18	The electro-optical panel according to claim 10, wherein contact area between the clock signal input terminal and the first wiring is greater than contact area between the at least one of the image signal input terminals and the second wiring.
	19	The electro-optical panel according to claim 10, wherein the mounting member is distinct from and connected to the first substrate.
	20	The electro-optical panel according to claim 19, wherein the mounting member is electrically and mechanically connected to a terminal group of the first substrate that comprises the clock signal input terminal and the image signal input terminals.
	21	The electro-optical panel according to claim 10, wherein the clock signal input terminal and the at least one of the image signal input terminals are connected between the substrate and the mounting member.

Claim	Limitation No.	Limitation
22		The electro-optical panel according to claim 10, wherein the mounting member is implemented as a flexible cable that is connected to the substrate over the clock signal input terminal and over the image signal input terminals.
23	[23pre]	An electro-optical panel comprising:
	[23a]	a substrate
	[23b]	data lines
	[23c]	scanning lines intersecting the data lines
	[23d]	pixels disposed corresponding to intersections between the data lines and the scanning lines
	[23e]	a clock signal input terminal supplied with a clock signal
	[23f]	an image signal input terminal supplied with an image signal
	[23g]	a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals
	[23h]	wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate
	[23i]	a mounting member that is distinct from and connected to the substrate, the mounting member comprising:
	[23j]	a first wiring that is connected to the clock signal input terminal;
	[23k]	a second wiring that is connected to the image signal input terminal;

Claim	Limitation No.	Limitation
	[231]	wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member

I, Richard Flasck, declare as follows:

1. I have been retained by Holland & Knight LLP on behalf of BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”) to provide certain opinions regarding the patentability of claims 1-23 of U.S. Patent No. 7,636,146 (“the ’146 patent”).

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. BOE is paying \$690 per hour for my services in this matter. I am not receiving any other form of compensation. I have no interest in the outcome of this proceeding, and my compensation is not depending on the content of my opinions or the outcome of this proceeding.

I. INTRODUCTION AND QUALIFICATIONS

4. My technical background and experience for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my curriculum vitae, which is attached as Appendix 1.

3. I received a Bachelor of Science degree in Physics from the University of Michigan, Ann Arbor, in 1970. I thereafter received a Master of Science degree in Physics from Oakland University in Rochester, Michigan, in 1976. I am the founder and owner of RAF Electronics, where I developed and patented Liquid Crystal on Silicon (LCOS) microdisplay projection technology

using active matrix transistor arrays as well as developed proprietary LED-based Solid State Lighting (SSL) products.

4. After receiving my bachelor's degree, I was employed as a scientist and a manager by Energy Conversion Devices, Inc., from 1970 through 1982. My work at Energy Conversion Devices concerned the development of electroluminescent displays, thin film photovoltaics, ablative imaging films, non-volatile memory, multi-chip modules, thin film transistors, and superconducting materials. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active matrix liquid crystal displays (AMLCDs). My work at Alphasil included active matrix liquid crystal display (AMLCD) design and production, thin film transistor array substrate process and circuit design, data driver and gate driver design, scalers, video circuits, gamma correction circuits, backlighting, and inverter design. I established the first amorphous silicon AMLCD pilot production line in the world. At Alphasil I also designed and incorporated touch panel screens into active matrix display devices. I worked at Alphasil from 1982 through 1989.

5. After leaving Alphasil, I founded RAF Electronics, described above. I have served as CEO of RAF Electronics since that time. At RAF I developed HDTV projection technology including transistor array substrates for liquid crystal

on silicon (LCOS) devices and the associated optical systems. My activities at RAF have included developments in lighting systems using both traditional LED and OLED (Organic Light Emitting Diode) technologies. In 2016 I was granted US Patent 9,328,898 which includes OLED and LED technology and lighting systems. In 2019 RAF received a CalSEED grant from the California Energy Commission to develop ultra-efficient lighting products and explore establishing a Central Valley manufacturing facility.

6. In 1997, I took the position of President and COO at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects Agency (DARPA) contract, and for implementing MEM fluidic self-assembly (FSA) technology for flat panel displays. I left that position in 1999.

7. In 2002, I co-founded and served as COO of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for HDTV projectors, such as polarization optics, condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED and thin film transistor arrays and devices. I left Diablo Optics in 2007.

8. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My

inventions concern technologies including LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, wafer based active matrices, and various transistor array substrates.

9. I have authored or co-authored twenty-five articles or conference presentations, including numerous papers and presentations concerning lighting and display technologies. My curriculum vitae lists these articles, conference presentations, and patents.

10. I am also a member of several professional organizations, including Optica, SPIE, AES, SID, and the IEEE.

11. In summary, I have about 55 years of experience in the field of high-tech product development including active matrix liquid crystal displays, transistor array substrates, touch panels, and OLED and LED devices.

12. I have been an expert witness in over 60 patent cases, have written scores of expert reports and declarations, and have testified in district court or before the International Trade Commission (ITC) eight times.

13. About half of the 60+ cases I have worked on have involved active matrix liquid crystal displays.

II. LEGAL PRINCIPLES

14. I am not a lawyer and I do not provide any legal opinions in this Declaration. Although I am not a lawyer, I have been advised certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and patentability / validity of patent claims.

15. In forming my analysis, opinions and conclusions expressed in this Declaration, I have applied the legal principles set forth below which were provided to me by counsel for BOE.

A. Independent and Dependent Claims

16. I understand that there are two types of patent claims: “independent” and “dependent claims.” I understand that independent claims include only the aspects stated in the independent claim. I further understand that a claim in dependent form shall contain a reference to a claim previously set forth (which previously set forth claim can be an independent or a dependent claim) and then specify a further limitation of the subject matter claimed. I understand that a claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

B. Prior Art

17. I understand that the Patent Act defines various categories of prior art.

18. For example, I understand that pre-AIA 35 U.S.C. §102(b) states that a “person shall be entitled to a patent unless . . . the invention was patented or

described in a printed publication in this or a foreign country ... more than one year prior to the date of the application for patent in the United States.” I also understand that pre-AIA 35 U.S.C. §119(a) states that “no patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country.” I understand that the actual filing date of the United States application leading to the ’146 patent (Application Serial No. 10/914,044) was August 6, 2004.

19. As another category of prior art, I understand that pre-AIA 35 U.S.C. §102(a) states that a “person shall be entitled to a patent unless . . . the invention was . . . patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.”

20. I further understand that pre-AIA 35 U.S.C. §102(e)(1) states that a “person shall be entitled to a patent unless . . . the invention was described in . . . an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent.”

21. For purposes of this Declaration, I have been instructed to assume that the invention date of all claims of the ’146 patent was August 8, 2003 (based on the date of an alleged “priority” application that the original owner of the ’146 patent filed in Japan).

22. I also understand that there can be applicant admitted prior art (“AAPA”) based on statements in the specification (*e.g.*, describing technology as “known”) or based on the applicant’s similar statements made during prosecution. I understand that the United States Court of Appeals for the Federal Circuit (“Federal Circuit”) has held that such admissions are binding on the applicant and patentee for determinations of anticipation and obviousness. I also understand that the Federal Circuit has held that AAPA can be important evidence of general background knowledge, and general knowledge can be used to supply a missing claim limitation. I further understand that the Federal Circuit has held that permissible uses for general background knowledge in an IPR include, for example, furnishing a motivation to combine prior art references, or supplying a missing claim limitation.

C. Anticipation and Obviousness

23. I understand that a claim is not patentable if it is anticipated or obvious. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in a single prior art reference. In this Declaration I am not setting forth any opinions that any claims of the ’146 patent are unpatentable due to anticipation.

24. I further understand that obviousness of a claim requires that the claim be obvious from the perspective of a person of ordinary skill in the art (“POSITA”)

at the time the invention of the challenged patent claim was made. Again, I have been instructed to assume that the invention date of all claims of the '146 patent was August 8, 2003.

25. I understand that to prove that prior art or a combination of prior art renders a patent claim obvious, it is necessary to: identify the particular reference that, alone or in combination with others, renders the claim obvious; specifically identify which elements of the claim are disclosed by one or more of the asserted references; and explain why a POSITA would have combined the teachings of the references, and how they would have done so, to create the inventions in the challenged patent claim.

26. I understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

- “obvious to try”—choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and
- some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second prior art reference can be explicit or implicit, and may provide further evidence of obviousness.

28. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant. I am not currently aware of any such evidence for the claims of the '146 patent and reserve my right to review and respond to such evidence if any is presented.

D. Claim Construction

29. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary

meaning of those terms. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have used the date of August 8, 2003 for reasons explained above.

III. BASIS FOR MY OPINIONS

30. In forming my opinions, I have considered the '146 patent (including the specification's written description of the invention, all of the figures, and all of claims) along with the prosecution history. I understand that the prosecution history is the written record with the U.S. Patent office. I have also considered the exhibits to BOE's Petition, as well as any additional materials identified in this Declaration, plus my own experience and expertise as a skilled artisan in the relevant art at the time of the invention.

IV. SUMMARY OF MY OPINIONS

31. I have been asked to consider whether claims 1-23 of the '146 patent are rendered obvious by certain prior art references. Based on the analysis set forth herein, including my experience and knowledge in the field, my understanding of the claims, the prior art, the applicable law, and the level of ordinary skill in art in the relevant timeframe, it is my opinion that claims 1-23 are obvious for the reasons set forth herein.

V. LEVEL OF ORDINARY SKILL IN THE ART AT THE TIME OF THE ALLEGED INVENTION

32. The relevant time for assessing the level of skill of the hypothetical person of ordinary skill in the art (“POSITA”) is the August 8, 2003 filing date of the earliest alleged priority Japanese application. To assess the level of ordinary skill in the art at that time, I understand that one should consider factors such as the educational level of the inventor; the type of problems encountered in the art; prior art solutions to those problems; the rapidity with which innovations are made; the sophistication of the technology; and the educational level of active workers in the field.

33. Considering these factors, it is my opinion that, as of August 8, 2003, a POSITA had at least: i) a B.S. in electrical engineering, physics, or a related subject and two plus years of experience working in the field of LCD displays; ii) an M.S. degree in the aforementioned subjects, and at least 1 year of experience in the design/development of LCD displays; or iii) a Ph.D. in the aforementioned subjects, and at least some experience in the area of LCD displays. Additional education may substitute for professional experience, and significant work experience may substitute for formal education.

34. I base the foregoing in part on my own experience discussed above in §I (including my work at Alphasil in the 1980s, my work at RAF before and at the time of the alleged invention, my work at Alien Technology Corporation in the late

1990's, and my work at Diablo Optics Inc.. which I joined shortly before the alleged invention date of the '146 patent). During the relevant timeframe, I interacted with many other engineers working in the art.

35. The claimed technology of the '146 patent was well-known and conventional long before the alleged invention date. For example, claim 1 of Pat. No., 3,824,003 to Koda (Ex. 1016), which issued in 1974, recites elements of a typical active-matrix liquid crystal display device ("AMLCD"). And indeed, as described further below, the original owner of the '146 patent admitted in the first column of the specification and during prosecution that virtually all elements of the claimed inventions were "known" and/or "well-known." *See, e.g.,* '146 patent, Ex. 1001, 1:23-62 ("Here, a known electro-optical apparatus has a structure, for example, as described below . . .").

36. According to the '146 patent, its alleged innovations include (1) increasing the area of input terminals for signals have a "higher frequency component," *e.g.*, clock signal input terminals (Ex. 1001, 2:24-3:9); (2) disposing input terminals having a wider area nearer the outer portions of the terminal block and near to the outside of an LCD panel's substrate, *i.e.*, at the location where heat and pressure are applied when ACF is used to connect input terminals to wiring (Ex. 1001 at 3:10-22); and (3) increasing the area of power source terminals (such that they are "not smaller" than clock-signal input terminals) to decrease their

resistance in order to “supply a predetermined voltage” (Ex. 1001 at 3:23-42).

However, as shown below, all of these alleged inventions were disclosed by prior art more than one year before the alleged invention date of the ’146 patent. And these alleged inventions are relatively simple in that they relate merely to the sizing and placement of input terminals, not to any truly groundbreaking technology.

37. Before the time of the alleged invention, a POSITA would have been well versed in the technology of AMLCD devices, including the various design choices available to them, and including the arrangement and sizing of input terminals in such devices as recited in the challenged claims.

VI. ACTIVE MATRIX DISPLAY TECHNOLOGY OVERVIEW

A. A Brief History

38. The Cathode Ray Tube (CRT) was the dominant display device from the 1940’s through the end of the last century. The CRT relies on raster scanning a focused electron beam inside a large vacuum tube, allowing the beam to impinge on a phosphor coating on the inner surface of the tube. The phosphor emits light in proportion to the electron beam intensity. Pictures are thus drawn on the inner surface of the CRT with an electron beam of modulated intensity.

39. During the 1970’s interest began to arise to find a “flat panel” technology to supplant the large, heavy CRT’s. Many technologies were pursued, including electroluminescent, electro-chromic, electrophoretic, vacuum fluorescent, plasma, liquid crystal, and others. By 1990, liquid crystal displays

(LCD) began emerging as the winning technology to supplant the CRT in most commercial and consumer applications. Organic Light Emitting Diode (OLED) displays are now common in smart phones. Today, both LCD and OLED displays are implemented with active matrix technology where one or more thin film transistors (TFTs) are located at each pixel.

40. The first LCD's were low segment count, direct driven displays, such as watch and calculator displays. Each segment had a common upper and a patterned lower electrode. These electrodes were continuously actively driven. Each segment required a separate dedicated conductor running to the segment. While this was feasible for low information content displays, passive and active matrix LCDs were required for higher pixel count display devices. Active matrix generally has brightness, contrast, response time, and viewing angle advantages over passive matrix.

41. Although there are exceptions, most LCD's comprise two outer polarizer sheets, with a glass plate adjacent to each polarizer. The inner surfaces of the glass plates have transparent indium-tin-oxide (ITO) conductive electrodes. The small gap (usually 1 to 5 micrometers) between the ITO electrodes is filled with liquid crystal material. An epoxy rim seal keeps the liquid crystal material in place.

42. There are several types of liquid crystal material, and generally several modes in which each type of liquid crystal material can be used. The types of liquid crystal materials include twisted nematic (TN), Electrically Controllable Birefringent (ECB), cholesteric, smectic, and ferro-electric, among others. Various modes include 90° twist, super (270°) twist, Polymer Dispersed (PDLC), vertically aligned (VA), In Plane Switching (IPS), Hybrid Aligned (HAN), bi-stable, normally white and normally black. The industry has migrated from direct driven segmented watch and calculator displays to active matrix thin film transistor (TFT) LCD's. Consumer demand has continually grown.

B. Active Matrix Liquid Crystal Displays (AMLCDs)

43. Most LCD monitors and televisions today use AMLCDs with Thin Film Transistors (TFTs). They use TN with a 90° twist, or a vertically aligned (VA) ECB with negative dielectric constant anisotropy operating in the normally black mode, or In Plane Switching (IPS) mode. Common to each of these modes is the fact that the light transmission at each pixel (picture element) is controlled by the voltage across the pixel electrodes. In the early 2000's, most liquid crystal displays used the TN mode.

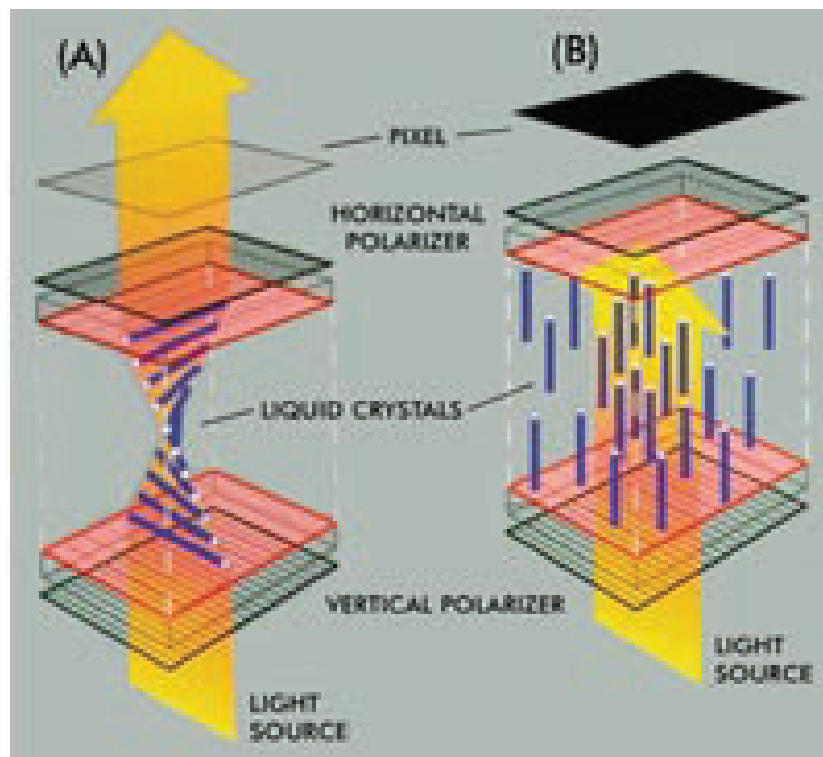
44. "Color TFT LCDs are turning up everywhere these days. The color TFT display, a light, slender display, with a beautiful image that does not tire the eyes even when viewed for hours at a time, is finding its way into many products,

even in demanding environments, like the dashboard of a car. Because the color TFT display is an LCD (liquid crystal display) panel incorporating thin film transistors, it can reproduce a wider range of colors than can competing technologies. The color TFT shows extremely uniform brightness, with no color degradation or distortion, even in the corners of the screen.” Pg 1, 1996, *Color TFT Liquid Crystal Displays*, Yamazaki, ASIN : B0728FCK38. “The momentum the LCD industry has gained is difficult to supplant by alternative flat panel technologies. Even if, on paper, they may have advantages over LCDs.” Pg7, 2005, *Active Matrix Liquid Crystal Displays*, Willem den Boer, ISBN- 13:978-0-7506-7813-1. The quotes above testify to the fact that by the early 2000’s POSITAS were well aware of the basic structure and operating principles of the ubiquitous Active Matrix Liquid Crystal Display (AMLCD). A summary of that technology follows.

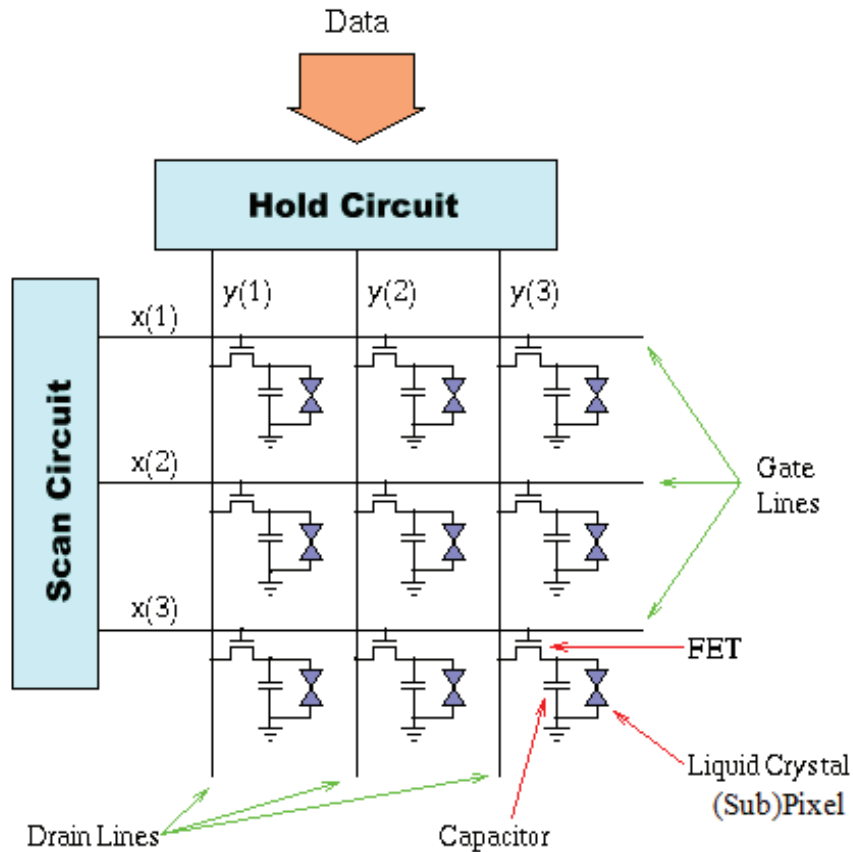
45. Liquid Crystal Materials (LCMs) are unusual liquids which exhibit stable states with long range order, wherein the stable state can be determined by the strength of the imposed electric field. These stable states can exhibit differing optical properties. These differing optical properties are exploited to vary the transmission of small segments (pixels or picture elements) of the display by application of an electric field.

46. Typical AMLCD comprises an array of pixels. Each pixel can comprise color sub-pixels, usually red, green and blue. At each sub-pixel is a sample and hold circuit, addressed by a thin film transistor, wherein the voltage across the LCM is held by a storage capacitor.

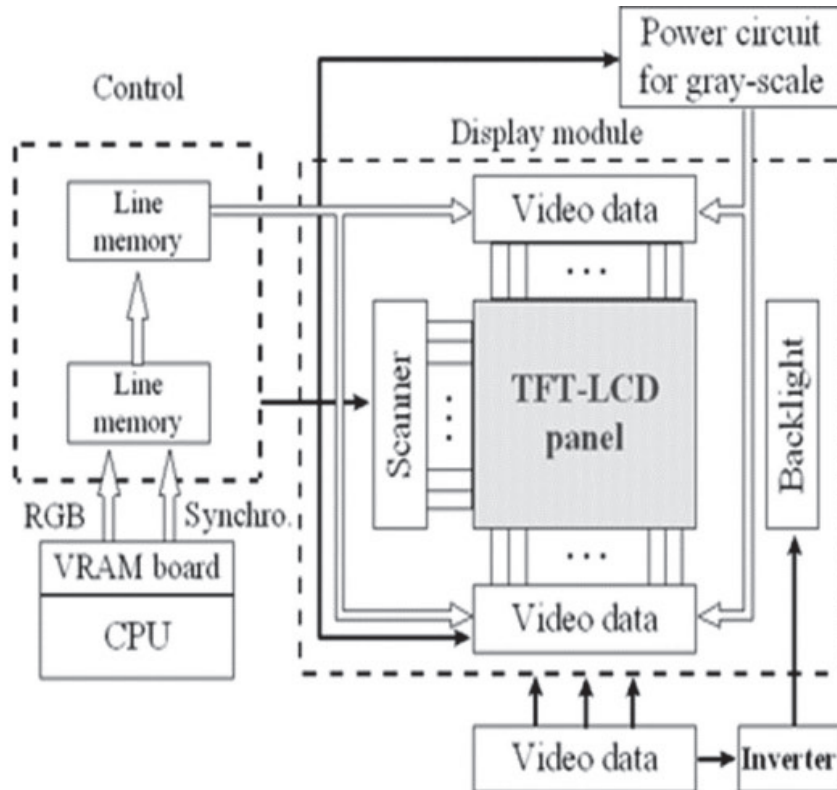
47. Each sub-pixel acts like a variable shutter, allowing a level of light transmission based on the voltage across the LCM, as shown below. In the figure below, on the left there is no voltage and all light is allowed to pass. On the right, full voltage is applied, and no light is allowed to pass. At intermediate voltages, an intermediate level of light is allowed to pass.



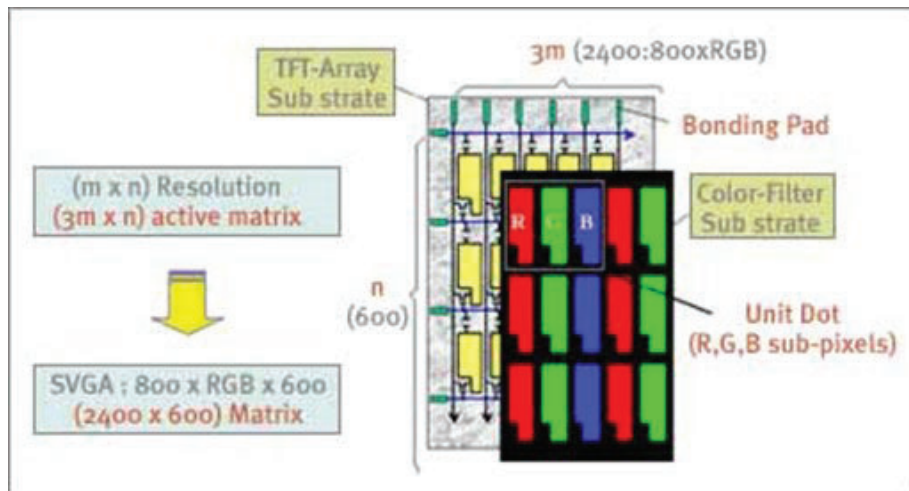
48. Below is a typical electrical diagram of the TFT active matrix showing the drive transistor, the storage capacitor and the liquid crystal element at each sub-pixel:



49. A block diagram of an AMLCD is shown below:

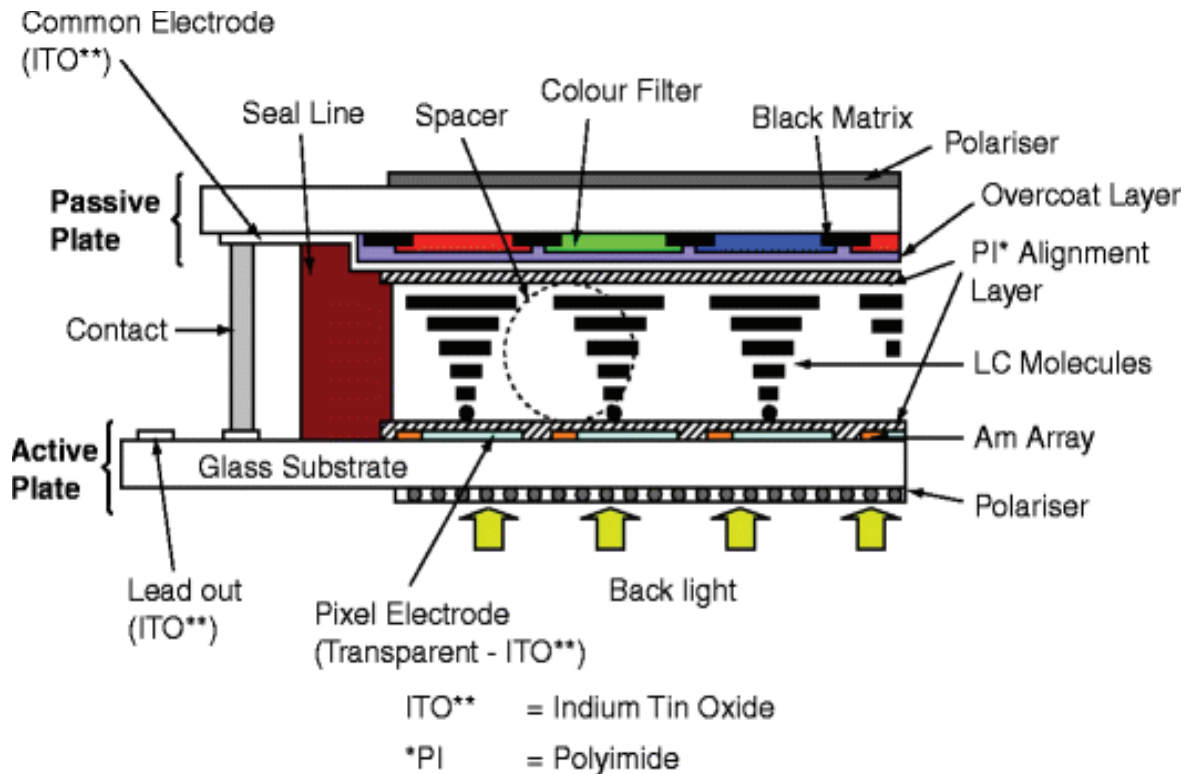


50. Each pixel is usually organized as three sub-pixels: one red, one green and one blue. The colors is determined by the color filter patch over each sub-pixel, as shown below:



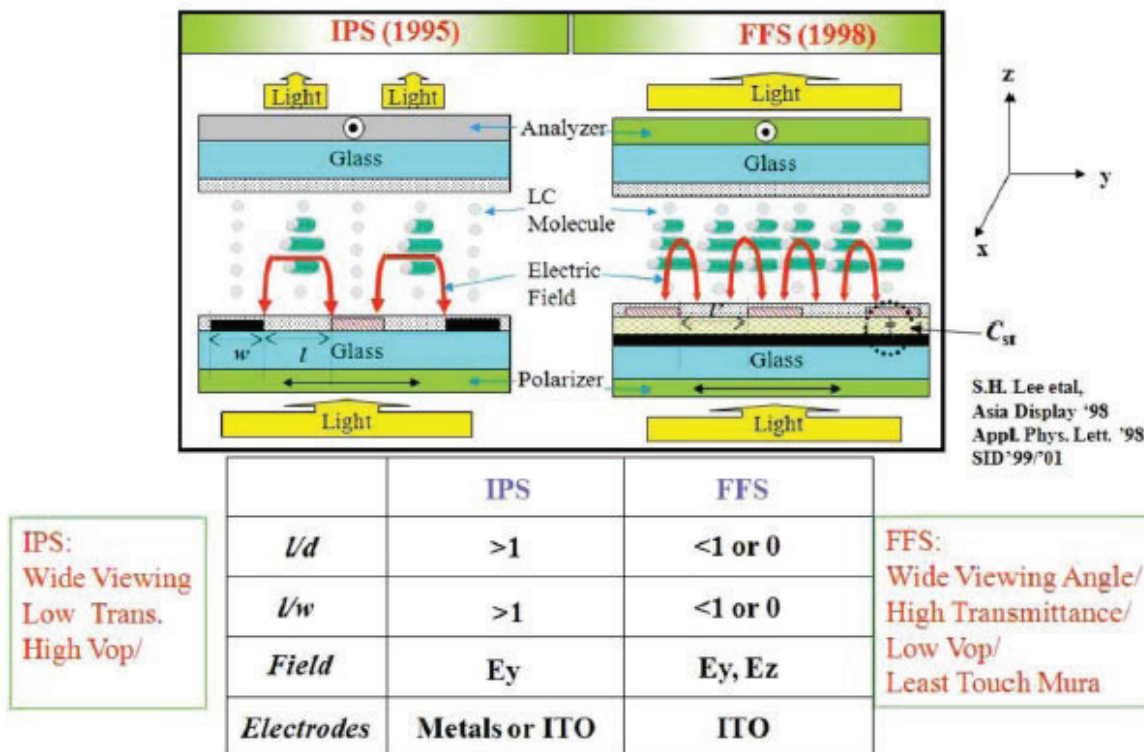
The specific color perceived by the human eye (including white) is determined by the proportions of red, green and blue light transmitted by each pixel.

51. As previously mentioned, each sub-pixel circuit comprises a Thin Film Transistor (TFT), a capacitor, and the LCM between the upper and lower pixel electrode. Below is a typical Twisted Nematic (TN) cross section of a pixel comprising three color sub-pixels:



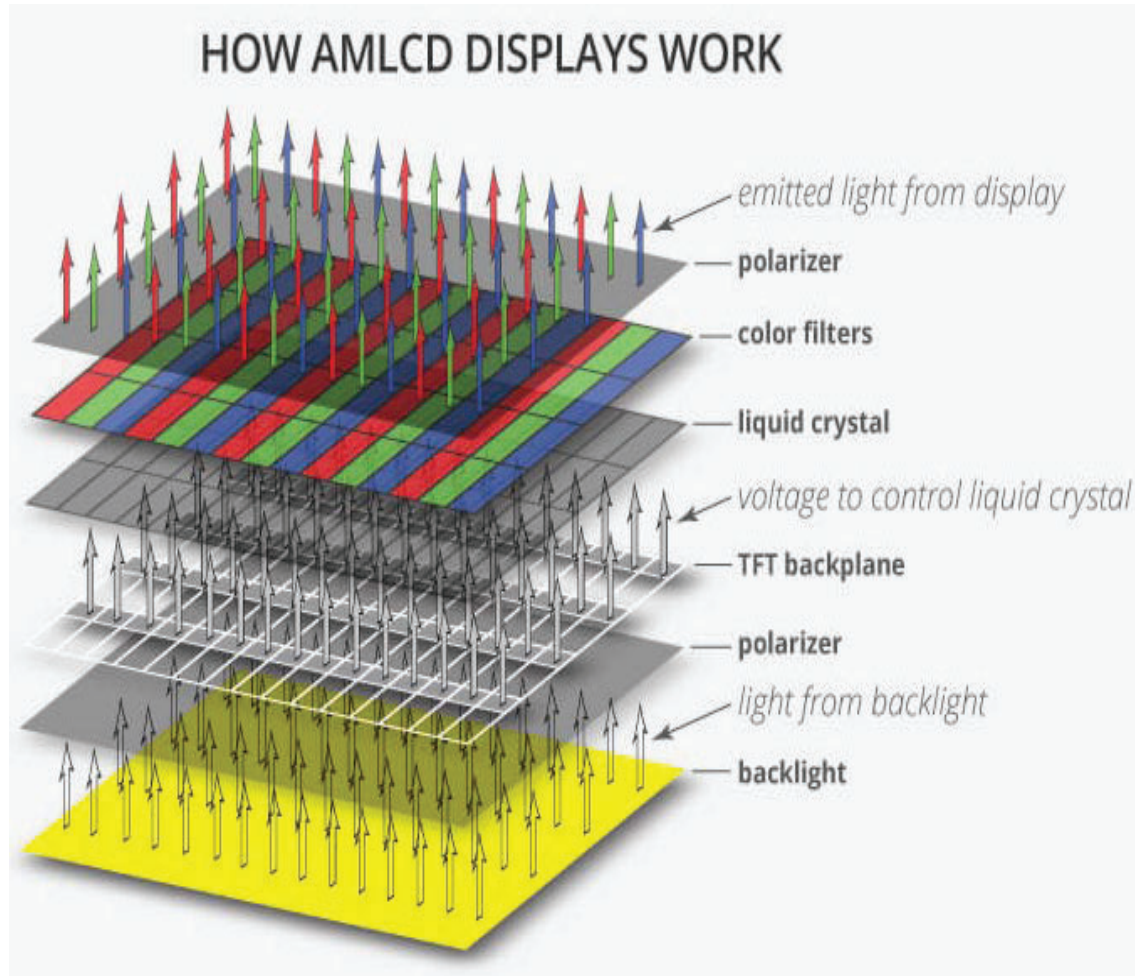
Note the ITO common electrode on the bottom of the upper substrate. The common electrode is usually kept at a constant potential. With in-cell touch panels, however, the common electrode can be divided into a multiple separate domains, and each domain is held at the constant potential, until a touch signal is sent to determine if the individual common electrode domain is touched. This interrogation time is usually brief compared to the frame time and may be within a blanking period.

52. Shown below is a second basic type of LCD configuration called In-Plane Switching (IPS) and its close cousin Fringe Field Switching (FFS):



In these modes, the pixel electrode and the common electrode are on the same substrate. The pixel electrodes are in pink and the common electrode(s) is in black. As with the TN mode, in-cell touch panels are implemented with the common electrode divided into a multiple domains, and each domain is held at the constant potential, until a touch signal is sent to determine if the individual common electrode domain is touched. This interrogation time is usually brief compared to the frame time and may be within a blanking period.

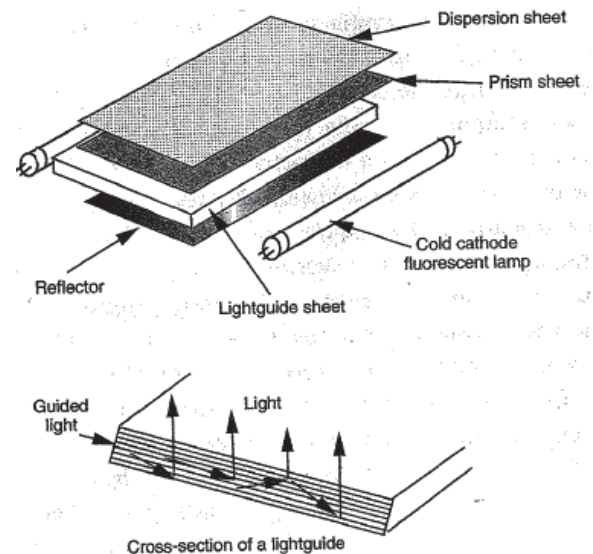
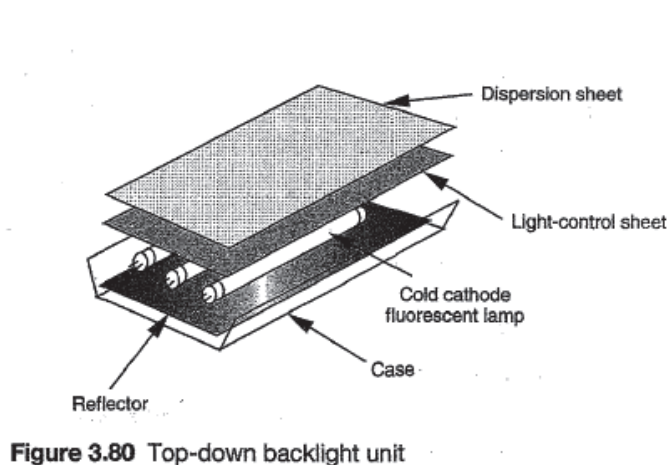
53. The physical structure of the typical AMLCD module is shown below:



54. Unlike active matrix OLED displays, the AMLCD is a non-emissive technology where the pixels control the amount of light passing through, rather than generating light. Therefore, virtually all AMLCDs comprise a backlight unit (BLU) as indicated in the image above. Active matrix OLED displays have pixels that emit light and have more complex circuitry (multiple transistors) at each pixel, but need no backlight. In-cell touch panels can also be implemented on OLED displays by dividing the common electrode as with AMLCDs.

C. The Backlight Unit (BLU)

55. Each AMLCD module has a BLU located below the AMLCD panel. The BLU provides the light that is modulated by each pixel. There are two generic types of BLUs: direct (or full array) BLUs and edge-lit BLUs. The two types are shown below from 1996 Yamazaki Pg 272-3, 1996, *Color TFT Liquid Crystal Displays* (ASIN : B0728FCK38):



56. The configuration Yamazaki refers to as “Top-down” is known as direct or full array in today’s terminology. Full array BLUs have the light source(s) directly underneath the LCD panel with a dispersion (diffuser) sheet between the light sources and the LCD panel. The edge-lit BLUs have the light

sources on one or more sides of a light guide or cavity with the light being directed into the light guide and then exiting toward the LCD panel above the BLU.

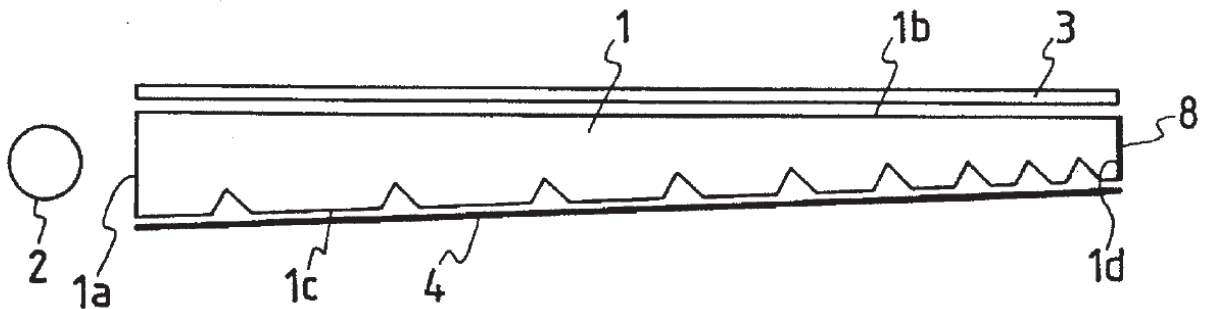
57. In both configurations, there is a diffuser plate between the light sources and the LCD panel. “Most AMLCDs operate in the transmissive mode. *They can be considered electronically controlled transparencies on a light box – the backlight.*” Pg. 105, 2005, *Active Matrix Liquid Crystal Displays*, Willem den Boer, ISBN- 13:978-0-7506-7813-1 (Emphasis added). Also, in both configurations there is a case holding the BLU components, and a reflector on the bottom of the case.

58. Further, on pages 274 and 275 Yamazaki states “Because they have a direct bearing on the performance of the display unit, backlight units are subject to stringent performance requirements as indicated below:.....2) Uniform brightness A minimum uniformity (minimum brightness divided by maximum brightness) of 0.8 is required.”

59. Thus, brightness uniformity of the BLU was a well-known, important performance parameter of BLUs, and substantial work throughout the years went into addressing this issue. For example: “concave portions are arranged to have specific shapes to obtain a bright surface light source with a uniform brightness. A light diffusing material is fulfilled within the concave portions of the light conducting member so that a more uniform brightness can be obtained in an easy

manner.” U.S. Pat. No. 5575549 to Ishikawa (filed in 1994, issued in 1996), at Abstract. And Ishikawa’s Figure 4 shows a linear (cold fluorescent lamp (“CCFL”)) light source 2 and a diffuser 3:

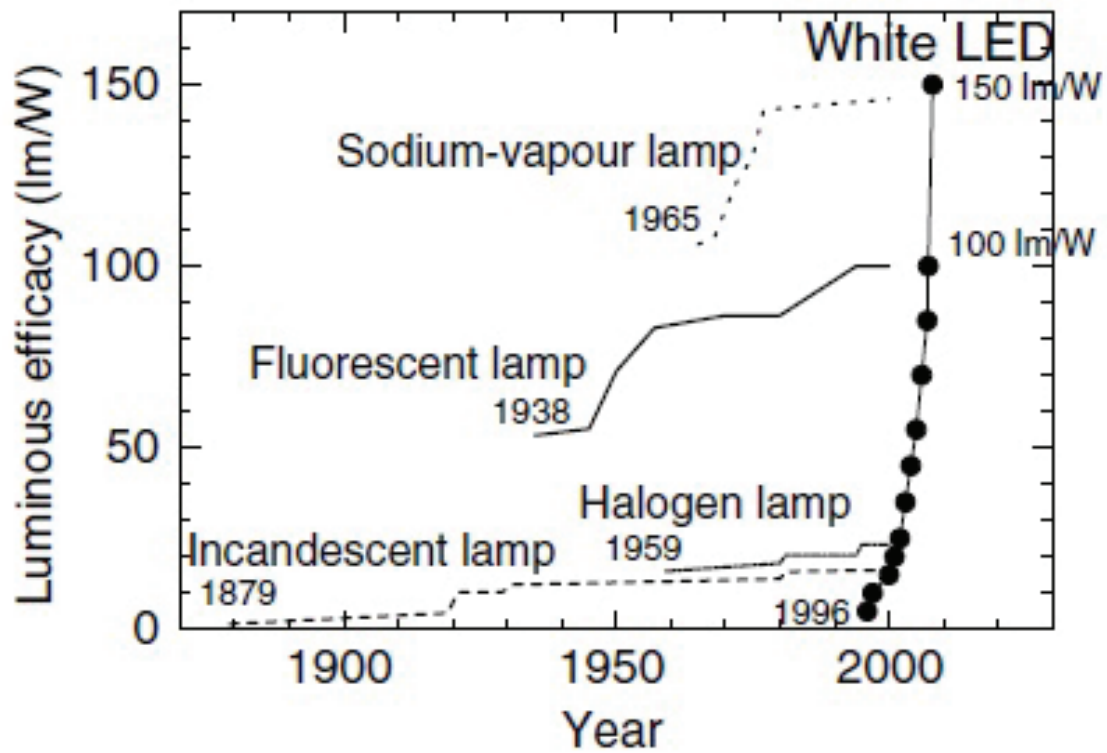
FIG. 4



Further uniformity was a known issue (identified in Saizo, Hansen, and Pelka).

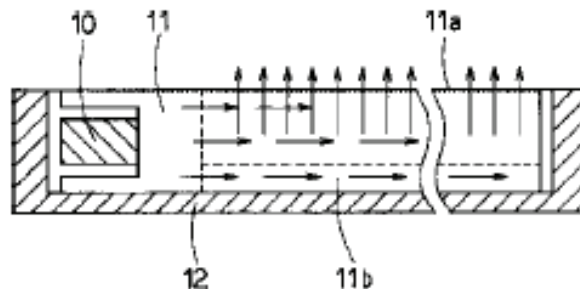
60. In the mid 1990’s, LED efficacy and brightness started an exponential rise as phosphor coated GaN blue LED began reaching the market, as reflected in the chart below:

<https://phys.org/news/2010-08-white-super-high-luminous-efficacy.html>



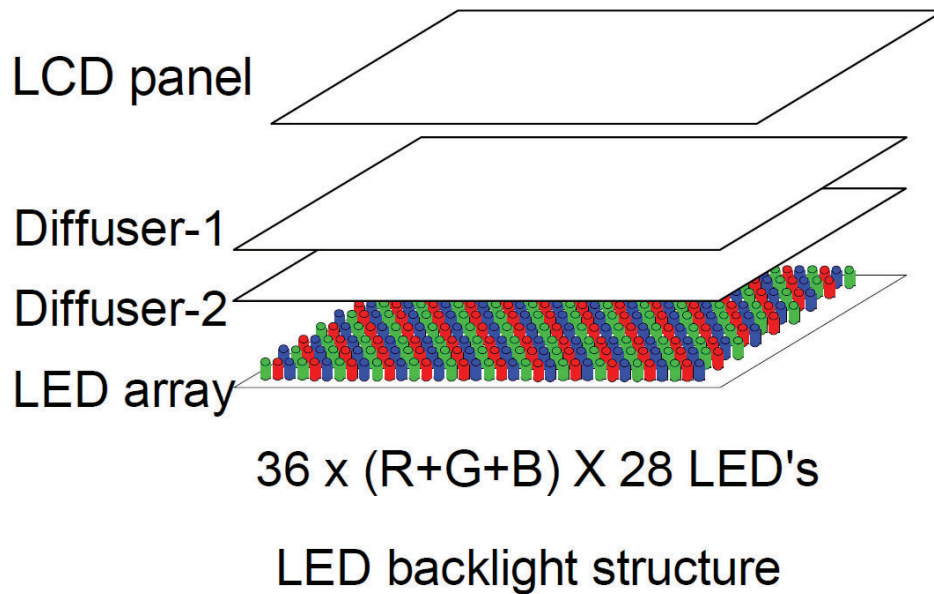
61. Starting as early as 1993 JPH06-230378 by Kisoo disclosed edge-lit BLUs having a diffuser plate, reflective bottom, a casing and using LEDs as light sources. See Kisoo Fig 5 below:

【图5】



62. The CCFL edge-lit BLU configuration dominated the marketplace throughout the 1990's. However, in the early 2000's there was a conflation of two powerful forces. First, high power, high efficiency LED technology took off, including both color and white LEDs. Second, consumers were becoming dissatisfied with the contrast and dynamic range of AMLCD compared to the much more expensive (low volume) plasma displays. Dynamic contrast ratio technology for AMLCD was developed to selectively dim portions of the screen when those portions had low brightness content. However, this dimming technology was not usable with edge-lit or CCFL BLU configurations. It could only be implemented with direct, full array BLUs using LEDs instead of CCFLs for light sources. This started the paradigm shift toward LED full array BLUs that is the industry standard today. One of the early transitions from CCFL edge-lit BLUs to LED full array BLUs is shown in Yamada from 2000:

Figure 4

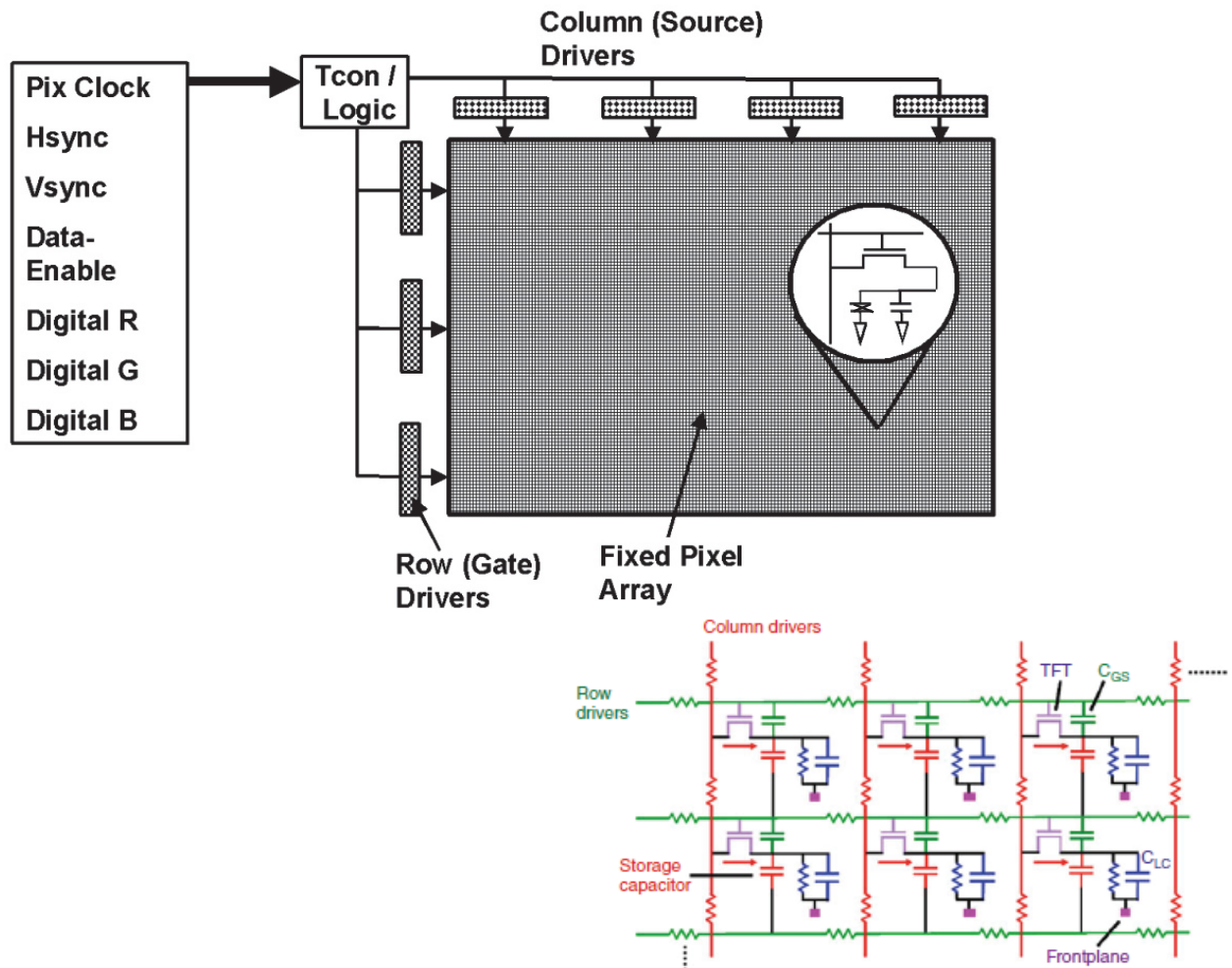


63. Thus, around 2000, full array LED BLUs were well known. These BLUs had Brightness Enhancement Films (BEFs), diffusers, and bottom reflectors.

D. AMLCD Operation, Timing, and Signal Integrity Requirements

64. An Active Matrix Liquid Crystal Display (AMLCD) is a display device comprising an array of pixels, row lines, row line drivers, column lines, column drivers, and a timing controller. A pixel is located at the intersection of the row lines and the column lines. There is a Thin Film Transistor (TFT), a storage capacitor (Cst), and a pixel electrode at every pixel. There is a common electrode shared by all of the pixels. Each pixel acts as variable microscopic shutter where

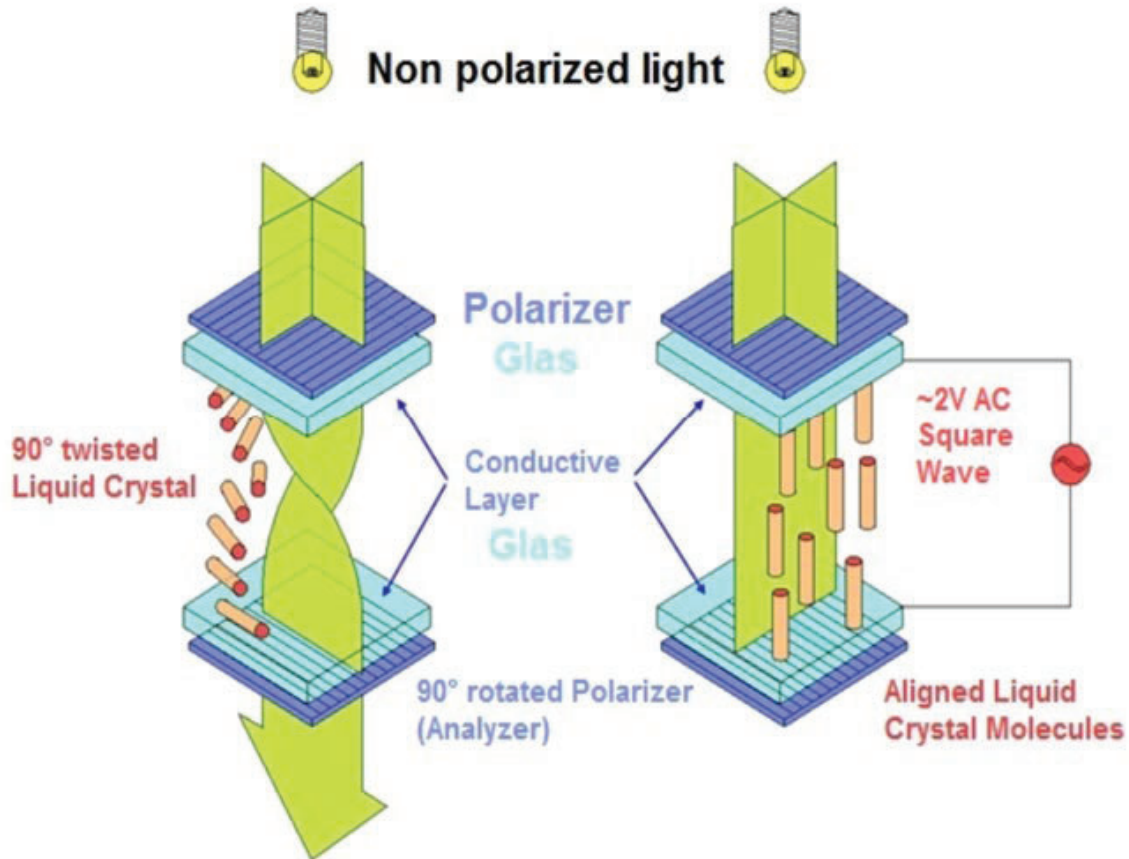
the light transmission is controlled by the voltage between the pixel electrode and the common electrode. The basic layout is shown below:



65. In the art, row lines are also known as gate lines, scan lines, or select lines. Column lines are also known as data lines, source line, or drain lines.

1. Pixel Grayscale Control

66. As shown below, the fundamental action of TN LCDs at the pixel level is the degree of twisting of the liquid crystal material as determined by the analog voltage between the pixel electrode and the common electrode.



A typical pixel transmission-voltage curve is illustrated below:

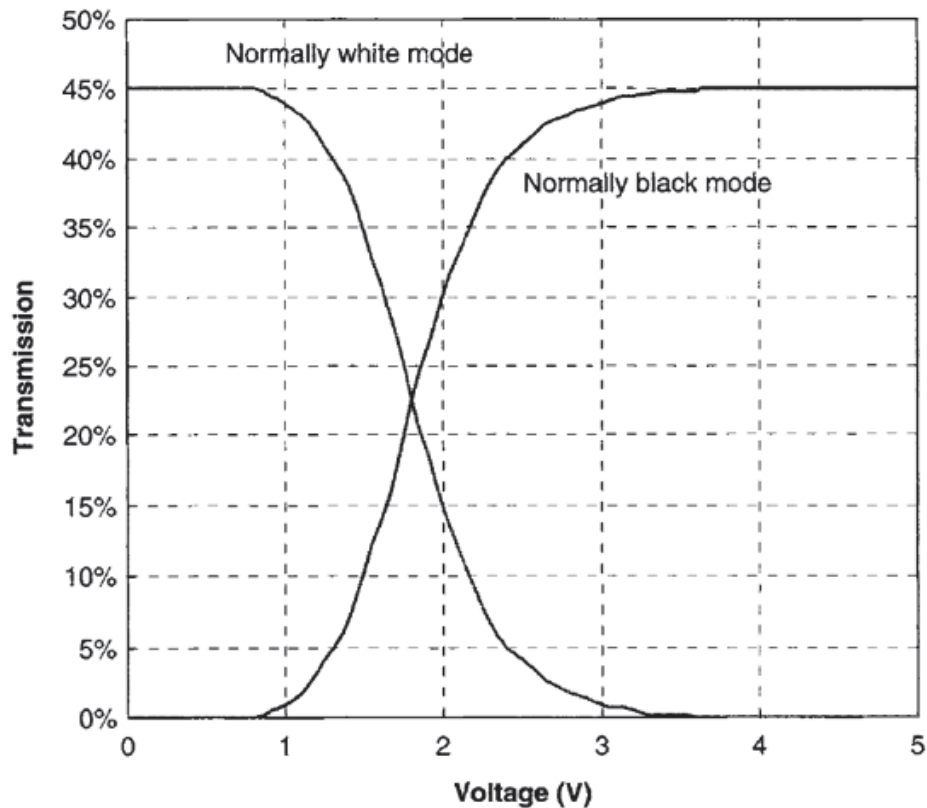


Figure 1.11: Transmittance-voltage curve for TN cell in normally white and normally black mode.

67. The normally white mode is implemented with crossed bottom and top polarizers, while the normally black mode is implemented with bottom and top polarizers having parallel alignment.

68. The level of voltage across the LCD material (from the pixel electrode to the common electrode) causes optical effects, such as changes in the polarization of light transiting the pixel, which in turn determines the fraction of light from a back light unit (BLU) allowed through the pixel. Thus, the brightness at each pixel

is determined by the analog voltage level written to each pixel, thereby creating a gray scale image on the whole screen.

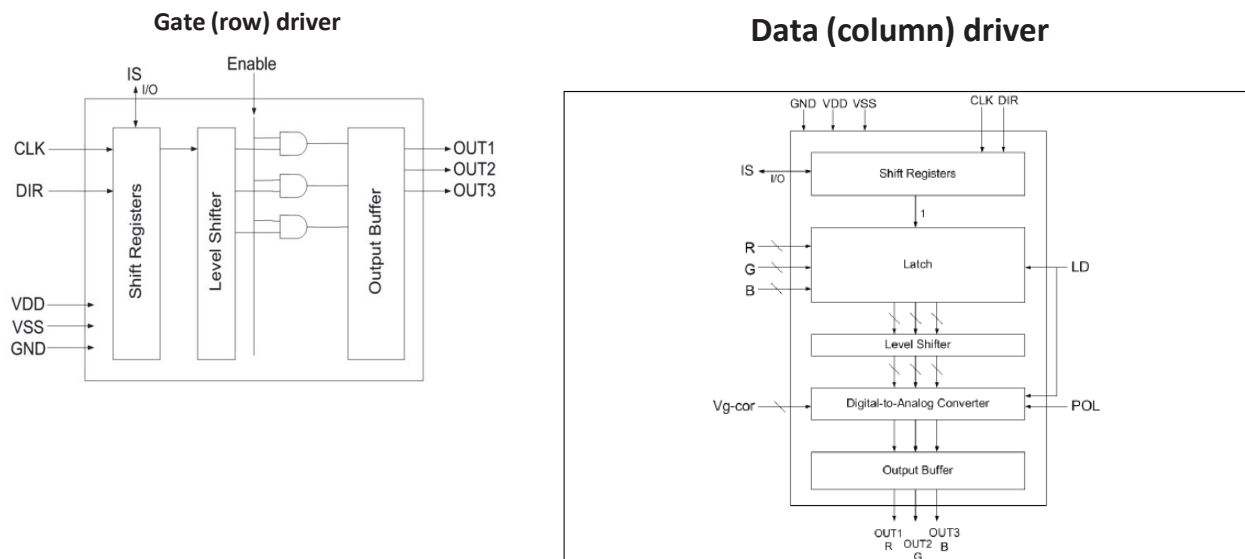
69. The basic addressing process by which grayscale screen images are produced comprises the coordinated action of the data drivers, the scan drivers, the scanning line clock and the data shift clock as explained below. This type of active matrix addressing has been well known since the 1980s.

70. The operation of the panel centers around implementing “line at a time” writing. Digital brightness data is shifted into the column drivers for an entire row. The row driver activates all of the TFT gates on an entire row by causing the row line to go high. At the same time, the digital data in each column register is sent through a digital to analog converter, and the resulting analog voltage level for each data line is provided to all data column line simultaneously. The gates of all of the TFTs in the activated row have a high voltage on them that makes the transistors conductive, and the voltage from each column line is transferred through each activated TFT to each target pixel electrode in the activated row. While the activated row is thus being written, the brightness data for the next row is being shifted into the column registers in preparation for writing the next row. At the end of the row writing period, the row driver de-activates the current row and activates the next row. At that time, the column driver delivers the analog voltages to the columns for that next row. The process repeats starting from

the first row and proceeds one row at a time to the bottom row; thus writing a complete frame of pixels. The process then cycles back to the first row and begins again for the following frame. The degree of pixel light transmission is determined by the analog voltage written to each pixel, thereby creating a gray scale screen image for each frame.

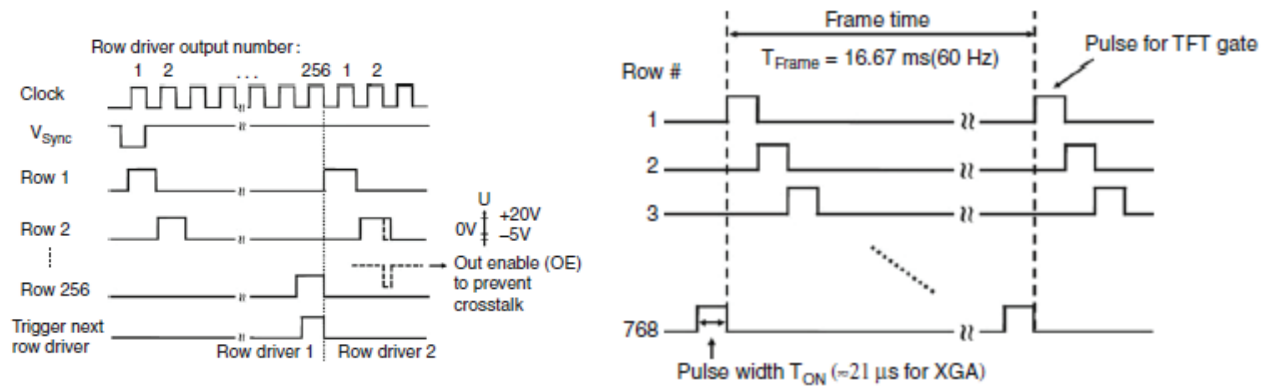
2. Row/Scan Driver and Column/Data Driver Designs

71. The basic designs of the row (scan) driver and the column (data) driver are shown below:

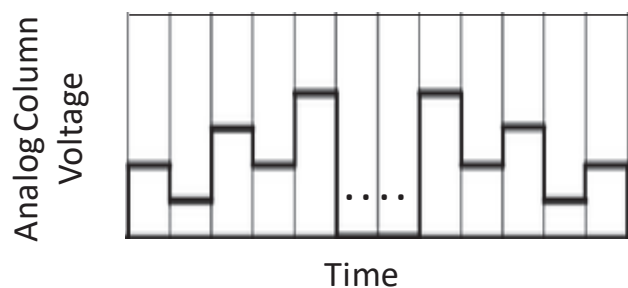


72. The row driver is a binary digital shift register with a single bit. When the output register has no bit, the line output for that register is low (generally around -5 volts). When the bit is in the output register, line output for

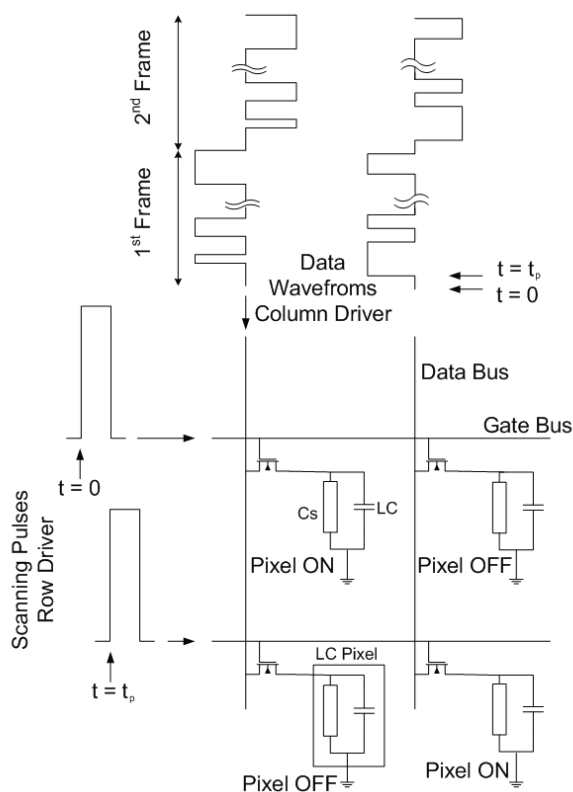
that register is high (generally about +15 volts). When the shift register receives a rising edge on the CLK clock input, the bit in the shift register is shifted down one line. The figure below shows an example of the operation of the row driver:



73. In contrast, the data (column) driver is much more complex. It is a mixed signal device (*i.e.* it must handle a mixture of digital and analog signals). It comprises a shift register where digital brightness data is shifted in, a latch to store the digital data while the next line of brightness data is being received, and a high speed precision digital to analog converter for each column. Each time the data driver clock has a rising edge, the next bit of digital brightness data is shifted into the shift register and all bits in the shift register are shifted one register to the right. The figure below is an example of gray scale analog voltages appearing on a column line during a frame. Since LCD pixels require an AC waveform, the next frame will have an inverted waveform from the one illustrated below.



The timing is illustrated below:

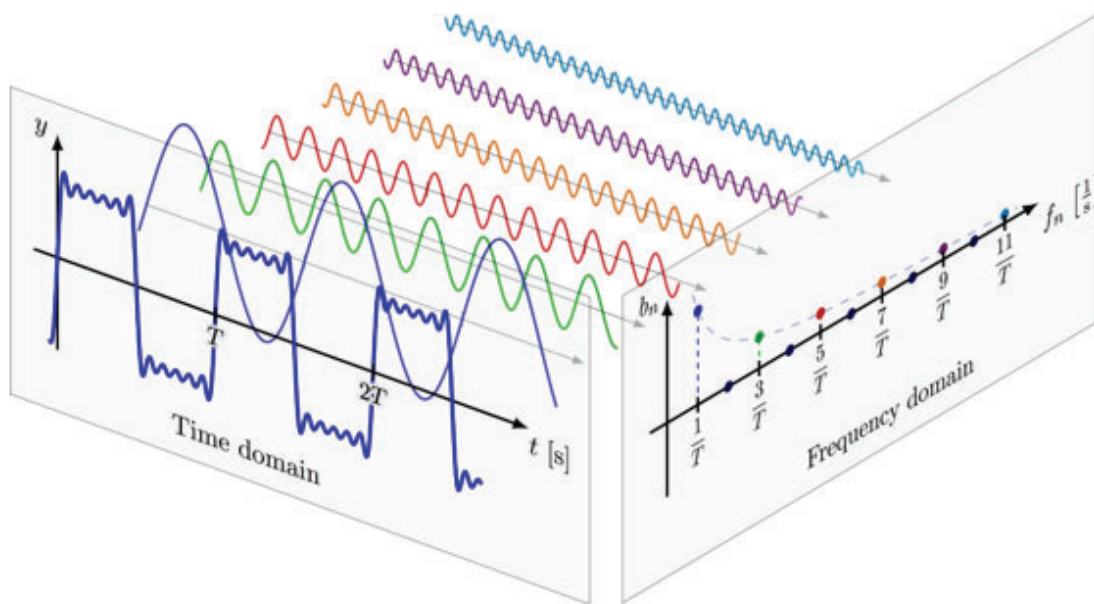


74. It is common to provide both the row and column waveforms to the pixel matrix using flex (flexible) connects, while locating the drivers on the flex. In principle, there is a cost and size advantage to moving the drivers onto the active

matrix glass substrate itself. This can be done for the row drivers. The data (column) drivers, however, are much more complex. The data drivers are mixed signal, have shift registers, latches, and precision high speed digital to analog converters and analog buffers. Therefore, it is much easier to move the row drivers onto the glass while leaving the column drivers on TAB/flex connecting to the active matrix substrate using anisotropic conductive film (“ACF”). It was also conventional at the time of the alleged invention to locate the “power source means” and the “signal generation means” (as recited in claim 6 of the ’146 patent) on the flex, instead of forming such components on the LCD panel’s substrate (which could not be easily done for similar reasons that forming row drivers on the substrate could not be easily done).

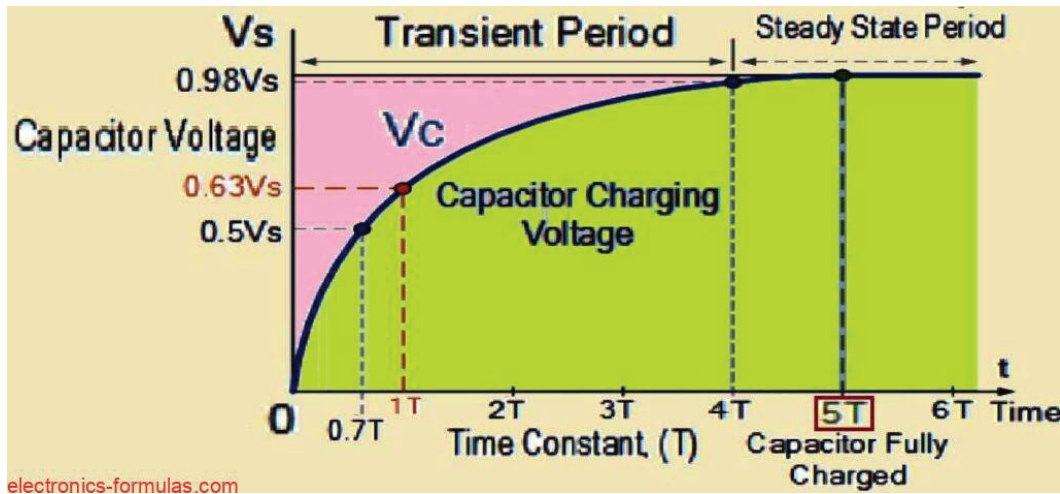
3. Row/Scan Driver Clock Considerations

75. Clock waveforms are usually square waves. In Fourier analysis, a square wave is the weighted sum of the fundamental and all of the harmonics. The fundamental and each harmonic is called a frequency “component.”



76. The row shift register clock (YCLK) is a square wave, supplied by the TCON to the row driver. Each leading edge of a YCLK pulse causes the row shift register to shift the bit down one register. Square waves are the sum of a fundamental frequency sinusoid and harmonics (whole # multiples of the fundamental frequency (Fourier transform theory). The “RC time constant” is a high frequency blocking filter, *i.e.*, it blocks the higher frequencies of the intended signal. The shift register clock at the shift register node must reach a trigger voltage level **before** the shift register actually shifts the bit to the next register (bringing gate line n-1 to Vmin while bringing next gate line n to Vmax). A long time constant (attenuation of high frequency harmonics/components) slows the rise of the leading edge of each YCLK pulse. If it slows it enough, the node will never

reach the trigger level and the shift register will not shift. In the image below the trigger level might be at the 0.5Vs level, for example:



77. Additionally, during the time period between when leading edge of the YCLK starts and when the voltage reaches the threshold voltage in the shift register, the bit in the shift register remains in register n-1 when it should be in register n. During this period, the data analog voltages on the columns are erroneously being written into row n-1 instead of row n.

78. Thus, by chopping the high frequency components (harmonics), the shift register (and thus the whole LCD display) can malfunction. The frequency of the clock is not how often a pulse starts (pulse rate) but the highest required harmonic frequency necessary for the shift register to reach the trigger level without causing the display to malfunction. Such chopping action can result from high resistance traces or contacts between the scan driver and the row shift register.

Bigger (wider / larger area) contacts result in lower resistance, a lower RC time constant, and therefore allow higher frequency harmonics of the YCLK signals to pass. This allows the row shift register to operate properly. The critical “frequency” is not a pulse initiation rate, but the frequency of the highest harmonic required for the system to operate properly.

79. Each data line voltage has indeed the same transition rate as the scan register clock, but it does not have the same high frequency component constraint as the YCLK, because for the display to operate, it is acceptable for the voltage on the data column line to “leisurely” approach or reach its intended analog level during a time interval between leading edges of two YCLK leading edges. That is, so long as the data line reaches its intended analog level, before the TFTs on the current line turn off, the intended analog voltage will be transferred to the pixel electrode, before the transistor turns off and the display will operate normally. Thus, the data line signal does not need the higher frequency components of its Fourier transform. It is much more tolerant of a slow leading edge (lack of high frequency Fourier components). For this reason, the image signal input terminals in an LCD display can have a relatively larger resistance (hence, a relatively smaller area), than the clock signal input terminals.

VII. THE '146 PATENT

A. The Invention

1. Applicant Admitted Prior Art (“AAPA”)

80. The specification admits that LCD displays were “widely used” and had a “known” structure. Ex. 1001, 1:18-25. The structure of a “known electro-optical apparatus” included: (i) “pixel electrodes arranged in a matrix state”; (ii) “an element substrate on which switching elements, such as TFTs (Thin Film Transistors), connected to the pixel electrodes, are disposed”; (iii) “an opposing substrate on which opposing electrodes opposed to the pixel electrodes are formed”; and (iv) “a liquid crystal, which serves as an electro-optical material, filled between both of these substrates.” Ex. 1001, 1:18-31.

81. It was known that a “pixel includes the switching element, the pixel electrode, the electro-optical material, and the opposing electrode, and is arranged in a matrix state.” Ex. 1001, 1:31-50. Conventional elements for controlling the pixels included TFTs, scanning lines, data lines, and capacitors. “[W]hen a scanning signal is applied to the switching element through a scanning line, that switching element adopts a conductive state.” *Id.* “In this conductive state, when an image signal having a voltage in accordance with grayscale is applied to the pixel electrode through a data line, a charge in accordance with the voltage of the image signal is stored in the liquid crystal layer between the pixel electrode and the opposing substrate.” *Id.* “After the charge is stored, even if the switching element is turned to an off state, the storage of the charge in that liquid crystal layer is maintained by the capacitance of the liquid crystal layer itself, the storage

capacitance, and the like.” *Id.* “In this manner, when each switching element is driven, and the charge amount to be stored is controlled in accordance with grayscale, the alignment state of the liquid crystal is changed for each pixel, and thus the density changes for each pixel.” *Id.* “It is, therefore, possible to display grayscale.” *Id.*

82. These known structures included “an electro-optical panel on which the above-described pixels are disposed in a matrix state.” Ex. 1001, 1:51-62. “A scanning-line drive circuit, which drives scanning lines, and a data-line drive circuit, which drives data lines, are sometimes formed on the electro-optical panel.” *Id.* “A power source, a driving signal, an image signal, etc. are supplied to the electro-optical panel having drive circuits.” *Id.* “As means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.” *Id.*

83. And during prosecution, the applicant admitted that supplying image signals “simultaneously to all of the data lines,” as recited in claim 10 (numbered claim 15 during prosecution), was known as the “line sequential method,” a technique that was admittedly “well-known to those skilled in the art.” Ex. 1003, (Response dated Sept. 17, 2008).

2. The Problem Addressed By the ’146 Patent

84. The claims recite admittedly conventional structures, with the alleged novelty lying in the input terminals' relative areas.

85. As was well-known, “the resistance of an input terminal becomes smaller as the area thereof becomes larger.” Ex. 1001, 1:63-2:2. While it was “desirable” to make the input terminals large (*i.e.*, make them wider than other terminals with the same length) to reduce their resistance, this would not work when “all of the input terminals cannot be disposed in a limited area.” *Id.* Further, when “the number of input terminals becomes large” and “when a flexible substrate, etc., are mounted, a problem of connection failure or the like has occurred.” *Id.*, 2:3-14. On the other hand, if the area of all input terminals was “made small,” their “contact resistance increases” as was well-known, which could cause “a problem in that the driving signal cannot be input at a proper timing.” *Id.*

86. The inventor solved this dilemma in exactly the same way as the prior art had already solved it: using “larger area” terminals for signals that need to utilize terminals having lower resistance (*e.g.*, power source signals or clock signals having a “higher frequency component”), while using smaller area image signals input terminals. Ex. 1001, Abstract (“The driving signal includes a higher frequency component than the image signal” so its input terminals “have a larger area”); 1:63-64 (“[T]he resistance of an input terminal becomes smaller as the area thereof becomes larger.”); 3:23-42 (if the power source input terminal “has a high

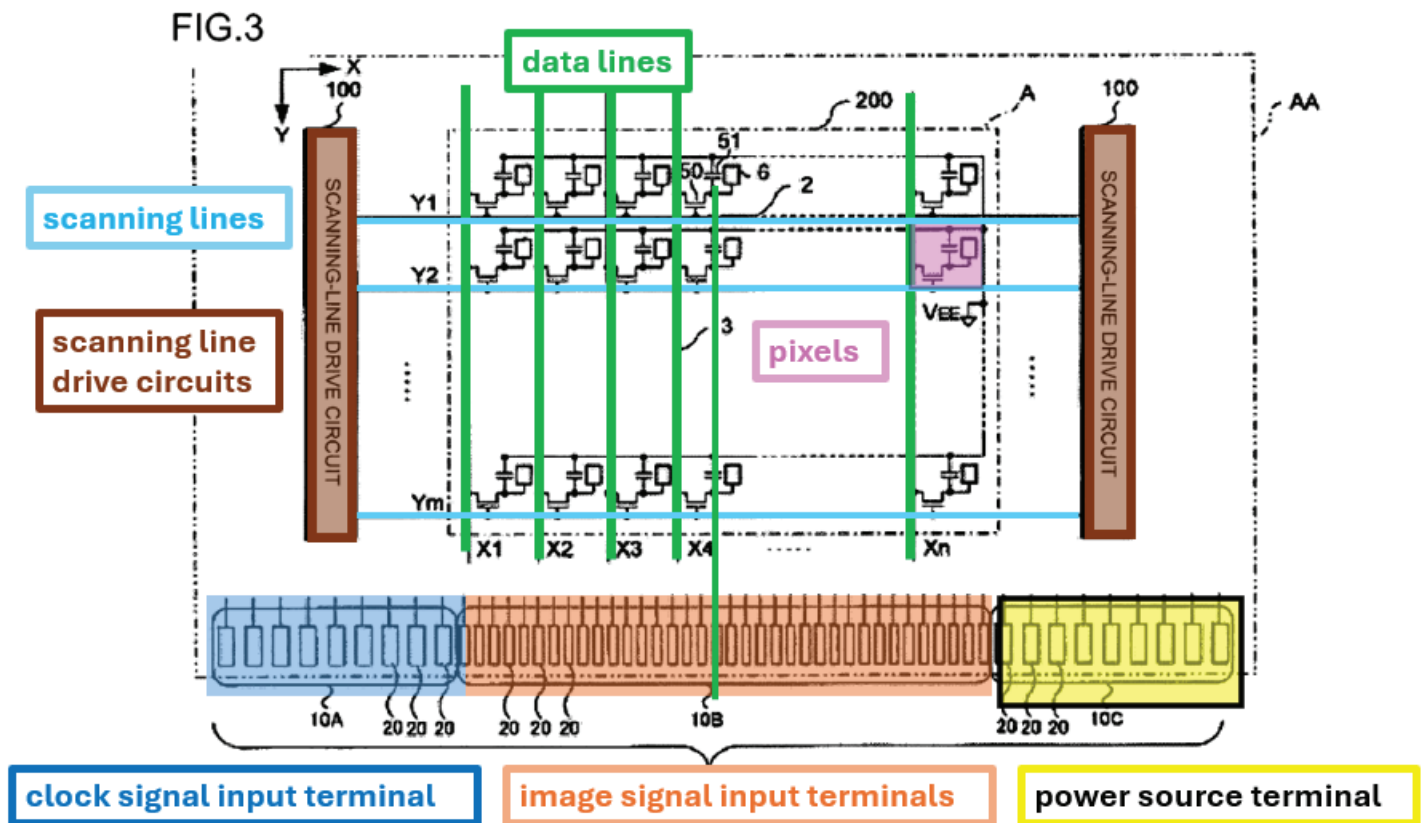
resistance, the voltage is trapped”); 3:5-9 (“[B]y . . . allocating the area of the input terminals, it becomes possible to appropriately dispose input terminals in a limited area.”); 7:56-8:3 (area of input terminal “to which the image signal having a relatively low frequency component is supplied is made smaller”); 2:52-58 (“For an input signal which includes a high-frequency component, the input signal waveform can be captured without becoming dull by setting the time constant to a small value. Whereas for the input signal which consists of relatively low-frequency components, there is no problem even if the time constant is large, and thus the area of the input terminal can be made small.”).

87. The inventor’s “idea” that the clock signal input terminal has a “larger area” than the image signal terminals is recited in every independent claim. *See* [1i], [10j], [23l]. [1h] also recites the related concept that a “power source terminal” has an area that “is not smaller” than the clock signal input terminal.

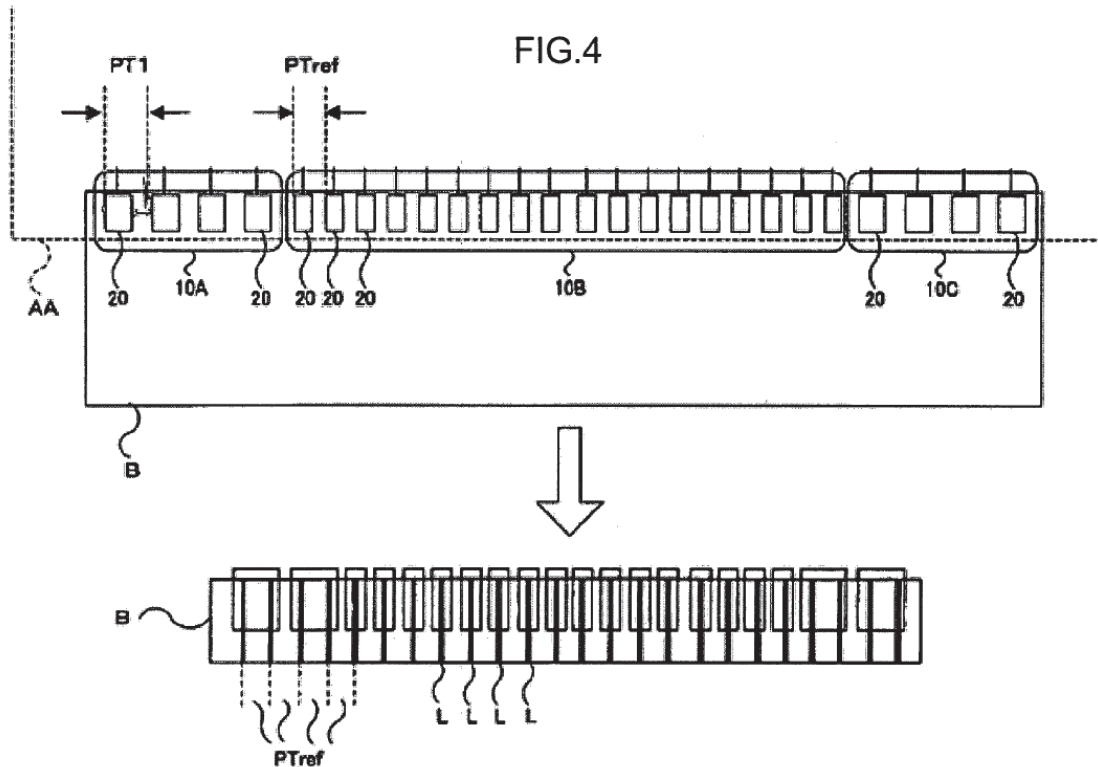
88. The patent states that it is “preferable” to put all of the input terminals “in line on a substrate” with the smaller area terminals “disposed in the central part of the substrate” and the larger area ones “disposed at the outer side of the substrate.” Ex. 1001, 3:10-21. This is beneficial because when “connecting each terminal with ACF [anisotropic conductive film], heat and pressure are applied, and thus the outer side of ACF tends to have a larger extension rate than the central part.” *Id.* “Therefore, by disposing an input terminal having a wider area at a

more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is a large one even if a slight misalignment of the connection arises.” *Id.*

89. The invention is illustrated in Figures 3:



Ex. 1001, Figure 3. The invention is also illustrated in Figure 4, where “AA” is an LCD panel, “B” is a flexible substrate external to the liquid crystal panel, and “10” is a terminal group as shown in Figure 3:



Ex. 1001, Fig. 4 and 8:55-9:39. The pitch between the smallest area input terminals (and wiring "L") is PT_{ref} and the pitch between the larger area terminals is PT_1 . *Id.* The specification states without explanation that it is "preferable" to set PT_1 as an "integer multiple" of PT_{ref} . *Id.*

B. Prosecution History

90. Seiko Epson filed the application and originally drafted claim 1 to cover a panel comprising data and scanning lines; pixels; first and second input terminals supplied with first and second input signals; a drive circuit to control the pixels based on the input signals; "wherein the first input signal includes a higher frequency component compared with the second input signal, and the first input

terminal has a larger area than the second input terminal.” Ex. 1003 (original claims).

91. After the examiner rejected the claim (Ex. 1003, November 2, 2007 Office Action), the applicant specified that the first and second input terminals are “clock signal” and “image signal” input terminals, respectively. Ex. 1003, January 31, 2008 Response. It also added a “scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal ...” and a “power terminal supplied with a power source”; required the terminals to be “formed in line on a substrate”; and specified that the “pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.” *Id.*

92. Independent claim 10 corresponds to application claim 15, which debuted on May 21, 2008. Ex. 1003 at May 21, 2008 Response. As first filed, it recited a panel comprising data lines; scanning lines; pixels; a clock signal input terminal supplied with a clock signal; an image signal input terminal supplied with an image signal; a scanning line drive circuit; “wherein the clock signal input terminal has a larger area than the image signal input terminal.” *Id.*

93. After the examiner rejected this claim (Ex. 1003, Office Action dated June 24, 2008), the applicant amended it to add details about terminals being connected to a “mounting member through anisotropic conductive film.” Ex.

1003, Response dated September 17, 2008. The applicant also added new independent claim 23, which required, among other things, that “a substrate, the clock signal input terminal and the image signal input terminal are arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.” *Id.* The examiner rejected these claims (Ex. 1003, Office Action dated January 23, 2009), while finding without explanation that claim 1 was allowable.

94. The applicant then amended application claim 15 to require that the clock-signal input terminal “overlaps a first wiring of the mounting member through said anisotropic film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film.” Ex. 1003, April 14, 2009 Response (underlining in original, text deleted by applicant omitted). And it amended claim 23 by requiring that the “contact area between the first wiring and the clock signal input terminal is greater than the contact area between the second wiring and the image input terminal.” *Id.* The examiner allowed claims 15 and 23 without explanation, with an amendment to claim 23 deleting the language and adding that “the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input

terminals overlaps the second wiring of the mounting member.” Ex. 1003, Notice of Allowance of August 6, 2008.

VIII. CLAIM CONSTRUCTION

95. I have been asked to use the plain meaning of each of the claim terms for purposes of my analysis. However, I reserve the right to respond to any constructions that Patent Owner may offer or that may be adopted by the Board. That said, two terms in claims 5 and 6 use the phrase “means for” and are addressed below.

A. “power source means for supplying the power source”

96. Power sources were well-known. Indeed, the specification admits that “means for supplying the power source, etc., to the electro optical panel ... are known.” Ex. 1001, 1:51-62. Figure 5 discloses “power source circuit 500” mounted on external substrate (“C”) that is connected to a liquid crystal panel (“AA”) through a flexible substrate (“B”). Ex. 1001, Figure 5, 9:40-55. “The power source circuit 500 supplies a predetermined power source to the timing generation circuit 300 and the image processing circuit 400 in addition to supplying a high potential power source VDD and a low potential power source VSS to the scanning-line drive circuit 100.” *Id.*, 10:9-13. As discussed below, the prior art discloses “power source means for supplying the power source” under any reasonable construction, and discloses structures that are substantially the same or equivalent to the structures disclosed in the ’146 patent’s specification.

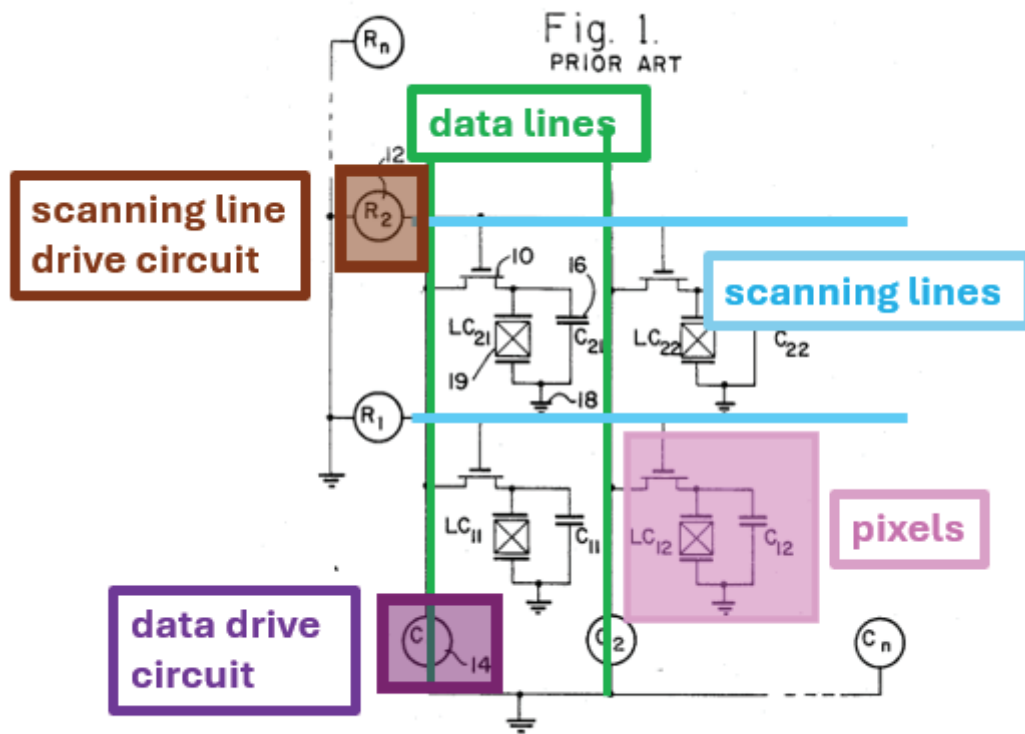
B. “signal generation means for supplying the input signals”

97. A signal generator is sufficient to supply input signals and such structures were well-known. In Figure 5 of the patent, “the data-line drive circuit 200, the timing generation circuit 300, and the image processing circuit 400 function as signal generation means for supplying input signals to the liquid crystal panel AA.” Ex. 1001, 10:13-17; *see* 9:40-10:17. As discussed below, the prior art discloses “signal generation means for supplying the input signals” under any reasonable construction, and discloses structures that are substantially the same or equivalent to the structures disclosed in the ’146 patent’s specification

IX. STATE OF THE ART

A. Koda (Ex. 1016)

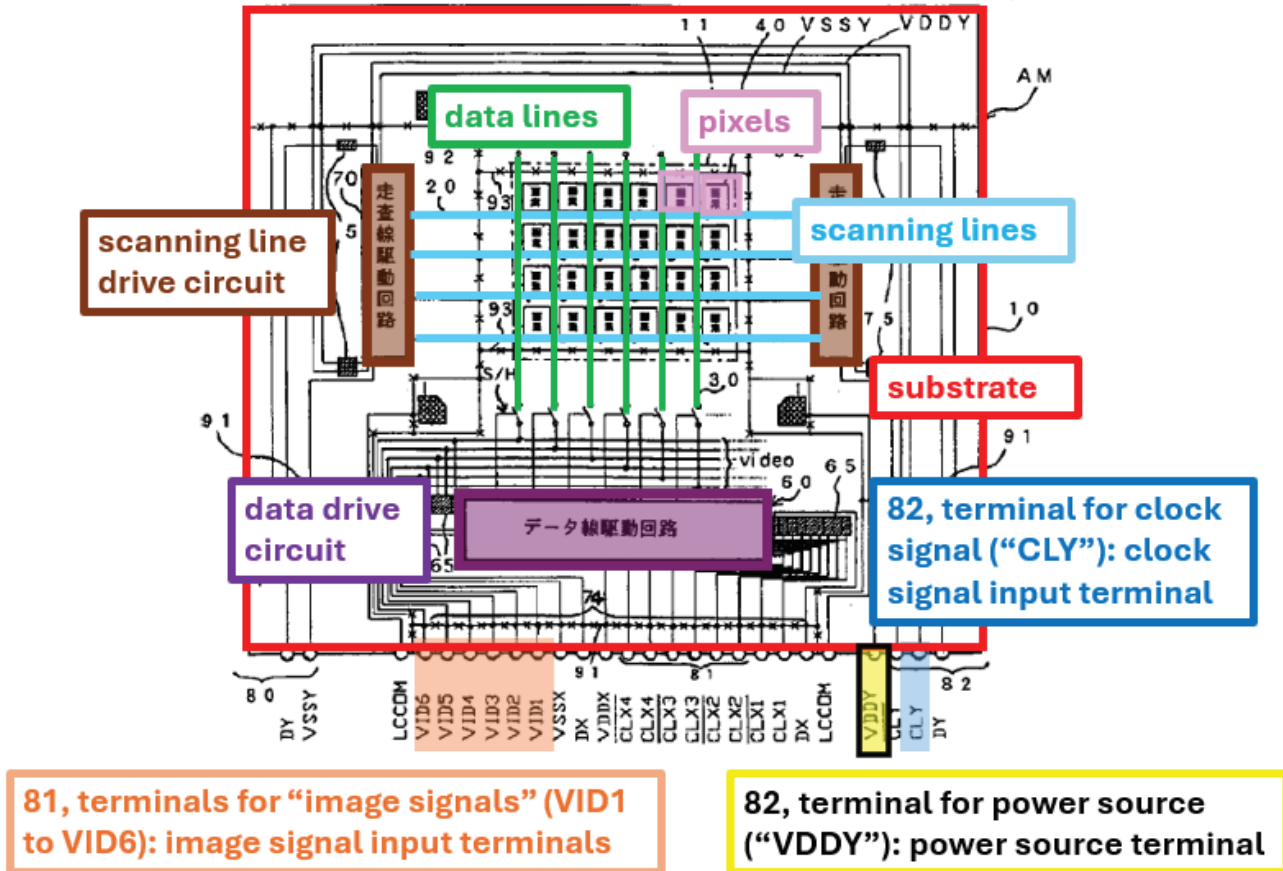
98. Most elements of the claims were patented decades ago. For example, claim 1 of Pat. No., 3,824,003 recites elements of a typical active-matrix liquid crystal display device, which are illustrated below:



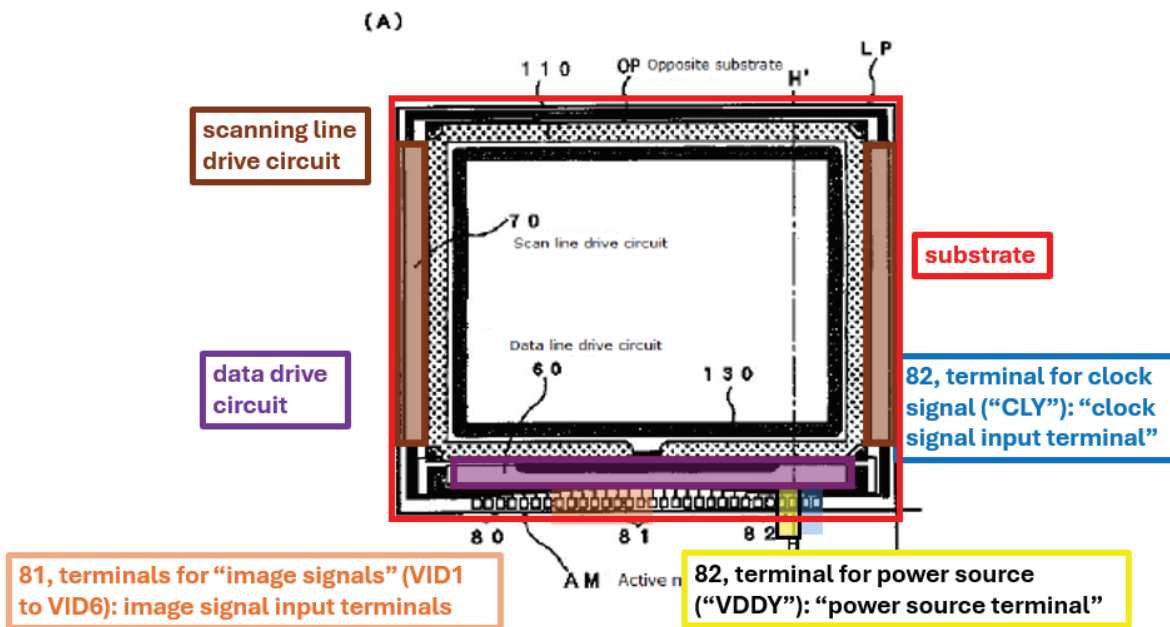
Ex. 1016, Figure 1 (the colored figures herein were annotated by Petitioner).

B. Kitawada (Ex. 1004)

99. Kitawada discloses the same conventional elements and more:



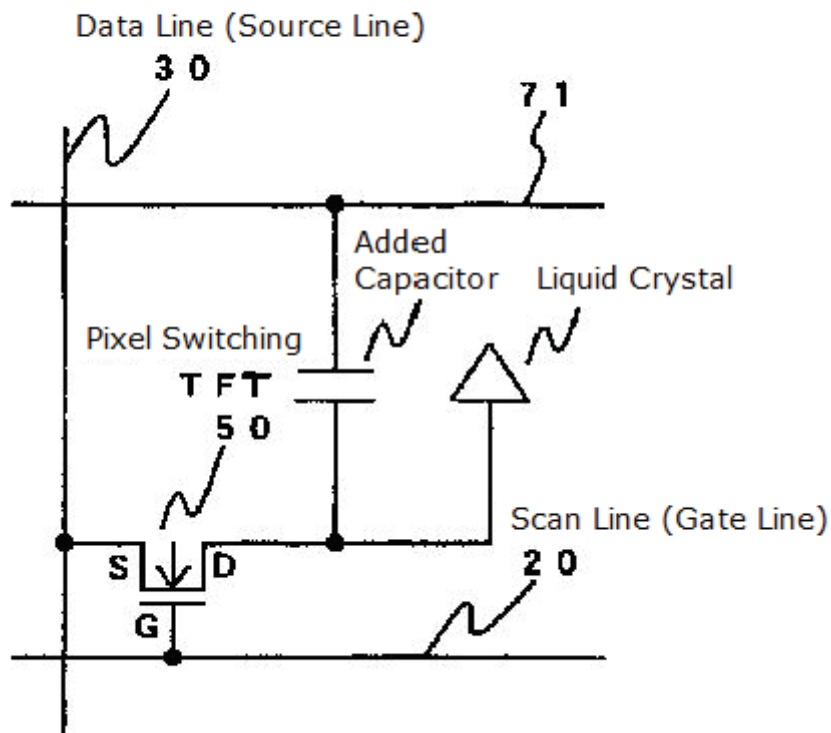
[FIG. 1]



Ex. 1004, Kitawada, Figure 2; Figure 1(A). In particular, just like the alleged invention of the '146 patent, Kitawada discloses input terminals arranged in a line on the edge of the substrate—with the clock signal input and power signal terminals located nearer to the substrate's edge than the image signal input terminals. As explained in detail herein, it would have been obvious to make the area of the clock signal input terminals larger than the area of the image signal input terminals, and it would have been obvious to make the area of the power source terminals at least as large as the area of the clock signal input terminals. Accordingly, all of the things that the '146 patent holds out as being novel were known and obvious at the time of the alleged invention.

100. Kitawada Fig 4 shows a typical pixel:

[FIG. 4]



20 is a scan line' 30 is a data line; and 50 is the thin film transistor (TFT). A storage capacitor is shown connected between the TFT drain and a fixed voltage "capacitance line" 71. The electro-optic portion of the pixel is the triangle comprising a pixel electrode, the liquid crystal material, and the common electrode.

101. Before the mid 1990s LCDs used the grayscale analog video voltage signals provided by TV tuners or by the VGA-type output of computers.

Kitawada uses an older style addressing/writing method to facilitate using such

video analog voltage signals coming from such a TV tuner or a VGA computer output to generate gray scale images on LCD screens.

102. Kitawada's drive architecture is shown in Figure 2 above. 11 is the pixel array; 20 is a gate line; 30 is a data line; 40 is a pixel; 70 is the scan driver; and 60 is the data driver shift register activating the sample and hold ("S/H") transistors. The basic Kitawada addressing process by which grayscale screen images are produced on the screen comprises the coordinated action of the data drivers, the scan drivers, the scanning line clock and the data driver shift clock as explained below. This type of "line at a time" active matrix addressing has been well known since the 1980's (and was also called "line sequential"). I personally used this addressing technique in the mid 1980's.

103. The operation of the Kitawada-type panel centers around implementing such "line at a time" writing utilizing incoming video analog grayscale signals. Referring to Kitawada Fig 2 above: Analog gray scale voltages are provided at the video inputs VIDx; a bit is moved through the data drive shift register by the CLXn clock signals; and as the bit moves through the shift register, the individual sample and hold transistors are activated and then deactivated. Each time a S/H transistor is activated, the analog grayscale voltage on the video line is transferred to a data line. The bit in the data shift register is then moved to the next register (by the CLXn clock) thereby deactivating the currently activated S/H

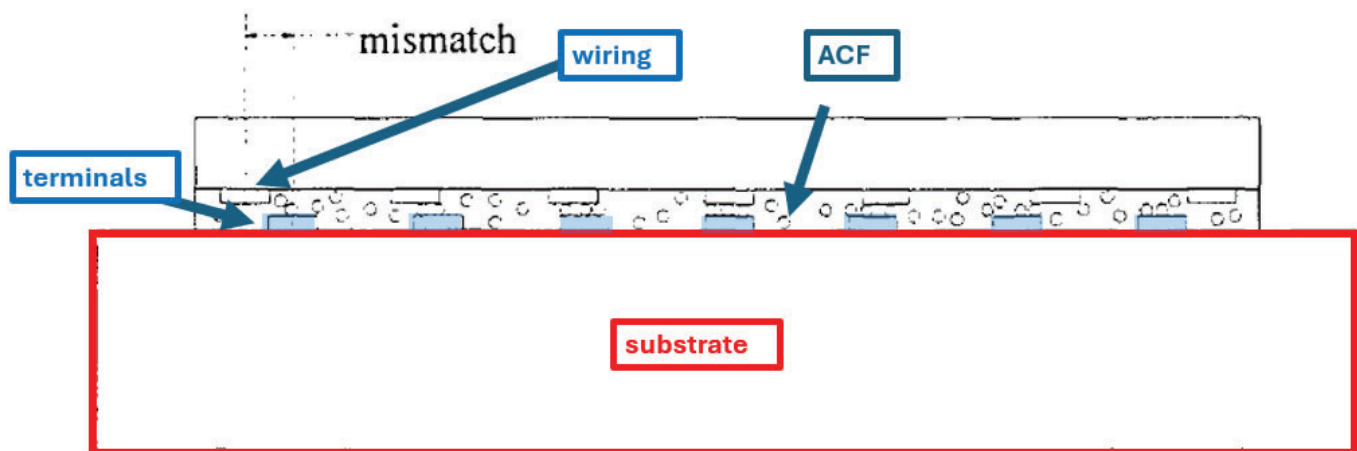
transistor thereby “trapping” the analog grayscale voltage on that data line by virtue of the data line capacitance, and also thereby activating the next S/H transistor to allow the next analog grayscale voltage to be transferred to the next data line. Once a whole line of video analog data voltages is stored on the data lines, the scan driver takes the target scan line high during the horizontal blanking period. The high voltage on the gates along the entire target row causes the TFTs in that row to conduct, thus transferring the analog grayscale voltages from the data lines to the pixels in the target row. At the end of the horizontal blanking period, the row driver takes the target row low, turning off all of the TFTs in that row, which traps the analog grayscale voltages on the storage capacitor at each pixel. The storage capacitor at each pixel then maintains the analog grayscale voltage across the pixel electrode/liquid crystal material/common electrode structure until re-written during the next frame.

104. After the next line of analog grayscale voltages are sampled and held on the data lines for the next row, the row driver takes the next row line high turning on all TFTs in that next row, so that all pixels in that next row receive the appropriate analog grayscale voltages. This process repeats line by line from the first row to the last row in a frame and then repeats the process, forming grayscale frames at the frame rate (typically 60 frames per second).

105. The degree of pixel light transmission is determined by the video analog voltage written to each pixel using the addressing process detailed above. Thus, a gray scale screen image is created for each frame.

C. Mismatch Analysis Report (Ex. 1014)

106. It was well-known that there could be a “mismatch” between input terminals having a “fine pitch” on an LCD substrate and wirings from an external “driver IC TAB” which are bonded using anisotropic conductive film (“ACF”). Ex. 1014 (“Mismatch Analysis Report”), at page 1 of 29. Like the ’146 inventor later realized, the mismatch is most acute for the “outer lead bonds (OLBs)” — terminals near the outside of the LCD’s substrate. *See id*:



Ex. 1014, Figure 1(b). This problem “will be inevitable if a uniform interconnection pitch is adopted in designing the TOG [tape on glass] connection.” *Id.* at page 2 of 29. This “will be likely to cause early failure of the LCD panel” and so “methods for alleviating the adverse effects induced by OLB [outer lead

bond] mismatch” were needed. *Id.* Similar to the claimed invention, Mismatch Analysis Report discloses “a nonuniform interconnection pitch” to mitigate these problems. *Id.*

107. As shown in detail below, Minami, Sano, Nakanishi, and Kato all disclose a nonuniform interconnection pitch, with certain terminals having larger areas. This (i) mitigates the problem of terminal-to-wiring “mismatch” and improves ACF bonding near the edges of an LCD panel’s substrate; (ii) reduces resistance for the scanning signal drive clock signal input terminals so that they can transmit “high frequency” components with fidelity; and (iii) reduces resistance for the power source terminals so they can conduct large currents.

D. Matsumoto (Ex. 1008)

108. Matsumoto discloses an LCD device having pixels at the intersection of scanning lines and data lines:

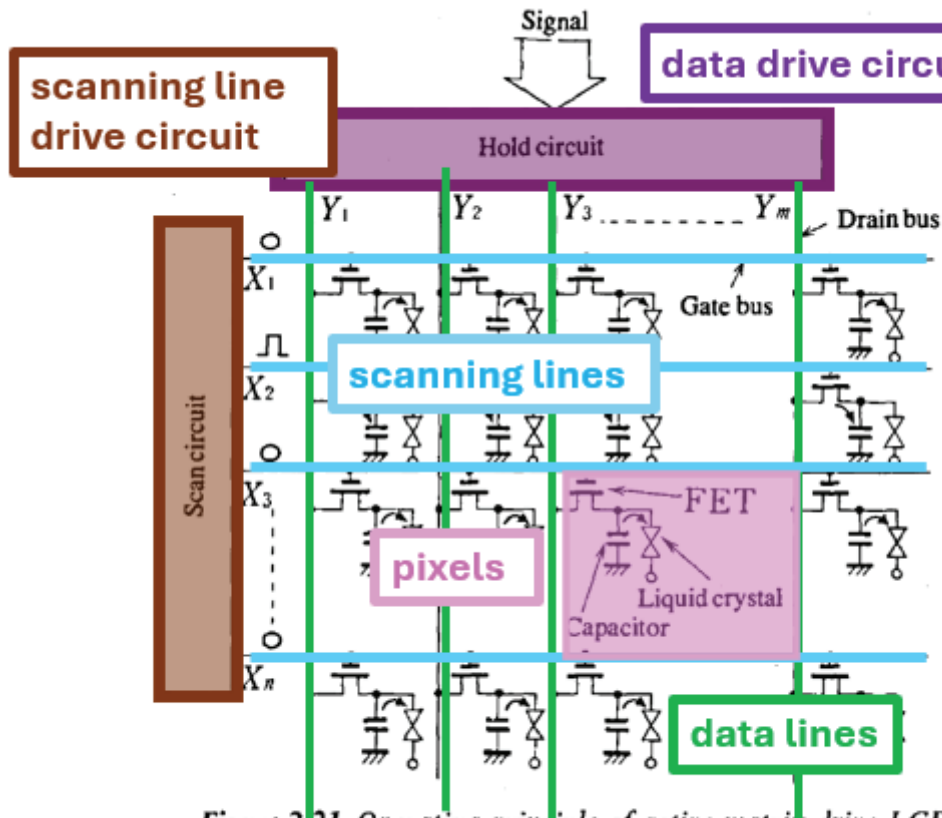


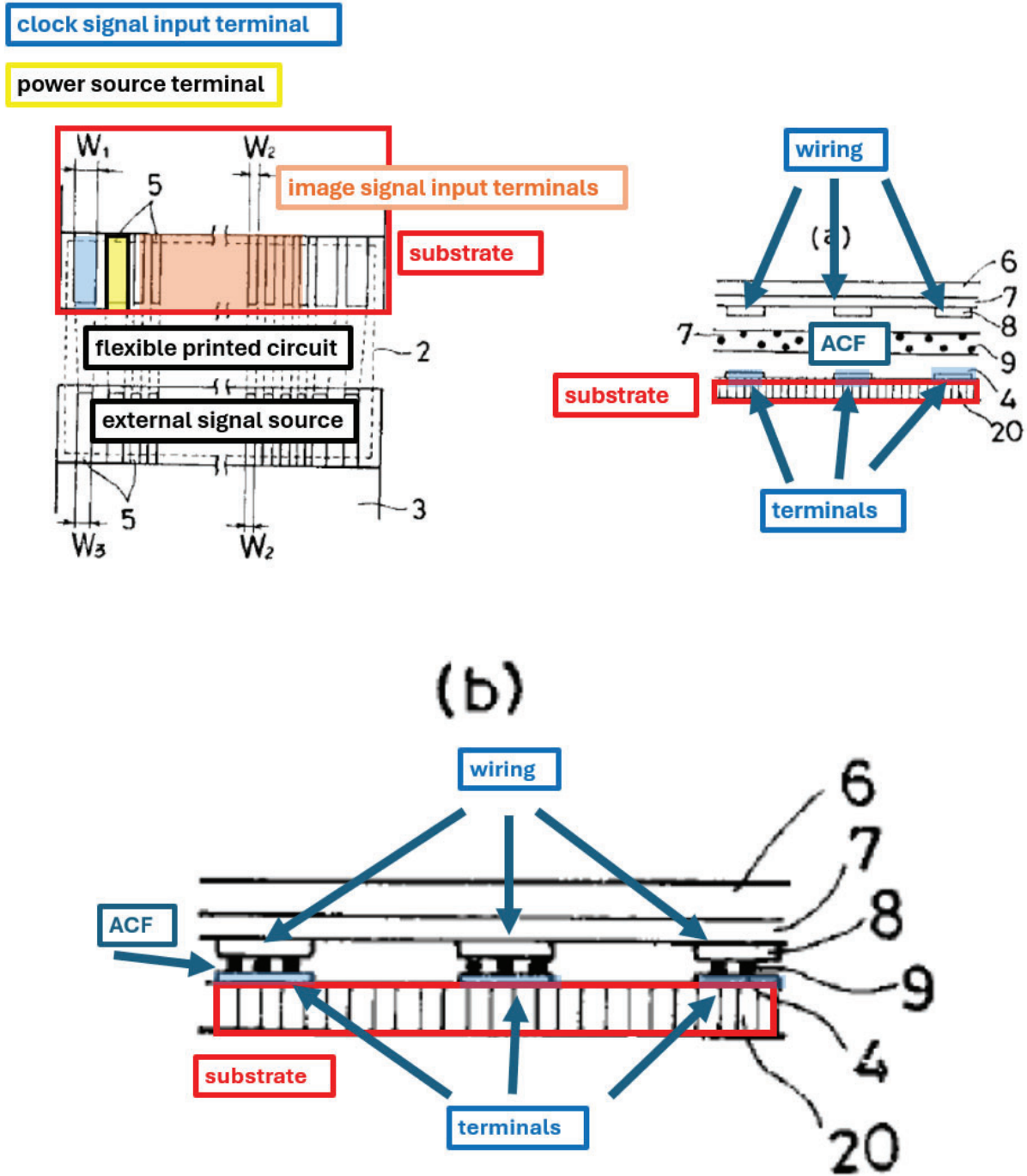
Figure 2.21 Operating principle of active matrix drive LCD

Ex. 1008, Fig. 2.21. A data line drive (“Hold circuit”) supplies the image signals, and a scanning line drive (“Scan circuit”) activates the pixel transistors in a row-sequential manner via a “Gate bus.” The image signals are supplied from the Hold circuit to all data lines “simultaneously” (*id.*, page 51 of 85), as recited in [10h].

E. Minami (Ex. 1007)

109. Minami teaches that LCD panels may “require high-density terminal pitch connection . . . between the drive circuit board and the display unit.” Ex. 1007 at page 13 of 18. When the “pitch is approximately 100 to 200 μm , the bonding area between the anisotropic conductive film and the LCD panel electrode

terminals is small, resulting in a decrease in bonding strength and bond delamination due to external pressure after connection.” *Id.* And “during assembly of the LCD panel unit or during transportation after connection, vibrations may cause a decrease in the reliability of electrical conductivity at the connection points.” *Id.* “In particular, external pressure, vibrations, and other factors cause stress on both ends of the FPC board, resulting in frequent electrical connection failures at both terminals.” *Id.* Just like the invention of the challenged claims, Minami discloses the solution, namely, “the pattern width near both ends of the electrode terminals connecting the liquid crystal display unit and the drive circuit unit is wider than the pattern width near the center.” *Id.* Minami’s Figure 3 (below on the left) shows that the outer terminals are wider (“ W_1 ”) and have a larger area than the narrower terminals (“ W_2 ”) near the center of the substrate:

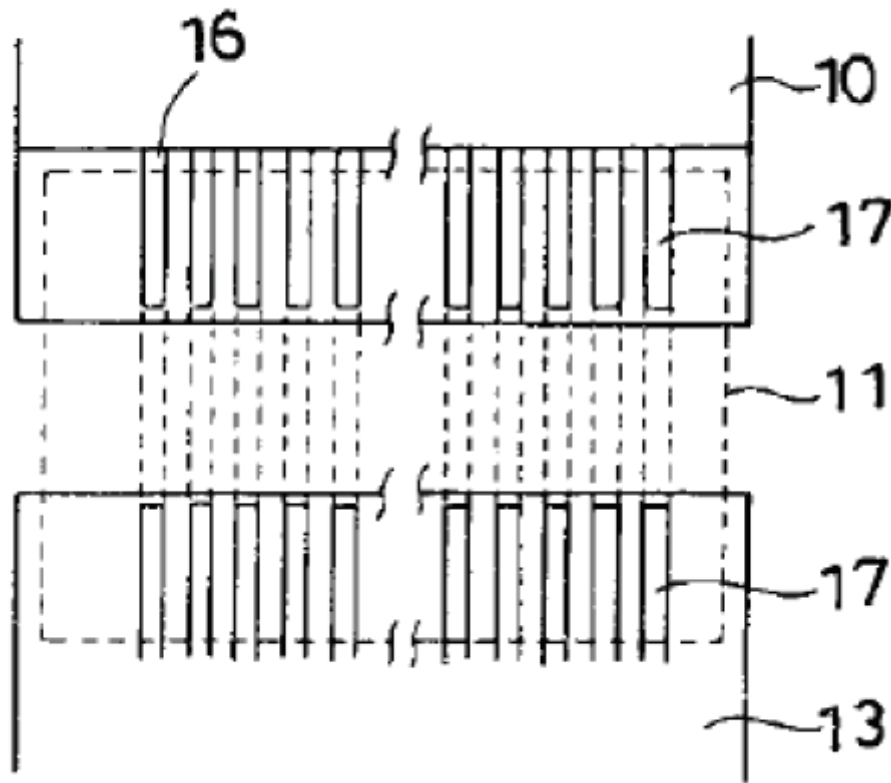


Ex. 1007, Figures 3, 2a, 2b. Figure 2 shows an “anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which

an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7.” *Id.* at page 14 of 18. “The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).” *Id.*

110. Wiring electrodes 5 (*see* Figure 3) also comprise ITO film 4, because Figure 2 shows that it is ITO film 4 overlapping the copper wiring pattern 8. The prior art section of Minami supports this conclusion. “FIG. 6 is a diagram used to explain an example of the prior art. The connecting material uses an anisotropic conductive film 15, and ITO ($\text{In}_2\text{O}_3 + \text{SnO}_2$) electrodes (transparent electrodes) 16 provided on the LCD panel 10 side and wiring electrodes 17 formed on the FPC board 11, as well as wiring electrodes 17 formed on the PWB board (printed circuit board) 13 . . .” Ex. 1007, at 13.

FIG. 6



Ex. 1007, Figure 6. Comparing Minami's Figures 1 and 3 with Figure 6, the ITO electrodes 16 and wiring electrodes 17 in the described prior art correspond to wiring electrodes 5 on LCD panel 1 and PWB board 3 in Figures 1 and 3. I note that ITO film 4 is annotated in Fig. 1. A POSITA would conclude that the ITO film 4 pattern of Fig. 2 corresponds to the wiring electrodes 5 on LCD panel 1 in Fig. 1, because the invention uses the same material ITO materials as the Minami's described prior art to form the wiring electrodes on LCD panel 1, while the novelty

of Minami's invention lies in the sizes (widths/areas) and positions of the terminals.

111. Since Minami's outer terminals have a larger area than the inner terminals (as shown in Figure 3), they overlap their respective wiring by a larger area through the ACF (as shown in Figure 2) as compared to the area that the (narrower) dinner terminals overlap their respective wiring through the ACF. It is clear from Minami's Figures 1-3 that wiring electrodes 5 (*i.e.*, terminals) on LCD panel 1 (LCD panel 1 corresponds to glass substrate 20 in Figure 2) overlap the copper wiring pattern 8 shown in Figure 2, in the area bounded by dashed lines in Figures 1 and 3 (which includes flexible printed circuit 2), by a larger area at the edges (recall that Kitawada's clock signal input terminals are near the edges of Kitawada's substrate) than in the center (Kitawada's image signal input terminals are located near the center of Kitawada's substrate). *See* Minami, Ex. 1007 at page 14 of 18 ("Because the pattern width near both ends of the electrode terminals in the liquid display device is wider than the pattern width of the electrode terminals near the center, ***the connection surface area*** of the electrical terminals is wider.") (emphasis added). Minami thus motivates and renders obvious elements [10j], [23l], [1h], [1i], and [1l].

F. Sano (Ex. 1006)

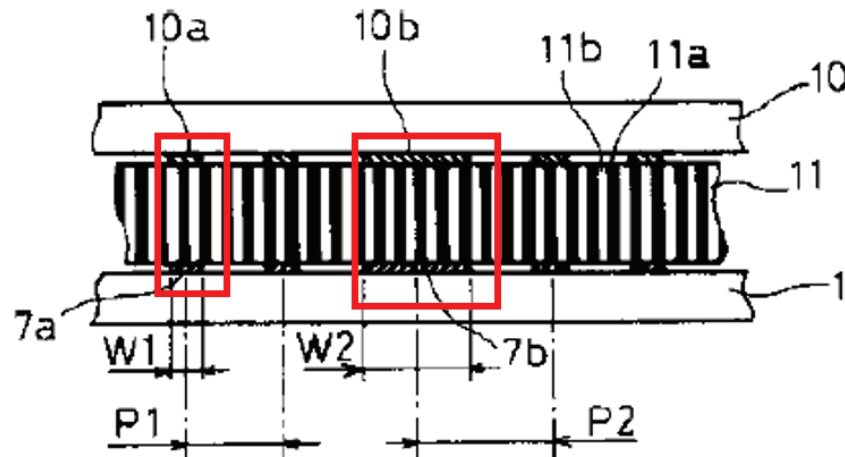
112. Sano teaches to increase the area of clock input terminals in LCD displays because they transmit a signal having “high frequency” components. Ex. 1006, ¶¶[0006]-[0008], [0018].¹ When an input terminal has a “high” resistance, “signal waveforms may become distorted” which “may cause malfunctioning of the liquid crystal panel driving IC 6 or the driving circuit of the panel.” Ex. 1006, ¶[0006]. I have explained this above in §VI.D.3, which I incorporate by reference herein.

113. Just like the alleged point of novelty of the '146 patent,² Sano discloses that the “terminal width and pitch for external connection terminals that transmit high-frequency signals” are “made wider than those for other external connection terminals.” Ex. 1006, ¶[0008]. “By adopting this structure, signal waveform distortion is minimized even at high frequencies, thus preventing malfunctions of the liquid crystal panel driving circuit.” *Id.*; ¶¶ [0009]-[0010],

¹ Cf. Ex. 1019, ¶[0063] (“the clock signal YCK has a much higher frequency (by a factor of 1000, for example) than usual, and continues to have this high frequency for at least m periods or more”); Ex. 1020, ¶[0040] (“the maximum frequency of an input image signal is about 6 MHz in the NTSC standard, and about 20 MHz to 30 MHz in the HDTV standard. In order to accurately display this image signal, a clock signal is required to have a frequency (for example, about 50 MHz to 60 MHz) several times that of this image signal”).

² Ex. 1001, 2:52-58 (“For an input signal which includes a high-frequency component, the input signal waveform can be captured without becoming dull by setting the time constant to a small value. Whereas for the input signal which consists of relatively low-frequency components, there is no problem even if the time constant is large, and thus the area of the input terminal can be made small.”).

[0018]. Similar to Minami's Figures 2 and 3 shown above, Sano's Figure 2 shows clock input terminals 7b (of width "W2") overlapping wirings 10b through an anisotropic connector by a larger area than input terminals 7a (of width "W1") overlap wirings 10a:



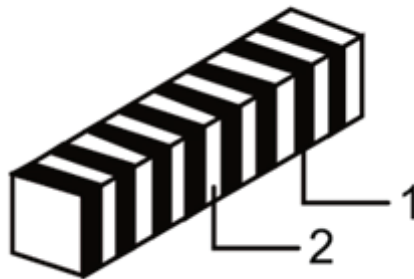
Ex. 1006, Figure 2. "Therefore, the connection resistance via the conductive sections 11a of the zebra rubber connector (11) at the terminals for transmitting high-frequency signals (i.e., between 7b, 8b and 10b) is lower than the connection resistance at other terminal portions of the transparent substrate electrode (9)."

¶[0014]. "As a result, distortion of the signal waveform for high-frequency signals is prevented, and malfunction of the liquid crystal panel driving circuit . . . can be effectively avoided." *Id.* "Moreover, at each connection point where high-frequency signals are transmitted . . . the terminal width is wider compared to other areas . . . This reduces wiring resistance and contributes effectively to the prevention of malfunctions." ¶[0015].

114. A POSITA would readily appreciate from Sano's teachings that an LCD panel's clock signal input terminals should have a larger area than its image signal input terminals. *See* Sano, Ex. 1006, ¶ [0018] (teaching that "malfunction of the drive circuit of the liquid crystal panel can be prevented and the reliability improved" by Sano's invention "***even if the external connection terminal is a terminal that transmits a high-frequency signal such as a clock signal***") (emphasis added); *cf.* Ex. 1019, ¶[0063] ("the clock signal YCK has a much higher frequency (by a factor of 1000, for example) than usual, and continues to have this high frequency for at least m periods or more"); Ex. 1020, ¶[0040] ("the maximum frequency of an input image signal is about 6 MHz in the NTSC standard, and about 20 MHz to 30 MHz in the HDTV standard. In order to accurately display this image signal, a clock signal is required to have a frequency (for example, about 50 MHz to 60 MHz) several times that of this image signal"). Sano thus independently motivates and renders obvious claim elements [1i], [1l], [10j], and [23l].

115. Sano refers to a "zebra rubber connector" so I want to explain what that means. As was well-known in the art, LCDs generally comprise two glass substrates with liquid crystal material in between the substrates. The substrates are held together (encapsulating the LC material) with an epoxy rim seal located near the periphery of the substrates. The substrates may be offset to allow scan line and

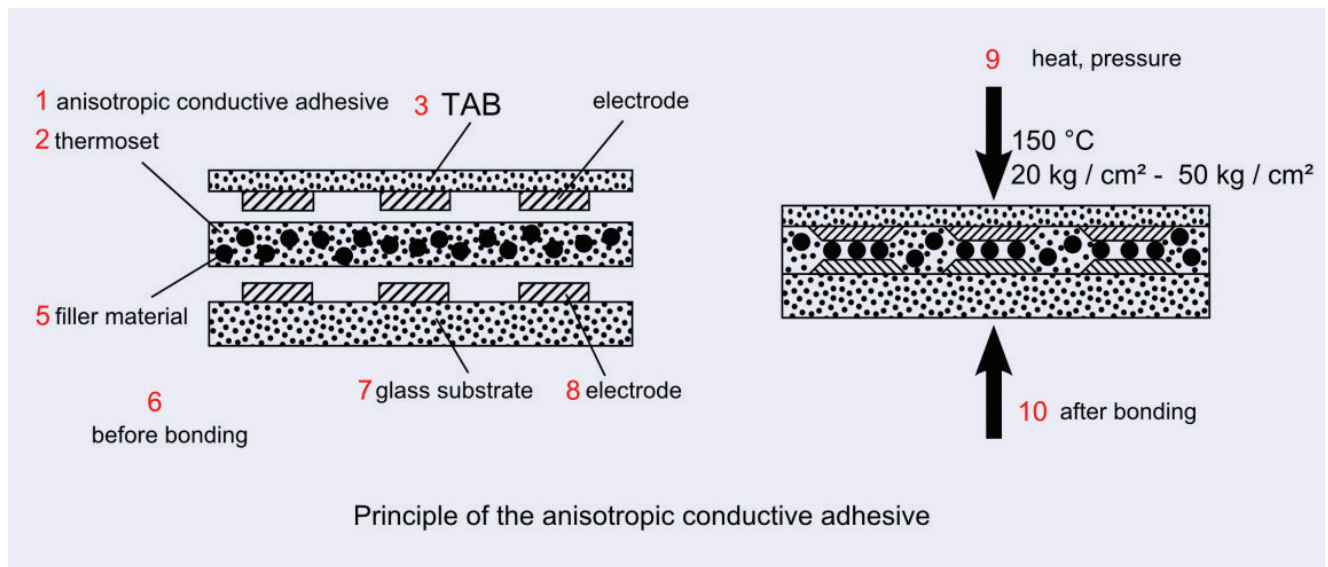
data line pads to be exposed. Typically, electrical connection is made to the pads. The pads may be connected Flex/TAB circuit where driver chips are located, or to a bridging flex circuit between the LCD pads and a rigid PCB where scan and data drivers are located, or the pads may be connected to the PCB directly (without the flex). In any case, there is an *anisotropic* connection means between the LCD pads and the flex or rigid PCB. A Zebra strip, comprising a monolithic block of alternating layers of silicone rubber and conductive film, was an early type of anisotropic connector and is illustrated below:



116. The connection methodology was simple mechanical placement and clamping pressure to allow the conductive sheets to make electrical contact between the LCD pads and the conductive trace on the flex or PCB. When using Zebra strips with flex, the flex required a rigid backing. The clamping pressure was supplied by a mechanical arrangement employing spring clips, pressure plates or the like.

117. In the early days of AMLCD (circa 1982), I was making prototype amorphous silicon AMLCDs at Alphasil, Inc. (the company I founded for that purpose). I was using Zebra stripes to make connection between the LCD glass and the PCB drive boards. The pressure was applied by picture frame bezels on the front side and back side of the LCD panel. The bezels had precision milled flat surfaces and were connected by screws. This arrangement supplied the pressure for connecting the LCD terminals to the PCB terminals.

118. These early prototypes worked initially. However, after a few months, all of the prototypes failed, because small inhomogeneities in the static pressure across the LCD glass substrates resulted in rim seal failure and air entering the region between the substrates. To remedy this problem, by the mid to late 1980s, I had switched from using Zebra strips to using the newer type of anisotropic connector, anisotropic conductive film (ACF) as shown below:

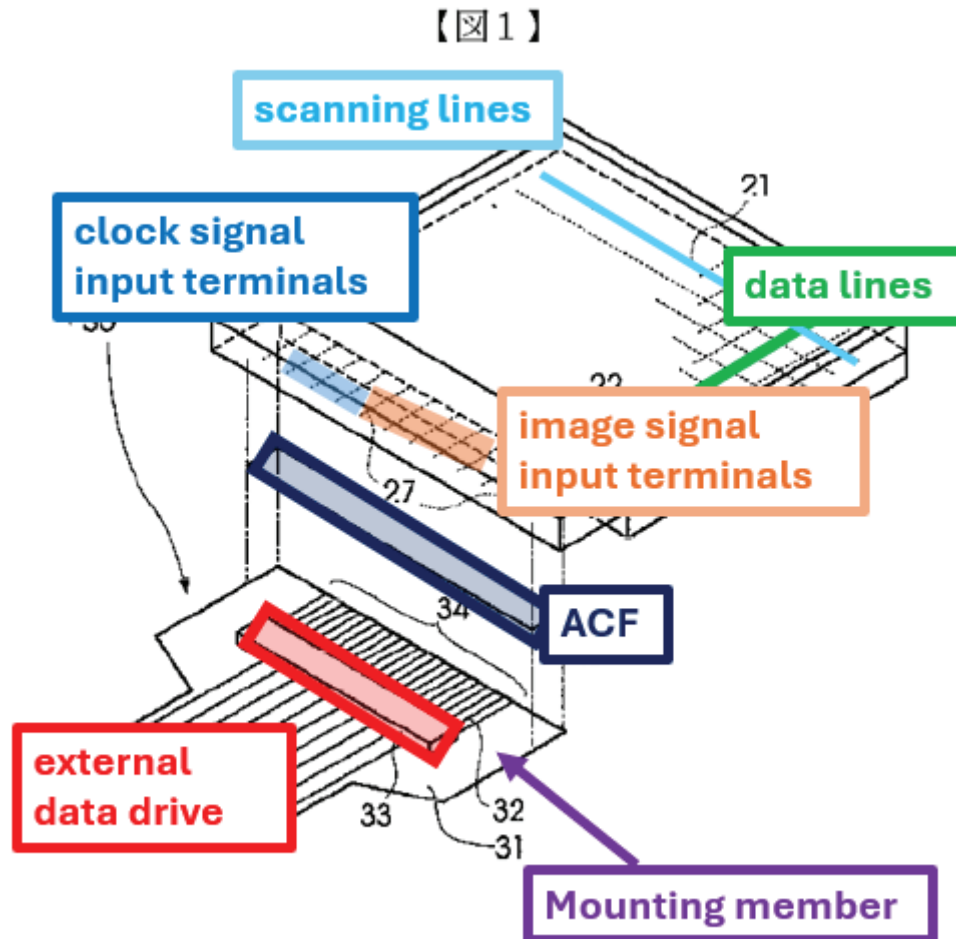


The ACF comprises conductive spheres in an insulating matrix. The LCD pads and flex pads are aligned with the ACF between the two. Electrical connection between the LCD pads and flex pads is formed by using a bonding head to supply heat and pressure for a few seconds to the terminal block. Once the bond is established, the bonding head is removed and there is no remaining pressure/stress on the LCD glass substrates. The result was by 1988 I had eliminated the failures caused by the constant pressure required by Zebra strips.

119. At the time of the invention of the '146 patent, a POSITA would have appreciated that Sano's teachings would work using ACF instead of a Zebra strip.

G. Nakanishi (Ex. 1010)

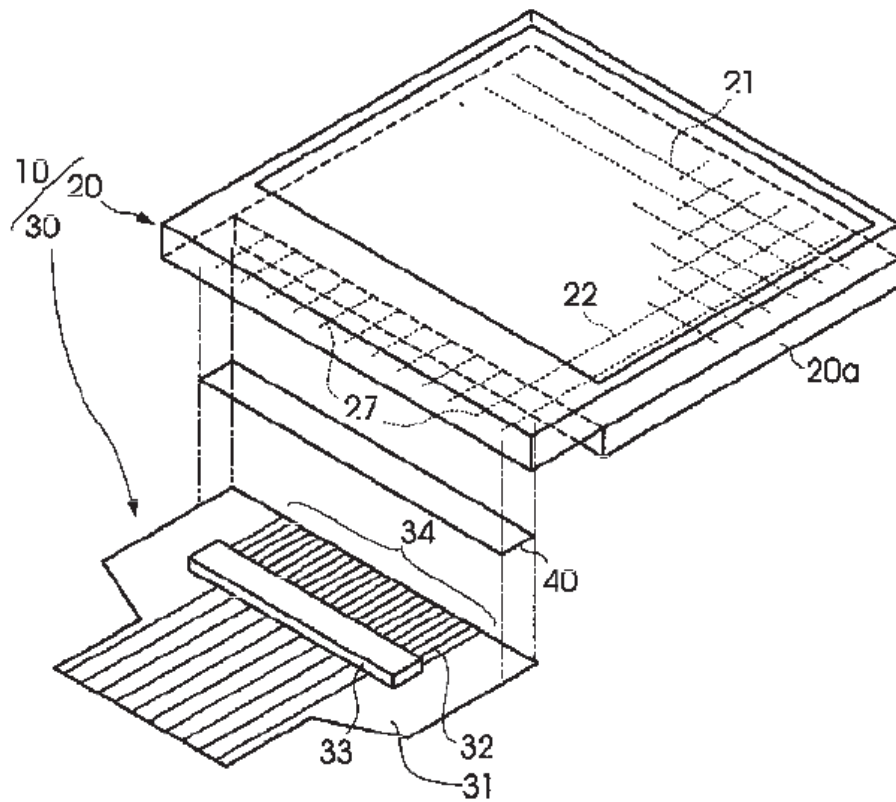
120. Nakanishi discloses using wider clock input terminals and power source terminals near the outer edges of a substrate, with narrower image signal input terminals near the center:



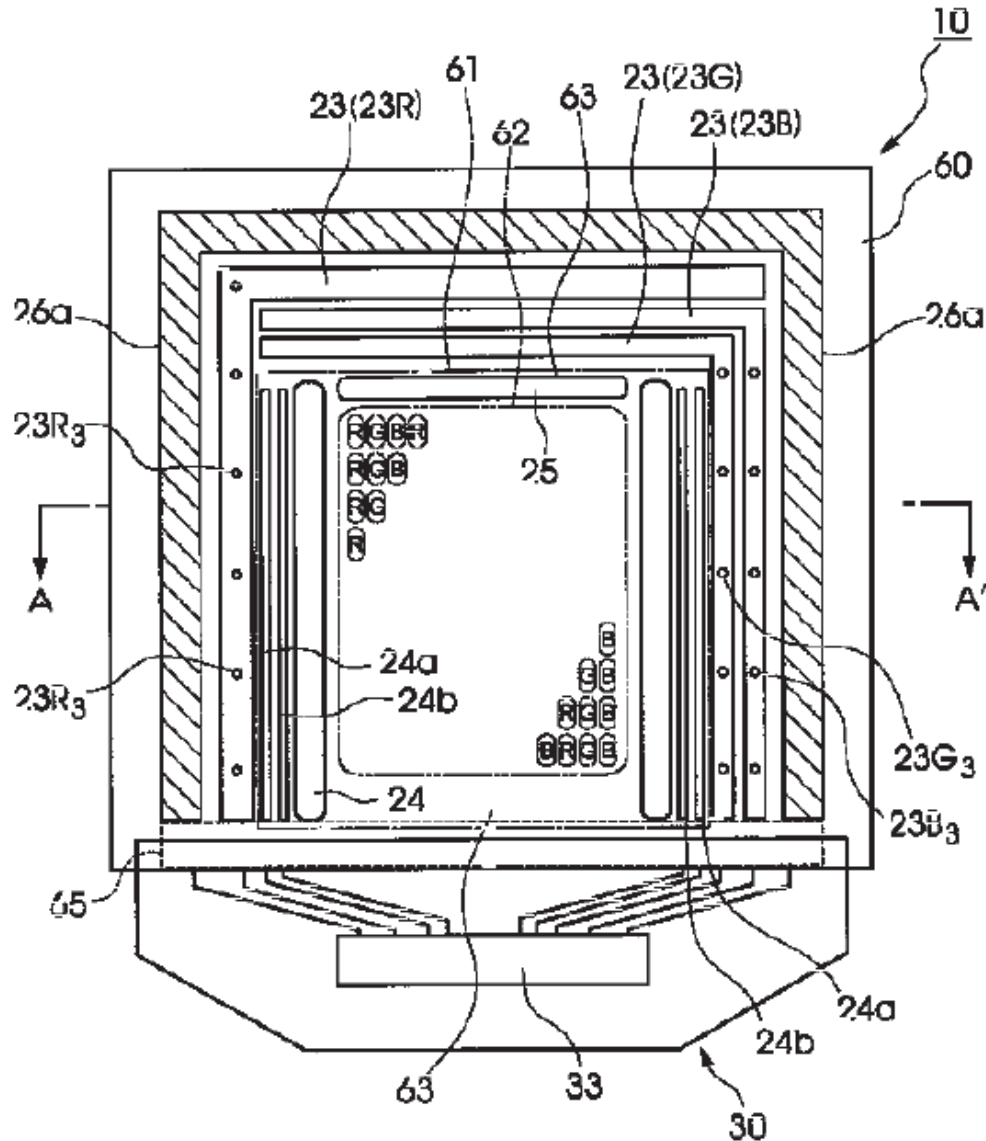


121. Nakanishi discloses an electro-optical panel (*i.e.*, “electro-optical device 10” of Figures 1 and 4).

【図1】



【図4】



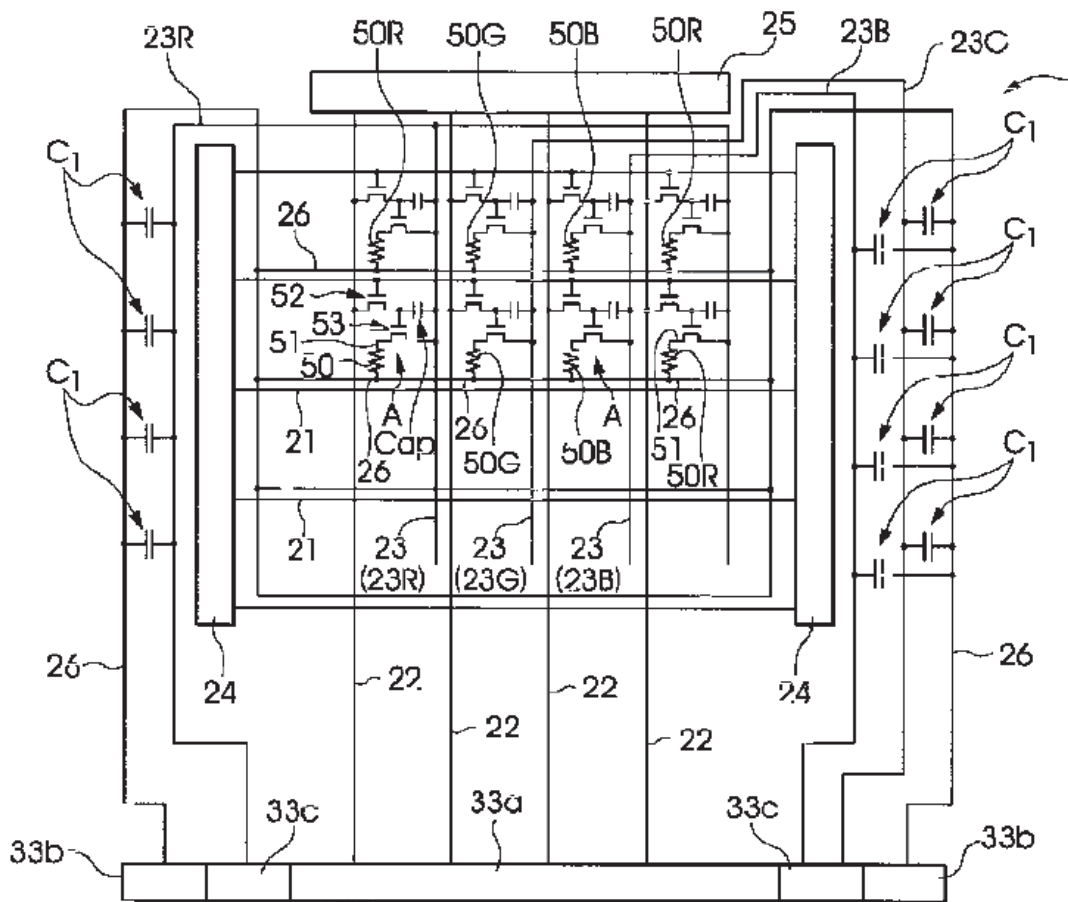
“FIG. 1 is an exploded perspective view of the electro-optical device in an embodiment of the present invention. As shown in FIG. 1, the electro-optical device 10 in the embodiment can be broadly divided into a display substrate 20 and an intermediate substrate 30 connected to the display substrate 20. The display

substrate 20 is an active matrix organic EL device that uses thin film transistors (TFTs) as switching elements.” ¶[0015]. “The specific configuration of the electro-optical device 10 in the present embodiment will now be described with reference to FIG. 4 and FIG. 5. FIG. 4 is a plan view of the electro-optical device in the present embodiment, and FIG. 5 is a cross-sectional view along line A-A’ in FIG. 4. As shown in FIG. 4, the electro-optical device 10 in the present embodiment is roughly composed of a substrate 60, a pixel electrode group area (not shown), light-emitting power supply lines 23 (23R, 23G, 23B), and a display pixel portion 61 (inside the single dotted-line box in the figure).” ¶[0030].

122. Nakanishi discloses a first substrate (*i.e.*, “display substrate 20” of Figure 1 and “substrate 60” of Figure 4).

123. Nakanishi discloses data lines (*i.e.*, “signal lines 22” in Figures 1, 3, 4, and 6):

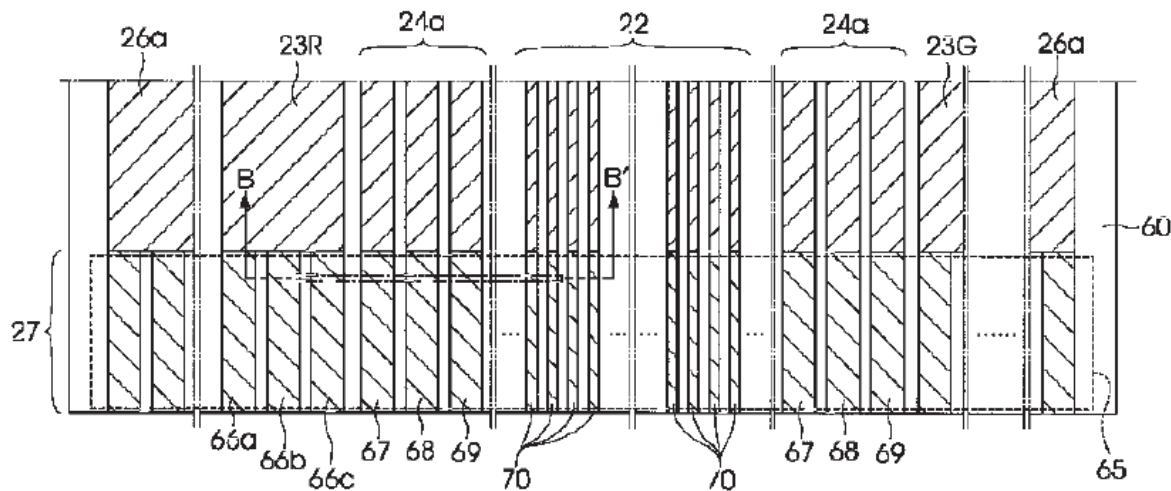
【図 3】



“A plurality of scanning lines 21 are formed on this display substrate 20, and a plurality of signal lines 22 extending in a direction intersecting the scanning lines 21 are also formed. In addition, the display substrate 20 is provided with display elements 20a in which a plurality of light-emitting elements are formed. Also, while not shown in FIG. 1, power supply lines and cathodes are also formed on the display substrate 20. In addition, external connection terminals 27 for the scanning lines 21, signal lines 22, power supply lines (not shown), and cathodes (not shown)

are formed at one end of the display substrate 20.” ¶[0016]. “The following is an explanation of an electro-optical device 10 in this embodiment. FIG. 3 shows the wiring structure of the electro-optical device in this embodiment of the present invention. As shown in FIG. 3, this electro-optical device 10 comprises a plurality of scanning lines 21, a plurality of signal lines 22 extending in a direction intersecting the scanning lines 21, a plurality of light emission power supply lines 23 extending parallel to the signal lines 22, and a pixel area A is provided at each intersection of a scanning line 21 and a signal line 22.” ¶[0023].

【図 6】

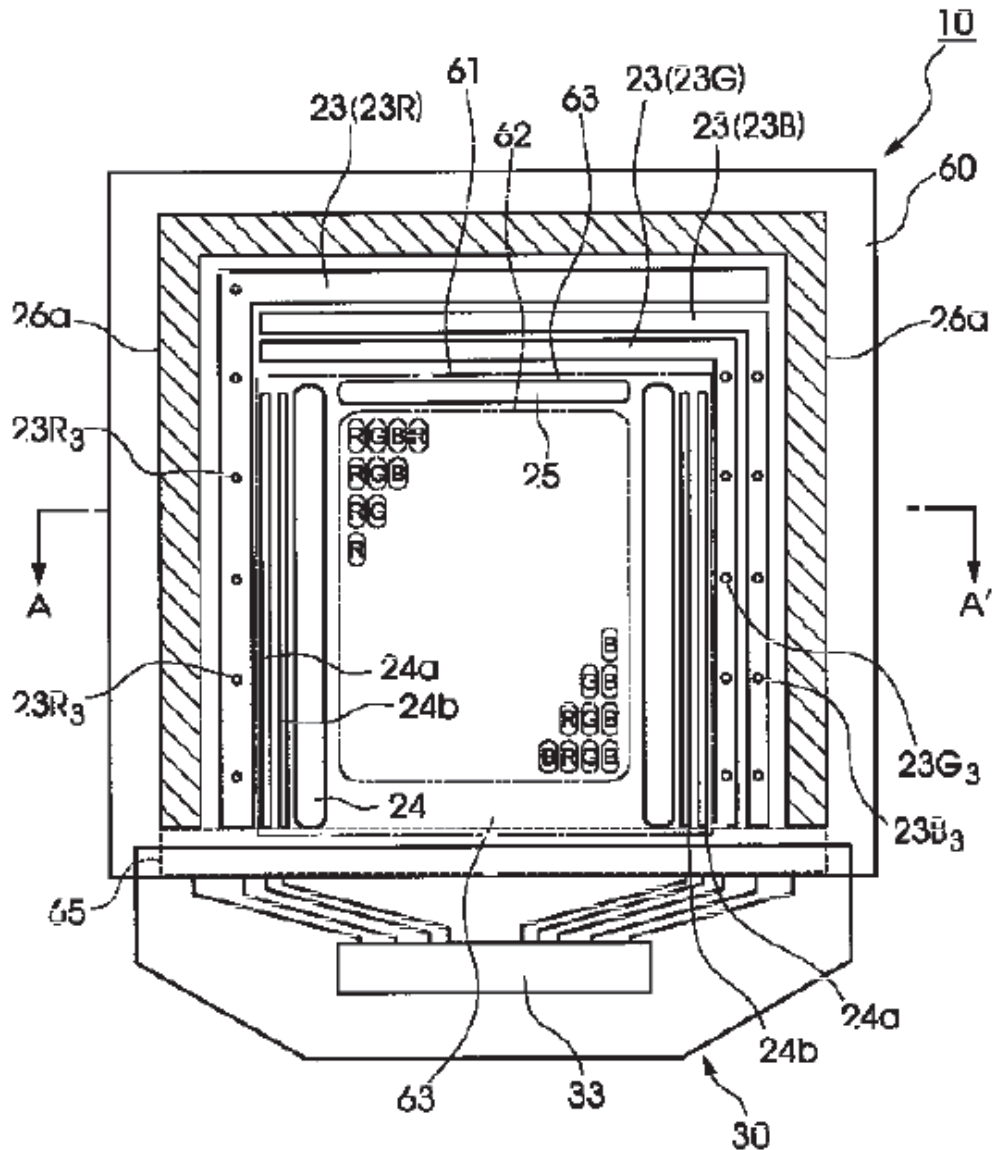


“In the bonded portion 65, as shown in FIG. 6, a first external connection terminal having a width equal to the width of the wiring is provided for each of the narrow

wiring lines, and a plurality of second external connection terminals having a width narrower than the width of the wiring are provided for the wide wiring lines. For example, a first external connection terminal 67, 68, 69 having a width equal to that of the scanning line drive circuit control signal wiring 24a is provided for each line of scanning line drive circuit control signal wiring 24a with a narrow line width. Meanwhile, second external connection terminals 66a, 66b, and 66c, which are narrower than the line width of the light emission power supply wiring 23R, are provided for the wide light emission power supply wiring 23R. In addition, a second external connection terminal 70 having a line width approximately equal to that of signal lines 22 is provided for each signal line 22, which is narrower than the scanning line drive circuit control signal wiring 24a. The number of the first external connection terminals and second external connection terminals is set based on the line width of the wiring formed on the substrate 60.” ¶[0053].

124. The “signal lines 22” are used in Figure 4, because Figure 4 shows “bonded portion 65” which is also depicted in greater detail in Figure 6 shown above. ¶¶[0052]-[0055].

【図4】



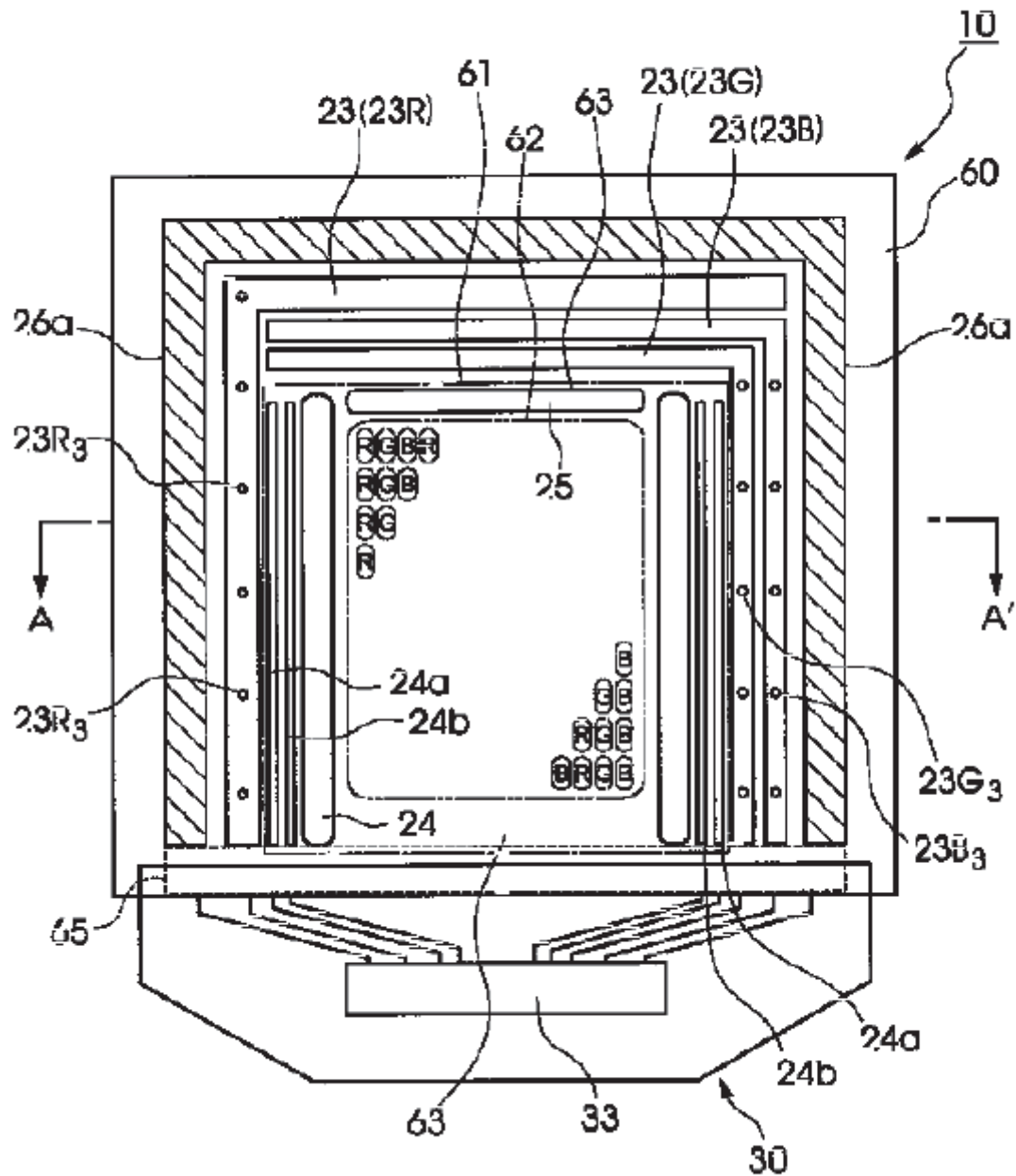
125. Nakanishi discloses scanning lines (*i.e.*, “scanning lines 21” in Figures 1 and 3) intersecting the data lines (*i.e.*, “signal lines 22”). “As shown in FIG. 3, this electro-optical device 10 comprises a plurality of scanning lines 21, a plurality of signal lines 22 extending in a direction intersecting the scanning lines 21, a

plurality of light emission power supply lines 23 extending parallel to the signal lines 22, and a pixel area A is provided at each intersection of a scanning line 21 and a signal line 22.” ¶[0023]. Scanning lines are also used in Figure 4, which depicts a “specific configuration of the electro-optical device 10 in the present embodiment.” ¶[0030]. And a POSITA would understand that specific configuration of Figure 4 necessarily uses scanning lines because “[s]can line drive circuits 24 are arranged on both sides of the actual display area 62 in the figure.” ¶[0032].

126. Nakanishi discloses pixels (*i.e.*, “areas A” in Figure 3) corresponding to intersections between the data lines and the scanning lines. “As shown in FIG. 3, this electro-optical device 10 comprises a plurality of scanning lines 21, a plurality of signal lines 22 extending in a direction intersecting the scanning lines 21, a plurality of light emission power supply lines 23 extending parallel to the signal lines 22, and a pixel area A is provided at each intersection of a scanning line 21 and a signal line 22.” ¶[0023].

127. The pixels are also shown in Figure 4 as “R,” “G,” and “B”:

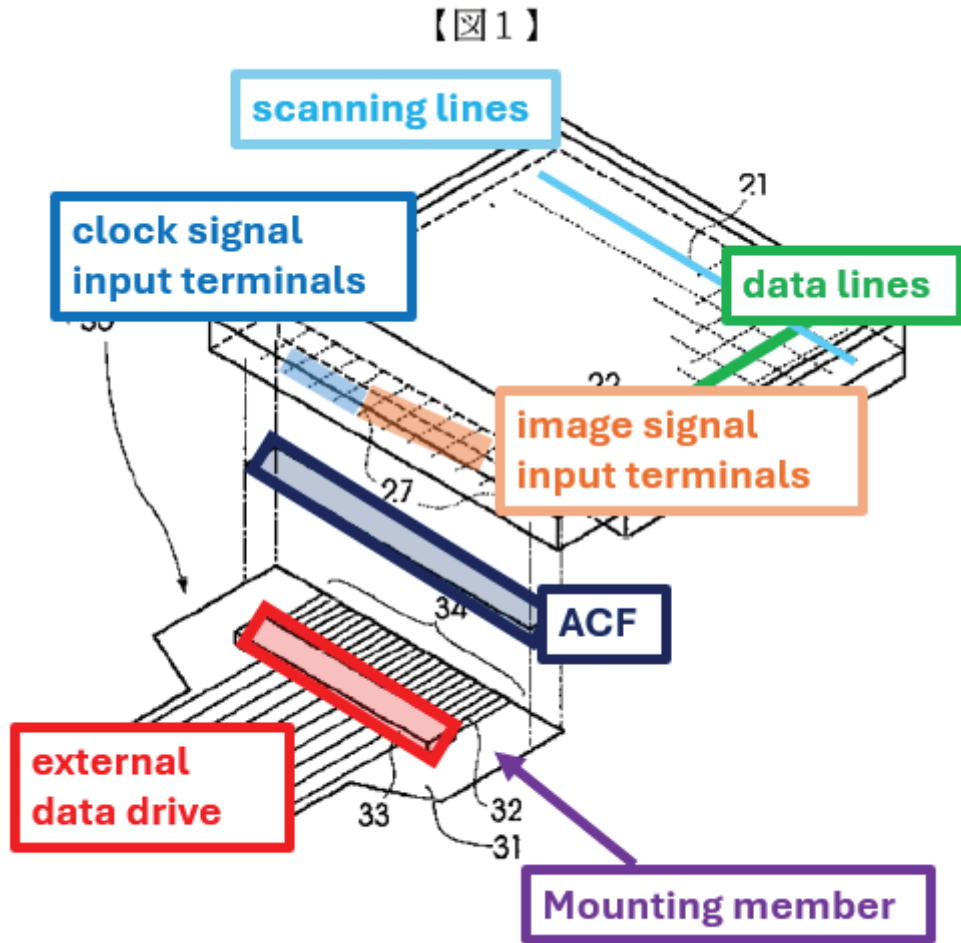
【图4】

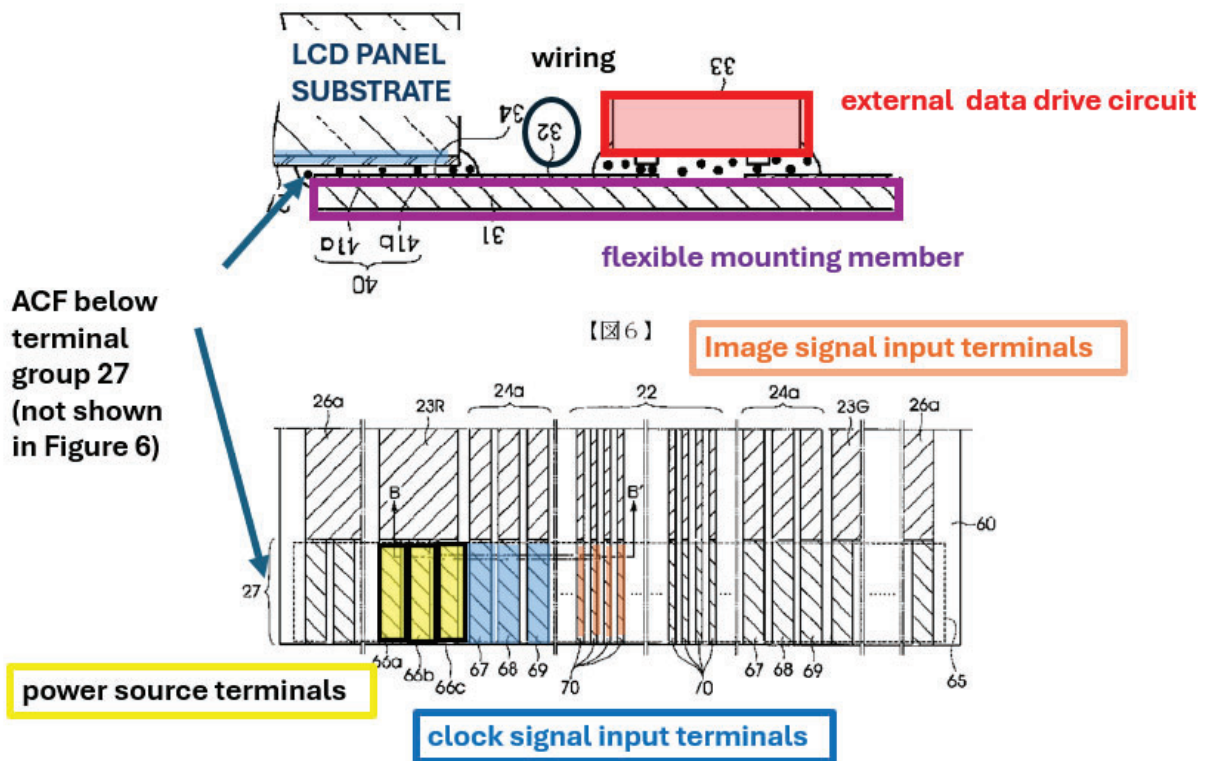


“The specific configuration of the electro-optical device 10 in the present embodiment will now be described with reference to FIG. 4 and FIG. 5.” ¶[0030].

“FIG. 4 is a plan view of the electro-optical device in the present embodiment, and FIG. 5 is a cross-sectional view along line A-A' in FIG. 4. As shown in FIG. 4, the electro-optical device 10 in the present embodiment is roughly composed of a substrate 60, a pixel electrode group area (not shown), light-emitting power supply lines 23 (23R, 23G, 23B), and a display pixel portion 61 (inside the single dotted-line box in the figure).” *Id.*

128. Nakanishi discloses input terminals (*i.e.*, “external connection terminals 27”). “Also, while not shown in FIG. 1, power supply lines and cathodes are also formed on the display substrate 20. In addition, external connection terminals 27 for the scanning lines 21, signal lines 22, power supply lines (not shown), and cathodes (not shown) are formed at one end of the display substrate 20.” ¶[0016]; *see also* ¶¶ [0017], [0019], [0020], [0022]. These input terminals are shown in at least Figures 1, 2, and 6:





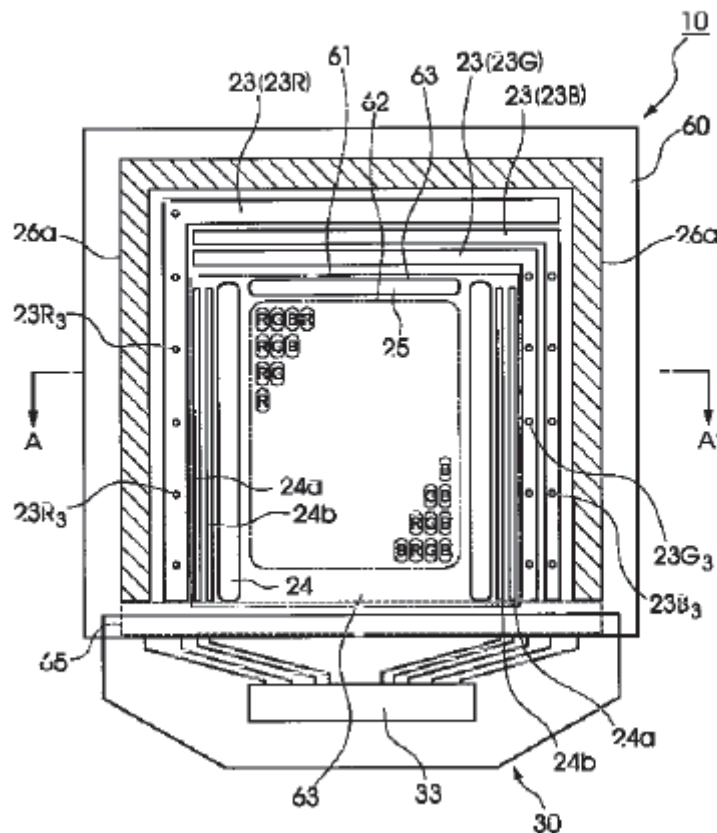
Ex. 1010, Figures 1, 2, 6.

129. Nakanishi discloses that input terminals 27 for the scanning lines are connected to a mounting member (*i.e.*, “flexible base substrate 31” (*see* ¶[0018]) shown in Figures 1 and 2) through anisotropic conductive film (*i.e.*, “anisotropic conductive film 40” shown in Figure 1). “As shown in FIG. 1, the intermediate substrate 30 is fixed to the display substrate 20 via an anisotropic conductive film 40. At this time, external connection terminals 34 on the intermediate substrate 30 are electrically connected to external connection terminals 27 on the display substrate 20 via the anisotropic conductive film 40. This anisotropic conductive film 40 is a conductive polymer film used to electrically connect pairs of terminals

in an anisotropic manner and is formed, for example, by dispersing a plurality of conductive particles 41b in a thermoplastic or thermosetting adhesive resin 41a, as shown in FIG. 2.” ¶[0019].

130. Figure 4 depicts a “specific configuration of the electro-optical device 10” of the “embodiment” disclosed in Figures 1-3 discussed above. ¶[0030].

【図4】



“Also, as shown in FIG. 4, the intermediate substrate 30 is bonded to one end of the substrate 60 using the anisotropic conductive film 40 described above. The semiconductor chips 33 mounted on the intermediate substrate 30 include the data

drive circuits 33a, cathode power supply circuits 33b, and light-emitting power supply circuits 33c shown in FIG. 3. The portion surrounded by dashed lines in FIG. 4 indicate the bonded portion between the display substrate 20 and the intermediate substrate 30. FIG. 6 is a top view of the bonded portion 65 shown in FIG. 4. In FIG. 6, the anisotropic conductive film 40 and the intermediate substrate 30 are omitted from the drawing.” ¶[0052].

131. “In the bonded portion 65, as shown in FIG. 6, a first external connection terminal having a width equal to the width of the wiring is provided for each of the narrow wiring lines, and a plurality of second external connection terminals having a width narrower than the width of the wiring are provided for the wide wiring lines.” ¶[0053]. “For example, a first external connection terminal 67, 68, 69 having a width equal to that of the scanning line drive circuit control signal wiring 24a is provided for each line of scanning line drive circuit control signal wiring 24a with a narrow line width.” *Id.* “Meanwhile, second external connection terminals 66a, 66b, and 66c, which are narrower than the line width of the light emission power supply wiring 23R, are provided for the wide light emission power supply wiring 23R.” *Id.* “In addition, a second external connection terminal 70 having a line width approximately equal to that of signal lines 22 is provided for each signal line 22, which is narrower than the scanning line drive circuit control signal wiring 24a.” *Id.* “The number of the first external

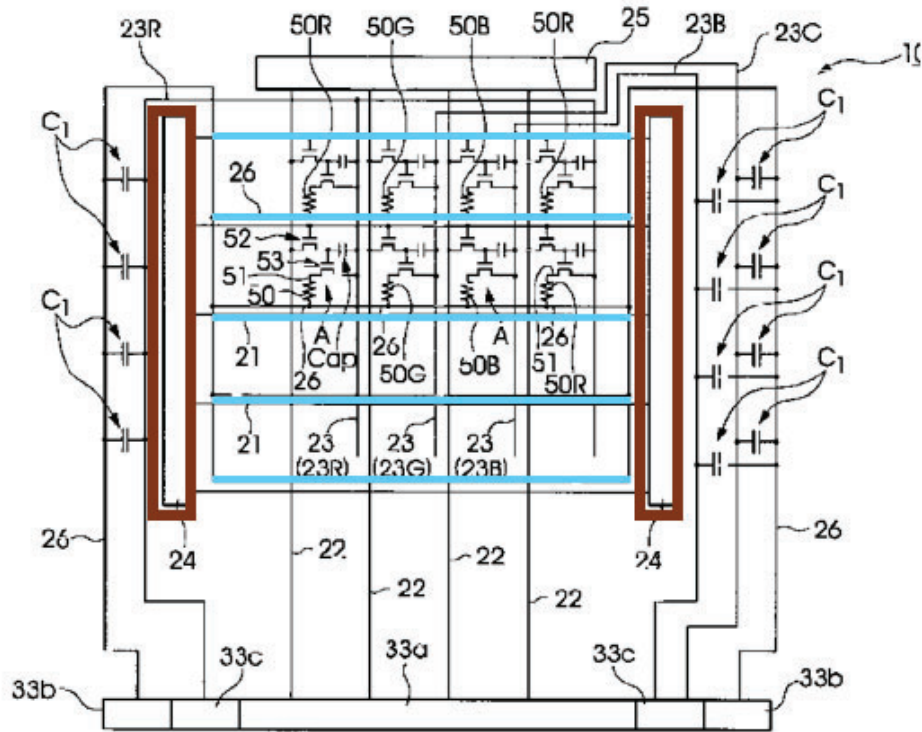
connection terminals and second external connection terminals is set based on the line width of the wiring formed on the substrate 60.” *Id.*

132. Moreover, the ’146 patent admits that electro-optical apparatuses similar to those recited in the claims were “known” (Ex. 1001, 1:17-62) and admits that “means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known (for example, Japanese Patent No. 2822558)” (*id.* at 1:51-62).

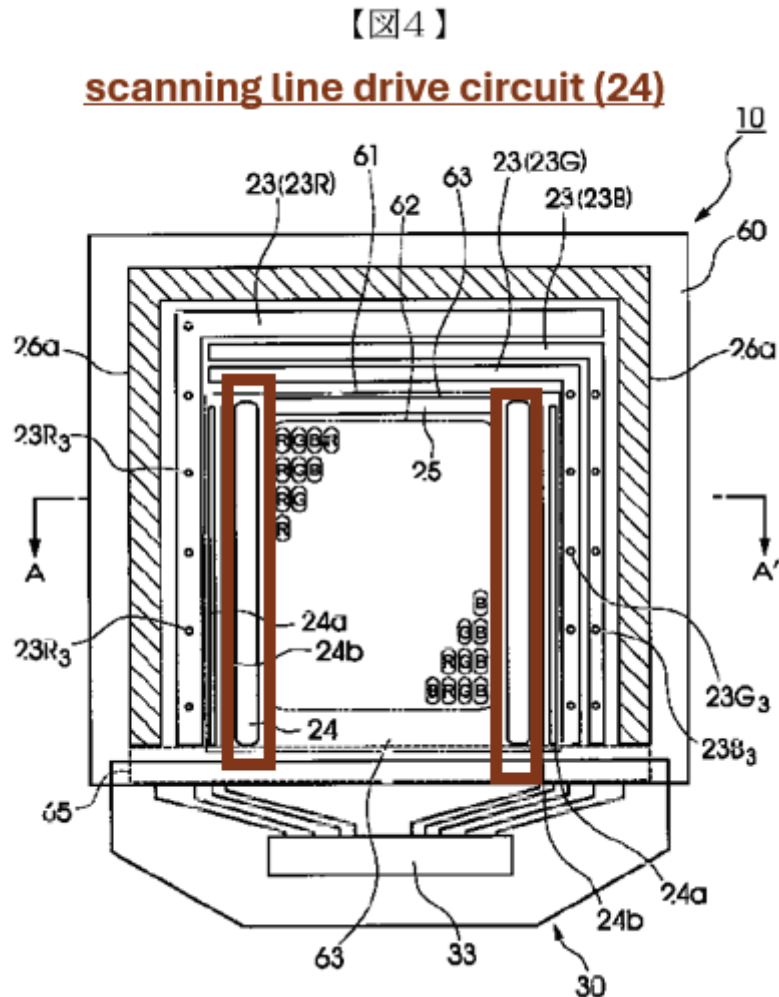
133. However, Nakanishi does not expressly disclose a “clock” signal input terminal supplied with a clock signal, but this is implied. In Nakanishi, “each scanning line 21 is connected to a scanning drive circuit 24 equipped with a shift register and a level shifter.” ¶[0024]; *see* Figures 3 and 6:

【図3】

scanning line drive circuit (24)



scanning lines (21)



“Scan line drive circuits 24 are arranged on both sides of the actual display area 62 in the figure. These scan line drive circuits 24 are located on the lower layer side (substrate 60 side) of the dummy area 63. Provided on the lower layer side of the dummy area 63 are scan line drive circuit control signal wiring 24a and scan line drive circuit power supply wiring 24b connected to a scan line drive circuit 24.”

¶[0032].

134. At the time of the invention, a POSITA would have appreciated that a clock signal could be beneficially used to control the scanning-line drive circuit,

for example, to cause it to sequentially transmit a transmission start pulse in synchronization with the clock signal (as specifically motivated and taught by other prior art references discussed below).

135. Nakanishi also discloses image-signal input terminals (*i.e.*, terminals 70 in Figure 6) supplied with image signals and connected to the mounting member through ACF. As discussed previously, Nakanishi discloses “external connection terminals 27.” ¶¶[0016], [0017], [0019], [0020], [0022]. These terminals are shown in at least Figures 1, 2, and 6 (shown above). Nakanishi discloses image signals being supplied to a plurality of data lines (*i.e.*, “signal lines 22” in at least Figures 1, 3, and 6). *See* ¶[0025]. Nakanishi discloses an external drive circuit (*i.e.*, “semiconductor chips 33”) that supplies the image signals. ¶[0018] (“The intermediate substrate 30 has wiring 32 formed on a flexible base substrate 31 and has semiconductor chips 33 mounted at predetermined positions on the intermediate substrate 30.). “Each of the pixel areas A is provided with a switching thin-film transistor 52, holding capacitance Cap, a current thin-film transistor 53, a pixel electrode 51, light-emitting layers 50, and a cathode 26. The switching thin film transistor 52 has a gate electrode connected to a scanning line 21 and is turned ON/OFF in response to scanning signals supplied from scanning line 21. The holding capacitance Cap holds an image signal supplied from the signal line 22 via the switching thin-film transistor 52.” ¶[0025]; [0024] (“Each

signal line 22 is connected to a data drive circuit 33a equipped with a shift register, a level shifter, a video line, and an analog switch.”).

136. Nakanishi discloses a scanning line drive circuit (*i.e.*, “24” shown in Figures 3 and 4) that is formed on the first substrate (*i.e.*, substrate 60 in Figure 4). “Furthermore, scanning line driving circuits 24 are arranged on both sides of the actual display area 62 in the figure. The scanning line driving circuit 24 is disposed below the dummy region 63 (on the substrate 60 side).” ¶[0032]. As I discussed previously in §VI.D.2, a POSITA at the time of the invention knew that it was much easier to form a scanning line drive circuit on an LCD panel’s substrate than it was to form a data line drive circuit there; data line drive circuits were conventionally located externally to the LCD substrate, on a mounting member connected to the LCD panel’s input terminals with ACF.

137. Similar to Minami and Sano discussed previously, Nakanishi’s wider terminals overlap wiring in a mounting member (*e.g.*, flexible printed circuit) through ACF by a larger area than the narrower terminals overlap their wiring through the ACF. *See* Figures 1, 2 and 6 (shown above); *see also* Ex. 1010 at ¶[0013] (“The electro-optical device according to the first aspect is also characterized in that the widths of the second external connection terminals are substantially equal. In this aspect of the present invention, since the widths of the second external connection terminals are set to be approximately equal, the

pressure conditions, such as the amount of pressure applied when fixing the wired substrate to the display substrate and establishing electrical connections, can be set to a more preferable state. The electro-optical device according to the first aspect is also characterized in that first intermediate wiring having a width equal to that of the first wiring and second intermediate wiring having a width equal to that of the second wiring are formed, and an intermediate substrate is provided in which the first wiring and the first intermediate wiring are electrically connected via a first external connection terminal, and the second wiring and the second intermediate wiring are electrically connected via a second external connection terminal. In order to solve the problem, a second aspect of the present invention is an electro-optical device comprising a plurality of light-emitting elements and switching elements that supply current to each of the light-emitting elements via a power supply line in response to signals supplied via a signal line, the electro-optical device characterized in that the width of the power supply lines is wider than the width of the signal lines, and a plurality of first external connection terminals are provided for the power supply lines. In this aspect of the present invention, a plurality of external connection terminals are provided for power supply lines that have been formed with an increased width due to the need to supply a large current to obtain light emission from light-emitting elements, even when mixed with thinner and narrower pitch signal lines to supply numerous signals. As a result, the

pressure conditions, such as the amount of pressure applied to fix the wired substrate to the display substrate and ensure electrical connections, can be made more uniform. This eliminates electrical resistance unevenness in the bonded portion, thereby preventing display defects such as display unevenness and contrast degradation caused by electrical resistance unevenness in the bonded portion.”).

138. And like the teachings of Minami, Nakanishi discloses that using larger area clock input terminals and power source terminals, nearer to the ends of the substrate (Ex. 1010, ¶¶[0052], [0053]), makes “the pressure application conditions as uniform as possible over the entire surface of the bonded portion.” ¶[0054]. This “eliminates electrical resistance unevenness in the bonded portion, thereby preventing display defects such as display unevenness and contrast degradation caused by electrical resistance unevenness in the bonded portion.” ¶[0013].

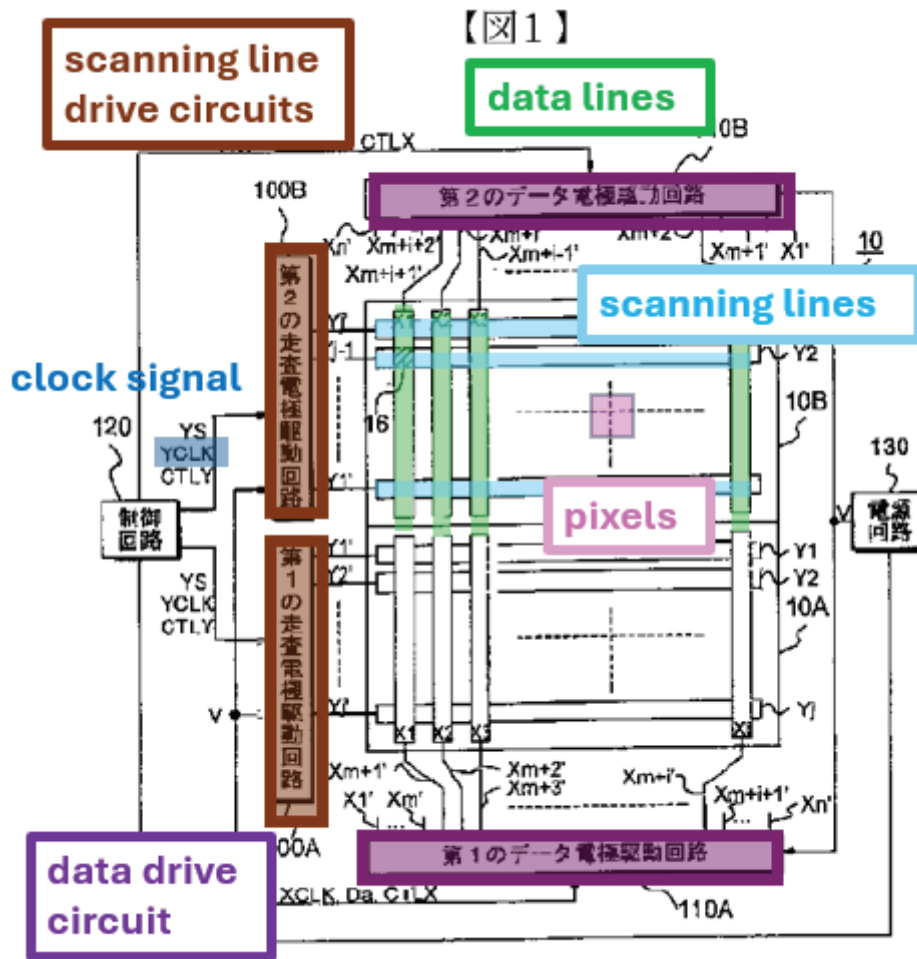
139. Thus, Nakanishi independently motivates and renders obvious claim elements [10j], [23l], [1h], [1i], and [1l].

140. Finally, I note that Nakanishi (referred to as “Hayoto” by the examiner) was discussed in prosecution, but only to a limited extent. The examiner cited Nakanishi’s ¶[0009], finding “Hayato teaches the power source terminal are formed wider than the scanning lines and signal lines.” Ex. 1003 at Nov. 2, 2007 Office Action. The applicant argued that ¶[0009] “discloses power

source wiring that is formed broader than a scan line and a signal line” but “does not suggest the forming of a power source terminal with a larger area.” *Id.* at January 31, 2008 Response (emphasis added). In my opinion, the examiner overlooked Nakanishi’s Figure 6 and the description thereof, which discloses and motivates larger area power source input terminals (66a, 66b, 66c) and clock signal input terminals (67, 68, 69) outside of smaller area image signal input terminals (70). Ex. 1010, Figure 6 and ¶¶[0052]-[0053].

H. Kawaguchi (Ex. 1005)

141. Kawaguchi also discloses the conventional technology recited in the challenged claims:



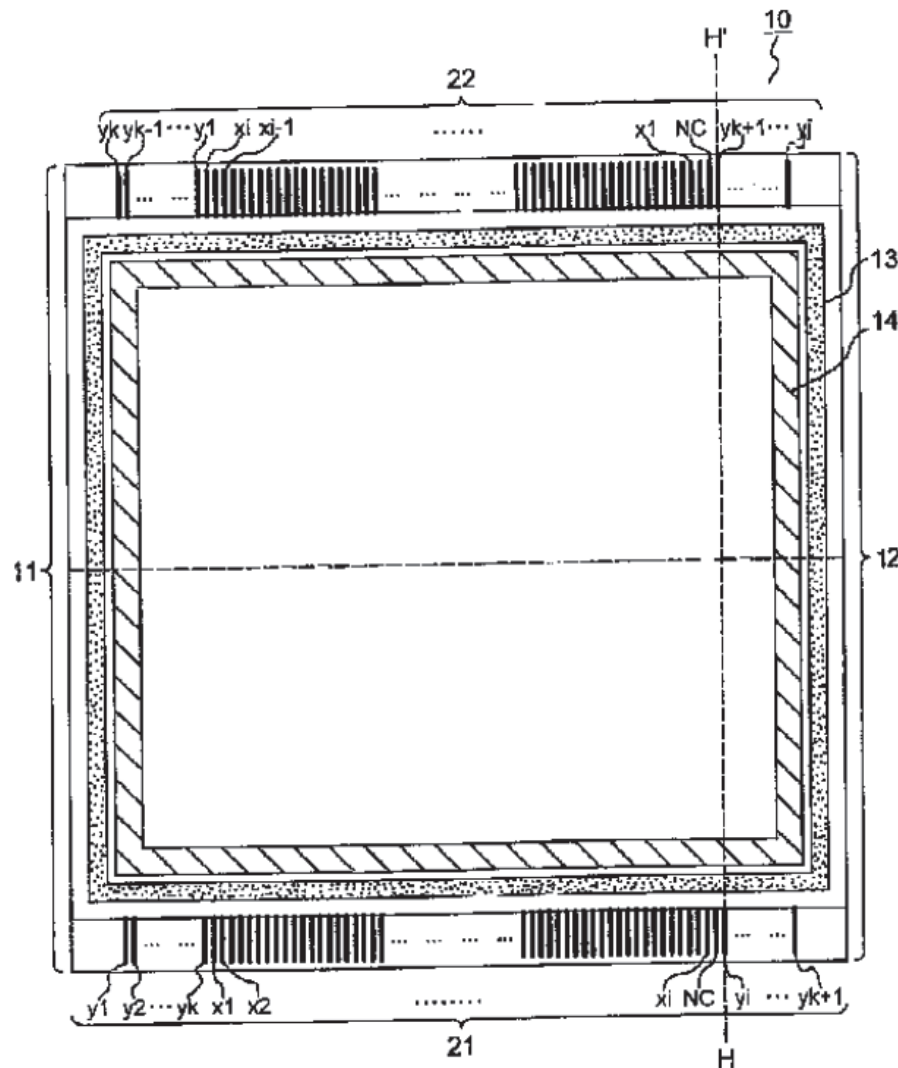
Ex. 1005, Figure 1.

142. Kawaguchi discloses an electro-optical panel (*i.e.*, “first panel (first screen) 10A” and “second panel (second screen) 10B” are electro-optical panels, each of which separately discloses the preamble); *see* Ex. 1005, ¶[0027]; ¶[0001] (“The present invention relates to an implementation structure suitable for a panel comprising two screens, an electro-optical device, an electronic apparatus, and a method for connecting a driving IC (Integrated Circuit).”).

143. Figure 1 (shown above) “is a block diagram showing the general configuration of key components of a liquid crystal display device according to the first embodiment.” Ex. 1005, ¶[0025]. “As shown in the figure, the liquid crystal display device is generally composed of: a passive matrix-type liquid crystal display panel 10, first and second scan electrode drive circuits 100A and 100B, first and second data electrode drive circuits 110A and 110B, a control circuit 120, and a power supply circuit 130.” ¶[0026]. “First, the liquid crystal display panel 10 comprises a first panel (first screen) 10A and a second panel (second screen) 10B. Each panel includes *i* data electrodes (segment electrodes) X1 to Xi and *j* scan electrodes (common electrodes) Y1 to Yj. At each intersection of the data electrodes X1–Xi and the scan electrodes Y1–Yj, a pixel region 16 is formed. Each pixel region 16 consists of a liquid crystal display element (a liquid crystal layer 18 to be described later).” ¶[0027]; ¶[0085] (“Also, in the above embodiments, the liquid crystal display panel 10 was explained as an example of a passive matrix type that includes scan and data electrodes. However, the invention is not limited to this; it can of course be applied to an active matrix-type liquid crystal display panel as well.”); ¶¶[0086]–[0087].

144. Kawaguchi discloses a first substrate (*i.e.*, substrate 11 in Figure 2):

【図2】



“As shown in the figure, the liquid crystal display panel 10 includes a substrate 11 and a counter substrate 12 that is shorter in the vertical direction than the substrate 11. The substrate 11 and counter substrate 12 are made of, for example, glass or plastic. On the substrate 11, a sealing section 13 is provided along its edges, and inside this, a light-shielding film 14 is formed to surround the non-display region

around the display region in parallel. As for the sealing section 13, an ultraviolet-curable adhesive or a thermosetting adhesive containing anisotropic conductive microparticles is used. Liquid crystal is injected into the inside of the sealing section 13, thereby forming a liquid crystal layer 18.” Ex. 1005, ¶[0041].

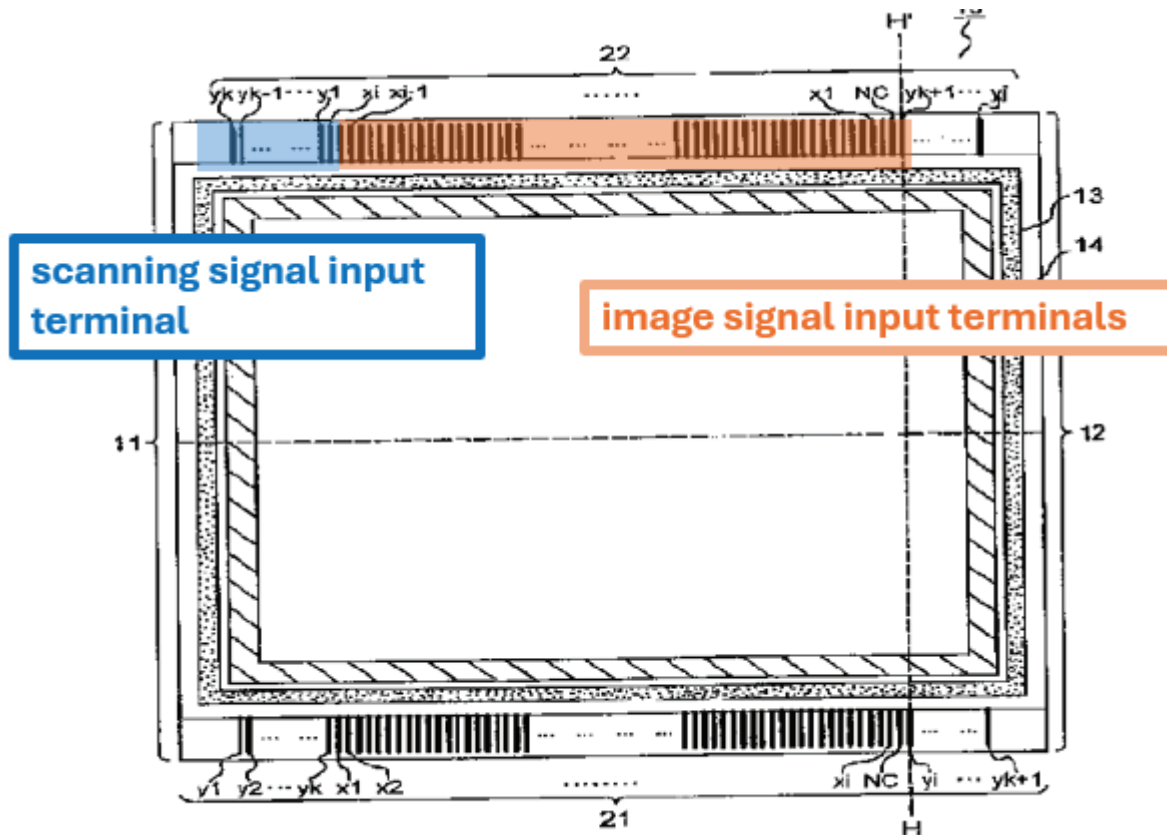
145. And as shown above in Figure 1, each screen 10A and 10B has data lines (*i.e.*, data electrodes X1 to Xi). And each screen 10A and 10B has scanning lines intersecting the data lines (*i.e.*, scanning electrodes Y1 to Yj intersect data electrodes X1 to Xi in Figure 1). *See* ¶[0027]. And screens 10A and 10B have pixels disposed corresponding to intersections between the screen’s data lines and its scanning lines. *See* ¶[0027]. Kawaguchi discloses both “passive matrix type” and “active matrix type” LCD devices, both of which have data lines. *See* ¶¶[0083]; [0085]-[0087].

146. Kawaguchi discloses that each screen 10A and 10B is supplied a clock signal (*i.e.*, “YCLK” from control circuit 120 as shown in Figure 1). “Next, the first and second scan electrode drive circuits 100A and 100B include so-called bidirectional shift registers. Based on the power supply voltage V, Y shift start pulse YS, Y shift clock YCLK, and control signal CTLY, these bidirectional shift registers generate scan signals with a specified pulse width and timing. The scan signals are supplied sequentially line-by-line to the scan electrodes Y1, Y2, ..., Yj.” Ex. 1005, ¶[0032]. “At this time, the shift register starts shifting in response to the

Y shift start pulse YS supplied every vertical scanning period and performs shifting operations in synchronization with the Y shift clock YCLK supplied every horizontal scanning period. As the shifting proceeds, the scan signals are sequentially generated in each horizontal scanning period.” ¶[0033]. “Therefore, the first and second scan electrode drive circuits 100A and 100B can fix the transfer direction (scan direction of the electrodes) of the above-mentioned bidirectional shift register to either the forward or reverse direction, based on the transfer direction control signal included in the control signal CTLY. As a result, scan signals can be output to the output terminals Y1', Y2', ..., Yj' either in top-to-bottom order (forward direction) or in bottom-to-top order (reverse direction).” ¶[0034].

147. Kawaguchi discloses that scan electrode driving circuits 100A and 100B (which are supplied with the clock signal as discussed above) have input terminals. *See* Ex. 1005, ¶[0042] (“Furthermore, at the lower edge of the substrate 11, an input terminal group 21 for the first panel 10A is provided, while at the upper edge of the substrate 11, an input terminal group 22 for the second panel 10B is provided. The input terminal group 21 includes: – Input terminals y1 to yk and input terminals yk+1 to yj, connected respectively to the scanning electrodes Y1 to Yk and Yk+1 to Yj of the first panel 10A, – Input terminals x1 to xi, connected respectively to the data electrodes X1 to Xi of the first panel 10A, and –

An input terminal NC that is adjacent to terminal x_i but not connected to any scanning or data electrode.”); *also* ¶¶[0043]-[0045]; Figures 3 and 4.



148. Kawaguchi discloses that the scan electrode driving circuits 100A and 100B (*see* Figure 1) are implemented in a respective external driver IC 311 which is part of a respective (TCP 31 and 32 are identical); *see* Figures 6, 7; ¶¶[0029], [0048]-[0055], [0050] (“As shown in the figures, the first TCP 31 is roughly composed of a driver IC 311 and a substrate 313. This driver IC 311 contains the first scanning electrode driving circuit 100A and the first data electrode driving

circuit 110A shown in Figure 1. Its input and output terminals are formed by gold bumps 312 protruding from the bottom surface of the driver IC 311.”).

149. It would have also been obvious to form Kawaguchi’s scanning line drive circuits (100A, 100B) directly on substrate 11 instead of in external driver IC 311, as expressly taught and motivated by Matsumoto—“the peripheral drive circuitry can be integrated on the same substrate as that for the FET array for the display, which simplifies the connection between the drive circuit and the display.” Matsumoto at page 52 of 85. Sano also expressly motivates a POSITA to place the scanning line drive circuit on the substrate instead of using the TCP method of Kawaguchi because it “simplifies the manufacturing process.” Sano, ¶[0002]. *See* [10 i], *infra* (incorporated by reference). This implementation would necessarily include a clock signal input terminal (*e.g.*, ‘y’ terminals in Kawaguchi Figure 2) to receive the clock signal from control circuit 120 as shown in Kawaguchi’s Figure 1. *See* ¶¶[0026], [0032]-[0038]. Sano also expressly teaches that LCD devices have input clock terminals. Sano at ¶[0018] (“Additionally, even if the external connection terminals are prone to malfunction due to waveform distortion caused by connection resistance through a uniaxial conductive rubber connector—particularly in terminals transmitting high-frequency signals such as clock signals—the invention allows the connection resistance at those terminals to be reduced. As a result, malfunctions of the liquid crystal panel driving circuit can be

effectively prevented, thereby improving the reliability of the device.”). As I explained above in §VI.D.2, a POSITA knew at the time of the invention that it was relatively easy to place the scan line driver on the substrate instead of using an external scan line driver.

150. Figure 5 of the ’146 patent discloses an external “power source circuit” (500), an external “data-line drive circuit” (200), an external “image processing circuit” (400), and an external “timing generation circuit” (300). These components are situated on an external substrate (C) and connected to the LCD panel (AA) by a flexible substrate (B). *See* Ex. 1001, Figure 5, 9:40-55. The ’146 patent also refers to the external substrate and the flexible substrate as a “mounting member.” *Id.*, claim 16 (“the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.”).

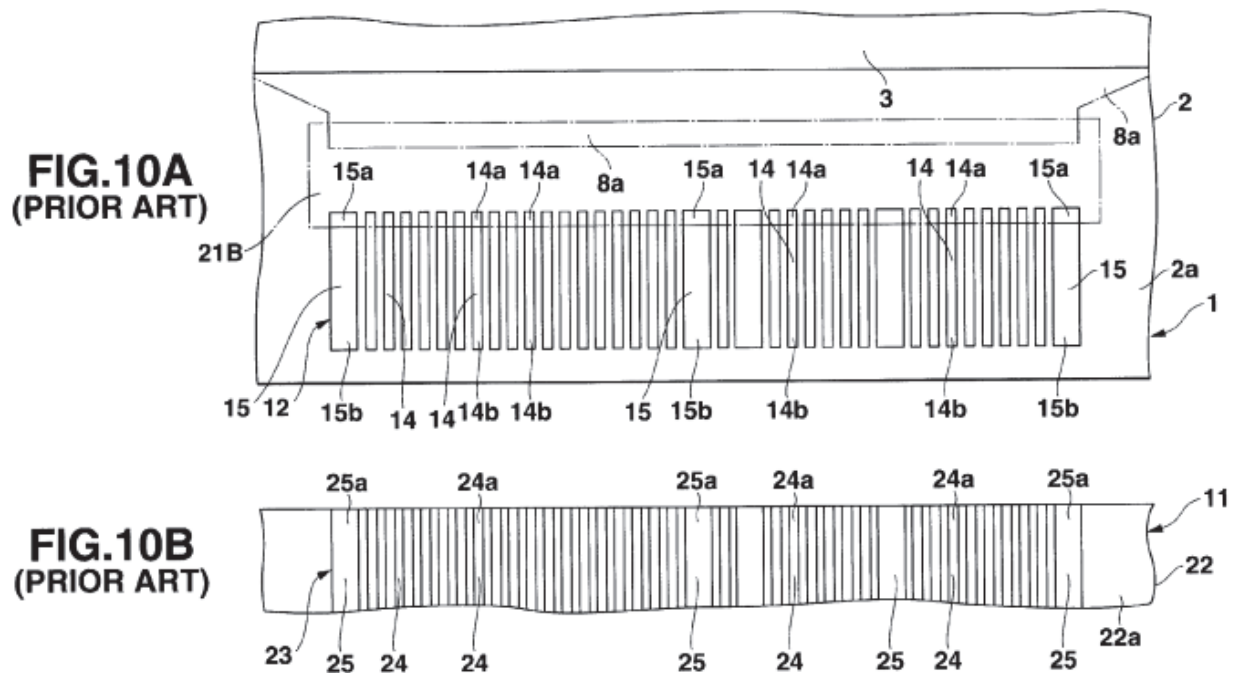
151. Similar to Figure 5 of the ’146 patent, Kawaguchi discloses an external TCP containing “data electrode driving circuit 110A” (Ex. 1005, ¶[0050]), and further discloses that the LCD device includes “a control circuit 120 [which supplies the clock signal], and a power supply circuit 130” which are shown in Figure 1. ¶[0026]. Figure 1 implies that control circuit 120 and the power supply circuit 130 are on an external substrate. A POSITA would have put these components on an external substrate because they are not optically transparent. Further, Kawaguchi teaches that each TCP includes a mounting member (*e.g.*,

substrate 313 shown in Figures 6 and 7; *see* ¶ [0051]) and that the mounting member is connected to terminals using ACF. ¶[0055]. Accordingly, Kawaguchi discloses and renders it obvious to put control circuit 120, which supplies the clock signal, on an external substrate, and to provide an electrical connection from control circuit 120 to the LCD device's clock signal input terminals through ACF. Kawaguchi expressly discloses connecting input terminals (which necessarily include clock signal input terminals to receive “YCLK” shown in Figure 1) to a mounting member through anisotropic conductive film (“ACF”). “The connection between the output terminal group 316 of the first TCP 31 and the input terminal group 21 of the first panel 10A is made using an anisotropic conductive film (ACF), which contains conductive microparticles in an adhesive.” ¶[0055].

152. Moreover, the '146 patent admits that electro-optical apparatuses similar to those recited in the claims were “known” (Ex. 1001, 1:17-62) and admits that “means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known (for example, Japanese Patent No. 2822558)” (*id.* at 1:51-62). These admissions show further that the claimed technology was conventional and within a POSITA's general knowledge.

I. Kato (Ex. 1009)

153. Kato teaches that power supply wiring in an LCD display must be “made wider than the signal input wire” in order “to reduce the wire resistance, because a larger current flows through the power supply wire than through the signal input wire.” Ex. 1009, ¶[0009]. The power supply input terminals (15b) therefore have a larger area than the image signal input terminals (14b), as shown in Figure 10A (illustrating input terminals on an LCD display panel (1)) and Figure 10B (illustrating wiring in a flexible wiring board (11) that is electrically connected to the input terminals of Figure 10A):



Ex. 1009, Figure 10 and ¶[0010]. A POSITA knew that power terminals conduct larger currents than clock signal input terminals, so it would have been obvious

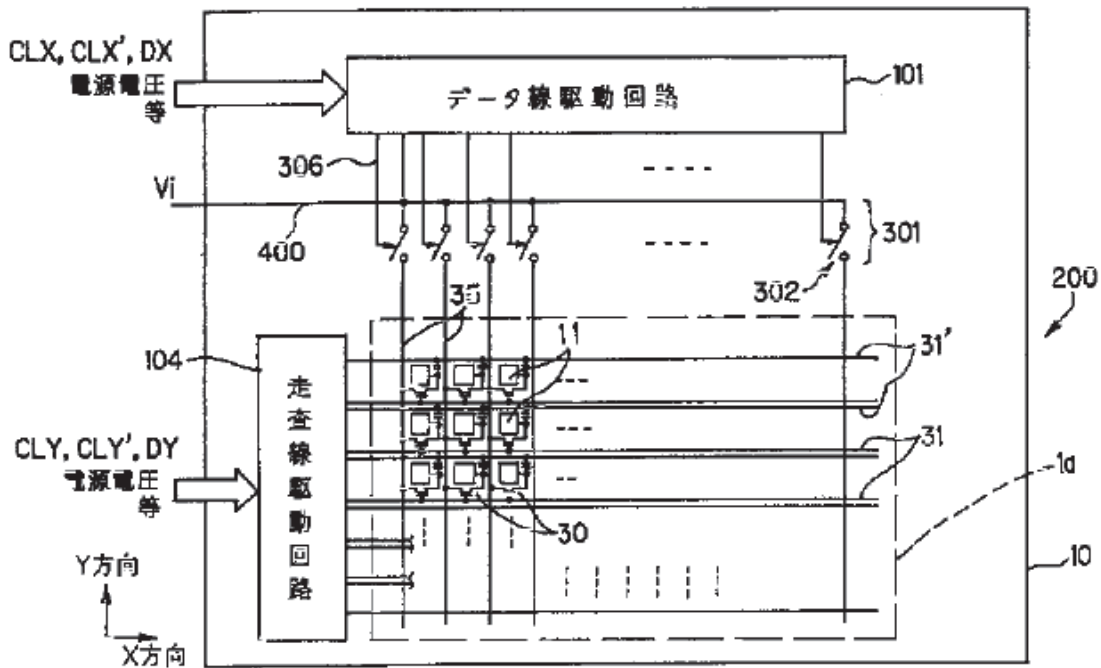
that the area of the power source terminals should be “not smaller than” than the clock input terminals’ area, as recited in [1h].

154. A POSITA knew that a high resistance power supply terminal would be problematic. First, the voltage drop is current times resistance (“IR drop”). Power supply signals use higher current than image signals, so the IR drop can be substantial. Any voltage drop at the terminal will be subtracted from the voltage intended to be delivered, thereby causing potential malfunctions in the LCD device. *See* Ex. 1011, ¶[0070] (“... the voltage drop at the upstream source driver ICs 20 becomes large because larger current flows through the power supply wiring line ...”). Second, currents in a terminal generate heat (with wattage of current squared times resistance), and an overheated terminal could cause damage. Kato teaches that a larger area power supply terminal has lower resistance, making this an obvious choice.

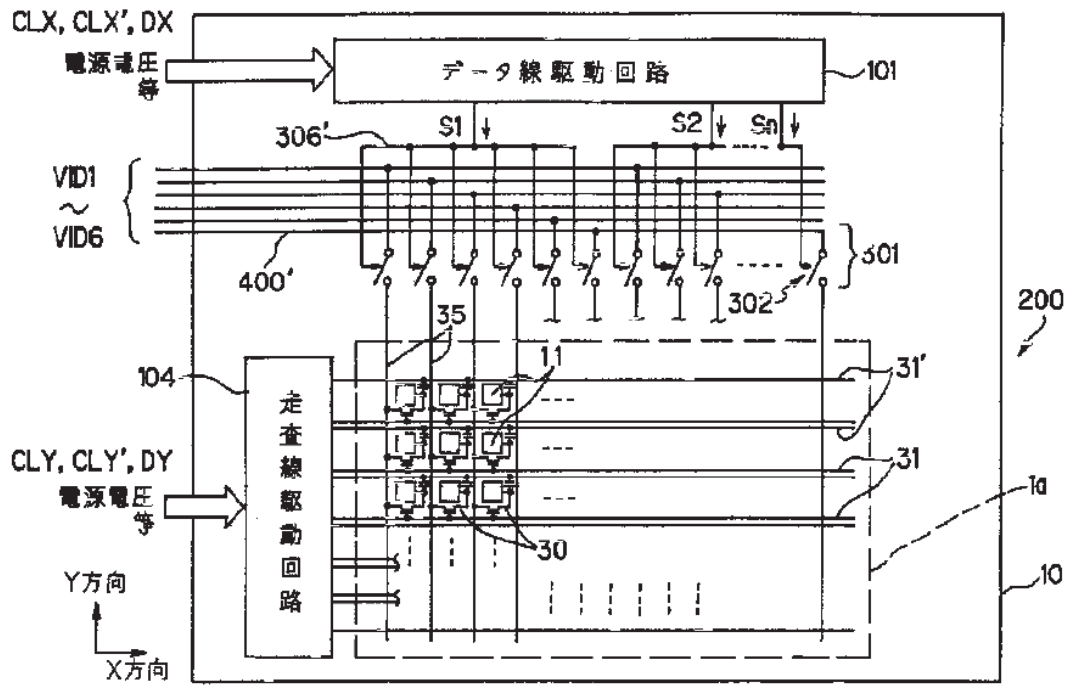
J. Shii (Ex. 1013)

155. Shii discloses an LCD display device similar to the devices of Kitawada, Yoshito, and Nakanishi, further underscoring that the claimed technology of the ’146 patent was conventional. Shii discloses an electro-optical panel (*i.e.*, LCD device 200 in Figures 1 and 6; the overall configuration of the embodiments of Figures 1 and 6 is shown in Figures 7 and 8).

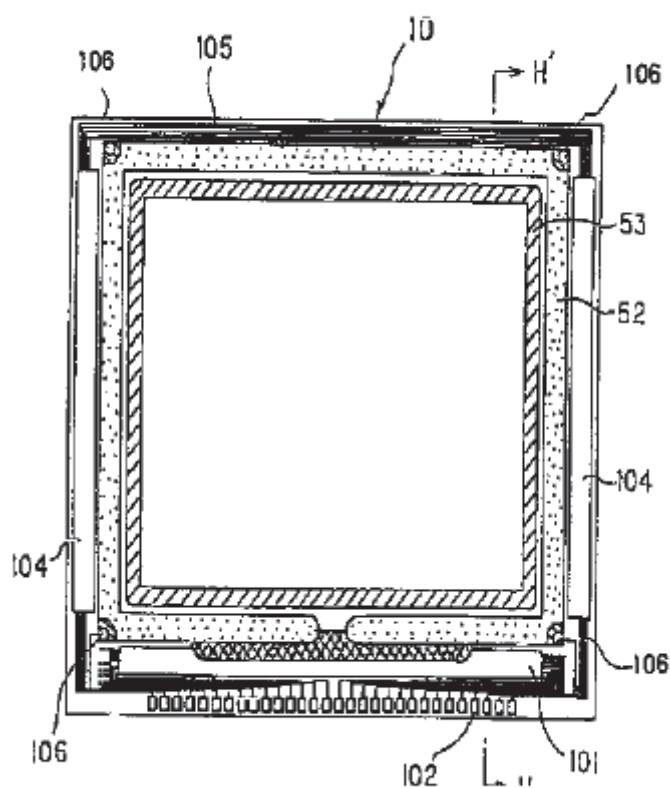
【図1】



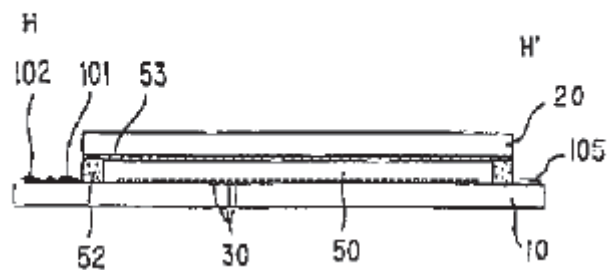
【図6】



【図7】



【図8】



“The present invention is included in the field of driving circuits for driving data lines in electro-optical devices such as liquid crystal devices of an active matrix

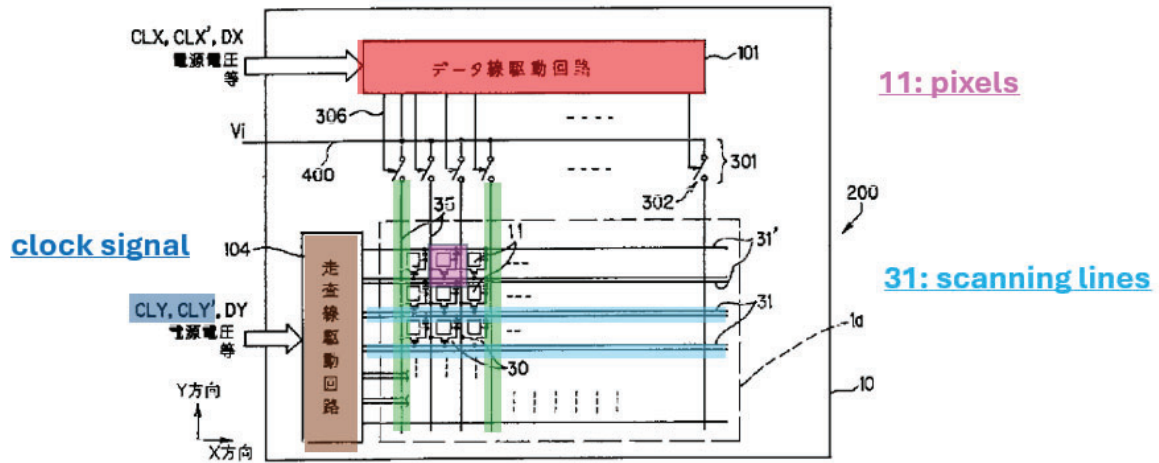
driving type through thin film transistor (which may be termed ‘TFT’ hereafter) driving, thin film diode (which may be termed "TFD" hereafter) driving, or the like, and to the technical field of electro-optical devices comprising such driving circuits.” Ex. 1013, ¶[0001]. “In FIG. 1, a liquid crystal device 200 is structured comprising a liquid crystal displaying portion 1a wherein a liquid crystal is filled between a pair of substrates, a data line driving circuit 101, a scan line driving circuit 104, and a sampling circuit 301.” Ex. 1013, ¶[0037]. “Overall structures for various embodiments of a liquid crystal device configured as described above will be explained in reference to FIG. 7 and FIG. 8. Note that FIG. 7 is a plan view of a TFT array substrate 10 and the various structural elements formed thereon when viewed from the opposing substrate 20 side, and FIG. 8 is a cross-sectional drawing along the section H-H' of FIG. 7, shown including the opposing substrate 20.” Ex. 1013, ¶[0066]; ¶[0061] (“A third embodiment will be explained next in reference to FIG. 6. Here FIG. 6 is an overall block diagram of a liquid crystal device, as an example of an electro-optical device, with the driving circuit provided on the same substrate.”); ¶[0062]-[0063].

156. Shii discloses “data lines 35” and “scanning lines 31” with “pixel electrodes 11” arrange in a “matrix”:

101: data drive circuit

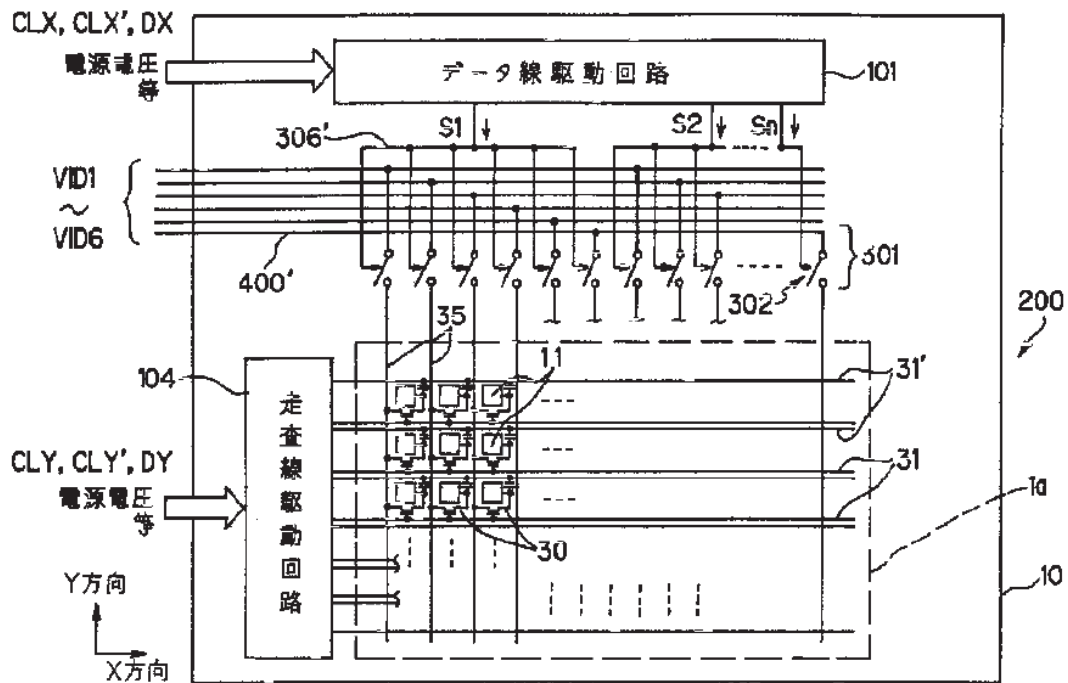
【図1】

35: data lines



104: scanning line drive circuit

【図6】



“These driving circuits, and the like, are provided in a peripheral region positioned at the periphery of a TFT array substrate 10 comprising, for example, quartz glass, hard glass, a silicon substrate, or the like. A plurality of pixel electrodes 11, provided in the form of a matrix, respective data lines 35 (source electrode lines) laid out in a plurality in the X direction and extending in the Y direction, a plurality of scan lines 31 (gate electrode lines) laid out in a plurality in the Y direction and extending in the X direction, a plurality of TFTs 30, interposed between each of the data lines 35 and pixel electrodes 11, for controlling respectively, in response to scan signals supplied through the respective scan lines 31, the conductive state or nonconductive state between each of the data lines 35 and pixel electrodes 11, and a liquid crystal displaying portion 1a are structured in a screen display region that is positioned in the center of the TFT array substrate 10. Additionally, capacitance lines 31' (power storage capacitance electrodes) that are interconnections for storage capacitors to maintain the voltages that are applied to the pixel electrodes 11 are formed in parallel with the scan lines 31 on the TFT array substrate 10.” Ex. 1013, ¶[0038].

157. Shii discloses a clock signal (“CLY”) supplied to the scanning line driving circuit 104. The “scanning line driving circuit 104 is configured to sequentially apply scanning signals to a plurality of scanning lines 31 based on a Y-side clock signal CLY (and its inverted clock CLY'), which is a reference clock

for applying the scanning signals, in order to perform vertical scanning in a direction perpendicular to the scanning lines 31 (Y direction) using data signals and scanning signals in the liquid crystal display section 1a consisting of a plurality of pixel sections arranged in a matrix.” Ex. 1013, ¶[0040].

158. Figure 7 shows “packaging terminals 102,” and it is apparent to a POSITA that these could function as clock signal input terminals, image signal input terminals, power source terminals, and the like. “The data line driving circuit 101 and packaging terminals 102 are provided along one edge of the TFT array substrates 10 in a region to the outside of the seal member 52, and a scan line driving circuit 104 is provided along the two edges that are adjacent to this one edge, in the peripheral region.” Ex. 1013, ¶[0067].

159. Shii teaches use of “TAB (tape automated bonding) packaging technology” to connect external components to the substrate’s input terminals. *See* Ex. 1013, ¶[0071] (“Furthermore, in each of the embodiments set forth above, a liquid crystal device with built-in driving circuitry may be achieved through forming the scan line driving circuit and data line driving circuit on the substrate. The data line driving circuit (and scan line driving circuit), having the features as described above, may be structured through application to the substrate using a TAB (Tape Automated Bonding) packaging technology”). Kang (Ex. 1017) explains that “Liquid crystal displays (LCD) have been a major application of TAB

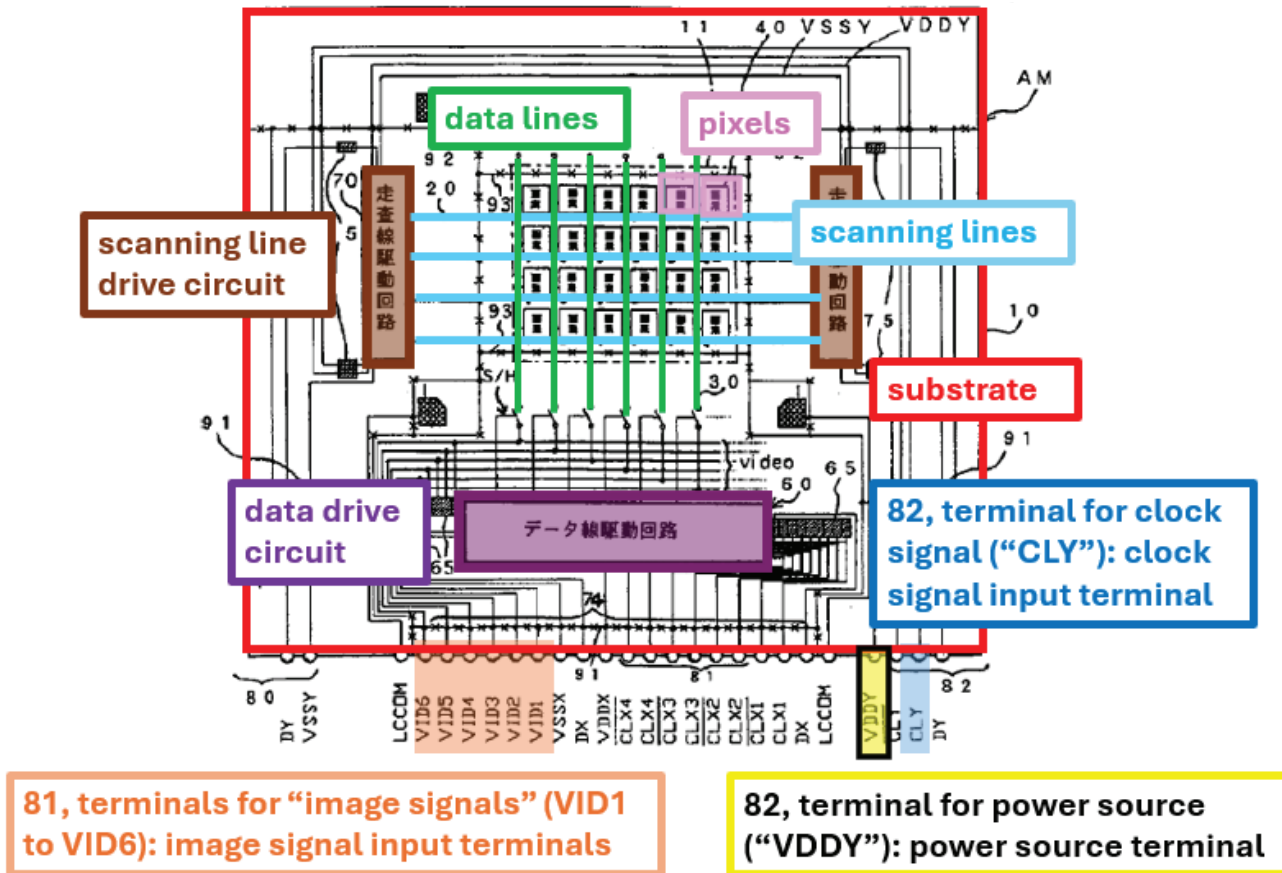
technology, especially in Japan (O'Mara 1993), because the technology provides a low profile, foldable, low cost interconnection between a LCD flat panel and its control printed circuit board (PCB). In this application, a driver chip is mounted on a flexible TAB tape, which connects a liquid crystal glass panel to a PCB. A transfer-bumped, tin-plated tape is commonly used with electroplated gold bumps attached to it. Anisotropic conductive film (ACF) is also used for the tape-to-glass connection to provide low-temperature, low-pressure bonding.” Ex. 1017 (first page, first column). As discussed previously, the ’146 patent admits that “means for supplying the power source, etc. to the electro optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known (for example, Japanese Patent No. 2822558).” Ex. 1001, 1:57-62.

160. Shii discloses and renders obvious image signal input terminals. Shii’s embodiment of Figure 6 is similar to its embodiment of Figure 1, but the Figure 6 embodiment uses “a plurality of image signal lines.” Ex. 1013, ¶[0062] (“When compared to the first embodiment, the third embodiment differs in the point that a phase-expanded image signal is supplied through a plurality of image signal lines, and the point that individual sampling circuit driving signals are supplied simultaneously to a plurality of sampling switches, to accommodate the phase expanded image signal, where the other structures are similar to those in the

first embodiment and explanations thereof will be omitted.”); ¶[0063]
(“Specifically, in FIG. 6 the image signals VID1 through VID6 are phase-expanded into six phases by an external image signal processing circuit, and are inputted into the sampling circuit 301 through six image signal lines 400'. The sampling circuit driving signals S_i ($i = 1, 2, 3, \dots$) that have the pulse widths thereof limited by the enable circuit in the data line driving circuit 101 are inputted into six adjacent sampling switches 302 through sampling circuit driving signal lines 306' that are each branched into six branches. Consequently, the sampling circuit 301 is driven simultaneously for each group of six sampling switches 302.”).

X. MOTIVATION TO COMBINE

161. The claims recite admittedly conventional technology that had been used for decades prior to the time of the alleged invention of the '146 patent, including a “substrate”; “pixels”; “data lines” and “data line drive” circuits; “scanning lines” and “scanning line drive” circuits; various signals with associated input terminals; and the admittedly “known” technique of connecting terminals to wiring through ACF. Kitawada discloses all of this plus clock signal, image signal, and power source terminals formed in a line along one side of an LCD panel's substrate (as recited in [1k], [10g], [23g], and claims 4 and 12):



Ex. 1004, Kitawada, Figure 2. While Kitawada may not expressly disclose larger area clock signal and power source terminals, the prior art discloses multiple, independent reasons for modifying Kitawada in this manner, rendering the challenged claims obvious (including elements [11], [10j], [23l], [1h], and [1i]).

162. **First**, Kitawada's clock signal and power source terminals are lined up on the edge of the substrate near the outer side of the terminal block, with the image signal input terminals near the center. Ex. 1004, Figure 2. Per the teachings of **Minami, Nakanishi, and Mismatch Analysis Report**, a POSITA would have been motivated to make the terminals on the outer side have a larger area to

mitigate known problems of weakened ACF bonding, outer terminal “mismatch,” and the like, rendering obvious elements [1i], [10j], and [23l].

163. Indeed, the ’146 patent inventor later realized that clock signal input terminals and power source terminals can be “disposed at the outer side of the substrate” where “heat and pressure are applied” when “connecting each terminal with ACF,” and he noted that “the outer side of ACF tends to have a larger extension rate than the central part.” Ex. 1001, 3:10-22. So, he adopted the *same* solution that Minami and Nakanishi disclosed previously, for the *same* reasons: “by disposing an input terminal having a wider area at a more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is a large one even if a slight misalignment of the connection arises.” *Id.*; 4:24-31.

164. **Second**, Sano independently motivates larger area clock input terminals, rendering obvious elements [1i], [10j], and [23l], because **Sano** teaches clock input terminals must transmit “high frequency” components to the scanning line driver with fidelity or else the LCD display will malfunction. Ex. 1006, ¶¶[0017], [0014], [0018]. I explained this phenomena in §VI.D.3 above, which I incorporate by reference here. Increasing the area of Kitawada’s clock input terminals would involve only ordinary skill.

165. The '146 patent' later adopted this *same* solution, for the *same* reason: when “the area of the input terminal of the driving signal having a high frequency component is larger than the area of the input terminal of the image signal having a lower frequency component,” then “the contact resistance can be made low, and thus the signal can be prevented from becoming dull.” Ex. 1001, 4:19-24; 2:42-58; 7:27-55.

166. *Third*, a POSITA would have been motivated to utilize power source terminals having an area “not smaller” than clock signal input terminals' area, rendering obvious element [1 h], because, as **Kato** teaches, power source terminals transmit “larger currents” and so their resistance needs to be lower. The '146 patent's inventor later adopted this *same* solution for the *same* reasons that Kato had previously disclosed it:

In general, if a power source, which is input into a power terminal, has a high resistance, the voltage is trapped, and there is a strong possibility that a predetermined voltage cannot be obtained. Therefore, the power source preferably has as low a resistance as possible. Accordingly, in the above-described panel, the power terminal to which power is supplied preferably has the same area or more as the area of the input terminal to which the driving signal is supplied. With this arrangement, it becomes possible to decrease the resistance, and to supply a predetermined voltage.

'146 patent, Ex. 1001, 3:23-41.

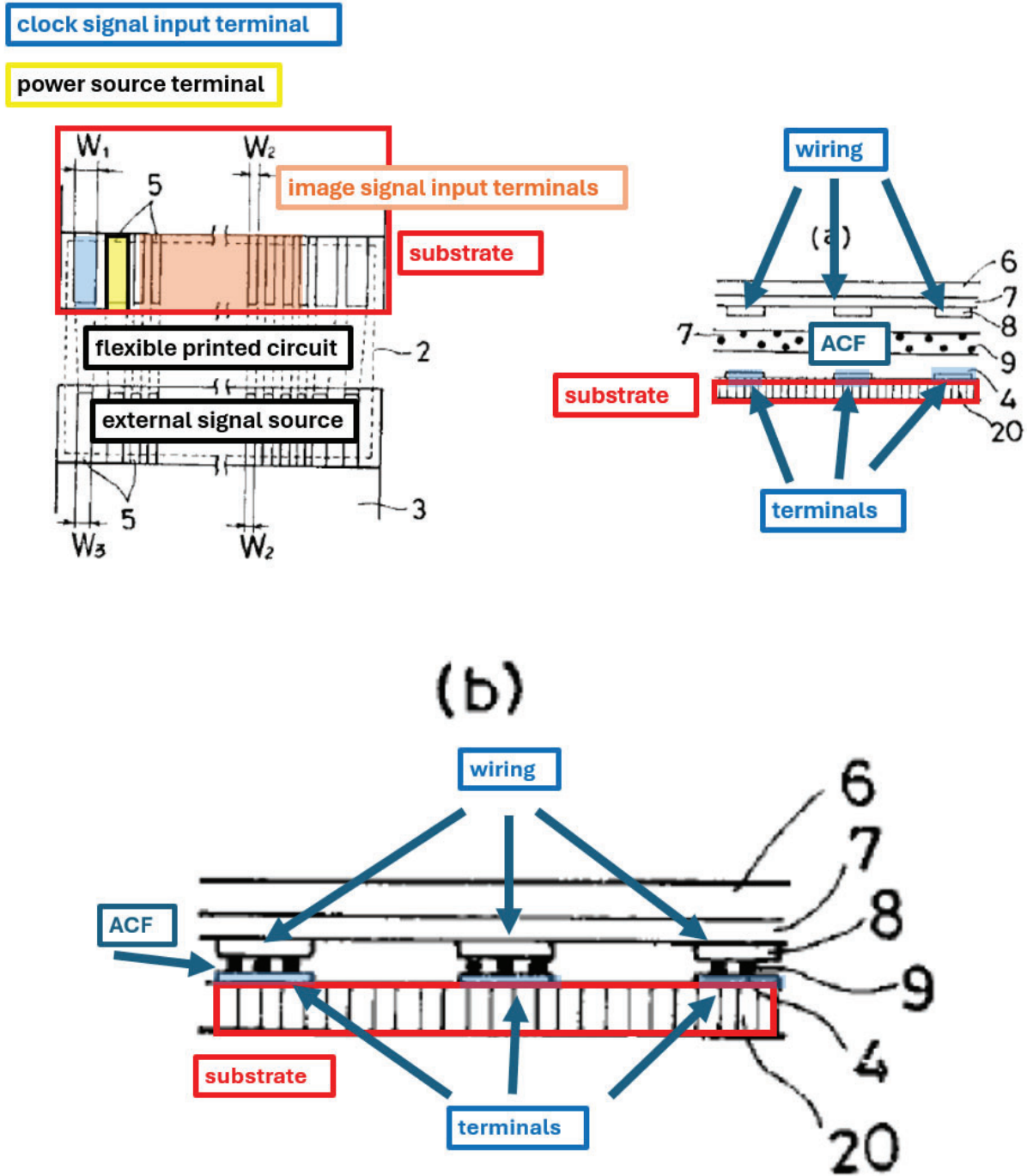
167. **Minami, Mismatch Analysis Report, and Nakashini** independently motivate “not smaller” power source terminals. As shown above, Kitawada’s power source terminals are directly adjacent to its clock signal input terminals, all of which are located near the outer ends of the substrate. Ex. 1004, Figures 1A and 2. Per the teachings of Minami, Mismatch Analysis Report, and Nakashini, terminals in that location should have a relatively larger area to mitigate known problems such as terminal-to-wiring mismatch and weakened ACF bonding strength. Since Kitawada’s power source terminals are directly adjacent to its clock signal input terminals, it would have been an obvious design choice that the power source terminals should not be smaller than the adjacent clock signal input terminals. This also would have enhanced the engineering simplicity of the design, as a POSITA would not have wanted to change the terminal width/area or pitch interval more times than necessary. Once there was a change to the terminal pad width / area for the VDDY power source (*i.e.*, increasing its area), there would have been no good reason to change it again for the clock signals (CLY, inverted CLY, DY) terminals, which are adjacent to the power source terminal

* * * * *

168. In summary, in my opinion, there are two reasons to use larger area clock signal input terminals in Kitawada—one is of a simple mechanical nature related to bonding terminals to wiring through ACF, and the other is of a simple

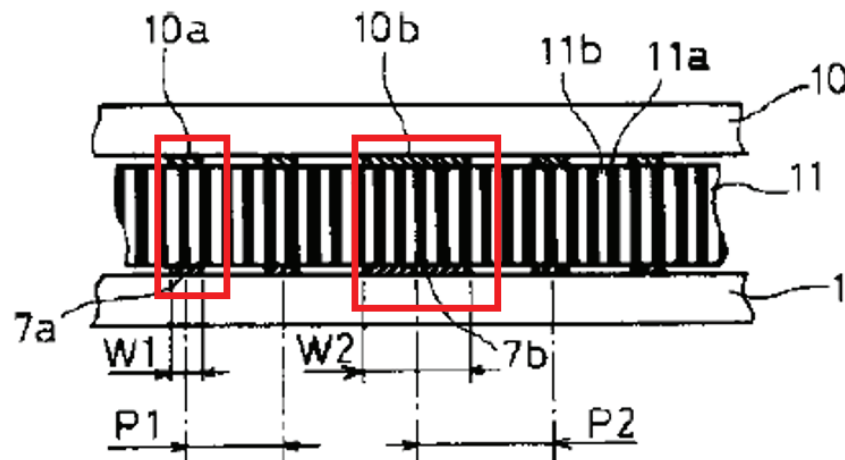
electrical nature related to resistance. First, Kitawada's clock signal terminals are near the outer side of the terminal block, so according to Minami's (and Nakanishi's and Mismatch Analysis Report's) teachings, they should have a larger area than the image signal terminals near the center. Second, clock terminals should have a larger area to lower their resistance so they can pass the "high frequency" components of clock signals, per the teachings of Sano.

169. When the LCD display's input terminals are connected to respective wiring through ACF, the larger area terminals necessarily overlap their wiring by a larger area through the ACF than do the smaller image signal input terminals. This is shown in at least Minami's (Ex. 1007) Figures 1-3. As explained previously, Minami's Figure 1 and 3 show larger area terminals near the outside of the substrate (larger area terminals are labelled "W1" in Figure 3 while smaller area terminals are labelled "W2"). Minami's Figure 2 shows that terminals overlap their respective wiring through ACF.

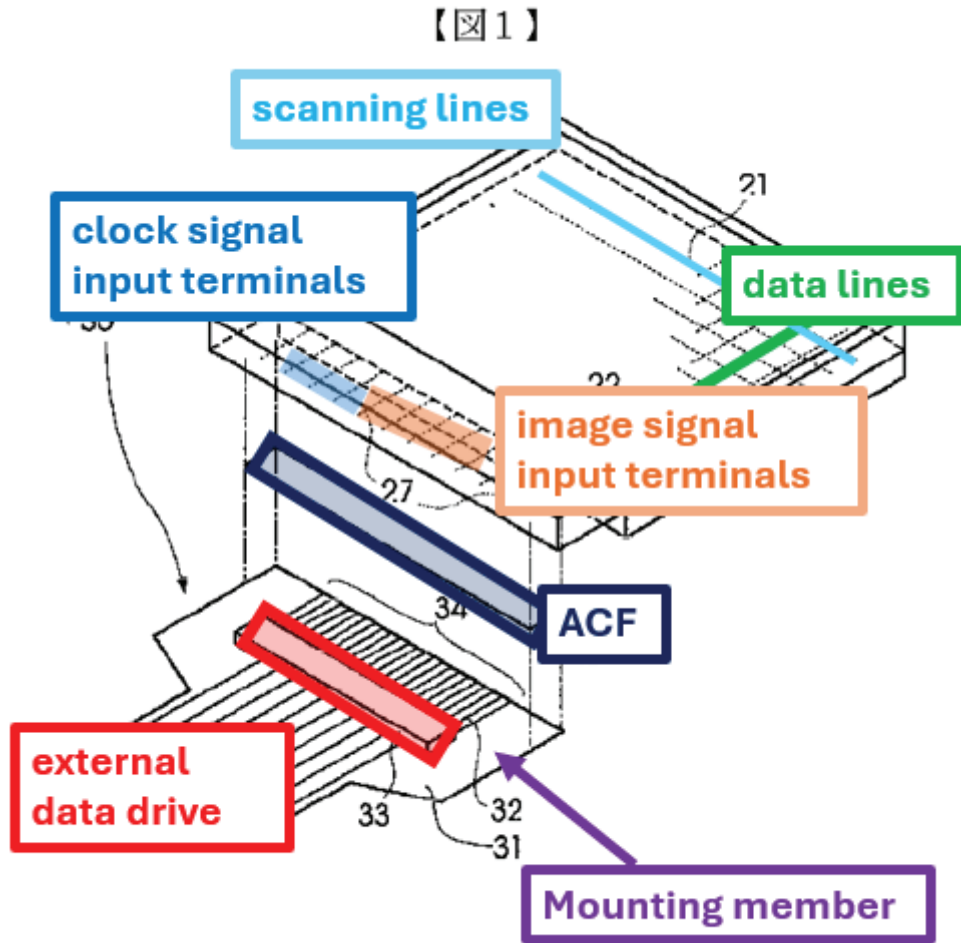


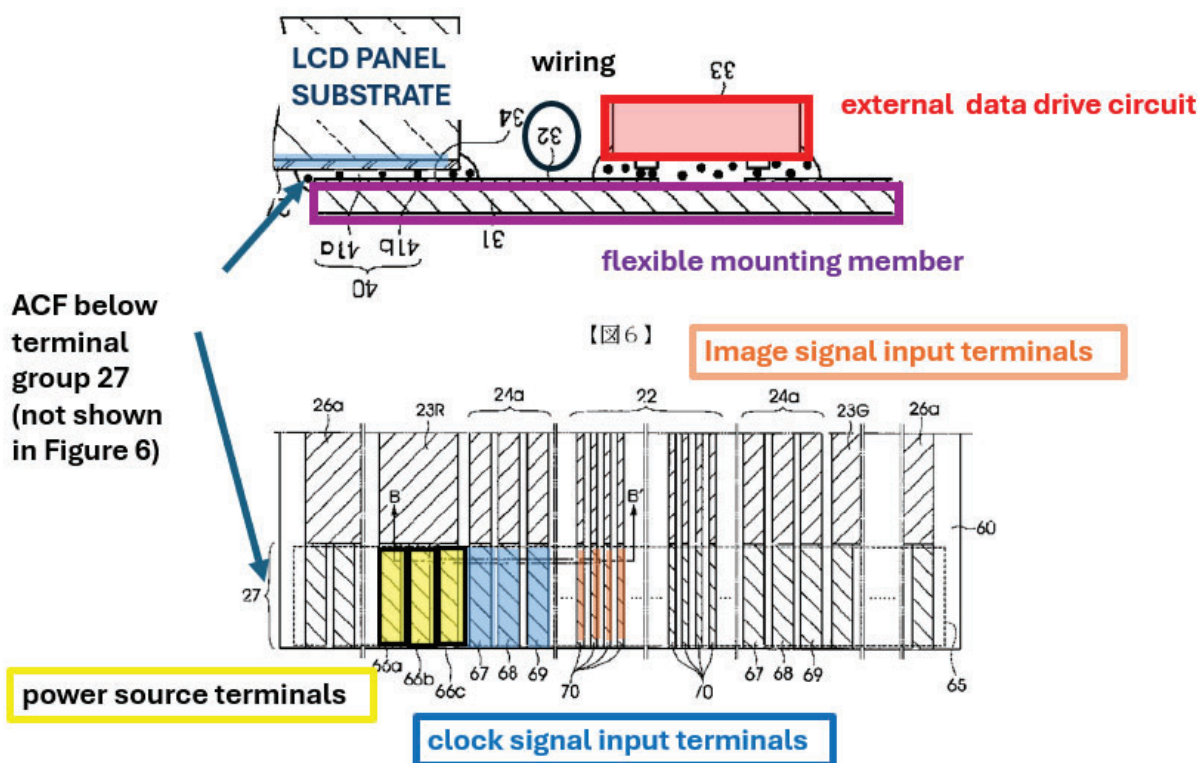
Ex. 1007, Figures 3, 2a, 2b. That larger area terminals necessarily overlap their wiring by a larger area is also shown in at least Sano's (Ex. 1006) Figure 2. As

explained previously, Sano's Figure 2 shows larger area terminal 7b (of width "W2") overlapping wiring 10b of a printed circuit board by a relatively large area through anisotropic connector 11. It also shows a smaller area terminal 7a (of width "W1") overlapping wiring 10a of a printed circuit board by a relatively small area through anisotropic connector 11.



Ex. 1006, Figure 2. That larger area terminals necessarily overlap their wiring by a larger area is also shown in at least Nakanishi's (Ex. 1010) Figures 1, 2, and 6:





Ex. 1010, Figures 1, 2, 6. As explained previously, Nakanishi's clock signal input terminals (Figure 6 at 67, 68, 69) and their wiring (24a) have equal width, while its narrower image signal input terminals (70) and their wiring (22) have the same width. Ex. 1010, ¶[0053]; (Note: in Figure 6 "the anisotropic conductive film 40 and the intermediate substrate 30 are omitted from the drawing." ¶[0052]).

Nakanishi's Figure 6 shows the terminal pads on the flex bonded to the display glass terminal pads (60 is the glass display substrate). Its terminals run from the top line to the bottom line. 65 is the bonded portion where the flex covers the glass and the terminals on the flex align with the terminals on the glass. The flex runs from the mid-line of the figure and down past the bottom of the figure. The power

terminals (66a, 66b, and 66c) lie on top of the glass substrate power wiring 23R.

All three (66a, 66b, and 66c) lie on the same wiring 23R. The total area of overlap is shown in yellow. Each clock signal terminal (67, 68, and 69) lies on one glass substrate clock wiring 24a on the glass substrate. Thus each clock terminal pair has an overlapping area as indicated in blue. Each image signal terminal 70 lies on one glass substrate signal wiring 22. Each signal terminal pair overlapping area is shown in orange. As can be seen, a signal terminal pair has the smallest area of overlap. A clock pair overlapping area is greater than the signal pair overlapping area. The power supply overlapping area (again, there are three power terminals) is larger than each signal pair overlap.

170. Similarly, there are two reasons to use larger area power source terminals in Kitawada. First, Kitawada's power source terminals are also near the outer side of the terminal block (*see* Ex. 1004, Figures 1 and 2) and should thus have a larger area, according to the teaching of Minami, Nakanishi, and Mismatch Analysis Report, discussed above. Second, and independently, power terminals should have a larger area to lower their resistance to conduct "larger currents" per Kato's teachings. Ex. 1009, ¶[0009]. A power source terminal's currents are at least as large as a clock signal input terminal's are, so it would have been obvious that the power source terminals have "not smaller" areas.

171. The prior art's reasons to selectively adjust the area of terminals are the *same* reasons that the '146 patent claims "larger area" clock signal terminals and "not smaller" power source terminals. Ex. 1001, 3:10-41; 4:24-31. In my opinion, this is significant evidence that the claims are obvious. Here, there were known problems when terminals (i) were too small when located near the corners of an LCD display's substrate and/or (ii) had too high of a resistance. The prior art addressed both problems in a straightforward and obvious way: using larger area clock signal and power source terminals (both of which require relatively lower resistance and, in the case of Kitawada, are located near the outside of the LCD panel's substrate) with smaller area image signal input terminals (which can have relatively higher resistance and, in the case of Kitawada, are located nearer to the center of the LCD panel's substrate). In my opinion, the mere change in area of Kitawada's terminals—as explicitly taught by the prior art references discussed above—would have involved no more than routine mechanical skill and would not have been patentable. Said another way, it would have been obvious to resize Kitawada's terminals in the manner claimed because doing so would improve the LCD display's operation—as taught, suggested, and motivated by the prior art.

XI. GROUNDS

A. Ground 1: Claims 10-23 are Obvious over Kitawada in view of Kawaguchi, Matsumoto, and Sano or Minami

1. Claim 10

a. [10pre]-[10d]

([10pre]: “*An electro-optical panel comprising:*”)

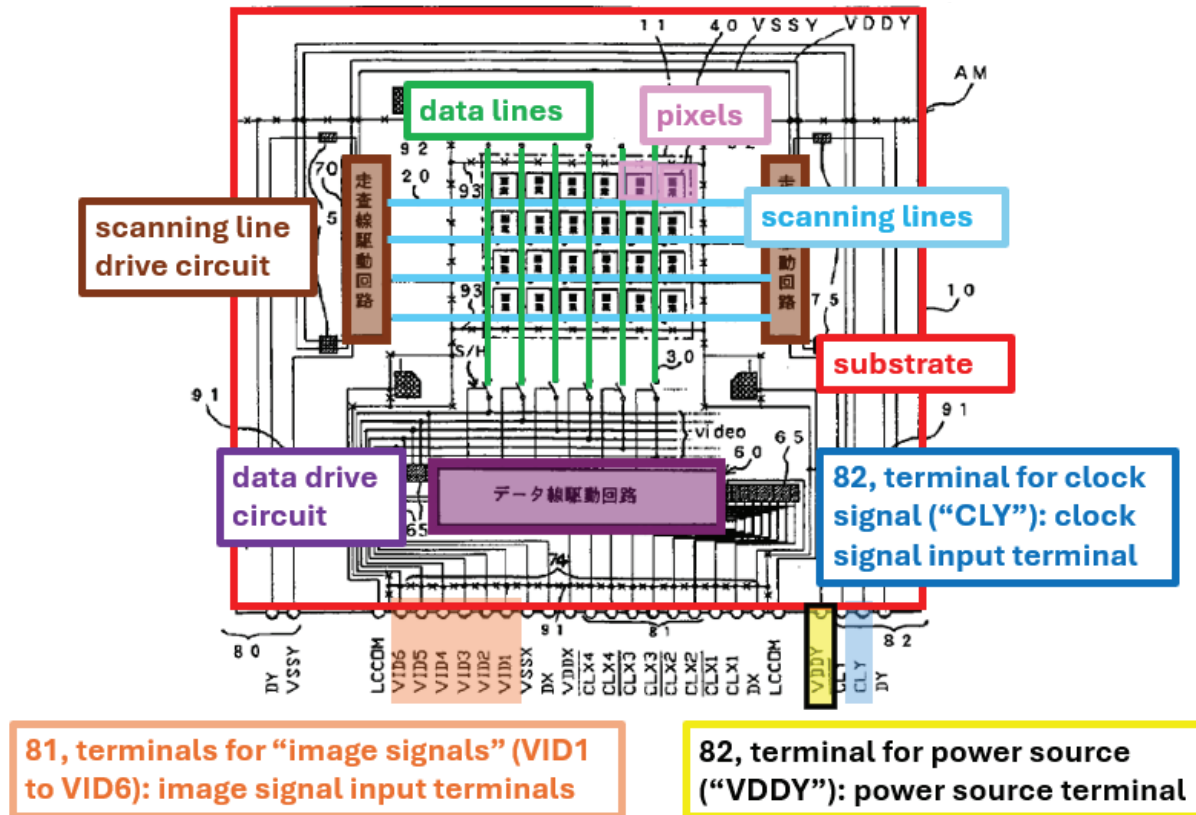
([10a]: “*a first substrate*”)

([10b]: “*data lines*”)

([10c]: “*scanning lines intersecting the data lines*”)

([10d]: “*pixels disposed corresponding to intersections between the data lines and the scanning lines*”)

172. Kitawada discloses a “liquid crystal display device.” Ex. 1004, ¶[0013]-[0014], Figures 1(A), 1(B), 2. The device includes a first substrate (“substrate 10”), data lines (“data lines 30”), scanning lines intersecting the data lines (“scan lines 20”) and pixels (“pixels 40”) disposed corresponding to the intersections between the data lines and scanning lines:



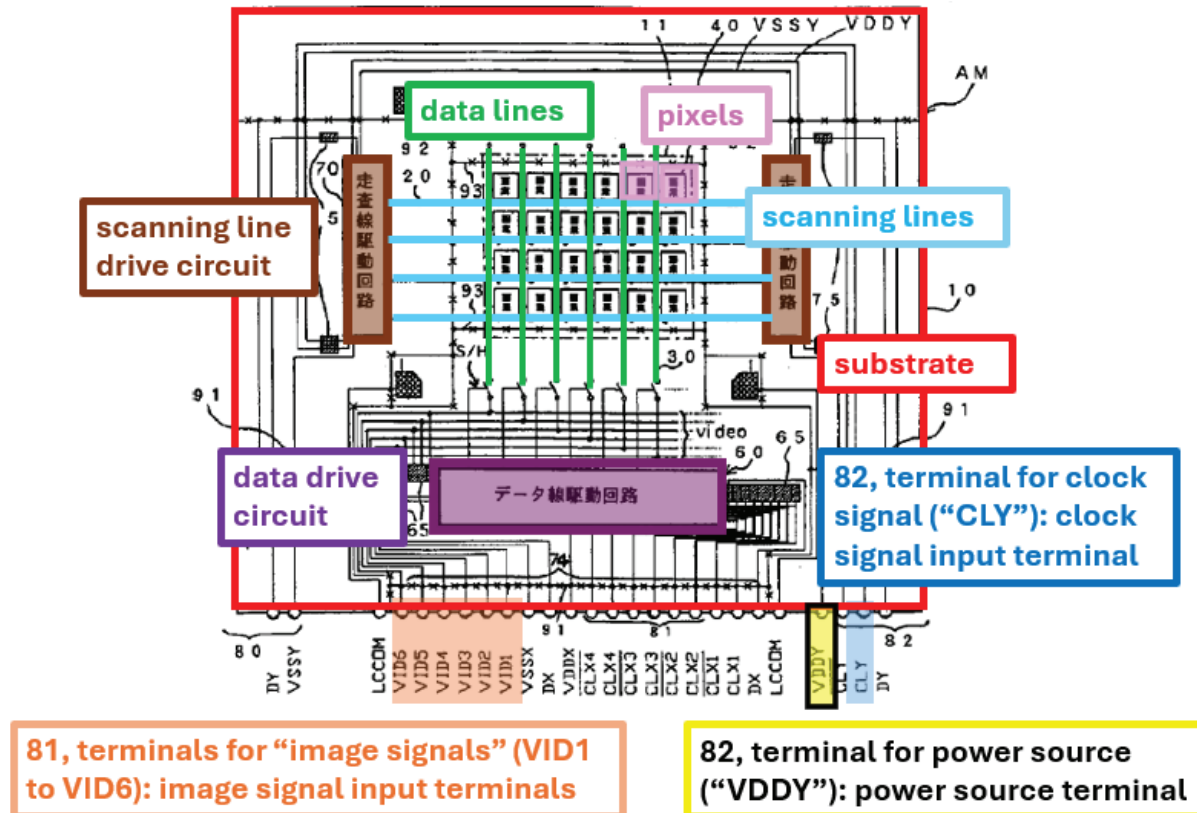
Ex. 1004, Figure 2; ¶[0017] (“the active matrix substrate AM with a built-in drive circuit used in the liquid crystal display device of the present invention, pixels 40 are arranged in a matrix on an insulating substrate 10 and connected to a plurality of scan lines 20 and data lines 30 that intersect each other.”).

b. [10e]

([10e]: “a clock-signal input terminal supplied with a clock signal and connected to a mounting member through anisotropic conductive film”)

173. Kitawada discloses a clock-signal input terminal (82, terminals for “CLY” and/or inverted CLY) supplied with a clock signal (“CLY” and/or inverted CLY). Ex. 1004, ¶[0019] (“Meanwhile, start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan

line drive circuits 70, and the scan line drive circuits 70 are driven by these signals.”); ¶[0014] (“various terminals 80, 81, 82, etc., data line drive circuit 60, and scan line drive circuits 70 are located to the outside of the opposing substrate OP.”); ¶[0020].

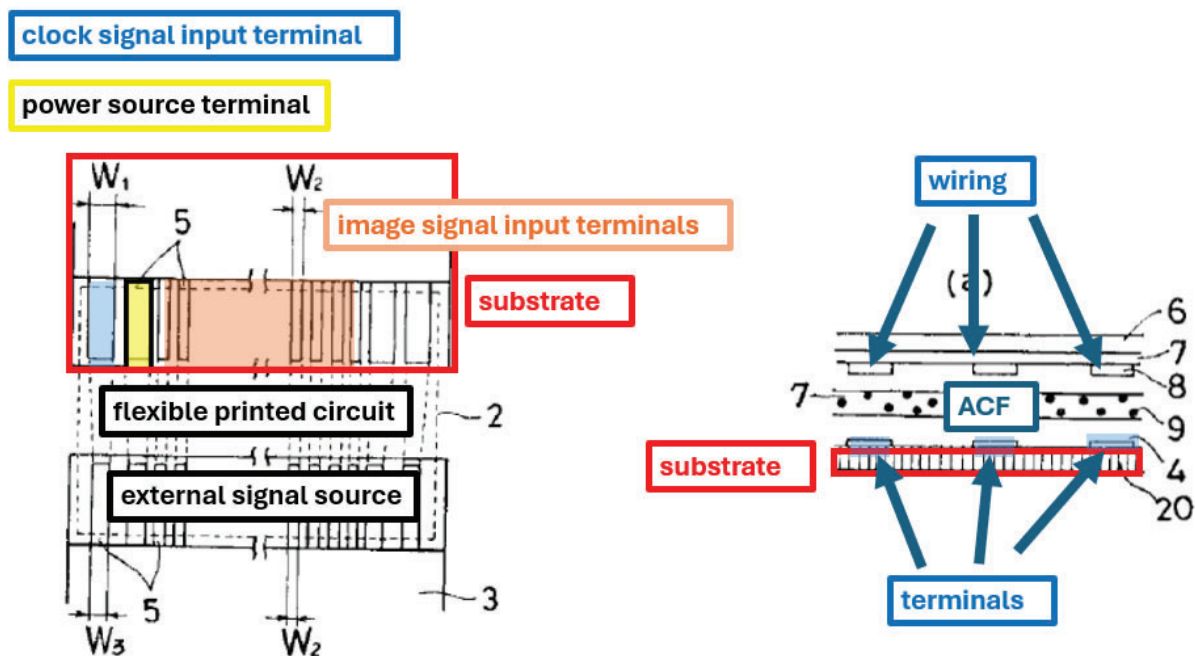


Ex. 1004, Figure 2. Kitawada renders it obvious that the clock-signal terminals are connected to a mounting member (“flexible wiring substrate, etc.”) through anisotropic conductive film. *See id.* ¶[0029] (“a flexible wiring substrate, etc., can be connected to the pads 9c (terminals) with a high degree of reliability.”).

174. Further, Kawaguchi discloses an LCD display similar to Kitawada's (See §IX.H, *supra*), and uses ACF to connect terminals to mounting members.

Kawaguchi, Ex. 1005, ¶[0055] (“The connection between the output terminal group 316 of the first TCP 31 and the input terminal group 21 of the first panel 10A is made using an anisotropic conductive film (ACF), which contains conductive microparticles in an adhesive.”). A POSITA would understand that ACF could be used in a similar way to, as Kitawada teaches, connect its “flexible wiring substrate, etc.” to the input terminals “with a high degree of reliability.” Ex. 1004, ¶[0029].

175. Similarly, Minami connects input terminals to a flexible printed circuit through ACF:

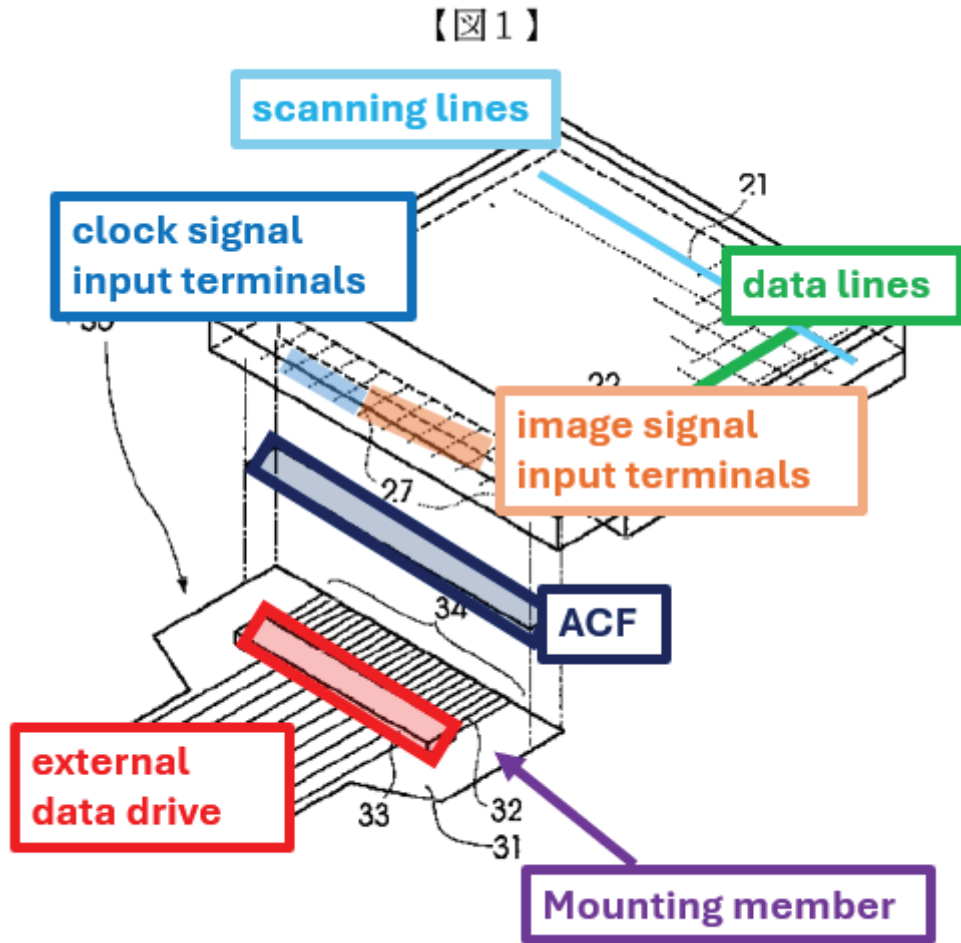


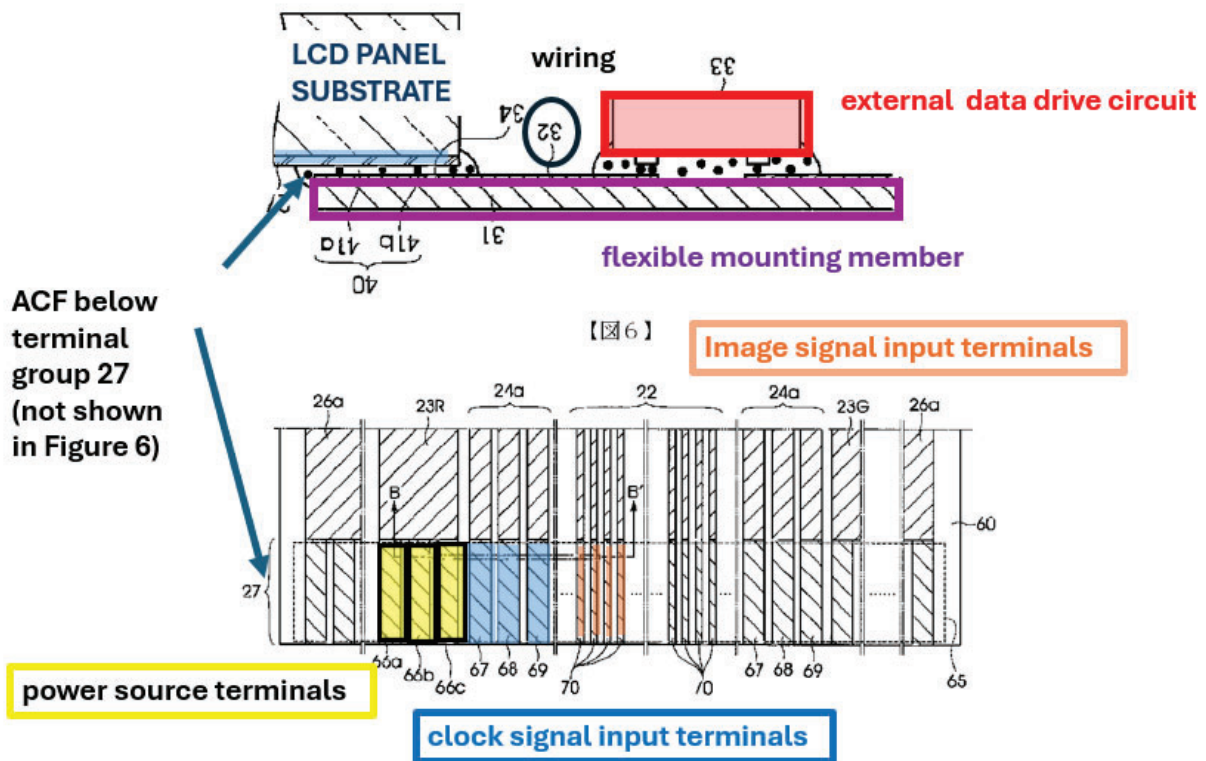
Ex. 1007, Figures 3 and 2a; page 14 of 18 (“FIG. 2 (a) shows the state of each material prior to thermal compression bonding, and FIG. 2 (b) shows the state after

thermal compression bonding. An anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7. The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).”).

176. Using ACF like this was conventional. *See* §IX.F above for my explanation of how the art moved to using ACF instead of using “zebra” anisotropic connectors that are discussed in Sano. In fact, the ’146 patent admits that displays like those recited in the claims were “known” (Ex. 1001, 1:17-62) and admits that “means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.” *Id.* at 1:51-62. These admissions underscore that it would have been obvious to connect Kitawada’s clock signal input terminals to a “flexible wiring substrate,” (Ex. 1004, ¶[0029]) through ACF—an admittedly known technique.

177. As another example, Nakanishi teaches connecting input terminals (for clock signals, image signals, and power sources) to a mounting member through ACF:





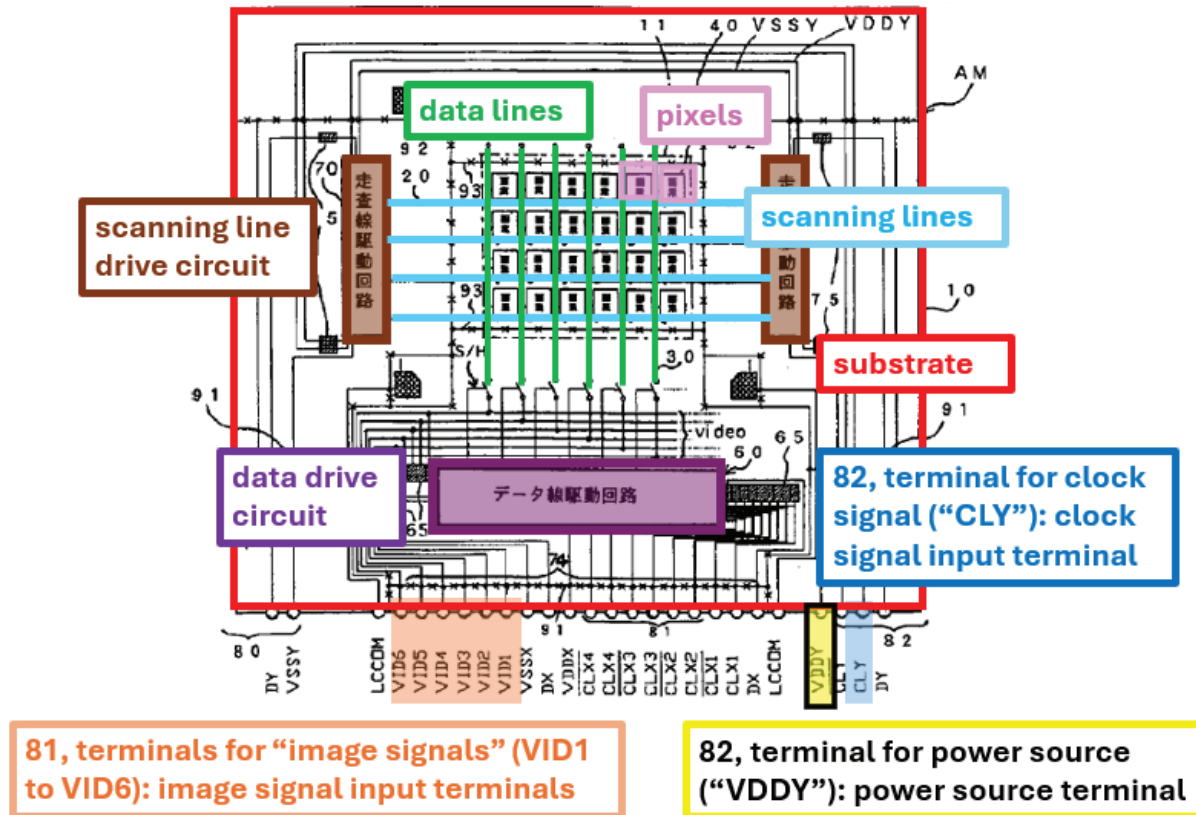
Ex. 1010, Figures 1, 2, 6; ¶[0019] (“As shown in FIG. 1, the intermediate substrate 30 is fixed to the display substrate 20 via an anisotropic conductive film 40. At this time, external connection terminals 34 on the intermediate substrate 30 are electrically connected to external connection terminals 27 on the display substrate 20 via the anisotropic conductive film 40. This anisotropic conductive film 40 is a conductive polymer film used to electrically connect pairs of terminals in an anisotropic manner and is formed, for example, by dispersing a plurality of conductive particles 41b in a thermoplastic or thermosetting adhesive resin 41a, as shown in FIG. 2.”).

178. Kitawada in view of a POSITA's general knowledge and/or in view of Kawaguchi and/or Minami renders [10e] obvious.

c. [10f]

([10f]: *“image-signal input terminals supplied with image signals and connected to the mounting member through anisotropic conductive film”*)

179. Kitawada discloses image-signal input terminals (81, terminals for “VID1” to “VID6”) supplied with image signals (“VID1” to “VID6”). Ex. 1004, ¶[0020] (“[A]long the edges of the insulating substrate 10, the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY, and a plurality of terminals 80, 81, 82 . . . to which modulated video signals (image signals VD1 to VD6), and various drive signals, etc. are inputted.”).

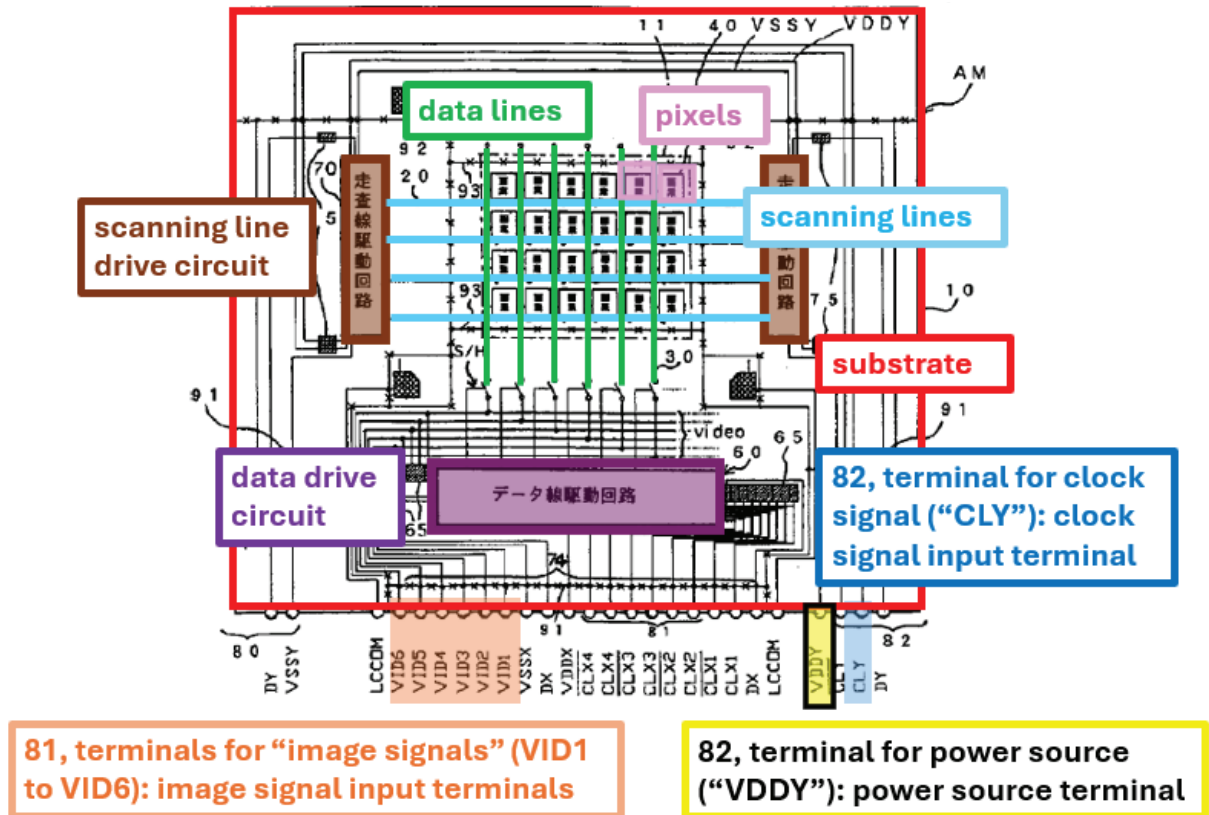


Ex. 1004 Figure 2. For the same reasons that [10e] is obvious, Kitawada renders it obvious that the image-signal input terminals are connected to a mounting member through anisotropic conductive film. ¶[0029] (“a flexible wiring substrate, etc., can be connected to the pads 9c (terminals) with a high degree of reliability.”).

d. [10g]

([10g]: “the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate”)

180. Kitawada discloses clock signal input terminals and image signal input terminals disposed along one side of the substrate:



Ex. 1004, Figure 2; also Figure 1; ¶[0020].

e. [10h]

([10h]: “the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines”)

181. Kitawada discloses a “data line drive circuit 60 is configured in the outer region (peripheral portion) of the pixel portion 11 on the insulating substrate 10 to supply video signals to each of the data lines 30.” Ex. 1004, ¶¶ [0018]-[0020]. To the extent it is argued or determined that Kitawada fails to disclose supplying image signals “simultaneously to all of the data lines,” it would have been obvious to do so. For example, Figure 2.21 of Matsumoto discloses an LCD

device that is remarkably similar to Kitawada's in that it has pixels disposed at the intersection of scanning lines ($X_1 \dots X_n$) and data lines ($Y_1 \dots Y_n$):

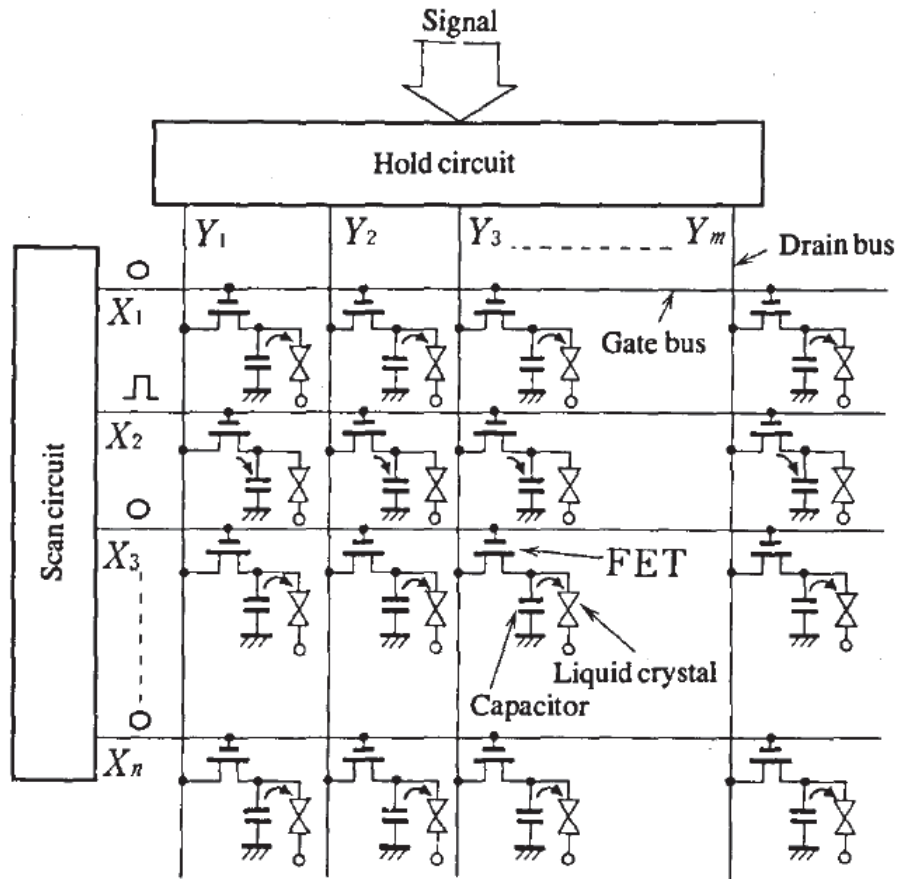


Figure 2.21 Operating principle of active matrix drive LCD

Ex. 1008, Figure 2.21. Also similar to Kitawada's teachings, Matsumoto teaches a data line drive (*i.e.*, "Hold circuit") that supplies the image signals, and a scanning line drive (*i.e.*, "Scan circuit") that activates the pixel transistors in a row-sequential manner via a "Gate bus." *See* above. The '146 patent admits that this structure was "known" and had been "widely used." Ex. 1001, 1:18-62.

Matsumoto teaches that the image signals are supplied from the Hold circuit to all

of the data lines simultaneously. Ex. 1008, page 51 of 85 (“Figure 2.21 shows the operating principle of an active matrix drive LCD using FETs. Using a line scan technique, the row electrodes (gate buses) X 1, X 2, .. , X n are scanned sequentially, so that all of the FETs on one gate bus are turned on (conducting) simultaneously, and the signals for the current row are supplied from the hold circuit through the drain buses Y1,Y2 , .. , Ym through the conducting FETs to the capacitors. The liquid crystal elements are sustained in their current state by the charge on the capacitor until the next scan.”).

182. Moreover, the original owner of the application admitted during prosecution that [10h] covers the line sequential method (taught by Matsumoto as discussed above) and that this technique was “well-known to those skilled in the art.” Ex. 1003, Response dated Sept. 17, 2008 at page 386 of 473. The applicant’s English translation of the discussed portion of the cited prior art (reproduced below) closely resembles the text of page 51 of 85 of Matsumoto cited above:

2008年 8月 7日 18時11分

NO. 1216 P. 7



SEIKO EPSON CORPORATION

Partial translation of Liquid Crystal Display Technology

Page 14, Fig. 1.11 and first paragraph

Fig. 1.11 shows the operating principle of an LCD using three-terminal elements by active matrix drive. The scanning row electrodes (gate bus) $X_1, X_2, \dots, X_n$ are scanned one after the other using a line sequential drive method so that all of the three-terminal elements on one gate bus are temporarily turned ON all at once. In synchronization with this scanning, signal electrical charges from the hold circuit are supplied through the signal column electrodes (drain bus) $Y_1, Y_2, \dots, Y_m$ to all of the capacitors connected to the three-terminal elements in this ON condition. These signal electrical charges continue to be applied to the liquid crystal of all pixels on the gate bus until the next frame of scanning.

Page 70, lines 12 to 14

Writing to the pixel electrodes is performed by a method wherein signals supplied simultaneously to the signal lines $D_1, D_2, \dots, D_m$ are sampled using address signals sequentially supplied to the scanning lines $G_1, G_2, \dots, G_n$. This is called line sequential drive.

See Ex. 1022 and Ex. 3 at September 17, 2008 “Non Patent Literature.” And Figure 1.1 of the applicant’s cited reference (reproduced below) is virtually identical to Figure 2.21 of Matsumoto (shown previously):

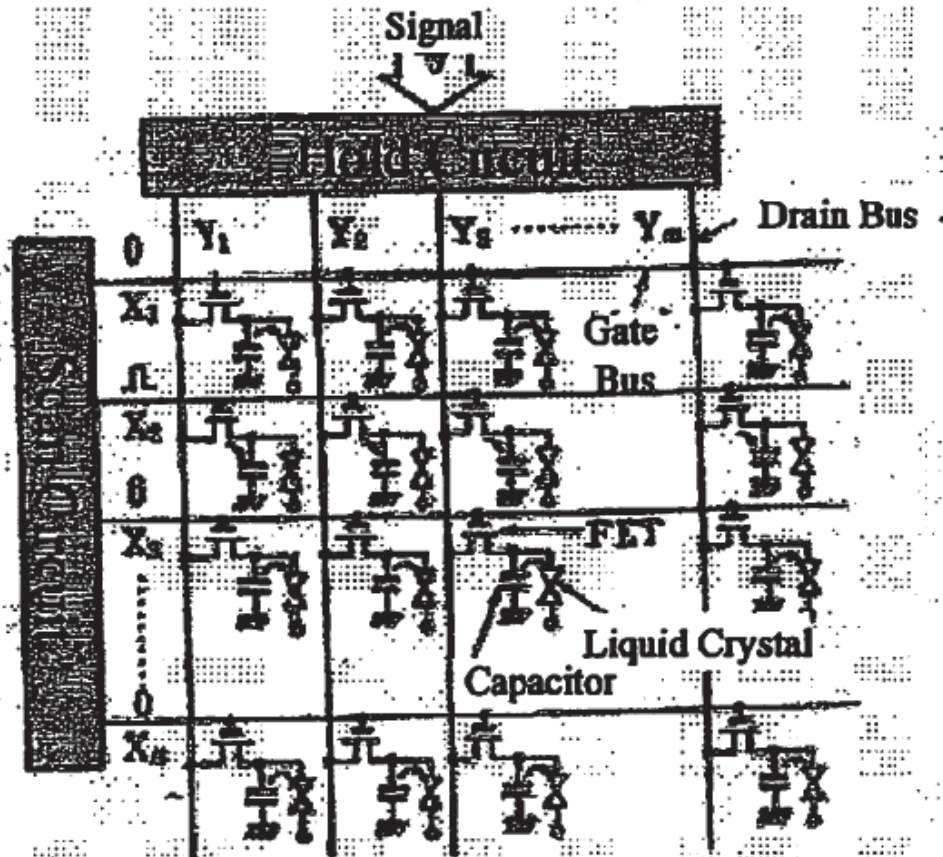


Fig. 1.11 Operating principle of three-terminal element type active matrix drive LCD

Ex. 1022. These admissions are binding and underscore that it would have been obvious to supply image signals simultaneously to all data lines. A POSITA would have been motivated to use this method, taught by Matsumoto and AAPA, with the LCD display of Kitawada to increase the display's refresh rate, decrease motion blur, reduce flickering and dynamic distortion, increase the accuracy of motion detection and compensation, and decrease the response time. This makes the display more stable, with smoother and more natural images and no flickering.

183. [10h] recites an “external data drive circuit” but Kitawada’s “data line drive circuit 60” is formed on the panel’s substrate. Kawaguchi and Nakanishi each disclose an external data driver circuit (as recited in [10h]) that is connected to the panel’s image signal input terminals using a flexible mounting member bonded with ACF. Nakanishi, Ex. 1010, Figures 1, 2 (shown previously); Kawaguchi, Ex. 1005, ¶[0055]; *see* §§IX.G and IX.H above for more detailed discussions of Kawaguchi and Nakanishi, which are incorporated by reference herein. This was admittedly a “known” technique (Ex. 1001, 1:57-62), and there are a finite number of ways of implementing a data driver, *viz.*, forming it on the substrate (like Kitawada) or using an external driver (like Kawaguchi and Nakanishi). Both configurations were conventional.

184. Many additional publications teach external data drives. Ex. 1012, Figure 1 and 18:31-38 (“Flexible wiring boards 4, 4', ... each having a drive IC 5 for driving the liquid crystal panel 20 mounted thereon are attached on the peripheral portion of one glass substrate 2.”); Ex. 1015, ¶[0047] (“The aforementioned . . . embodiments have described methods of mounting flexible circuit boards equipped with driver circuits for driving a liquid crystal display device. These embodiments have the same effects when applied to any kind of flexible circuit board containing driver circuits which supply signals to any type of

wiring on the insulating substrate, such as scanning lines or image signal lines, which contributes to display.”).

185. A POSITA would understand the benefits of forming the *scanning* line drives on the LCD panel’s substrate while using an external *data* drive to supply image signals to the data lines. Scanning signals generally involve only two levels of voltage, one for “ON” (*e.g.*, +15 to + 25 Volts), and one for “OFF” (*e.g.*, -5 to -30 Volts). It was easy for a POSITA to implement a scanning line driving circuit on the LCD’s substrate using semiconductor materials that were commonly used for displays at the time (*e.g.*, amorphous silicon, polysilicon, oxide semiconductors). *Id.* On the other hand, a POSITA would have known that image / data signals utilized a range of voltages (*e.g.*, -5 to + 5 Volts), divided into 256 subdivisions to control the grayscale of the pixels (*e.g.*, 8 bits = $2^8 = 256$).

Therefore, a POSITA would have known that such voltage levels required delicate fine tuning of the transistor characteristics and precise output of the voltage. A POSITA knew that this was relatively difficult to achieve on a TFT made of amorphous silicon, polysilicon, or oxide semiconductor—which are the materials that could be manufactured to form the TFT on the LCD’s glass substrate. *Id.* So, a POSITA normally would have implemented an external image signal driver on silicon chips made of single crystalline silicon. *See also* §VI.D.2 above. It would have been obvious to modify Kitawada by using an “external” data driver (*i.e.*, not

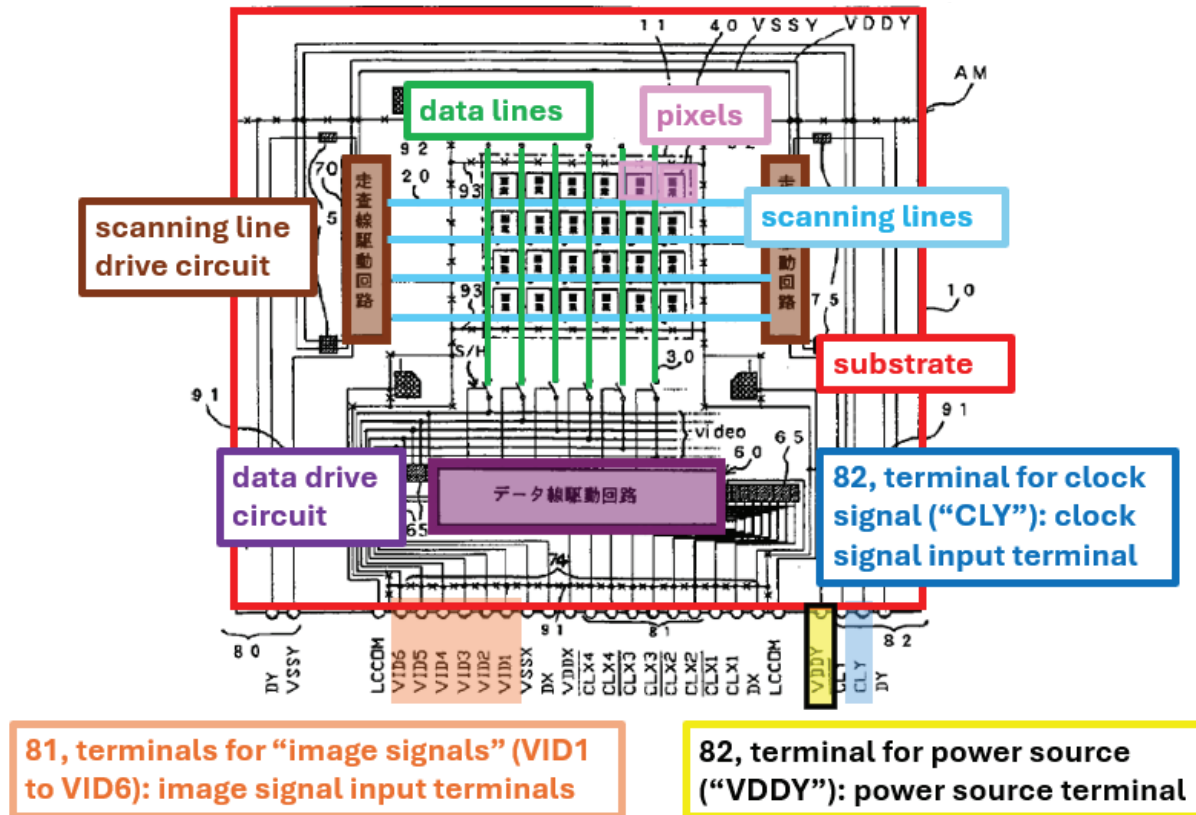
formed on the LCD panel's substrate), as taught by Kawaguchi, Nakanishi, and many others.

186. It would have been obvious to modify Kitawada to utilize an external data driver circuit (as recited in 10[h]) that is, for example, connected to the panel's image signal input terminals using a flexible mounting member bonded with ACF (as taught by Kawaguchi and Nakanishi), and a POSITA would have seen the benefits in doing so for the reasons mentioned above.

f. [10i]

([10i]: “*and a scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal*”)

187. Kitawada discloses a scanning-line drive circuit (“scan line drive circuits 70”) that is formed on the first substrate:



Ex. 1004, Fig. 2; ¶[0018] (“In addition, scan line drive circuits 70 are configured at the ends of each scan line 20 to supply scan signals for pixel selection to each scan line 20.”). To the extent it is argued or determined that Kitawada’s scanning-line drives are not on the first substrate, it would have been obvious to form them there. As discussed above in [10h] and §VI.D.2, scanning line drives are far simpler than data drivers and can be fabricated using thin film transistors which can be formed on the LCD’s substrate. Further, Matsumoto teaches that “the peripheral drive circuitry can be integrated on the same substrate as that for the FET array for the display” and motivates this configuration because it “simplifies the connection between the drive circuit and the display.” Ex. 1008 at page 52 of 85. Sano also

motivates “mounting” drivers “on the transparent substrate” because it “simplifies the manufacturing process.” Ex. 1006, ¶[0002].

188. A POSITA would understand that Kitawada’s scan line drive circuits sequentially transmit a start pulse (“start signal DY”) in synchronization with the clock signal. Ex. 1004, ¶[0019] (“start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals”). Similarly, Kawaguchi’s scanning line drive circuit sequentially transmits a transmission start pulse (“YS”) in synchronization with its clock signal (“YCLK”). Ex. 1005, ¶[0032] (“Next, the first and second scan electrode drive circuits 100A and 100B include so-called bidirectional shift registers. Based on the power supply voltage V, Y shift start pulse YS, Y shift clock YCLK, and control signal CTLY, these bidirectional shift registers generate scan signals with a specified pulse width and timing. The scan signals are supplied sequentially line-by-line to the scan electrodes Y1, Y2, ..., Yj.”); ¶[0033] (“At this time, the shift register starts shifting in response to the Y shift start pulse YS supplied every vertical scanning period and performs shifting operations in synchronization with the Y shift clock YCLK supplied every horizontal scanning period. As the shifting proceeds, the scan signals are sequentially generated in each horizontal scanning period.”). A

POSITA would appreciate that Kawaguchi's shift register would work equally well with Kitawada's scanning line drive circuits.

189. This conventional technology was disclosed by other patents. Ex. 1021, 1:12-18 (“Shift registers, which receive a clock pulse and a start pulse to output pulses (sampling pulses) sequentially, are used in various circuits. In a display device which has a plurality of pixels arranged to form a matrix, shift registers are particularly used as a gate signal line driving circuit and a gate signal line driving circuit for selecting pixels and inputting signals to the selected pixels.”), 1:61-2:3 (“When a start pulse SP is inputted to the first stage, the shift register composed of the first stage circuit SR₁ to the r-th stage circuit SR_r that are structured as above sequentially outputs shifted pulses S₁ to S_r from the output terminals of the first stage circuit SR₁ to the r-th stage circuit SR_r in sync with a clock pulse CK and an inverted clock pulse CKB which is obtained by inverting the polarity of the clock pulse CK. The clock pulse CK and inverted clock pulse CKB are inputted to the first clocked inverters CKINV1 and second clocked inverters CKINV2 of the first to r-th stages.”), *also id.*, Figures 2 and 3.

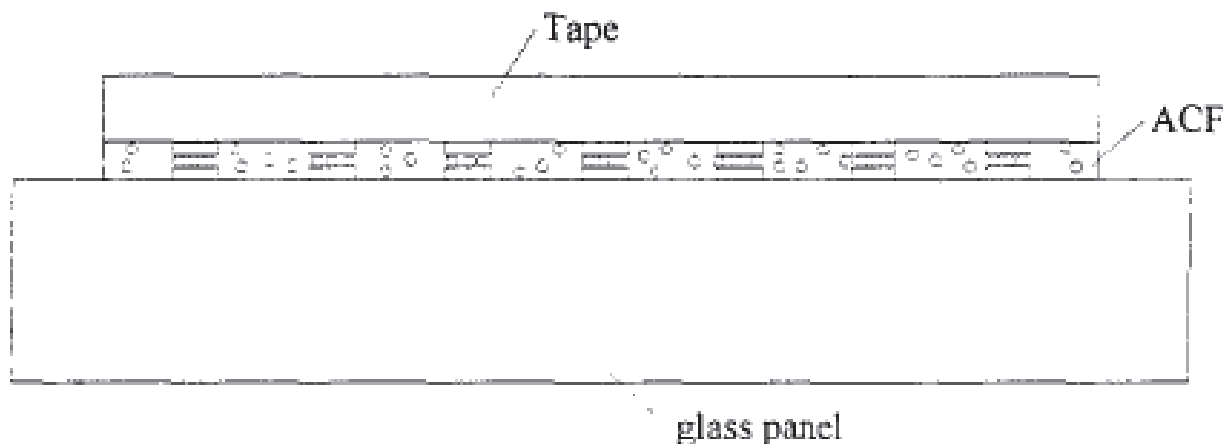
190. Kitawada renders [10i] obvious, alone or in view of Kawaguchi and/or Matsumoto and/or Sano.

g. [10j]

([10]j: “*wherein the clock-signal input terminal overlaps a first wiring of the mounting member through said anisotropic conductive film by a larger area than an area at which at least one of the image-signal input terminals overlaps a second wiring of the mounting member through said anisotropic conductive film*”)

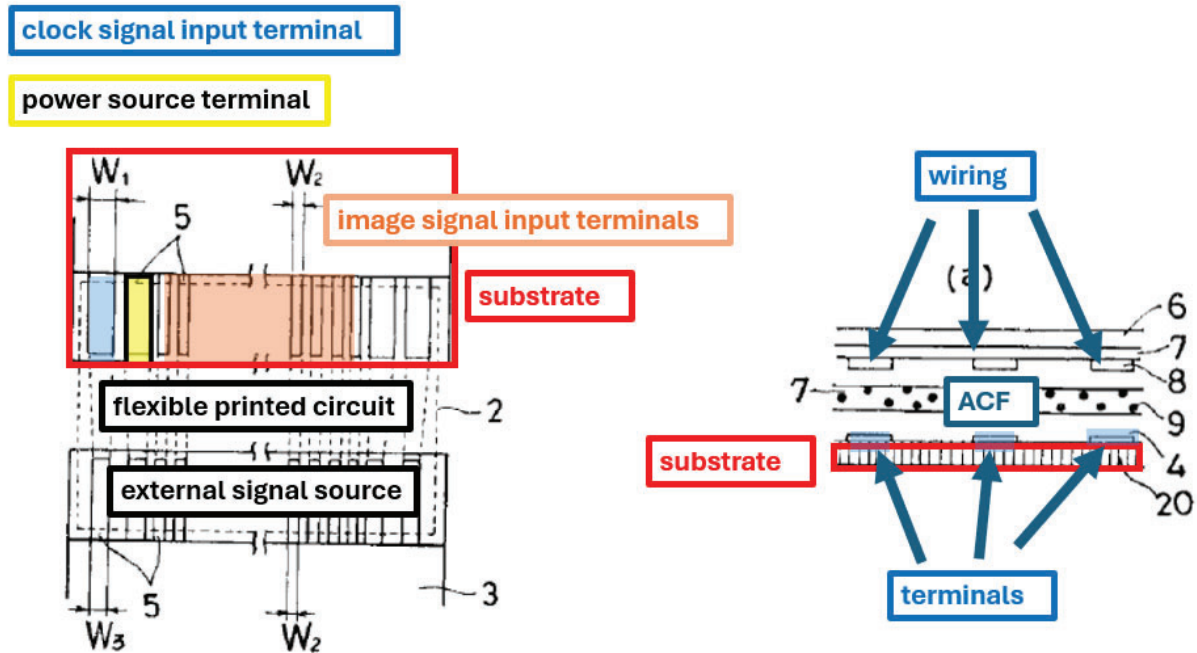
191. For several reasons, it would have been obvious to modify Kitawada to use clock signal input terminals having a “larger area” than the area of the Kitawada’s image signal input terminals. *See* §X above. With this slight modification, Kitawada’s larger area clock signal input terminals would overlap a first wiring (supplying clock signals) in the mounting member (which Kitawada calls “a flexible wiring substrate, etc.”) through the ACF by a larger area than an area at which at least one of Kitawada’s smaller area image signal input terminals overlaps a second wiring (supplying image signals) of the mounting member through the ACF (*see* [10e] and [10f] above).

192. It was commonplace to connect terminals to wiring through ACF, which naturally causes the terminals to “overlap” the wiring through the ACF, as illustrated in Mismatch Analysis Report:



Ex. 1014, Figure 1(a).

193. Similarly, Minami's Figure 3 (below on the left) shows that the outer terminals are wider (width " W_1 ") and have a larger area than the narrower terminals (width " W_2 ") near the center of the substrate:

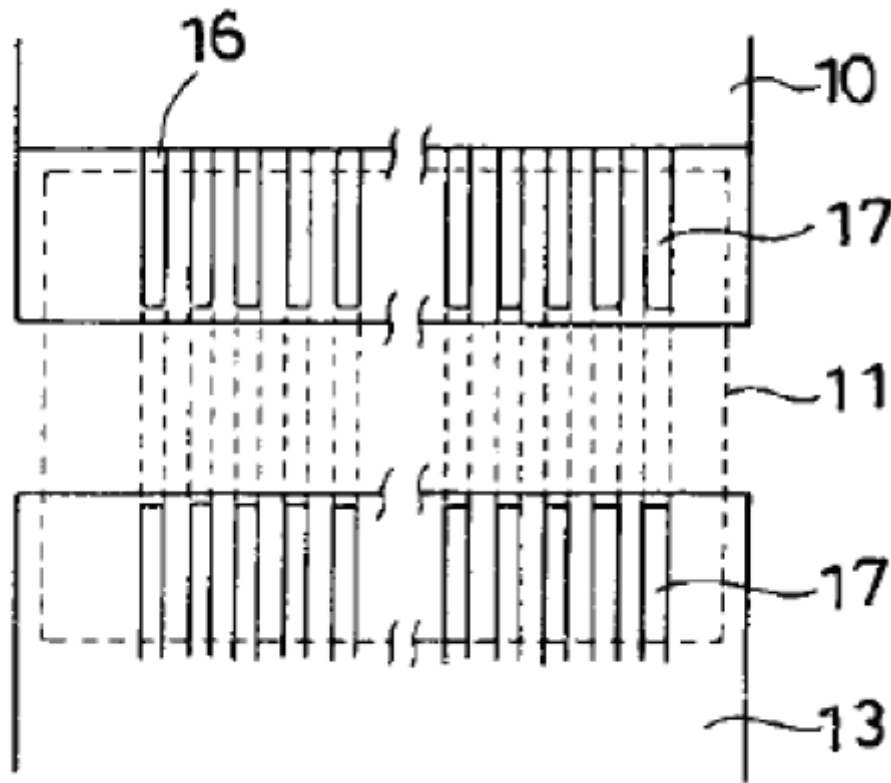


Ex. 1007, Figures 3 and 2a. Since the outer terminals have a larger area, they will overlap their respective wiring by a larger area through the ACF—the alleged point of novelty and recited in [10j]. It is clear from Minami's Figures 1-3 that wiring electrodes 5 on LCD panel 1 (panel 1 corresponds to substrate 20 in Figure 2) overlap the copper wiring 8 shown in Figure 2 (corresponding to the dashed lines of FPC 2 in Figures 1 and 3) through the ACF by a larger area at the edges of the substrate (the location of Kitawada's clock signal input terminals) than in the

center (where Kitawada's image signal input terminals are located). *See* Minami, Ex. 1007 at page 14 of 18 ("Because the pattern width near both ends of the electrode terminals in the liquid display device is wider than the pattern width of the electrode terminals near the center, ***the connection surface area*** of the electrical terminals is wider.") (emphasis added).

194. As explained previously, Minami's wiring electrodes 5 (*see* Figure 3) also comprise ITO film 4, because Figure 2 shows that it is ITO film 4 overlapping the copper wiring pattern 8. The prior art section of Minami supports this conclusion. "FIG. 6 is a diagram used to explain an example of the prior art. The connecting material uses an anisotropic conductive film 15, and ITO ($\text{In}_2\text{O}_3 + \text{SnO}_2$) electrodes (transparent electrodes) 16 provided on the LCD panel 10 side and wiring electrodes 17 formed on the FPC board 11, as well as wiring electrodes 17 formed on the PWB board (printed circuit board) 13 . . ."

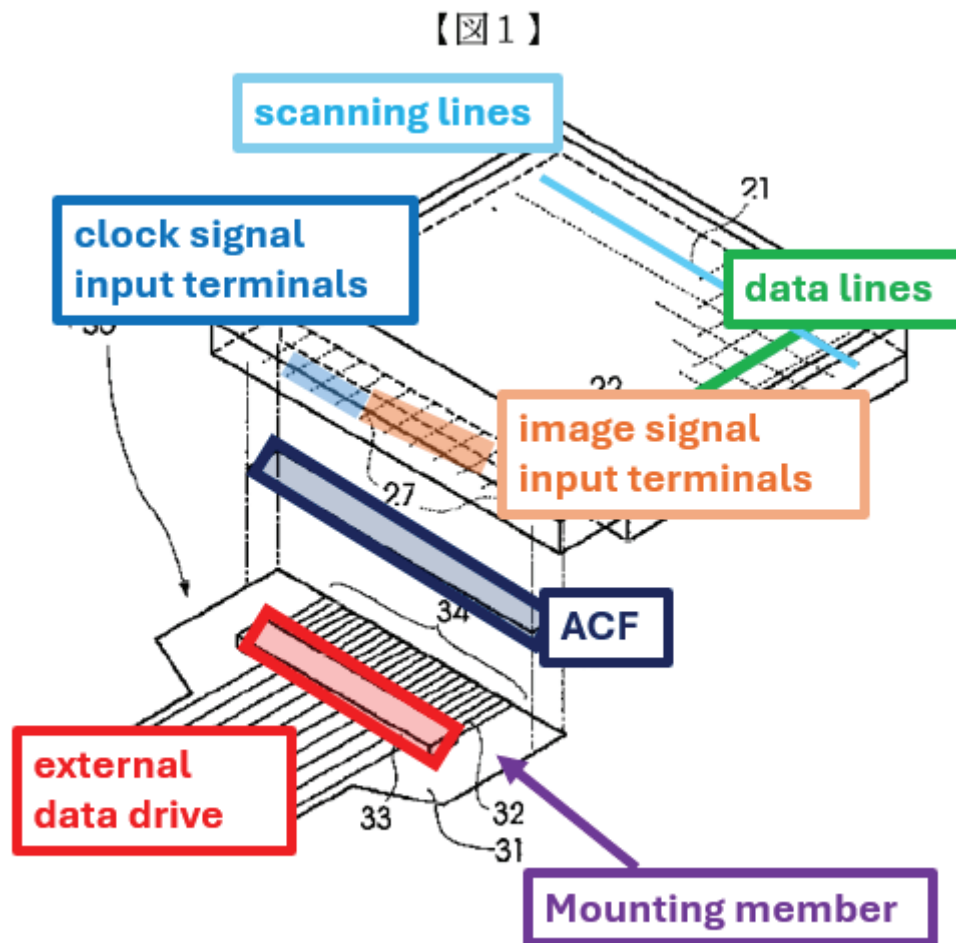
FIG. 6

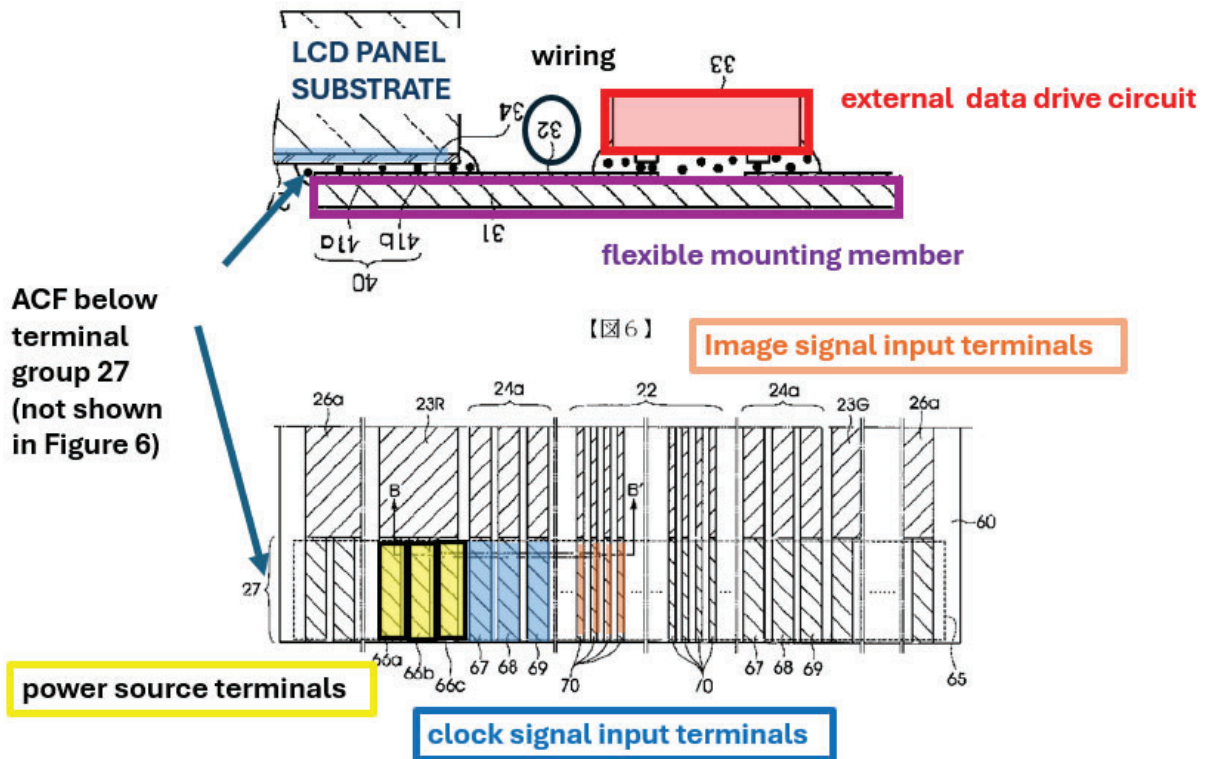


Ex. 1007, Figure 6. Comparing Minami's Figures 1 and 3 with its Figure 6, the ITO electrodes 16 and wiring electrodes 17 in the described prior art correspond to wiring electrodes 5 on LCD panel 1 and PWB board 3 in Figures 1 and 3. I note that ITO film 4 is annotated in Fig. 1. A POSITA would conclude that the ITO film 4 pattern of Fig. 2 corresponds to the wiring electrodes 5 on LCD panel 1 in Fig. 1, because the invention uses the same material ITO materials as the Minami's described prior art to form the wiring electrodes on LCD panel 1, while the novelty

of Minami's invention lies in the sizes (widths/areas) and positions of the terminals.

195. Nakanishi similarly discloses and renders obvious use of wider clock input terminals and power source terminals near the outer side of a substrate, with narrower image signal input terminals near the center:





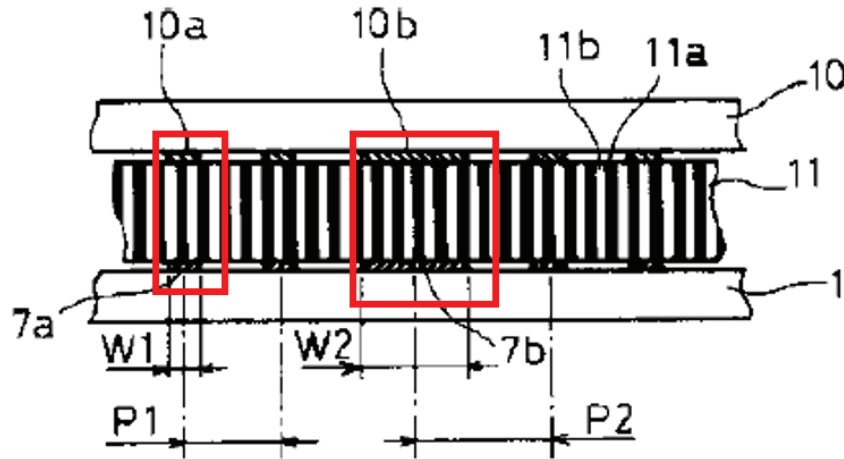
Ex. 1010, Figures 1, 2, 6.

196. Nakanishi's clock signal input terminals (Figure 6 at 67, 68, 69) and their wiring (24a) have equal width, while its narrower image signal input terminals (70) and their wiring (22) have the same width. *Id.*, ¶[0053]; (Note: in Figure 6 “the anisotropic conductive film 40 and the intermediate substrate 30 are omitted from the drawing.” ¶[0052]). Nakanishi's Figure 6 shows the terminal pads on the flex bonded to the display glass terminal pads (60 is the glass display substrate). Its terminals run from the top line to the bottom line. 65 is the bonded portion where the flex covers the glass and the terminals on the flex align with the

terminals on the glass. The flex runs from the mid-line of the figure and down past the bottom of the figure.

197. The power terminals (66a, 66b, and 66c) lie on top of the glass substrate power wiring 23R. All three (66a, 66b, and 66c) lie on the same wiring 23R. The total area of overlap is shown in yellow. Each clock signal terminal (67, 68, and 69) lies on one glass substrate clock wiring 24a on the glass substrate. Thus each clock terminal pair has an overlapping area as indicated in blue. Each image signal terminal 70 lies on one glass substrate signal wiring 22. Each signal terminal pair overlapping area is shown in orange. As can be seen, a signal terminal pair has the smallest area of overlap. A clock pair overlapping area is greater than the signal pair overlapping area. The power supply overlapping area (again, there are three power terminals) is larger than each signal pair overlap. Therefore, Nakanishi also discloses and renders obvious clock signal input terminals “overlapping” their wiring through ACF by a larger area, as claimed in [10j].

198. Finally, similar to Minami and Nakanishi, Sano’s Figure 2 shows a side view of clock input terminals 7b (of width “W2”) overlapping wirings 10b through an anisotropic connector by a larger area than the other input terminals 7a (of narrower width “W1”) overlap wirings 10a through the anisotropic connector:



Ex. 1006, Figure 2; ¶¶ [0014]-[0015]. Sano's Figure 1(a) is a top view confirming that terminals 7b have a larger area than terminals 7a, such that the larger terminals overlap their wiring through the anisotropic connector by a larger area, which also motivates the arrangement of [10j].

2. Claim 11

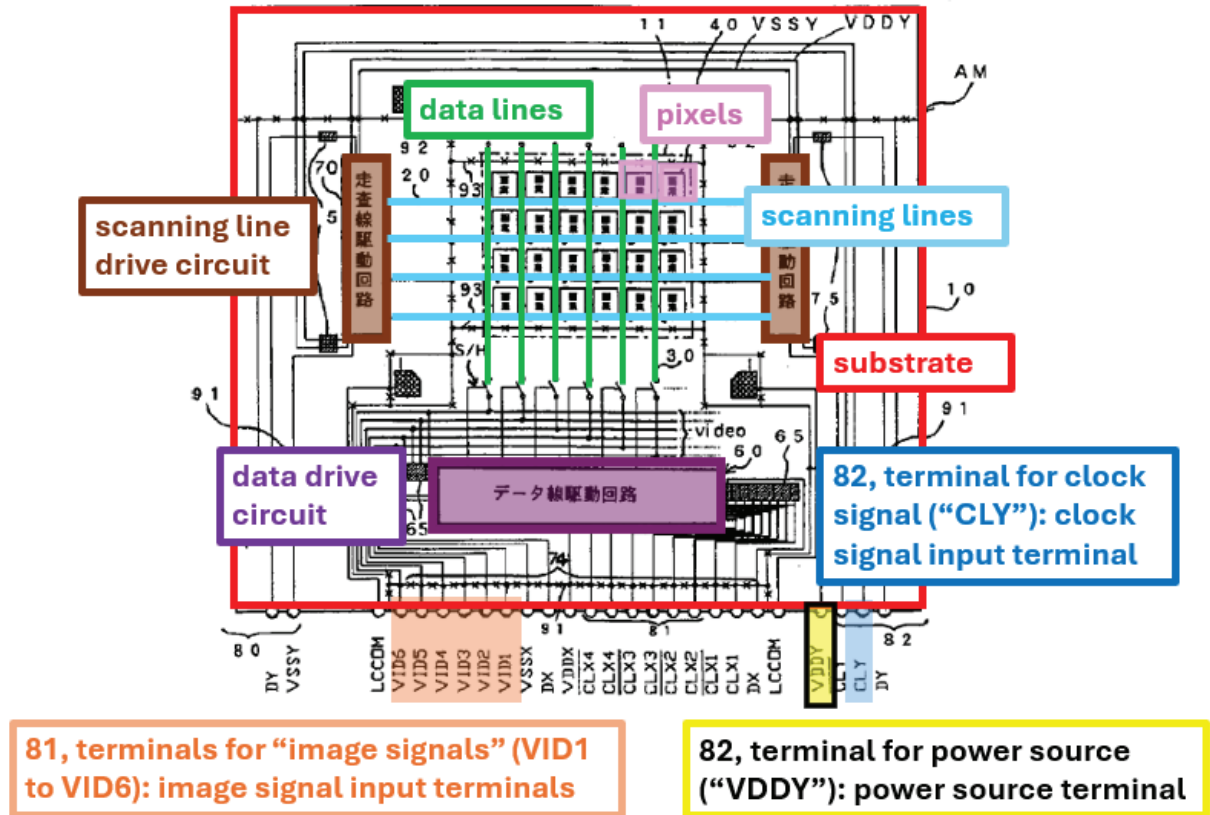
(“The electro-optical panel according to claim 10, the clock-signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.”)

199. As shown above in §X, it obvious to modify Kitawada so that its clock signal input terminal has a larger area than its image signal input terminal. A larger area terminal inherently has a smaller input resistance, a well-known fact that is also taught by Sano and Kato.

3. Claim 12

(“The electro-optical panel according to claim 10 the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal.”)

200. Kitawada's input terminals are arranged in line on an edge of the first substrate, with the image signal input terminal closer to a center of the edge:



Ex. 1004, Figure 2; Figure 1; $\nabla[0020]$.

4. Claim 13

(“The electro-optical panel according to claim 10, the external data line circuit being formed on a second substrate other than the first substrate.”)

201. As discussed in [10h] it would have been obvious to modify Kitawada by using an external data drive circuit that is formed on a mounting member separate from the LCD panel's first substrate. Again, Kawaguchi and Nakanishi (and many others including Ex. 1012, Figure 1 and 18:31-38 and Ex. 1015, ¶¶0047)) disclose an external data drive circuit that is connected to the panel's

image signal input terminals using a flexible mounting member bonded with ACF.

Nakanishi, Ex. 1010, Figures 1, 2 (shown above); Kawaguchi, Ex. 1005, ¶[0055];

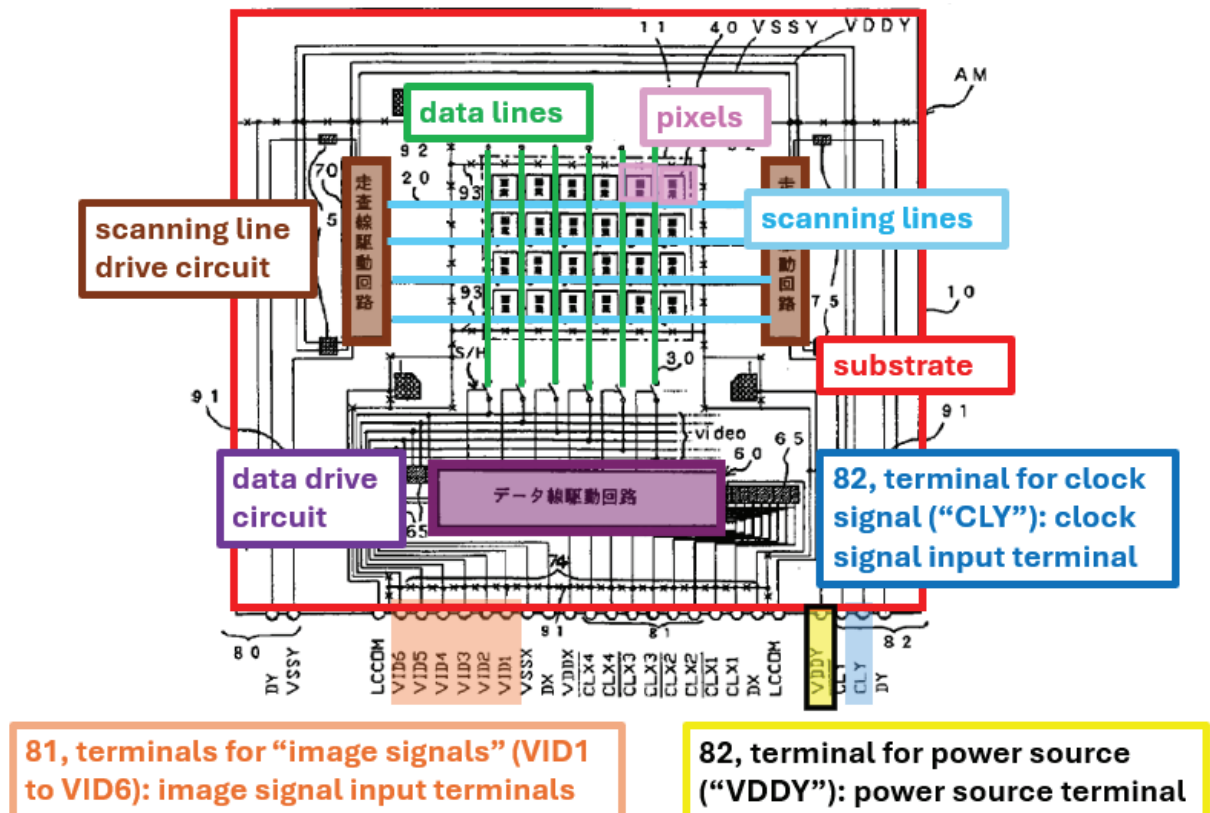
¶¶183-186, *supra.*; §§IX.G and IX.H This was a “known” technique. Ex. 1001, 1:57-62.

5. Claims 14, 15

(Claim 14: “*The electro-optical panel according to claim 10, the clock-signal input terminal being disposed further out on the first substrate relative to a central part of an outer edge of the first substrate than the image signal input terminal.*”)

(Claim 15: “*The electro-optical panel according to claim 10, the pixels arranged on the first substrate.*”)

202. Kitawada discloses claims 14 and 15:



Ex. 1004, Figure 2; Figure 1; ¶[0020].

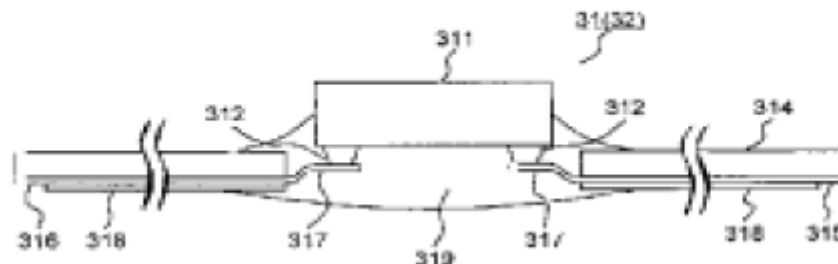
6. Claim 16

(“The electro-optical panel according to claim 10, the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.”)

203. As discussed in [10h] and claim 13, it would have been obvious to modify Kitawada by using an external data drive circuit that is formed on a mounting member separate from the LCD panel’s first substrate. Again, Kawaguchi and Nakanishi (among others) disclose such an external data driver connected to the panel’s image signal input terminals using a flexible mounting member bonded with ACF. Nakanishi, Ex. 1010, Figures 1, 2 (shown above); Kawaguchi, Ex. 1005, ¶[0055]. This was a “known” technique. Ex. 1001, 1:57-62.

204. Kawaguchi discloses a flexible substrate (“base substrate 314”) and an external substrate (“mold 319”) that are different than the LCD panel’s first substrate:

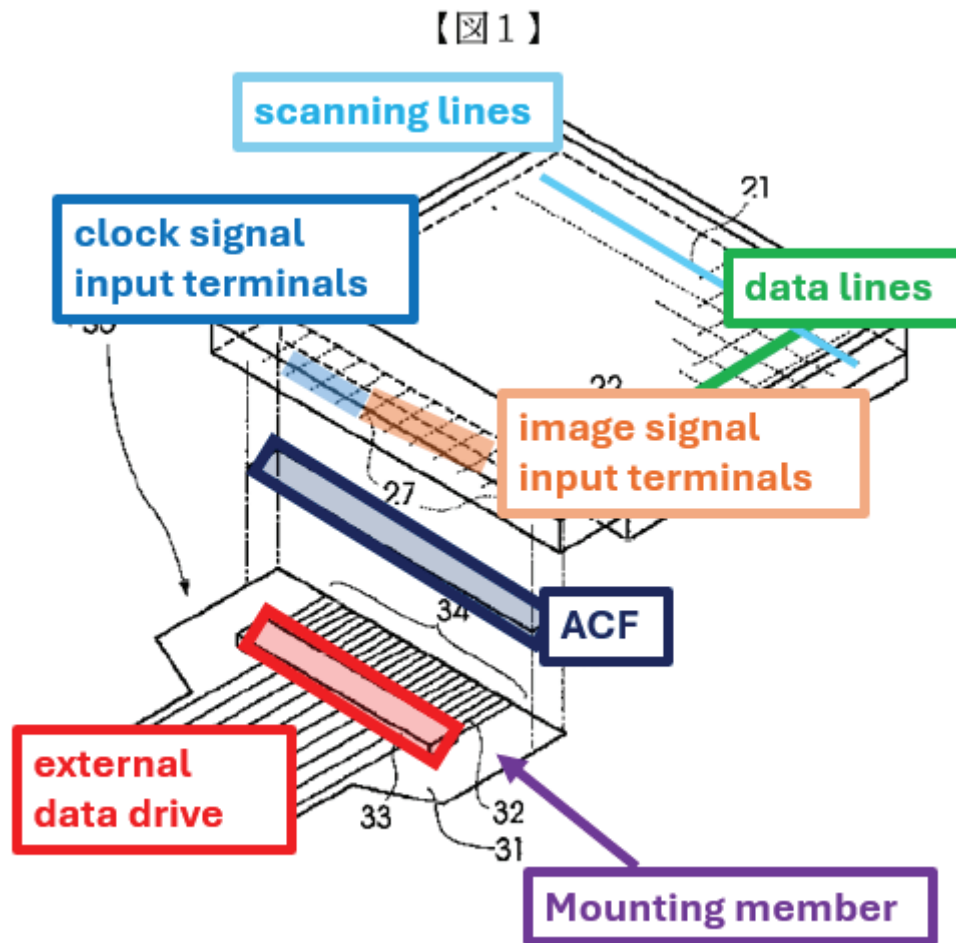
Figure 7



Ex. 1005, Figure 7; ¶[0051] (“Next, the substrate 313 is composed of a base substrate 314, input terminal group 315, output terminal group 316, connection

leads 317, resist film 318, and mold 319. As the material for the base substrate 314, a plastic such as a polyimide film is preferably used. This allows the first TCP 31 to be bent, enabling flexible mounting.”).

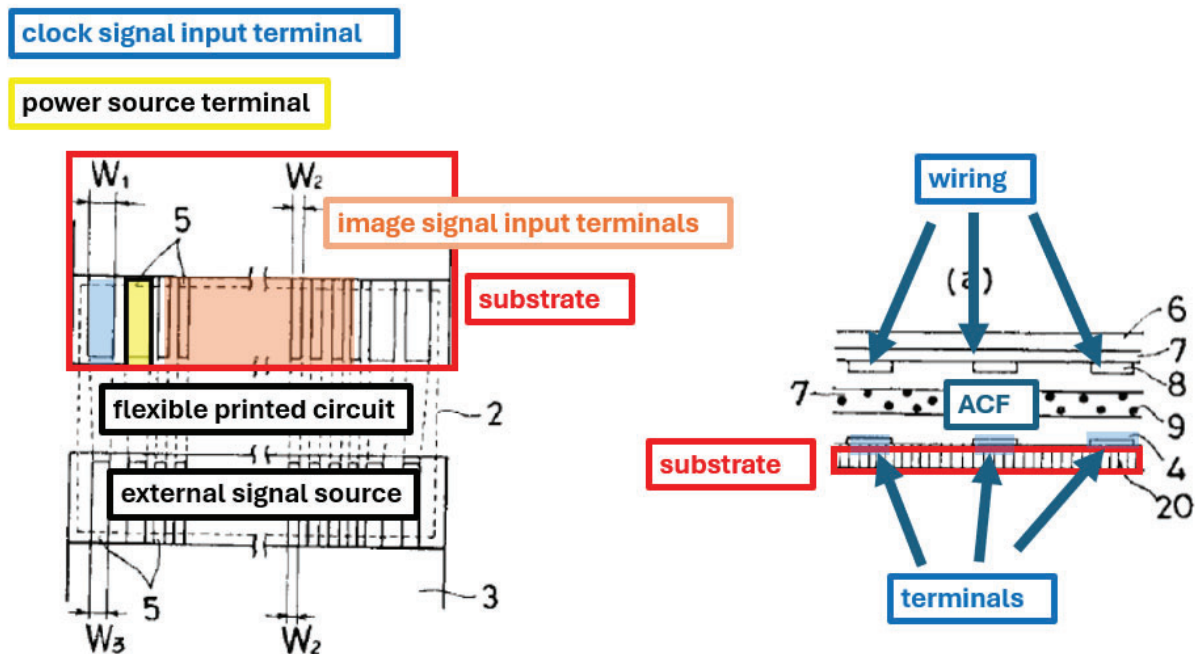
205. Similarly, Nakanishi discloses a flexible substrate (“flexible base substrate 31”) and an external substrate (“intermediate substrate 30”) that are different than the LCD panel’s first substrate:



Ex. 1010, Figure 1; ¶[0018] (“The intermediate substrate 30 has wiring 32 formed on a flexible base substrate 31 and has semiconductor chips 33 mounted at

predetermined positions on the intermediate substrate 30. External connection terminals 34 are formed at one end of wiring 32 for electrical connection to wiring such as scanning lines 21 and signal lines 22 formed on display substrate 20.”).

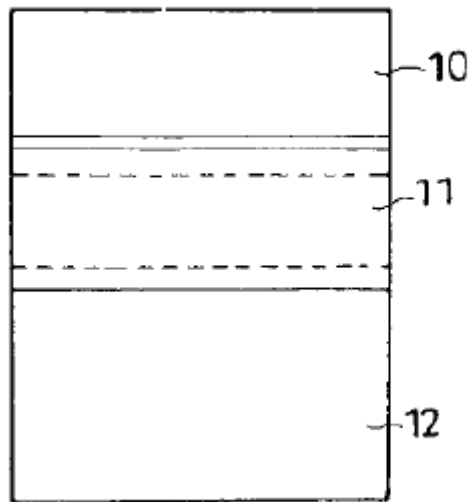
206. Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit (corresponding to the claimed “flexible substrate”) that is between the terminal and PWB board 3 (corresponding to the claimed “external substrate”) through ACF:



Ex. 1007, Figures 3 and 2a; page 14 of 18 (“FIG. 2 (a) shows the state of each material prior to thermal compression bonding, and FIG. 2 (b) shows the state after thermal compression bonding. An anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film

4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7. The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).”). *See also* Figure 4:

FIG. 4



“As shown in FIG. 4, the liquid crystal display device (LCD) comprises an LCD panel 10 formed from a glass material, a drive circuit board 12 that drives the display, and an FPC board (flexible printed circuit board) 11 that electrically connects the LCD panel 10 and the drive circuit board 12.” Ex. 1007. Using ACF in this manner was conventional. In fact, the patent admits that LCD displays like those claimed were “known” (Ex. 1001, 1:17-62) and that “means for supplying the power source, etc. to the electro-optical panel, techniques which connect an

input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.” *Id.* at 1:51-62. These admissions underscore that it would have been obvious to connect Kitawada’s clock-signal input terminals to a “flexible wiring substrate,” (Ex. 1004, ¶[0029]) through ACF.

7. Claim 17

(“The electro-optical panel according to claim 10, wherein each of the first wiring and the second wiring comprise at least one wire.”)

207. As shown in [10j] it would have been obvious to make Kitawada’s clock signal terminal overlap a “first wiring” and its image signal input terminals overlap a “second wiring.” Under the plain meaning, a “wiring” comprises “at least one wire,” and Minami, Sano, and Nakanishi teach wires. *See* [10j]; §§IX.E, IX.F, IX.G, *supra*.

8. Claim 18

(“The electro-optical panel according to claim 10, wherein contact area between the clock signal input terminal and the first wiring is greater than contact area between the at least one of the image signal input terminals and the second wiring.”)

208. As shown above, it would have been obvious to modify Kitawada such that the contact area (*e.g.*, through ACF) between its clock signal input terminal and first wiring is greater than the contact area (*e.g.*, through ACF) between its image signal input terminals and the second wiring, as motivated and taught by Minami’s Figures 1-3, Nakanishi’s Figures 1, 2 and 6, and Sano’s Figures 1-3. *See* [10j]; Minami, Ex. 1007 at page 14 of 18 (“Because the pattern

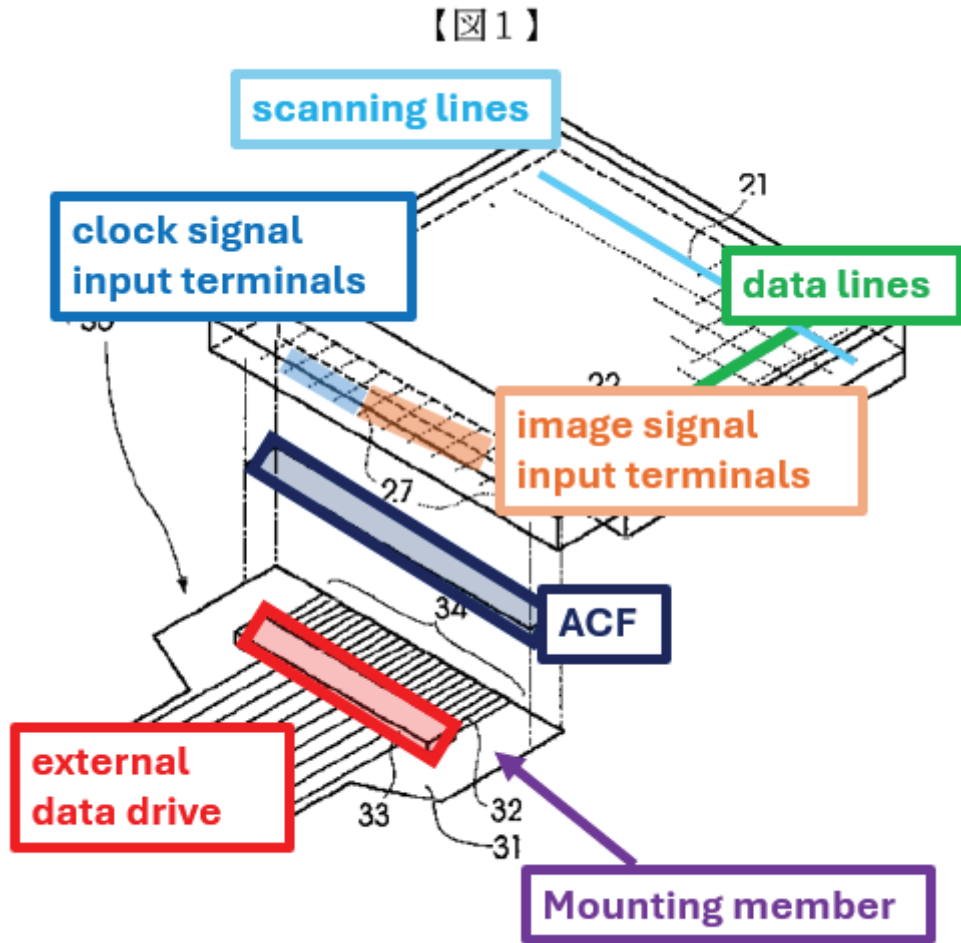
width near both ends of the electrode terminals in the liquid display device is wider than the pattern width of the electrode terminals near the center, *the connection surface area* of the electrical terminals is wider.”) (emphasis added).

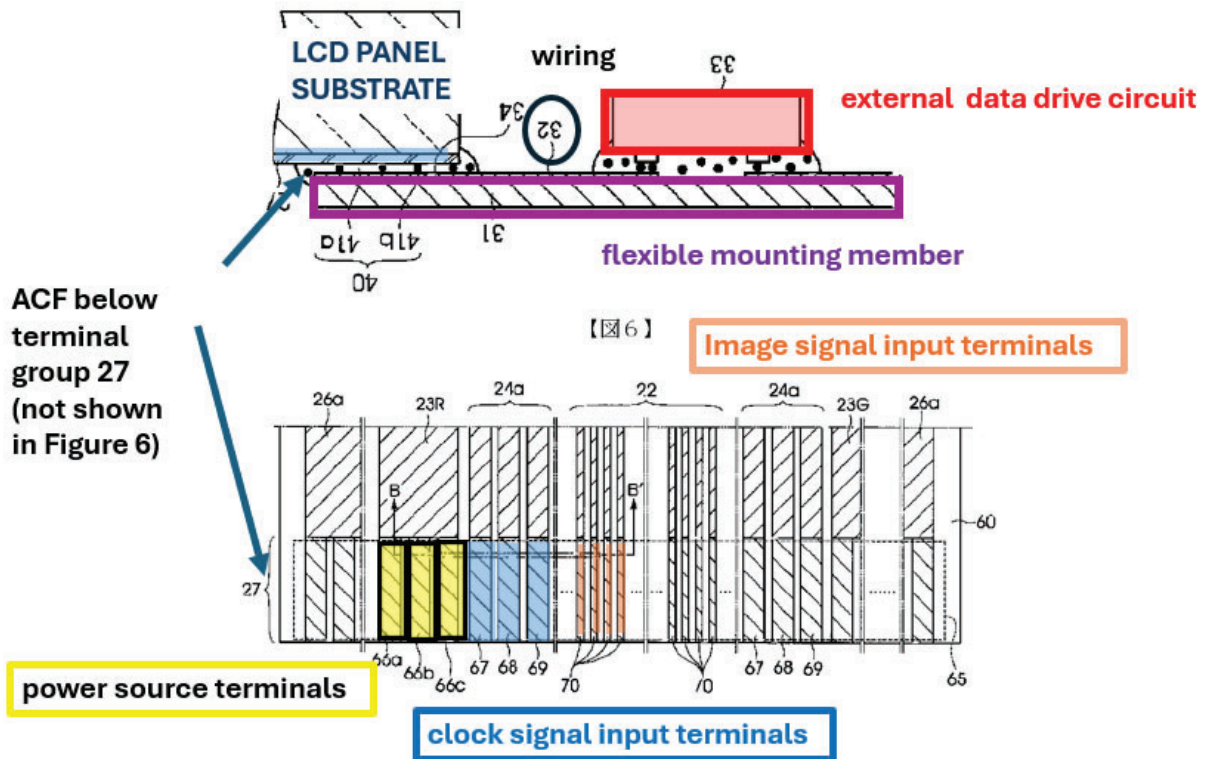
9. Claim 19

(“The electro-optical panel according to claim 10, wherein the mounting member is distinct from and connected to the first substrate.”)

209. Claim 19 is obvious for the same reasons as claim 16. Kawaguchi’s mounting member is distinct from the first substrate and is connected to terminals on its LCD panel’s substrate (through ACF). Ex. 1005, Figure 2 (showing terminal groups 21 and 22); ¶[0042] (“Furthermore, at the lower edge of the substrate 11, an input terminal group 21 for the first panel 10A is provided, while at the upper edge of the substrate 11, an input terminal group 22 for the second panel 10B is provided.”); ¶[0055] (“The connection between the output terminal group 316 of the first TCP 31 and the input terminal group 21 of the first panel 10A is made using an anisotropic conductive film (ACF)[.]”).

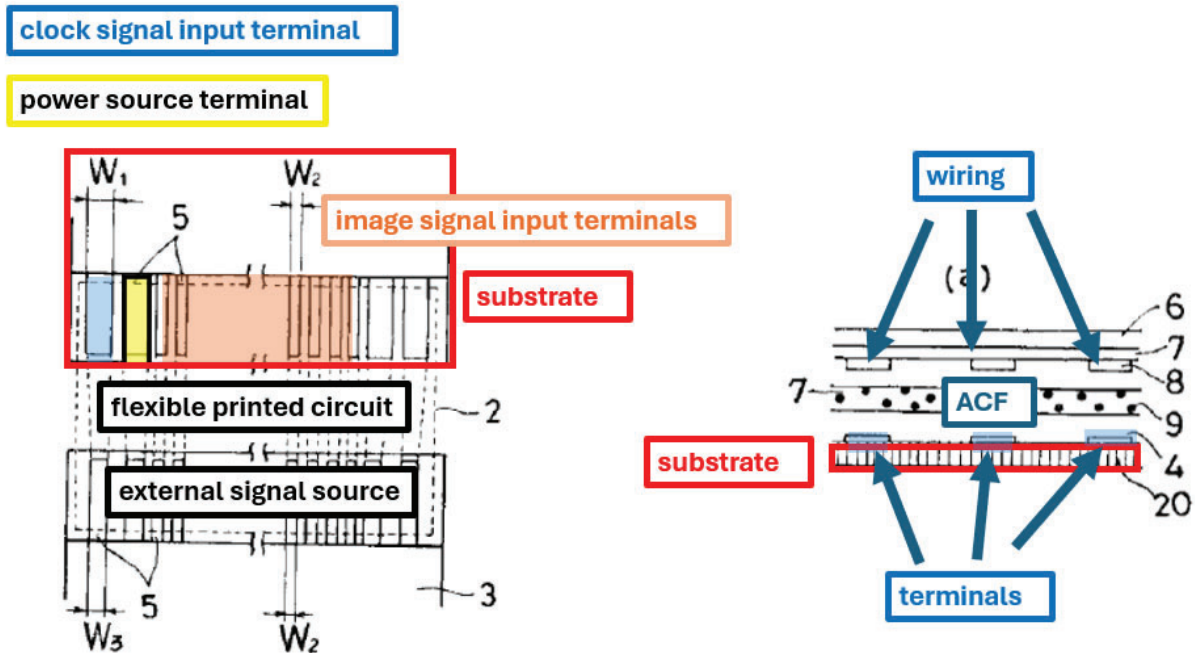
210. Similarly, Nakanishi’s distinct mounting member is connected to terminals on Nakanishi’s LCD panel’s substrate through ACF:





Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

211. Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit through ACF:



Ex. 1007, Figures 3 and 2a.

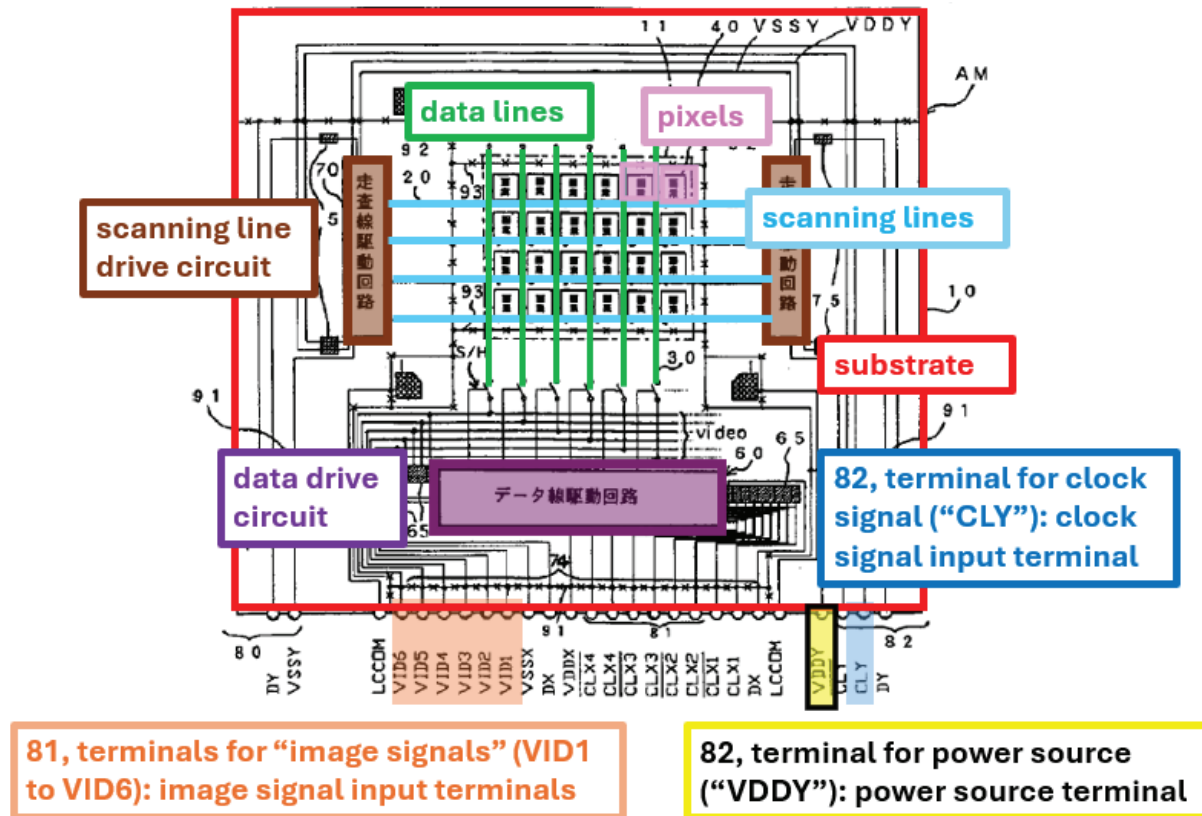
212. Using ACF in this manner was conventional. The '146 patent admits that displays like those claimed were “known” (Ex. 1001, 1:17-62) and that “means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.”

Id. at 1:51-62.

10. Claim 20

(“The electro-optical panel according to claim 19, wherein the mounting member is electrically and mechanically connected to a terminal group of the first substrate that comprises the clock signal input terminal and the image signal input terminals.”)

213. Kitawada's terminal group 82 on the first substrate comprises the clock signal input terminal while terminal group 81 on the first substrate comprises image signal input terminals:



after heat and pressure are applied and the connection “is cooled down to room temperature ... the ACF becomes solidified.” Mismatch Analysis Report, Ex. 1014, Abstract. Minami’s Figure 2(a) shows ACF inserted between wiring and terminals before heat and pressure are applied, while its Figure 2(b) shows ACF forming an electrical and mechanical connection after heat and pressure are applied. *See* Minami, Ex. 1007, at page 14 of 18 (“FIG. 2 (a) shows the state of each material prior to thermal compression bonding, and FIG. 2 (b) shows the state after thermal compression bonding. An anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7. The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).”); *id.* (“Because the pattern width near both ends of the electrode terminals in the liquid display device is wider than the pattern width of the electrode terminals near the center, ***the connection surface area*** of the electrical terminals is wider.”) (emphasis added).

11. Claim 21

(“The electro-optical panel according to claim 10, wherein the clock signal input terminal and the at least one of the image signal input terminals are connected between the substrate and the mounting member.”)

214. Claim 21 recites that “at least one of the image signal input terminals are connected between the substrate and the mounting member,” which for

purposes of this IPR, I interpret as “at least one of the image signal input terminals are connected to wiring between the substrate and the mounting member.” As discussed above with respect to [10e], [10f], [10h], [10j] and claims 16, 19, and 22, it would have been obvious to connect a mounting member to Kitawada’s terminal group using ACF. Thus, Kitawada’s clock signal input terminal and at least one its image signal input terminals would be connected to wiring, through the ACF, between the LCD panel’s substrate and the mounting member.

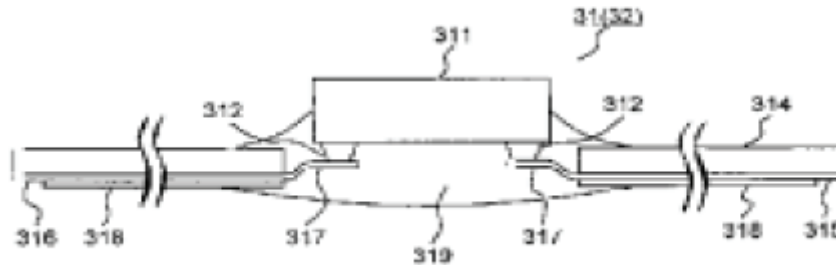
12. Claim 22

(“The electro-optical panel according to claim 10, wherein the mounting member is implemented as a flexible cable that is connected to the substrate over the clock signal input terminal and over the image signal input terminals.”)

215. This claim is obvious for the same reasons that [10e], [10f], [10h], [10j] and claims 16, 19, and 22 are. As discussed in [10h], it would have been obvious to modify Kitawada by using an external data drive circuit formed on a mounting member separate from the LCD panel’s first substrate. Kawaguchi and Nakanishi (and others) disclose such an external data drive circuit connected to the panel’s image signal input terminals using a flexible mounting member bonded with ACF. Nakanishi, Ex. 1010, Figures 1, 2; Kawaguchi, Ex. 1005, ¶[0055]. The ’146 patent admits that this was a “known” technique. Ex. 1001, 1:57-62.

216. For example, Kawaguchi discloses a flexible substrate (“base substrate 314”) and an external substrate (“mold 319”) that are different than the LCD panel’s first substrate:

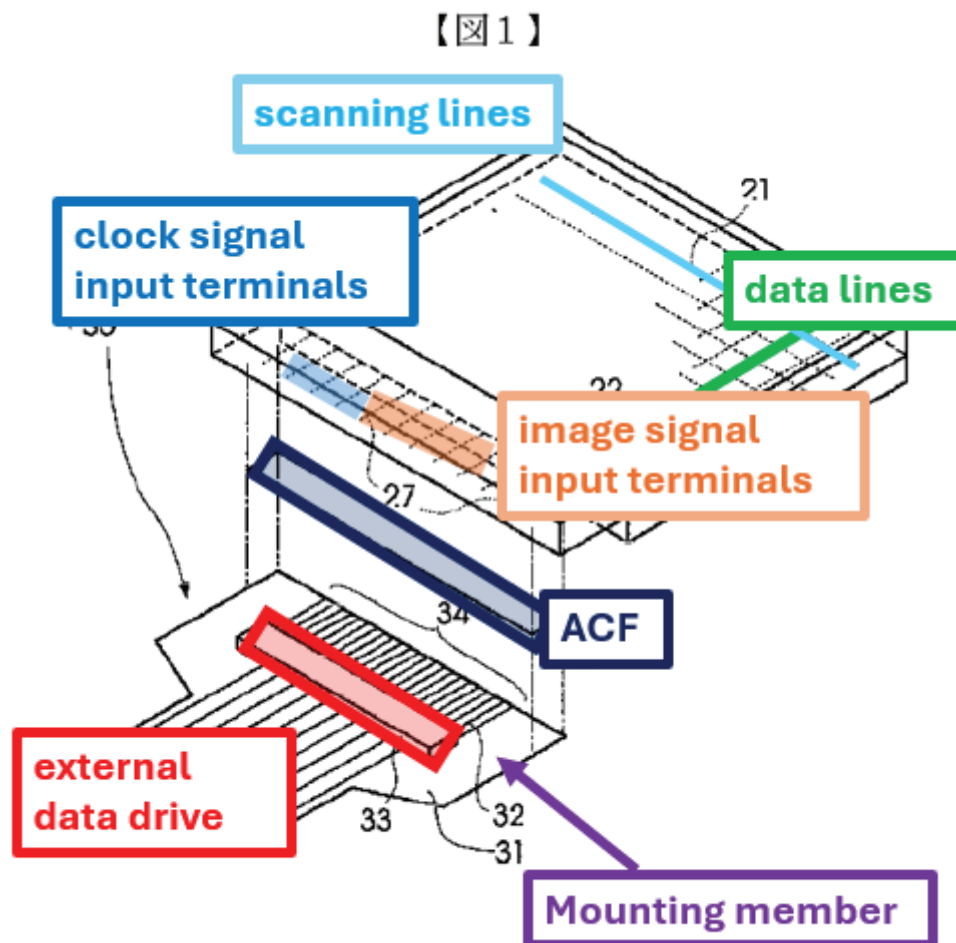
Figure 7

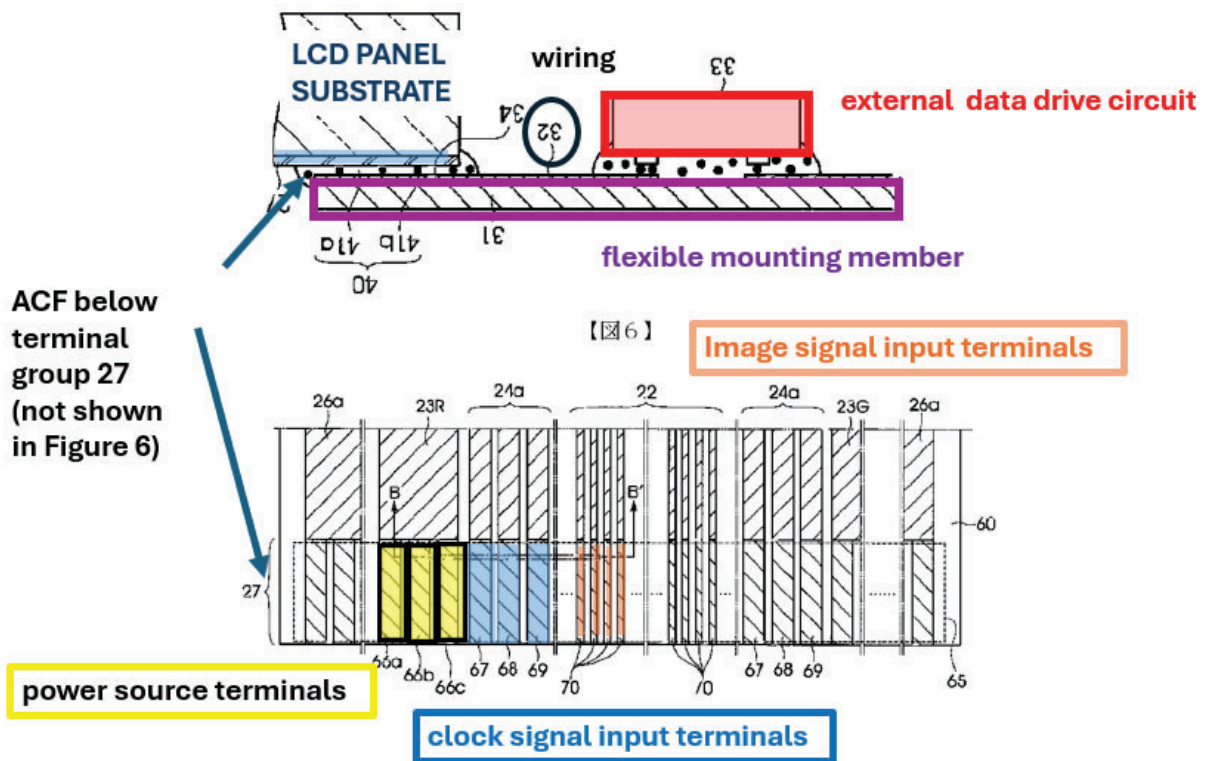


Ex. 1005, Figure 7; ¶[0051]. Kawaguchi’s flexible mounting member (which is a flexible cable as claimed) is connected to Kawaguchi’s LCD panel’s substrate (through ACF) over the clock signal input terminal and over the image signal input terminals. Ex. 1005, Figure 2 (showing terminal groups 21 and 22, including ‘x’ terminals for image signals and ‘y’ terminals that could receive clock signals for the scanning line drive circuit); ¶[0042] (“[A]t the lower edge of the substrate 11, an input terminal group 21 for the first panel 10A is provided, while at the upper edge of the substrate 11, an input terminal group 22 for the second panel 10B is provided.”); *id.* (“The input terminal group 21 includes: – Input terminals y1 to yk and input terminals yk+1 to yj, connected respectively to the scanning electrodes Y1 to Yk and Yk+1 to Yj of the first panel 10A, – Input terminals x1 to xi, connected respectively to the data electrodes X1 to Xi of the first panel 10A[.]”); ¶[0055] (“The connection between the output terminal group 316 of the first TCP

31 and the input terminal group 21 of the first panel 10A is made using an anisotropic conductive film (ACF)[.]”).

217. Similarly, Nakanishi discloses a flexible substrate (“flexible base substrate 31”) and an external substrate (“intermediate substrate 30”) that are different than the LCD panel’s first substrate. Ex. 1010, ¶[0018]. Nakanishi’s flexible substrate (which is a flexible cable as claimed) is connected to Nakanishi’s LCD panel’s substrate (through ACF) over the clock signal input terminal and over the image signal input terminals:





Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

218. As discussed above, Minami also discloses connecting terminals to wiring using ACF. Ex. 1007, Figure 2.

13. Claim 23

a. [23pre] – [23d]

([23pre]: “An electro-optical panel comprising”)

([23a]: “a substrate”)

([23b]: “data lines”)

([23c]: “scanning lines intersecting the data lines”)

([23d]: “pixels disposed corresponding to intersections between the data lines and the scanning lines”)

219. These elements are the same as claim 10's preamble through [10d], and are obvious for at least the same reasons. Additionally, the '146 patent admits that this technology was conventional. *See* §VII.A.1, *supra*.

b. [23e], [23f]

([23e]: “*a clock signal input terminal supplied with a clock signal*”)

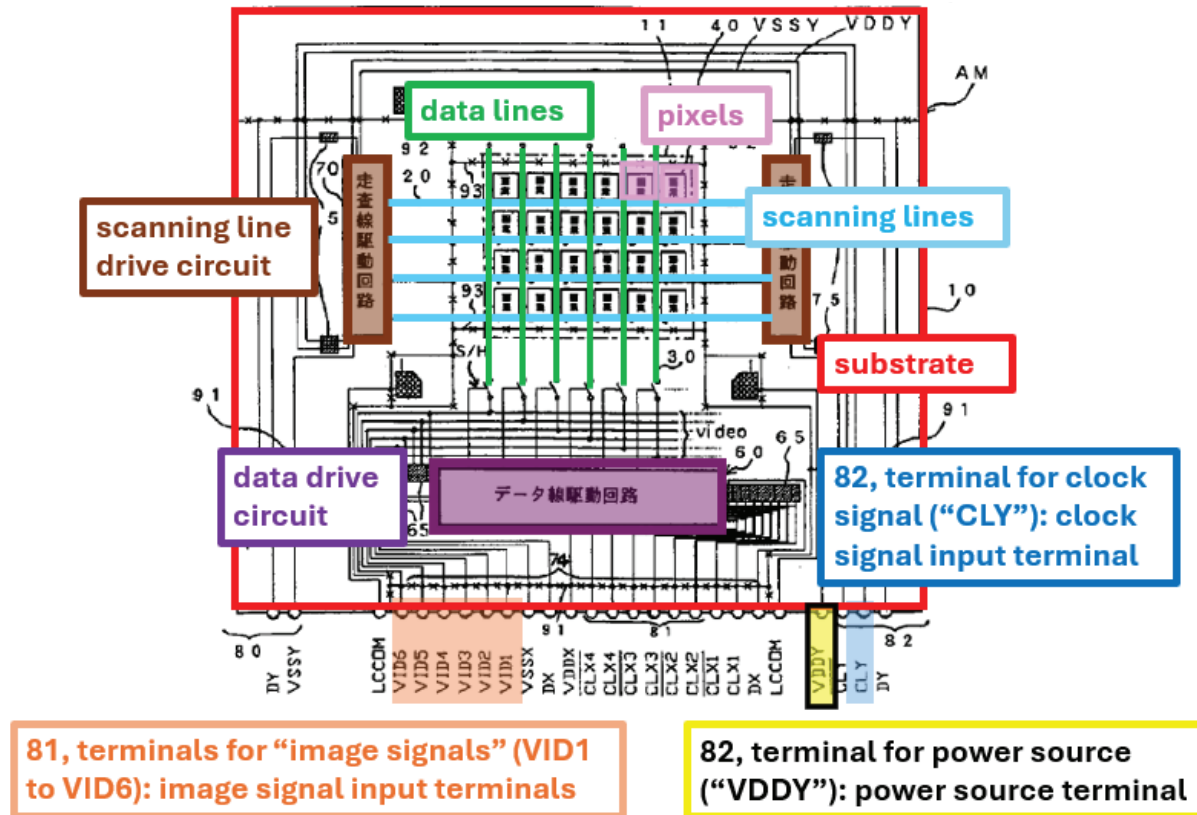
([23f]: “*an image signal input terminal supplied with an image signal*”)

220. [23e] and [23f] are the same as [10e] and [10f], respectively, without requiring connection to a mounting member through ACF, and they are thus obvious for at least the same reasons. Additionally, the '146 patent admits that this technology was conventional. *See* §VII.A.1, *supra*.

c. [23g]

([23g]: “*a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals*”)

221. As shown above in Ground 1 [10h] and [10i], Kitawada discloses and renders obvious a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals supplied from the data lines supplied to the pixels as selected by the scanning signals:



Ex. 1004, Figure 2.

222. See also ¶[0017] (“As shown in Figure 2, in the active matrix substrate AM with a built-in drive circuit used in the liquid crystal display device of the present invention, pixels 40 are arranged in a matrix on an insulating substrate 10 and connected to a plurality of scan lines 20 and data lines 30 that intersect each other. The scan lines 20 are composed of a tantalum film, an aluminum film, or an aluminum alloy film, etc., and the data lines 30 are composed of an aluminum film or an aluminum alloy film, etc., and each is formed as a single layer or a laminate. The region in which these pixels 40 are formed is the pixel portion 11 (screen display region).”), ¶[0018] (“data line drive circuit 60 is

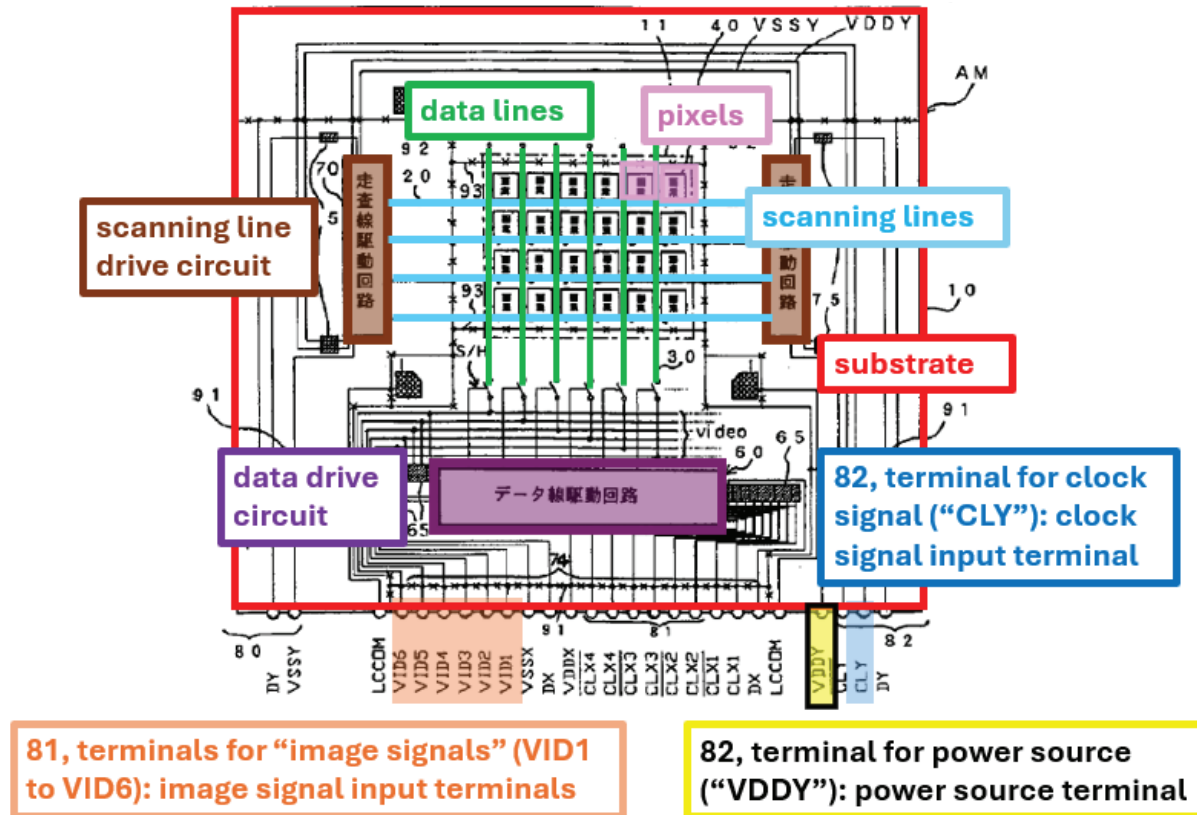
configured in the outer region (peripheral portion) of the pixel portion 11 on the insulating substrate 10 to supply video signals to each of the data lines 30. In addition, scan line drive circuits 70 are configured at the ends of each scan line 20 to supply scan signals for pixel selection to each scan line 20.”), ¶[0019] (“The data line drive circuit 60 comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6 expanded to six phases. In this example, the data line drive circuit 60 is configured with the X-side shift register circuit in a four-phase configuration, and start signal DX, clock signals CLX1 to CLX4, and their inverted clock signals CLX1 bar to CLX4 bar are supplied to the X-side shift register circuit via terminals, and the data line drive circuit 60 is driven by these signals. Therefore, the sample hold circuit S/H causes each TFT to operate based on the signal outputted from the X-side shift register circuit, and enables video signals VD1 to VD6 supplied via the video signal line to be captured at a predetermined timing and supplied to the data lines 30 and each pixel 40. Meanwhile, start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals.”), ¶[0020] (“In the active matrix substrate AM of the present embodiment, along the edges of the

insulating substrate 10, the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY, and a plurality of terminals 80, 81, 82, etc. composed of conductive films such as aluminum film, metal silicide films or ITO films, to which modulated video signals (image signals VD1 to VD6), and various drive signals, etc. are inputted. Multiple signal lines 74, 75 consisting of a low-resistance metal film such as aluminum film are drawn from these terminals 80, 81, 82, etc. to drive the data line drive circuit 60 and the scan line drive circuits 70. In addition, electrostatic protection circuits 65, 75, to be described later, are formed at intermediate positions between signal lines 74, 75. Note that the active matrix substrate AM and the opposing substrate (not shown) are supplied with the opposing electrode potential LCCOM inputted from outside via upper and lower conductive materials.”). Additionally, the ’146 patent admits that this technology was conventional. *See* §VII.A.1, *supra*.

d. [23h]

([23h]: “*wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate*”)

223. As shown in Ground 1 [10a]-[10g], Kitawada’s data lines, scanning lines, pixels, clock signal terminal, and image signal terminal are on the substrate.



Ex. 1004. Figure 2; ¶[0020].

e. [23i]-[23k]

([23i]: "a mounting member that is distinct from and connected to the substrate, the mounting member comprising")

([23j]: "a first wiring that is connected to the clock signal input terminal")

([23k]: "a second wiring that is connected to the image signal input terminal")

224. As shown above in Ground 1 [10e], [10f], [10h], and claims 16 and 19, it would have been obvious to modify Kitawada to use a mounting member distinct from and connected to the LCD panel's substrate, with the mounting member comprising a first wiring (supplying clock signals) connected to the clock signal input terminal (e.g., through ACF) and a second wiring (supplying image

signals) connected to the image signal input terminal (e.g., through ACF).

Additionally, this technology is admittedly conventional. *See* §VII.A.1, *supra*.

f. [23I]

(“wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member”)

225. This element is the same as [10 j] in Ground 1, but does not require that the overlap be “through said anisotropic film,” and is therefore obvious for at least the same reasons.

B. Ground 2: Claims 1-9 are Obvious over Kitawada in view of Kawaguchi, Matsumoto, Sano or Minami, and optionally Kato

1. Claim 1

a. [1pre] – [1c]

[1pre]: *“An electro-optical panel comprising”*)

[1a]: *“a plurality of data lines”*)

[1b]: *“a plurality of scanning lines intersecting the plurality of data lines”*)

[1c]: *“a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines”*)

226. The preamble through [1c] are materially the same as [10pre], and [10b]-[10d], respectively, and are obvious for at least the same reasons. *See* Ground 1.

b. [1d], [1e]

[1d]: *“a clock signal input terminal supplied with a scanning line clock signal”*)

[1e]: *“an image signal input terminal supplied with an image signal”*)

227. [1d] and [1e] are the same as [10e] and [10f], respectively, but without requiring connection to a mounting member through ACF, and are obvious for at least the same reasons. *See* Ground 1.

c. [1f]

([1f]: “*a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals*”)

228. As shown in [10i] and [23g] in Ground 1, Kitawada discloses and renders obvious (alone and/or in view of Kawaguchi) a scanning-line drive circuit that is formed on the first substrate and sequentially transmits a transmission start pulse in synchronization with the clock signal. Kitawada’s scanning-line drive circuit outputs a scanning signal to each of the scanning lines. Ex. 1004, ¶¶[0017]-[0020]. Similarly, Kawaguchi’s scanning-line drive circuit outputs a scanning signal to each of the scanning lines. Ex. 1005, ¶¶[0032]-[0034]. And as shown in [10h] and [23g], Kitawada discloses and renders obvious image signals from the plurality of data lines are supplied to pixels selected by the scanning signals.

Additionally, this technology is admittedly conventional. *See* §VII.A.1, *supra*.

d. [1g]

([1g]: “*a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal*”)

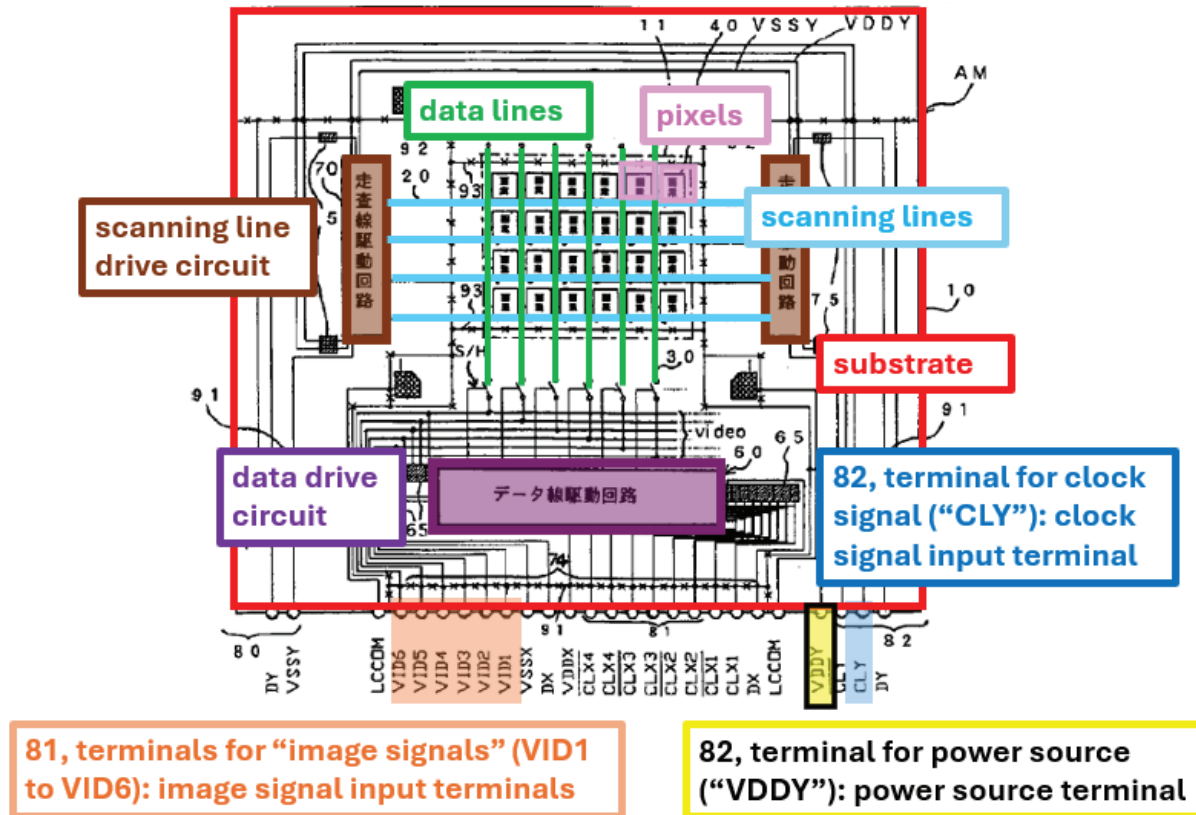
229. As shown in [10h] and [10i] in Ground 1, Kitawada discloses and renders obvious image signals being supplied from a data drive circuit and a scanning-line drive circuit that sequentially transmits a transmission start pulse in

synchronization with the clock signal. A POSITA would readily understand that Kitawada's data drive circuit "controls a grayscale of the pixels based on the scanning line clock signal and the image signal" as claimed. See §§VI.D.1 and IX.B above; *also* Ex. 1018, ¶[0004] ("[A] conventional optical switching element . . . comprises polarizers . . . , glass plates . . . , transparent electrodes . . . , and a liquid crystal . . . , so that when a voltage is applied between the transparent electrodes, the direction of liquid crystal molecules is changed to rotate the surface of polarization, resulting in optical switching. A conventional image display device comprises a liquid crystal panel having such optical switching elements (liquid crystal cells) arranged in a two-dimensional form, in which the direction of liquid crystal molecules is controlled by adjusting the applied voltage to achieve grayscale."). Additionally, this technology is admittedly conventional. See §VII.A.1, *supra*.

e. [1h]

([1h]: "a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal")

230. Kitawada discloses a power source input terminal (82, terminal for power source "VDDY") supplied with a power source ("VDDY"):



Ex. 1004, Figure 2; ¶[0020]. Kitawada does not expressly disclose the area of the power input terminal, but it would have been obvious that its area is not less than that of the clock signal input terminal.

231. **First**, Kitawada’s power source terminals are near the outer side of the substrate and should thus have a relatively larger area (according to Minami, Nakanishi, and Mismatch Analysis Report) to mitigate known problems such as terminal-to-wiring mismatch and weakened ACF bonding strength. *See* §X, *supra*. Kitawada’s power source terminals are directly adjacent to its clock signal input terminals in terminal group 82. *See* Ex. 1004, Figures 1A and 2. Thus, it would have been an obvious design choice that the power source terminals should not be

smaller than the adjacent clock signal input terminals. This also would have enhanced the engineering simplicity of the design, as a POSITA would not have wanted to change the terminal width/area or pitch interval more times than necessary. Once there was a change to the terminal pad width / area for the VDDY power source (*i.e.*, increasing its area), there would have been no good reason to change it again for the clock signals (CLY, inverted CLY, DY) terminals, which are adjacent to the power source terminal

232. ***Second***, power terminals should have a larger area to lower their resistance to conduct “larger currents” per Kato. *See* §X, *supra*. A POSITA knew that a power source terminal’s currents are at least as large as a clock signal input terminal’s currents, so it would have been obvious that the former terminals have “not smaller” areas.

f. [1i]

([1i]: “***wherein the clock signal input terminal has a larger area than the image signal input terminal***”)

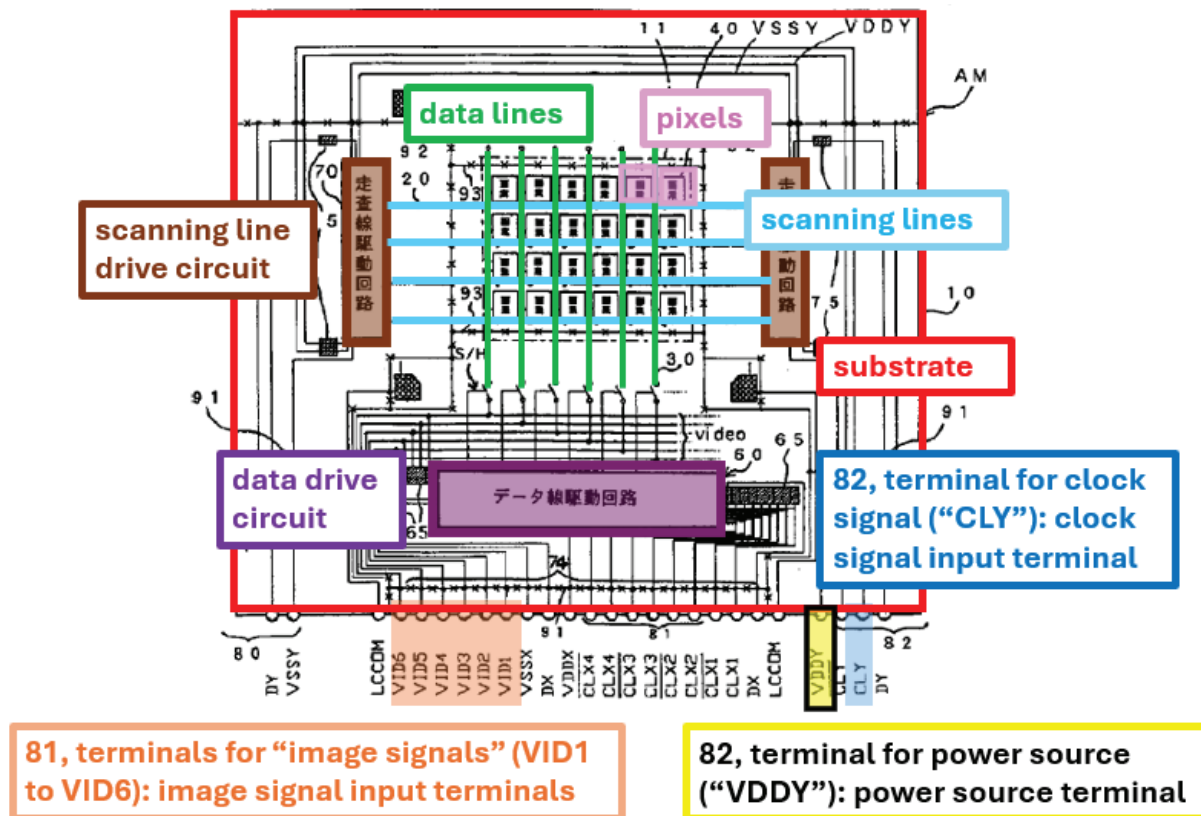
233. As shown in [10j] in Ground 1, it would be obvious to modify Kitawada so that its clock signal input terminal has a larger area than its image signal input terminal.

g. [1j], [1k]

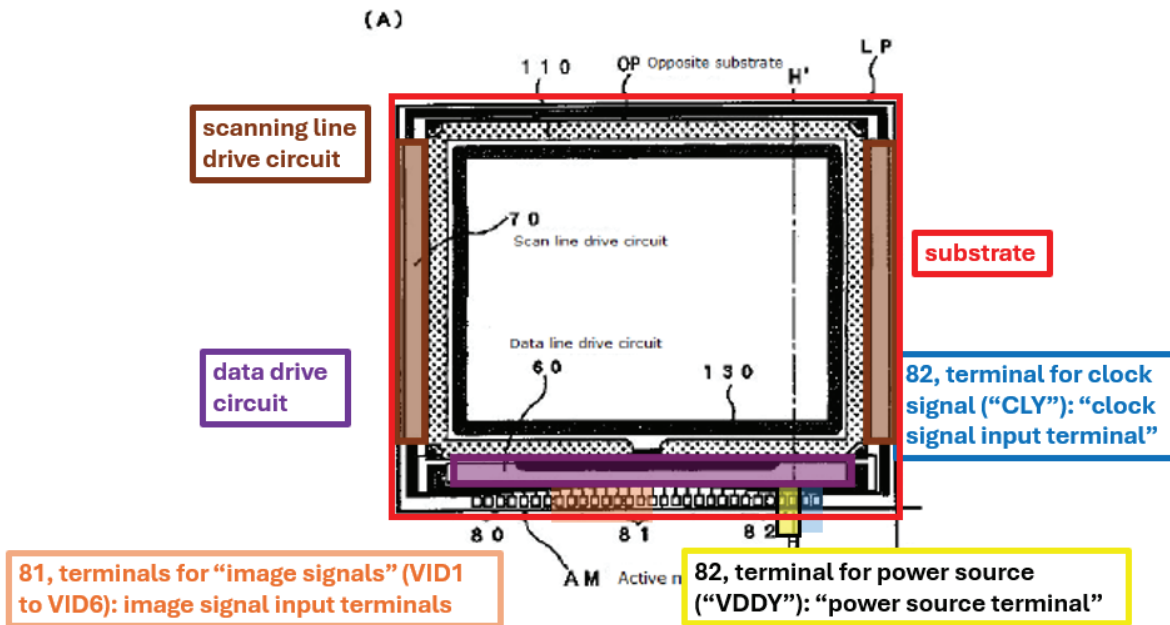
([1j]: “***wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included***”)

([1k]: “the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate”)

234. Kitawada discloses a plurality of power source terminals (82, terminal for “VDDY”; 81, terminals for “VDDX” and “VSSX”), clock signal input terminals (82, terminals for “CLY” and inverted CLY), and image signal input terminals (81, terminals for “VID1” through “VID6”) formed in line on the LCD panel’s substrate:



[FIG. 1]



Ex. 1004, Figure 2 and Figure 1(A); ¶[0020]; *see also* Ground 1, [10g].

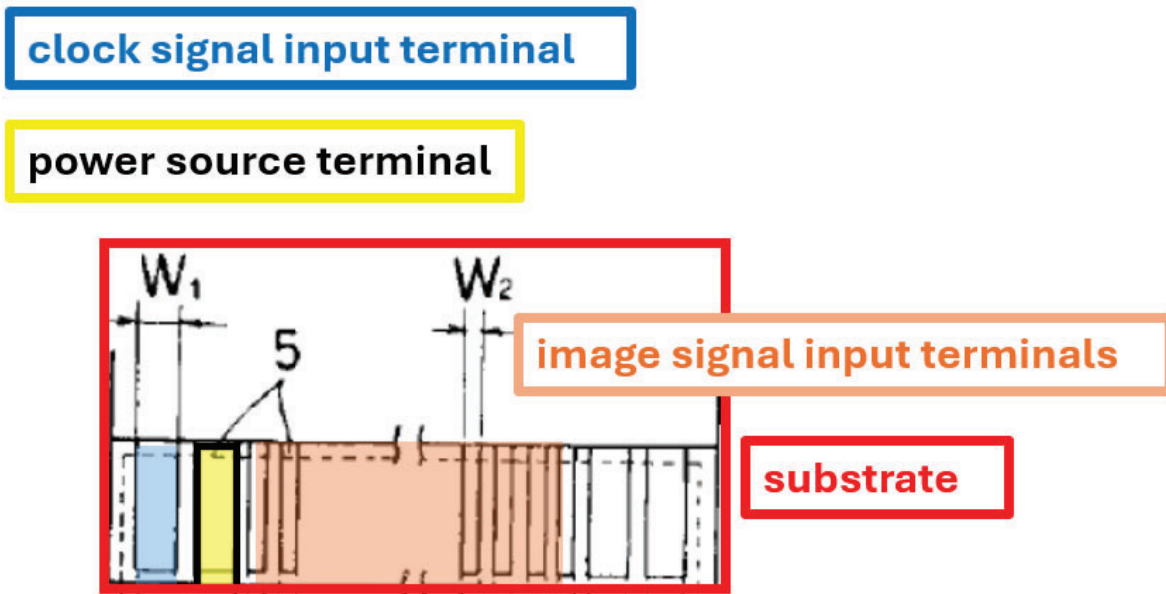
h. [11]

([11]: “a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals”)

235. It would have been obvious to increase the area of Kitawada’s clock signal terminals relative to the area of its image signal input terminals. *See* Ground 1 [10j]. It follows that it would have been an obvious to use a pitch interval for adjacent clock signal input terminals that is a multiple of the pitch interval of adjacent (smaller) image signal input terminals—whether that multiple be an integer or otherwise. In fact, the ’146 patent does not disclose any reason for using an integer multiple, it only states that this is “preferable.” Ex. 1001, 9:9-11. And

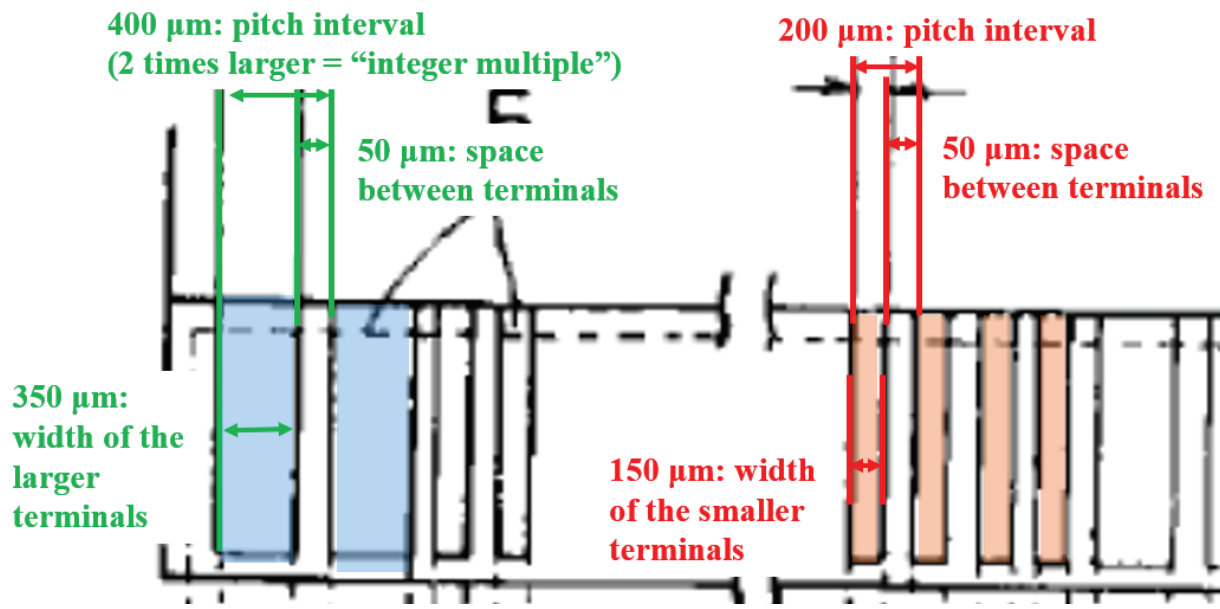
the patent does not disclose any unexpected results or benefits resulting from using an integer multiple pitch interval.

236. Further, Minami discloses that terminals located near the outside of the substrate (corresponding to Kitawada's clock signal input terminals) should have a larger area than the terminals closer to the center of the substrate (corresponding to Kitawada's image signal terminals) when a display requires "high-density terminal pitch connections . . . between the drive circuit board and the display unit." Ex. 1007, at 1. "When the pitch is approximately 100 to 200 μm , the bonding area between the anisotropic conductive film and the LCD panel electrode terminals is small, resulting in a decrease in bonding strength and bond delamination due to external pressure after connection." *Id.* In Figure 3, the "width of the connection pattern is 150 μm for the pattern width W2 at the center, and the pattern width W1 near both ends on the LCD panel 1 side is 2 to 5 times the width of the connection pattern at the center, for example 500 μm ." *Id.* at 2:



Ex. 1007, Figure 3.

237. Since the pitch interval can be “200 μm ” and the “width of the connection pattern is 150 μm for the pattern width W_2 at the center,” the space between the narrow terminals is 50 μm (*i.e.*, $200 \mu\text{m} - 150 \mu\text{m} = 50 \mu\text{m}$). Therefore, if the wider terminals near the ends of the panel are 350 μm wide (within the range of “2 to 5 times the width of the connection pattern at the center”), then the pitch interval of the adjacent wider terminals is 400 μm (*i.e.*, 350 μm terminal width + 50 μm space between terminals):



Ex. 1007, Figure 3. Thus, the pitch interval of the wider terminals (400 μm) would be twice the pitch interval of the narrower terminals (200 μm), which is an “integer multiple” as claimed. As explained previously, a POSITA would have been motivated to modify Kitawada using Minami’s teachings.

238. Further, in the field of semiconductor chip pads, “varying pad pitch between pads” was known. Pat. No. 5,155,065, Ex. 1023, 2:37-45. Similar to terminals used in an LCD display, a pad array “is an external interface of a semiconductor chip for coupling signals to the semiconductor chip. *Id.*, 1:8-10. This technology is analogous to the claimed technology; indeed, the active matrix display industry grew out of the semiconductor industry, not out of the (segmented) liquid crystal industry. And all design and manufacturing processes for AMLCD (except the LCM fill) were ported over from the semiconductor industry. Further, active matrix design rules (including pad width and spacing

rules) were conceptually ported over from the semiconductor industry. Among other benefits of varying pad pitch, it could “shorten development time, minimize need for customization, reduce cost, allow current developments to be used with next generation process flows, and give customers a choice on using different package technologies.” Ex. 1023, 2:25-34. The same benefits would apply to varying terminal pitch interval in an LCD display. Adjustable pad pitch was achieved using a reference “grid size” where “pad widths and pad spacings are integer multiples of the grid size.” Ex. 1023, 6:22-33 and claim 1 (“... defining an incremental pad pitch, wherein predetermined pads in the row of pads can be contacted at pad pitch equal to the minimum pad pitch plus an integer multiple of the incremental pad pitch . . .”). This would result in some pad pitch intervals being an integer multiple (*e.g.*, two times or three times) of other pad pitch intervals. The pitch interval of LCD input terminals could easily be adjusted in the same way, and a POSITA would have been motivated to do so because using integer multiple pitch intervals could make manufacturing easier while satisfying design rules and still allowing for varying pitch intervals. Indeed, as shown above, Minami discloses a pitch interval for the wider terminals (400 μm) that is twice as large as the pitch interval of the narrower terminals (200 μm).

2. Claim 2

(“An electro-optical panel according to claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.”)

239. See Ground 1, claim 11.

3. Claim 3

(“An electro-optical panel according to claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.”)

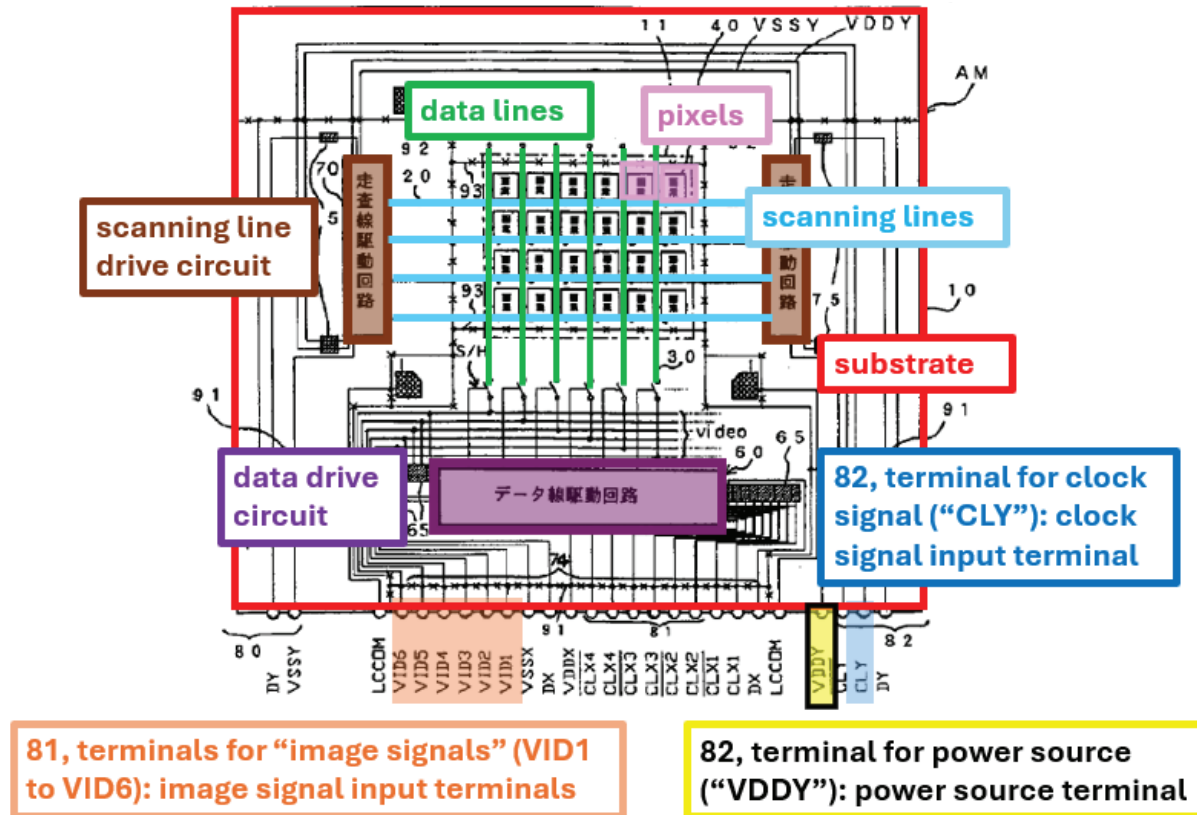
240. Kitawada discloses “start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals.” Ex.

1004, ¶[0019]; also ¶[0020] and Figure 2; [10i] in Ground 1.

4. Claim 4

(“An electro-optical panel according to claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.”)

241. Kitawada discloses claim 4:



Ex. 1004, Figure 2; ¶[0020]; *see* Ground 1, claim 12.

5. Claim 5

(“An electro-optical apparatus comprising: an electro-optical panel set forth in claim 1; power source means for supplying the power source; and signal generation means for supplying the input signals.”)

242. Kitawada discloses (at least inherently or implicitly) and renders obvious a power source means because “the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY” and by the principle of the conservation of energy, those power supplies must be provided by a power source means. Ex. 1004, ¶[0020]. Thus, as a POSITA understands, it is obvious that there must be power source means to supply “constant power supplies VDDX, VSSX, VDDY, VSSY.” Moreover, the

specification admits that “means for supplying the power source, etc., to the electro optical panel ... are known.” Ex. 1001, 1:51-62.

243. Kitawada’s power source means is the same or equivalent to “power source circuit” 500 shown in Figure 5 of the ’146 patent, as both perform substantially the same function, in substantially the same way, to achieve substantially the same result. Power source circuit 500 in the ’146 patent “supplies a predetermined power source to the timing generation circuit 300 and the image processing circuit 400 in addition to supplying a high potential power source VDD and a low potential power source VSS to the scanning-line drive circuit 100.” Ex. 1001, 10:9-13. Similarly, Kitawada discloses “the edge portion on the side with the data line drive circuit 60 includes constant power supplies VDDX, VSSX, VDDY, VSSY.” Ex. 1004, ¶[0020].

244. And Kitawada discloses and renders obvious signal generation means for supplying the input signals. A POSITA would understand that there inherently must be signal generation means to supply “video signals VD1 to VD6.” Ex. 1004, ¶[0019] (“The data line drive circuit 60 comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6 expanded to six phases. In this example, the data line drive circuit 60 is configured with the X-side shift

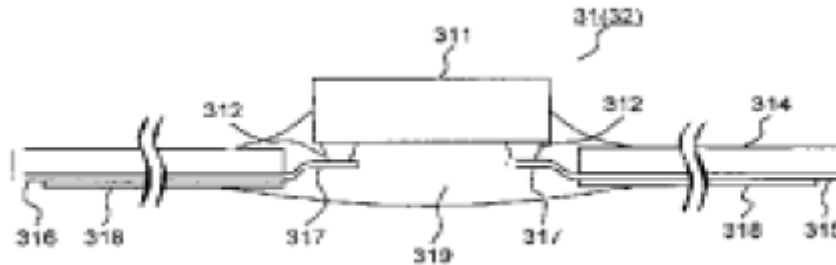
register circuit in a four-phase configuration, and start signal DX, clock signals CLX1 to CLX4, and their inverted clock signals CLX1 bar to CLX4 bar are supplied to the X-side shift register circuit via terminals, and the data line drive circuit 60 is driven by these signals. Therefore, the sample hold circuit S/H causes each TFT to operate based on the signal outputted from the X-side shift register circuit, and enables video signals VD1 to VD6 supplied via the video signal line to be captured at a predetermined timing and supplied to the data lines 30 and each pixel 40. Meanwhile, start signal DY, clock signal CLY, and inverted clock signal CLY bar are supplied from outside via terminals to the scan line drive circuits 70, and the scan line drive circuits 70 are driven by these signals.”); *see also* ¶[0020]. Alternatively, the voltage made available to (and stored on) each data line amounts to a grayscale analog signal; thus, the data line drive circuit (which “comprises an X-side shift register circuit, a sample hold circuit S/H equipped with TFTs that function as analog switches based on signals outputted from the X-side shift register circuit, and six video signal lines corresponding to each of the video signals VD1 to VD6” (Ex. 1004, ¶[0019]) is a signal generation means.

245. A POSITA would also understand that there inherently must be signal generation means to supply any other input signal into Kitawada, including the various clock signals and power source signals shown in Figure 2 and discussed previously. Kitawada’s signal generations means is at least equivalent to the

structure disclosed in the '146 patent and renders claim 5 obvious. The '146 patent states that, in its Figure 5, “the data-line drive circuit 200, the timing generation circuit 300, and the image processing circuit 400 function as signal generation means for supplying input signals to the liquid crystal panel AA.” Ex. 1001, 10:13-17; *see also* 9:40-10:17. Kitawada’s signal generations means performs substantially the same function (*i.e.*, supply input signals), in substantially the same way (*i.e.*, the input signals come in to the LCD display via input terminals on the substrate), to achieve substantially the same result (*i.e.*, control the operation of the LCD display by providing power, clock signals, and video signals). *See* Ex. 1004, ¶[0019] and §IX.B above.

246. Many other prior art references also disclose external power source and signal generation means on a mounting member that is connected to input terminals on the LCD panel’s substrate. The claimed technology was conventional and, to the extent it is argued or determined that Kitawada fails to disclose or render this claim obvious, Kitawada in view of other prior art renders the claim obvious. For example, as discussed in Ground 1, Kawaguchi discloses a flexible substrate (“base substrate 314”) and an external substrate (“mold 319”) that are different than the LCD panel’s first substrate:

Figure 7



Ex. 1005, Figure 7; ¶[0051]. Kawaguchi's flexible mounting member is connected to Kawaguchi's LCD panel's substrate (through ACF) over the clock signal input terminal and image signal input terminals. Ex. 1005, Figure 2 (showing terminal groups 21 and 22, including 'x' terminals for image signals and 'y' terminals that could receive clock signals for the scanning line drive circuit); ¶[0042], [0055].

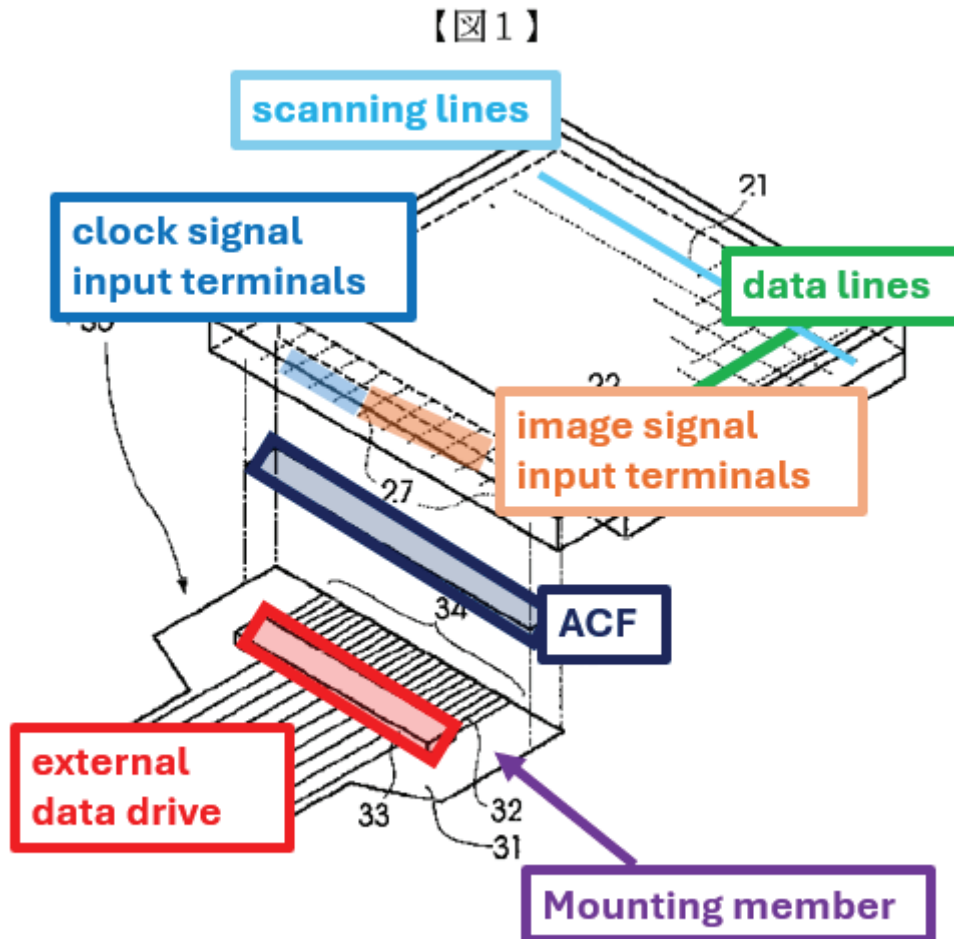
Kawaguchi's Tape Carrier Package (TCP, 31 shown in Figure 7 above) comprises external drive circuitry having signal generation means. Ex. 1005, ¶[0029].

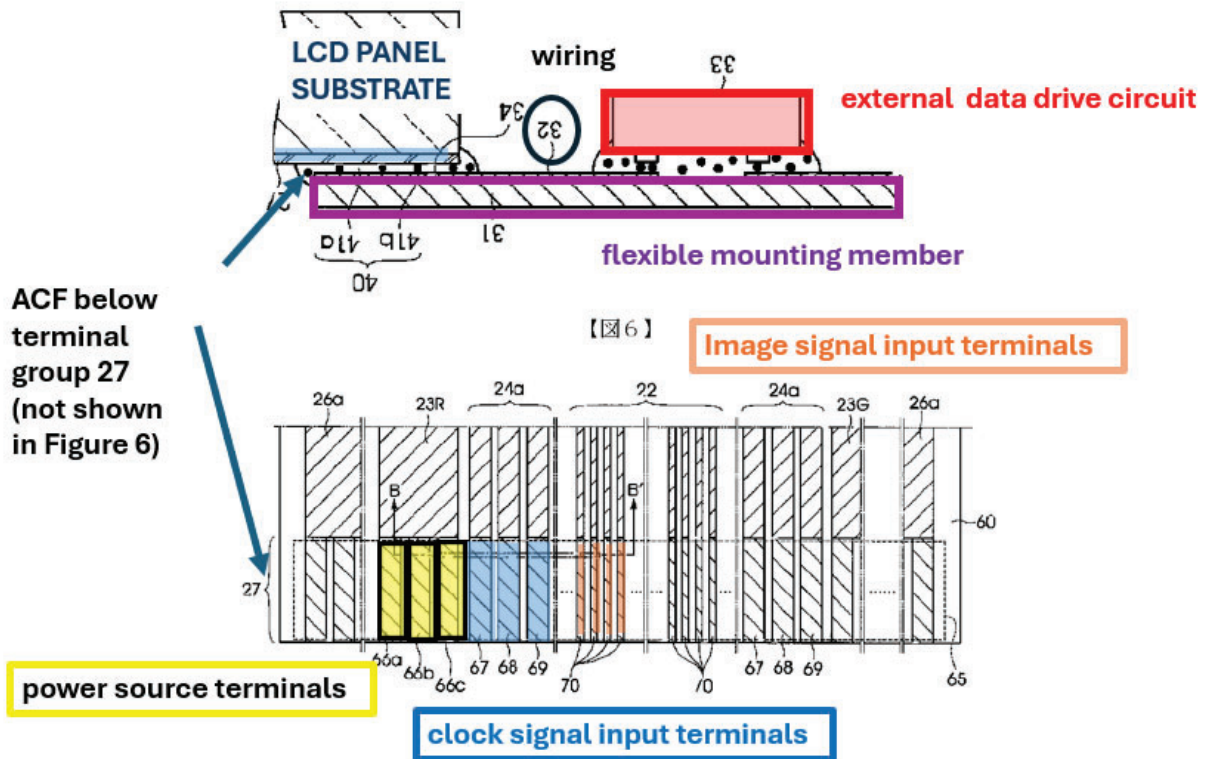
Kawaguchi also discloses "a control circuit 120, and a power supply circuit 130."

¶[0026]. The "control circuit 120 generates the Y shift start pulse YS, Y shift clock YCLK, control signal CTLY, X shift start pulse XS, X shift clock XCLK, gradation data Da, and control signal CTLX described above." ¶[0038].

247. Similarly, Nakanishi discloses a flexible substrate ("flexible base substrate 31") and an external substrate ("intermediate substrate 30") that are different than the LCD panel's first substrate. Ex. 1010, ¶[0018]. Nakanishi's

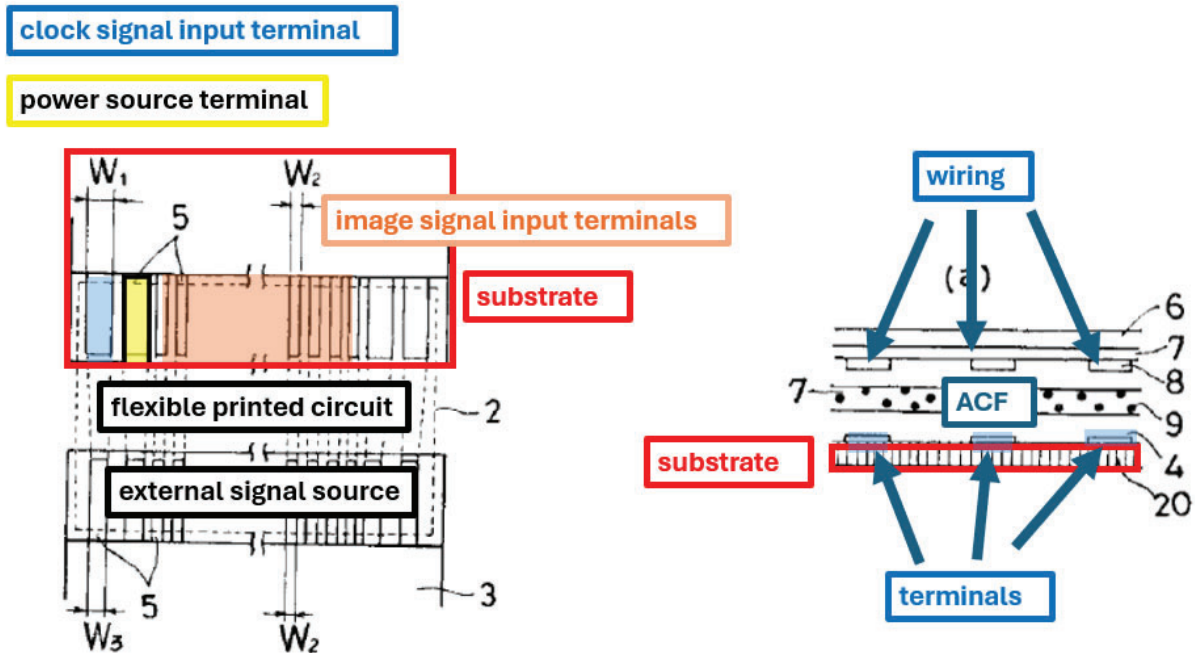
flexible substrate is connected to Nakanishi's LCD panel's substrate (through ACF) over the clock signal input terminals, the image signal input terminals, and the power source terminals:





Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022]. Component 33 in Nakanishi comprises “semiconductor chips.” ¶[0018]. “The semiconductor chips mounted on the intermediate substrate 30 include the data drive circuits 33a, cathode power supply circuits 33b, and light-emitting power supply circuits 33c shown in FIG. 3.” Ex. 1010, ¶[0052].

248. Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit through ACF, confirming that it would have been obvious to connect external power source means and signal generation means (like those disclosed by Kitawada, Kawaguchi, and Nakanishi) to input terminals on an LCD panel’s substrate:



Ex. 1007, Figures 3 and 2a; page 14 of 18 (“FIG. 2 (a) shows the state of each material prior to thermal compression bonding, and FIG. 2 (b) shows the state after thermal compression bonding. An anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7. The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).”).

249. Using ACF in this manner was conventional. The ’146 patent admits that displays like those recited in the claims were “known” (Ex. 1001, 1:17-62) and admits that “means for supplying the power source, etc. to the electro-optical

panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.” *Id.* at 1:51-62.

6. Claim 6

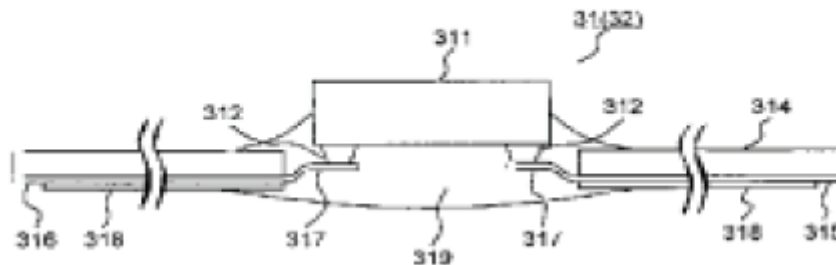
(“An electro-optical apparatus comprising: an electro-optical panel set forth in claim 5; an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and a flexible substrate which connects the external substrate and the electro-optical panel, wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.”)

250. As discussed in [10e], [10f], [10h], and claims 16 and 19-22 in Ground 1, it would have been obvious to modify Kitawada to utilize an external substrate containing an external data circuit for supplying image signals, with the external substrate comprising a flexible substrate connected to the LCD panel’s plurality of input terminals through ACF. For similar reasons, it would have been obvious to use an external substrate including the “power source means” and “signal generation means” recited in claim 5, because there are a finite number of ways to include such means (*e.g.*, implementing them on the LCD’s panel’s substrate or on an external substrate) and there were known technical benefits of using an external substrate for such components. As explained above in [10e], [10f], [10h], and claims 16 and 19-22 in Ground 1, it would have been obvious that such an external substrate would include a flexible substrate to connect to the LCD panel’s substrate via connection to Kitawada’s power source terminals, clock

signal input terminals, and image signal input terminals (*see* Kitawada, Ex. 1004, Figure 2, ¶[0020]) through ACF.

251. And as discussed in Ground 1, Kawaguchi discloses a flexible substrate (“base substrate 314”) and an external substrate (“mold 319”) that are different than the LCD panel’s first substrate:

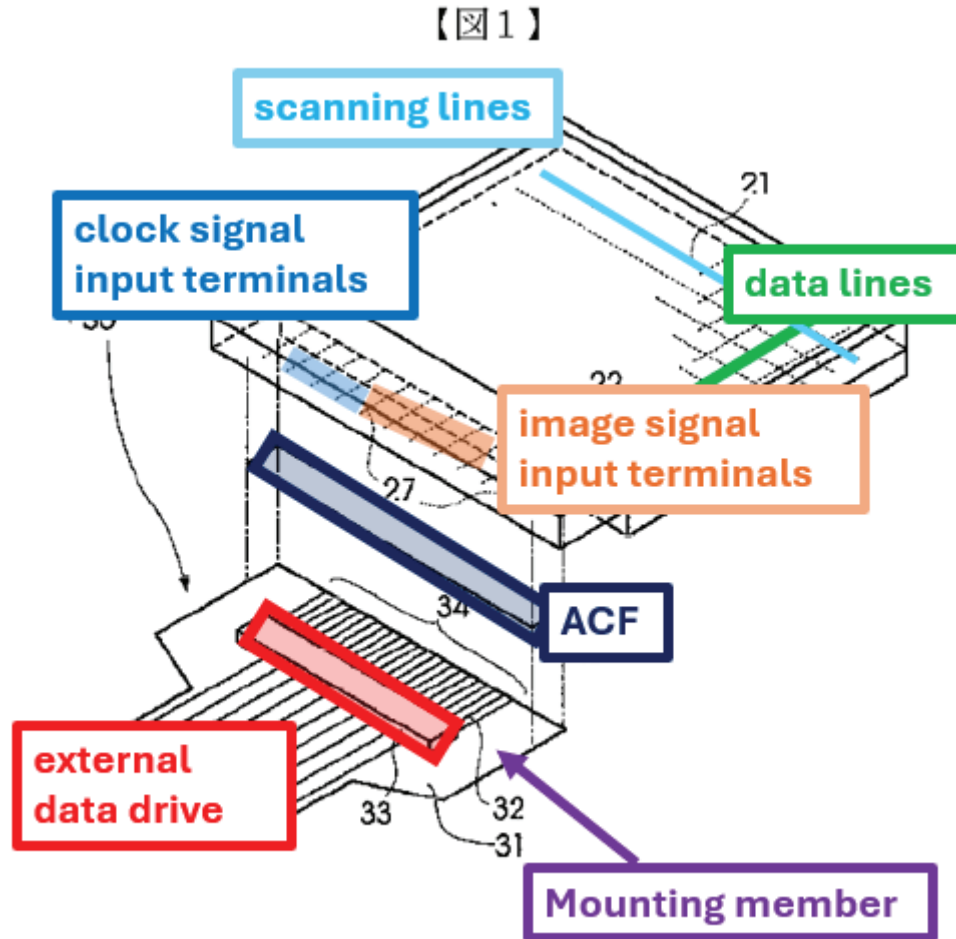
Figure 7

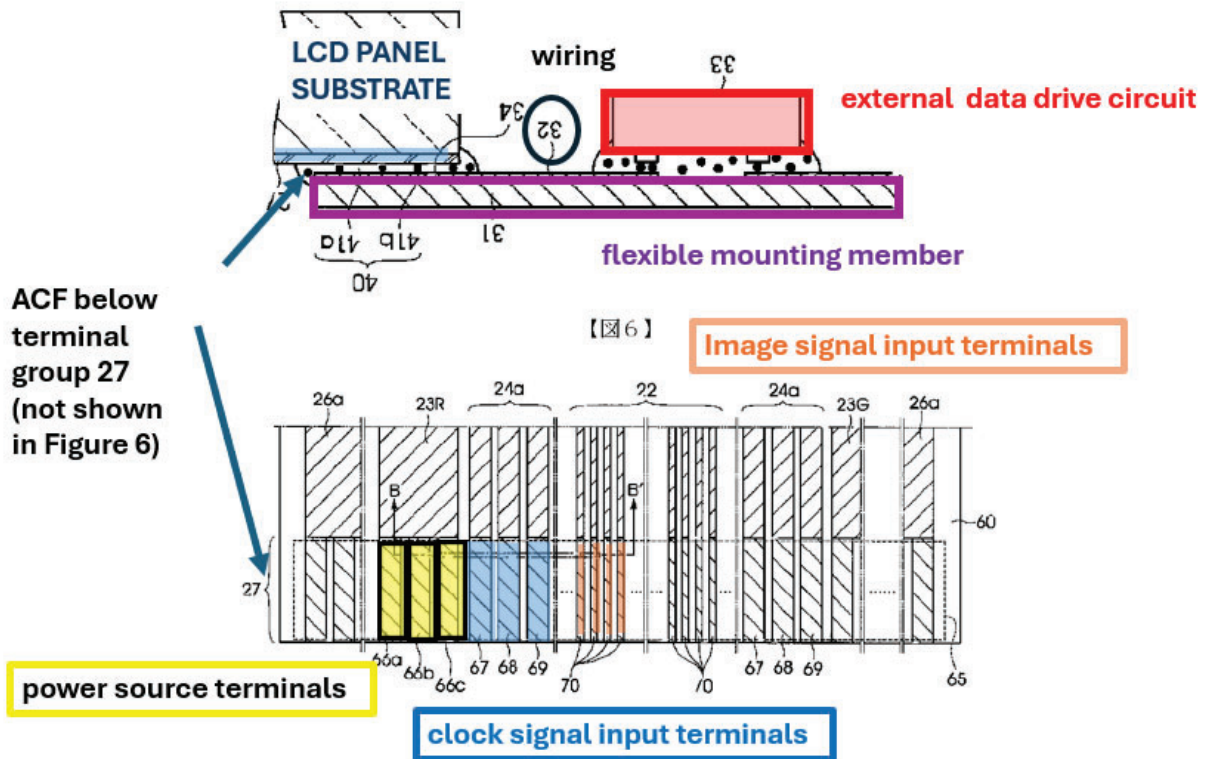


Ex. 1005, Figure 7; ¶[0051]. Kawaguchi’s flexible mounting member is connected to Kawaguchi’s LCD panel’s substrate (through ACF) over the clock signal input terminal and image signal input terminals. Ex. 1005, Figure 2 (showing terminal groups 21 and 22, including ‘x’ terminals for image signals and ‘y’ terminals that could receive clock signals for the scanning line drive circuit); ¶¶[0042], [0055].

252. Similarly, Nakanishi discloses a flexible substrate (“flexible base substrate 31”) and an external substrate (“intermediate substrate 30”) that are different than the LCD panel’s first substrate. Ex. 1010, ¶[0018]. Nakanishi’s flexible substrate is connected to Nakanishi’s LCD panel’s substrate (through

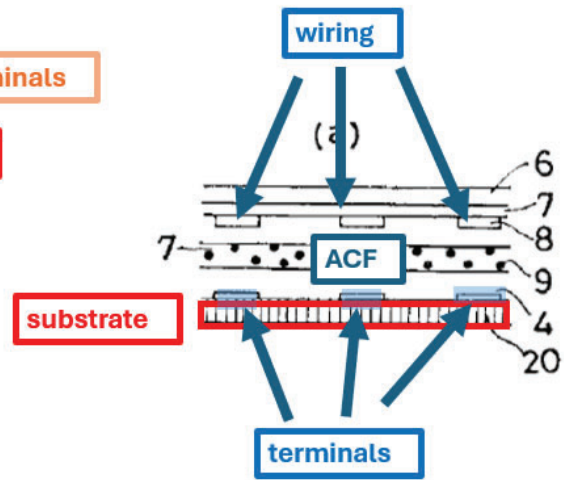
ACF) over the clock signal input terminals, the image signal input terminals, and the power source terminals:





Ex. 1010, Figures 1, 2, 6; ¶¶[0019]-[0022].

253. Similarly, Minami teaches using ACF to connect input terminals to a flexible printed circuit through ACF:



Ex. 1007, Figures 3 and 2a; page 14 (“FIG. 2 (a) shows the state of each material prior to thermal compression bonding, and FIG. 2 (b) shows the state after thermal compression bonding. An anisotropic conductive film, such as one made of carbon fibers 9, is interposed between a glass substrate 20 on which an ITO film 4 has been formed and a polyimide film 6 on which a copper pattern 8 has been formed via an adhesive layer 7. The connection portion is then subjected to thermal compression bonding at approximately 170 to 250 °C, resulting in a state in which each material is connected as shown in FIG. 2 (b).”).

254. Using ACF in this manner was conventional. The '146 patent admits that displays like those recited in the claims were “known” (Ex. 1001, 1:17-62) and admits that “means for supplying the power source, etc. to the electro-optical

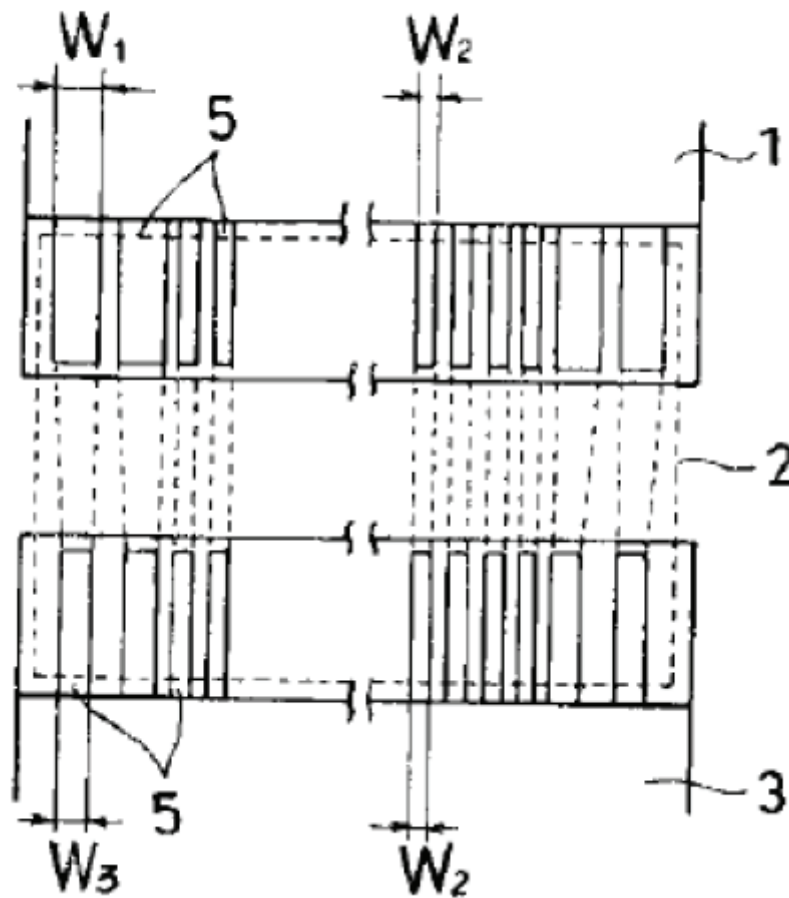
panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible substrate as a connection cable through an anisotropic conductive film are known.” *Id.* at 1:51-62. These admissions underscore that it would have been obvious to connect Kitawada’s clock-signal input terminals to a “flexible wiring substrate,” (Ex. 1004, ¶[0029]) through ACF.

7. Claim 7

(“An electro-optical apparatus according to claim 6, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.”)

255. It would have been obvious to modify Kitawada such that image signal wiring lines in the flexible substrate are formed corresponding to a reference pitch interval of the image signal input terminals. Minami discloses that terminals near the center of the substrate (corresponding to Kitawada’s image signal input terminals) should have a narrow width (“W2”) and a pitch interval that matches the pitch interval of the wirings in flexible printed circuit 2 and printed wiring board 3:

FIG. 3



Ex. 1007, Figure 3. This figure is like Figure 4 of the '146 patent, which shows that every narrow input terminal overlaps with one wiring line ("L"). Ex. 1001, Figure 4. It would have been obvious to use the pitch interval of image signal input terminals as a "reference pitch" because they have the smallest pitch interval, which, per Minami, matches the interval of the fine pitch wiring (*e.g.*, in the flexible printed circuit / printed wiring board).

8. Claim 8

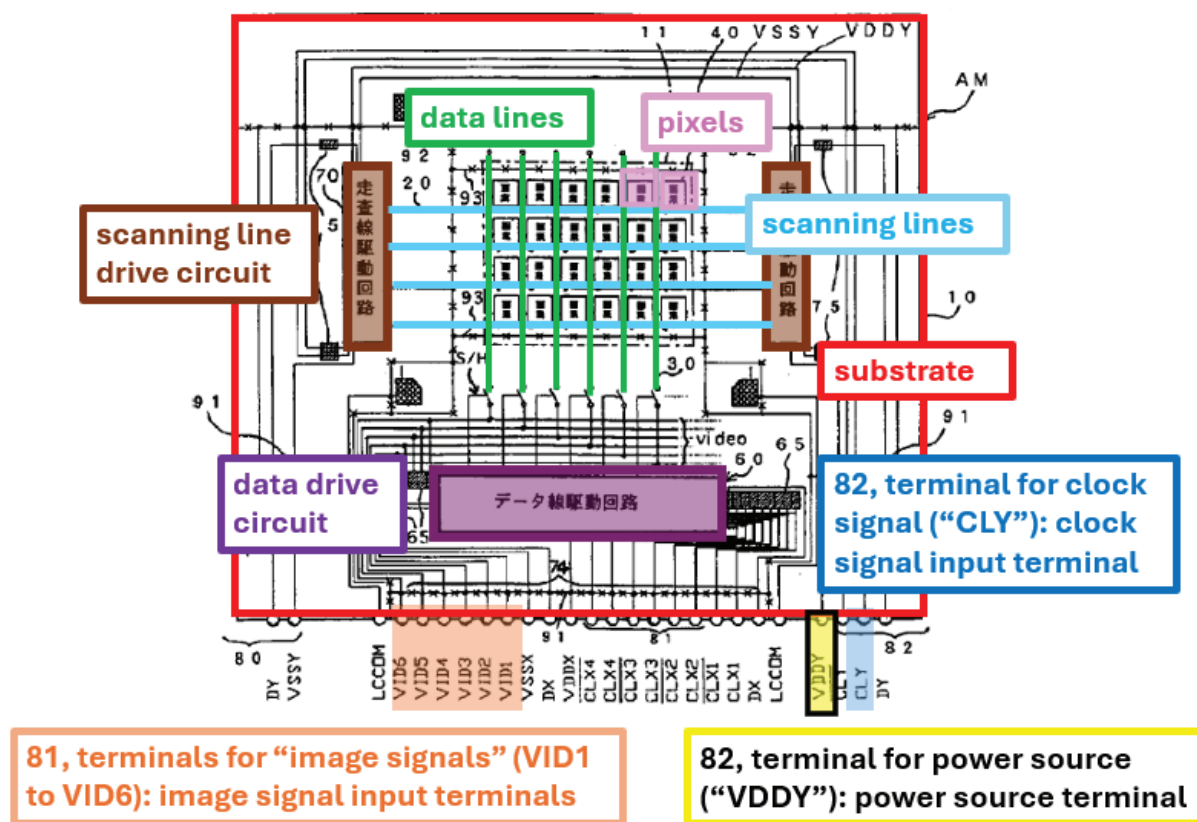
(“An electronic system comprising the electro-optical apparatus set forth in claim 1.”)

256. Kitawada discloses and renders it obvious to use the display of claim 1 in an electronic system. Ex. 1004, claim 7 (“A liquid crystal display device using the active matrix substrate according to claim 6.”). Further, a POSITA would have been away of many applications for LCD displays like those disclosed by Kitawada. For example, Kawaguchi discloses projectors and computers having LCD displays (Ex. 1005, Figures 11, 12) while Matsumoto discloses televisions and many additional LCD applications. Ex. 1008, §2.7.

9. Claim 9

(“The electro-optical panel according to claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.”)

257. Kitawada discloses claim 9:



Ex. 1004, Figure 2; ¶[0020]; see [10b], [10g], and claim 12 in Ground 1.

XII. CONCLUSION

258. Claims 1-23 are obvious for the reasons set forth above.

259. The findings and opinions set forth in this Declaration are based on my work and analysis to date. I may continue my analysis. I may also receive additional documentation and other factual evidence over the course of this proceeding that will allow me to supplement and/or refine my opinions. I reserve the right to add to, alter, or delete my opinions and my Declaration upon discovery of any additional information. I also reserve the right to make such changes as may be deemed necessary.

260. In signing this Declaration, I recognize that it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

APPENDIX 1

CV

Curriculum Vitae of Richard A. Flasck

My fifty-five year professional career has involved high tech product development, intellectual property (IP) issues, projection displays, lens and optical system design, thin film optical filters, non-imaging optics, LCD flat panel displays and modules including touch panels, backlighting of flat panel displays, light emitting diode (LED and OLED) product development, injection molding, chip-on-board development, and High Definition Television (HDTV) systems.

I am an inventor on twenty-six patents (26), both US and foreign, including one US design patent. I have concluded several licensing agreements, demonstrating both technical innovation and expertise in Intellectual Property (IP) issues. Additionally, on several occasions I have testified before the US International Trade Commission and in US District Court as an expert witness on display and lighting technologies.

I am also an author of twenty-five (25) published papers and conference presentations.

Education

- 1970 BS – Physics University of Michigan (Ann Arbor, MI)
- 1976 MS – Physics Oakland University (Rochester, MI)

Employment

- 1989 – Present
 - Organization: RAF Electronics
 - Position: Founder / CEO / Owner
 - Developed, patented, and licensed Liquid Crystal on Silicon (LCOS) microdisplay technology. Engaged in development and patent prosecution of proprietary LED based Solid State Lighting (SSL) products. Etendue limited optics, non-imaging and hybrid optics, thermal management, layout and electronic drive of LED arrays. Expertise in semiconductor IC's, touch panels, Active Matrix Liquid Crystals Displays (AMLCD), thin films, optics, and video electronics. Optics and electronics manufacturing, technical consulting and independent testifying expert witness work in numerous patent lawsuits.
- 2002-2007
 - Organization: Diablo Optics, Inc.
 - Position: Co-founder and COO
 - Development, production and commercialization of key optical components for HDTV projectors. Polarization optics, condenser lenses, projection lenses, ultra-high performance optical thin film stacks. Established, and

managed international supply chain. Developed domestic and international customers.

- 1997 – 1999
 - Organization: Alien Technology Corporation
 - Position: President and COO
 - Responsible for successful MEM fluidic self-assembly (FSA) technology implementation and completion of a DARPA contract. Managed company growth from a four-person start-up to a VC funded twenty person operation. Cleanroom, photolith, thin film deposition (back-end) semiconductor processing.
- 1982-1989
 - Organization: Alphasil, Inc.
 - Position: Founder and CEO
 - Pioneered amorphous silicon thin film transistor (TFT) active matrix Liquid Crystal Displays (AMLCD). World's first amorphous silicon TFT LCD pilot line in 1986. TFT process and circuit design, data driver and gate driver design, scalars, video circuits, backlighting, and inverter design. Worked with touch screen pioneer Elographics to develop and integrate resistive and capacitive touch screens into Alphasil LCD modules.
- 1970 – 1982
 - Organization: Energy Conversion Devices, Inc.
 - Position: Scientist, Manager
 - Originated, managed, developed, and licensed several high tech products including thin film photovoltaics, ablative imaging films, EEPROMs, multi-chip modules, and superconducting materials.

Professional Affiliations

- Member - SPIE, Optica (formerly OSA), SID, IEEE, AES
- Co-Chairman – SPIE/ IS&T Symposium on Electronic Imaging (1991 and 1992)
- Former Board Member - RAF Electronics Corp., Alphasil, Inc., Somanetics Corporation, Diablo Optics, Inc.

Testifying Expert Witness Experience in Patent Litigation

I have been an expert witness on over 65 cases, 14 of which involved touch panel patents and technology, and 12 of which involved OLED display patents. I have written scores of expert reports and declarations, have been deposed over 24 times, and have testified in district court or at ITC hearings 8 times. I am familiar with IPRs, EPRs, and PGRs. None of my testimony or opinions have ever been excluded.

Date	2006 - 2007
Law Firm	Bingham McCutchen LLP
Client	Defendant - Seoul Semiconductor Company, Inc.
Case	Nichia Corporation v. Seoul Semiconductor 3:06-cv-0162 United States District Court, Northern District of California
Services	Expert witness, reports, deposition, trial testimony

Date	2007-2008
Law Firm	Orrick, Herrington & Sutcliffe LLP
Client	Respondent - Acer Incorporated and Acer America Corporation
Case	Hewlett Packard v. Acer Incorporated et al. U. S. International Trade Commission Investigation No. 337-TA-606
Services	Expert witness, reports, deposition, ITC hearing testimony

Date	2008
Law Firm	Fish & Richardson P.C.
Client	Complainant - Samsung
Case	Samsung v Sharp U. S. International Trade Commission Investigation No. 337-TA-631
Services	Expert witness, reports, ITC hearing testimony

Date	2008 - 2009
Law Firm	Fish & Richardson P.C.
Client	Respondent - Samsung
Case	Sharp v Samsung U. S. International Trade Commission Investigation No. 337-TA-634
Services	Expert witness reports, deposition, ITC hearing testimony

Date	2008 - 2009
Law Firm	Howrey LLP
Client	Complainant - O2Micro
Case	O2Micro v Monolithic Power Systems, MicroSemi U. S. International Trade Commission Investigation No. 337-TA-666
Services	Expert witness, reports, deposition, ITC hearing testimony

Date	2014
Law Firm	Kenyon & Kenyon
Client	Petitioner: Sony
Case	IPR: No. IPR2014-0168 Patent: USP 7,612,843
Services	Declaration supporting IPR and litigation prep
Date	2014 - 2015
Law Firm	Prebeg, Faucett & Abbott PLLC
Client	Plaintiff - Masakazu Ushijima
Case	Ushijima v. Samsung 1:12-cv-00318-LY United States District Court, Western District of Texas
Services	Expert witness, reports, deposition, trial testimony
Date	2015
Law Firm	Lerner, David, Littenberg, Krumholz & Mentlik, LLP
Client	Petitioner: Sony Corporation
Case	Delaware Display Group LLC and Innovative Display Technologies LLC v Sony Corp. et al., Case No. 1:13-cv-02111-UNA (D. Del.).
Services	Multiple expert declarations supporting IPR and litigation prep
Date	2015-2016
Law Firm	Marc Labgold PC
Client	IPR petitioner: Funai Corporation
Case	Funai v Gold Charm Limited Case No. IPR2015-01468
Services	Expert Declarations and deposition
Date	2015
Law Firm	Sidley Austin LLP
Client	Defendant Exar Corporation
Case	Phenix, LLC v Exar et al. Case No. 6:15-CV-00436-JRG-KNM.
Services	Expert Declaration and deposition
Date	2016
Law Firm	Kellogg, Huber, Hansen, Todd, Evans & Figel, P.L.L.C.
Client	Defendant Funai Corporation
Case	MiiC v Funai. C.A. No. 14-804-RGA.
Services	Expert Declaration
Date	2016
Law Firm	Gibson, Dunn & Crutcher LLP.
Client	Defendant Vizio, Inc.
Case	Delaware Display Group LLC v Vizio. Case No. 13-cv-02112-RGA.
Services	Expert Invalidity Report and Deposition
Date	2017
Law Firm	Kurth Kenyon LLP
Client	Defendant Sony.

Case ARRIS v Sony US International Trade Commission Investigation No. 337-TA-1060
 Services IPR Expert Declaration

Date 2018
 Law Firm Taft Stettinius & Hollister LLP
 Client Petitioner BlueHouse Global, LTD..
 Case BlueHouse v Semiconductor Energy Laboratory Co. LTD IPR Petitions
 Services IPR Expert Declaration for five patents

Date 2018
 Law Firm K&L Gates LLP
 Client Defendant Wistron Corp.
 Case Phenix, LLC v Wistron Case No. 2:17-cv-00711-RWS
 Services Expert Declaration, deposition

Date 2018
 Law Firm Goodwin LLP et al.
 Client Respondent Absen et al.
 Case Ultravision v Absen et al ITC Investigation No. 337-TA-1114
 Services Expert Report

Date 2018
 Law Firm DLA Piper.
 Client Petitioner Viavi Solutions, inc..
 Case Viavi v Materion Corp PRG Unassigned US Pat No. 9,989,684
 Services Declaration for PGR

Date 2019
 Law Firm Jones Day
 Client Petitioner NEC
 Case NEC v Ultravision IPR2019-01123, IPR2019-01117
 Services Declarations for IPRs

Date 2020
 Law Firm Russ August & Kabat
 Client Plaintiff Solas OLED Ltd.
 Case Solas v Samsung Case No. 2:19-cv-00152-JRG
 Services CC Declaration and Deposition

Date 2020
 Law Firm Russ August & Kabat
 Client Plaintiff Solas OLED Ltd.
 Case Solas v LG / Sony Case No. 6:19-cv-00236-ADA
 Services CC Declarations and Deposition

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v Lenovo / Motorola Case No. 3:19-cv-05644-SI
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v Dell Case No. 1:19-cv-00819-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v HP Case No. 1:19-cv-00873-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v Microsoft Case No. 1:19-cv-00874-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v Amazon Case No. 1:19-cv-00898-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Neodron
Case Neodron v Samsung Case No. 1:19-cv-00903-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Solas
Case Solas v Samsung Case 2:19-cv-00152-JRG
Services CC Declaration, Deposition

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Solas OLED Ltd.
Case Solas v Dell Case No. 6:19-cv-00514-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Solas OLED Ltd.
Case Solas v Google Case No. 6:19-cv-00515-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Solas OLED Ltd.
Case Solas v Apple Case No. 6:19-cv-00537-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Plaintiff Solas OLED Ltd.
Case Solas v HP Case No. 6:19-cv-00631-ADA
Services CC Declaration

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Solas OLED Ltd.
Case LGD v Solas OLED Case IPR2020-00177
Services IPR Declaration, Deposition

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00192
Services IPR Declaration

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00234
Services IPR Declaration

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00225
Services IPR Declaration

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00406
Services IPR Declaration, Deposition

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00267
Services IPR Declaration

Date 2020
Law Firm Russ August & Kabat
Client Patent Owner Neodron Ltd.
Case Samsung v Neodron Case IPR2020-00267
Services IPR Declaration

Date 2020
Law Firm Goodwin
Client Govision.
Case Ultravision v Govision Case 2:18-cv-00100-JRG-RSP
Services Invalidity Expert Report, Deposition

Date 2020-2021
Law Firm Goodwin
Client Shenzhen Absen
Case Ultravision v Shenzhen Absen Case 2:18-cv-00112-JRG-RSP
Services Invalidity Expert Report, Deposition, Trial testimony

Date 2020
Law Firm Goodwin
Client Barco
Case Ultravision v Barco Case 2:18-cv-00253-JRG-RSP
Services Invalidity Expert Report, Deposition

Date 2020
Law Firm Goodwin
Client Yaham Optoelectronics
Case Ultravision v Yaham Optoelectronics Case 2:18-cv-00118-JRG-RSP
Services Invalidity Expert Report, Deposition

Date 2020
Law Firm Goodwin
Client Ledman Optoelectronic
Case Ultravision v Ledman Optoelectronic Case 2:18-cv-00101-JRG-RSP
Services Invalidity Expert Report, Deposition

Date 2020
Law Firm Russ August & Kabat
Client Patent owner Solas
Case Samsung v Solas Case IPR2020-00140
Services IPR Declaration, Deposition

Date	2020
Law Firm	Russ August & Kabat
Client	Patent Owner Solas
Case	Samsung v Solas Case IPR2020-00320
Services	IPR Declaration, Deposition

Date	2020
Law Firm	Russ August & Kabat
Client	Patent Owner Neodron Ltd.
Case	Samsung v Neodron Case IPR2020-00515
Services	IPR Declaration

Date	2020
Law Firm	Russ August & Kabat
Client	Patent Owner Neodron Ltd.
Case	Dell, Lenovo, HP v Neodron Case IPR2020-00731
Services	IPR Declaration

Date	2020
Law Firm	Russ August & Kabat
Client	Patent Owner Neodron Ltd.
Case	Samsung v Neodron Case IPR2020-00308
Services	IPR Declaration

Date	2021
Law Firm	Perkins Coie
Client	TCL
Case	TCL v Philips Case IPR2021-00498
Services	IPR Declaration

Date	2020-2021
Law Firm	Goodwin
Client	Shenzhen Absen
Cases	Shenzhen Absen v Ultravision IPR 2020-01049 IPR 2020-01050 IPR 2020-01052
Services	Invalidity Declarations

Date	2021
Law Firm	Russ August & Kabat
Client	Solas
Case	Solas v BOE/Samsung ITC 337-TA-1243
Services	Claim Construction Declaration

Date	2021
Law Firm	Finnegan
Client	Tianma

Date	2023		
Law Firm	Winston & Strawn		
Client	Hisense		
Case	Hisense v Vista Peak Ventures	IPR2023-00651	
Services	IPR Declaration		

Date	2023	
Law Firm	Winston & Strawn	
Client	Hisense	
Case	Hisense v Vista Peak Ventures	IPR2023-00725
Services	IPR Declaration	
Date	2023	
Law Firm	Winston & Strawn	
Client	Hisense	
Case	Vista Peak Ventures v Hisense	2:21-CV-262-JRG 2:21-CV-260-JRG 2:21-CV-263-JRG
Services	Claim Construction Declaration	
Date	2023	
Law Firm	Kilpatrick Townsend	
Client	Manufacturing Resources International (MRI)	
Case	Samsung v MRI	ITC 337-TA-1349
Services	CC Declaration, Expert reports, Deposition, ITC Testimony	
Date	2024	
Law Firm	Kramer	
Client	Polaris PowerLED	
Case	Polaris v Samsung	2:22-cv-00469-JRG
Services	Expert Report, Deposition	
Date	2024	
Law Firm	Venable	
Client	Signify	
Case	Signify v Menard's	3:22-cv-00706-jdp
Services	Expert Reports	
Date	2024	
Law Firm	Perkins Coie	
Client	TCL	
Case	TCL v Philips	EPR 6/4/2024
Services	EPR Declaration	
Date	2024	
Law Firm	Finnegan	
Client	BOE	
Case	BOE v 138 East LCD Advancements	IPR2024-00976
Services	IPR Declaration	
Date	2024	
Law Firm	Finnegan	
Client	Acer	

Case	Acer v SVV Technology Innovations	EPR TBD
Services	EPR Declaration	
Date	2025	
Law Firm	Orrick	
Client	BOE	
Case	BOE v Paneltouch Technologies LLC	IPR2025-01267
Services	IPR Declaration	

Patents & Patent Applications

<u>Patent</u>	<u>Date</u>	<u>Description</u>
9,328,898	5/3/16	High Efficiency Hybrid Illumination System
6,266,037	7/24/01	Wafer Based Active Matrix
700353/1991	8/19/99	Wafer Based Active Matrix
0438565B1	6/4/97	Wafer Based Active Matrix
5,123,847	6/23/92	Method of Manufacturing Flat Panel Back Planes, Display Transistors
5,108,172	4/28/92	An Improved Active Matrix Reflective Image Plane Module and Projection System
UM-68958	2/21/92	Wafer Based Active Matrix
5,024,524	6/18/91	Reflective Image Plane Module
UM-67108	12/14/91	An Active Matrix Reflective Projection Apparatus
D320,403	10/1/91	Liquid Crystal Screen for Overhead Projector
5,022,750	6/11/91	An Active Matrix Reflective Projection System
4,842,378	6/27/89	Method of illuminating Flat Panel Displays to Provide CRT Appearing Displays
4,820,222	4/11/89	Method of manufacturing Flat Panel Backplanes Including Improved Testing and Yields Thereof and Displays Made Thereby
4,736,229	4/5/88	Method of Manufacturing Flat Panel Backplanes, Display Transistors and Displays Made Thereby
4,651,185	3/17/87	Method of Manufacturing Thin Film Transistors and Transistors Made Thereby
4,599,705	7/8/86	Programmable Cell for Use in Programmable Electronic Arrays
4,545,112	10/8/85	Method of Manufacturing Thin Film Transistors and Transistors Made Thereby
4,499,557	2/12/85	Programmable Cell for Use in Programmable Electronic Arrays: Doped Amorphous Silicon Alloy
4,458,297	7/3/84	Universal Interconnect Substrate
4,339,255	7/13/82	Method and Apparatus for Making Modified Amorphous Glass Materials
4,332,466	6/1/82	Apparatus for Producing Microform Records at High Speed from Computer or Other Electronic Data Signal Sources
FR2489843A1	13/12/82	Apparatus and Method for Producing Amorphous Modified Glass
GB2083455A	9/7/81	Spinning Ribbons of Metallic, Dielectric, and Semiconductor Modified Amorphous Glass Materials

4,170,728	10/9/79	Heat Applying Microfilm Recording Apparatus
3,983,076	9/28/76	N-Type Amorphous Semiconductor Materials: Chalcogenides
DE2429507	1/23/75	N Conductivity Amorphous Semiconductor Material

Papers and Conference Presentations

1. J. Ferry, R. Winston, R. Flasck, "Nonimaging Optics Applications in Theater Lighting", SPIE Optics+Photonics Conference, San Diego, CA, August 19, 2018
2. Richard Flasck, "Ultra High Efficiency Beam Forming Solid State Lighting Luminaires", SAIC Non-Imaging Optics Workshop, La Jolla, CA, August 24, 2013
3. Richard Flasck, "Ultra High Efficiency Beam Forming Solid State Lighting Luminaires", Society for Information Display Conference, Boston, June 7, 2012.
4. R. Flasck, "Design, Production, and Application of High Performance Dichroic Coatings - One Step Beyond the Cutting Edge -", presented at the SAIC Non-Imaging Optics Workshop, La Jolla, CA, August 25, 2007
5. R. Flasck, "The Critical Role of Optical Interference Coatings in High Brightness - Etendue Limited Systems Such as HDTV Projectors", at The 2007 Optical Interference Coatings Topical Meeting and Tabletop Exhibit, Optical Society of America, June 7, 2007.
6. R. Flasck, "X-Cubes - Revisited for LCOS", Bay Area Society for Information Display Meeting, October 24, 2002
7. R. Flasck, "The Care and Feeding of Single Crystal Silicon Light Valve Design," Society for Information Display FPD Strategic and Technical Symposium, September 9-10, 1998.
8. R. Flasck, "The Care and Feeding of Single Crystal Silicon Light Valve Design," Stanford Resources 1998 Display Conference
9. R. Flasck, and E. Rawson, "High Optical Efficiency PDLC/CMOS Projection Systems," IC Expo/WESCON 1996
10. R. Flasck, "Current and Near Term Applications of Flat Panel Display Devices," Applications of Electronic Imaging; John Urbach, Editor; Proceedings of SPIE, Vol 1082 (1989). - Invited Critical Review Paper
11. R. Flasck, "U.S. Display Suppliers and Developers: Comments on Developments and Manufacturing," Flat Panel Displays 1988 Conference and Exhibition; Stanford Resources, Inc. (1988). - Invited Presentation and Expert Panel Member
12. S. Ladderman, A. Bienenstock, R. Flasck, and F. Betts, "Structural Studies of Sputtered Ni-As-O Films," Journal of Non-Crystalline Solids, Vol 70, Num 3, 409-427 (1985).

13. R. Flasck, and S. Holmberg, "Amorphous Silicon Thin Film Transistor (TFT) Driven Liquid Crystal Displays (LCD)," *Advances in Display Technology V*, Elliott Schlam, Editor, *Proceedings of SPIE*, Vol 526, 94-98 (1985).
14. S. Ovshinski, K. Sapru, and R. Flasck, "Modification of SiO_2 ," *Bulletin of the American Physical Society*, Vol 23, Num 3, 461 (1978).
15. R. Flasck, M. Izu, K. Sapru, T. Anderson, S. Ovshinski, and H. Fritzsche, "Optical and Electronic Properties of Modified Amorphous Materials," *Proceedings of the Seventh International Conference on Amorphous and Liquid Semiconductors*, University of Edinburgh, Scotland, 527-528 (1977).
16. S. Ovshinski, R. Flasck, M. Shaw, and K. Dec, "An Experimental Study of Threshold Switching in Some Binary Chalcogenide Based Glass Films," *Tr. 6-iMezhdunar.Konf.po Amorfin. I Zhidk, Poluprovodn*, (1975). *Struktura I Svoistva Nekristal. Poluprovodn.*, 190-194 (1976).
17. M. Tenhover, P. Boolchand, and R. Flasck, "Mossbauer Effect Studies in Amorphous $\text{As}_x\text{Te}_{1-x}$ Binary," *Bulletin of the American Physical Society*, Vol 21, Num1, 20 (1976).
18. P. Boolchand, M. Tenhover, and R. Flasck, "Te-125 Mossbauer Effect in Amorphous $\text{As}_x\text{Te}_{1-x}$," *Bulletin of the American Physical Society*, Vol 21, Num 3, 460 (1976).
19. M. Tenhover, P. Boolchand, and R. Flasck, "Amorphous to Crystalline Transition in $\text{As}_x\text{Te}_{1-x}$ System," *Bulletin of the American Physical Society*, Vol 21, Num7, 928 (1976).
20. H. Rockstad, R. Flasck, and J. P. deNeufville, *Bulletin of the American Physical Society*, Vol 18, 454 (1973).
21. H. Rockstad, and R. Flasck, "Photo -thermopower in Amorphous Chalcogenide Films," *Proceedings of the Fifth International Conference on Amorphous and Liquid Semiconductors*, Garmisch-Partenkirchen, Germany, 1311-1315 (1973).
22. R. Flasck, and H. Rockstad, "The Thermal Conductivity of Some Chalcogenide Glasses," *Journal of Non-Crystalline Solids*, Vol 12, 353-356 (1973).
23. H. Rockstad, and R. Flasck, *Bulletin of the American Physical Society*, Vol 17, 116 (1972).
24. H. Rockstad, R. Flasck, and S. Iwasa, "Seebeck Coefficient in Amorphous Chalcogenide Films," *Journal of Non-Crystalline Solids*, Vol 8-10, 326-333 (1972).
25. D. Meyer, and R. Flasck, "New Configuration for a Dipole Magnet for Use in High Energy Physics Applications," *Nuclear Instrumentation and Methods*, Vol 80, Num 2, 339-341 (1970).