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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	9319S-000838
First Inventor	Shin FUJITA
Title	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Express Mail Label No.	EV 533 145 647 US (8/6/2004)

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 33]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention ☒ Specification filed in English
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) (*35 U.S.C.113*) [*Total Sheets* 8]
5. Oath or Declaration [*Total Sheets* ___]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63 (d))
   (for a continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☒ Application Data Sheet. See 37 CFR 1.76

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ACCOMPANYING APPLICATIONS PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. 3.73(b) Statement ☐ Power of Attorney *(when there is an assignee)*
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12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
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EV 533 145 647 US

ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM

RELATED APPLICATIONS

[0001] This application claims priority to Japanese Patent Application No. 2003-290650 filed August 8, 2003, and 2004-193515 filed June 30, 2004 which is hereby expressly incorporated by reference herein in its entirety.

BACKGROUND

[0002] Technical Field

[0003] The present invention relates to an electro-optical panel, an electro-optical apparatus, and an electronic system.

[0004] Background Art

[0005] Display devices, for example, liquid crystal display devices using a liquid crystal as an electro-optical material, are widely used for display units of various information processing systems and liquid crystal televisions as display devices in place of cathode ray tubes (CRTs).

[0006] Here, a known electro-optical apparatus has a structure, for example, as described below. That is to say, the known electro-optical apparatus includes: pixel electrodes arranged in a matrix state; an element substrate on which switching elements, such as TFTs (Thin Film Transistors), connected to the pixel electrodes, are disposed; an opposing substrate on which opposing electrodes opposed to the pixel electrodes are formed; and a

liquid crystal, which serves as an electro-optical material, filled between both of these substrates. A pixel includes the switching element, the pixel electrode, the electro-optical material, and the opposing electrode, and is arranged in a matrix state. In such an arrangement, when a scanning signal is applied to the switching element through a scanning line, that switching element adopts a conductive state. In this conductive state, when an image signal having a voltage in accordance with grayscale is applied to the pixel electrode through a data line, a charge in accordance with the voltage of the image signal is stored in the liquid crystal layer between the pixel electrode and the opposing substrate. After the charge is stored, even if the switching element is turned to an off state, the storage of the charge in that liquid crystal layer is maintained by the capacitance of the liquid crystal layer itself, the storage capacitance, and the like. In this manner, when each switching element is driven, and the charge amount to be stored is controlled in accordance with grayscale, the alignment state of the liquid crystal is changed for each pixel, and thus the density changes for each pixel. It is, therefore, possible to display grayscale.

[0007] Such an electro-optical apparatus includes an electro-optical panel on which the above-described pixels are disposed in a matrix state. A scanning-line drive circuit, which drives scanning lines, and a data-line drive circuit, which drives data lines, are sometimes formed on the electro-optical panel. A power source, a driving signal, an image signal, etc. are supplied to the electro-optical panel having drive circuits. As means for supplying the power source, etc. to the electro-optical panel, techniques which connect an input terminal formed on the electro-optical panel and a flexible

substrate as a connection cable through an anisotropic conductive film are known (for example, Japanese Patent No. 2822558).

[0008] Incidentally, the resistance of an input terminal becomes smaller as the area thereof becomes larger. Thus, in terms of the reduction of the resistance value, it is desirable that the size of the input terminal is large. However, if the area of the input terminal is made large in terms of the reduction of the contact resistance, there has been a problem in that all of the input terminals cannot be disposed in a limited area.

[0009] In particular, in an electro-optical panel of the type which does not contain a data-line drive circuit, or an electro-optical panel of the type which contains a multiplexer, it is necessary to take a plurality of image signals into the electro-optical panel, and thus the number of the input terminals becomes large. Together with this, when a flexible substrate, etc., are mounted, a problem of connection failure or the like has occurred. On the other hand, when the area of the input terminal is made small in terms of the reduction of the mounting area, the contact resistance increases, and there has been a problem in that the driving signal cannot be input at a proper timing.

[0010] Accordingly, it is an object of the present invention to provide an electro-optical panel and an electro-optical apparatus in which mounting parts such as a flexible substrate, etc., can be connected with high reliability, and a band necessary for signal transmission can be obtained, and to provide an electronic system using these.

SUMMARY

[0011] In order to solve the above-described problem, according to the present invention, there is provided an electro-optical panel including: a plurality of data lines; a plurality of scanning lines; a plurality of pixels disposed corresponding to intersections between the data lines and the scanning lines; a first input terminal supplied with a first input signal; a second input terminal supplied with a second input signal; and a drive circuit which controls grayscale of the pixel based on the first and the second input signals, wherein the first input signal includes a higher frequency component compared with the second input signal, and the first input terminal has a larger area than the second input terminal.

[0012] In general, the input resistance of a terminal is inversely proportional to the area thereof. Thus, the larger the area of the input terminal, the smaller the input resistance value becomes. Incidentally, the input resistance value includes the contact resistance value in case of connection of mounting parts.

[0013] According to this invention, the area of the input terminal can be changed in accordance with the transmission characteristics of the input signal, and thus it is possible to make smaller the area of the input terminal capable of sufficiently transmitting the signal in spite of a large time constant. Whereas for the input terminal supplied with the input signal which is required to have a small time constant characteristic, it becomes possible to obtain a large area. In this case, it is preferable that the area of the input terminal supplied with the plurality of input signals is set in accordance with the frequency characteristics of the input signal. For an input signal which includes a high-frequency component, the input signal

waveform can be captured without becoming dull by setting the time constant to a small value. Whereas for the input signal which consists of relatively low-frequency components, there is no problem even if the time constant is large, and thus the area of the input terminal can be made small.

[0014] More specifically, it is preferable that the plurality of input signals include a plurality of driving signals and a plurality of image signals, the frequency characteristics of the plurality of driving signals include a higher frequency component compared with the frequency characteristics of the plurality of image signals, and the area of the first input terminal supplied with a plurality of driving signals is larger than the area of the second input terminal supplied with the plurality of the image signals. In this case, the waveform of the driving signal is captured into the electro-optical panel without becoming dull, and thus an erroneous operation of displaying an image can be prevented. At the same time, the area of the input terminal of the image signal can be made small, and thus multiple input terminals can be disposed in a limited area. As described above, by focusing attention on the frequency characteristics of the input signals and allocating the area of the input terminals, it becomes possible to appropriately dispose input terminals in a limited area.

[0015] In the above-described electro-optical panel, it is preferable that the first input terminal and the second input terminal are formed in line on a substrate, the second input terminal is disposed in the central part of the substrate, and the first input terminal is disposed at the outer side of the substrate. When connecting each terminal with ACF, heat and pressure are applied, and thus the outer side of ACF tends to have a larger extension rate

than the central part. Therefore, by disposing an input terminal having a wider area at a more outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is a large one even if a slight misalignment of the connection arises.

[0016] Furthermore, the electro-optical panel preferably includes a third input terminal, wherein the third input terminal is a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first input terminal. In general, if a power source, which is input into a power terminal, has a high resistance, the voltage is trapped, and there is a strong possibility that a predetermined voltage cannot be obtained. Therefore, the power source preferably has as low a resistance as possible. Accordingly, in the above-described panel, the power terminal to which power is supplied preferably has the same area or more as the area of the input terminal to which the driving signal is supplied. With this arrangement, it becomes possible to decrease the resistance, and to supply a predetermined voltage. Also, the larger as possible the power source terminal, the lower the resistance becomes, and thus the power terminal may include a plurality of adjacent terminals of the first input terminal or the second input terminal. Thus, the area of the input terminal can be increased, and the resistance can be decreased.

[0017] In the above-described electro-optical panel, a plurality of the power source terminals to which power is supplied, a plurality of the first input terminals, and a plurality of the second input terminals are preferably included; the plurality of the power source terminals, the plurality of the first

input terminals, and the plurality of the second input terminals are preferably formed in line on a substrate; and a pitch interval of the adjacent first input terminals is preferably an integer multiple of a pitch interval of the adjacent second input terminals.

[0018] According to this invention, when mounting members are mounted onto a plurality of power source terminals and a plurality of input terminals, the estimation of the contraction rate of the mounting members becomes easy, thereby it is possible to prevent a mounting failure in advance.

[0019] Furthermore, according to the present invention, there is provided an electro-optical panel including: on a substrate, a plurality of data lines; a plurality of scanning lines; an image display area which includes a plurality of pixels disposed corresponding to intersections between the data lines and the scanning lines; a scanning-line drive circuit for driving the pixels; a data-line drive circuit for supplying data signals to the pixels; and an input terminal group for supplying signals to the scanning-line drive circuit and the data-line drive circuit, wherein the scanning-line drive circuit is disposed along one side of the substrate on the substrate, the data-line drive circuit is disposed along a side which is not opposed to the one side on the substrate, the input terminal group is disposed along the data-line drive circuit and is disposed at an edge side of the substrate further than the data-line drive circuit, the input terminal group has a first input terminal group for supplying a driving signal to the scanning-line drive circuit and a second input terminal group for supplying an image signal to the data-line drive circuit, the second input terminal is disposed in the central part of the input terminal group, the first input terminal is disposed at the outer side of the

input terminal group, and the first input terminal has a larger area than the second input terminal.

[0020] With this arrangement, it becomes possible for the wiring lines from the second terminal to the data-line drive circuit and the wiring lines from the first input terminal to the scanning-line drive circuit not to intersect with each other. Also, since the wiring lines are not drawn around, it is possible to suppress the generation of wiring resistance and parasitic capacitance. Since the area of the input terminal of the driving signal having a high frequency component is larger than the area of the input terminal of the image signal having a lower frequency component, the contact resistance can be made low, and thus the signal can be prevented from becoming dull. Also, the input terminal having a large area is disposed at a more outer side than the input terminal having a small area. In the connection of the input terminal and the ACF, etc., in general, the ACF tends to have a larger extension rate at the outer side than in the central part. However, if the area of the outer input terminal is made large, even if the misalignment due to the difference of the extension rate occurs, it is possible to prevent a connection failure.

[0021] Furthermore, the electro-optical panel preferably includes a fourth input terminal for supplying a driving signal to the data-line drive circuit, wherein the fourth input terminal has an area equal to an area of the first input terminal, and the fourth input terminal is preferably disposed between the first input terminal and the second input terminal.

[0022] In this manner, by preferably disposing the terminals having a large area on the periphery of the substrate together, it is possible to

prevent a mounting failure.

[0023] Next, an electro-optical apparatus according to the present invention includes: an electro-optical panel described above; power source means for supplying the power source; and signal generation means for supplying the first input signals and the second signals. Since this electro-optical apparatus includes the above-described electro-optical panel, it is possible to connect a mounting part such as a flexible substrate, etc., with high reliability, and it becomes possible to obtain a band necessary for the transmission of the signals.

[0024] Also, an electro-optical apparatus according to the present invention includes: an electro-optical panel described above; an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and a flexible substrate which connects the external substrate and the electro-optical panel, wherein the flexible substrate is preferably connected to the plurality of power source terminals and the plurality of first input terminals and the plurality of the second input terminals through an anisotropic conductive film.

[0025] Here, wiring lines are preferably formed corresponding to a reference pitch interval of the second input terminals on the flexible substrate. For a terminal group in which terminals having different widths are mixed, it is possible to reliably connect each wiring line. For a terminal having a large area, a plurality of wiring lines are assigned, and thus it is possible to reduce the contact resistance and the wiring resistance.

[0026] Next, an electronic system according to the present invention includes an electro-optical apparatus described above. Such an

electronic system includes a liquid crystal projector, a personal computer, a mobile phone, an electronic camera, a PDA, etc.

[0027] In this manner, according to the present invention, it is possible to provide an electro-optical panel and an electro-optical apparatus which can connect a mounting part such as a flexible substrate, etc., with high reliability, and can obtain a band necessary for the transmission of the signals, and an electronic system using these.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Fig. 1 is a perspective view illustrating the structure of a liquid crystal panel AA according to an embodiment of the present invention.

[0029] Fig. 2 is a cross-sectional view taken on Z-Z' line of Fig. 1.

[0030] Fig. 3 is a block diagram illustrating the electrical configuration of the liquid crystal panel AA of a first embodiment.

[0031] Fig. 4 is a plan view illustrating the structure concerning the connection between a terminal group 10 and a flexible substrate B according to the embodiment.

[0032] Fig. 5 is a block diagram illustrating the entire configuration of a liquid crystal display device.

[0033] Fig. 6 is a plan view illustrating the structure concerning the connection between a terminal group 10 and a flexible substrate B according to an application.

[0034] Fig. 7 is a cross-sectional view of a video projector, which is an example of an electronic system to which the liquid crystal display device is applied.

[0035] Fig. 8 is a perspective view illustrating the structure of a personal computer, which is an example of an electronic system to which the liquid crystal display device is applied.

[0036] Fig. 9 is a perspective view illustrating the structure of a mobile phone, which is an example of an electronic system to which the liquid crystal display device is applied.

[0037] Fig. 10 is a block diagram illustrating the configuration of the liquid crystal panel of a second embodiment.

DETAILED DESCRIPTION

[0038] In the following, a description will be given of an embodiment according to the present invention with reference to the drawings. In this regard, in this embodiment, a description will be given by taking a liquid crystal panel, which uses a liquid crystal as an electro-optical material, as an example of an electro-optical panel, and by taking a liquid crystal device, which uses a liquid crystal panel, as an example of an electro-optical apparatus. However, the present invention is not limited to this, and an organic EL panel including an organic light-emitting diode element, and the like are included in the electro-optical panel as a matter of course.

[0039] 1. Mechanical structure of liquid crystal panel

[0040] First, a description will be given of the mechanical structure of a liquid crystal panel AA according to the first embodiment with reference to Figs. 1 and 2. Here, Fig. 1 is a perspective view illustrating the structure of the liquid crystal panel AA. Fig. 2 is a cross-sectional view taken

on Z-Z' line of Fig. 1.

[0041] As shown in these figures, the liquid crystal panel AA has a structure in which an element substrate 151 including glass or a semiconductor, or the like, on which a pixel electrodes 6, etc. are formed; and a transparent opposing substrate 152 including glass, etc. on which a common electrode 158 is formed, are bonded together by a sealing material 154 mixed with a spacer 153, while keeping a certain gap apart, with the electrode-formed surfaces being opposed to each other, and a liquid crystal 155 as an electro-optical material is enclosed in the gap. In this regard, the sealing material 154 is formed along the surroundings of the substrate of the opposed substrate 152, and has an opening in part in order to enclose the liquid crystal 155. Thus after enclosing the liquid crystal 155, the opening part is closed by a closing material 156.

[0042] Here, a terminal group 10 is formed at one outer side of the sealing material 154 on the opposed surface of the element substrate 151. The terminal group 10 consists of a plurality of input terminals 20. An image signal is supplied to a part of the plurality of input terminals 20 to drive data lines 3 extending in a Y direction. Furthermore, the terminal group 10 is formed at this side. Also, a scanning-line drive circuit 100 is formed on one side adjacent to this side. Scanning lines 2 extending in an X direction are individually driven from both of the sides.

[0043] The terminal group 10 is electrically and mechanically connected to a mounting member through an anisotropic conductive film. The mounting member of this example includes a flexible substrate as a connection cable and external substrate. The common electrode 158 of the

opposed substrate 152 is conductive to the element substrate 151 through a conductive material provided at least on one of the four corners of the bonding parts with the element substrate 151. In addition, depending on the use of the liquid crystal panel AA, the opposed substrate 152 is provided with for example, first, a color filter arranged in a stripe-shaped state, a mosaic-shaped state, a triangle-shaped state, etc.; second, for example, a black matrix such as a resin black made by dispersing a metallic material such as chrome or nickel, and carbon, titanium on photo resist; third, a back light emitting light to the liquid crystal panel AA. In particular, in the case of use for color light modulation, a color filter is not formed, and a black matrix is provided on the opposed substrate 152.

[0044] In addition, alignment layers, which have undergone rubbing processing individually in a predetermined direction, etc. are disposed on the opposed surfaces of the element substrate 151 and the opposed substrate 152. At the same time, a polarizer (omitted in the figure) in accordance with the alignment direction is disposed on each of the back surfaces. However, if a polymer-dispersed liquid crystal, in which droplets are dispersed in the polymer, is used as a liquid crystal 155, the above-described alignment layer, polarizer, etc. become unnecessary. As a result, the light utilization rate is increased, and thus it is advantageous in achieving higher luminance and lower power consumption.

[0045] In this regard, in place of forming a part of or the entire peripheral circuit, such as the scanning-line drive circuit 100, etc., on the element substrate 151, for example, a driving IC chip mounted on a film may be electrically and mechanically connected through the anisotropic conductive

film disposed at a predetermined position on the element substrate 151 using a TAB (Tape Automated Bonding) technique. Alternatively, the driving IC chip itself may be electrically and mechanically connected through the anisotropic conductive film disposed at a predetermined position on the element substrate 151 using a COG (Chip On Glass) technique.

[0046] 2. Electrical structure of liquid crystal panel

[0047] Fig. 3 is a block diagram illustrating the electrical configuration of the liquid crystal panel. As shown in this figure, the liquid crystal panel AA includes the scanning-line drive circuit 100, an image display area A, and the terminal group 10. The terminal group 10 includes a first terminal group 10A, a second terminal group 10B, and a third terminal group 10C. Various driving signals which drive the scanning-line drive circuit 100 and the power source are supplied to the first terminal group 10A and the third terminal group 10C. That is to say, a part of the input terminals 20, which constitute the first terminal group 10A and the third terminal group 10C, may function as a power source terminal supplied with a power source (a third input signal). At the same time, an image signal is supplied to the second terminal group 10B. It is better that the resistance of the power source terminal should be kept as small as possible, because a predetermined voltage cannot be obtained by a voltage trap when the resistance is high. Thus, the power source terminal preferably has the same area as the first terminal group or more. Furthermore, if the power source terminal is structured in two parts such that the power source terminal extends over both of the two terminals adjacent with the first terminal group or the second terminal group,

the resistance can be further suppressed. Also, it is preferable that the power source terminal is disposed at the side more outer than the input terminal of the driving signal on the substrate. That is to say, it is preferable that, in the input terminal group arranged in line on one side of the substrate, an input terminal of the image signal is disposed in the central part, and the input terminal of drive circuit and the power source terminal are disposed in this order from the center.

[0048] In this example, the driving signal (first input signal) and the image signal (second input signal) are supplied to the liquid crystal panel AA as input signals in addition to the power source. Among them, the driving signal includes a Y transmission start pulse DY, a Y clock signal YCK, an inverted Y clock signal YCKB, and the like. The frequency characteristics of these driving signals include a higher frequency component compared with the frequency characteristics of the image signal. Accordingly, in order to normally operate the scanning-line drive circuit 100, it is necessary for the driving signal to be transmitted without becoming dull. The driving signal is transmitted through the flexible substrate, and a distributed capacitance and a distributed resistance exist on this transmission path, equivalently constituting a low-path filter. Accordingly, in order for the driving signal to be transmitted without becoming dull, it is necessary to decrease the time constant of the equivalent low-path filter. Among distributed resistors, the rate of the contact resistance generated in the input terminal 20 is large, so that the resistance cannot be disregarded. The contact resistance becomes smaller as the area of the input terminal 20 becomes larger. Thus, in this embodiment, the area of the input terminal to which the driving signal is

supplied is made larger compared with that of the input terminal to which the image signal is supplied. Specifically, the input terminal 20, which is included in the first and the third terminal groups 10A and 10C, has a larger area than the input terminal 20 which is included in the second terminal group 10B.

[0049] In other words, a plurality of input terminals 20 to which input signals are supplied include a plurality of kinds of input terminals 20 having different input resistance values, and the kind of the input terminal 20 to which each input signal is supplied is determined in accordance with the transmission characteristic required for transmitting each input signal. Thus, a driving signal having a relatively high frequency component is correctly transmitted. At the same time, the area of the input terminal 20 included in the second terminal group 10B to which the image signal having a relatively low frequency component is supplied is made smaller than the area of the input terminal 20 included in the first terminal group 10A and the third terminal group 10C, and thus it becomes possible to dispose a necessary number of the input terminals 20 in a limited area.

[0050] Next, the scanning-line drive circuit 100 includes a shift register, etc. The Y transmission start pulse DY, the Y clock signal YCK, the inverted Y clock signal YCKB, a high potential power source VHH, and a low potential power source VSS are supplied to the scanning-line drive circuit 100. In Fig. 3, the driving signal and the power source are supplied from the first terminal group 10A to the scanning-line drive circuit 100 of the left side, whereas the driving signal and the power source are supplied from the third terminal group 10C to the scanning-line drive circuit 100 of the right side.

[0051] The scanning-line drive circuit 100 transmits the Y

transmission start pulse DY in sequence in synchronism with the Y clock signal YCK and the inverted Y clock signal YCKB using the shift register, and further performs a level conversion to generate the scanning signals Y1, Y2, ..., Ym, and outputs each signal on each scanning line 2.

[0052] Next, as shown in Fig. 3, in the image display area A, m (m is a natural number of 2 or more) pieces of scanning lines 2 are arranged in parallel along the X direction, whereas n (n is a natural number of 2 or more) pieces of data lines 3 are arranged in parallel along the Y direction. In the vicinity of the intersections between the scanning lines 2 and the data lines 3, the gate of a TFT 50 is connected to the scanning line 2, the source of the TFT 50 is connected to the data line 3, and the drain of the TFT 50 is connected to a pixel electrode 6. Each pixel is constituted by the pixel electrode 6, an opposed electrode (which will be described below) formed on the opposed substrate, and a liquid crystal sandwiched between both of these electrodes. As a result, the pixels are arranged in a matrix state corresponding to each intersection between the scanning lines 2 and the data lines 3.

[0053] Also, each scanning line 2, to which the gate of the TFT 50 is connected, is supplied with scanning signals Y1, Y2, ..., Ym in a pulse state for each line in sequence. Thus when a scanning signal is supplied onto a scanning line 2, the TFT 50 connected to that scanning line is turned on. Therefore, data-line signals X1, X2, ..., Xn (image signal) supplied from the data line 3 at a predetermined timing are written into the corresponding pixel in sequence, and then maintained for a predetermined time period.

[0054] Since the alignment and the order of liquid crystal molecules are changed in accordance with an electric potential level applied to

each pixel, it becomes possible to display grayscale by light modulation. For example, the amount of light passing a liquid crystal is restricted with the increase of the applied potential in a normally white mode, whereas the amount of light is released with the increase of the applied potential in a normally black mode. Thus, light having contrast in accordance with the image signal is emitted from each pixel as the entire liquid crystal display device. Accordingly, it becomes possible to perform a predetermined display.

[0055] 3. Relationship between terminal group 10 and flexible substrate B

[0056] Next, a description will be given of the detailed structure of the terminal group 10 and a flexible substrate B. Fig. 4 is a plan view illustrating the structure concerning the connection between the terminal group 10 and the flexible substrate B. As described above, the terminal group 10 includes two kinds of input terminals 20 having different areas. In this example, the area of the input terminal 20 constituting the second terminal group 10B is the smallest, and the pitch between the input terminals 20 becomes the smallest. In this embodiment, among a plurality of kinds of input terminals 20 (including a power source terminal) having different areas, the pitch between the terminals having the smallest area is called a reference pitch PTref. In this example, since the area of the input terminal 20 constituting the second terminal group 10B is the smallest, the interval of the input terminal 20 constituting the second terminal group 10B becomes the reference pitch PTref.

[0057] In contrast, the pitches of the input terminals 20

constituting the first terminal group 10A and the third terminal group 10C are the same. This pitch is called a first pitch PT1. Furthermore, it is preferable to set the first pitch PT1 to an integer multiple of the reference pitch PTref. The flexible substrate B and the terminal group 10 are connected through an anisotropic conductive film (ACF). At this time, heat and pressure are applied, and thus the flexible substrate B contracts. When the pitches are set to have a relationship of an integer multiple as described above, and when the mounting members of the flexible substrate B, etc. are mounted onto the terminal group 10, the estimation of the contraction rate of the mounting parts becomes easy, thereby it is possible to prevent a mounting failure in advance. Also, when connecting each terminal with the ACF, heat and pressure are applied, and thus the outer side of the ACF tends to have a larger extension rate than the central part. Therefore, by disposing a terminal having a wider area at the outer side than the input terminal having a smaller area, it is possible to prevent a connection failure because of the difference in the contraction rates as long as the input terminal is large even if a slight misalignment of the connection arises. Accordingly, it is desirable to dispose the input terminal having a small pitch and a small area in the central part of the substrate, and to dispose an input terminal having a large pitch and a large area at the outer side thereof.

[0058] Also, wiring lines L are formed on the flexible substrate B at intervals of the reference pitch PTref. By this, for a terminal group 10 in which input terminals 20 having different widths are mixed, each of the wiring lines L can be reliably connected. For the input terminal 20 having a large area, two wiring lines L are assigned, and thus the contact resistance

and the wiring resistance can be reduced.

[0059] 4. Entire configuration of liquid crystal display device

[0060] Fig. 5 illustrates the entire configuration of a liquid crystal display device. An external substrate C is connected to a liquid crystal panel AA through a flexible substrate B. The external substrate C includes a data-line drive circuit 200, a timing generation circuit 300, an image processing circuit 400, and a power source circuit 500. Input image data D supplied to this liquid crystal display device has, for example, a three-bit parallel format. The timing generation circuit 300 generates the Y clock signal YCK in synchronism with the input image data D, the inverted Y clock signal YCKB, an X clock signal XCK, an inverted X clock signal XCKB, the Y transmission start pulse DY, and the X transmission start pulse DX. Also, the timing generation circuit 300 generates various timing signals for controlling the image processing circuit 400, and outputs the signals.

[0061] The Y clock signal YCK identifies a period for selecting the scanning line 2, and the inverted Y clock signal YCKB has the logic level inverted from the Y clock signal YCK. The X clock signal XCK identifies a period for selecting the data line 3, and the inverted X clock signal XCKB has the logic level inverted from the X clock signal XCK.

[0062] The image processing circuit 400 performs gamma correction on the input image data D in consideration of the light transmission characteristics of the liquid crystal panel AA, and then supplies the image data to the data-line drive circuit 200. The data-line drive circuit 200 transmits the X transmission start pulse DX in sequence in synchronism with

the X clock signal XCK and the inverted X clock signal XCKB to generate a sampling signal. The image data is sampled using the generated sampling signal to generate image data for each line in sequence. Furthermore, the image data is D/A converted to generate an image signal for each line in sequence. This image signal is supplied to the liquid crystal panel AA through the flexible substrate B.

[0063] The power source circuit 500 supplies a predetermined power source to the timing generation circuit 300 and the image processing circuit 400 in addition to supplying a high potential power source VDD and a low potential power source VSS to the scanning-line drive circuit 100. In the above configuration, the data-line drive circuit 200, the timing generation circuit 300, and the image processing circuit 400 function as signal generation means for supplying input signals to the liquid crystal panel AA.

[0064] 5. Applications

[0065] 5-1: Relationship between the terminal group 10 and flexible substrate B

[0066] In the above-described embodiment, two kinds of terminals having different areas are used for the input terminal 20. However, the present invention is not limited to this, and the present invention may be applied to the case where the input terminal 20 of three kinds or more is provided. Fig. 6 is a plan view illustrating the structure concerning the connection between terminal groups 10 and a flexible substrate B according to an application. In this example, the area of the input terminal 20 constituting the third terminal group 10C is the smallest. Thus, the interval of the input

terminal 20 constituting the third terminal group 10C becomes the reference pitch PTref. The input terminal 20 constituting the second terminal group 10B is formed at intervals of a second pitch PT2, and the input terminal 20 constituting the first terminal group 10A is formed at intervals of a first pitch PT1.

[0067] In this case, among PTref, PT1, and PT2, the following relationship holds: 2PTref = PT2, and 3PTref = PT1. That is to say, among a plurality of power source terminals and a plurality of kinds of input terminals, given that the pitch of the terminals having the smallest area is PTref, the pitches PT1 and PT2 of the input terminals of the other kinds, or the pitches PT1 and PT2 of the power source terminals become an integer multiple of the reference pitch PTref.

[0068] Also, the wiring lines L are formed at intervals of the reference pitch PTref on the flexible substrate B. Thus, for the terminal group 10 in which input terminals 20 having different widths are mixed, it is possible to reliably connect each wiring line L. For an input terminal 20 having a large area, two or three wiring lines L are assigned, and thus it is possible to reduce the contact resistance and the wiring resistance.

[0069] 5-2: Second embodiment of electro-optical apparatus

[0070] A description will be given of a second embodiment of the present invention using Fig. 10. Fig. 10 is a block diagram of the second embodiment, and is a figure illustrating a layout. The second embodiment has almost the same configuration as the first embodiment described above. A different point is that the second embodiment includes the disposition of the

data-line driver circuit such as a multiplexer, and the like. In this configuration, an image display area A is disposed in the central part of the substrate, scanning-line drive circuits 100 are disposed along the two sides opposed to each other in the surroundings on the substrate, the data-line drive circuit 200 is disposed along one side on which the scanning-line drive circuits 100 are not disposed in the surroundings of the substrate, and further, each input terminal (input terminals for the driving signal and the image signal) is disposed at a more outer side of the substrate than the data-line drive circuit 200. In this embodiment, a driving signal 10A is input into the scanning-line drive circuit 100 through the input terminal 10A, and an image signal 10B is input into the data-line drive circuit 200, such as a multiplexer, etc., through the input terminal 10B. The input terminal 10A has a larger area compared with the input terminal 10B. Furthermore, the input terminal 10B is disposed in the central part of the substrate, and the input terminal 10A is disposed at the outer side. Also, the input terminal to which the driving signal (fourth input signal) of the multiplexer is input has an area equal to the terminal to which the driving signal of the scanning-line drive circuit is input. Furthermore, the terminal to which the driving signal of the multiplexer is input is disposed at a more peripheral side than the terminal to which the image signal is input, and, in particular, is desirable to be disposed between the terminal to which the driving signal of the scanning-line drive circuit is input and the terminal to which the image signal is input. With this arrangement, by disposing the terminals having a large area and the terminals having a small area at each of the parts together, respectively, it is possible to prevent a connection failure of an ACF, etc. Also, with this

arrangement, it becomes possible for the wiring line from the input terminal 10B to the data-line drive circuit 200 and the wiring line from the input terminal 10A to the scanning-line drive circuit 100 not to intersect with each other. Also, since the wiring lines are not drawn around, it is possible to suppress the generation of wiring resistance and parasitic capacitance.

[0071] Also, in the embodiments described above, a description has been given of the case where the switching element of the pixel is a three-terminal element typified by a TFT. However, the switching element may be constituted by a two-terminal element such as a diode, etc. However, when a two-terminal element is used as the switching element of a pixel, it is necessary to form the scanning line 2 on one of the substrates, to form the data line 3 on the other of the substrates at the same time, and to form the two-terminal element between either of the scanning line 2 or the data line 3, and the pixel electrode. In this case, the pixel is constituted by the two-terminal element connected in series between the scanning line 2 and the data line 3, and a liquid crystal.

[0072] Also, the present invention has been described as a liquid crystal display device of an active matrix type. However, the present invention is not limited to this, and can be applied to a liquid crystal display device of a passive matrix type using an STN (Super Twisted Nematic) liquid crystal. Furthermore, the present invention can be applied to a display device which uses an electroluminescent element as an electro-optical material in addition to a liquid crystal and performs display by the electro-optical effects thereof. That is to say, the present invention can be applied to all the electro-optical apparatuses having a similar structure as the liquid crystal device

described above.

[0073] Also, in the above-described embodiment, the data-line drive circuit 200 is disposed on the external substrate C. However, the data-line drive circuit 200 may be disposed on the flexible substrate B. Furthermore, a multiplexer may be disposed at the end of each data line 3 of the liquid crystal panel AA. In this case, the number of image signals supplied to the liquid crystal panel AA can be reduced, and thus the number of input terminals 20 can be reduced. In addition, the data-line drive circuit 200 may be formed on the liquid crystal panel AA.

[0074] 5-3: Electronic system

[0075] Next, a description will be given of the case where the liquid crystal display apparatus described above is applied to various electronic systems.

[0076] 5-3-1: Projector

[0077] First, a description will be given of a projector using this liquid crystal display device as light valves. Fig. 7 is a plan view illustrating an example of the structure of the projector.

[0078] As shown in this figure, a lamp unit 1102 including a white light source such as a halogen lamp, etc. is provided in the inside of a projector 1100. The projection light emitted from the lamp unit 1102 is separated into three primary colors, RGB, by four mirrors 1106 and two dichroic mirrors 1108 disposed in a light guide 1104, and enters into liquid crystal panels 1110R, 1110B, and 1110G, each of which serves as a light valve corresponding to each

primary color.

[0079] The structure of the liquid crystal panels 1110R, 1110B, and 1110G is the same as the above-described liquid crystal panel AA, and the individual panels are driven by primary color signals of R, G, and B, supplied from the image signal processing circuit (omitted in the figure). Then each light modulated by one of these liquid crystal panels enters into a dichroic prism 1112 from three directions. The R and B light is deflected 90 degrees via the dichroic prism 1112, while the G light goes straight through. Accordingly, each color image is synthesized. As a result, a color image is projected onto a screen, etc. through a projection lens 1114.

[0080] Here, when attention is focused on the display image by each of the liquid crystal panels 1110R, 1110B, and 1110G, the display image by the liquid crystal panel 1110G needs to be horizontally reversed with respect to the display images by the liquid crystal panels 1110R and 1110B.

[0081] In this regard, the light corresponding to each primary color, R, G, and B enters into the liquid crystal panels 1110R, 1110B, and 1110G by the dichroic mirror 1108, and thus it is not necessary to dispose color filters.

[0082] 5-3-2: Mobile computer

[0083] Next, a description will be given of an example in which this liquid crystal panel AA is applied to a mobile personal computer. Fig. 8 is a perspective view illustrating the structure of such a personal computer. In the figure, a computer 1200 includes a main unit 1204 having a keyboard 1202, and a liquid crystal display unit 1206. This liquid crystal display unit 1206 is

constituted by adding a back light to the back surface of the liquid crystal panel 1005 described above.

[0084] 5-3-3: Mobile phone

[0085] Furthermore, a description will be given of an example in which the above-described liquid crystal panel AA is applied to a mobile phone. Fig. 9 is a perspective view illustrating the structure of such a mobile phone. In the figure, the mobile phone 1300 includes a reflective liquid crystal panel 1005 together with a plurality of operation buttons 1302. In this reflective liquid crystal panel 1005, a front light is provided on the front surface as necessary.

[0086] In this regard, in addition to the electronic systems described with reference to Figs. 7 to 9, the electronic systems include liquid crystal TVs, view finder-type/monitor-directly-view-type video tape recorders, car navigation systems, pagers, electronic diaries, calculators, word processors, workstations, TV telephones, POS terminals, devices with touch panels, and so on. It goes without saying that the present invention can be applied to these various electronic systems. The panel board may be a panel using an organic LED, plasma, inorganic electro-luminescent element in place of a liquid crystal as an electro-optical material. Moreover, the present invention can be applied to an electrophoretic panel such as electronic paper, and so on.

CLAIMS

What is claimed is:

1. An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a first input terminal supplied with a first input signal;

a second input terminal supplied with a second input signal; and

a drive circuit which controls a grayscale of the pixels based on the first and the second input signals,

wherein the first input signal includes a higher frequency component compared with the second input signal, and the first input terminal has a larger area than the second input terminal.

2. An electro-optical panel according to Claim 1, wherein the first input terminal has a smaller input resistance compared with the second input terminal.

3. An electro-optical panel according to Claim 1, wherein a signal supplied to the first input terminal comprises a driving signal supplied to a scanning-line drive circuit.

4. An electro-optical panel according to Claim 1, wherein a signal

supplied to the second input terminal comprises an image signal.

5. An electro-optical panel according to Claim 1, wherein the first input terminal and the second input terminal, which are disposed along an edge of a substrate, are formed in line, the second input terminal is disposed in the central part of the substrate, and the first input terminal is disposed at the outer side of the substrate.

6. An electro-optical panel according to Claim 1, further comprising a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first input terminal.

7. An electro-optical panel according to Claim 6, wherein the third input terminal includes a plurality of adjacent terminals of at least one of the first input terminal and the second input terminal.

8. An electro-optical panel according to Claim 1, wherein a plurality of the power source terminals, a plurality of the first input terminals, and a plurality of the second input terminals are included;

the plurality of the power source terminals, the plurality of the first input terminals, and the plurality of the second input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first input terminals is an integer multiple of a pitch interval of the adjacent second input terminals.

9. An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 1;

power source means for supplying the power source; and

signal generation means for supplying the input signals.

10. An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 9;

an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate which connects the external substrate and the electro-optical panel,

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of first input terminals and the plurality of second input terminals through an anisotropic conductive film.

11. An electro-optical apparatus according to Claim 10, wherein wiring lines are formed corresponding to a reference pitch interval of the second input terminals on the flexible substrate.

12. An electro-optical panel comprising:

a plurality of data lines on a substrate;

a plurality of scanning lines on the substrate and intersecting the plurality of data lines;

an image display area on the substrate which includes a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a scanning-line drive circuit for driving the pixels;

a data-line drive circuit for supplying data signals to the pixels; and

an input terminal group for supplying signals to the scanning-line drive circuit and the data-line drive circuit,

wherein the scanning-line drive circuit is disposed along one side of the substrate on the substrate, the data-line drive circuit is disposed along a side which is not opposed to the one side on the substrate, the input terminal group is disposed along the data-line drive circuit and is disposed at a further edge side of the substrate than the data-line drive circuit; and

the input terminal group has a first input terminal group for supplying a driving signal to the scanning-line drive circuit and a second input terminal group for supplying an image signal to the data-line drive circuit, the second input terminal is disposed in the central part of the input terminal group, the first input terminal is disposed at the outer side of the input terminal group, and the first input terminal has a larger area than the second input terminal.

13. An electro-optical panel according to Claim 12, further comprising a fourth input terminal for supplying a driving signal to the data-line drive circuit, wherein the fourth input terminal has an area equal to an area of the first input terminal, and the fourth input terminal is disposed between the

first input terminal and the second input terminal.

14. An electronic system comprising the electro-optical apparatus set forth in Claim 1.

ABSTRACT

A liquid crystal panel includes a terminal group made of first to third terminal groups. A driving signal is supplied to the first and the third terminal groups. At the same time, an image signal is supplied to the second terminal group. The driving signal includes a higher frequency component than the image signal. Input terminals of the first and the third terminal groups have a larger area than the input terminals of the second terminal group, and thus the contact resistance thereof is small. Accordingly, it is possible to prevent the driving signal from becoming dull.

FIG.1

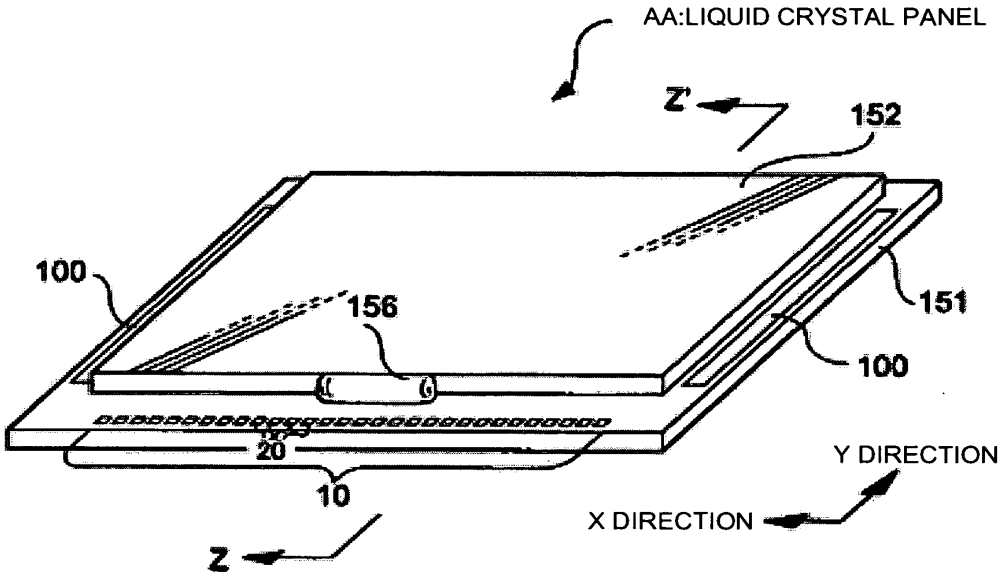
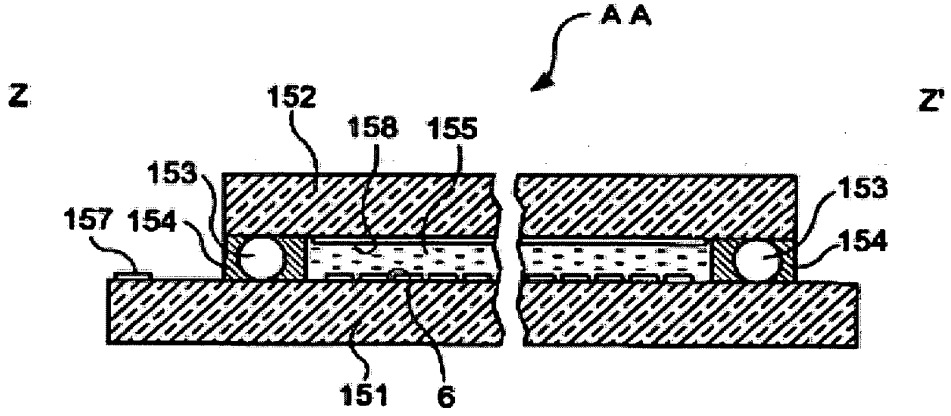

AA:LIQUID CRYSTAL PANEL
Z'
152
100
156
151
100
20
10
Y DIRECTION
X DIRECTION
Z

FIG.2


A A
Z
Z'
152
158
155
153
153
157
154
154
151
6

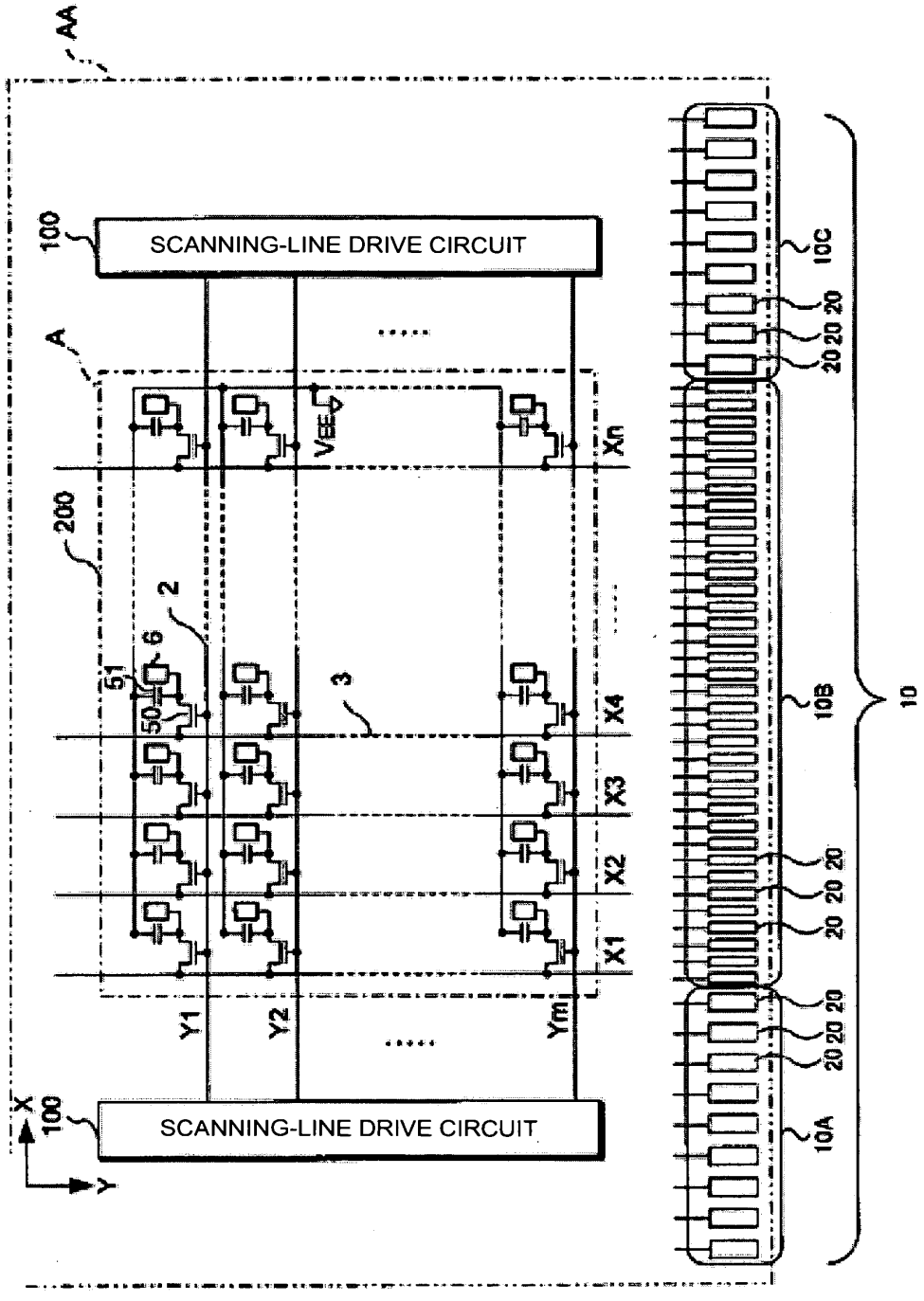

AA
100
SCANNING-LINE DRIVE CIRCUIT
A
200
VEE
Xn
X4
X3
X2
X1
2
6
51
50
3
Y1
Y2
Ym
X
Y
100
SCANNING-LINE DRIVE CIRCUIT
10C
20
10B
10A
10

FIG.3

FIG.4

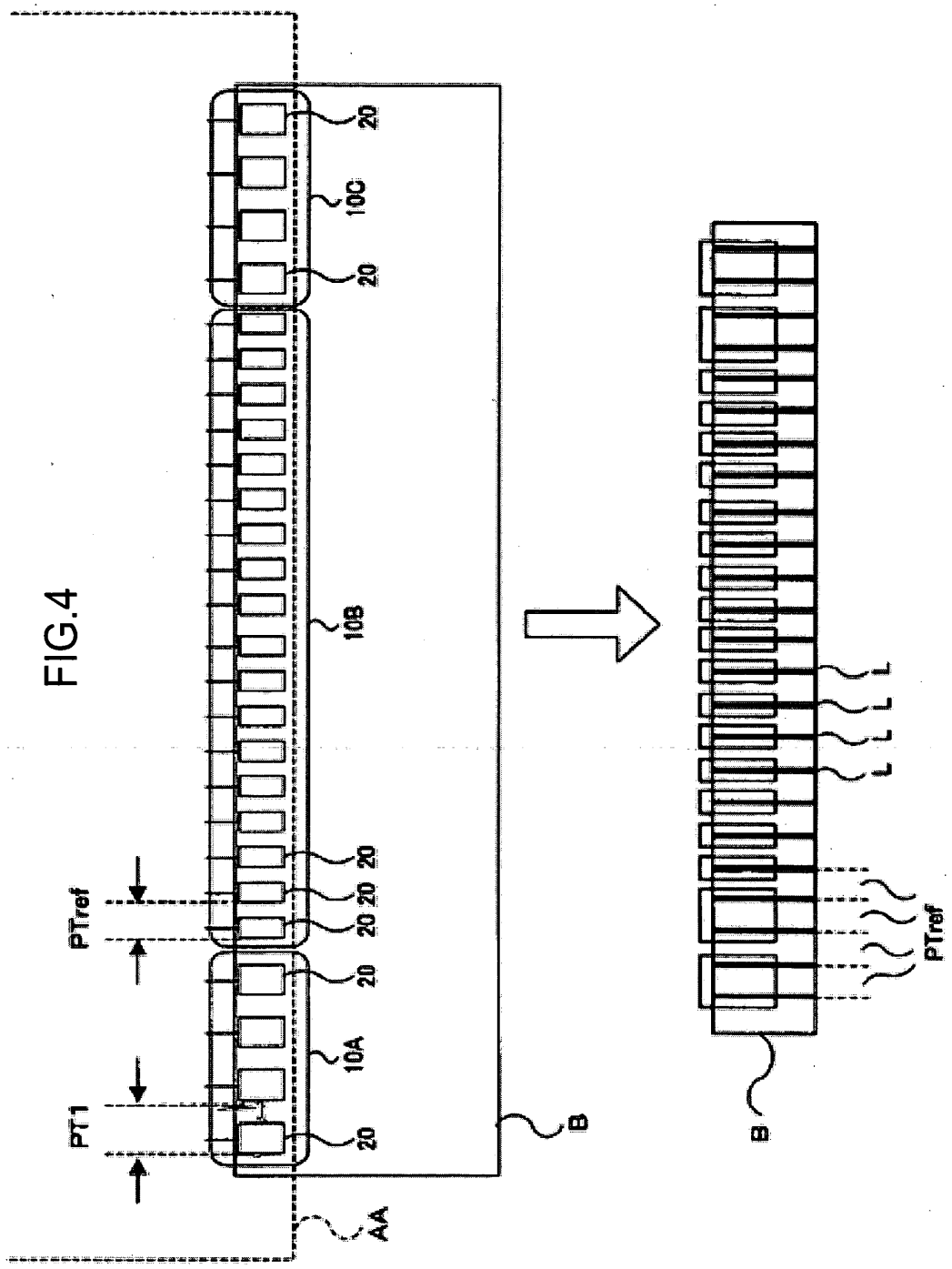


FIG.5

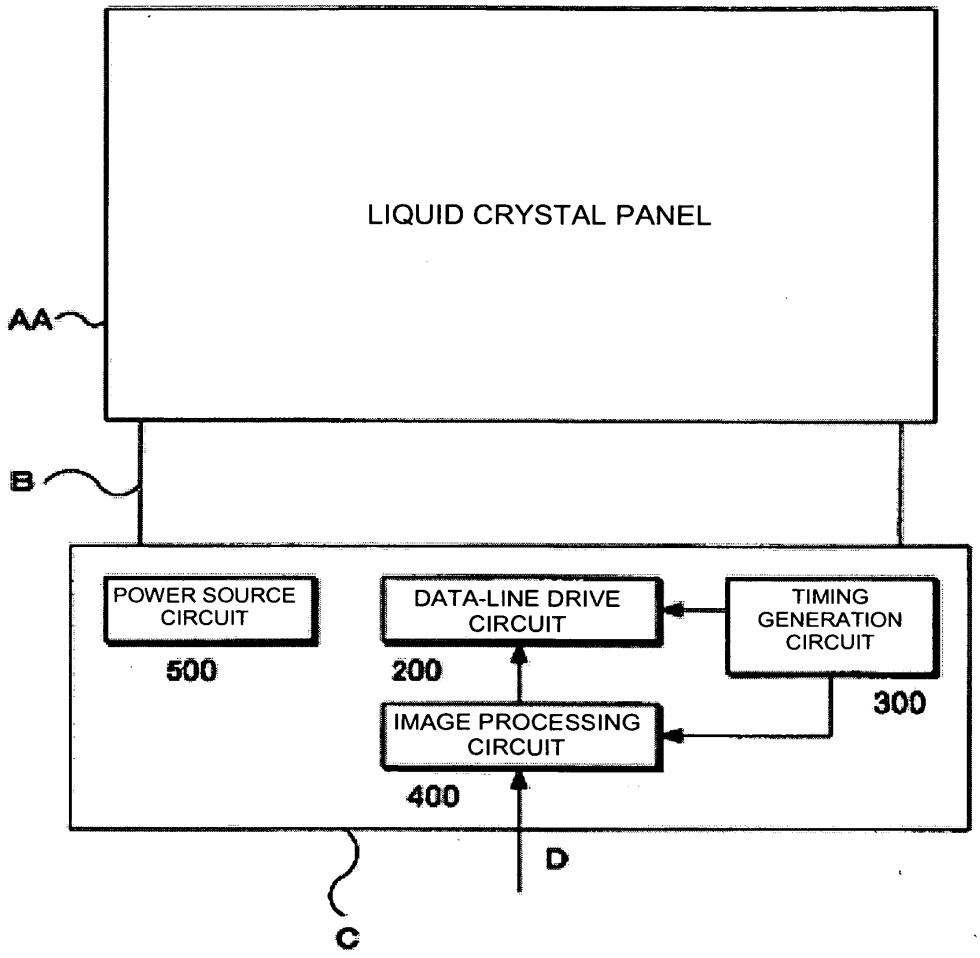

LIQUID CRYSTAL PANEL
AA
B
POWER SOURCE CIRCUIT
500
DATA-LINE DRIVE CIRCUIT
200
TIMING GENERATION CIRCUIT
300
IMAGE PROCESSING CIRCUIT
400
D
C

FIG.6

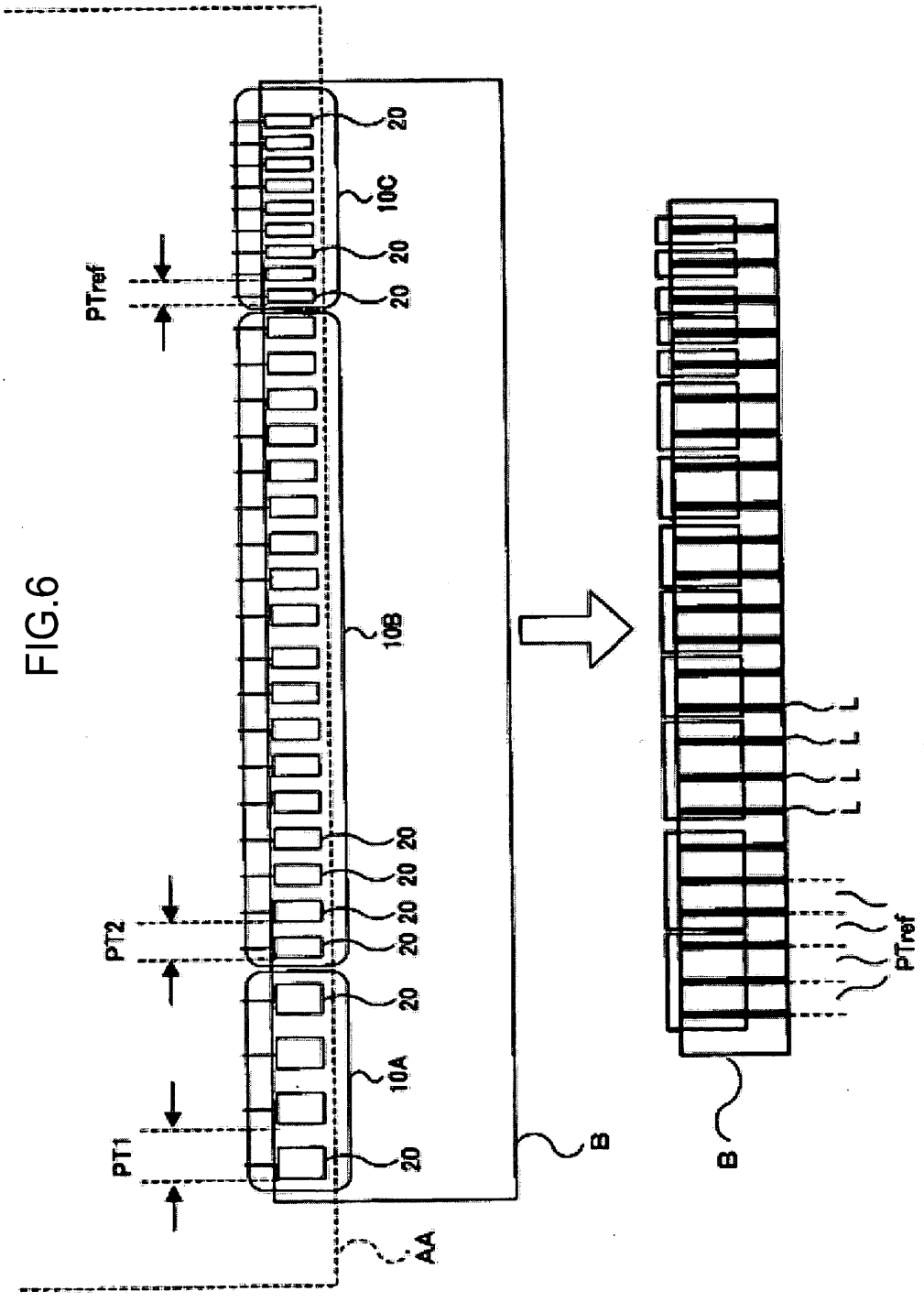

20
10C
20
20
PTref
10B
20
20
20
20
PT2
20
10A
20
PT1
AA
B
L
L
L
L
PTref
B

FIG.7

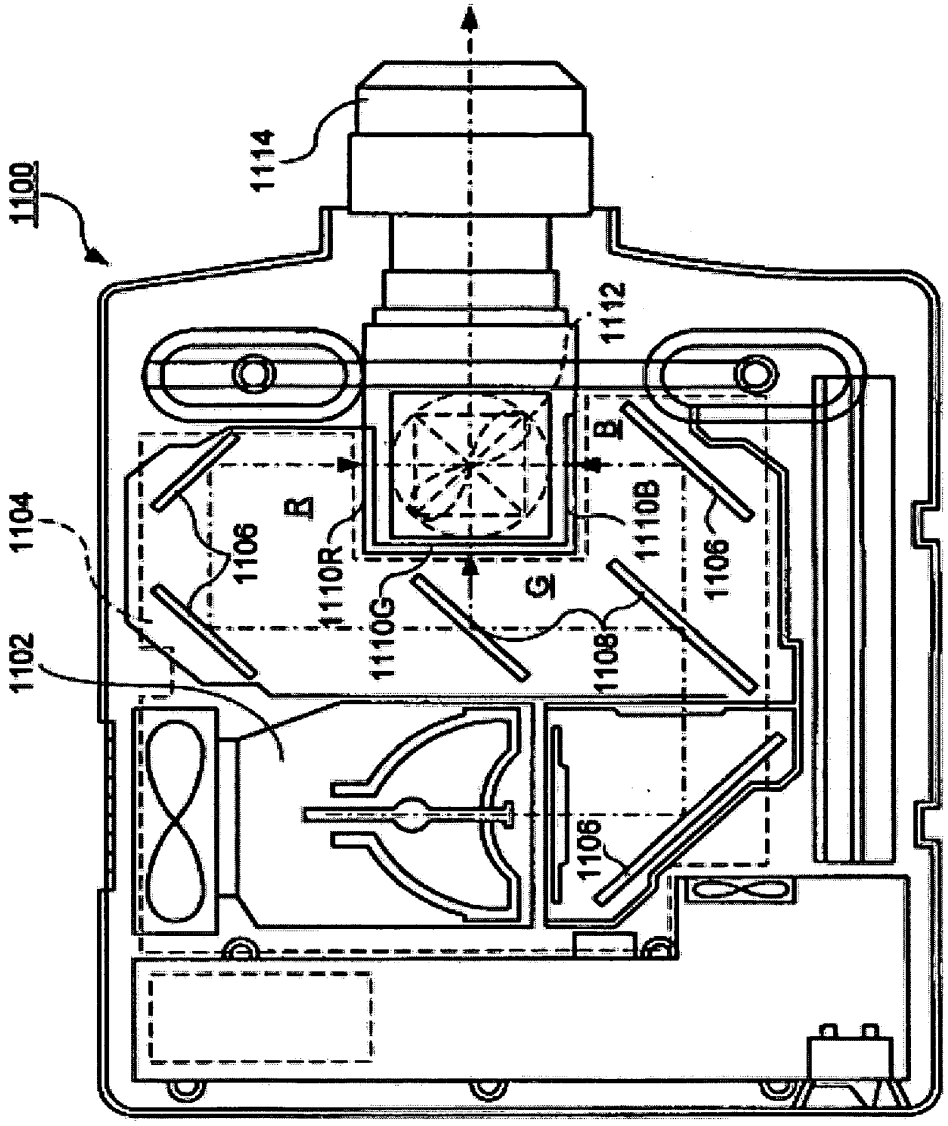

1100
1114
1112
1104
1102
1106
R
1110R
1110G
G
B
1110B
1108
1106
1106

FIG.8

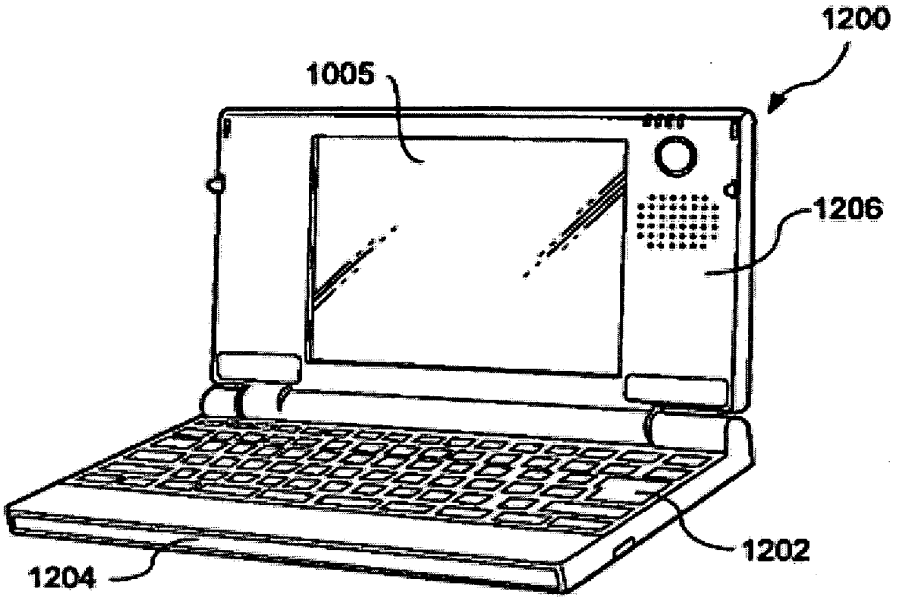


FIG.9

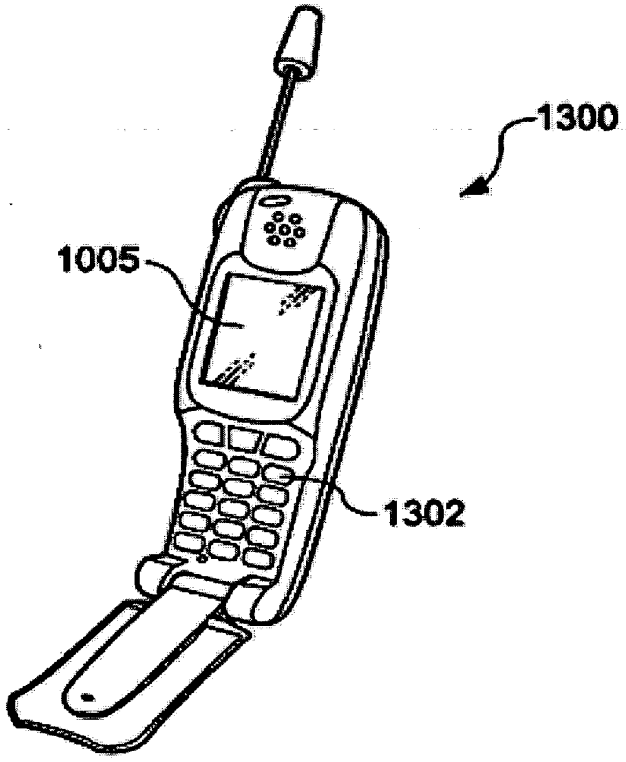
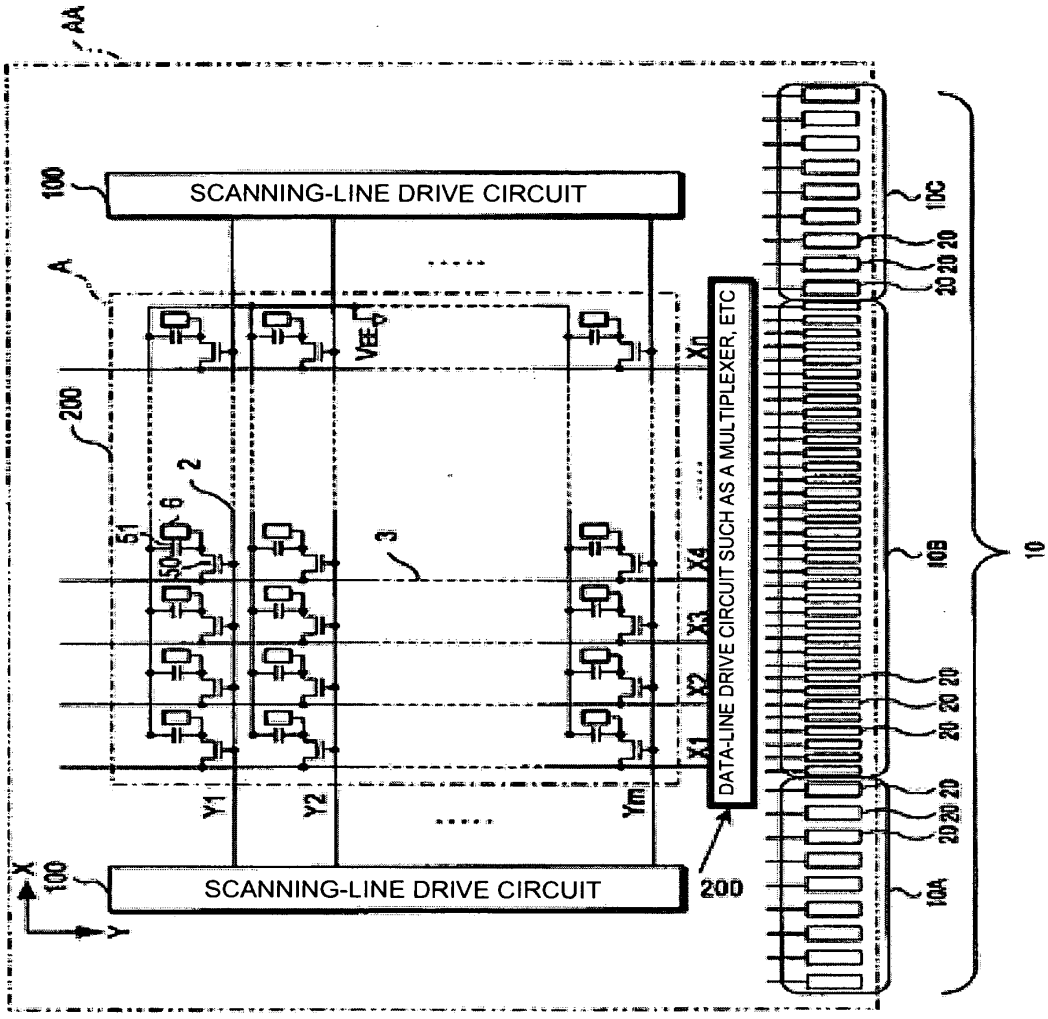


FIG.10


AA
100
SCANNING-LINE DRIVE CIRCUIT
A
200
2
6
51
50
3
VEE
X0
X1
X2
X3
X4
Y1
Y2
Ym
DATA-LINE DRIVE CIRCUIT SUCH AS A MULTIPLEXER, ETC
200
SCANNING-LINE DRIVE CIRCUIT
100
X
Y
10C
10B
10A
10
20

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Citizenship Country:: Japan

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Formal Drawings?:: Yes
Application Type:: Utility
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Secrecy Order in Parent Appl.?:: No

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Priority Claimed:: Yes
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Filing Date:: 06-30-2004
Country:: Japan
Priority Claimed:: Yes

Source:: PrintEFS Version 1.0.1

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Application or Docket Number: 10914044

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	14	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	14 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL		OR	TOTAL	790

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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BOE EXHIBIT 1003
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Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **790** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$920** for a Large Entity

- **$790** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Meaza.W

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 3 - OFFICE COPY

11-12-04

IFW

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NOV 11 2004 PATENT & TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/914,044	08/06/2004	Shin Fujita	9319S-000838

CONFIRMATION NO. 5848

27572
HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

FORMALITIES LETTER

OC000000014019202

Date Mailed: 10/06/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **790** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$920** for a Large Entity

- **$790** Statutory basic filing fee.
- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

11/15/2004 BABRAHA1 00000046 503213 10914044
01 FC:1001 790.00 DA
02 FC:1051 130.00 DA

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/914,044
Filing Date	August 6, 2004
First Named Inventor	Shin Fujita
Art Unit	2673
Examiner Name	N/A
Total Number of Pages in This Submission	
Attorney Docket Number	9319S-000838

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☒ Certified Copy of Priority Document(s)
- ☒ Response to Missing Parts/ Incomplete Application
  - ☒ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:

  Copy of Notice to File Missing Parts, executed Declaration/Power of Attorney, Form HDP-1449 with copy of cited reference and acknowledgement postcard.

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name G. Gregory Schivley	Reg. No. 27,382
Signature			
Date	November 11, 2004		

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	G. Gregory Schivley	Express Mail Label No.	EV 406 076 330 US (11/11/2004)
Signature		Date	November 11, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EV 406 076 330 US

Cc: Hisa Tuttle
408-954-9058
2 Pages

PTO/SB/17 (10-04)
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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 920

Complete If Known	
Application Number	10/914,044
Filing Date	August 6, 2004
First Named Inventor	Shin Fujita
Examiner Name	To Be Assigned
Art Unit	2673
Attorney Docket No.	9319S-000838

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 50-3213

Deposit Account Name: Epson R & D

The Director is authorized to: *(check all that apply)*
☒ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	790
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filling fee	

SUBTOTAL (1) ($) 790

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20 **	0	X		=	0
Independent Claims		-3 **	0	X		=	0
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	130
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,370	2453	685	Petition to revive – unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify) ____	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 130

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	G. Gregory Schivley	*Registration No. (Attorney/Agent)*	27,382	*Telephone*	248-641-1600
Signature				*Date*	November 11, 2004

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE JC103
NOV 11 2004
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PTO/SB/106 (8-96)
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Seiko Epson Ref. No.: J0101160US01 Attorney's Ref. No.: 9319S-000838

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。	As a below named inventor, I hereby declare that:
私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。	My residence, post office address and citizenship are as stated next to my name.
下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
電気光学パネル、電気光学装置及び電子機器	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、	the specification of which is attached hereto unless the following box is checked:
☒ 2004年8月6日に提出され、米国出願番号または特許協定条約 国際出願番号を 10/914,044 とし、（該当する場合） _____ に訂正されました。	☒ was filed on August 6, 2004 as United States Application Number or PCT International Application Number 10/914,044 and was amended on _____ (if applicable).
私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。	I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。	I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office. Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks. Washington, DC 20231.

IPR2025-01396
BOE EXHIBIT 1003
Page 52 of 473

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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条（ａ）－（ｄ)項又は３６５条(ｂ)項に基き下記の、米国以外の国の少なくとも１ヶ国を指定している特許協力条約３６５条(ａ)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
2003-290650	Japan	08/August/2003	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
2004-193515	Japan	30/June/2004	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

私は、第３５編米国法典１１９条(ｅ)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(ｃ)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１章５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

IPR2025-01396
BOE EXHIBIT 1003
Page 53 of 473

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Japanese Language Declaration
(日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

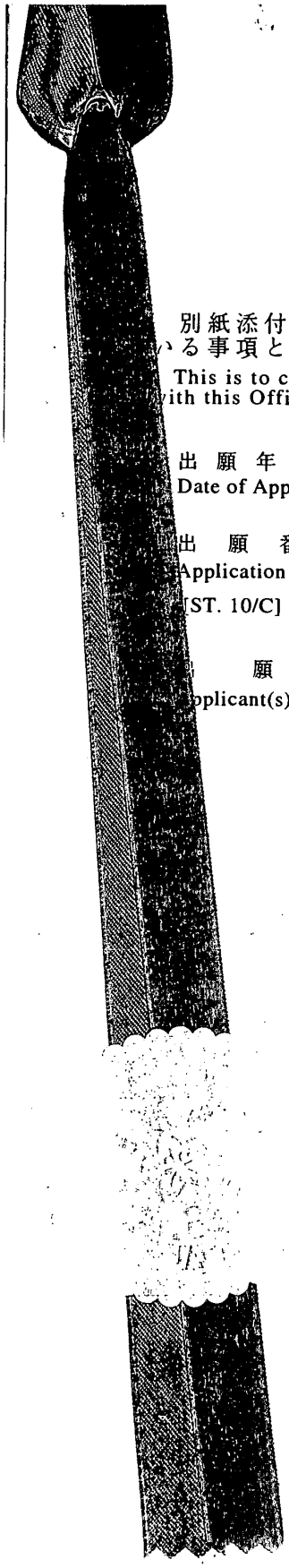
G. Gregory Schivley, (Reg. 27,382)
Bryant Wade, (Reg. 40,344)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

G. Gregory Schivley, (Reg. 27,382)
Bryant Wade, (Reg. 40,344)

書類送付先： Harness, Dickey & Pierce, P.L.C. P.O. Box 828 Bloomfield Hills, Michigan 48303	Send Correspondence to: Harness, Dickey & Pierce, P.L.C. P.O. Box 828 Bloomfield Hills, Michigan 48303
直接電話連絡先： (名前及び電話番号) Harness, Dickey & Pierce, P.L.C. (248) 641-1600	Direct Telephone Calls to: *(name and telephone number)* Harness, Dickey & Pierce, P.L.C. (248) 641-1600
唯一または第一発明者名 藤田 伸	Full name of sole or first inventor Shin FUJITA
発明者の署名 日付 藤田 伸 2004年 10月19日	Inventor's signature Date Shin Fujita October 19, 2004
住所 日本国, 長野県, 諏訪市	Residence Suwa-shi, Nagano-ken, Japan
国籍 日本	Citizenship Japan
私書箱 392-8502 日本国長野県諏訪市大和3丁目3番5号 セイコーエプソン株式会社内	Post Office Address c/o Seiko Epson Corporation 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan
第二共同発明者	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所 日本国, _____, _____	Residence _____, _____, Japan
国籍	Citizenship
私書箱	Post Office Address
(第三以降の共同発明者についても同様に記載し、署名をすること)	(Supply similar information and signature for third and subsequent joint inventors.)

IPR2025-01396
BOE EXHIBIT 1003
Page 54 of 473



日本国特許庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出願年月日
Date of Application: ２００３年　８月　８日

出願番号
Application Number: 特願２００３－２９０６５０

[ST. 10/C]: [ＪＰ２００３－２９０６５０]

願人
Applicant(s): セイコーエプソン株式会社

CERTIFIED COPY OF
PRIORITY DOCUMENT
BEST AVAILABLE COPY

２００４年　７月２７日

特許庁長官
Commissioner,
Japan Patent Office

小川

出証番号　出証特２００４－３０６６０５３

IPR2025-01396
BOE EXHIBIT 1003
Page 55 of 473

【書類名】　特許願
【整理番号】　J0101160
【あて先】　特許庁長官殿
【国際特許分類】　G02F　1/13
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【書類名】特許請求の範囲
【請求項１】
複数のデータ線、複数の走査線、及び前記データ線と前記走査線との交差に対応して設けられた複数の画素と、電源が供給される複数の電源端子と複数の入力信号が各々供給される複数の入力端子と、前記複数の電源端子を介して前記電源が供給され、前記複数の入力端子を介して供給される前記複数の入力信号に基づいて前記画素の階調を制御する駆動回路とを備えた電気光学パネルであって、
前記複数の入力端子は、入力抵抗値の異なる複数種類の入力端子を含み、
前記複数の入力信号の伝送するために必要とされる伝送特性に応じて、前記各入力信号が供給される前記入力端子の種類が定められている
ことを特徴とする電気光学パネル。
【請求項２】
前記複数種類の入力端子は、面積の相違によって入力抵抗値が異なることを特徴とする請求項１に記載の電気光学パネル。
【請求項３】
前記複数の入力信号が供給される前記入力端子の面積は、前記入力信号の周波数特性に応じて設定されていることを特徴とする請求項２に記載の電気光学パネル。
【請求項４】
前記複数の入力信号は、複数の駆動信号と複数の画像信号とを含み、
前記複数の駆動信号の周波数特性は、前記複数の画像信号の周波数特性と比較して、高域の周波数成分を含み、
前記複数の駆動信号が供給される前記入力端子の面積は、前記複数の画像信号が供給される前記入力端子の面積よりも大きいことを特徴とする請求項３に記載の電気光学パネル。
【請求項５】
前記複数の電源端子及び前記複数の入力端子は、一列に並んで形成されており、
前記複数の電源端子及び前記複数種類の入力端子のうち、面積が最小の端子間のピッチを基準ピッチとしたとき、他の種類における入力端子間のピッチ又は電源端子間のピッチは、前記基準ピッチの整数倍となることを特徴とする請求項２乃至４のうちいずれか１項に記載した電気光学パネル。
【請求項６】
請求項１乃至５のうちいずれか１項に記載した電気光学パネルと、
前記電源を供給する電源手段と、
前記入力信号を供給する信号生成手段と
を備えたことを特徴とする電気光学装置。
【請求項７】
請求項５に記載した電気光学パネルと、
前記電源を供給する電源手段と、前記入力信号を供給する信号生成手段とを備えた外部基板と、
前記外部基板と前記電気光学パネルとを接続するフレキシブル基板とを備え、
前記フレキシブル基板は、異方性導電膜を介して前記複数の電源端子及び前記複数の入力端子と接続される
ことを特徴とする電気光学装置。
【請求項８】
前記フレキシブル基板には、前記基準ピッチの間隔で配線が形成されていることを特徴とする請求項７に記載の電気光学装置。
【請求項９】
請求項６乃至８のうちいずれか１項に記載した電気光学装置を備えたことを特徴とする電子機器。

出証特２００４－３０６６０５３

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【書類名】明細書
【発明の名称】電気光学パネル、電気光学装置及び電子機器
【技術分野】
【０００１】
本発明は、電気光学パネル、電気光学装置及び電子機器に関する。
【背景技術】
【０００２】
表示装置、例えば、電気光学材料として液晶を用いた液晶表示装置は、陰極線管（ＣＲＴ）に代わるディスプレイデバイスとして、各種情報処理機器の表示部や液晶テレビなどに広く用いられている。
【０００３】
ここで、従来の電気光学装置は、例えば、次のように構成されている。すなわち、従来の電気光学装置は、マトリクス状に配列した画素電極と、この画素電極に接続されたＴＦＴ（Thin Film Transistor：薄膜トランジスタ）のようなスイッチング素子などが設けられた素子基板と、画素電極に対向する対向電極が形成された対向基板と、これら両基板との間に充填された電気光学材料たる液晶とを備える。画素は、スイッチング素子、画素電極、電気光学材料及び対向電極によって構成され、マトリクス状に配置される。このような構成において、走査線を介してスイッチング素子に走査信号を印加すると、当該スイッチング素子が導通状態となる。この導通状態の際に、データ線を介して画素電極に、階調に応じた電圧の画像信号を印加すると、当該画素電極および対向電極の間の液晶層に画像信号の電圧に応じた電荷が蓄積される。電荷蓄積後、当該スイッチング素子をオフ状態としても、当該液晶層における電荷の蓄積は、液晶層自身の容量や蓄積容量などによって維持される。このように、各スイッチング素子を駆動させ、蓄積させる電荷量を階調に応じて制御すると、画素毎に液晶の配向状態が変化するので、画素毎に濃度が変化することになる。このため、階調表示することが可能となるのである。
【０００４】
このような電気光学装置は、上述した画素がマトリクス状に配置される電気光学パネルを備える。電気光学パネルには、走査線を駆動する走査線駆動回路、あるいはデータ線を駆動するデータ線駆動回路が形成されることがある。駆動回路を備えた電気光学パネルには、電源、駆動信号、及び画像信号等が供給される。電源等を電気光学パネルに供給する手段として、電気光学パネルに形成された入力端子と接続ケーブルとしてのフレキシブル基板と異方性導電膜を介して接続する技術が知られている（例えば、特許文献１）。
【０００５】
【特許文献１】特許第２８２２５５８号公報
【発明の開示】
【発明が解決しようとする課題】
【０００６】
ところで、入力端子の抵抗は、その面積が大きい程小さくなるため、抵抗値を低減する観点からは入力端子の大きさは大きいことが望ましい。しかしながら、接触抵抗を低減する観点から、入力端子の面積を大きくすると、限られた面積の中に全ての入力端子を配置することができないといった問題があった。
【０００７】
特に、データ線駆動回路を内蔵しないタイプの電気光学パネル、又はマルチプレクサを内蔵するタイプの電気光学パネルにおいては、複数の画像信号を電気光学パネルに取り込む必要があるため、入力端子の数が多くなる。これに伴って、フレキシブル基板等を実装した際に、接続不良等の問題が発生していた。一方、実装エリアを狭くする観点から、入力端子の面積を小さくすると、接触抵抗が増加し、駆動信号が正規のタイミングで入力できないという問題があった。
【０００８】
そこで、本発明は、フレキシブル基板等の実装部品を高い信頼性の下に接続することが

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でき、且つ、信号の伝送に必要な帯域を確保することが可能な電気光学パネル及び電気光学装置、並びにこれらを用いた電子機器を提供することを解決課題とする。

【課題を解決するための手段】

【０００９】

上述した課題を解決するため、本発明に係る電気光学パネルは、複数のデータ線、複数の走査線、及び前記データ線と前記走査線との交差に対応して設けられた複数の画素と、電源が供給される複数の電源端子と複数の入力信号が各々供給される複数の入力端子と、前記複数の電源端子を介して前記電源が供給され、前記複数の入力端子を介して供給される前記複数の入力信号に基づいて前記画素の階調を制御する駆動回路とを備えたものであって、前記複数の入力端子は、入力抵抗値の異なる複数種類の入力端子を含み、前記複数の入力信号の伝送するために必要とされる伝送特性に応じて、前記各入力信号が供給される前記入力端子の種類が定められていることを特徴とする。

【００１０】

この発明によれば、電気光学パネルには、入力抵抗値が異なる複数種類の入力端子が設けられている。そして、複数の入力信号の伝送するために必要とされる伝送特性に応じて、各入力信号が供給される入力端子の種類が定められている。このため、必要とされる伝送特性の時定数が小さい入力信号は、入力抵抗値の低い入力端子に供給され、必要とされる伝送特性の時定数が大きい入力信号は、入力抵抗値の高い入力端子に供給される。従って、入力信号の伝送特性に応じて、入力端子を適切に設定することが可能となる。なお、入力抵抗値には、実装部材を接続する場合の接触抵抗値が含まれる。

【００１１】

ここで、前記複数種類の入力端子は、面積の相違によって入力抵抗値が異なるものであってもよい。一般に、端子の入力抵抗は、面積に比例する。従って、面積が大きい入力端子程、入力抵抗値が低くなる。この発明によれば、入力信号の伝送特性に応じて、入力端子の面積を相違させることができるので、時定数が大きくても信号を十分伝送することが可能な入力端子の面積を小さくする一方、時定数が小さい特性が要求される入力信号が供給される入力端子については、大きな面積を確保することが可能となる。この場合、前記複数の入力信号が供給される前記入力端子の面積は、前記入力信号の周波数特性に応じて設定されることが好ましい。高い周波数成分を含む入力信号については、時定数を小さく設定することにより、当該入力信号の波形をなまらずに取り込むことができ、比較的低い周波数成分から構成される入力信号については、時定数が大きくても問題が無いので、入力端子の面積を小さくすることが可能である。

【００１２】

より具体的には、前記複数の入力信号は、複数の駆動信号と複数の画像信号とを含み、前記複数の駆動信号の周波数特性は、前記複数の画像信号の周波数特性と比較して、高域の周波数成分を含み、前記複数の駆動信号が供給される前記入力端子の面積は、前記複数の画像信号が供給される前記入力端子の面積よりも大きいことが好ましい。この場合には、駆動信号の波形をなまらせずに電気光学パネルに取り込むことによって、画像の表示の誤動作を防止できる一方、画像信号の入力端子の面積を小さくすることができるので、限られた面積に多数の入力端子を配置することができる。このように、入力信号の周波数特性に着目して、入力端子の面積を割り当てることによって、限られた面積に中に入力端子を適切に配置することが可能となる。

【００１３】

上述した電気光学パネルにおいて、前記複数の電源端子及び前記複数の入力端子は、一列に並んで形成されており、前記複数の電源端子及び前記複数種類の入力端子のうち、面積が最小の端子間のピッチを基準ピッチとしたとき、他の種類における入力端子間のピッチ又は電源端子間のピッチは、前記基準ピッチの整数倍となることが好ましい。この発明によれば、実装部材を複数の電源端子及び複数の入力端子に実装する場合に、実装部材の収縮率の見積もりが容易となり、実装不良を未然に防止することができる。

【００１４】

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次に、本発明に係る電気光学装置は、上述した電気光学パネルと、前記電源を供給する電源手段と、前記入力信号を供給する信号生成手段とを備えたことを特徴とする。この電気光学装置は上述した電気光学パネルを備えるので、フレキシブル基板等の実装部品を高い信頼性の下に接続することができ、且つ、信号の伝送に必要な帯域を確保することが可能となる。

【００１５】

また、本発明に係る電気光学装置は、前記電源を供給する電源手段と、前記入力信号を供給する信号生成手段とを備えた外部基板と、前記外部基板と前記電気光学パネルとを接続するフレキシブル基板とを備え、前記フレキシブル基板は、異方性導電膜を介して前記複数の電源端子及び前記複数の入力端子と接続されることが好ましい。

【００１６】

ここで、前記フレキシブル基板には、前記基準ピッチの間隔で配線が形成されていることが好ましい。幅の異なる端子が混在する端子群に対して各配線を確実に接続することができる。そして、面積の広い端子に対しては、複数の配線が割り当てられるから、接触抵抗と配線抵抗を低減することができる。

【００１７】

次に、本発明に係る電子機器は上述した電気光学装置を備える。このような電子機器としては、液晶プロジェクタ、パーソナルコンピュータ、携帯電話、電子カメラ、ＰＤＡ等が該当する。

【００１８】

このように本発明によれば、フレキシブル基板等の実装部品を高い信頼性の下に接続することができ、且つ、信号の伝送に必要な帯域を確保することが可能な電気光学パネル及び電気光学装置、並びにこれらを用いた電子機器を提供することができる。

【発明を実施するための最良の形態】

【００１９】

以下、図面を参照して、本発明に係わる実施形態を説明する。なお、本実施形態では、電気光学材料として液晶を用いた液晶パネルを電気光学パネルの一例とし、液晶パネルを用いた液晶表示装置を電気光学装置の一例として説明するが、本発明はこれに限定されるものではなく、有機発光ダイオード素子を備える有機ＥＬパネル等も電気光学パネルに含まれることは勿論である。

【００２０】

＜１．液晶パネルの機械的構成＞

まず、第１実施形態に係わる液晶パネルＡＡの機械的構成について図１及び図２を参照して説明する。ここで、図１は、液晶パネルＡＡの構成を示す斜視図であり、図２は、図１におけるＺ－Ｚ’線断面図である。

【００２１】

これらの図に示されるように、液晶パネルＡＡは、画素電極６等が形成されたガラスや半導体等の素子基板１５１と、共通電極１５８等が形成されたガラス等の透明な対向基板１５２とを、スペーサ１５３が混入されたシール材１５４によって一定の間隙を保って、互いに電極形成面が対向するように貼り合わせるとともに、この間隙に電気光学材料としての液晶１５５を封入した構造となっている。なお、シール材１５４は、対向基板１５２の基板周辺に沿って形成されるが、液晶１５５を封入するために一部が開口している。このため、液晶１５５の封入後に、その開口部分が封止材１５６によって封止されている。

【００２２】

ここで、素子基板１５１の対向面であって、シール材１５４の外側一辺においては、端子群１０が形成されている。端子群１０は、複数の入力端子２０から構成される。複数の入力端子２０の一部には、画像信号が供給され、Ｙ方向に延在するデータ線３を駆動する構成となっている。さらに、この一辺には端子群１０が形成されている。また、この一辺に隣接する一辺には、走査線駆動回路１００が形成されて、Ｘ方向に延在する走査線２をそれぞれ両側から駆動する構成となっている。

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【００２３】
端子群１０は、異方性導電フィルムを介して電気的および機械的に実装部材と接続される。この例の実装部材は、接続ケーブルとしてのフレキシブル基板と外部基板とを含む。対向基板１５２の共通電極１５８は、素子基板１５１との貼合部分における４隅のうち、少なくとも１箇所において設けられた導通材によって、素子基板１５１との電気的導通が図られている。ほかに、対向基板１５２には、液晶パネルＡＡの用途に応じて、例えば、第１に、ストライプ状や、モザイク状、トライアングル状等に配列したカラーフィルタが設けられ、第２に、例えば、クロムやニッケルなどの金属材料や、カーボンやチタンなどをフォトレジストに分散した樹脂ブラックなどのブラックマトリクスが設けられ、第３に、液晶パネルＡＡに光を照射するバックライトが設けられる。特に色光変調の用途の場合には、カラーフィルタは形成されずにブラックマトリクスが対向基板１５２に設けられる。

【００２４】
くわえて、素子基板１５１および対向基板１５２の対向面には、それぞれ所定の方向にラビング処理された配向膜などが設けられる一方、その各背面側には配向方向に応じた偏光板（図示省略）がそれぞれ設けられる。ただし、液晶１５５として、高分子中に微小粒として分散させた高分子分散型液晶を用いれば、前述の配向膜、偏光板等が不要となる結果、光利用効率が高まるので、高輝度化や低消費電力化などの点において有利である。

【００２５】
なお、走査線駆動回路１００等の周辺回路の一部または全部を、素子基板１５１に形成する替わりに、例えば、ＴＡＢ（Tape Automated Bonding）技術を用いてフィルムに実装された駆動用ＩＣチップを、素子基板１５１の所定位置に設けられる異方性導電フィルムを介して電気的および機械的に接続する構成としても良いし、駆動用ＩＣチップ自体を、ＣＯＧ（Chip On Grass）技術を用いて、素子基板１５１の所定位置に異方性導電フィルムを介して電気的および機械的に接続する構成としても良い。

【００２６】
＜２．液晶パネルの電気的構成＞
図３は、液晶パネルの電気的構成を示すブロック図である。この図に示すように液晶パネルＡＡは、走査線駆動回路１００、画像表示領域Ａ、及び端子群１０を備える。端子群１０は、第１端子群１０Ａ、第２端子群１０Ｂ、第３端子群１０Ｃを備える。第１端子群１０Ａ及び第３端子群１０Ｂには、走査線駆動回路１００を駆動するため各駆動信号及び電源が供給される。即ち、第１端子群１０Ａ及び第３端子群１０Ｂを構成する一部の入力端子２０は、電源端子として機能する。一方、第２端子群１０Ｂには画像信号が供給される。

【００２７】
この例において、液晶パネルＡＡには、電源の他に入力信号として駆動信号と画像信号とが供給される。このうち、駆動信号は、Ｙ転送開始パルスＤＹ、Ｙクロック信号ＹＣＫ及び反転Ｙクロック信号ＹＣＫＢ等を含む。これらの駆動信号の周波数特性は、画像信号の周波数特性と比較して、高域の周波数成分を含む。従って、走査線駆動回路１００を正常に動作させるためには、駆動信号がなまらないように伝送する必要がある。駆動信号は、フレキシブル基板を介して伝送されるが、この伝送路には、分布容量や分布抵抗が存在し、等価的にローパスフィルタが構成される。従って、駆動信号の信号波形がなまらないように伝送するためには、等価的なローパスフィルタの時定数を下げる必要がある。分布抵抗のうち、入力端子２０で発生する接触抵抗の割合は、大きく無視することはできない。接触抵抗は入力端子２０の面積が大きくなる程、小さくなる。そこで、本実施形態においては、画像信号が供給される入力端子と比較して駆動信号が供給される入力端子の面積を大きくしている。具体的には、第１及び第３端子群１０Ａ及び１０Ｃを構成する入力端子２０は、第２端子群１０Ｂを構成する入力端子２０よりも面積が大きい。

【００２８】
換言すれば、入力信号が供給される複数の入力端子２０は、入力抵抗値の異なる複数種

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類の入力端子２０を含み、各入力信号の伝送するために必要とされる伝送特性に応じて、各入力信号が供給される入力端子２０の種類が定められている。これにより、比較的高い周波数成分を有する駆動信号を正確に伝送するとともに、比較的低い周波数成分を有する画像信号が供給される第２端子群１０Ｂを構成する入力端子２０の面積を小さくすることにより、限られた面積の中に必要とされる数の入力端子２０を配置することが可能となる。

【００２９】

次に、走査線駆動回路１００は、シフトレジスタ等を備える。走査線駆動回路１００には、Ｙ転送開始パルスＤＹ、Ｙクロック信号ＹＣＫ及び反転Ｙクロック信号ＹＣＫＢ、電源ＶＨＨ及びＶＳＳが供給される。図３において、左側の走査線駆動回路１００には第１端子群１０Ａから駆動信号及び電源が供給される一方、右側の走査線駆動回路１００には第３端子群１０Ｃから駆動信号及び電源が供給される。

【００３０】

走査線駆動回路１００は、シフトレジスタを用いてＹクロック信号ＹＣＫおよび反転Ｙクロック信号ＹＣＫＢに同期して、Ｙ転送開始パルスＤＹを順次転送し、さらにレベル変換を行って走査信号Ｙ１、Ｙ２、…、Ｙｍを生成し、各走査線２に出力する。

【００３１】

次に、画像表示領域Ａには、図３に示されるように、ｍ（ｍは２以上の自然数）本の走査線２が、Ｘ方向に沿って平行に配列して形成される一方、ｎ（ｎは２以上の自然数）本のデータ線３が、Ｙ方向に沿って平行に配列して形成されている。そして、走査線２とデータ線３との交差付近においては、ＴＦＴ５０のゲートが走査線２に接続される一方、ＴＦＴ５０のソースがデータ線３に接続されるとともに、ＴＦＴ５０のドレインが画素電極６に接続される。そして、各画素は、画素電極６と、対向基板に形成される対向電極（後述する）と、これら両電極間に挟持された液晶とによって構成される。この結果、走査線２とデータ線３との各交差に対応して、画素はマトリクス状に配列されることとなる。

【００３２】

また、ＴＦＴ５０のゲートが接続される各走査線２には、走査信号Ｙ１、Ｙ２、…、Ｙｍが、パルス的に線順次で印加されるようになっている。このため、ある走査線２に走査信号が供給されると、当該走査線に接続されるＴＦＴ５０がオンするので、データ線３から所定のタイミングで供給されるデータ線信号Ｘ１、Ｘ２、…、Ｘｎ（画像信号）は、対応する画素に順番に書き込まれた後、所定の期間保持されることとなる。

【００３３】

各画素に印加される電位レベルに応じて液晶分子の配向や秩序が変化するので、光変調による階調表示が可能となる。例えば、液晶を通過する光量は、ノーマリーホワイトモードであれば、印加電位が高くなるにつれて制限される一方、ノーマリーブラックモードであれば、印加電位が高くなるにつれて緩和されるので、液晶表示装置全体では、画像信号に応じたコントラストを持つ光が各画素毎に出射される。このため、所定の表示が可能となる。

【００３４】

＜３．端子群１０とフレキシブル基板Ｂとの関係＞

次に、端子群１０とフレキシブル基板Ｂとの詳細な構成について説明する。図４は、端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。上述したように端子群１０は、面積の異なる２種類の入力端子２０から構成されている。この例では、第２端子群１０Ｂを構成する入力端子２０の面積が最も小さく、また、入力端子２０間のピッチが最小となる。本実施形態においては、面積の異なる複数種類の入力端子２０（電源端子を含む）のうち、面積が最小の端子間のピッチを基準ピッチＰＴｒｅｆと称する。この例では、第２端子群１０Ｂを構成する入力端子２０の面積が最小であるから、第２端子群１０Ｂを構成する入力端子２０の間隔が基準ピッチＰＴｒｅｆとなる。

【００３５】

一方、第１端子群１０Ａ及び第３端子群１０Ｃを構成する入力端子２０のピッチは等し

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い。このピッチを第１ピッチＰＴ１と称する。さらに、第１ピッチＰＴ１は基準ピッチＰＴｒｅｆの整数倍となるように設定することが好ましい。フレキシブル基板Ｂと端子群１０の接続は異方性導電膜（ＡＣＦ：anisotropic conductive film）を介して行われる。この際、熱と圧力とを加えるため、フレキシブル基板Ｂが収縮する。上述したように整数倍の関係に設定すると、フレキシブル基板Ｂ等の実装部材を端子群１０に実装する場合に、実装部品の収縮率の見積もりが容易となり、実装不良を未然に防止することができる。

【００３６】

また、フレキシブル基板Ｂには、配線Ｌが基準ピッチＰＴｒｅｆの間隔で形成されている。これによって、幅の異なる入力端子２０が混在する端子群１０に対して各配線Ｌを確実に接続することができる。そして、面積の広い入力端子２０に対しては、２本の配線Ｌが割り当てられるから、接触抵抗と配線抵抗を低減することができる。

【００３７】

＜４．液晶表示装置の全体構成＞

図５に液晶表示装置の全体構成を示す。外部基板Ｃは、フレキシブル基板Ｃを介して液晶パネルＡＡに接続されている。外部基板Ｃは、データ線駆動回路２００、タイミング発生回路３００、画像処理回路４００、及び電源回路５００を備える。この液晶表示装置に供給される入力画像データＤは、例えば、３ビットパラレルの形式である。タイミング発生回路３００は、入力画像データＤに同期してＹクロック信号ＹＣＫ、反転Ｙクロック信号ＹＣＫＢ、Ｘクロック信号ＸＣＫ、反転Ｘクロック信号ＸＣＫＢ、Ｙ転送開始パルスＤＹおよびＸ転送開始パルスＤＸを生成する。また、タイミング発生回路３００は、画像処理回路４００を制御する各種のタイミング信号を生成し、これを出力する。

【００３８】

Ｙクロック信号ＹＣＫは、走査線２を選択する期間を特定し、反転Ｙクロック信号ＹＣＫＢはＹクロック信号ＹＣＫの論理レベルを反転したものである。Ｘクロック信号ＸＣＫは、データ線３を選択する期間を特定し、反転Ｘクロック信号ＸＣＫＢはＸクロック信号ＸＣＫの論理レベルを反転したものである。

【００３９】

画像処理回路４００は、入力画像データＤに、液晶パネルＡＡの光透過特性を考慮したガンマ補正等を施した後、画像データをデータ線駆動回路２００に供給する。データ線駆動回路２００は、Ｘクロック信号ＸＣＫ及び反転Ｘクロック信号ＸＣＫＢに同期してＸ転送開始パルスＤＸを順次転送してサンプリング信号を生成し、生成したサンプリング信号を用いて画像データをサンプリングして、線順次の画像データを生成し、さらにＤ／Ａ変換を施して、線順次の画像信号を生成する。この画像信号はフレキシブル基板Ｃを介して液晶パネルＡＡに供給される。

【００４０】

電源回路５００は、走査線駆動回路１００に高電位電源ＶＤＤ及び低電位電源ＶＳＳを供給する他、タイミング発生回路３００及び画像処理回路４００に所定の電源を供給する。以上の構成において、データ線駆動回路２００、タイミング発生回路３００、及び画像処理回路４００は、液晶パネルＡＡに入力信号を供給する信号生成手段として機能する。

【００４１】

＜５．応用例＞

＜５－１：端子群１０とフレキシブル基板Ｂとの関係＞

上述した実施形態においては、入力端子２０として面積が異なる２種類の端子を用いたが本発明はこれに限定されるものではなく、３種類以上の入力端子２０を備えるものであってもよい。図６は、応用例における端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。この例においては、第３端子群１０Ｃを構成する入力端子２０の面積が最小である。このため、第３端子群１０Ｃを構成する入力端子２０の間隔が基準ピッチＰＴｒｅｆとなる。第２端子群１０Ｂの入力端子２０は第２ピッチＰＴ２の間隔で形成されており、第１端子群１０Ａの入力端子２０は第１ピッチＰＴ１の間隔で形成されている。

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【００４２】
この場合、ＰＴｒｅｆ、ＰＴ１、ＰＴ２には、２ＰＴｒｅｆ＝ＰＴ２、３ＰＴｒｅｆ＝ＰＴ１の関係がある。即ち、複数の電源端子及び複数種類の入力端子のうち、面積が最小の端子間のピッチを基準ピッチＰＴｒｅｆとしたとき、他の種類における入力端子間のピッチＰＴ１、ＰＴ２又は電源端子間のピッチＰＴ１、ＰＴ２は、基準ピッチＰＴｒｅｆの整数倍となる。
【００４３】
また、フレキシブル基板Ｂには、配線Ｌが基準ピッチＰＴｒｅｆの間隔で形成されている。これによって、幅の異なる入力端子２０が混在する端子群１０に対して各配線Ｌを確実に接続することができる。そして、面積の広い入力端子２０に対しては、２本又は３本の配線Ｌが割り当てられるから、接触抵抗と配線抵抗を低減することができる。
【００４４】
＜５－２：電気光学装置の他の例＞
また、上述した実施の形態にあっては、画素のスイッチング素子を、ＴＦＴで代表される３端子素子として説明したが、ダイオード等の２端子素子で構成しても良い。ただし、画素のスイッチング素子として２端子素子を用いる場合には、走査線２を一方の基板に形成し、データ線３を他方の基板に形成するとともに、２端子素子を、走査線２またはデータ線３のいずれか一方と、画素電極との間に形成する必要がある。この場合、画素は、走査線２とデータ線３との間に直列接続された二端子素子と、液晶とから構成されることとなる。
【００４５】
また、本発明は、アクティブマトリクス型液晶表示装置として説明したが、これに限られず、ＳＴＮ（Super Twisted Nematic）液晶などを用いたパッシブ型にも適用可能である。さらに、電気光学材料としては、液晶のほかに、エレクトロルミネッセンス素子などを用いて、その電気光学効果により表示を行う表示装置にも適用可能である。すなわち、本発明は、上述した液晶装置と類似の構成を有するすべての電気光学装置に適用可能である。
【００４６】
また、上述した実施形態では、データ線駆動回路２００を外部基板Ｃに設けたが、フレキシブル基板Ｂ上に設けてもよい。さらに、液晶パネルＡＡの各データ線３の端部にマルチプレクサを設けてもよい。この場合には、液晶パネルＡＡに供給する画像信号の数を減らすことができるので、入力端子２０の数を低減できる。加えて、データ線駆動回路２００を液晶パネルＡＡに形成してもよい。
【００４７】
＜５－３：電子機器＞
次に、上述した液晶表示装置を各種の電子機器に適用される場合について説明する。
＜５－３－１：プロジェクタ＞
まず、この液晶装置をライトバルブとして用いたプロジェクタについて説明する。図７は、プロジェクタの構成例を示す平面図である。
【００４８】
この図に示されるように、プロジェクタ１１００内部には、ハロゲンランプ等の白色光源からなるランプユニット１１０２が設けられている。このランプユニット１１０２から射出された投射光は、ライトガイド１１０４内に配置された４枚のミラー１１０６および２枚のダイクロイックミラー１１０８によってＲＧＢの３原色に分離され、各原色に対応するライトバルブとしての液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇに入射される。
【００４９】
液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇの構成は、上述した液晶パネルＡＡと同等であり、画像信号処理回路（図示省略）から供給されるＲ、Ｇ、Ｂの原色信号でそれぞれ駆動されるものである。そして、これらの液晶パネルによって変調された光は、

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ダイクロイックプリズム１１１２に３方向から入射される。このダイクロイックプリズム１１１２においては、ＲおよびＢの光が９０度に屈折する一方、Ｇの光が直進する。したがって、各色の画像が合成される結果、投射レンズ１１１４を介して、スクリーン等にカラー画像が投写されることとなる。

【００５０】

ここで、各液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇによる表示像について着目すると、液晶パネル１１１０Ｇによる表示像は、液晶パネル１１１０Ｒ、１１１０Ｂによる表示像に対して左右反転することが必要となる。

【００５１】

なお、液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇには、ダイクロイックミラー１１０８によって、Ｒ、Ｇ、Ｂの各原色に対応する光が入射するので、カラーフィルタを設ける必要はない。

【００５２】

＜５－３－２：モバイル型コンピュータ＞

次に、この液晶パネルＡＡを、モバイル型のパーソナルコンピュータに適用した例について説明する。図８は、このパーソナルコンピュータの構成を示す斜視図である。図において、コンピュータ１２００は、キーボード１２０２を備えた本体部１２０４と、液晶表示ユニット１２０６とから構成されている。この液晶表示ユニット１２０６は、先に述べた液晶パネル１００５の背面にバックライトを付加することにより構成されている。

【００５３】

＜５－３－３：携帯電話＞

さらに、この液晶パネルＡＡを、携帯電話に適用した例について説明する。図９は、この携帯電話の構成を示す斜視図である。図において、携帯電話１３００は、複数の操作ボタン１３０２とともに、反射型の液晶パネル１００５を備えるものである。この反射型の液晶パネル１００５にあっては、必要に応じてその前面にフロントライトが設けられる。

【００５４】

なお、図７～図９を参照して説明した電子機器の他にも、液晶テレビや、ビューファインダ型、モニタ直視型のビデオテープレコーダ、カーナビゲーション装置、ページャ、電子手帳、電卓、ワードプロセッサ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが挙げられる。そして、これらの各種電子機器に適用可能なのは言うまでもない。パネル板は、電気光学材料として液晶の替わりに有機ＬＥＤを用いたもの、プラズマを用いたもの、無機エレクトロルミネッセンス素子を用いたものであってもよい。さらに、電子ペーパー等の電気泳動パネルにも適用することができる。

【図面の簡単な説明】

【００５５】

【図１】本発明の実施形態に係る液晶パネルＡＡの構成を示す斜視図である。

【図２】図２は、図１におけるＺ－Ｚ’線の断面図である。

【図３】液晶パネルＡＡの電気的な構成を示すブロック図である。

【図４】実施形態に係る端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。

【図５】液晶表示装置の全体構成を示すブロック図である。

【図６】応用例に係る端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。

【図７】同液晶表示装置を適用した電子機器の一例たるビデオプロジェクタの断面図である。

【図８】同液晶表示装置を適用した電子機器の一例たるパーソナルコンピュータの構成を示す斜視図である。

【図９】同液晶表示装置を適用した電子機器の一例たる携帯電話の構成を示す斜視図である。

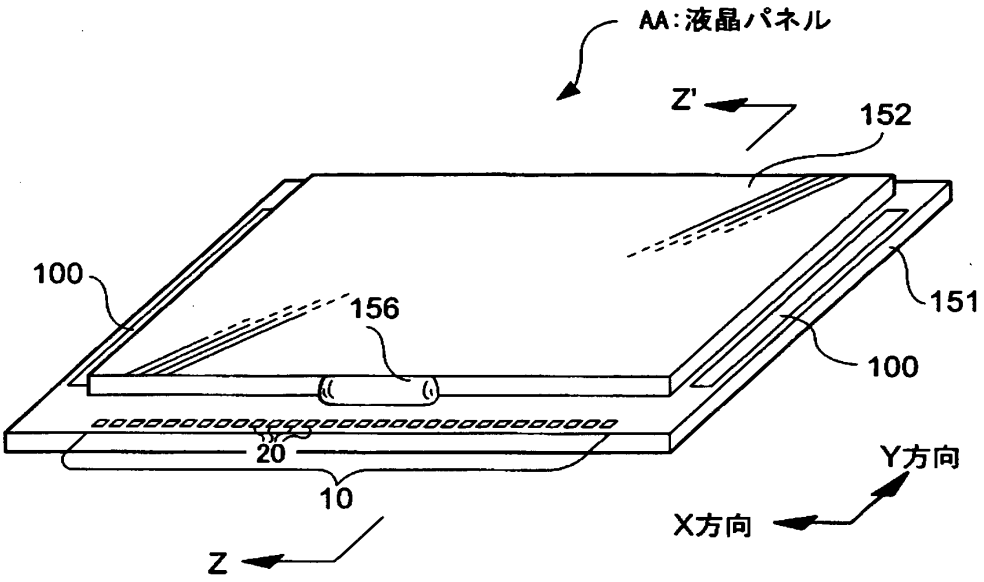
【符号の説明】

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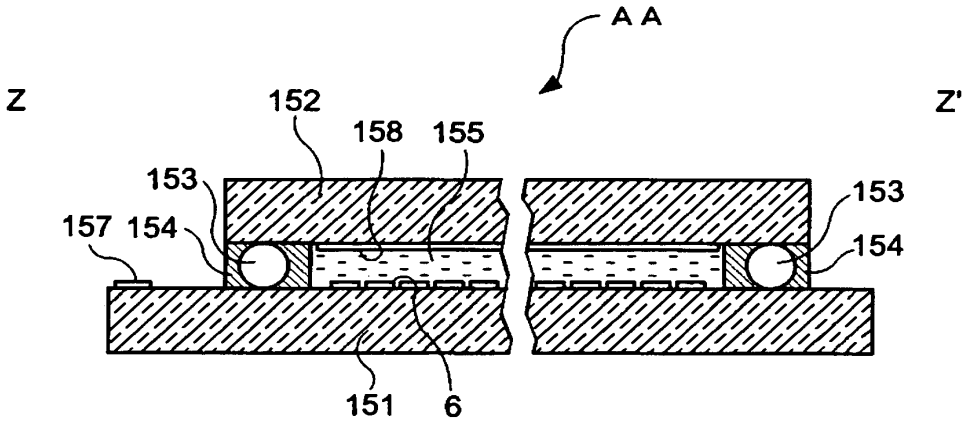
【００５６】
２…走査線、３…データ線、１００…走査線駆動回路、２００…データ線駆動回路、１０…端子群、ＰＴｒｅｆ…基準ピッチ、ＰＴ１、ＰＴ２…第１ピッチ，第２ピッチ、ＡＡ…液晶パネル、Ｂ…フレキシブル基板、Ｃ…外部基板。

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【書類名】図面
【図１】

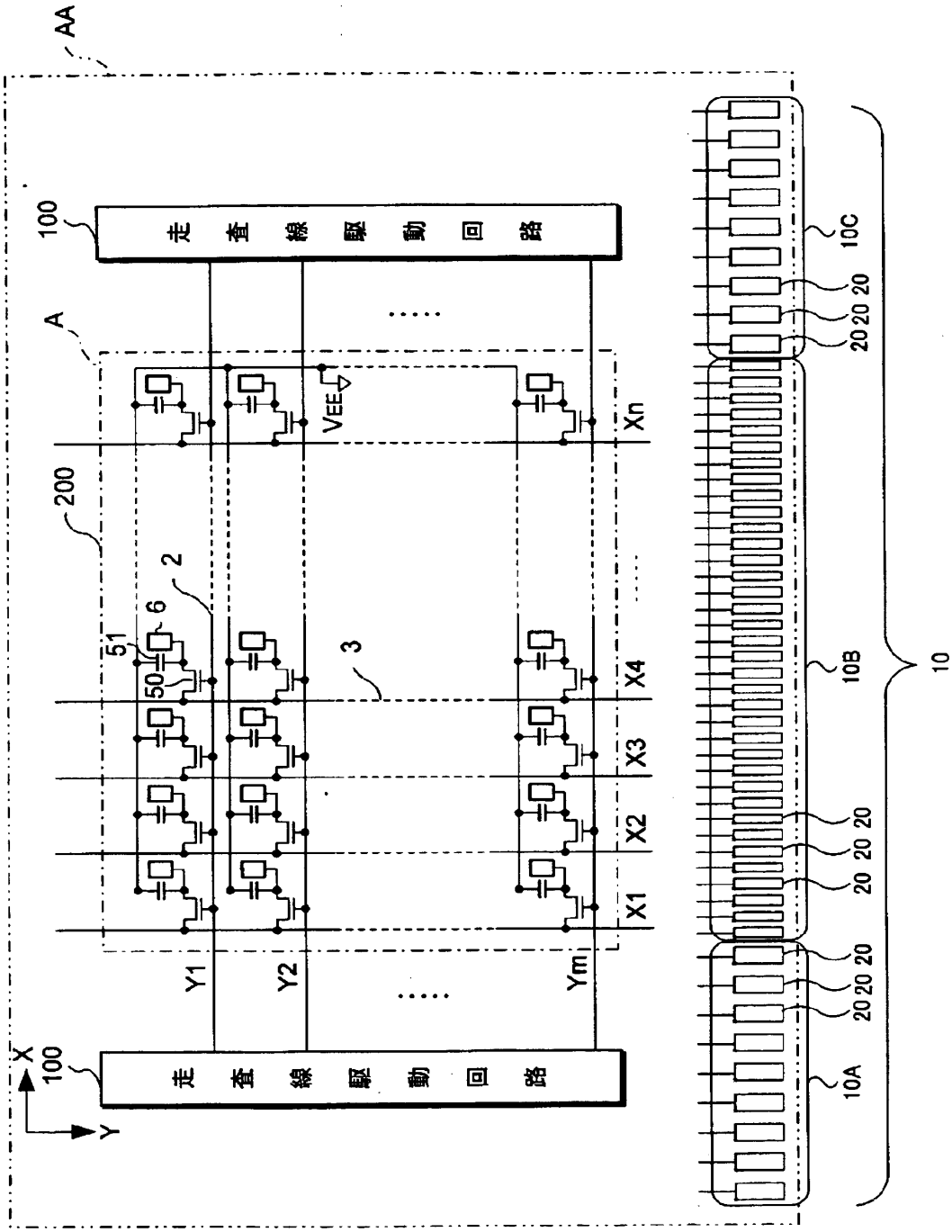


【図２】



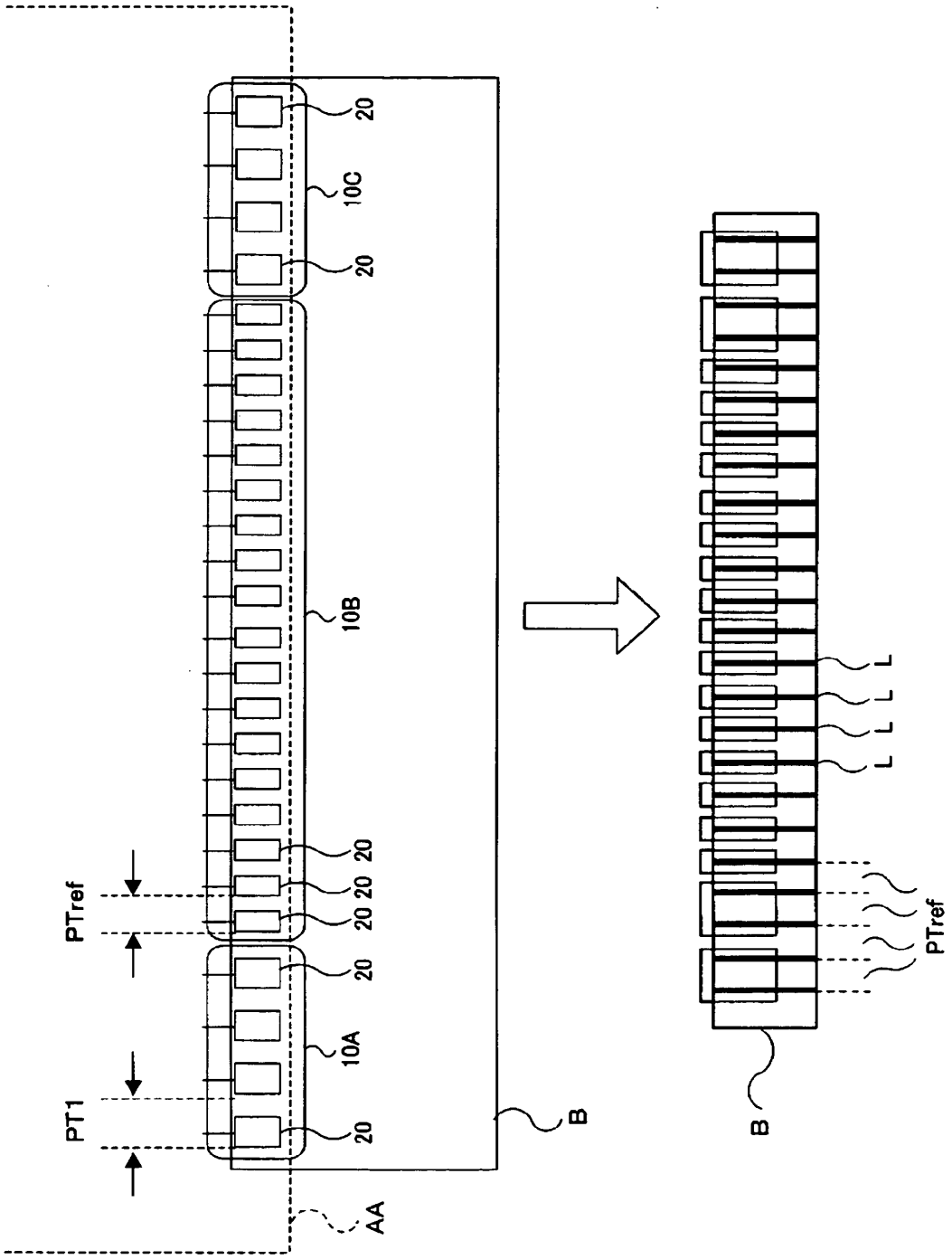
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【図３】



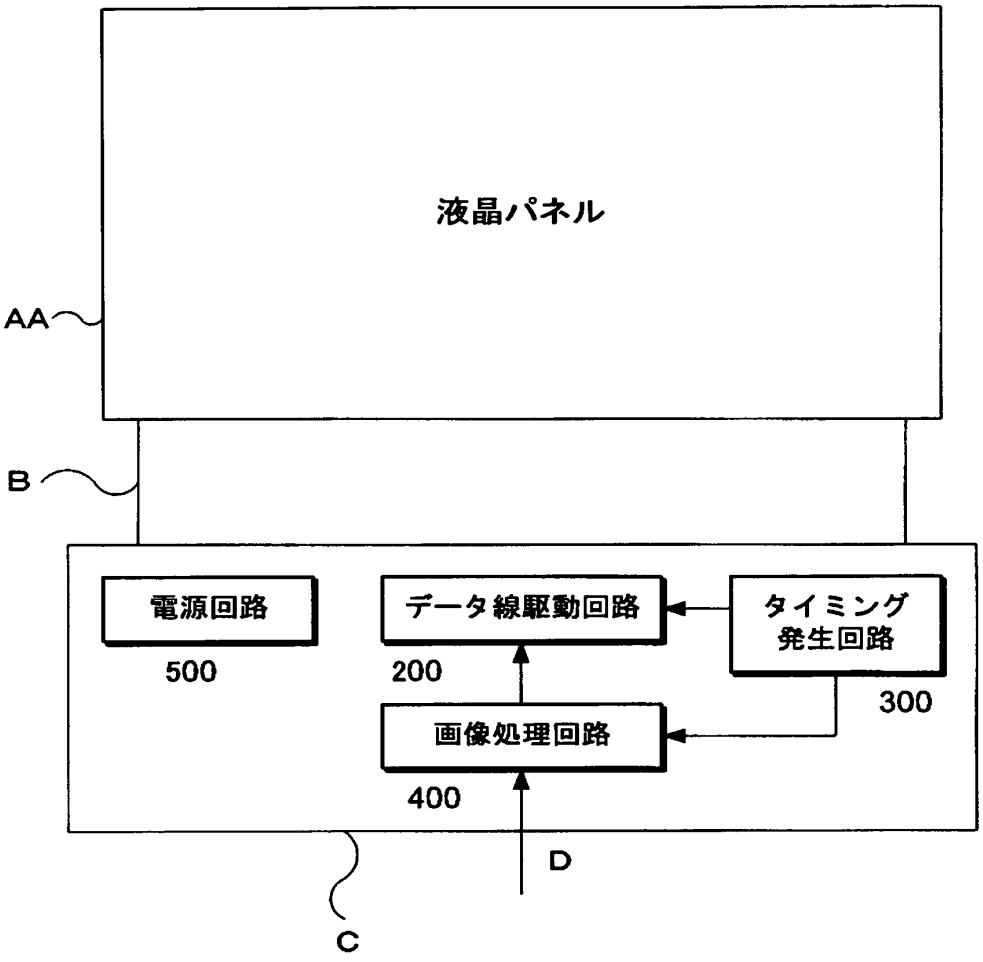
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【図４】



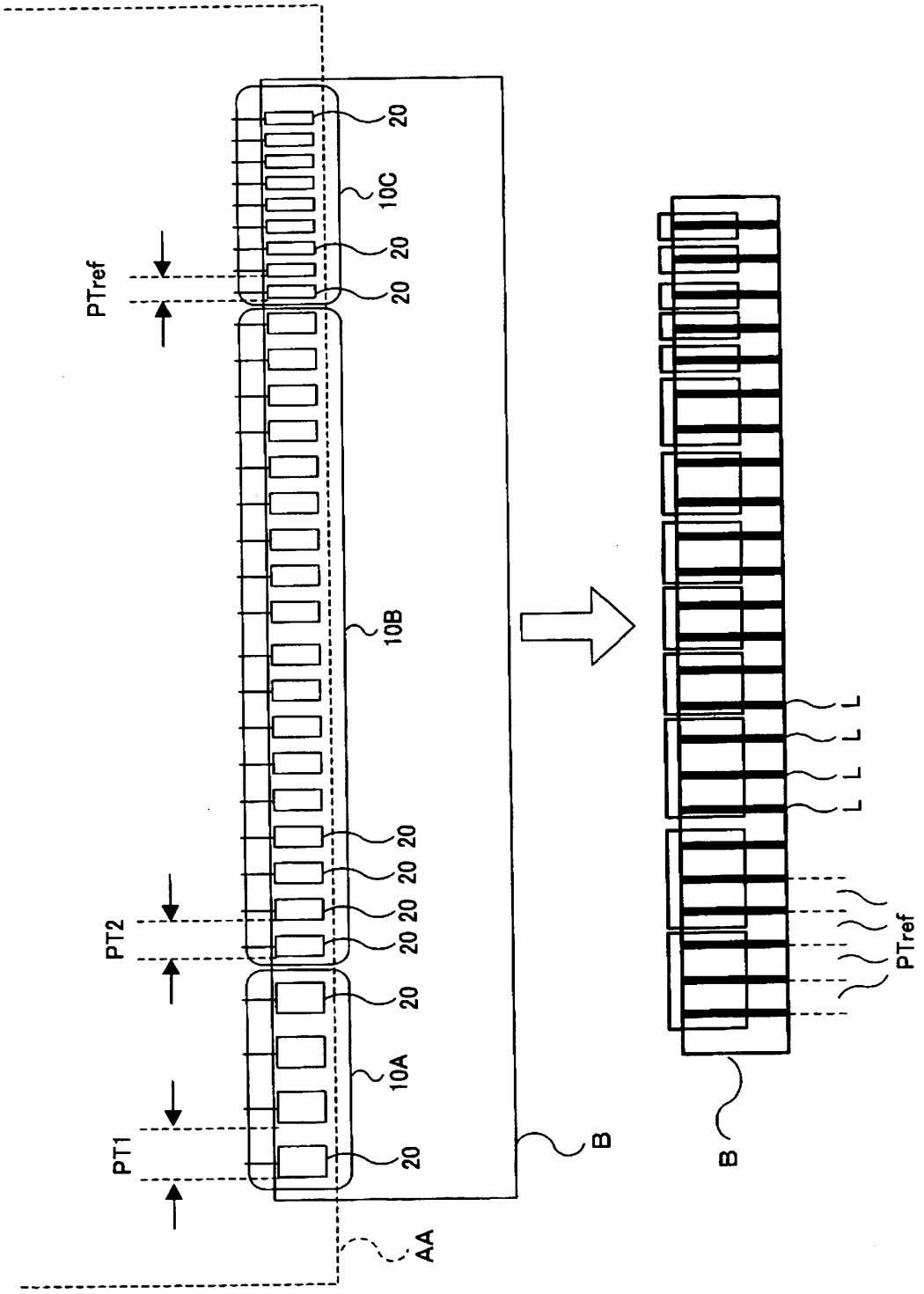
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【図５】



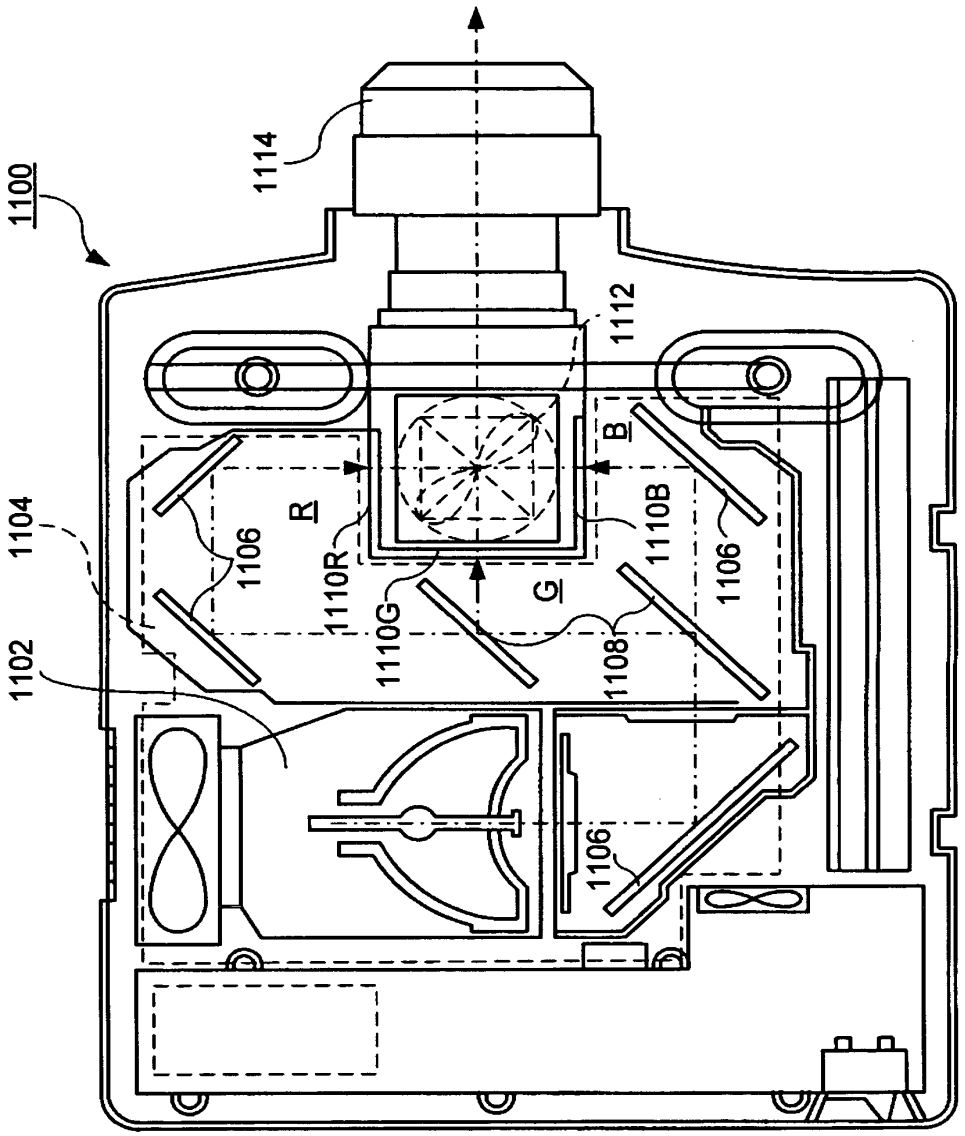
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【図６】



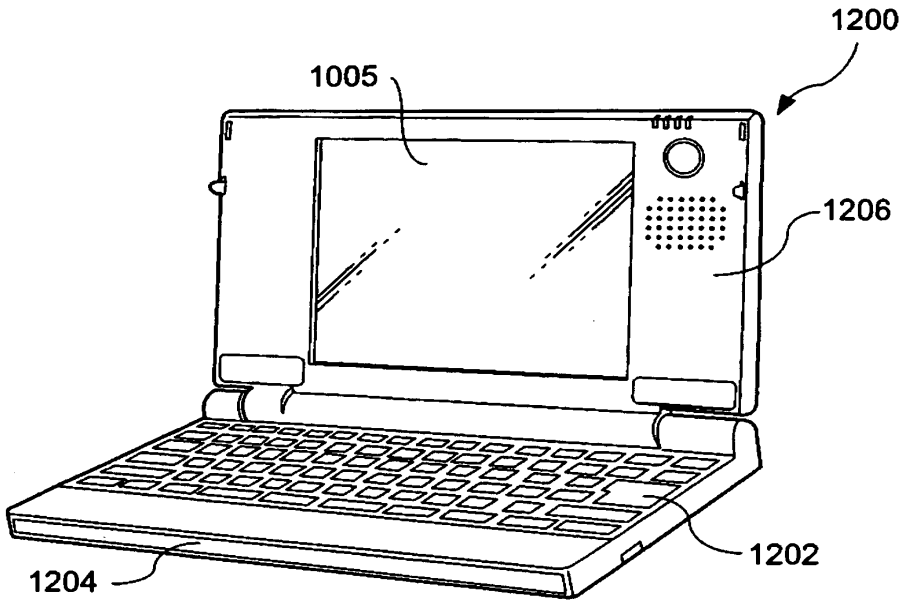
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【図７】

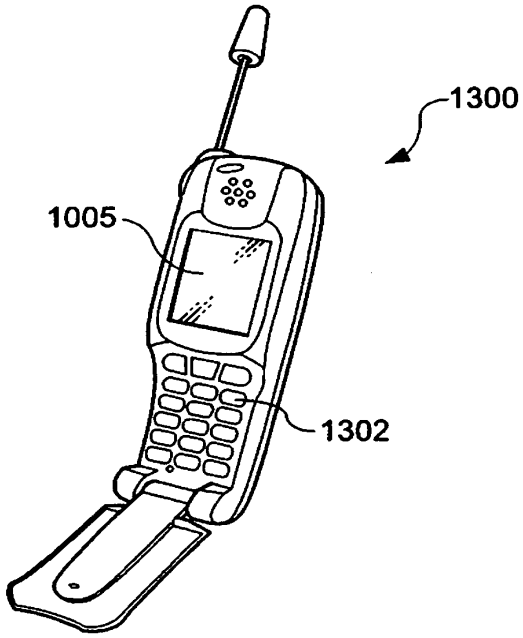


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【図８】



【図９】



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【書類名】要約書
【要約】
【課題】　実装部材を液晶パネルに高い信頼性の下に接続し、信号の伝送に必要な帯域を確保する。
【解決手段】　液晶パネルＡＡは、第１～第３端子群１０Ａ～１０Ｃからなる端子群１０を備える。第１及び第３端子群１０Ａ及び１０Ｃには、駆動信号が供給される一方、第２端子群１０Ｂには画像信号が供給される。駆動信号は画像信号より高い周波数成分を含む。第１及び第３端子群１０Ａ及び１０Ｃの入力端子２０は、第２端子群２０の入力端子２０よりも面積が大きいので、接触抵抗が小さい。従って、駆動信号のなまりを防止できる。
【選択図】　図４

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認定・付加情報

特許出願の番号	特願２００３－２９０６５０
受付番号	５０３０１３２４３３６
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特願２００３－２９０６５０

出　願　人　履　歴　情　報

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日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日
Date of Application: ２００４年　６月３０日

出 願 番 号
Application Number: 特願２００４－１９３５１５

[ST. 10/C]: ［ＪＰ２００４－１９３５１５］

願 人
Applicant(s): セイコーエプソン株式会社

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２００４年　７月２７日

特許庁長官
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出証番号　出証特２００４－３０６６１１５

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【書類名】　特許願
【整理番号】　J010116002
【提出日】　平成16年 6月30日
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【国際特許分類】　G02F 1/13
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　【氏名又は名称】　須澤　修
【先の出願に基づく優先権主張】
　【出願番号】　特願2003-290650
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　【納付金額】　16,000円
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　【物件名】　明細書　1
　【物件名】　図面　1
　【物件名】　要約書　1
　【包括委任状番号】　0109826

出証特２００４－３０６６１１５

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【書類名】特許請求の範囲
【請求項１】
複数のデータ線と、複数の走査線と、前記データ線と前記走査線との交差に対応して設けられた複数の画素と、第１の入力信号が供給される第１の入力端子と、第２の入力信号が供給される第２の入力端子と、前記第１及び第２の入力信号に基づいて前記画素の階調を制御する駆動回路とを備えた電気光学パネルであって、
前記第１の入力信号は前記第２の入力信号に比べて高域周波数成分を含み、且つ前記第１の入力端子は前記第２の入力端子よりも面積が大きいことを特徴とする電気光学パネル。
【請求項２】
前記第１の入力端子は、前記第２の入力端子に比べて入力抵抗値が小さいことを特徴とする請求項１に記載の電気光学パネル。
【請求項３】
前記第１の入力信号は走査線駆動回路に供給される駆動信号であることを特徴とする請求項１又は２に記載の電気光学パネル。
【請求項４】
前記第２の入力信号は画像信号であることを特徴とする請求項１乃至３のいずれか１項に記載の電気光学パネル。
【請求項５】
基板上の基板端に沿って配置された前記第１の入力端子と前記第２の入力端子とは列状に形成されてなり、前記第２の入力端子が前記基板上の中央側に、前記第１の入力端子が前記基板上の外側に設けられていることを特徴とする請求項１乃至４のいずれか１項に記載の電気光学パネル。
【請求項６】
第３の入力端子をさらに有し、前記第３の入力端子は電源が供給される電源端子であり、前記第３の入力端子の面積は、前記第１の入力端子と同等あるいは前記第１の入力端子の面積よりも大きいことを特徴とする請求項１乃至５のいずれか一項に記載の電気光学パネル。
【請求項７】
前記第３の入力端子は、前記第１の入力端子あるいは前記第２の入力端子の隣り合う複数の端子を用いて構成されていることを特徴とする請求項６に記載の電気光学パネル。
【請求項８】
前記電源端子、前記第１の入力端子、前記第２の入力端子をそれぞれ複数含み、
前記複数の電源端子、前記複数の第１の入力端子及び前記複数の第２の入力端子が、基板上に列状に並んで形成されており、
隣り合う第１の入力端子間のピッチは、隣り合う第２の入力端子間のピッチ間の整数倍であることを特徴とする請求項１乃至７のうちいずれか１項に記載した電気光学パネル。
【請求項９】
請求項１乃至８のうちいずれか１項に記載した電気光学パネルと、
前記電源を供給する電源手段と、
前記入力信号を供給する信号生成手段と
を備えたことを特徴とする電気光学装置。
【請求項１０】
請求項９に記載した電気光学パネルと、
前記電源を供給する電源手段と、前記第１の入力信号と前記第２の入力信号を供給する信号生成手段とを備えた外部基板と、
前記外部基板と前記電気光学パネルとを接続するフレキシブル基板とを備え、
前記フレキシブル基板は、異方性導電膜を介して前記複数の電源端子及び前記複数の第１の入力端子と前記複数の第２の入力端子とを接続されることを特徴とする電気光学装置。

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【請求項１１】
前記フレキシブル基板には、基準となる前記第２の丹生慮気宇端子間のピッチに対応して配線が形成されていることを特徴とする請求項１０に記載の電気光学装置。
【請求項１２】
基板上に複数のデータ線と、複数の走査線と、前記データ線と前記走査線との交差に対応して設けられた複数の画素からなる画像表示領域と、前記画素を駆動するための走査線駆動回路と、前記画素にデータ信号を供給するためのデータ線駆動回路と、前記走査線駆動回路と前記データ線駆動回路に信号を供給するための入力端子群を具備し、前記走査線駆動回路は前記基板上に前記基板の一辺に沿って配置され、前記データ線駆動回路は前記基板上に前記一辺に対向しない辺に沿って配置され、前記入力端子群は、前記データ線駆動回路に沿うとともに、前記データ線駆動回路よりも更に基板端側に配置されてなり、
前記入力端子群は、前記走査線駆動回路に駆動信号を供給するための第１の入力端子群と、前記データ線駆動回路に画像信号を供給するための第２の入力端子群とを有し、前記入力端子群のうち中央側に前記第２の入力端子が配置され、前記入力端子群のうち外側に前記第１の入力端子が配置され、前記第１の入力端子は前記第２の入力端子よりも面積が大きいことを特徴とする電気光学パネル。
【請求項１３】
前記データ線駆動回路に駆動信号を供給するための第４の入力端子を含み、前記第４の入力端子の面積は前記第１の入力端子と同等の面積を有するとともに、前記第４の入力端子は前記第１の入力端子と前記第２の入力端子との間に配置されていることを特徴とする請求項１２に記載の電気光学パネル。
【請求項１４】
請求項１乃至１３のうちいずれか１項に記載した電気光学装置を備えたことを特徴とする電子機器。

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【書類名】明細書
【発明の名称】電気光学パネル、電気光学装置及び電子機器
【技術分野】
【０００１】
本発明は、電気光学パネル、電気光学装置及び電子機器に関する。
【背景技術】
【０００２】
表示装置、例えば、電気光学材料として液晶を用いた液晶表示装置は、陰極線管（ＣＲＴ）に代わるディスプレイデバイスとして、各種情報処理機器の表示部や液晶テレビなどに広く用いられている。
【０００３】
ここで、従来の電気光学装置は、例えば、次のように構成されている。すなわち、従来の電気光学装置は、マトリクス状に配列した画素電極と、この画素電極に接続されたＴＦＴ（Thin Film Transistor：薄膜トランジスタ）のようなスイッチング素子などが設けられた素子基板と、画素電極に対向する対向電極が形成された対向基板と、これら両基板との間に充填された電気光学材料たる液晶とを備える。画素は、スイッチング素子、画素電極、電気光学材料及び対向電極によって構成され、マトリクス状に配置される。このような構成において、走査線を介してスイッチング素子に走査信号を印加すると、当該スイッチング素子が導通状態となる。この導通状態の際に、データ線を介して画素電極に、階調に応じた電圧の画像信号を印加すると、当該画素電極および対向電極の間の液晶層に画像信号の電圧に応じた電荷が蓄積される。電荷蓄積後、当該スイッチング素子をオフ状態としても、当該液晶層における電荷の蓄積は、液晶層自身の容量や蓄積容量などによって維持される。このように、各スイッチング素子を駆動させ、蓄積させる電荷量を階調に応じて制御すると、画素毎に液晶の配向状態が変化するので、画素毎に濃度が変化することになる。このため、階調表示することが可能となるのである。
【０００４】
このような電気光学装置は、上述した画素がマトリクス状に配置される電気光学パネルを備える。電気光学パネルには、走査線を駆動する走査線駆動回路、あるいはデータ線を駆動するデータ線駆動回路が形成されることがある。駆動回路を備えた電気光学パネルには、電源、駆動信号、及び画像信号等が供給される。電源等を電気光学パネルに供給する手段として、電気光学パネルに形成された入力端子と接続ケーブルとしてのフレキシブル基板と異方性導電膜を介して接続する技術が知られている（例えば、特許文献１）。
【０００５】
【特許文献１】特許第２８２２５５８号公報
【発明の開示】
【発明が解決しようとする課題】
【０００６】
ところで、入力端子の抵抗は、その面積が大きい程小さくなるため、抵抗値を低減する観点からは入力端子の大きさは大きいことが望ましい。しかしながら、接触抵抗を低減する観点から、入力端子の面積を大きくすると、限られた面積の中に全ての入力端子を配置することができないといった問題があった。
【０００７】
特に、データ線駆動回路を内蔵しないタイプの電気光学パネル、又はマルチプレクサを内蔵するタイプの電気光学パネルにおいては、複数の画像信号を電気光学パネルに取り込む必要があるため、入力端子の数が多くなる。これに伴って、フレキシブル基板等を実装した際に、接続不良等の問題が発生していた。一方、実装エリアを狭くする観点から、入力端子の面積を小さくすると、接触抵抗が増加し、駆動信号が正規のタイミングで入力できないという問題があった。
【０００８】
そこで、本発明は、フレキシブル基板等の実装部品を高い信頼性の下に接続することが

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でき、且つ、信号の伝送に必要な帯域を確保することが可能な電気光学パネル及び電気光学装置、並びにこれらを用いた電子機器を提供することを解決課題とする。

【課題を解決するための手段】

【０００９】

上述した課題を解決するため、本発明に係る電気光学パネルは、複数のデータ線、複数の走査線、及び前記データ線と前記走査線との交差に対応して設けられた複数の画素と、第１の入力信号が供給される第１の入力端子と、第２の入力信号が供給される第２の入力端子と、前記第１及び第２の入力信号に基づいて前記画素の階調を制御する駆動回路とを備えた電気光学パネルであって、前記第１の入力信号は前記第２の入力信号に比べて高域周波数成分を含み、且つ前記第１の入力端子は前記第２の入力端子よりも面積が大きいことを特徴とする。

【００１０】

一般に、端子の入力抵抗は、面積に比例する。従って、面積が大きい入力端子程、入力抵抗値が低くなる。なお、入力抵抗値には、実装部材を接続する場合の接触抵抗値が含まれる。

【００１１】

この発明によれば、入力信号の伝送特性に応じて、入力端子の面積を相違させることができるので、時定数が大きくても信号を十分伝送することが可能な入力端子の面積を小さくする一方、時定数が小さい特性が要求される入力信号が供給される入力端子については、大きな面積を確保することが可能となる。この場合、前記複数の入力信号が供給される前記入力端子の面積は、前記入力信号の周波数特性に応じて設定されることが好ましい。高い周波数成分を含む入力信号については、時定数を小さく設定することにより、当該入力信号の波形をなまらずに取り込むことができ、比較的低い周波数成分から構成される入力信号については、時定数が大きくても問題が無いので、入力端子の面積を小さくすることが可能である。

【００１２】

より具体的には、前記複数の入力信号は、複数の駆動信号と複数の画像信号とを含み、前記複数の駆動信号の周波数特性は、前記複数の画像信号の周波数特性と比較して、高域の周波数成分を含み、前記複数の駆動信号が供給される第１の入力端子の面積は、前記複数の画像信号が供給される第２の入力端子の面積よりも大きいことが好ましい。この場合には、駆動信号の波形をなまらせずに電気光学パネルに取り込むことによって、画像の表示の誤動作を防止できる一方、画像信号の入力端子の面積を小さくすることができるので、限られた面積に多数の入力端子を配置することができる。このように、入力信号の周波数特性に着目して、入力端子の面積を割り当てることによって、限られた面積に中に入力端子を適切に配置することが可能となる。

上述した電気光学パネルは、基板上に前記第１の入力端子、前記第２の入力端子が列状に形成されてなり、前記第２の入力端子が前記基板上の中央側に、前記第１の入力端子が前記基板上の外側に設けることが好ましい。各端子とＡＣＦの接続の際には熱と圧力を加えるため、ＡＣＦは中央側よりも外側のほうがＡＣＦの伸び率が大きくなる傾向がある。そのため面積の広い入力端子を面積の狭い入力端子よりも外側に設ければ、収縮率の異なりにより、接続のわずかなずれが生じても大きな入力端子であれば接続不良を防ぐことができる。

さらに、電源が供給される第３の入力端子である電源端子を含み、前記第３の入力端子の面積は、前記第１の入力端子と同等あるいは前記第１の入力端子の面積よりも大きいことが好ましい。一般に電源端子に入力される電源は抵抗が高いと電圧がトラップして所定の電圧が得られなくなる可能性が高い。そのため、電源はできるだけ抵抗を低くすることが好ましい。そのために、上述したパネルにおいて、電源が供給される電源端子は駆動信号が供給される入力端子と同等もしくはそれ以上の面積とすることが好ましい。このような構成にすることにより、抵抗を下げることができ所定の電圧を供給することが可能となる。また、電源端子は、できるだけ大きいほうが低抵抗化にすることができるため、第１

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の入力端子あるいは第２の入力端子の隣り合う複数の端子を用いて構成することでもよい。このようにすれば、入力端子の面積を増大することができ、抵抗を下げることが可能となる。

【００１３】

上述した電気光学パネルにおいて、電源が供給される電源端子、前記第１の入力端子、前記第２の入力端子をそれぞれ複数含み、前記複数の電源端子、前記複数の第１の入力端子及び前記複数の第２の入力端子が、基板上に列状に並んで形成されており、

隣り合う第１の入力端子間のピッチは、隣り合う第２の入力端子間のピッチの整数倍とすることが好ましい。

この発明によれば、実装部材を複数の電源端子及び複数の入力端子に実装する場合に、実装部材の収縮率の見積もりが容易となり、実装不良を未然に防止することができる。

さらに、本発明は、基板上に複数のデータ線と、複数の走査線と、前記データ線と前記走査線との交差に対応して設けられた複数の画素からなる画像表示領域と、前記画素を駆動するための走査線駆動回路と、前記画素にデータ信号を供給するためのデータ線駆動回路と、前記走査線駆動回路と前記データ線駆動回路に信号を供給するための入力端子群を具備し、前記走査線駆動回路は前記基板上に前記基板の一辺に沿って配置され、前記データ線駆動回路は前記基板上に前記一辺に対向しない辺に沿って配置され、前記入力端子群は、前記データ線駆動回路に沿うとともに、前記データ線駆動回路よりも更に基板端側に配置されてなり、前記入力端子群は、前記走査線駆動回路に駆動信号を供給するための第１の入力端子群と、前記データ線駆動回路に画像信号を供給するための第２の入力端子群とを有し、前記入力端子群のうち中央側に前記第２の入力端子が配置され、前記入力端子群のうち外側に前記第１の入力端子が配置され、前記第１の入力端子は前記第２の入力端子よりも面積が大きいことを特徴とする。

このような構成とすることにより、第２の入力端子からデータ線駆動回路までの配線、第１の入力端子から走査線駆動回路までの配線をそれぞれ交差させないことが可能となり、また配線を引き回さないため、配線抵抗や寄生容量の発生を抑えることができる。また高域周波数成分を有する駆動信号の入力端子をそれよりも低域の周波数成分を有する画像信号の入力端子よりも面積を大きくしてあるため、接触抵抗を小さくすることができ、信号のなまりを防ぐことができる。また、面積の大きな入力端子を面積の小さい入力端子よりも外側に配置している。入力端子とＡＣＦ等との接続において、一般にＡＣＦは中央より外側において伸び率が大きくなる傾向であるが、外側の入力端子の面積を大きくしておけば、たとえ伸び率の違いによりずれが生じても接続不良を防ぐことができる。

さらに、データ線駆動回路に駆動信号を供給するための第４の入力端子を含み、前記第４の入力端子の面積は前記第１の入力端子と同等の面積を有するとともに、前記第４の入力端子は前記第１の入力端子と前記第２の入力端子との間に配置されていることが好ましい。

このように、大きな面積の端子をできるだけまとめて基板の周辺側に設けることにより、実装不良を防ぐことができる。

【００１４】

次に、本発明に係る電気光学装置は、上述した電気光学パネルと、前記電源を供給する電源手段と、前記第１の入力信号及び第２の入力信号を供給する信号生成手段とを備えたことを特徴とする。この電気光学装置は上述した電気光学パネルを備えるので、フレキシブル基板等の実装部品を高い信頼性の下に接続することができ、且つ、信号の伝送に必要な帯域を確保することが可能となる。

【００１５】

また、本発明に係る電気光学装置は、前記電源を供給する電源手段と、前記入力信号を供給する信号生成手段とを備えた外部基板と、前記外部基板と前記電気光学パネルとを接続するフレキシブル基板とを備え、前記フレキシブル基板は、異方性導電膜を介して前記複数の電源端子及び前記複数の第１入力端子及び第２の入力端子と接続されることが好ましい。

出証特２００４－３０６６１１５

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【００１６】
ここで、前記フレキシブル基板には、基準となる前記第２の入力端子間のピッチの間隔に対応して配線が形成されていることが好ましい。幅の異なる端子が混在する端子群に対して各配線を確実に接続することができる。そして、面積の広い端子に対しては、複数の配線が割り当てられるから、接触抵抗と配線抵抗を低減することができる。　.
【００１７】
次に、本発明に係る電子機器は上述した電気光学装置を備える。このような電子機器としては、液晶プロジェクタ、パーソナルコンピュータ、携帯電話、電子カメラ、ＰＤＡ等が該当する。
【００１８】
このように本発明によれば、フレキシブル基板等の実装部品を高い信頼性の下に接続することができ、且つ、信号の伝送に必要な帯域を確保することが可能な電気光学パネル及び電気光学装置、並びにこれらを用いた電子機器を提供することができる。
【発明を実施するための最良の形態】
【００１９】
以下、図面を参照して、本発明に係わる実施形態を説明する。なお、本実施形態では、電気光学材料として液晶を用いた液晶パネルを電気光学パネルの一例とし、液晶パネルを用いた液晶表示装置を電気光学装置の一例として説明するが、本発明はこれに限定されるものではなく、有機発光ダイオード素子を備える有機ＥＬパネル等も電気光学パネルに含まれることは勿論である。
【００２０】
＜１．液晶パネルの機械的構成＞
まず、第１実施形態に係わる液晶パネルＡＡの機械的構成について図１及び図２を参照して説明する。ここで、図１は、液晶パネルＡＡの構成を示す斜視図であり、図２は、図１におけるＺ－Ｚ’線断面図である。
【００２１】
これらの図に示されるように、液晶パネルＡＡは、画素電極６等が形成されたガラスや半導体等の素子基板１５１と、共通電極１５８等が形成されたガラス等の透明な対向基板１５２とを、スペーサ１５３が混入されたシール材１５４によって一定の間隙を保って、互いに電極形成面が対向するように貼り合わせるとともに、この間隙に電気光学材料としての液晶１５５を封入した構造となっている。なお、シール材１５４は、対向基板１５２の基板周辺に沿って形成されるが、液晶１５５を封入するために一部が開口している。このため、液晶１５５の封入後に、その開口部分が封止材１５６によって封止されている。
【００２２】
ここで、素子基板１５１の対向面であって、シール材１５４の外側一辺においては、端子群１０が形成されている。端子群１０は、複数の入力端子２０から構成される。複数の入力端子２０の一部には、画像信号が供給され、Ｙ方向に延在するデータ線３を駆動する構成となっている。さらに、この一辺には端子群１０が形成されている。また、この一辺に隣接する一辺には、走査線駆動回路１００が形成されて、Ｘ方向に延在する走査線２をそれぞれ両側から駆動する構成となっている。
【００２３】
端子群１０は、異方性導電フィルムを介して電気的および機械的に実装部材と接続される。この例の実装部材は、接続ケーブルとしてのフレキシブル基板と外部基板とを含む。
対向基板１５２の共通電極１５８は、素子基板１５１との貼合部分における４隅のうち、少なくとも１箇所において設けられた導通材によって、素子基板１５１との電気的導通が図られている。ほかに、対向基板１５２には、液晶パネルＡＡの用途に応じて、例えば、第１に、ストライプ状や、モザイク状、トライアングル状等に配列したカラーフィルタが設けられ、第２に、例えば、クロムやニッケルなどの金属材料や、カーボンやチタンなどをフォトレジストに分散した樹脂ブラックなどのブラックマトリクスが設けられ、第３に、液晶パネルＡＡに光を照射するバックライトが設けられる。特に色光変調の用途の場

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合には、カラーフィルタは形成されずにブラックマトリクスが対向基板１５２に設けられる。

【００２４】

くわえて、素子基板１５１および対向基板１５２の対向面には、それぞれ所定の方向にラビング処理された配向膜などが設けられる一方、その各背面側には配向方向に応じた偏光板（図示省略）がそれぞれ設けられる。ただし、液晶１５５として、高分子中に微小粒として分散させた高分子分散型液晶を用いれば、前述の配向膜、偏光板等が不要となる結果、光利用効率が高まるので、高輝度化や低消費電力化などの点において有利である。

【００２５】

なお、走査線駆動回路１００等の周辺回路の一部または全部を、素子基板１５１に形成する替わりに、例えば、ＴＡＢ（Tape Automated Bonding）技術を用いてフィルムに実装された駆動用ＩＣチップを、素子基板１５１の所定位置に設けられる異方性導電フィルムを介して電気的および機械的に接続する構成としても良いし、駆動用ＩＣチップ自体を、ＣＯＧ（Chip On Grass）技術を用いて、素子基板１５１の所定位置に異方性導電フィルムを介して電気的および機械的に接続する構成としても良い。

【００２６】

＜２．液晶パネルの電気的構成＞

図３は、液晶パネルの電気的構成を示すブロック図である。この図に示すように液晶パネルＡＡは、走査線駆動回路１００、画像表示領域Ａ、及び端子群１０を備える。端子群１０は、第１端子群１０Ａ、第２端子群１０Ｂ、第３端子群１０Ｃを備える。第１端子群１０Ａ及び第３端子群１０Ｃには、走査線駆動回路１００を駆動するため各駆動信号及び電源が供給される。即ち、第１端子群１０Ａ及び第３端子群１０Ｃを構成する一部の入力端子２０は、電源（第３の入力信号）が供給される電源端子として機能してもよい。一方、第２端子群１０Ｂには画像信号が供給される。電源端子は、抵抗が高いと電圧トラップにより所定の電圧が得られなくなくなるため、できるだけ抵抗を低くしておいたほうがよい。そのため、電源端子は第１端子群と同等の面積あるいはそれ以上の面積を有する端子とすることが好ましい。さらに、電源端子は、第１の端子群あるいは第２の端子群の隣り合う２つの端子の両方をまたがって２つ以上により構成すれば抵抗をさらに抑えることができる。また電源端子は基板上の駆動信号の入力端子よりもさらに外側に、つまり基板端に沿って一列に配列された入力端子群は、中央側に画像信号の入力端子を設け、外側に向かって駆動回路の入力端子、そして電源端子の順に設けることが好ましい。

【００２７】

この例において、液晶パネルＡＡには、電源の他に入力信号として駆動信号（第１の入力信号）と画像信号（第２の入力信号）とが供給される。このうち、駆動信号は、Ｙ転送開始パルスＤＹ、Ｙクロック信号ＹＣＫ及び反転Ｙクロック信号ＹＣＫＢ等を含む。これらの駆動信号の周波数特性は、画像信号の周波数特性と比較して、高域の周波数成分を含む。従って、走査線駆動回路１００を正常に動作させるためには、駆動信号がなまらないように伝送する必要がある。駆動信号は、フレキシブル基板を介して伝送されるが、この伝送路には、分布容量や分布抵抗が存在し、等価的にローパスフィルタが構成される。従って、駆動信号の信号波形がなまらないように伝送するためには、等価的なローパスフィルタの時定数を下げる必要がある。分布抵抗のうち、入力端子２０で発生する接触抵抗の割合は、大きく無視することはできない。接触抵抗は入力端子２０の面積が大きくなる程、小さくなる。そこで、本実施形態においては、画像信号が供給される入力端子と比較して駆動信号が供給される入力端子の面積を大きくしている。具体的には、第１及び第３端子群１０Ａ及び１０Ｃを構成する入力端子２０は、第２端子群１０Ｂを構成する入力端子２０よりも面積が大きい。

【００２８】

換言すれば、入力信号が供給される複数の入力端子２０は、入力抵抗値の異なる複数種類の入力端子２０を含み、各入力信号の伝送するために必要とされる伝送特性に応じて、各入力信号が供給される入力端子２０の種類が定められている。これにより、比較的高い

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周波数成分を有する駆動信号を正確に伝送するとともに、比較的低い周波数成分を有する画像信号が供給される第２端子群１０Ｂを構成する入力端子２０の面積を第１端子群１０Ａ及び第３端子群１０Ｃを構成する入力端子２０の面積よりも小さくすることにより、限られた面積の中に必要とされる数の入力端子２０を配置することが可能となる。

【００２９】

次に、走査線駆動回路１００は、シフトレジスタ等を備える。走査線駆動回路１００には、Ｙ転送開始パルスＤＹ、Ｙクロック信号ＹＣＫ及び反転Ｙクロック信号ＹＣＫＢ、高電位電源ＶＨＨ及び低電位電源ＶＳＳが供給される。図３において、左側の走査線駆動回路１００には第１端子群１０Ａから駆動信号及び電源が供給される一方、右側の走査線駆動回路１００には第３端子群１０Ｃから駆動信号及び電源が供給される。

【００３０】

走査線駆動回路１００は、シフトレジスタを用いてＹクロック信号ＹＣＫおよび反転Ｙクロック信号ＹＣＫＢに同期して、Ｙ転送開始パルスＤＹを順次転送し、さらにレベル変換を行って走査信号Ｙ１、Ｙ２、…、Ｙｍを生成し、各走査線２に出力する。

【００３１】

次に、画像表示領域Ａには、図３に示されるように、ｍ（ｍは２以上の自然数）本の走査線２が、Ｘ方向に沿って平行に配列して形成される一方、ｎ（ｎは２以上の自然数）本のデータ線３が、Ｙ方向に沿って平行に配列して形成されている。そして、走査線２とデータ線３との交差付近においては、ＴＦＴ５０のゲートが走査線２に接続される一方、ＴＦＴ５０のソースがデータ線３に接続されるとともに、ＴＦＴ５０のドレインが画素電極６に接続される。そして、各画素は、画素電極６と、対向基板に形成される対向電極（後述する）と、これら両電極間に挟持された液晶とによって構成される。この結果、走査線２とデータ線３との各交差に対応して、画素はマトリクス状に配列されることとなる。

【００３２】

また、ＴＦＴ５０のゲートが接続される各走査線２には、走査信号Ｙ１、Ｙ２、…、Ｙｍが、パルス的に線順次で印加されるようになっている。このため、ある走査線２に走査信号が供給されると、当該走査線に接続されるＴＦＴ５０がオンするので、データ線３から所定のタイミングで供給されるデータ線信号Ｘ１、Ｘ２、…、Ｘｎ（画像信号）は、対応する画素に順番に書き込まれた後、所定の期間保持されることとなる。

【００３３】

各画素に印加される電位レベルに応じて液晶分子の配向や秩序が変化するので、光変調による階調表示が可能となる。例えば、液晶を通過する光量は、ノーマリーホワイトモードであれば、印加電位が高くなるにつれて制限される一方、ノーマリーブラックモードであれば、印加電位が高くなるにつれて緩和されるので、液晶表示装置全体では、画像信号に応じたコントラストを持つ光が各画素毎に出射される。このため、所定の表示が可能となる。

【００３４】

＜３．端子群１０とフレキシブル基板Ｂとの関係＞

次に、端子群１０とフレキシブル基板Ｂとの詳細な構成について説明する。図４は、端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。上述したように端子群１０は、面積の異なる２種類の入力端子２０から構成されている。この例では、第２端子群１０Ｂを構成する入力端子２０の面積が最も小さく、また、入力端子２０間のピッチが最小となる。本実施形態においては、面積の異なる複数種類の入力端子２０（電源端子を含む）のうち、面積が最小の端子間のピッチを基準ピッチＰＴｒｅｆと称する。この例では、第２端子群１０Ｂを構成する入力端子２０の面積が最小であるから、第２端子群１０Ｂを構成する入力端子２０の間隔が基準ピッチＰＴｒｅｆとなる。

【００３５】

一方、第１端子群１０Ａ及び第３端子群１０Ｃを構成する入力端子２０のピッチは等しい。このピッチを第１ピッチＰＴ１と称する。さらに、第１ピッチＰＴ１は基準ピッチＰＴｒｅｆの整数倍となるように設定することが好ましい。フレキシブル基板Ｂと端子群１

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０の接続は異方性導電膜（ＡＣＦ：anisotropic conductive film）を介して行われる。
この際、熱と圧力とを加えるため、フレキシブル基板Ｂが収縮する。上述したように整数倍の関係に設定すると、フレキシブル基板Ｂ等の実装部材を端子群１０に実装する場合に、実装部品の収縮率の見積もりが容易となり、実装不良を未然に防止することができる。また、ＡＣＦの接続の際には熱と圧力を加えるため、ＡＣＦは中央よりも外側のほうがＡＣＦの伸び率が大きくなる傾向がある。そのため面積の広い入力端子を面積の狭い入力端子よりも外側に設ければ、たとえ収縮率の異なりによる接続のわずかなずれが生じても大きな入力端子であれば接続不良を防ぐことができる。よって、基板の中央側にピッチが狭くて面積の狭い入力端子、その外側にピッチの広くて面積の大きな入力端子を設けることがよい。

【００３６】

また、フレキシブル基板Ｂには、配線Ｌが基準ピッチＰＴｒｅｆの間隔で形成されている。これによって、幅の異なる入力端子２０が混在する端子群１０に対して各配線Ｌを確実に接続することができる。そして、面積の広い入力端子２０に対しては、２本の配線Ｌが割り当てられるから、接触抵抗と配線抵抗を低減することができる。

【００３７】

＜４．液晶表示装置の全体構成＞

図５に液晶表示装置の全体構成を示す。外部基板Ｃは、フレキシブル基板Ｃを介して液晶パネルＡＡに接続されている。外部基板Ｃは、データ線駆動回路２００、タイミング発生回路３００、画像処理回路４００、及び電源回路５００を備える。この液晶表示装置に供給される入力画像データＤは、例えば、３ビットパラレルの形式である。タイミング発生回路３００は、入力画像データＤに同期してＹクロック信号ＹＣＫ、反転Ｙクロック信号ＹＣＫＢ、Ｘクロック信号ＸＣＫ、反転Ｘクロック信号ＸＣＫＢ、Ｙ転送開始パルスＤＹおよびＸ転送開始パルスＤＸを生成する。また、タイミング発生回路３００は、画像処理回路４００を制御する各種のタイミング信号を生成し、これを出力する。

【００３８】

Ｙクロック信号ＹＣＫは、走査線２を選択する期間を特定し、反転Ｙクロック信号ＹＣＫＢはＹクロック信号ＹＣＫの論理レベルを反転したものである。Ｘクロック信号ＸＣＫは、データ線３を選択する期間を特定し、反転Ｘクロック信号ＸＣＫＢはＸクロック信号ＸＣＫの論理レベルを反転したものである。

【００３９】

画像処理回路４００は、入力画像データＤに、液晶パネルＡＡの光透過特性を考慮したガンマ補正等を施した後、画像データをデータ線駆動回路２００に供給する。データ線駆動回路２００は、Ｘクロック信号ＸＣＫ及び反転Ｘクロック信号ＸＣＫＢに同期してＸ転送開始パルスＤＸを順次転送してサンプリング信号を生成し、生成したサンプリング信号を用いて画像データをサンプリングして、線順次の画像データを生成し、さらにＤ／Ａ変換を施して、線順次の画像信号を生成する。この画像信号はフレキシブル基板Ｃを介して液晶パネルＡＡに供給される。

【００４０】

電源回路５００は、走査線駆動回路１００に高電位電源ＶＤＤ及び低電位電源ＶＳＳを供給する他、タイミング発生回路３００及び画像処理回路４００に所定の電源を供給する。以上の構成において、データ線駆動回路２００、タイミング発生回路３００、及び画像処理回路４００は、液晶パネルＡＡに入力信号を供給する信号生成手段として機能する。

【００４１】

＜５．応用例＞

＜５－１：端子群１０とフレキシブル基板Ｂとの関係＞

上述した実施形態においては、入力端子２０として面積が異なる２種類の端子を用いたが本発明はこれに限定されるものではなく、３種類以上の入力端子２０を備えるものであってもよい。図６は、応用例における端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。この例においては、第３端子群１０Ｃを構成する入力端子２０の

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面積が最小である。このため、第３端子群１０Ｃを構成する入力端子２０の間隔が基準ピッチＰＴｒｅｆとなる。第２端子群１０Ｂの入力端子２０は第２ピッチＰＴ２の間隔で形成されており、第１端子群１０Ａの入力端子２０は第１ピッチＰＴ１の間隔で形成されている。

【００４２】

この場合、ＰＴｒｅｆ、ＰＴ１、ＰＴ２には、２ＰＴｒｅｆ＝ＰＴ２、３ＰＴｒｅｆ＝ＰＴ１の関係がある。即ち、複数の電源端子及び複数種類の入力端子のうち、面積が最小の端子間のピッチを基準ピッチＰＴｒｅｆとしたとき、他の種類における入力端子間のピッチＰＴ１、ＰＴ２又は電源端子間のピッチＰＴ１、ＰＴ２は、基準ピッチＰＴｒｅｆの整数倍となる。

【００４３】

また、フレキシブル基板Ｂには、配線Ｌが基準ピッチＰＴｒｅｆの間隔で形成されている。これによって、幅の異なる入力端子２０が混在する端子群１０に対して各配線Ｌを確実に接続することができる。そして、面積の広い入力端子２０に対しては、２本又は３本の配線Ｌが割り当てられるから、接触抵抗と配線抵抗を低減することができる。

【００４４】

＜５－２：電気光学装置の第２実施形態＞

本発明の第２実施実施形態について図１０を用いて説明する。図１０は第２実施形態のブロック図であり、レイアウトを示す図である。第２実施形態は、上述の第１実施形態とほとんど同様な構成を有している。異なる点は、マルチプレクサ等のデータ線ドライバ回路の配置が含まれている点である。この構成では、基板の中央部に画像表示領域Ａを配置し、基板上の周辺の対向する２辺に沿って走査線駆動回路１００を配置し、基板の周辺であって走査線駆動回路１００が配置されていない１辺に沿ってデータ線駆動回路２００が配置され、さらにデータ線駆動回路２００より基板端側に各入力端子（駆動信号と画像信号のための入力端子）が配置されている。この実施形態では、入力端子１０Ａを介して走査線駆動回路１００に駆動信号１０Ａが入力され、入力端子１０Ｂを介してマルチプレクサ等のデータ線駆動回路２００に画像信号１０Ｂが入力される。入力端子１０Ａは入力端子１０Ｂに比べて面積が大きく、さらに基板端の中央側に入力端子１０Ｂを配置し、外側に入力端子１０Ａを配置されている。また、マルチプレクサの駆動信号（第４の入力信号）が入力される入力端子は、走査線駆動回路の駆動信号が入力される端子と同等の面積を有するように構成されている。さらに、マルチプレクサの駆動信号が入力される端子は画像信号が入力される端子よりも周辺側に配置し、特に走査線駆動回路の駆動信号が入力される端子と画像信号が入力される端子の間に配置すればよい。このような構成により、面積の大きな入力端子と面積の小さい入力端子とをそれぞれまとめて配置するため、ＡＣＦ等の接続不良を防ぐことができる。またこのような構成とすることにより、入力端子１０Ｂからデータ線駆動回路２００までの配線と、入力端子１０Ａから走査線駆動回路１００までの配線とをそれぞれ交差させないことが可能となる。また配線を引き回さないため、配線抵抗や寄生容量の発生を抑えることができる。

また、上述した実施の形態にあっては、画素のスイッチング素子を、ＴＦＴで代表される３端子素子として説明したが、ダイオード等の２端子素子で構成しても良い。ただし、画素のスイッチング素子として２端子素子を用いる場合には、走査線２を一方の基板に形成し、データ線３を他方の基板に形成するとともに、２端子素子を、走査線２またはデータ線３のいずれか一方と、画素電極との間に形成する必要がある。この場合、画素は、走査線２とデータ線３との間に直列接続された二端子素子と、液晶とから構成されることとなる。

【００４５】

また、本発明は、アクティブマトリクス型液晶表示装置として説明したが、これに限られず、ＳＴＮ（Super Twisted Nematic）液晶などを用いたパッシブ型にも適用可能である。さらに、電気光学材料としては、液晶のほかに、エレクトロルミネッセンス素子などを用いて、その電気光学効果により表示を行う表示装置にも適用可能である。すなわち、

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本発明は、上述した液晶装置と類似の構成を有するすべての電気光学装置に適用可能である。

【００４６】

また、上述した実施形態では、データ線駆動回路２００を外部基板Ｃに設けたが、フレキシブル基板Ｂ上に設けてもよい。さらに、液晶パネルＡＡの各データ線３の端部にマルチプレクサを設けてもよい。この場合には、液晶パネルＡＡに供給する画像信号の数を減らすことができるので、入力端子２０の数を低減できる。加えて、データ線駆動回路２００を液晶パネルＡＡに形成してもよい。

【００４７】

＜５－３：電子機器＞

次に、上述した液晶表示装置を各種の電子機器に適用される場合について説明する。

＜５－３－１：プロジェクタ＞

まず、この液晶装置をライトバルブとして用いたプロジェクタについて説明する。図７は、プロジェクタの構成例を示す平面図である。

【００４８】

この図に示されるように、プロジェクタ１１００内部には、ハロゲンランプ等の白色光源からなるランプユニット１１０２が設けられている。このランプユニット１１０２から射出された投射光は、ライトガイド１１０４内に配置された４枚のミラー１１０６および２枚のダイクロイックミラー１１０８によってＲＧＢの３原色に分離され、各原色に対応するライトバルブとしての液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇに入射される。

【００４９】

液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇの構成は、上述した液晶パネルＡＡと同等であり、画像信号処理回路（図示省略）から供給されるＲ、Ｇ、Ｂの原色信号でそれぞれ駆動されるものである。そして、これらの液晶パネルによって変調された光は、ダイクロイックプリズム１１１２に３方向から入射される。このダイクロイックプリズム１１１２においては、ＲおよびＢの光が９０度に屈折する一方、Ｇの光が直進する。したがって、各色の画像が合成される結果、投射レンズ１１１４を介して、スクリーン等にカラー画像が投写されることとなる。

【００５０】

ここで、各液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇによる表示像について着目すると、液晶パネル１１１０Ｇによる表示像は、液晶パネル１１１０Ｒ、１１１０Ｂによる表示像に対して左右反転することが必要となる。

【００５１】

なお、液晶パネル１１１０Ｒ、１１１０Ｂおよび１１１０Ｇには、ダイクロイックミラー１１０８によって、Ｒ、Ｇ、Ｂの各原色に対応する光が入射するので、カラーフィルタを設ける必要はない。

【００５２】

＜５－３－２：モバイル型コンピュータ＞

次に、この液晶パネルＡＡを、モバイル型のパーソナルコンピュータに適用した例について説明する。図８は、このパーソナルコンピュータの構成を示す斜視図である。図において、コンピュータ１２００は、キーボード１２０２を備えた本体部１２０４と、液晶表示ユニット１２０６とから構成されている。この液晶表示ユニット１２０６は、先に述べた液晶パネル１００５の背面にバックライトを付加することにより構成されている。

【００５３】

＜５－３－３：携帯電話＞

さらに、この液晶パネルＡＡを、携帯電話に適用した例について説明する。図９は、この携帯電話の構成を示す斜視図である。図において、携帯電話１３００は、複数の操作ボタン１３０２とともに、反射型の液晶パネル１００５を備えるものである。この反射型の液晶パネル１００５にあっては、必要に応じてその前面にフロントライトが設けられる。

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【００５４】
なお、図７～図９を参照して説明した電子機器の他にも、液晶テレビや、ビューファインダ型、モニタ直視型のビデオテープレコーダ、カーナビゲーション装置、ページャ、電子手帳、電卓、ワードプロセッサ、ワークステーション、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが挙げられる。そして、これらの各種電子機器に適用可能なのは言うまでもない。パネル板は、電気光学材料として液晶の替わりに有機ＬＥＤを用いたもの、プラズマを用いたもの、無機エレクトロルミネッセンス素子を用いたものであってもよい。さらに、電子ペーパー等の電気泳動パネルにも適用することができる。

【図面の簡単な説明】

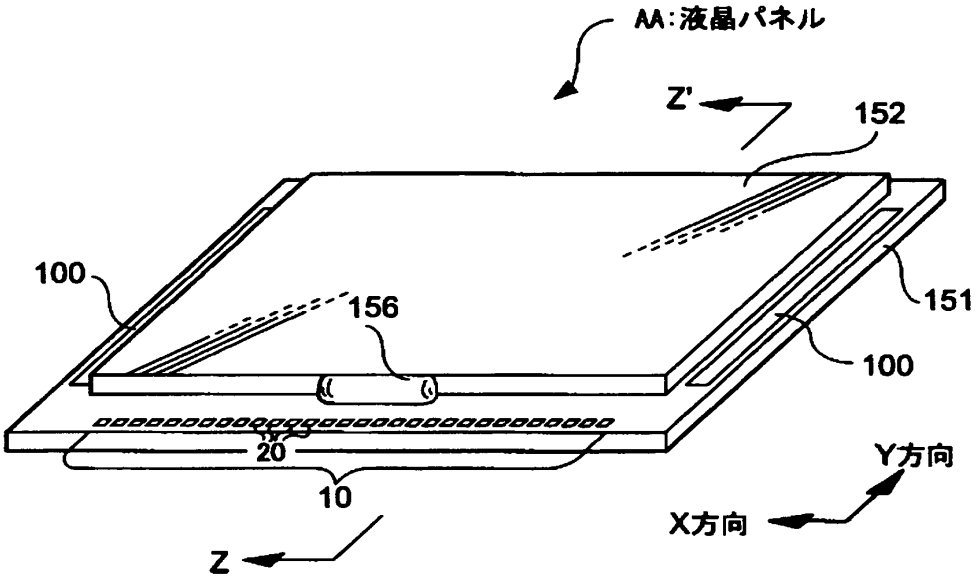
【００５５】
【図１】本発明の実施形態に係る液晶パネルＡＡの構成を示す斜視図である。
【図２】図２は、図１におけるＺ－Ｚ’線の断面図である。
【図３】第１実施形態の液晶パネルＡＡの電気的な構成を示すブロック図である。
【図４】実施形態に係る端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。
【図５】液晶表示装置の全体構成を示すブロック図である。
【図６】応用例に係る端子群１０とフレキシブル基板Ｂとの接続に係る構成を示す平面図である。
【図７】同液晶表示装置を適用した電子機器の一例たるビデオプロジェクタの断面図である。
【図８】同液晶表示装置を適用した電子機器の一例たるパーソナルコンピュータの構成を示す斜視図である。
【図９】同液晶表示装置を適用した電子機器の一例たる携帯電話の構成を示す斜視図である。
【図１０】第２実施形態の液晶パネルの構成を示すブロック図である。

【符号の説明】

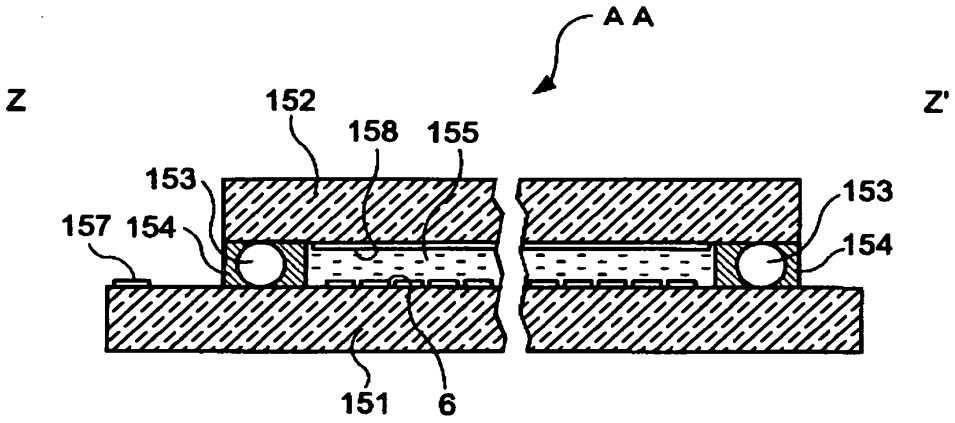
【００５６】
２…走査線、３…データ線、１００…走査線駆動回路、２００…データ線駆動回路、１０…端子群、ＰＴｒｅｆ…基準ピッチ、ＰＴ１、ＰＴ２…第１ピッチ，第２ピッチ、ＡＡ…液晶パネル、Ｂ…フレキシブル基板、Ｃ…外部基板。

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【書類名】図面
【図１】

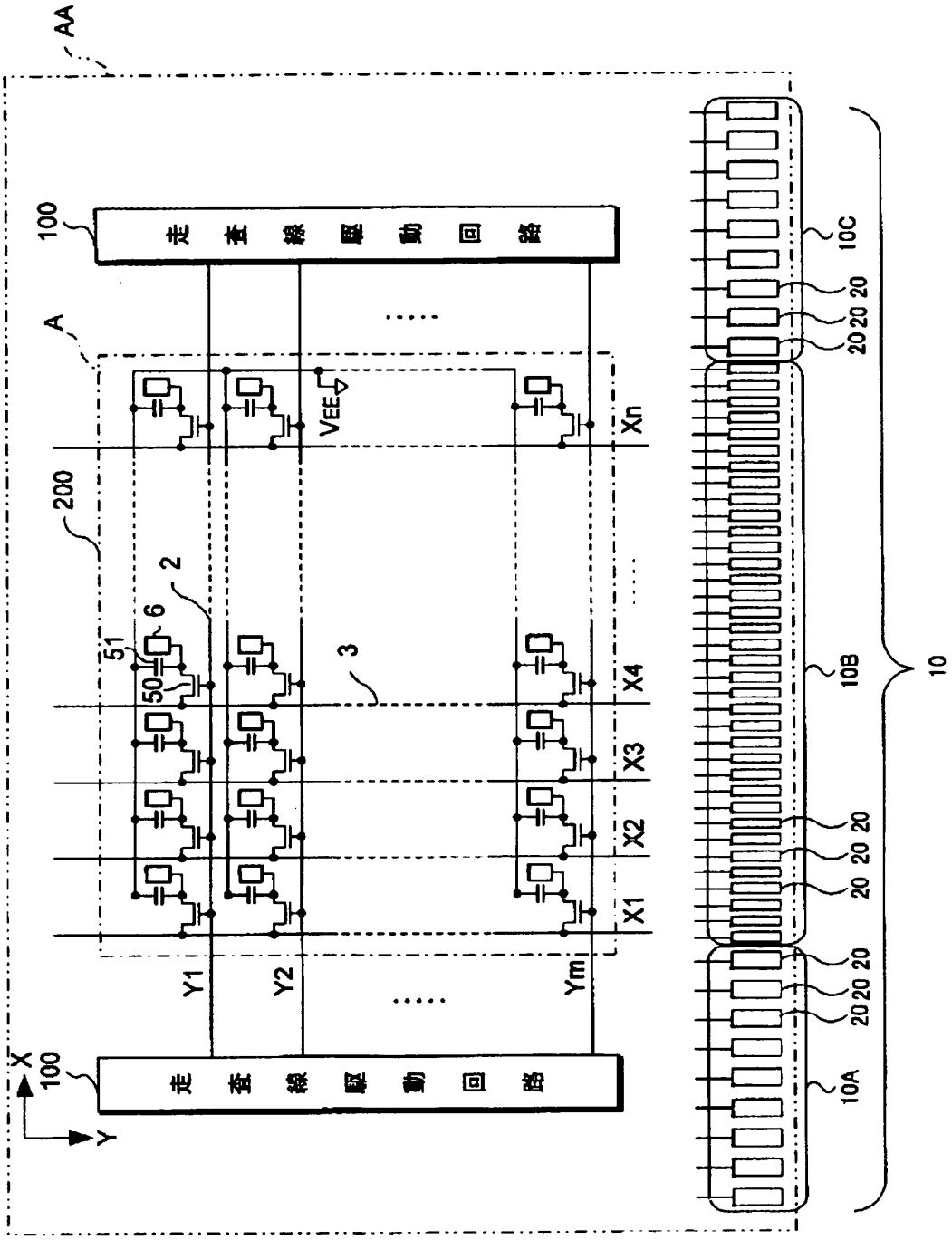


【図２】



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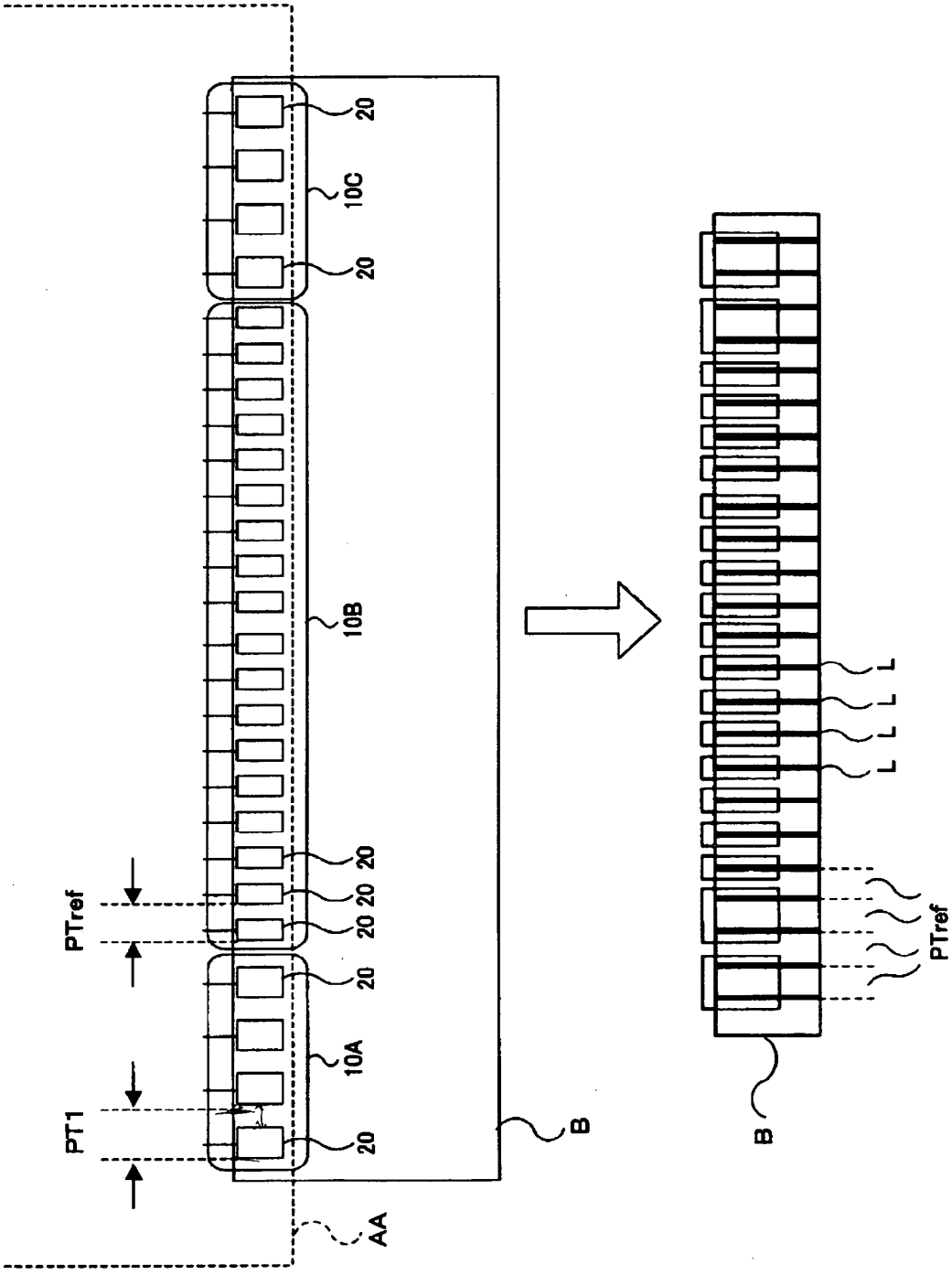
【図３】



出証特２００４－３０６６１１５

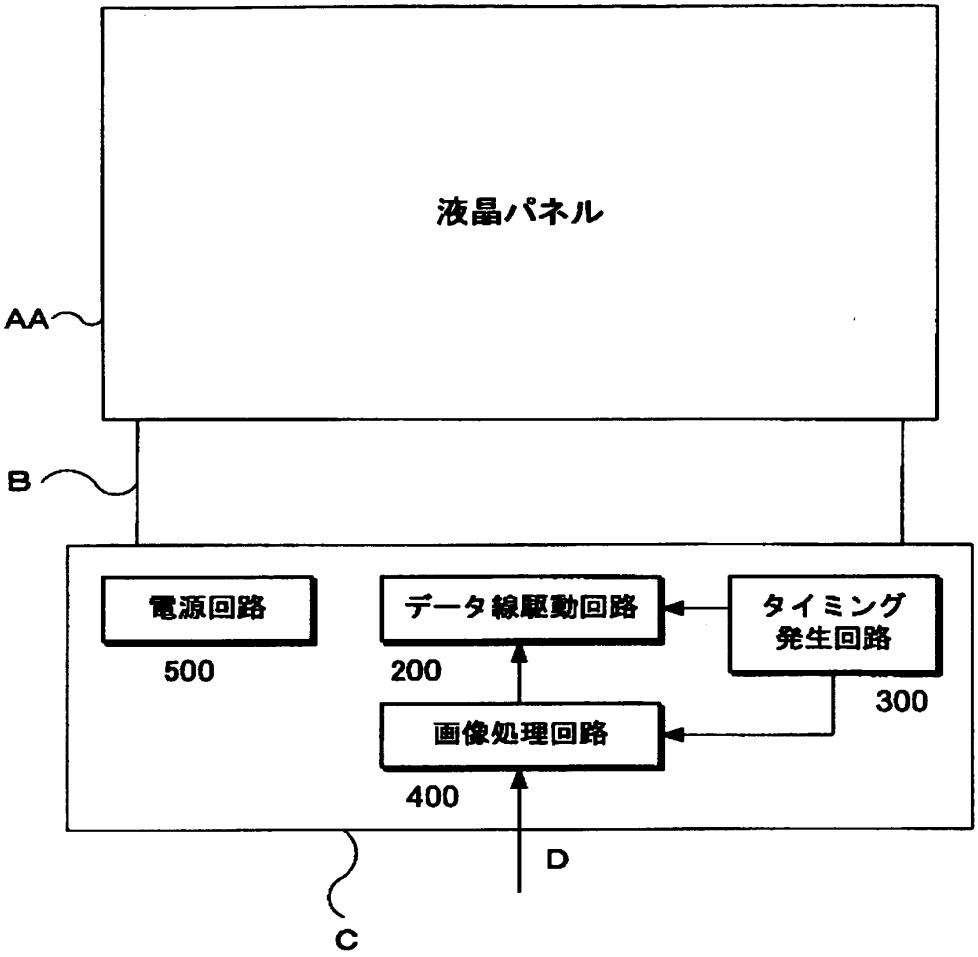
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【図４】



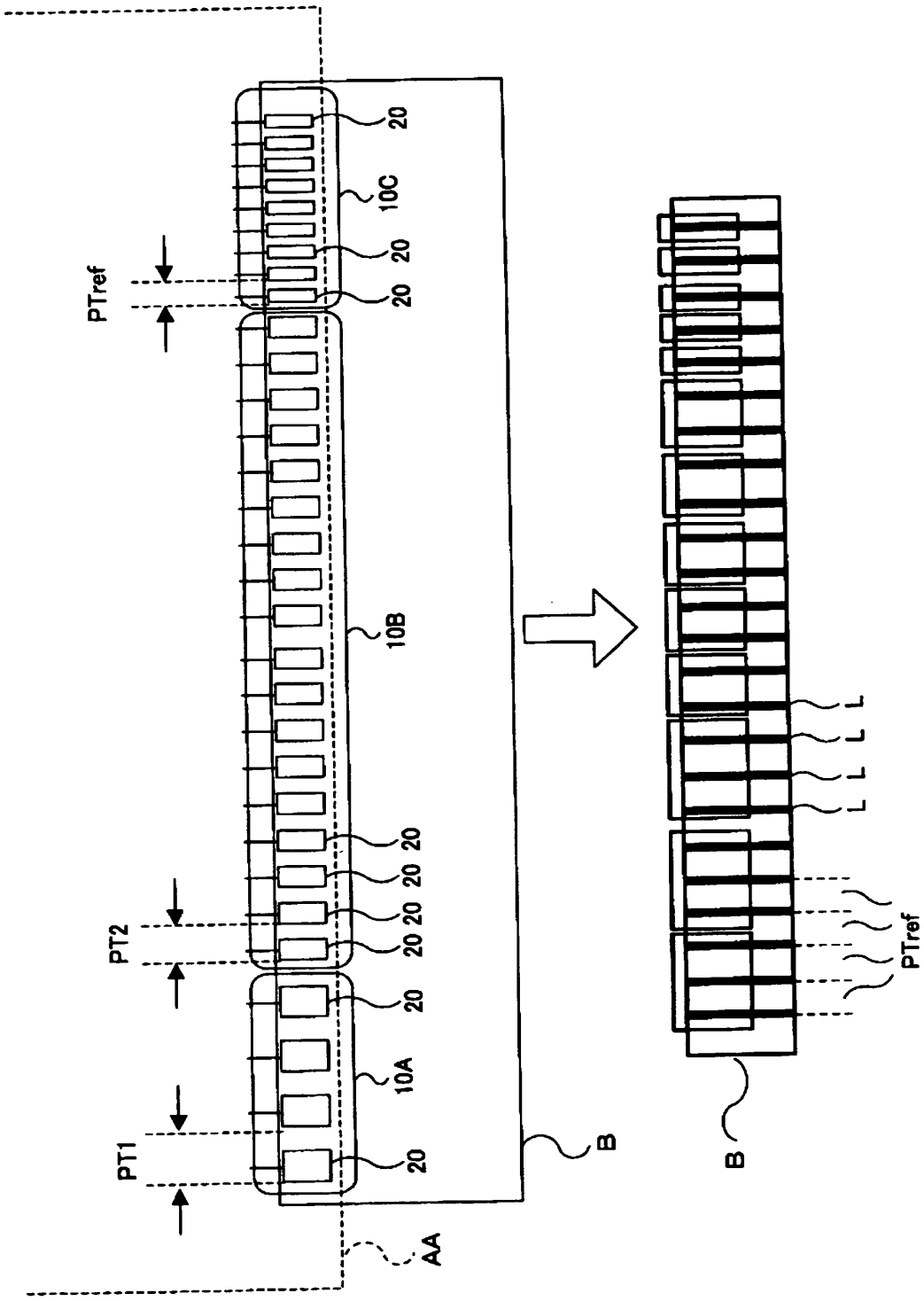
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【図５】



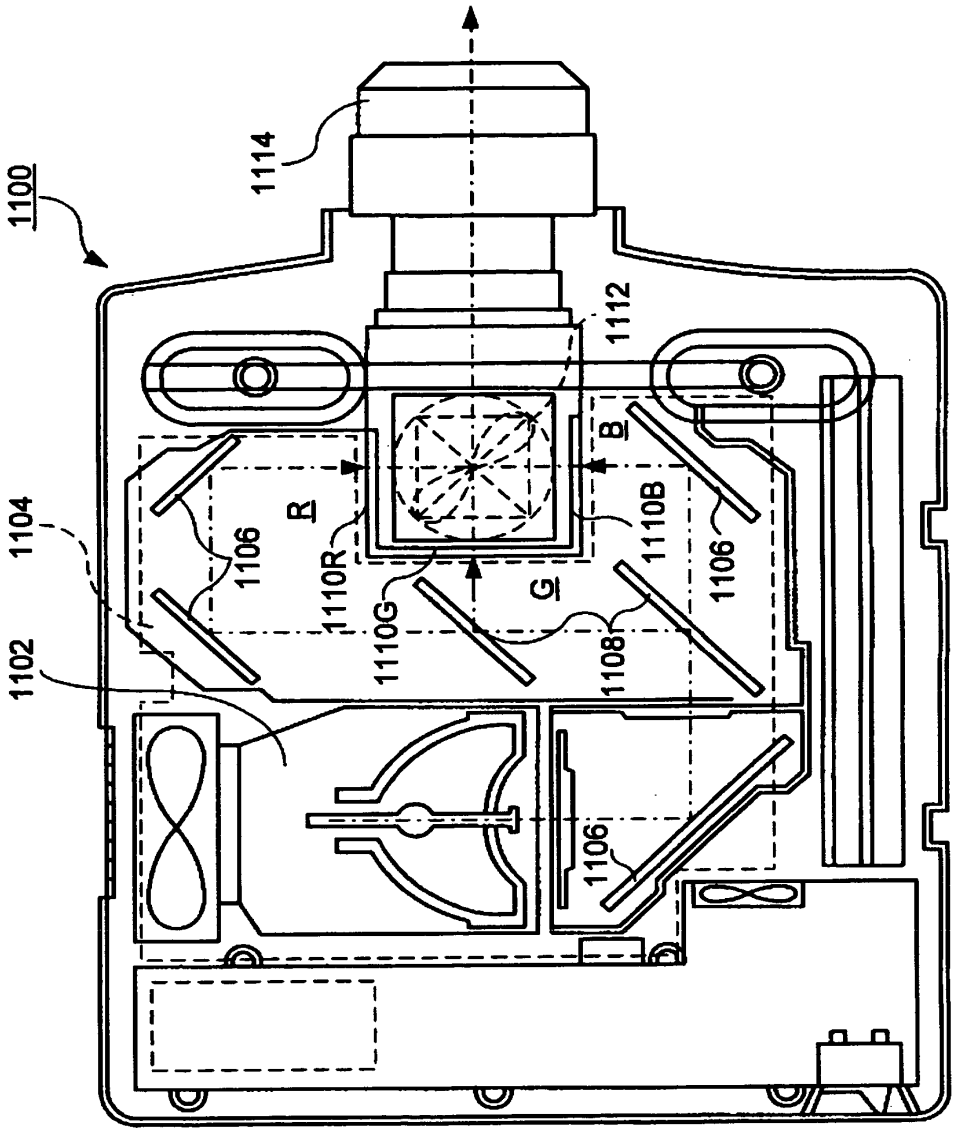
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【図６】



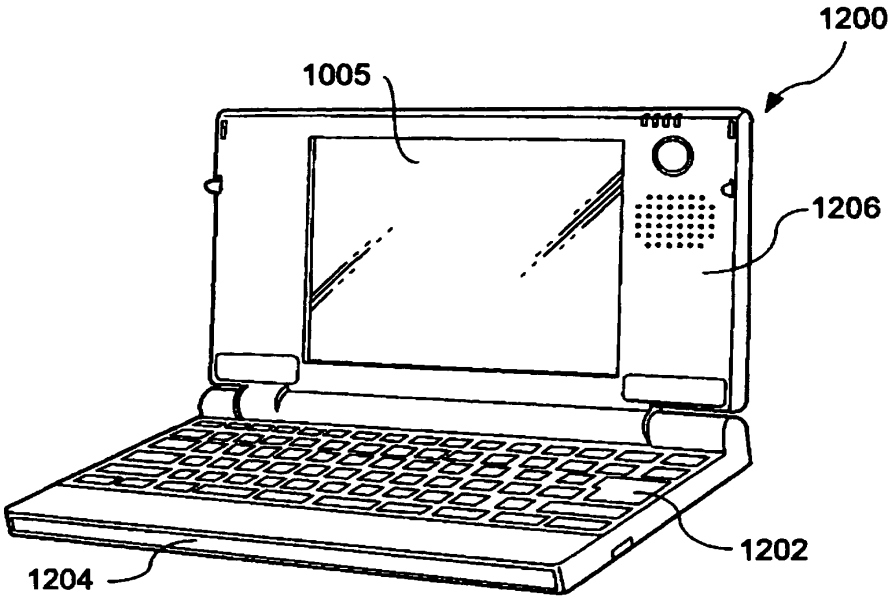
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【図７】

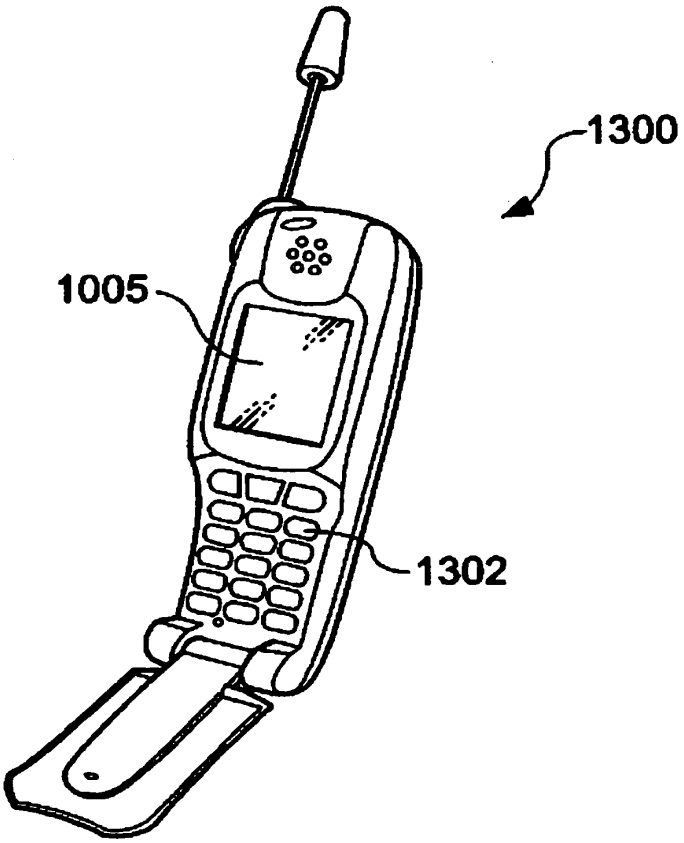


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【図８】

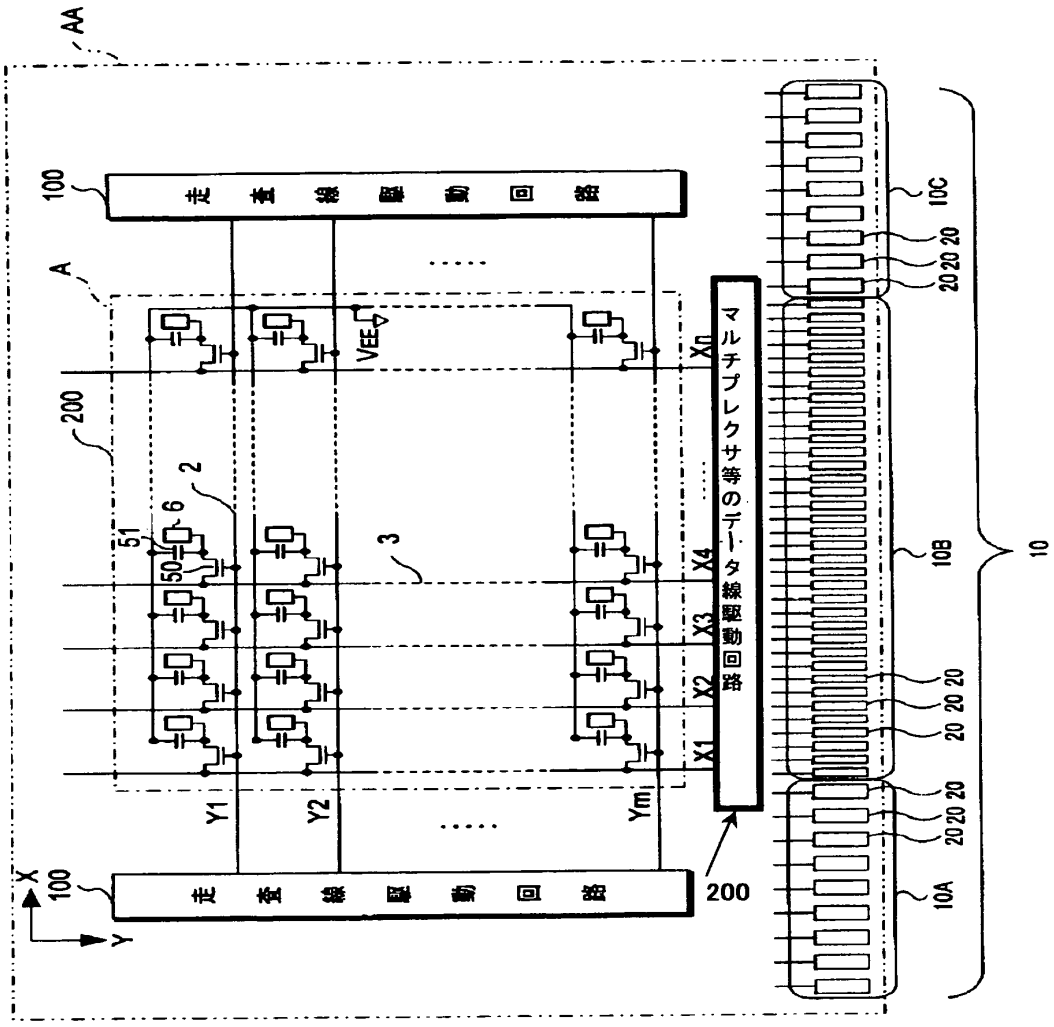


【図９】



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【図１０】



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【書類名】要約書
【要約】
【課題】　実装部材を液晶パネルに高い信頼性の下に接続し、信号の伝送に必要な帯域を確保する。
【解決手段】　液晶パネルＡＡは、第１～第３端子群１０Ａ～１０Ｃからなる端子群１０を備える。第１及び第３端子群１０Ａ及び１０Ｃには、駆動信号が供給される一方、第２端子群１０Ｂには画像信号が供給される。駆動信号は画像信号より高い周波数成分を含む。第１及び第３端子群１０Ａ及び１０Ｃの入力端子２０は、第２端子群２０の入力端子２０よりも面積が大きいので、接触抵抗が小さい。従って、駆動信号のなまりを防止できる。
【選択図】　図４

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認定・付加情報

特許出願の番号	特願２００４－１９３５１５
受付番号	５０４０１１０３１３５
書類名	特許願
担当官	第二担当上席　　００９１
作成日	平成１６年　７月　５日

＜認定情報・付加情報＞

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特願２００４－１９３５１５

出　願　人　履　歴　情　報

識別番号　［０００００２３６９］

１．変更年月日　１９９０年　８月２０日
［変更理由］　新規登録
住　所　東京都新宿区西新宿２丁目４番１号
氏　名　セイコーエプソン株式会社

出証番号　出証特２００４－３０６６１１５

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OIPE JC181
NOV 11 2004
PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin Fujita
Group Art Unit:	2673
Examiner:	N/A
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Director of the United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant hereby submits an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS, AND OTHER INFORMATION

The patents, publications and other information requested to be considered by the Office (except unpublished U.S. patent applications) are listed on Form 1449 attached hereto.

II. COPIES

A.____ Submitted herewith is a legible copy of (i) each U.S. patent application publication and U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; (iii) for each cross-referenced pending U.S. application listed below in Section IV, the application specification including the claims, and any drawing of the application which caused it to be listed including the claims directed to that portion; and (iv) all other information or that portion which caused it to be listed.

B. ____ Any patents, publications or other information which are listed on Form 1449 or on the copies of PTO-892, but which are not enclosed herewith, were previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Serial Number U.S. Filing Date

C.__X__ Because the present application was/is being filed after June 30, 2003, no copies of the U.S. patents or U.S. patent application publications which are listed on the attached Form 1449 are enclosed pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i). Any foreign patent documents or non-patent literature listed on the attached Form 1449 are enclosed herewith.

D.____ This is a PCT application in the entry of the National Phase in the United States. A copy of the International Search Report is attached for the Examiner's information. The documents listed on the International Search Report are listed on the attached Form-1449 for consideration by the Examiner and for listing on any patent resulting from this application. If the International Search Report was from the US, EPO, or JPO search authorities, copies of these references should have been supplied to the USPTO under the trilateral agreement and are believed to be in the file of the above-identified application. (MPEP 1893.03(g))

III. CONCISE EXPLANATION OF THE RELEVANCE (check at least one box)

A._X__ Except as may be indicated below in (B), all of the patents, publications or other information are in the English language (concise explanation not required).

B._X__ A concise explanation of the relevance of each patent, publication or other information listed that is not in the English language is as follows (see 37 C.F.R. § 1.98(a)(3)):

1.____See the attached foreign patent office communication from a counterpart foreign application.
2._X__English translations are provided as indicated on Form-1449.
3.____Other:

C. __X_The following additional information is provided for the Examiner's consideration: JP2822558B is discussed in Applicant's specification

IV. CROSS REFERENCE TO RELATED APPLICATION(S)

A.____The Examiner is advised that the following co-pending application(s) contain(s) subject matter that may be related to the present application. By bringing this(these) application(s) to the Examiner's attention, Applicant(s) does(do) not waive the confidentiality provisions of 35 U.S.C. § 122.

Serial No. Filing Date Art Unit

V. THIS IDS IS BEING FILED UNDER

A.____**37 C.F.R. § 1.97(b)**: (check only one box)

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1. ____ within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) (37 C.F.R. § 1.97(b)(1)). No fee or certification is required.

2. ____ within three months of the date of entry of the national stage as set forth in §1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or certification is required.

3. __X__ before the mailing of a first Office Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or certification is required. In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the certification under 37 C.F.R. § 1.97(e) below; or, if no certification has been made, charge our deposit account a fee in the amount of $180.00 as required by 37 C.F.R. § 1.17(p).

4. ____ before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No fee or certification is required.

B. ____**37 C.F.R. § 1.97(c)**: (check only one box)

before the mailing date of either any Final Office Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution.

1. ____No certification; therefore, a fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

2. ____See the certification below. No fee is required.

C. ____**37 C.F.R. § 1.97(d)**:

after the mailing date of either a Final Office Action under 37 C.F.R. § 1.113 or a Notice of Allowance under 37 C.F.R. § 1.311, yet on or before payment of the issue fee.

1. ____See the certification below. A fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

VI. CERTIFICATION UNDER 37 C.F.R. § 1.97(e): (check only one box)

The undersigned hereby certifies that:

A. ____ each item of information contained in this IDS was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS (See 37 C.F.R. §

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1.97(e)(1)). See further statement under 37 C.F. R. 1.704(d) below in section VII, if applicable; or

B. ____ no item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS (See 37 C.F.R. § 1.97(e)(2)).

C. ____Some of the items of information were first cited in a communication from a foreign patent office. As to this information, the undersigned hereby certifies that each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby certifies that no item of this remaining information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS.

VII. STATEMENT UNDER 37 CFR 1.704(d)

The undersigned hereby states that:

___ each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this IDS.

VIII. PAYMENT OF FEES (check only one box)

A. ____ A check in the amount of $180.00 is enclosed for the above-identified fee.

B. ____Please charge Deposit Account No. 50-3213 in the amount of $180.00 for the above-indicated fee. A duplicate copy of this paper is attached.

The above references are being cited only in the interest of candor and without any admission that they constitute statutory prior art, contain matter which anticipates the invention, or which would render the same obvious, either singly or in combination, to a person of ordinary skill in the art. Furthermore, this Information Disclosure Statement shall not be construed as a representation that a search has been made.

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If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule (with a petition if necessary) and charge the appropriate fee to Deposit Account No. 50-3213.

Please charge any additional fees or credit any overpayment pursuant to 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 50-3213.

Respectfully submitted,

Dated: November 11, 2004

By: _____
G. Gregory Schivley
Reg. No. 27,382

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

GGS/msm

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NOV 1 1 2004
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FORM HDP-1449 (Based on Form PTO-1449)

PATENT AND TRADEMARK OFFICE
INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Sheet 1 of 1

ATTORNEY DOCKET NO.	SERIAL NO.
9319S-000838	10/914,044
APPLICANT	
Shin Fujita	
FILING DATE	GROUP
8/6/2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.		2822558	Sept/1998	Japan		Abstract	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.		

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EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PATENT ABSTRACTS OF JAPAN

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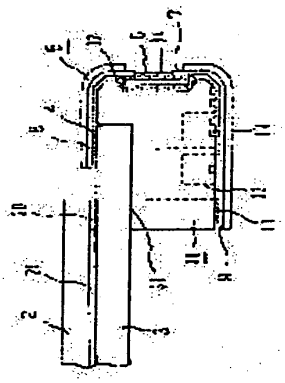
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OTSUKI HIDEAKI
KOKOGAWA TOORU
TAKASAGO HAYATO

(54) PRODUCTION OF LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:
PURPOSE: To obtain the compact liquid crystal display device which has good workability of assembly and is free from the degradation in electrical insulating characteristic by using a three-dimensional frame body circuit board in which chip-shaped electronic parts and an IC for driving of a film carrier can be housed and in which a liquid crystal panel can be mounted.
CONSTITUTION: The frame body circuit board 30 is worked by molding with a recessed part 31 for housing the liquid crystal panel stop the frame body, a recessed part 32 for housing the IC for driving on the side face of the frame body and a recessed part 33 for housing the electronic parts on the under surface of the frame body. Wiring patterns 14 constituting a control circuit for the IC 6 for driving are formed on the under surface of the frame body. The need for bending the film carrier after the connection of the circuit boards in the conventional manner or for connecting leads to each other between the circuit boards on the respective sides is eliminated by using this frame body circuit board. The effect of having the good workability for the assembly of the driving circuit parts of the liquid crystal display device and allowing the compact packaging with high reliability is obtd.



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最終頁に続く

(54)【発明の名称】　液晶表示装置及びその製造方法

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(57)【特許請求の範囲】

【請求項１】液晶パネル、回路基板、電子部品及び駆動用ICを搭載したフイルムキャリアから構成され、上記液晶パネルと上記回路基板を複数個のフイルムキャリアで接続される構造を有する液晶表示装置において、上記回路基板が、上面に液晶パネル収納凹部を設けると共に所定面に駆動用IC収納凹部と電子部品収納凹部とを設けた３次元的な枠体により構成されたことを特徴とする液晶表示装置。

【請求項２】液晶パネルと、電子部品及び駆動用ICを搭載した複数のフイルムキャリアと、上面に液晶パネル収納凹部を、側面に駆動用IC収納凹部を、下面に電子部品収納凹部を設けた枠体からなる回路基板とを使用し、下記（ａ）～（ｄ）の工程を含む液晶表示装置の製造方法。

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（ａ）液晶パネルの接続端子にフイルムキャリアのリードを接続する

（ｂ）液晶パネルを回路基板の液晶パネル収納凹部に載置する

（ｃ）フイルムキャリアを枠体の側面に沿って折り曲げて駆動用ICを駆動用IC収納凹部に収納する

（ｄ）フイルムキャリアを枠体の下面に沿って折り曲げてフイルムキャリアのリードを回路基板に接続する

【発明の詳細な説明】

［産業上の利用分野］

本発明は、液晶テレビやOA機器の液晶ディスプレイ等に用いられる液晶表示装置及びその製造方法に関するものである。

［従来の技術］

近年、液晶表示装置は、従来の陰極旋管を用いた表示

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装置に匹敵する表示性能が得られるようになり、陰極線管に替わって、テレビやディスプレイに広く用いられている。液晶表示装置には、ドットマトリックス型やアクティブマトリックス型の両者があるが、いずれも液晶パネルと電子部品を搭載した回路基板及び駆動用ICから構成されている。

駆動回路モジュールの形態や駆動回路基板の取り付け方法は各種にあるが、一般的に液晶パネルの３辺あるいは４辺に画素本数に対応する外部接続端子が配置され、駆動用ICを搭載したフィルムキャリアが液晶パネルの外部接続端子と電子部品を搭載した回路基板を橋渡しする形態で接続される。

液晶表示装置のコンパクト化を実現するために、表示エリアの外縁における実装エリアを極力小さくし、かつ薄型化する必要がある。

従来例として、薄膜トランジスタ（TFT）アクティブマトリックス型液晶表示装置における実装形態には、特開昭63－253390号公報に記載される第３図及び第４図に示すものがある。第３図は従来の実施例における側面図、第４図は完成前の側面図である。

図中、（１）は液晶パネル、（２）はカラーフィルタ基板、（３）はTFTアレイ基板で、TFTアレイ基板の各辺の端縁部には内部画素に繋がる外部接続端子（４）を画素数に対応した数だけ並べて設けてある。（５）はフィルムキャリアで、駆動用IC（６）がインナーリードボンディング（７）されており、IC出力につながるアウターリード（８）はアレイ基板の外部接続端子（４）に異方性導電膜で接続され、IC入力につながるアウターリード（９）は回路基板（12）の接続パッド（10）に半田付け接続される。回路基板上には、駆動用ICのコントロール回路を構成するコントロールICの他、ノイズ低減用部品として抵抗チップ、コンデンサチップ、インダクタチップ、ボリウムチップ、トリマーコンデンサ等のチップ部品からなる電子部品（15）が搭載されている。

フィルムキャリア（５）には空隙部（11）が複数箇所に設けられており、第４図に示すように液晶パネルの各辺でパネルの外部接続端子及び回路基板の接続パッドに接続した後、第３図に示すように上記空隙部で内側に折曲することにより回路基板が中段に位置する形態で液晶パネル（１）、回路基板（12）及び駆動用IC（６）が重層的に配置され、さらに各辺の回路基板は接続リードにより相互接続される。回路基板（12）は液晶パネル（１）及びフィルムキャリア（５）のいずれにも重ならない部分を有し、この部分に背の高い電子部品（15）が取り付けられる。

［発明が解決しようとする課題］

上記構成によると、液晶パネル下部に回路基板及びフィルムキャリアに実装された駆動用ICが配置されるため、表示エリア外縁の実装寸法を小さくできる利点はあるものの、フィルムキャリアのアウターリード接続後に

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ベースフィルム（13）に設けた空隙部（11）で巻取るように折曲し、さらに各辺に接続された回路基板間の接続リードで接続する必要があるため組立て作業性が悪い。また、折曲する空隙部は、ベースフィルムがないため機械的強度が弱く、接続端子数に伴いフィルムキャリアの配線パターン（14）のパターン幅が小さくなると、断線する危険性があるだけでなく、導体が露出しているため、パターン間隔が小さくなると電気的絶縁性が低下するという課題があった。

この発明は上記のような課題を解消するためになされたもので、組立て作業性がよく、かつ電気的絶縁性が低下しないコンパクトな液晶表示装置及びその製造方法を得ることを目的とする。

［課題を解決するための手段］

本発明に係る液晶表示装置は、液晶パネル、回路基板、電子部品及び駆動用ICを搭載したフイルムキャリアから構成され、上記液晶パネルと上記回路基板を複数個のフイルムキャリアで接続され、上記回路基板を、上面に液晶パネル収納凹部を設けると共に所定面に駆動用IC収納凹部と電子部品収納凹部とを設けた３次元的な枠体により構成したものである。

本発明に係る液晶表示装置の製造方法は、液晶パネルと、電子部品及び駆動用ICを搭載した複数のフイルムキャリアと、上面に液晶パネル収納凹部を、側面に駆動用IC収納凹部を、下面に電子部品収納凹部を設けた枠体からなる回路基板とを使用し、下記（ａ）～（ｄ）の工程を含むものである。

（ａ）液晶パネルの接続端子にフイルムキャリアのリードを接続する

（ｂ）液晶パネルを回路基板の液晶パネル収納凹部に載置する

（ｃ）フイルムキャリアを枠体の側面に沿って折り曲げて駆動用ICを駆動用IC収納凹部に収納する

（ｄ）フイルムキャリアを枠体の下面に沿って折り曲げてフイルムキャリアのリードを回路基板に接続する

［作用］

本発明では、回路基板の上面に設けられた液晶パネル収納凹部には液晶パネルが配置され、所定面に設けられた駆動用IC収納凹部には駆動用ICが、電子部品収納凹部には電子部品がそれぞれ収納されている。

別の発明では、液晶パネルの接続端子にフイルムキャリアのリードを接続し（工程ａ）、液晶パネルを回路基板の液晶パネル収納凹部に載置し（工程ｂ）、フイルムキャリアを枠体の側面に沿って折り曲げて駆動用ICを駆動用IC収納凹部に収納し（工程ｃ）、フイルムキャリアを枠体の下面に沿って折り曲げてフイルムキャリアのリードを回路基板に接続している（工程ｅ）、従って、表示エリア外縁部に駆動用ICや回路基板を配置することがないため、駆動回路部分の実装構造をコンパクトに形成することが可能となる。

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[実施例]

以下、本発明の一実施例を図について説明する。

第１図は３辺に複数個のフィルムキャリアを接続した液晶パネルを、枠体上部の凹部に載置した状態を示す斜視図である。また、第２図は、フィルムキャリアのアウターリード接続完了後の液晶表示装置の側面図である。

図中、（１）は液晶パネルで、TFTアレイ基板（３）とカラーフィルタ基板（２）がシール（20）で一体化され、両基板間には液晶（21）が充填されている。アレイ基板上には、内部のTFTのソースラインあるいはゲートラインに繋がる外部接続端子（４）が形成されており、フィルムキャリア（５）のアウターリード（８）が異方性導電膜で接続されいてる。フィルムキャリアには駆動用IC（６）がインナーリードボンディング（７）がされている。（30）は枠体回路基板で、枠体上面には液晶パネルを収納するための凹部（31）、枠体側面には駆動用ICを収納するための凹部（32）、枠体下面には電子部品を収納するための凹部（33）が成型加工されている。また、枠体下面には、駆動用IC（６）のコントロール回路を構成する配線パターン（14）が形成されている。

液晶パネルの外部接続端子に接続されたフィルムキャリアは、枠体上面コーナー部で枠体側面の凹部に駆動用ICを収納する状態で直角に折り曲げられ、さらにフィルムキャリアのアウターリードは枠体表面の接続パッドに半田付け接続される。さらに、枠体側面の凹部に収納された駆動用IC（６）は保護コート（34）が施される。

本発明の枠体回路基板は、例えば導体パターンを形成したフィルムを型内転写した射出成型加工された樹脂からなり、枠体表面及び凹部の一部に所望の導体パターンが形成されている。枠体上面には液晶パネルを載置するための凹部、枠体側面にはフィルムキャリアの駆動用ICを収納するための凹部、枠体下面にはチップ部品を収納するための凹部を有し、該凹部内に転写された配線パターンに接続されたチップ部品が枠体回路基板から突出しない凹部深さを有している。

実装手順は、まず所望の位置に成型加工した凹部を有する枠体回路基板の凹部内の配線パターン上に、上記の種々のチップ部品を電気的接続する。次にい該枠体回路基板上部の凹部に複数個のフィルムキャリアのアウターリードを、外部接続端子に接続した液晶パネルを載置した後、フィルムキャリアを枠体に沿って枠体側面の凹部に駆動用ICを収納するように液晶パネル下部方向に直角に折り曲げ、さらに枠体下面にフィルムキャリアを折り曲げアウターリードを、枠体表面に形成された接続パッドに接続する。次に枠体側面の駆動ICを収納した凹部に、IC保護コートを施すことにより組立ては完了する。

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上記の実施例では、枠体回路基板として配線パターンを型内転写した３次元形状の射出成型樹脂基板を使用したが、立体成型された他の製造方法による樹脂基板やアルミ等の金属ベース基板も適用可能である。

また、上記の実施例では、駆動用ICの収納凹部あるいは電子部品の収納凹部を枠体回路基板の側面あるいは下面の配置したが、液晶表示装置に要求される形態によって、それぞれ枠体回路基板の下面あるいは側面に配置してもよい。

[発明の効果]

以上のように本発明によれば、上記の回路基板を、上面に液晶パネル収納凹部を設けると共に所定面に駆動用IC収納凹部と電子部品収納凹部とを設けた３次元的な枠体により構成したので、コンパクトな液晶表示装置を実現することができる。

更に、別の発明によれば、液晶パネルの接続端子にフィルムキャリアのリードを接続する工程ａ、液晶パネルを回路基板の液晶パネル収納凹部に載置する工程ｂ、フィルムキャリアを枠体の側面に沿って折り曲げて駆動用ICを駆動用IC収納凹部に収納する工程ｃ、フィルムキャリアを枠体の下面に沿って折り曲げてフィルムキャリアのリードを回路基板に接続する工程ｅを備えているので、従来のように回路基板を接続後にフィルムキャリアを折り曲げたり、各辺の回路基板間をリードで相互接続する必要がないため、液晶表示装置の駆動回路部分の組立て作業性が良く、高信頼でコンパクト実装できるといった効果がある。

【図面の簡単な説明】

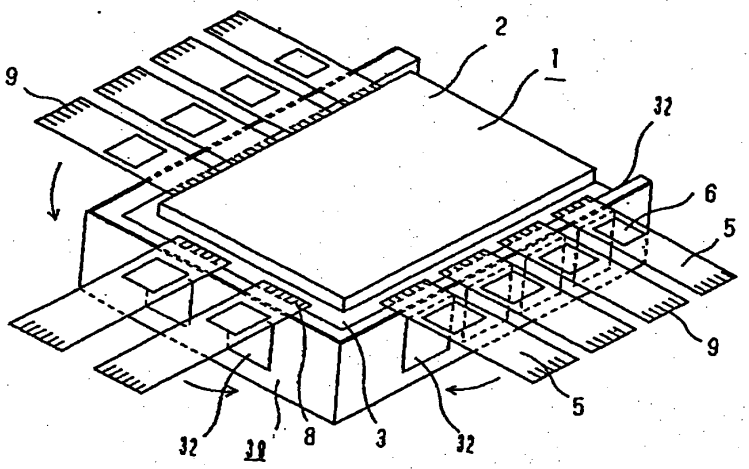
第１図は３辺に複数個のフィルムキャリアを接続した液晶パネルを、枠体上部の凹部に載置した状態を示す斜視図、第２図はフィルムキャリアのアウターリード接続完了後の液晶表示装置の側面断面図、第３図は従来の実施例を示す側面断面図、第４図は第３図のフィルムキャリアの折り曲げ前の状態を示す側面図である。

図において（１）は液晶パネル、（２）はカラーフィルタ基板、（３）はTFTアレイ基板、（４）は外部接続端子、（５）はフィルムキャリア、（６）は駆動用IC、（７）はインナーリードボンディング、（８）はIC出力につながるアウターリード、（９）はIC入力につながるアウターリード、（10）は接続パッド、（11）は空隙部、（12）は回路基板、（13）はベースフィルム、（14）は配線パターン、（15）は電子部品、（20）はシール、（21）は液晶、（30）は枠体回路基板、（31）は液晶パネル収納凹部、（32）は駆動用IC収納凹部、（33）は電子部品収納凹部、（34）は保護コートである。

なお、図中、同一符号は同一または相当部分を示す。

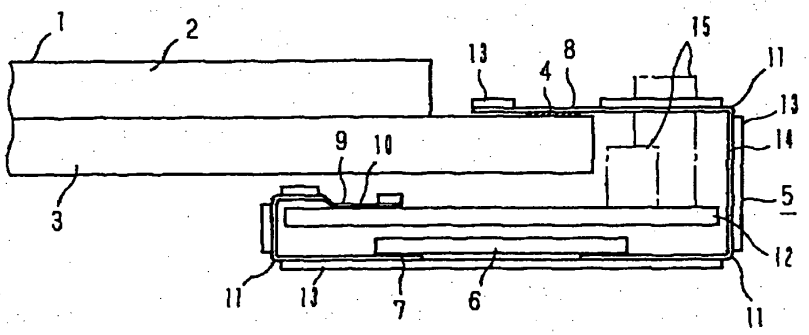
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【第１図】

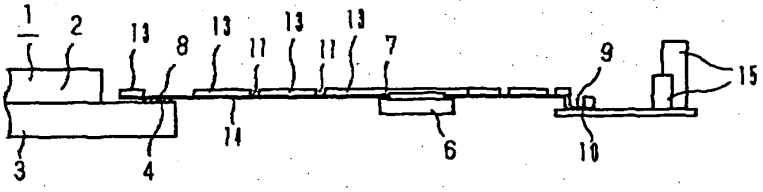


１：液晶パネル
２：カラーフィルタ基板
３：ＴＦＴアレイ基板
５：フィルムキャリア
６：駆動用ＩＣ
30：枠体回路基板
32：駆動用ＩＣ収納凹部

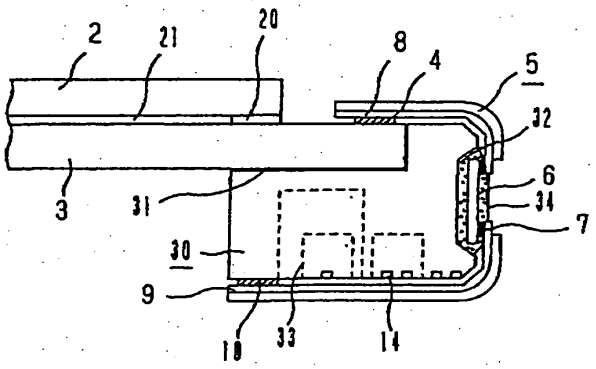
【第３図】



【第４図】



【第２図】



7：インナーリードボンディング
9：アウターリード
10：接続パッド
14：配線パターン
20：シール
21：液晶
31：液晶パネル収納凹部
33：電子部品収納凹部
34：保護コート

フロントページの続き

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(58)調査した分野(Int.Cl.6，ＤＢ名)
G02F　1/1333
G02F　1/1345

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3-8-06

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/914,044
Filing Date	August 6, 2004
First Named Inventor	Shin FUJITA
Art Unit	2673
Examiner Name	To be assigned
Total Number of Pages in This Submission	
Attorney Docket Number	9319S-000838

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:

  Form 1449 with 4 attached references; and Return Receipt Postcard

Remarks: The Commissioner is hereby authorized to charge any additional fees that may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 50-3213. A duplicate copy of this sheet is enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name G. Gregory Schivley Bryant E. Wade	Reg. No. 27,382 40,344
Signature			
Date	March 6, 2006		

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

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Signature		Date	March 6, 2006

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EV 853 855 768 US



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin FUJITA
Group Art Unit:	2673
Examiner:	To be assigned
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Director of the United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant hereby submits an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS, AND OTHER INFORMATION

The patents, publications and other information requested to be considered by the Office (except unpublished U.S. patent applications) are listed on Form 1449 attached hereto.

II. COPIES

A. ☒ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed, other than U.S. patents and U.S. patent application publications unless required by the Office; (iii) each unpublished U.S. application listed below in Section IV (i.e., including the specification, claims, and any drawing of the application, or that portion of the application which caused it to be listed, including any claims directed to that portion), except for such applications filed on or after June 30, 2003, pursuant to the Waiver of the Copy Requirement in 37 C.F.R. 1.98 (OG Notice dated October 19, 2004); and (iv) all other information or that portion which caused it to be listed.

B. ☐ Any patents, publications or other information which are listed on Form 1449 or on the copies of PTO-892, but which are not enclosed herewith, were

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previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Serial Number	U.S. Filing Date

C. ☐ This is a PCT application in the entry of the National Phase in the United States. A copy of the International Search Report is attached for the Examiner's information. The documents listed on the International Search report are listed on the attached Form 1449 for consideration by the Examiner and for listing on any patent resulting from this application. If the International Search report was from the US, EPO, or JPO search authorities, copies of these references should have been supplied to the USPTO under the trilateral agreement and are believed to be in the file of the above-identified application. (MPEP 1893.03(g).)

III. CONCISE EXPLANATION OF THE RELEVANCE (check at least one box)

A. ☐ Except as may be indicated below in (B), all of the patents, publications or other information are in the English language (concise explanation not required).

B. ☒ A concise explanation of the relevance of each patent, publication or other information listed that is not in the English language is as follows (see 37 C.F.R. § 1.98(a)(3)):

1. ☒ See the attached foreign patent office communication regarding a related foreign application in: Japan

2. ☒ English translations are provided as follows: As indicated on attached Form 1449.

3. ☐ Other:

C. ☐ The following additional information is provided for the Examiner's consideration:

IV. CROSS REFERENCE TO RELATED APPLICATION(S)

A. ☐ The Examiner is advised that the following co-pending application(s) contain(s) subject matter that may be related to the present application. By bringing this(these) application(s) to the Examiner's attention, Applicant(s) does (do) not waive the confidentiality provisions of 35 U.S.C. § 122.

Serial No.	Filing Date	Inventor(s)

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V. THIS IDS IS BEING FILED UNDER

A. ☒ **37 C.F.R. § 1.97(b):** (check only one box)

1. ☐ within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) (37 C.F.R. § 1.97(b)(1)). No fee or certification is required.

2. ☐ within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or certification is required.

3. ☒ before the mailing of a first Office Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or certification is required. In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the certification under 37 C.F.R. § 1.97(e) below; or, if no certification has been made, charge our deposit account a fee in the amount of $180.00 as required by 37 C.F.R. § 1.17(p).

4. ☐ before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No fee or certification is required.

B. ☐ **37 C.F.R. § 1.97(c):** (check only one box)

before the mailing date of either any Final Office Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution.

1. ☐ No certification; therefore, a fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

2. ☐ See the certification below. No fee is required.

C. ☐ **37 C.F.R. § 1.97(d):**

after the mailing date of either a Final Office Action under 37 C.F.R. § 1.113 or a Notice of Allowance under 37 C.F.R. § 1.311, yet on or before payment of the issue fee.

1. ☐ See the certification below. A fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

VI. CERTIFICATION UNDER 37 C.F.R. § 1.97(e): (check only one box)

The undersigned hereby certifies that:

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A. ☒ each item of information contained in this IDS was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS (See 37 C.F.R. § 1.97(e)(1)). See further statement under 37 C.F.R. 1.704(d) below in section VII, if applicable; or

B. ☐ no item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS (See 37 C.F.R. § 1.97(e)(2)).

C. ☐ some of the items of information were first cited in a communication from a foreign patent office. As to this information, the undersigned hereby certifies that each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby certifies that no item of this remaining information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS.

VII. STATEMENT UNDER 37 C.F.R. 1.704(d)

The undersigned hereby states that:

☐ each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this IDS.

VIII. PAYMENT OF FEES (check only one box)

A. ☐ A check in the amount of $180.00 is enclosed for the above identified fee.

B. ☐ Please charge Deposit Account No. 50-3213 in the amount of $180.00 for the above-indicated fee.

The above references are being cited only in the interest of candor and without any admission that they constitute statutory prior art, contain matter which anticipates the invention, or which would render the same obvious, either singly or in combination, to a person of ordinary skill in the art. Furthermore, this Information Disclosure Statement shall not be construed as a representation that a search has been made.

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If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule (with a petition if necessary) and charge the appropriate fee to Deposit Account No. 50-3213 (Epson R&D).

Please charge any additional fees or credit any overpayment pursuant to 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 50-3213 (Epson R&D).

Respectfully submitted,

Dated: March 6, 2006

By: _____
G. Gregory Schivley
Reg. No. 27,382
Bryant E. Wade
Reg. No. 40,344

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[GGS/BEW/pvd]

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FORM HDP-1449 (Based on Form PTO-1449)

PATENT AND TRADEMARK OFFICE
INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Sheet 1 of 1

ATTORNEY DOCKET NO.	SERIAL NO.
9319S-000838	10/914,044
APPLICANT	
Shin FUJITA	
FILING DATE	GROUP
August 6, 2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.		2003-152019A	05/23/2003	Japan		X	
2.		2003-216064A	07/30/2003	Japan		X	
3.		11-223832A	08/17/1999	Japan		X	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.		Examination result regarding corresponding Japanese application

*One or more of the English translation documents submitted herewith may be Abstracts only or partial machine created translations from the Japanese Patent Office. As such, the submitter does not necessarily vouch for their accuracy. Additional information may be obtained from the Japanese Patent Office web site at www.jpo.go.jp

Examiner:	Date Considered:

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2003－152019
（P2003－152019A）
(43)公開日　平成15年５月23日(2003.5.23)

(51)Int.Cl.'	識別記号	ＦＩ		テーマコード'(参考)
Ｈ０１Ｌ　21/60	３１１	Ｈ０１Ｌ　21/60	３１１Ｒ	２Ｈ０９２
Ｇ０２Ｆ　1/1345		Ｇ０２Ｆ　1/1345		５Ｆ０４４

審査請求　未請求　請求項の数３　ＯＬ　（全　７　頁）

(21)出願番号　特願2001－346085(P2001－346085)

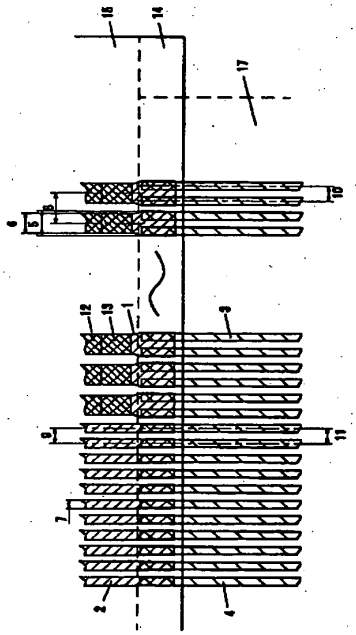
(22)出願日　平成13年11月12日(2001.11.12)

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最終頁に続く

(54)【発明の名称】　電極端子の接続構造及びその構造を用いた液晶表示装置

(57)【要約】
【課題】　異方性導電樹脂で熱圧着接続される電極部分における気泡発生を防止し、信頼性の高い、大容量表示の液晶表示装置を提供する。
【解決手段】　広狭少なくとも２種類の幅５，７の電極端子１，２が形成された第１の基板１５を第２の基板１７に異方性導電樹脂２３で熱圧着する接続構造において、第２の基板１７の電極端子３，４は第１の基板１５における最も狭い方の幅７と接続されるようほぼ同じ幅で形成され、第１の基板１５における広い幅の電極端子1には、第２の基板１７の電極端子３が複数本接続される。



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【特許請求の範囲】

【請求項１】　広狭少なくとも２種類の幅の電極端子が形成された第１の基板を第２の基板に異方性導電樹脂で熱圧着する接続構造において、

第２の基板の電極端子は第１の基板における最も狭い方の幅とそれぞれ接続されるようほぼ同じ幅で形成され、第１の基板における広い幅の電極端子には、第２の基板の電極端子が複数本接続されることを特徴とする電極端子の接続構造。

【請求項２】　前記第２の基板に形成される電極端子の間隔が全て均等であることを特徴とする請求項１記載の電極端子の接続構造。

【請求項３】　前記第１の基板は、液晶表示パネルの一方の基板であり、前記第２の基板は、テープキャリアパッケージであることを特徴とする請求項１又は請求項２記載の電極端子の接続構造を持った液晶表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、異方性導電樹脂を用いた電極端子の接続構造、特に、液晶表示装置に使用されるガラス基板とテープキャリアパッケージにおける電極端子の接続構造に関する。

【０００２】

【従来の技術】近年の携帯電話の普及により、画面に用いられる液晶表示装置に対する更なる大容量表示及び高信頼性が求められている。以下に、従来の液晶表示装置について、図を使用して説明する。図２（ａ）は、液晶表示装置の上面図及び側面図、図２（ｂ）は、接続部近辺の側面図である。図４は、従来の液晶表示装置の表ガラスとＴＣＰの接続部近辺の図である。液晶表示装置には、個々の表示部に相当する透明電極が備えられており、透明電極は共通に制御されるコモン（common：以下「ＣＯＭ」）電極と、個々に制御されるセグメント（segment：以下「ＳＥＧ」）電極とからなる。これらの電極は表ガラス１５上に配線され、表ガラス１５に形成された接続部１４に、それぞれＣＯＭ電極端子１、ＳＥＧ電極端子２が形成される。また、裏ガラス１６にもＣＯＭ電極端子１２が形成される。接続部１４近辺のＣＯＭ電極端子１の接続部１３において、表ガラスＣＯＭ電極端子１と裏ガラスＣＯＭ電極端子１２が、シール剤２２に組み込まれた金属メッキ付き樹脂ボール２１により、電気的に接続されている。ＴＣＰ１７は、ポリイミド樹脂フィルム２４に各透明電極の制御を行う駆動ドライバーＩＣを具備し、その裏面側にＣＯＭ電極端子３及びＳＥＧ電極端子４が形成されたもので、それぞれ表ガラス１５のＣＯＭ電極端子１及びＳＥＧ電極端子２と接続部１４にて接続されている。接続部１４における接続は、通常、接着剤中に導電性の粒子が混合された異方性導電樹脂（anisotropic conductive film：ＡＣＦ）２３を用いて熱圧着で行われる。接着後、液晶表示装置の狭

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額縁化のために、ＴＣＰ１７は折り曲げスリットＳにおいて裏面側に折り曲げられる。

【０００３】最近の携帯電話においては、単なる音声通信だけではなく、文字通信のニーズが高まり、一画面にたくさんの文字情報が表示できる大容量の液晶表示装置が求められている。具体的には、ＣＯＭ６４ドット×ＳＥＧ９６ドットの合計６１４４画素程度の表示容量から、ＣＯＭ９６ドット×ＳＥＧ１２０ドットの合計１１５２０画素程度への表示容量増大が求められている。これらの制御に必要な配線は、各ドット合計の２１６本である。これらの配線は全て接続部１４に集中されており、ＴＣＰ１７に接続されている。携帯電話の横幅は通常４０ｍｍ程度であり、これに使用される表ガラス１５の横幅は３２．５ｍｍ程度であり、これにより、接続部１４の幅は２７ｍｍ程度が割り当てられている。このとき、表示容量を増大させても携帯電話の横幅を変更させないとすれば、接続部１４の幅は２７ｍｍ程度のまま、配線数のみを増大させることとなる。前述のように、接続部１４には２１６本の配線が必要になるが、表ガラス１５のＣＯＭ電極端子１と裏ガラス１６のＣＯＭ電極端子１２との電気的接続を確実に行うため、接続部１３における金属メッキ付き樹脂ボール２１の数量を最低限確保することが必要となる。金属メッキ付き樹脂ボール２１の大きさを考慮することにより、実際には、表ガラスＣＯＭ電極端子１の幅５及び間隔８は、それぞれ０．１２ｍｍ及び０．１８ｍｍとしていた。これにより、接続部１４において、表ガラスＣＯＭ電極端子１の配線に必要なスペースを除いた部分にＳＥＧ電極端子４を全て配線させることとなる。すなわち、ＣＯＭ電極端子１及びＳＥＧ電極端子２の配線数をともに増大させ、かつ、表ガラス１５のＣＯＭ電極端子１と裏ガラス１６のＣＯＭ電極端子１２との電気的接続を確実に行うためには、ＳＥＧ電極端子２の幅７及び配線間隔９を狭くする必要があり、したがって、ＳＥＧ電極端子２の幅７及び間隔９は、それぞれ０．０５ｍｍ及び０．０７ｍｍ程度となり、ＣＯＭ電極端子１に比べて極端に細く狭いものとなっている。ＴＣＰ１７に形成されるＣＯＭ電極端子３及びＳＥＧ電極端子４は、表ガラスＣＯＭ電極端子１及びＳＥＧ電極端子２に合わせて形成される。この状態を図５に示す。

【０００４】異方性導電樹脂を用いた接続の手順は、図６に示すとおりである。まず、異方性導電樹脂２３を表ガラスＣＯＭ電極端子１及び表ガラスＳＥＧ電極端子２を覆うように乗せる（図６（ａ））。次に、ＴＣＰ１７を所定の位置に搭載し、ＴＣＰ１７の裏面（上方）から圧力をあまりかけずにヒートツール２５にて加熱する（図６（ｂ））。このとき、ヒートツール２５の熱がＴＣＰ１７のＣＯＭ電極端子３及びＳＥＧ電極端子４を通じて異方性導電樹脂２３に伝わり、異方性導電樹脂２３が流動性を持つ。その後、さらにヒートツール２５の加

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圧力を増加させて、異方性導電樹脂２３が各電極端子１，２，３，４のすき間を満たすようにする（図６（ｃ））。異方性導電樹脂２３を硬化させ、ヒートツール２５を外して冷却する（図６（ｄ））。

【０００５】

【発明が解決しようとする課題】ところが、表ガラスＳＥＧ電極端子２の間隔（ピッチ）９の変更に伴い、異方性導電樹脂２３を０．１４mmピッチ対応品から０．０６mmピッチ対応品に変更させる必要がある。これにより、樹脂の接続信頼性を確保するために樹脂の種類が変わり、従来の樹脂では起きなかった熱圧着時の気泡発生という不具合が生じた。この原因を調査したところ、ＴＣＰ１７におけるＣＯＭ電極端子３の間隔１０と、ＴＣＰ１７におけるＳＥＧ電極端子４の間隔１１とが不均一であることに起因していることが、判明した。

【０００６】気泡発生の概要は、次に示す通りである。ヒートツール２５で加熱する際、ＴＣＰ１７のＣＯＭ電極端子３及びＳＥＧ電極端子４の幅及び間隔１０，１１の差があまりに大きい場合、異方性導電樹脂２３への熱の伝わり方に偏りが生じる。これにより、加熱不足もしくは過熱による有機溶剤の減少が生じて異方性導電樹脂２３の流動性に不均一が生じ、この状態で圧力をかけると、十分に流動性を持たない部分が電極端子１，２，３，４のすき間を満たすことができず、気泡（図６の符号Ａｉｒ）が発生してしまっていた。

【０００７】本発明は、上記課題を解決するもので、異方性導電樹脂で熱圧着接続される電極部分における気泡発生を防止し、信頼性の高い、大容量表示の液晶表示装置を提供することを目的とする。

【０００８】

【課題を解決するための手段】上記課題を解決するために、本発明における請求項１記載の電極端子の接続構造は、広狭少なくとも２種類の幅の電極端子が形成された第１の基板を第２の基板に異方性導電樹脂で熱圧着する接続構造において、第２の基板の電極端子は第１の基板における最も狭い電極端子の幅とそれぞれ接続されるようほぼ同じ幅で形成され、第１の基板における広い幅の電極端子には、第２の基板の電極端子が複数本接続されることを特徴とする。

【０００９】この発明によれば、第２の基板の電極端子が第１の基板における狭い方の幅と同じ幅で形成されるため、熱圧着時に加わる圧力が各接続箇所で均一になり、各電極端子に挟まれる異方性導電樹脂の量にばらつきが少なくなる。これにより、異方性導電樹脂の量のばらつきによる気泡の発生が防止され、信頼性の高い接続構造が得られる。

【００１０】本発明の請求項２記載の電極端子の接続構造は、請求項１記載の発明を前提に、前記第２の基板に形成される電極端子の幅と間隔が全て均等であることを特徴とする。

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【００１１】この発明によれば、第２の基板に形成される電極端子の幅と間隔が全て均等であるため、請求項１記載の発明に比べて、各電極端子に挟まれる異方性導電樹脂の量にばらつきがさらに少なくなり、より効果的に液晶表示装置の気泡の発生を防ぐことができる。

【００１２】本発明の請求項３記載の液晶表示装置は、請求項１または請求項２記載の電極端子の接続構造を持ち、前記第１の基板は、液晶表示パネルの一方の基板であり、前記第２の基板は、テープキャリアパッケージであることを特徴とする。

【００１３】この発明によれば、請求項１または請求項２に示すように、信頼性の高い電極端子の接続構造を持つことにより、大容量表示の液晶表示装置のように電極端子の幅や間隔の広狭の差が大きい接続構造においても、高い信頼性を保つことができる。

【００１４】

【発明の実施の形態】以下に、本発明の実施の形態を図を使用して説明する。図１は、本実施の形態における液晶表示装置の表ガラスとＴＣＰの接続部近辺の図である。図２（ａ）は、液晶表示装置の上面図及び側面図、図２（ｂ）は、接続部近辺の側面図である。液晶表示装置には、個々の表示部に相当する透明電極が備えられており、透明電極は共通に制御されるコモン（ＣＯＭ）電極と、個々に制御されるセグメント（ＳＥＧ）電極とからなる。これらの電極は表ガラス１５上に配線され、表ガラス１５に形成された接続部１４に、それぞれＣＯＭ電極端子１、ＳＥＧ電極端子２が形成される。また、裏ガラス１６にもＣＯＭ電極端子１２が形成される。接続部１４近辺のＣＯＭ電極端子接続部１３において、表ガラスＣＯＭ電極端子１と裏ガラスＣＯＭ電極端子１２が、シール剤２２に組み込まれた金属メッキ付き樹脂ボール２１により、電気的に接続されている。ＴＣＰ１７は、ポリイミド樹脂フィルム２４に各透明電極の制御を行う駆動ドライバーＩＣを具備し、その裏面側にＣＯＭ電極端子３及びＳＥＧ電極端子４が形成され、それぞれ表ガラス１５のＣＯＭ電極端子１及びＳＥＧ電極端子２と接続部１４にて接続されている。接続部１４における接続は、通常、異方性導電樹脂（ＡＣＦ）２３を用いて熱圧着で行われる。接着後、液晶表示装置の狭額縁化のために、ＴＣＰ１７は折り曲げスリットＳにおいて裏面側に折り曲げられる。

【００１５】ところで、本実施の形態の液晶表示装置は、携帯電話に使用される液晶画面である。今後要望される表示容量は、ＣＯＭ９６ドット×ＳＥＧ１２０ドット程度であり、これらの制御に必要な配線は、各ドット合計の２１６本である。これらの配線は全て接続部１４に集中されており、ＴＣＰ１７に接続されている。携帯電話の横幅は通常４０mm程度であり、これに使用される表ガラス１５の横幅は３２．５mm程度であり、これにより、接続部１４の幅は２７mm程度が割り当てられ

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ている。このとき、表示容量を増大させても携帯電話の横幅を変更しないとすれば、接続部１４の幅は２７mm程度のまま、配線数のみを増大させることとなる。前記のように、接続部１４には２１６本の配線が必要になるが、表ガラス１５のCOM電極端子１と裏ガラス１６のCOM電極端子１２との電気的接続を確実に行うため、接続部１３における金属メッキ付き樹脂ボール２１の数量を最低限確保することが必要となる。金属メッキ付き樹脂ボール２１の大きさを考慮することにより、まず、表ガラスCOM電極端子１の幅６とおおよその間隔８を設定する（間隔８の詳細な設定は後に詳述する）。これにより、接続部１４において、表ガラスCOM電極端子１の配線に必要なスペースを除いた部分にSEG電極端子４を全て配線させることとなる。すなわち、COM電極端子１及びSEG電極端子２の配線数をともに増大させ、かつ、表ガラス１５のCOM電極端子１と裏ガラス１６のCOM電極端子１２との電気的接続を確実に行うためには、SEG電極端子２の幅７及び配線間隔９を狭くする必要がある。

【００１６】TCP１７に形成されるSEG電極端子４は、表ガラスSEG電極端子２の幅７及び間隔９に合わせて、設定され、TCP１７に形成されるCOM電極端子３も、SEG電極端子４と同様の間隔１０及び幅で形成される。これにより、TCP１７には電極端子が均一な間隔１０、１１及び幅で形成されている。

【００１７】ここで、表ガラス１５のCOM電極端子１は、接続部１４にかかる部分において、TCP１７のCOM電極端子３の間隔１０にあわせて、TCP１７のCOM電極端子３が２本重なるように幅５及び間隔８が設定される。すなわち、接続部１４における幅５は、COM電極端子接続部１３における幅６と異なり、本実施の形態においては、幅５はTCP１７のCOM電極端子３が２本重なるように幅６より若干広く形成され、また、表ガラス１５のCOM電極端子１の間隔８はTCP１７のCOM電極端子３の間隔１０の２倍となるように形成されることにより、表ガラス１５のCOM電極端子１には、TCP１７のCOM電極端子３が２本ずつ接続されることとなる。これにより、表ガラス１５のCOM電極端子１の幅５及び間隔８は、それぞれ０．０９mm及び０．１４mmと設定され、表ガラス１５のSEG電極端子２の幅７及び間隔９は、それぞれ０．０５mm及び０．０７mmと設定され、TCP１７のCOM電極端子３及びSEG電極端子４の幅及び間隔１１は、それぞれ０．０３５mm及び０．０７mmと設定される。なお、表ガラス１５のCOM電極端子１に接続される２本のCOM電極端子３のうち、１本は電気信号のやりとりを行わないダミー端子としてもよい。

【００１８】このような構成を持つ表ガラス１５及びTCP１７の接着は、図３に示すように、接続部１４に異方性導電樹脂２３を貼付し、熱圧着によって行う。熱圧着の工程の流れは、従来と同様である。異方性導電樹脂２３を表ガラス１５の電極端子１，２に乗せ、TCP１７を所定の位置に搭載し、TCP１７の裏面（上方）から圧力をあまりかけずにヒートツール２５にて加熱する（図３（ｂ））とき、TCP１７に形成された電極端子３，４は均一な幅及び間隔１０，１１であり、また、表ガラスSEG電極端子２は均一な間隔９及び幅７であり、表ガラス１５に形成されたCOM電極端子１もそれらの間隔１１と幅７を抱合するように形成されているため、ヒートツール２５の熱がいずれの電極端子１，２，３，４についても均一に伝わり、異方性導電樹脂２３の流動性が均一となる。これにより、異方性導電樹脂２３が同時に各電極端子１，２，３，４のすき間を満たし（図３（ｃ））、従来（図６（ｃ），（ｄ））のように気泡が残ることがない。また、熱圧着されるとき、接続部１４における各電極端子には均一に圧力がかかる。これにより、異方性導電樹脂２３の量に偏りが生じないため、さらに強力に気泡が発生することを防ぐ。

【００１９】以上、本発明を液晶表示装置に適用する場合について説明したが、本発明はこれに限らず、二つの基板を接合する構成に広く適用可能である。

【００２０】

【発明の効果】本発明の電極端子の接続構造は、異方性導電樹脂を用いた２枚の基板の接続において、第１の基板に形成された少なくとも２種類の幅及び間隔を持つ電極端子のうち、最も狭い幅の電極端子の幅及び間隔に合わせて第２の基板の電極端子を形成し、広い幅の電極端子に第２の基板の電極端子が複数本接続されるため、各電極端子の接続時における異方性導電樹脂の流動性及び量にばらつきがなくなり、気泡の発生が防止され、信頼性の高い接続構造となる。また、この電極端子の接続構造を液晶表示装置のガラス基板とTCPの接続に用いることにより、大容量表示の液晶表示装置においても高い信頼性を保つことが可能である。

【００２１】

【図面の簡単な説明】

【図１】本実施の形態における液晶表示装置の表ガラスとTCPの接続部近辺の図

【図２】（ａ）液晶表示装置の上面図及び側面図（ｂ）接続部近辺の側面図

【図３】本実施の形態における液晶表示装置の表ガラスとTCPの接続工程を示す図

【図４】従来の液晶表示装置の表ガラスとTCPの接続部近辺の図

【図５】従来の大容量液晶表示装置の表ガラスとTCPの接続部近辺の図

【図６】従来の液晶表示装置の表ガラスとTCPの接続工程を示す図

【符号の説明】

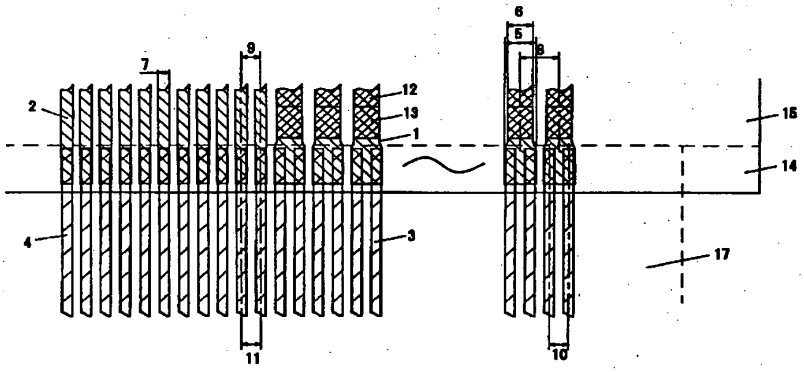
１　表ガラスのCOM電極端子、

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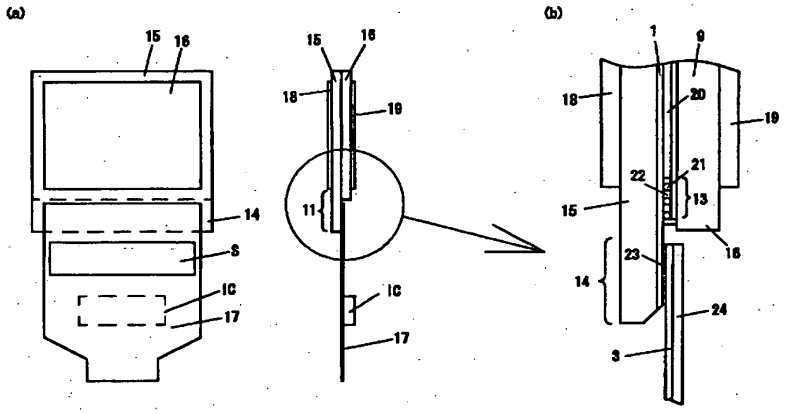
2　表ガラスのＳＥＧ電極端子、
3　ＴＣＰのＣＯＭ電極端子、
4　ＴＣＰのＳＥＧ電極端子、
5　表ガラスのＣＯＭ電極端子の幅、
6　ＣＯＭ電極端子接続部の幅、
7　表ガラスのＳＥＧ電極端子の幅、
8　表ガラスのＣＯＭ電極端子の間隔、
9　表ガラスのＳＥＧ電極端子の間隔、
１０　ＴＣＰのＣＯＭ電極端子の間隔、
１１　ＴＣＰのＳＥＧ電極端子の間隔、
１２　裏ガラスのＣＯＭ電極端子、
１３　表ガラスと裏ガラスのＣＯＭ電極端子接続部、

１４　表ガラスとＴＣＰの接続部、
１５　表ガラス、
１６　裏ガラス、
１７　ＴＣＰ、
１８　表偏光板、
１９　裏偏光板、
２０　液晶組成物、
２１　金属メッキ付き樹脂ボール、
２２　シール剤、
２３　異方性導電樹脂（ＡＣＦ）、
２４　ポリイミド樹脂フィルム
２５　ヒートツール

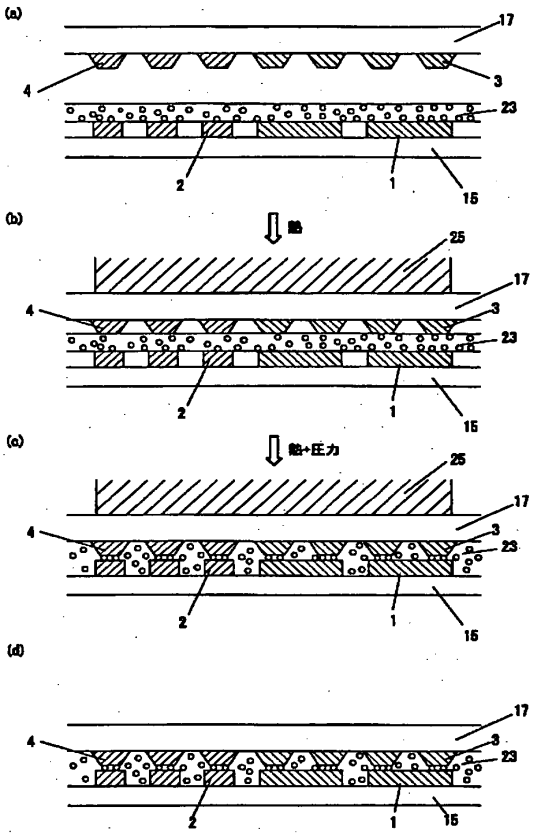
【図１】



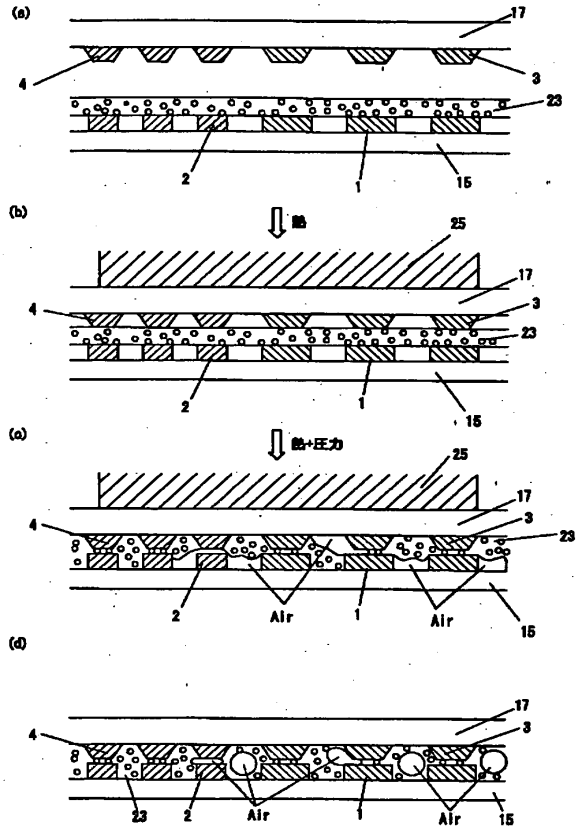
【図２】



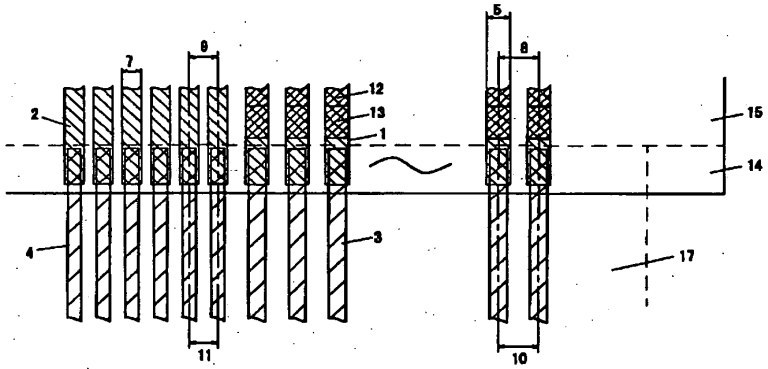
【図３】


(a)
(b)
(c)
(d)
熱
熱+圧力
17
3
4
23
2
1
15
25

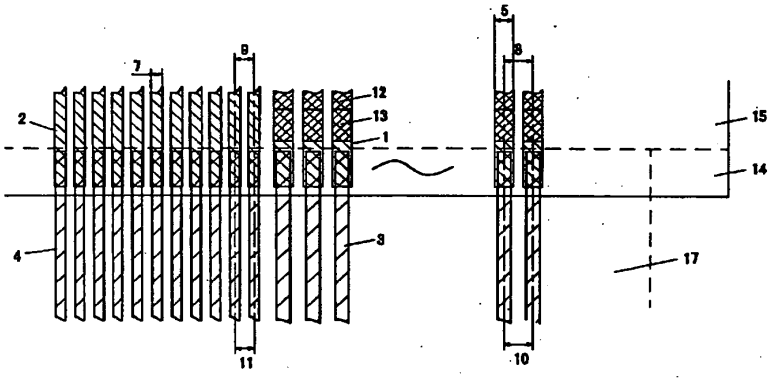
【図６】


(a)
(b)
(c)
(d)
熱
熱+圧力
17
3
4
23
2
1
15
25
Air

【図４】


5
6
7
8
2
12
13
1
15
14
4
3
17
11
10

【図５】



フロントページの続き

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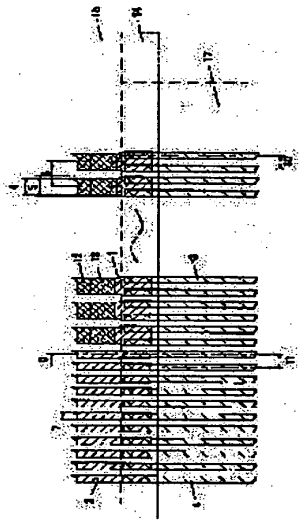
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HIGUCHI KENJI

(54) CONNECTION STRUCTURE OF ELECTRODE TERMINAL AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a liquid crystal display device which prevents generation of bubbles in an electrode which is connected by a thermal contact-bonding with an anisotropic conductive resin, and has high reliability and a large capacity display.
SOLUTION: In a connection structure, a first substrate 15 formed with electrode terminals 1, 2 having at least two kinds of wide and narrow widths 5, 7 is thermally contact-bonded to a second substrate 17 with an anisotropic conductive resin 23. Electrode terminals 3, 4 of the second substrate 17 are formed with a substantially same width so as to connect with the narrowest width 7 in the first substrate 15, and a plurality of electrode terminals 3 of the second substrate 17 are connected to the electrode terminal 1 having a wide width in the first substrate 15.



LEGAL STATUS

[Date of request for examination]

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[Date of final disposal for application]

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CLAIMS

[Claim(s)]
[Claim 1] In the connection structure which carries out thermocompression bonding of the 1st substrate with which the electrode terminal of two kinds of width of face was formed even if few to the 2nd substrate by anisotropy electric conduction resin extensive ** -- The electrode terminal of the 2nd substrate is the connection structure of the electrode terminal characterized by being formed by the almost same width of face so that it may connect with the width of face of the narrower one in the 1st substrate, respectively, and connecting two or more electrode terminals of the 2nd substrate to the electrode terminal of the large width of face in the 1st substrate.
[Claim 2] Connection structure of the electrode terminal according to claim 1 characterized by all spacing of the electrode terminal formed in said 2nd substrate being equal.
[Claim 3] It is a liquid crystal display with the connection structure of the electrode terminal according to claim 1 or 2 which said 1st substrate is one substrate of a liquid crystal display panel, and is characterized by said 2nd substrate being a tape career package.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the connection structure of an electrode terminal where anisotropy electric conduction resin was used, and the connection structure of the electrode terminal in the glass substrate and tape career package which are especially used for a liquid crystal display.
[0002]
[Description of the Prior Art] By the spread of cellular phones in recent years, the further mass display and the high-reliability over the liquid crystal display used for a screen are searched for. Below, the conventional liquid crystal display is explained using drawing. The plan of a liquid crystal display and a

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side elevation, and drawing 2 (b) of drawing 2 (a) are the side elevations of the connection neighborhood. Drawing 4 is the table glass of the conventional liquid crystal display, and drawing of the connection neighborhood of TCP. The liquid crystal display is equipped with the transparent electrode equivalent to each display, and a transparent electrode consists of a common (below common: "COM") electrode controlled in common and a segment (below segment: "SEG") electrode controlled separately. These electrodes are wired on table glass 15, and the COM electrode terminal 1 and the SEG electrode terminal 2 are formed in the connection 14 formed in table glass 15, respectively. Moreover, the COM electrode terminal 12 is formed also in flesh-side glass 16. In the connection 13 of the COM electrode terminal 1 of the connection 14 neighborhood, the table glass COM electrode terminal 1 and the flesh-side glass COM electrode terminal 12 are electrically connected by the resin ball 21 with metal plating built into the sealing compound 22. The actuation driver IC which controls each transparent electrode on the polyimide resin film 24 was provided, the COM electrode terminal 3 and the SEG electrode terminal 4 were formed in the rear-face side, and TCP17 is connected with the COM electrode terminal 1 of table glass 15, and the SEG electrode terminal 2 in the connection 14, respectively. Connection in a connection 14 is usually made by thermocompression bonding using the anisotropy electric conduction resin (anisotropic conductive film:ACF) 23 with which the conductive particle was mixed into adhesives. TCP17 is bent in the bending slit S after adhesion at a rear-face side for narrow-picture-frame-izing of a liquid crystal display.

[0003] In the latest cellular phone, the needs of ** increase literally not only in mere voice communication, and the mass liquid crystal display which can display much text on one screen is called for. Specifically, the display capacity buildup to about a total of 11520 pixels of 120 dot of COM96 dot xSEG(s) from the display capacity of about a total of 6144 pixels of 96 dot of COM64 dot xSEG(s) is searched for. Wiring required for these control is 216 of each dot sum total. It is concentrated on the connection 14 and all of these wiring are connected to TCP17. The breadth of a cellular phone is usually about 40mm, the breadth of the table glass 15 used for this is about 32.5mm, and, thereby, as for the width of face of a connection 14, about 27mm is assigned. Even if it increases display capacity, supposing it does not make the breadth of a cellular phone change at this time, the width of face of a connection 14 makes only the number of wiring increase with about 27mm. As mentioned above, although wiring of 216 is needed for a connection 14, in order to perform certainly electrical installation of the COM electrode terminal 1 of table glass 15, and the COM electrode terminal 12 of flesh-side glass 16, it is necessary to secure the quantity of the resin ball 21 with metal plating in a connection 13 at worst. By taking into consideration the magnitude of the resin ball 21 with metal plating, the width of face 5 and spacing 8 of the table glass COM electrode terminal 1 were actually set to 0.12mm and 0.18mm, respectively. Thereby, the SEG electrode terminal 4 is made to wire altogether the part except a tooth space required for wiring of the table glass COM electrode terminal 1 in a connection 14. Namely, both the numbers of wiring of the COM electrode terminal 1 and the SEG electrode terminal 2 are increased. and in order to perform certainly electrical installation of the COM electrode terminal 1 of table glass 15, and the COM electrode terminal 12 of flesh-side glass 16 It is necessary to narrow the width of face 7 and the wiring spacing 9 of the SEG electrode terminal 2, therefore the width of face 7 and spacing 9 of the SEG electrode terminal 2 are set to 0.05mm and about 0.07mm, respectively, and have become an extremely thin narrow thing compared with the COM electrode terminal 1. The COM electrode terminal 3 and the SEG electrode terminal 4 which are formed in TCP17 are formed according to the table glass COM electrode terminal 1 and the SEG electrode terminal 2. This condition is shown in drawing 5 R> 5.

[0004] The procedure of connection using anisotropy electric conduction resin is as being shown in drawing 6 R> 6. First, anisotropy electric conduction resin 23 is put so that the table glass COM electrode terminal 1 and the table glass SEG electrode terminal 2 may be covered (drawing 6 (a)). Next, TCP17 is carried in a position and it heats with the heat tool 25, without seldom putting a pressure from the rear face (upper part) of TCP17 (drawing 6 (b)). At this time, propagation and anisotropy electric

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conduction resin 23 have [the heat of the heat tool 25] a fluidity in anisotropy electric conduction resin 23 through the COM electrode terminal 3 and the SEG electrode terminal 4 of TCP17. Then, the welding pressure of the heat tool 25 is made to increase further, and it is made for anisotropy electric conduction resin 23 to fill the crevice between each electrode terminals 1, 2, 3, and 4 (drawing 6 (c)). Anisotropy electric conduction resin 23 is stiffened, and the heat tool 25 is removed and it cools (drawing 6 (d)).

[0005]

[Problem(s) to be Solved by the Invention] However, it is necessary to make anisotropy electric conduction resin 23 change into the elegance corresponding to 0.06mm pitch from the elegance corresponding to 0.14mm pitch with modification of the spacing (pitch) 9 of the table glass SEG electrode terminal 2. By this, in order to secure the connection dependability of resin, the class of resin changed, and by conventional resin, the nonconformity of gassing at the time of the thermocompression bonding which did not occur arose. When this cause was investigated, it became clear that it originated in the spacing 10 of the COM electrode terminal 3 in TCP17 and the spacing 11 of the SEG electrode terminal 4 in TCP17 being uneven.

[0006] The outline of gassing is as being shown below. In case it heats with the heat tool 25, when the width of face of the COM electrode terminal 3 of TCP17 and the SEG electrode terminal 4 and the difference of spacing 10 and 11 are too much large, a bias arises in how to transmit the heat to anisotropy electric conduction resin 23. When reduction of the organic solvent by underheat or overheating arose, the ununiformity arose to the fluidity of anisotropy electric conduction resin 23 by this and the pressure was put in this condition, the part which does not fully have a fluidity could not fill the crevice between electrode terminals 1, 2, 3, and 4, but air bubbles (sign Air of drawing 6) were generated.

[0007] This invention solves the above-mentioned technical problem, prevents gassing in the electrode section by which thermocompression bonding connection is made by anisotropy electric conduction resin, and aims at offering the reliable liquid crystal display of a mass display.

[0008]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the connection structure of the electrode terminal according to claim 1 in this invention In the connection structure which carries out thermocompression bonding of the 1st substrate with which the electrode terminal of two kinds of width of face was formed even if few to the 2nd substrate by anisotropy electric conduction resin extensive ** -- The electrode terminal of the 2nd substrate is formed by the almost same width of face so that it may connect with the width of face of the narrowest electrode terminal in the 1st substrate, respectively, and it is characterized by connecting two or more electrode terminals of the 2nd substrate to the electrode terminal of the large width of face in the 1st substrate.

[0009] Since the electrode terminal of the 2nd substrate is formed by the same width of face as the width of face of the narrower one in the 1st substrate according to this invention, the pressure added at the time of thermocompression bonding becomes homogeneity in each connection place, and dispersion decreases in the amount of the anisotropy electric conduction resin inserted into each electrode terminal. Thereby, generating of the air bubbles by dispersion in the amount of anisotropy electric conduction resin is prevented, and reliable connection structure is acquired.

[0010] Connection structure of the electrode terminal of this invention according to claim 2 is characterized by all of the width of face and spacing of the electrode terminal formed in said 2nd substrate being equal a premise [invention according to claim 1].

[0011] According to this invention, dispersion decreases further in the amount of the anisotropy electric conduction resin with which the width of face and spacing of the electrode terminal formed in the 2nd substrate are altogether inserted into each electrode terminal compared with invention according to claim 1 since it is equal, and generating of the air bubbles of a liquid crystal display can be prevented more effectively.

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[0012] The liquid crystal display of this invention according to claim 3 has the connection structure of an electrode terminal according to claim 1 or 2, said 1st substrate is one substrate of a liquid crystal display panel, and said 2nd substrate is characterized by being a tape career package.
[0013] As shown in claim 1 or claim 2, according to this invention, the width of face of an electrode terminal and the difference of extensive ** of spacing can maintain high dependability also in large connection structure by having the connection structure of a reliable electrode terminal like the liquid crystal display of a mass display.
[0014]
[Embodiment of the Invention] Below, the gestalt of operation of this invention is explained using drawing. Drawing 1 is the table glass of the liquid crystal display in the gestalt of this operation, and drawing of the connection neighborhood of TCP. The plan of a liquid crystal display and a side elevation, and drawing 2 (b) of drawing 2 (a) are the side elevations of the connection neighborhood. The liquid crystal display is equipped with the transparent electrode equivalent to each display, and a transparent electrode consists of a common (COM) electrode controlled in common and a segment (SEG) electrode controlled separately. These electrodes are wired on table glass 15, and the COM electrode terminal 1 and the SEG electrode terminal 2 are formed in the connection 14 formed in table glass 15, respectively. Moreover, the COM electrode terminal 12 is formed also in flesh-side glass 16. In the COM electrode terminal strapping section 13 of the connection 14 neighborhood, the table glass COM electrode terminal 1 and the flesh-side glass COM electrode terminal 12 are electrically connected by the resin ball 21 with metal plating built into the sealing compound 22. The actuation driver IC which controls each transparent electrode on the polyimide resin film 24 is provided, the COM electrode terminal 3 and the SEG electrode terminal 4 are formed in the rear-face side, and TCP17 is connected with the COM electrode terminal 1 of table glass 15, and the SEG electrode terminal 2 in the connection 14, respectively. Connection in a connection 14 is usually made by thermocompression bonding using anisotropy electric conduction resin (ACF) 23. TCP17 is bent in the bending slit S after adhesion at a rear-face side for narrow-picture-frame-izing of a liquid crystal display.
[0015] By the way, the liquid crystal display of the gestalt of this operation is a liquid crystal screen used for a cellular phone. The display capacity demanded from now on is about 120 dot of COM96 dot xSEG(s), and wiring required for these control is 216 of each dot sum total. It is concentrated on the connection 14 and all of these wiring are connected to TCP17. The breadth of a cellular phone is usually about 40mm, the breadth of the table glass 15 used for this is about 32.5mm, and, thereby, as for the width of face of a connection 14, about 27mm is assigned. Even if it increases display capacity, supposing it does not change the breadth of a cellular phone at this time, the width of face of a connection 14 makes only the number of wiring increase with about 27mm. As mentioned above, although wiring of 216 is needed for a connection 14, in order to perform certainly electrical installation of the COM electrode terminal 1 of table glass 15, and the COM electrode terminal 12 of flesh-side glass 16, it is necessary to secure the quantity of the resin ball 21 with metal plating in a connection 13 at worst. By taking into consideration the magnitude of the resin ball 21 with metal plating, the width of face 6 of the table glass COM electrode terminal 1 and the near spacing 8 are set up first (detailed setting out of spacing 8 is explained in full detail behind). Thereby, the SEG electrode terminal 4 is made to wire altogether the part except a tooth space required for wiring of the table glass COM electrode terminal 1 in a connection 14. That is, in order to increase both the numbers of wiring of the COM electrode terminal 1 and the SEG electrode terminal 2 and to perform certainly electrical installation of the COM electrode terminal 1 of table glass 15, and the COM electrode terminal 12 of flesh-side glass 16, it is necessary to narrow the width of face 7 and the wiring spacing 9 of the SEG electrode terminal 2.
[0016] The SEG electrode terminal 4 formed in TCP17 is set up according to the width of face 7 and spacing 9 of the table glass SEG electrode terminal 2, and the COM electrode terminal 3 formed in TCP17 is also formed by the same spacing 10 and width of face as the SEG electrode terminal 4.

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Thereby, the electrode terminal is formed in TCP17 by uniform spacing 10 and 11 and width of face.
[0017] Here, in the part which the COM electrode terminal 1 of table glass 15 requires for a connection 14, in accordance with the spacing 10 of the COM electrode terminal 3 of TCP17, width of face 5 and spacing 8 are set up so that two COM electrode terminals 3 of TCP17 may lap. Namely, unlike the width of face 6 in the COM electrode terminal strapping section 13, the width of face 5 in a connection 14 is set in the gestalt of this operation. By being formed so that width of face 5 may be widely formed a little from width of face 6 so that two COM electrode terminals 3 of TCP17 may lap, and the spacing 8 of the COM electrode terminal 1 of table glass 15 may become twice the spacing 10 of the COM electrode terminal 3 of TCP17 Two COM electrode terminals 3 of TCP17 will be connected to the COM electrode terminal 1 of table glass 15 at a time. Thereby, the width of face 5 and spacing 8 of the COM electrode terminal 1 of table glass 15 are set up with 0.09mm and 0.14mm, respectively, the width of face 7 and spacing 9 of the SEG electrode terminal 2 of table glass 15 are set up with 0.05mm and 0.07mm, respectively, and the width of face and spacing 11 of the COM electrode terminal 3 of TCP17 and the SEG electrode terminal 4 are set up with 0.035mm and 0.07mm, respectively. In addition, one of two COM electrode terminals 3 connected to the COM electrode terminal 1 of table glass 15 is good also as a dummy terminal which does not exchange an electrical signal.
[0018] As shown in drawing 3 , adhesion of table glass 15 and TCP17 with such a configuration sticks anisotropy electric conduction resin 23 on a connection 14, and thermocompression bonding performs it. The flow of the process of thermocompression bonding is the same as usual. When heating with the heat tool 25, without putting anisotropy electric conduction resin 23 on the electrode terminals 1 and 2 of table glass 15, carrying TCP17 in a position, and seldom putting a pressure from the rear face (upper part) of TCP17 (drawing 3 (b)), The electrode terminals 3 and 4 formed in TCP17 are uniform width of face and spacing 10 and 11. Moreover, since it is formed so that the COM electrode terminal 1 which the table glass SEG electrode terminals 2 are the uniform spacing 9 and width of face 7, and was formed in table glass 15 may also carry out conjugation of those spacing 11 and width of face 7, The fluidity of propagation and anisotropy electric conduction resin 23 serves as [the heat of the heat tool 25] homogeneity also about which electrode terminals 1, 2, 3, and 4 at homogeneity. Thereby, anisotropy electric conduction resin 23 fills the crevice between each electrode terminals 1, 2, 3, and 4 simultaneously (drawing 3 (c)), and air bubbles do not remain like before (drawing 6 (c), (d)). Moreover, when thermocompression bonding is carried out, a pressure is applied to homogeneity at each electrode terminal in a connection 14. Thereby, since a bias does not arise in the amount of anisotropy electric conduction resin 23, it prevents generating air bubbles still more powerfully.
[0019] As mentioned above, although the case where this invention was applied to a liquid crystal display was explained, this invention is widely applicable to the configuration which joins not only this but two substrates.
[0020]
[Effect of the Invention] In connection of two substrates with which anisotropy electric conduction resin was used for the connection structure of the electrode terminal of this invention The inside of an electrode terminal with at least two kinds of width of face and spacing which were formed in the 1st substrate, Since the electrode terminal of the 2nd substrate is formed according to the width of face and spacing of an electrode terminal of the narrowest width of face and two or more electrode terminals of the 2nd substrate are connected to the electrode terminal of large width of face, Dispersion is lost in the fluidity of anisotropy electric conduction resin and amount at the time of connection of each electrode terminal, generating of air bubbles is prevented, and it becomes reliable connection structure. Moreover, it is possible by using the connection structure of this electrode terminal for the glass substrate of a liquid crystal display, and connection of TCP to maintain high dependability also in the liquid crystal display of a mass display.
[0021]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Table glass of the liquid crystal display in the gestalt of this operation, and drawing of the connection neighborhood of TCP
[Drawing 2] (a) The plan of a liquid crystal display, and the side elevation of the (side elevation b) connection neighborhood
[Drawing 3] Drawing showing the connection process of the table glass of a liquid crystal display, and TCP in the gestalt of this operation
[Drawing 4] Table glass of the conventional liquid crystal display, and drawing of the connection neighborhood of TCP
[Drawing 5] Table glass of the conventional mass liquid crystal display, and drawing of the connection neighborhood of TCP
[Drawing 6] Drawing showing the connection process of the table glass of the conventional liquid crystal display, and TCP
[Description of Notations]
1 COM Electrode Terminal of Table Glass,
2 SEG Electrode Terminal of Table Glass,
3 COM Electrode Terminal of TCP,
4 SEG Electrode Terminal of TCP,
5 Width of Face of COM Electrode Terminal of Table Glass,
6 Width of Face of COM Electrode Terminal Strapping Section,
7 Width of Face of SEG Electrode Terminal of Table Glass,
8 Spacing of COM Electrode Terminal of Table Glass,
9 Spacing of SEG Electrode Terminal of Table Glass,
10 Spacing of COM Electrode Terminal of TCP,
11 Spacing of SEG Electrode Terminal of TCP,
12 COM Electrode Terminal of Flesh-Side Glass,
13 COM Electrode Terminal Strapping Section of Table Glass and Flesh-Side Glass,
14 Connection of Table Glass and TCP,
15 Table Glass,
16 Flesh-Side Glass,
17 TCP,
18 Table Polarizing Plate,
19 Flesh-Side Polarizing Plate,

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20 Liquid Crystal Constituent,
21 Resin Ball with Metal Plating,
22 Sealing Compound,
23 Anisotropy Electric Conduction Resin (ACF),
24 Polyimide Resin Film
25 Heat Tool

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	1/1368		1/1368		５Ｅ３４４

審査請求　未請求　請求項の数12　ＯＬ　（全 14 頁）　最終頁に続く

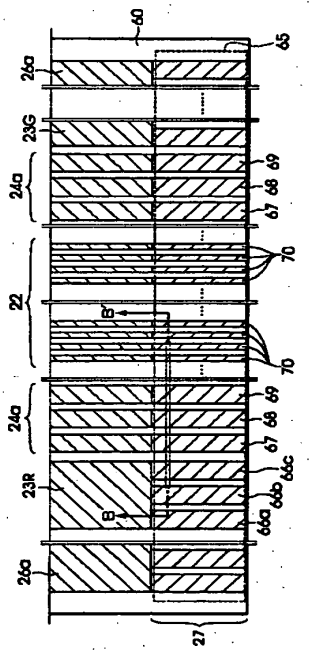
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最終頁に続く

(54)【発明の名称】　電気光学装置及び電子機器

(57)【要約】
【課題】　表示基板と中継基板との圧着条件を固着部全体に亘って同一にすることにより、固着部における電気的抵抗の不均一性を解消することができるとともに、コントラストの低下等の表示上の不具合を生ずることがない電気光学装置、及び当該電気光学装置を備える電子機器を提供する。
【解決手段】　複数の発光素子と、走査線駆動回路用制御信号配線２４ａ等の信号線を介して供給される信号に応じて発光用電源配線２３Ｒ等の電源線を介して供給される電流を発光素子に供給するスイッチング素子とが形成された表示基板を備える電気光学装置であって、発光用電源配線２３Ｒ等の電源線は走査線駆動回路用制御信号配線２４ａ等の信号線より幅広に形成されており、発光用電源配線２３Ｒ等の電源線には、外部接続端子６６ａ，６６ｂ，６６ｃ等の複数の外部接続端子が設けられている。



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【特許請求の範囲】

【請求項１】　第１外部接続端子に接続してなる第１配線と、当該第１配線の幅より広い第２配線とが少なくとも形成された電気光学装置において、

前記第２配線に対して複数の第２外部接続端子が設けられていることを特徴とする電気光学装置。

【請求項２】　前記第１外部接続端子及び前記第２外部接続端子には、凸部が形成されていることを特徴とする請求項１記載の電気光学装置。

【請求項３】　前記第１外部接続端子及び前記第２外部接続端子の表面には複数の凹部が形成されていることを特徴とする請求項１又は請求項２記載の電気光学装置。

【請求項４】　前記第２外部接続端子の幅がほぼ等しいことを特徴とする請求項１から請求項３の何れか一項に記載の電気光学装置。

【請求項５】　前記第１配線と同程度の幅を有する第１中継配線と、前記第２配線と同程度の幅を有する第２中継配線とが形成され、

前記第１外部接続端子を介して前記第１配線と前記第１中継配線とが電気的に接続され、前記第２外部接続端子を介して前記第２配線と前記第２中継配線とが電気的に接続された中継基板を有することを特徴とする請求項１から請求項４の何れか一項に記載の電気光学装置。

【請求項６】　複数の発光素子と、信号線を介して供給される信号に応じて電源線を介して供給される電流を各前記発光素子に供給するスイッチング素子とが形成された電気光学装置において、

前記電源線の幅は前記信号線の幅より広く形成されており、前記電源線に対して複数の第１外部接続端子が設けられていることを特徴とする電気光学装置。

【請求項７】　前記第１外部接続端子及び前記信号線に対して設けられる第２外部接続端子には、凸部が形成されていることを特徴とする請求項６記載の電気光学装置。

【請求項８】　前記第１外部接続端子及び前記第２外部接続端子の表面には複数の凹部が形成されていることを特徴とする請求項６又は請求項７記載の電気光学装置。

【請求項９】　前記第２外部接続端子の幅がほぼ等しいことを特徴とする請求項６から請求項８の何れか一項に記載の電気光学装置。

【請求項１０】　前記信号線と同程度の幅を有する第１中継配線と、前記電源線と同程度の幅を有する第２中継配線とが形成され、

前記第１外部接続端子を介して前記信号線と前記第１中継配線とが電気的に接続され、前記第２外部接続端子を介して前記電源線と前記第２中継配線とが電気的に接続された中継基板を有することを特徴とする請求項６から請求項９の何れか一項に記載の電気光学装置。

【請求項１１】　前記第１外部接続端子及び前記第１中継配線、並びに、前記第２外部接続端子及び前記第２中

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継配線が異方性導電膜により固着されていることを特徴とする請求項１０記載の電気光学装置。

【請求項１２】　請求項１から請求項１１の何れか一項に記載の電気光学装置を備えることを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、電気光学装置及び電子機器に係り、特に有機エレクトロルミネッセンス材料を備えた電気光学装置及び当該電気光学装置を備える電子機器に関する。

【０００２】

【従来の技術】近年、画素電極（陽極）及び陰極の間に、有機蛍光材料等の発光材料からなる発光素子が挟持された構造のカラー電気光学装置、特に発光材料として有機エレクトロルミネッセンス（有機ＥＬ）材料を用いた有機ＥＬ表示装置の開発が行われている。以下、従来の電気光学装置（有機ＥＬ表示装置）について簡単に説明する。

【０００３】図１１は、従来の電気光学装置の配線構造を示す図である。図１１に示すように、従来の電気光学装置は、複数の走査線９０１と、走査線９０１に対して交差する方向に延びる複数の信号線９０２と、信号線９０２に並行して延びる複数の発光用電源配線９０３とがそれぞれ配線され、走査線９０１と信号線９０２との各交点毎に、画素領域Ａが設けられている。各信号線９０２は、シフトレジスタ、レベルシフタ、ビデオライン、及びアナログスイッチを備えるデータ側駆動回路９０４に接続されており、各走査線９０１は、シフトレジスタ及びレベルシフタを備える走査側駆動回路９０５に接続されている。

【０００４】また、画素領域Ａの各々には、走査線９０１を介して走査信号がゲート電極に供給されるスイッチング薄膜トランジスタ９１３と、このスイッチング薄膜トランジスタ９１３を介して信号線９０２から供給される画像信号を保持する保持容量Ｃａｐと、保持容量Ｃａｐによって保持された画像信号がゲート電極に供給されるカレント薄膜トランジスタ９１４と、このカレント薄膜トランジスタ９１４を介して発光用電源配線９０３に電気的に接続されたときに発光用電源配線９０３から駆動電流が流れ込む画素電極９１１と、この画素電極９１１と陰極９１２との間に挟み込まれる発光層９１０とが設けられている。陰極９１２は、陰極用電源回路９３１に接続されている。

【０００５】上記の発光層９１０には、赤色に発光する発光層９１０Ｒ、緑色に発光する発光層９１０Ｇ、青色に発光する発光層９１０Ｂの３種の発光素子が含まれ、各発光層９１０Ｒ，９１０Ｇ，９１０Ｂがストライプ配置されている。そして、カレント薄膜トランジスタ９１４を介して各発光層９１０Ｒ，９１０Ｇ，９１０Ｂに接

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続される発光用電源配線９０３Ｒ，９０３Ｇ，９０３Ｂは、それぞれ発光用電源回路９３２に接続されている。各色毎に発光用電源配線が配線されているのは、発光層９１０の駆動電位が各色毎に異なるためである。

【０００６】以上の構成において、走査線９０１に走査信号が供給されてスイッチング薄膜トランジスタ９１３がオン状態になると、そのときに信号線９０２に供給されている画像信号に応じた電荷が保持容量Ｃａｐに保持される。この保持容量Ｃａｐに保持された電荷の量に応じて、カレント薄膜トランジスタ９１４のオン・オフ状態が決まる。そして、カレント薄膜トランジスタ９１４を介して発光用電源配線９０３Ｒ，９０３Ｇ，９０３Ｂから画素電極９１１に電流が流れ、更に発光層９１０を介して陰極９１２に駆動電流が流れる。このとき、発光層９１０を流れた電流量に応じた量の発光が発光層９１０から得られる。

【０００７】

【発明が解決しようとする課題】ところで、図１１に示した電気光学装置は、走査線９０１、信号線９０２、陰極９１２、発光用電源配線９０３（９０３Ｒ，９０３Ｇ，９０３Ｂ）、走査側駆動回路９０５、及び画素領域Ａがガラス等の透明基板（表示基板）上に形成され、陰極用電源回路９３１、発光用電源回路９３２、及びデータ側駆動回路９０４等の回路が可撓性のあるフレキシブル基板（中継基板）上に配置された構成とされることがある。

【０００８】かかる構成の場合には、基板に対してフレキシブル基板を固着させ、走査線９０１、信号線９０２、陰極９１２、及び発光用電源配線９０３とフレキシブル基板上に形成された回路とを電気的に導通させる必要がある。基板とフレキシブル基板との固着及び電気的な接続は、基板とフレキシブル基板との間に導電粒子を含む異方性導電膜を配置し、フレキシブル基板を基板に対して圧着させることにより行われる。

【０００９】上述した電気光学装置に設けられる発光層９１０を安定して発光させるためには、発光用電源配線９０３から画素電極９１１に印加する駆動電流の電位変動をできるだけ少なくすることが要求される。特に、図１１に示した電気光学装置は電流駆動型の電気光学装置であり、表示ムラ及びコントラスト低下等の表示上の不具合を防止するためには、陰極９１２及び発光用電源配線９０３の配線抵抗等による電圧降下を極力抑える必要がある。このため、陰極９１２及び発光用電源配線９０３は、走査線９０１及び信号線９０２よりも幅広に形成されている。

【００１０】基板とフレキシブル基板と固着させる際には、主として圧着部において生ずる電気的抵抗の均一化を図るために、固着部の全面に亘って圧着条件を同一にしたいという要求がある。この要求を満たすためには、固着部に設けられ、上述した種々の配線が接続される端

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子の形状を同一にする必要がある。

【００１１】しかしながら、上述したように、図１１に示した電気光学装置は電流駆動型の電気光学装置であるため、陰極９１２及び発光用電源配線９０３の配線幅を狭くすることは配線抵抗等による電圧降下を考慮すると困難である。また、走査線９０１及び信号線９０２は数が多く、これら全てを配置するためには細線化及び狭ピッチ化する必要があるため、走査線９０１及び信号線９０２の線幅を陰極９１２及び発光用電源配線９０３の線幅と同程度にすることも困難である。

【００１２】本発明は、上記事情に鑑みてなされたものであり、表示基板と中継基板との圧着条件を固着部全体に亘って同一にすることにより、固着部における電気的抵抗の不均一性を解消することができるとともに、コントラストの低下等の表示上の不具合を生ずることがない電気光学装置、及び当該電気光学装置を備える電子機器を提供することを目的とする。

【００１３】

【課題を解決するための手段】上記課題を解決するために、本発明の第１の観点による電気光学装置は、第１外部接続端子に接続してなる第１配線と、当該第１配線の幅より広い第２配線とが少なくとも形成された電気光学装置において、前記第２配線に対して複数の第２外部接続端子が設けられていることを特徴としている。この発明によれば、第１配線よりも幅広の第２配線に対しては、外部接続端子が複数設けられているため、配線が施された基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件を固着部全体に亘って均一化することができる。このため、固着部における電気的抵抗の不均一性を解消することができ、その結果として、固着部における電気的抵抗の不均一性に起因する表示ムラ及びコントラストの低下等の表示上の不具合を生ずることがない。また、本発明の第１の観点による電気光学装置は、前記第１外部接続端子及び前記第２外部接続端子には、凸部が形成されていることを特徴としている。この発明によれば、第１配線及び第２配線に対して設けられる第１外部接続端子及び第２外部接続端子の何れにも凸部が形成されており、例えば異方性導電膜で配線が施された基板を表示基板に固着させるときには、異方性導電膜に含まれる導電粒子が、第１外部接続端子及び第２外部接続端子の両端からはみ出す割合が少なくなり、逆に外部接続端子上に留まる割合が上昇するため、固着部における電気的抵抗を低減する上で極めて好適である。また、本発明の第１の観点による電気光学装置は、前記第１外部接続端子及び前記第２外部接続端子の表面には複数の凹部が形成されていることを特徴としている。この発明によれば、第１外部接続端子及び第２外部接続端子の表面に形成された複数の凹部により、第１外部接続端子及び第２外部接続端子がいわば複数の電極として分割した構成となっているため、配線が施さ

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れた基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件をより均一化することができる。また、本発明の第１の観点による電気光学装置は、前記第２外部接続端子の幅がほぼ等しいことを特徴としている。この発明によれば、第２外部接続端子の幅がほぼ等しく設定されているため、配線が施された基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件をより好ましい状態に設定することができる。また、本発明の第１の観点による電気光学装置は、前記第１配線と同程度の幅を有する第１中継配線と、前記第２配線と同程度の幅を有する第２中継配線とが形成され、前記第１外部接続端子を介して前記第１配線と前記第１中継配線とが電気的に接続され、前記第２外部接続端子を介して前記第２配線と前記第２中継配線とが電気的に接続された中継基板を有することを特徴としている。上記課題を解決するために、本発明の第２の観点による電気光学装置は、複数の発光素子と、信号線を介して供給される信号に応じて電源線を介して供給される電流を各前記発光素子に供給するスイッチング素子とが形成された電気光学装置において、前記電源線の幅は前記信号線の幅より広く形成されており、前記電源線に対して複数の第１外部接続端子が設けられていることを特徴としている。この発明によれば、発光素子からの発光を得るため大電流を供給する必要から幅広に形成された電源線と、数多くの信号を供給するために細線化及び狭ピッチかされた信号線とが混在する場合においても、幅広に形成された電源線に対しては外部接続端子が複数設けられているため、配線が施された基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件を固着部全体に亘って均一化することができる。このため、固着部における電気的抵抗の不均一性を解消することができ、その結果として、固着部における電気的抵抗の不均一性に起因する表示ムラ及びコントラストの低下等の表示上の不具合を生ずることがない。また、本発明の第２の観点による電気光学装置は、前記第１外部接続端子及び前記信号線に対して設けられる第２外部接続端子には、凸部が形成されていることを特徴としている。この発明によれば、電源線及び信号線に対して設けられる第１外部接続端子及び第２外部接続端子の何れにも凸部が形成されており、例えば異方性導電膜で配線が施された基板を表示基板に固着させるときには、異方性導電膜に含まれる導電粒子が、第１外部接続端子及び第２外部接続端子の両端からはみ出す割合が少なくなり、逆に外部接続端子上に留まる割合が上昇するため、固着部における電気的抵抗を低減する上で極めて好適である。また、本発明の第２の観点による電気光学装置は、前記第１外部接続端子及び前記第２外部接続端子の表面には複数の凹部が形成されていることを特徴とする請求項６又は請求項７記載の電気光学装置。この発明によれば、第１外部接続端子及び第

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２外部接続端子の表面に形成された複数の凹部により、外部接続端子がいわば複数の電極として分割した構成となっているため、配線が施された基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件をより均一化することができる。また、本発明の第２の観点による電気光学装置は、前記第２外部接続端子の幅がほぼ等しいことを特徴としている。また、本発明の第２の観点による電気光学装置は、前記信号線と同程度の幅を有する第１中継配線と、前記電源線と同程度の幅を有する第２中継配線とが形成され、前記第１外部接続端子を介して前記信号線と前記第１中継配線とが電気的に接続され、前記第２外部接続端子を介して前記電源線と前記第２中継配線とが電気的に接続された中継基板を有することを特徴としている。また、本発明の第２の観点による電気光学装置は、前記第１外部接続端子及び前記第１中継配線、並びに、前記第２外部接続端子及び前記第２中継配線が異方性導電膜により固着されていることが好ましい。本発明の電子機器は、上記の何れかに記載の電気光学装置を備えることを特徴としている。

【００１４】

【発明の実施の形態】以下、図面を参照して本発明の一実施形態による電気光学装置及び電子機器について詳細に説明する。尚、以下の説明で参照する各図は、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならせてある。

【００１５】図１は、本発明の一実施形態による電気光学装置を模式的に示す分解斜視図である。図１に示すように、本実施形態の電気光学装置１０は、大別すると表示基板２０と、表示基板２０に接続される中継基板３０とから構成される。表示基板２０は、スイッチング素子として薄膜トランジスタ（Thin Film Transistor）を用いたアクティブマトリクス方式の有機ＥＬ装置である。

【００１６】この表示基板２０には、複数の走査線２１が形成されており、この走査線２１に交差する方向に延びる複数の信号線２２が形成されている。また、表示基板２０には、発光素子が複数形成された表示素子２０ａが設けられている。更に、図１においては図示を省略しているが、表示基板２０には電源線及び陰極が形成されている。また、表示基板２０の一端には、走査線２１、信号線２２、並びに不図示の電源線及び陰極各々に対する外部接続端子２７が形成されている。

【００１７】尚、図１に示した電気光学装置１０は、あくまでも主要な構成を模式的に示したものであり、実際の走査線２１、信号線２２、及び外部接続端子２７は、極めて狭い間隔をもって多数が表示基板２０上にそれぞれ形成されている点に注意されたい。また、外部接続端子２７と走査線２１との接続状態との接続状態も図１においては図示を省略している。

【００１８】中継基板３０は、可撓性を有するベース基

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板３１上に複数の配線３２が形成されており、更に中継基板３０の所定位置に半導体チップ３３を搭載した構成である。配線３２の一端には、表示基板２０に形成された走査線２１及び信号線２２等の配線と電気的に接続するための外部接続端子３４が形成されている。尚、図１では、中継基板３０上に半導体チップ３３のみが実装された構成であるが、半導体チップ３３が実装される部位以外の部位の所定位置に抵抗、コンデンサ、その他のチップ部品を実装しても良い。また、中継基板３０に形成される配線３２及び外部接続端子３４も、その構造の理解を容易にするために、間隔を拡大して模式的に示すとともに、構造を簡略化して図示してある。

【００１９】図１に示すように、中継基板３０は、異方性導電膜４０を介して表示基板２０に固着される。このとき、中継基板３０の外部接続端子３４は異方性導電膜４０を介して表示基板２０の外部接続端子２７と電気的に接続される。この異方性導電膜４０は、一対の端子間を異方性を持たせて電気的に一括接続するために用いられる導電性のある高分子フィルムであって、例えば、図２に示すように、熱可塑性又は熱硬化性の接着用樹脂４１ａの中に多数の導電粒子４１ｂを分散させることによって形成される。

【００２０】図２は、異方性導電膜４０により中継基板３０と表示基板２０とが固着される様子を示す断面図である。図２に示すように、表示基板２０に形成された外部接続端子２７と中継基板３０に形成された外部接続端子３４との間に導電粒子４１ｂが挟持されるため、外部接続端子２７と中継配線である外部接続端子３４との間が電気的に接続されることになる。一方、外部接続端子２７及び外部接続端子３４が形成されている部位以外の部位においては、導電粒子４１ｂが挟持されていても、接続端子が存在しないため、導通は取れていない。このようにして、外部接続端子２７及び外部接続端子３４との間のみで導通をとることができる。

【００２１】異方性導電膜４０を用いて表示基板２０と中継基板３０とを固着させるには、表示基板２０を表面が粗面とされた案内板を有する載置台（何れも図示省略）上に配置し、表示基板２０を真空吸着する。このとき、少なくとも表示基板２０に対して中継基板３０が固着される部位が案内板の上方に位置するように表示基板２０を載置台上に載置する。ここで、表面が粗面とされた案内板を用いるのは、案内板と表示基板２０の接触面積を低減して案内板からの熱放散を抑えることで、表示基板２０に加える温度を低下させるためである。

【００２２】表示基板２０の載置台上への載置が完了すると、中継基板３０が固着される表示基板２０の部位に異方性導電膜４０を貼付し、更に、半導体チップ３３が搭載された面を下側にして、外部接続端子３４が異方性導電膜４０の上方に位置するように中継基板３０の位置合わせを行う。以上の工程が終了すると、図示しない加熱加圧ヘッドを用いて外部接続端子３４が形成されている面の裏面を加熱・加圧して、外部接続端子３４と表示基板２０に形成されている外部接続端子２７との導通をとるとともに、中継基板３０を表示基板２０に固着させる。このとき、加熱加圧ヘッドから中継基板３０及び表示基板２０に加える温度は百数十～数百℃程度であり、加える圧力は数メガパスカルである。以上の工程を経ることにより、中継基板３０を表示基板２０に固着させることができる。

【００２３】次に、本実施形態の電気光学装置１０の配線構造の詳細について説明する。図３は、本発明の一実施形態による電気光学装置の配線構造を模式的に示す図である。図３に示したように電気光学装置１０は、複数の走査線２１と、走査線２１に対して交差する方向に延びる複数の信号線２２と、信号線２２に並行して延びる複数の発光用電源配線２３とがそれぞれ配線されており、走査線２１及び信号線２２の各交点付近に、画素領域Ａが設けられている。

【００２４】各信号線２２には、シフトレジスタ、レベルシフタ、ビデオライン、及びアナログスイッチを備えるデータ側駆動回路３３ａが接続されている。また、各信号線２２には、薄膜トランジスタを備える検査回路２５が接続されている。更に、各走査線２１には、シフトレジスタ及びレベルシフタを備える走査線駆動回路２４が接続されている。

【００２５】また、画素領域Ａの各々には、スイッチング薄膜トランジスタ５２、保持容量Ｃａｐ、カレント薄膜トランジスタ５３、画素電極５１、発光層５０、及び陰極２６が設けられる。スイッチング薄膜トランジスタ５２は、そのゲート電極に走査線２１が接続されており、走査線２１から供給される走査信号に応じて駆動されてオン状態又はオフ状態となる。保持容量Ｃａｐは、スイッチング薄膜トランジスタ５２を介して信号線２２から供給される画像信号を保持する。

【００２６】カレント薄膜トランジスタ５３は、そのゲート電極がスイッチング薄膜トランジスタ５２及び保持容量Ｃａｐに接続されており、保持容量Ｃａｐによって保持された画像信号がゲート電極に供給される。画素電極５１は、カレント薄膜トランジスタ５３に接続されており、カレント薄膜トランジスタ５３を介して発光用電源配線２３に電気的に接続したときに発光用電源配線２３から駆動電流が流れ込む。発光層５０は画素電極５１と陰極２６との間に挟み込まれている。

【００２７】上記、発光層５０には、赤色に発光する発光層５０Ｒ、緑色に発光する発光層５０Ｇ、及び青色に発光する発光層５０Ｂの３種の発光素子が含まれ、各発光層５０Ｒ，５０Ｇ，５０Ｂがストライプ配置されている。そして、カレント薄膜トランジスタ５３を介して各発光層５０Ｒ，５０Ｇ，５０Ｂに接続される発光用電源配線２３Ｒ，２３Ｇ，２３Ｂがそれぞれ、発光用電源回

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路３３ｃに接続されている。各色毎に発光用電源配線２３Ｒ，２３Ｇ，２３Ｂが配線されているのは、発光層５０Ｒ，５０Ｇ，５０Ｂの駆動電位が各色毎に異なるためである。

【００２８】また、本実施形態の電気光学装置においては、陰極２６と発光用電源配線２３Ｒ，２３Ｇ，２３Ｂとの間に静電容量C_1が形成されている。電気光学装置１０が駆動するとこの静電容量C_1に電荷が蓄積される。電気光学装置１０の駆動中に各発光用電源配線２３を流れる駆動電流の電位が変動した場合には、蓄積された電荷が各発光用電源配線２３に放電されて駆動電流の電位変動を抑制する。これにより、電気光学装置１０の画像表示を正常に保つことができる。

【００２９】尚、この電気光学装置１０においては、走査線２１から走査信号が供給されてスイッチング薄膜トランジスタ５２がオン状態になると、そのときの信号線２２の電位が保持容量Ｃａｐに保持され、保持容量Ｃａｐに保持された電位に応じてカレント薄膜トランジスタ５３のオン・オフ状態が決まる。そして、カレント薄膜トランジスタ５３のチャネルを介して、発光用電源配線２３Ｒ，２３Ｇ，２３Ｂから画素電極５１に駆動電流が流れ、更に発光層５０Ｒ，５０Ｇ，５０Ｂを介して陰極２６に電流が流れる。このとき、発光層５０を流れた電流量に応じた量の発光が発光層５０から得られる。

【００３０】次に、本実施形態の電気光学装置１０の具体的な構成について、図４及び図５を参照して説明する。図４は、本実施形態の電気光学装置の平面模式図であり、図５は、図４のＡ－Ａ′線に沿う断面図である。図４に示すように、本実施形態の電気光学装置１０は、基板６０、不図示の画素電極群領域、発光用電源配線２３（２３Ｒ，２３Ｇ，２３Ｂ）、及び表示画素部６１（図中一点鎖線の枠内）とから概略構成される。

【００３１】基板６０は、例えばガラス等からなる透明な基板である。画素電極群領域は、図３に示したカレント薄膜トランジスタ５３に接続された画素電極（図示省略）を基板６０上にマトリックス状に配置した領域である。発光用電源配線２３（２３Ｒ，２３Ｇ，２３Ｂ）は、図４に示したように、画素電極群領域の周囲に配置され、各画素電極に接続されている。表示画素部６１は、少なくとも画素電極群領域上に位置し、平面視略矩形形状である。この表示画素部６１は、中央部分の実表示領域（又は、有効表示領域ともいう）６２（図中二点鎖線の枠内）と、実表示領域６２の外側に配置されたダミー領域６３（一点鎖線及び二点鎖線の間の領域）とに区画されている。

【００３２】また、実表示領域６２の図中両側には、走査線駆動回路２４が配置されている。この走査線駆動回路２４はダミー領域６３の下層側（基板６０側）に位置して設けられている。更に、ダミー領域６３の下層側には、走査線駆動回路２４に接続される走査線駆動回路用制御信号配線２４ａと走査線駆動回路用電源配線２４ｂとが設けられている。また更に、実表示領域６２の図中上側には、前述の検査回路２５が配置されている。この検査回路２５はダミー領域６３の下層側（基板側２）に位置して設けられており、この検査回路２５により、製造途中や出荷時の電気光学装置の品質、欠陥の検査を行うことができる。

【００３３】図４に示すように、発光用電源配線２３Ｒ，２３Ｇ，２３Ｂは、ダミー領域６３の周囲に配設されている。各発光用電源配線２３Ｒ，２３Ｇ，２３Ｂは、基板６０の図２中下側から走査線駆動回路用制御信号配線２４ａに沿って図４中上方に延在し、走査線駆動回路用制御信号配線２４ａが途切れた位置から折曲してダミー領域６３の外側に沿って延在し、実表示領域６２内にある図示略の画素電極に接続されている。また、基板６０には、陰極２６に接続される陰極用配線２６ａが形成されている。この陰極用配線２６ａは、発光用電源配線２３Ｒ，２３Ｇ，２３Ｂを囲むように平面視略コ字状に形成されている。

【００３４】次に、図５に示すように、基板６０上には回路部１１が形成され、この回路部１１上に表示画素部６１が形成されている。また、基板６０には、表示画素部６１を環状に囲む封止材１３が形成されており、更に表示画素部６１上に封止基板１４が備えられている。封止基板１４は、封止材１３を介して基板６０に接合されており、ガラス、金属、又は樹脂等からなるものである。この封止基板１４の裏側には、吸着剤１５が貼付され、表示画素部６１と封止基板１４との間の空間に混入した水又は酸素を吸収できるようになっている。尚、吸着剤１５に代えてゲッター剤を用いても良い。また、封止材１３は、例えば熱硬化樹脂又は紫外線硬化樹脂からなるものであり、特に熱硬化樹脂の一種であるエポキシ樹脂よりなることが好ましい。

【００３５】回路部１１の中央部分には、画素電極群領域１１ａが設けられている。この画素電極群領域１１ａには、カレント薄膜トランジスタ５３と、カレント薄膜トランジスタ５３に接続された画素電極５１が備えられている。カレント薄膜トランジスタ５３は、基板６０上に積層された下地保護層２８１、第２層間絶縁層２８３、及び第１層間絶縁層２８４に埋め込まれて形成され、画素電極５１は、第１層間絶縁層２８４上に形成されている。カレント薄膜トランジスタ５３に接続され、第２層間絶縁層２８３上に形成された電極の一方（ソース電極）には、発光用電源配線２３（２３Ｒ，２３Ｇ，２３Ｂ）が接続されている。尚、回路部１１には、前述した保持容量Ｃａｐ及びスイッチング薄膜トランジスタ５２も形成されているが、図５ではこれらの図示を省略している。更に、図５においては、信号線２２の図示を省略している。

【００３６】次に、図５において、画素電極群領域１１

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aの図中両側には、前述の走査線駆動回路２４が設けられている。図４に示した走査線駆動回路２４には、シフトレジスタに含まれるインバータを構成するNチャネル型又はPチャネル型の薄膜トランジスタ２４ｃが備えられ、この薄膜トランジスタ２４ｃは、画素電極５１に接続されていない点を除いて上記のカレント薄膜トランジスタ５３と同様の構造とされている。尚、図５においては、検査回路２５の図示を省略しているが、この検査回路２５にも同様に薄膜トランジスタが備えられている。検査回路２５に備えられている薄膜トランジスタは、後述するダミー画素電極５１′に接続されていない点を除いてカレント薄膜トランジスタ５３と同様の構造とされている。

【００３７】図５に示すように、走査線駆動回路２４の図中外側の下地保護層２８１上には、走査線駆動回路用制御信号配線２４ａが形成されている。また、走査線駆動回路用制御信号配線２４ａの外側の第２層間絶縁層２８３上には、走査線駆動回路用電源配線２４ｂが形成されている。また、走査線駆動回路用電源配線２４ｂの外側には、発光用電源配線２３が形成されている。この発光用電源配線２３は、２つの配線からなる二重配線構造を採用しており、前述したように表示画素部６１の外側に配置されている。二重配線構造を採用することで配線抵抗を軽減できる。

【００３８】例えば、図５中左側にある赤色用の発光用電源配線２３Ｒは、下地保護層２８１上に形成された第１配線$２３Ｒ_1$と、第２層間絶縁層２８３を介して第１配線$２３Ｒ_1$上に形成された第２配線$２３Ｒ_2$とから構成されている。第１配線$２３Ｒ_1$及び第２配線$２３Ｒ_2$は、図２に示すように第２層間絶縁層２８３を貫通するコンタクトホール$２３Ｒ_3$により接続されている。このように、第１配線$２３Ｒ_1$は、陰極用配線２６ａと同じ階層位置に形成されており、第１配線$２３Ｒ_1$と陰極用配線２６ａとの間は第２層間絶縁層２８３が配置されている。また、図５に示す通り、陰極用配線２６ａはコンタクトホールを介して第２層間絶縁層２８３上に形成された陰極用配線２６ｂと電気的に接続されおり、いわば陰極用配線２６ａも二重配線構造になっている。よって、第２配線$２３Ｒ_2$は、陰極用配線２６ｂと同じ階層位置に形成されており、第１配線$２３Ｒ_2$と陰極用配線２６ｂとの間は第１層間絶縁層２８４が配置されている。このような構造をとることで、第１配線$２３Ｒ_1$と陰極用配線２６ａとの間、及び、第２配線$２３Ｒ_2$と陰極用配線２６ｂとの間に第２の静電容量$Ｃ_2$が形成されている。

【００３９】同様に、図５の右側にある青色及び緑色用の発光用電源配線２３Ｇ，２３Ｂも二重配線構造を採用しており、それぞれ下地保護層２８１上に形成された第１配線$２３Ｇ_1$，$２３Ｂ_1$と、第２層間絶縁層２８３上に形成された第２配線$２３Ｇ_2$，$２３Ｂ_2$とから構成され、第１配線$２３Ｇ_1$，$２３Ｂ_1$及び第２配線$２３Ｇ_2$，$２３Ｂ_2$は、図４に示すように第２層間絶縁層２８３を貫通するコンタクトホール$２３Ｇ_3$，$２３Ｂ_3$により接続されている。そして、青色の第１配線$２３Ｂ_1$と陰極用配線２６ａの間、及び、青色の第２配線$２３Ｂ_2$と陰極用配線２６ｂとの間に第２の静電容量$Ｃ_2$が形成されている。

【００４０】第１配線$２３Ｒ_1$と第２配線$２３Ｒ_2$との間隔は、例えば、０．６～１．０μmの範囲が好ましい。間隔が０．６μm未満であると、信号線２２及び走査線２１のような異なる電位を有するソースメタルとゲートメタルとの間の寄生容量が増えるため好ましくない。例えば、実表示領域６２内においては、ソースメタルとゲートメタルとが交差する箇所が多く存在し、かかる箇所の寄生容量が多いと画像信号の時間遅延を引き起こす虞がある。その結果として、定められた期間内に画像信号を画素電極５１に書き込む事ができないため、コントラストの低下を引き起こす。第１配線$２３Ｒ_1$及び第２配線$２３Ｒ_2$に挟まれる第２層間絶縁層２８３の材質は、例えば$ＳｉＯ_2$等が好ましいが、１．０μm以上形成すると$ＳｉＯ_2$の応力により基板６０が割れる恐れが生じる。

【００４１】また、各発光用電源配線２３Ｒの上側には、表示画素部６１から延出した陰極２６が形成されている。これにより、各発光用電源配線２３Ｒの第２配線$２３Ｒ_2$が、第１層間絶縁層２８４を挟んで陰極２６と対向配置され、これにより第２配線$２３Ｒ_2$と陰極２６との間に前述の第１の静電容量$Ｃ_1$が形成される。ここで、第２配線$２３Ｒ_2$と陰極２６との間隔は、例えば、０．６～１．０μmの範囲が好ましい。間隔が０．６μm未満だと、画素電極及びソースメタルのような異なる電位を有する画素電極とソースメタルとの間の寄生容量が増える為、ソースメタルを用いている信号線の配線遅延が生じる。その結果、定められた期間内に画像信号を書き込む事ができない為、コントラストの低下を引き起こす。第２配線$２３Ｒ_2$と陰極２６に挟まれる第１層間絶縁層２８４の材質は、例えば$ＳｉＯ_2$やアクリル樹脂等が好ましい。しかしながら、$ＳｉＯ_2$を１．０μm以上形成すると応力により基板６０が割れる恐れが生じる。また、アクリル樹脂の場合は、２．０μm程度まで形成することができるが、水を含むと膨張する性質があるため、その上に形成する画素電極を割る恐れがある。

【００４２】このように、表示基板２０には、発光用電源配線２３と陰極２６との間に第１の静電容量$Ｃ_1$が設けられるので、発光用電源配線２３を流れる駆動電流の電位が変動した場合に第１の静電容量$Ｃ_1$に蓄積された電荷が発光用電源配線２３に供給され、駆動電流の電位不足分がこの電荷により補われて電位変動を抑制することができ、発光装置１の画像表示を正常に保つことができる。特に、発光用電源配線２３と陰極２６とが表示画

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素部６１の外側で対向しているので、発光用電源配線２３と陰極２６との間隔を小さくして第１の静電容量C_1に蓄積される電荷量を増大させることができ、駆動電流の電位変動をより小さくして画像表示を安定に行うことができる。更に、発光用電源配線２３が第１配線及び第２配線からなる二重配線構造を有し、第１配線と陰極用配線との間に第２の静電容量C_2が設けられているので、第２の静電容量C_2に蓄積された電荷も発光用電源配線２３に供給されるため、電位変動をより抑制することができ、発光装置１の画像表示をより正常に保つことができる。

【００４３】次に、表示画素部６１の実画素領域６２には、発光層５０及びバンク部（絶縁部）１２２が形成されている。発光層５０は図５に示すように、画素電極５１上の各々に積層されている。また、バンク部１２２は、各画素電極５１及び各発光層５０の間に備えられており、各発光層５０を区画している。バンク部１２２は、基板６０側に位置する無機物バンク層１２２ａと基板６０から離れて位置する有機物バンク層１２２ｂとが積層されて構成されている。尚、無機物バンク層１２２ａと有機物バンク層１２２ｂとの間に遮光層を配置してもよい。

【００４４】無機物、有機物バンク層１２２ａ，１２２ｂは、画素電極５１の周縁部上に乗上げるまで延出形成されており、また無機物バンク層１２２ａは、有機物バンク層１２２ｂよりも画素電極５１の中央側に延出形成されている。また、無機物バンク層１２２ａは、例えば、SiO_2、TiO_2、ＳｉＮ等の無機材料からなることが好ましい。また無機物バンク層１２２ａの膜厚は、５０～２００ｎｍの範囲が好ましく、特に１５０ｎｍがよい。膜厚が５０ｎｍ未満では、無機物バンク層１２２ａが後述する正孔注入／輸送層より薄くなり、正孔注入／輸送層の平坦性を確保できなくなるので好ましくない。また膜厚が２００ｎｍを越えると、無機物バンク層１２２ａによる段差が大きくなって、正孔注入／輸送層上に積層する後述の発光層の平坦性を確保できなくなるので好ましくない。

【００４５】更に、有機物バンク層１２２ｂは、アクリル樹脂、ポリイミド樹脂等の通常のレジストから形成されている。この有機物バンク層１２２ｂの厚さは、０．１～３．５μｍの範囲が好ましく、特に２μｍ程度がよい。厚さが０．１μｍ未満では、後述する正孔注入／輸送層及び発光層の合計厚より有機物バング層１２２ｂが薄くなり、発光層が上部開口部から溢れるおそれがあるので好ましくない。また、厚さが３．５μｍを越えると、上部開口部による段差が大きくなり、有機物バンク層１２２ｂ上に形成する陰極２６のステップカバレッジを確保できなくなるので好ましくない。また、有機物バンク層１２２ｂの厚さを２μｍ以上にすれば、陰極２６と画素電極５１との絶縁を高めることができる点でより好ましい。このようにして、発光層５０は、バンク部１２２より薄く形成されている。

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【００４６】また、バンク部１２２の周辺には、親液性を示す領域と、撥液性を示す領域が形成されている。親液性を示す領域は、無機物バンク層１２２ａ及び画素電極５１であり、これらの領域には、酸素を反応ガスとするプラズマ処理によって水酸基等の親液基が導入されている。また、撥液性を示す領域は、有機物バンク層１２２ｂであり、４フッ化メタンを反応ガスとするプラズマ処理によってフッ素等の撥液基が導入されている。

【００４７】発光層５０は、画素電極５１上に積層された図示せぬ正孔注入／輸送層上に積層されている。尚、本明細書では、発光層５０及び正孔注入／輸送層を含む構成を機能層といい、画素電極５１、機能層、及び陰極２６含む構成を発光素子という。正孔注入／輸送層は、正孔を発光層５０に注入する機能を有するとともに、正孔を正孔注入／輸送層内部において輸送する機能を有する。このような正孔注入／輸送層を画素電極５１と発光層５０の間に設けることにより、発光層５０の発光効率、寿命等の素子特性が向上する。また、発光層５０では、正孔注入／輸送層から注入された正孔と、陰極２６からの電子とが結合して蛍光を発生させる。発光層５０は、赤色（Ｒ）に発光する赤色発光層、緑色（Ｇ）に発光する緑色発光層、及び青色（Ｂ）に発光する青色発光層の３種類を有し、図３及び図４に示すように、各発光層がストライプ配置されている。

【００４８】次に、図５に示したように、表示画素部６１のダミー領域６３には、ダミー発光層２１０及びダミーバンク部２１２が形成されている。ダミーバンク部２１２は、基板６０側に位置するダミー無機物バンク層２１２ａと基板６０から離れて位置するダミー有機物バンク層２１２ｂとが積層されて構成されている。ダミー無機物バンク層２１２ａは、ダミー画素電極５１′の全面に形成されている。またダミー有機物バンク層２１２ｂは、有機物バンク層１２２ｂと同様に画素電極５１の間に形成されている。そして、ダミー発光層２１０は、ダミー無機物バンク２１２ａを介してダミー画素電極５１′上に形成されている。

【００４９】ダミー無機物バンク層２１２ａ及びダミー有機物バンク層２１１ｂは、先に説明した無機物、有機物バンク層１２２ａ，１２２ｂと同様の材質、同様の膜厚を有するものである。また、ダミー発光層２１０は、図示略のダミー正孔注入／輸送層上に積層されており、ダミー正孔注入／輸送層及びダミー発光層の材質や膜厚は、前述の正孔注入／輸送層及び発光層５０と同様である。従って、上記の発光層５０と同様に、ダミー発光層２１０はダミーバンク部２１２より薄く形成されている。

【００５０】ダミー領域６３を実表示領域６２の周囲に配置することにより、実表示領域６２の発光層５０の厚

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さを均一にすることができ、表示ムラを抑制することができる。即ち、ダミー領域６３を配置することで、表示素子をインクジェット法によって形成する場合における吐出した組成物インクの乾燥条件を実表示領域６２内で一定にすることができ、実表示領域６２の周縁部で発光層５０の厚さに偏りが生じる虞がない。

【００５１】次に、陰極２６は、実表示領域６２とダミー領域６３の全面に形成されるとともにダミー領域６３の外側にある基板６０上まで延出され、ダミー領域６３の外側、即ち表示画素部６１の外側で発光用電源配線２３と対向配置されている。また陰極２６の端部が、回路部１１に形成された陰極用配線２６ａに接続されている。陰極２６は、画素電極５１の対向電極として発光層５０に電流を流す役割を果たす。この陰極２６は、例えば、フッ化リチウムとカルシウムの積層体からなる陰極層２６ｂと反射層２６ｃとが積層されて構成されている。陰極２６のうち、反射層２６ｃのみが表示画素部６１の外側まで延出されている。反射層２６ｃは、発光層５０から発した光を基板６０側に反射させるもので、例えば、Ａｌ、Ａｇ、Ｍｇ／Ａｇ積層体等からなることが好ましい。更に、反射層２６ｃ上にSiO_2、ＳｉＮ等からなる酸化防止用の保護層を設けても良い。

【００５２】また、図４に示すように、基板６０の一端には前述した異方性導電膜４０を用いて中継基板３０が固着されている。尚、中継基板３０上に搭載された半導体チップ３３には、図３に示したデータ側駆動回路３３ａ、陰極用電源回路３３ｂ、及び発光用電源回路３３ｃが内蔵されている。図４中の破線で囲った部分は、表示基板２０と中継基板３０との固着部を示している。図６は、図４に示した固着部６５付近の上面図である。尚、図６においては、異方性導電膜４０及び中継基板３０の図示を省略している。

【００５３】図６に示したように、固着部６５においては、線幅の細い配線各々に対して配線の幅と同程度の幅を有する第１外部接続端子が設けられ、幅広の配線に対しては線幅よりも幅の狭い複数の第２外部接続端子が設けられる。例えば、線幅の細い走査線駆動回路用制御信号配線２４ａの各々に対しては、走査線駆動回路用制御信号配線２４ａの線幅と同程度の幅を有する第１外部接続端子６７，６８，６９が設けられる。一方、幅が広い発光用電源配線２３Ｒに対しては、発光用電源配線２３Ｒの線幅よりも幅の狭い第２外部接続端子６６ａ，６６ｂ，６６ｃが設けられる。また、走査線駆動回路用制御信号配線２４ａよりも幅が狭い信号線２２に対しては、信号線２２と同程度の線幅を有する第２外部接続端子７０がそれぞれ設けられる。尚、第１外部接続端子及び第２外部接続端子の数は、基板６０に形成される配線の線幅に応じて適宜設定される。

【００５４】このように、基板６０に形成された配線の線幅に応じて第１外部接続端子及び第２外部接続端子の数を変えるのは、固着部６５の全面に亘って圧着条件を極力同一にするためである。つまり、図１及び図２を用いて説明したように、表示基板１０と中継基板２０とは異方性導電膜４０により固着されるが、固着条件（例えば、端子の幅、接着面積、圧力の掛かり具合等）が異なると固着部６５内部における電気的抵抗がその位置に応じて異なる。固着部６５における電気的抵抗が位置に応じて異なると、表示ムラ及びコントラスト低下等の表示上の不具合を生ずる。このために、固着部６５において、基板６０に形成された配線の線幅に応じて外部接続端子の数を変えることにより圧着条件を極力同一にしている。更に、複数の外部接続端子を設けることにより、接着面積を増大させることができる。即ち、複数の外部接続端子ｎ間に異方性導電膜を配置することができるので、強固な接着が可能となる。

【００５５】次に、固着部６５に形成される外部接続端子の構造について詳細に説明する。図７は、図６中のＢ－Ｂ′線に沿う第２外部接続端子６６ｃ及び第２外部接続端子７０の断面図であり、図８は、図７中の外部接続端子７０の拡大図である。図７及び図８に示すように、基板６０上には下地保護層２８１が形成されており、この下地保護層２８１上にSiO_2及び／又はＳｉＮを主体とするゲート絶縁層７１が形成されている。このゲート絶縁層７１は、図示しない薄膜トランジスタのチャネル領域とゲート電極とを電気的に絶縁するために形成されるものである。尚、本明細書において、「主体」とする成分とは最も含有率の高い成分のことをいうものとする。

【００５６】ゲート絶縁層７１上には信号線２２及び発光用電源配線２３Ｒが形成されており、更に信号線２２及び発光用電源配線２３Ｒ上に第２層間絶縁層２８３が形成されている。また、発光用電源配線２３、走査線駆動回路用制御信号配線２４ａは、図３に記載の走査線２１と同時に形成される。

【００５７】上記第２層間絶縁層２８３には、信号線２２及び発光用電源配線２３Ｒの上部位置にコンタクトホールＨが複数形成されている。また、発光用電源配線２３Ｒの上方の第２層間絶縁層２８３上には電極７３が形成され、信号線２２の上方の第２層間絶縁層２８３上には電極７４，７５が形成されている。

【００５８】これらの電極７３，７４，７５は、コンタクトホールＨを形成した後でスパッタリング法等により形成されるため、コンタクトホールＨの上部にはコンタクトホールＨ内に堆積した金属材料の分だけ表面に凹部Ｂが形成される。このようにして、コンタクトホールＨを介して、第２層間絶縁層２８３に覆われた発光用電源配線２３Ｒと第２層間絶縁層２８３上に形成された電極７４との導通、及び、第２層間絶縁層２８３に覆われた信号線２２と第２層間絶縁層２８３上に形成された電極７４，７５の導通がとられる。

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【００５９】また、第２層間絶縁層２８３上に形成された電極７３，７４，７５の端部、側部、及びこれらの電極７３，７４，７５間には、電気的な絶縁を目的としたＳｉＮ等の無機材料からなる第１層間絶縁層２８４が形成されている。電極７３，７４，７５の上部、側部、及び周辺部には、ＩＴＯ等からなる透明電極７７が形成され、更に電極７３，７４，７５の周辺部に形成された透明電極７７及び第２外部接続端子６６ｃ，７０，７０間にはSiO_2からなる保護層７８が形成されている。尚、電極７３，７４，７５は、図３に記載されているゲート線と同時に形成され、又、透明電極７７は、ＩＴＯにより形成され、画素電極（陽極）と同時に形成される。

【００６０】図７及び図８に示すように、本実施形態の電気光学装置に設けられる第２外部接続端子６６ｃ，７０，７０の表面には複数の凹部Ｂが形成されされており、この凹部Ｂにより、第２外部接続端子６６ｃ，７０，７０をいわば複数の電極として分割した構成となっている。図６に示したように、発光用電源配線２３Ｒ及び信号線２２の線幅に応じて外部接続端子の数を変えることにより、固着部６５における固着条件の均一化を図っているが、第２外部接続端子６６ｃ，７０，７０の表面に複数の凹部Ｂが形成されているため、第２外部接続端子６６ｃ，７０，７０は更に複数の電極に分割されたものとなり、固着条件の均一化を図る上で極めて好適である。

【００６１】また、電極７３，７４，７５の端部に第１層間絶縁層２８４を形成することにより、第２外部接続端子６６ｃ，７０，７０の端部に凸部７９が形成される。この凸部７９は、異方性導電膜４０を用いて表示基板１０と中継基板２０とを固着する際に、異方性導電膜４０に含まれる導電粒子４１ｂが第２外部接続端子６６ｃ，７０，７０の側部にはみ出るのを防止するように作用する。その結果、より多くの導電粒子４１ｂが第２外部接続端子６６ｃ，７０，７０上に配置されることになるため、固着部６５における電気的抵抗を低減する極めて優れた構造である。

【００６２】以上説明した本実施形態の表示基板２０は、固着部６５において圧着条件を均一化するための構成が設けられているため、固着部６５に固着される中継基板３０に形成される外部接続端子３４は、図６に示す発光用電源配線２３Ｒ及び走査線駆動回路用制御信号配線２４ａ等と同様の線幅で形成されていても良い。しかしながら、より均一な圧着条件下で中継基板３０と表示基板２０とを固着するには、固着部６５に形成された第２外部接続端子６６ｃ，７０，７０等と同様のパターンであることが好適である。

【００６３】以上、本発明の一実施形態による電気光学装置について説明したが、以上説明した電気光学装置、ＣＰＵ（中央処理装置）等を備えたマザーボード、キーボード、ハードディスク等の電子部品を筐体内に組み込むことで、例えば図９に示すノート型のパーソナルコンピュータ６００（電子機器）が製造される。図９は、本発明の一実施形態による電気光学装置を備える電子機器の一例を示す図である。尚、図９において６０１は筐体であり、６０２は液晶表示装置であり、６０３はキーボードである。図１０は、他の電子機器としての携帯電話機を示す斜視図である。図１０に示した携帯電話機７００は、アンテナ７０１、受話器７０２、送話器７０３、液晶表示装置７０４、及び操作釦部７０５等を備えて構成されている。

【００６４】また、上記実施形態では、電子機器としてノート型コンピュータ及び携帯電話機を例に挙げて説明したが、これらに限らず、液晶プロジェクタ、マルチメディア対応のパーソナルコンピュータ（ＰＣ）及びエンジニアリング・ワークステーション（ＥＷＳ）、ページャ、ワードプロセッサ、テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、電子手帳、電子卓上計算機、カーナビゲーション装置、ＰＯＳ端末、タッチパネルを備えた装置等の電子機器に適用することが可能である。

【００６５】

【発明の効果】以上説明したように、本発明によれば、第１配線よりも幅広の第２配線に対しては、第２外部接続端子が複数設けられているため、配線が施された基板を表示基板に固着させるとともに導通を取るときの圧力の掛かり具合等の圧着条件を固着部全体に亘って均一化することができるという効果がある。このため、固着部における電気的抵抗の不均一性を解消することができ、その結果として、固着部における電気的抵抗の不均一性に起因する表示ムラ及びコントラストの低下等の表示上の不具合を生ずることがないという効果がある。

【図面の簡単な説明】

【図１】　本発明の一実施形態による電気光学装置を模式的に示す分解斜視図である。

【図２】　異方性導電膜４０により中継基板３０と表示基板２０とが固着される様子を示す断面図である。

【図３】　本発明の一実施形態による電気光学装置の配線構造を模式的に示す図である。

【図４】　本実施形態の電気光学装置の平面模式図である。

【図５】　図４のＡ－Ａ′線に沿う断面図である。

【図６】　図４に示した固着部６５付近の上面図である。

【図７】　図６中のＢ－Ｂ′線に沿う第２外部接続端子６６ｃ及び第２外部接続端子７０の断面図である。

【図８】　図７中の外部接続端子７０の拡大図である。

【図９】　本発明の一実施形態による電気光学装置を備える電子機器の一例を示す図である。

【図１０】　他の電子機器としての携帯電話機を示す斜

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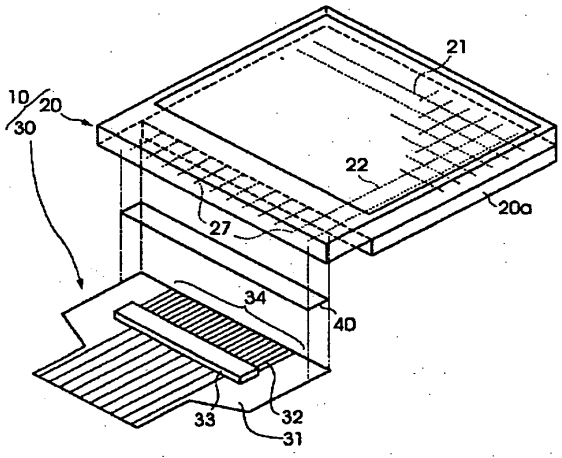
視図である。

【図１１】　従来の電気光学装置の配線構造を示す図である。

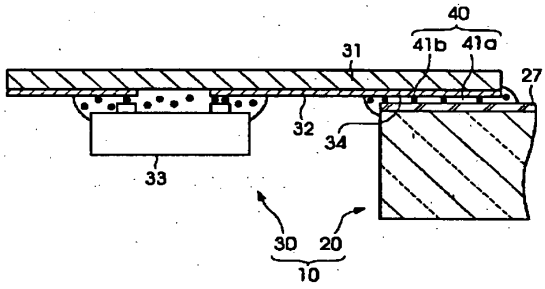
【符号の説明】

１０……電気光学装置
２０……表示基板
２２……信号線（第１配線）
２３，２３Ｒ……発光用電源配線（第２配線、電源線）
２４ａ……走査線駆動回路用制御信号配線（第１配線）
３０……中継基板
４０……異方性導電膜
５０……発光素子
５３……スイッチング素子
６６ａ，６６ｂ，６６ｃ……第２外部接続端子
６７，６８，６９，７０……第１外部接続端子
７９……凸部
Ｂ……凹部

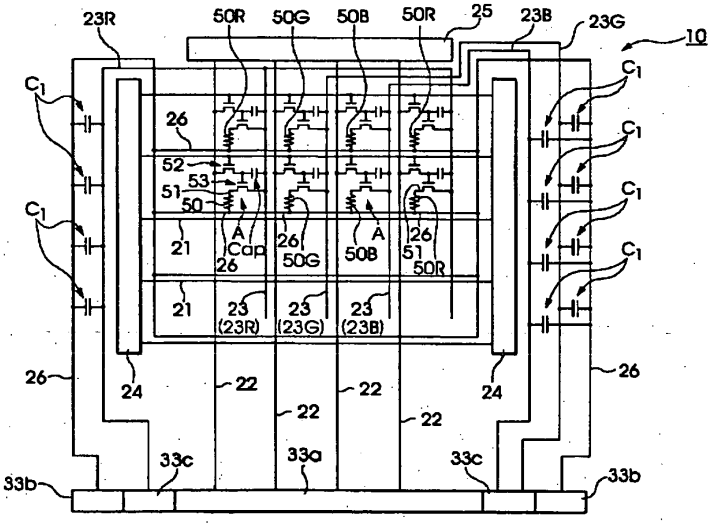
【図１】



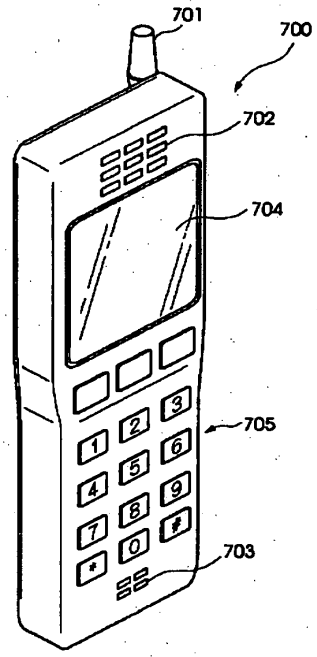
【図２】



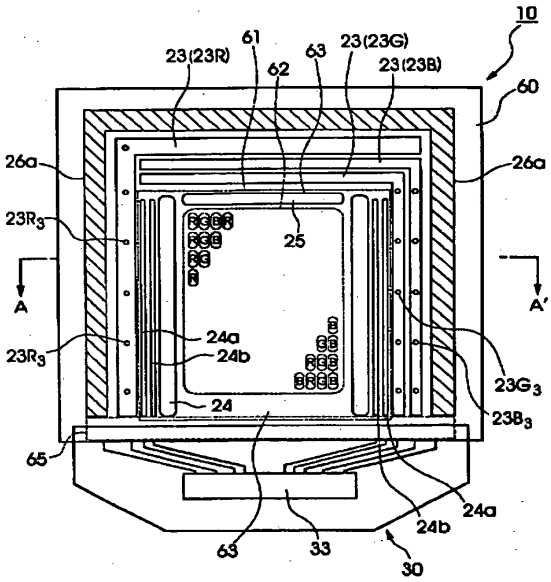
【図３】



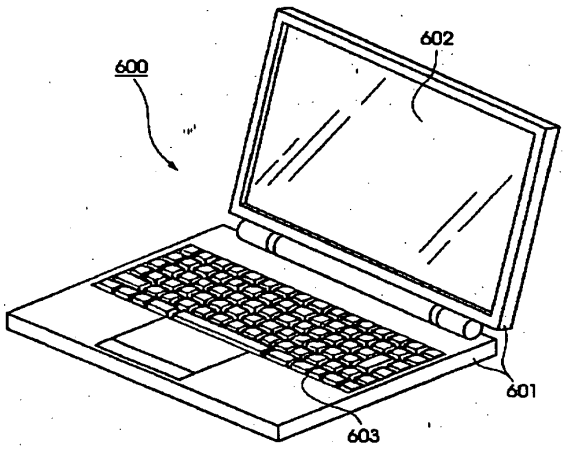
【図１０】



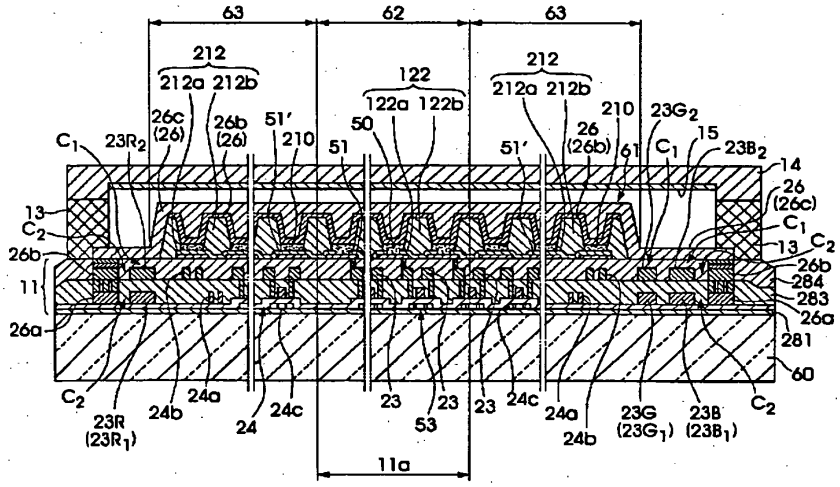
【図４】


10
23(23R)
61
62
63
23(23G)
23(23B)
60
26a
26a
23R3
25
A
A'
23R3
24a
24b
23G3
24
23B3
65
24a
24b
63
33
30

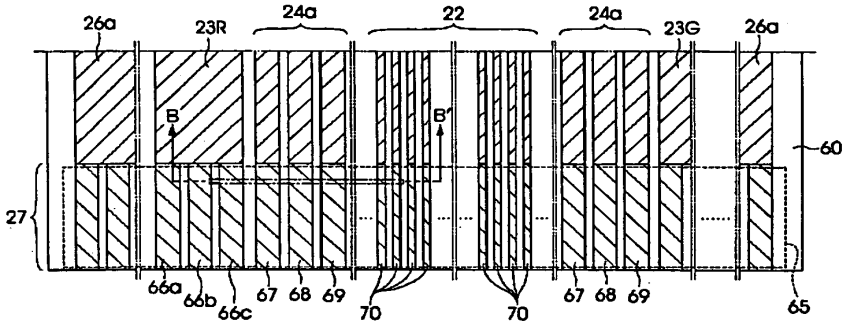
【図９】


600
602
601
603

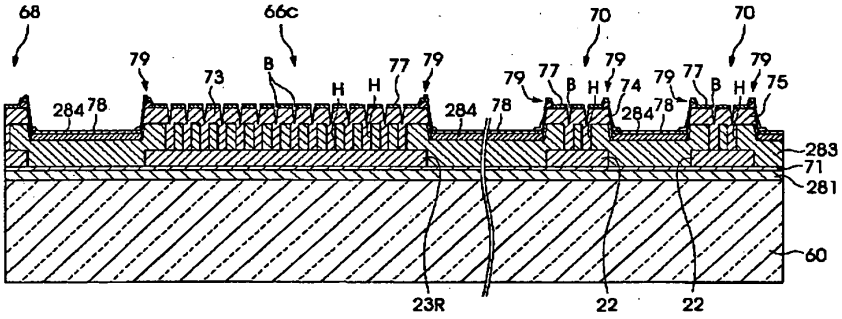
【図５】


63
62
63
212
212a 212b
122
122a 122b
212
212a 212b
C1
23R2
26c (26)
26b (26)
51'
210
51
50
51'
26 (26b)
210
23G2
61
C1
15
23B2
14
26 (26c)
C1
13
C2
26b
11
283
26a
281
60
C2
23R (23R1)
24b
24a
24
24c
23
53
23
23
24c
24a
24b
23G (23G1)
23B (23B1)
C2
11a

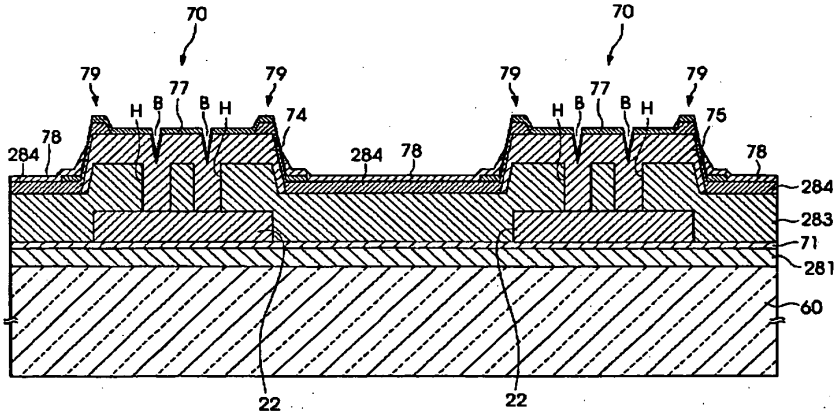
【図６】


26a
23R
24a
22
24a
23G
26a
B
B'
60
27
66a
66b
66c
67
68
69
70
70
67
68
69
65

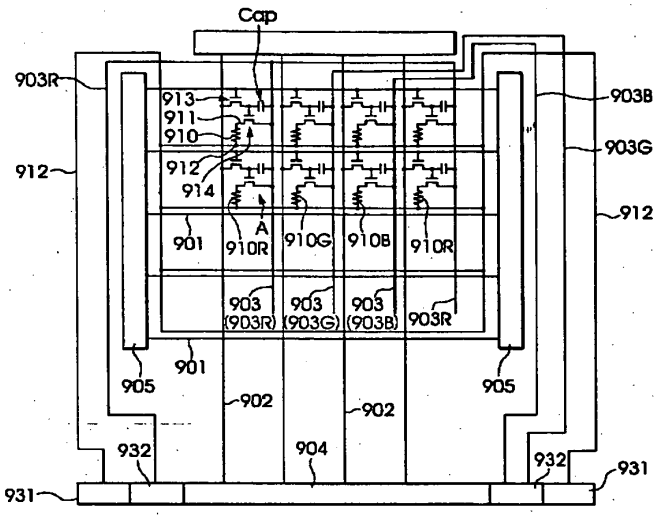
【図７】


68
66c
70
70
79
73
B
H
H
77
79
284
78
283
71
281
60
23R
22
22

【図８】


70
70
79
77
74
75
284
78
283
71
281
60
22
22

【図１１】



フロントページの続き

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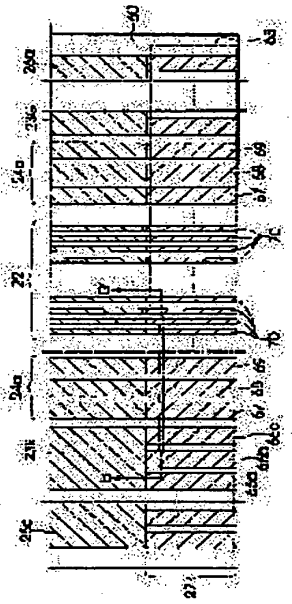
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(54) ELECTROOPTICAL DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electrooptical device in which unevenness in electrical resistivity in a fixed section is resolved by making pressing condition of a display substrate and a relay substrate same over the entire fixed section and generation of display failure such as reduction in contrast is eliminated and to provide electronic equipment having the device.

SOLUTION: The electrooptical device is provided with a display substrate on which a plurality of light emitting elements and a switching element are formed. The switching element supplies currents, which are being supplied through a power supply line such as a light emitting power supply wiring 23R, to the light emitting elements in accordance with the signals supplied through a signal line such as a scanning line driving circuit control signal wiring 24a. The power supply line such as the wiring 23R is formed with a width which is made wider than the signal line such as the wiring 24a. A plurality of external connection terminals such as external connection terminals 66a, 66b and 66c are provided for the power supply line such as the wiring 23R.



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CLAIMS

[Claim(s)]
[Claim 1] The electro-optic device characterized by preparing two or more 2nd external connection terminals to said 2nd wiring in the electro-optic device with which the 1st wiring which it comes to connect with the 1st external connection terminal, and the 2nd wiring larger than the width of face of the 1st wiring concerned were formed at least.
[Claim 2] The electro-optic device according to claim 1 characterized by forming heights in said 1st external connection terminal and said 2nd external connection terminal.
[Claim 3] The electro-optic device according to claim 1 or 2 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal.
[Claim 4] An electro-optic device given in any 1 term of claim 1 to claim 3 to which width of face of said 2nd external connection terminal is characterized by the almost equal thing.
[Claim 5] Said 1st wiring, the 1st junction wiring which has comparable width of face, and said 2nd wiring and the 2nd junction wiring which has comparable width of face are formed. Said 1st wiring and said 1st junction wiring are electrically connected through said 1st external connection terminal. An electro-optic device given in any 1 term of claim 1 to claim 4 characterized by having the junction substrate to which said 2nd wiring and said 2nd junction wiring were electrically connected through said 2nd external connection terminal.
[Claim 6] It is the electro-optic device characterized by forming more widely than the width of face of said signal line the width of face of said power-source line in the electro-optic device with which two or more light emitting devices and the switching element which supplies the current supplied through a power-source line according to the signal supplied through a signal line to each aforementioned light emitting device were formed, and preparing two or more 1st external connection terminals to said power-source line.
[Claim 7] The electro-optic device according to claim 6 characterized by forming heights in the 2nd external connection terminal prepared to said 1st external connection terminal and said signal line.
[Claim 8] The electro-optic device according to claim 6 or 7 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal.
[Claim 9] An electro-optic device given in any 1 term of claim 6 to claim 8 to which width of face of said 2nd external connection terminal is characterized by the almost equal thing.
[Claim 10] Said signal line, the 1st junction wiring which has comparable width of face, and said power-source line and the 2nd junction wiring which has comparable width of face are formed. Said signal line and said 1st junction wiring are electrically connected through said 1st external connection terminal. An electro-optic device given in any 1 term of claim 6 to claim 9 characterized by having the junction substrate to which said power-source line and said 2nd junction wiring were electrically connected through said 2nd external connection terminal.
[Claim 11] The electro-optic device according to claim 10 characterized by said 2nd external connection terminal and said 2nd junction wiring having fixed with the anisotropy electric conduction film in said 1st

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external connection terminal and said 1st junction wiring, and a list.
[Claim 12] Electronic equipment characterized by equipping any 1 term of claim 1 to claim 11 with the electro-optic device of a publication.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to electronic equipment equipped with the electro-optic device which was built over an electro-optic device and electronic equipment, especially was equipped with the organic electroluminescence ingredient, and the electro-optic device concerned.
[0002]
[Description of the Prior Art] In recent years, development of the color electro-optic device of the structure where the light emitting device which consists of luminescent material, such as an organic fluorescence ingredient, between a pixel electrode (anode plate) and cathode was pinched, especially the organic electroluminescence display using the organic electroluminescence (organic electroluminescence) ingredient as a luminescent material is performed. Hereafter, the conventional electro-optic device (organic electroluminescence display) is explained briefly.
[0003] Drawing 11 is drawing showing the wiring structure of the conventional electro-optic device. As shown in drawing 11 , two or more power-source wiring 903 for luminescence with which the conventional electro-optic device is prolonged in parallel to two or more scanning lines 901, two or more signal lines 902 prolonged in the direction in which it crosses to the scanning line 901, and a signal line 902 is wired, respectively, and the pixel field A is formed for each [of the scanning line 901 and a signal line 902] intersection of every. Each signal line 902 is connected to the shift register, the level shifter, the video line, and the data side actuation circuit 904 equipped with an analog switch, and each scanning line 901 is connected to the scan side actuation circuit 905 equipped with a shift register and a level shifter.
[0004] Moreover, the switching thin film transistor 913 by which a scan signal is supplied to each of the pixel field A through the scanning line 901 at a gate electrode, The retention volume Cap holding the picture signal supplied from a signal line 902 through this switching thin film transistor 913, The current thin film transistor 914 by which the picture signal held with retention volume Cap is supplied to a gate electrode, The luminous layer 910 put between the pixel electrode 911 with which an actuation current flows in from the power-source wiring 903 for luminescence when it connects with the power-source wiring 903 for luminescence electrically through this current thin film transistor 914, and this pixel electrode 911 and cathode 912 is formed. Cathode 912 is connected to the power circuit 931 for cathode.

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[0005] Luminous layer 910R which emits light in red, luminous layer 910G which emit light green, and three sorts of light emitting devices of luminous layer 910B which emit light blue are contained in the above-mentioned luminous layer 910, and stripe arrangement of each luminous layers 910R, 910G, and 910B is carried out. And the power-source wiring 903R, 903G, and 903B for luminescence connected to each luminous layers 910R, 910G, and 910B through the current thin film transistor 914 is connected to the power circuit 932 for luminescence, respectively. Power-source wiring for luminescence is wired for every color, because the actuation potentials of a luminous layer 910 differ for every color.
[0006] In the above configuration, if a scan signal is supplied to the scanning line 901 and the switching thin film transistor 913 is turned on, the charge according to the picture signal currently then supplied to the signal line 902 will be held at retention volume Cap. According to the amount of the charge held at this retention volume Cap, the on-off condition of the current thin film transistor 914 is decided. And a current flows to the pixel electrode 911 through the current thin film transistor 914 from the power-source wiring 903R, 903G, and 903B for luminescence, and an actuation current flows to cathode 912 through a luminous layer 910 further. At this time, luminescence of an amount according to the amount of currents which flowed the luminous layer 910 is obtained from a luminous layer 910.
[0007]
[Problem(s) to be Solved by the Invention] The electro-optic device shown in drawing 11 By the way, the scanning line 901, a signal line 902, cathode 912, power-source wiring 903 (903R, 903G, 903B) for luminescence, The scan side actuation circuit 905 and the pixel field A may be formed on transparence substrates (display substrate), such as glass, and the circuit of the power circuit 931 for cathode, the power circuit 932 for luminescence, and data side actuation circuit 904 grade may be considered as the configuration arranged on a flexible substrate (junction substrate) with flexibility.
[0008] It is necessary to make a flexible substrate fix to a substrate in this configuration, and to make it flow through the scanning line 901, a signal line 902, cathode 912, and the power-source wiring 903 for luminescence and the circuit formed on the flexible substrate electrically in it. Fixing and the electric connection between a substrate and a flexible substrate are made by arranging the anisotropy electric conduction film containing an electric conduction particle between a substrate and a flexible substrate, and making a flexible substrate stick to it by pressure to a substrate.
[0009] In order to be stabilized and to make the luminous layer 910 prepared in the electro-optic device mentioned above emit light, it is required that potential fluctuation of the actuation current impressed to the pixel electrode 911 from the power-source wiring 903 for luminescence should be lessened as much as possible. Especially the electro-optic device shown in drawing 1111 is an electro-optic device of a current actuation mold, and in order to prevent the nonconformity on the display of display nonuniformity, contrast lowering, etc., it needs to suppress the voltage drop by wiring resistance of cathode 912 and the power-source wiring 903 for luminescence etc. as much as possible. For this reason, cathode 912 and the power-source wiring 903 for luminescence are formed more broadly than the scanning line 901 and a signal line 902.
[0010] In case it is made to fix with a substrate and a flexible substrate, in order to attain equalization of the electric resistance produced mainly in the sticking-by-pressure section, there is a demand of wanting to make sticking-by-pressure conditions the same all over the fixing section. In order to fill this demand, it is necessary to make the same the configuration of a terminal where it is prepared in the fixing section and various wiring mentioned above is connected.
[0011] However, as mentioned above, since it is an electro-optic device of a current actuation mold, if the voltage drop by wiring resistance etc. is taken into consideration, it is difficult [the electro-optic device shown in drawing 11] for narrowing wiring width of face of cathode 912 and the power-source wiring 903 for luminescence. Moreover, in order to arrange these [all], thinning and since it is necessary to form a ** pitch, it is also difficult [it / as for the scanning line 901 and a signal line 902, there are many numbers, and] to make line breadth of the scanning line 901 and a signal line 902 comparable as the line breadth of cathode 912 and the power-source wiring 903 for luminescence.

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[0012] This invention is made in view of the above-mentioned situation, and it aims at offering electronic equipment equipped with the electro-optic device which does not produce the nonconformity on the display of lowering of contrast etc., and the electro-optic device concerned while it can cancel the heterogeneity of the electric resistance in the fixing section by covering the whole fixing section and making the same the sticking-by-pressure conditions of a display substrate and a junction substrate.
[0013]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the electro-optic device by the 1st viewpoint of this invention is characterized by preparing two or more 2nd external connection terminals to said 2nd wiring in the electro-optic device with which the 1st wiring which it comes to connect with the 1st external connection terminal, and the 2nd wiring larger than the width of face of the 1st wiring concerned were formed at least. According to this invention, since two or more external connection terminals are prepared to the 2nd wiring broader than the 1st wiring, while making a display substrate fix the substrate with which wiring was given, the whole fixing section can be covered and sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc. is not produced. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by forming heights at said 1st external connection terminal and said 2nd external connection terminal. According to this invention, heights are formed in both the 1st external connection terminal prepared to the 1st wiring and the 2nd wiring, and the 2nd external connection terminal. for example, when making a display substrate fix the substrate to which wiring was given by the anisotropy electric conduction film Since the rate of the rate which the electric conduction particle contained in the anisotropy electric conduction film protrudes from the ends of the 1st external connection terminal and the 2nd external connection terminal decreasing, and stopping on an external connection terminal at reverse rises, it is very suitable when reducing the electric resistance in the fixing section. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal. Since the 1st external connection terminal and the 2nd external connection terminal have the composition divided as two or more electrodes so to speak by two or more crevices formed in the front face of the 1st external connection terminal and the 2nd external connection terminal according to this invention, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as the charge condition of the pressure when taking a flow, can equalize more. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by the width of face of said 2nd external connection terminal being almost equal. According to this invention, since the width of face of the 2nd external connection terminal is set up almost equally, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be set as a more desirable condition. Moreover, the electro-optic device by the 1st viewpoint of this invention Said 1st wiring, the 1st junction wiring which has comparable width of face, and said 2nd wiring and the 2nd junction wiring which has comparable width of face are formed. It is characterized by having the junction substrate to which said 1st wiring and said 1st junction wiring were electrically connected to through said 1st external connection terminal, and said 2nd wiring and said 2nd junction wiring were electrically connected through said 2nd external connection terminal. In order to solve the above-mentioned technical problem, the electro-optic device by the 2nd viewpoint of this invention In the electro-optic device with which two or more light emitting devices and the switching element which supplies the current supplied through a power-source line according to the signal supplied through a signal line to each aforementioned light emitting device were formed The width of face of said power-source line is formed more widely than the width of face of said signal line, and it is characterized by preparing two or more 1st external connection terminals to said

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power-source line. [when the power-source line formed broadly and the signal line carried out in thinning and a ** pitch in order to supply many signals are intermingled from the need of supplying a high current in order to obtain luminescence from a light emitting device according to this invention] Since two or more external connection terminals are prepared to the power-source line formed broadly, while making a display substrate fix the substrate with which wiring was given, the whole fixing section can be covered and sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc. is not produced. Moreover, the electro-optic device by the 2nd viewpoint of this invention is characterized by forming heights at the 2nd external connection terminal prepared to said 1st external connection terminal and said signal line. According to this invention, heights are formed in both the 1st external connection terminal prepared to a power-source line and a signal line, and the 2nd external connection terminal. for example, when making a display substrate fix the substrate to which wiring was given by the anisotropy electric conduction film Since the rate of the rate which the electric conduction particle contained in the anisotropy electric conduction film protrudes from the ends of the 1st external connection terminal and the 2nd external connection terminal decreasing, and stopping on an external connection terminal at reverse rises, it is very suitable when reducing the electric resistance in the fixing section. Moreover, the electro-optic device by the 2nd viewpoint of this invention is an electro-optic device according to claim 6 or 7 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal. Since the external connection terminal has composition divided as two or more electrodes so to speak by two or more crevices formed in the front face of the 1st external connection terminal and the 2nd external connection terminal according to this invention, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized more. Moreover, the electro-optic device by the 2nd viewpoint of this invention is characterized by the width of face of said 2nd external connection terminal being almost equal. Moreover, the electro-optic device by the 2nd viewpoint of this invention Said signal line, the 1st junction wiring which has comparable width of face, and said power-source line and the 2nd junction wiring which has comparable width of face are formed. It is characterized by having the junction substrate to which said signal line and said 1st junction wiring were electrically connected to through said 1st external connection terminal, and said power-source line and said 2nd junction wiring were electrically connected through said 2nd external connection terminal. Moreover, as for the electro-optic device by the 2nd viewpoint of this invention, it is desirable that said 2nd external connection terminal and said 2nd junction wiring have fixed with the anisotropy electric conduction film in said 1st external connection terminal and said 1st junction wiring, and a list. The electronic equipment of this invention is characterized by having an electro-optic device given in above any they are.

[0014]

[Embodiment of the Invention] Hereafter, with reference to a drawing, the electro-optic device and electronic equipment by 1 operation gestalt of this invention are explained to a detail. In addition, each drawing referred to by the following explanation has changed the contraction scale for each class or every each part material in order to make each class and each part material the magnitude of extent which can be recognized on a drawing.

[0015] Drawing 1 is the decomposition perspective view showing typically the electro-optic device by 1 operation gestalt of this invention. As shown in drawing 1 , general classification of the electro-optic device 10 of this operation gestalt constitutes it from a display substrate 20 and a junction substrate 30 connected to the display substrate 20. The display substrate 20 is organic electroluminescence equipment of the active matrix which used the thin film transistor (Thin Film Transistor) as a switching element.

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[0016] Two or more scanning lines 21 are formed in this display substrate 20, and two or more signal lines 22 prolonged in the direction which intersects this scanning line 21 are formed in it. Moreover, display device 20a by which two or more formation of the light emitting device was carried out is prepared in the display substrate 20. Furthermore, although the graphic display is omitted in drawing 1 , a power-source line and cathode are formed in the display substrate 20. Moreover, the scanning line 21, the signal line 22, the power-source line that is not illustrated in a list, and the external connection terminal 27 to the cathode of each are formed in the end of the display substrate 20.
[0017] In addition, the electro-optic device 10 shown in drawing 1 should show strictly main configurations typically, and should notice the actual scanning line 21, a signal line 22, and the external connection terminal 27 about the point that a large number are formed on the display substrate 20 with very narrow spacing, respectively. Moreover, the connection condition with the connection condition of the external connection terminal 27 and the scanning line 21 is also omitting the graphic display in drawing 1 .
[0018] Two or more wiring 32 is formed on the base substrate 31 which has flexibility, and the junction substrate 30 is the configuration of having carried the semiconductor chip 33 in the predetermined location of the junction substrate 30 further. The external connection terminal 34 for connecting with wiring and the electric target of the scanning line 21 formed in the display substrate 20 and signal-line 22 grade is formed in the end of wiring 32. In addition, although it is the configuration that only the semiconductor chip 33 was mounted on the junction substrate 30, in drawing 1 , resistance, a capacitor, and other chips may be mounted in the predetermined location of parts other than the part where a semiconductor chip 33 is mounted. Moreover, in order to make an understanding of the structure easy, while wiring 32 and the external connection terminal 34 which are formed in the junction substrate 30 also expand spacing and show it typically, structure is simplified and it has illustrated.
[0019] As shown in drawing 1 , the junction substrate 30 fixes to the display substrate 20 through the anisotropy electric conduction film 40. At this time, the external connection terminal 34 of the junction substrate 30 is electrically connected with the external connection terminal 27 of the display substrate 20 through the anisotropy electric conduction film 40. This anisotropy electric conduction film 40 is formed by distributing much electric conduction particle 41b into thermoplastic or thermosetting resin 41a for adhesion, as it is a high polymer film with the conductivity used in order to give an anisotropy and to make package connection electrically, for example, between the terminals of a couple is shown in drawing 2 R> 2.
[0020] Drawing 2 is the sectional view showing signs that the junction substrate 30 and the display substrate 20 fix with the anisotropy electric conduction film 40. Since electric conduction particle 41b is pinched between the external connection terminal 27 formed in the display substrate 20, and the external connection terminal 34 formed in the junction substrate 30 as shown in drawing 2 , between the external connection terminal 27 and the external connection terminals 34 which are junction wiring will be connected electrically. On the other hand, since a connection terminal does not exist in parts other than the part in which the external connection terminal 27 and the external connection terminal 34 are formed even if electric conduction particle 41b is pinched, the flow has not been taken. Thus, a flow can be taken only between the external connection terminal 27 and the external connection terminal 34.
[0021] In order to make the display substrate 20 and the junction substrate 30 fix using the anisotropy electric conduction film 40, it arranges on the installation base (all are graphic display abbreviations) which has the guide plate with which the front face was made into the split face in the display substrate 20, and vacuum adsorption of the display substrate 20 is carried out. At this time, the display substrate 20 is laid on an installation base so that the part which the junction substrate 30 fixes to the display substrate 20 at least may be located above a guide plate. Reducing the touch area of a guide plate and the display substrate 20, and stopping the heat leakage from a guide plate uses the guide plate with which the front face was made into the split face here, and it is for reducing the temperature applied to the display substrate 20.

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[0022] If installation of a up to [the installation base of the display substrate 20] is completed, the anisotropy electric conduction film 40 will be stuck on the part of the display substrate 20 which the junction substrate 30 fixes, the field in which the semiconductor chip 33 was carried will be turned further down, and alignment of the junction substrate 30 will be performed so that the external connection terminal 34 may be located above the anisotropy electric conduction film 40. The rear face of the field in which the external connection terminal 34 is formed using the heating application-of-pressure head which is not illustrated is heated and pressurized, and while taking a flow with the external connection terminal 34 and the external connection terminal 27 currently formed in the display substrate 20, the display substrate 20 is made to fix the junction substrate 30, after the above process is completed. At this time, the temperature applied to the junction substrate 30 and the display substrate 20 from a heating application-of-pressure head is more than 100 [10] - about 100 degrees C of numbers, and the pressure to apply is several mega PASCAL. The display substrate 20 can be made to fix the junction substrate 30 by passing through the above process.

[0023] Next, the detail of the wiring structure of the electro-optic device 10 of this operation gestalt is explained. Drawing 3 is drawing showing typically the wiring structure of the electro-optic device by 1 operation gestalt of this invention. As shown in drawing 3 , two or more power-source wiring 23 for luminescence with which an electro-optic device 10 is prolonged in parallel to two or more scanning lines 21, two or more signal lines 22 prolonged in the direction in which it crosses to the scanning line 21, and a signal line 22 is wired, respectively, and the pixel field A is formed near [each] the intersection of the scanning line 21 and a signal line 22.

[0024] Data side actuation circuit 33a equipped with a shift register, a level shifter, a video line, and an analog switch is connected to each signal line 22. Moreover, the inspection circuit 25 equipped with a thin film transistor is connected to each signal line 22. Furthermore, the scanning-line actuation circuit 24 equipped with a shift register and a level shifter is connected to each scanning line 21.

[0025] Moreover, the switching thin film transistor 52, retention volume Cap, the current thin film transistor 53, the pixel electrode 51, a luminous layer 50, and cathode 26 are established in each of the pixel field A. The scanning line 21 is connected to the gate electrode, and the switching thin film transistor 52 will be driven according to the scan signal supplied from the scanning line 21, and will be in an ON state or an OFF state. Retention volume Cap holds the picture signal supplied from a signal line 22 through the switching thin film transistor 52.

[0026] As for the current thin film transistor 53, the picture signal with which it connects with the switching thin film transistor 52 and retention volume Cap, and the gate electrode was held with retention volume Cap is supplied to a gate electrode. The pixel electrode 51 is connected to the current thin film transistor 53, and when it connects with the power-source wiring 23 for luminescence electrically through the current thin film transistor 53, an actuation current flows in from the power-source wiring 23 for luminescence. The luminous layer 50 is put between the pixel electrode 51 and cathode 26.

[0027] Three sorts of light emitting devices, luminous layer 50R which emits light in red, luminous layer 50G which emit light green, and luminous layer 50B which emits light blue, are contained in the above and a luminous layer 50, and stripe arrangement of each luminous layers 50R, 50G, and 50B is carried out. And the power-source wiring 23R, 23G, and 23B for luminescence connected to each luminous layers 50R, 50G, and 50B through the current thin film transistor 53 is connected to power circuit 33c for luminescence, respectively. The power-source wiring 23R, 23G, and 23B for luminescence is wired for every color, because the actuation potentials of luminous layers 50R, 50G, and 50B differ for every color.

[0028] Moreover, in the electro-optic device of this operation gestalt, electrostatic capacity C1 is formed between cathode 26 and the power-source wiring 23R, 23G, and 23B for luminescence. Actuation of an electro-optic device 10 accumulates a charge in this electrostatic capacity C1. When the potential of the actuation current which flows each power-source wiring 23 for luminescence during

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actuation of an electro-optic device 10 is changed, the accumulated charge discharges to each power-source wiring 23 for luminescence, and controls potential fluctuation of an actuation current. Thereby, the image display of an electro-optic device 10 can be kept normal.

[0029] In addition, in this electro-optic device 10, if a scan signal is supplied from the scanning line 21 and the switching thin film transistor 52 is turned on, according to the potential with which the potential of the signal line 22 at that time was held at retention volume Cap, and was held at retention volume Cap, the on-off condition of the current thin film transistor 53 will be decided. And through the channel of the current thin film transistor 53, an actuation current flows to the pixel electrode 51 from the power-source wiring 23R, 23G, and 23B for luminescence, and a current flows to cathode 26 through luminous layers 50R, 50G, and 50B further. At this time, luminescence of an amount according to the amount of currents which flowed the luminous layer 50 is obtained from a luminous layer 50.

[0030] Next, the concrete configuration of the electro-optic device 10 of this operation gestalt is explained with reference to drawing 4 and drawing 5 . Drawing 4 is the mimetic diagram of the electro-optic device of this operation gestalt, and drawing 5 is a sectional view which meets the A-A' line of drawing 4 . As shown in drawing 4 , the outline configuration of the electro-optic device 10 of this operation gestalt is carried out from a substrate 60, a non-illustrated pixel electrode group field, the power-source wiring 23 (23R, 23G, 23B) for luminescence, and the display pixel section 61 (within the limit [of the alternate long and short dash line in drawing]).

[0031] A substrate 60 is a transparent substrate which consists of glass etc. A pixel electrode group field is a field which has arranged the pixel electrode (graphic display abbreviation) connected to the current thin film transistor 53 shown in drawing 3 in the shape of a matrix on a substrate 60. As shown in drawing 4 , the power-source wiring 23 (23R, 23G, 23B) for luminescence is arranged around a pixel electrode group field, and is connected to each pixel electrode. The display pixel section 61 is located on a pixel electrode group field at least, and is a plane view abbreviation rectangle configuration. This display pixel section 61 is divided in the real viewing area 62 (within the limit [of the two-dot chain line in drawing]) for a center section (or it is also called an effective viewing area), and the dummy area 63 (field between an alternate long and short dash line and a two-dot chain line) arranged on the outside of the real viewing area 62.

[0032] Moreover, the scanning-line actuation circuit 24 is arranged at the both sides in drawing of the real viewing area 62. This scanning-line actuation circuit 24 is located and established in the lower layer side (substrate 60 side) of a dummy area 63. Furthermore, control signal wiring 24a for scanning-line actuation circuits and power-source wiring 24b for scanning-line actuation circuits which are connected to the scanning-line actuation circuit 24 are prepared in the lower layer side of a dummy area 63. Furthermore, the above-mentioned inspection circuit 25 is arranged at the drawing Nakagami side of the real viewing area 62. This inspection circuit 25 is located and established in the lower layer side (substrate side 2) of a dummy area 63, and inspection of the quality of the electro-optic device at the manufacture middle or the time of shipment and a defect can be conducted by this inspection circuit 25.

[0033] As shown in drawing 4 , the power-source wiring 23R, 23G, and 23B for luminescence is arranged in the perimeter of a dummy area 63. Each power-source wiring 23R, 23G, and 23B for luminescence extends in the method of drawing 4 Nakagami along with control signal wiring 24a for scanning-line actuation circuits from the drawing 2 Nakashita side of a substrate 60, is bent from the location where control signal wiring 24a for scanning-line actuation circuits broke off, extends along the outside of a dummy area 63, and is connected to the pixel electrode of the graphic display abbreviation in the real viewing area 62. Moreover, wiring 26a for cathode connected to cathode 26 is formed in the substrate 60. This wiring 26a for cathode is formed in the shape of a plane view abbreviation KO character so that the power-source wiring 23R, 23G, and 23B for luminescence may be surrounded.

[0034] Next, as shown in drawing 5 , the circuit section 11 is formed on a substrate 60, and the display pixel section 61 is formed on this circuit section 11. Moreover, the sealing agent 13 which surrounds the display pixel section 61 annularly is formed in the substrate 60, and it has the closure substrate 14 on

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the display pixel section 61 further. It is joined to the substrate 60 through the sealing agent 13, and the closure substrate 14 consists of glass, a metal, or resin. An adsorbent 15 is stuck on the background of this closure substrate 14, and the water or oxygen mixed in the space between the display pixel section 61 and the closure substrate 14 can be absorbed now on it. In addition, it may replace with an adsorbent 15 and a getter agent may be used. Moreover, as for a sealing agent 13, it is desirable to consist of for example, heat-curing resin or ultraviolet-rays hardening resin, and to consist of an epoxy resin which is especially a kind of heat-curing resin.

[0035] Pixel electrode group field 11a is prepared in a part for the center section of the circuit section 11. This pixel electrode group field 11a is equipped with the pixel electrode 51 connected to the current thin film transistor 53 and the current thin film transistor 53. The current thin film transistor 53 is embedded at the substrate protective layer 281 by which the laminating was carried out on the substrate 60, the insulating layer 283 between the 2nd layer, and the insulating layer 284 between the 1st layer, it is formed, and the pixel electrode 51 is formed on the insulating layer 284 between the 1st layer. It connects with the current thin film transistor 53, and the power-source wiring 23 (23R, 23G, 23B) for luminescence is connected to one side (source electrode) of the electrode formed on the insulating layer 283 between the 2nd layer. In addition, although the retention volume Cap and the switching thin film transistor 52 which were mentioned above are also formed in the circuit section 11, these graphic displays are omitted in drawing 5 . Furthermore, the graphic display of a signal line 22 is omitted in drawing 5 .

[0036] Next, in drawing 5 , the above-mentioned scanning-line actuation circuit 24 is established in the both sides in drawing of pixel electrode group field 11a. The scanning-line actuation circuit 24 shown in drawing 4 is equipped with thin film transistor 24c of the N channel mold which constitutes the inverter contained in a shift register, or a P channel mold, and this thin film transistor 24c is made into the same structure as the above-mentioned current thin film transistor 53 except for the point which is not connected to the pixel electrode 51. In addition, in drawing 5 , although the graphic display of the inspection circuit 25 is omitted, it has the thin film transistor also like this inspection circuit 25. The thin film transistor with which the inspection circuit 25 is equipped is made into the same structure as the current thin film transistor 53 except for the point which is not connected to dummy pixel electrode 51' mentioned later.

[0037] As shown in drawing 5 , on the substrate protective layer 281 of drawing Chugai of the scanning-line actuation circuit 24, control signal wiring 24a for scanning-line actuation circuits is formed. Moreover, on the insulating layer 283 between the 2nd layer of the outside of control signal wiring 24a for scanning-line actuation circuits, power-source wiring 24b for scanning-line actuation circuits is formed. Moreover, the power-source wiring 23 for luminescence is formed in the outside of power-source wiring 24b for scanning-line actuation circuits. This power-source wiring 23 for luminescence has adopted the duplex wiring structure which consists of two wiring, and as mentioned above, it is arranged on the outside of the display pixel section 61. Wiring resistance is mitigable by adopting duplex wiring structure.

[0038] For example, power-source wiring 23R for luminescence for red in the left-hand side in drawing 5 consists of the 1st wiring 23R1 formed on the substrate protective layer 281, and the 2nd wiring 23R2 formed on the 1st wiring 23R1 through the insulating layer 283 between the 2nd layer. The 1st wiring 23R1 and the 2nd wiring 23R2 are connected by the contact hole 23R3 which penetrates an insulating layer 283 between the 2nd layer as shown in drawing 2 . Thus, the 1st wiring 23R1 is formed in the same hierarchy location as wiring 26a for cathode, and the insulating layer 283 is arranged between the 2nd layer between the 1st wiring 23R1 and wiring 26a for cathode. Moreover, it connects with wiring 26b for cathode formed on the insulating layer 283 between the 2nd layer through the contact hole electrically, and gets down from wiring 26a for cathode, and, so to speak, wiring 26a for cathode also has duplex wiring structure as shown in drawing 5 . Therefore, the 2nd wiring 23R2 is formed in the same hierarchy location as wiring 26b for cathode, and the insulating layer 284 is arranged between the 1st layer

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between the 1st wiring 23R2 and wiring 26b for cathode. By taking such structure, the 2nd electrostatic capacity C2 is formed between the 1st wiring 23R1 and wiring 26a for cathode, and between the 2nd wiring 23R2 and wiring 26b for cathode.

[0039] the 1st by which similarly the blue in the right-hand side of drawing 5 and the power-source wiring 23G and 23B for luminescence for green had also adopted duplex wiring structure, and were formed on the substrate protective layer 281, respectively -- with wiring 23G1 and 23B1 the 2nd formed on the insulating layer 283 between the 2nd layer -- it constitutes from wiring 23G2 and 23 B-2 -- having -- the 1st -- wiring 23G1, 23B1, and the 2nd -- wiring 23G2 and 23 B-2 are connected by contact hole 23 G3 which penetrates an insulating layer 283 between the 2nd layer as shown in drawing 4 , and 23B3. And the 2nd electrostatic capacity C2 is formed between the 1st blue wiring 23B1 and wiring 26a for cathode, and between blue 2nd wiring 23 B-2 and wiring 26b for cathode.

[0040] Spacing of the 1st wiring 23R1 and the 2nd wiring 23R2 has the desirable range of 0.6-1.0 micrometers. Since the parasitic capacitance between the source metal and gate metal which have different potential like a signal line 22 and the scanning line 21 as spacing is less than 0.6 micrometers increases, it is not desirable. For example, many parts where source metal and gate metal cross in the real viewing area 62 exist, and when there is much parasitic capacitance of this part, there is a possibility of causing the time delay of a picture signal. Since a picture signal cannot be written in the pixel electrode 51 within the defined period as the result, lowering of contrast is caused. Between the 2nd layer inserted into the 1st wiring 23R1 and the 2nd wiring 23R2, although the construction material of an insulating layer 283 has for example, desirable SiO2 grade, if 1.0 micrometers or more are formed, a possibility that a substrate 60 may break with the stress of SiO2 will arise.

[0041] Moreover, the cathode 26 which extended from the display pixel section 61 is formed in each power-source wiring 23R upside for luminescence. Thereby, on both sides of an insulating layer 284, opposite arrangement of the 2nd wiring 23R2 of each power-source wiring 23R for luminescence is carried out with cathode 26 between the 1st layer, and the 1st above-mentioned electrostatic capacity C1 is formed between the 2nd wiring 23R2 and cathode 26. Here, spacing of the 2nd wiring 23R2 and cathode 26 has the desirable range of 0.6-1.0 micrometers. If spacing is less than 0.6 micrometers, since the parasitic capacitance between the pixel electrodes and source metal which have different potential like a pixel electrode and source metal will increase, the wiring delay of a signal line which uses source metal arises. Consequently, since a picture signal cannot be written in within the defined period, lowering of contrast is caused. The construction material of an insulating layer 284 has SiO2, desirable acrylic resin, etc. between the 1st layer inserted into the 2nd wiring 23R2 and cathode 26. However, formation of 1.0 micrometers or more of SiO(s)2 produces a possibility that a substrate 60 may break with stress. Moreover, in the case of acrylic resin, it can form to about 2.0 micrometers, but since there is a property to expand if water is included, there is a possibility of breaking the pixel electrode formed on it.

[0042] Thus, to the display substrate 20, since the 1st electrostatic capacity C1 is formed between the power-source wiring 23 for luminescence, and cathode 26 The charge accumulated in the 1st electrostatic capacity C1 when the potential of the actuation current which flows the power-source wiring 23 for luminescence was changed is supplied to the power-source wiring 23 for luminescence. The potential insufficiency of an actuation current can be compensated with this charge, can control potential fluctuation, and can keep the image display of luminescence equipment 1 normal. Since the power-source wiring 23 for luminescence and cathode 26 have countered especially on the outside of the display pixel section 61, the amount of charges which makes small spacing of the power-source wiring 23 for luminescence and cathode 26, and is accumulated in the 1st electrostatic capacity C1 can be increased, potential fluctuation of an actuation current can be made smaller, and image display can be carried out to stability. Furthermore, since it has the duplex wiring structure where the power-source wiring 23 for luminescence consists of the 1st wiring and the 2nd wiring, the 2nd electrostatic capacity C2 is formed between the 1st wiring and wiring for cathode and the charge accumulated in the 2nd electrostatic capacity C2 is also supplied to the power-source wiring 23 for luminescence, potential

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fluctuation can be controlled more and the image display of luminescence equipment 1 can be maintained more at normal.

[0043] Next, a luminous layer 50 and the bank section (insulating section) 122 are formed in the real pixel field 62 of the display pixel section 61. As shown in drawing 5 , the laminating of the luminous layer 50 is carried out to each on the pixel electrode 51. Moreover, it has the bank section 122 between each pixel electrode 51 and each luminous layer 50, and it has divided each luminous layer 50. The laminating of the organic substance bank layer 122b separated and located is carried out, and the bank section 122 consists of inorganic substance bank layer 122a and the substrates 60 which are located in a substrate 60 side. In addition, a protection-from-light layer may be arranged between inorganic substance bank layer 122a and organic substance bank layer 122b.

[0044] Extension formation of them is carried out until an inorganic substance and the organic substance bank layers 122a and 122b run aground on the periphery section of the pixel electrode 51, and extension formation of the inorganic substance bank layer 122a is carried out rather than organic substance bank layer 122b at the central site of the pixel electrode 51. Moreover, as for inorganic substance bank layer 122a, it is desirable to consist of inorganic materials, such as SiO2, TiO2, and SiN. Moreover, the thickness of inorganic substance bank layer 122a has the desirable range of 50-200nm, and especially its 150nm is good. Since thickness becomes thin and it becomes impossible to secure the surface smoothness of a hole injection/transporting bed from the hole injection/transporting bed which inorganic substance bank layer 122a mentions later in less than 50nm, it is not desirable. Moreover, since it becomes impossible to secure the surface smoothness of the below-mentioned luminous layer which carries out a laminating on a hole injection/transporting bed by the level difference by inorganic substance bank layer 122a becoming large when thickness exceeds 200nm, it is not desirable.

[0045] Furthermore, organic substance bank layer 122b is formed from the usual resists, such as acrylic resin and polyimide resin. The thickness of this organic substance bank layer 122b has the desirable range of 0.1-3.5 micrometers, and especially its about 2 micrometers are good. Since there is a possibility that organic substance bank layer 122b may become thin, and a luminous layer may overflow from up opening from the total thickness of the hole injection / transporting bed which thickness mentions later in less than 0.1 micrometers, and a luminous layer, it is not desirable. Moreover, since it becomes impossible to secure the step coverage of the cathode 26 formed on organic substance bank layer 122b by the level difference by up opening becoming large when thickness exceeds 3.5 micrometers, it is not desirable. Moreover, if thickness of organic substance bank layer 122b is set to 2 micrometers or more, it is more desirable at the point which can raise the insulation with cathode 26 and the pixel electrode 51. Thus, the luminous layer 50 is formed more thinly than the bank section 122.

[0046] Moreover, the field which shows lyophilic, and the field which shows liquid repellance are formed around the bank section 122. The fields which show lyophilic are inorganic substance bank layer 122a and the pixel electrode 51, and lyophilic groups, such as a hydroxyl group, are introduced into these fields by the plasma treatment which makes oxygen reactant gas. Moreover, the field which shows liquid repellance is organic substance bank layer 122b, and **** machines, such as a fluorine, are introduced by the plasma treatment which makes 4 methane fluoride reactant gas.

[0047] The laminating of the luminous layer 50 is carried out on the hole injection/transporting bed by which the laminating was carried out on the pixel electrode 51 and which is not illustrated. In addition, on these descriptions, the configuration containing a luminous layer 50, and a hole injection/transporting bed is called stratum functionale, and the pixel electrode 51, the stratum functionale, and the configuration included cathode 26 are called light emitting device. A hole injection/transporting bed has the function to convey an electron hole in the interior of a hole injection/transporting bed while having the function to pour an electron hole into a luminous layer 50. By preparing such a hole injection/a transporting bed between the pixel electrode 51 and a luminous layer 50, component properties, such as luminous efficiency of a luminous layer 50 and a life, improve. Moreover, in a luminous layer 50, the electron hole poured in from the hole injection/transporting bed and the electron from cathode 26 join

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together, and fluorescence is generated. A luminous layer 50 has three kinds, the red luminous layer which emits light in red (R), the green luminous layer which emits light in green (G), and the blue luminous layer which emits light in blue (B), and as shown in drawing 3 and drawing 4 , stripe arrangement of each luminous layer is carried out.

[0048] Next, as shown in drawing 5 , the dummy luminous layer 210 and the dummy bank section 212 are formed in the dummy area 63 of the display pixel section 61. The laminating of the dummy organic substance bank layer 212b separated and located is carried out, and the dummy bank section 212 consists of dummy inorganic substance bank layer 212a and the substrates 60 which are located in a substrate 60 side. Dummy inorganic substance bank layer 212a is formed all over dummy pixel electrode 51'. Moreover, dummy organic substance bank layer 212b is formed between the pixel electrodes 51 like organic substance bank layer 122b. And the dummy luminous layer 210 is formed on dummy pixel electrode 51' through dummy inorganic substance bank 212a.

[0049] Dummy inorganic substance bank layer 212a and dummy organic substance bank layer 211b have the inorganic substance explained previously, the same construction material as the organic substance bank layers 122a and 122b, and the same thickness. Moreover, the laminating of the dummy luminous layer 210 is carried out on the dummy hole injection / transporting bed of graphic display abbreviation, and the construction material and thickness of a dummy hole injection / transporting bed, and a dummy luminous layer of it are the same as that of the above-mentioned hole injection / transporting bed, and a luminous layer 50. Therefore, the dummy luminous layer 210 is formed like the above-mentioned luminous layer 50 more thinly than the dummy bank section 212.

[0050] By arranging a dummy area 63 around the real viewing area 62, thickness of the luminous layer 50 of the real viewing area 62 can be made into homogeneity, and display nonuniformity can be controlled. That is, the desiccation conditions of the breathed-out constituent ink in the case of forming a display device by the ink jet method by arranging a dummy area 63 can be made regularity within the real viewing area 62, and there is no possibility that a bias may arise in the thickness of a luminous layer 50 in the periphery section of the real viewing area 62.

[0051] Next, cathode 26 extends on the substrate 60 on the outside of a dummy area 63 while being formed all over the real viewing area 62 and a dummy area 63, and opposite arrangement is carried out with the power-source wiring 23 for luminescence on the outside of a dummy area 63, i.e., the outside of the display pixel section 61. Moreover, the edge of cathode 26 is connected to wiring 26a for cathode formed in the circuit section 11. Cathode 26 plays the role which passes a current to a luminous layer 50 as a counterelectrode of the pixel electrode 51. The laminating of catholyte 26b and reflecting layer 26c which consist of a layered product of lithium fluoride and calcium is carried out, and this cathode 26 is constituted. Only reflecting layer 26c has extended to the outside of the display pixel section 61 among cathode 26. As for reflecting layer 26c, it is desirable to reflect in a substrate 60 side the light emitted from the luminous layer 50, and to consist of aluminum, Ag, a Mg/Ag layered product, etc. Furthermore, the protective layer for antioxidizing which consists of SiO2, SiN, etc. may be prepared on reflecting layer 26c.

[0052] Moreover, as shown in drawing 4 , at the end of a substrate 60, the junction substrate 30 has fixed using the anisotropy electric conduction film 40 mentioned above. In addition, data side actuation circuit 33a shown in drawing 3 , power circuit 33for cathode b, and power circuit 33c for luminescence are built in the semiconductor chip 33 carried on the junction substrate 30. The part enclosed with the broken line in drawing 4 shows the fixing section of the display substrate 20 and the junction substrate 30. Drawing 6 is the plan of the fixing section 65 neighborhood shown in drawing 4 . In addition, in drawing 6 , the graphic display of the anisotropy electric conduction film 40 and the junction substrate 30 is omitted.

[0053] As shown in drawing 6 , in the fixing section 65, the 1st external connection terminal which has width of face comparable as the width of face of wiring to thin wiring of each of line breadth is prepared, and two or more 2nd external connection terminals with width of face narrower than line breadth are

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prepared to broad wiring. For example, to each of control signal wiring 24a for scanning-line actuation circuits with thin line breadth, the 1st external connection terminals 67, 68, and 69 which have width of face comparable as the line breadth of control signal wiring 24a for scanning-line actuation circuits are formed. On the other hand, to power-source wiring 23R for luminescence with wide width of face, the 2nd external connection terminals 66a, 66b, and 66c with width of face narrower than the line breadth of power-source wiring 23R for luminescence are formed. Moreover, the 2nd external connection terminal 70 which has line breadth comparable as a signal line 22 to the signal line 22 with narrow width of face rather than control signal wiring 24a for scanning-line actuation circuits is formed, respectively. In addition, the number of the 1st external connection terminal and the 2nd external connection terminals is suitably set up according to the line breadth of wiring formed in a substrate 60.

[0054] Thus, according to the line breadth of wiring formed in the substrate 60, the number of the 1st external connection terminal and the 2nd external connection terminals is changed for continuing all over the fixing section 65 and making sticking-by-pressure conditions the same as much as possible. That is, as explained using drawing 1 and drawing 2 , although the display substrate 10 and the junction substrate 20 fix with the anisotropy electric conduction film 40, when fixing conditions (for example, the width of face of a terminal, adhesion area, charge condition of a pressure, etc.) differ, the electric resistance in the fixing section 65 interior differs according to the location. If the electric resistance in the fixing section 65 differs according to a location, the nonconformity on the display of display nonuniformity, contrast lowering, etc. will be produced. For this reason, in the fixing section 65, sticking-by-pressure conditions are made the same as much as possible by changing the number of external connection terminals according to the line breadth of wiring formed in the substrate 60. Furthermore, adhesion area can be increased by preparing two or more external connection terminals. That is, since the anisotropy electric conduction film can be arranged among two or more external connection terminals n, firm adhesion is attained.

[0055] Next, the structure of the external connection terminal formed in the fixing section 65 is explained to a detail. Drawing 7 is the sectional view of the 2nd external connection terminal 66c and the 2nd external connection terminal 70 which meet the B-B' line in drawing 6 , and drawing 8 is the enlarged drawing of the external connection terminal 70 in drawing 7 . As shown in drawing 7 and drawing 8 , the substrate protective layer 281 is formed on the substrate 60, and the gate insulating layer 71 which makes SiO2 and/or SiN a subject is formed on this substrate protective layer 281. This gate insulating layer 71 is formed in order to insulate electrically the channel field and gate electrode of a thin film transistor which are not illustrated. In addition, in this description, the component made into a "subject" shall mean a component with the highest content.

[0056] On the gate insulating layer 71, a signal line 22 and power-source wiring 23R for luminescence are formed, and the insulating layer 283 is further formed between the 2nd layer on a signal line 22 and power-source wiring 23R for luminescence. Moreover, the power-source wiring 23 for luminescence and control signal wiring 24a for scanning-line actuation circuits are formed in drawing 3 simultaneously with the scanning line 21 of a publication.

[0057] Two or more formation of the contact hole H is carried out in the up location of a signal line 22 and power-source wiring 23R for luminescence at the above-mentioned insulating layer 283 between the 2nd layer. Moreover, an electrode 73 is formed on the insulating layer 283 between the 2nd layer above power-source wiring 23R for luminescence, and electrodes 74 and 75 are formed on the upper insulating layer 283 between the 2nd layer of a signal line 22.

[0058] Since these electrodes 73, 74, and 75 are formed by the sputtering method etc. after they form a contact hole H, Crevice B is formed in a front face only for the part of the metallic material deposited in the contact hole H in the upper part of a contact hole H. Thus, a flow with power-source wiring 23R for luminescence covered with the insulating layer 283 between the 2nd layer and the electrode 74 formed on the insulating layer 283 between the 2nd layer and the flow of the signal line 22 covered with the insulating layer 283 between the 2nd layer and the electrodes 74 and 75 formed on the insulating layer

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283 between the 2nd layer are taken through a contact hole H.
[0059] Moreover, between the edge of the electrodes 73, 74, and 75 formed on the insulating layer 283 between the 2nd layer, flanks and these electrodes 73 and 74, and 75, while [the 1st layer] consisting of inorganic materials, such as SiN aiming at an electric insulation, the insulating layer 284 is formed. Between the transparent electrode 77 which the transparent electrode 77 which consists of ITO etc. was formed, and was further formed in the periphery of electrodes 73, 74, and 75 and the 2nd external connection terminals 66c and 70, and 70, the protective layer 78 which consists of SiO2 is formed in the upper part of electrodes 73, 74, and 75, the flank, and the periphery. In addition, electrodes 73, 74, and 75 are formed in the gate line and coincidence which are indicated by drawing 3 , and a transparent electrode 77 is formed of ITO and formed simultaneously with a pixel electrode (anode plate).
[0060] As shown in drawing 7 and drawing 8 , two or more crevices B are formed in the front face of the 2nd external connection terminals 66c, 70, and 70 established in the electro-optic device of this operation gestalt, and it is carried out, and has the composition that so to speak this crevice B divided the 2nd external connection terminals 66c, 70, and 70 as two or more electrodes. Although equalization of the fixing conditions in the fixing section 65 is in drawing by changing the number of external connection terminals according to the line breadth of power-source wiring 23for luminescence R, and a signal line 22 as shown in drawing 6 Since two or more crevices B are formed in the front face of the 2nd external connection terminals 66c, 70, and 70, the 2nd external connection terminals 66c, 70, and 70 are very suitable, when becoming what was divided into further two or more electrodes and attaining equalization of fixing conditions.
[0061] Moreover, heights 79 are formed in the edge of the 2nd external connection terminals 66c, 70, and 70 by forming an insulating layer 284 in the edge of electrodes 73, 74, and 75 between the 1st layer. In case these heights 79 fix the display substrate 10 and the junction substrate 20 using the anisotropy electric conduction film 40, they act so that it may prevent that electric conduction particle 41b contained in the anisotropy electric conduction film 40 overflows into the flank of the 2nd external connection terminals 66c, 70, and 70. Consequently, since more electric conduction particle 41b will be arranged on the 2nd external connection terminals 66c and 70 and 70, it is the extremely excellent structure which reduces the electric resistance in the fixing section 65.
[0062] since a configuration for the display substrate 20 of this operation gestalt explained a substrate above to equalize sticking by pressure conditions in the fixing section 65 be prepare , form the external connection terminal 34 form in the junction substrate 30 which fix to the fixing section 65 with the same line breadth as the power source wiring 23for luminescence R and the control signal wiring 24for scanning line actuation circuits a a be show in drawing 6 . However, in order to fix the junction substrate 30 and the display substrate 20 under more uniform sticking-by-pressure conditions, it is suitable that it is the same pattern as the 2nd external connection terminals 66c and 70 and 70 grades which were formed in the fixing section 65.
[0063] As mentioned above, although the electro-optic device by 1 operation gestalt of this invention was explained, the personal computer 600 (electronic equipment) of a note type shown in drawing 9 is manufactured by incorporating in a case electronic parts, such as a mother board equipped with the electro-optic device explained above, CPU (central processing unit), etc., a keyboard, and a hard disk. Drawing 9 is drawing showing an example of electronic equipment equipped with the electro-optic device by 1 operation gestalt of this invention. In addition, in drawing 9 , 601 is a case, 602 is a liquid crystal display, and 603 is a keyboard. Drawing 10 is the perspective view showing the portable telephone as other electronic equipment. The portable telephone 700 shown in drawing 10 is equipped with an antenna 701, an earphone 702, a telephone transmitter 703, a liquid crystal display 704, and operating button section 705 grade, and is constituted.
[0064] Moreover, although the notebook computer and the portable telephone were mentioned as the example and the above-mentioned operation gestalt explained them as electronic equipment, it is possible to apply to electronic equipment, such as equipment equipped with the video tape recorder of

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not only these but a liquid crystal projector, the personal computer corresponding to multimedia (PC) and an engineering workstation (EWS), a pager, a word processor, television, a viewfinder mold, or a monitor direct viewing type, an electronic notebook, an electronic calculator, car navigation equipment, the POS terminal, and the touch panel.

[0065]

[Effect of the Invention] Since two or more 2nd external connection terminals are prepared to the 2nd wiring broader than the 1st wiring according to this invention, while making a display substrate fix the substrate with which wiring was given as explained above, it is effective in the ability to cover the whole fixing section and equalize sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and it is effective in not producing nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the decomposition perspective view showing typically the electro-optic device by 1 operation gestalt of this invention.

[Drawing 2] It is the sectional view showing signs that the junction substrate 30 and the display substrate 20 fix with the anisotropy electric conduction film 40.

[Drawing 3] It is drawing showing typically the wiring structure of the electro-optic device by 1 operation gestalt of this invention.

[Drawing 4] It is the mimetic diagram of the electro-optic device of this operation gestalt.

[Drawing 5] It is the sectional view which meets the A-A' line of drawing 4 .

[Drawing 6] It is the plan of the fixing section 65 neighborhood shown in drawing 4 .

[Drawing 7] It is the sectional view of the 2nd external connection terminal 66c and the 2nd external connection terminal 70 which meet the B-B' line in drawing 6 .

[Drawing 8] It is the enlarged drawing of the external connection terminal 70 in drawing 7 .

[Drawing 9] It is drawing showing an example of electronic equipment equipped with the electro-optic device by 1 operation gestalt of this invention.

[Drawing 10] It is the perspective view showing the portable telephone as other electronic equipment.

[Drawing 11] It is drawing showing the wiring structure of the conventional electro-optic device.

[Description of Notations]

10 .... Electro-optic device

20 .... Display substrate

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22 .... Signal line (the 1st wiring)
23 23R .... Power-source wiring for luminescence (the 2nd wiring, power-source line)
24a .... Control signal wiring for scanning-line actuation circuits (the 1st wiring)
30 .... Junction substrate
40 .... Anisotropy electric conduction film
50 .... Light emitting device
53 .... Switching element
66a, 66b, 66c .... The 2nd external connection terminal
67, 68, 69, 70 .... The 1st external connection terminal
79 .... Heights
B .... Crevice

[Translation done.]

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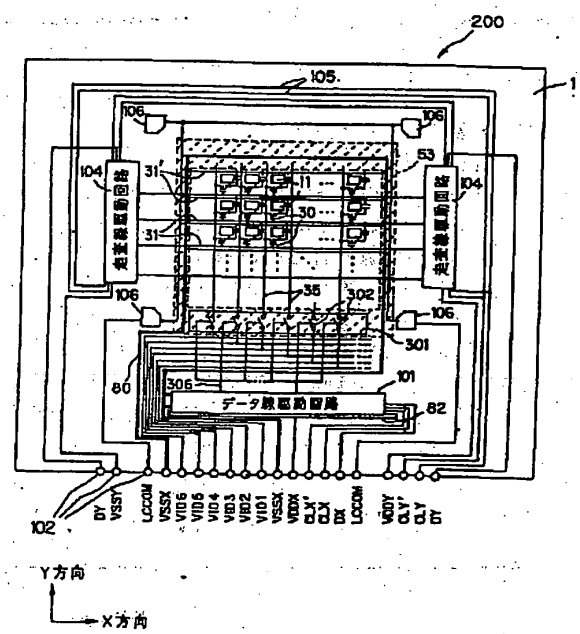
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(57)【要約】

【課題】　アクティブマトリクス駆動方式の液晶装置等の電気光学装置において、入力された画像信号中やこれに基づいて生成されるデータ信号中の高周波のクロックノイズの発生を低減する。

【解決手段】　液晶装置（２００）は、一対の基板間に挟持された液晶層と、基板（１）にマトリクス状に設けられた画素電極（１１）と、これをスイッチング制御するＴＦＴ（３０）とを備える。画像信号線（ＶＩＤ１～ＶＩＤ６）をクロック信号線（ＣＬＸ、ＣＬＸ'）から電気的にシールドする定電位のシールド線（８０、８２）が基板上に配線されている。



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【特許請求の範囲】

【請求項１】　基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、クロック信号に基づいて画像信号に対応するデータ信号を前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力される前記画像信号を前記データ信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする電気光学装置。

【請求項２】　前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むことを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、

該第１定電位線から構成された前記導電線部分は、前記基板上で前記画像信号線を囲み、

前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むことを特徴とする請求項２に記載の電気光学装置。

【請求項４】　前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていることを特徴とする請求項２又は３に記載の電気光学装置。

【請求項５】　前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていることを特徴とする請求項２から４のいずれか一項に記載の電気光学装置。

【請求項６】　前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記第１基板上で囲むように延設されたこと特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、

前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むことを特徴とする請求項６に記載の電気光学装置。

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【請求項８】　前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。

【請求項９】　前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されたことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

【請求項１０】　前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていることを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。

【請求項１２】　請求項１から１１に記載の電気光学装置を備えたことを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、薄膜トランジスタ（以下適宜、ＴＦＴと称す）駆動によるアクティブマトリクス駆動方式の電気光学装置及びこれを用いた電子機器の技術分野に属し、特に、ＴＦＴアレイ基板上に設けられたデータ線駆動回路によりクロック信号に基づいてデータ線を高周波で駆動する形式の電気光学装置及びこれを用いた電子機器の技術分野に属する。

【０００２】

【従来の技術】従来、ＴＦＴ駆動によるアクティブマトリクス駆動方式の液晶装置等の電気光学装置においては、縦横に夫々配列された多数の走査線及びデータ線並びにこれらの各交点に対応して多数の画素電極がＴＦＴアレイ基板上に設けられている。そして、これらに加えて、データ線駆動回路、サンプリング回路等を含みデータ線にデータ信号を供給するデータ信号供給手段や、走査線駆動回路等を含み走査線に走査信号を供給する走査信号供給手段が、このようなＴＦＴアレイ基板上に設けられる場合がある。

【０００３】この場合、データ信号供給手段には、データ信号の供給タイミングの基準となるデータ線側基準クロック、表示すべき画像の内容に対応しておりデータ信号の基となる画像信号、正や負の定電位電源等が、ＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して夫々供給される。他方、走査信号供給手段には、走査

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信号の供給タイミングの基準となる走査線側基準クロック、正や負の定電位電源等が、やはりＴＦＴアレイ基板に設けられた外部入力端子及び配線を介して供給される。そして走査信号供給手段においては、例えば走査線駆動回路により、走査線側基準クロックに基づくタイミングで走査信号を走査線に線順次で供給する。これに対応してデータ信号供給手段においては、例えば入力された画像信号をサンプリングするサンプリング回路を、データ線駆動回路がデータ線側基準クロックに基づくタイミングで順次駆動して、サンプリング回路からデータ信号がデータ線に供給される。これらの結果、走査線にゲート接続された各ＴＦＴは、走査信号の供給に応じて導通状態とされ、データ信号が当該ＴＦＴを介して画素電極に供給されて各画素における画像表示が行われる。

【０００４】近年特に、液晶プロジェクタ用の液晶装置等では、表示画像の高解像度化に伴って、非常に高い周波数のシリアルな画像信号が入力されるようになってきている。これに対応すべく、特にデータ信号供給手段に供給されるデータ線側基準クロックの周波数も非常に高くされる。

【０００５】

【発明が解決しようとする課題】しかしながら、近年の表示画像の高品位化の要請の下では、このように基準クロックの周波数を高くすることによる、高周波のクロックノイズの発生が無視し得ないようになる。

【０００６】即ち、例えば従来の比較的周波数の低いデータ線側基準クロックをデータ線駆動回路に供給してサンプリング回路を駆動する構成において、そのままクロック信号の周波数を上げたのでは、サンプリング回路に入力される画像信号中やサンプリング回路から出力されるデータ信号中に高周波のクロックノイズが発生して、データ線に供給すべきデータ信号が劣化してしまう。このように劣化したデータ信号の供給を受けたのでは、各画素電極により表示される画像もやはり劣化してしまうという問題点がある。

【０００７】本発明は上述の問題点に鑑みなされたものであり、入力された画像信号中やこれに基づいて生成されるデータ信号中の高周波のクロックノイズの発生を低減でき、高品位の画像表示を行える電気光学装置及び当該電気光学装置を備えた電子機器を提供することを課題とする。

【０００８】

【課題を解決するための手段】請求項１に記載の電気光学装置は上記課題を解決するために、基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線に接続された複数のスイッチング素子と、前記複数のスイッチング素子に接続された複数の画素電極と、クロック信号に基づいて画像信号に対応するデータ信号を前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力

される前記画像信号を前記データ信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする。

【０００９】請求項１に記載の電気光学装置によれば、第１外部入力端子から入力される画像信号は、基板に配線された画像信号線を介して、データ信号供給手段に供給される。これと並行して、第２外部入力端子から入力されるクロック信号は、基板に配線されたクロック信号線を介して、データ信号供給手段に供給される。すると、基板に設けられた、例えばデータ線駆動回路、サンプリング回路等を含んで構成されるデータ信号供給手段により、クロック信号に基づいて画像信号に対応するデータ信号が、複数のデータ線に供給される。ここで特に、基板に配線された定電位の導電線により、画像信号線は、クロック信号線から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。

【００１０】他方で、基板に形成されるか又は基板に接続された走査線駆動回路等を含む走査信号供給手段により、走査信号が走査線を介してスイッチング素子に供給される。これと並行して、上述のように高周波のクロックノイズが低減された画像信号に対応するデータ信号が、データ線を介してスイッチング素子に供給され、更にスイッチング素子を介して供給されるデータ信号により画素電極に印加される電圧が変化し、当該画素電極に対向する液晶が駆動される。以上の結果、表示すべき画像の解像度が高く、高周波のシリアルな画像信号が入力される場合にも、これに対応して周波数が高いクロック信号を用いつつ、高周波のクロックノイズの発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。

【００１１】請求項２に記載の電気光学装置は請求項１に記載の電気光学装置において、前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むことを特徴とする。

【００１２】請求項２に記載の電気光学装置によれば、導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むので、外部入力端子や配線そのものを共用することにより、言い換えれば定電位線を延設して導電線とすることにより、構成の簡略化と省スペース化を図ることが出来、特に導電線を定電位とすることも極めて容易となる。

【００１３】請求項３に記載の電気光学装置は請求項２に記載の電気光学装置において、前記定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、該第１定電位線から構

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成された前記導電線部分は、前記基板上で前記画像信号線を囲み、前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むことを特徴とする。

【００１４】請求項３に記載の電気光学装置によれば、画像信号線は、例えば接地電位の負電源を供給するための第１定電位線から構成された導電線部分により、基板上で囲まれている。クロック信号線は、例えば正電源を供給するための第２定電位線から構成された導電線部分により、基板上で囲まれている。従って、画像信号線は、基板上でクロック信号線から２重にシールドされた構成が得られる。

【００１５】請求項４に記載の電気光学装置は請求項２又は３に記載の電気光学装置において、前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていることを特徴とする。

【００１６】請求項４に記載の電気光学装置によれば、走査信号供給手段において、画像信号は、サンプリング回路によりサンプリングされる。そして、定電位線からの電源供給を受けるデータ線駆動回路により、クロック信号に基づいてサンプリング回路が駆動されて、サンプリングされた画像信号がデータ信号としてデータ線に供給される。ここで特に、画像信号線とクロック信号線とは、基板上でデータ線駆動回路に対して反対方向から引き回されているが、一般に距離及び障害物の介在に応じて電磁波は減少するので、クロック信号線から画像信号線に印加される電磁波が両信号線間の距離に応じて且つデータ線駆動回路の存在に応じて減少する。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを更に低減できる。

【００１７】請求項５に記載の電気光学装置は請求項２から４のいずれか一項に記載の電気光学装置において、前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていることを特徴とする。

【００１８】請求項５に記載の電気光学装置によれば、第１及び第２外部入力端子は、第３外部入力端子を間に介して、基板の周辺部において相互に所定間隔を隔てて配置されており、好ましくは、基板の周辺部において外部入力端子を形成可能な領域において可能な限り相互に離して配置される。従って、例えば画像信号線とクロック信号線とを隣接配置した場合と比較して、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。

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【００１９】請求項６に記載の電気光学装置は請求項１から５のいずれか一項に記載の電気光学装置において、前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記基板上で囲むように延設されたこと特徴とする。

【００２０】請求項６に記載の電気光学装置によれば、導電線により、画像表示領域及び複数のデータ線は、基板上で囲まれているので、当該画像表示領域及び複数のデータ線も、クロック信号線からシールドされることになる。従って、データ信号供給手段から出力されたデータ信号、スイッチング素子や画素電極に到達したデータ信号等における、高周波のクロックノイズの発生を低減できる。

【００２１】請求項７に記載の電気光学装置は請求項６に記載の電気光学装置において、前記基板に対向して対向基板が設けられてなり、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むことを特徴とする。

【００２２】請求項７に記載の電気光学装置によれば、導電線は、基板の額縁下に設けられているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。

【００２３】請求項８に記載の電気光学装置は請求項１から７のいずれか一項に記載の電気光学装置において、前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする。

【００２４】請求項８に記載の電気光学装置によれば、導電線は例えば、Ａｌ（アルミニウム）等の、データ線と同一の低抵抗金属材料から形成されているので、導電線の引き回し領域が、たとえ長くても、導電線の抵抗は実用上十分に低く抑えられる。即ち、抵抗増加によりシールドの効果を下げることなく、例えば他の配線や回路等の隙間を縫ってジグザグに導電線を長く配線したり、画像表示領域等までも含めた広い領域に導電線を長く配線することが可能となるので、比較的簡単な構成により、当該シールドの効果を全体として、より高めることが出来る。更に、当該電気光学装置の製造プロセスにおいて、導電線及びデータ線を、同一の低抵抗金属材料から同一工程により形成できる。即ち、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。

【００２５】請求項９に記載の電気光学装置は請求項１から８のいずれか一項に記載の電気光学装置において、

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前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記第１基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されたことを特徴とする。

【００２６】請求項９に記載の電気光学装置によれば、画像信号線及びクロック信号線の間に介在する導電線部分は、画像信号線やクロック信号線と、基板に平行な同一平面上に形成されているので、シールドの効果がより効率良く発揮される。ここで、同一平面上とは、基板の上に直接これらを配線してもよく、或いは基板上に形成された下地となる絶縁層上やＴＦＴ等のスイッチング素子の半導体層上に形成された層間絶縁層上にこれらを配線してもよいという意味である。更に、当該電気光学装置の製造プロセスにおいて、導電線、画像信号線及びクロック信号線を、例えば、Ａｌ層等の同一の低抵抗金属層から一括して形成できるので、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。

【００２７】請求項１０に記載の電気光学装置は請求項１から９のいずれか一項に記載の電気光学装置において、前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする。

【００２８】請求項１０に記載の電気光学装置によれば、容量線により画素電極に所定量の容量が付与されているので、デューティー比が小さくても高精細な表示が可能とされる。そして、容量線は導電線に接続されている。従って、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。

【００２９】請求項１１に記載の電気光学装置は、前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていることを特徴とする。

【００３０】請求項１１に記載の電気光学装置によれば、導電線は、基板の額縁に対向配置されているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。また、容量線は導電線に接続されているため、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。また、導電線と容量線との接続は額縁に対向配置されるため、ＴＦＴ基板上有効表示面積を減少させることなく、スペースを有効利用することができる。

【００３１】請求項１２に記載の電子機器は、請求項１から１０に記載の電気光学装置を備えたことを特徴とする。

【００３２】請求項１２に記載の電子機器によれば、電子機器は、上述した本願発明の電気光学装置を備えており、高周波のクロックノイズが低減されており、高品位の画像表示が可能となる。

【００３３】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにする。

【００３４】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて説明する。尚、本実施形態では電気光学装置の一例として液晶装置を用いて説明する。

【００３５】（液晶装置の構成）液晶装置の実施の形態の構成について図１から図６に基づいて説明する。図１は、液晶装置の実施の形態におけるＴＦＴアレイ基板上に設けられた各種配線、周辺回路等の構成を示す平面図であり、図２は、図１のより詳細な２次元的レイアウトを示す平面図であり、図３は、画像信号線及びクロック信号線等の配線を示す図２のＡ－Ａ’断面図であり、図４は、図１の画素部分の拡大平面図であり、図５は、ＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図であり、図６は、対向基板を含めて示す図５のＨ－Ｈ’断面図である。

【００３６】図１において、液晶装置２００は、例えば石英基板、ハードガラス等からなるＴＦＴアレイ基板１を備えている。ＴＦＴアレイ基板１上には、マトリクス状に設けられた複数の画素電極１１と、Ｘ方向に複数配列されており夫々がＹ方向に沿って伸びるデータ線３５と、Ｙ方向に複数配列されており夫々がＸ方向に沿って伸びる走査線３１と、各データ線３５と画素電極１１との間に夫々介在すると共に該間における導通状態及び非導通状態を、走査線３１を介して夫々供給される走査信号に応じて夫々制御するスイッチング素子の一例としての複数のＴＦＴ３０とが形成されている。またＴＦＴアレイ基板１上には、後述の蓄積容量（図６参照）のための配線である容量線３１’（蓄積容量電極）が、走査線３１と平行に形成されている。

【００３７】ＴＦＴアレイ基板１上には更に、データ信号供給手段の一例を構成するサンプリング回路３０１及びデータ線駆動回路１０１と、走査線駆動回路１０４とが形成されている。また、複数の画素電極１１により規定される画像表示領域（即ち、実際に液晶の配向状態変

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化により画像が表示される液晶装置の領域）の上辺には、画像表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられており、画像表示領域の四隅には、ＴＦＴアレイ基板１と対向基板との間で電気的導通をとるための上下導通端子１０６が設けられている。以下図１から図３の説明において、ＴＦＴアレイ基板１の下辺に沿って複数設けられた外部入力端子１０２を介して入力される信号名称と、その信号配線とは、説明の容易化のために同一のアルファベット記号を信号及び配線の後に夫々付加して参照する（例えば、信号名称である“クロック信号ＣＬＸ”に対し、その信号配線を“配線ＣＬＸ”と呼ぶ）ことにする。

【００３８】走査線駆動回路１０４は、外部制御回路から外部入力端子１０２並びに配線ＶＳＳＹ及びＶＤＤＹを介して供給される、走査線駆動回路用の負電源ＶＳＳＹ及び正電源ＶＤＤＹを電源として用いて、走査線駆動回路用のスタート信号ＤＹの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＹ及びＣＬＹ’を介して供給される、走査線駆動回路用の基準クロック信号ＣＬＹ及びその反転クロック信号ＣＬＹ’に基づく所定タイミングで、走査線３１に走査信号をパルス的に線順次で印加する。

【００３９】データ線駆動回路１０１は、外部制御回路から外部入力端子１０２並びに信号配線ＶＳＳＸ及びＶＤＤＸを介して供給される、データ線駆動回路用の負電源ＶＳＳＸ及び正電源ＶＤＤＸを電源として用いて、データ線駆動回路用のスタート信号ＤＸの入力により内蔵シフトレジスタ回路をスタートさせる。そして、外部入力端子１０２並びに配線ＣＬＸ及びＣＬＸ’を介して供給されるデータ線駆動回路用の基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＸ’に基づき、走査線駆動回路１０４が走査信号を印加するタイミングに合わせて、外部入力端子１０２及び配線ＶＩＤ１～ＶＩＤ６を介して供給される例えば６相にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ６夫々について、データ線３５毎にサンプリング回路駆動信号をサンプリング回路３０１にサンプリング回路駆動信号線３０６を介して所定タイミングで供給する。

【００４０】サンプリング回路３０１は、ＴＦＴ３０２を各データ線３５毎に備えており、配線ＶＩＤ１～ＶＩＤ６がＴＦＴ３０２のソース電極に接続されており、サンプリング回路駆動信号線３０６がＴＦＴ３０２のゲート電極に接続されている。そして、画像信号ＶＩＤ１～ＶＩＤ６が入力されると、これらの画像信号をサンプリングする。また、サンプリング回路駆動信号線３０６を介して、データ線駆動回路１０１からサンプリング回路駆動信号が入力されると、画像信号ＶＩＤ１～ＶＩＤ６夫々についてサンプリングされた画像信号を、６つの隣接するデータ線３５からなるグループ毎に順次印加する。以上のように、データ線駆動回路１０１とサンプリング回路３０１とは、６相にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ６をデータ線３５にデータ信号として供給するように構成されている。本実施の形態では隣接する６つのデータ線３５に接続されるサンプリング回路３０１を同時に選択し、６つのデータ線３５からなるグループ毎に順次転送していく方式を述べたが、データ線３５を１本毎に選択してもよいし、隣接する２、３、…、５本或いは７本以上を同時に選択してもよい。また、データ線３５に供給される画像信号のシリアルーパラレル変換数は６相のみならず、サンプリング回路３０１を構成するＴＦＴ３０２の書き込み特性が良ければ、５相以下でもよいし、画像信号の周波数が高ければ、７相以上に増やしてもよい。この際、少なくとも画像信号のシリアルーパラレル変換数だけ、画像信号用の外部入力端子１０２及び画像信号線が必要なことは言うまでもない。

【００４１】図２に示すように、データ線駆動回路１０１は、スタート信号ＤＸが入力されると、基準クロック信号ＣＬＸ及びその反転クロック信号ＣＬＫ’に基づく転送信号の順次生成を開始するシフトレジスタ回路１０１ａと、シフトレジスタ回路１０１ａからの転送信号を波形整形しバッファリングした後、サンプリング回路駆動信号線３０６を介してサンプリング回路３０１に供給する波形制御回路１０１ｂ及びバッファ回路１０１ｃとを備えている。また、サンプリング回路３０１は、６相にシリアルーパラレル変換された画像信号ＶＩＤ１～ＶＩＤ６に対応してＴＦＴ３０２が６個ずつパラレルに各サンプリング回路駆動信号線３０６に接続されている。即ち、ＴＦＴ３０２から構成されるスイッチＳ１～Ｓ６が左から１本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳ７～Ｓ１２が左から２本目のサンプリング回路駆動信号線３０６に接続されており、スイッチＳｎ－５～Ｓｎが右端のサンプリング回路駆動信号線３０６に接続されている。

【００４２】本実施の形態では特に、図１及び図２に示すように、ＴＦＴアレイ基板１には、負電源ＶＳＳＸ用の配線ＶＳＳＸを兼ねた定電位の導電線（以下、シールド線と称す）８０及び正電源ＶＤＤＸ用の配線ＶＤＤＸを兼ねた定電位のシールド線８２が配線されている。これらのシールド線８０及び８２により、配線ＶＩＤ１～ＶＩＤ６は、配線ＣＬＸ及びＣＬＸ’から電気的にシールドされている。従って、クロック信号ＣＬＸの周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを低減できる。

【００４３】尚、走査線駆動用のクロック信号ＣＬＹ（及びその反転クロック信号ＣＬＹ’）の周波数は、データ線駆動用の上述のクロック信号ＣＬＸ（及びその反転クロック信号ＣＬＸ’）の周波数に比べて遥かに低

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い。従って、クロック信号ＣＬＹ及びＣＬＹ’については、高周波のクロックノイズが問題となることは少ない。しかしながら、本実施の形態においては、図１及び図２に示したように、シールド線８０及び８２により、配線ＣＬＹ及びＣＬＹ’からも、配線ＶＩＤ１～ＶＩＤ６は、シールドされるように配線されている。すなわち、外部入力端子１０２から延設され、データ線駆動回路１０１の負電源ＶＳＳＸを兼ねたシールド線８０は、対向基板２に設けられた遮光性の額縁５３下に沿って、画像表示領域を囲むように配線される。従って、画像信号用の配線ＶＩＤ１～ＶＩＤ６ばかりではなく、サンプリング回路３０１のＴＦＴ３０２を介してデータ信号が書き込まれるデータ線３５への周辺回路からのノイズの飛び込みをも低減できる。

【００４４】特に本実施の形態では、配線ＶＳＳＸ及びＶＤＤＸを夫々延設してシールド線８０及び８２とすることにより、外部入力端子や配線を共用することが可能となり、装置構成の簡略化と省スペース化を図ることが出来る。また、シールド線８０及び８２の電位は、このように定電位線との共用化により、容易に定電位とされる。但し、電源用の配線とシールド線を別個に配線してもよい。

【００４５】また、データ線駆動回路１０１及び走査線駆動回路１０４を駆動するための電源電圧が互いに同じであれば、正電源の電位（正電位）であるＶＤＤＸ及びＶＤＤＹ、負電源の電位（負電位）であるＶＳＳＸ及びＶＳＳＹはそれぞれ共用させてもよい。このような構成を採れば、外部入力端子及びそれから延設される配線が削減できるので有利である。

【００４６】本実施の形態では、図２に示すように、負電源ＶＳＳＸが入力される外部入力端子１０２が２つ設けられており、配線ＶＳＳＸもこれに対応して２本設けられている。そして、配線ＶＩＤ１～ＶＩＤ６は、負電源ＶＳＳＸの電位（負電位）とされたシールド線８０により、ＴＦＴアレイ基板１上で囲まれている。特に、シフトレジスタ回路１０１ａと波形制御回路１０１ｂとの間にも、データ線３５と同じＡｌ等の金属層から形成されたシールド線８０は延設されている。そして、延設されたシールド線８０の先端部は、後述のように第１層間絶縁層を介してＡｌ等の金属層の下方において、例えば走査線３１と同じポリシリコン等の導電層から形成されたシールド線接続部８１を介して、波形制御回路１０１ｂ及びバッファ回路１０１ｃを囲むようにしてシールド線８０に接続されている。

【００４７】他方、図２に示すように、配線ＣＬＸ及びＣＬＸ’は、データ線駆動回路１０１に隣接する部分においては、正電源ＶＤＤＸの電位（正電位）とされたシールド線8-2により、ＴＦＴアレイ基板1上で囲まれている。特に、波形制御回路１０１ｂとバッファ回路１０１ｃとの間にも、データ線３５と同じＡｌ等の金属層から形成されたシールド線８２は延設されており、その先端部は、例えば走査線３１と同じポリシリコン等の導電層から形成されたシールド線接続部８３を介して波形制御回路１０１ｂ及びシフトレジスタ回路１０１ａを囲むようにしてシールド線８２に接続されている。

【００４８】従って、配線ＶＩＤ１～ＶＩＤ６は、ＴＦＴアレイ基板１上で配線ＣＬＸ及びＣＬＸ’から２重にシールドされた構成が採られており、シフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃに対するシールドも信頼性が高いものとされている。但し、このように囲む構成を採らなくても、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６との間にシールド線８０又は８２が少なくとも一本介在するように構成すれば、シールドの効果は多少なりとも得られる。

【００４９】本実施の形態では、図１及び図２に示したように、配線ＶＩＤ１～ＶＩＤ６と配線ＣＬＸ及びＣＬＸ’とは、ＴＦＴアレイ基板１上でＸ方向に沿って反対向きに（即ち、前者は時計回りに、後者は反時計回りに）引き回されている。従って、これらの配線間の距離が全体として大きくなるため、且つこれらの配線間にあるデータ線駆動回路１０１の介在に応じてこれらの配線間を伝達する電磁波は減少するので、クロック信号ＣＬＸ及びＣＬＸ’の周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から、配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを更に低減できる。また、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６の引き回しは、その方向が入れ替わっても何ら問題はない。すなわち、配線ＣＬＸ及びＣＬＸ’を負電源ＶＳＳＸでシールドし、配線ＶＩＤ１～ＶＩＤ６を正電源ＶＤＤＸでシールドしてもよい。但し、このように反対方向に引き回す構成を採らなくても、配線ＣＬＸ及びＣＬＸ’と配線ＶＩＤ１～ＶＩＤ６との間にシールド線８０又は８２が少なくとも一本介在するように構成すれば、シールドの効果は多少なりとも得られる。

【００５０】本実施の形態では、クロック信号ＣＬＸ及びＣＬＸ’用の外部入力端子１０２と、画像信号ＶＩＤ１～ＶＩＤ６用の外部入力端子１０２とは、負電源ＶＳＳＸ用、正電源ＶＤＤＸ用及びスタート信号ＤＸ用の３つの外部入力端子１０２を間に介して、相互に所定間隔を隔てて配置されている。そして好ましくは、ＴＦＴアレイ基板１の周辺部において外部入力端子１０２を形成可能な領域において、可能な限りクロック信号ＣＬＸ及びＣＬＸ’用の外部入力端子１０２と、画像信号ＶＩＤ１～ＶＩＤ６用の外部入力端子１０２とは、相互に離して配置され、少なくとも一個以上の外部入力端子１０２が両者間に配置される。このように構成すれば、例えば画像信号線とクロック信号線とを隣接配置した場合と比較して、クロック用の配線から画像信号用の配線への高周波のクロックノイズの飛び込みを低減できる。

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【００５１】本実施の形態では図１及び図２に示したように、シールド線８０により、画像表示領域及び複数のデータ線３５は、ＴＦＴアレイ基板１上で囲まれている。このため、当該画像表示領域及び複数のデータ線３５も、配線ＣＬＸ及びＣＬＸ’からシールドされている。従って、データ線駆動回路１０１から出力されたサンプリング回路駆動信号、ＴＦＴ３０や画素電極１１に到達したデータ信号等における、高周波のクロックノイズの発生を低減できる。但し、このように画像表示領域までも囲む構成を採らなくても、サンプリング回路３０１に至るまでの配線ＶＩＤ１～ＶＩＤ６をシールド線８０又は８２によりシールドするように構成すれば、シールドの効果は多少なりとも得られる。

【００５２】図３に断面図で示すように、シールド線８０及び８２を含む外部入力端子１０２に接続された各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、例えば、Ａｌ（アルミニウム）等の、データ線３５と同一の低抵抗金属材料から形成されている。従って、シールド線８０及び８２の引き回し領域が、たとえ長くても、シールド線８０及び８２の抵抗は実用上十分に低く抑えられる。即ち、図２に示したように、他の各種配線やシフトレジスタ回路１０１ａ並びに波形制御回路１０１ｂ及びバッファ回路１０１ｃの隙間を縫ってジグザグにシールド線８２を長く配線でき、更に画像表示領域までも含めた広い領域にシールド線８０を長く配線できる。このように比較的簡単な構成により、当該シールドの効果を全体として高めることが出来る。また図３に示すように、シールド線８０及び８２を含む外部入力端子１０２に接続された各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸは、ＴＦＴアレイ基板１に形成された第１層間絶縁層４２上に、即ち同一層上に形成されている。従って、シールドの効果がより効率良く発揮される。更に、このように構成すると、液晶装置２００の製造プロセスにおいて、各種配線ＤＹ、ＶＳＳＹ、…、ＶＤＤＸを、例えば、Ａｌ層等の同一の低抵抗金属層から同一工程により一括して形成できるので、製造上有利である。

【００５３】尚、図１から図３に示した外部入力端子１０２から入力される信号ＬＣＣＯＭは、共通電極の電源信号であり、配線ＬＣＣＯＭ及び前述の上下導通端子１０６上の導通材を介して、後述の対向基板に設けられた共通電極（図７参照）に供給される。

【００５４】ここで図４の平面図に示すように、容量線３１’は、ＴＦＴアレイ基板１上において走査線３１と平行に、例えば走査線３１と同じく導電性のポリシリコン層等から形成されており、シールド線８０にコンタクトホール８０ａを介して接続されている。このように構成すれば、容量線３１’を定電位とするための配線をシールド線８０で兼用でき、容量線３１’を定電位にするために必要な外部入力端子も、シールド線８０用の外部入力端子１０２で兼用できる。

【００５５】本実施の形態では特に、サンプリング回路３０１は、図１中斜線領域で示すように且つ図５及び図６に示すように、対向基板２に形成された遮光性の額縁５３に対向する位置においてＴＦＴアレイ基板１上に設けられており、データ線駆動回路１０１及び走査線駆動回路１０４は、液晶層５０に面しないＴＦＴアレイ基板１の狭く細長い周辺部分上に設けられている。ＴＦＴアレイ基板１の上には、画像表示領域の周囲において両基板を貼り合わせて液晶層５０を包囲するシール部材の一例としての光硬化性樹脂からなるシール材５２が、画像表示領域に沿って設けられている。そして、対向基板２上における画像表示領域とシール材５２との間には、遮光性の額縁５３が設けられている。

【００５６】額縁５３は、後に画像表示領域に対応して開口が開けられた遮光性のケースにＴＦＴアレイ基板１が入れられた場合に、当該画像表示領域が製造誤差等により当該ケースの開口の縁に隠れてしまわないように、即ち、例えばＴＦＴアレイ基板１のケースに対する数百μｍ程度のずれを許容するように、画像表示領域の周囲に例えば５００μｍ以上の幅を持つ帯状の遮光性材料から形成されたものである。このような遮光性の額縁５３は、例えば、Ｃｒ（クロム）、Ｎｉ（ニッケル）、Ａｌ（アルミニウム）等の金属材料を用いたスパッタリング、フォトリソグラフィ及びエッチングにより対向基板２に形成される。或いは、カーボンやＴｉ（チタン）をフォトレジストに分散した樹脂ブラックなどの材料から形成される。

【００５７】シール材５２の外側の領域には、画像表示領域の下辺に沿ってデータ線駆動回路１０１及び外部入力端子１０２が設けられており、画像表示領域の左右の２辺に沿って走査線駆動回路１０４が画像表示領域の両側に設けられている。そして、シール材５２とほぼ同じ輪郭を持つ対向基板２が当該シール材５２によりＴＦＴアレイ基板１に固着されている。

【００５８】以上のようにシールド線８０及びサンプリング回路３０１は、ＴＦＴアレイ基板１上の額縁５３に対向配置、即ち本実施形態の場合は額縁５３の下に設けるようにすれば、ＴＦＴアレイ基板１上の省スペース化が図られ、例えば、走査線駆動回路１０４やデータ線駆動回路１０１をＴＦＴアレイ基板１の周辺部分に余裕を持って形成することができ、シールド線８０の形成により液晶装置２００における有効表示面積が減少することも殆ど又は全くない。またシールド線８０は額縁５３に対向する位置に延設されるとともに、対向する位置においてシールド線８０と容量線３１’とを接続するようにすれば、ＴＦＴ基板上の有効表示面積を減少させることなく、スペースを有効利用することができる。

【００５９】（液晶装置全体の構成）次に、液晶装置２００の具体的構成について図７及び図８を参照して説明する。ここに、図７は液晶装置のＴＦＴ３０部分を示し

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ており、図４におけるＢ－Ｂ’に沿った断面図であり、図８は額縁の下における液晶装置のシールド線８０に沿った断面図である。尚、図７及び図８においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００６０】図７の断面図において、液晶装置２００は、各画素に設けられるＴＦＴ３０部分において、ＴＦＴアレイ基板１並びにその上に積層された半導体層３２、ゲート絶縁層３３、走査線３１（ゲート電極）、第１層間絶縁層４２、データ線３５、第２層間絶縁層４３、画素電極１１及び配向膜１２を備えている。液晶装置２００はまた、例えばガラス基板から成る対向基板２並びにその上に積層された共通電極２１、配向膜２２及び遮光膜２３を備えている。液晶装置２００は更に、これらの両基板間に挟持された電気光学物質として液晶層５０を備えている。

【００６１】ここでは先ず、これらの層のうち、ＴＦＴ３０を除く各層の構成について順に説明する。

【００６２】第１及び第２層間絶縁層４２及び４３は夫々、５０００～１５０００オングストローム程度の層みを持つＮＳＧ（ノンシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）などのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる。尚、ＴＦＴアレイ基板１上に、ＴＦＴ３０の下地となる層間絶縁層をシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等から形成してもよい。

【００６３】画素電極１１は例えば、ＩＴＯ（インジウム・ティン・オキサイド）膜などの透明導電性薄膜からなる。このような画素電極１１は、スパッタリング処理等によりＩＴＯ膜等を約５００～２０００オングストロームの厚さに堆積した後、フォトリソグラフィ工程、エッチング工程を施すこと等により形成される。尚、当該液晶装置２００を反射型の液晶装置に用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極１１を形成してもよい。

【００６４】配向膜１２は例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜１２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００６５】共通電極２１は、対向基板２の全面に渡って形成されている。このような共通電極２１は、例えばスパッタリング処理等によりＩＴＯ膜等を約５００～２０００オングストロームの厚さに堆積した後、フォトリソグラフィ工程、エッチング工程を施すこと等により形成される。

【００６６】配向膜２２は、例えば、ポリイミド薄膜などの有機薄膜からなる。このような配向膜２２は、例えばポリイミド系の塗布液を塗布した後、所定のプレティルト角を持つように且つ所定方向でラビング処理を施すこと等により形成される。

【００６７】遮光膜２３は、ＴＦＴ３０に対向する所定領域に設けられている。このような遮光膜２３は、前述の額縁５３同様に、ＣｒやＮｉなどの金属材料を用いたスパッタリング、フォトリソグラフィ及びエッチングにより形成されたり、カーボンやＴｉをフォトレジストに分散した樹脂ブラックなどの材料から形成される。遮光膜２３は、ＴＦＴ３０の半導体層３２に対する遮光の他に、コントラストの向上、色材の混色防止などの機能を有する。

【００６８】液晶層５０は、画素電極１１と共通電極２１とが対面するように配置されたＴＦＴアレイ基板１と対向基板２との間において、シール材５２（図５及び図６参照）により囲まれた空間に液晶が真空吸引等により封入されることにより形成される。液晶層５０は、画素電極１１からの電界が印加されていない状態で配向膜１２及び２２により所定の配向状態を採る。液晶層５０は、例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材５２は、二つの基板１及び２をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのスペーサが混入されている。

【００６９】次に、ＴＦＴ３０に係る各層の構成について順に説明する。

【００７０】ＴＦＴ３０は、走査線３１、走査線３１からの電界によりチャネルが形成される半導体層３２、走査線３１と半導体層３２とを絶縁するゲート絶縁層３３、半導体層３２に形成されたソース領域３４、データ線３５、及び半導体層３２に形成されたドレイン領域３６を備えている。ドレイン領域３６には、複数の画素電極１１のうちの対応する一つが接続されている。ソース領域３４及びドレイン領域３６は後述のように、半導体層３２に対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のｎ型用又はｐ型用のドーパントをドープすることにより形成されている。ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子であるＴＦＴ３０として用いられることが多い。

【００７１】ＴＦＴ３０を構成する半導体層３２は、例えば、ＴＦＴアレイ基板１上にａ－Ｓｉ（アモルファスシリコン）膜を形成後、アニール処理を施して約５００～２０００オングストロームの厚さに固相成長させることにより形成する。この際、ｎチャネル型のＴＦＴ３０の場合には、Ｓｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素のドーパントを用いたイオン注入等によりドープしてもよい。また、ｐチャネル型のＴＦＴ３０の場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素のドーパントを用いたイオン注入等によりドープする。特にＴＦＴ

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３０をＬＤＤ（Ｌｉｇｈｔｌｙ　ＤｏｐｅｄＤｒａｉｎ）構造を持つｎチャネル型のＴＦＴとする場合、ｐ型の半導体層３２に、ソース領域３４及びドレイン領域３６のうちチャネル側に夫々隣接する一部にＰなどのＶ族元素のドーパントにより低濃度ドープ領域を形成し、同じくＰなどのＶ族元素のドーパントにより高濃度ドープ領域を形成する。また、ｐチャネル型のＴＦＴ３０とする場合、ｎ型の半導体層３２に、 Ｂなどの III族元素のドーパントを用いてソース領域３４及びドレイン領域３６を形成する。このようにＬＤＤ構造とした場合、ショートチャネル効果を低減できる利点が得られる。尚、ＴＦＴ３０は、ＬＤＤ構造における低濃度ドープ領域にイオン注入したオフセット構造のＴＦＴとしてもよいし、ゲート電極をマスクとして高濃度の不純物イオンをドープすることにより自己整合的に高濃度なソース及びドレイン領域を形成するセルフアライン型のＴＦＴとしてもよい。また、ゲート電極を２個直列に設けデュアルゲート構造としてもよいし、ゲート電極を３個以上直列に設けてもよいことは言うまでもない。このような構成を採れば、ＴＦＴ３０のオフ時におけるリーク電流が低減され、クロストーク等の発生を抑制できるため、高品位な液晶装置を提供することができる。

【００７２】ゲート絶縁層３３は、半導体層３２を約９００～１３００℃の温度により熱酸化することにより、３００～１５００オングストローム程度の比較的薄い厚さの熱酸化膜を形成して得ることができる。これにより半導体層３２とゲート絶縁層３３の界面状態の優れた良質の絶縁膜を形成することができる。

【００７３】走査線３１は、減圧ＣＶＤ法等によりポリシリコン膜を堆積した後、フォトリソグラフィ工程、エッチング工程等により形成される。或いは、Ａｌ等の金属膜又は金属シリサイド膜から形成されてもよい。この場合、走査線３１を、遮光膜２３が覆う領域の一部又は全部に対応する遮光膜として配置すれば、金属膜や金属シリサイド膜の持つ遮光性により、遮光膜２３の一部又は全部を省略することも可能となる。この場合特に、対向基板２とＴＦＴアレイ基板１との貼り合わせずれによる画素開口率の低下を防ぐことが出来る利点がある。

【００７４】データ線３５は、画素電極１１と同様にＩＴＯ膜等の透明導電性薄膜から形成してもよい。或いは、スパッタリング処理等により、約１０００～５０００オングストロームの厚さに堆積されたＡｌ等の低抵抗金属や金属シリサイド等から形成してもよい。

【００７５】また、第１層間絶縁層４２には、ソース領域３４へ通じるコンタクトホール３７及びドレイン領域３６へ通じるコンタクトホール３８が夫々形成されている。このソース領域３４へのコンタクトホール３７を介して、データ線３５はソース領域３４に電気的接続される。更に、第２層間絶縁層４３には、ドレイン領域３６へのコンタクトホール３８が形成されている。このドレイン領域３６へのコンタクトホール３８を介して、画素電極１１はドレイン領域３６に電気的接続される。前述の画素電極１１は、このように構成された第２層間絶縁層４３の上面に設けられている。各コンタクトホールは、例えば、反応性エッチング、反応性イオンビームエッチング等のドライエッチングにより形成すれば、開口サイズの微細化が可能となり、画素の高開口率化が実現できる。

【００７６】尚、一般にはチャネルが形成される半導体層３２は、光が入射するとｐ－Ｓｉが有する光電変換効果により光電流が発生してしまいＴＦＴ３０のトランジスタ特性が劣化するが、本実施の形態では、対向基板２には各ＴＦＴ３０に夫々対向する位置に遮光膜２３が形成されているので、入射光が半導体層３２に入射することが防止される。更にこれに加えて又は代えて、ゲート電極を上側から覆うようにデータ線３５をＡｌ等の不透明な金属薄膜から形成すれば、遮光膜２３と共に又は単独で、半導体層３２への入射光（即ち、図７で上側からの光）の入射を効果的に防ぐことが出来る。

【００７７】図７において、画素電極１１には蓄積容量７０が夫々設けられている。この蓄積容量７０は、より具体的には、半導体層３２と同一工程により形成される第１蓄積容量電極３２’、ゲート絶縁層３３と同一工程により形成される誘電体層３３’、走査線３１と同一工程により形成される容量線３１’（第２蓄積容量電極）、第１及び第２層間絶縁層４２及び４３、並びに第１及び第２層間絶縁層４２及び４３を介して容量線３１’に対向する画素電極１１の一部から構成されている。このように蓄積容量７０が設けられているため、デューティー比が小さくても高精細な表示が可能とされる。

【００７８】図８の断面図に示すように、額縁５３に対向し且つ複数の走査線３１の上方の位置において第１層間絶縁層４２上をシールド線８０は通過する。そして、このシールド線８０は、その殆どの部分が、前述したデータ線３５と同一工程で形成されたＡｌ等の金属薄膜からなる低抵抗な配線である。このように液晶装置２００の製造プロセスにおいて、シールド線８０とデータ線３５とを一括して形成できるので、製造上有利である。

【００７９】本実施の形態では特に、ＴＦＴ３０の形成時に同一薄膜形成工程で、サンプリング回路３０１、データ線駆動回路１０１、走査線駆動回路１０４等の周辺回路を形成できるので製造上有利である。例えば、これらの周辺回路は、ｎチャネル型ポリシリコンＴＦＴ及びｐチャネル型ポリシリコンＴＦＴから構成される相補型構造の複数のＴＦＴからＴＦＴアレイ基板１上の周辺部分に形成される。

【００８０】尚、図７及び図８には示されていないが、液晶装置２００においては、対向基板２の投射光が入射する側及びＴＦＴアレイ基板１の投射光が出射する側に

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は夫々、例えば、ＴＮ（ツイステッドネマティック）モード、ＳＴＮ（スーパーＴＮ）モード、Ｄ－ＳＴＮ（ダブルーＳＴＮ）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光板などが所定の方向で配置される。

【００８１】また、以上説明した液晶装置２００は、カラー液晶プロジェクタに適用されるため、３つの液晶装置２００がＲＧＢ用のライトバルブとして夫々用いられ、各装置には夫々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が入射光として夫々入射されることになる。従って、各実施の形態では、対向基板２に、カラーフィルタは設けられていない。しかしながら、液晶装置２００においても遮光膜２３の形成されていない画素電極１１に対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２上に形成してもよい。あるいは、ＴＦＴアレイ基板１上の各画素に対応するように、ＲＧＢのカラーレジストによりカラーフィルター層を内蔵しても良い。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー液晶テレビなどのカラー液晶装置に本実施の形態の液晶装置を適用できる。更に、対向基板２上に１画素1個対応するようにマイクロレンズを形成してもよい。このようにすれば、入射光の集光効率を向上することで、明るい液晶装置が実現できる。更にまた、対向基板２上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイックフィルタ付き対向基板によれば、より明るいカラー液晶装置が実現できる。

【００８２】液晶装置２００において、ＴＦＴアレイ基板１側における液晶分子の配向不良を抑制するために、第２層間絶縁層４３の上に更に平坦化膜をスピンコート等で塗布してもよく、又はＣＭＰ（Chemical Mechanical Polishing）処理を施してもよい。或いは、第２層間絶縁層４３を平坦化膜で形成してもよい。

【００８３】液晶装置２００のスイッチング素子は、正スタガ型又はコプラナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、本実施の形態は有効である。

【００８４】液晶装置２００においては、一例として液晶層５０をネマティック液晶から構成したが、液晶を高分子中に微小粒として分散させた高分子分散型液晶を用いれば、配向膜１２及び２２、並びに前述の偏光フィルム、偏光板等が不要となり、光利用効率が高まることによる液晶装置の高輝度化や低消費電力化の利点が得られる。更に、画素電極１１をＡｌ等の反射率の高い金属膜から構成することにより、液晶装置２００を反射型液晶装置に適用する場合には、電圧無印加状態で液晶分子がほぼ垂直配向されたＳＨ（スーパーホメオトロピック）型液晶などを用いても良い。更にまた、液晶装置２００においては、液晶層５０に対し垂直な電界（縦電界）を印加するように対向基板２の側に共通電極２１を設けているが、液晶層５０に平行な電界（横電界）を印加するように一対の横電界発生用の電極から画素電極１１を夫々構成する（即ち、対向基板２の側には縦電界発生用の電極を設けることなく、ＴＦＴアレイ基板１の側に横電界発生用の電極を設ける）ことも可能である。このように横電界を用いると、縦電界を用いた場合よりも視野角を広げる上で有利である。その他、各種の液晶材料（液晶相）、動作モード、液晶配列、駆動方法等に本実施の形態を適用することが可能である。また、上述の実施形態では基板上にＴＦＴを形成する構成を用いて説明したがこのような構成に限らず、シリコン基板にスイッチング素子を形成する構成でも適用可能である。また、電気光学物質として液晶を用いて説明したが液晶に限らず、エレクトロルミネッセンス、あるいはプラズマディスプレイ等にも適用可能である。

【００８５】以上説明した実施の形態において更に、額縁５３下やＴＦＴアレイ基板１の周辺部に、プリチャージ回路、検査回路等の周知の周辺回路を設けてもよい。プリチャージ回路は、コントラスト比の向上、データ線３５の電位レベルの安定、表示画面上のラインむらの低減等を目的として、データ線３５に対し、データ線駆動回路１０１から供給されるデータ信号に先行するタイミングで、プリチャージ信号を供給することにより、データ信号をデータ線３５に書き込む際の負荷を軽減する回路である。例えば、特開平７－２９５２０号公報に、このようなプリチャージ回路の一例が開示されている。他方、検査回路は、額縁５３下やＴＦＴアレイ基板の周辺部に、製造途中や出荷時の当該液晶装置の品質、欠陥等を検査するための回路である。

【００８６】また、以上の実施の形態において、特開平９－１２７４９７号公報、特公平３－５２６１１号公報、特開平３－１２５１２３号公報、特開平８－１７１１０１号公報等に開示されているように、ＴＦＴアレイ基板１上においてＴＦＴ３０に対向する位置（即ち、ＴＦＴ３０の下側）にも、例えば高融点金属からなる遮光層を設けてもよい。このようにＴＦＴ３０の下側にも遮光層を設ければ、ＴＦＴアレイ基板１の側からの戻り光等がＴＦＴ３０に入射するのを未然に防ぐことができる。従って、当該液晶装置２００をプロジェクタ用のライトバルブとして好適に用いることが出来る。

【００８７】更にまた、以上の実施の形態において、ＴＦＴ３０に代えてＴＦＤ（Thin Film Diode）等の２端子型非線形素子等からスイッチング素子を構成してもよい。この場合、データ線及び走査線のうち一方の線を対向基板に配置して共通電極として機能させ、ＴＦＴアレイ基板に設けられた他方の線と画素電極との間にスイッ

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チング素子を夫々配置して液晶駆動する。このように構成しても、画素信号線やデータ線をクロック信号線からシールドすることにより、高周波のクロックノイズの画像信号やデータ信号への飛び込みを防止する効果は発揮される。

【００８８】（液晶装置の動作）次に、以上のように構成された液晶装置２００の動作について図１を参照して説明する。

【００８９】先ず、走査線駆動回路１０４は、所定タイミングで走査線３１に走査信号をパルス的に線順次で印加する。

【００９０】これと並行して、６つの配線ＶＩＤ１～ＶＩＤ６からパラレルな画像信号を受けると、サンプリング回路３０１は、これらの画像信号をサンプリングする。データ線駆動回路１０１は、走査線駆動回路１０４がゲート電圧を印加するタイミングに合わせて、６つの配線ＶＩＤ１～ＶＩＤ６夫々について一つのデータ線毎にサンプリング回路駆動信号を供給して、サンプリング回路３０１のＴＦＴ３０２をオン状態とする。これにより、隣接する６つのデータ線３５に対して、サンプリング回路３０１にサンプリングされたデータ信号を順次印加する。即ち、データ線駆動回路１０１とサンプリング回路３０１により、配線ＶＩＤ１～ＶＩＤ６から入力された６相にシリアルーパラレル変換されたパラレルな画像信号ＶＩＤ１～ＶＩＤ６は、データ線３５に供給される。

【００９１】このように、走査信号（ゲート電圧）及びデータ信号（ソース電圧）の両方が印加されたＴＦＴ３０においては、ソース領域３４、半導体層３２に形成されたチャネル及びドレイン領域３６を介して画素電極１１に電圧が印加される。そして、この画素電極１１の電圧は、ソース電圧が印加された時間よりも例えば３桁も長い時間だけ蓄積容量（図７参照）により保持される。ここで特に、シールド線８０及び８２により、配線ＶＩＤ１～ＶＩＤ６は、配線ＣＬＸ及びＣＬＸ’からシールドされているので、クロック信号ＣＬＸの周波数が高い場合でも、配線ＣＬＸ及びＣＬＸ’から配線ＶＩＤ１～ＶＩＤ６への高周波のクロックノイズの飛び込みを低減できる。

【００９２】以上のように、画素電極１１に電圧が印加されると、液晶層５０におけるこの画素電極１１と共通電極２１とに挟まれた部分における液晶の配向状態が変化し、ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として液晶装置２００からは画像信号に応じたコントラストを持つ光が出射する。

【００９３】以上の結果、表示すべき画像の解像度が高く、高周波のシリアルな画像信号ＶＩＤ１～ＶＩＤ６が

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入力される場合にも、これに対応して周波数が高いクロック信号ＣＬＸ及びＣＬＸ’を用いつつ、高周波のクロックノイズの発生により画質が劣化することは殆ど又は全く無くなり、高品位の画像表示が可能とされる。

【００９４】（電子機器）次に、以上詳細に説明した液晶装置２００を備えた電子機器の実施の形態について図９から図１３を参照して説明する。

【００９５】先ず図９に、このように液晶装置２００を備えた電子機器の概略構成を示す。

【００９６】図９において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、液晶装置２００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、テレビ信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、シリアルーパラレル変換回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号ＣＬＫと共に駆動回路１００４に出力する。駆動回路１００４は、液晶装置２００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、液晶装置２００を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【００９７】次に図１０から図１３に、このように構成された電子機器の具体例を夫々示す。

【００９８】図１０において、電子機器の一例たる液晶プロジェクタ１１００は、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された液晶装置２００を含む液晶モジュールを３個用意し、夫々ＲＧＢ用のライトバルブ２００Ｒ、２００Ｇ及び２００Ｂとして用いたプロジェクタとして構成されている。液晶プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイックミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ２００Ｒ、２００Ｇ及び２００Ｂに夫々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ２００Ｒ、２００Ｇ及び２００Ｂにより夫々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投

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射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【００９９】本実施の形態においては特に、前述のように遮光層をＴＦＴの下側にも設けておけば、当該液晶装置２００からの入射光に基づく液晶プロジェクタ内の投射光学系による反射光、入射光が通過する際のＴＦＴアレイ基板の表面からの反射光、他の液晶装置から出射した後にダイクロイックプリズム１１１２を突き抜けてくる入射光の一部（Ｒ光及びＧ光の一部）等が、戻り光としてＴＦＴアレイ基板の側から入射しても、画素スイッチング用のＴＦＴ３０等のチャネルに対する遮光を十分に行うことができる。この場合、小型化に適したプリズムを投射光学系に用いても、各液晶装置のＴＦＴアレイ基板とプリズムとの間において、戻り光防止用のＡＲ(Anti Reflection)フィルムを貼り付けたり、偏光板にＡＲ被膜処理を施したりすることが不要となるので、構成を小型且つ簡易化する上で大変有利である。

【０１００】図１１において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した液晶装置２００がトップカバーケース内に備えられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１０１】図１２において、電子機器の他の例たるページャ１３００は、金属フレーム１３０２内に前述の駆動回路１００４がＴＦＴアレイ基板上に搭載されて液晶モジュールをなす液晶装置２００が、バックライト１３０６ａを含むライトガイド１３０６、回路基板１３０８、第１及び第２のシールド板１３１０及び１３１２、二つの弾性導電体１３１４及び１３１６、並びにフィルムキャリアテープ１３１８と共に収容されている。この例の場合、前述の表示情報処理回路１００２（図９参照）は、回路基板１３０８に搭載してもよく、液晶装置２００のＴＦＴアレイ基板上に搭載してもよい。更に、前述の駆動回路１００４を回路基板１３０８上に搭載することも可能である。

【０１０２】尚、図１２に示す例はページャであるので、回路基板１３０８等が設けられている。しかしながら、駆動回路１００４や更に表示情報処理回路１００２を搭載して液晶モジュールをなす液晶装置２００の場合には、金属フレーム１３０２内に液晶装置２００を固定したものを液晶装置として、或いはこれに加えてライトガイド１３０６を組み込んだバックライト式の液晶装置として、生産、販売、使用等することも可能である。

【０１０３】また図１３に示すように、駆動回路１００４や表示情報処理回路１００２を搭載しない液晶装置２００の場合には、駆動回路１００４や表示情報処理回路１００２を含むＩＣ１３２４がポリイミドテープ１３２２上に実装されたＴＣＰ（Tape Carrier Package）１３２０に、ＴＦＴアレイ基板１の周辺部に設けられた異方性導電フィルムを介して物理的且つ電気的に接続して、液晶装置として、生産、販売、使用等することも可能である。

【０１０４】以上図１０から図１３を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図９に示した電子機器の例として挙げられる。

【０１０５】以上説明したように、本実施の形態によれば、高周波のクロックノイズの発生が低減されており、高品位の画像表示が可能な液晶装置２００を備えた各種の電子機器を実現できる。

【０１０６】

【発明の効果】請求項１に記載の電気光学装置によれば、第１基板に配線された定電位の導電線により、画像信号線は、クロック信号線からシールドされているので、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減でき、従って、高解像度の画像を表示するための高周波数の画像信号に応じて高品位の画像表示を行える。

【０１０７】請求項２に記載の電気光学装置によれば、導電線及び定電位線の配線自体や外部入力端子を共用することにより、構成の簡略化と省スペース化を図ることが出来るので、比較的簡易な構成により高品位の画像表示を行える電気光学装置を実現できる。

【０１０８】請求項３に記載の電気光学装置によれば、画像信号線を、クロック信号線から２重にシールドする構成により、画像信号やデータ信号中の高周波のクロックノイズの発生をより強力に且つ信頼性高く低減し得る。

【０１０９】請求項４に記載の電気光学装置によれば、画像信号線とクロック信号線とをデータ線駆動回路に対して反対向きに引き回すことにより、画像信号線への高周波のクロックノイズの飛び込みを更に低減できるので、簡単な構成上の工夫により効率良くシールドの効果を高めることが出来る。

【０１１０】請求項５に記載の電気光学装置によれば、第１及び第２外部入力端子を、第３外部入力端子を間に介して相互に所定間隔を隔てて配置することにより、画像信号線への高周波のクロックノイズの飛び込みを低減できるので、簡単な構成上の工夫により効率良くシールドの効果を高めることが出来る。

【０１１１】請求項６に記載の電気光学装置によれば、画像表示領域及び複数のデータ線をクロック信号線からシールドできるので、データ線上のデータ信号等における、高周波のクロックノイズの発生を低減でき、より高品位の画像表示が可能となる。

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【０１１２】請求項７に記載の電気光学装置によれば、導電線は基板の額縁下に設けられているので、基板上のスペースの有効利用を図ることができる。

【０１１３】請求項８及び９に記載の電気光学装置によれば、比較的簡易な製造工程により、シールド効果の高い導電線を形成することができ、低コストで高品位の画像表示が可能な電気光学装置を実現できる。

【０１１４】請求項１０に記載の電気光学装置によれば、容量線の電位変動によるスイッチング素子や画素電極への悪影響を防止しつつ、容量線を定電位とするための定電位線や外部入力端子を他の配線や端子で兼用できるので、比較的簡易な構成により高品位の画像表示が可能となる。

【０１１５】請求項１１に記載の電子機器によれば、高周波のクロックノイズが低減されており、高品位の画像表示が可能な、液晶プロジェクタ、パーソナルコンピュータ、ページャ等の様々な電子機器を実現可能となる。

【図面の簡単な説明】

【図１】　液晶装置の実施の形態においてＴＦＴアレイ基板上に形成された各種配線、周辺回路等の概略平面図である。

【図２】　図１の２次元的レイアウトをより詳細に示す概略平面図である。

【図３】　図１のＴＦＴアレイ基板上のＡ－Ａ’線に沿った断面図である。

【図４】　図１のＴＦＴアレイ基板上に形成された画素電極、走査線、データ等の画像表示領域端部における拡大平面図である。

【図５】　図１の液晶装置の全体構成を示す平面図である。

【図６】　図１の液晶装置の全体構成を示す断面図である。

【図７】　図１の液晶装置の画像表示領域に設けられた画素スイッチング用ＴＦＴの断面図である。

【図８】　図１の液晶装置の額縁領域に設けられたシールド線部分における断面図である。

【図９】　本発明による電子機器の実施の形態の概略構成を示すブロック図である。

【図１０】　電子機器の一例としての液晶プロジェクタを示す断面図である。

【図１１】　電子機器の他の例としてのパーソナルコンピュータを示す正面図である。

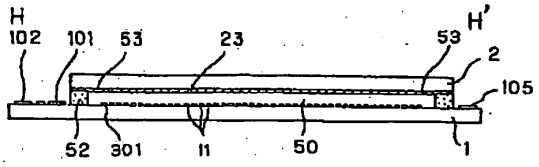
【図１２】　電子機器の一例としてのページャを示す分解斜視図である。

【図１３】　電子機器の一例としてのＴＣＰを用いた液晶装置を示す斜視図である。

【符号の説明】

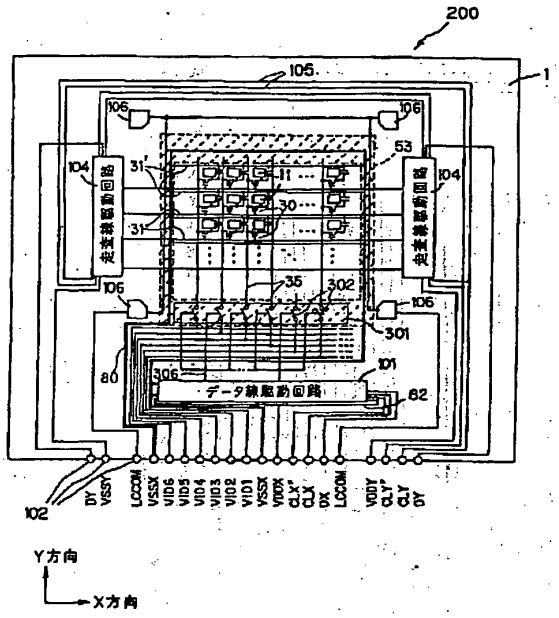
１…ＴＦＴアレイ基板
２…対向基板
１１…画素電極
１２…配向膜
２１…共通電極
２２…配向膜
２３…遮光膜
３０…ＴＦＴ
３１…走査線（ゲート電極）
３２…半導体層
３３…ゲート絶縁層
３４…ソース領域
３５…データ線
３６…ドレイン領域
３７、３８…コンタクトホール
４２…第１層間絶縁層
４３…第２層間絶縁層
５０…液晶層
５２…シール材
５３…額縁
７０…蓄積容量
８０、８２…シールド線（定電位線）
１０１…データ線駆動回路
１０２…外部入力端子
１０４…走査線駆動回路
２００…液晶装置
３０１…サンプリング回路
３０２…ＴＦＴ

【図６】

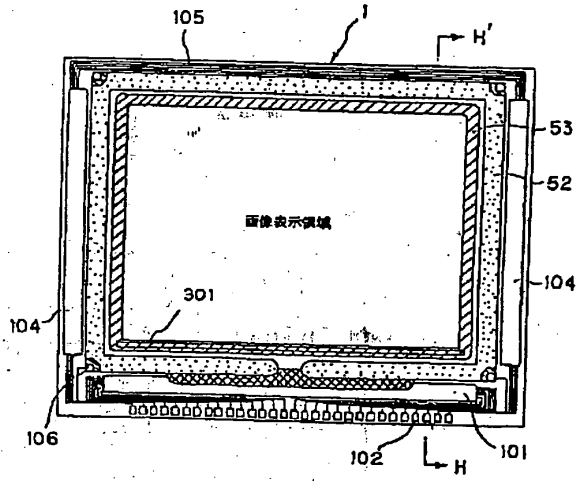


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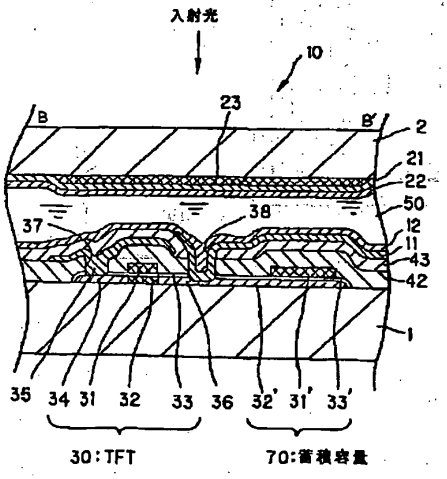
【図１】


200
105
1
106
53
104
走査線駆動回路
31
11
30
35
302
301
80
306
データ線駆動回路
101
62
102
DY
VSSY
LCOM
VSSX
VID6
VID5
VID4
VID3
VID2
VID1
VSSX
VDDX
CLX'
CLX
DX
LCOM
VDDY
CLY'
CLY
DY
Y方向
X方向

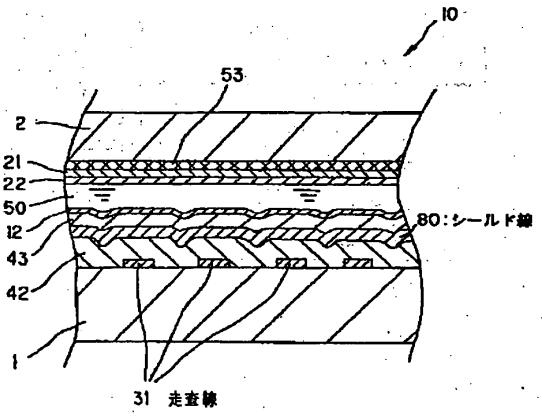
【図５】


105
1
H'
53
52
画像表示領域
104
301
104
106
102
101
H

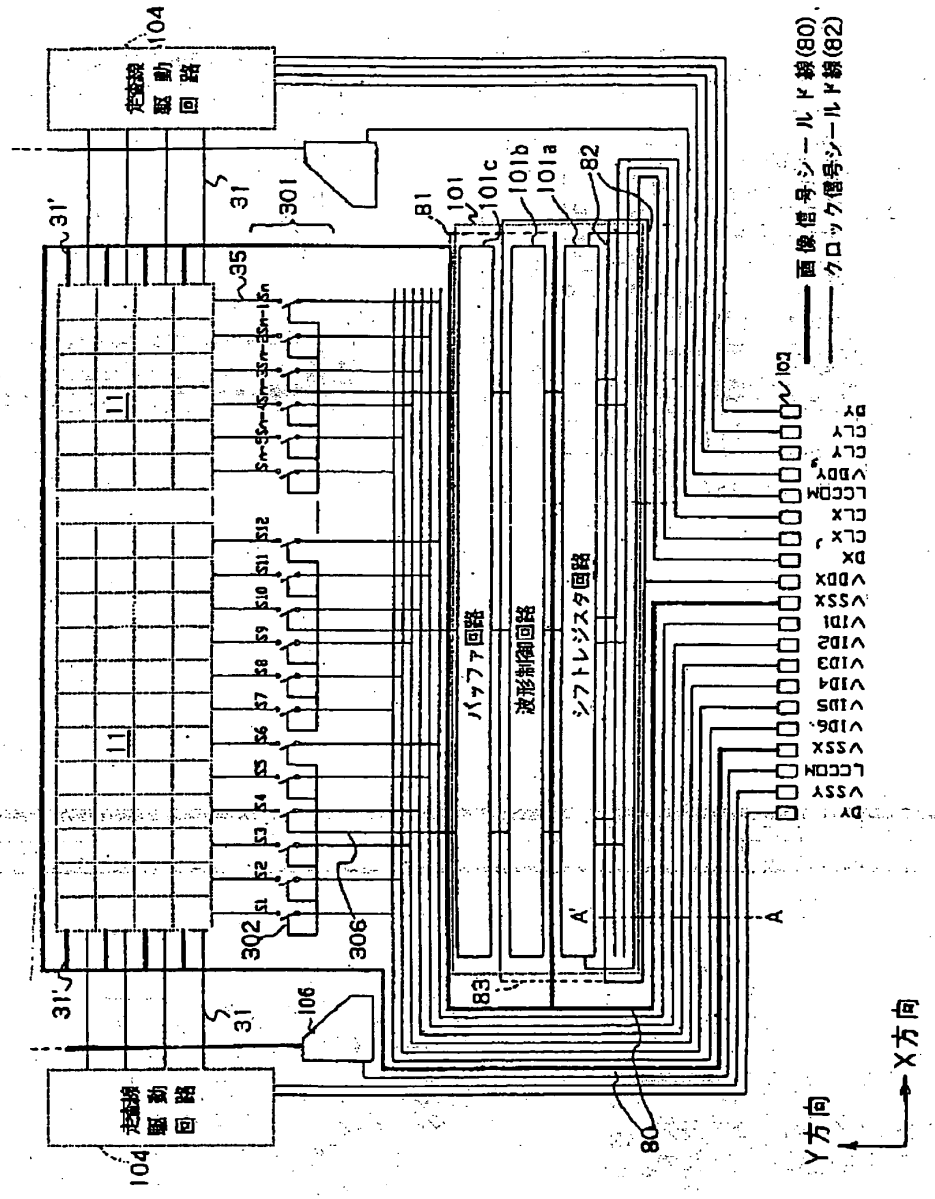
【図７】


入射光
10
23
B
B'
2
21
22
50
38
37
12
11
43
42
1
35
34
31
32
33
36
32'
31'
33'
30:TFT
70:蓄積容量

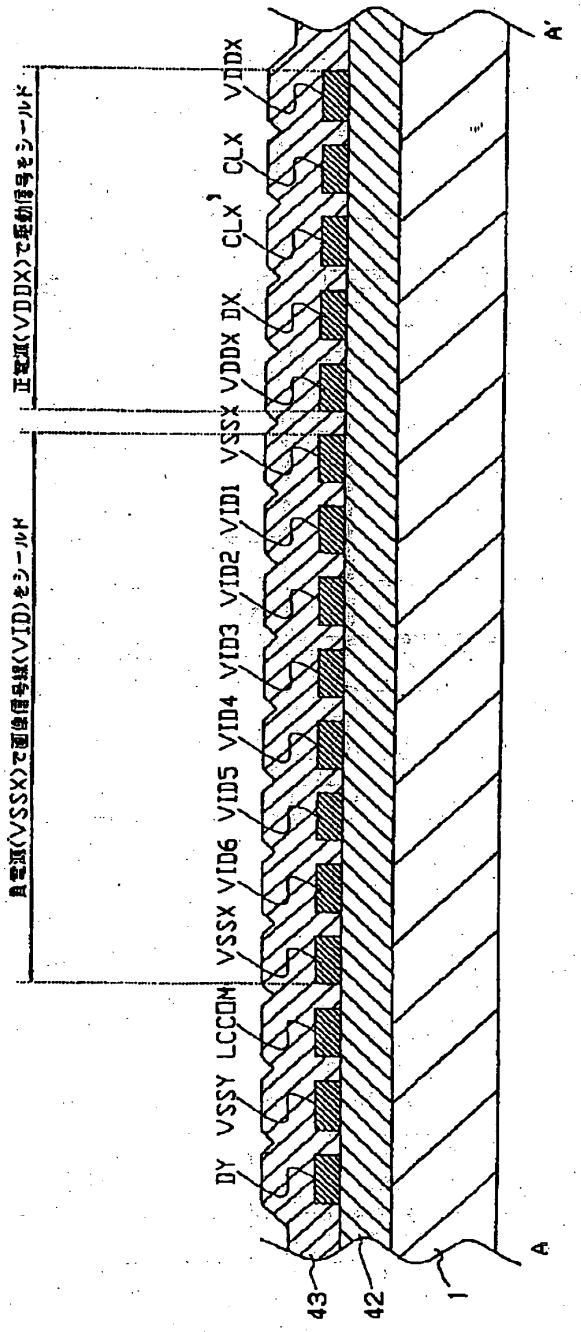
【図８】


10
53
2
21
22
50
12
43
42
1
80:シールド線
31 走査線

【図2】

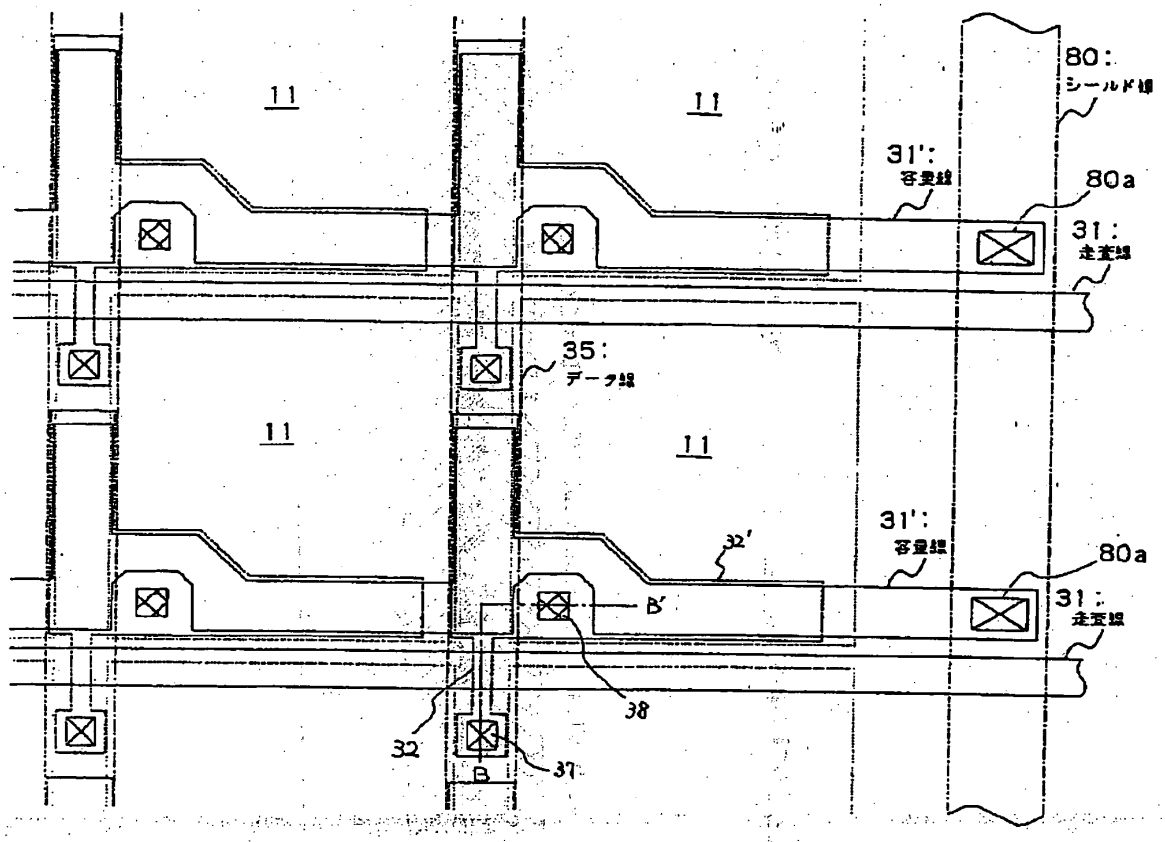

走査線駆動回路
104
31'
31
301
35
11
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
302
306
106
B1
101
101c
101b
101a
82
83
80
A
A'
バッファ回路
波形制御回路
シフトレジスタ回路
103
画像信号シールド線(80)
クロック信号シールド線(82)
DY
CLY
CLY
VDDY
LCCOM
CLX
CLX
DX
VDDX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSX
LCCOM
VSSY
DY
Y方向
X方向

【図３】

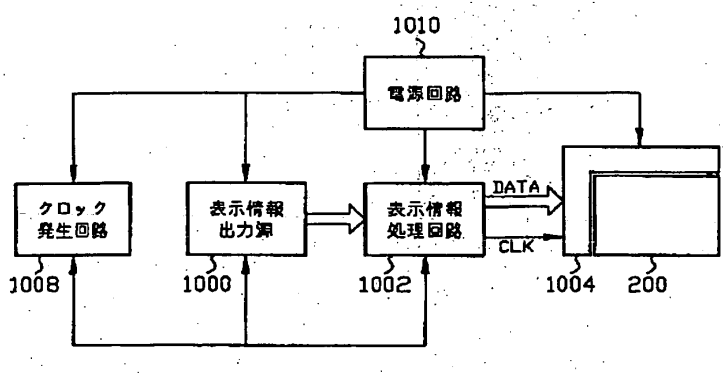

正電源(VDDX)で駆動信号をシールド
負電源(VSSX)で画像信号線(VID)をシールド
A'
VDDX
CLX
CLX'
DX
VDDX
VSSX
VID1
VID2
VID3
VID4
VID5
VID6
VSSX
LCCOM
VSSY
DY
A
43
42
1

(18)

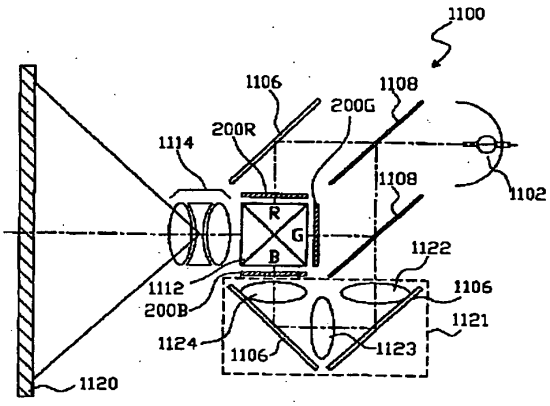
【図４】


11
11
80:
シールド線
31':
容量線
80a
31:
走査線
35:
データ線
11
11
31':
容量線
80a
31:
走査線
32'
B'
38
32
37
B

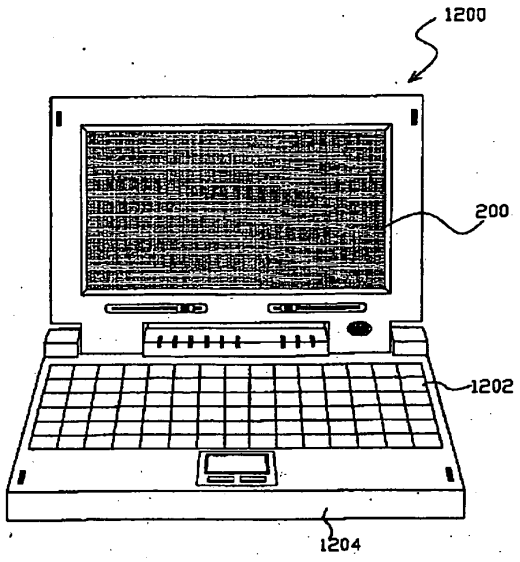
【図９】


1010
電源回路
クロック
発生回路
表示情報
出力源
表示情報
処理回路
DATA
CLK
1008
1000
1002
1004
200

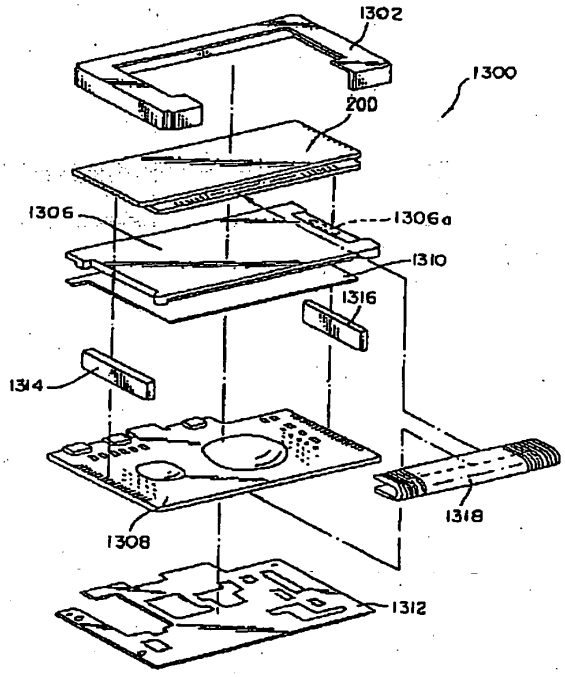
【図１０】



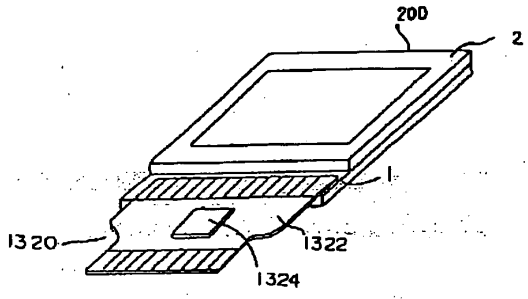
【図１１】



【図１２】



【図１３】



【公開番号】特開平１１－２２３８３２
【公報種別】特許法第１７条の２の規定による補正の掲載
【ＳＴ公報種別】A5
【公開日】平成１１年（１９９９）８月１７日
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【国際特許分類第７版】
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G02F 1/136 500
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G09G 3/36
H01L 29/78 612 C

【手続補正書】
【提出日】２００３年（２００３）６月２３日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正の内容】

【特許請求の範囲】
【請求項１】
基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線の交差に対応して設けられた複数のスイッチング素子と、前記複数のスイッチング素子に対応して設けられた複数の画素電極と、クロック信号に基づいて画像信号に対応するデータ信号を前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力される前記画像信号を前記データ信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする電気光学装置。
【請求項２】
前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むことを特徴とする請求項１に記載の電気光学装置。
【請求項３】
前記定電位線は、相異なる定電位の電源を前記データ信号供給手段に供給する第１及び第２定電位線からなり、
該第１定電位線から構成された前記導電線部分は、前記基板上で前記画像信号線を囲み、
前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むことを特徴とする請求項２に記載の電気光学装置。
【請求項４】
前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていることを特徴とする請求項２又は３に記載の電気光学装置。

日本国特許庁(JP)
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【請求項５】 3 0 4
前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていることを特徴とする請求項２から４のいずれか一項に記載の電気光学装置。
【請求項６】
前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記第特開平11-223832ように延設されたこと特徴とする請求項１から５のいずれか一項に記載の電気光学装置。
【請求項７】
前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、
前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むことを特徴とする請求項６に記載の電気光学装置。
【請求項８】
前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されたことを特徴とする請求項１から７のいずれか一項に記載の電気光学装置。
【請求項９】
前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されたことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。
【請求項１０】
前記画素電極に所定量の容量を付与する容量線を更に備えており、該容量線が前記導電線に接続されたことを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。
【請求項１１】
前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていることを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。
【請求項１２】
前記定電位配線は、前記画像信号線を囲むことを特徴とする請求項１に記載の電気光学装置。
【請求項１３】
前記定電位配線は、前記クロック信号線を囲むことを特徴とする請求項１または請求項１２に記載の電気光学装置。

【請求項１４】
前記データ信号供給手段は、シフトレジスタ回路と、前記シフトレジスタ回路からの転送信号を波形整形する波形制御回路と、前記波形制御回路から信号をバッファリングするためのバッファ回路とを備え、
前記定電位配線は、前記波形制御回路及び前記バッファ回路を囲むことを特徴とする請求項１、請求項１２、請求項１３ののいずれか一項に記載の電気光学装置。
【請求項１５】
請求項１から１４に記載の電気光学装置を備えたことを特徴とする電子機器。
【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】０００８
【補正方法】変更
【補正の内容】

【０００８】

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【課題を解決するための手段】
本発明の電気光学装置は上記課題を解決するために、基板上には複数の走査線と、前記複数の走査線に交差する複数のデータ線と、前記複数の走査線とデータ線の交差に対応して設けられた複数のスイッチング素子と、前記複数のスイッチング素子に対応して設けられた複数の画素電極と、クロック信号に基づいて画像信号に対応する前記複数のデータ線に供給するデータ信号供給手段と、第１外部入力端子から入力される前記画像信号供給手段に供給する画像信号線と、第２外部入力端子から入力される前記クロック信号を前記データ信号供給手段に供給するクロック信号線と、前記画像信号線を前記クロック信号線から電気的にシールドする定電位の導電線とを備えたことを特徴とする。【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】０００９
【補正方法】変更
【補正の内容】

【０００９】
この電気光学装置によれば、第１外部入力端子から入力される画像信号は、基板に配線された画像信号線を介して、データ信号供給手段に供給される。これと並行して、第２外部入力端子から入力されるクロック信号は、基板に配線されたクロック信号線を介して、データ信号供給手段に供給される。すると、基板に設けられた、例えばデータ線駆動回路、サンプリング回路等を含んで構成されるデータ信号供給手段により、クロック信号に基づいて画像信号に対応するデータ信号が、複数のデータ線に供給される。ここで特に、基板に配線された定電位の導電線により、画像信号線は、クロック信号線から電気的にシールドされている。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００１１
【補正方法】変更
【補正の内容】

【００１１】
また、本発明の電気光学装置の前記導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むと良い。【手続補正５】
【補正対象書類名】明細書
【補正対象項目名】００１２
【補正方法】変更
【補正の内容】

【００１２】
この電気光学装置によれば、導電線は、前記データ信号供給手段に定電位の電源を供給する定電位線から構成された部分を含むので、外部入力端子や配線そのものを共用することにより、言い換えれば定電位線を延設して導電線とすることにより、構成の簡略化と省スペース化を図ることが出来、特に導電線を定電位とすることも極めて容易となる。【手続補正６】
【補正対象書類名】明細書
【補正対象項目名】００１３
【補正方法】変更
【補正の内容】

【００１３】
また、本発明の電気光学装置の前記定電位線は、相異なる定電位の電源を前記データ信号

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供給手段に供給する第１及び第２定電位線からなり、該第１定電位線から構成された前記導電線部分は、前記基板上で前記画像信号線を囲み、前記第２定電位線から構成された前記導電線部分は、前記基板上で前記クロック信号線を囲むと良い。【手続補正７】

【補正対象書類名】明細書

【補正対象項目名】００１４

【補正方法】変更

【補正の内容】

【００１４】

この電気光学装置によれば、画像信号線は、例えば接地電位の負電源を供給するための第１定電位線から構成された導電線部分により、基板上で囲まれている。クロック信号線は、例えば正電源を供給するための第２定電位線から構成された導電線部分により、基板上で囲まれている。従って、画像信号線は、基板上でクロック信号線から２重にシールドされた構成が得られる。【手続補正８】

【補正対象書類名】明細書

【補正対象項目名】００１５

【補正方法】変更

【補正の内容】

【００１５】

また、本発明の電気光学装置の前記データ信号供給手段は、前記画像信号をサンプリングするサンプリング回路と、前記定電位線からの電源供給を受けて前記クロック信号に基づいて該サンプリング回路を駆動するデータ線駆動回路とを備えており、前記画像信号線と前記クロック信号線とは、前記基板上で前記データ線駆動回路に対して反対方向から引き回されていると良い。【手続補正９】

【補正対象書類名】明細書

【補正対象項目名】００１６

【補正方法】変更

【補正の内容】

【００１６】

この電気光学装置によれば、走査信号供給手段において、画像信号は、サンプリング回路によりサンプリングされる。そして、定電位線からの電源供給を受けるデータ線駆動回路により、クロック信号に基づいてサンプリング回路が駆動されて、サンプリングされた画像信号がデータ信号としてデータ線に供給される。ここで特に、画像信号線とクロック信号線とは、基板上でデータ線駆動回路に対して反対方向から引き回されているが、一般に距離及び障害物の介在に応じて電磁波は減少するので、クロック信号線から画像信号線に印加される電磁波が両信号線間の距離に応じて且つデータ線駆動回路の存在に応じて減少する。従って、クロック信号の周波数が高い場合でも、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを更に低減できる。【手続補正１０】

【補正対象書類名】明細書

【補正対象項目名】００１７

【補正方法】変更

【補正の内容】

【００１７】

また、本発明の電気光学装置の前記第１及び第２外部入力端子は、前記基板の周辺部において相互に所定間隔を隔てて配置されており、前記第１及び第２外部入力端子の間には、前記定電位の電源を前記定電位線に入力するための第３外部入力端子が配置されていると良い。

【手続補正１１】
【補正対象書類名】明細書
【補正対象項目名】００１８
【補正方法】変更
【補正の内容】

【００１８】
この電気光学装置によれば、第１及び第２外部入力端子は、第３外部入力端子を間に介して、基板の周辺部において相互に所定間隔を隔てて配置されており、好ましくは、基板の周辺部において外部入力端子を形成可能な領域において可能な限り相互に離して配置される。従って、例えば画像信号線とクロック信号線とを隣接配置した場合と比較して、クロック信号線から画像信号線への高周波のクロックノイズの飛び込みを低減できる。【手続補正１２】
【補正対象書類名】明細書
【補正対象項目名】００１９
【補正方法】変更
【補正の内容】

【００１９】
また、本発明の電気光学装置の前記導電線は、前記複数の画素電極により規定される画像表示領域及び前記複数のデータ線を前記基板上で囲むように延設されると良い。【手続補正１３】
【補正対象書類名】明細書
【補正対象項目名】００２０
【補正方法】変更
【補正の内容】

【００２０】
この電気光学装置によれば、導電線により、画像表示領域及び複数のデータ線は、基板上で囲まれているので、当該画像表示領域及び複数のデータ線も、クロック信号線からシールドされることになる。従って、データ信号供給手段から出力されたデータ信号、スイッチング素子や画素電極に到達したデータ信号等における、高周波のクロックノイズの発生を低減できる。【手続補正１４】
【補正対象書類名】明細書
【補正対象項目名】００２１
【補正方法】変更
【補正の内容】

【００２１】
また、本発明の電気光学装置は、前記基板に対向して対向基板が設けられてなり、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁を更に備えており、前記導電線は前記額縁に対向する位置において前記額縁に沿って前記基板に設けられた部分を含むと良い。【手続補正１５】
【補正対象書類名】明細書
【補正対象項目名】００２２
【補正方法】変更
【補正の内容】

【００２２】
この電気光学装置によれば、導電線は、基板の額縁下に設けられているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。

【手続補正１６】
【補正対象書類名】明細書
【補正対象項目名】００２３
【補正方法】変更
【補正の内容】

【００２３】
また、本発明の電気光学装置の前記導電線及び前記データ線は、同一の低抵抗金属材料から形成されると良い。【手続補正１
【補正対象書類名】明細書
【補正対象項目名】００２４
【補正方法】変更
【補正の内容】

【００２４】
この電気光学装置によれば、導電線は例えば、Ａｌ（アルミニウム）等の、データ線と同一の低抵抗金属材料から形成されているので、導電線の引き回し領域が、たとえ長くても、導電線の抵抗は実用上十分に低く抑えられる。即ち、抵抗増加によりシールドの効果を下げることなく、例えば他の配線や回路等の隙間を縫ってジグザグに導電線を長く配線したり、画像表示領域等までも含めた広い領域に導電線を長く配線することが可能となるので、比較的簡単な構成により、当該シールドの効果を全体として、より高めることが出来る。更に、当該電気光学装置の製造プロセスにおいて、導電線及びデータ線を、同一の低抵抗金属材料から同一工程により形成できる。即ち、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。【手続補正１８】
【補正対象書類名】明細書
【補正対象項目名】００２５
【補正方法】変更
【補正の内容】

【００２５】
また、本発明の電気光学装置は、前記画像信号線及びクロック信号線の間に介在する前記導電線部分並びに前記画像信号線及びクロック信号線は、前記第１基板に平行な同一平面上に形成された同一の低抵抗金属層から構成されると良い。【手続補正１９】
【補正対象書類名】明細書
【補正対象項目名】００２６
【補正方法】変更
【補正の内容】

【００２６】
この電気光学装置によれば、画像信号線及びクロック信号線の間に介在する導電線部分は、画像信号線やクロック信号線と、基板に平行な同一平面上に形成されているので、シールドの効果がより効率良く発揮される。ここで、同一平面上とは、基板の上に直接これらを配線してもよく、或いは基板上に形成された下地となる絶縁層上やＴＦＴ等のスイッチング素子の半導体層上に形成された層間絶縁層上にこれらを配線してもよいという意味である。更に、当該電気光学装置の製造プロセスにおいて、導電線、画像信号線及びクロック信号線を、例えば、Ａｌ層等の同一の低抵抗金属層から一括して形成できるので、導電線を形成することによる製造プロセスの増加を最低限に抑えることができる。【手続補正２０】
【補正対象書類名】明細書
【補正対象項目名】００２７
【補正方法】変更

【補正の内容】 13 14

【００２７】
また、本発明の電気光学装置は、前記画素電極に所定量の容量を付与する容量線を更に備えており導電線に接続されると良い。【手続補正２１】
【補正対象書類名】明細書
【補正対象項目名】００２８
【補正方法】変更
【補正の内容】

【００２８】
この電気光学装置によれば、容量線により画素電極に所定量の容量が付与されているので、デューティー比が小さくても高精細な表示が可能とされる。そして、容量線は導電線に接続されている。従って、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。【手続補正２２】
【補正対象書類名】明細書
【補正対象項目名】００２９
【補正方法】変更
【補正の内容】

【００２９】
また、本発明の電気光学装置は、前記基板に対向して対向基板が設けられ、前記画像表示領域の輪郭に沿って前記基板及び前記対向基板のうち少なくとも一方に形成された遮光性の額縁と、前記画素電極に容量を付与する容量線とを更に備えており、前記導電線は前記額縁に対向する位置に延設されるとともに、前記対向する位置において前記導電線に前記容量線が接続されていると良い。【手続補正２３】
【補正対象書類名】明細書
【補正対象項目名】００３０
【補正方法】変更
【補正の内容】

【００３０】
この電気光学装置によれば、導電線は、基板の額縁に対向配置されているので、ＴＦＴアレイ基板上の省スペース化が図られ、例えば、走査線駆動回路やデータ線駆動回路を第１基板の周辺部分に余裕を持って形成することができ、導電線形成により電気光学装置における有効表示面積が減少することも殆ど又は全くない。また、容量線は導電線に接続されているため、容量線の電位変動によるスイッチング素子や画素電極への悪影響は防止されている。しかも、容量線を定電位とするための配線を導電線で兼用でき、更に、容量線を定電位にするために必要な外部入力端子も、例えば、前述の第３外部入力端子或いは導電線専用の外部入力端子で兼用できる。また、導電線と容量線との接続は額縁に対向配置されるため、ＴＦＴ基板上有効表示面積を減少させることなく、スペースを有効利用することができる。【手続補正２４】
【補正対象書類名】明細書
【補正対象項目名】００３１
【補正方法】変更
【補正の内容】

【００３１】
また、本発明の電子機器は、上述した電気光学装置を備えたことを特徴とする。

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特開平11-223832

【手続補正２５】
【補正対象書類名】明細書
【補正対象項目名】００３２
【補正方法】変更
【補正の内容】

【００３２】
この電子機器によれば、電子機器は、上述した本願発明の電気光学装置を備えており、高周波のクロックノイズが低減されており、高品位の画像表示が可能となる。

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PATENT ABSTRACTS OF JAPAN

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(72)Inventor : MURADE MASAO

(30)Priority

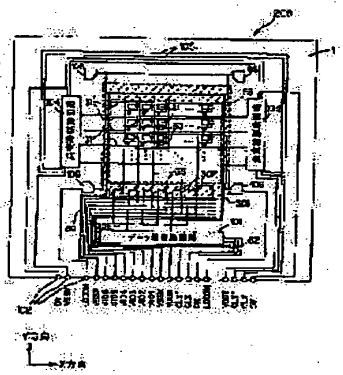
Priority number : 09301253 Priority date : 31.10.1997 Priority country : JP

(54) ELECTROOPTIC DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the occurrence of high frequency clock noise in an inputted image signal and a data signal formed on the basis thereof in an electrooptic device such as an active matrix drive type liquid crystal device.

SOLUTION: A liquid crystal device 200 has a liquid crystal layer sandwiched between a couple of substrates, pixel electrodes 11 provided in matrix on the substrate 1, and TFTs 30 which perform switching control over the electrodes, Shield wires 80 and 82 of a constant potential which electrically shield image signal lines VID1 to VID6 from clock signal lines CLX and CLX' are wired on the substrates. Thus, a high quality image can be displayed according to the high frequency image signal for displaying a high resolution image.



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CLAIMS

[Claim(s)]
[Claim 1] Two or more data lines which intersect two or more scanning lines and said two or more scanning lines on a substrate, Two or more switching elements connected to two or more of said scanning lines and data lines, Two or more pixel electrodes connected to said two or more switching elements, and a data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, The electro-optic device characterized by having the clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line.
[Claim 2] Said electric conduction line is an electro-optic device according to claim 1 characterized by including the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means.
[Claim 3] said law -- a potential line -- difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part It is the electro-optic device according to claim 2 characterized by surrounding said picture signal line on said substrate, and the amount of [said / which consisted of potential lines the 2nd law] said electric conduction line part surrounding said clock signal line on said substrate.
[Claim 4] Said data signal supply means is an electro-optic device according to claim 2 or 3 which is equipped with the sampling circuit which samples said picture signal, and the data-line actuation circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line, and is characterized by taking about said picture signal line and said clock signal line from an opposite direction to said data-line actuation circuit on said substrate.
[Claim 5] said 1st and 2nd external input terminal separates and arranges predetermined spacing mutually in the periphery of said substrate -- having -- **** -- between said 1st and 2nd external input terminals -- said law -- the power source of potential -- said law -- an electro-optic device given in any 1 term of claims 2-4 characterized by arranging the 3rd external input terminal for inputting into a potential line.
[Claim 6] Said electric conduction line is an electro-optic device given in any 1 term of claims 1-5 by which it is installing [so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said 1st substrate] characterized.
[Claim 7] It is the electro-optic device according to claim 6 which said substrate was countered, and the opposite substrate was formed, is further equipped with the frame of the protection-from-light nature formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, and is characterized by said electric conduction line containing the part prepared in said substrate along with said frame in the location which counters said frame.
[Claim 8] Said electric conduction line and said data line are an electro-optic device given in any 1 term of claims 1-7 characterized by being formed from the same low resistance metallic material.

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[Claim 9] It is an electro-optic device given in any 1 term of claims 1-8 characterized by consisting of same low resistance metal layers formed by said electric conduction line part part list which intervenes between said picture signal line and a clock signal line on the same flat surface where said picture signal line and a clock signal line are parallel to said substrate.
[Claim 10] An electro-optic device given in any 1 term of claims 1-9 characterized by equipping said pixel electrode with the capacity line which gives the capacity of the specified quantity further, and connecting this capacity line to said electric conduction line.
[Claim 11] The frame of the protection-from-light nature which said substrate was countered, and the opposite substrate was formed and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, It is an electro-optic device given in any 1 term of claims 1-6 which equip said pixel electrode with the capacity line which gives capacity further, and are characterized by connecting said capacity line to said electric conduction line in said location which counters while said electric conduction line is installed in the location which counters said frame.
[Claim 12] Electronic equipment characterized by equipping claims 1-11 with the electro-optic device of a publication.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of the electronic equipment using the electro-optic device of a active-matrix actuation method and this by thin film transistor (TFT is called suitably below) actuation, and belongs to the technical field of the electro-optic device of the format of driving the data line by the RF based on a clock signal by the data-line actuation circuit especially prepared on the TFT array substrate, and the electronic equipment using this.
[0002]
[Description of the Prior Art] Conventionally, in electro-optic devices, such as liquid crystal equipment of the active-matrix actuation method by TFT actuation, many pixel electrodes are prepared on the TFT array substrate at many the scanning lines and the data-line lists which were arranged in all directions, respectively corresponding to each of these intersections. And in addition to these, a data signal supply means to supply a data signal to the data line including a data-line actuation circuit, a sampling circuit, etc., and a scan signal supply means to supply a scan signal to the scanning line including a scanning-line actuation circuit etc. may be established on such a TFT array substrate.
[0003] In this case, the data-line side reference clock used as the criteria of the supply timing of a data signal, the picture signal which supports the content of the image which should be displayed and serves

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as a radical of a data signal, forward, a negative constant potential power source, etc. are supplied to a data signal supply means through the external input terminal and wiring which were prepared in the TFT array substrate, respectively. On the other hand, forward [used as the criteria of the supply timing of a scan signal / the scanning-line side reference clock and forward], a negative constant potential power source, etc. are supplied to a scan signal supply means through the external input terminal and wiring which were too prepared in the TFT array substrate. And in a scan signal supply means, a scan signal is supplied to the scanning line to the timing based on a scanning-line side reference clock, for example by the scanning-line actuation circuit line sequential. A data-line actuation circuit carries out sequential actuation of the sampling circuit which samples the picture signal inputted in the data signal supply means corresponding to this, for example to the timing based on a data-line side reference clock, and a data signal is supplied to the data line from a sampling circuit. These results, each TFT by which gate connection was made is made into switch-on at the scanning line according to supply of a scan signal, a data signal is supplied to a pixel electrode through the TFT concerned, and image display in each pixel is performed.

[0004] With the liquid crystal equipment for liquid crystal projectors, a picture signal with a serial, very high frequency is increasingly inputted recent years especially with high-resolution-izing of a display image. That it should correspond to this, the frequency of the data-line side reference clock supplied to especially a data signal supply means is also very high, and it is carried out.

[0005]

[Problem(s) to be Solved by the Invention] However, under the request of high-definition-izing of a display image in recent years, generating of the clock noise of a RF by making the frequency of a reference clock high in this way cannot ignore now.

[0006] That is, in the configuration which supplies the conventional data-line side reference clock with a comparatively low frequency to a data-line actuation circuit, for example, and drives a sampling circuit, by having raised the frequency of a clock signal as it was, the clock noise of high frequency will occur in the data signal outputted from the inside of the picture signal inputted into a sampling circuit, or a sampling circuit, and the data signal which should be supplied at the data line will deteriorate. Thus, by that of a carrier beam, there is a trouble displayed with each pixel electrode of carrying out image mist beam degradation, about supply of the data signal which deteriorated.

[0007] This invention is made in view of an above-mentioned trouble, and generating of the clock noise of the RF in the data signal generated based on the inside of the inputted picture signal or this can be reduced, and let it be a technical problem to offer electronic equipment equipped with the electro-optic device which can perform high-definition image display, and the electro-optic device concerned.

[0008]

[Means for Solving the Problem] Two or more scanning lines [top / substrate] in order that an electro-optic device according to claim 1 may solve the above-mentioned technical problem, Two or more data lines which intersect said two or more scanning lines, and two or more switching elements connected to two or more of said scanning lines and data lines, Two or more pixel electrodes connected to said two or more switching elements, and a data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, It is characterized by having the clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line.

[0009] According to the electro-optic device according to claim 1, the picture signal inputted from the 1st external input terminal is supplied to a data signal supply means through the picture signal line wired by the substrate. In parallel to this, the clock signal inputted from the 2nd external input terminal is supplied to a data signal supply means through the clock signal line wired by the substrate. Then, based on a clock signal, the data signal corresponding to a picture signal is supplied to two or more data lines

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by the data signal supply means which was formed in the substrate, for example, is constituted including a data-line actuation circuit, a sampling circuit, etc. The picture signal line is electrically shielded from the clock signal line by the electric conduction line of the constant potential wired by the substrate especially here. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.

[0010] A scan signal is supplied to a switching element through the scanning line by the scan signal supply means including the scanning-line actuation circuit which was formed in the substrate or was connected to the substrate on the other hand. The electrical potential difference impressed to a pixel electrode by the data signal which the data signal corresponding to the picture signal with which the clock noise of high frequency was reduced as mentioned above is supplied to a switching element through the data line in parallel to this, and is further supplied through a switching element changes, and the liquid crystal which counters the pixel electrode concerned drives. image quality deteriorates according to generating of the clock noise of a RF, using [the resolution of the image which should be displayed is high the above result, and] a clock signal with a high frequency corresponding to this, also when the serial picture signal of a RF is inputted -- most -- or it is completely lost and high-definition image display is made possible.

[0011] An electro-optic device according to claim 2 is characterized by said electric conduction line containing the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means in an electro-optic device according to claim 1.

[0012] Since the part which consisted of constant potential lines by which an electric conduction line supplies the power source of constant potential to said data signal supply means according to the electro-optic device according to claim 2 is included, in other words, it also becomes very easy by sharing an external input terminal and the wiring itself to be able to attain simplification and space-saving-izing of a configuration, especially to make an electric conduction line into constant potential by installing a constant potential line and considering as an electric conduction line.

[0013] An electro-optic device according to claim 3 is set to an electro-optic device according to claim 2. Said constant potential line difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part Said picture signal line is surrounded on said substrate, and a part for said said electric conduction line part which consisted of potential lines the 2nd law is characterized by surrounding said clock signal line on said substrate.

[0014] According to the electro-optic device according to claim 3, the picture signal line is surrounded by the amount of [by which potential lines were consisted of the 1st law in order to supply the negative supply of for example, touch-down potential] electric conduction line part on the substrate. The clock signal line is surrounded by the amount of [by which potential lines were consisted of the 2nd law in order to supply a positive supply] electric conduction line part on the substrate. Therefore, the configuration from which the picture signal line was shielded [line / clock signal] by the duplex on the substrate is obtained.

[0015] The electro-optic device according to claim 4 is equipped with the sampling circuit where said data signal supply means samples said picture signal, and the data-line actuation circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line in the electro-optic device according to claim 2 or 3, and said picture signal line and said clock signal line are characterized by taking about from an opposite direction to said data-line actuation circuit on said substrate.

[0016] According to the electro-optic device according to claim 4, a picture signal is sampled by the sampling circuit in a scan signal supply means. And the picture signal with which the sampling circuit drove and was sampled by the data-line actuation circuit which receives the current supply from a constant potential line based on the clock signal is supplied to the data line as a data signal. Especially,

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although the picture signal line and the clock signal line are taken about from the opposite direction to the data-line actuation circuit on the substrate, since an electromagnetic wave generally decreases according to inclusion of distance and an obstruction, the electromagnetic wave impressed to a picture signal line decreases here according to existence of a data-line actuation circuit from a clock signal line, corresponding to the distance between both signal lines. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced further.

[0017] In an electro-optic device given in any 1 term of claims 2-4, in the periphery of said substrate, said 1st and 2nd external input terminal separates predetermined spacing mutually,,and is arranged, and an electro-optic device according to claim 5 is characterized by arranging the 3rd external input terminal for inputting the power source of said constant potential into said constant potential line between said 1st and 2nd external input terminals.

[0018] According to the electro-optic device according to claim 5, in between, the 1st and 2nd external input terminal separates predetermined spacing mutually, is arranged in the periphery of a substrate, through the 3rd external input terminal, mutually, and is preferably detached and arranged as much as possible mutually in the field which can form an external input terminal in the periphery of a substrate. As compared with the case where followed, for example, contiguity arrangement of a picture signal line and the clock signal line is carried out, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.

[0019] An electro-optic device according to claim 6 is installing [so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said substrate] characterized by said electric conduction line in an electro-optic device given in any 1 term of claims 1-5.

[0020] According to the electro-optic device according to claim 6, by the electric conduction line, since an image display field and two or more data lines are surrounded on the substrate, an image display field and two or more data lines concerned will also be shielded from a clock signal line. Therefore, generating of the clock noise of a RF in the data signal outputted from the data signal supply means, the data signal which reached the switching element and the pixel electrode can be reduced.

[0021] An electro-optic device according to claim 7 is set to an electro-optic device according to claim 6. It has further the frame of the protection-from-light nature which countered said substrate, and it came to prepare an opposite substrate, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field. It is characterized by said electric conduction line containing the part prepared in said substrate along with said frame in the location which counters said frame.

[0022] since the electric conduction line is formed in the bottom of the frame of a substrate according to the electro-optic device according to claim 7, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line actuation circuit and a data-line actuation circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing.

[0023] An electro-optic device according to claim 8 is characterized by forming said electric conduction line and said data line from the same low resistance metallic material in an electro-optic device given in any 1 term of claims 1-7.

[0024] According to the electro-optic device according to claim 8, since the electric conduction line is formed from the same low resistance metallic material as the data lines, such as aluminum (aluminum), even if the leading-about field of an electric conduction line is long, resistance of an electric conduction line will be suppressed low practically enough. That is, since it becomes possible to wire the large field which sewed clearances, such as other wiring and a circuit, for example, wired zigzag for a long time, or included the electric conduction line in it to the image display field etc. for a long time in an electric conduction line, without lowering the effectiveness of shielding by the increment in resistance, a

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comparatively easy configuration can raise the effectiveness of the shielding concerned more as a whole. Furthermore, in the manufacture process of the electro-optic device concerned, an electric conduction line and the data line can be formed according to the same process from the same low resistance metallic material. That is, the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.

[0025] An electro-optic device according to claim 9 is characterized by said picture signal line and a clock signal line consisting of same low resistance metal layers formed on the same flat surface parallel to said 1st substrate at said electric conduction line part part list which intervenes between said picture signal line and a clock signal line in an electro-optic device given in any 1 term of claims 1-8.

[0026] According to the electro-optic device according to claim 9, since a part for the electric conduction line part which intervenes between a picture signal line and a clock signal line is formed on the picture signal line, the clock signal line, and the same flat surface parallel to a substrate, the effectiveness of shielding is demonstrated more efficiently. Here, the same flat-surface top means that you may wire these on the layer insulation layer formed on the semi-conductor layer of switching elements, such as an insulating-layer top used as the substrate which could wire these directly on the substrate or was formed on the substrate, and TFT. Furthermore, in the manufacture process of the electro-optic device concerned, since an electric conduction line, a picture signal line, and a clock signal line can be collectively formed from a low resistance metal layer for example, with same aluminum layer etc., the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.

[0027] The electro-optic device according to claim 10 equips said pixel electrode with the capacity line which gives the capacity of the specified quantity further in the electro-optic device given in any 1 term of claims 1-9, and it is characterized by connecting this capacity line to said electric conduction line.

[0028] According to the electro-optic device according to claim 10, since the capacity of the specified quantity is given to the pixel electrode by the capacity line, even if duty ratio is small, a high definition display is enabled. And the capacity line is connected to the electric conduction line. Therefore, the adverse effect to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines.

[0029] The frame of the protection-from-light nature which the electro-optic device according to claim 11 countered said substrate, and the opposite substrate was formed, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, Said pixel electrode is further equipped with the capacity line which gives capacity, and said electric conduction line is characterized by connecting said capacity line to said electric conduction line in said location which counters while it is installed in the location which counters said frame.

[0030] since opposite arrangement of the electric conduction line is carried out at the frame of a substrate according to the electro-optic device according to claim 11, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line actuation circuit and a data-line actuation circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing. Moreover, since the capacity line is connected to the electric conduction line, the adverse effect to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction

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lines. Moreover, the connection between an electric conduction line and a capacity line can use a tooth space effectively for a frame, without decreasing a TFT substrate top display area, since opposite arrangement is carried out.

[0031] Electronic equipment according to claim 12 is characterized by equipping claims 1-10 with the electro-optic device of a publication.

[0032] According to electronic equipment according to claim 12, it has the electro-optic device of the invention in this application mentioned above, the clock noise of a RF is reduced, and the high-definition image display of electronic equipment becomes possible.

[0033] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.

[0034]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing. In addition, this operation gestalt explains, using liquid crystal equipment as an example of an electro-optic device.

[0035] (Configuration of liquid crystal equipment) The configuration of the gestalt of operation of liquid crystal equipment is explained based on drawing 6 from drawing 1 . Drawing 1 is the top view showing the configuration of a various wiring, a circumference circuit, etc. which were prepared on the TFT array substrate in the gestalt of operation of liquid crystal equipment. Drawing 2 It is the top view showing the more detailed two-dimensional layout of drawing 1 . Drawing 3 It is the A-A' sectional view of drawing 2 showing wiring of a picture signal line, a clock signal line, etc. drawing 4 R> 4 It is the amplification top view of the pixel part of drawing 1 , drawing 5 is the top view which looked at the TFT array substrate from the opposite substrate side with each component formed on it, and drawing 6 is a H-H' sectional view of drawing 5 shown including an opposite substrate.

[0036] Liquid crystal equipment 200 is equipped with the TFT array substrate 1 which consists of a quartz substrate, hard glass, etc. in drawing 1 . Two or more pixel electrodes 11 prepared in the shape of a matrix on the TFT array substrate 1, The data line 35 which two or more arrays are carried out in the direction of X, and is extended along the direction of Y, respectively, The scanning line 31 which two or more arrays are carried out in the direction of Y, and is extended along the direction of X, respectively, While intervening between each data line 35 and the pixel electrode 11, respectively, two or more TFT30 as an example of the switching element which controls the switch-on and the non-switch-on between these according to the scan signal supplied through the scanning line 31, respectively, respectively is formed. Moreover, on the TFT array substrate 1, capacity line 31' (storage capacitance electrode) which is wiring for the below-mentioned storage capacitance (refer to drawing 6) is formed in the scanning line 31 and parallel.

[0037] On the TFT array substrate 1, the sampling circuit 301 and the data-line actuation circuit 101 which constitute an example of a data signal supply means, and the scanning-line actuation circuit 104 are formed further. moreover, to the top chord of the image display field (namely, field of the liquid crystal equipment with which an image is actually displayed by the orientation change of state of liquid crystal) specified with two or more pixel electrodes 11 Two or more wiring 105 for connecting between the scanning-line actuation circuits 104 established in the both sides of an image display field is formed, and the vertical flow terminal 106 for taking an electric flow between the TFT array substrate 1 and an opposite substrate is formed in the four corners of an image display field. The signal name inputted through the external input terminal 102 prepared along the lower side of the TFT array substrate 1 in explanation of drawing 3 and its signal wiring are made into what (for example, the signal wiring is called "Wiring CLX" to the "clock signal CLX" which is a signal name) the alphabet notation same for easy-izing of explanation is added, respectively, and is referred to for after a signal and wiring from drawing 1 below. [two or more]

[0038] The scanning-line actuation circuit 104 starts a built-in shift register circuit by the input of the start signal DY for scanning-line actuation circuits, using the negative supply VSSY and positive supply

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VDDY for scanning-line actuation circuits which are supplied to external input terminal 102 list through Wiring VSSY and VDDY from an external-control circuit as a power source. and -- an external input -- a terminal -- 102 -- a list -- wiring -- CLY -- and -- CLY -- ' -- minding -- supplying -- having -- the scanning line -- actuation -- a circuit -- ** -- a reference clock -- a signal -- CLY -- and -- the -- reversal -- a clock signal -- CLY -- ' -- being based -- predetermined -- timing -- the scanning line 31 -- a scan signal -- a pulse ---like -- line sequential -- impressing .

[0039] The data-line actuation circuit 101 starts a built-in shift register circuit by the input of start signal DX for data-line actuation circuits, using the negative supply VSSX and positive supply VDDX for data-line actuation circuits which are supplied to external input terminal 102 list through signal wiring VSSX and VDDX from an external-control circuit as a power source. and the reference clock signal CLX for data-line actuation circuits supplied to external input terminal 102 list through Wiring CLX and CLX' and its reversal clock signal CLX -- ' -- being based -- It doubles with the timing to which the scanning-line actuation circuit 104 impresses a scan signal. About picture signal [which is supplied through the external input terminal 102 and wiring VID1-VID6 / by which serial-parallel conversion was carried out] VID1 - VID6 each, for example to six phases A sampling circuit driving signal is minded every data line 35, the sampling circuit actuation signal line 306 is minded [301], and it supplies to predetermined timing.

[0040] The sampling circuit 301 is equipped with TFT302 every data line 35, wiring VID1-VID6 is connected to the source electrode of TFT302, and the sampling circuit actuation signal line 306 is connected to the gate electrode of TFT302. And an input of picture signals VID1-VID6 samples these picture signals. Moreover, if a sampling circuit driving signal is inputted from the data-line actuation circuit 101 through the sampling circuit actuation signal line 306, sequential impression of the picture signal sampled about picture signal VID1 - VID6 each will be carried out for every group who consists of the six adjoining data lines 35. As mentioned above, the data-line actuation circuit 101 and the sampling circuit 301 are constituted so that the picture signals VID1-VID6 by which serial-parallel conversion was carried out may be supplied to six phases as a data signal at the data line 35. 2 which may choose the data line 35 for [every] and adjoins although the gestalt of this operation described the method which chooses simultaneously the sampling circuit 301 connected to the six adjoining data lines 35, and consists of the six data lines 35, and which carries out the sequential transfer for every group, 3, --, 5 - - or seven or more may be chosen simultaneously. moreover, as long as the write-in property of TFT302 which constitutes not only six phases but the sampling circuit 301 of the number of serial-parallel conversion of the picture signal supplied to the data line 35 is good, five or less phases are sufficient as it -- if it carries out and the frequency of a picture signal is high -- the increase more than seven phase -- you may carry out. Under the present circumstances, it cannot be overemphasized that the external input terminal 102 and picture signal line for picture signals only of the number of serial-parallel conversion of a picture signal are the need at least.

[0041] As shown in drawing 2 , if start signal DX is inputted, after the data-line actuation circuit 101 shapes in waveform and buffers the transfer signal from shift-register-circuit 101a which starts sequential generation of the reference clock signal CLX and the transfer signal based on the reversal clock signal CLK', and shift-register-circuit 101a, it is equipped with wave control circuit 101b and buffer circuit 101c which are supplied to a sampling circuit 301 through the sampling circuit actuation signal line 306. Moreover, corresponding to the picture signals VID1-VID6 with which serial-parallel conversion of the sampling circuit 301 was carried out at six phases, six TFT(s)302 are connected at a time to each sampling circuit actuation signal line 306 at parallel. That is, the switches S1-S6 which consist of TFT(s)302 are connected to 1 Motome's sampling circuit actuation signal line 306 from the left, switches S7-S12 are connected to 2 Motome's sampling circuit actuation signal line 306 from the left, and switch Sn-5 - Sn are connected to the right end sampling circuit actuation signal line 306.

[0042] Especially with the gestalt of this operation, as shown in drawing 1 and drawing 2 , the shielding wire 82 of the constant potential which served as the electric conduction line (shielding wire is called

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hereafter) 80 of the constant potential which served as the wiring VSSX for negative supplies VSSX, and the wiring VDDX for positive supplies VDDX to the TFT array substrate 1 is wired. By such shielding wire 80 and 82, wiring VID1-VID6 is electrically shielded from Wiring CLX and CLX'. Therefore, even when the frequency of a clock signal CLX is high, the diving of the clock noise of the RF to Wiring CLX and the wiring VID1-VID6 from CLX' can be reduced.

[0043] In addition, the frequency of the clock signal CLY (and the reversal clock signal CLY') for scanning-line actuation is far low compared with the frequency of the above-mentioned clock signal CLX (and the reversal clock signal CLX') for data-line actuation. Therefore, about a clock signal CLY and CLY', it is rare for the clock noise of a RF to pose a problem. However, in the gestalt of this operation, as shown in drawing 1 and drawing 2 , wiring VID1-VID6 is wired also from Wiring CLY and CLY', by shielding wire 80 and 82, so that it may shield. That is, along the bottom of the frame 53 of the protection-from-light nature prepared in the opposite substrate 2, the shielding wire 80 which was installed from the external input terminal 102 and served as the negative supply VSSX of the data-line actuation circuit 101 is wired so that an image display field may be surrounded. Therefore, not only the wiring VID1-VID6 for picture signals but the diving of the noise from the circumference circuit to the data line 35 with which a data signal is written in through TFT302 of a sampling circuit 301 can be reduced.

[0044] Especially, with the gestalt of this operation, by installing Wiring VSSX and VDDX, respectively and considering as shielding wire 80 and 82, it becomes possible to share an external input terminal and wiring, and simplification and space-saving-izing of an equipment configuration can be attained. Moreover, potential of shielding wire 80 and 82 is easily made constant potential by common use-ization with a constant potential line in this way. However, you may wire wiring for power sources, and shielding wire separately.

[0045] Moreover, as long as the supply voltage for driving the data-line actuation circuit 101 and the scanning-line actuation circuit 104 is mutually the same, VSSX and VSSY which are the potential (negative potential) of VDDX which is the potential (forward potential) of a positive supply and VDDY, and a negative supply may be made to share, respectively. If such a configuration is taken, since wiring installed from an external input terminal and it is reducible, it is advantageous.

[0046] With the gestalt of this operation, as shown in drawing 2 , two external input terminals 102 into which a negative supply VSSX is inputted are formed, and the-two wiring VSSX is formed corresponding to this. And wiring VID1-VID6 is surrounded on the TFT array substrate 1 by the shielding wire 80 made into the potential (negative potential) of a negative supply VSSX. Especially the shielding wire 80 formed from metal layers, such as the same aluminum as the data line 35, also between shift-register-circuit 101a and wave control circuit 101b is installed. And through the shielding-wire connection 81 which metal layers, such as aluminum, set caudad through the insulating layer between the 1st layer like the after-mentioned, for example, was formed from conductive layers, such as the same polish recon as the scanning line 31, as the point of the installed shielding wire 80 surrounds wave control circuit 101b and buffer circuit 101c, it is connected to shielding wire 80.

[0047] On the other hand, as shown in drawing 2 , Wiring CLX and CLX' are surrounded on the TFT array substrate 1 in the part which adjoins the data-line actuation circuit 101 by the shielding wire 82 made into the potential (forward potential) of a positive supply VDDX. Especially the shielding wire 82 formed from metal layers, such as the same aluminum as the data line 35, also between wave control circuit 101b and buffer circuit 101c is installed, and as the point surrounds wave control circuit 101b and shift-register-circuit 101a through the shielding-wire connection 83 formed from conductive layers, such as the same polish recon as the scanning line 31, it is connected to shielding wire 82.

[0048] Therefore, the configuration shielded by the duplex is taken from Wiring CLX and CLX' on the TFT array substrate 1, and let wiring VID1-VID6 be what has dependability high [shielding to wave control circuit 101b and buffer circuit 101c] at the shift-register-circuit 101a list. However, if it constitutes as intervened in shielding wire 80 or at least one 82 between Wiring CLX, and CLX' and

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wiring VID1–VID6 even if it does not take the configuration surrounded in this way, the effectiveness of shielding will be acquired somewhat.

[0049] With the gestalt of this operation, as shown in drawing 1 and drawing 2 , wiring VID1–VID6, Wiring CLX, and CLX' are taken about by the reverse sense along the direction of X on the TFT array substrate 1 (namely, the former a clockwise rotation, latter is counter clockwise). Therefore, since the electromagnetic wave which transmits between these wiring according to inclusion of the data–line actuation circuit 101 among these wiring decreases since the distance during these wiring becomes large as a whole and, even when the frequency of a clock signal CLX and CLX' is high, the diving of the clock noise of the RF to Wiring CLX and the wiring VID1–VID6 from CLX' can be reduced further. Moreover, even if, as for leading about of Wiring CLX, and CLX' and wiring VID1–VID6, the direction interchanges, it is satisfactory in any way. That is, Wiring CLX and CLX' may be shielded by the negative supply VSSX, and wiring VID1–VID6 may be shielded by the positive supply VDDX. However, if it constitutes as intervened in shielding wire 80 or at least one 82 between Wiring CLX, and CLX' and wiring VID1–VID6 even if it does not take the configuration taken about to an opposite direction in this way, the effectiveness of shielding will be acquired somewhat.

[0050] With the gestalt of this operation, in between, through three external input terminals 102 for the object for negative supply VSSX, the object for positive supply VDDX, and start signal DX, a clock signal CLX and the external input terminal 102 for CLX', and the external input terminal 102 a picture signal VID1 – for VID6 separate predetermined spacing mutually, and are arranged mutually. And in the periphery of the TFT array substrate 1, in the field which can form the external input terminal 102, the external input terminal 102 of a clock signal CLX and the external input terminal 102 for CLX', and the for a picture signal VID1 – for VID6 as possible detaches mutually, and is arranged, and the external input terminal 102 more than a piece is preferably arranged among both at least. Thus, if constituted, as compared with the case where contiguity arrangement of a picture signal line and the clock signal line is carried out, for example, the diving of the clock noise of the RF to wiring for picture signals from wiring for clocks can be reduced.

[0051] With the gestalt of this operation, as shown in drawing 1 and drawing 2 , an image display field and two or more data lines 35 are surrounded on the TFT array substrate 1 by shielding wire 80. For this reason, an image display field and two or more data lines 35 concerned are also shielded from Wiring CLX and CLX'. Therefore, generating of the clock noise of a RF in the sampling circuit driving signal outputted from the data–line actuation circuit 101, the data signal which reached TFT30 and the pixel electrode 11 can be reduced. However, if it constitutes so that the wiring VID1–VID6 until it reaches a sampling circuit 301 may be shielded by shielding wire 80 or 82 even if it does not take the configuration surrounded to an image display field in this way, the effectiveness of shielding will be acquired somewhat.

[0052] It is formed from the various wiring DY connected to the external input terminal 102 which contains shielding wire 80 and 82 in drawing 3 as shown in a sectional view, VSSY, —, the low resistance [with same VDDX] metallic material as the data lines 35, such as aluminum (aluminum). Therefore, even if the leading–about field of shielding wire 80 and 82 is long, resistance of shielding wire 80 and 82 will be suppressed low practically enough. That is, as shown in drawing 2 , the clearance between wave control circuit 101b and buffer circuit 101c is sewn in other various wiring or a shift–register–circuit 101a list, and the large field which could wire zigzag for a long time and included shielding wire 82 in it to the image display field further can be wired for a long time in shielding wire 80. Thus, a comparatively easy configuration can raise the effectiveness of the shielding concerned as a whole. Moreover, as shown in drawing 3 , it is formed the various wiring DY connected to the external input terminal 102 containing shielding wire 80 and 82, VSSY, —, on the insulating layer 42 between the 1st layer by which VDDX was formed in the TFT array substrate 1, i.e., the same layer. Therefore, the effectiveness of shielding is demonstrated more efficiently. Furthermore, if constituted in this way, since the various wiring DY, VSSY, —, VDDX are put in block according to the same process and can be formed in the manufacture process of liquid crystal equipment 200 from a low resistance metal layer for

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example, with same aluminum layer etc., it is advantageous on manufacture.
[0053] In addition, the signal LCCOM inputted from the external input terminal 102 shown in drawing 3 from drawing 1 is a power-source signal of a common electrode, and is supplied to the common electrode (refer to drawing 7) prepared in the below-mentioned opposite substrate through the flow material on Wiring LCCOM and the above-mentioned vertical flow terminal 106.
[0054] As shown in the top view of drawing 4 here, capacity line 31' is formed from the conductive polish recon layer same with the scanning line 31 etc. on the TFT array substrate 1 at the scanning line 31 and parallel, and is connected to shielding wire 80 through contact hole 80a. Thus, if constituted, wiring for making capacity line 31' into constant potential can be made to serve a double purpose with shielding wire 80, and an external input terminal required in order to make capacity line 31' into constant potential can also be made to serve a double purpose with the external input terminal 102 for shielding-wire 80.
[0055] Especially with the gestalt of this operation, the sampling circuit 301 is formed on the TFT array substrate 1 in the location which counters the frame 53 of the protection-from-light nature formed in the opposite substrate 2 as shown in drawing 5 and drawing 6 R> 6, as the slash field in drawing 1 shows, and the data-line actuation circuit 101 and the scanning-line actuation circuit 104 are formed on the narrow long and slender circumference part of the TFT array substrate 1 which does not face the liquid crystal layer 50. On the TFT array substrate 1, the sealant 52 which consists of a photo-setting resin as an example of the seal member which sticks both substrates in the perimeter of an image display field, and surrounds the liquid crystal layer 50 is formed along the image display field. And between the image display fields and sealants 52 on the opposite substrate 2, the frame 53 of protection-from-light nature is formed.
[0056] When put into the TFT array substrate 1 by the case of protection-from-light nature which opening was able to open behind corresponding to the image display field, a frame 53 so that the image display field concerned may not hide in the edge of opening of the case concerned according to a manufacture error etc. That is, it is formed from the band-like protection-from-light nature ingredient which has width of face of 500 micrometers or more in the perimeter of an image display field so that the gap of about hundreds of micrometers to the case of the TFT array substrate 1 may be permitted, for example. The frame 53 of such protection-from-light nature is formed in the opposite substrate 2 of sputtering and the photolithography which used metallic materials, such as Cr (chromium), nickel (nickel), and aluminum (aluminum), and etching. Or it is formed from ingredients, such as resin black which distributed carbon and Ti (titanium) to the photoresist.
[0057] The data-line actuation circuit 101 and the external input terminal 102 are formed in the field of the outside of a sealant 52 along the lower side of an image display field, and the scanning-line actuation circuit 104 is established in the both sides of an image display field along with two sides of right and left of an image display field. And the opposite substrate 2 with the almost same profile as a sealant 52 has fixed to the TFT array substrate 1 by the sealant 52 concerned.
[0058] As mentioned above shielding wire 80 and a sampling circuit 301 If the case of opposite arrangement, i.e., this operation gestalt, is prepared in the bottom of a frame 53 at the frame 53 on the TFT array substrate 1 Space-saving-ization on the TFT array substrate 1 is attained, for example, the scanning-line actuation circuit 104 and the data-line actuation circuit 101 can be formed in the circumference part of the TFT array substrate 1 with allowances. the display area in liquid crystal equipment 200 also decreases by formation of shielding wire 80 -- most -- or there is completely nothing. Moreover, shielding wire 80 can use a tooth space effectively, without decreasing the display area on a TFT substrate, if shielding wire 80 and capacity line 31' are connected in the location which counters while being installed in the location which counters a frame 53.
[0059] (Configuration of the whole liquid crystal equipment) Next, the concrete configuration of liquid crystal equipment 200 is explained with reference to drawing 7 and drawing 8 . It is the sectional view where it is the sectional view which drawing 7 shows TFT30 part of liquid crystal equipment, and met at

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B-B' in drawing 4 , and drawing 8 met the shielding wire 80 of the liquid crystal equipment under a frame here. In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, contraction scales are made to have differed for each class or every each part material in drawing 7 and drawing 8 .

[0060] In the sectional view of drawing 7 , liquid crystal equipment 200 is equipped with an insulating layer 43, the pixel electrode 11, and the orientation film 12 between an insulating layer 42, the data line 35, and the 2nd layer in TFT30 part prepared in each pixel between the semi-conductor layer 32 by which the laminating was carried out to the TFT array substrate 1 list on it, the gate insulating layer 33, the scanning line 31 (gate electrode), and the 1st layer. Liquid crystal equipment 200 is equipped with the common electrode 21, the orientation film 22, and light-shielding film 23 by which the laminating was carried out to the opposite substrate 2 list which consists of a glass substrate on it again. Liquid crystal equipment 200 is further equipped with the liquid crystal layer 50 as electrooptic material pinched among both these substrates.

[0061] Here, the configuration of each class except TFT30 is first explained in order among these layers.

[0062] Insulating layers 42 and 43 consist of silicate glass film, such as NSG (non silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), a silicon nitride film, silicon oxide film, etc. with about 5000-15000A **** between the 1st and the 2nd layer, respectively. In addition, the layer insulation layer used as the substrate of TFT30 may be formed from the silicate glass film, a silicon nitride film, the silicon oxide film, etc. on the TFT array substrate 1.

[0063] The pixel electrode 11 consists of transparent conductive thin films, such as for example, ITO (indium Tin oxide) film. Such a pixel electrode 11 is formed by giving a photolithography process and an etching process etc., after depositing the ITO film etc. on the thickness of about 500-2000A by sputtering processing etc. In addition, when using the liquid crystal equipment 200 concerned for the liquid crystal equipment of a reflective mold, the pixel electrode 11 may be formed from an opaque ingredient with high reflection factors, such as aluminum.

[0064] The orientation film 12 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 12 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.

[0065] It goes across the common electrode 21 all over the opposite substrate 2, and it is formed. Such a common electrode 21 is formed by giving a photolithography process and an etching process etc., after depositing the ITO film etc. on the thickness of about 500-2000A for example, by sputtering processing etc.

[0066] The orientation film 22 consists of organic thin films, such as for example, a polyimide thin film. Such orientation film 22 is formed by performing rubbing processing in the predetermined direction so that it may have a predetermined pre tilt angle etc., after applying the coating liquid of for example, a polyimide system.

[0067] The light-shielding film 23 is formed in the predetermined field which counters TFT30. Like the above-mentioned frame 53, such a light-shielding film 23 is formed of sputtering and the photolithography using metallic materials, such as Cr and nickel, and etching, or is formed from ingredients, such as resin black which distributed carbon and Ti to the photoresist. A light-shielding film 23 has functions other than the protection from light to the semi-conductor layer 32 of TFT30, such as improvement in contrast, and color mixture prevention of color material.

[0068] The liquid crystal layer 50 is formed when liquid crystal is enclosed with the space surrounded by the sealant 52 (drawing 5 and R> drawing 6 6 reference) between the TFT array substrates 1 and the opposite substrates 2 which have been arranged so that the pixel electrode 11 and the common electrode 21 may meet by vacuum attraction etc. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 12 and 22 in the condition that the electric field from the pixel electrode 11 are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed

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the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant 52 may stick two substrates 1 and 2 around those, and the spacer for making distance between both substrates into a predetermined value is mixed.

[0069] Next, the configuration of each class concerning TFT30 is explained in order.

[0070] TFT30 is equipped with the source field 34 formed in the gate insulating layer 33 which insulates the semi-conductor layer 32 in which a channel is formed of the electric field from the scanning line 31 and the scanning line 31, and the scanning line 31 and the semi-conductor layer 32, and the semi-conductor layer 32, the data line 35, and the drain field 36 formed in the semi-conductor layer 32. One to which it corresponds of two or more pixel electrodes 11 is connected to the drain field 36. The source field 34 and the drain field 36 are formed by doping the dopant the object for n molds of predetermined concentration, or for p molds to the semi-conductor layer 32 like the after-mentioned according to whether the channel of n mold or p mold is formed. TFT of an n-type channel has the advantage that working speed is quick, and it is used as TFT30 which is the switching element of a pixel in many cases.

[0071] The semi-conductor layer 32 which constitutes TFT30 is formed by performing annealing treatment and making the thickness of about 500-2000A carry out solid phase growth after forming the a-Si (amorphous silicon) film for example, on the TFT array substrate 1. Under the present circumstances, in the case of TFT30 of an n channel mold, you may dope by the ion implantation which used the dopant of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn). Moreover, in the case of TFT30 of a p channel mold, it dopes by the ion implantation which used the dopant of III group elements, such as B (boron), Ga (gallium), and In (indium). When setting especially TFT30 to TFT of an n channel mold with LDD (Lightly DopedDrain) structure, among the source field 34 and the drain field 36, a low concentration dope field is formed in the part which adjoins at a channel side, respectively by the dopant of V group elements, such as P, and, similarly a high concentration dope field is formed in the semi-conductor layer 32 of p mold by the dopant of V group elements, such as P. Moreover, when referred to as TFT30 of a p channel mold, the dopant of III group elements, such as B, is used for the semi-conductor layer 32 of n mold, and the source field 34 and the drain field 36 are formed. Thus, when it considers as LDD structure, the advantage which can reduce the short channel effect is acquired. In addition, TFT30 is good for the low concentration dope field in LDD structure also as TFT of the offset structure which carried out the ion implantation, and good also as TFT of the self aryne mold which forms the source [high concentration / in self align], and a drain field by doping high-concentration impurity ion by using a gate electrode as a mask. Moreover, a gate electrode is prepared in a two-piece serial, it is good also as dual gate structure, and it cannot be overemphasized that a gate electrode may be prepared in a three or more piece serial. If such a configuration is taken, since the leakage current at the time of OFF of TFT30 is reduced and generating of a cross talk etc. can be controlled, high-definition liquid crystal equipment can be offered.

[0072] The gate insulating layer 33 can form and obtain the thermal oxidation film with a comparatively thin thickness of about 300-1500A by oxidizing the semi-conductor layer 32 thermally with the temperature of about 900-1300 degrees C. The good insulator layer which was excellent in the interface condition of the semi-conductor layer 32 and the gate insulating layer 33 by this can be formed.

[0073] After the scanning line 31 deposits the polish recon film with a reduced pressure CVD method etc., it is formed of a photolithography process, an etching process, etc. Or it may be formed from a metal membrane or metal silicide film, such as aluminum. in this case, it also becomes possible to omit a part or all of a light-shielding film 23 by the protection-from-light nature which the metal membrane metallurgy group silicide film has if a light-shielding film 23 arranges the scanning line 31 as the part or the light-shielding film which boils all and corresponds of a wrap field. In this case, there is an advantage which can prevent decline in the pixel numerical aperture by the lamination gap with the opposite substrate 2 and the TFT array substrate 1 especially.

[0074] The data line 35 may be formed from transparent conductive thin films, such as ITO film, like the

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pixel electrode 11. Or you may form by sputtering processing etc. from low resistance metal metallurgy group silicide, such as aluminum deposited on the thickness of about 1000-5000A, etc.
[0075] Moreover, the contact hole 38 which leads to the contact hole 37 and the drain field 36 which lead to the source field 34 is formed in the insulating layer 42 between the 1st layer, respectively. Electrical installation of the data line 35 is carried out to the source field 34 through the contact hole 37 to this source field 34. Furthermore, the contact hole 38 to the drain field 36 is formed in the insulating layer 43 between the 2nd layer. Electrical installation of the pixel electrode 11 is carried out to the drain field 36 through the contact hole 38 to this drain field 36. The above-mentioned pixel electrode 11 is formed in the top face of an insulating layer 43 between the 2nd layer constituted in this way. If each contact hole is formed by dry etching, such as for example, reactant etching and reactant ion beam etching, detailed-ization of opening size of it is attained, and it can realize high numerical aperture-ization of a pixel.
[0076] In addition, if light carries out incidence of the semi-conductor layer 32 in which a channel is generally formed, a photocurrent will occur according to the photo-electric-translation effectiveness which p-Si has, the transistor characteristics of TFT30 will deteriorate, but with the gestalt of this operation, since the light-shielding film 23 is formed in the location which counters the opposite substrate 2 at each TFT30, respectively, it is prevented that incident light carries out incidence to the semi-conductor layer 32. furthermore, this -- adding -- or -- replacing with -- a gate electrode -- the wrap from an upside -- if the data line 35 is formed from opaque metal thin films, such as aluminum, like -- a light-shielding film 23 -- or the incidence of the incident light (namely, drawing 7 </A> light from an upside) to the semi-conductor layer 32 can be prevented effectively independently.
[0077] In drawing 7 , storage capacitance 70 is formed in the pixel electrode 11, respectively. 1st storage capacitance electrode 32' more specifically [this storage capacitance 70] formed of the same process as the semi-conductor layer 32, dielectric layer 33' formed of the same process as the gate insulating layer 33, and the capacity line 31 formed of the same process as the scanning line 31 -- ' (the 2nd storage capacitance electrode) -- It consists of some of insulating layers 42 and 43 and pixel electrodes 11 which counter a list at capacity line 31' through the 1st and the insulating layers 42 and 43 between the 2nd layer between the 1st and the 2nd layer. Thus, since storage capacitance 70 is formed, even if duty ratio is small, a high definition display is enabled.
[0078] As shown in the sectional view of drawing 8 , a frame 53 is countered and shielding wire 80 passes through an insulating-layer 42 top between the 1st layer in the upper location of two or more scanning lines 31. and low [which consists of metal thin films, such as aluminum formed at the process as the data line 35 mentioned above that almost all those parts of this shielding wire 80 are the same,] -- it is wiring [****]. Thus, in the manufacture process of liquid crystal equipment 200, since shielding wire 80 and the data line 35 can be formed collectively, it is advantageous on manufacture.
[0079] Since it is the same film formation process and a sampling circuit 301, the data-line actuation circuit 101, and the circumference circuit of scanning-line actuation circuit 104 grade can be formed especially with the gestalt of this operation at the time of formation of TFT30, it is advantageous on manufacture. For example, these circumference circuits are formed in the circumference part on the TFT array substrate 1 from two or more TFT(s) of the complementary-type structure which consists of n channel mold poly-Si TFT and p channel mold poly-Si TFT.
[0080] In addition, although not shown in drawing 7 and drawing 8 , it sets to liquid crystal equipment 200. To the side in which the incident light of the side in which the incident light of the opposite substrate 2 carries out incidence, and the TFT array substrate 1 carries out outgoing radiation, respectively For example, TN (Twisted Nematic) mode and STN (super TN) mode, According to the exception of modes of operation, such as D-STN (double-STN) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, a polarizing plate, etc. are arranged in a predetermined direction.
[0081] Moreover, since the liquid crystal equipment 200 explained above is applied to an

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electrochromatic display projector, three liquid crystal equipments 200 will be used as a light valve for RGB, respectively, and incidence of the light of each color decomposed through the dichroic mirror for RGB color separation, respectively will be carried out to each equipment as incident light, respectively. Therefore, with the gestalt of each operation, the light filter is not prepared in the opposite substrate 2. However, the light filter of RGB may be formed in the predetermined field which counters the pixel electrode 11 with which a light-shielding film 23 is not formed in liquid crystal equipment 200 on the opposite substrate 2 with the protective coat. Or a light filter layer may be built in by the color resist of RGB so that it may correspond to each pixel on the TFT array substrate 1. If it does in this way, the liquid crystal equipment of the gestalt of this operation is applicable to electrochromatic display equipments, such as electrochromatic display television of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 2. If it does in this way, bright liquid crystal equipment is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 2 again may be formed. According to this opposite substrate with a die clo IKKU filter, brighter electrochromatic display equipment is realizable.

[0082] In order to set to liquid crystal equipment 200 and to control the poor orientation of the liquid crystal molecule by the side of the TFT array substrate 1, the flattening film may be further applied on a spin coat etc. on an insulating layer 43 between the 2nd layer, or CMP (Chemical Mechanical Polishing) processing may be performed. Or an insulating layer 43 may be formed by the flattening film between the 2nd layer.

[0083] Although it was explained that the switching element of liquid crystal equipment 200 was the poly-Si TFT of a forward stagger mold or a coplanar mold, the gestalt of this operation is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0084] In liquid crystal equipment 200, although the liquid crystal layer 50 was constituted from a pneumatic liquid crystal as an example, if the polymer dispersed liquid crystal which distributed liquid crystal as a minute grain in the macromolecule is used, the above-mentioned polarization film, a polarizing plate, etc. will become unnecessary in the orientation film 12 and 22 and a list, and the advantage of a raise in the brightness of liquid crystal equipment or low-power-izing by efficiency for light utilization increasing will be acquired. Furthermore, when applying liquid crystal equipment 200 to high-reflective-liquid-crystal equipment by constituting the pixel electrode 11 from a metal membrane with high reflection factors, such as aluminum, SH (super HOMEOTORO pick) mold liquid crystal with which vertical orientation of the liquid crystal molecule was mostly carried out in the state of no electrical-potential-difference impressing may be used. Furthermore, although the common electrode 21 is provided in the opposite substrate 2 side in liquid crystal equipment 200 again so that vertical electric field (vertical electric field) may be impressed to the liquid crystal layer 50 What (that is, the electrode for horizontal electric-field generating is prepared in the TFT array substrate 1 side, without preparing the electrode for vertical electric-field generating in the opposite substrate 2 side) the pixel electrode 11 is constituted also for from an electrode for horizontal electric-field generating of a couple, respectively so that electric field (horizontal electric field) parallel to the liquid crystal layer 50 may be impressed is possible. Thus, if horizontal electric field are used, it is advantageous when extending an angle of visibility rather than the case where vertical electric field are used. In addition, it is possible to apply the gestalt of this operation to various kinds of liquid crystal ingredients (liquid crystal phase), a mode of operation, a liquid crystal array, the actuation approach, etc. Moreover, with an above-mentioned operation gestalt, although explained using the configuration which forms TFT on a substrate, the configuration which forms a switching element is also applicable not only to such a configuration but a silicon substrate. Moreover, although explained using liquid crystal as electrooptic material, it is applicable not only to liquid crystal but electroluminescence or a plasma display etc.

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[0085] In the gestalt of the operation explained above, well-known circumference circuits, such as a precharge circuit and an inspection circuit, may be further established in the periphery of the bottom of a frame 53, or the TFT array substrate 1. A precharge circuit is the timing preceded with the data signal supplied from the data-line actuation circuit 101 to the data line 35 for the purpose of reduction of improvement in a contrast ratio, the stability of the potential level of the data line 35, and the line unevenness on a display screen etc., and is a circuit which mitigates the load at the time of writing a data signal in the data line 35 by supplying a precharge signal. For example, an example of such a precharge circuit is indicated by JP,7-295520,A. On the other hand, an inspection circuit is a circuit for inspecting the quality of the liquid crystal equipment concerned at the manufacture middle or the time of shipment, a defect, etc. to the periphery of the bottom of a frame 53, or a TFT array substrate.
[0086] Moreover, in the gestalt of the above operation, the protection-from-light layer which consists of a refractory metal may be prepared also in the location (namely, under TFT30) which counters on the TFT array substrate 1 at TFT30 as indicated by JP,9-127497,A, JP,3-52611,B, JP,3-125123,A, JP,8-171101,A, etc. Thus, if a protection-from-light layer is prepared also in the TFT30 bottom, it can prevent that the return light from the TFT array substrate 1 side etc. carries out incidence to TFT30. Therefore, the liquid crystal equipment 200 concerned can be suitably used as a light valve for projectors.
[0087] Furthermore, in the gestalt of the above operation, it may replace with TFT30 and a switching element may consist of 2 terminal mold nonlinear elements, such as TFD (Thin Film Diode), etc. again. In this case, arrange one line to an opposite substrate among the data line and the scanning line, and it is made to function as a common electrode, and a switching element is arranged, respectively between the line of another side established in the TFT array substrate, and a pixel electrode, and liquid crystal actuation is carried out between. Thus, even if constituted, the effectiveness of preventing the diving to the picture signal and data signal of a clock noise of high frequency is demonstrated by shielding a pixel signal line and the data line from a clock signal line.
[0088] (Actuation of liquid crystal equipment) Next, actuation of the liquid crystal equipment 200 constituted as mentioned above is explained with reference to drawing 1 .
[0089] First, the scanning-line actuation circuit 104 impresses a scan signal to the scanning line 31 by line sequential in pulse to predetermined timing.
[0090] If a parallel picture signal is received from six wiring VID1-VID6 in parallel to this, a sampling circuit 301 will sample these picture signals. The scanning-line actuation circuit 104 supplies a sampling circuit driving signal for every data line about six wiring VID1 - VID6 each according to the timing which impresses gate voltage, and the data-line actuation circuit 101 makes TFT302 of a sampling circuit 301 an ON state. Thereby, sequential impression of the data signal sampled by the sampling circuit 301 is carried out to the six adjoining data lines 35. That is, the parallel picture signals VID1-VID6 by which serial-parallel conversion was carried out are supplied to six phases inputted from wiring VID1-VID6 by the data-line actuation circuit 101 and the sampling circuit 301 at the data line 35.
[0091] Thus, in TFT30 to which both the scan signal (gate voltage) and the data signal (source electrical potential difference) were impressed, an electrical potential difference is impressed to the pixel electrode 11 through the channel and the drain field 36 which were formed in the source field 34 and the semi-conductor layer 32. And as for the electrical potential difference of this pixel electrode 11, only time amount also with triple figures longer than the time amount to which the source electrical potential difference was impressed is held with storage capacitance (refer to drawing 7). With shielding wire 80 and 82, since especially the wiring VID1-VID6 is shielded from Wiring CLX and CLX', even when the frequency of a clock signal CLX is high, it can reduce the diving of the clock noise of the RF to Wiring CLX and the wiring VID1-VID6 from CLX' here.
[0092] As mentioned above, if an electrical potential difference is impressed to the pixel electrode 11, the orientation condition of the liquid crystal in the part pinched by this pixel electrode 11 and common electrode 21 in the liquid crystal layer 50 changes, and if it is in no MARI White mode According to the

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impressed electrical potential difference, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from liquid crystal equipment 200 as a whole.
[0093] image quality deteriorates according to generating of the clock noise of a RF, using [the resolution of the image which should be displayed is high the above result, and] the clock signal CLX with a high frequency, and CLX' corresponding to this, also when the serial picture signals VID1-VID6 of a RF are inputted -- most -- or it is completely lost and high-definition image display is made possible.
[0094] (Electronic equipment) Next, the gestalt of operation of electronic equipment equipped with the liquid crystal equipment 200 explained to the detail above is explained with reference to drawing 13 from drawing 9 R> 9.
[0095] The outline configuration of the electronic equipment which equipped drawing 9 with liquid crystal equipment 200 in this way is shown first.
[0096] In drawing 9 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the actuation circuit 1004, liquid crystal equipment 200, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a TV signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial-parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the actuation circuit 1004 with a clock signal CLK. The actuation circuit 1004 drives liquid crystal equipment 200. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes liquid crystal equipment 200, the actuation circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.
[0097] Next, the example of the electronic equipment constituted in this way from drawing 10 by drawing 13 is shown, respectively.
[0098] In drawing 10 , an example slack liquid crystal projector 1100 of electronic equipment prepares three liquid crystal modules containing the liquid crystal equipment 200 with which the actuation circuit 1004 mentioned above was carried on the TFT array substrate, and is constituted as a projector used as light valves 200R, 200G, and 200B for RGB, respectively. In a liquid crystal projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be led to the light valves 200R, 200G, and 200B corresponding to each color, respectively. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors modulated with light valves 200R, 200G, and 200B, respectively is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.
[0099] If the protection-from-light layer is especially prepared also in the TFT bottom as mentioned above in the gestalt of this operation The reflected light by the incident light study system in the liquid crystal projector based on the incident light from the liquid crystal equipment 200 concerned, A part of incident light (a part of R light and G light) which runs through a dichroic prism 1112 after carrying out

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outgoing radiation from the reflected light from the front face of the TFT array substrate at the time of incident light passing and other liquid crystal equipments Even if it carries out incidence from a TFT array substrate side as a return light, protection from light to the channel of the TFT30 grade for pixel switching can fully be performed. In this case, in a configuration, since it becomes unnecessary to stick AR (Anti Reflection) film for return light prevention, or to perform AR coat processing between the TFT array substrate of each liquid crystal equipment and prism at a polarizing plate even if it uses the prism suitable for a miniaturization for an incident light study system, small and when being simplified, it is very advantageous.

[0100] In drawing 11 , other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while it has liquid crystal equipment 200 mentioned above in the top covering case and they hold CPU, memory, a modem, etc. further.

[0101] In drawing 12 , the actuation circuit 1004 of the above-mentioned [other example slack pagers 1300 of electronic equipment] in the metal frame 1302 is held in the light guide [in which the liquid crystal equipment 200 which is carried at a TFT array substrate top and forms a liquid crystal module contains back light 1306a] 1306, circuit board 1308, 1st, and 2nd shielding plates 1310 and 1312 or 2 elastic conductors 1314 and 1316, and a list with the tape carrier package tape 1318. In the case of this example, the above-mentioned display information processing circuit 1002 (refer to drawing 9) may be carried in the circuit board 1308, and may be carried on the TFT array substrate of liquid crystal equipment 200. Furthermore, it is also possible to carry the above-mentioned actuation circuit 1004 on the circuit board 1308.

[0102] In addition, since the example shown in drawing 12 is a pager, the circuit board 1308 grade is prepared. However, it is also possible to carry out production, a sale, an activity, etc. as back light-type liquid crystal equipment which incorporated [in the case of the actuation circuit 1004 or the liquid crystal equipment 200 which carries the display information processing circuit 1002 further, and forms a liquid crystal module] the light guide 1306 by using as liquid crystal equipment what fixed liquid crystal equipment 200 in the metal frame 1302 in addition to this.

[0103] moreover, as shown in drawing 13 , in the case of the liquid crystal equipment 200 which carries neither the actuation circuit 1004 nor the display information processing circuit 1002 To TCP (Tape Carrier Package)1320 mounted on the polyimide tape 1322, IC1324 including the actuation circuit 1004 or the display information processing circuit 1002 It is also possible to connect physically and electrically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 1, and to carry out production, a sale, an activity, etc. as liquid crystal equipment.

[0104] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 13 from drawing 10 above etc. is mentioned as an example of the electronic equipment shown in drawing 9 .

[0105] As explained above, according to the gestalt of this operation, generating of the clock noise of a RF is reduced and various kinds of electronic equipment equipped with the liquid crystal equipment 200 in which high-definition image display is possible can be realized.

[0106]

[Effect of the Invention] According to the electro-optic device according to claim 1, by the electric conduction line of the constant potential wired by the 1st substrate, since the picture signal line is shielded from the clock signal line, high-definition image display can be performed according to the picture signal of the high frequency for being able to reduce the diving of the clock noise of the RF from a clock signal line to a picture signal line, therefore displaying the image of high resolution.

[0107] Since simplification and space-saving-izing of a configuration can be attained by sharing the wiring itself and the external input terminal of an electric conduction line and a constant potential line

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according to the electro-optic device according to claim 2, the electro-optic device which can perform high-definition image display by the comparatively simple configuration is realizable.
[0108] the configuration which shields a picture signal line from a clock signal line to a duplex according to the electro-optic device according to claim 3 -- generating of the clock noise of the RF in a picture signal or a data signal -- more -- powerful -- and dependability -- it can decrease highly.
[0109] Since the diving of the clock noise of the RF to a picture signal line can be further reduced by taking about a picture signal line and a clock signal line to the reverse sense to a data-line actuation circuit according to the electro-optic device according to claim 4, the device on an easy configuration can raise the effectiveness of shielding efficiently.
[0110] Since the diving of the clock noise of the RF to a picture signal line can be reduced by separating predetermined spacing mutually and arranging the 1st and 2nd external input terminal mutually through the 3rd external input terminal in between according to the electro-optic device according to claim 5, the device on an easy configuration can raise the effectiveness of shielding efficiently.
[0111] According to the electro-optic device according to claim 6, since an image display field and two or more data lines can be shielded from a clock signal line, generating of the clock noise of a RF in the data signal on the data line etc. can be reduced, and more nearly high-definition image display becomes possible.
[0112] According to the electro-optic device according to claim 7, since the electric conduction line is formed in the bottom of the frame of a substrate, a deployment of the tooth space on a substrate can be aimed at.
[0113] According to the electro-optic device given in claims 8 and 9, according to a comparatively simple production process, the high electric conduction line of a shielding effect can be formed, and the electro-optic device in which image display high-definition by low cost is possible can be realized.
[0114] Since the constant potential line and external input terminal for making a capacity line into constant potential can be made to serve a double purpose with other wiring or a terminal according to the electro-optic device according to claim 10, preventing the adverse effect to the switching element and pixel electrode by potential fluctuation of a capacity line, high-definition image display becomes possible by the comparatively simple configuration.
[0115] According to electronic equipment according to claim 11, the clock noise of high frequency is reduced and it becomes realizable about various electronic equipment, such as the liquid crystal projector and personal computer in which high-definition image display is possible, and a pager.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] They are outline top views formed on the TFT array substrate in the gestalt of operation of

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liquid crystal equipment, such as various wiring and a circumference circuit.
[Drawing 2] It is the outline top view showing the two-dimensional layout of drawing 1 in a detail more.
[Drawing 3] It is the sectional view which met the A-A' line on the TFT array substrate of drawing 1 .
[Drawing 4] It is an amplification top view in image display field edges, such as a pixel electrode formed on the TFT array substrate of drawing 1 , the scanning line, and data.
[Drawing 5] It is the top view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 6] It is the sectional view showing the whole liquid crystal equipment configuration of drawing 1 .
[Drawing 7] It is the sectional view of TFT for pixel switching established in the image display field of the liquid crystal equipment of drawing 1 .
[Drawing 8] It is a sectional view in the shielding-wire part prepared in the frame field of the liquid crystal equipment of drawing 1 .
[Drawing 9] It is the block diagram showing the outline configuration of the gestalt of operation of the electronic equipment by this invention.
[Drawing 10] It is the sectional view showing the liquid crystal projector as an example of electronic equipment.
[Drawing 11] It is the front view showing the personal computer as other examples of electronic equipment.
[Drawing 12] It is the decomposition perspective view showing the pager as an example of electronic equipment.
[Drawing 13] It is the perspective view showing the liquid crystal equipment using TCP as an example of electronic equipment.
[Description of Notations]
1 -- TFT array substrate
2 -- Opposite substrate
11 -- Pixel electrode
12 -- Orientation film
21 -- Common electrode
22 -- Orientation film
23 -- Light-shielding film
30 -- TFT
31 -- Scanning line (gate electrode)
32 -- Semi-conductor layer
33 -- Gate insulating layer
34 -- Source field
35 -- Data line
36 -- Drain field
37 38 -- Contact hole
42 -- Insulating layer between the 1st layer
43 -- Insulating layer between the 2nd layer
50 -- Liquid crystal layer
52 -- Sealant
53 -- Frame
70 -- Storage capacitance
80 82 -- Shielding wire (constant potential line)
101 -- Data-line actuation circuit
102 -- External input terminal
104 -- Scanning-line actuation circuit
200 -- Liquid crystal equipment

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301 -- Sampling circuit
302 -- TFT

[Translation done.]

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CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
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[Procedure amendment 1]
[Document to be Amended] Description
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[The content of amendment]
[Claim(s)]
[Claim 1]
The electro-optic device characterized by providing the following. Two or more scanning lines [top / substrate] Two or more data lines which intersect said two or more scanning lines Two or more switching elements prepared corresponding to the crossover of two or more of said scanning lines and

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data lines Two or more pixel electrodes prepared corresponding to said two or more switching elements, A data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, The clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line

[Claim 2]

Said electric conduction line is an electro-optic device according to claim 1 characterized by including the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means.

[Claim 3]

said law -- a potential line -- difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming

this -- a part for said electric conduction line part which consisted of potential lines the 1st law -- said substrate top -- said picture signal line -- surrounding

A part for said said electric conduction line part which consisted of potential lines the 2nd law is an electro-optic device according to claim 2 characterized by surrounding said clock signal line on said substrate.

[Claim 4]

Said data signal supply means is an electro-optic device according to claim 2 or 3 which is equipped with the sampling circuit which samples said picture signal, and the data-line actuation circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line, and is characterized by taking about said picture signal line and said clock signal line from an opposite direction to said data-line actuation circuit on said substrate.

[Claim 5]

said 1st and 2nd external input terminal separates and arranges predetermined spacing mutually in the periphery of said substrate -- having -- **** -- between said 1st and 2nd external input terminals -- said law -- the power source of potential -- said law -- an electro-optic device given in any 1 term of claims 2-4 characterized by arranging the 3rd external input terminal for inputting into a potential line.

[Claim 6]

Said electric conduction line is an electro-optic device given in any 1 term of claims 1-5 by which it is installing [so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes might be surrounded on said 1st substrate] characterized.

[Claim 7]

Said substrate was countered, the opposite substrate was formed and it has further the frame of the protection-from-light nature formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field,

Said electric conduction line is an electro-optic device according to claim 6 characterized by including the part prepared in said substrate along with said frame in the location which counters said frame.

[Claim 8]

Said electric conduction line and said data line are an electro-optic device given in any 1 term of claims 1-7 characterized by being formed from the same low resistance metallic material.

[Claim 9]

It is an electro-optic device given in any 1 term of claims 1-8 characterized by consisting of same low resistance metal layers formed by said electric conduction line part part list which intervenes between said picture signal line and a clock signal line on the same flat surface where said picture signal line and a clock signal line are parallel to said substrate.

[Claim 10]

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An electro-optic device given in any 1 term of claims 1-9 characterized by equipping said pixel electrode with the capacity line which gives the capacity of the specified quantity further, and connecting this capacity line to said electric conduction line.
[Claim 11]
The frame of the protection-from-light nature which said substrate was countered, and the opposite substrate was formed and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, It is an electro-optic device given in any 1 term of claims 1-6 which equip said pixel electrode with the capacity line which gives capacity further, and are characterized by connecting said capacity line to said electric conduction line in said location which counters while said electric conduction line is installed in the location which counters said frame.
[Claim 12]
Said constant potential wiring is an electro-optic device according to claim 1 characterized by surrounding said picture signal line.
[Claim 13]
Said constant potential wiring is an electro-optic device according to claim 1 or 12 characterized by surrounding said clock signal line.
[Claim 14]
Said data signal supply means is equipped with a shift register circuit, the wave control circuit which shapes the transfer signal from said shift register circuit in waveform, and the buffer circuit for buffering a signal from said wave control circuit,
Said constant potential wiring is an electro-optic device given in claim 1 characterized by surrounding said wave control circuit and said buffer circuit, claim 12, and ** any 1 term of claim 13.
[Claim 15]
Electronic equipment characterized by equipping claims 1-14 with the electro-optic device of a publication.
[Procedure amendment 2]
[Document to be Amended] Description
[Item(s) to be Amended] 0008
[Method of Amendment] Modification
[The content of amendment]
[0008]
[Means for Solving the Problem]
Two or more scanning lines [top / substrate] in order that the electro-optic device of this invention may solve the above-mentioned technical problem, Two or more data lines which intersect said two or more scanning lines, and two or more switching elements prepared corresponding to the crossover of two or more of said scanning lines and data lines, Two or more pixel electrodes prepared corresponding to said two or more switching elements, A data signal supply means to supply the data signal corresponding to a picture signal to said two or more data lines based on a clock signal, The picture signal line which supplies said picture signal inputted from the 1st external input terminal to said data signal supply means, It is characterized by having the clock signal line which supplies said clock signal inputted from the 2nd external input terminal to said data signal supply means, and the electric conduction line of the constant potential which shields said picture signal line electrically from said clock signal line.
[Procedure amendment 3]
[Document to be Amended] Description
[Item(s) to be Amended] 0009
[Method of Amendment] Modification
[The content of amendment]
[0009]

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According to this electro-optic device, the picture signal inputted from the 1st external input terminal is supplied to a data signal supply means through the picture signal line wired by the substrate. In parallel to this, the clock signal inputted from the 2nd external input terminal is supplied to a data signal supply means through the clock signal line wired by the substrate. Then, based on a clock signal, the data signal corresponding to a picture signal is supplied to two or more data lines by the data signal supply means which was formed in the substrate, for example, is constituted including a data-line actuation circuit, a sampling circuit, etc. The picture signal line is electrically shielded from the clock signal line by the electric conduction line of the constant potential wired by the substrate especially here. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.

[Procedure amendment 4]
[Document to be Amended] Description
[Item(s) to be Amended] 0011
[Method of Amendment] Modification
[The content of amendment]
[0011]
Moreover, said electric conduction line of the electro-optic device of this invention is good to include the part which consisted of constant potential lines which supply the power source of constant potential to said data signal supply means.

[Procedure amendment 5]
[Document to be Amended] Description
[Item(s) to be Amended] 0012
[Method of Amendment] Modification
[The content of amendment]
[0012]
Since the part which consisted of constant potential lines by which an electric conduction line supplies the power source of constant potential to said data signal supply means according to this electro-optic device is included, in other words, it also becomes very easy by sharing an external input terminal and the wiring itself to be able to attain simplification and space-saving-izing of a configuration, especially to make an electric conduction line into constant potential by installing a constant potential line and considering as an electric conduction line.

[Procedure amendment 6]
[Document to be Amended] Description
[Item(s) to be Amended] 0013
[Method of Amendment] Modification
[The content of amendment]
[0013]
moreover, said law of the electro-optic device of this invention -- a potential line -- difference -- the 1st and 2nd laws which supply the power source of constant potential to said data signal supply means -- from a potential line -- becoming -- this -- the amount of [which consisted of potential lines the 1st law] said electric conduction line part surrounds said picture signal line on said substrate, and a part for said said electric conduction line part which consisted of potential lines the 2nd law is good to surround said clock signal line on said substrate.

[Procedure amendment 7]
[Document to be Amended] Description
[Item(s) to be Amended] 0014
[Method of Amendment] Modification
[The content of amendment]
[0014]

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According to this electro-optic device, the picture signal line is surrounded by the amount of [by which potential lines were consisted of the 1st law in order to supply the negative supply of for example, touch-down potential] electric conduction line part on the substrate. The clock signal line is surrounded by the amount of [by which potential lines were consisted of the 2nd law in order to supply a positive supply] electric conduction line part on the substrate. Therefore, the configuration from which the picture signal line was shielded [line / clock signal] by the duplex on the substrate is obtained.
[Procedure amendment 8]
[Document to be Amended] Description
[Item(s) to be Amended] 0015
[Method of Amendment] Modification
[The content of amendment]
[0015]
Moreover, said data signal supply means of the electro-optic device of this invention is equipped with the sampling circuit which samples said picture signal, and the data-line actuation circuit which drives this sampling circuit based on said clock signal in response to the current supply from said constant potential line, and those of taking about from the opposite direction to said data-line actuation circuit on said substrate is [said picture signal line and said clock signal line] good.
[Procedure amendment 9]
[Document to be Amended] Description
[Item(s) to be Amended] 0016
[Method of Amendment] Modification
[The content of amendment]
[0016]
According to this electro-optic device, a picture signal is sampled by the sampling circuit in a scan signal supply means. And the picture signal with which the sampling circuit drove and was sampled by the data-line actuation circuit which receives the current supply from a constant potential line based on the clock signal is supplied to the data line as a data signal. Especially, although the picture signal line and the clock signal line are taken about from the opposite direction to the data-line actuation circuit on the substrate, since an electromagnetic wave generally decreases according to inclusion of distance and an obstruction, the electromagnetic wave impressed to a picture signal line decreases here according to existence of a data-line actuation circuit from a clock signal line, corresponding to the distance between both signal lines. Therefore, even when the frequency of a clock signal is high, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced further.
[Procedure amendment 10]
[Document to be Amended] Description
[Item(s) to be Amended] 0017
[Method of Amendment] Modification
[The content of amendment]
[0017]
Moreover, in the periphery of said substrate, said 1st and 2nd external input terminal of the electro-optic device of this invention separates predetermined spacing mutually, is arranged, and is good between said 1st and 2nd external input terminals to arrange the 3rd external input terminal for inputting the power source of said constant potential into said constant potential line.
[Procedure amendment 11]
[Document to be Amended] Description
[Item(s) to be Amended] 0018
[Method of Amendment] Modification
[The content of amendment]
[0018]

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According to this electro-optic device, in between, the 1st and 2nd external input terminal separates predetermined spacing mutually, is arranged in the periphery of a substrate, through the 3rd external input terminal, mutually, and is preferably detached and arranged as much as possible mutually in the field which can form an external input terminal in the periphery of a substrate. As compared with the case where followed, for example, contiguity arrangement of a picture signal line and the clock signal line is carried out, the diving of the clock noise of the RF from a clock signal line to a picture signal line can be reduced.

[Procedure amendment 12]
[Document to be Amended] Description
[Item(s) to be Amended] 0019
[Method of Amendment] Modification
[The content of amendment]
[0019]
Moreover, said electric conduction line of the electro-optic device of this invention is good to be installed so that the image display field and said two or more data lines which are specified with said two or more pixel electrodes may be surrounded on said substrate.

[Procedure amendment 13]
[Document to be Amended] Description
[Item(s) to be Amended] 0020
[Method of Amendment] Modification
[The content of amendment]
[0020]
According to this electro-optic device, by the electric conduction line, since an image display field and two or more data lines are surrounded on the substrate, an image display field and two or more data lines concerned will also be shielded from a clock signal line. Therefore, generating of the clock noise of a RF in the data signal outputted from the data signal supply means, the data signal which reached the switching element and the pixel electrode can be reduced.

[Procedure amendment 14]
[Document to be Amended] Description
[Item(s) to be Amended] 0021
[Method of Amendment] Modification
[The content of amendment]
[0021]
Moreover, the electro-optic device of this invention is further equipped with the frame of the protection-from-light nature which countered said substrate, and it came to prepare an opposite substrate, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, and said electric conduction line is good to include the part prepared in said substrate along with said frame in the location which counters said frame.

[Procedure amendment 15]
[Document to be Amended] Description
[Item(s) to be Amended] 0022
[Method of Amendment] Modification
[The content of amendment]
[0022]
since the electric conduction line is formed in the bottom of the frame of a substrate according to this electro-optic device, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line actuation circuit and a data-line actuation circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing.

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[Procedure amendment 16]
[Document to be Amended] Description
[Item(s) to be Amended] 0023
[Method of Amendment] Modification
[The content of amendment]
[0023]
Moreover, said electric conduction line and said data line of an electro-optic device of this invention are good to be formed from the same low resistance metallic material.
[Procedure amendment 17]
[Document to be Amended] Description
[Item(s) to be Amended] 0024
[Method of Amendment] Modification
[The content of amendment]
[0024]
According to this electro-optic device, since the electric conduction line is formed from the same low resistance metallic material as the data lines, such as aluminum (aluminum), even if the leading-about field of an electric conduction line is long, resistance of an electric conduction line will be suppressed low practically enough. That is, since it becomes possible to wire the large field which sewed clearances, such as other wiring and a circuit, for example, wired zigzag for a long time, or included the electric conduction line in it to the image display field etc. for a long time in an electric conduction line, without lowering the effectiveness of shielding by the increment in resistance, a comparatively easy configuration can raise the effectiveness of the shielding concerned more as a whole. Furthermore, in the manufacture process of the electro-optic device concerned, an electric conduction line and the data line can be formed according to the same process from the same low resistance metallic material. That is, the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.
[Procedure amendment 18]
[Document to be Amended] Description
[Item(s) to be Amended] 0025
[Method of Amendment] Modification
[The content of amendment]
[0025]
Moreover, said picture signal line and the clock signal line of consisting of same low resistance metal layers formed on the same flat surface parallel to said 1st substrate are [the electro-optic device of this invention] good for said electric conduction line part part list which intervenes between said picture signal line and a clock signal line.
[Procedure amendment 19]
[Document to be Amended] Description
[Item(s) to be Amended] 0026
[Method of Amendment] Modification
[The content of amendment]
[0026]
According to this electro-optic device, since a part for the electric conduction line part which intervenes between a picture signal line and a clock signal line is formed on the picture signal line, the clock signal line, and the same flat surface parallel to a substrate, the effectiveness of shielding is demonstrated more efficiently. Here, the same flat-surface top means that you may wire these on the layer insulation layer formed on the semi-conductor layer of switching elements, such as an insulating-layer top used as the substrate which could wire these directly on the substrate or was formed on the substrate, and TFT. Furthermore, in the manufacture process of the electro-optic device concerned,

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since an electric conduction line, a picture signal line, and a clock signal line can be collectively formed from a low resistance metal layer for example, with same aluminum layer etc., the increment in the manufacture process by forming an electric conduction line can be suppressed to minimum.
[Procedure amendment 20]
[Document to be Amended] Description
[Item(s) to be Amended] 0027
[Method of Amendment] Modification
[The content of amendment]
[0027]
Moreover, the electro-optic device of this invention is good to equip said pixel electrode with the capacity line which gives the capacity of the specified quantity further, and to connect this capacity line to said electric conduction line.
[Procedure amendment 21]
[Document to be Amended] Description
[Item(s) to be Amended] 0028
[Method of Amendment] Modification
[The content of amendment]
[0028]
According to this electro-optic device, since the capacity of the specified quantity is given to the pixel electrode by the capacity line, even if duty ratio is small, a high definition display is enabled. And the capacity line is connected to the electric conduction line. Therefore, the adverse effect to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines.
[Procedure amendment 22]
[Document to be Amended] Description
[Item(s) to be Amended] 0029
[Method of Amendment] Modification
[The content of amendment]
[0029]
Moreover, the frame of the protection-from-light nature which the electro-optic device of this invention countered said substrate, and the opposite substrate was formed, and was formed at least in one side among said substrate and said opposite substrate along with the profile of said image display field, Said pixel electrode is further equipped with the capacity line which gives capacity, and said electric conduction line is good to connect said capacity line to said electric conduction line in said location which counters while it is installed in the location which counters said frame.
[Procedure amendment 23]
[Document to be Amended] Description
[Item(s) to be Amended] 0030
[Method of Amendment] Modification
[The content of amendment]
[0030]
since opposite arrangement of the electric conduction line is carried out at the frame of a substrate according to this electro-optic device, space-saving-ization on a TFT array substrate is attained, for example, can form a scanning-line actuation circuit and a data-line actuation circuit in the circumference part of the 1st substrate with allowances, and the display area in an electro-optic device also decreases by electric conduction line formation -- most -- or there is completely nothing.

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Moreover, since the capacity line is connected to the electric conduction line, the adverse effect to the switching element and pixel electrode by potential fluctuation of a capacity line is prevented. And wiring for making a capacity line into constant potential can be made to serve a double purpose by the electric conduction line, and an external input terminal still more nearly required in order to make a capacity line into constant potential can also be made to serve a double purpose with the above-mentioned 3rd external input terminal or the external input terminal only for electric conduction lines. Moreover, the connection between an electric conduction line and a capacity line can use a tooth space effectively for a frame, without decreasing a TFT substrate top display area, since opposite arrangement is carried out.

[Procedure amendment 24]
[Document to be Amended] Description
[Item(s) to be Amended] 0031
[Method of Amendment] Modification
[The content of amendment]
[0031]
Moreover, the electronic equipment of this invention is characterized by having the electro-optic device mentioned above.

[Procedure amendment 25]
[Document to be Amended] Description
[Item(s) to be Amended] 0032
[Method of Amendment] Modification
[The content of amendment]
[0032]
According to this electronic equipment, it has the electro-optic device of the invention in this application mentioned above, the clock noise of a RF is reduced, and the high-definition image display of electronic equipment becomes possible.

[Translation done.]

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期限 '06. 2. 06 知的財産室 SEIKO EPSON CORPORATION

特許出願の番号	特願２００４－１９３５１５
起案日	平成１７年１１月２５日
特許庁審査官	河原　英雄　　８５０６　２Ｍ００
特許出願人代理人	上柳　雅誉（外　２名）　様
適用条文	第２９条第１項、第２９条第２項、第３６条

J0101160
US01 公開

この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から６０日以内に意見書を提出して下さい。

理　由

〈理由１〉

この出願の下記の請求項に係る発明は、その出願前に日本国内又は外国において、頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

請求項１－１１、１４に対して　　引用文献１

［備考］

引用文献１（特に段落００５３、図６を参照）には、走査駆動回路用制御信号配線の外部接続端子の線幅を、信号線の外部接続端子の線幅より広くした電気光学装置が記載されている。

端子間のピッチは当業者が適宜に設計し得る事項にすぎず、また、電気光学パネルと外部基板とを、フレキシブル基板及び異方性導電膜を用いて接続することは、周知の技術（例えば特開２００３－１５２０１９号公報）である。

してみると、本願の上記請求項に係る発明は、引用文献１に記載された発明に比し格別の相違点が認められない。

引例手配済

〈理由２〉

この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法

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請求項１－１１、１４に対して　　引用文献１

請求項１２、１３　　引用文献１及び２

［備考］

請求項１－１１、１４については、理由１の備考欄で述べたとおりである。

入力端子群をデータ線駆動回路に沿って基板端側に設けることは引用文献２（図１）に記載されている。引用文献１に記載された電気光学装置において、引用文献２に記載されているのと同様に、入力端子群をデータ線駆動回路に沿って基板端側に設けることに格別の困難性は認められない。

引　用　文　献　等　一　覧

１．特開２００３－２１６０６４号公報　引例手配済

２．特開平１１－２２３８３２号公報　引例手配済

〈理由３〉

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記

（１）請求項１０において「請求項９に記載した電気光学パネル」なる記載があるが、請求項９に記載された発明は「電気光学装置」に係る発明である。したがって、請求項１０の記載は請求項９の記載と整合していない。結果として、請求項１０に係る発明は明確でない。

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－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－

先行技術文献調査結果の記録

・調査した分野　　ＩＰＣ第７版　　Ｇ０９Ｆ　９／００

Ｇ０９Ｆ　９／３０

Ｇ０２Ｆ　１／１３４５

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, BAO QUAN T	
ART UNIT	**PAPER NUMBER**
4131	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/914,044	FUJITA, SHIN	
	Examiner	Art Unit	
	Bao-Quan T. Ho	4131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

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Status

1)☒ Responsive to communication(s) filed on *06 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, US Patent 6,262,702, in view of Hirosue et al., US Patent 7,002,657 (hereafter referenced as Hirosue).

Regarding claim 12, Murade discloses an electro-optical panel in fig. 1 comprising:

a plurality of data lines (35) on a substrate;

a plurality of scanning lines (31) on the substrate and intersecting the plurality of data lines;

an image display area (seen in fig. 1) on the substrate which includes a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a scanning-line drive circuit (104) for driving the pixels;

a data-line drive circuit (101) for supplying data signals to the pixels; and

an input terminal group (terminals located on the bottom of fig. 1) for supplying signals to the scanning-line drive circuit and the data-line drive circuit,

wherein the scanning-line drive circuit is disposed along one side of the substrate on the substrate, the data-line drive circuit is disposed along a side which is not opposed to the one side on the substrate, the input terminal group is disposed along the data-line drive circuit and is disposed at a further edge side of the substrate than the data-line drive circuit (circuit and terminals placements can be seen in fig. 1 and col. 15 lines 28-51); and

the input terminal group has a first input terminal group for supplying a driving signal to the scanning-line drive circuit and a second input terminal group for supplying an image signal to the data-line drive circuit, the second input terminal is disposed in the central part of the input terminal group, the first input terminal is disposed at the outer side of the input terminal group (terminal grouping to scan and data circuit can be seen in figure 1).

But, Murade does not specifically teach the first input terminal has a larger area than the second input terminal.

However, Hirosue teaches terminals having larger widths in order to reduce resistance (col. 7 lines 34-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have the first input terminal has a larger area than the second input terminal as taught by Murade for the purpose of reducing the resistance of the terminal and the wiring.

Regarding claim 13, Murade and Hirosue discloses an electro-optical panel according to claim 12, Murade further comprising a fourth input terminal (terminal of DX)

for supplying a driving signal (DX) to the data-line drive circuit and the fourth input terminal is disposed between the first input terminal and the second input terminal (seen in figure 1).

But, Murade does not specifically teach wherein the fourth input terminal has an area equal to an area of the first input terminal,

However, Hirosue teaches terminals having larger widths in order to reduce resistance (col. 7 lines 34-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade wherein the fourth input terminal has an area equal to an area of the first input terminal as taught by Murade for the purpose of reducing the resistance of the terminal and the wiring.

3. **Claims 1-5, 9, 10, and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, in view of Hirosue, and in further view of Morozumi et al., US Patent 4,242,679 (hereafter referenced as Morozumi).

Regarding claims 1 and 2, Murade discloses in figure 1 an electro-optical panel comprising:

a plurality of data lines (35);

a plurality of scanning lines (31) intersecting the plurality of data lines;

a plurality of pixels (fig. 1) disposed corresponding to the intersections between the data lines and the scanning lines;

a first input terminal (terminal of DY) supplied with a first input signal (DY); a

second input terminal (terminal of DX) supplied with a second input signal.(DX); and

a drive circuit (scanning line driving circuit 104 and data line driving circuit 101) which controls a grayscale of the pixels based on the first and the second input signals,

Murade does not specifically teach wherein the first input signal includes a higher frequency component compared with the second input signal.

However, Morozumi teaches a high frequency component to be included in the driving signal (col. 8 lines 13-23).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have the first input signal to have a high frequency component as taught by Morozumi for the purpose of operating of the liquid crystal display cell to be compensated in response to changes in external conditions (col. 8 lines 17-20).

Murade does not specifically teach the first input terminal has a larger area than the second input terminal, as claimed in claim 1, and wherein the first input terminal has a smaller input resistance compared with the second input terminal, as claimed in claim 2.

However, Hirosue teaches terminals having larger widths in order to reduce resistance (col. 7 lines 34-44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have the first input terminal has a larger area than the second input terminal, and wherein the first input terminal has a

smaller input resistance compared with the second input terminal as taught by Murade for the purpose of reducing the resistance of the terminal and the wiring.

Regarding claim 3, Murade, Moromuzi, and Hirosue discloses an electro-optical panel according to claim 1, Murade also discloses wherein a signal supplied to the first input terminal comprises a driving signal supplied to a scanning-line drive circuit (col. 15 lines 53-65).

Regarding claim 4, Murade, Moromuzi, and Hirosue discloses an electro-optical panel according to claim 1, Murade also discloses wherein a signal supplied to the second input terminal comprises an image signal col. 15 lines 66-67 to col. 16 lines 1-13).

Regarding claim 5, Murade, Moromuzi, and Hirosue discloses an electro-optical panel according to claim 1, Murade also discloses in figure 1 wherein the first input terminal and the second input terminal, which are disposed along an edge of a substrate, are formed in line, the second input terminal is disposed in the central part of the substrate, and the first input terminal is disposed at the outer side of the substrate.

Regarding claim 9, Murade, Moromuzi, and Hirosue discloses an electro-optical apparatus comprising: an electro-optical panel set forth in claim 1;

power source (display information processing circuit 1002, fig. 14, col. 33 lines 39-66 to col. 34 lines 1-6) means for supplying the power source; and

signal generation (driving circuit 1004, fig. 14, col. 33 lines 39-66 to col. 34 lines 1-6) means for supplying the input signals.

Regarding claim 10, Murade, Moromuzi, and Hirosue discloses an electro-optical apparatus comprising: an electro-optical panel set forth in claim 9;

Murade also discloses an electro-optical apparatus comprising:

an external substrate (polymide tape 1322, fig. 18, col. 35 lines 19-28) which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate (Tape carrier package 1320, fig. 18, col. 35 lines 19-28) which connects the external substrate and the electro-optical panel.

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of first input terminals and the plurality of second input terminals through an anisotropic conductive film (fig. 18, col. 35 lines 19-28).

Regarding claim 14, this is rejected the same reason as stated above in claim 1 as this is the corresponding apparatus.

4. **Claims 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, in view of Morozumi, in further view of Hirosue, and in further view Hayato, Japan Publication 2003-216064A.

Regarding claim 6, Murade, Moromuzi, and Hirosue discloses an electro-optical panel according to claim 1, Murade further discloses a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source (power supply of VSSY or VDDY, col. 15 lines 53-65).

The Murade does not specifically teach wherein the area of the third input terminal is not smaller than that of the first input terminal.

However, Hayato teaches the power source terminal are formed wider than the scanning lines and signal lines (paragraph [0009]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have the area of the third input terminal not smaller than that of the first input terminal as taught by Hayato in paragraph [0009] for the purpose of preventing nonconformity on the display of display nonuniformity and contrast lowering.

Regarding claim 7, Murade, Moromuzi, Hirosue, and Hayato discloses an electro-optical panel according to claim 6, Murade also discloses in figure 1 wherein the third input terminal includes a plurality of adjacent terminals of at least one of the first input terminal (terminal of DY) and the second input terminal (terminal of DX).

5. **Claims 8 and 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, in view of Moromuzi, in further view of Hirosue, and in further view of Totjutsu et al., Japan Publication 2003-43517.

Regarding claim 8, Murade, Moromuzi, and Hirosue disclose an electro-optical panel according to claim 1, also Murade discloses in fig. 1 wherein a plurality of the power source terminals, a plurality of the first input terminals, and a plurality of the second input terminals are included;

the plurality of the power source terminals, the plurality of the first input terminals, and the plurality of the second input terminals are formed in line on a substrate (fig. 1); and

But, Murade, Moromuzi, and Hirosue does not specifically teach a pitch interval of the adjacent first input terminals is an integer multiple of a pitch interval of the adjacent second input terminals.

However, Totjutsu teaches placing dummy terminals that is an integer multiple of a lead terminal pitch (paragraph [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have the pitch interval of the adjacent first input terminals is an integer multiple of a pitch interval of the adjacent second input terminals as taught by Totjutsu for the purpose of determining the existence of the position gaps between each terminals, and also for scaling the structure size to the user's preference (paragraph [0007] and [0019]).

Regarding claim 11, Murade, Moromuzi, and Hirosue discloses an electro-optical apparatus according to claim 10.

But, Murade, Moromuzi, and Hirosue does not specifically teach wherein wiring lines are formed corresponding to a reference pitch interval of the second input terminals on the flexible substrate.

However, Totjutsu teaches placing dummy terminals that is an integer multiple of a lead terminal pitch (paragraph [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to modify Murade to have a reference pitch interval of the second input terminals on the flexible substrate as taught by Totjutsu for the purpose of determining the existence of the position gaps between each terminals, and also for scaling the structure size to the user's preference (paragraph [0007] and [0019]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao-Quan T. Ho whose telephone number is (571) 270-3264. The examiner can normally be reached on M-F, 7:30 am to 5:00 pm EST, alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian T. Pendleton can be reached on (571) 272-7527. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH

BRIAN TYRONE PENDLETON
SUPERVISORY PATENT EXAMINER

OIPE IAP50 MAR 07 2006 PATENT & TRADEMARK OFFICE

FORM HDP-1449 (Based on Form PTO-1449)

PATENT AND TRADEMARK OFFICE
INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Sheet 1 of 1

ATTORNEY DOCKET NO.	SERIAL NO.
9319S-000838	10/914,044
APPLICANT	
Shin FUJITA	
FILING DATE	GROUP
August 6, 2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.	/BTH/	2003-152019A	05/23/2003	Japan		X	
2.	/BTH/	2003-216064A	07/30/2003	Japan		X	
3.	/BTH/	11-223832A	08/17/1999	Japan		X	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.		Examination result regarding corresponding Japanese application

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Examiner:	/Bao-Quan T Ho/	Date Considered:	10/24/2007

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FORM HDP-1449 (Based on Form PTO-1449)	ATTORNEY DOCKET NO.	SERIAL NO.
PATENT AND TRADEMARK OFFICE	9319S-000838	10/914,044
INFORMATION DISCLOSURE CITATION	APPLICANT	
(Use several sheets if necessary)	Shin Fujita	
Sheet 1 of 1	FILING DATE	GROUP
	8/6/2004	2673

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FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.	/BTH/	2822558	Sept/1998	Japan		Abstract	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

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1.		

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Examiner:	/Bao-Quan T Ho/	Date Considered:	10/24/2007

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Notice of References Cited	Application/Control No. 10/914,044	Applicant(s)/Patent Under Reexamination FUJITA, SHIN	
	Examiner Bao-Quan T. Ho	Art Unit 4131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,262,702	07-2001	Murade, Masao	345/87
*	B	US-7,002,657	02-2006	Hirosue et al.	349/149
*	C	US-4,242,679	12-1980	Morozumi et al.	345/52
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 2003216064 A	07-2003	Japan	NAKANISHI, HAYATO	X
	O	JP 2003043517 A	02-2003	Japan	SAI et al.	X
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BOE EXHIBIT 1003
Page 247 of 473

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-216064

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H05K 1/14
H05K 3/36

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(71)Applicant : SEIKO EPSON CORP

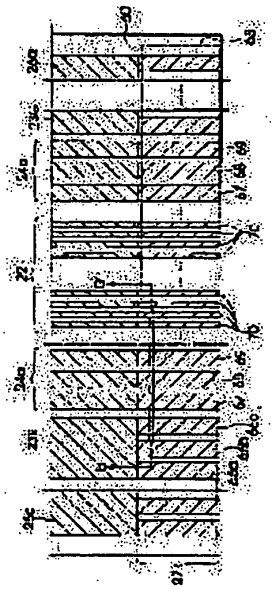
(72)Inventor : NAKANISHI HAYATO

(54) ELECTROOPTICAL DEVICE AND ELECTRONIC EQUIPMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electrooptical device in which unevenness in electrical resistivity in a fixed section is resolved by making pressing condition of a display substrate and a relay substrate same over the entire fixed section and generation of display failure such as reduction in contrast is eliminated and to provide electronic equipment having the device.

SOLUTION: The electrooptical device is provided with a display substrate on which a plurality of light emitting elements and a switching element are formed. The switching element supplies currents, which are being supplied through a power supply line such as a light emitting power supply wiring 23R, to the light emitting elements in accordance with the signals supplied through a signal line such as a scanning line driving circuit control signal wiring 24a. The power supply line such as the wiring 23R is formed with a width which is made wider than the signal line such as the wiring 24a. A plurality of external connection terminals such as external connection terminals 66a, 66b and 66c are provided for the power supply line such as the wiring 23R.



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LEGAL STATUS

[Date of request for examination] 01.09.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

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CLAIMS

[Claim(s)]

[Claim 1] The electro-optic device characterized by preparing two or more 2nd external connection terminals to said 2nd wiring in the electro-optic device with which the 1st wiring which it comes to connect with the 1st external connection terminal, and the 2nd wiring larger than the width of face of the 1st wiring concerned were formed at least.

[Claim 2] The electro-optic device according to claim 1 characterized by forming heights in said 1st external connection terminal and said 2nd external connection terminal.

[Claim 3] The electro-optic device according to claim 1 or 2 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal.

[Claim 4] An electro-optic device given in any 1 term of claim 1 to claim 3 to which width of face of said 2nd external connection terminal is characterized by the almost equal thing.

[Claim 5] Said 1st wiring, the 1st junction wiring which has comparable width of face, and said 2nd wiring and the 2nd junction wiring which has comparable width of face are formed. Said 1st wiring and said 1st junction wiring are electrically connected through said 1st external connection terminal. An electro-optic device given in any 1 term of claim 1 to claim 4 characterized by having the junction substrate to which said 2nd wiring and said 2nd junction wiring were electrically connected through said 2nd external connection terminal.

[Claim 6] It is the electro-optic device characterized by forming more widely than the width of face of said signal line the width of face of said power-source line in the electro-optic device with which two or more light emitting devices and the switching element which supplies the current supplied through a power-source line according to the signal supplied through a signal line to each aforementioned light emitting device were formed, and preparing two or more 1st external connection terminals to said power-source line.

[Claim 7] The electro-optic device according to claim 6 characterized by forming heights in the 2nd external connection terminal prepared to said 1st external connection terminal and said signal line.

[Claim 8] The electro-optic device according to claim 6 or 7 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal.

[Claim 9] An electro-optic device given in any 1 term of claim 6 to claim 8 to which width of face of said 2nd external connection terminal is characterized by the almost equal thing.

[Claim 10] Said signal line, the 1st junction wiring which has comparable width of face, and said power-source line and the 2nd junction wiring which has comparable width of face are formed. Said signal line and said 1st junction wiring are electrically connected through said 1st external connection terminal. An electro-optic device given in any 1 term of claim 6 to claim 9 characterized by having the junction substrate to which said power-source line and said 2nd junction wiring were electrically connected through said 2nd external connection terminal.

[Claim 11] The electro-optic device according to claim 10 characterized by said 2nd external connection terminal and said 2nd junction wiring having fixed with the anisotropy electric conduction film in said 1st

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external connection terminal and said 1st junction wiring, and a list.
[Claim 12] Electronic equipment characterized by equipping any 1 term of claim 1 to claim 11 with the electro-optic device of a publication.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to electronic equipment equipped with the electro-optic device which was built over an electro-optic device and electronic equipment, especially was equipped with the organic electroluminescence ingredient, and the electro-optic device concerned.
[0002]
[Description of the Prior Art] In recent years, development of the color electro-optic device of the structure where the light emitting device which consists of luminescent material, such as an organic fluorescence ingredient, between a pixel electrode (anode plate) and cathode was pinched, especially the organic electroluminescence display using the organic electroluminescence (organic electroluminescence) ingredient as a luminescent material is performed. Hereafter, the conventional electro-optic device (organic electroluminescence display) is explained briefly.
[0003] Drawing 11 is drawing showing the wiring structure of the conventional electro-optic device. As shown in drawing 11 , two or more power-source wiring 903 for luminescence with which the conventional electro-optic device is prolonged in parallel to two or more scanning lines 901, two or more signal lines 902 prolonged in the direction in which it crosses to the scanning line 901, and a signal line 902 is wired, respectively, and the pixel field A is formed for each [of the scanning line 901 and a signal line 902] intersection of every. Each signal line 902 is connected to the shift register, the level shifter, the video line, and the data side actuation circuit 904 equipped with an analog switch, and each scanning line 901 is connected to the scan side actuation circuit 905 equipped with a shift register and a level shifter.
[0004] Moreover, the switching thin film transistor 913 by which a scan signal is supplied to each of the pixel field A through the scanning line 901 at a gate electrode, The retention volume Cap holding the picture signal supplied from a signal line 902 through this switching thin film transistor 913, The current thin film transistor 914 by which the picture signal held with retention volume Cap is supplied to a gate electrode, The luminous layer 910 put between the pixel electrode 911 with which an actuation current flows in from the power-source wiring 903 for luminescence when it connects with the power-source wiring 903 for luminescence electrically through this current thin film transistor 914, and this pixel electrode 911 and cathode 912 is formed. Cathode 912 is connected to the power circuit 931 for cathode.

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[0005] Luminous layer 910R which emits light in red, luminous layer 910G which emit light green, and three sorts of light emitting devices of luminous layer 910B which emit light blue are contained in the above-mentioned luminous layer 910, and stripe arrangement of each luminous layers 910R, 910G, and 910B is carried out. And the power-source wiring 903R, 903G, and 903B for luminescence connected to each luminous layers 910R, 910G, and 910B through the current thin film transistor 914 is connected to the power circuit 932 for luminescence, respectively. Power-source wiring for luminescence is wired for every color, because the actuation potentials of a luminous layer 910 differ for every color.
[0006] In the above configuration, if a scan signal is supplied to the scanning line 901 and the switching thin film transistor 913 is turned on, the charge according to the picture signal currently then supplied to the signal line 902 will be held at retention volume Cap. According to the amount of the charge held at this retention volume Cap, the on-off condition of the current thin film transistor 914 is decided. And a current flows to the pixel electrode 911 through the current thin film transistor 914 from the power-source wiring 903R, 903G, and 903B for luminescence, and an actuation current flows to cathode 912 through a luminous layer 910 further. At this time, luminescence of an amount according to the amount of currents which flowed the luminous layer 910 is obtained from a luminous layer 910.
[0007]
[Problem(s) to be Solved by the Invention] The electro-optic device shown in drawing 11 By the way, the scanning line 901, a signal line 902, cathode 912, power-source wiring 903 (903R, 903G, 903B) for luminescence, The scan side actuation circuit 905 and the pixel field A may be formed on transparence substrates (display substrate), such as glass, and the circuit of the power circuit 931 for cathode, the power circuit 932 for luminescence, and data side actuation circuit 904 grade may be considered as the configuration arranged on a flexible substrate (junction substrate) with flexibility.
[0008] It is necessary to make a flexible substrate fix to a substrate in this configuration, and to make it flow through the scanning line 901, a signal line 902, cathode 912, and the power-source wiring 903 for luminescence and the circuit formed on the flexible substrate electrically in it. Fixing and the electric connection between a substrate and a flexible substrate are made by arranging the anisotropy electric conduction film containing an electric conduction particle between a substrate and a flexible substrate, and making a flexible substrate stick to it by pressure to a substrate.
[0009] In order to be stabilized and to make the luminous layer 910 prepared in the electro-optic device mentioned above emit light, it is required that potential fluctuation of the actuation current impressed to the pixel electrode 911 from the power-source wiring 903 for luminescence should be lessened as much as possible. Especially the electro-optic device shown in drawing 1111 is an electro-optic device of a current actuation mold, and in order to prevent the nonconformity on the display of display nonuniformity, contrast lowering, etc., it needs to suppress the voltage drop by wiring resistance of cathode 912 and the power-source wiring 903 for luminescence etc. as much as possible. For this reason, cathode 912 and the power-source wiring 903 for luminescence are formed more broadly than the scanning line 901 and a signal line 902.

power wiring broadly than scanning
[0010] In case it is made to fix with a substrate and a flexible substrate, in order to attain equalization of the electric resistance produced mainly in the sticking-by-pressure section, there is a demand of wanting to make sticking-by-pressure conditions the same all over the fixing section. In order to fill this demand, it is necessary to make the same the configuration of a terminal where it is prepared in the fixing section and various wiring mentioned above is connected.
[0011] However, as mentioned above, since it is an electro-optic device of a current actuation mold, if the voltage drop by wiring resistance etc. is taken into consideration, it is difficult [the electro-optic device shown in drawing 11] for narrowing wiring width of face of cathode 912 and the power-source wiring 903 for luminescence. Moreover, in order to arrange these [all], thinning and since it is necessary to form a ** pitch, it is also difficult [it / as for the scanning line 901 and a signal line 902, there are many numbers, and] to make line breadth of the scanning line 901 and a signal line 902 comparable as the line breadth of cathode 912 and the power-source wiring 903 for luminescence.

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[0012] This invention is made in view of the above-mentioned situation, and it aims at offering electronic equipment equipped with the electro-optic device which does not produce the nonconformity on the display of lowering of contrast etc., and the electro-optic device concerned while it can cancel the heterogeneity of the electric resistance in the fixing section by covering the whole fixing section and making the same the sticking-by-pressure conditions of a display substrate and a junction substrate.

[0013]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the electro-optic device by the 1st viewpoint of this invention is characterized by preparing two or more 2nd external connection terminals to said 2nd wiring in the electro-optic device with which the 1st wiring which it comes to connect with the 1st external connection terminal, and the 2nd wiring larger than the width of face of the 1st wiring concerned were formed at least. According to this invention, since two or more external connection terminals are prepared to the 2nd wiring broader than the 1st wiring, while making a display substrate fix the substrate with which wiring was given, the whole fixing section can be covered and sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc. is not produced. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by forming heights at said 1st external connection terminal and said 2nd external connection terminal. According to this invention, heights are formed in both the 1st external connection terminal prepared to the 1st wiring and the 2nd wiring, and the 2nd external connection terminal. for example, when making a display substrate fix the substrate to which wiring was given by the anisotropy electric conduction film Since the rate of the rate which the electric conduction particle contained in the anisotropy electric conduction film protrudes from the ends of the 1st external connection terminal and the 2nd external connection terminal decreasing, and stopping on an external connection terminal at reverse rises, it is very suitable when reducing the electric resistance in the fixing section. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal. Since the 1st external connection terminal and the 2nd external connection terminal have the composition divided as two or more electrodes so to speak by two or more crevices formed in the front face of the 1st external connection terminal and the 2nd external connection terminal according to this invention, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as the charge condition of the pressure when taking a flow, can equalize more. Moreover, the electro-optic device by the 1st viewpoint of this invention is characterized by the width of face of said 2nd external connection terminal being almost equal. According to this invention, since the width of face of the 2nd external connection terminal is set up almost equally, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be set as a more desirable condition. Moreover, the electro-optic device by the 1st viewpoint of this invention Said 1st wiring, the 1st junction wiring which has comparable width of face, and said 2nd wiring and the 2nd junction wiring which has comparable width of face are formed. It is characterized by having the junction substrate to which said 1st wiring and said 1st junction wiring were electrically connected to through said 1st external connection terminal, and said 2nd wiring and said 2nd junction wiring were electrically connected through said 2nd external connection terminal. In order to solve the above-mentioned technical problem, the electro-optic device by the 2nd viewpoint of this invention In the electro-optic device with which two or more light emitting devices and the switching element which supplies the current supplied through a power-source line according to the signal supplied through a signal line to each aforementioned light emitting device were formed The width of face of said power-source line is formed more widely than the width of face of said signal line, and it is characterized by preparing two or more 1st external connection terminals to said

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power-source line. [when the power-source line formed broadly and the signal line carried out in thinning and a ** pitch in order to supply many signals are intermingled from the need of supplying a high current in order to obtain luminescence from a light emitting device according to this invention] Since two or more external connection terminals are prepared to the power-source line formed broadly, while making a display substrate fix the substrate with which wiring was given, the whole fixing section can be covered and sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc. is not produced. Moreover, the electro-optic device by the 2nd viewpoint of this invention is characterized by forming heights at the 2nd external connection terminal prepared to said 1st external connection terminal and said signal line. According to this invention, heights are formed in both the 1st external connection terminal prepared to a power-source line and a signal line, and the 2nd external connection terminal. for example, when making a display substrate fix the substrate to which wiring was given by the anisotropy electric conduction film Since the rate of the rate which the electric conduction particle contained in the anisotropy electric conduction film protrudes from the ends of the 1st external connection terminal and the 2nd external connection terminal decreasing, and stopping on an external connection terminal at reverse rises, it is very suitable when reducing the electric resistance in the fixing section. Moreover, the electro-optic device by the 2nd viewpoint of this invention is an electro-optic device according to claim 6 or 7 characterized by forming two or more crevices in the front face of said 1st external connection terminal and said 2nd external connection terminal. Since the external connection terminal has composition divided as two or more electrodes so to speak by two or more crevices formed in the front face of the 1st external connection terminal and the 2nd external connection terminal according to this invention, while making a display substrate fix the substrate with which wiring was given, sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow, can be equalized more. Moreover, the electro-optic device by the 2nd viewpoint of this invention is characterized by the width of face of said 2nd external connection terminal being almost equal. Moreover, the electro-optic device by the 2nd viewpoint of this invention Said signal line, the 1st junction wiring which has comparable width of face, and said power-source line and the 2nd junction wiring which has comparable width of face are formed. It is characterized by having the junction substrate to which said signal line and said 1st junction wiring were electrically connected to through said 1st external connection terminal, and said power-source line and said 2nd junction wiring were electrically connected through said 2nd external connection terminal. Moreover, as for the electro-optic device by the 2nd viewpoint of this invention, it is desirable that said 2nd external connection terminal and said 2nd junction wiring have fixed with the anisotropy electric conduction film in said 1st external connection terminal and said 1st junction wiring, and a list. The electronic equipment of this invention is characterized by having an electro-optic device given in above any they are.

[0014]

[Embodiment of the Invention] Hereafter, with reference to a drawing, the electro-optic device and electronic equipment by 1 operation gestalt of this invention are explained to a detail. In addition, each drawing referred to by the following explanation has changed the contraction scale for each class or every each part material in order to make each class and each part material the magnitude of extent which can be recognized on a drawing.

[0015] Drawing 1 is the decomposition perspective view showing typically the electro-optic device by 1 operation gestalt of this invention. As shown in drawing 1 , general classification of the electro-optic device 10 of this operation gestalt constitutes it from a display substrate 20 and a junction substrate 30 connected to the display substrate 20. The display substrate 20 is organic electroluminescence equipment of the active matrix which used the thin film transistor (Thin Film Transistor) as a switching element.

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[0016] Two or more scanning lines 21 are formed in this display substrate 20, and two or more signal lines 22 prolonged in the direction which intersects this scanning line 21 are formed in it. Moreover, display device 20a by which two or more formation of the light emitting device was carried out is prepared in the display substrate 20. Furthermore, although the graphic display is omitted in drawing 1 , a power-source line and cathode are formed in the display substrate 20. Moreover, the scanning line 21, the signal line 22, the power-source line that is not illustrated in a list, and the external connection terminal 27 to the cathode of each are formed in the end of the display substrate 20.
[0017] In addition, the electro-optic device 10 shown in drawing 1 should show strictly main configurations typically, and should notice the actual scanning line 21, a signal line 22, and the external connection terminal 27 about the point that a large number are formed on the display substrate 20 with very narrow spacing, respectively. Moreover, the connection condition with the connection condition of the external connection terminal 27 and the scanning line 21 is also omitting the graphic display in drawing 1 .
[0018] Two or more wiring 32 is formed on the base substrate 31 which has flexibility, and the junction substrate 30 is the configuration of having carried the semiconductor chip 33 in the predetermined location of the junction substrate 30 further. The external connection terminal 34 for connecting with wiring and the electric target of the scanning line 21 formed in the display substrate 20 and signal-line 22 grade is formed in the end of wiring 32. In addition, although it is the configuration that only the semiconductor chip 33 was mounted on the junction substrate 30, in drawing 1 , resistance, a capacitor, and other chips may be mounted in the predetermined location of parts other than the part where a semiconductor chip 33 is mounted. Moreover, in order to make an understanding of the structure easy, while wiring 32 and the external connection terminal 34 which are formed in the junction substrate 30 also expand spacing and show it typically, structure is simplified and it has illustrated.
[0019] As shown in drawing 1 , the junction substrate 30 fixes to the display substrate 20 through the anisotropy electric conduction film 40. At this time, the external connection terminal 34 of the junction substrate 30 is electrically connected with the external connection terminal 27 of the display substrate 20 through the anisotropy electric conduction film 40. This anisotropy electric conduction film 40 is formed by distributing much electric conduction particle 41b into thermoplastic or thermosetting resin 41a for adhesion, as it is a high polymer film with the conductivity used in order to give an anisotropy and to make package connection electrically, for example, between the terminals of a couple is shown in drawing 2 R> 2.
[0020] Drawing 2 is the sectional view showing signs that the junction substrate 30 and the display substrate 20 fix with the anisotropy electric conduction film 40. Since electric conduction particle 41b is pinched between the external connection terminal 27 formed in the display substrate 20, and the external connection terminal 34 formed in the junction substrate 30 as shown in drawing 2 , between the external connection terminal 27 and the external connection terminals 34 which are junction wiring will be connected electrically. On the other hand, since a connection terminal does not exist in parts other than the part in which the external connection terminal 27 and the external connection terminal 34 are formed even if electric conduction particle 41b is pinched, the flow has not been taken. Thus, a flow can be taken only between the external connection terminal 27 and the external connection terminal 34.
[0021] In order to make the display substrate 20 and the junction substrate 30 fix using the anisotropy electric conduction film 40, it arranges on the installation base (all are graphic display abbreviations) which has the guide plate with which the front face was made into the split face in the display substrate 20, and vacuum adsorption of the display substrate 20 is carried out. At this time, the display substrate 20 is laid on an installation base so that the part which the junction substrate 30 fixes to the display substrate 20 at least may be located above a guide plate. Reducing the touch area of a guide plate and the display substrate 20, and stopping the heat leakage from a guide plate uses the guide plate with which the front face was made into the split face here, and it is for reducing the temperature applied to the display substrate 20.

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[0022] If installation of a up to [the installation base of the display substrate 20] is completed, the anisotropy electric conduction film 40 will be stuck on the part of the display substrate 20 which the junction substrate 30 fixes, the field in which the semiconductor chip 33 was carried will be turned further down, and alignment of the junction substrate 30 will be performed so that the external connection terminal 34 may be located above the anisotropy electric conduction film 40. The rear face of the field in which the external connection terminal 34 is formed using the heating application-of-pressure head which is not illustrated is heated and pressurized, and while taking a flow with the external connection terminal 34 and the external connection terminal 27 currently formed in the display substrate 20, the display substrate 20 is made to fix the junction substrate 30, after the above process is completed. At this time, the temperature applied to the junction substrate 30 and the display substrate 20 from a heating application-of-pressure head is more than 100 [10] - about 100 degrees C of numbers, and the pressure to apply is several mega PASCAL. The display substrate 20 can be made to fix the junction substrate 30 by passing through the above process.

[0023] Next, the detail of the wiring structure of the electro-optic device 10 of this operation gestalt is explained. Drawing 3 is drawing showing typically the wiring structure of the electro-optic device by 1 operation gestalt of this invention. As shown in drawing 3 , two or more power-source wiring 23 for luminescence with which an electro-optic device 10 is prolonged in parallel to two or more scanning lines 21, two or more signal lines 22 prolonged in the direction in which it crosses to the scanning line 21, and a signal line 22 is wired, respectively, and the pixel field A is formed near [each] the intersection of the scanning line 21 and a signal line 22.

[0024] Data side actuation circuit 33a equipped with a shift register, a level shifter, a video line, and an analog switch is connected to each signal line 22. Moreover, the inspection circuit 25 equipped with a thin film transistor is connected to each signal line 22. Furthermore, the scanning-line actuation circuit 24 equipped with a shift register and a level shifter is connected to each scanning line 21.

[0025] Moreover, the switching thin film transistor 52, retention volume Cap, the current thin film transistor 53, the pixel electrode 51, a luminous layer 50, and cathode 26 are established in each of the pixel field A. The scanning line 21 is connected to the gate electrode, and the switching thin film transistor 52 will be driven according to the scan signal supplied from the scanning line 21, and will be in an ON state or an OFF state. Retention volume Cap holds the picture signal supplied from a signal line 22 through the switching thin film transistor 52.

[0026] As for the current thin film transistor 53, the picture signal with which it connects with the switching thin film transistor 52 and retention volume Cap, and the gate electrode was held with retention volume Cap is supplied to a gate electrode. The pixel electrode 51 is connected to the current thin film transistor 53, and when it connects with the power-source wiring 23 for luminescence electrically through the current thin film transistor 53, an actuation current flows in from the power-source wiring 23 for luminescence. The luminous layer 50 is put between the pixel electrode 51 and cathode 26.

[0027] Three sorts of light emitting devices, luminous layer 50R which emits light in red, luminous layer 50G which emit light green, and luminous layer 50B which emits light blue, are contained in the above and a luminous layer 50, and stripe arrangement of each luminous layers 50R, 50G, and 50B is carried out. And the power-source wiring 23R, 23G, and 23B for luminescence connected to each luminous layers 50R, 50G, and 50B through the current thin film transistor 53 is connected to power circuit 33c for luminescence, respectively. The power-source wiring 23R, 23G, and 23B for luminescence is wired for every color, because the actuation potentials of luminous layers 50R, 50G, and 50B differ for every color.

[0028] Moreover, in the electro-optic device of this operation gestalt, electrostatic capacity C1 is formed between cathode 26 and the power-source wiring 23R, 23G, and 23B for luminescence. Actuation of an electro-optic device 10 accumulates a charge in this electrostatic capacity C1. When the potential of the actuation current which flows each power-source wiring 23 for luminescence during

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actuation of an electro-optic device 10 is changed, the accumulated charge discharges to each power-source wiring 23 for luminescence, and controls potential fluctuation of an actuation current. Thereby, the image display of an electro-optic device 10 can be kept normal.

[0029] In addition, in this electro-optic device 10, if a scan signal is supplied from the scanning line 21 and the switching thin film transistor 52 is turned on, according to the potential with which the potential of the signal line 22 at that time was held at retention volume Cap, and was held at retention volume Cap, the on-off condition of the current thin film transistor 53 will be decided. And through the channel of the current thin film transistor 53, an actuation current flows to the pixel electrode 51 from the power-source wiring 23R, 23G, and 23B for luminescence, and a current flows to cathode 26 through luminous layers 50R, 50G, and 50B further. At this time, luminescence of an amount according to the amount of currents which flowed the luminous layer 50 is obtained from a luminous layer 50.

[0030] Next, the concrete configuration of the electro-optic device 10 of this operation gestalt is explained with reference to drawing 4 and drawing 5 . Drawing 4 is the mimetic diagram of the electro-optic device of this operation gestalt, and drawing 5 is a sectional view which meets the A-A' line of drawing 4 . As shown in drawing 4 , the outline configuration of the electro-optic device 10 of this operation gestalt is carried out from a substrate 60, a non-illustrated pixel electrode group field, the power-source wiring 23 (23R, 23G, 23B) for luminescence, and the display pixel section 61 (within the limit [of the alternate long and short dash line in drawing]).

[0031] A substrate 60 is a transparent substrate which consists of glass etc. A pixel electrode group field is a field which has arranged the pixel electrode (graphic display abbreviation) connected to the current thin film transistor 53 shown in drawing 3 in the shape of a matrix on a substrate 60. As shown in drawing 4 , the power-source wiring 23 (23R, 23G, 23B) for luminescence is arranged around a pixel electrode group field, and is connected to each pixel electrode. The display pixel section 61 is located on a pixel electrode group field at least, and is a plane view abbreviation rectangle configuration. This display pixel section 61 is divided in the real viewing area 62 (within the limit [of the two-dot chain line in drawing]) for a center section (or it is also called an effective viewing area), and the dummy area 63 (field between an alternate long and short dash line and a two-dot chain line) arranged on the outside of the real viewing area 62.

[0032] Moreover, the scanning-line actuation circuit 24 is arranged at the both sides in drawing of the real viewing area 62. This scanning-line actuation circuit 24 is located and established in the lower layer side (substrate 60 side) of a dummy area 63. Furthermore, control signal wiring 24a for scanning-line actuation circuits and power-source wiring 24b for scanning-line actuation circuits which are connected to the scanning-line actuation circuit 24 are prepared in the lower layer side of a dummy area 63. Furthermore, the above-mentioned inspection circuit 25 is arranged at the drawing Nakagami side of the real viewing area 62. This inspection circuit 25 is located and established in the lower layer side (substrate side 2) of a dummy area 63, and inspection of the quality of the electro-optic device at the manufacture middle or the time of shipment and a defect can be conducted by this inspection circuit 25.

[0033] As shown in drawing 4 , the power-source wiring 23R, 23G, and 23B for luminescence is arranged in the perimeter of a dummy area 63. Each power-source wiring 23R, 23G, and 23B for luminescence extends in the method of drawing 4 Nakagami along with control signal wiring 24a for scanning-line actuation circuits from the drawing 2 Nakashita side of a substrate 60, is bent from the location where control signal wiring 24a for scanning-line actuation circuits broke off, extends along the outside of a dummy area 63, and is connected to the pixel electrode of the graphic display abbreviation in the real viewing area 62. Moreover, wiring 26a for cathode connected to cathode 26 is formed in the substrate 60. This wiring 26a for cathode is formed in the shape of a plane view abbreviation KO character so that the power-source wiring 23R, 23G, and 23B for luminescence may be surrounded.

[0034] Next, as shown in drawing 5 , the circuit section 11 is formed on a substrate 60, and the display pixel section 61 is formed on this circuit section 11. Moreover, the sealing agent 13 which surrounds the display pixel section 61 annularly is formed in the substrate 60, and it has the closure substrate 14 on

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the display pixel section 61 further. It is joined to the substrate 60 through the sealing agent 13, and the closure substrate 14 consists of glass, a metal, or resin. An adsorbent 15 is stuck on the background of this closure substrate 14, and the water or oxygen mixed in the space between the display pixel section 61 and the closure substrate 14 can be absorbed now on it. In addition, it may replace with an adsorbent 15 and a getter agent may be used. Moreover, as for a sealing agent 13, it is desirable to consist of for example, heat-curing resin or ultraviolet-rays hardening resin, and to consist of an epoxy resin which is especially a kind of heat-curing resin.

[0035] Pixel electrode group field 11a is prepared in a part for the center section of the circuit section 11. This pixel electrode group field 11a is equipped with the pixel electrode 51 connected to the current thin film transistor 53 and the current thin film transistor 53. The current thin film transistor 53 is embedded at the substrate protective layer 281 by which the laminating was carried out on the substrate 60, the insulating layer 283 between the 2nd layer, and the insulating layer 284 between the 1st layer, it is formed, and the pixel electrode 51 is formed on the insulating layer 284 between the 1st layer. It connects with the current thin film transistor 53, and the power-source wiring 23 (23R, 23G, 23B) for luminescence is connected to one side (source electrode) of the electrode formed on the insulating layer 283 between the 2nd layer. In addition, although the retention volume Cap and the switching thin film transistor 52 which were mentioned above are also formed in the circuit section 11, these graphic displays are omitted in drawing 5 . Furthermore, the graphic display of a signal line 22 is omitted in drawing 5 .

[0036] Next, in drawing 5 , the above-mentioned scanning-line actuation circuit 24 is established in the both sides in drawing of pixel electrode group field 11a. The scanning-line actuation circuit 24 shown in drawing 4 is equipped with thin film transistor 24c of the N channel mold which constitutes the inverter contained in a shift register, or a P channel mold, and this thin film transistor 24c is made into the same structure as the above-mentioned current thin film transistor 53 except for the point which is not connected to the pixel electrode 51. In addition, in drawing 5 , although the graphic display of the inspection circuit 25 is omitted, it has the thin film transistor also like this inspection circuit 25. The thin film transistor with which the inspection circuit 25 is equipped is made into the same structure as the current thin film transistor 53 except for the point which is not connected to dummy pixel electrode 51' mentioned later.

[0037] As shown in drawing 5 , on the substrate protective layer 281 of drawing Chugai of the scanning-line actuation circuit 24, control signal wiring 24a for scanning-line actuation circuits is formed. Moreover, on the insulating layer 283 between the 2nd layer of the outside of control signal wiring 24a for scanning-line actuation circuits, power-source wiring 24b for scanning-line actuation circuits is formed. Moreover, the power-source wiring 23 for luminescence is formed in the outside of power-source wiring 24b for scanning-line actuation circuits. This power-source wiring 23 for luminescence has adopted the duplex wiring structure which consists of two wiring, and as mentioned above, it is arranged on the outside of the display pixel section 61. Wiring resistance is mitigable by adopting duplex wiring structure.

[0038] For example, power-source wiring 23R for luminescence for red in the left-hand side in drawing 5 consists of the 1st wiring 23R1 formed on the substrate protective layer 281, and the 2nd wiring 23R2 formed on the 1st wiring 23R1 through the insulating layer 283 between the 2nd layer. The 1st wiring 23R1 and the 2nd wiring 23R2 are connected by the contact hole 23R3 which penetrates an insulating layer 283 between the 2nd layer as shown in drawing 2 . Thus, the 1st wiring 23R1 is formed in the same hierarchy location as wiring 26a for cathode, and the insulating layer 283 is arranged between the 2nd layer between the 1st wiring 23R1 and wiring 26a for cathode. Moreover, it connects with wiring 26b for cathode formed on the insulating layer 283 between the 2nd layer through the contact hole electrically, and gets down from wiring 26a for cathode, and, so to speak, wiring 26a for cathode also has duplex wiring structure as shown in drawing 5 . Therefore, the 2nd wiring 23R2 is formed in the same hierarchy location as wiring 26b for cathode, and the insulating layer 284 is arranged between the 1st layer

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between the 1st wiring 23R2 and wiring 26b for cathode. By taking such structure, the 2nd electrostatic capacity C2 is formed between the 1st wiring 23R1 and wiring 26a for cathode, and between the 2nd wiring 23R2 and wiring 26b for cathode.

[0039] the 1st by which similarly the blue in the right-hand side of drawing 5 and the power-source wiring 23G and 23B for luminescence for green had also adopted duplex wiring structure, and were formed on the substrate protective layer 281, respectively -- with wiring 23G1 and 23B1 the 2nd formed on the insulating layer 283 between the 2nd layer — it constitutes from wiring 23G2 and 23 B-2 — having -- the 1st — wiring 23G1, 23B1, and the 2nd -- wiring 23G2 and 23 B-2 are connected by contact hole 23 G3 which penetrates an insulating layer 283 between the 2nd layer as shown in drawing 4 , and 23B3. And the 2nd electrostatic capacity C2 is formed between the 1st blue wiring 23B1 and wiring 26a for cathode, and between blue 2nd wiring 23 B-2 and wiring 26b for cathode.

[0040] Spacing of the 1st wiring 23R1 and the 2nd wiring 23R2 has the desirable range of 0.6-1.0 micrometers. Since the parasitic capacitance between the source metal and gate metal which have different potential like a signal line 22 and the scanning line 21 as spacing is less than 0.6 micrometers increases, it is not desirable. For example, many parts where source metal and gate metal cross in the real viewing area 62 exist, and when there is much parasitic capacitance of this part, there is a possibility of causing the time delay of a picture signal. Since a picture signal cannot be written in the pixel electrode 51 within the defined period as the result, lowering of contrast is caused. Between the 2nd layer inserted into the 1st wiring 23R1 and the 2nd wiring 23R2, although the construction material of an insulating layer 283 has for example, desirable SiO2 grade, if 1.0 micrometers or more are formed, a possibility that a substrate 60 may break with the stress of SiO2 will arise.

[0041] Moreover, the cathode 26 which extended from the display pixel section 61 is formed in each power-source wiring 23R upside for luminescence. Thereby, on both sides of an insulating layer 284, opposite arrangement of the 2nd wiring 23R2 of each power-source wiring 23R for luminescence is carried out with cathode 26 between the 1st layer, and the 1st above-mentioned electrostatic capacity C1 is formed between the 2nd wiring 23R2 and cathode 26. Here, spacing of the 2nd wiring 23R2 and cathode 26 has the desirable range of 0.6-1.0 micrometers. If spacing is less than 0.6 micrometers, since the parasitic capacitance between the pixel electrodes and source metal which have different potential like a pixel electrode and source metal will increase, the wiring delay of a signal line which uses source metal arises. Consequently, since a picture signal cannot be written in within the defined period, lowering of contrast is caused. The construction material of an insulating layer 284 has SiO2, desirable acrylic resin, etc. between the 1st layer inserted into the 2nd wiring 23R2 and cathode 26. However, formation of 1.0 micrometers or more of SiO(s)2 produces a possibility that a substrate 60 may break with stress. Moreover, in the case of acrylic resin, it can form to about 2.0 micrometers, but since there is a property to expand if water is included, there is a possibility of breaking the pixel electrode formed on it.

[0042] Thus, to the display substrate 20, since the 1st electrostatic capacity C1 is formed between the power-source wiring 23 for luminescence, and cathode 26 The charge accumulated in the 1st electrostatic capacity C1 when the potential of the actuation current which flows the power-source wiring 23 for luminescence was changed is supplied to the power-source wiring 23 for luminescence. The potential insufficiency of an actuation current can be compensated with this charge, can control potential fluctuation, and can keep the image display of luminescence equipment 1 normal. Since the power-source wiring 23 for luminescence and cathode 26 have countered especially on the outside of the display pixel section 61, the amount of charges which makes small spacing of the power-source wiring 23 for luminescence and cathode 26, and is accumulated in the 1st electrostatic capacity C1 can be increased, potential fluctuation of an actuation current can be made smaller, and image display can be carried out to stability. Furthermore, since it has the duplex wiring structure where the power-source wiring 23 for luminescence consists of the 1st wiring and the 2nd wiring, the 2nd electrostatic capacity C2 is formed between the 1st wiring and wiring for cathode and the charge accumulated in the 2nd electrostatic capacity C2 is also supplied to the power-source wiring 23 for luminescence, potential

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fluctuation can be controlled more and the image display of luminescence equipment 1 can be maintained more at normal.

[0043] Next, a luminous layer 50 and the bank section (insulating section) 122 are formed in the real pixel field 62 of the display pixel section 61. As shown in drawing 5 , the laminating of the luminous layer 50 is carried out to each on the pixel electrode 51. Moreover, it has the bank section 122 between each pixel electrode 51 and each luminous layer 50, and it has divided each luminous layer 50. The laminating of the organic substance bank layer 122b separated and located is carried out, and the bank section 122 consists of inorganic substance bank layer 122a and the substrates 60 which are located in a substrate 60 side. In addition, a protection-from-light layer may be arranged between inorganic substance bank layer 122a and organic substance bank layer 122b.

[0044] Extension formation of them is carried out until an inorganic substance and the organic substance bank layers 122a and 122b run aground on the periphery section of the pixel electrode 51, and extension formation of the inorganic substance bank layer 122a is carried out rather than organic substance bank layer 122b at the central site of the pixel electrode 51. Moreover, as for inorganic substance bank layer 122a, it is desirable to consist of inorganic materials, such as SiO2, TiO2, and SiN. Moreover, the thickness of inorganic substance bank layer 122a has the desirable range of 50-200nm, and especially its 150nm is good. Since thickness becomes thin and it becomes impossible to secure the surface smoothness of a hole injection/transporting bed from the hole injection/transporting bed which inorganic substance bank layer 122a mentions later in less than 50nm, it is not desirable. Moreover, since it becomes impossible to secure the surface smoothness of the below-mentioned luminous layer which carries out a laminating on a hole injection/transporting bed by the level difference by inorganic substance bank layer 122a becoming large when thickness exceeds 200nm, it is not desirable.

[0045] Furthermore, organic substance bank layer 122b is formed from the usual resists, such as acrylic resin and polyimide resin. The thickness of this organic substance bank layer 122b has the desirable range of 0.1-3.5 micrometers, and especially its about 2 micrometers are good. Since there is a possibility that organic substance bank layer 122b may become thin, and a luminous layer may overflow from up opening from the total thickness of the hole injection / transporting bed which thickness mentions later in less than 0.1 micrometers, and a luminous layer, it is not desirable. Moreover, since it becomes impossible to secure the step coverage of the cathode 26 formed on organic substance bank layer 122b by the level difference by up opening becoming large when thickness exceeds 3.5 micrometers, it is not desirable. Moreover, if thickness of organic substance bank layer 122b is set to 2 micrometers or more, it is more desirable at the point which can raise the insulation with cathode 26 and the pixel electrode 51. Thus, the luminous layer 50 is formed more thinly than the bank section 122.

[0046] Moreover, the field which shows lyophilic, and the field which shows liquid repellance are formed around the bank section 122. The fields which show lyophilic are inorganic substance bank layer 122a and the pixel electrode 51, and lyophilic groups, such as a hydroxyl group, are introduced into these fields by the plasma treatment which makes oxygen reactant gas. Moreover, the field which shows liquid repellance is organic substance bank layer 122b, and **** machines, such as a fluorine, are introduced by the plasma treatment which makes 4 methane fluoride reactant gas.

[0047] The laminating of the luminous layer 50 is carried out on the hole injection/transporting bed by which the laminating was carried out on the pixel electrode 51 and which is not illustrated. In addition, on these descriptions, the configuration containing a luminous layer 50, and a hole injection/transporting bed is called stratum functionale, and the pixel electrode 51, the stratum functionale, and the configuration included cathode 26 are called light emitting device. A hole injection/transporting bed has the function to convey an electron hole in the interior of a hole injection/transporting bed while having the function to pour an electron hole into a luminous layer 50. By preparing such a hole injection/a transporting bed between the pixel electrode 51 and a luminous layer 50, component properties, such as luminous efficiency of a luminous layer 50 and a life, improve. Moreover, in a luminous layer 50, the electron hole poured in from the hole injection/transporting bed and the electron from cathode 26 join

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together, and fluorescence is generated. A luminous layer 50 has three kinds, the red luminous layer which emits light in red (R), the green luminous layer which emits light in green (G), and the blue luminous layer which emits light in blue (B), and as shown in drawing 3 and drawing 4 , stripe arrangement of each luminous layer is carried out.

[0048] Next, as shown in drawing 5 , the dummy luminous layer 210 and the dummy bank section 212 are formed in the dummy area 63 of the display pixel section 61. The laminating of the dummy organic substance bank layer 212b separated and located is carried out, and the dummy bank section 212 consists of dummy inorganic substance bank layer 212a and the substrates 60 which are located in a substrate 60 side. Dummy inorganic substance bank layer 212a is formed all over dummy pixel electrode 51'. Moreover, dummy organic substance bank layer 212b is formed between the pixel electrodes 51 like organic substance bank layer 122b. And the dummy luminous layer 210 is formed on dummy pixel electrode 51' through dummy inorganic substance bank 212a.

[0049] Dummy inorganic substance bank layer 212a and dummy organic substance bank layer 211b have the inorganic substance explained previously, the same construction material as the organic substance bank layers 122a and 122b, and the same thickness. Moreover, the laminating of the dummy luminous layer 210 is carried out on the dummy hole injection / transporting bed of graphic display abbreviation, and the construction material and thickness of a dummy hole injection / transporting bed, and a dummy luminous layer of it are the same as that of the above-mentioned hole injection / transporting bed, and a luminous layer 50. Therefore, the dummy luminous layer 210 is formed like the above-mentioned luminous layer 50 more thinly than the dummy bank section 212.

[0050] By arranging a dummy area 63 around the real viewing area 62, thickness of the luminous layer 50 of the real viewing area 62 can be made into homogeneity, and display nonuniformity can be controlled. That is, the desiccation conditions of the breathed-out constituent ink in the case of forming a display device by the ink jet method by arranging a dummy area 63 can be made regularity within the real viewing area 62, and there is no possibility that a bias may arise in the thickness of a luminous layer 50 in the periphery section of the real viewing area 62.

[0051] Next, cathode 26 extends on the substrate 60 on the outside of a dummy area 63 while being formed all over the real viewing area 62 and a dummy area 63, and opposite arrangement is carried out with the power-source wiring 23 for luminescence on the outside of a dummy area 63, i.e., the outside of the display pixel section 61. Moreover, the edge of cathode 26 is connected to wiring 26a for cathode formed in the circuit section 11. Cathode 26 plays the role which passes a current to a luminous layer 50 as a counterelectrode of the pixel electrode 51. The laminating of catholyte 26b and reflecting layer 26c which consist of a layered product of lithium fluoride and calcium is carried out, and this cathode 26 is constituted. Only reflecting layer 26c has extended to the outside of the display pixel section 61 among cathode 26. As for reflecting layer 26c, it is desirable to reflect in a substrate 60 side the light emitted from the luminous layer 50, and to consist of aluminum, Ag, a Mg/Ag layered product, etc. Furthermore, the protective layer for antioxidizing which consists of SiO2, SiN, etc. may be prepared on reflecting layer 26c.

[0052] Moreover, as shown in drawing 4 , at the end of a substrate 60, the junction substrate 30 has fixed using the anisotropy electric conduction film 40 mentioned above. In addition, data side actuation circuit 33a shown in drawing 3 , power circuit 33for cathode b, and power circuit 33c for luminescence are built in the semiconductor chip 33 carried on the junction substrate 30. The part enclosed with the broken line in drawing 4 shows the fixing section of the display substrate 20 and the junction substrate 30. Drawing 6 is the plan of the fixing section 65 neighborhood shown in drawing 4 . In addition, in drawing 6 , the graphic display of the anisotropy electric conduction film 40 and the junction substrate 30 is omitted.

[0053] As shown in drawing 6 , in the fixing section 65, the 1st external connection terminal which has width of face comparable as the width of face of wiring to thin wiring of each of line breadth is prepared, and two or more 2nd external connection terminals with width of face narrower than line breadth are

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prepared to broad wiring. For example, to each of control signal wiring 24a for scanning-line actuation circuits with thin line breadth, the 1st external connection terminals 67, 68, and 69 which have width of face comparable as the line breadth of control signal wiring 24a for scanning-line actuation circuits are formed. On the other hand, to power-source wiring 23R for luminescence with wide width of face, the 2nd external connection terminals 66a, 66b, and 66c with width of face narrower than the line breadth of power-source wiring 23R for luminescence are formed. Moreover, the 2nd external connection terminal 70 which has line breadth comparable as a signal line 22 to the signal line 22 with narrow width of face rather than control signal wiring 24a for scanning-line actuation circuits is formed, respectively. In addition, the number of the 1st external connection terminal and the 2nd external connection terminals is suitably set up according to the line breadth of wiring formed in a substrate 60.

[0054] Thus, according to the line breadth of wiring formed in the substrate 60, the number of the 1st external connection terminal and the 2nd external connection terminals is changed for continuing all over the fixing section 65 and making sticking-by-pressure conditions the same as much as possible. That is, as explained using drawing 1 and drawing 2 , although the display substrate 10 and the junction substrate 20 fix with the anisotropy electric conduction film 40, when fixing conditions (for example, the width of face of a terminal, adhesion area, charge condition of a pressure, etc.) differ, the electric resistance in the fixing section 65 interior differs according to the location. If the electric resistance in the fixing section 65 differs according to a location, the nonconformity on the display of display nonuniformity, contrast lowering, etc. will be produced. For this reason, in the fixing section 65, sticking-by-pressure conditions are made the same as much as possible by changing the number of external connection terminals according to the line breadth of wiring formed in the substrate 60. Furthermore, adhesion area can be increased by preparing two or more external connection terminals. That is, since the anisotropy electric conduction film can be arranged among two or more external connection terminals n, firm adhesion is attained.

[0055] Next, the structure of the external connection terminal formed in the fixing section 65 is explained to a detail. Drawing 7 is the sectional view of the 2nd external connection terminal 66c and the 2nd external connection terminal 70 which meet the B-B' line in drawing 6 , and drawing 8 is the enlarged drawing of the external connection terminal 70 in drawing 7 . As shown in drawing 7 and drawing 8 , the substrate protective layer 281 is formed on the substrate 60, and the gate insulating layer 71 which makes SiO2 and/or SiN a subject is formed on this substrate protective layer 281. This gate insulating layer 71 is formed in order to insulate electrically the channel field and gate electrode of a thin film transistor which are not illustrated. In addition, in this description, the component made into a "subject" shall mean a component with the highest content.

[0056] On the gate insulating layer 71, a signal line 22 and power-source wiring 23R for luminescence are formed, and the insulating layer 283 is further formed between the 2nd layer on a signal line 22 and power-source wiring 23R for luminescence. Moreover, the power-source wiring 23 for luminescence and control signal wiring 24a for scanning-line actuation circuits are formed in drawing 3 simultaneously with the scanning line 21 of a publication.

[0057] Two or more formation of the contact hole H is carried out in the up location of a signal line 22 and power-source wiring 23R for luminescence at the above-mentioned insulating layer 283 between the 2nd layer. Moreover, an electrode 73 is formed on the insulating layer 283 between the 2nd layer above power-source wiring 23R for luminescence, and electrodes 74 and 75 are formed on the upper insulating layer 283 between the 2nd layer of a signal line 22.

[0058] Since these electrodes 73, 74, and 75 are formed by the sputtering method etc. after they form a contact hole H, Crevice B is formed in a front face only for the part of the metallic material deposited in the contact hole H in the upper part of a contact hole H. Thus, a flow with power-source wiring 23R for luminescence covered with the insulating layer 283 between the 2nd layer and the electrode 74 formed on the insulating layer 283 between the 2nd layer and the flow of the signal line 22 covered with the insulating layer 283 between the 2nd layer and the electrodes 74 and 75 formed on the insulating layer

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283 between the 2nd layer are taken through a contact hole H.
[0059] Moreover, between the edge of the electrodes 73, 74, and 75 formed on the insulating layer 283 between the 2nd layer, flanks and these electrodes 73 and 74, and 75, while [the 1st layer] consisting of inorganic materials, such as SiN aiming at an electric insulation, the insulating layer 284 is formed. Between the transparent electrode 77 which the transparent electrode 77 which consists of ITO etc. was formed, and was further formed in the periphery of electrodes 73, 74, and 75 and the 2nd external connection terminals 66c and 70, and 70, the protective layer 78 which consists of SiO2 is formed in the upper part of electrodes 73, 74, and 75, the flank, and the periphery. In addition, electrodes 73, 74, and 75 are formed in the gate line and coincidence which are indicated by drawing 3 , and a transparent electrode 77 is formed of ITO and formed simultaneously with a pixel electrode (anode plate).
[0060] As shown in drawing 7 and drawing 8 , two or more crevices B are formed in the front face of the 2nd external connection terminals 66c, 70, and 70 established in the electro-optic device of this operation gestalt, and it is carried out, and has the composition that so to speak this crevice B divided the 2nd external connection terminals 66c, 70, and 70 as two or more electrodes. Although equalization of the fixing conditions in the fixing section 65 is in drawing by changing the number of external connection terminals according to the line breadth of power-source wiring 23for luminescence R, and a signal line 22 as shown in drawing 6 Since two or more crevices B are formed in the front face of the 2nd external connection terminals 66c, 70, and 70, the 2nd external connection terminals 66c, 70, and 70 are very suitable, when becoming what was divided into further two or more electrodes and attaining equalization of fixing conditions.
[0061] Moreover, heights 79 are formed in the edge of the 2nd external connection terminals 66c, 70, and 70 by forming an insulating layer 284 in the edge of electrodes 73, 74, and 75 between the 1st layer. In case these heights 79 fix the display substrate 10 and the junction substrate 20 using the anisotropy electric conduction film 40, they act so that it may prevent that electric conduction particle 41b contained in the anisotropy electric conduction film 40 overflows into the flank of the 2nd external connection terminals 66c, 70, and 70. Consequently, since more electric conduction particle 41b will be arranged on the 2nd external connection terminals 66c and 70 and 70, it is the extremely excellent structure which reduces the electric resistance in the fixing section 65.
[0062] since a configuration for the display substrate 20 of this operation gestalt explained a substrate above to equalize sticking by pressure conditions in the fixing section 65 be prepare , form the external connection terminal 34 form in the junction substrate 30 which fix to the fixing section 65 with the same line breadth as the power source wiring 23for luminescence R and the control signal wiring 24for scanning line actuation circuits a a be show in drawing 6 . However, in order to fix the junction substrate 30 and the display substrate 20 under more uniform sticking-by-pressure conditions, it is suitable that it is the same pattern as the 2nd external connection terminals 66c and 70 and 70 grades which were formed in the fixing section 65.
[0063] As mentioned above, although the electro-optic device by 1 operation gestalt of this invention was explained, the personal computer 600 (electronic equipment) of a note type shown in drawing 9 is manufactured by incorporating in a case electronic parts, such as a mother board equipped with the electro-optic device explained above, CPU (central processing unit), etc., a keyboard, and a hard disk. Drawing 9 is drawing showing an example of electronic equipment equipped with the electro-optic device by 1 operation gestalt of this invention. In addition, in drawing 9 , 601 is a case, 602 is a liquid crystal display, and 603 is a keyboard. Drawing 10 is the perspective view showing the portable telephone as other electronic equipment. The portable telephone 700 shown in drawing 10 is equipped with an antenna 701, an earphone 702, a telephone transmitter 703, a liquid crystal display 704, and operating button section 705 grade, and is constituted.
[0064] Moreover, although the notebook computer and the portable telephone were mentioned as the example and the above-mentioned operation gestalt explained them as electronic equipment, it is possible to apply to electronic equipment, such as equipment equipped with the video tape recorder of

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not only these but a liquid crystal projector, the personal computer corresponding to multimedia (PC) and an engineering workstation (EWS), a pager, a word processor, television, a viewfinder mold, or a monitor direct viewing type, an electronic notebook, an electronic calculator, car navigation equipment, the POS terminal, and the touch panel.

[0065]

[Effect of the Invention] Since two or more 2nd external connection terminals are prepared to the 2nd wiring broader than the 1st wiring according to this invention, while making a display substrate fix the substrate with which wiring was given as explained above, it is effective in the ability to cover the whole fixing section and equalize sticking-by-pressure conditions, such as charge condition of the pressure when taking a flow. For this reason, the heterogeneity of the electric resistance in the fixing section can be canceled, and it is effective in not producing nonconformity on the display of lowering of the display nonuniformity and contrast which originate in the heterogeneity of the electric resistance in the fixing section as that result etc.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the decomposition perspective view showing typically the electro-optic device by 1 operation gestalt of this invention.

[Drawing 2] It is the sectional view showing signs that the junction substrate 30 and the display substrate 20 fix with the anisotropy electric conduction film 40.

[Drawing 3] It is drawing showing typically the wiring structure of the electro-optic device by 1 operation gestalt of this invention.

[Drawing 4] It is the mimetic diagram of the electro-optic device of this operation gestalt.

[Drawing 5] It is the sectional view which meets the A-A' line of drawing 4 .

[Drawing 6] It is the plan of the fixing section 65 neighborhood shown in drawing 4 .

[Drawing 7] It is the sectional view of the 2nd external connection terminal 66c and the 2nd external connection terminal 70 which meet the B-B' line in drawing 6 .

[Drawing 8] It is the enlarged drawing of the external connection terminal 70 in drawing 7 .

[Drawing 9] It is drawing showing an example of electronic equipment equipped with the electro-optic device by 1 operation gestalt of this invention.

[Drawing 10] It is the perspective view showing the portable telephone as other electronic equipment.

[Drawing 11] It is drawing showing the wiring structure of the conventional electro-optic device.

[Description of Notations]

10 .... Electro-optic device

20 .... Display substrate

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22 .... Signal line (the 1st wiring)
23 23R .... Power-source wiring for luminescence (the 2nd wiring, power-source line)
24a .... Control signal wiring for scanning-line actuation circuits (the 1st wiring)
30 .... Junction substrate
40 .... Anisotropy electric conduction film
50 .... Light emitting device
53 .... Switching element
66a, 66b, 66c .... The 2nd external connection terminal
67, 68, 69, 70 .... The 1st external connection terminal
79 .... Heights
B .... Crevice

[Translation done.]

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G09F	9/30	330	G09F	9/30	330Z	2H088
		365			365Z	2H092
G02F	1/13	505	G02F	1/13	505	3K007
	1/1345			1/1345		5C094
	1/1368			1/1368		5E344

審査請求　未請求　請求項の数12　ＯＬ　（全 14 頁）　最終頁に続く

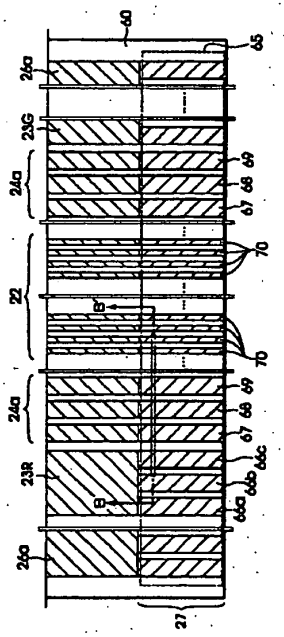
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最終頁に続く

(54)【発明の名称】　電気光学装置及び電子機器

(57)【要約】
【課題】　表示基板と中継基板との圧着条件を固着部全体に亘って同一にすることにより、固着部における電気的抵抗の不均一性を解消することができるとともに、コントラストの低下等の表示上の不具合を生ずることがない電気光学装置、及び当該電気光学装置を備える電子機器を提供する。
【解決手段】　複数の発光素子と、走査線駆動回路用制御信号配線２４ａ等の信号線を介して供給される信号に応じて発光用電源配線２３Ｒ等の電源線を介して供給される電流を発光素子に供給するスイッチング素子とが形成された表示基板を備える電気光学装置であって、発光用電源配線２３Ｒ等の電源線は走査線駆動回路用制御信号配線２４ａ等の信号線より幅広に形成されており、発光用電源配線２３Ｒ等の電源線には、外部接続端子６６ａ，６６ｂ，６６ｃ等の複数の外部接続端子が設けられている。



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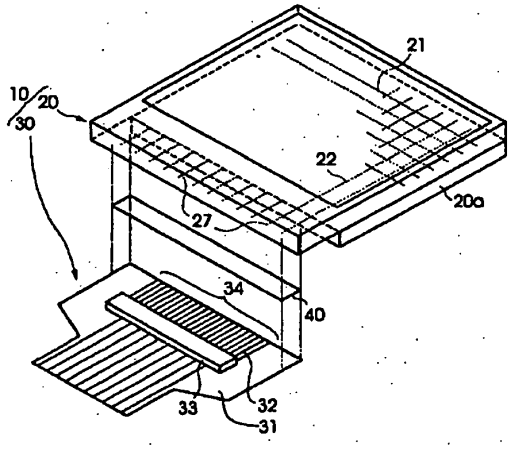
視図である。

【図１１】　従来の電気光学装置の配線構造を示す図である。

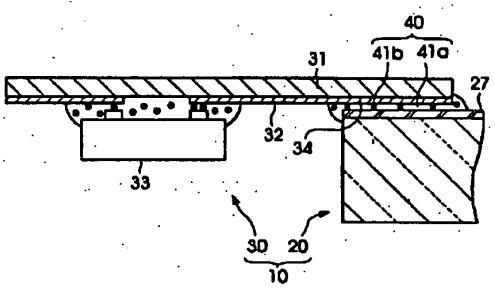
【符号の説明】

１０……電気光学装置
２０……表示基板
２２……信号線（第１配線）
２３，２３Ｒ……発光用電源配線（第２配線、電源線）
２４ａ……走査線駆動回路用制御信号配線（第１配線）
３０……中継基板
４０……異方性導電膜
５０……発光素子
５３……スイッチング素子
６６ａ，６６ｂ，６６ｃ……第２外部接続端子
６７，６８，６９，７０……第１外部接続端子
７９……凸部
Ｂ……凹部

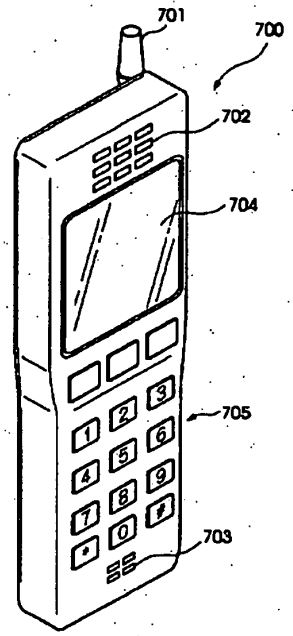
【図１】



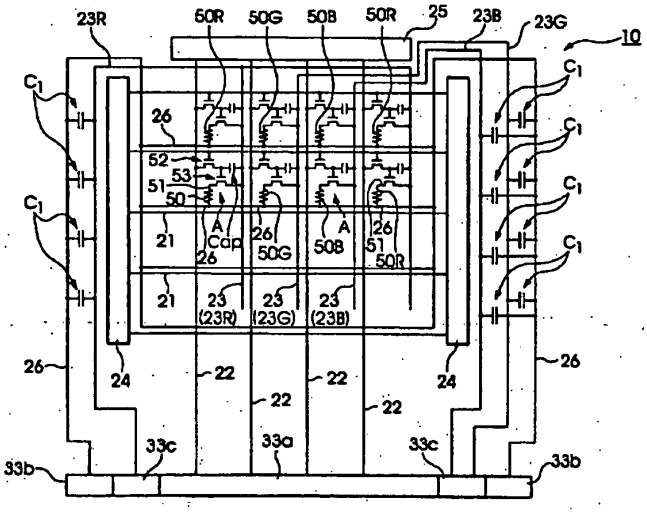
【図２】



【図１０】

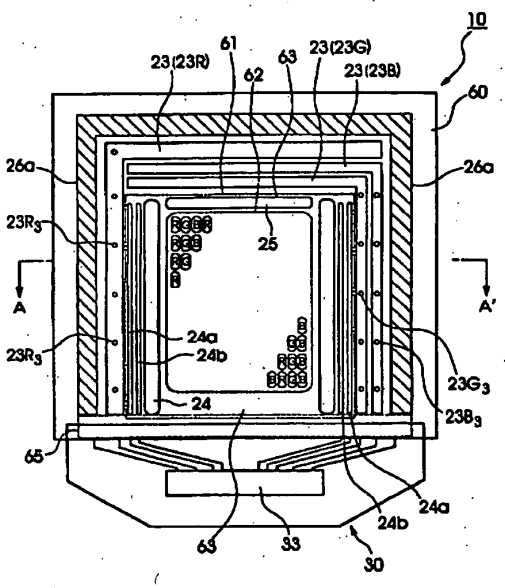


【図３】

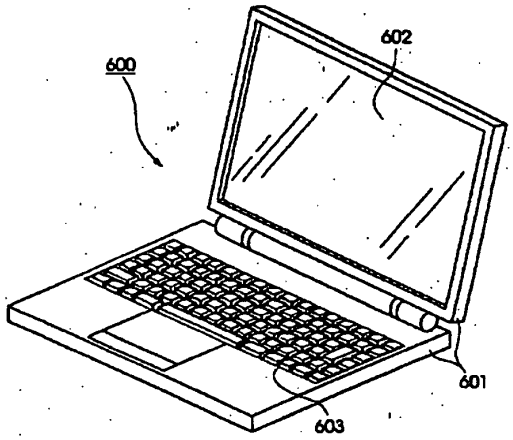


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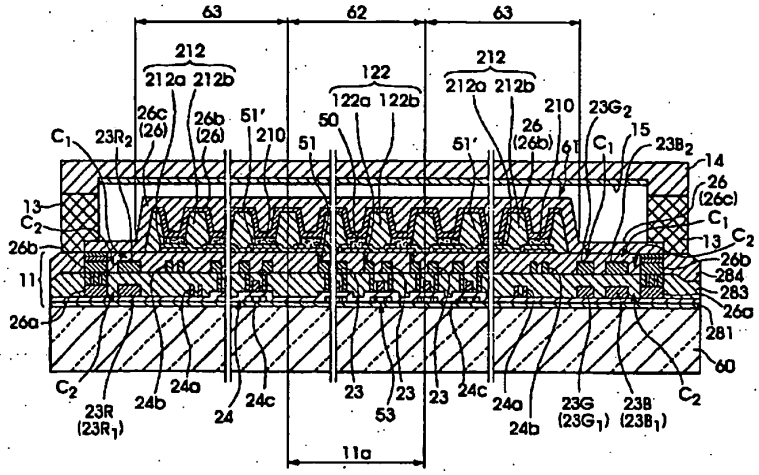
【図４】



【図９】

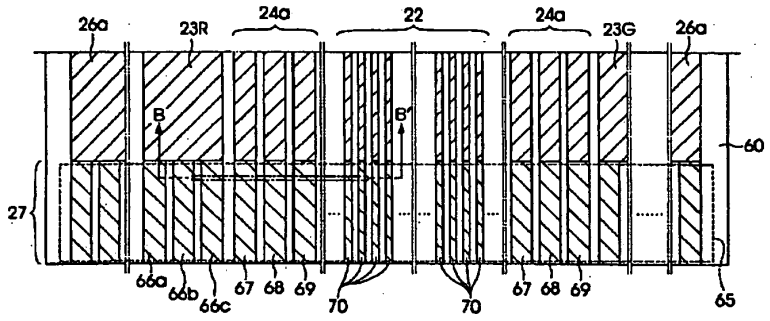


【図５】

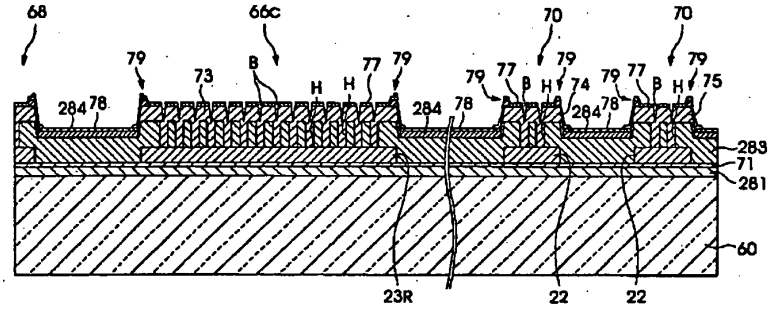


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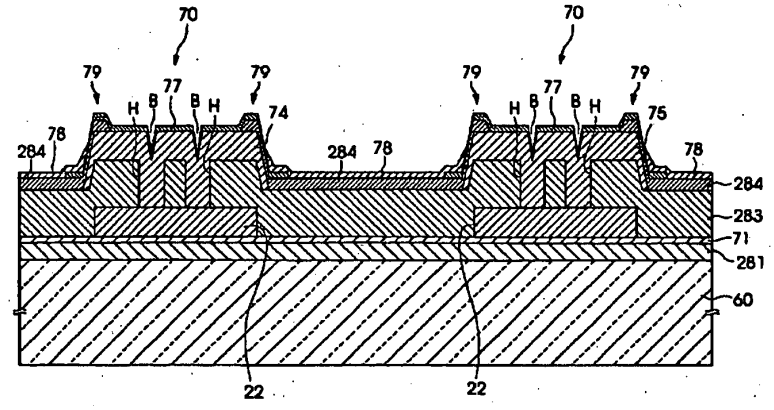
【図6】



【図7】

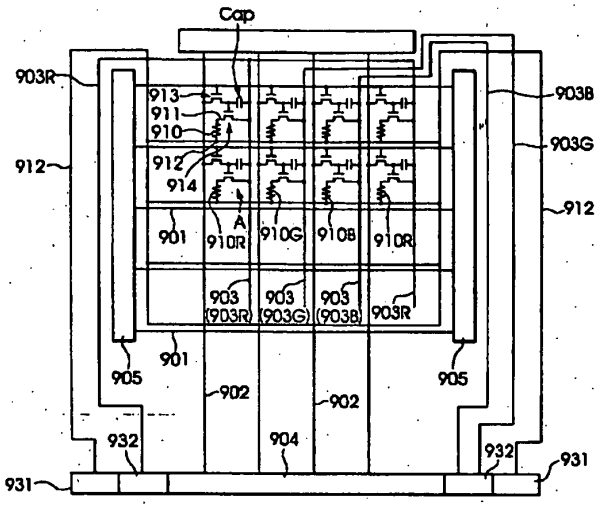


【図8】



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【図１１】



フロントページの続き

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H05K	1/14	H05K	1/14	C
	3/36		3/36	A

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2H092 GA33 GA40 GA48 GA50 HA18
HA26 JA24 NA01 NA25
3K007 AB17 CC05 DB03
5C094 AA03 BA29 CA19 CA24 DB03
EA10 FA01 FA04 HA08
5E344 AA02 AA12 AA22 BB02 BB04
BB12 BB13 BB15 CC14 CC17
CC23 CD04 CD14 DD06 EE06
EE23

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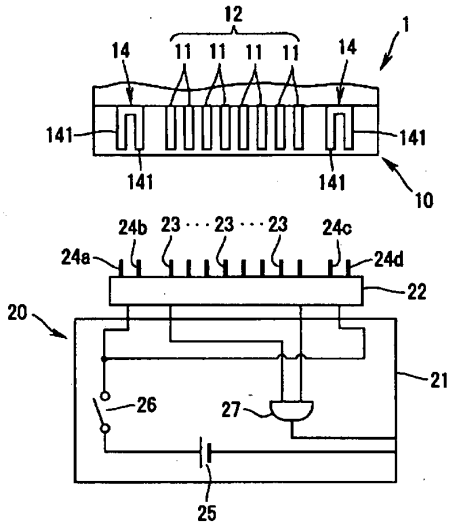
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(54)【発明の名称】　液晶表示パネルおよびその点灯検査方法

(57)【要約】
【課題】　位置ずれの有無を実際のプローブの接触状態で確認できるようにする。
【解決手段】　端子部１０に複数本のリード端子１１を含むリード端子群１２を備えている液晶表示パネル１を点灯検査するにあたって、端子部１０にピッチがリード端子群１２内の最小端子ピッチと同一、かつ、端子幅がリード端子群１２内の最小端子幅と同一であって、互いに導通している一対のずれ検出用のダミー端子１４１，１４１をリード端子群１２の両側に最小端子ピッチの整数倍の距離を置いて配置し、プローブヘッド２２側にダミー端子１４１，１４１に対応する各一対の電流プローブピン２４ａ，２４ｂ；２４ｃ，２４ｄを設け、リード端子１１の各々に点灯電圧を印加する前に、電流プローブピン２４ａ，２４ｂ；２４ｃ，２４ｄ間に導通チェック電流を流し、その導通・非導通により、位置ずれの有無を検出する。



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【特許請求の範囲】
【請求項１】　端子部に所定のピッチで配列された複数本のリード端子を含むリード端子群を備えている液晶表示パネルを検査対象とし、上記リード端子の各々に電圧プローブピンを接触させてチェックユニットより上記液晶表示パネルに所定の点灯電圧を印加してその点灯状態を検査する液晶表示パネルの点灯検査方法において、
上記端子部に、ピッチが上記リード端子群内の最小端子ピッチと同一、かつ、端子幅が上記リード端子群内の最小端子幅と同一であって、互いに導通するパターンとして形成されたずれ検出用の一対のダミー端子を上記リード端子群の両側に上記最小端子ピッチの整数倍の距離を置いて配置するとともに、
上記電圧プローブピンを保持するプローブヘッド側に、上記ダミー端子を介して導通チェック電流を流す各一対の電流プローブピンを設け、
上記電圧プローブピンおよび上記電流プローブピンを上記端子部に接触させたのち、上記電圧プローブピンから上記リード端子の各々に上記点灯電圧を印加するに先だって、上記電流プローブピン間に導通チェック電流を流し、その導通・非導通により、上記電圧プローブピンと上記リード端子との間の位置ずれの有無を検出することを特徴とする液晶表示パネルの点灯検査方法。
【請求項２】　上記一対のダミー端子が、互いに導通するＵ字状パターンとして形成されている請求項１に記載の液晶表示パネルの点灯検査方法。
【請求項３】　端子部に所定のピッチで配列された複数本のリード端子を含むリード端子群を備えている液晶表示パネルにおいて、
上記端子部には、ピッチが上記リード端子群内の最小端子ピッチと同一、かつ、端子幅が上記リード端子群内の最小端子幅と同一であって、互いに導通するパターンとして形成された一対のずれ検出用のダミー端子が、上記リード端子群の両側に上記最小端子ピッチの整数倍の距離を置いて配置されていることを特徴とする液晶表示パネル。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、液晶表示パネルおよびその点灯検査方法に関し、さらに詳しく言えば、端子部に形成されている各リード端子にプローブピンを同時に接触させて点灯電圧を印加する際のリード端子とプローブピン間の位置ずれ検出技術に関するものである。
【０００２】
【従来の技術】どの製品でも同じく組み立て後に最終な性能検査が行われるが、液晶表示パネルの場合には点灯検査がそれに該当する。液晶表示パネルの点灯検査は、端子部に形成されているリード端子にチェックユニットのプローブピンを接触させて所定の点灯電圧を印加し、その点灯状態によって透明電極の断線もしくは短絡の有無を検査する。

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【０００３】この点灯検査には、リード端子とプローブピンとの正確な位置合わせが要求される。例えば、ＴＦＴ液晶表示パネルにおいては、位置ずれによりリード端子を間違えて電圧をかけると、その電圧印加のタイミングによってはＴＦＴが破壊されることがある。そのため多くの場合、オートアライメント機構を有する検査装置が用いられている。
【０００４】この検査装置によると、液晶表示パネルに設けられているアライメントマークをＣＣＤカメラにて撮像し、その撮像信号を画像処理ユニットで処理して液晶表示パネルのリード端子位置を特定する。そして、その位置データに基づいてプローブピンもしくはパネルのいずれかを移動させて、リード端子とプローブピンとを位置合わせする。
【０００５】
【発明が解決しようとする課題】しかしながら、上記のオートアライメント機構を有する検査装置を含めて従来の検査装置は、位置合わせ後において、最終的に位置合わせ状態を確認する手段を備えていないため、信頼性に欠ける嫌いがあった。
【０００６】本発明は、上記課題を解決するためになされたもので、その目的は、リード端子に点灯電圧を印加するに先だって、リード端子とプローブピンの位置合わせ状態を、実際にプローブピンを接触させた状態で確実に検出することができる信頼性の高い液晶表示パネルの点灯検査方法を提供することにある。また、本発明の別の目的は、リード端子とプローブピンの位置合わせ状態を確実に検出することができる信頼性の高いずれ検出用のダミー端子を備えた液晶表示パネルを提供することにある。
【０００７】
【課題を解決するための手段】上記目的を達成するため、本願の第１発明は、端子部に所定のピッチで配列された複数本のリード端子を含むリード端子群を備えている液晶表示パネルを検査対象とし、上記リード端子の各々に電圧プローブピンを接触させてチェックユニットより上記液晶表示パネルに所定の点灯電圧を印加してその点灯状態を検査する液晶表示パネルの点灯検査方法において、上記端子部に、ピッチが上記リード端子群内の最小端子ピッチと同一、かつ、端子幅が上記リード端子群内の最小端子幅と同一であって、互いに導通するパターンとして形成されたずれ検出用の一対のダミー端子を上記リード端子群の両側に上記最小端子ピッチの整数倍の距離を置いて配置するとともに、上記電圧プローブピンを保持するプローブヘッド側に、上記ダミー端子を介して導通チェック電流を流す各一対の電流プローブピンを設け、上記電圧プローブピンおよび上記電流プローブピンを上記端子部に接触させたのち、上記電圧プローブピンから上記リード端子の各々に上記点灯電圧を印加する

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に先だって、上記電流プローブピン間に導通チェック電流を流し、その導通・非導通により、上記電圧プローブピンと上記リード端子との間の位置ずれの有無を検出することを特徴としている。

【０００８】本発明において、ずれ検出用の一対のダミー端子は導通していれば、その導通箇所はどこでもよいが、電流プローブピンの配設位置精度を考慮してリード端子と同じく短冊状であることが好ましく、また誤判定をなくすためには、互いに導通するＵ字状（もしくは逆Ｕ字状）パターンがよい。

【０００９】また、本願の第２発明は、端子部に所定のピッチで配列された複数本のリード端子を含むリード端子群を備えている液晶表示パネルにおいて、上記端子部には、ピッチが上記リード端子群内の最小端子ピッチと同一、かつ、端子幅が上記リード端子群内の最小端子幅と同一であって、互いに導通するパターンとして形成された一対のずれ検出用のダミー端子が、上記リード端子群の両側に上記最小端子ピッチの整数倍の距離を置いて配置されていることを特徴としている。

【００１０】

【発明の実施の形態】次に、図面を参照して、本発明の実施形態について説明する。図１に液晶表示パネル１の端子部１０の構成を示し、図２に端子部１０と点灯検査装置であるチェックユニット２０との相対位置関係を示す。

【００１１】端子部１０には、複数本のリード端子１１を含むリード端子群１２が設けられており、各リード端子１１は、液晶表示パネル１内の図示しない透明電極に接続されている。各リード端子１１は、透明電極と同じくＩＴＯ（インジウム・錫酸化物）よりなり、短冊状パターンとして形成されている。

【００１２】この実施形態において、各リード端子１１の端子間ピッチおよび端子幅はともに同一とされているが、そのいずれか一方もしくは双方が異なっている場合も、本発明の検査対象に含まれる。

【００１３】リード端子群１２の両側には、ずれ検出部１４，１４が設けられている。このずれ検出部１４，１４は同一構成であるため、その一方について説明すると、ずれ検出部１４は、一対のダミー端子１４１，１４１を備えている。

【００１４】ダミー端子１４１，１４１は、リード端子１１と同じくＩＴＯにより短冊状に形成されているとともに、短絡パターン１４２にて互いに導通されている。この実施形態において、短絡パターン１４２は、ダミー端子１４１，１４１の各一端側に配置されている。これにより、ずれ検出部１４は全体してＵ字状パターンを呈している。

【００１５】短絡パターン１４２は、端子部１０の基端部側（パネル表示部側）に配置され、かつ、その線幅Ｗ２は基端部から０．５ｍｍ以下であることが好ましい。

なお、変形例の一つとして、短絡パターン１４２をダミー端子１４１，１４１の中央に配置して、ずれ検出部１４をＨ字状パターンとしてもよい。

【００１６】ダミー端子１４１，１４１の端子幅Ｗ１は、リード端子１１の端子幅と同一幅である。なお、リード端子群１２に異なる端子幅のリード端子が含まれる場合には、その中の最小端子幅と同一とされる。

【００１７】また、ダミー端子１４１，１４１間のピッチＰ１は、リード端子１１，１１間のピッチと同一である。なお、リード端子群１２に異なるピッチのリード端子が含まれる場合には、その中の最小端子ピッチと同一とされる。

【００１８】ずれ検出部１４とリード端子群１２との間の距離Ｌも、本発明にとって重要な要素である。すなわち、この距離Ｌは、リード端子１１，１１間のピッチ（リード端子群１２に異なるピッチのリード端子が含まれる場合には、その中の最小端子ピッチ）の整数倍に設定される。

【００１９】なお、整数倍であることを条件として、リード端子群１２に対する図１の右側ずれ検出部１４と左側ずれ検出部１４の各距離Ｌを異ならせてもよい。例えば、図１の右側ずれ検出部１４の距離Ｌを端子間ピッチの２倍とし、左側ずれ検出部１４の距離Ｌを端子間ピッチの３倍としてもよい。

【００２０】図２を参照して、チェックユニット２０は、測定部２１とプローブヘッド２２とを備えている。プローブヘッド２２は、図示しない駆動手段により端子部１０に対して接近・離反するように動かされる。

【００２１】プローブヘッド２２には、各リード端子１１に対応して配置された点灯電圧印加用の電圧プローブ２３と、ずれ検出部１４に対応して配置され、その各ダミー端子１４１，１４１を介して導通チェック電流を流す各一対の電流プローブピン２４ａ，２４ｂ；２４ｃ，２４ｄとが設けられている。

【００２２】この実施形態において、測定部２１は、導通チェック用の電源である電池２５を有し、この電池２５の例えば正極側には、対をなす内のそれぞれ一方の電流プローブピン２４ａと電流プローブピン２５ｄとがスイッチ２６を介して接続されている。

【００２３】対をなすそれぞれ他方の電流プローブピン２４ｂと電流プローブピン２５ｃは、アンド回路２７の入力側に接続され、アンド回路２７の出力側は図示しない判定部に接続されている。なお、電圧プローブ２３に対する点灯電圧制御回路は本発明の要旨でないため、その図示を省略している。

【００２４】次に、本発明の動作について説明する。例えば、液晶表示パネル１０が図示しない位置合わせ用のＸ－Ｙ移動テーブルに載置され、オートアライメント機構などにより位置合わせが終了すると、本発明の点灯検査が行われる。

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【００２５】まず、プローブヘッド２２を下降させてすべてのプローブピン２３，２４を端子部１０に接触させる。そして、電圧プローブピン２３から各リード端子１１に点灯電圧を印加する前に、スイッチ２６をオンして電流プローブピン２４ａと電流プローブピン２５ｄとに電圧を加える。

【００２６】このとき、電流プローブピン２４ａ，２４ｂ；２４ｃ，２４ｄの各々が、ずれ検出部１４のダミー端子１４１，１４１に接触していれば、電流プローブピン２４ａ，２４ｂ間および電流プローブピン２４ｃ，２４ｄ間に電流が流れ、アンド回路２７の各入力側「Ｈ」となるため、アンド回路２７の出力が「Ｈ」となる。

【００２７】これにより、判定部にて位置ずれ「なし（ＯＫ）」と判定され、次のステップとして電圧プローブピン２３から各リード端子１１に点灯電圧が印加される。スイッチ２６をオンしても、アンド回路２７の出力が「Ｌ」のままであると、判定部にて位置ずれ「あり（ＮＧ）」と判定され、例えばブザーなどにより警告が発せられる。

【００２８】このように、本発明によれば、点灯電圧を印加する前に位置ずれの有無を実際のプローブの接触状態で確認できるため、信頼性の高い点灯検査を行うことができる。特に、ＴＦＴパネルの場合、間違った電圧印加によるＴＦＴの破壊を防止できるので好適である。

【００２９】なお、本明細書において、点灯電圧を印加するプローブピンを電圧プローブピン、導通チェック用のプローブピンを電流プローブピンとしているが、これは説明の都合上のものであって、実際には同じプローブピンが用いられている。

【００３０】

【発明の効果】以上説明したように、本発明によれば、端子部に複数本のリード端子を含むリード端子群を備えている液晶表示パネルを点灯検査するにあたって、端子

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部にピッチがリード端子群内の最小端子ピッチと同一、かつ、端子幅がリード端子群内の最小端子幅と同一であって、互いに導通している一対のずれ検出用のダミー端子をリード端子群の両側に最小端子ピッチの整数倍の距離を置いて配置するとともに、プローブヘッド側にダミー端子を介して導通チェック電流を流す各一対の電流プローブピンを設け、リード端子の各々に点灯電圧を印加する前に、電流プローブピン間に導通チェック電流を流し、その導通・非導通により、位置ずれの有無を検出するようにしたことにより、信頼性の高い液晶表示パネルの点灯検査を行うことができる。

【００３１】また、本発明によれば、リード端子とプローブピンの位置合わせ状態を確実に検出することができる信頼性の高いずれ検出用のダミー端子を備えた液晶表示パネルが提供される。

【図面の簡単な説明】

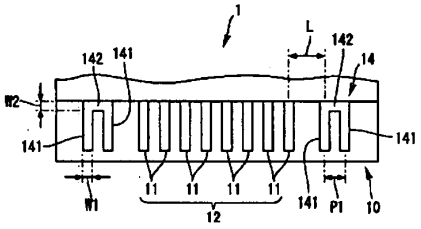
【図１】本発明の実施形態に係る液晶表示パネルの端子部を示した要部平面図。

【図２】上記液晶表示パネルとチェックユニットの相対位置関係を示す説明図。

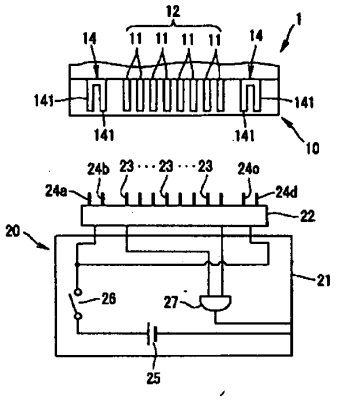
【符号の説明】

１　液晶表示パネル
１０　端子部
１１　リード端子
１２　リード端子群
１４　ずれ検出部
１４１　ダミー端子
１４２　短絡パターン
２０　チェックユニット
２１　測定部
２２　プローブヘッド
２３　電圧プローブピン
２４ａ～２４ｄ　電流プローブピン

【図１】



【図２】



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フロントページの続き

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NA30

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PAT-NO: JP02003043517A

DOCUMENT-IDENTIFIER: JP 2003043517 A

TITLE: LIQUID CRYSTAL DISPLAY PANEL AND LIGHTING INSPECTION METHOD THEREFOR

PUBN-DATE: February 13, 2003

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APPL-NO: JP2001231588

APPL-DATE: July 31, 2001

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ABSTRACT:

PROBLEM TO BE SOLVED: To make it possible to confirm the presence or absence of positional deviation by a contact state of an actual probe.

SOLUTION: To perform lighting inspection of a liquid crystal display panel 1 provided with a group of lead terminals 12 including a plurality of lead terminals 11 on a terminal part 10, the terminal part 10 is provided with a pairs of dummy terminals 141 for detecting the deviation, which are arranged at the same pitch as the minimum terminal pitch in the lead terminal group 12 and have the minimum terminal width in the lead terminal group 12 and are continuous with each other, on both sides of the lead terminal group 12 with a distance spaced by an integral multiple of the minimum terminal pitch; each pair of current probe pins 24a, 24b; 24c, 24d

corresponding to the dummy terminals 141, 141 is arranged on a probe head 22 side; a continuity check current is made to flow across the current probe pins 24a, 24b; 24c, 24d before applying lighting voltage to each of the lead terminal 11; and the presence or absence of the positional deviation is detected by the continuity or discontinuity.

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Notes:
1. Untranslatable words are replaced with asterisks (****).
2. Texts in the figures are not translated and shown as it is.

Translated: 05:34:06 JST 10/24/2007
Dictionary: Last updated 10/12/2007 / Priority:

[Document Name] Description

[Title of the Invention] A liquid-crystal-display panel and its lighting inspection method

[Claim(s)]

[Claim 1] A liquid-crystal-display panel equipped with the lead terminal group containing two or more lead terminals arranged by the terminal area in the predetermined pitch is made into a subject of examination. In the lighting inspection method of the liquid-crystal-display panel which a voltage probe pin is contacted to each of the above-mentioned lead terminal, impresses predetermined lighting voltage to the above-mentioned liquid-crystal-display panel from a check unit, and inspects the lighting state A pitch to the above-mentioned terminal area The minimum terminal pitch in the above-mentioned lead terminal group, and the same, And [a pair of dummy terminals for gap detection formed as a pattern through which terminal width flows / both sides] while placing and arranging the distance of the integral multiple of the above-mentioned minimum terminal pitch on both sides of the above-mentioned lead terminal group A pair each of current probe pins which send cable check current through the probe head side holding the above-mentioned voltage probe pin through the above-mentioned dummy terminal are prepared. After contacting the above-mentioned voltage probe pin and the above-mentioned current probe pin to the above-mentioned terminal area, precede impressing the above-mentioned lighting voltage to each of the above-mentioned lead terminal from the above-mentioned voltage probe pin, send cable check current between the above-mentioned current probe pins, and [its flow and un-flowing] The lighting inspection method of the liquid-crystal-display panel characterized by detecting the existence of the position gap between the above-mentioned voltage probe pin and the above-mentioned lead terminal.

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[Claim 2] The lighting inspection method of the liquid-crystal-display panel according to claim 1 currently formed as a U character-like pattern through which an above-mentioned pair of dummy terminals flow.

[Claim 3] In the liquid-crystal-display panel which it has, the lead terminal group containing two or more lead terminals arranged by the terminal area in the predetermined pitch [the above-mentioned terminal area] The pitch of the minimum terminal pitch in the above-mentioned lead terminal group, the same, and terminal width is the same as that of the minimum terminal width in the above-mentioned lead terminal group. The liquid-crystal-display panel characterized by a pair of dummy terminals for gap detection formed as a pattern which flows mutually keeping the distance of the integral multiple of the above-mentioned minimum terminal pitch from the both sides of the above-mentioned lead terminal group, and arranging them.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Concerning a liquid-crystal-display panel and its lighting inspection method in more detail, this invention relates to the position gap detection technology between the lead terminal at the time of contacting a probe pin for each lead terminal currently formed in the terminal area simultaneously, and impressing lighting voltage to it, and a probe pin.

[0002]

[Description of the Prior Art] Although performance inspection [same every product and last / after an assembly] is conducted, in the case of a liquid-crystal-display panel, lighting inspection corresponds at it. Lighting inspection of a liquid-crystal-display panel contacts the probe pin of a check unit for the lead terminal currently formed in the terminal area, impresses predetermined lighting voltage, and inspects disconnection of a transparent electrode or the

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existence of a short circuit according to the lighting state.

[0003] Exact position ****** of a lead terminal and a probe pin is required of this lighting inspection. For example, in a TFT-liquid-crystal display panel, when a lead terminal is mistaken by position gap and voltage is applied, TFT may be destroyed depending on the timing of the voltage impression. Therefore, in many cases, the inspection equipment which has an auto alignment mechanism is used.

[0004] According to this inspection equipment, the alignment mark prepared in the liquid-crystal-display panel is picturized with a CCD camera, that image pick-up signal is processed in the Image Processing Division unit, and the lead terminal position of a liquid-crystal-display panel is pinpointed. And either a probe pin or a panel is moved based on the position data, and position ****** of a lead terminal and the probe pin is carried out.

[0005]

[Problem to be solved by the invention] However, since it did not have means including the inspection equipment which has the above-mentioned auto alignment mechanism by which conventional inspection equipment finally checks a position ****** state after position ******, there was a tendency for reliability to be missing.

[0006] Were made in order that this invention might solve the above-mentioned technical problem, and [the purpose] It is in preceding impressing lighting voltage to a lead terminal, and offering the lighting inspection method of a liquid-crystal-display panel with high reliability which can detect certainly the position ****** state of a lead terminal and a probe pin where a probe pin is actually contacted. Moreover, another purpose of this invention is to offer the liquid-crystal-display panel equipped with the lead terminal and the dummy terminal for gap detection with high reliability which can detect the position ****** state of a probe pin certainly.

[0007]

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[Means for solving problem] In order to attain the above-mentioned purpose, [the 1st invention of an application concerned] A liquid-crystal-display panel equipped with the lead terminal group containing two or more lead terminals arranged by the terminal area in the predetermined pitch is made into a subject of examination. In the lighting inspection method of the liquid-crystal-display panel which a voltage probe pin is contacted to each of the above-mentioned lead terminal, impresses predetermined lighting voltage to the above-mentioned liquid-crystal-display panel from a check unit, and inspects the lighting state A pitch to the above-mentioned terminal area The minimum terminal pitch in the above-mentioned lead terminal group, and the same, And [a pair of dummy terminals for gap detection formed as a pattern through which terminal width flows / both sides] while placing and arranging the distance of the integral multiple of the above-mentioned minimum terminal pitch on both sides of the above-mentioned lead terminal group A pair each of current probe pins which send cable check current through the probe head side holding the above-mentioned voltage probe pin through the above-mentioned dummy terminal are prepared. After contacting the above-mentioned voltage probe pin and the above-mentioned current probe pin to the above-mentioned terminal area, precede impressing the above-mentioned lighting voltage to each of the above-mentioned lead terminal from the above-mentioned voltage probe pin, send cable check current between the above-mentioned current probe pins, and [its flow and un-flowing] It is characterized by detecting the existence of the position gap between the above-mentioned voltage probe pin and the above-mentioned lead terminal.

[0008] [a pair of dummy terminals for gap detection] in this invention if it has flowed Although the flow part is good anywhere, in order it is desirable that it is a strip of paper-like as well as a lead terminal and to lose an incorrect judging in consideration of the arrangement accuracy of position of a current probe pin, the U character-like (or inverted-L-shaped) pattern which flows mutually is good.

[0009] Moreover, the 2nd invention of an application concerned the lead terminal group containing two or more lead terminals arranged by the terminal area in the predetermined pitch in the liquid-crystal-display panel which it has [the above-mentioned terminal area] The pitch of the minimum terminal pitch in the above-mentioned lead terminal group, the same, and terminal width is the same as that of the minimum terminal width in the above-mentioned lead terminal group. It is characterized by a pair of dummy terminals for gap detection formed as a pattern which flows mutually keeping the distance of the integral multiple of the above-

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mentioned minimum terminal pitch from the both sides of the above-mentioned lead terminal group, and arranging them.

[0010]

[Mode for carrying out the invention] Next, the embodiment of this invention is explained with reference to Drawings. The composition of the terminal area 10 of the liquid-crystal-display panel 1 is shown in drawing 1, and the relative physical relationship of a terminal area 10 and the check unit 20 which is lighting inspection equipment is shown in drawing 2.

[0011] The lead terminal group 12 containing two or more lead terminals 11 is formed in the terminal area 10, and each lead terminal 11 is connected to the transparent electrode in the liquid-crystal-display panel 1 which is not illustrated. Each lead terminal 11 consists of ITO (indium and tin oxide) as well as a transparent electrode, and is formed as a strip-of-paper-like pattern.

[0012] In this embodiment, although both the pitches between terminals and terminal width of each lead terminal 11 are the same, also when those either or both sides is different, it is contained in the subject of examination of this invention.

[0013] The gap primary detecting elements 14 and 14 are formed in the both sides of the lead terminal group 12. Since these gap primary detecting elements 14 and 14 are the same composition, if one of these is explained, the gap primary detecting element 14 is equipped with a pair of dummy terminals 141,141.

[0014] The dummy terminal 141,141 has flowed mutually by the short circuit pattern 142 while being formed in the shape of a strip of paper of ITO as well as the lead terminal 11. In this embodiment, the short circuit pattern 142 is arranged at one one end each of the dummy terminal 141,141. Thereby, the whole of the gap primary detecting element 14 is carried out, and it is assuming the U character-like pattern.

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[0015] The short circuit pattern 142 is arranged at the end face part side (panel display part side) of a terminal area 10, and, as for the line width W2, it is desirable that it is 0.5mm or less from a end face part. In addition, as one of the modifications, the short circuit pattern 142 is arranged in the center of the dummy terminal 141,141, and it is good also considering the gap primary detecting element 14 as an H character-like pattern.

[0016] The terminal width W1 of the dummy terminal 141,141 is the same width as the terminal width of the lead terminal 11. In addition, when the lead terminal of terminal width which is different in the lead terminal group 12 is contained, it is supposed that it is the same as that of the minimum terminal width in it.

[0017] Moreover, the pitch P1 between the dummy terminals 141,141 is the same as that of the pitch between the lead terminals 11 and 11. In addition, when the lead terminal of a pitch which is different in the lead terminal group 12 is contained, it is supposed that it is the same as that of the minimum terminal pitch in it.

[0018] The distance L between the gap primary detecting element 14 and the lead terminal group 12 is an element important for this invention. That is, this distance L is set as the integral multiple of the pitch between the lead terminals 11 and 11 (when the lead terminal of a pitch which is different in the lead terminal group 12 is contained, it is the minimum terminal pitch in it).

[0019] In addition, on condition that it is an integral multiple, you may change each distance L of the right-hand side gap primary detecting element 14 of drawing 1 to the lead terminal group 12, and the left-hand side gap primary detecting element 14. For example, distance L of the right-hand side gap primary detecting element 14 of drawing 1 is made into twice the pitch between terminals, and it is good also considering the distance L of the left-hand side gap primary detecting element 14 as 3 times of the pitch between terminals.

[0020] The check unit 20 is equipped with the measurement part 21 and the probe head 22 with reference to drawing 2. The probe head 22 is moved so that approach and estrangement

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of may be done to a terminal area 10 by the drive means which is not illustrated.

[0021] The voltage probe 23 for lighting voltage impression arranged at the probe head 22 corresponding to each lead terminal 11, It is arranged corresponding to the gap primary detecting element 14, and a pair each of current probe pins 24a and 24b;24c which send cable check current through each of that dummy terminal 141,141, and 24d are prepared.

[0022] In this embodiment, the measurement part 21 has the battery 25 which is a power supply for cable checks, and the inner current probe pin 24a which is one side, respectively and the current probe pin 25d of this battery 25 which make a pair are connected to the plus terminal side through the switch 26.

[0023] It connects with the judgment [which makes a pair] part which the current probe pin 24b and the current probe pin 25c of another side are connected to the input side of the and circuit 27, and the output side of the and circuit 27 does not illustrate, respectively. In addition, since the lighting voltage control circuit to the voltage probe 23 is not the summary of this invention, it is omitting the illustration.

[0024] Next, operation of this invention is explained. For example, after being laid in the X-Y trolley table for position ****** which the liquid-crystal-display panel 10 does not illustrate and completing position ****** according to an auto alignment mechanism etc., lighting inspection of this invention is conducted.

[0025] First, the probe head 22 is dropped and all the probe pins 23 and 24 are contacted to a terminal area 10. And a switch 26 is turned on and voltage is applied to the current probe pin 24a and the current probe pin 25d, before impressing lighting voltage to each lead terminal 11 from the voltage probe pin 23.

[0026] If the current probe pin 24a, 24b;24c, and 24d each touch the dummy terminal 141,141 of the gap primary detecting element 14 at this time Since current flows between the current probe pin 24a and 24b and between the current probe pin 24c and 24d and it becomes each

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input side "H" of the and circuit 27, the output of the and circuit 27 is set to "H."

[0027] thereby -- a judgment part -- a position gap -- "-- it is judged with nothing (O.K.)", and lighting voltage is impressed to each lead terminal 11 from the voltage probe pin 23 as a following step. even if it turns on a switch 26, the output of the and circuit 27 continues being "L" -- a judgment part -- a position gap -- "-- it is, and is judged with (NG)", for example, warning is emitted at a buzzer etc.

[0028] Thus, since according to this invention the existence of a position gap can be checked in the state of contact of an actual probe before impressing lighting voltage, reliable lighting inspection can be conducted. Since the destruction of TFT by the wrong voltage impression can be prevented especially in the case of the TFT panel, it is suitable.

[0029] In addition, in this Description, although the voltage probe pin and the probe pin for cable checks are used as the current probe pin for the probe pin which impresses lighting voltage, this is a thing on account of explanation, and the same probe pin is used in fact.

[0030]

[Effect of the Invention] In conducting lighting inspection of the liquid-crystal-display panel equipped with the lead terminal group which contains two or more lead terminals in a terminal area according to this invention, as explained above The pitch of the minimum terminal pitch in a lead terminal group, the same, and terminal width is the same as that of the minimum terminal width in a lead terminal group to a terminal area. [a pair of dummy terminals for gap detection which have flowed mutually] while placing and arranging the distance of the integral multiple of the minimum terminal pitch on both sides of a lead terminal group Before preparing a pair each of current probe pins which send cable check current through the probe head side through a dummy terminal and impressing lighting voltage to each of a lead terminal, send cable check current between current probe pins, and [its flow and un-flowing] By having detected the existence of the position gap, lighting inspection of a reliable liquid-crystal-display panel can be conducted.

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[0031] Moreover, according to this invention, the liquid-crystal-display panel equipped with the lead terminal and the dummy terminal for gap detection with high reliability which can detect the position ****** state of a probe pin certainly is offered.

[Brief Description of the Drawings]

[Drawing 1] The important section top view showing the terminal area of the liquid-crystal-display panel concerning the embodiment of this invention.

[Drawing 2] The explanatory view showing the relative physical relationship of the above-mentioned liquid-crystal-display panel and a check unit.

[Explanations of letters or numerals] 1 Liquid-Crystal-Display Panel 10 Terminal Area 11 Lead terminal 12 Lead terminal group 14 Gap primary detecting element 141 Dummy terminal 142 Short circuit pattern 20 Check unit 21 Measurement part 22 Probe head 23 Voltage probe pins 24a-24d Current probe pin

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[Translation done.]

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Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /BAO-QUAN T HO/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	8	14	2

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TITLE
Electro-optical panel, electro-optical apparatus, and electronic system

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/24/2007								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

SEARCHED			
Class	Subclass	Date	Examiner
345	60-100, 690-699, 204-213	10/02/07	BTH
349		10/02/07	BTH

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5	electro$1optical same grayscale same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/09/28 07:25
S2	144	electro$1optical and grayscale and terminal and frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/09/28 07:26
S3	69920	"345".clas.	US-PGPUB; USPAT	AND	ON	2007/09/28 07:26
S4	70	S2 S3	US-PGPUB; USPAT	AND	ON	2007/09/28 08:13
S5	39106	(first and second) same (higher or lower or greater or less$3 or least or more) same resistance same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 11:24
S7	64288	(first and second) same resistance same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 08:21
S8	498	S3 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 08:34
S9	1067	(driv$3 and imag$3) near signal same frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 09:39

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S10	1390	345/690.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 08:38
S11	5	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 08:38
S12	137	(driv$3 and imag$3) near (signal or line) same gray$1scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 09:55
S13	1423	((driv$3 or gate) near (terminal)) and ((img$3 or source) near terminal) same frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:44
S14	0	S10 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:43
S15	20	S3 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:43
S16	1967	((driv$3 or gate) near (terminal or signal or line)) and ((img$3 or source) near terminal) same frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:49

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S17	24	S3 S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:45
S18	0	S10 and S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 10:45
S19	851	((driv$3 or gate) near (terminal or signal or line)) and ((img$3 or source) near terminal) same (frequency near2 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 15:32
S20	1	((driv$3 or gate) near (terminal or signal or line)) and ((img$3 or source) near terminal) same (frequency near2 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 11:20
S21	439	((driv$3 or gate or select) same (img$3 or source or data)) same (frequency near2 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 11:33
S22	182	S3 and S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 11:23
S23	600	((driv$3 or gate or select or scan or scanning) same (img$3 or source or data)) same (frequency near2 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 07:45

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EAST Search History

S24	850	((driv$3 or gate or select or scan or scanning or horizontal) same (img$3 or source or data or vertical)) same (frequency near2 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/09/28 11:45
S25	1	("20050057467").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/01 07:43
S26	742	((driv$3 or gate or select or scan or scanning) same (img$3 or source or data)) same (area near3 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 07:46
S27	45	((driv$3 or gate or select or scan or scanning) same (img$3 or source or data)) same (area near3 (different or larg$3 or small$3 or less$3 or big$3 or high$3 or low$3)) and gray$scale and (frequency adj component)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 08:04
S28	1	("6697040").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/01 08:04
S29	38624	(first and second) same (higher or lower or greater or less$3 or least or more) same frequency same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 07:55
S30	681747	display adj (device or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 08:19

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S31	971	S29 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 08:19
S32	3	("5274483" | "5283565" | "6525718").PN. OR ("6842164"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/01 10:49
S33	7	("5745087" | "5748164" | "6160535" | "6169532").PN. OR ("6483493").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/01 11:28
S34	10	("5745087" | "5748164" | "6160535" | "6169532").PN. OR ("6262702").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/01 11:32
S35	18	("5565885" | "5598283" | "5670994" | "5731854" | "5739887" | "5838412" | "5893623" | "6104464" | "6147739").PN. OR ("6525718").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/01 16:04
S36	48	high adj frequency adj component near3 (scan or scanning or gate) adj (line or signal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/01 16:06
S37	430355	frequency near3 (bigger or higher or lower or greater or less$2 or different)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 13:19
S38	107716	area near5 (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 13:57
S39	83477	(flat adj (panel or display))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 08:03

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S40	929225	(gray$1scale or intensity or grey$1scale or half$1tone or gradation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 08:04
S41	16493	345/60-100.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 08:04
S42	2491	345/690-699.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 08:05
S44	8455	345/204-213.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 08:08
S45	74	S37 S38 S39 S40	US-PGPUB; USPAT	AND	ON	2007/10/02 08:30
S46	3	S45 and (S41 or S42 or S44)	US-PGPUB; USPAT	AND	ON	2007/10/02 08:11
S47	98510	((driver or signal or line) near2 (gate or scan or scanning or select)) same ((driver or signal or line) near2 (data or source or image))	US-PGPUB; USPAT	AND	ON	2007/10/02 08:31
S48	10	S37 S38 S39 S40 and S47	US-PGPUB; USPAT	AND	ON	2007/10/02 08:31
S49	917	S37 same S47	US-PGPUB; USPAT	AND	ON	2007/10/02 08:31
S50	200	S37 same S47 and (S41 or S42 or S44)	US-PGPUB; USPAT	AND	ON	2007/10/02 08:36
S51	135474	((driver or signal or line) near2 (gate or scan or scanning or select)) same ((driver or signal or line) near2 (data or source or image))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 08:32
S52	1	("6742762").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/02 08:43
S53	1	("6249325").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/02 08:43

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S56	1	("20020180673").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/02 11:02
S57	1	("20050057467").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/02 12:32
S58	908	forth near4 (terminal or pad) same area	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/02 11:56
S59	7	S58 and (S41 or S42 or S44)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/02 11:56
S60	1436	fourth near4 (terminal or pad) same area	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/02 11:56
S62	32	S60 and (S41 or S42 or S44)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/02 11:57
S63	13	("5093655" | "5168270" | "5414443" | "5748165" | "6028587" | "6147667" | "6157358" | "6331844" | "6424328" | "6429838" | "6603465" | "6693616" | "6717179").PN. OR ("7259740"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/02 12:16
S64	308091	(printed adj circuit adj board) or PCB or (dlexible adj printed adj circuit adj board) or FCB	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 12:17

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S66	218310	(first and second and third) same (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 12:27
S67	14125	S64 S66	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 12:28
S68	431	S67 and "345".clas.	US-PGPUB; USPAT	AND	ON	2007/10/02 12:29
S69	215	S68 and S51	US-PGPUB; USPAT	AND	ON	2007/10/02 12:29
S70	4	S37 S38 S39 S40 S51 S64 S66	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/02 13:18
S71	1624	349/149-152.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/02 13:18
S72	14	S37 S38 S71	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/02 13:19
S73	1629	349/149-152.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/15 15:00
S74	4700	higher adj frequency adj component	US-PGPUB; USPAT	AND	ON	2007/10/15 11:15
S75	0	S73 S74	US-PGPUB; USPAT	AND	ON	2007/10/15 11:14
S76	38	higher adj frequency adj component same (input adj signal) same terminal	US-PGPUB; USPAT	AND	ON	2007/10/15 11:21
S77	343405	(four or fourth or third or three) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:49

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S78	539	S73 S77	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 11:24
S79	117428	(higher or lower or greater or less$3 or least or more) same frequency same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 11:25
S80	1	S73 and S77 same S79	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 11:25
S81	17	S73 and S77 and S79	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 11:26
S82	4	("20020171638" | "6011607" | "6531996" | "6979839").PN. OR ("7116390").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/15 13:54
S83	889187	frequency near2 (big$4 or high$4 or great$4 or least or less$4 or different or larg$4 or small$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 16:30
S84	108101	area near5 (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 13:58

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S85	2485521	(flat adj panel) or display	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 12:43
S86	16580	345/60-100.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/15 13:59
S87	2504	345/690-699.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/15 14:00
S88	8492	345/204-213.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/15 14:00
S89	301	S83 same S84 and S85	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:03
S90	5	(S83 same S84 and S85).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:02
S91	4	S83 same S84 and S85 and (S86 or S87 or S88)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:04
S92	3233168	(terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:49
S93	12475	S92 same S83 and S85	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:50

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S94	5067	S92 with S83 and S85	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:50
S95	602	(S92 same S83 and S85).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 14:52
S97	27128	"349".clas.	US-PGPUB; USPAT	AND	ON	2007/10/15 14:52
S98	70333	"345".clas.	US-PGPUB; USPAT	AND	ON	2007/10/15 14:52
S99	0	S95 S97	US-PGPUB; USPAT	AND	ON	2007/10/15 14:52
S100	21	S95 S98	US-PGPUB; USPAT	AND	ON	2007/10/15 14:52
S101	156	frequency and resist$4 and S73	US-PGPUB; USPAT	AND	ON	2007/10/15 15:15
S102	1	("20050057467").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/15 15:15
S103	147	masao near1 murade and matrix	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 15:32
S104	147	(masao near1 murade).in. and matrix	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 15:33

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S105	130	(masao near1 murade).in. and electro-optical	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 15:33
S106	88	(masao near1 murade).in. and electro-optical	US-PGPUB; USPAT	AND	ON	2007/10/15 15:34
S107	113	(masao near1 murade).in. and terminal	US-PGPUB; USPAT	AND	ON	2007/10/15 15:34
S108	84	(masao near1 murade).in. and (external near3 terminal)	US-PGPUB; USPAT	AND	ON	2007/10/15 16:18
S109	20	(masao near1 murade).in. and (external near3 terminal) and (frequency near2 (big$4 or high$4 or great$4 or least or less$4 or different or larg$4 or small$4))	US-PGPUB; USPAT	AND	ON	2007/10/15 16:20
S110	4271	((scanning or scan$2 or drive or driv$4 or gate) adj2 (signal or circuit or line or level or device)) near3 frequency near2 (big$4 or high$4 or great$4 or larg$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 16:36
S111	253	S110 and (S86 or S87 or S88)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 16:34
S112	865	((scanning or scan$2 or gate) adj2 (signal or circuit or line or level or device)) near3 frequency near2 (big$4 or high$4 or great$4 or larg$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/15 16:37
S113	68	S112 and (S86 or S87 or S88)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 12:41

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S114	484	(terminal adj area) near3 (big$4 or high$4 or great$4 or least or less$4 or different or larg$4 or small$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:24
S115	2486424	(flat adj panel) or display	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 12:44
S116	98	S114 S115	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 12:48
S117	375	(terminal adj area) near3 (big$4 or high$4 or great$4 or less$4 or different or larg$4 or small$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:52
S118	77	S117 S115	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:26
S119	1312	((terminal or pad) adj area) near3 (big$4 or high$4 or great$4 or less$4 or different or larg$4 or small$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:54
S120	234	S119 S115	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:53

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S121	938	((pad) adj area) near3 (big$4 or high$4 or great$4 or less$4 or different or larg$4 or small$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 13:54
S122	157	S115 S121	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/16 15:49
S123	1	("5870163").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/16 15:49
S124	14	("4297004" | "4838656" | "5499131" | "5670994").PN. OR ("5870163").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 08:22
S125	1	("6424400").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/17 08:22
S126	14	("5592365" | "6144216" | "6320691").PN. OR ("6424400"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 08:23
S127	9	("5402255" | "5592199" | "5670994" | "5737053" | "6424400" | "6437764" | "6519020" | "6864941").PN. OR ("7002812"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 08:27
S129	4	pitch and S127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 08:52
S132	2	(("6618111") or ("20040169645")). PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/17 09:14

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S133	1	("6198522").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/17 09:18
S134	1	("6052171").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/17 09:18
S135	449	terminal adj (size or region or area or width or length) and ("349".clas. or "345".clas.)	US-PGPUB; USPAT	AND	ON	2007/10/17 09:58
S136	5	("20030076460" | "20040141137" | "6781162" | "6946802" | "6999150").PN. OR ("7129645"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 09:39
S137	12	("20020113246" | "20020173178" | "20030209786" | "5995088" | "6184585" | "6424092" | "6518962" | "6809390" | "6809411" | "6822164" | "6861279").PN. OR ("6946802").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 09:46
S138	71	terminal adj (size or region or area or width or length) near3 (width or length) and ("349".clas. or "345". clas.)	US-PGPUB; USPAT	AND	ON	2007/10/17 10:29
S139	6	terminal adj (size or region or area or width or length) near3 (width or length) with (resistance or frequency) and ("349".clas. or "345".clas.)	US-PGPUB; USPAT	AND	ON	2007/10/17 10:32
S140	68	terminal adj (size or region or area or width or length) near3 (width or length) with (resistance or frequency)	US-PGPUB; USPAT	AND	ON	2007/10/17 10:42
S141	34	terminal adj (size or region or area or width or length) near3 (width or length) with (frequency)	US-PGPUB; USPAT	AND	ON	2007/10/17 10:47
S142	36	terminal adj (size or region or area or width or length) near3 (width or length) with (resistance)	US-PGPUB; USPAT	AND	ON	2007/10/17 10:47
S143	6	("20020044251" | "20020109814" | "5488498" | "6493056" | "6664942" | "6724456").PN. OR ("7002657"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 10:58

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S144	1	("6780055").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/17 13:27
S145	5	"439".clas. and (terminal or pad) near3 (wide or wider or larger or large) with frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 13:30
S146	3867	"439".clas. and (terminal or pad) near3 (wide or wider or larger or large)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 13:30
S147	2620	"439".clas. and ((terminal or pad) near2 (wide or wider or larger or large))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 13:30
S148	173	"439".clas. and ((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:07
S149	84	"439".clas. and ((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2)) and @ad<"20030101"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:08
S150	84	"439".clas. and ((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2)) and @ad<"20030108"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:11
S151	27	"345".clas. and ((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2)) and @ad<"20030108"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:11

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S152	20	"349".clas. and ((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2)) and @ad<"20030108"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:43
S153	11	((terminal or pad) near2 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2) near3 frequency) and @ad<"20030108"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:46
S154	35	((terminal) near4 (wide or wider or larger or large) with (reduce or reduced or increas$2 or decreas$2) near3 frequency) and @ad<"20030108"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/17 14:47
S155	16	("5349226" | "5453991" | "5473261").PN. OR ("5945984"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/17 15:02
S156	1	("20050057467").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/18 13:35
S157	1717	345/100.ccls.	US-PGPUB; USPAT	AND	ON	2007/10/18 13:36
S158	1094	(scanning or scan or gate) adj3 (circuit or line or driv$4) near4 ((high$4 or great$4 or larg$4) near2 (frequency))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 14:24
S159	22	S157 S158	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 13:39
S160	134	(scanning or scan or gate) adj3 (circuit or line or driv$4) near4 (high adj frequency adj component)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 14:52

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S16 1	0	signal near3 dull near4 flexible	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 14:53
S16 2	40	signal same dull same flexible	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 15:20
S16 3	77	((high or higher) adj frequency adj component)and "349".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 16:21
S16 4	796	((high or higher) adj frequency adj component)and "345".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 16:25
S16 5	9	((scanning or scan or gate) adj3 (high or higher) adj frequency adj component)and "345".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/18 16:25
S16 6	1	("4609256").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/22 07:53
S16 7	282	(drive or driving or scan or scanning or gate) near4 (high adj frequency adj (component or content)) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 08:40

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S168	1384	(image or data or source) near4 (low adj frequency adj (component or content)) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 13:18
S169	314	pitch near5 (integer adj multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 13:57
S170	1	(pitch with terminal) near5 (integer adj multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 13:57
S171	1	(pitch near5 terminal) near5 (integer adj multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 13:58
S172	4	pitch same terminal same (integer adj multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:00
S173	44	pitch same terminal same (flexible adj substrate) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:20
S174	9	("5402255" | "5592199" | "5670994" | "5737053" | "6424400" | "6437764" | "6519020" | "6864941").PN. OR ("7002812"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/22 14:17
S175	467	pitch same terminal same (scal$2 or uniform$4 or integer) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:22

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S176	79	(select or scan or scanning or gate or driving or drive) same (data or image or source) same pitch same terminal same (scal$2 or uniform$4 or integer) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:27
S177	10	((pitch or pitches) near4 terminal) near4 (scal$2 or uniform$4 or integer or multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:29
S178	22	((pitch or pitches) near4 terminal) near4 (scal$2 or uniform$4 or integer or multiple or relation$4) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:45
S179	1344	((pitch or pitches) near4 (scal$2 or uniform$4 or integer or multiple or relation$4)) and (print$2 adj2 circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 14:47
S180	70504	"345".clas.	US-PGPUB; USPAT	AND	ON	2007/10/22 14:47
S181	27193	"349".clas.	US-PGPUB; USPAT	AND	ON	2007/10/22 14:47
S182	14	S179 S180	US-PGPUB; USPAT	AND	ON	2007/10/22 14:48
S183	20	S179 S181	US-PGPUB; USPAT	AND	ON	2007/10/22 14:57
S184	1012	pitch with (integral adj multiple)	US-PGPUB; USPAT	AND	ON	2007/10/22 14:58
S185	432	pitch with (integral adj multiple) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/10/22 15:28
S186	1	("6750924").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/22 15:31

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S187	685	terminal near3 (spac$4 or separat$4) near4 (scal$2 or uniform$4 or integer or multiple or relation$4) and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 15:36
S188	11	S180 S187	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 15:42
S189	3	S181 S187	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 15:36
S193	1	("6157870").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/22 15:55
S194	1	("4127432").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/22 15:58
S195	1	("6459161").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/22 15:58
S196	740	"349".clas. and (pitch near4 arrang$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:03
S197	138	"349".clas. and (pitch near4 arrang$4) same (first and second)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:02

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S198	3	"349".clas. and (pitch near4 arrang$4) same (first and second) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:02
S199	12	"349".clas. and (pitch near4 arrang$4) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:25
S200	4	"349".clas. and (pitch near3 (length or width)) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:31
S201	6	"345".clas. and (pitch near3 (length or width)) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:38
S202	113	structur$2 same pitch same terminal same (integral or integer) same (arrang$4 or setup)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 16:49
S203	405	pitch same terminal same (integral or integer) same (arrang$4 or setup)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 17:02
S204	42	(driving and image) adj3 signal same pitch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 17:08
S205	2	(driving and image) adj3 signal same pitch same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 17:09

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S206	3	(driving and image) adj3 (signal or line) same pitch same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/22 17:12
S207	146	((driving or drive or gate or scan or scanning) and (source or data or image)) adj3 (signal or line) same pitch same terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 07:49
S208	90	((driving or drive or gate or scan or scanning) and (source or data or image)) adj3 (signal or line) same pitch same ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:18
S209	513	pitch same ((first and second) near2 (signal or line)) same (multiple or ratio or scal$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:19
S210	9	("5402255" | "5592199" | "5670994" | "5737053" | "6424400" | "6437764" | "6519020" | "6864941").PN. OR ("7002812"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/23 08:19
S211	803	pitch same ((first and second) near2 (signal or line)) same (multiple or ratio or scal$4 or relation or relationship)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:26
S212	7257	pitch same (signal or line) same (multiple or ratio or scal$4 or relation or relationship) and (display)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:27
S213	2384	pitch same (signal or line) same (multiple or ratio or scal$4 or relation or relationship) and (substrate and display)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:28

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S214	726	pitch same (signal or line) same (multiple or ratio or scal$4 or relation or relationship) and (substrate and display and board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:16
S215	819	pitch same (signal or line or wire or terminal) same (multiple or ratio or scal$4 or relation or relationship) and (substrate and display and board)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 08:28
S216	20	("5671030" | "5757450" | "5818563" | "5893624" | "5982470").PN. OR ("6172732"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/23 10:01
S217	11	(pitch or pitches) near4 (relation or relationship) near4 (multiple near1 integer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:20
S218	67	(pitch or pitches) near4 (arrang$2 or setup or plac$2 or structur$2 or form$2) near4 (multiple near1 integer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 13:39
S219	9	(pitch or pitches) near4 (layout) near3 integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:35
S220	40	((pitch or pitches) near4 (layout)) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:38
S222	120	((pitch or pitches) near4 (structur$2)) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:40

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S223	271	((pitch or pitches) near4 (width)) same integer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 10:40
S224	243	(pitch or pitches) near4 (arrang$2 or setup or place$4 or structur$2 or form$2) near4 (integer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 14:06
S225	14	("5737272").URPN.	USPAT	AND	ON	2007/10/23 13:53
S226	19	("4613855" | "4655551" | "4758896" | "4907128" | "5029984").PN. OR ("5737272"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/10/23 13:53
S227	54712	(terminal near1 spac$4 or gap) near4 width	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 14:12
S228	10380	S227 and (display or panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 14:10
S229	698	S228 and "349".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 14:10
S230	92	(terminal near1 (spac$4 or gap)) near4 width	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	ON	2007/10/23 14:12
S231	1	("6697040").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/10/23 15:56

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PTO/SB/21 (03-07)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/914,044
Filing Date	March 6, 2004
First Named Inventor	Shin Fujita
Art Unit	4131
Examiner Name	Bao-Quan T. Ho
Total Number of Pages in This Submission	Attorney Docket Number: 9319S-000838/US

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
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- ☐ Petition to Convert to a Provisional Application
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- ☐ CD, Number of CD(s) ____
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- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
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Remarks: The Commissioner is hereby authorized to charge any additional fees that may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 50-3213. A duplicate copy of this sheet is enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name G. Gregory Schivley Bryant E. Wade	Reg. No. 27,382 40,344
Signature			
Date	January 31, 2008		

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	March 6, 2004
Applicant:	Shin Fujita
Group Art Unit:	4131
Examiner:	Bao-Quan T. Ho
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Mail Stop Amendment
Director of The United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed November 2, 2007, please amend the application as follows and consider the remarks set forth below.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a ~~first~~ clock signal input terminal supplied with a ~~first input~~ scanning line clock signal;

~~a second~~an image signal input terminal supplied with ~~a second input~~ an image signal;[[and]]

a scanning line drive circuit that sequenctially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals;

a drive circuit which controls a grayscale of the pixels based on the ~~first and the second input signals~~scanning line clock signal and the image signal; and

a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,

wherein ~~the first input signal includes a higher frequency component compared with the second input signal, and~~ the ~~first~~ clock signal input terminal has a larger area than the ~~second~~ image signal input terminal, and

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wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included;

the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.

2. (Currently Amended) An electro-optical panel according to Claim 1, wherein the first ~~input terminal~~clock signal input terminal has a smaller input resistance compared with the ~~second~~ image signal input terminal.

3. (Currently Amended) An electro-optical panel according to Claim 1, wherein a signal supplied to the ~~first~~ clock signal input terminal comprises a driving signal supplied to [[a]]the scanning-line drive circuit.

4. (Cancelled).

5. (Currently Amended) An electro-optical panel according to Claim 1, wherein the ~~first~~ clock signal input terminal and the ~~second~~ image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the ~~second~~ image signal input terminal is disposed in the central part of the substrate, and the ~~first~~ clock signal input terminal is disposed at the outer side of the substrate.

6. (Cancelled).

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7. (Currently Amended) An electro-optical panel according to Claim 6, wherein the third input terminal includes a plurality of adjacent terminals of at least one of the ~~first~~ clock signal input terminal and the ~~second~~ image signal input terminal.

8. (Cancelled).

9. (Currently Amended) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 1;

power source means for supplying the power source; and

signal generation means for supplying the input signals.

10. (Currently Amended) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 9;

an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate which connects the external substrate and the electro-optical panel,

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of ~~first~~ clock signal input terminals and the plurality of ~~second~~ image signal input terminals through an anisotropic conductive film.

11. (Currently Amended) An electro-optical apparatus according to Claim 10, wherein wiring lines are formed corresponding to a reference pitch interval of the ~~second~~ image signal input terminals on the flexible substrate.

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12. (Currently Amended) An electro-optical panel comprising:

a plurality of data lines on a substrate;

a plurality of scanning lines on the substrate and intersecting the plurality of data lines;

an image display area on the substrate which includes a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a scanning-line drive circuit for driving the pixels;

a data-line drive circuit for supplying data signals to the pixels; and

an input terminal group for supplying signals to the scanning-line drive circuit and the data-line drive circuit,

wherein the scanning-line drive circuit is disposed along one side of the substrate on the substrate, the data-line drive circuit is disposed along a side which is not opposed to the one side on the substrate, the input terminal group is disposed along the data-line drive circuit and is disposed at a further edge side of the substrate than the data-line drive circuit; and

the input terminal group has a first input terminal ~~group~~ for supplying a driving signal to the scanning-line drive circuit and a second input terminal ~~group~~ for supplying an image signal to the data-line drive circuit, the second input terminal is disposed in the central part of the input terminal group, the first input terminal is disposed at the outer side of the input terminal group based on size of the first input terminal relative to size of the second input terminal, and the first input terminal has a larger area than the second input terminal based on frequencies of signals transmitted on the first input terminal and the second input terminal.

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13. (Original) An electro-optical panel according to Claim 12, further comprising a fourth input terminal for supplying a driving signal to the data-line drive circuit, wherein the fourth input terminal has an area equal to an area of the first input terminal, and the fourth input terminal is disposed between the first input terminal and the second input terminal.

14. (Original) An electronic system comprising the electro-optical apparatus set forth in Claim 1.

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REMARKS

Claims 1-14 are now pending in the application. Claims 4, 6 and 8 are cancelled. Claims 1-3 and 5-12 are amended herein. Applicant has amended the claims to expedite prosecution. Applicant reserves the right to pursue the claims as originally filed in one or more continuing applications. Support for the amendments to the claims can be found throughout the drawings and specification. As such, no new matter is added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murade (U.S. Pat. No. 6,262,702) in view of Hirosue et al. (U.S. Pat. No. 7,002,657). This rejection is respectfully traversed.

With respect to Claim 12, Murade and Hirosue do not show, teach or suggest an electro-optical panel that includes an input terminal group that supplies signals to a scanning-line drive circuit and a data-line drive circuit, as claimed. The input terminal group has a first input terminal that supplies a driving signal to the scanning-line drive circuit and a second input terminal that supplies an image signal to the data-line drive circuit. The second input terminal is disposed in a central part of the input terminal group. The first input terminal is disposed at an outer side of the input terminal group based on size of the first input terminal relative to size of the second input terminal. The first input terminal has a larger area than the second input terminal.

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Thus, the invention of Claim 12 positions input terminals based on the relative sizes of the input terminals. This accounts for extension and contraction rates of terminals during manufacturing, which prevents connection failures. See, for example, paragraph [0057] of the present application.

As best understood by Applicant, Murade discloses scan line terminals on an outer side and data line terminals on a central part. However, Murade does not disclose scan line terminals that have a larger area than data line terminals. Murade does not disclose sizing scan line and data line terminals differently. This is admitted to by the Examiner. The Examiner relies on Hirosue for the disclosure of this feature.

As best understood by Applicant, Hirosue discloses that terminals may be of different size based on length of the corresponding signal lines to equalize resistance among all signal lines. Thus, Hirosue suggests the sizing of terminals based on length of their corresponding signal lines. Hirosue does not suggest the positioning of terminals based on the sizes of the terminals.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991).

Thus, Claim 12 is allowable for at least the above reasons.

With respect to Claim 12, Murade and Hirosue do not show, teach or suggest a first input terminal that has a larger area than a second input terminal based on frequencies of signals transmitted on the first input terminal and the second input terminal.

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The invention of Claim 12 sizes input terminals based on a signal transmission characteristic, specifically frequency. The first input terminal may be associated with signals that have a higher frequency component than signals associated with the second input terminal. The first input terminal thus has a larger area than the second input terminal to improve transmission performance. See paragraphs [0048] and [0049] of the present application.

As stated, Murade does not disclose scan line terminals having larger area than data line terminals. Hirosue, although disclosing terminals of different size, does not disclose sizing terminals based on signal transmission characteristics.

Therefore, Claim 12 is further allowable for at least the above reasons. Claim 13 depends upon Claim 12 and is allowable for at least similar reasons.

Claims 1-5, 9, 10, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murade in view of Hirosue and further in view of Morozumi et al. (U.S. Pat. No. 4,242,679). This rejection is respectfully traversed.

With respect to Claim 1, Murade, Hirosue and Morozumi do not show, teach or suggest an electro optical panel that includes: A) a power source terminal that has an area that is not smaller than that of a first input terminal; and B) a pitch interval of adjacent clock signal input terminals that is an integer multiple of a pitch interval of adjacent image signal input terminals. Note that the limitations A and B are similar to features of originally filed Claims 6 and 8. The Examiner has admitted that the features of Claims 6 and 8 are not provided by Murade, Hirosue and Morozumi. The Examiner

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relies on Hayato (JP Pub. No. 2003-216064A) and Totjutsu et al. (JP Pub. No. 2003-43517) for such disclosure.

With respect to limitation A, the Examiner relies on Hayato for the disclosure of a power source terminal formed wider than scanning lines and signal lines. The Examiner refers to paragraph [0009] of Hayato which, as best uderstood by Applicant, discloses power source wiring that is formed broader than a scan line and a signal line. The forming of power source wiring broader than a scan line and signal line does not suggest the forming of a power terminal with a larger area than the area of a scan line terminal or a data line terminal. The terms "wider" and "broader" refer to a single dimension, whereas the term "area" refers to two dimensions.

Nevertheless, the forming of broader power source wiring does not suggest the forming of a power source terminal that is not smaller than a first input terminal. In other words, the power source terminal may be the same size as or may have a larger area than a first input terminal.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03.

Thus, Claim 1 is allowable for at least the above reasons.

With respect to limitation B, the Examiner relies on Totjutsu for disclosure of a pitch interval of adjacent first input terminals that is an integer multiple of a pitch interval of adjacent second input terminals. The Examiner refers to paragraphs [0007] and [0019] of Totjutsu.

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As best understood by Applicant, Totjutsu is directed to a method of inspecting a LCD panel. In paragraph [0007], Totjutsu discloses lead terminals, dummy terminals, and current probe pins. It appears that the dummy terminals have the same pitch as the lead terminals, see the Abstract Solution of Totjustu. An integral multiple of a minimum terminal pitch is provided on either side of a lead terminal group. The current probe pins are provided on the other sides of the integral multiple pitch areas than the lead terminal group. The spacing of current probe pins away from a lead terminal group is unrelated to the pitch of clock signal and image signal input terminals of an electro-optical panel.

Claim 1 is further allowable for at least the above reasons. Claims 2, 3, 5, 7, 9-11 and 14 ultimately depend from Claim 1 and are allowable for at least similar reasons.

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CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: January 31, 2008

By: _____
G. Gregory Schivley, Reg. No. 27,382
Bryant E. Wade, Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C.
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(248) 641-1600

GGS/BEW/JJC/mrg

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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10/914,044	Filing Date 08/06/2004	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/31/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DONNA D. SMALLS LOGAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

27572 7590 04/04/2008

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EXAMINER	
HO, BAO QUAN T	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
04/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/914,044	FUJITA, SHIN	
	Examiner	Art Unit	
	BAO-QUAN T. HO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5,9-11 and 14* is/are allowed.

6)☒ Claim(s) *7,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 01/31/2008 has been entered and considered by examiner.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 recites the limitation "An electro-optical panel according to Claim 6" in line 1. There is insufficient antecedent basis for this limitation in the claim, because claim 6 was canceled by applicant.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, US Patent 6,262,702, in view of Yazawa, US Pub. 2002/0003595.

Regarding claim 12, Murade discloses an electro-optical panel in fig. 5 comprising:

a plurality of data lines (35) on a substrate;

a plurality of scanning lines (31) on the substrate and intersecting the plurality of data lines;

an image display area (seen in fig. 5) on the substrate which includes a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a scanning-line drive circuit (104) for driving the pixels;

a data-line drive circuit (101) for supplying data signals to the pixels; and

an input terminal group (terminals located on the bottom of fig. 5) for supplying signals to the scanning-line drive circuit and the data-line drive circuit,

wherein the scanning-line drive circuit (left scanning circuit 104) is disposed along one side of the substrate on the substrate, the data-line drive circuit (data circuit 101) is disposed along a side which is not opposed to the one side on the substrate, the input terminal group is disposed along the data-line drive circuit and is disposed at a further edge side of the substrate than the data-line drive circuit (circuit and terminals placements can be seen in FIG. 5 and col. 15 lines 28-51); and

the input terminal group has a first input terminal (left terminal DY) for supplying a driving signal to the scanning-line drive circuit and a second input terminal (VID7) for supplying an image signal to the data-line drive circuit, the second input terminal is disposed in the central part of the input terminal group, the first input terminal is disposed at the outer side of the input terminal group (terminal placement can be seen in FIG. 5).

But, Murade does not specifically teach the first input terminal is disposed at the outer side of the input terminal group based on size of the first input terminal relative to size of the second input terminal, and the first input terminal has a larger area than the second input terminal based on frequencies of signals transmitted on the first input terminal and the second input terminal.

However, Yazawa discloses in FIG. 2 wherein teach the first input terminal (terminal 30a) is disposed at the outer side (seen in FIG. 2) of the input terminal group based on size of the first input terminal relative to size of the second input terminal (terminal 30b), and the first input terminal (30a) has a larger area than the second input terminal (30b) based on frequencies of signals transmitted on the first input terminal and the second input terminal (Page 2 paragraph [0024]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the first input terminal area to be larger as taught by Yazawa than the second imputer terminal of Murade for the purpose of allowing higher frequencies signals to supply to the display panel (Page 2 paragraph [0024]).

Thus, in combination of Murade with Yazawa, the first input terminal is disposed at the outer side of the input terminal group as Murade disclosed, and the area of the first input terminal is larger than the second input terminal as taught by Yazawa based on the size and frequencies of the first input terminal relative to the second input terminal. Therefore all the limitation has been meet with the combination of Murade with Yazawa.

Regarding claim 13, Murade discloses an electro-optical panel according to claim 12, Murade further discloses a fourth input terminal (terminal DX, col. 20 lines 45-50) for supplying a driving signal to the data-line drive circuit, wherein the fourth input terminal has an area equal to an area of the first input terminal (showing in FIG. 5, the terminals of the first, DY, is the same area as the forth terminal, DX), and the fourth input terminal is disposed between the first input terminal (left terminal DY) and the second input terminal (terminal VID7).

Allowable Subject Matter

7. Claims 1-3, 5, 7, 9-10, 11, and 14 are allowed.

Response to Arguments

8. Applicant's arguments with respect to claims 12-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Kato, US Pub. 2002/0018169, is cited for disclosing connection structure of a display device.

b. Hagiwara, US Patent 6,665,037, is cited for disclosing connection structure of a display device.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BAO-QUAN T. HO whose telephone number is (571)270-3264. The examiner can normally be reached on M-F, 8:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629

BTH

Notice of References Cited	Application/Control No. 10/914,044	Applicant(s)/Patent Under Reexamination FUJITA, SHIN	
	Examiner BAO-QUAN T. HO	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0018169	02-2002	Kato, Shin-ichi	349/149
*	B	US-2002/0003595	01-2002	Yazawa, Kazuki	349/65
*	C	US-6,665,037	12-2003	Hagiwara, Takeshi	349/148
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/24/2007	03/20/2008							
	1	✓	=							
	2	✓	=							
	3	✓	=							
	4	✓	-							
	5	✓	=							
	6	✓	-							
	7	✓	✓							
	8	✓	-							
	9	✓	=							
	10	✓	=							
	11	✓	=							
	12	✓	✓							
	13	✓	✓							
	14	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

SEARCHED			
Class	Subclass	Date	Examiner
345	60-100, 690-699, 204-213	10/02/07	BTH
349		10/02/07	BTH

SEARCH NOTES		
Search Notes	Date	Examiner
Updated Search	03/20/2008	BTH
Inventor Name Search (PALM)	03/20/2008	BTH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	20	(fujita near1 shin).in. and terminal.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/20 11:40
L15	20	(fujita near1 shin).in. and terminal.clm.	US-PGPUB; USPAT	AND	OFF	2008/03/20 11:40
S2	701144	(liquid adj crystal) or lcd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/15 18:55
S4	392757	(scan or scanning or gate) and (data or source) and substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/15 18:58
S6	65273	(base or based) same (size or area or length or width) same (terminal$1 or pad$1) same (position $3 or dispos$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/15 19:03
S7	219	S6 S2 S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/15 19:04
S8	1	("6665037").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/15 19:18
S9	10	("20010033264" | "5717475" | "6052169" | "6456279").PN. OR ("6665037").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/15 19:19
S10	1	("20020003595").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/17 14:44
S11	1	("6519019").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/17 14:46
S12	7	("4118111" | "5270847" | "5294920" | "5386309" | "5675397" | "5774199" | "6222597").PN. OR ("6519019").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/17 14:46

S13	2554784	(terminal$1 or pad$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:04
S14	4026104	(placing or placement$1 or dispos$3 or setup)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:07
S15	640152	(substrate or panel) same (inside or outer or inner or inside or center or central)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:08
S16	5474042	(area or width or wide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:36
S17	97578	S13 S14 S15 S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:36
S18	5304	S13 same S14 same S15 same S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:46
S19	703279	(liquid adj crystal) or lcd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/17 15:47
S20	2952307	assemble or assembly or manfacture or manfacturing	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/17 15:48
S22	153	S18 S19 S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/17 15:49
S23	7953766	(depend$1 or depending or based or (base adj2 on))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/17 15:57

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S24	6137	S13 S14 S15 S16 S19 S20 S23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2008/03/17 15:57
S25	9	S13 same S14 same S15 same S16 same S23 and S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 15:58
S26	4131	different same terminal same size same S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 16:05
S27	55	S19 S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 16:06
S28	8	("5517036" | "5905303" | "5920115" | "6018188").PN. OR ("6448634").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/17 17:21
S29	7802	S13 same position$3 same S16 same S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/17 18:36
S30	1702	349/149-152.ccls.	US-PGPUB; USPAT	AND	OFF	2008/03/17 18:40
S31	68	S30 S29	US-PGPUB; USPAT	AND	OFF	2008/03/17 18:40
S32	67	S30 S29 not S27	US-PGPUB; USPAT	AND	OFF	2008/03/17 18:40
S34	44	S30 S29 and different	US-PGPUB; USPAT	AND	OFF	2008/03/17 18:54
S35	3055	349/56,139,149-152.ccls.	US-PGPUB; USPAT	AND	OFF	2008/03/18 09:55
S36	2555866	(terminal$1 or pad$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 09:56
S37	640422	(substrate or panel) same (inside or outer or inner or inside or center or central)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 09:56
S38	5476464	(area or width or wide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 09:56

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S39	7804	S36 same position$3 same S38 same S37	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 09:56
S40	2377	S39	US-PGPUB; USPAT	AND	OFF	2008/03/18 09:56
S41	1473	349/56,139.ccls.	US-PGPUB; USPAT	AND	OFF	2008/03/18 09:59
S42	11	S39 S41	US-PGPUB; USPAT	AND	OFF	2008/03/18 09:59
S43	24	("3928658").PN. OR ("4586789").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 10:10
S44	8	("4586789" | "5712493" | "5742074" | "6025891" | "6043971" | "6059624"). PN. OR ("6930744"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 10:29
S45	10	("4586789" | "4682858" | "4985663" | "5712493" | "5798812").PN. OR ("6147739").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 10:31
S46	31	("4469568" | "4586789" | "4601097" | "4624737" | "4704002" | "4723838" | "4803536" | "4821092" | "4990460").PN. OR ("5146301").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 10:38
S47	12	("20020100974" | "4136356" | "5555116" | "5712493" | "6091475" | "6147739" | "6198522" | "6297868" | "6678028" | "6738123" | "6894758" | "6954249").PN. OR ("7224424").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 11:03
S48	6	("20020100974" | "6297868").PN. OR ("6678028").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 11:09
S49	12	("4604644" | "5157476" | "5311341" | "5367763" | "5402255" | "5925931"). PN. OR ("6059624"). URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2008/03/18 11:11
S50	1	((terminal$1 or pad$1) near4 arrangment$1) same (inner or inside) same (outer or outside)	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:11
S51	45	((terminal$1 or pad$1) near4 arrangment$1)	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:12
S52	39028	((terminal$1 or pad$1) near4 arrangement$1)	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:14

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S53	2073	((terminal$1 or pad$1) near4 arrangement$1) same (inner or inside) same (outer or outside)	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:14
S55	28547	"349".clas.	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:15
S56	26	S53 S55	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 13:15
S57	1	("6587177").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/18 14:11
S58	1	("6406946").PN. OR ("6587177").URPN.	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 14:11
S59	1	("7335953").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/18 14:17
S60	12	("20070034875" | "4819047" | "5034845" | "5635822" | "5717559" | "5736732" | "5917220" | "5991134" | "6211554" | "6696701" | "6967826" | "7115952").PN. OR ("7335953").URPN.	US-PGPUB; USPAT; USOCR	AND	OFF	2008/03/18 14:18
S64	9	small near3 (pad$1 or terminal$1) near5 (center or central) near5 substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 14:45
S65	8	smaller near3 (pad$1 or terminal$1) near5 (center or central) near5 substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	AND	OFF	2008/03/18 14:52
S73	1	("20070171115").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/18 16:45
S74	1	("20060017715").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/03/18 18:48

3/20/2008 12:03:52 PM
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PATENT AND TRADEMARK OFFICE
INFORMATION DISCLOSURE CITATION
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Sheet 1 of 1

ATTORNEY DOCKET NO.	SERIAL NO.
9319S-000838	10/914,044
APPLICANT	
Shin FUJITA	
FILING DATE	GROUP
August 6, 2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.	/B.T.H./	2003-152019A	05/23/2003	Japan		X	
2.	/B.T.H./	2003-216064A	07/30/2003	Japan		X	
3.	/B.T.H./	11-223832A	08/17/1999	Japan		X	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.	/B.T.H./	Examination result regarding corresponding Japanese application

*One or more of the English translation documents submitted herewith may be Abstracts only or partial machine created translations from the Japanese Patent Office. As such, the submitter does not necessarily vouch for their accuracy. Additional information may be obtained from the Japanese Patent Office web site at www.jpo.go.jp

Examiner:	/Bao-Quan Ho/	Date Considered:	03/20/2008

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Day : Thursday
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Time: 11:33:19

Inventor Name Search Result

Your Search was:

Last Name = FUJITA
First Name = SHIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09731668	6784880	150	12/08/2000	ELECTRO-OPTICAL DEVICE, CLOCK SIGNAL ADJUSTING METHOD AND CIRCUIT THEREFOR, PRODUCING METHOD THEREFOR, AND ELECTRONIC EQUIPMENT	FUJITA, SHIN
09763942	Not Issued	95	06/01/2001	SYSTEM FOR MANAGING PROCESS AND MAN-HOUR	FUJITA, SHIN
09910879	6791523	150	07/24/2001	ELECTRO-OPTICAL PANEL, METHOD FOR DRIVING THE SAME, ELECTROOPTICAL DEVICE, AND ELECTRONIC EQUIPMENT	FUJITA, SHIN
09994675	6703856	150	11/28/2001	TEST METHOD OF ELECTRO-OPTICAL DEVICE, TEST CIRCUIT OF ELECTRO-OPTICAL DEVICE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC EQUIPMENT	FUJITA, SHIN
10014439	6753839	150	12/14/2001	ELECTRO-OPTICAL PANEL AND ELECTRONIC DEVICE	FUJITA, SHIN
10347581	6828817	150	01/22/2003	ELECTROOPTIC DEVICE, ELECTRONIC APPARATUS, AND METHOD FOR MAKING THE ELECTROOPTIC DEVICE	FUJITA, SHIN
10406232	7023415	150	04/04/2003	SHIFT REGISTER, DATA-LINE DRIVING CIRCUIT, AND SCAN-LINE DRIVING CIRCUIT	FUJITA, SHIN
10406259	6879179	150	04/04/2003	IMAGE-SIGNAL SUPPLYING CIRCUIT AND ELECTRO-OPTICAL PANEL	FUJITA, SHIN
10629590	Not Issued	161	07/30/2003	Timing adjustment circuit, drive circuit, electrooptic device and electronic equipment	FUJITA, SHIN

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10629591	7095405	150	07/30/2003	OUTPUT CONTROL CIRCUIT, DRIVING CIRCUIT, ELECTRO-OPTIC APPARATUS, AND ELECTRONIC INSTRUMENT	FUJITA, SHIN
10671451	7084940	150	09/29/2003	ELECTRO-OPTIC DEVICE COMPRISING A RECESS/PROJECTION PATTERN OBTAINED BY ROTATING A REFERENCE PATTERN ABOUT A PREDETERMINED POSITION	FUJITA, SHIN
10673243	7157739	150	09/30/2003	ACTIVE MATIX TYPE ELECTRO-OPTICAL DEVICE WITH PATTERNS OF CONTACT HOLE FORMATION-POSITIONS AND ELECTRONIC APPARATUS	FUJITA, SHIN
10677341	7088415	150	10/03/2003	ELECTRO-OPTIC PANEL AND MANUFACTURING METHOD THEREOF	FUJITA, SHIN
10779712	Not Issued	161	02/18/2004	Electro-optical panel and electronic equipment	FUJITA, SHIN
10792327	Not Issued	41	03/02/2004	Data processing system, data processing apparatus and data processing method	FUJITA, SHIN
10843421	7064573	150	05/12/2004	DRIVING CIRCUIT, METHOD OF TESTING DRIVING CIRCUIT, ELECTRO-OPTICAL APPARATUS, AND ELECTRO-OPTICAL DEVICE	FUJITA, SHIN
10853000	Not Issued	61	05/25/2004	Apparatus and method for packet error correction	FUJITA, SHIN
10894020	Not Issued	90	07/20/2004	DRIVING CIRCUIT, METHOD FOR PROTECTING THE SAME, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC APPARATUS	FUJITA, SHIN
10914044	Not Issued	71	08/06/2004	Electro-optical panel, electro-optical apparatus, and electronic system	FUJITA, SHIN
10979144	7233155	150	11/03/2004	ELECTROOPTIC DEVICE, ELECTRONIC APPARATUS, AND METHOD FOR MAKING THE ELECTROOPTIC DEVICE	FUJITA, SHIN
10994343	7320099	150	11/23/2004	METHOD AND APPARATUS FOR GENERATING ERROR	FUJITA, SHIN

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				CORRECTION DATA, AND A COMPUTER-READABLE RECORDING MEDIUM RECORDING AN ERROR CORRECTION DATA GENERATING PROGRAM THEREON	
11010429	Not Issued	61	12/14/2004	Electro-optical device and electronic apparatus	FUJITA, SHIN
11036370	7157740	150	01/18/2005	ELECTRO-OPTICAL DEVICE AND ELECTRONIC APPARATUS	FUJITA, SHIN
11101502	Not Issued	41	04/08/2005	Shift register, data line driving circuit, scanning line driving circuit, electro-optical device, and electronic apparatus	FUJITA, SHIN
11147250	Not Issued	61	06/08/2005	ELECTRO-OPTICAL AND ELECTRONIC APPARATUS WITH A PROTECTIVE CIRCUIT	FUJITA, SHIN
11188763	Not Issued	30	07/26/2005	Electro-optical device, method of driving electro-optical device, and electronic apparatus	FUJITA, SHIN
11299334	Not Issued	30	12/09/2005	Electro-optical device and electronic apparatus	FUJITA, SHIN
11301749	Not Issued	30	12/13/2005	Electro-optical device and electronic apparatus	FUJITA, SHIN
11365681	Not Issued	25	03/02/2006	Image transmitting apparatus and image transmitting system	FUJITA, SHIN
11399673	Not Issued	30	04/06/2006	Driving circuit for liquid crystal display device, liquid crystal display device, method of driving liquid crystal display device, and electronic apparatus	FUJITA, SHIN
11431518	Not Issued	30	05/11/2006	Test circuit, electro-optical device, and electronic apparatus	FUJITA, SHIN
11436032	Not Issued	30	05/18/2006	Electro-optical device, method of driving electro-optical device, and electronic apparatus	FUJITA, SHIN
11514176	Not Issued	30	09/01/2006	Liquid crystal device, light emitting device, electronic apparatus, method of controlling liquid crystal device, and method of controlling light emitting device	FUJITA, SHIN
11521452	Not Issued	30	09/15/2006	Liquid crystal device and electronic apparatus	FUJITA, SHIN

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11525938	Not Issued	30	09/25/2006	Liquid crystal device, light-emitting device, and electronic apparatus	FUJITA, SHIN
11640838	Not Issued	30	12/19/2006	Electro-optical device, driving method thereof, and electronic apparatus	FUJITA, SHIN
11652623	Not Issued	30	01/12/2007	Liquid crystal apparatus and electronic device	FUJITA, SHIN
11703763	Not Issued	30	02/08/2007	Liquid crystal device and electronic apparatus	FUJITA, SHIN
11704196	Not Issued	30	02/09/2007	Electro-optical device, light receiving device, and electronic apparatus	FUJITA, SHIN
11704197	Not Issued	30	02/09/2007	Liquid crystal device and electronic apparatus	FUJITA, SHIN
11708534	Not Issued	30	02/21/2007	Electro-optical device and electronic apparatus	FUJITA, SHIN
11710403	Not Issued	41	02/26/2007	Electro-optical device and electronic apparatus	FUJITA, SHIN
11715974	Not Issued	30	03/09/2007	Liquid crystal device and electronic apparatus	FUJITA, SHIN
11812348	Not Issued	30	06/18/2007	Liquid crystal device, method of driving liquid crystal device, and electronic apparatus	FUJITA, SHIN
11812502	Not Issued	30	06/19/2007	Electro-optical device and electronic apparatus	FUJITA, SHIN
11892288	Not Issued	25	08/21/2007	Liquid crystal device and electronic apparatus	FUJITA, SHIN
11892624	Not Issued	25	08/24/2007	Driving circuit, liquid crystal device, electronic apparatus, and method of driving liquid crystal device	FUJITA, SHIN
11902033	Not Issued	25	09/18/2007	Driving circuit and driving method of liquid crystal device, liquid crystal device, and electronic apparatus	FUJITA, SHIN
11902771	Not Issued	25	09/25/2007	Packet distribution band controlling method, distributing apparatus, and video distributing system	FUJITA, SHIN
11976326	Not Issued	25	10/23/2007	Encoding/decoding system, encoding system, and decoding system	FUJITA, SHIN

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FUJITA SHIN Search

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PTO/SB/30 (01-08)
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Request For Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/914,044
Filing Date	March 6, 2004
First Named Inventor	Shin Fujita
Art Unit	2629
Examiner Name	Bao-Quan T. Ho
Attorney Docket Number	9319S-000838

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
ii. ☐ Other _____

b. . ☒ Enclosed

i. ☒ Amendment/Reply
ii ☐ Affidavit(s)/Declaration(s)
iii. ☐ Information Disclosure Statement (IDS)
iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) **required**)

b. ☐ Other _____

3. Fees The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-3213

i. ☒ RCE fee required under 37 C.F.R. 1.17(e)
ii. ☐ Extension of time fee (37 C.F.R. 1.136 and 1.17)
iii. ☐ Other _____

b. ☐ Check in the amount of $ _____ enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Bryant E. Wade/	*Date*	May 21, 2008
Name (Print /Type)	G. Gregory Schivley / Bryant E. Wade	*Registration No. (Attorney/Agent)*	27,382 / 40,344

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	10914044
Filing Date:	06-Aug-2004
Title of Invention:	Electro-optical panel, electro-optical apparatus, and electronic system
First Named Inventor/Applicant Name:	Shin Fujita
Filer:	Bryant Edward Wade/Mary Aiello
Attorney Docket Number:	9319S-000838

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	2	210	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**1230**

Electronic Acknowledgement Receipt

EFS ID:	3338214
Application Number:	10914044
International Application Number:	
Confirmation Number:	5848
Title of Invention:	Electro-optical panel, electro-optical apparatus, and electronic system
First Named Inventor/Applicant Name:	Shin Fujita
Customer Number:	27572
Filer:	Bryant Edward Wade/Mary Aiello
Filer Authorized By:	Bryant Edward Wade
Attorney Docket Number:	9319S-000838
Receipt Date:	21-MAY-2008
Filing Date:	06-AUG-2004
Time Stamp:	16:17:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1230
RAM confirmation Number	1459
Deposit Account	503213
Authorized User	

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Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment_Accompanying_RCE.pdf	64486 f4763719b8ea26da98f84bacd568c807efd3e6dc	yes	10

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment After Final	1	1
Specification	2	2
Claims	3	7
Applicant Arguments/Remarks Made in an Amendment	8	10

Warnings:

Information:

2	Request for Continued Examination (RCE)	Request_for_Continued_Examination.pdf	91166 37048860e2b30805fb4754501a3ff0c45ff6c14b	no	1

Warnings:

This is not a USPTO supplied RCE SB30 form.

Information:

3	Fee Worksheet (PTO-06)	fee-info.pdf	8324 191e3bb7e007db040c579ffaf82be7d94f6845a5	no	2

Warnings:

Information:

Total Files Size (in bytes):	163976

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	March 6, 2004
Applicant:	Shin Fujita
Group Art Unit:	2629
Examiner:	Bao-Quan T. Ho
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT ACCOMPANYING
REQUEST FOR CONTINUED EXAMINATION

Sir:

In response to the Office Action mailed April 4, 2008, please amend the application as follows and consider the remarks set forth below. A Request for Continued Examination (RCE) is submitted herewith.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 8 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph the Title of the present application with the following Title rewritten in amendment format:

ELECTRO-OPTICAL PANEL ~~, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC~~ SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS

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BOE EXHIBIT 1003
Page 358 of 473

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a scanning line clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that ~~sequenctially~~ sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals;

a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and

a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,

wherein the clock signal input terminal has a larger area than the image signal input terminal, and

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wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included;

the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.

2. (Previously Presented) An electro-optical panel according to Claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.

3. (Previously Presented) An electro-optical panel according to Claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.

4. (Cancelled).

5. (Previously Presented) An electro-optical panel according to Claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.

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6-8. (Cancelled).

9. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 1;

power source means for supplying the power source; and

signal generation means for supplying the input signals.

10. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 9;

an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate which connects the external substrate and the electro-optical panel,

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.

11. (Previously Presented) An electro-optical apparatus according to Claim 10, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.

12-13. (Cancelled).

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14. (Original) An electronic system comprising the electro-optical apparatus set forth in Claim 1.

15. (New) An electro-optical panel comprising:

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a clock signal;

an image signal input terminal supplied with an image signal; and

a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the clock signal and outputs a scanning signal to each of the scanning lines, image signals from the data lines supplied to pixels selected by the scanning signals,

wherein the clock signal input terminal has a larger area than the image signal input terminal.

16. (New) The electro-optical panel according to Claim 15, the clock signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.

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17. (New) The electro-optical panel according to Claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.

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REMARKS

Claims 1-3, 5, 7 and 9-14 are now pending in the application. Claim 1 is amended herein. Claims 7, 12 and 13 are cancelled herein. New Claims 15-17 are presented herein. While Applicants disagree with the current rejections, Applicant has cancelled Claims 7, 12 and 13 to expedite prosecution. Applicant reserves the right to pursue Claims 7, 12 and 13 as previously presented in one or more continuing applications. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

SPECIFICATION

The Examiner alleges that the Title of the present application is not descriptive. The Title is amended as suggested by the Examiner. Therefore, reconsideration and withdrawal of this objection are respectfully requested.

REJECTION UNDER 35 U.S.C. § 112

Claim 7 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention.

Claim 7 is cancelled herein. Reconsideration and withdrawal of this rejection are requested.

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REJECTION UNDER 35 U.S.C. § 103

Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murade (U.S. Pat. No. 6,262,702) in view of Yazawa (U.S. Pub. No. 2002/0003595) This rejection is respectfully traversed.

Claims 12 and 13 are cancelled herein. Reconsideration and withdrawal of this rejection are requested.

NEW CLAIMS

New Claims 15-17 are added. Support for these new claims can be found throughout the specification, claims, and drawings as originally filed. No new matter is added.

ALLOWABLE SUBJECT MATTER

Claims 1-3, 5, 9-11 and 14 are allowed.

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CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: May 21, 2008

By: /Bryant E. Wade/
G. Gregory Schivley
Reg. No. 27,382
Bryant E. Wade
Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C.
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GGS/BEW/JJC/mea

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

27572 7590 06/24/2008

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
HO, BAO QUAN T	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
06/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/914,044	FUJITA, SHIN	
	Examiner	Art Unit	
	BAO-QUAN T. HO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,9-11 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5,9-11,14 and 17* is/are allowed.

6)☒ Claim(s) *15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The amendment filed on 05/21/2008 has been entered and considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, US Patent 6,262,702, and in view of Onishi, US Patent 6,469,767.

As to claim 15, Murade discloses an electro-optical panel (FIG. 1) comprising:

data lines (35);

scanning lines (31) intersecting the data lines;

pixels (11) disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal (CLY terminal, seen in FIG. 1) supplied with a clock signal (CLY);

an image signal input terminal (VID1-12 terminals, seen in FIG.1) supplied with an image signal (VID1-12); and

a scanning line drive circuit (104) that sequentially (shift register) transmits a transmission start pulse (Start signal DY) in synchronization with the clock signal (CLY

from scan driver 104) and outputs a scanning signal to each of the scanning lines, image signals (VID1-12 from data driver 101) from the data lines supplied to pixels selected by the scanning signals,

but Murade does not specifically discloses wherein the clock signal input terminal has a larger area than the image signal input terminal.

However, Onishi discloses in FIG. 2 wherein the plurality terminals (43) for inputting serial data and a shift clock (see col. 6, lines 38-42). As shown in Figure 2, the right most terminals (43) has larger area than the left most terminals (43). Since Murade teaches the clock terminal located on right most of the plural terminals, thus combining Murade and Onishi would meet the claimed "the clock signal input terminal (Shift clock of the right most Plural Terminals 43, col. 6 lines 38-42) has a larger area (seen in FIG. 1) than the image signal input terminal (Serial data of the left most Plural Terminals 43, col. 6 lines 38-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the arrangements of the terminals as taught by Onishi but maintaining the terminal orders of Murade, to have the clock signal terminal arrangement be made to the right outer most terminal of as like Onishi, while the image signal terminal is the left most terminal as like the plural terminal 43 in reference Onishi, wherein the clock terminal is larger than the image terminal as like the reference of Onishi for the purpose of providing efficient amount of space of the display panel (col. 3 lines 54-60).

As to claim 16, Murade in view of Onishi discloses the clock signal input terminal having a smaller resistance compared with resistance of the image signal input terminal (As an electrical trait, larger the terminal becomes that the resistance reduces, therefore the clock signal terminal will have a smaller resistance than the image signal terminal because the clock signal terminal is larger than the image signal terminal).

Allowable Subject Matter

4. Claims 1-3, 5, 9-11, 14, and17 are allowed.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BAO-QUAN T. HO whose telephone number is (571)270-3264. The examiner can normally be reached on M-F, 8:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629

Notice of References Cited	Application/Control No. 10/914,044	Applicant(s)/Patent Under Reexamination FUJITA, SHIN	
	Examiner BAO-QUAN T. HO	Art Unit 2629	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,469,767	10-2002	Onishi, Hiroaki	349/149
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/24/2007	03/20/2008	06/15/2008						
	1	✓	=	=						
	2	✓	=	=						
	3	✓	=	=						
	4	✓	-	-						
	5	✓	=	=						
	6	✓	-	-						
	7	✓	✓	-						
	8	✓	-	-						
	9	✓	=	=						
	10	✓	=	=						
	11	✓	=	=						
	12	✓	✓	-						
	13	✓	✓	-						
	14	✓	=	=						
	15			✓						
	16			✓						
	17			=						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

SEARCHED			
Class	Subclass	Date	Examiner
345	60-100, 690-699, 204-213	10/02/07	BTH
349	149-152	10/02/07	BTH

SEARCH NOTES		
Search Notes	Date	Examiner
Updated Search	03/20/2008	BTH
Inventor Name Search (PALM)	03/20/2008	BTH
Updated Search	06/18/2008	BTH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin Fukita
Group Art Unit:	2629
Examiner:	Bao Quan T. Ho
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed June 24, 2008, please amend the application as follows and consider the remarks set forth below. A Supplemental Invention Disclosure Statement is submitted herewith.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 10 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [0062] with the following paragraph rewritten in amendment format:

[0062] The image processing circuit 400 performs gamma correction on the input image data D in consideration of the light transmission characteristics of the liquid crystal panel AA, and then supplies the image data to the data-line drive circuit 200. The data-line drive circuit 200 transmits the X transmission start pulse DX in sequence in synchronism with the X clock signal XCK and the inverted X clock signal XCKB to generate a sampling signal. The data-line drive circuit 200 samples the image data ~~is sampled~~ using the generated sampling signal to generate line sequential image data ~~for each line in sequence~~. Furthermore, the data-line drive circuit 200 performs D/A conversion on the image data ~~is D/A converted~~ to generate line sequential image signals~~an image signal for each line in sequence~~. This image signal is supplied to the liquid crystal panel AA through the flexible substrate B.

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AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a scanning line clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals;

a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and

a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,

wherein the clock signal input terminal has a larger area than the image signal input terminal, and

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wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included;

the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.

2. (Previously Presented) An electro-optical panel according to Claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.

3. (Previously Presented) An electro-optical panel according to Claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.

4. (Cancelled).

5. (Previously Presented) An electro-optical panel according to Claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.

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6-8. (Cancelled).

9. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 1;

power source means for supplying the power source; and

signal generation means for supplying the input signals.

10. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 9;

an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate which connects the external substrate and the electro-optical panel,

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.

11. (Previously Presented) An electro-optical apparatus according to Claim 10, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.

12-13. (Cancelled).

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14. (Original) An electronic system comprising the electro-optical apparatus set forth in Claim 1.

15. (Currently Amended) An electro-optical panel comprising:

a first substrate;

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock-~~—~~signal input terminal supplied with a clock ~~signal;~~signal and connected to a mounting member through anisotropic conductive film;

~~an image signal~~ image-signal input ~~terminal~~ terminals supplied with image signals and connected to the mounting member through anisotropic conductive film, the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate, the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines; and ~~an image signal; and~~

a ~~scanning line~~ scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal ~~and outputs a scanning signal to each of the scanning lines, image signals from the data lines supplied to pixels selected by the scanning signals~~,

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wherein the clock-signal input terminal connected to the mounting member through said anisotropic conductive film has a larger area than at least one of the ~~image signal~~ image-signal input ~~terminal~~terminals connected to the mounting member through anisotropic conductive film.

16. (Currently Amended) The electro-optical panel according to Claim 15, the clock-signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.

17. (Previously Presented) The electro-optical panel according to Claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.

18. (New) The electro-optical panel according to Claim 15 the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal.

19. (New) The electro-optical panel according to Claim 15, the external data line circuit being formed on a second substrate other than the first substrate.

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20. (New) The electro-optical panel according to Claim 15, the clock-signal input terminal being disposed further out on the first substrate relative to a central part of an outer edge of the first substrate than the image signal input terminal.

21. (New) The electro-optical panel according to Claim 15, the pixels arranged on the first substrate.

22. (New) The electro-optical panel according to Claim 15, the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.

23. (New) An electro-optical panel comprising:

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals; and

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a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.

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REMARKS

Claims 1-3, 5, 9-11 and 14-19 are now pending in the application. Claims 15 and 16 are amended herein. New Claims 18-23 are presented herein. Support for the amendments to the claims can be found throughout the drawings and specification. As such, no new matter is added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

SPECIFICATION

Paragraph [0062] is amended herein to correct errors that occurred in translation between the Japanese Patent Application No. 2004-193515 filed on June 30, 2004 and the present application. The Japanese Patent Application is incorporated by reference in its entirety in paragraph [0001] of the present application. Paragraph [0039] of the Japanese Patent Application corresponds with paragraph [0062] of the present application.

In paragraph [0039] of the Japanese Patent Application different functions of the data line drive circuit 200 are stated. In the translation, the translator parsed up a long Japanese sentence into smaller English sentences without adding the sentence subject (i.e., the data line drive circuit 200) to each of the smaller sentences. Also, a phrase "generate line sequential image signals" was incorrectly translated to "generate an image signal for each line in sequence".

The term "line sequential" refers to a line sequential drive method that is used. The line sequential drive method includes the outputting of image signals to all data lines

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simultaneously. In other words, the image signals are not applied to one data line at a time, but rather all at once. This is a feature of a hybrid drive and enables fast operation.

The term "line sequential" is a term well-known to those skilled in the art. As an example and to show that this term was well-known at the time the present invention was made, a copy of relevant sections and corresponding English translations of "Liquid Crystal Display Technology", by Shoichi Matsumoto, published in 1996 is submitted herewith. In the first paragraph of page 14 and in lines 12-14 of page 70 of Matsumoto a line sequential drive method is described. The line sequential drive method includes applying signals simultaneously to signal lines D_1, D_2, ... D_m (data lines) and sampling the signals by using address signals supplied to scanning lines G_1, G_2, ... G_n sequentially. Signal electrical charges are supplied through signal column electrodes (drain bus) Y1, Y2, ... Ym to all of the capacitors connected to three-terminal elements to provide signals simultaneously to the data lines. The signal electrical charges are applied to all pixels on a gate bus.

REJECTION UNDER 35 U.S.C. § 103

Claims 15-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murade (U.S. Pat. No. 6,262,702) in view of Onishi (U.S. Pat. No. 6,469,767). This rejection is respectfully traversed.

With respect to Claim 15, Murade and Onishi do not at least show, teach or suggest: A) supplying image signals simultaneously to all data lines of an electro-optical panel; B) forming a scanning-line drive circuit of a first substrate and connecting an image signal input and a clock signal input to a mounting member via an anisotropic

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conductive film; and C) transmitting a transmission start pulse via a scanning-line driver circuit in synchronization with a clock signal of an electro-optical panel. Feature A is disclosed at least in paragraph [0062] of the present application. Feature B is disclosed in at least paragraph [0007], [0024], [0043], [0045], and [0057] of the present application. Feature C is disclosed at least in paragraph [0051] of the present application.

With respect to feature A, Murade appears to disclose supplying image data to blocks of data line switches S1-S6, S7 to S12, Sn-5 to Sn-1 (shown in FIG. 2) in sequence, not simultaneously. The image signals of Murade are applied to data lines in sequence. See, for example, col. 16, lines 24-26 and lines 46-50 of Murade.

Onishi only discloses a passive panel, which does not have data lines and thus does not incorporate a data line drive circuit.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03.

Claim 15 is allowable for at least the above reasons.

With respect to feature B, Murade appears to disclose the forming of a scanning line driver circuit, an image signal input and a clock signal input on the same insulating layer of a single substrate. Murade does not disclose the forming of an image signal input and a clock signal input on a different layer, substrate, or other circuit supporting element than a scanning line drive circuit.

Onishi does not disclose a scanning line driver circuit.

Claim 15 is further allowable for at least the above reasons.

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With respect to feature C, although Murade appears to disclose a scanning line driver circuit start signal DY and a clock signal CLY, Murade does not disclose a transmission start pulse of a scanning line driver circuit that is transmitted in synchronization with a clock signal. The scanning line driver circuit start signal DY is used to start shift register circuits. Some time after the shift register circuits are started, the clock signal CLY of Murade is used to apply a scanning signal to scanning lines in sequence (line by line). Thus, the clock signal CLY of Murade is a shift clock signal. Murade does not disclose the synchronization of the clock signal CLY with the scanning line driver circuit start signal DY. See col. 15, lines 56-65 of Murade.

As Onishi does not disclose a scanning line drive circuit, Onishi does not disclose the claimed transmission start pulse.

Claim 15 is further allowable for at least the above reasons.

Claims 16 (and new Claims 18-22) ultimately depend on Claim 15 and are allowable for at least similar reasons.

With respect to new Claims 18, 20 and 21, Murade and Onishi do not at least show, teach or suggest an image signal input terminal that is disposed closer to a center of an edge of a substrate than a clock signal input terminal. This appears to be admitted to by the Examiner in the allowance of Claim 17.

With respect to new Claim 19, Murade and Onishi do not at least show, teach or suggest a scanning-line drive circuit that is formed on a first substrate and an external

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data line circuit that is formed on a second substrate other than the first substrate. This feature is disclosed at least in paragraph [0060] and FIG. 5 of the present application.

By forming the scanning-line drive circuit on a first substrate, the scanning-line drive circuit is formed using semiconductor methods. In other words, the scanning-line drive circuit is not formed on a separate chip. By forming the external data line drive circuit on a second substrate that is different than the first substrate, the data line drive circuit may be formed on a separate chip and/or on a flexible substrate of an input cable. Paragraph [0045] of the present application discloses different mounting techniques, such as mounting a driving IC chip (including a scanning-line drive circuit, an external data line drive circuit, etc.) on a film using tape automated bonding (TAB) or circuit on glass (COG) techniques. The IC chip mounting techniques are different than techniques used when a scanning line drive circuit or a data line drive circuit are formed on a substrate.

As best understood by Applicant, Murade discloses a data line driving circuit 1010 that is formed on a TFT array substrate 1 with a sampling circuit 301 and a scanning line driver circuit 104. See col. 15, lines 28-30 of Murade. Murade does not disclose the formation of the data line driving circuit 1010 and the scanning line driver circuit 104 on different substrates.

As Onishi does not disclose a scanning line drive circuit or a data line drive circuit, Onishi also does not disclose the separate mounting of a data line drive circuit as claimed.

New Claim 19 is allowable for at least the above reasons.

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CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: September 17, 2008

By: /Bryant E. Wade/
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[GGS/BEW/pvd]

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FORM HDP-1449 (Based on Form PTO-1449) **PATENT AND TRADEMARK OFFICE** **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary) Sheet 1 of 1	ATTORNEY DOCKET NO.	APPLICATION NO.
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	Shin Fukita	
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	August 6, 2004	2629

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
1.		Liquid Crystal Display Technology, by Shoichi Matsumoto, published 1996, pages 10, 14-15, 70-71, and 326-327, Figures 1.11 and 2.14.

Examiner:	Date Considered:

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Partial translation of Liquid Crystal Display Technology

Page 14, Fig. 1.11 and first paragraph

Fig. 1.11 shows the operating principle of an LCD using three-terminal elements by active matrix drive. The scanning row electrodes (gate bus) X_1, X_2, ... X_n are scanned one after the other using a line sequential drive method so that all of the three-terminal elements on one gate bus are temporarily turned ON all at once. In synchronization with this scanning, signal electrical charges from the hold circuit are supplied through the signal column electrodes (drain bus) Y_1, Y_2, ... Y_m to all of the capacitors connected to the three-terminal elements in this ON condition. These signal electrical charges continue to be applied to the liquid crystal of all pixels on the gate bus until the next frame of scanning.

Page 70, lines 12 to 14

Writing to the pixel electrodes is performed by a method wherein signals supplied simultaneously to the signal lines D_1, D_2, ...D_m are sampled using address signals sequentially supplied to the scanning lines G_1, G_2, ... G_n. This is called line sequential drive.

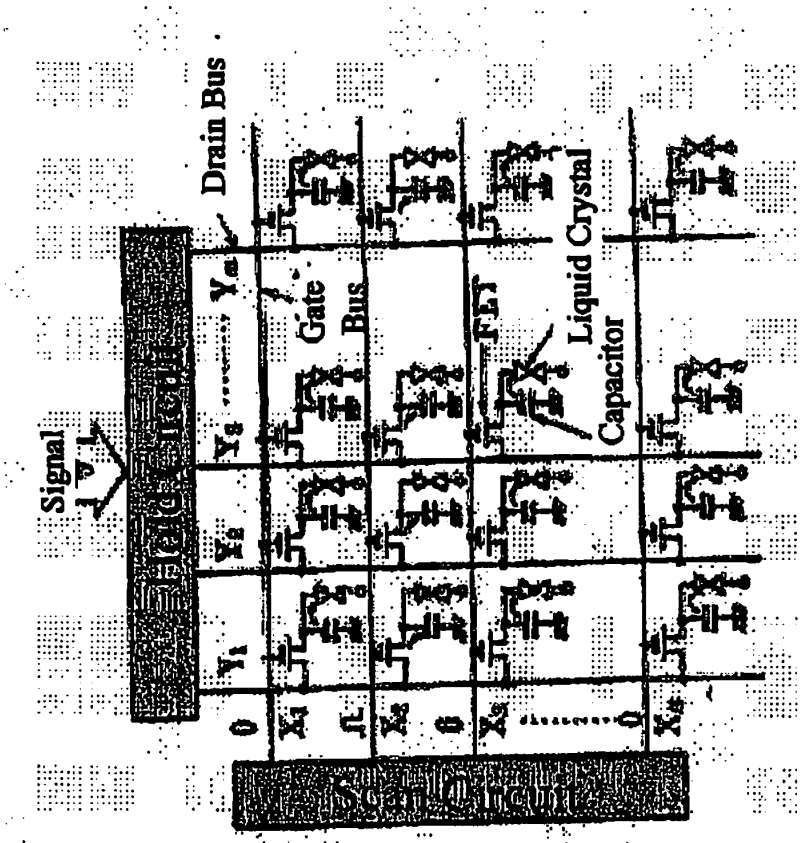


Fig. 1.11 Operating principle of three-terminal element type active matrix drive LCD

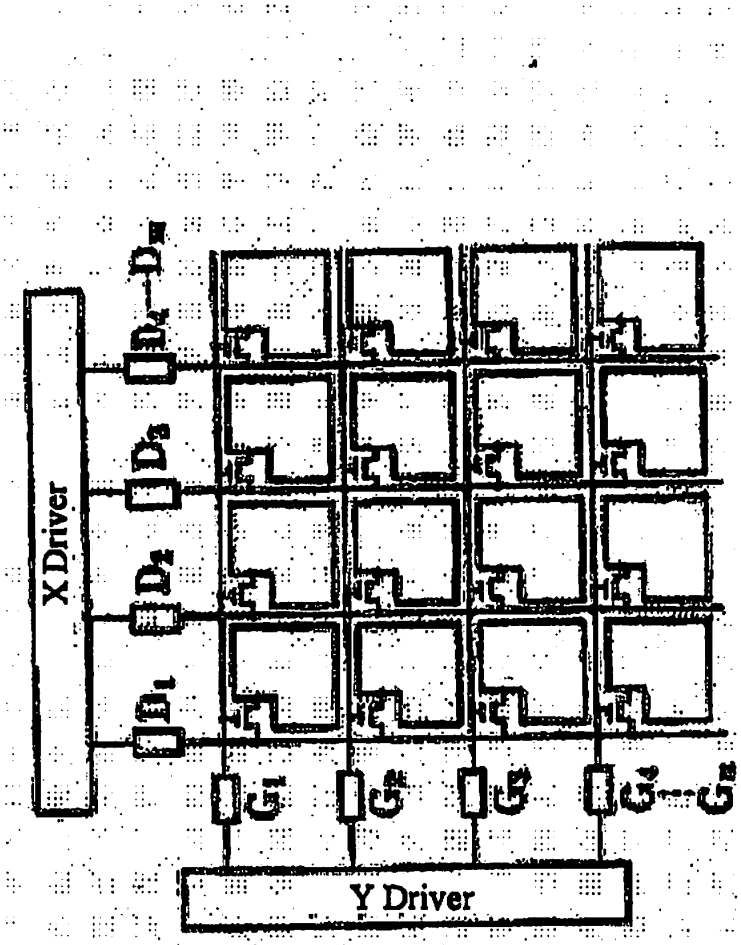


Fig. 2.14 Basic circuitry structure of an a-Si type TFT drive LCD

液晶ディスプレイ技術

—アクティブマトリクスLCD—

松本正一 編著

LIQUID CRYSTAL DISPLAY TECHNOLOGY : Active-Matrix LCDs

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—アクティブマトリクスLCD—
松本正一 編著

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図2.14 a-Si系TFT駆動LCDの基本構成

(1) 基本動作原理とフレーム反転駆動

このような回路構成のAM-LCDの駆動について考える．液晶に長時間DC電圧を印加すると，材料特性が変化し表示品質が劣化するなどの弊害が生じてくる．したがって，LCDパネル各点の極性から交流駆動が必要となり，駆動電圧の極性を反転しなくてはならない．このため，フレームごとに極性が反転する．m×n行列のAM-LCDを駆動する場合，走査線にはアドレス信号（線順次走査信号）を供給し，信号線にはフレーム走査期間ごとに極性反転した画像信号を供給する．また列方向表示信号を供給することになる．この表示信号は，アドレス信号でオン／オフ制御されるTFTスイッチを介して，各画素の蓄積容量に書き込まれ，画素電圧と共通対向電極に供給される電圧との電位差によって，各々の画素の電荷量が決まり，液晶上の表示が動作することになる．

図2.15 a-Si系TFT駆動LCDの駆動電圧波形（フレーム反転駆動）

[redacted]

書き込み特性，(c)保持特性に分けて説明する．対向電圧を $V=0$ Vとして，$V=V_d$ のゲート電圧パルスを走査期間 t_s の間ゲートに印加されるとする．信号電圧は各画素電圧中心 V_{mid} に対して，フレーム周期ごとに正負と交互に反転駆動されている．つまり，図2.15で第 n フレーム期間を書き込み，第 $(n+1)$ フレームが負書き込みとなる．書き込み特性は，TFTのオン抵抗，画素容量，書き込み時間，信号電圧に依存する．t_s 時間後にゲートがオフした瞬間，画素電圧値 V_0 はフィードスルー電圧 ΔV_p（突き抜け電圧ということもある）分だけ低くなる．その後の保持特性は，TFTのオフ抵抗，画素容量，液晶抵抗を通じてのリーク電流などに依存する．

(2) フィードスルー現象と対策

フィードスルー特性について，図2.16に示す画素の等価回路で考える．

図2.16 画素の等価回路

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図 1.10 3端子素子形 AM 駆動 LCD の断面

図 1.11 3端子素子形 AM 駆動 LCD の動作原理

晶の電気容量や比抵抗が十分に大きい場合には，信号を安定するためのキャパシタを特別に設ける必要はない．

(2) 2端子素子マトリクス駆動方式

2端子素子をスイッチング素子として用いるアクティブマトリクス駆動方式は，図 1.9 に示したように，MIM (metal-insulator-metal) 形，ダイオード形，バリスタ形などに分類され，いずれも TFT 駆動方式に比べ製造工程と低コスト化を目指している．これらの2端子素子は基板と直列に接続され，液晶の電気光学特性の印加電圧を制御している．

MIM 形では，Ta/Ta_2O_5/Cr で代表される金属層(M)/絶縁層(I)/金属層(M)構造のスイッチング素子を用いる．図 1.12 に，ラテラル構造を特徴とするその具体例を示す[7]．MIM 素子の場合，陽極酸化によって形成された Ta_2O_5 薄膜を流れる Poole-Frenkel 電流が利用されるので，動作電圧が低い利点を有するが，動作特性の温度に依存することが難点である．

バリスタ形では，少量の Bi_2O_3 や Nr_2O_3 などを添加した焼結 ZnO バリスタをスイッチング素子とキャパシタとして用いる．この場合，ZnO の粒界に存在する絶縁層間を流れるトンネル電流が利用されるために，動作特性の温度依存性は小さい．しかしながら，ZnO の粒径分布の組成に基づく動作特性のばらつきは，基本的に避けられない．

ダイオード形には，2個の a-Si 形ショットキーダイオードを互いに逆向きに直列接続することで双極形な特性を持つ back-to-back ダイオード方式，2個の a-Si 形 pin ダイオードを互いに逆向きに直列接続したダイオードリング方式などがある．

図 1.12 MIM スイッチの構造

図 1.11 に，3端子素子を用いたアクティブマトリクス駆動による LCD の動作原理を示す．[illegible] この生産に関係してホール回路から信号別電圧 (ドレインバス) V_1, V_2, …, V_n を介し，この選択線の3端子素子に結合している．キャパシタに信号電荷を蓄積する．この信号電荷は，次のフレームの走査までこのゲートバス上の全画素の液晶を駆動し続ける．

なお，3端子素子のしゃ断 (off) 時の内部抵抗が十分に大きい場合や，

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin Fukita
Group Art Unit:	2629
Examiner:	Bao Quan T. Ho
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Director of the United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant hereby submits an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS, AND OTHER INFORMATION

The patents, publications and other information requested to be considered by the Office (except unpublished U.S. patent applications) are listed on Form 1449 attached hereto.

II. COPIES

A. ☒ Submitted herewith is a legible copy of (i) each foreign patent; (ii) each publication or that portion which caused it to be listed, other than U.S. patents and U.S. patent application publications unless required by the Office; (iii) each unpublished U.S. application listed below in Section IV (i.e., including the specification, claims, and any drawing of the application, or that portion of the application which caused it to be listed, including any claims directed to that portion), except for such applications filed on or after June 30, 2003, pursuant to the Waiver of the Copy Requirement in 37 C.F.R. 1.98 (OG Notice dated October 19, 2004); and (iv) all other information or that portion which caused it to be listed.

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B. ☐ Any patents, publications or other information which are listed on Form 1449 or on the copies of PTO-892, but which are not enclosed herewith, were previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Serial Number	U.S. Filing Date

C. ☐ This is a PCT application in the entry of the National Phase in the United States. A copy of the International Search Report is attached for the Examiner's information. The documents listed on the International Search report are listed on the attached Form 1449 for consideration by the Examiner and for listing on any patent resulting from this application. If the International Search report was from the US, EPO, or JPO search authorities, copies of these references should have been supplied to the USPTO under the trilateral agreement and are believed to be in the file of the above-identified application. (MPEP 1893.03(g).)

III. CONCISE EXPLANATION OF THE RELEVANCE (check at least one box)

A. ☐ Except as may be indicated below in (B), all of the patents, publications or other information are in the English language (concise explanation not required).

B. ☒ A concise explanation of the relevance of each patent, publication or other information listed that is not in the English language is as follows (see 37 C.F.R. § 1.98(a)(3)):

1. ☐ See the attached foreign patent office communication from a counterpart foreign application:

2. ☒ English translations are provided.

3. ☐ Other:

C. ☐ The following additional information is provided for the Examiner's consideration.

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IV. CROSS REFERENCE TO RELATED APPLICATION(S)

A. ☐ The Examiner is advised that the following co-pending application(s) contain(s) subject matter that may be related to the present application. By bringing this(these) application(s) to the Examiner's attention, Applicant(s) does (do) not waive the confidentiality provisions of 35 U.S.C. § 122.

Serial No.	Filing Date	Inventor(s)

V. THIS IDS IS BEING FILED UNDER

A. ☐ **37 C.F.R. § 1.97(b):** (check only one box)

1. ☐ within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) (37 C.F.R. § 1.97(b)(1)). No fee or certification is required.

2. ☐ within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or certification is required.

3. ☐ before the mailing of a first Office Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or certification is required. In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the certification under 37 C.F.R. § 1.97(e) below; or, if no certification has been made, charge our deposit account a fee in the amount of $180.00 as required by 37 C.F.R. § 1.17(p).

4. ☐ before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No fee or certification is required.

B. ☒ **37 C.F.R. § 1.97(c):** (check only one box)

before the mailing date of either any Final Office Action under 37 C.F.R. § 1.113, a Notice of Allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution.

1. ☒ No certification; therefore, a fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

2. ☐ See the certification below. No fee is required.

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C. ☐ **37 C.F.R. § 1.97(d):**

after the mailing date of either a Final Office Action under 37 C.F.R. § 1.113 or a Notice of Allowance under 37 C.F.R. § 1.311, yet on or before payment of the issue fee.

1. ☐ See the certification below. A fee in the amount of $180.00 is required by 37 C.F.R. § 1.17(p).

VI. CERTIFICATION UNDER 37 C.F.R. § 1.97(e): (check only one box)

The undersigned hereby certifies that:

A. ☐ each item of information contained in this IDS was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS (See 37 C.F.R. § 1.97(e)(1)). See further statement under 37 C.F.R. 1.704(d) below in section VII, if applicable; or

B. ☐ no item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS (See 37 C.F.R. § 1.97(e)(2)).

C. ☐ some of the items of information were first cited in a communication from a foreign patent office. As to this information, the undersigned hereby certifies that each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby certifies that no item of this remaining information contained in this IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS.

VII. STATEMENT UNDER 37 C.F.R. 1.704(d)

The undersigned hereby states that:

☐ each item of information contained in this IDS was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this IDS.

VIII. PAYMENT OF FEES (check only one box, if applicable)

A. ☐ A check in the amount of $180.00 is enclosed for the above-identified fee.

B. ☒ Please charge Deposit Account No. 50-3213 in the amount of $180.00 for the above-identified fee. A duplicate copy of this paper is attached.

Please charge any additional fees or credit any overpayment pursuant to 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 50-3213.

The above references are being cited only in the interest of candor and without any admission that they constitute statutory prior art, contain matter which anticipates the invention, or which would render the same obvious, either singly or in combination, to a person of ordinary skill in the art. Furthermore, this Information Disclosure Statement shall not be construed as a representation that a search has been made.

If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule (with a petition if necessary) and charge the appropriate fee to Deposit Account No. 08-0750.

Respectfully submitted,

Dated: September 17, 2008

By: /Bryant E. Wade/
G. Gregory Schivley
Reg. No. 27,382
Bryant E. Wade
Reg. No. 40,344

Harness, Dickey & Pierce, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
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GGS/BEW

IPR2025-01396
BOE EXHIBIT 1003
Page 403 of 473

Electronic Patent Application Fee Transmittal

Application Number:	10914044
Filing Date:	06-Aug-2004
Title of Invention:	Electro-optical panel,system with terminals having different corresponding characteristics
First Named Inventor/Applicant Name:	Shin Fujita
Filer:	Bryant Edward Wade/Patricia Dennis
Attorney Docket Number:	9319S-000838

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	3957192
Application Number:	10914044
International Application Number:	
Confirmation Number:	5848
Title of Invention:	Electro-optical panel,system with terminals having different corresponding characteristics
First Named Inventor/Applicant Name:	Shin Fujita
Customer Number:	27572
Filer:	Bryant Edward Wade/Patricia Dennis
Filer Authorized By:	Bryant Edward Wade
Attorney Docket Number:	9319S-000838
Receipt Date:	17-SEP-2008
Filing Date:	06-AUG-2004
Time Stamp:	14:15:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	18808
Deposit Account	503213
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment.pdf	96212 c15e44d3ed9c4a309221cad77bf7b4d4923096c5	yes	15

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	2
Claims	3	9
Applicant Arguments/Remarks Made in an Amendment	10	15

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	1449.pdf	44103 1ccfd66befd6b95b5718600f2ea5b9baf2af93c8	no	1

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

3	NPL Documents	LiquidCrystalDisplayTechnologyReference.pdf	357395 7d565fe5c9dcfa6438dae40353c8b4545e21ea7f	no	7

Warnings:

Information:

4	Information Disclosure Statement Letter	IDS.pdf	60637 4d24fd20af0f2929bc16333317078cc31e9047a2	no	5

Warnings:

Information:

5	Fee Worksheet (PTO-06)	fee-info.pdf	30098 f7982ecf337f276e6df3fd63cc65eb595863de6a	no	2

Warnings:

Information:

Total Files Size (in bytes):	588445

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

27572 7590 01/23/2009

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
HO, BAO QUAN T	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
01/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/914,044	FUJITA, SHIN	
	Examiner	Art Unit	
	BAO-QUAN T. HO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,9-11 and 14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5,9-11,14 and 17* is/are allowed.

6)☒ Claim(s) *15,16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The amendment filed on 05/21/2008 has been entered and considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-16, and 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade, US Patent 6,262,702, and in view of "Liquid Crystal Display Technology", by Shoichi Matsumoto (hereafter referenced as Matsumoto), and further in view of Onishi, US Patent 6,469,767.

As to claim 15, Murade discloses an electro-optical panel comprising:

a first substrate (Substrate 1, FIG. 3);

data lines (35, FIG. 1);

scanning lines (31, FIG. 1) intersecting the data lines;

pixels (11, FIG. 1) disposed corresponding to intersections between the data lines and the scanning lines;

a clock-signal input terminal (CLY terminal, seen in FIG. 1) supplied with a clock signal (CLY) and connected to a mounting member (Layer 42, FIG. 3 and Col. 19 lines 34-44) through anisotropic conductive film (Col. 35 lines 19-28);

image-signal input terminals (VID1-6 terminals, seen in FIG.1) supplied with image signals (VID1-6) and connected to the mounting member (Layer 42, FIG. 3 and Col. 19 lines 34-44) through anisotropic conductive film (Col. 35 lines 19-28), the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate (Seen in FIG. 1), the image signals being supplied from an external data drive circuit (information processing circuit 1002, FIG. 14) and being supplied simultaneously to all of the data lines (Data lines 35 may be selected line by line or more data lines may be selected at the same time, Col. 16 lines 34-36. Although Murade does not specifically state “all” data lines, as applicant stated in Applicant’s remarks 09/17/2008 on page 11, the Matsumoto teaches supplying all data lines simultaneously. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention for Murade to supply all data lines simultaneous as taught by Matsumoto for the purpose of faster operation); and

Murade also discloses a scanning-line drive circuit (104) that is formed on the first substrate (Seen in FIG. 1) and that sequentially (shift register) transmits a transmission start pulse (Start signal DY) in synchronization with the clock signal (CLY, Col. 15 lines 57-65, although it does not specifically recite "in synchronization"; it would have been obvious to one of ordinary skill in the art at the time of invention to have provided the start pulse in synchronization with the clock signal as Murade provided with the shift register 101a, wherein the start signal DX and clock signals CLX are provided in synchronized, Col. 21 lines 8-44 and seen in FIG. 6b),

but Murade does not specifically disclose wherein the clock-signal input terminal has a larger area than at least one of the image-signal input terminals.

However, Onishi discloses in FIG. 2 wherein the plurality terminals (43) for inputting serial data and a shift clock (see col. 6, lines 38-42). As shown in Figure 2, the right most terminals (43) have larger area than the left most terminals (43). Since Murade teaches the clock terminal located on right most of the plural terminals, thus combining Murade and Onishi would meet the claimed "the clock-signal input terminal (Shift clock of the right most Plural Terminals 43, col. 6 lines 38-42) has a larger area (seen in FIG. 1) than the image-signal input terminal (Serial data of the left most Plural Terminals 43, col. 6 lines 38-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the arrangements of the terminals as taught by Onishi but maintaining the terminal orders of Murade as modified by Matsumoto to have the clock signal terminal arrangement be made to the right outer most terminal of as like Onishi, while the image signal terminal is the left most terminal as like the plural terminal 43 in reference Onishi, wherein the clock terminal is larger than the image terminal as like the reference of Onishi for the purpose of providing efficient amount of space of the display panel (col. 3 lines 54-60).

As to claim 16, Murade in view of Onishi discloses the clock signal input terminal having a smaller resistance compared with resistance of the image signal input terminal (As an electrical trait, larger the terminal becomes that the resistance reduces,

therefore the clock signal terminal will have a smaller resistance than the image signal terminal because the clock signal terminal is larger than the image signal terminal).

As to claim 18, Murade discloses the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal (Seen in FIG. 1, image-signal terminals VID 1-6 are closer to a center than the clock-signal terminal CLY).

As to claim 19, Murade discloses the external data line circuit (1002) being formed on a second substrate other than the first substrate (Circuit 1002 is mounted on substrate 1322, seen in FIG. 18).

As to claim 20, Murade discloses the clock-signal imputer terminal being disposed further out on the first substrate relative to the central part of an outer edge of the first substrate than the image signal input terminal (Seen in FIG. 1, image-signal terminals VID 1-6 are closer to a center than the clock-signal terminal CLY).

As to claim 21, Murade discloses the pixels arrange on the first substrate (seen in FIG. 1).

As to claim 22, Murade discloses the mounting member comprising a flexible substrate (Tape Carrier Package 1320) and an external substrate (Substrate 1322) that are different than the first substrate (Seen in FIG. 18, Col. 35 lines 19-28).

As to claim 23, Murade discloses an electro-optical panel comprising:

data lines (35, FIG. 1);

scanning lines (31, FIG. 1) intersecting the data lines;

pixels (11, FIG. 1) disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal (CLY terminal, seen in FIG. 1) supplied with a clock signal (CLY);

an image signal input terminal (VID1-12 terminals, seen in FIG.1) supplied with an image signal (VID1-12);

a scanning line drive circuit (104) that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals (Col. 26 lines 5-29); and

a substrate (1, FIG. 1) the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal (Seen in FIG. 1, image-signal terminals VID 1-6 are closer to a center than the clock-signal terminal CLY).

Allowable Subject Matter

4. Claims 1-3, 5, 9-11, 14, and 17 are allowed.

Response to Arguments

5. Applicant's arguments filed 09/17/2008 have been fully considered but they are not persuasive.

6. Applicant's arguments with respect to claim 15 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 12, “Murade does not disclose the forming of an image signal input and a clock signal input on a different layer…”, however this limitation is not recited in the amended claim 15. Applicant states, “Murade appears to disclose the forming of a scanning line driver circuit, an image signal input and a clock signal input on the same insulating layer of a single substrate. As shown in FIGS. 1 and 3, the insulating layer 42 is on top of substrate 1, which reads on the "clock-signal input terminal ... connected to a mounting member", the "image-signal input terminals ... connected to the mounting member", and the “scanning-line drive circuit that is formed on the first substrate” of the amended claim 15.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BAO-QUAN T. HO whose telephone number is (571)270-3264. The examiner can normally be reached on M-F, 8:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	4131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/24/2007	03/20/2008	06/15/2008	01/21/2009					
	1	✓	=	=	=					
	2	✓	=	=	=					
	3	✓	=	=	=					
	4	✓	-	-	-					
	5	✓	=	=	=					
	6	✓	-	-	-					
	7	✓	✓	-	-					
	8	✓	-	-	-					
	9	✓	=	=	=					
	10	✓	=	=	=					
	11	✓	=	=	=					
	12	✓	✓	-	-					
	13	✓	✓	-	-					
	14	✓	=	=	=					
	15			✓	✓					
	16			✓	✓					
	17			=	=					
	18				✓					
	19				✓					
	20				✓					
	21				✓					
	22				✓					
	23				✓					

FORM HDP-1449 (Based on Form PTO-1449) **PATENT AND TRADEMARK OFFICE** **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary) Sheet 1 of 1	ATTORNEY DOCKET NO.	APPLICATION NO.
	9319S-000838	10/914,044
	APPLICANT	
	Shin Fukita	
	FILING DATE	GROUP
	August 6, 2004	2629

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)		
Ref. Desig.	Examiner's Initials	
1.	/B.T.H./	Liquid Crystal Display Technology, by Shoichi Matsumoto, published 1996, pages 10, 14-15, 70-71, and 326-327, Figures 1.11 and 2.14.

Examiner: /Bao-Quan Ho/	Date Considered: 01/21/2009

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO/SB/30 (01-09)
Approved for use through 02/28/2009. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Request For Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/914,044
Filing Date	August 6, 2004
First Named Inventor	Shin Fujita
Art Unit	2629
Examiner Name	Bao Quan T. Ho
Attorney Docket Number	9319S-000838

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
ii. ☐ Other _____

b. . ☒ Enclosed

i. ☒ Amendment/Reply
ii ☐ Affidavit(s)/Declaration(s)
iii. ☐ Information Disclosure Statement (IDS)
iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) **required**)

b. ☐ Other _____

3. Fees The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No.50-3213

i. ☒ RCE fee required under 37 C.F.R. 1.17(e)
ii. ☐ Extension of time fee (37 C.F.R. 1.136 and 1.17)
iii. ☐ Other _____

b. ☐ Check in the amount of $ _____ enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/G. Gregory Schivley/	*Date*	April 14, 2009
Name (Print /Type)	G. Gregory Schivley	*Registration No. (Attorney/Agent)*	27,382

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, e-filed, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below:

Signature	N/A	*Date*	
Name (Print /Type)			

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

14462771.1

Electronic Patent Application Fee Transmittal

Application Number:	10914044
Filing Date:	06-Aug-2004
Title of Invention:	Electro-optical panel,system with terminals having different corresponding characteristics
First Named Inventor/Applicant Name:	Shin Fujita
Filer:	G. Gregory Schivley/Mary Aiello
Attorney Docket Number:	9319S-000838

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	5150185
Application Number:	10914044
International Application Number:	
Confirmation Number:	5848
Title of Invention:	Electro-optical panel,system with terminals having different corresponding characteristics
First Named Inventor/Applicant Name:	Shin Fujita
Customer Number:	27572
Filer:	G. Gregory Schivley/Mary Aiello
Filer Authorized By:	G. Gregory Schivley
Attorney Docket Number:	9319S-000838
Receipt Date:	14-APR-2009
Filing Date:	06-AUG-2004
Time Stamp:	14:16:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

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Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	456
Deposit Account	503213
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment_after_Final_Office_Action.PDF	51620 128684ef46181f806d39309288b682aa579922a3	yes	12

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment After Final	1	1
Claims	2	9
Applicant Arguments/Remarks Made in an Amendment	10	12

Warnings:

Information:

2	Request for Continued Examination (RCE)	Request_for_Continued_Examination.PDF	31043 5e57a4bf83e75e7e66bb6fae4ba3f4242f947989	no	1

Warnings:

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Information:

3	Fee Worksheet (PTO-06)	fee-info.pdf	30071 852e6e581c7ffce569f1e59084fa64016183f7a0	no	2

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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin Fujita
Group Art Unit:	2629
Examiner:	Bao-Quan T. Ho
Title:	ELECTRO-OPTICAL PANEL, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC SYSTEM
Attorney Docket:	9319S-000838

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT AFTER FINAL OFFICE ACTION

Sir:

In response to the Office Action mailed January 23, 2009, please amend the application as follows and consider the remarks set forth below. A Request for Continued Examination (RCE) is submitted herewith.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) An electro-optical panel comprising:

a plurality of data lines;

a plurality of scanning lines intersecting the plurality of data lines;

a plurality of pixels disposed corresponding to the intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a scanning line clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that sequentially transmits a transmission start pulse in synchronization with the scanning line clock signal and outputs a scanning signal to each of the plurality of scanning lines, image signals from the plurality of data lines are supplied to pixels selected by the scanning signals;

a drive circuit which controls a grayscale of the pixels based on the scanning line clock signal and the image signal; and

a third input terminal, wherein the third input terminal comprises a power source terminal supplied with a power source, and the area of the third input terminal is not smaller than that of the first clock signal input terminal,

wherein the clock signal input terminal has a larger area than the image signal input terminal, and

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wherein a plurality of the power source terminals, a plurality of the first clock signal input terminals, and a plurality of the second image signal input terminals are included;

the plurality of the power source terminals, the plurality of the first clock signal input terminals, and the plurality of the second image signal input terminals are formed in line on a substrate; and

a pitch interval of the adjacent first clock signal input terminals is an integer multiple of a pitch interval of the adjacent second image signal input terminals.

2. (Previously Presented) An electro-optical panel according to Claim 1, wherein the first clock signal input terminal has a smaller input resistance compared with the image signal input terminal.

3. (Previously Presented) An electro-optical panel according to Claim 1, wherein a signal supplied to the clock signal input terminal comprises a driving signal supplied to the scanning-line drive circuit.

4. (Cancelled).

5. (Previously Presented) An electro-optical panel according to Claim 1, wherein the clock signal input terminal and the image signal input terminal, which are disposed along an edge of a substrate, are formed in line, the image signal input terminal is disposed in the central part of the substrate, and the clock signal input terminal is disposed at the outer side of the substrate.

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6-8. (Cancelled).

9. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 1;

power source means for supplying the power source; and

signal generation means for supplying the input signals.

10. (Previously Presented) An electro-optical apparatus comprising:

an electro-optical panel set forth in Claim 9;

an external substrate which includes power source means for supplying the power source and signal generation means for supplying the input signals; and

a flexible substrate which connects the external substrate and the electro-optical panel,

wherein the flexible substrate is connected to the plurality of power source terminals, the plurality of clock signal input terminals and the plurality of image signal input terminals through an anisotropic conductive film.

11. (Previously Presented) An electro-optical apparatus according to Claim 10, wherein wiring lines are formed corresponding to a reference pitch interval of the image signal input terminals on the flexible substrate.

12-13. (Cancelled).

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14. (Original) An electronic system comprising the electro-optical apparatus set forth in Claim 1.

15. (Currently Amended) An electro-optical panel comprising:

a first substrate;

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock-signal input terminal supplied with a clock signal and connected to a mounting member through anisotropic conductive film;

image-signal input terminals supplied with image signals and connected to the mounting member through anisotropic conductive film, the clock-signal input terminal and the image-signal input terminals being disposed along one side of the first substrate, the image signals being supplied from an external data drive circuit and being supplied simultaneously to all of the data lines; and

a scanning-line drive circuit that is formed on the first substrate and that sequentially transmits a transmission start pulse in synchronization with the clock signal,

wherein the clock-signal input terminal ~~connected to~~ overlaps a first wiring of the mounting member through said anisotropic conductive film [[has]]by a larger area than an area at which at least one of the image-signal input terminals ~~connected to~~ overlaps a second wiring of the mounting member through said anisotropic conductive film.

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16. (Previously Presented) The electro-optical panel according to Claim 15, the clock-signal input terminal having a smaller resistance compared with resistance of the image signal input terminal.

17. (Previously Presented) The electro-optical panel according to Claim 1, further comprising a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal.

18. (Previously Presented) The electro-optical panel according to Claim 15 the clock-signal input terminal and the image-signal input terminal arranged in a line on an edge of the first substrate, the image-signal input terminal being disposed closer to a center of the edge of the first substrate than the clock-signal input terminal.

19. (Previously Presented) The electro-optical panel according to Claim 15, the external data line circuit being formed on a second substrate other than the first substrate.

20. (Previously Presented) The electro-optical panel according to Claim 15, the clock-signal input terminal being disposed further out on the first substrate relative to a central part of an outer edge of the first substrate than the image signal input terminal.

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21. (Previously Presented) The electro-optical panel according to Claim 15, the pixels arranged on the first substrate.

22. (Previously Presented) The electro-optical panel according to Claim 15, the mounting member comprising a flexible substrate and an external substrate that are different than the first substrate.

23. (Currently Amended) An electro-optical panel comprising:

a substrate;

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals~~; and~~,

wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate; and

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~~a substrate, the clock signal input terminal and the image signal input terminal arranged in a line on an edge of the substrate, and the image signal input terminal disposed closer to a center of an edge of the substrate than the clock signal input terminal~~a mounting member that is distinct from and connected to the substrate, the mounting member comprising:

a first wiring that is connected to the clock signal input terminal; and

a second wiring that is connected to the image signal input terminal,

wherein contact area between the first wiring and the clock signal input terminal is greater than contact area between the second wiring and the image signal input terminal.

24. (New) The electro-optical panel according to Claim 15, wherein each of the first wiring and the second wiring comprise at least one wire.

25. (New) The electro-optical panel according to Claim 15, wherein contact area between the clock signal input terminal and the first wiring is greater than contact area between the at least one of the image signal input terminals and the second wiring.

26. (New) The electro-optical panel according to Claim 15, wherein the mounting member is distinct from and connected to the first substrate.

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27. (New) The electro-optical panel according to Claim 26, wherein the mounting member is electrically and mechanically connected to a terminal group of the first substrate that comprises the clock signal input terminal and the image signal input terminals.

28. (New) The electro-optical panel according to Claim 15, wherein the clock signal input terminal and the at least one of the image signal input terminals are connected between the substrate and the mounting member.

29. (New) The electro-optical panel according to Claim 15, wherein the mounting member is implemented as a flexible cable that is connected to the substrate over the clock signal input terminal and over the image signal input terminals.

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REMARKS

Claims 1-3, 5, 9-11 and 14-23 were pending in the application. New Claims 24-29 are presented herein. Accordingly, Claims 1-29 are now pending in the application. Claims 15 and 23 are amended herein. Support for the amendments and new claims can be found throughout the written description, claims, and drawings as originally filed. Therefore, no new matter has been added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 15-16 and 18-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murade (U.S. Pat. No. 6,262,702) in view of "Liquid Crystal Display Technology," by Shoichi Matsumoto (hereinafter referred to as Matsumoto) and Onishi (U.S. Pat. No. 6,469,767). This rejection is respectfully traversed.

With respect to Claim 15, Murade, Matsumoto and Onishi do not show, teach or suggest a panel with a clock-signal input terminal that overlaps a first wiring of a mounting member by a larger area than an area at which an image-signal input terminal overlaps a second wiring of the mounting member. This is shown and described at least in FIG. 4 and paragraph [0058] of the present application, where an example of a different number of wiring lines L are used for respective terminals 20 of terminal group 10.

As best understood by Applicant, the contact surface areas between terminals and wiring in each of Murade and Onishi appear to be the same. Murade and Onishi

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are silent with respect to the contact surface areas between wiring and terminals. It appears from the figures of each of Murade and Onishi that the wiring associated with each input terminal is the same. For example and with respect to Murade, the contact areas between the wiring 105 and each of the terminals 102 of FIG. 1 appear to be the same. As another example and with respect to Onishi, the contact areas between the wiring 41, 42 and each of the terminals 43 and parts 40, 42 of FIG. 1 appear to be the same.

With respect to the mounting member of Claim 1, although in FIG. 18 Murade discloses a tape carrier package that is mounted on a substrate 1, Murade is silent with respect to the wiring of the tape carrier package relative to terminals on the substrate 1. Onishi does not appear to disclose a substrate and terminals that overlap wiring of a mounting member.

Matsumoto does not appear to disclose or describe a contact area relationship between wiring and terminals, as claimed. Thus, the relied upon references do not disclose each and every element of Claim 15.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03.

Therefore, Claim 15 is allowable for at least the above reasons. Claim 23 is allowable for at least similar reasons. Claims 16, 18-22 and 24-29 ultimately depend from Claim 15 and are allowable for at least similar reasons.

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ALLOWABLE SUBJECT MATTER

Claims 1-3, 5, 9-11, 14 and 17 are allowed.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: April 14, 2009

By: /G. Gregory Schivley/
G. Gregory Schivley
Reg. No. 27,382

Bryant E. Wade
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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/914,044	08/06/2004	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	04/14/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 23	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

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Legal Instrument Examiner:
/DEBRA a. SAVOY/

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27572 7590 08/06/2009

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
WALTHALL, ALLISON N	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/06/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

TITLE OF INVENTION: ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	11/06/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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PART B - FEE(S) TRANSMITTAL

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(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

TITLE OF INVENTION: ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS

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nonprovisional	NO	$1510	$300	$0	$1810	11/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
WALTHALL, ALLISON N	2629	345-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

27572 7590 08/06/2009

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
WALTHALL, ALLISON N	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/06/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 763 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 763 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/914,044	FUJITA, SHIN	
	Examiner	Art Unit	
	ALLISON WALTHALL	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed 4/14/2009*.

2. ☒ The allowed claim(s) is/are *1-3,5,9-11 and 14-29*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/11/2004, 3/7/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Allison Walthall/ Examiner, Art Unit 2629	/Chanh Nguyen/ Supervisory Patent Examiner, Art Unit 2629

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Bryant Wade on 7/8/2009.

The application has been amended as follows:

Claim 23. An electro-optical panel comprising:

a substrate;

data lines;

scanning lines intersecting the data lines;

pixels disposed corresponding to intersections between the data lines and the scanning lines;

a clock signal input terminal supplied with a clock signal;

an image signal input terminal supplied with an image signal;

a scanning line drive circuit that outputs scanning signals to the scanning lines, image signals from the data lines supplied to the pixels are selected by the scanning signals;

wherein the data lines, the scanning lines, the pixels, the clock signal input terminal and the image signal input terminal are implemented on the substrate; and

a mounting member that is distinct from and connected to the substrate, the mounting member comprising:

a first wiring that is connected to the clock signal input terminal; and

a second wiring that is connected to the image signal input terminal,

~~wherein contact area between the first wiring and the clock signal input terminal is greater than contact area between the second wiring and the image signal input terminal.~~

wherein the clock signal input terminal overlaps the first wiring of the mounting member by a larger area than an area at which at least one of the image signal input terminals overlaps the second wiring of the mounting member.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLISON WALTHALL whose telephone number is (571)270-3571. The examiner can normally be reached on Mon - Fri 9:30-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

anw
July 8, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	ALLISON WALTHALL	2629

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/24/2007	03/20/2008	06/15/2008	01/21/2009	07/08/2009				
1	1	✓	=	=	=	=				
2	2	✓	=	=	=	=				
3	3	✓	=	=	=	=				
	4	✓	-	-	-	-				
4	5	✓	=	=	=	=				
	6	✓	-	-	-	-				
	7	✓	✓	-	-	-				
	8	✓	-	-	-	-				
5	9	✓	=	=	=	=				
6	10	✓	=	=	=	=				
7	11	✓	=	=	=	=				
	12	✓	✓	-	-	-				
	13	✓	✓	-	-	-				
8	14	✓	=	=	=	=				
10	15			✓	✓	=				
11	16			✓	✓	=				
9	17			=	=	=				
12	18				✓	=				
13	19				✓	=				
14	20				✓	=				
15	21				✓	=				
16	22				✓	=				
23	23				✓	=				
17	24					=				
18	25					=				
19	26					=				
20	27					=				
21	28					=				
22	29					=				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(clock with terminal with overlap with wiring).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:36
L2	4	(clock with terminal with contact with wiring).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:37
L3	2	(clock with terminal with mounting with wiring). clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:37
L4	4	(clock with terminal with image with terminal with wiring).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:38
L5	0	(clock with terminal with area with pitch).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:39
L6	12	(terminal with pitch interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/07/08 13:39
S1	2	(("6262702") or ("6469767")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/06/02 12:50
S2	2165	(LCD or liquid crystal display) and (terminal or pad) with anisotropic with film	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 13:45

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S3	156	(LCD or liquid crystal display) and (terminal or pad) with anisotropic with film with (wire or wiring or line) and (data or image) signal and clock and power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 13:45
S4	101	(LCD or liquid crystal display) and (terminal or pad) with area with (wire or wiring or line) and (data or image) signal and clock and power and FPC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 13:55
S5	12	(LCD or liquid crystal display) and (terminal or pad) with area with (data or image) signal and (terminal or pad) with (clock) with area	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 14:08
S6	55	(terminal or pad) with area with (data or image) signal and (terminal or pad) with (clock) with area	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 14:12
S7	8	(contact) with area with (data or image) signal and (contact) with (clock) with area	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 14:16
S8	2331	345/204.ccls. and (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 14:18
S9	303	345/204.ccls. and (terminal or pad) with (area or size)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 14:18
S10	5403	display and clock with (terminal or pad or contact) and (data or image or source or video) with (terminal or pad or contact) and (FPC or IC or flexible cable)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 15:08

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S11	1721	S10 and (terminal or pad or contact) with (area or size or width)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 15:08
S12	5	S11 and clock with (terminal or pad or contact) with (area or size or width) with (bigger or greater or larger or wider)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 15:10
S13	4	"6876000"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 15:14
S14	86	external with terminal with larger with data with terminal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 15:18
S15	290	hitachi.as. and external with terminal and data with terminal and display. ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/02 16:04
S16	5667	(external or clock or power) with (terminal or pad) same (bigger or larger or wider) same (data or image or source or video) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 12:37
S17	1314	(external or clock or power) with (terminal or pad) with (bigger or larger or wider) with (data or image or source or video) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 12:37
S18	352	display and (external or clock or power) with (terminal or pad) with (bigger or larger or wider) with (data or image or source or video) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 12:38

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S19	202	(LCD or liquid crystal display) and (external or clock or power) with (terminal or pad) with (bigger or larger or wider) with (data or image or source or video) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 12:39
S20	2	"7088350".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 12:47
S21	0	("2006/0022969").URPN.	USPAT	ADJ	ON	2009/06/03 13:58
S22	1	"6897909".pn.	USPAT	ADJ	ON	2009/06/03 14:05
S23	9	("5241304" | "5841414" | "5926157" | "5945984" | "5953003" | "6670940" | "6771239").PN. OR ("6985128").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 14:22
S24	1698	(LCD or liquid crystal display) and terminal with pitch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 14:50
S25	128	(LCD or liquid crystal display) and terminal with pitch with (bigger or larger or wider)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 14:50
S26	1	("2004/0036833").URPN.	USPAT	ADJ	ON	2009/06/03 15:06
S27	8	("20010026345" | "20040036833" | "20050162577" | "20060086532" | "20060118786" | "20060232533" | "20070085960" | "6583845").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 15:06
S28	5	("6107685" | "6657137" | "6750549" | "6940176" | "6940178").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 15:11
S29	314	kimura.in. and terminal and semiconductor.as.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 15:23

S30	40	monzen.in.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 15:39
S31	3	JP 2000-312070	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 15:49
S32	1	JP2000312070	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 15:51
S33	2	JP "2000312070"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 15:51
S34	1	2001-047626.NRAN.	DERWENT	ADJ	ON	2009/06/03 15:51
S35	2	"6750838".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 16:06
S36	2	"20040080478".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/03 16:17
S37	25	("5043714" | "5168270" | "5192945" | "5196738" | "5457482" | "5543824" | "5574475" | "5585816" | "5598180" | "5643826" | "5648277" | "5771031" | "5801674" | "5907313" | "5923962" | "5949397"). PN. OR ("6750838"). URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/03 16:18
S38	529	349/150.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 12:58

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S39	333	S38 and @ad<"20030808"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 12:59
S49	954	349/149-152.ccls. and (pitch or size or width or area) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:23
S50	589	S49 and @ad<"20030808"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:23
S51	40	S50 and (clock or timing) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:24
S52	671	349/152.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:51
S53	38	S52 and (clock or timing) with (terminal or pad)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:51
S54	2	"6982568".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 13:54

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S55	20	("20010030729" | "20020027634" | "20020044242" | "20020145697" | "20020191140" | "20030103184" | "20030128326" | "20030174271" | "20030180975" | "20030227592" | "20040165138" | "20040239863" | "20050157244" | "5530568" | "5872610" | "5986723" | "6198522" | "6522378" | "6828817" | "6862071").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2009/06/04 13:58
S58	201	S52 and pitch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 14:12
S59	145	S52 and (two or multiple or additional) with (wire or wiring or line) with (pad or terminal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 14:29
S60	40	S52 and (two or multiple or additional) near2 (wire or wiring or line) with (pad or terminal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2009/06/04 14:29

7/8/2009 1:40:22 PM
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OIPE JC181 NOV 1 1 2004 PATENT & TRADEMARK OFFICE

FORM HDP-1449 (Based on Form PTO-1449)	ATTORNEY DOCKET NO.	SERIAL NO.
PATENT AND TRADEMARK OFFICE	9319S-000838	10/914,044
INFORMATION DISCLOSURE CITATION	APPLICANT	
(Use several sheets if necessary)	Shin Fujita	
Sheet 1 of 1	FILING DATE	GROUP
	8/6/2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.	/A.W./	2822558	Sept/1998	Japan	.....	Abstract	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.		

*One or more of the English translation documents submitted herewith may be Abstracts only or partial machine created translations from the Japanese Patent Office. As such, the submitter does not necessarily vouch for their accuracy. Additional information may be obtained from the Japanese Patent Office web site at www.jpo.go.jp

Examiner: /Allison Walthall/	Date Considered: 07/17/2009

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE IAP50 MAR 07 2006 PATENT & TRADEMARK OFFICE

FORM HDP-1449 (Based on Form PTO-1449)

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INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Sheet 1 of 1

ATTORNEY DOCKET NO.	SERIAL NO.
9319S-000838	10/914,044
APPLICANT	
Shin FUJITA	
FILING DATE	GROUP
August 6, 2004	2673

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.						

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation * Yes	No
1.	/A.W./	2003-152019A	05/23/2003	Japan		X	
2.	/A.W./	2003-216064A	07/30/2003	Japan		X	
3.	/A.W./	11-223832A	08/17/1999	Japan		X	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.	/A.W./	Examination result regarding corresponding Japanese application 02/06/06

*One or more of the English translation documents submitted herewith may be Abstracts only or partial machine created translations from the Japanese Patent Office. As such, the submitter does not necessarily vouch for their accuracy. Additional information may be obtained from the Japanese Patent Office web site at www.jpo.go.jp

Examiner:	/Allison Walthall/	Date Considered:	07/17/2009

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5848

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/914,044	08/06/2004 RULE	345	2629	9319S-000838

APPLICANTS
Shin Fujita, Suwa-shi, JAPAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
JAPAN 2003-290650 08/08/2003
JAPAN 2004-193515 06/30/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
10/06/2004

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☑ Yes ☐ No	/ALLISON N WALTHALL/ Examiner's Signature	☐ Initials	JAPAN	8	14	2

ADDRESS
HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303
UNITED STATES

TITLE
Electro-optical panel,system with terminals having different corresponding characteristics

FILING FEE RECEIVED		
1340	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	**Art Unit**
	ALLISON WALTHALL	2629

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED									
349	152	G	0	2	F	1 / 1345 (2006.0)										

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
345	204				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	17												
2	2	12	18												
3	3	13	19												
	4	14	20												
4	5	15	21												
	6	16	22												
	7	23	23												
	8	17	24												
5	9	18	25												
6	10	19	26												
7	11	20	27												
	12	21	28												
	13	22	29												
8	14														
10	15														
11	16														

/ALLISON WALTHALL/ Examiner.Art Unit 2629	7/8/2009	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	23	
/Chanh Nguyen/ Supervisory Patent Examiner.Art Unit 2629	07/16/2009	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10914044	FUJITA, SHIN
	Examiner	Art Unit
	Ho, Bao-Quan T	2629

SEARCHED			
Class	Subclass	Date	Examiner
345	60-100, 690-699, 204-213	10/02/07	BTH
349	149-152	10/02/07	BTH

SEARCH NOTES		
Search Notes	Date	Examiner
Updated Search	03/20/2008	BTH
Inventor Name Search (PALM)	03/20/2008	BTH
Updated Search	06/18/2008	BTH
updated EAST search	7/8/2009	anw

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see search history	7/8/2009	anw

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27572 7590 08/06/2009

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	08/06/2004	Shin Fujita	9319S-000838	5848

TITLE OF INVENTION: ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	11/06/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
WALTHALL, ALLISON N	2629	345-690000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Harness, Dickey & Pierce, P.L.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Seiko Epson Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 2

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 503213 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date November 6, 2009

Typed or printed name G. Gregory Schivley Registration No. 27,382

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IPR2025-01396
BOE EXHIBIT 1003
Page 459 of 473

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/914,044
Filing Date:	August 6, 2004
Applicant:	Shin FUJITA
Group Art Unit:	2629
Examiner:	Allison N. Walthall
Title:	ELECTRO-OPTICAL PANEL, SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS
Attorney Docket:	9319S-000838

Director of the United States Patent and Trademark Office
Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Reasons for allowance are only warranted in instances in which "the record of the prosecution as a whole does not make clear [the Examiner's] reasons for allowing a claim or claims." 37 C.F.R. 1.104 (e). In the present case, Applicant believes the record as a whole makes clear the reasons for allowance and therefore no statement by the Examiner is necessary or warranted, especially since the statement may unfairly focus on certain reasons for allowance which are not reflected by the prosecution history. Therefore, the record should reflect that Applicant does not necessarily agree with each statement in the reasons for allowance. For example, while Applicant believes the claims are allowable, Applicant may not unequivocally agree that patentability resides

solely in the specific feature or combination of features identified, or that each feature or combination of features identified is required for patentability, or that equivalents of any of the recited features are outside the scope of the claims. Moreover, to the extent the reasons for allowance do not separately address the subject matter of all the claims, Applicant does not acquiesce to any inference that the non-addressed claims fail to present other reasons for patentability apart from the patentability of the claims which were specifically addressed by the Examiner.

Respectfully submitted,

Dated: Nov 6, 2009

By: _____
G. Gregory Schivley
Reg. No. 27,382
Bryant E. Wade
Reg. No. 40,344

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

GGS/BEW/pvd

IPR2025-01396
BOE EXHIBIT 1003
Page 461 of 473

Electronic Patent Application Fee Transmittal

Application Number:	10914044
Filing Date:	06-Aug-2004
Title of Invention:	ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS
First Named Inventor/Applicant Name:	Shin Fujita
Filer:	G. Gregory Schivley/Rebecca Hartkopf
Attorney Docket Number:	9319S-000838

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	2	3	6
		Total in USD ($)		**1816**

Electronic Acknowledgement Receipt

EFS ID:	6407230
Application Number:	10914044
International Application Number:	
Confirmation Number:	5848
Title of Invention:	ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS
First Named Inventor/Applicant Name:	Shin Fujita
Customer Number:	27572
Filer:	G. Gregory Schivley/Rebecca Hartkopf
Filer Authorized By:	G. Gregory Schivley
Attorney Docket Number:	9319S-000838
Receipt Date:	06-NOV-2009
Filing Date:	06-AUG-2004
Time Stamp:	14:07:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1816
RAM confirmation Number	299
Deposit Account	503213
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PTOL-85.PDF	163156 31cfb3678982f37d2197f06e41df93f4c8febc46	no	1
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	Comments.PDF	84469 201a483354e44ec965190738fde7d5ad84a692d2	no	2
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	33924 2709c559e550755ba8ebf0aad65e119458bad610	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	281549		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/914,044	12/22/2009	7636146	9319S-000838	5848

27572 7590 12/02/2009

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 763 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shin Fujita, Suwa-shi, JAPAN;

Doc Code: PET.PTA.RCAL
Document Description: Request for Recalculation in view of Wyeth

PTO/SB/131 (01-10)
Approved for use through 02/28/2011. OMB 0651-0020
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR RECALCULATION OF PATENT TERM ADJUSTMENT IN VIEW OF *WYETH**

Attorney Docket Number: 9319S-000838/US	Patent Number: 7,636,146
Filing Date (or 371(b) or (f) Date): August 6, 2004	Issue Date: December 22, 2009
First Named Inventor: Shin Fujita	
Title: ELECTRO-OPTICAL PANEL, SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS	

PATENTEE HEREBY REQUESTS RECALCULATION OF THE PATENT TERM ADJUSTMENT (PTA) UNDER 35 USC 154(b) INDICATED ON THE ABOVE-IDENTIFIED PATENT. THE PATENTEE'S SOLE BASIS FOR REQUESTING THE RECALCULATION IS THE USPTO'S PRE-*WYETH* INTERPRETATION OF 35 U.S.C. 154(b)(2)(A).

Note: This form is only for requesting a recalculation of PTA for patents issued before March 2, 2010, if the sole basis for requesting the recalculation is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A). See Instruction Sheet on page 2 for more information.

Patentees are reminded that to preserve the right to review in the United States District Court for the District of Columbia of the USPTO's patent term adjustment determination, a patentee must ensure that he or she also takes the steps required under 35 U.S.C. 154(b)(3) and (b)(4) and 37 CFR 1.705 in a timely manner.

**Wyeth v. Kappos*, No. 2009-1120 (Fed. Cir., Jan. 7, 2010).

Signature /Jason A. Heist/	Date Feb. 17, 2010
Name (Print/Typed) Jason A. Heist	Registration Number 51,797

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below**.*

☑ *Total of 1 forms are submitted.

The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/131 (01-10)
Approved for use through 02/28/2011. OMB 0651-0020
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Instruction Sheet for:
REQUEST FOR RECALCULATION OF PATENT TERM ADJUSTMENT IN VIEW OF *WYETH**

(Not to be Submitted to the USPTO)

This form is only for requesting a recalculation of PTA for patents issued before March 2, 2010, if the sole basis for requesting the recalculation is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A).

This form must be filed within 180 days of the day the patent was granted, with the following exception:

> Patentees who received a decision from the USPTO under the USPTO's pre-Wyeth interpretation of 35 U.S.C. 154(b)(2)(A) may file a request for reconsideration of that decision if such a request for reconsideration is filed within **two months** of the date of the decision (37 CFR 1.181(f)). If the patentee's sole basis for requesting reconsideration of the decision is the USPTO's pre-Wyeth interpretation of 35 U.S.C. 154(b)(2)(A), the request for reconsideration need only state that reconsideration is being requested in view of Wyeth (this form may be used for this purpose if it is filed within **two months** of the date of the decision from the USPTO).

Do not use this form if the application has been allowed, but not yet issued as a patent.

1. **For patents issued before March 2, 2010:** A request for reconsideration under 37 CFR 1.705(d) and the fee set forth in 37 CFR 1.18(e) are not required, provided that the patentee's sole basis for requesting recalculation of the PTA in the patent is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A) and this form is filed within 180 days of the day the patent was granted.

2. **For patents issued on or after March 2, 2010 (do not use this form):** Patentees seeking a revised PTA in a patent issued on or after March 2, 2010, must file a request for reconsideration under 37 CFR 1.705(d) that complies with the requirements of 37 CFR 1.705(b)(1) and (b)(2) within two months of the day the patent issued.

For more information, see "Notice Concerning Calculation of the Patent Term Adjustment With Respect to the Overlapping Delay Provision of 35 U.S.C. 154(b)(2)(A)" available on the USPTO Web site at http://www.uspto.gov/patents/law/notices/2010.jsp.

**Wyeth v. Kappos*, No. 2009-1120 (Fed. Cir., Jan. 7, 2010).

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	7024046
Application Number:	10914044
International Application Number:	
Confirmation Number:	5848
Title of Invention:	ELECTRO-OPTICAL PANEL,SYSTEM WITH TERMINALS HAVING DIFFERENT CORRESPONDING CHARACTERISTICS
First Named Inventor/Applicant Name:	Shin Fujita
Customer Number:	27572
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Attorney Docket Number:	9319S-000838
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Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Patent Term Adjustment Petition	Request_Recalc_PTA.PDF	150744 cfce6fe6dd320906fb2a4a42334d89819e285347	no	3

Warnings:	
Information:	

Total Files Size (in bytes):	150744

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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Mail Date: 04/21/2010

Applicant	: Shin Fujita	: DECISION ON REQUEST FOR
Patent Number	: 7636146	: RECALCULATION of PATENT
Issue Date	: 12/22/2009	: TERM ADJUSTMENT IN VIEW
Appliction No	: 10/914,044	: OF WYETH AND NOTICE OF INTENT TO
Filed	: 08/06/2004	: ISSUE CERTIFICATE OF CORRECTION
		:

The Request for Recalculation is **GRANTED** to the extent indicated.

The patent term adjustment has been determined to be **963** days. The USPTO will *sua sponte* issue a certificate of correction reflecting the amount of PTA days determined by the recalculation.

Prior to the issuance of the certificate of correction, the USPTO will afford patentee an opportunity to be heard and request reconsideration. Accordingly, patentee has **one month or thirty (30) days**, whichever is longer, to file a request for reconsideration of this patent term adjustment calculation. See 35 U.S.C. 154(b)(3)(B)(ii) and 37 CFR 1.322(a)(4). No extensions of time will be granted under 37 CFR 1.136.

Patentee should use document code PET.OP if electronically filing a request for reconsideration of this patent term adjustment calculation. The patentee must also include the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e). If patentee does not file a timely request for reconsideration of this patent term adjustment calculation including the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e), the USPTO will issue a certificate of correction reflecting the PTA determination noted above.

Patentee should be aware that in order to preserve the right to review in the United States District Court for the District of Columbia of the USPTO patent term adjustment determination, patentee must ensure that he or she also take the steps required under 35 U.S.C. 154(b)(4)(A) in a timely manner. Nothing in the request for recalculation should be construed as providing an alternative time frame for commencing a civil action under 35 U.S.C. 154(b)(4)(A).

Any questions concerning this decision should be directed to the Office of Patent Legal Administration at 571-272-7702.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,636,146 B2
APPLICATION NO. : 10/914044
DATED : December 22, 2009
INVENTOR(S) : Shin Fujita

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page:

The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 963 days.

Signed and Sealed this

Ninth Day of November, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office