UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	NL070-14US03
First Inventor	Hyun Lee
Title	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*
Electronically filed	March 14, 2022

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents.

Address to: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☐ Fee Transmittal Form (with duplicate for fee processing)
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☐ Applicant certifies Micro Entity status, see 37 C.F.R. § 1.29
4. ☒ Specification [Total Pages 36]
5. ☒ Drawing(s) (35 USC § 113) [Total Sheets 8]
6. ☒ Oath and Declaration [Total Pages 1]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR § 1.63(d))
7. ☒ Application Data Sheet, see 37 C.F.R. § 1.76
8. ☐ CD-Rom or CD-R in duplicate, large table or Computer Program (Appendix)
   ☐ Landscape Table on CD
9. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

10. ☐ Assignment Papers (cover sheet & document(s))
    Name of Assignee: Netlist, Inc.
11. ☐ 37 CFR § 3.73(c) Statement
    ☒ Power of Attorney
12. ☐ English Translation Document (if applicable)
13. ☐ Information Disclosure Statement and PTO-1449
    ☐ Copies of citations attached
14. ☐ Preliminary Amendment
15. ☐ Return Receipt Postcard (MPEP 503)
16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
17. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
18. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 MUST be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

Signature	/Jamie J. Zheng/	Date	March 14, 2022
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL070-14US03
	Application Number	
Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Ladera Ranch	CA	US

Mailing Address of Inventor:

Address 1	21 Thalia
Address 2	

City	State/Province	Postal Code	Country
Ladera Ranch	CA	92694	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141	
Email Address		Add Email Remove Email

Application Information:

Title of the Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD		
Attorney Docket Number	NL070-14US03	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	3

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17/157903	2021-01-25

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL070-14US03
	Application Number	
Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17/157903	Continuation of	16/412308	2019-05-14	10902886	2021-01-26

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/412308	Continuation of	15/602099	2017-05-22	10290328	2019-05-14

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/602099	Continuation of	15/095288	2016-04-11	9659601	2017-05-23

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/095288	Continuation of	14/337168	2014-07-21	9318160	2016-04-19

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/337168	Continuation of	13/288850	2011-11-03	8787060	2014-07-22

Prior Application Status: Expired — Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13/288850	Claims benefit of provisional	61/409893	2010-11-03

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. — Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. — Add

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL070-14US03
	Application Number	
Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	111 Academy Way, Suite 100		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92617
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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	Application Number	
Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /			Date (YYYY-MM-DD)	2022-03-14
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL070-14US03
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Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

RELATED APPLICATION

[0001] This application is a continuation application of U.S. Pat. App. No. 17/157,903, filed January 25, 2021, which is a continuation application of U.S. Pat. App. No. 16/412,308, filed May 14, 2019, now U.S. Pat. No. 10,902,886, which is a continuation application of U.S. Pat. App. No. 15/602,099, filed May 22, 2017, now U.S. Pat. No. 10,602,099, which is a continuation application of U.S. Pat. App. No. 15/095,288, filed April 11, 2016, now U.S. Pat. No. 9,659,601 on May 23, 2017, which is a continuation of U.S. Pat. App. No. 14/337,168, filed July 21, 2014, now U.S. Pat. No. 9,318,160, which is a continuation of U.S. Pat. App. No. 13/288,850, filed November 3, 2011, now U.S. Pat. No. 8,787,060, which claims the benefit of priority under 35 U.S.C. § 119(e) of U.S. Provisional Patent Application No. 61/409,893, filed November 03, 2010, and entitled "Architecture For Memory Module With Packages Of Three-Dimensional Stacked (3ds) Memory Chips." The disclosure of each of the above applications is hereby incorporated by reference in its entirety.

BACKGROUND

Technical Field

[0002] The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to a memory package having stacked array dies and methods for reducing driver load in the memory package.

Description of the Related Art

[0003] Memory modules may include a number of memory packages. Each memory package may itself include a number of array dies that are packaged together. Each array die may include an individual semiconductor chip that includes a number of memory cells. The memory cell may serve as the basic building block of computer storage representing a single bit of data.

[0004] FIGS. 1A and 1B schematically illustrate examples of existing memory package

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designs currently used or proposed to be used to provide the dynamic random-access memory of memory modules. FIG. 1A schematically illustrates a memory package 100 with three array dies 110 and a control die 130. The control die 130 is configured to respond to signals received by the memory package 100 by sending appropriate control signals to the array dies 110 and includes a driver 134 for driving data signals to each of the array dies 110 via a corresponding die interconnect 120. Further, the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142. For simplicity, FIG. 1A shows only a single driver 134, die interconnect 120, driver 140, and die interconnect 142. However, additional drivers and die interconnects may be included for each bit the memory package 100 is designed to support. Thus, a 16-bit memory may include 16 pairs of drivers and die interconnects for the data signals and other similar drivers and die interconnects for the command and/or address signals. Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.

[0005] In some cases, the control die 130 may include memory cells and therefore, also serve as an array die. Thus, as can be seen from FIG. 1A, the control die 130 may also include a chip select port 144. Alternatively, the control die 130 and the array dies 110 may be distinct elements and the control die 130 may not include any memory cells.

[0006] FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 and a control die 170 that does not include memory cells. As can be seen in FIG. 1B, each array die 160 includes a chip select port 174. However, because the control die 170 does not also serve as an array die, the control die 170 does not include a chip select port. As with memory package 100, memory package 150 includes a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182. Further, the memory package 150 includes a driver 186 for driving command and/or address signals to each of the array dies 160 via another die interconnect 188.

[0007] Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue

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of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.

SUMMARY

[0008] In certain embodiments, an apparatus is provided that comprises a DRAM package operable to communicate with a system memory controller via a command/address bus and a data bus. The DRAM package comprises stacked array dies including at least a first array die and a second array die stacked over at least the first array die, and terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals. The DRAM package further comprises control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies, first data interconnects between respective ones of the data terminals and the first array die, and second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die. The DRAM package further comprises drivers coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size.

[0010] In certain embodiments, a method is provided for optimizing load in a memory package. The DRAM package comprises stacked array dies including at least a first array die and a second array die stacked over at least the first array die, and terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals. The DRAM package further comprises control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies, first data interconnects between respective ones of the data terminals and the first

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array die, and second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die. The method comprises selecting a first driver size to drive a first signal received at one of the data terminals to the first array die via one of the first data interconnects and selecting a second driver size to drive a second signal received at the one of the data terminals to the second array die via one of the second data interconnects. The second driver size is different from the first driver size.

[0011] In some embodiments, a respective one of the first data interconnects has a first load and a respective one of the second data interconnect has a second load larger than the first load. The second driver size is larger than the first driver size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Throughout the drawings, reference numbers are re-used to indicate correspondence between referenced elements. The drawings are provided to illustrate certain example embodiments of the inventive subject matter described herein and not to limit the scope thereof.

[0013] FIGS. 1A and 1B schematically illustrate examples of existing memory package designs.

[0014] FIG. 2 schematically illustrates an example embodiment of a memory package in accordance with the present disclosure.

[0015] FIG. 3 schematically illustrates another example embodiment of a memory package in accordance with the present disclosure.

[0016] FIG. 4 schematically illustrates an example embodiment of a driver structure of a control die in accordance with the present disclosure.

[0017] FIG. 5 presents a flowchart for an example embodiment of a load optimization process.

[0018] FIGS. 6A and 6B schematically illustrate an example of a Load Reduction Dual In-line Memory Module (LRDIMM) and a HyperCloud™ Dual In-line Memory Module (HCDIMM) architecture respectively.

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[0019] FIG. 7 schematically illustrates an example of a Three-Dimensional Structure Dual In-line Memory Module (3DS-DIMM) architecture.

[0020] FIG. 8 schematically illustrates an example embodiment of a memory module architecture in accordance with the present disclosure.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0021] In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Patent Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. Further, the following U.S. patent applications are incorporated in their entirety by reference herein: U.S. Patent Application Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 12/815,339.

[0022] Certain embodiments of the present disclosure reduce the size of drivers that are configured to drive a signal, such as a data signal, along a die interconnect to one or more array dies. Further, certain embodiments of the present disclosure reduce the power consumption of the drivers.

[0023] In certain embodiments, reducing one or both of driver size and driver power consumption may be accomplished by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect. For example, instead of one die interconnect in electrical communication with four array dies, there may be two die interconnects, each in electrical communication with a different pair of the four array dies.

[0024] In certain embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect is based, at least in part, on a load of each array die and a load of the die interconnect that is in electrical communication with one or more of the array dies.

[0025] In some embodiments, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies. In such embodiments, determining the number of die interconnects and the number of array dies in electrical

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communication with each die interconnect may be based, at least in part, on a load of each array die without considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become physically smaller, it becomes more important to consider the load of the die interconnect in determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect. Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect.

[0026] FIG. 2 schematically illustrates an example embodiment of a memory package 200 in accordance with the present disclosure. One example of a memory package that includes array dies and a control die is the Hybrid Memory Cube (HMC). Examples of an HMC compatible with certain embodiments described herein are described by the IDF2011 Intel Developer Forum website, http://www.intel.com/idf/index.htm, which includes presentations and papers from the IDF2011 Intel Developer Forum including the keynote address given by Justin Rattner on September 15, 2011. Additional examples of an HMC compatible with certain embodiments described herein are described by the Hybrid Memory Cube Consortium website, http://www.hybridmemorycube.org. The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few. A memory module (not shown) may include one or more memory packages in accordance with the memory package 200. Further, the memory package 200 may include input/output terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).

[0027] The memory package 200 may include a plurality of array dies 210 (e.g., array dies 210a-210d). The plurality of array dies 210 may be sealed within the memory package 200. Further, circuitry of the array dies 210 may be in electrical communication

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with the input/output terminals of the memory package 200. Although generally referred to as array dies herein, the array dies 210 may also be called slave dies or slave chips. Each of the array dies 210a-210d may include circuitry (e.g., memory cells) (not shown) for storing data. Examples of array dies compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS). Examples of 3DS compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). However, the structure or layout of the plurality of array dies 210 is not limited as such, and other structures are possible in accordance with the present disclosure. For example, the plurality of array dies 210 may be arranged in a planar structure, or in a structure that combines 3DS with a planar structure. Moreover, while the memory package 200 is illustrated as including four array dies, the memory package 200 is not limited as such and may include any number of array dies. For example, as illustrated in FIG. 3, the memory package 200 may include eight array dies. As further examples, the memory package 200 may include three or sixteen array dies.

[0028] Each of the array dies 210 may include one or more data ports (not shown). The data ports enable electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication pathway (e.g., a die interconnect).

[0029] In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g., U.S. Patent Nos. 7,633,165 and 7,683,459.) Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die

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210, which may be in electrical communication with a different die interconnect 220.

[0030] For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., 00). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, ...) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d.

[0031] However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, ...) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.

[0032] In addition to the plurality of array dies 210, the memory package 200 includes a control die 230, which may also be called a master die. Examples of master dies

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compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). In some embodiments, the control die 230 may be one of the array dies 210. Alternatively, the control die 230 may be a modified version of one of the array dies 210. Thus, in some implementations, memory package 200 may include four dies or chips instead of the five illustrated in FIG. 2. Further, in some embodiments, the control die 230 may comprise a logic layer (e.g., the logic layer of an HMC).

[0033] The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).

[0034] In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2. The drivers 234 may be configured to drive the data signals along the corresponding die interconnects 220. In some embodiments, a single data conduit 232 or driver 234 may be in electrical communication with multiple die interconnects 220, each of which may be in electrical communication with different array dies 210.

[0035] Each of the data conduits 232 may be configured to receive the data signal from a common source. For instance, the data conduit 232a and the data conduit 232b may each receive a substantially similar, if not identical, data signal from the same signal source (e.g. the data signal corresponding to the same data bit). The source of the data signal may include a data path, a driver, a latch, a pin, or any other construct that may provide a data signal to a data conduit.

[0036] The data conduits 232 may each be subject to a load. Although not limited as such, this load may be measured as a capacitive load, such as a parasitic capacitance. The load on each of the data conduits 232 may include at least a load of the die

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interconnect 220 to which the data conduit 232 is coupled or connected as well as a load of each array die 210 with which the die interconnect 220 is in electrical communication via a data port of the die interconnect 220. Thus, for example, the load of the data conduit 232a may include loads of the die interconnect 220a, the array die 210a, and the array die 210b. Similarly, the load of the data conduit 232b may include loads of the die interconnect 220b, the array die 210c, and the array die 210d.

[0037] Generally, a load that would be on a data conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one data port of each of the array dies 210 can be considered the maximum load for a data conduit. This maximum load is the load of a data conduit of a memory package that does not implement the teachings of this disclosure, but is in accordance with conventional configurations.

[0038] In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is less than the maximum load for a data conduit as described above. Thus, in some cases, there may exist a degree of balance or equalization between the loads of the data conduits 232a, 232b. In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is zero or substantially zero. In some embodiments, the length of each die interconnect 220, and the number of array dies 210 in electrical communication with each die interconnect 220 may be selected to maintain the difference between the load of the data conduit 232a and the load of the data conduit 232b to be at or below a threshold load difference. For example, suppose that the load of each array die 210 is 1, the load of each segment of the die interconnects 220 is 0.25, and that the threshold load difference is 0.5. Using the configuration schematically illustrated in FIG. 2, the load on the data conduit 232a in this example is 2.5 and the load on the data conduit 232b in this example is 3. Thus, in this example, the difference between the load of the data conduit 232a and the load of the data conduit 232b is at the threshold load difference value of 0.5. However, an alternative configuration that places the die interconnect 220a in electrical communication with only the array die 210a, and the die interconnect 220b in electrical communication with the array dies 210b-210d would not satisfy the threshold load difference value of 0.5 of the above example. In the alternative configuration, the load on the data conduit 232a would be

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1.25 and the load on the data conduit 232b would be 4. Thus, in the alternative configuration, the difference between the load of the data conduit 232a and the load of the data conduit 232b is 2.75, which is above the threshold load difference value of 0.5.

[0039] For certain embodiments, the load of each data conduit is less than the maximum load as described above. Thus, in some cases, the load of the data conduit 232a is less than the maximum load and the load of the data conduit 232b is less than the maximum load. Further, in many implementations, the combined load of the data conduit 232a and the data conduit 232b is less than the maximum load of a single data conduit. In other words, it is possible to design the data conduit 232a and the data conduit 232b to reduce the overall load compared to a single data conduit that is in electrical communication with a die interconnect that is in electrical communication with at least one data port of each of the array dies 210. By reducing the overall load compared to the single data conduit, it is possible in many cases to reduce power consumption. Further, it is possible in many cases to maintain signal quality (e.g. maintain signal amplitude, maintain low signal distortion, etc.) while reducing power consumption. Advantageously, in a number of embodiments, by using multiple data conduits instead of a single data conduit, the speed of the memory package 200 can be increased. In some cases, this speed increase can include a reduced latency in accessing array dies 210 and/or operating the memory package 200 at a higher clock frequency.

[0040] Each of the die interconnects 220 may include any type of conducting material. For example, the die interconnects 220 may include copper, gold, or a conductive alloy, such as a copper/silver alloy. Further, the die interconnects 220 may include any type of structure for enabling electrical communication between the data conduits 232 and the data ports of the array dies 210. For example, the die interconnects 220 may include a wire, a conducting rod, or a conducting trace, to name a few. Moreover, the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, die interconnect 220a may be connected with data ports of the array dies 210a and 210b using vias (illustrated by the filled or darkened circles). Examples of TSVs which may be used with the present disclosure are described further in U.S. Patent Nos. 7,633,165 and 7,683,459.

[0041] In addition, the die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect.

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For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not enable electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signals being transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.

[0042] Although FIG. 2 illustrates a single pair of data conduits 232 corresponding to a single pair of die interconnects 220, this is only to simplify the drawing figure. The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the memory package 200 is designed or configured to support per memory address. Thus, if, for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32-or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210. However, it is possible that, in some embodiments, the data conduits and die interconnects of different bits may be configured differently.

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[0043] In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bi-directional. In alternative embodiments, separate die interconnects and corresponding data conduits may be used to transfer data to the array dies 210 and data from the array dies 210 to the control die 230. Thus, such embodiments may include double the number of die interconnects and data conduits as embodiments that use the same die interconnect to transfer data to and from an array die.

[0044] In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2 shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.

[0045] In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250a-250d as shown in FIG. 2). Further, the control die 230 may include corresponding die interconnects 252 (e.g., die interconnects 252a-252d) with one die interconnect 252 in electrical communication with one chip select conduit 250 and one array die 210. Each of the die interconnects 252 may be in electrical communication with a different array die 210. For example, the die interconnect 252a may be in electrical communication with the array die 210a and the die interconnect 252b may be in electrical communication with the array die 210b. Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252.

[0046] In some embodiments, the control die 230 may include additional drivers that

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are configured to drive the chip select signals along the die interconnects 252. Alternatively, the chip select signals may be driven by drivers that are external to the control die 230. For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210. As a second example, the chip select signals may be provided by an MCH. In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.

[0047] FIG. 3 schematically illustrates another example embodiment of a memory package 300 in accordance with the present disclosure. In certain embodiments, some or all of the embodiments described above with respect to the memory package 200 may be applicable to the memory package 300. However, for ease of illustration and to simplify discussion, certain elements are omitted in FIG. 3, such as the chip select conduits. Nevertheless, it should be understood that the memory package 300 can include the same or similar elements as described above with respect to the memory package 200, including, for example, the chip select conduits.

[0048] The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG. 3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.

[0049] In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die interconnect 320.

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[0050] Further, implementations of the conduits 332 may include one or more drivers 334 (e.g., drivers 334a-334f). Each of the drivers 334 may be configured to drive a signal along a corresponding die interconnect 320. For instance, the driver 334a of the conduit 332a may be configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b. As a second example, the driver 334b of the conduit 332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b, because the die interconnect 320b, in the example illustrated in FIG. 3, is not configured to be in electrical communication with the array dies 310a and 310b, the driver 334b does not drive the signal to the array dies 310a and 310b.

[0051] In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.

[0052] Generally, the signal that each of the drivers 334 drive to the corresponding die interconnects 320 is from a common source. Thus, each of the drivers 334, in certain embodiments, is driving the same signal to each corresponding die interconnect 320.

[0053] The size of the drivers 334 is generally related to the load on the driver 334. In certain embodiments, the load on each driver 334 corresponds to the load of the respective conduit 332. Although not limited as such, the load may be measured as a capacitive load, such as a parasitic capacitance.

[0054] The load on each of the conduits 332 may include at least the loads of the die interconnect 320 with which the conduit 332 is coupled or connected as well as the loads of each array die 310 with which the die interconnect 320 is in electrical communication via a port of the die interconnect 320. Thus, for example, the loads of the conduit 332a may include the loads of the die interconnect 320a, the array die 310a,

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and the array die 310b. Similarly, the loads of the conduit 332b may include the loads of the die interconnect 320b, the array die 310c, and the array die 310d. The loads of both conduits 332a and 332b include a load of two array dies 310 because the corresponding die interconnects 320 are each configured to be in electrical communication with two array dies 310. On the other hand, the load of the conduit 332c, which may include the loads of the die interconnect 320c and the array die 310e, includes a load of one array die 310e because the corresponding die interconnect 320c is configured to be in electrical communication with only one array die 310.

[0055] As previously described with respect to FIG. 2, a load that would be on a conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one port of each of the array dies 310 can be considered the maximum load for a conduit. This maximum load is the load of a conduit of a memory package that does not implement the teachings of this disclosure, but is used in accordance with conventional configurations.

[0056] In some implementations, the difference between the loads of any pair of the conduits 332 is less than the maximum load for a conduit as described above. For instance, the difference between the load of the conduit 332a and the load of the conduit 332b is less than the maximum load. As a second example, the difference between the load of the conduit 334f and any one of the conduits 334a to 334e is less than the maximum load. Thus, in some cases, the load on each of the conduits 332 may be, at least partially balanced or equalized to reduce or minimize the difference between the load of any pair of the conduits 332. In some implementations, the difference between the load of a pair of the conduits 332 is zero or substantially zero. In some embodiments, the length of each die interconnect 320, and the number of array dies 310 in electrical communication with each die interconnect 320 may be selected to maintain the difference between the load of any pair of the conduits 332 to be at or below a threshold load difference.

[0057] For certain embodiments, the load of each conduit is less than the maximum load as described above. Thus, for example, the load of the conduit 332a, the load of the conduit 332b, and the load of the conduit 332c are each less than the maximum load defined above.

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[0058] In certain embodiments, the load associated with each of the array dies 310 may be substantially equivalent. For example, the load of the array die 310a may be substantially equal to the load of the array die 310h. Thus, the load contribution from the array dies 310 for a specific conduit 332 may be measured as a multiple of the array dies that are in electrical communication with a die interconnect 320 corresponding to a specific conduit 332. For example, assuming that the load of each of the array dies 310 is 'L', then the contribution of the load from the array dies 310 to the conduit 332a would be 2L because the die interconnect 320a corresponding to the conduit 332a is in electrical communication with two array dies 310, array dies 310a and 310b. In alternative embodiments, the load of each of the array dies 310a may differ. For example, the load of array die 310a may be L and the load of the array die 310b may be 1.25L.

[0059] Similar to the array dies 310, in some embodiments, a die interconnect 320 can be considered to comprise a plurality of segments, with each segment of a die interconnect 320 contributing a substantially equivalent load to the load of the die interconnect 320. In this case, the segment of the die interconnect 320 may refer to the portion of the die interconnect between two successive or adjacent dies (array die-to-array die, master die-to-array die, or both) along the die interconnect 320. Further, the segment may be defined as a portion of the die interconnect 320 between the dies exclusive of a portion of the dies. For example, one segment of the die interconnect 320a may extend from the top of the array die 310a to the bottom of the array die 310b. Alternatively, the segment may be defined to include at least a portion of at least one of the array dies 310. For example, one segment of the die interconnect 320a may extend from the center of array die 310a to the center of array die 310b. As a second example, one segment of the die interconnect 320a may extend from the top of the control die 330 to the top of the array die 310a, and therefore may include a portion of the die interconnect 320a extending from the bottom of the array die 310a to the top of the array die 310a. In some implementations, the segments are substantially equal in length to each other. Moreover, the load contribution of each segment may be substantially equal to each other. Alternatively, the segments may be unequal in length and/or may each contribute a different load to the total load of a die interconnect 320. Further, in some cases, the load contribution of a segment of the die interconnect 320 that is in electrical communication with a port of an array die 310 may differ from the

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load contribution of a segment of the die interconnect 320 that is not in electrical communication with a port of an array die 310.

[0060] In some cases, the load contribution of each segment of the die interconnect 320 may be measured as a fraction of the load contribution from an array die 310. For example, the load of one segment of the die interconnect 320a may be equivalent to one quarter of the load of an array die 310. Thus, for example, the load of the conduit 332a may be 2.5L assuming a load contribution of L per array die 310 (two in this case) in electrical communication with the die interconnect 320a and a load contribution of 0.25L per segment (two in this case) of the die interconnect 320a. As a second example, the load of the conduit 332f may be 3L assuming the same load values as the previous example and a load contribution from one array die 310h and eight die interconnect 320f segments. Table 1 specifies the capacitive load values for each conduit 332 assuming, as with the previous two examples, that the load of each of the array dies 310 is L, and that the load of each segment of the die interconnects 320 is 0.25L. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f.

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5L	0.5
332b	2	4	3L	0
332c	1	5	2.25L	0.75
332d	1	6	2.5L	0.5
332e	1	7	2.75L	0.25
332f	1	8	3L	0

[0061] As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is 3L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10L. Thus, certain embodiments of the present disclosure enable a reduction in the load of the conduits 332. Consequently, in some embodiments, the drivers 334 may each be smaller than a single driver that is configured to drive a signal from a conduit along a single die interconnect that is in electrical communication with a port from each of the array dies 310. Moreover, the drivers 334 may include

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smaller transistor sizes than a single driver that is configured to drive a signal to each of the array dies 110.

[0062] As can be seen from Table 1, conduits 332b and 332f have the largest capacitive load of the group of conduits, which is 3L. Conduit 332 has the smallest capacitive load of the group of conduits, which is 2.25L and which is a deviation of only 0.75 from the maximum load. Thus, in some embodiments, each of the drivers 334 may be substantially similar in size. In certain implementations, the drivers 334 may vary in size based on the total capacitive load on each conduit 332. Thus, the driver 334f may be larger than the driver 334e. Alternatively, each driver 334 may be substantially equal and may be configured based on the drivers 334 with the largest load, which are drivers 334b and 334f in the example illustrated in FIG. 3 and Table 1.

[0063] In some embodiments, the capacitive load of each conduit 332 or driver 334 can be calculated using formula (1).

$$CL = AD + {}^{S}/_{M} \qquad (1)$$

[0064] In formula (1), CL represents the capacitive load of a conduit 332 or driver 334, AD represents the number of array dies 310 in electrical communication with a die interconnect 320 that is in electrical communication with the conduit 332 and/or driver 334, S represents the number of die interconnect segments of the die interconnect 320, and M represents the ratio of the load of an array die 310 to the load of a segment of a die interconnect 320. Thus, using formula (1) and the example values described above, the load of the driver 332a, for example, can be calculated with the following values: AD=2, for two array dies 310; S=2, for the two segments of the die interconnect 320a; and M=4, for the ratio of the load of an array die 310, L, to the load of a segment of the die interconnect 320a, 0.25L. Therefore, as can be seen from Table 1, the capacitive load of the driver 332a is 2.5L where L is the load of a single array die.

[0065] In some cases, the load on each conduit 332 and/or driver 334 may be evenly balanced. In other words, the load on each conduit 332 and/or driver 334 may be substantially the same. To achieve a balanced load, each of the conduits 332 may be in electrical communication with a combination of array dies 310 and die interconnect 320 segments that results in a load that is substantially equivalent to the loads of the other

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conduits 332. In certain embodiments, the load of the conduits 332 is balanced despite each conduit 332 being in electrical communication with a different subset of the array dies 310. However, in alternative embodiments, the load of each conduit 332 and/or driver 334 may differ. This difference in the load of the conduits 332 and/or drivers 334 may be a design decision (e.g. to maintain a specific number of drivers). Alternatively, or in addition, the load difference between conduits 332 and/or drivers 334 may occur because the loads of the array dies 310 and the die interconnect segments 320 do not allow for perfect or substantially even load balancing.

[0066] As previously stated, in some embodiments the loads of the conduits 332 and/or drivers 334 may be balanced to minimize the difference between any pair of conduits 332 and/or drivers 334. For example, as illustrated in FIG. 3, a driver in electrical communication with a longer die interconnect, which may consequently include more die interconnect segments, is likely to obtain a larger load contribution from the die interconnect than a driver in electrical communication with a shorter die interconnect (e.g., compare driver 334f to 334a). Thus, the driver in electrical communication with the longer die interconnect may be in electrical communication with fewer array dies than the driver in electrical communication with the shorter die interconnect (e.g. compare driver 334f to 334a). The selection of die interconnect length and the selection of array dies to place in electrical communication with the die interconnects may therefore be dependent on the load of each segment of the die interconnects 320 and the loads of the array dies 310.

[0067] Alternatively, or in addition, the loads of the conduits 332 and/or drivers 334 may be balanced to reduce the maximum load of each conduit 332 and/or driver 334. Further, in some embodiments, the maximum load of each conduit 332 and/or driver 334 may be reduced to maintain the load of each conduit 332 and/or driver 334 to be at or below a threshold load difference.

[0068] Although not illustrated in FIG. 3, each of the conduits 332 may include one or more additional drivers configured to drive a signal received from an array die via a corresponding die interconnect 320. The additional drivers may drive the signal to a processor, a register, a latch, or any other component or device that may or may not be part of a memory module that includes the memory package 300. In some implementations, one or more of the die interconnects 320 are configured to be bi-

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directional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330. Alternatively, the memory package 300 comprises one or more die interconnects 320 that are configured to enable a signal to be driven to the array dies 310 without enabling a signal to be received from the array dies 310 (e.g., the die interconnects 320 may not be bi-directional). In certain embodiments where one or more of the die interconnects 320 are not bi-directional, the memory package 300 may include additional die interconnects (not shown) that are in electrical communication with the one or more additional conduits or drivers and that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.

[0069] In addition to the drivers 334 of the control die 330, the memory package 300 may include one or more pre-drivers 340. A pre-driver 340, shown schematically in FIG. 3, may be large enough to drive a signal (e.g., a data signal) to any of the drivers 332 and subsequently, to any of the array dies 310. Thus, using the same example values as described above in relation to Table 1, a load of the pre-driver 340 may be at least 10L, which is the load of a conduit in electrical communication with a die interconnect that is in electrical communication with a port from each of the array dies 310. In some embodiments, the memory package 300 may include any number of additional drivers and/or latches for buffering and/or driving the signal to any of the array dies 310.

[0070] Just as the memory package 300 may include a pre-driver 340 for providing a signal to the conduits 332, the memory package 300 may include a post-driver (not shown) for driving an output signal from the control die 330. This post-driver may drive the output signal to additional latches and/or drivers. In some embodiments, the post-driver may drive the signal from the memory package 300 to a bus or other electrical path that is in electrical communication with the memory package 300.

[0071] FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. The driver structure 400 is configured for a single data bit. Thus, a control die for a 32-bit memory package will generally include at least 32 instances of the driver structure 400, one per bit. In some embodiments, the control die 230 may include the driver structure 400 in place

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of the combination of drivers 232a and 232b. Similarly, in certain embodiments, the control die 330 may include a structure similar to the driver structure 400 in place of the drivers 334. In such embodiments, the driver structure 400 would be modified to enable a signal (e.g., data signal) to be driven to the six conduits 332.

[0072] The driver structure 400 can include an input/output port 402 configured to receive or send a signal, such as a data signal. Signals received at the input/output port 402 can be provided to the drivers 404a and 404b. In turn, these drivers 404a and 404b can drive the signal to conduits 406a and 406b respectively, which are in electrical communication with corresponding die interconnects. Each of the die interconnects may be in electrical communication with different array dies in accordance with certain embodiments described herein.

[0073] In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal. In some implementations, the drivers 404a and 404b may drive a signal to the array die corresponding to the chip select signal, and not to array dies that do not correspond to a chip select signal. For example, suppose the conduit 406a is in electrical communication with array dies one and two (not shown), and that the conduit 406b is in electrical communication with array dies three and four (not shown). If a chip select signal is received corresponding to array die two, then in some implementations, driver 404a may be configured to drive a signal along a die interconnect in electrical communication with the conduit 406a to array die one and two. In this example, the driver 404b would not drive the signal because the chip select signal does not correspond to either array die three or array die four.

[0074] In some embodiments, the drivers 404a and 404b may drive a signal to all of the array dies. For example, assume the memory package that includes the driver structure 400 also includes four array dies. If the die interconnect in electrical communication with the conduit 406a is in electrical communication with two of the array dies, and if the die interconnect in electrical communication with the conduit 406b is in electrical communication with the other two array dies, then the drivers 404a and 404b may drive a signal to all four of the array dies of this example.

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[0075] Similar to the input/output port 402, the conduits 406a and 406b can be configured to receive a signal from the die interconnects that are in electrical communication with the conduits 406a and 406b. In turn, the signal received at one of the conduits 406a and 406b can be provided to drivers 408a and 408b respectively. The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.

[0076] In some embodiments, one or more chip selects, as illustrated in FIG. 2, may be used to select, determine, or enable the array die that communicates the signal to or from one or more of the conduits 406a and 406b and the drivers 408a and 408b. Similarly, in some embodiments, the chip select may select, determine, or enable the array die to receive and/or respond to the signal driven by the drivers 404a and 404b to the array dies.

[0077] It should be noted that the driver structure 400 is a non-limiting example for arranging drivers in a control die. Other driver structures are possible. For example, instead of the drivers 404a and 408a being in electrical communication with the same conduit 406a, each of the drivers 404a and 408a can be in electrical communication with a separate conduit and consequently a separate die interconnect. In such an example, the drivers 404a and 408a may still be in electrical communication with the same input/output port 402, or each driver may be in electrical communication with a separate port, the driver 404a in electrical communication with an input port, and the driver 408a in communication with an output port.

[0078] FIG. 5 presents a flowchart for an example embodiment of a load optimization process 500. In certain embodiments, the load optimization process 500 may be performed, at least in part, by one or more computing systems. Further, the process 500, in some embodiments, may be used to optimize one or more loads in a memory package (e.g. memory package 200 or memory package 300). Optimizing the loads in the memory package can include optimizing the load on one or more conduits and/or drivers. As previously described with respect to FIGS. 2 and 3, the memory package can include a plurality of array dies, a plurality of die interconnects, and a control die. Furthermore, the control die can include a plurality of drivers, each of which may be

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configured to drive a signal along a die interconnect.

[0079] In some implementations, the process 500 can comprise selecting a first subset of array dies and a second subset of array dies from a plurality of array dies (e.g., array dies 310), as shown in operational block 502. Generally, the first subset of array dies and the second subset of array dies may be exclusive of one another. Thus, the first subset of array dies does not include any array dies from the second subset of array dies and vice versa. However, in some cases there may be some overlap between the first subset of array dies and the second subset of array dies. Further, in some cases, at least one of the subsets of array dies includes more than one array die. For instance, the first subset of array dies may include two array dies, and the second subset of array dies may include one array die, which, depending on the embodiment, may or may not be included in the first subset of array dies.

[0080] Further, the first subset of array dies and the second subset of array dies may be selected to balance a load on a first driver and a load on a second driver based, at least in part, on the loads of the array dies 310 and on the loads of the die interconnect segments from a first and a second die interconnect. The first die interconnect may be in electrical communication with the first driver and the second die interconnect may be in electrical communication with the second driver. In some embodiments, the first subset of array dies and the second subset of array dies are selected to balance a load on a first conduit and a load on a second conduit. The load on each driver and/or conduit may be calculated using formula (1) as previously described above. In some embodiments, the first subset of array dies and the second subset of array dies may be selected to balance a load on a first driver and a load on a second driver based, at least in part, on the loads of the array dies 310 without considering the loads of the die interconnect segments from the first die interconnect and the second die interconnect.

[0081] The process 500 further comprises forming electrical connections between the first die interconnect and the first subset of array dies in an operational block 504. The process 500 further comprises forming electrical connections between the second die interconnect and the second subset of array dies in an operational block 506. Forming the electrical connections places the die interconnects in electrical communication with the respective subsets of array dies. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects

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and at least one port from each array die of the respective subsets of array dies.

[0082] The process 500 further comprises selecting a driver size for a first driver at block 508 and selecting a driver size for a second driver at block 510. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package.

[0083] In some embodiments, the size of the first driver and the size of the second driver are both less than the size sufficient for a driver to drive a signal along a die interconnect to each of the array dies 310 (e.g., with less than a predetermined or threshold signal degradation). The threshold signal degradation can be based on any one or more characteristics of a signal. For example, the threshold signal degradation can be based on the amplitude of the signal, the frequency of the signal, the noise distortion included in or introduced into the signal, or the shape of the signal, to name a few.

[0084] The process 500 further comprises forming electrical connections between the first die interconnect and the first driver in an operational block 512. Similarly, the process 500 further comprises forming electrical connections between the second die interconnect and the second driver in an operational block 514. Forming the electrical connections places the die interconnects in electrical communication with the respective drivers. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and a data conduit that includes the respective driver.

[0085] Advantageously, certain embodiments of the present disclosure reduce the load on each conduit and on each corresponding driver. In certain embodiments, reducing the load on a driver may increase the speed of data transfer between the array dies and other components in a computer system (e.g. a MCH or a processor). Further, reducing the load on a driver may result in reduced power consumption by the driver and consequently, by the memory package. In addition, certain embodiments of the present

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disclosure may minimize current switching noise.

Operational Modes

[0086] A proposed three-dimensional stacking (3DS) standard for dual in-line memory modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC) addresses three major shortcomings in the current JEDEC registered DIMM (RDIMM) and JEDEC load reduced DIMM (LRDIMM) standards (an example LRDIMM structure 600 is schematically illustrated in FIG. 6A). These shortcomings include: a) The DIMM density limitation due to the fixed number of chip-select signals received by the DIMM from the system memory controller; b) The performance loss due to the increased load on the data bus as the DIMM density (e.g., the number of DRAM devices and number of ranks) increases; and c) The upper bound of the DIMM density due to the physical DIMM form factor.

[0087] Further, the LRDIMM structure 600 may have timing issues due to signals passing through a single memory buffer 601. In addition, the increased size of the data path of the LRDIMM architecture 600, compared to the HCDIMM architecture 602, an example of which is schematically illustrated in FIG. 6B, may result in more latency and signal integrity issues.

[0088] FIG. 7 schematically illustrates an example memory module 700 that has previously been proposed for the 3DS-DIMM standard. The proposed 3DS Dual In-line Memory Module (3DS-DIMM) schematically illustrated in FIG. 7 attempts to address the above shortcomings using two components, a 3DS register 712 and a controller die 722. In some implementations, the 3DS-DIMM 700 includes the 3DS register 712 (also known as an enhanced DDR3 register). The 3DS register 712 may include a DDR3 JEDEC standard register with a "rank multiplication" circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller. The 3DS Register 712 can also include a command/address buffer, a register operational code buffer (RC word buffer), and rank multiplication logic (e.g., supporting rank multiplication of 1-to-2, 1-to-4, and/or 1-to-8). The 3DS register addresses shortcoming (a) of the JEDEC RDIMM and LRDIMM listed above.

[0089] Another component of the proposed 3DS-DIMM is a 3DS dynamic random-

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access memory (DRAM) package 720. The 3DS DRAM package 720 includes a plurality of stacked DDR DRAM chips 724 or array dies. The 3DS DRAM package 720 has a data I/O load that is equivalent to the data I/O load of a single-die DRAM package, regardless of the actual number of DRAM dies in the 3DS DRAM package 720. The 3DS DRAM package 720 may comprise a plurality of array dies (e.g., 2, 4 or 8 DDR DRAM dies) and a controller die 722. The controller die 722 may include data buffers, a data path timing controller, a secondary command/address buffer, a programmable secondary 1-to-2 rank decoder, and a data path signal (e.g., ODT, ODT, RTT) controller. Examples of such memory packages include HMC. The 3DS DRAM package 720 addresses the shortcomings (b) and (c) of the JEDEC RDIMM and LRDIMM listed above. However, there are deficiencies in the proposed 3DS-DIMM standard as described below.

[0090] The JEDEC DDR3 RDIMM standard contains two major components: a DDR3 register and a plurality of DRAM packages each comprising one or more DRAM chips or dies. The DDR3 register serves as a command/address signal buffer and as a command/control decoder. This DDR3 register holds a set of register control (RC) words, which a computer system configures to ensure the proper operation of the RDIMM. The DDR3 register contains a phase-lock-loop (PLL), which functions as a clock synchronizer for each RDIMM. The DDR3 register outputs a set of buffered command/address signals to all the DRAM packages on the RDIMM, but the data signals are directly fed to the DRAM packages from the system memory controller.

[0091] In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations. This arrangement of the DRAM package reduces the load on the data bus, however, it presents three significant shortcomings: 1) The command/address buffer in the 3DS DRAM package introduces clock cycle latency since it needs to provide clock synchronous operation to the DRAM dies in the package; 2) The data path control circuit (e.g., ODT, read/write data direction) in the control die becomes very complicated to support semi-synchronous (fly-by) data path control among all 3DS DRAM packages that are on a DIMM; and 3) The variations in the DRAM die timing characteristics within each 3DS DRAM package would be likely to require resynchronization of the data signals during the read/write operations, which

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increases the read/write latency and the read-to-write and write-to-read turn around time.

[0092] The 3DS-DIMM proposal can also be compared to the HyperCloud™ (HC) DIMM architecture of Netlist, Inc. An example of the HCDIMM architecture 602 is illustrated in FIG. 68. Further details and embodiments of the HCDIMM architecture is disclosed in U.S. Pat. Nos. 7,289,386, 7,532,537, 7,619,912, and 7,636,274, each of which is incorporated in its entirety by reference herein. One of the main topological differences between the 3DS-DIMM and HCDIMM architectures is that while the 3DS-DIMM architecture uses a control die 722 to buffer the data signals and to decode command/address signals from the 3DS register, certain configurations of the HCDIMM architecture include a plurality of isolation devices (ID), each of which includes data buffers, but no decoding capability. Unlike the HCDIMM architecture, since the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720, the 3DS-DIMM proposal presents the same shortcoming (b) of the controller die described above. The data path control signals are generated by the register device (RD) 612 in the HCDIMM architecture 602, while the data path control signals are generated by the control die 722 in the 3DS DRAM. This aspect of the 3DS-DIMM architecture creates timing critical control paths in 3DS-DIMM architecture.

[0093] In certain embodiments described herein, a memory module architecture is proposed that includes a set of device components that support JEDEC 3DS operation with the benefit of RDIMM and HCDIMM architectures (see, e.g., FIG. 8). This set of device components may comprise two components: a register device 812 (RD), which in some embodiments may be the same or similar RD component as used in HCDIMM architectures, and a plurality of array dies 824, such as a DDR DRAM Stack Package (DDSP). The DDSP may comprise a DRAM control die that can include command/address buffers and a data path control circuit. Certain embodiments of the architecture described herein differs from the 3DS-DIMM architecture in that instead of the controller die of the 3DS-DIMM (which provides a secondary address buffer, and a second rank multiplication decoder), certain embodiments described herein use an "ID+" die as a control die 822, which can provide both selective isolation and address pass-through. Selective isolation refers generally to a driver corresponding to an array die driving a signal to the array die in response to a corresponding chip select signal while additional drivers corresponding to additional array dies maintain a previous state

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(e.g. do not drive the signal). For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect 320a to the array die 310b, and the remaining drivers (e.g., drivers 334b-334f) will maintain their state (e.g., not drive the signal). Address pass-through is described in further detail below.

[0094] The data path control circuit of certain embodiments may have at least two operational modes: mode-C (HCDIMM/RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the array dies 824 (e.g. a DDSP) receive the data path control signals from the register device 812, which can be configured to control a command/address time slot and a data bus time slot. In mode-3DS, the control die 822 internally generates the data path control signals to ensure the proper operation of the data path.

[0095] The control die 822 of certain embodiments enables the memory module 800 to work as either a 3DS-DIMM, a RDIMM, or a HCDIMM. However, the memory module 800 may comprise a set of optional control input pins (in addition to the package pins that are included in 3DS-DRAM packages) which in mode-C receive the data path control signals from the register device 812.

[0096] As previously mentioned, FIG. 8 schematically illustrates an example embodiment of a memory module architecture 800 in accordance with the present disclosure. Advantageously, certain embodiments of the memory module architecture 800 address the shortcomings described above without adding complexity or latency, and without causing performance loss. The memory module architecture 800 includes a memory control hub 802 (also known as a memory controller hub, a memory control handler, or a northbridge) and a memory module 810. As schematically illustrated in FIG. 8, the memory control hub 802 may communicate directly with one or more components of the memory module 810. Alternatively, the memory control hub 802 may communicate with one or more intermediary system components (not shown), which in turn communicate with one or more components of the memory module 810. In some embodiments, the memory control hub 802 may be integrated with another component of the computer system, such as a Central Processing Unit (CPU).

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[0097] Further, in some embodiments, the memory control hub 802 may communicate with one or more memory modules. Each of the memory modules may be similar or substantially similar to the memory module 810. Alternatively, some of the memory modules may differ from memory module 810 in configuration, type, or both. For example, some of the memory modules may be capable of operating at different frequencies, may include a different amount of storage capability, or may be configured for different purposes (e.g. graphics versus non-graphics memory). Although in some cases a system may include memory modules capable of operating at different frequencies, each memory module may be configured to operate at the same frequency when used in a specific device. In certain implementations, the memory control hub 802 may set the operating frequency for the one or more memory modules.

[0098] The memory module 810 may include a register device 812, which is configured to receive command, address, or command and address signals from the memory control hub 802. For the purpose of simplifying discussion, and not to limit these signals, the signals will be referred to herein as command/address signals.

[0099] In some embodiments, the register device 812 receives the command/address signals via a command/address bus 814. The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.

[0100] Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.

[0101] In certain embodiments, each control die 822, or isolation device, may be capable of address pass-through. Address pass-through, in some cases, enables the control die 822 to provide an address signal to one or more array dies 824 without decoding the address signal. This is possible, in some implementations, because the

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address signal received by the control die 822 is not encoded.

[0102] Some implementations of the control dies 822 include a plurality of command/address buffers (not shown). These buffers may comprise latches. In certain embodiments, the buffers are configured to hold command/address signals to control the timing of command/address signals. In some cases, controlling the timing of the command/address signals may reduce or slow signal degradation. In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to control command/address time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818. In some implementations, the data path control circuit may be separate from the control die 822.

[0103] Each of the control dies 822 may be configured to receive data signals from the memory control hub 802 via the data bus 818. Further, the control dies 822 may provide data signals to the memory control hub 802 via the data bus 818. The control dies 822 may also receive data path control signals and/or command/address signals from the register device 812 via the data path control lines 816.

[0104] As illustrated in FIG. 8, each memory package 820 may include one or more array dies 824 operatively coupled to the control die 822. The array dies 824 may be configured to receive data signals from the control die 822. As with the array dies 210 and 310, the array dies 824 may include any type of Random Access Memory (RAM) die. For example, the array dies 824 may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory module 810 is utilized for graphics, the array dies 824 may include GDDR SDRAM or any other type of graphics memory. In addition, the array dies 824 may be configured in a stack arrangement as illustrated in FIG. 8. Alternatively, the array dies 824 may be arranged in a planar configuration or a hybrid configuration utilizing both a planar and a stack arrangement.

[0105] In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates

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data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.

[0106] In the second operational mode, the control dies 822 may operate the data path control circuits to provide command/address signals to the array dies 824 without decoding the command/address signals. In this mode, the control dies 822 may use address pass-through to provide received address signals to the array dies 824.

[0107] Other operational modes may also be possible. In some embodiments, the data path control signals generated by the register device 812 may include decoded command/address signals that are decoded from command/address signals received from the memory control hub 802 via the command/address bus 814.

[0108] In some embodiments, the register device 812 may be configured to perform rank multiplication. In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication. Embodiments of rank multiplication are described in greater detail in U.S. Patent Nos. 7,289,386 and 7,532,537, each of which are incorporated in their entirety by reference herein. In such embodiments, the register device 812 can generate additional chip select signals that are provided to the array dies 824. For instance, if the memory control hub 802 is configured to recognize a single array die 824 per memory package 820, but there exists four array dies 824 per memory package 820, the memory control hub 802 may not provide the correct number of chip select signals to access a specific memory location of the plurality of array dies 824 is memory package 820. Thus, to access the specific memory location, the register device 812 can determine the array die that includes the specific memory location to be accessed based on the command/address signals received from the memory control hub 802 and can generate the correct chip select signal to access the array die that includes the specific memory location. In certain embodiments, when the memory module 810 is operating in the second operation module as described above, the memory module 810 does not perform rank multiplication.

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Terminology

[0109] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The term "coupled" is used to refer to the connection between two elements, the term refers to two or more elements that may be either directly connected or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0110] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0111] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0112] Conditional language used herein, such as, among others, "can," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood

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within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0113] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

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WHAT IS CLAIMED IS:

1. A DRAM package, comprising:

stacked array dies including at least a first array die and a second array die, the second array die being stacked over at least the first array die;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies;

first data interconnects between respective ones of the data terminals and the first array die;

second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size.

2. A method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

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MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

ABSTRACT OF THE DISCLOSURE

A DRAM packages comprises stacked array dies including at least a first array die and a stacked over at least the first array die, data terminals, via which the DRAM package receives or outputs data signals, first data interconnects between respective ones of the data terminals and the first array die, and second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die. The DRAM package further comprises drivers configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects. A first data signal is driven by one or more drivers having a first driver size, and a second data signal is driven by one or more drivers having a second driver size different from the first driver size.

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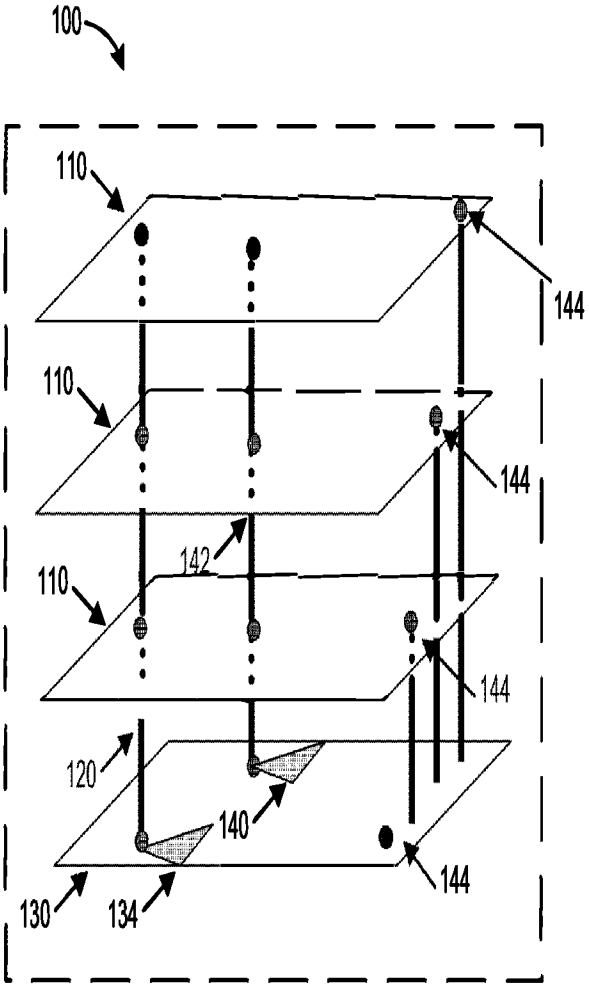

100
110
110
110
144
144
142
144
120
140
144
130
134

FIG. 1A

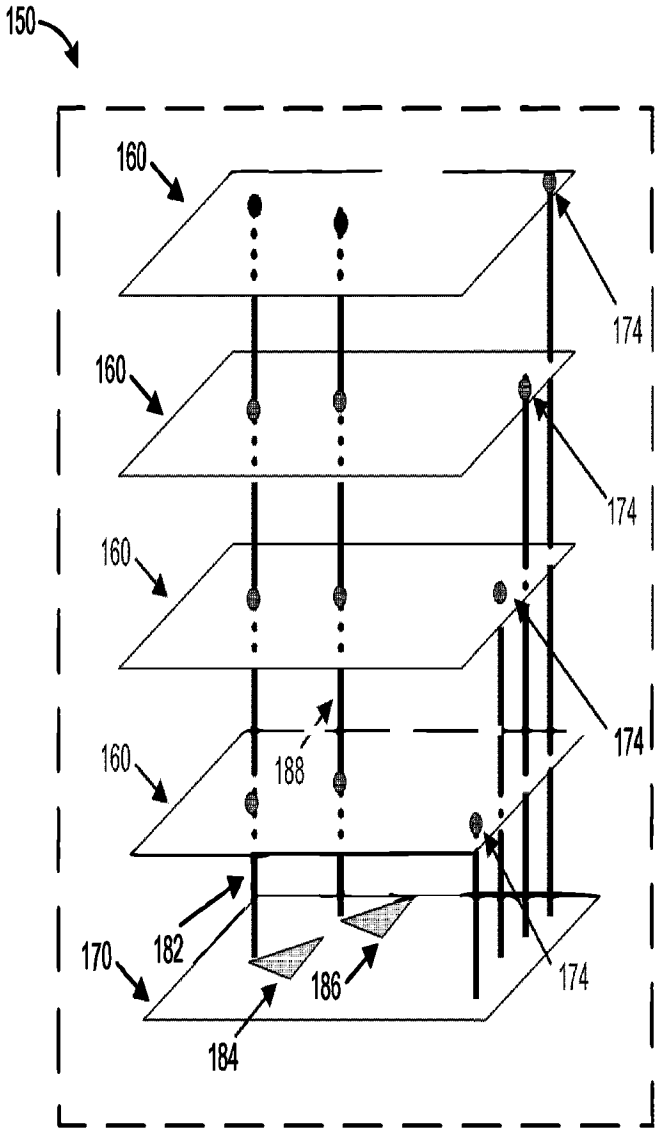

150
160
160
160
160
174
174
174
188
182
170
186
184
174

FIG. 1B

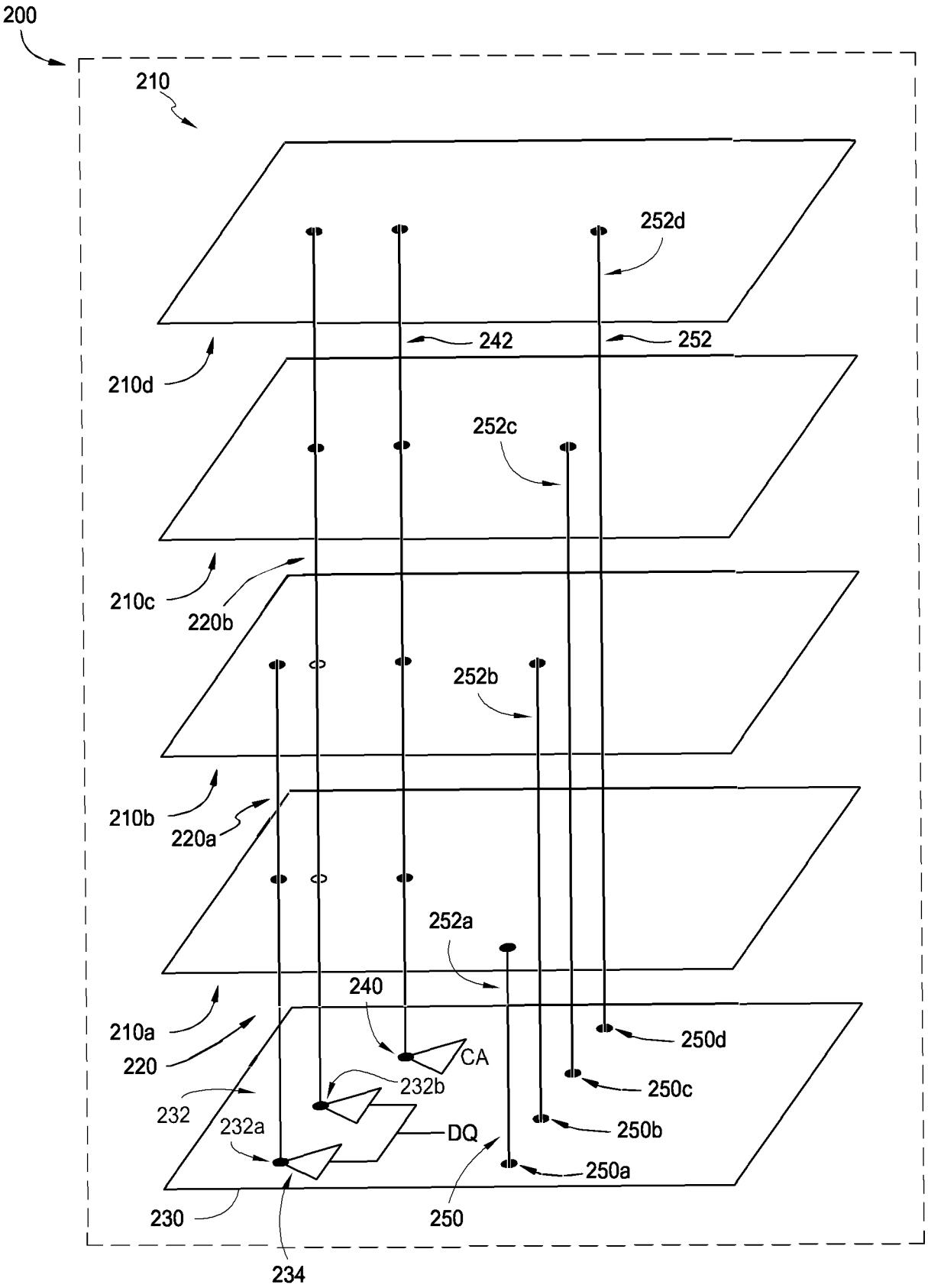

200
210
252d
242
252
210d
252c
210c
220b
252b
210b
220a
252a
240
210a
220
CA
250d
232b
250c
232
232a
DQ
250b
250a
230
250
234

FIG. 2

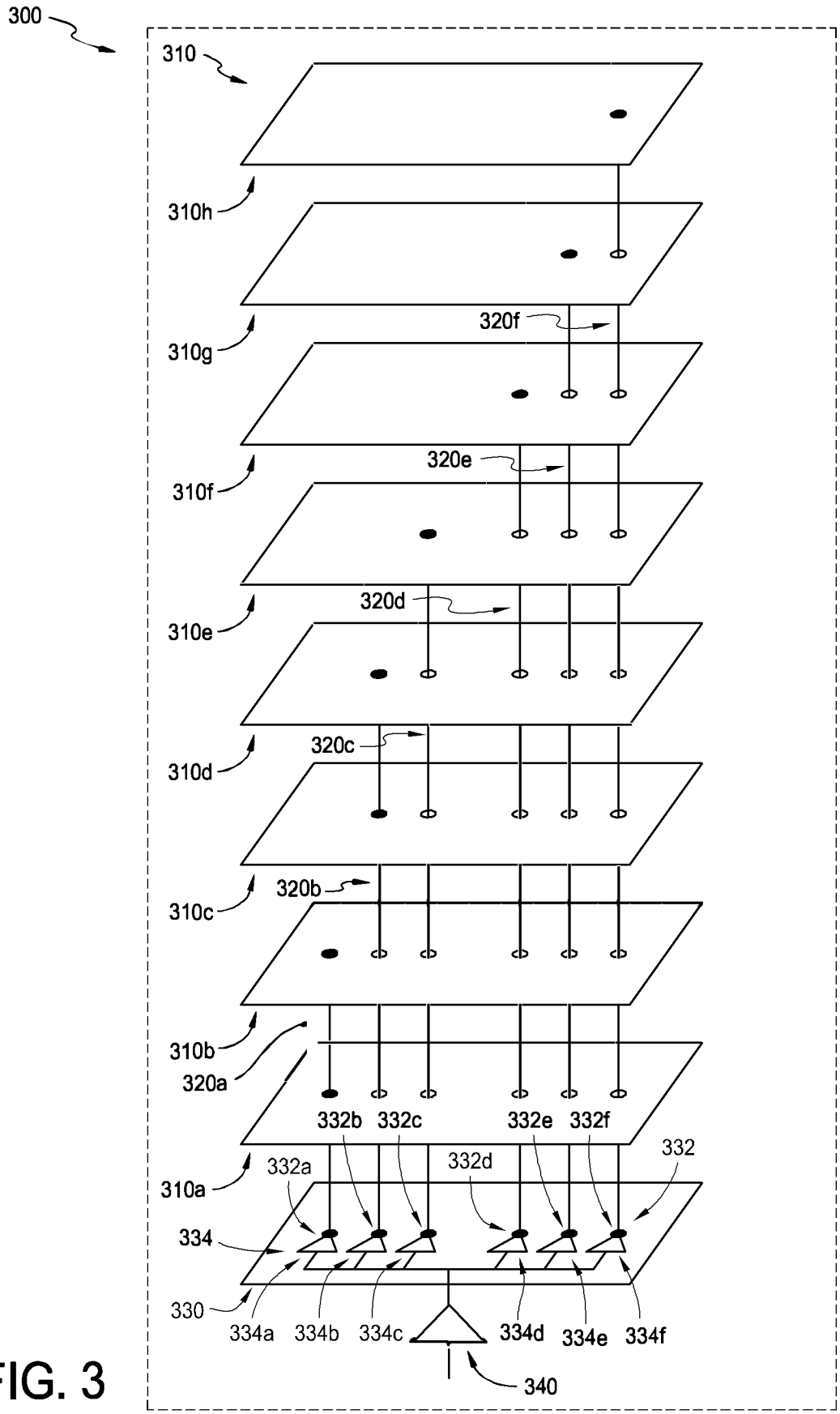

300
310
310h
320f
310g
320e
310f
320d
310e
320c
310d
320b
310c
310b
320a
332b
332c
332e
332f
332
332a
332d
310a
334
330
334a
334b
334c
334d
334e
334f
340

FIG. 3

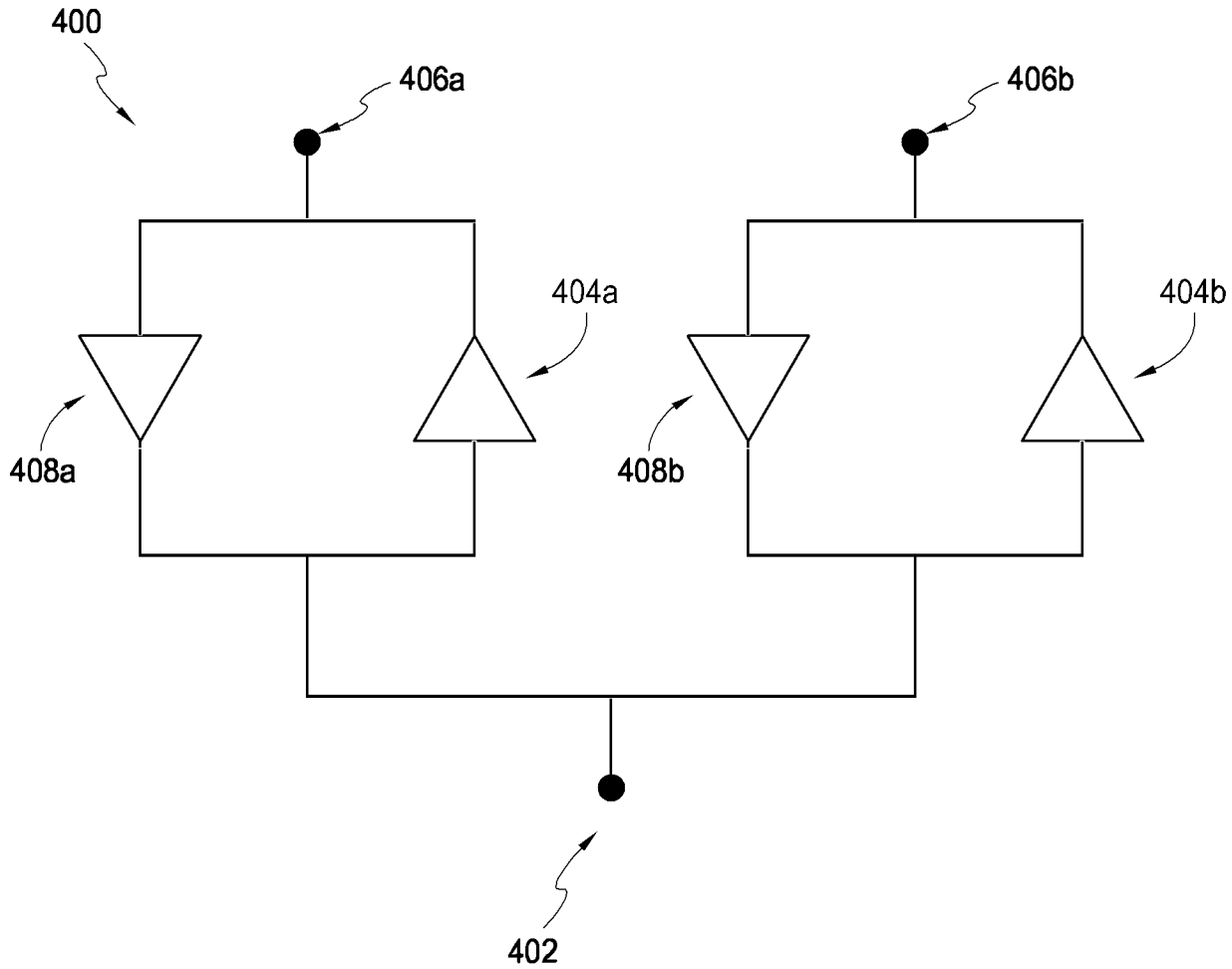


FIG. 4

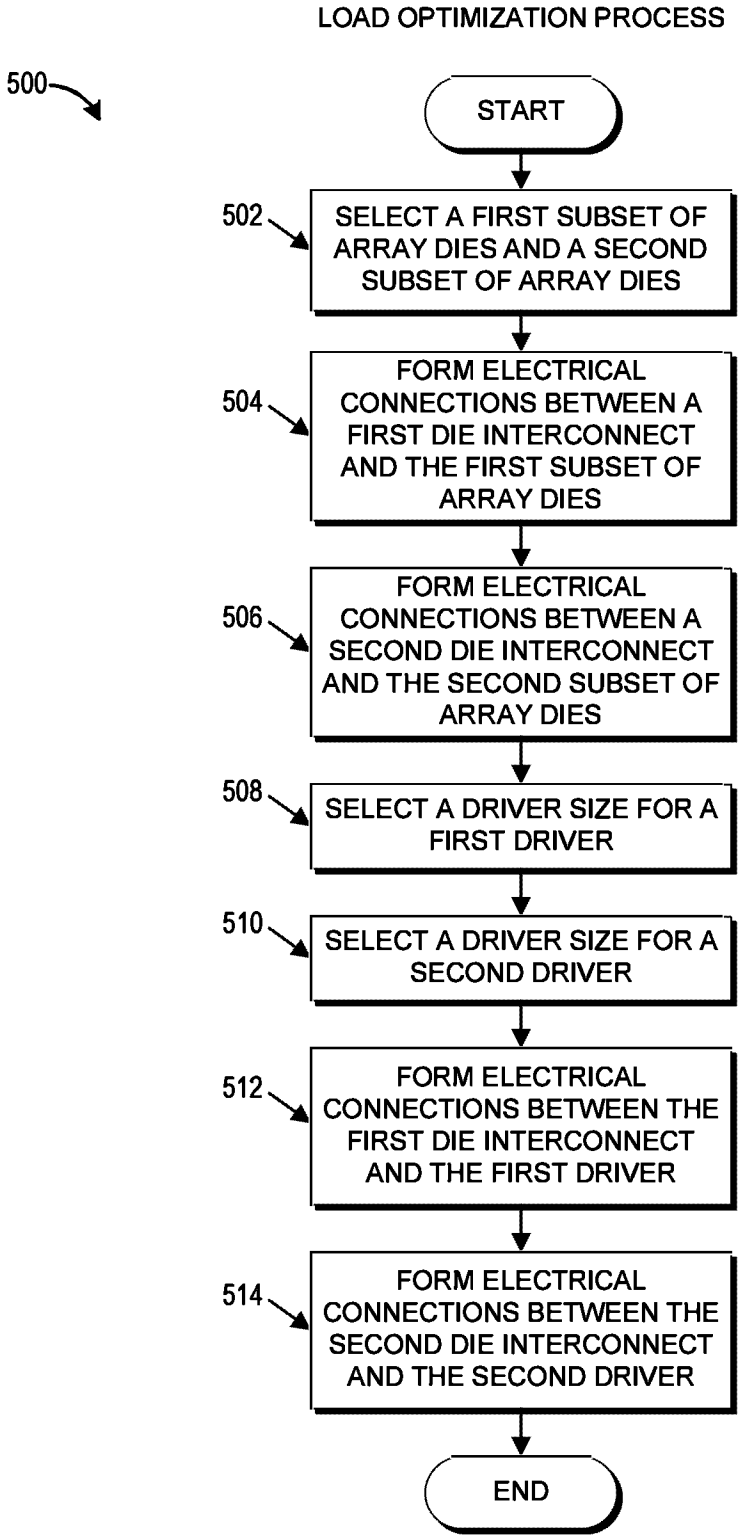

LOAD OPTIMIZATION PROCESS
500
START
502
SELECT A FIRST SUBSET OF ARRAY DIES AND A SECOND SUBSET OF ARRAY DIES
504
FORM ELECTRICAL CONNECTIONS BETWEEN A FIRST DIE INTERCONNECT AND THE FIRST SUBSET OF ARRAY DIES
506
FORM ELECTRICAL CONNECTIONS BETWEEN A SECOND DIE INTERCONNECT AND THE SECOND SUBSET OF ARRAY DIES
508
SELECT A DRIVER SIZE FOR A FIRST DRIVER
510
SELECT A DRIVER SIZE FOR A SECOND DRIVER
512
FORM ELECTRICAL CONNECTIONS BETWEEN THE FIRST DIE INTERCONNECT AND THE FIRST DRIVER
514
FORM ELECTRICAL CONNECTIONS BETWEEN THE SECOND DIE INTERCONNECT AND THE SECOND DRIVER
END

FIG. 5

FIG. 6B

FIG. 6A

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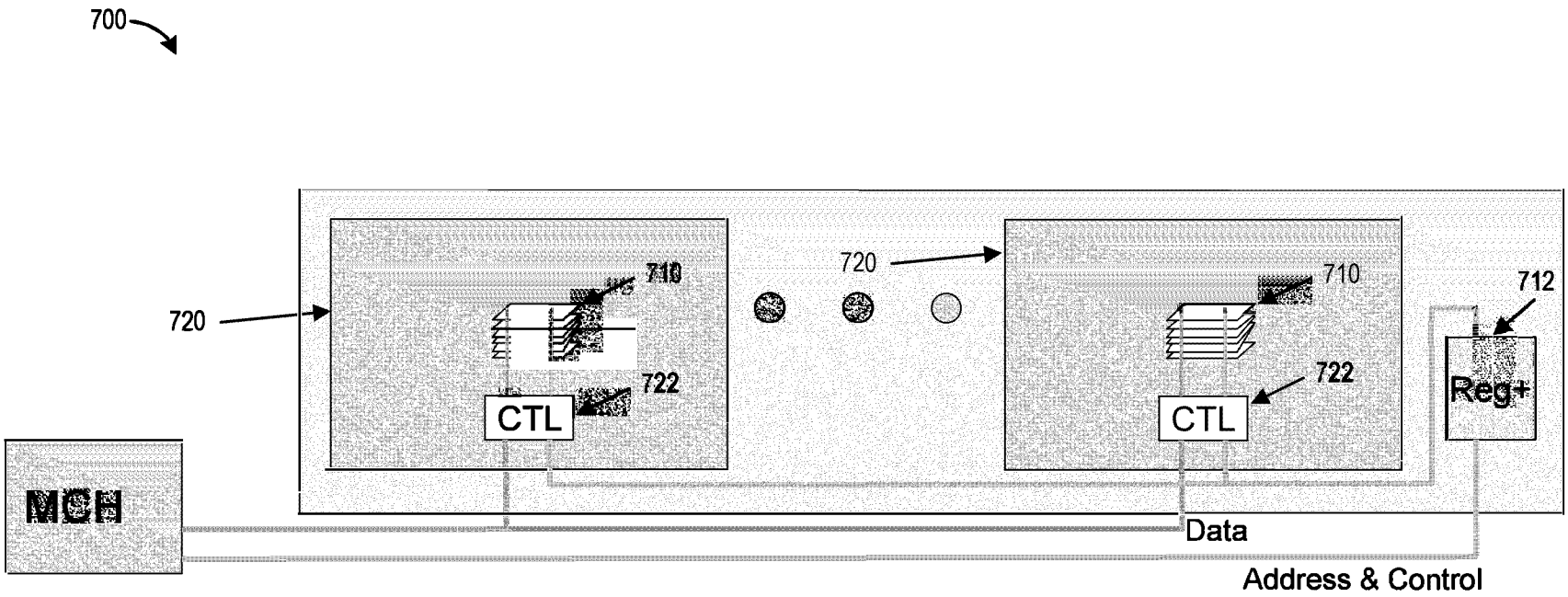


FIG. 7

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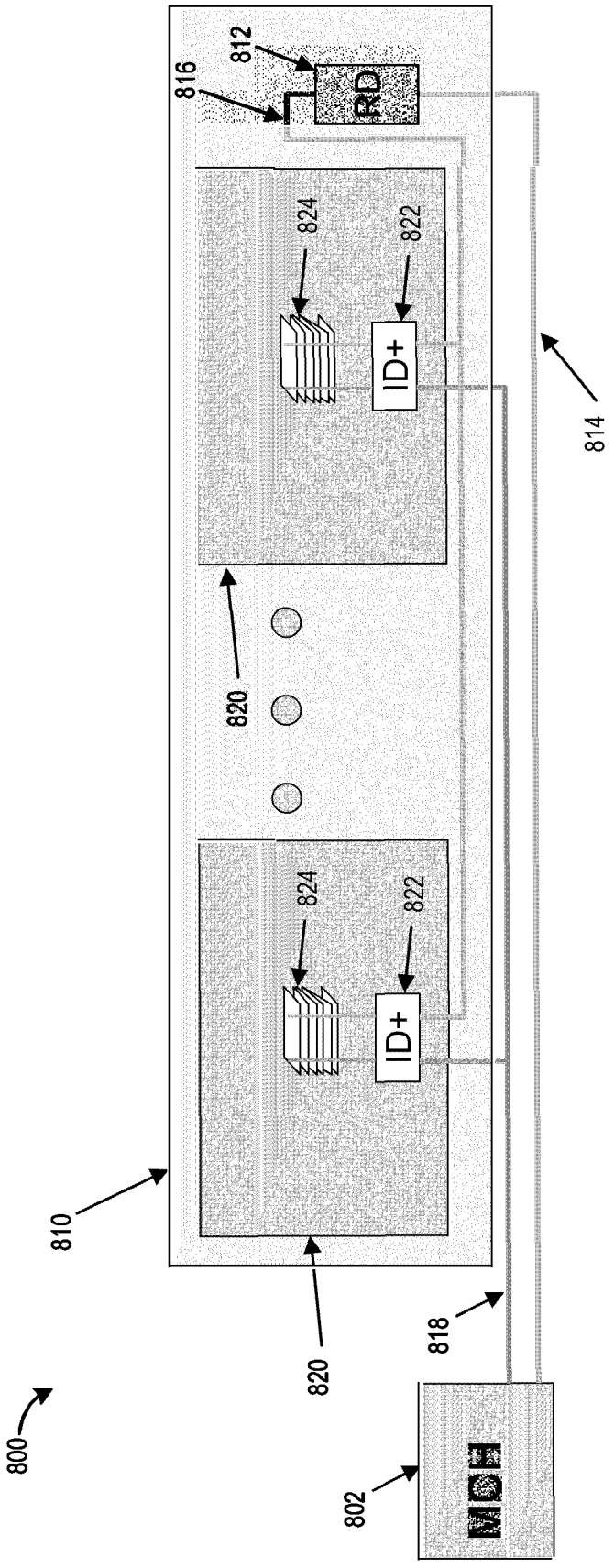


FIG. 8

Customer No. 79141
Attorney Docket No.: NETL.071C1

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	MEMORY PACKAGE WITH OPTIMIZED DRIVER LOAD AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 14/337,168 filed on July 21, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 3/2/2016

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL070-14US03

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1820**

Electronic Acknowledgement Receipt

EFS ID:	45225725
Application Number:	17694649
International Application Number:	
Confirmation Number:	3889
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL070-14US03
Receipt Date:	14-MAR-2022
Filing Date:	
Time Stamp:	23:37:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1820
RAM confirmation Number	E20223DN37563947
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_Netlist_General.pdf	151681 b397f182d5ebb2bff6bfab96b1036487015b2d89	no	1
Warnings:					
Information:					
2	Power of Attorney	NL070-14US03_POATrans.pdf	60313 3a3b17d4e3448a287f6c5c6abafd91cc377bc792	no	1
Warnings:					
Information:					
3	Transmittal of New Application	NL070-14US03_AppTrans.pdf	101261 5384be0af73114c72445c77331ebc9478222b806	no	1
Warnings:					
Information:					
4	Application Data Sheet	NL070-14US03_ADS.pdf	1256603 6b5ab57af4e43cd82f065471e5afcd1b05555824	no	9
Warnings:					
Information:					
5		NL070-14US03_Specification.pdf	310530 920700ce4ddf0d3a6e7621b5f3b150470772f6cf	yes	36

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	34
Claims	35	35
Abstract	36	36

Warnings:					
Information:					
6	Drawings-only black and white line drawings	NL070-14US03_Drawings.pdf	1448094 5d919b66b7f0e4b7cbb076d55020b7cfa67c0d2a	no	8
Warnings:					
Information:					
7	Oath or Declaration filed	NL070-14US03_Declaration.pdf	98862 6bffb6e78e427484e164b066a23a86c6ba6c87cb	no	1
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	43779 5ec13a7146cfa7fe99cacee2dc4b17b2c4ded0e9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3471123		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number.**

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

Doc Code: PA

Document Description: Power of Attorney

PTO/AIA/82A (07-13) Equivalent

Approved for use through 03/31/2021. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Application Number	Filed Herewith
Filing Date	March 14, 2022
First Named Inventor	Hyun Lee
Title	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
Art Unit	TBA
Examiner Name	TBA
Attorney Docket Number	NL070-14US03

SIGNATURE OF Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date (Optional)	March 14, 2022
Name	Jamie J. Zheng	Registration Number	51167
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of 1 forms are submitted

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1 .11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/694,649

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	2 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/694,649	03/14/2022	2811	1820	NL070-14US03	2	2

CONFIRMATION NO. 3889

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

FILING RECEIPT

OC000000132356008

Date Mailed: 03/21/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 17/157,903 01/25/2021
which is a CON of 16/412,308 05/14/2019 PAT 10902886
which is a CON of 15/602,099 05/22/2017 PAT 10290328
which is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

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Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 03/17/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/694,649**
Projected Publication Date: 06/30/2022
Non-Publication Request: No
Early Publication Request: No
Title

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/694,649	03/14/2022	Hyun Lee	NL070-14US03

CONFIRMATION NO. 3889

79141
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3790 El Camino Real #1147
Palo Alto, CA 94304

PUBLICATION NOTICE

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Title:MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Publication No.US-2022-0208233-A1
Publication Date:06/30/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
Sheet	1	of	19	Attorney Docket Number	NL070-14US03

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Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
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				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
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				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
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				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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Examiner Initials	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines,	T

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
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				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
Sheet	5	of	19	Attorney Docket Number	NL070-14US03

		Country Code – Number - Kind Code *(if known)*			Where Relevant Passages or Relevant Figures Appear	
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NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'First Amended Complaint,' filed 03May22, 71 pages
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
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				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Invalidity of U.S. Patent No. 9,318,160 in View of U.S. Patent App. Pub. No. 2011/0026293 (Riho 293),' filed 13JUL22, 53 pages.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Invalidity of U.S. Patent No. 9,318,160 in View of U.S. Patent App. Pub. No. 2010/0195364 (Riho 364),' filed 13JUL22, 46 pages.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Invalidity of U.S. Patent No. 9,318,160 in View of U.S. Patent App. Pub. No. 2010/0091537 (Best),' filed 13JUL22, 60 pages.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Invalidity of U.S. Patent No. 9,318,160 in View of U.S. Patent No. 8,258,619 (Foster),' filed 13JUL22, 24 pages.
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		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of Inter Partes Review, filed August 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1003, 'Declaration of Harold S. Stone,' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1009, 'TI 74LS245 datasheet (2002),' filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Preliminary Response, filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Response, filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February, 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Trial Instituted Document, filed July, 7, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1002, 'Excerpts of FH for U.S. Patent 8,756,364,' filed December, 30, 2016

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1003, 'Declaration of Harold Stone,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1008, 'JEDEC Declaration for DDR Specification,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1015, 'Texas Instruments 74LS245 datasheet (2002),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1017, '2000-03 Samsung CMOS SDRM data sheet,' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1019, 'Final Decision [IPR2014-01011],' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1020, 'Final Decision [IPR2014-00883],' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1023, 'Gordon_Moore_1965_article,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1026, 'Xilinx CoolRunner XPLA3 CPLD product specification (2000),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1027, 'Xilinx Programmable Logic Design Quick Start Handbook (2004),' filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1028, 'Xilinx TQFP package datasheet (2000),' filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1029, 'Xilinx VQFP package datasheet (2002),' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1030, 'Xilinx CS280 package datasheet (1999),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1031, 'Petitioners Demonstratives,' filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2001, 'Exhibit 2001,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2002, 'Exhibit 2002,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2003, 'Exhibit 2003,' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2004, 'Exhibit 2004,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2005, 'Exhibit 2005,' filed September, 15, 2017

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed May 3, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Response, filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Trial Instituted Document, filed May, 15, 2017
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of Inter Partes Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1003, 'Declaration of Dr. Harold Stone,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1009, 'JEDEC Standard Double Data Rate DDR SDRAM Specification, JESD79 June 2000,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1010, 'JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification January 2002,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1011, 'JEDEC Standard DDR2 SDRAM Specification, JESD79-2B January 2005,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1022, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SanDisk Corp. v. Netlist, Inc., IPR2014-01029, Paper No. 11 Dec. 16, 2014,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1023, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, Smart Modular Techs. Inc. v. Netlist, Inc., IPR2014-01369, Paper No. 12 Mar. 9, 2015,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1024, 'Excerpts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 8, 2017,' filed December, 22, 2017

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1025, 'Complainant Netlist, Inc.'s Initial Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1026, 'Respondents' Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1027, 'High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex.1026),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1028, 'Complainant Netlist Inc.'s Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1029, 'Respondents' Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1030, 'High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1031, 'Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SK hynix Inc. et al. v. Netlist, Inc., IPR2017-00577, Paper No. 8 (July 7, 2017),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1032, 'Final Written Decision, Diablo Techs., Inc. v. Netlist, Inc., IPR2014-00882, Paper No. 33 (Dec. 14, 2015),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1033, 'Netlist, Inc. v. Diablo Techs., Inc., No. 2016-1742 (Fed. Cir. July 25, 2017),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1034, 'Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 June 14, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1035, 'Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982,' filed December, 22, 2017

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1039, 'Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1040, 'Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1041, 'Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1042, 'Direct RDRAM datasheet (2000),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 14, 'Patent Owner's Response,' filed October 19,2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February 20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Examination Report, European Patent Application No. 10730021.2, dated April 14, 2014.
		Response to Examination Report, European Patent Application No. 10730021.2, dated June 4, 2014.
		Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015.
		Response to Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015, filed November 4, 2015.
		English Translation of the Notice of Grounds for Rejection, Korean Patent Application No. 2012-7004038, dated May 11, 2016

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
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		Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016
		Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015
		Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs
		Observations by third parties, EP 18179414.0, 22FEB2019, 1 pg
		Patent Document filed by a third party, 20FEB2019, 10 pgs
		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs
		European Search Opinion, EP 18179414, 23OCT2018, 3 pgs
		CN201080039043.0, ‘Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' 30MAY2018, 43 pgs.

Examiner Signature		Date Considered	

Electronically filed August 8, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	TBA
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,

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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 8, 2022

/ Jamie J. Zheng / 51,167

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UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**08/08/2022 05:52:13 PM ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	60853222	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 57

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
160_Inv_Chart1_Admitted_Prior_Art.pdf	39	Non Patent Literature	661 KB
160_Inv_Chart2_Rajan_137.pdf	42	Non Patent Literature	1003 KB
160_Inv_Chart3_Kim.pdf	43	Non Patent Literature	874 KB
160_Inv_Chart4_Ware.pdf	33	Non Patent Literature	815 KB
160_Inv_Chart5_Riho-293.pdf	53	Non Patent Literature	714 KB
160_Inv_Chart6_Riho-	46	Non Patent Literature	778 KB

364.pdf			
160_Inv_Chart7_Best.pdf	60	Non Patent Literature	727 KB
160_Inv_Chart8_Foster.pdf	24	Non Patent Literature	438 KB
160_Inv_Chart9_Jeddeloh.pdf	36	Non Patent Literature	747 KB
160_Inv_Chart10_Gillingham.pdf	61	Non Patent Literature	644 KB
160_Inv_Chart11_Bilger.pdf	45	Non Patent Literature	624 KB
160_Inv_Chart12_Keeth.pdf	47	Non Patent Literature	611 KB
160_Inv_Chart13_Wyman.pdf	31	Non Patent Literature	541 KB
160_Inv_Chart14_Ma.pdf	66	Non Patent Literature	863 KB
160_Inv_Chart15_Ruckerbauer.pdf	44	Non Patent Literature	710 KB
160_Inv_Chart16_Loh.pdf	28	Non Patent Literature	511 KB
160_Inv_Chart17_Rajan-881.pdf	65	Non Patent Literature	670 KB
160_Inv_Chart18_JEDEC.pdf	95	Non Patent Literature	2256 KB
160_Inv_Chart19_Micron_HMC.pdf	30	Non Patent Literature	876 KB
160_Inv_Chart20_Lee.pdf	104	Non Patent Literature	1096 KB
060_Inv_Chart1_Admitted_Prior_Art.pdf	96	Non Patent Literature	900 KB
060_Inv_Chart2_Rajan-	61	Non Patent Literature	1100 KB

137.pdf			
060_Inv_Chart3_Kim.pdf	65	Non Patent Literature	989 KB
060_Inv_Chart5_Riho-293.pdf	71	Non Patent Literature	807 KB
060_Inv_Chart6_Riho-364.pdf	66	Non Patent Literature	879 KB
060_Inv_Chart7_Best.pdf	76	Non Patent Literature	905 KB
060_Inv_Chart8_Foster.pdf	43	Non Patent Literature	536 KB
060_Inv_Chart9_Jeddeloh.pdf	53	Non Patent Literature	836 KB
060_Inv_Chart10_Gillingham.pdf	81	Non Patent Literature	764 KB
060_Inv_Chart11_Bilger.pdf	63	Non Patent Literature	715 KB
060_Inv_Chart12_Keeth.pdf	65	Non Patent Literature	705 KB
060_Inv_Chart13_Wyman.pdf	48	Non Patent Literature	632 KB
060_Inv_Chart14_Ma.pdf	101	Non Patent Literature	1047 KB
060_Inv_Chart20_Lee.pdf	124	Non Patent Literature	1193 KB
060_Inv_Chart19_Micron_HMC.pdf	50	Non Patent Literature	977 KB
060_Inv_Chart18_JEDEC.pdf	114	Non Patent Literature	2353 KB
060_Inv_Chart17_Rajan-881.pdf	82	Non Patent Literature	761 KB
060_Inv_Chart16_Loh.pdf	46	Non Patent Literature	607 KB

060_Inv_Chart15_Ruckerbauer.pdf	67	Non Patent Literature	834 KB
060_Inv_Chart4_Ware.pdf	60	Non Patent Literature	975 KB
2022-07-13_Samsung_Inv_Contentions.pdf	199	Non Patent Literature	1560 KB
Loh_Article.pdf	12	Non Patent Literature	542 KB
Micron_HMC_Presentation.pdf	24	Non Patent Literature	1722 KB
JEDEC_Committee_Proposal_1777-18.pdf	3	Non Patent Literature	504 KB
JEDEC_Committee_Proposal_1777-29.pdf	4	Non Patent Literature	1040 KB
JEDEC_Read_Clock_Proposal.pdf	6	Non Patent Literature	1857 KB
JEDEC_Committee_Proposal_1728.pdf	7	Non Patent Literature	2027 KB
JEDEC_Committee_Proposal_1777-00.pdf	13	Non Patent Literature	2573 KB
JEDEC_Committee_Proposal_1776.pdf	38	Non Patent Literature	8100 KB
JEDEC_Committee_Proposal_1787-01.pdf	11	Non Patent Literature	3044 KB
JEDEC_Committee_Proposal_1797-00c.pdf	20	Non Patent Literature	3744 KB
JEDEC_Committee_Proposal_1787-05.pdf	5	Non Patent Literature	657 KB

JEDEC_Committee_Proposal_1797-00v.pdf	18	Non Patent Literature	2708 KB
2022-05-03_First_Amended_Complaint.pdf	71	Non Patent Literature	3817 KB
NL070-14US03_IDS_Transmittal_2022-08-08.pdf	4	Transmittal Letter	112 KB
NL070-14US03_IDS_List_2022-08-08.pdf	19	Information Disclosure Statement (IDS) Form (SB08)	495 KB

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2022_06_10_Netlist_Complaint_CORRRECTED.pdf	71	Non Patent Literature	9885 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
160_Inv_Chart1_Admitted_Prior_Art.pdf	3F8ECF98FDDF867E7D358A58C799336B7A0A1A16C3AB389B52217676BD9BAC3B8140A0679DFE23AFF9A6A752F07EC216022D102FE0F1FD257109E77F47ADE649
160_Inv_Chart2_Rajan_137.pdf	847A53C7018678CB1FFF1E27881A283405247DAACAE9576AEFEC958BF82CE07B30EB4CD79F0A415C063613956DB9CB6F6CF22FB29DAF9901216303DE816E4034
160_Inv_Chart3_Kim.pdf	583C9EEB3E0D5EBE55E58DDF8C48CC2D633E538EF0D88A58151012F30D0AA0136FB7A954C7B0602B814756085B76A6610880D496E775B03A9A07B030ECD9DB64
160_Inv_Chart4_Ware.pdf	952B3A978550E6A7042FEFB30344030E50A786EF1472A6A0F4

	197D5A3D18141BE9054269BE2D7BA214F225A13A5DF8308918EE57390677 3E3D9881AF1235DBEB
160_Inv_Chart5_Riho-293.pdf	7CF51512B16DBB89E609E8B136B0A0D7562E4872CD3E7ED4B3D26E6C5B4B2A1C01164ADD41B1C984B6B156858433EC2CB30AA7B77B479C74F07ECA85E2B3AB61
160_Inv_Chart6_Riho-364.pdf	63C519E4ACF4E3FF5AE2D20366C00C89E546297EC72A6507D841D3440517A11B89485B746791B5F136EA1B67F35FF0A6878E23DB1134C82AE042E9560D599DB6
160_Inv_Chart7_Best.pdf	B6556D5B07953DE47EE3118B26BAF52231045DD9356350B5117345F0EC3B04FCDE89AC53CF7DED8301E8A0AB8EB4EA14FC07E638D0CE90E302582F24CDB26026
160_Inv_Chart8_Foster.pdf	8A0B52E67D8655A6D92509AFB792BEDBD3778C040D333F4BF64E5B49D1F3D44826DDC57CC286354001614A463B659628DD4A068151D0CBB10B677C9D8B120239
160_Inv_Chart9_Jeddeloh.pdf	6984B67D61C78B8DCDFD94BAAC0652F6E4D5031C7BD3D450B294E2CFFB35E08EBCA523DD6E657A639D911D87217F047B37E203A164061F356CBAA4C80AA1A6AF
160_Inv_Chart10_Gillingham.pdf	14F6D3C15B081DCEC5859303592023AD8CBA1994AE32AA73A08EC8709CAA37580F1C9D6977E6FD360B573B4FA1A1B987615836200A58AB67D3492AD1D0CFE405
160_Inv_Chart11_Bilger.pdf	1D363A4CE67F1186CDA440D12736D6585F67A2FD524F47A04545E0E86C2FC9C11795E4A51DAF450B9C2DFF4E905C28B7BF4FECD98C38203467EE51009C248A30
160_Inv_Chart12_Keeth.pdf	52FBE8C3E298BD94570E75A6D3DAD13020CC43A32EA68EF391C9261C19339864C0308FFA8A9475EC6996BC5CC100AC765FF383AA0E5F6372ADF5E1657A6B84B4
160_Inv_Chart13_Wyman.pdf	098E22DDC3CD4F96136281EE7312B017DD7A308074B3BE9B95BB1790CEF6C59F9569136594064 4BBB6416A18577136644AAB3A7A60EEBE797CBBA40397BB6893
160_Inv_Chart14_Ma.pdf	F7255D8B18260691048B4C53CE9BB5415884 1103BE7E9D089A

	083F4F08B095C72C72EF2DC95D919708A4FE5ED9404A5AAFB119D5A8A82FD17755BB14DF8F6B56
160_Inv_Chart15_Ruckerbauer.pdf	6CF23BD633B08EFA57996720A8B8CACFC98E1E3D840220D798E41F78B897D7BBCBB1C71961DE76CB32A776A141226A09BCBC2CD0F5E7160718819DB85630F890
160_Inv_Chart16_Loh.pdf	7EB6881436B468F51F56A88EB6A3DF39751903B8152FFE32899CB014BEFA966798567E2B878D86292568DAAB68717049A2411232E3F8B552745B3F0D0D965691
160_Inv_Chart17_Rajan-881.pdf	38EB5CABA0744A531042D026132B6E908A98A171E38873D88EE46A9E7C56A1B93DD518F0FA611A652F31457708 4D0A04D7D6254C763BDAECDEF6D12F3262F64A
160_Inv_Chart18_JEDEC.pdf	CA4EC44EA66B92F9C459EEF8C3FE0F686877017B41989C41348F262F1EB7F893442ED9D489CA31726AC0F7A97D2E0C3EF589CD3556100F82C3D5CBD0BD14F6A0
160_Inv_Chart19_Micron_HMC.pdf	7173039368B9595848B774690E2795D027AA659554A27124B4F0149DB44E825C92B637E70E709DCF697940CC49299719FCB6FDA74E9439523097CCBFFD0C1E65
160_Inv_Chart20_Lee.pdf	803F77D4BF83B42E43D744AA1FB07A38FD896AE11A0B8DFF3347FDD72A6EE2445BE44D753AB442E26D7A0961A47124EF442FFF39663C1297368119D797E2AAAA
060_Inv_Chart1_Admitted_Prior_Art.pdf	A9F375193B7C9CD381050F88458E149CDF91A96C68C2BB86420569358343A4E419A7F0DC52935C9531FF3ECFC1DB51754FF42D8D035BACCDA3726EA08E228E98
060_Inv_Chart2_Rajan-137.pdf	DDBFBC64077C89D8ACA240752D7D46AF3B9C43395816B4C59DBD5132284234E4CC489BB65E9EE202C347E97CBF6F69BE334E5678601E6659C3A6E47F598C98E2
060_Inv_Chart3_Kim.pdf	B00BA5306BE4941CD7BF7EF4BD3A3A38EC819B2CF0AE25DD43D466C7519206BE837C9D8FADE4A1EE3B6636B70EC2051A23D1C494F16BCFE35D5F4C146088CCE2
060_Inv_Chart5_Riho-293.pdf	C01D0B343128FEC8267802E46CA8B988BA32A572F484259A1E

	D8640C70EB509D1594BA7C567522F1DA31CCF5D8E5DE55DE44F7DA75B47EBF36D4ACC91CCFF42F
060_Inv_Chart6_Riho-364.pdf	3173AD33A414DC8A696F1EA838001250DDB0430DD5E15CCEC40551C9486F8C7E829749C6840AB7B5DDDE62A5C1EB40B436757B37A8E6DB0C1C1A1509A9CD39AC
060_Inv_Chart7_Best.pdf	E0C0B06ECAD802BD59E61F800C4697F8F1147A411D8E92053F69DEAFD7F69F21344B79A8B2FD05510F35AE03369939 4B68A52549019368FA12A9253A8C996A79
060_Inv_Chart8_Foster.pdf	44A9E73F414E62601C2242BA3B440A4188CED1FD9E8876425D30196920FEC8A15D11DE8D75958FD61C086CCECEAB98508D2964D518CD5E839D833EF0198ACB24
060_Inv_Chart9_Jeddeloh.pdf	B1E22787DB039A465D856FE6522905C36C8EE5457552A3E338FDB9B141ADA8C0E387F1D13AAB950D5A382A22E0CC38539BCFBCBD0B61C8AF96D7A967967F6A26
060_Inv_Chart10_Gillingham.pdf	E9C8E78B08F9776F5D76542CB0B32931E4EB3326C8A088249D81CE45FD63CB0706D762F70EF2476AFEF7A1B22E1FAF856F059E5FE0C60EEB4E5622DF608E6C02
060_Inv_Chart11_Bilger.pdf	5EF5880842B43ED3CC8E429C41DAE010EE07639DFEFA08D55E1022302ADB2A557C7900D2CA7440860B14233956F935F544F28FC2A2A7766BAB3163EC710EE2FA
060_Inv_Chart12_Keeth.pdf	C6E2711D2C07E51B063D8E7651B1DCFBC98479193779E179C6D4C0BDA84D52CE80010E00F0391AC1AB58A521B6ED73A23085791C871940884AF2A45368113218
060_Inv_Chart13_Wyman.pdf	9A6407E5312125D76895326D3771185A13E91F9896FC621F2DFA68137B865594F94B95D84CD17BA51C8D9A289BB546662DCFAFD8426A35B09FB2D8A98BE55FE6
060_Inv_Chart14_Ma.pdf	4B709DC98B8F4E1FDB7B3412609A499ACAE72FEF3C76AD181626A658408EBB006ECF65FB146CC783A57798FFF92300BCDD0574EDAF6B4C2D650FD981CB51B105
060_Inv_Chart20_Lee.pdf	921556BC206FF11A59EF63E7625CAEA7CF6207F25DA768D8D

	916FCC606DE2A7DEA755E61B520784269AF987DA2E7C9F7DA16A3D69147D086F1E078D451E042A5
060_Inv_Chart19_Micron_HMC.pdf	FD62266264E88226118D0D92ACBB865AD4FE5BCD122A507E077C4F06038E12B68A76B1E7126A52481076DE88D33E232F0CF8144B6E4E5424069B53CAA9B38903
060_Inv_Chart18_JEDEC.pdf	CE962C031097BBB97A931B0138574C9BD83D4FEDA9ACFD438A6D3DF8283DF0E8DDA4D9328371D08784F9D05EBE9EEC82C4F566935A2BC1999665C09ACC3A77CB
060_Inv_Chart17_Rajan-881.pdf	0B236FC18C3C48710240E80984F5E573AA697BE6A254C95B794E2C2F0F7F25AD37DFD3556106ED7EE9C0828424A3EB00F73023AAD393730E9C483B93FA1EED1E
060_Inv_Chart16_Loh.pdf	C7CAC78D6458F533075E9FF9BF03D2354159C43A18572ADE0F12137680864568F0F0EDEDD36CADF47889FDD389EA0DBF5056658C9C746DB131C7A404D7296E1E
060_Inv_Chart15_Ruckerbauer.pdf	4E63F5D640960010238E32B0C60F5045A7C3A0E0B602BC4CB756235F96F74E5FCF73D9FB3C57C86D3780668C6F1C235324BEFB1C29D6DF9A5627A734F876A83A
060_Inv_Chart4_Ware.pdf	8B4E70680A62226930D85D41F13B430F352C4E9AB3D4D4E105A2E899725D0923D5E0A814F9BA85BBD8A41486AE7CDE08874E9C4B69FBD4C188DBEEECC6411BA1
2022-07-13_Samsung_Inv_Contentions.pdf	297CC51F84DDB998617C376920B6F5C3B93CD5F6534A8B780A1FF9B8AC92ECCC52FFB6EF26A2AC12962A11BA33B2A4C4270412F58E565C2F5E434BF374FE0B5D
Loh_Article.pdf	7C84DE54450E4CD6436104F88B4454B7B1F3F980C5CCC607D3E791773C8D24AF876A33EDA7321DB0C19983A29287441D690D3F272DB39568906247AAC127A275
Micron_HMC_Presentation.pdf	513C70C9DEAC95B723FD049853BCFA6615C5F0A02C92802063F750F06860E001E5B1145FEF10CF53E75D046EB05D30BE6407C042CAF3B3A80379CEFA56C9A2C8
JEDEC_Committee_Proposal_1	93E8BE33ED339AF430EEF11E2F4329B9ED6C4B29C1B68E918

777-18.pdf	0D4E72801B3F0BB7942B983D1660334FDD67F6B1965604E4C499B2C93567D2C21C60BF56D3116A2
JEDEC_Committee_Proposal_1777-29.pdf	CE258B324AF314DBA65033509ECA599E73D904546DDCE694ECB1515288B9DDB41E8F3CA167A24F4090C950246455F074C7E1C684693648D4279FCBC1B18A4AA3
JEDEC_Read_Clock_Proposal.pdf	0FCAD919EEB3FF4B215977AD3D5FBF92F4718BA1E3569B9344F376681075AEF248F4427110D30D3C2A3C33C5B4EAD27C9BA59995D73F650EFC211A3BF31BAE18
JEDEC_Committee_Proposal_1728.pdf	8266FE6363A467A44B63900B857D213F8A7CD06C272B6F8B9DCF7A351C4F5F2A15CF32DD241714B493CA6CE2E98A5B2C92637C6068FB23BAB4D4ED22CCB6D801
JEDEC_Committee_Proposal_1777-00.pdf	3CB504837F35B5D9C1DBFE1082F43CB5CAA5F34810CA5413962A3757C1974C665EEAF5997FCBF4A8AF393B90023D681E2F48BF1BDDD30D27AB9F4E4D8A1E5C93
JEDEC_Committee_Proposal_1776.pdf	934070FB8CB8637A267CFA93F4CC3FDA64DF0BBD689B04CF41AF346D28FE39735FF0F8F64AD73EB3CBE398ED6EC827BB4766C7779DC4E3DC03A1FC4AE30F7C65
JEDEC_Committee_Proposal_1787-01.pdf	8C15C0E866004096B0C916D634973D0C51449C5D50E8222DCC8B333D3EE19C5BB86555D372BC8783B7E96B9C259BFFE997002042D8776E63CDEBD980EB6370F4
JEDEC_Committee_Proposal_1797-00c.pdf	0FEF50E1F3694E8C26A1694BB515C2AA381D3BFF9BD9DD853B900CBBA5445D731C365A59B54B30EBBF2D7EB08D112E4466E4580F7BFE77B54EAE656E54F7AB11
JEDEC_Committee_Proposal_1787-05.pdf	8D9017C19EC571F1501F59F16096C78B101775B0D2B31281E3EAD82EE16B18FBA33B36C2F104258C42306C9C51F9E49742BD77418945C7E59E277C8767A5FB9A
JEDEC_Committee_Proposal_1797-00v.pdf	25892598FE49B96624775DD9A909B6C40455CF502F76EC4D0EF92F50A18B56AE3C153737AB9C491D3D36FA823EB4873E3AFC2E559A35F1B8A7ABCB74F9BB01D3
2022-05-	F6529A3F2A6742A3C0CAB0E86C5A422DBF2BE89863C337796

03_First_Amended_Complaint.pdf	2050D6CB1D5F31BCFF45845A1FAD0CB5E4C0DD780AEFF633D2068A401F348FA1D1CB3C22AAEDCE5
NL070-14US03_IDS_Transmittal_2022-08-08.pdf	26B2C7B2C63676C666B96B7F5182B0853DFE2501BE7F881F2CC7AD613A31729B024037D4F1225741A658391135AA88DEB9BEA6250E947BFF08B3F3EEB0C75C70
NL070-14US03_IDS_List_2022-08-08.pdf	10766AF33F63729F4B969BDD342A0BB15BC102882640AC00F899FD66B127DE5B03B43D258768C2897F45EF79F75F71478660A5D4FD0BAAFC6F20F9BCFD21BE49
2022_06_10_Netlist_Complaint_CORRRECTED.pdf	9F377C36E76A95F329339DADB2DA4625C42D81C5A039FD501D2F405781AD97E87294C6BE046661B1A40A16D77F07B24060F9B9ADB14DE7B884495D554350734F

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 10/05/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/05/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 103

Office Action Summary	Application No. 17/694,649	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 14 March 2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-2 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-2 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 14 March 2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a

result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claims 1 and 2 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 8 and 9 of U.S. Patent No. 10,902,886. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 is anticipated by claims 1, 8 and 9 of the patent and claim 2 would have been obvious over claims 1, 8 and 9 of the patent.

Regarding claim 1: Claims 1, 8 and 9 of the patent recite a DRAM package, comprising:

stacked array dies including at least a first array die and a second array die, the second array die being stacked over at least the first array die (claim 1, line 17);

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals (claim 1, lines 12-16);

control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies (claim 8);

first data interconnects between respective ones of the data terminals and the first array die;

second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size (claim 9).

Regarding claim 2: It would have been obvious to one of ordinary skill in the art to recognize that the DRAM package of claims 1, 8 and 9 is used to perform a method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via

which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

4. Claims 1 and 2 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 and 11 of U.S. Patent No. 10,290,328. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 is anticipated by claims 1 and 11 of the patent and claim 2 would have been obvious over claims 1 and 11 of the patent.

Regarding claim 1: Claims 1 and 11 of the patent recite a DRAM package (claim 1, lines 11-12), comprising:

stacked array dies (claim 1, line 16) including at least a first array die and a second array die, the second array die being stacked over at least the first array die;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals (claim 1, lines 13-15);

control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies;

first data interconnects between respective ones of the data terminals and the first array die;

second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size (claim 11).

Regarding claim 2: It would have been obvious to one of ordinary skill in the art to recognize that the DRAM package of claims 1 and 11 of the patent is used to perform a method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second

data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

5. Claims 1 and 2 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 ad 2 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 is anticipated by claims 1 and 2 of the patent and claim 2 would have been obvious over claims 1 and 2 of the patent.

Regarding claim 1: Claims 1 and 2 of the patent recite a DRAM package (claim 1, line 7), comprising:

stacked array dies (claim 1, line 14) including at least a first array die and a second array die, the second array die being stacked over at least the first array die;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals (claim 1, lines 9-12);

control interconnects (die interconnects) between respective ones of the control terminals and one or more array dies in the stacked array dies;

first data interconnects (die interconnects) between respective ones of the data terminals and the first array die;

second data interconnects (die interconnects) distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers (claim 1, lines 27-34) coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second

data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size (claim 2).

Regarding claim 2: It would have been obvious to one of ordinary skill in the art to recognize that the DRAM package of claims 1 and 2 of the patent is used to perform a method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

6. Claims 1 and 2 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of U.S. Patent No. 9,318,160. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1

is anticipated by claims 10 of the patent and claim 2 would have been obvious over claim 10 of the patent..

Regarding claim 1: Claim 10 of the patent recites a DRAM package (claim 10, line 6), comprising:

stacked array dies (claim 10, line 12) including at least a first array die and a second array die, the second array die being stacked over at least the first array die;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals (claim 10, lines 8-11);

control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies;

first data interconnects between respective ones of the data terminals and the first array die;

second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers (claim 10, lines 23-31) coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size.

Regarding claim 2: It would have been obvious to one of ordinary skill in the art to recognize that the DRAM package of claim 10 of the patent is used to perform a method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

7. Claims 1 and 2 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 11, 15 and 29 of U.S. Patent No. 8,787,060. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 is anticipated by claims 11, 15 and 29 of the patent and claim 2 would have been obvious over claims 11, 15 and 29 of the patent.

Regarding claim 1: Claims 11, 15 and 29 of the patent recite a DRAM package (claim 29, line 6), comprising:

stacked array dies (claim 11, line 5 and claim 29, line 12) including at least a first array die and a second array die, the second array die being stacked over at least the first array die;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals (claim 29, lines 8-11);

control interconnects between respective ones of the control terminals and one or more array dies in the stacked array dies;

first data interconnects between respective ones of the data terminals and the first array die;

second data interconnects distinct from the first data interconnects and between respective ones of the data terminals and the second array die; and

drivers (claim 15) coupled to the data terminals and configured to drive first data signals to the first array die via the first data interconnects and second data signals to the second array die via the second data interconnects, a respective signal of the first data signals being driven by one or more drivers having a first driver size, a respective signal of the second data signals being driven by one or more drivers having a second driver size different from the first driver size.

Regarding claim 2: It would have been obvious to one of ordinary skill in the art to recognize that the DRAM package of claims 11, 15 and 29 of the patent is used to perform a method, comprising:

at a DRAM package including stacked array dies, terminals and drivers configured to drive signals from the terminals to the stacked array dies, the stacked

array dies including a first array die and a second array die, the second array die being stacked over at least the first array die, the terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

selecting a first driver size to drive a first data signal received at one of the data terminals to the first array die via a first data interconnect; and

selecting a second driver size to drive a second data signal received at the one of the data terminals to the second array die via a second data interconnect, the second data interconnect being distinct from the first data interconnect, the second driver size being different from the first driver size.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 17/694,649	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-10290328-B2	05-2019	Lee; Hyun	G11C7/1057	1/1
*	B	US-10902886-B2	01-2021	Lee; Hyun	G11C5/06	1/1
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	09/28/2022								
	1	✓								
	2	✓								

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

CPC - Searched*		
Symbol	Date	Examiner
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	09/28/2022	HH

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
365	63	09/28/2022	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search	09/28/2022	HH
Assignee and Inventor search	09/28/2022	HH

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	32	"10902886"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 08:37 AM
L2	99	"8787060"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 08:37 AM
L3	32	1	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 11:27 AM
L4	62347	(G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:25 PM
L5	2848	4 AND (dram dynamic ADJ ram dynamic ADJ random) WITH (package module)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:26 PM
L6	187	5 AND control adj3 terminal AND data adj3 terminal	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:27 PM
L7	85	6 AND interconnect$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2022/09/28 02:27 PM

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			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	15	7 AND driver WITH size	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:28 PM
L9	116069	(dram dynamic ADJ ram dynamic ADJ random) WITH (package module)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:29 PM
L10	1693	9 AND control adj3 terminal AND data adj3 terminal	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:29 PM
L11	415	10 AND interconnect$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:29 PM
L12	17	11 AND driver WITH size	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:30 PM
L13	15	12 AND stack$3 WITH die	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:34 PM
L14	3946532	netlist.as. lee.in.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2022/09/28 02:35 PM

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			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	1500	14 AND dram WITH package	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:36 PM
L16	23	15 AND control$4 adj2 terminal AND data adj3 terminal	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:36 PM
L17	20	16 AND die WITH stack$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:36 PM
L18	15	17 AND driver WITH size	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 02:37 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
Sheet	1	of	19	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,345,412	1994-09-06	Shiratsuchi	
		5,537,584	1996-07-16	Miyai	
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		6,618,791	2003-09-09	Dodd	
		6,683,372	2004-01-27	Wong	
		6,704,910	2004-03-09	Hong	
		6,717,855	2004-04-06	Underwood	
		6,721,860	2004-04-13	Klein	
		6,747,887	2004-06-08	Halbert	
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		7,093,066	2006-08-15	Klein	
		7,098,541	2006-08-29	Adelmann	
		7,130,308	2006-10-31	Haddock	

Examiner Signature	/HUAN HOANG/	Date Considered	/HUAN HOANG/

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1035, 'Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982,' filed December, 22, 2017

Examiner Signature	/HUAN HOANG/	Date Considered	09/28/2022

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
Sheet	18	of	19	Attorney Docket Number	NL070-14US03

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1039, 'Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1040, 'Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1041, 'Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1042, 'Direct RDRAM datasheet (2000),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 14, 'Patent Owner's Response,' filed October 19,2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February 20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Examination Report, European Patent Application No. 10730021.2, dated April 14, 2014.
		Response to Examination Report, European Patent Application No. 10730021.2, dated June 4, 2014.
		Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015.
		Response to Examination Report, European Patent Application No. 10730021.2, dated April 29, 2015, filed November 4, 2015.
		English Translation of the Notice of Grounds for Rejection, Korean Patent Application No. 2012-7004038, dated May 11, 2016

Examiner Signature	/HUAN HOANG/	Date Considered	09/28/2022

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 8, 2022	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	TBA
Sheet	19	of	19	Attorney Docket Number	NL070-14US03

		Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016
		Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015
		Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs
		Observations by third parties, EP 18179414.0, 22FEB2019, 1 pg
		Patent Document filed by a third party, 20FEB2019, 10 pgs
		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs
		European Search Opinion, EP 18179414, 23OCT2018, 3 pgs
		CN201080039043.0, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' 30MAY2018, 43 pgs.

Examiner Signature	/HUAN HOANG/	Date Considered	09/28/2022

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/694,649	Filing Date 03/14/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/05/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronically filed April 5, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated October 5, 2022, for the above identified patent application.

Applicant petitions for a three-month extension of time, which extends the due date for responding to the Office Action from January 5, 2023, to April 5, 2023.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM array dies including at least a first plurality of DRAM array dies and a second plurality of DRAM array dies~~, the second array die being stacked over at least the first array die~~;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects ~~between~~ coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a control or address signal to [[~~and~~]] one or more DRAM array dies in the stacked DRAM array dies;

first data interconnects electrically coupled to data ports on ~~between respective ones of the data terminals and~~ the first plurality of DRAM array dies and electrically isolated from data ports on any of the second plurality of DRAM array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies;

second data interconnects electrically coupled to data ports on ~~distinct from the first data interconnects and between respective ones of the data terminals and~~ the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die; and

drivers coupled to the data terminals and including ~~one or more~~ first drivers ~~configured~~ configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and ~~one or more~~ second drivers ~~configured~~ configurable to drive second data signals to the second plurality of DRAM array dies via the second data

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interconnects, a respective signal of the first data signals being driven by ~~the one or more first drivers~~ a respective first driver having a first driver size, a respective signal of the second data signals being driven by ~~the one or more second drivers~~ a respective second driver having a second driver size different from the first driver size.

2. A method, comprising:

at a dynamic random access memory (DRAM) package including stacked DRAM array dies, ~~terminals and drivers configured to drive signals from the terminals to the stacked array dies,~~ the stacked DRAM array dies including a first plurality of DRAM array dies and a second plurality of DRAM array dies, ~~the second array die being stacked over at least the first array die,~~ the ~~terminals~~ DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a command/address signal to one or more DRAM array dies in the stacked DRAM array dies,[[;]]

driving first data signals received at respective data terminals to the first plurality of DRAM array die via respective first data interconnects, including enabling ~~selecting~~ a first driver having a first driver size to drive a first data signal ~~received at one of the data terminals~~ to the first plurality of DRAM array dies via a first data interconnect, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies; and

driving second data signals received at respective data terminals to the second plurality of DRAM array dies via respective second data interconnects, including enabling ~~selecting~~ a second driver having a second size to drive a second data signal ~~received at the one of the data terminals~~ to the second plurality of DRAM array dies via a second data interconnect, each of the second data interconnects ~~being distinct from the first data interconnect~~ including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die, the second driver size being different from the first driver size;

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wherein the first data interconnects are electrically coupled to data ports on the first plurality of DRAM array dies and electrically isolated from data ports on any of the second plurality of DRAM array dies, and wherein the second data interconnects are electrically coupled to circuitry on the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies.

3. (New) The DRAM package of claim 1, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

4. (New) The DRAM package of claim 1, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

5. (New) The DRAM package of claim 1, wherein:

each of the second plurality of DRAM array dies is stacked over at least one of the first plurality of DRAM array dies; and

the second driver size is greater than the first driver size.

6. (New) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of DRAM array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of DRAM array dies and one of the second data interconnects.

7. (New) The DRAM package of claim 1, wherein:

the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;

the plurality of chip select interconnects respectively coupled to the first plurality of DRAM array dies; and

the plurality of chip select signals are configured to select one array die among the first plurality of DRAM array dies to receive data in the first data signals.

8. (New) The DRAM package of claim 7, further comprising a control die between the stacked DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers

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coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

9. (New) The method of claim 2, wherein each of the drivers includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (New) The method of claim 2, wherein each of the drivers includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (New) The method of claim 2, wherein the control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of DRAM array dies, the method further comprising:

driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects, to select one array die among the first plurality of DRAM array dies to receive the first data signals.

12. (New) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM array dies;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the plurality of stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the plurality of

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stacked DRAM array dies, the control interconnects including a plurality of chip select interconnects; and

data interconnects, wherein:

each of the data interconnects is electrically coupled to data ports on a subset of the plurality of stacked DRAM array dies and is electrically isolated from data ports on any other array die not in the subset of the plurality of stacked DRAM array dies;

the data interconnects include first data interconnects electrically coupled to a first subset of DRAM array dies in the plurality of stacked DRAM array dies, the first subset of DRAM array dies including a first plurality of DRAM array dies;

each respective array die of the first plurality of DRAM array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of DRAM array dies and at least one second TSV in at least one second array die not in the first subset of DRAM array dies;

a respective TSV in the first subset of TSVs is coupled to a corresponding data port on a respective array die in the first subset of DRAM array dies; and

the at least one second TSV is electrical isolated from any data port on the at least one second array die.

13. (New) The DRAM package of claim 12, wherein each of the plurality of stacked DRAM array dies includes a DRAM integrated circuit (IC) chip, the DRAM IC chip including a number of memory cells.

14. (New) The DRAM package of claim 13, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is electrically isolated from memory cells on the corresponding array die.

15. (New) The DRAM package of claim 14, wherein each of the at least one second TSV includes a conducting material in a corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

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16. (New) The DRAM package of claim 14, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is connected to a stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (New) The DRAM package of claim 13, further comprising a control die between the stack of DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

18. (New) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects electrically coupled to a second subset of DRAM array dies in the plurality of stacked DRAM array dies, the second subset of DRAM array dies including a second plurality of DRAM array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals being driven by a respective first driver having a first driver size, a respective signal of the second data signals being driven by a respective second driver having a second driver size different from the first driver size.

19. (New) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

20. (New) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

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REMARKS

This amendment responds to the Non-Final Office Action dated October 5, 2022. In the office action, the Examiner:

- rejected claims 1 and 2 on the ground of nonstatutory double patenting as being unpatentable over claims 1, 8 and 9 of U.S. Patent No. 10,902,886;
- rejected claims 1 and 2 on the ground of nonstatutory double patenting as being unpatentable over claims 1 and 11 of U.S. Patent No. 10,290,328;
- rejected claims 1 and 2 on the ground of nonstatutory double patenting as being unpatentable over claims 1 ad 2 of U.S. Patent No. 9,659,601;
- rejected claims 1 and 2 on the ground of nonstatutory double patenting as being unpatentable over claim 10 of U.S. Patent No. 9,318,160; and
- rejected claims 1 and 2 on the ground of nonstatutory double patenting as being unpatentable over claims 11, 15 and 29 of U.S. Patent No. 8,787,060.

REMARKS CONCERNING CLAIMS

Claims 1 and 2 have been amended.

New claims 3-20 are presented. Support for the amendments and the new claims can be found throughout the specification as filed with reference to the drawings as filed.

No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 1-20.

REMARKS CONCERNING REJECTIONS OF ORIGINAL CLAIMS

I. REJECTION OF CLAIMS 1 AND 2 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d).

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Applicant believes that claims 1 and 2 as amended and the added new claims are patentably distinct from any of claims 1, 8 and 9 of U.S. Patent No. 10,902,886, claims 1 and 11 of U.S. Patent No. 10,290,328, claims 1 ad 2 of U.S. Patent No. 9,659,601, claim 10 of U.S. Patent No. 9,318,160, and claims 11, 15 and 29 of U.S. Patent No. 8,787,060. Therefore, Applicant's filing of the terminal disclaimer is for the sole purpose of advancing prosecution. It should not be understood as implying that Applicant agrees with the rejection of original claims 1 and 2 on the ground of nonstatutory double patenting made in the Office Action, or that any of the pending claims after entry of this amendment is subject to rejection on the same ground.

REMARKS CONCERNING AMENDED AND NEW CLAIMS

Claims 1-2 as amended are believed to be patentable.

New claims 3-8 depend from claim 1 as amended and include further limitations in addition to the limitations in claim 1 as amended. Therefore, claims 3-8 are patentable for at least analogous reasons claim 1 as amended is patentable.

New claim 9-11 depend from claim 2 as amended and include further limitations in addition to the limitations in claim 2 as amended. Therefore, claims 9-11 are patentable for at least analogous reasons claim 2 as amended is patentable.

New claims 12-20 are believed to be patentable.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner

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is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 5, 2023

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Electronic Patent Application Fee Transmittal

Application Number:	17694649
Filing Date:	14-Mar-2022
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL070-14US03

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
			Total in USD ($)	**1480**

Electronic Acknowledgement Receipt

EFS ID:	47799670
Application Number:	17694649
International Application Number:	
Confirmation Number:	3889
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL070-14US03
Receipt Date:	05-APR-2023
Filing Date:	14-MAR-2022
Time Stamp:	22:37:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1480
RAM confirmation Number	E202345M53109716
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL070-14US03_Amendment_NFOA.pdf	185177 dfca2f9cfe19bd54efa226241b23a409a47a9ccb	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	38532 63eabcd4ae6c36097884155b0d6f15172103d1b0	no	2

Warnings:

Information:

Total Files Size (in bytes):	223709

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	17694649
Filing Date	14-Mar-2022
First Named Inventor	Hyun Lee
Attorney Docket Number	NL070-14US03
Title of Invention	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

( ) Small Entity

( ) Micro Entity

(●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

(●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

( ) A sole inventor

( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

( ) A joint inventor; all of whom are signing this request

Signature	/Jamie Zheng/
Name	Jamie Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	17694649
Filing Date:	14-Mar-2022
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL070-14US03

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17694649

Filing Date: 14-Mar-2022

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on April 5, 2023

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	47799727
Application Number:	17694649
International Application Number:	
Confirmation Number:	3889
Title of Invention:	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL070-14US03
Receipt Date:	05-APR-2023
Filing Date:	14-MAR-2022
Time Stamp:	23:02:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E202345N02125401
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	42984 65f27746a1bf81aa3a1b0cbf99b77d8cd5223d04	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37774 40bbc4293f26667370a0a7c3506e32f0019bac3c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	80758		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/694,649	Filing Date 03/14/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/07/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	5	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,466,496	2002-10-15	Shigehiro Kuge	
		6,553,450	2003-04-22	Jim M. Dodd	
		6,594,167	2003-07-15	Kyoji Yamasaki	
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		8,258,619	2012-09-04	Jimmy G. Foster, Sr.	
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		8,315,068	2012-11-20	Jimmy G. Foster	
		8,325,539	2012-12-04	Hwan-Wook Park	

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	2	of	5	Attorney Docket Number	NL070-14US03

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		8,411,478	2013-04-02	Tae Sik Yun	
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		20110193226	2011-08-11	Kyle K. Kirby	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Petition for Inter Partes Review of U.S. Patent No. 8,787,060, filed August 26, 2022.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Patent Owner Prelminary Response, filed January 19, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Petitioner's Authorized Reply to POPR, filed February 17, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, PO's Preliminary Sur-Reply, filed March 1, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Institution Decision: Granting Institution of Inter Partes Review 35 U.S.C. sec. 314, filed April 12, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petition for Inter Partes Review of U.S. Patent No. 9,318,160, filed August 26, 2022.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Patent Owner Prelminary Response, filed January 19, 2023.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	3	of	5	Attorney Docket Number	NL070-14US03

		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petitioner's Authorized Reply to POPR, filed February 17, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Patent Owner's Preliminary Sur-Reply, filed March 1, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Institution Decision: Granting Institution of Inter Partes Review 35 U.S.C. sec. 314, filed April 12, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Exhibit 1003, 'Wolfe declaration,' filed August 26, 2022.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Exhibit 1003, 'Wolfe declaration,' filed August 26, 2022.
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		USPTO Patent Trial and Appeal Board, Appeal 2014-007777, Inter Partes Reexamination Control 95/000,546 & 95/000,577, US Patent 7,289,386, DECISION ON APPEAL, issued 2015-02-25, 25 pgs.
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	4	of	5	Attorney Docket Number	NL070-14US03

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		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, "Samsung's Fourth Amended Initial and Additional Disclosures," filed 2022-12-06, 23 pgs.
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		Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, 296 pgs. (uploaded in three parts).
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	5	of	5	Attorney Docket Number	NL070-14US03

		Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design," 2nd Edition, Chapter 3, Department of Electrical and Computer Engineering University of Toronto, 2008, McGraw-Hill Companies, Inc. 10 pgs.
		HAROLD S. STONE, "Microcomputer Interfacing," University of Massachusetts, Amherst, 1982, Addison-Wesley Publishing Company, Inc. 399 pgs. (uploaded in three parts).

Examiner Signature		Date Considered	

Electronically filed May 12, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,

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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: May 12, 2023

/ Jamie J. Zheng / 51,167

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UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**05/12/2023 11:12:32 PM ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	62085915	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 46

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
IPR2022-01428_Prelim_Sur-Reply.pdf	12	Non Patent Literature	165 KB
IPR2022-01428_Reply_POPR.pdf	24	Non Patent Literature	354 KB
IPR2022-01427_Prelim_Sur-Reply.pdf	12	Non Patent Literature	166 KB
IPR2022-01427_Reply_POPR.pdf	22	Non Patent Literature	324 KB
IPR2022-01428_Institution_Decision.p	29	Non Patent Literature	720 KB

df			
IPR2022-01427_Institution_Decision.pdf	29	Non Patent Literature	713 KB
IPR2022-01428_POPR.pdf	64	Non Patent Literature	1966 KB
IPR2022-01427_POPR.pdf	66	Non Patent Literature	2001 KB
IPR2017-00668_FWD.pdf	46	Non Patent Literature	1145 KB
IPR2017-00667_FWD.pdf	44	Non Patent Literature	1145 KB
IPR2018-00362_FWD.pdf	94	Non Patent Literature	3431 KB
IPR2022-01427_Petition.pdf	146	Non Patent Literature	9176 KB
Exh1035_GDDR4_SGRAM.pdf	72	Non Patent Literature	4669 KB
Exh1030_Digital_Logic_Book.pdf	10	Non Patent Literature	5121 KB
Exh1023_Jacob_Paper.pdf	22	Non Patent Literature	861 KB
Ex_2020_Sams_Oppo_N_MPSJ_Sams_Invalidity_Defenses.pdf	29	Non Patent Literature	955 KB
Ex_2019_N_MPSJ_Sams_Invalidity_Defenses.pdf	22	Non Patent Literature	820 KB
Ex_2013_Sams_4th_Amended_Initial_and_Addtl_Disclosures.pdf	10	Non Patent Literature	374 KB
IPR2022-01428_Petition.pdf	164	Non Patent Literature	11838 KB
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Ex_2017_JEDEC_Standard_21-C.pdf	82	Non Patent Literature	1665 KB
Ex_2006_Sams_Resp_N_Objs_CC_Memo_Ord.pdf	11	Non Patent Literature	492 KB
Ex_2008_N_Oppo_Sams_MSJ_Non-Infringement_Patents.pdf	23	Non Patent Literature	717 KB
Ex_2005_N_Objs_Memo_Opinion_and_Order_re_CC.pdf	5	Non Patent Literature	259 KB
Ex_2007_Stacked_DRAM_Spiral_TSV_Structure.pdf	3	Non Patent Literature	1545 KB
Ex_2003_Sams_Responsive_CC_Brief.pdf	38	Non Patent Literature	1175 KB
IPR2022-01428_Ex_1003_Decl_Andrew_Wolfe.pdf	440	Non Patent Literature	14272 KB
Ex_2001_Sams_Prelim_CC_and_Extrinsic_Evid.pdf	55	Non Patent Literature	858 KB
Ex_2002_Sams_Constructions.pdf	69	Non Patent Literature	1125 KB
Ex_2004_CC_Order.pdf	35	Non Patent Literature	1906 KB
IPR2022-01427_Ex1003_Wolfe_Declaration.pdf	343	Non Patent Literature	12146 KB
Ex_1045_Sams_Answer_FAC.pdf	53	Non Patent Literature	637 KB

Ex_1049_Sams_MSJ_Noninfringment.pdf	19	Non Patent Literature	852 KB
Ex_1029_386_Reexam_Decision.pdf	25	Non Patent Literature	2479 KB
Ex_1043_Netlist_v_Samsung_Complaint.pdf	49	Non Patent Literature	4082 KB
Ex_1038_Microcomputer_Interfacing_pt2.pdf	121	Non Patent Literature	9638 KB
Ex_1021_JEDEC_MO-207.pdf	22	Non Patent Literature	953 KB
Ex_1038_Microcomputer_Interfacing_pt1.pdf	140	Non Patent Literature	11144 KB
Ex_1020_Decl_Julie_Carlson.pdf	7	Non Patent Literature	214 KB
Ex_1038_Microcomputer_Interfacing_pt3.pdf	142	Non Patent Literature	11942 KB
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt1.pdf	89	Non Patent Literature	10251 KB
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt3.pdf	111	Non Patent Literature	14845 KB
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt2.pdf	96	Non Patent Literature	11963 KB
Ex_1019_JEDEC_Standard_DDR3_SDRAM.pdf	211	Non Patent Literature	10928 KB
NL070-14US03_IDS_Transmittal_2023-05-12.pdf	4	Transmittal Letter	120 KB

NL070-14US03_IDS_List_2023-05-12.pdf	5	Information Disclosure Statement (IDS) Form (SB08)	250 KB

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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
IPR2022-01428_Prelim_Sur-Reply.pdf	79EBAC2817EBD831045F9ED49BBEAB8B347566CD389115EA32DE3C692C66993D2560DB196672232705D22310321547E9D7F862B129912F4BC59E1B7DF4B453A0
IPR2022-01428_Reply_POPR.pdf	7FA984F9C5EFE3834F102FADFFF167FD3A4C35BB4309624EC8AD78814844DC4B6BA2D3272D2546CED4EBC56248BEF97AAE6676A238AD88516AAD83301E47D311
IPR2022-01427_Prelim_Sur-Reply.pdf	3E82BC7E0A431371B8A7A106469F3A815242077E54E81B123BF4BCA7735CB16F071288F40C10D84831B8F75CE82AA8681121A498BADEE19A0CC634CD0F3C71A3
IPR2022-01427_Reply_POPR.pdf	016D7C0794A9FC0EBF7CD38967C458AA0C3E289D144C5DA95201FC65F2B33E309B00D2DC2FB16BB5CFEB8EC7C86CC46A99777D2484820E3FF5BF5D739DB0603A
IPR2022-01428_Institution_Decision.pdf	F66F979F562BF56286C357ADBEFE3978C7D0259B6FA89AB871B9773F0A2C4E824AEFD7FB7D8AA223D37B1D710944A001024898C71A6778730BEE16A08FCC4FE7
IPR2022-01427_Institution_Decision.pdf	5AD606F591A6CCB10AC2C81D3E04AFCD0E495E4F8A62CB3D47CD8F11C0EEE871EE444D5FC91B8026885C3A22C0B56653048FBB513AE357C2310125E23A9609BF
IPR2022-01428_POPR.pdf	E2C79935D334ECFFBC84F0E00B3B9C985F685108B31F7B32AA3D895F4D563B308C005A0942153001EFC7FC03263E3771F8FA456CF8A91E18EA46417E4A633A5E

IPR2022-01427_POPR.pdf	A4785AB78155199F954EAEF571ACA80D0BF06440E6C92FC8299FF0224C74311218ABA8B867C3F89AC90DE6E3DEB98D0F6AEBA4CD2D74D5C60FEA1CBC3A6647D1
IPR2017-00668_FWD.pdf	B3DF4ACC1A8412C36DEC31BC28CB847A4ED54E6A3D35D73DFB815A26FE2757F9280A8D9C43D687737BD9CFFF38A57F744FEDB97BE0C3ABC6F6452491D2A6BBBD
IPR2017-00667_FWD.pdf	F89DD1BF27AEADB5CE718BD4A910D41820E49EE8974CD7317B79F5C28AE628824436093A3D2179806CE4C91D636EC50AB893FF0020ECCD85D8F6477ED79EC4D3
IPR2018-00362_FWD.pdf	39814EB08154EDEC4A9EE82DD94109A065C4AF7E2AC7340DF2980C215E63AA50C29A56DE59A9F973BA7DD0B06CA891724FE38E583F9E4FBB6E4B62A1C2231567
IPR2022-01427_Petition.pdf	0CC0F8147F8DF0C7259EC686C3195F8E1E48D0B30F05A299B84851F50D377EDDF07DB25F9930928D3E39E755FEE3DAB519F307C8DEB2AD9D91AC4CB54295E59A
Exh1035_GDDR4_SGRAM.pdf	78129798694A10EC679325D7DDA71B94383D03D3365A637DE09DF4279898D1AFF95EAE751BC6C9F2B2C19F0993132D0ABC7C4D836D99843BDA1F6D522DFF6E1C
Exh1030_Digital_Logic_Book.pdf	79DECCAB4E9C2A01A2833987F6E620988B5DDBC50F465B472D5804E016C620365C92F59A7211265DCB45C9B3DBAFE93419526A0D524D28B00E268CA0C186ACF9
Exh1023_Jacob_Paper.pdf	14F6FBDF4735B096439A8D62D45D8075DCB02BBEF8CE86F13E3C5E76AC519186135C34C1348754DA52781191214 8B2D6DD1D3F439B9D6600019B08A7D12A56E5
Ex_2020_Sams_Oppo_N_MPSJ_Sams_Invalidity_Defenses.pdf	78FC9E92CD65C75420077C542B9A860432A41CD4FF1281FCB754E0F151C1C3B6DF918896C5933501A50F1EEBAEB67D98FF1F8CC416B321A9E5A77719D7F4B65B
Ex_2019_N_MPSJ_Sams_Invalidity_Defenses.pdf	C1A65C894E715C00FB6CD598769A7B209738124C475A48322C00CB34AF4F20D289A433B74101523BA91972CF6A5206E40208BA55FACF00347A3864CEBA606BE3

Ex_2013_Sams_4th_Amended_Initial_and_Addtl_Disclosures.pdf	8F2501D4D642DF7F3E41B156A9271928C2C69671871105BC52E89E58B6653F3AA2F89460631CF4E4A4658A1762E917D57DFB1C4EF1BFB9C6C39C2D8BEEA10F34
IPR2022-01428_Petition.pdf	521DD00C297B5E58F6E9E58B510EF4EF6D31C547E22F074BA3C87E241B151B0F0AA0E3075F398F23F7748B9091EC293832098DDD92F8513E102629F292109AD9
Ex_2009_Sungjoo_Park_Depo-REDACTED.pdf	9EAED2B6B39C19DB9B44F1300EF0D13AC9FCEDBC6FB440273DCD175B09266F83968A224EB51B3CECCEAD2102AFA73B342E46CD01ADEEC75E9C23D34A9BE61D4C
Ex_2017_JEDEC_Standard_21-C.pdf	5EE5E3DE3814D9DF3B6FD3DDB00CD9F4ED6EFBEA23CDCE37FC040737C24C1E479D07188F7A29F636757F5E3CB843512EB4360A7D2AD8F21421693316C2061D2D
Ex_2006_Sams_Resp_N_Objs_CC_Memo_Ord.pdf	A6E5763DE5FD3B59F81267CD286E43235B7CC669A335238D50C08B4CA7C7B1816A32B9AF9B605AEC1E4E835691147D30B64ECB557716DEC3E398E440334F3047
Ex_2008_N_Oppo_Sams_MSJ_Non-Infringement_Patents.pdf	AEF50E04D8EE5AEA812EEF18A7FD1D9F65C3D473082E3A96DAABD4A1845C2590C001A55F9560A1A3D690D7573E3106CB046AE2D947F5CFFEFE59DB26698EEA46
Ex_2005_N_Objs_Memo_Opinion_and_Order_re_CC.pdf	898C611369E86A3A48A0C13A8DB0B9210C2CF7B8486B465E6625E1A036A1E19FEFCFFEE871D70A2AB96C1F6093F46C1036470C76FC30FB255B22D5E37424331A
Ex_2007_Stacked_DRAM_Spiral_TSV_Structure.pdf	E01AC4738F0588E00221473AC5002835CF5427C464EF809AA300DBDC24E5699A4A64D7B68BCC0EF8D7624E3ACEE9B30AC98FFDAE4B6CFD54E058D054B9D07DBC
Ex_2003_Sams_Responsive_CC_Brief.pdf	EF223128B2834B4B78A90091E74A3D679F6D75FC6BA04C74809C1A326A481F5E780B1DE6CC6632CE4CCB28E014342D6BCFBF06CEEB29E3359ABA1E579BDB788A
IPR2022-01428_Ex_1003_Decl_Andrew_Wolfe.pdf	B18BD6D28F9ED74E99FB0709298EED1D40E62F4B9DF7285D9EAA33D0C97261D5AD36905D10930243A5D4D0D7A4FBA65E286A43793A617A163FDAB5E9336D69E6

Ex_2001_Sams_Prelim_CC_and_Extrinsic_Evid.pdf	E1543E24EFEABC6FA526A45E6336BD2DB1E6A772EE25B1A475C5D5BF0BC43835A3231FCC2FA2AD2136F844C13549D49354B6D98B18344C8C9F08FE6078B80774
Ex_2002_Sams_Constructions.pdf	C124C2F79CCE48B1D05771BF3A7FE5F9439299FB51732CE3E5EB0A88780E2C2EC9ABFE4EBBF714DC3C4CD123896D7B045C00CB7866D5D972C1DA8D384435F7B7
Ex_2004_CC_Order.pdf	546690DC6E6271F097778E0CE17C0CEE7A85F922582EFCB3403283A9FD6802CCB65CBA97C53820D5209398BA74843DA3948B218B4418585D552818D53FB48CBB
IPR2022-01427_Ex1003_Wolfe_Declaration.pdf	39BC58DE7B82F0669D50DB9EC8806ED46512B9D9FF5B06BEE6C548B2F385F94DE9ADB04F7D64587973852A330238A5A68F4DB2EFF1F61FD91F35D52198D853CA
Ex_1045_Sams_Answer_FAC.pdf	61DDD83A28C28D055D743429855A95F961C2AB540BB4047E0D5DA2B3E4FA7E8564C7D8F126805BAB5E684DD606FD1D84123F2CF98599FF9EA248D2933A8600AE
Ex_1049_Sams_MSJ_Noninfringment.pdf	B12F9C428F851F7C729C4A7D1DFE63859A975FA456AD1DDF2FB0418758BABDEE5419CAAED3884AFC7042BB783202F2FEF7CB40E739B39BBA2A1AC83FA05DB002
Ex_1029_386_Reexam_Decision.pdf	16561327EEB35C8EBF4374B037D53326740A27B029FB6A88AE1E890F17831BD4E8037C6EF5C15909C05534555B66CF5004BFDB9EC3D8D7808304A5C805CFBBE3
Ex_1043_Netlist_v_Samsung_Complaint.pdf	105FBBFAC890EADBED86702DC47C7C9B86068D29E02819A728C01872CD7A8DE9351941027FF3E46FA4D2F115A1FD2469257EB8EAE917312B7AD11589C2C53ADA
Ex_1038_Microcomputer_Interfacing_pt2.pdf	B77C7E811964DCC68437683326B77878F5C0A7C10E6015C7154E34B6D0076DC3F322070DC8692126BFBCB241D415B3A9BFAC9A652074E9D59D28E7C05FB4E832
Ex_1021_JEDEC_MO-207.pdf	C67820B3EA7F7D72F1BC97B28D8E6815BCB1CE18E987C9C93370FE6C9E74133799421DA638C9F3AEE16AEEAC0A6BF57859113FAB105335BF70C412D95A813ABA

Ex_1038_Microcomputer_Interfacing_pt1.pdf	505A2B7A0713375DD32591EA6267C41117C6A14B7ECBF4B7C52AD524255BDABDCF1E302C5936C2DA5935661F67FA4365E5A7ACA04434284CBFF2C09D01CF75AA
Ex_1020_Decl_Julie_Carlson.pdf	C1140AFB4BC0970453570BFEC8683207F5B062A434CC171071AA630096D5C1EFF5E55A9AFA0F05B2CC6A5ABEF38D9FB1EAB2CD443F5A481DFC6CB75567CEBE2B
Ex_1038_Microcomputer_Interfacing_pt3.pdf	80B6988E1D27E61B45FA632D856F2BEA4F1241C9935256FDBCBB71907BA89F122AFE5CDC0D3C2BD9C98583AFA3E098D02AEFD554430184E75FF0C6CF7600888F
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt1.pdf	B496E94DD6420DCA7E246BDAA6F7C5E64305A5A75C5394B070CE889F0EF3055C7412C344C5A8CFCEFB2792EA039B6E006DBF63F1F3DC5EEFEBAFA61779713997
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt3.pdf	DCD03216588A1FA0AEEA358CE531663E8F93AD1704C1E8DF735E39ABDB509286BF2A14F95C66F8EAF48020737907024DC74F4C411197B101A00631B950A786E7
Ex_1022_Memory_Systems_Cache_DRAM_Disk_pt2.pdf	FE4B57B04D2A59295BA84ABD0DBD9CF7BD4974E6D4D69BEA8E5E09F9B80D98FC2B8D82A6E38D2D4B609FE72E53F95F76AED6FB902E99BF8831AB3A76A5F2947C
Ex_1019_JEDEC_Standard_DDR3_SDRAM.pdf	1A188F99A261A251091C2F7FB4EEAA07CB93C846EAB1DA1F15445BB64B8E963EC3F5F661A7C51CC790B00AD0116F1883A646A038568C5C549A416C33D177AA72
NL070-14US03_IDS_Transmittal_2023-05-12.pdf	C19F9CCD557E378BD2FC624F9D538A1C5F19FFC36059891435B7EE3443C4829828BE530D4F1F2B52B59EB12A040BFB7E2A4AA58D2F35BBFA38A0074AD55CF969
NL070-14US03_IDS_List_2023-05-12.pdf	64FCEC782F12A140BAB3DFB70FCF2D02889A7510BAE7B417B88F245138AE1190F2D1C13D5ED19388A778A9B6BFA80FE2630ECAD10F533E28E32338DFD8B41DEE

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	05/12/2023 11:12:32 PM ET	NL070-14US03

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	62085915	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	03/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2819	E20235BN13155104	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	$260.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Notice of References Cited	Application/Control No. 17/694,649	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20110211411-A1	09-2011	Ide; Akira	G11C11/4076	365/219
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	09/28/2022	HH
Above Updated	07/07/2023	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/28/2022	HH
Above	Updated	07/07/2023	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
PE2E Search	09/28/2022	HH
Assignee and Inventor search	09/28/2022	HH
PE2E Search	07/07/2023	HH
IPR2022-01427 Reviewed Inter Partes Review of U.S. Patent No. 9,318,160 on 07/05/23	07/05/2023	HH
IPR2022-01428 Reviewed Inter Partes Review of U.S. Patent No. 8,787,060 on 07/06/23	07/06/2023	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/28/2022	07/07/2023							
	1	✓	✓							
	2	✓	✓							
	3		✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							
	12		✓							
	13		✓							
	14		✓							
	15		✓							
	16		✓							
	17		✓							
	18		✓							
	19		✓							
	20		✓							

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	65753	(G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:01 AM
L2	922	1 AND (dynamic ADJ ram dynamic ADJ random dram) WITH stack$3 WITH (die dice ic integrated ADJ circuit chip)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:09 AM
L3	557	2 AND (command near3 address command/address)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:10 AM
L4	407	3 AND data WITH (terminal node pad pin)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:12 AM
L5	255	4 AND (tsv through ADJ silicon ADJ via)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:13 AM
L6	106	4 AND (tsv through ADJ silicon ADJ via) WITH address$3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:13 AM
L7	106	6 AND (data bit) WITH (through ADJ silicon ADJ via tsv)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD,	OR	ON	ON	2023/07/06 08:14 AM

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			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	65	7 AND driv$3 WITH data	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 08:15 AM
L9	3	"8717828".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 10:54 AM
L10	2	"8787060".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 03:23 PM
L11	4	"20110103156".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 03:57 PM
L12	13964	(memory storage) AND (dynamic ADJ ram dynamic ADJ random dram) WITH stack$3 WITH (die dice ic integrated ADJ circuit chip)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:41 AM
L13	418	12 AND control$4 WITH (terminal pad node pin) WITH command WITH address$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:42 AM
L15	273	13 AND (data bit) WITH (terminal pad node pin) WITH output$4	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2023/07/07 10:45 AM

			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L16	70	15 AND (through ADJ silicon ADJ via tsv) WITH command WITH address$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:45 AM
L17	5	16 AND driv$3 WITH (size different greater smaller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:47 AM
L18	42	16 AND driv$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:48 AM
L19	30	16 AND driv$3 WITH (die chip ic integrated ADJ circuit)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:49 AM
L20	0	16 AND interconnect$4 WITH chip ADJ (select$3 enabl$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:56 AM
L21	9	15 AND interconnect$4 WITH chip ADJ (select$3 enabl$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 10:57 AM
L22	70	16 AND (set group subset plurality) WITH (die dice ic integrated	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2023/07/07 10:59 AM

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		ADJ circuit chip)	DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L23	41	16 AND (second another different) adj3 (set group subset plurality) WITH (die dice ic integrated ADJ circuit chip)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:00 AM
L24	2	16 AND (set subset group plurality) adj4 (through ADJ silicon ADJ via tsv) WITH command WITH address$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:04 AM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	5	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		6,553,450	2003-04-22	Jim M. Dodd	
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		8,325,539	2012-12-04	Hwan-Wook Park	

Examiner Signature		Date Considered	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	2	of	5	Attorney Docket Number	NL070-14US03

		8,369,122	2013-02-05	Sang Jin Byeon	
		8,400,781	2013-03-19	Peter B. Gillingham	
		8,411,478	2013-04-02	Tae Sik Yun	
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		8,949,538	2015-02-03	Joe M. Jeddeloh	
		9,160,349	2015-10-13	Yantao Ma	
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		20100195364	2010-08-05	Yoshiro Riho	
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		20110103156	2011-05-05	Jae Il Kim	
		20110193226	2011-08-11	Kyle K. Kirby	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Petition for Inter Partes Review of U.S. Patent No. 8,787,060, filed August 26, 2022.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Patent Owner Prelminary Response, filed January 19, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Petitioner's Authorized Reply to POPR, filed February 17, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, PO's Preliminary Sur-Reply, filed March 1, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Institution Decision: Granting Institution of Inter Partes Review 35 U.S.C. sec. 314, filed April 12, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petition for Inter Partes Review of U.S. Patent No. 9,318,160, filed August 26, 2022.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Patent Owner Prelminary Response, filed January 19, 2023.

Examiner Signature		Date Considered	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	3	of	5	Attorney Docket Number	NL070-14US03

		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petitioner's Authorized Reply to POPR, filed February 17, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Patent Owner's Preliminary Sur-Reply, filed March 1, 2023.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Institution Decision: Granting Institution of Inter Partes Review 35 U.S.C. sec. 314, filed April 12, 2023.
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Exhibit 1003, 'Wolfe declaration,' filed August 26, 2022.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Exhibit 1003, 'Wolfe declaration,' filed August 26, 2022.
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, EX2009, 'Park, Sung Joo Deposition Transcript (2022.11.23),' filed January 19, 2023
		IPR2018-00362, US Patent 9,606,907, Final Written Decision, entered: June 27, 2019, 94 pgs.
		IPR2017-00667, US Patent 7,532,537 B2, Final Written Decision 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, entered July 18, 2018, 44 pgs.
		IPR2017-00668, US Patent 7,532,537 B2, Final Written Decision 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, entered July 18, 2018, 46 pgs.
		USPTO Patent Trial and Appeal Board, Appeal 2014-007777, Inter Partes Reexamination Control 95/000,546 & 95/000,577, US Patent 7,289,386, DECISION ON APPEAL, issued 2015-02-25, 25 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'SAMSUNG'S MOTION FOR SUMMARY JUDGMENT,' filed 2023-02-10, 19 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Defendants' P.R. 4-2(A) Preliminary Claim Construction and Extrinsic Evidence,' 2022-08-05, 55 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, "Samsung Defendants' Proposed Constructions of Disputed Claim Terms and Supporting Evidence," filed on August 19, 2022, 69 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, "Defendants' Responsive Claim Construction Brief," filed 2022-09-16, 38 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'CLAIM CONSTRUCTION ORDER,' filed 2022-12-14, 35 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, " Plaintiff Netlist Inc.'s objections to the magistrate judge's memorandum opinion and order regarding claim construction," filed on 2022-12-28, 23 pgs.

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
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				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	4	of	5	Attorney Docket Number	NL070-14US03

		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, " Defendants' Response to Netlist's Objections to Claim Construction Memorandum Order," filed on 2023-01-11, 11 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, "Plaintiff Netlist Inc.'s Opposition to Samsung's Motion for Summary Judgment of Non-Infringement," filed 2023-02-23, 23 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, "Samsung's Fourth Amended Initial and Additional Disclosures," filed 2022-12-06, 23 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Netlist Inc.'s Motion for Partial Summary Judgment on Samsung's Invalidity Defenses,' filed on 2023-02-09, 22 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'Samsung's Opposition to Netlist's Motion for Partial Summary Judgment on Samsung's Invalidity Defenses,' filed on 2023-02-22, 29 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'COMPLAINT' filed 2021-12-20, 49 pgs.
		USDC, ED Texas, Netlist Inc. v. Samsung Electronics Co., Ltd., Civil Action No. 2:21-CV-463-JRG, 'THE SAMSUNG DEFENDANTS' ANSWERTO FIRST AMENDED COMPLAINT,' filed 2022-05-18, 53 pgs.
		JEDEC Standard No. 21-C, GDDR4 Specific SGRAM Functions, Page 3.11.5.8, From JEDEC Board Ballot JCB-06-007, Formulated Under the Cognizance of the JC42.3 Sub-Committee on DRAM Parametrics, Release1.0, November 2005.
		JEDEC Standard No. 21-C, "PC2100 and PC1600 DDR SDRAM Registered DIMM," Revision 1.3, January 2002.
		JEDEC Standard No. 79-3C, DDR3 SDRAM, JESD79-3C, Revision of JESD79-3B, April 2008.
		JEDEC Standard No. MO-207, " Square & Rectangular Die-Size, Ball Grid Array Family," JEDEC Solid State Product Outline, December 10, 22 pgs.
		Declaration of Julie Carlson re JEDEC Standard No. 79-3C, DDR3 SDRAM, JESD79-3C (Revision of JESD79-3B, April 2008), dated 2021-09-16, 7 pgs.
		Cho et al., "A 1.2V 64Gb 341GB/s HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and Improved Bank Group Data Control," IEEE International Solid-State Circuits Conference, ISSCC 2018 / SESSION 12 / DRAM / 12.3, Article No. 978-1-5090-4940-0/18, 2018, 3pgs.
		Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, 296 pgs. (uploaded in three parts).
		Bruce L. Jacob, " Synchronous DRAM Architectures, Organizations, and Alternative Technologies", Electrical & Computer Engineering Dept., University of Maryland, MD 20742, December 10, 2002, URL: http://www.ece.umd.edu/~blj/.

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 12, 2023	
				Application Number	17/694,649
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				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	5	of	5	Attorney Docket Number	NL070-14US03

		Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design," 2nd Edition, Chapter 3, Department of Electrical and Computer Engineering University of Toronto, 2008, McGraw-Hill Companies, Inc. 10 pgs.
		HAROLD S. STONE, "Microcomputer Interfacing," University of Massachusetts, Amherst, 1982, Addison-Wesley Publishing Company, Inc. 399 pgs. (uploaded in three parts).

Examiner Signature	/HUAN HOANG/	Date Considered	07/07/2023

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 07/12/2023

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Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
07/12/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 201

Office Action Summary	Application No. 17/694,649	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 05 April 2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

The Amendment filed on 04/05/2023 has been received and entered.

Claim Objections

2. Claims 2 and 9-11 are objected to because of the following informalities:

The limitation "the plurality of DRAM array die" in claim 2, lines 13-14 should be "the plurality of DRAM array dies". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

The recitations of "each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies" (claim 1, lines 9-10), "each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies" (claim 1, lines 15-17) and "each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die" (claim 1, lines 21-25) are not disclosed in the specification and are nor shown in any of the drawings.

According to paragraph {0029], lines 4-5, a single die interconnect corresponds to a TSV and the drawings shows any interconnect corresponds to only a TSV, not a plurality of TSVs.

Claims 2 and 12 recite similar limitations and are also rejected for the same reasons.

5. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 9 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

Claim 9 recites the limitation "the drivers" in line 1. There is insufficient antecedent basis for this limitation in the claim. The limitation “the drivers” is unclear to relate back to “a first driver” (claim 2, lines 14 and 15) and “a second driver” (claim 2, line 22) and may be different drivers from the first driver and the second driver.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571) 272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Electronically filed September 12, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Final Office Action dated July 12, 2023, for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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Ex. 1002, p. 207

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM array dies including at least a first plurality of DRAM array dies and a second plurality of DRAM array dies;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the stacked DRAM array dies;

first data interconnects electrically coupled to data ports on the first plurality of DRAM array dies and electrically isolated from data ports on any of the second plurality of DRAM array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies;

second data interconnects electrically coupled to data ports on the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die; and

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals being driven by a respective first driver having a first driver size, a respective signal of the second

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data signals being driven by a respective second driver having a second driver size different from the first driver size.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked DRAM array dies, the stacked DRAM array dies including a first plurality of DRAM array dies and a second plurality of DRAM array dies, the DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a command/address signal to one or more DRAM array dies in the stacked DRAM array dies,

driving first data signals received at respective data terminals to the first plurality of DRAM array [[die]] dies via respective first data interconnects, including enabling a first driver having a first driver size to drive a first data signal to the first plurality of DRAM array dies via a first data interconnect, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies; and

driving second data signals received at respective data terminals to the second plurality of DRAM array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a second data signal to the second plurality of DRAM array dies via a second data interconnect, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die, the second driver size being different from the first driver size;

wherein the first data interconnects are electrically coupled to data ports on the first plurality of DRAM array dies and electrically isolated from data ports on any of the second plurality of DRAM array dies, and wherein the second data interconnects are electrically coupled to circuitry on the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies.

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3. (Previously Presented) The DRAM package of claim 1, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

4. (Previously Presented) The DRAM package of claim 1, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

5. (Previously Presented) The DRAM package of claim 1, wherein:

each of the second plurality of DRAM array dies is stacked over at least one of the first plurality of DRAM array dies; and

the second driver size is greater than the first driver size.

6. (Previously Presented) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of DRAM array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of DRAM array dies and one of the second data interconnects.

7. (Previously Presented) The DRAM package of claim 1, wherein:

the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;

the plurality of chip select interconnects respectively coupled to the first plurality of DRAM array dies; and

the plurality of chip select signals are configured to select one array die among the first plurality of DRAM array dies to receive data in the first data signals.

8. (Previously Presented) The DRAM package of claim 7, further comprising a control die between the stacked DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

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9. (Currently Amended) The method of claim 2, wherein each of the ~~drivers~~ first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (Currently Amended) The method of claim 2, wherein each of the ~~drivers~~ first driver and the second driver includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (Previously Presented) The method of claim 2, wherein the control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of DRAM array dies, the method further comprising:

driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects, to select one array die among the first plurality of DRAM array dies to receive the first data signals.

12. (Previously Presented) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM array dies;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the plurality of stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the plurality of stacked DRAM array dies, the control interconnects including a plurality of chip select interconnects; and

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data interconnects, wherein:

each of the data interconnects is electrically coupled to data ports on a subset of the plurality of stacked DRAM array dies and is electrically isolated from data ports on any other array die not in the subset of the plurality of stacked DRAM array dies;

the data interconnects include first data interconnects electrically coupled to a first subset of DRAM array dies in the plurality of stacked DRAM array dies, the first subset of DRAM array dies including a first plurality of DRAM array dies;

each respective array die of the first plurality of DRAM array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of DRAM array dies and at least one second TSV in at least one second array die not in the first subset of DRAM array dies;

a respective TSV in the first subset of TSVs is coupled to a corresponding data port on a respective array die in the first subset of DRAM array dies; and

the at least one second TSV is electrical isolated from any data port on the at least one second array die.

13. (Previously Presented) The DRAM package of claim 12, wherein each of the plurality of stacked DRAM array dies includes a DRAM integrated circuit (IC) chip, the DRAM IC chip including a number of memory cells.

14. (Previously Presented) The DRAM package of claim 13, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is electrically isolated from memory cells on the corresponding array die.

15. (Previously Presented) The DRAM package of claim 14, wherein each of the at least one second TSV includes a conducting material in a corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

16. (Previously Presented) The DRAM package of claim 14, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is connected to a

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stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (Previously Presented) The DRAM package of claim 13, further comprising a control die between the stack of DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

18. (Previously Presented) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects electrically coupled to a second subset of DRAM array dies in the plurality of stacked DRAM array dies, the second subset of DRAM array dies including a second plurality of DRAM array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals being driven by a respective first driver having a first driver size, a respective signal of the second data signals being driven by a respective second driver having a second driver size different from the first driver size.

19. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

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REMARKS

This amendment responds to the Final Office Action dated July 12, 2022. In the office action, the Examiner:

- objected to claims 2 and 9-11 because of informalities;
- rejected claims 1-20 under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement; and
- rejected claim 9 under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor regards as the invention.

REMARKS CONCERNING CLAIMS

Claims 2 and 9-10 have been amended.

No new matter has been added and the amendments should not necessitate additional search or examination.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 1-20.

REMARKS CONCERNING CLAIM OBJECTIONS

Claims 2 and 9-11 are objected to because of an informality in claim 2. Claim 2 has been amended to address the informality. Withdrawal of the objections to claims 2 and 9-11 is therefore respectfully requested.

REMARKS CONCERNING CLAIM REJECTIONS

In rejecting claims 1-20 under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, the Office Action states, on page 3: "According to paragraph [0029], lines 4-5, a

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single die interconnect corresponds to a TSV and the drawings shows any interconnect corresponds to only a TSV, not a plurality of TSVs." Applicant respectfully disagrees.

The specification in paragraph [0029], lines 4-5, simply states: "Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins." Thus, while these lines in the specification state that multiple die interconnects may include multiple TSVs, they do not specify that a single die interconnect corresponds to a TSV. The drawings also do not show that an interconnect corresponds to only a TSV.

On the contrary, the specification and drawings are clear that an interconnect can include a plurality of TSVs. For example, as described in paragraph [0040], lines 6-10 (emphasis added):

> "the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, ***die interconnect 220a*** may be connected with data ports of the array dies 210a and 210b using ***vias*** (*illustrated by the filled or darkened circles*)." As shown in FIG. 2, the ***die interconnect 220a include two vias*** illustrated by the ***two*** filled or darkened circles in array dies 210a and 210b. Thus, the die interconnect 220a includes two TSVs, one TSV through array die 210a and another TSV through array die 210b.

Further, the specification in paragraph [0041], lines 3-9, provides (emphasis added):

> "For instance, ***die interconnect*** 220b may pass through array dies 210a and 210b using ***TSVs*** that do not enable electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). . . However, the ***die interconnect*** 220b may be connected with at least one data port of ***each*** of the array dies 210c and 210d using ***a via*** (*illustrated by the filled or darkened circles*)."

This is in line with paragraph [0031], lines 9-11, stating (emphasis added):

> "the ***die interconnect*** 220b may pass through the array dies 210a and 210b (*as illustrated by the unfilled circles*) e.g., through ***through-holes or vias*** of array dies 210a and 210b."

Also, the specification describes, in paragraph [0051], lines 5-8:

> "As a second example, the driver 334b of the conduit 332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c

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> and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b. . ."

This is illustrated in FIG. 3, where the die interconnect 320b is shown as including two TSVs (illustrated by the unfilled circles) in dies 310a and 310b and two TSVs (illustrated by the dark and filled circles) in dies 310c and 310d. The specification further provides, in paragraph [0051], lines 3-5 (emphasis added):

> "Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits ***configured to provide a command or address signal, a chip select signal,*** a supply voltage signal, or a ground voltage signal to one or more die interconnects. "

Therefore, the specification and drawings provide sufficient support that a die interconnect can include a plurality of TSVs, one for each die, which the die interconnect either connects with or passes through. In other words, the below-quoted claim elements meet the written description requirement under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph:

> "each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the stacked DRAM array dies;"
> "each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies;" and
> "each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies"

Therefore, claims 1-20 reciting the above limitations or limitations similar to the above are patentable under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph.

Claim 9 was rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite because the recitation of "the drivers" lack antecedent basis. Claim 9 has been amended to address the antecedent basis issues.

Withdrawal of the claim rejections is therefore respectfully requested.

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CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 12, 2023

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**09/12/2023 11:44:57 PM ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	62785271	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 4

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_Amendment_FOA.pdf		11	-	179 KB
NL070-14US03_Amendment_FOA-A.NE.pdf	(1-1)	1	Response After Final Action	110 KB
NL070-14US03_Amendment_FOA-CLM.pdf	(2-7)	6	Claims	106 KB
NL070-14US03_Amendment_FOA-REM.pdf	(8-11)	4	Applicant Arguments/Remarks Made in an Amendment	133 KB

NL070-14US03_USPTO_SB434.pdf	2	After Final Consideration Program Request	258 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL070-14US03_Amendment_FOA.pdf	23F12BFE81E3E44672D0DCA5A189443E94CD784645189EC6B8E5DC87A7E1569B61A32E7532D09E4DA4D81123A8775E16B561294B806CC3F887A89074EFC0541C
NL070-14US03_Amendment_FOA-A.NE.pdf	1447DF14C391AD5BBC0EBA0E3EC90EC7CED63CA0BEBB61452F1A1AFAFD7975A4DA3F687DBBB2F389E220EE2D7ACB44201BE3FA3BE312DF75B2474438959340DD
NL070-14US03_Amendment_FOA-CLM.pdf	0AC653502E06D35381B56D212F00010C91650906B08C08399C5003B83E4B7C8BD240FC91F956C57FAEF4AD32A75756D3D9B1A092A0B804EA7911C8FB6EE8182F
NL070-14US03_Amendment_FOA-REM.pdf	B64912F7B8BD2116F255F5365B168B11A4B94C738C2A41E20D914A76CE3E4A881164324B09766C122B348B58099DE7D21FF77E7FA8365960A0B43E4466BCC3C8
NL070-14US03_USPTO_SB434.pdf	CDE13740205C03D57131998AEEE82272433CA5CA67A9E756E3B8281E26C34B1DB8CC02A20E526AFED263869FF830A8DD61E9E4474EC8EEECB8751EE11CBE8A60

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Program Request

PTO/SB/434 (3-22)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
NL070-14US03	17/694,649	2022-03-14
First Named Inventor:	**Title:**	
Hyun LEE	MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the USPTO's patent electronic filing system.
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
    - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
    - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
        - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
        - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
            - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
            - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date	Practitioner Registration No.
/Jamie J. Zheng/	2023-09-12	51167
Name (Print/Typed)	**Telephone Number**	
Jamie J. Zheng	650-521-4828	

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**09/17/2023 10:32:59 PM ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	62810866	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 38

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_IDS_Transmittal_2023-09-17.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	120 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
IPR2022-01427_POR.pdf	95	Non Patent Literature	4777 KB
IPR2022-01428_POR.pdf	96	Non Patent Literature	4747 KB
IPR2022-01428_Ex2023.pdf	216	Non Patent Literature	3818 KB
IPR2022-01427_Ex2023.pdf	216	Non Patent Literature	10379 KB

IPR2022-01427_Obj_PO_Evidence.pdf	31	Non Patent Literature	230 KB
Ex2028.pdf	4	Non Patent Literature	45 KB
Ex2027.pdf	24	Non Patent Literature	98 KB
Ex2029.pdf	13	Non Patent Literature	140 KB
Ex2024.pdf	266	Non Patent Literature	816 KB
Ex2025.pdf	245	Non Patent Literature	879 KB
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Ex2045.pdf	16	Non Patent Literature	366 KB
Ex2046.pdf	2	Non Patent Literature	677 KB
Ex2039.pdf	6	Non Patent Literature	5134 KB
Ex2040.pdf	3	Non Patent Literature	3378 KB
Ex2036-part1.pdf	10	Non Patent Literature	6231 KB
Ex2036-part2.pdf	9	Non Patent Literature	8480 KB

Ex2050.pdf	11	Non Patent Literature	268 KB
Ex2048.pdf	11	Non Patent Literature	3693 KB
Ex2052.pdf	2	Non Patent Literature	419 KB
Ex2053.pdf	27	Non Patent Literature	98 KB
Ex2047-part2.pdf	450	Non Patent Literature	5871 KB
Ex2051.pdf	11	Non Patent Literature	3106 KB
Ex2100.pdf	1	Non Patent Literature	160 KB
Ex2049-part1.pdf	484	Non Patent Literature	6799 KB
Ex2054.pdf	29	Non Patent Literature	3264 KB
Ex2049-part2.pdf	485	Non Patent Literature	6936 KB
Ex2055.pdf	4	Non Patent Literature	2213 KB
Ex2101.pdf	3	Non Patent Literature	1627 KB
Ex2047-part1.pdf	417	Non Patent Literature	10682 KB
NL070-14US03_IDS_List_2023-09-17.pdf	3	Information Disclosure Statement (IDS) Form (SB08)	203 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)

NL070-14US03_IDS_Transmittal_2023-09-17.pdf	8D797B2805722A044D269A61775D9BB17F1AA06D6C9A1CF32CE389E95DCE1F0C633DB979C051F1BCD7076FE8B6A7069E6E4CF6EF21DB211A5A2D4DD889A0D331
IPR2022-01427_POR.pdf	9515AB927CD1D8A8496231390DE59F5F945514FE38CE621BA352949974F6D5A71D4889DCDE3A5E26A1B7CE2957564396147235F2AF46421C2BF5AD0B0717F466
IPR2022-01428_POR.pdf	61BC56998E7DCA58D5488D6AEABF0F9406BC7FDB2331EB16103AE5DFB66FD4B680E5028D69F0E97765B56BC5320B6ABD7D71889F695C8ECE00C310FF6B839D2C
IPR2022-01428_Ex2023.pdf	AD77D5AD8E819DBE4B671B950A980E79C2F767085A2B346446DD7AA77D438190DF7AE72EA3B8832223BBCD50C7134BBDFA1D9DC3C66DD54E5628129A078D356C
IPR2022-01427_Ex2023.pdf	ACA26964398E5BE218DAE12A2CBDF59E9EDE42CF3A421A0038ED1E2B45169C302FEEDD6811050341D1ECB9663C8354D661A9DD8EBC4A0F28FB2BE8005AD4EBA6
IPR2022-01427_Obj_PO_Evidence.pdf	92E8FFA44C7133BE93FBFF189DB50D50911322A48BBB36E5121612E896F5D882375EB83CD12F58ECB9995DC0B22657622111A2703E1985F01CBC62FAEF87AA60
Ex2028.pdf	95ADD2F00640E4216A437CCC1525EC8D681E0EECC259137DD2165FCB15402B435106812B6CAB1C74661EF0CA0084139D4DEAF522382B6DDD812D844A45E25F89
Ex2027.pdf	468F6BE3F20F68AF2296D8432B154F9E46A6CCC129E464A3F09CC582F106986BDA4694A5057DBCD8E9DEDF958C724667C73F65DEC081DD51D198C9DA1A7A88C7
Ex2029.pdf	3F1CE2ECF32F76B7622D8F0F5498CCD3EC0FDA2732664E639114CB2EC09B18F21EA1764E058C0287339D33353563E8AB6C2422AC631AE0AAFD573F9A8E534679
Ex2024.pdf	6D72F54F95171876895E4D7013DF0927F1D3AB0DE435CBACC5410E3C6698562EAFCBDCD0B26882534D0C7E9A4BA4E4606A6A8BDD504A92C72937766DC2E27CD9

Ex2025.pdf	5663523D952BBC9DF3D3DBF99493DBE70BC3A99F8A93DC92 E993DF02812C472BBC70661F448B18428ECDCDAD3F8F0A643 C45326F5210CC182FE9E2DF44FAC27C
Ex2030.pdf	007DCDAEB58EC2E1BD1C5889F9A65EBA23AFC59B26536B62 D0B2A2BBA669B9DD7A25F3213F7181DEA3D0E34A54A04E600 C34BF569415E96F856D69F1C14A9B24
Ex2032.pdf	F4A7EA4C172BD42431A9A5A5A7802AD91BEC397B47865FEBF AFB4A21501DDD0D0AAD61DCE8F5822FC3F44AA53FC0A9E18 62541E6B6BD05AAAD1B94435271FA9E
Ex2037.pdf	466597BD4663DC7F4DD4595C1204223EEB3685842C513B0E0 BD86DE9DC99E4B1277D1CFFE2BE6FF28931C2D8869AC2F1A A4C7FB7CA6162EE65D7DD2808853CCE
Ex2041.pdf	604C16B7553B6B0A213F83D4ECBA36DABC9C77193228D687C 55E6BF78279CFA40D3FA1B147044DBB22659947F4BE31725C1 943D4481774A353486725A6AC0296
Ex2043.pdf	D14887CD7CCC104CCDAC5EC491B1F7A4C7BFC1A3AF665C7 9962359EE4DE5450949C3945FBEE260176B184E44E3E6F9FD8 77C514D85F764615A5F0C5894C631F1
Ex2044.pdf	8BED12710A49CA1416EEFBE8656D81EA384F9B55E93BBB807 ECEAAABE960FA1DDBE6BD014B16A7F9B2B3163FACA2AFF6 443BC2FB6F5379A8FDECC3F8D8030112
Ex2031.pdf	D77086983A043698EC7FC7E5FF7D50906B3405376459A29CDB 0787AB4E63C7C495767BA831E585DFFCA65574DA0A254B214 00B22FB630262509FC9CE8FC2F4B0
Ex2045.pdf	1BC2DBA948AEE985E980352E0E402F3BA041421A63ADAF30F A56B574BCA42F4554455AE2450202ADCA244FBA9973B14B78 09D3EC9E7F67D945F8678FC5553817
Ex2046.pdf	20030D00F683E0FD11D091F95E9C345AC3B9BDB28ADFB7D99 3C4F672D123AEADA0D14C5F2052C2BE1E269605D4E6CED4C 161AD1EF919EBE5326286D124160E96

Ex2039.pdf	A55EC39FDC9666E2D3F358AAA626F969AA2660268742FFB8D 186418042053797050ADBACA31DD449CBB99D8737DB53BA7F 60E2364235421732B65B65C45240C6
Ex2040.pdf	D45AC0552CB251833CE379331D16C88AF9DA7830EB6CCF454 6E80B8300EBBD824E012DB414BA5638A1B8F835CA1C5816A3 AEC3BE9D7D05D20226526812A3FBC8
Ex2036-part1.pdf	C5D920A4D408FBE61773E2175CB5E4F1D1A29147BBEC38AB7 C4D124FC5B227F9DA51A2BAF3B43EB51A9D9DACB8CA9EDF BD091607B8BD898841CD4450557DDBB5
Ex2036-part2.pdf	E66B094C2BA115144D3EDFBFE74589B554CC32B9E5D4802B7 444D5586CFA7DC1058AF2640754405D5DBA4085F046840FA90 09DEFDFD3F9A6FA0CBBAD9E5FCF24
Ex2050.pdf	E2D3971A1676164437A05FD796CE2DFFCACC88DD121F94410 002223369B3C9F9CA48637312586D2F81AB7CB14AC85C87937 CACB82B200B1739ECC84B6456531C
Ex2048.pdf	6964D69F718E62B2385C0656569190C545F033303E3163E2B92 422D663C3DB714B7A98CCDB7459D5C181F04BAAF3CDEF54B EC330CF05A5DAFB3E33C0F16C4411
Ex2052.pdf	0A199717268BA4A9FA5A0259C311012B9B10A9D6882EE1FDA ABEE480D6A2A6525459744A21099EDFCB2CE7A470E4EB903A 664D96AF64D1295A4486FB7045A7E0
Ex2053.pdf	E4BD566468D6B79064B278C8C04675034E6ACF2677DAC8435 B75ABE783ECC4189CDDD46FAC44403D9F74F752BCB81D7F3 AD7FB8F6E36F36E7105F7365965600B
Ex2047-part2.pdf	2C1BAFC50999E9530BCFEC8E2BF1411A304E46187477A4945 E1954EB728B064B93F6A9596F34F4E416F555A073FAB311B82 FECE86FBAE54569D301B3EAE995F0
Ex2051.pdf	316D35C3675CE8BD1E6C7FFE0F748AA54EE17B753D946F890 16250245226707C997A652DE0FE01E8801C949D1AD5A0DD545 A7288EAA16A0AAE8AC565D235982B

Ex2100.pdf	A1CB41C937162F33DA63E65E9BCEB31E7E0986EDF6CCE773E1D6C14FC5E8B6F258B28E22095EB7E4E397BF344C196F23B9F1BF5347CE45DD3119C220BB0FE38D
Ex2049-part1.pdf	8598507B07BD597304B86FC72EEB2A7B462110E72E2BA57CD365E482412C7F4300C246E292655C86E99A03BD86D9FBA40A9D6A787E6F2588D1DBB99EF42FEFB2
Ex2054.pdf	9B0AD2F968E288EAB74823D7E0C6CCB729CBB64BF002235BA0C2CCAB85930F630F93DFF332B54A49506821739C1EA5524DB900F4785554066E834306C456B966
Ex2049-part2.pdf	0CD209220BF2A745AE7BE1BF2981A82F6E53637063C0604A934D8DDA205E7D602818AE2D352804DA254BCDD6C2601953B28E75FC0D73F68863D27DE96809AB11
Ex2055.pdf	78CCABEBB4B9EB0B64FD1E6C54C0DFFCA60CC7C8C6C8B1C5B7FA52261FF749845DEB25E9800E07963077446160162C027DF7EBBCE37F713B4A3BEEBEBB3C68CC
Ex2101.pdf	BA24CEBF6F6B7FA0016B0D51D7E4F87526D53FCB54FB84C17890ADBB84A4A3F48D8713425DF753F0C55563447CBCCCEC61E39E44642A886ADF9B4A045337A16A
Ex2047-part1.pdf	E3EFA064A944A13C06BA18A10589E151959930044B1AE0AC8D87447B599E8A0AF56DBACCB8477BB25897EB5E58F106C5844DB822BCD12C1B4F0F213E5F583A5C
NL070-14US03_IDS_List_2023-09-17.pdf	F230DCC26BA17FB6B42010E381A7653DA9224FD3741B99F3E60DDA85454F6924F7E9D8AB6FD8A6AA01539997415F1378F825B6595FF59F778F444D82340A2864

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**09/17/2023 10:32:59 PM ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	62810866	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	03/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2172	E20239GM35009602	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	**$260.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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Electronically filed September 17, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☒ The Certification Statement in Item 5 below is applicable.

4b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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Ex. 1002, p. 234

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,

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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 17, 2023

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
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Samsung Electronics Co., Ltd.
Ex. 1002, p. 236

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	3	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 9318160, Case No. IPRIPR2022-01427, Patent Owner Response, filed July 27, 2023
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Patent Owner Response, filed July 27, 2023
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2023, "Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner's Response," July 27, 2023
		IPR2022-01428 of US Patent No. 8787060, Exhibit 2023, "Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner's Response," July 27, 2023
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petitioner's Objections to Patent Owner's Evidence Submitted with Patent Owner's Response, filed August 3, 2023
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2024, USDC, Eastern District of Texas, Marshall Division, Case No. 2:22-cv-203-JRG-RSP, Netlist, Inc. vs. Micron Technology, Inc., et al., Transcript of June 26, 2023, Videotaped Deposition of Harold Stone, Ph.D.
		IPR2022-01427 and IPR2022-01428, Exhibit 2025, Transcript of June 27, 2023, Videoconference Deposition of Andrew Wolfe, Ph.D.
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2027, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Jury Trial Day 1-2023.4.14
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2028, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Trial Transcript-Vol 3 2023.04.18 excerpt
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2029, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Trial Transcript-Vol 4 - 2023.04.19 excerpt
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		IPR2022-01427 of US Patent No. 9318160, Exhibit 2031, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Milton Direct PDX2 Demonstratives-excerpts

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	2	of	3	Attorney Docket Number	NL070-14US03

		IPR2022-01427 of US Patent No. 9318160, Exhibit 2032, Netlist Presentation on US Patent No. 8,787,060, undated
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2036, JEDEC, "Next Big Thing: DDR4 3DS," Server Forum 2014
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2037, SK hynix Newsroom, "Continuing to Make HBM History: The Story of SK hynix's HBM Development," September 8, 2022
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2039, Steve, "Building an SRAM Substitute," September 4, 2015
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2040, Data Centers, "How Long Des NAND Flash Memory Last," December 19, 2008
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2041, Lucas Mearian, "Micron boosts NAND flash endurance six-fold," Computer World, October 19, 2009
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		IPR2022-01427 of US Patent No. 9318160, Exhibit 2045, Everspin Technologies, MR4A08B, 2Mx8RAM Memory, March 2018
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		IPR2022-01427 of US Patent No. 9318160, Exhibit 2050, "Principles of VLSI Design - Capacitance and Resistance Model", CMPE 413, UMBC, undated
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		IPR2022-01427 of US Patent No. 9318160, Exhibit 2052, JIM COOKE, EDN, "Flash memory 101: An introduction to NAND flash," March 20, 2006
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2053, ECE UNM, "Hardware Design with VHDL Design Example: SRAM," December 3, 2008

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	3	of	3	Attorney Docket Number	NL070-14US03

		IPR2022-01427 of US Patent No. 9318160, Exhibit 2054, DONGHYUK LEE, et al. "Simultaneous Multi-Layer Access: Improving 3D-Stacked Memory Bandwidth at Low Cost," ACM Transactions on Architecture and Code Optimization, Vol. 12, No. 4, Article 63, Publication date: December 2015
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2055, Tech Blog, "High Bandwidth Memory is Catching on for Data-Intensive Computer," May 21, 2018
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2100, FIG. 3 of US Patent Publication No. 20110103156
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2101, Jin Hee Cho, et al., "A 1.2V 64Gb 341GB/s HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and Improved Bank Group Data Control," 2018 IEEE International Solid-State Circuits Conference

Examiner Signature		Date Considered	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	09/28/2022	HH
Above Updated	07/07/2023	HH
Above Updated	09/18/2023	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/28/2022	HH
Above	Updated	07/07/2023	HH
Above	Updated	09/18/2023	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
PE2E Search	09/28/2022	HH
Assignee and Inventor search	09/28/2022	HH
PE2E Search	07/07/2023	HH
IPR2022-01427 Reviewed Inter Partes Review of U.S. Patent No. 9,318,160 on 07/05/23	07/05/2023	HH
IPR2022-01428 Reviewed Inter Partes Review of U.S. Patent No. 8,787,060 on 07/06/23	07/06/2023	HH
PE2E Search	09/18/2023	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 240

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	PE2E Search (US-PGPUB)	09/18/2023	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 241

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC						
Symbol					**Type**	**Version**
G11C	/	5	/	066	F	2013-01-01
G11C	/	5	/	06	I	2013-01-01
G11C	/	7	/	1057	I	2013-01-01
G11C	/	7	/	1084	I	2013-01-01
G11C	/	7	/	12	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	18 September 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20230918

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G11C	/	5	/	06	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827 (Primary Examiner) 18 September 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	19	19										
8	2	11	11	20	20										
2	3	12	12												
3	4	13	13												
4	5	14	14												
5	6	15	15												
6	7	16	16												
7	8	17	17												
9	9	18	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	18 September 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20230918

Samsung Electronics Co., Ltd.
Ex. 1002, p. 244

AFCP 2.0 Decision

Application No.	Applicant(s)	
17/694,649	Lee, Hyun	
Examiner	**Art Unit**	**AIA (FITF) Status**
HUAN HOANG	2827	No

This is in response to the After Final Consideration Pilot request filed 12 September 2023.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ The request is not the first proper AFCP 2.0 request submitted in response to the most recent final rejection.

   ☐ Other: _____

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☑ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action . See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other: _____

   Examiner Note: Please attach an interview summary when necessary as described above.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 245

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	66252	(G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:35 PM
L2	11134	(dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:38 PM
L3	1351	2 AND (terminal pad pin) WITH control$4 WITH (data information bit)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:39 PM
L4	1777	2 AND (terminal pad pin) WITH (control$4 command address) WITH (data information bit)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:40 PM
L5	380	4 AND (through ADJ silicon tsv) WITH (die dice ic chip integrated ADJ circuit) WITH (control$4 address)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:43 PM
L6	32	5 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:44 PM
L7	0	6 AND (second another different) WITH (data bit information) near5 port	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD,	OR	ON	ON	2023/09/18 04:45 PM

Samsung Electronics Co., Ltd.
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		WITH (die dice ic chip integrated ADJ circuit) WITH (through ADJ silicon tsv)	DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	142	1 AND package WITH (dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:48 PM
L9	0	8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv) WITH driv$3 WITH size	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:51 PM
L10	268	5 AND chip near3 (select$3 enabl$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:54 PM
L11	31	10 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:54 PM
L12	754	1 AND (dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:57 PM
L13	283	12 AND (terminal pad pin) WITH control$4 WITH (data information bit)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:58 PM
L14	333	12 AND (terminal pad pin) WITH (control$4 command address)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2023/09/18 04:58 PM

		WITH (data information bit)	DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L15	67	14 AND (through ADJ silicon tsv) WITH (die dice ic chip integrated ADJ circuit) WITH (control$4 address)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:59 PM
L16	5	15 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 04:59 PM
L17	0	8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv) WITH driv$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:00 PM
L18	1	8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:01 PM
L19	12579	stack$3 WITH dram WITH (die dice chip)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:03 PM
L20	1019	19 AND (command address) WITH terminal	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:03 PM
L21	915	20 AND data WITH terminal	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD,	OR	ON	ON	2023/09/18 05:04 PM

			DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L22	61	20 AND (command address) WITH terminal WITH (through ADJ silicon tsv)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:05 PM
L23	0	22 AND data WITH port WITH (die dice chip) WITH (through ADJ silicon tsv)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/09/18 05:07 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	(dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND respective AND port AND driver AND size AND different).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/09/18 05:09 PM
N2	0	(dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND enabl$3 AND driver AND isolat$3 AND size AND different).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/09/18 05:12 PM
N3	0	(dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND chip AND select AND port).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/09/18 05:14 PM

Samsung Electronics Co., Ltd.
Ex. 1002, p. 249

Bibliographic Data

Application No: 17/694,649

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /HUAN HOANG/ Examiner's Signature | Initials

Title: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
03/14/2022	365	2827	NL070-14US03
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA, UNITED STATES

INVENTORS

Hyun Lee, Ladera Ranch, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17157903 01/25/2021ABN

17157903 is a CON of 16412308 05/14/2019 PAT 10902886

16412308 is a CON of 15602099 05/22/2017 PAT 10290328

15602099 is a CON of 15095288 04/11/2016 PAT 9659601

15095288 is a CON of 14337168 07/21/2014 PAT 9318160

14337168 is a CON of 13288850 11/03/2011 PAT 8787060

13288850 has PRO of 61409893 11/03/2010

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

03/17/2022

STATE OR COUNTRY

UNITED STATES

ADDRESS

USCH Law, PC

3790 El Camino Real #1147

Palo Alto, CA 94304

UNITED STATES

FILING FEE RECEIVED

$1,820

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	3	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 9318160, Case No. IPRIPR2022-01427, Patent Owner Response, filed July 27, 2023
		Inter Partes Review of US Patent No.8787060, Case No. IPRIPR2022-01428, Patent Owner Response, filed July 27, 2023
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2023, "Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner's Response," July 27, 2023
		IPR2022-01428 of US Patent No. 8787060, Exhibit 2023, "Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner's Response," July 27, 2023
		Inter Partes Review of US Patent No.9318160, Case No. IPRIPR2022-01427, Petitioner's Objections to Patent Owner's Evidence Submitted with Patent Owner's Response, filed August 3, 2023
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2024, USDC, Eastern District of Texas, Marshall Division, Case No. 2:22-cv-203-JRG-RSP, Netlist, Inc. vs. Micron Technology, Inc., et al., Transcript of June 26, 2023, Videotaped Deposition of Harold Stone, Ph.D.
		IPR2022-01427 and IPR2022-01428, Exhibit 2025, Transcript of June 27, 2023, Videoconference Deposition of Andrew Wolfe, Ph.D.
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2027, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Jury Trial Day 1-2023.4.14
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2028, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Trial Transcript-Vol 3 2023.04.18 excerpt
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2029, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Trial Transcript-Vol 4 - 2023.04.19 excerpt
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2030, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Robins Direct Testimony Demonstratives
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2031, USDC, Eastern District of Texas, Marshall Division, Case No. 2:21-CV-463-JRG, Netlist, Inc. v. Samsung Electronics Co., Ltd, et al, Milton Direct PDX2 Demonstratives-excerpts

Examiner Signature	/HUAN HOANG/	Date Considered	09/18/2023

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	2	of	3	Attorney Docket Number	NL070-14US03

		IPR2022-01427 of US Patent No. 9318160, Exhibit 2032, Netlist Presentation on US Patent No. 8,787,060, undated
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2036, JEDEC, "Next Big Thing: DDR4 3DS," Server Forum 2014
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2037, SK hynix Newsroom, "Continuing to Make HBM History: The Story of SK hynix's HBM Development," September 8, 2022
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2039, Steve, "Building an SRAM Substitute," September 4, 2015
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2040, Data Centers, "How Long Des NAND Flash Memory Last," December 19, 2008
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2041, Lucas Mearian, "Micron boosts NAND flash endurance six-fold," Computer World, October 19, 2009
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2043, Micron, "2, 4, 8Gb: x8/x16 Multiplexed NAND Flash Memory Features," ©2004 Micron Technology, Inc.
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2044, STMicroelectronics, M48Z512A M48Z512AY, M48Z512AV, 4 Mbit (512 Kbit x 8) ZEROPOWER® SRAM, June 2011
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2045, Everspin Technologies, MR4A08B, 2Mx8RAM Memory, March 2018
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2046, "3DS Technology," © 2023 Impress Corporation
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2047, Neil H. E. Weste et al., "CMOS VLSI Design - A Circuits and Systems Perspective," 4th Ed. © 2011, 2005, 1993, 1985 Pearson Education, Inc., publishing as Addison-Wesley
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2048, Ji-Young Kim et al. "An Energy-Efficient Design of TSV I/O for HBM With a Data Rate up to 10 Gb/s," IEEE Journal of Solid-State Circuits, 2023
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2049, NangateOpenCellLibrary_typical, February 17, 2011
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2050, "Principles of VLSI Design - Capacitance and Resistance Model", CMPE 413, UMBC, undated
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2051, Kyomin Sohn et al., "A 1.2 V 20 nm 307 GB/s HBM DRAM With At-Speed Wafer-Level IO Test Scheme and Adaptive Refresh Considering Temperature Distribution," IEEE 2016
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2052, JIM COOKE, EDN, "Flash memory 101: An introduction to NAND flash," March 20, 2006
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2053, ECE UNM, "Hardware Design with VHDL Design Example: SRAM," December 3, 2008

Examiner Signature	/HUAN HOANG/	Date Considered	09/18/2023

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 17, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	3	of	3	Attorney Docket Number	NL070-14US03

		IPR2022-01427 of US Patent No. 9318160, Exhibit 2054, DONGHYUK LEE, et al. "Simultaneous Multi-Layer Access: Improving 3D-Stacked Memory Bandwidth at Low Cost," ACM Transactions on Architecture and Code Optimization, Vol. 12, No. 4, Article 63, Publication date: December 2015
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2055, Tech Blog, "High Bandwidth Memory is Catching on for Data-Intensive Computer," May 21, 2018
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2100, FIG. 3 of US Patent Publication No. 20110103156
		IPR2022-01427 of US Patent No. 9318160, Exhibit 2101, Jin Hee Cho, et al., "A 1.2V 64Gb 341GB/s HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and Improved Bank Group Data Control," 2018 IEEE International Solid-State Circuits Conference

Examiner Signature	/HUAN HOANG/	Date Considered	09/18/2023

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 09/21/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/21/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	12/21/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/21/2023
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	12/21/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via Patent Center or EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

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Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/21/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Ex. 1002, p. 257

Notice of Allowability	Application No. 17/694,649	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 09/12/23.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☑ Other PTO-2323.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

REASONS FOR ALLOWANCE

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "second data interconnects electrically coupled to data ports on the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die; and drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals being driven by a respective first driver having a first driver size, a respective signal of the second data signals being driven by a respective second driver having a second driver size different from the first driver size." in combination with the other limitations thereof as is recited in the claim. Claims 3-8 depend on claim 1.

Regarding claim 2: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of “driving second data signals received at respective data terminals to the second plurality of DRAM array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a second data signal to the second plurality of DRAM array dies via a second data interconnect, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is electrically isolated from any data port on the at least one array die, the second driver size being different from the first driver size; wherein the first data interconnects are electrically coupled to data ports on the first plurality of DRAM array dies and electrically isolated from data ports on any of the second plurality of DRAM array dies, and wherein the second data interconnects are electrically coupled to circuitry on the second plurality of DRAM array dies and electrically isolated from data ports on any of the first plurality of DRAM array dies.” in combination with the other limitations thereof as is recited in the claim. Claims 9-11 depend on claim 2.

Regarding claim 12: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of “wherein: each of the data interconnects 1s electrically coupled to data ports on a subset of the plurality of stacked DRAM array dies and is electrically isolated from data ports on any other array die not in the subset of the plurality of stacked DRAM array dies; the data interconnects include

first data interconnects electrically coupled to a first subset of DRAM array dies in the plurality of stacked DRAM array dies, the first subset of DRAM array dies including a first plurality of DRAM array dies; each respective array die of the first plurality of DRAM array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals; each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of DRAM array dies and at least one second TSV in at least one second array die not in the first subset of DRAM array dies; a respective TSV in the first subset of TSVs is coupled to a corresponding data port on a respective array die in the first subset of DRAM array dies; and the at least one second TSV is electrical isolated from any data port on the at least one second array die." in combination with the other limitations thereof as is recited in the claim. Claims 13-20 depend on claim 12.

Therefore, the application is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Terminal Disclaimer

3. The terminal disclaimer filed on 04/05/23 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US

Patent Nos. 8,787,060, 10,902,886, 10,290,328, 9,659,601 and 9,318,160 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 10/04/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/04/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 264

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 17694649
Applicant : Lee
Filing Date : 03/14/2022
Date Mailed : 10/04/2023

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Kam Sin/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 17694649 **Drawings filed: 03/14/2022**

IDENTIFICATION OF DRAWING DEFICIENCIES

- [ ] There is a hole or the image thereof within the illustration. FIG(s)
- [ ] The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- [ ] An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- [ ] The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- [ ] Figure numbers are duplicated or missing. FIG(s)
- [ ] Drawing sheet or figure is missing. FIG(s)
- [ ] Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- [X] The character of the lines, numbers, and letters is poor. FIG(s) 7-8
- [ ] The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- [ ] The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- [ ] Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s)
- [ ] The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- [ ] This utility application contains a photograph of a view that is capable of being illustrated as a line drawing. FIG(s)
- [ ] A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iii).
- [ ] This reissue application contains added and/or amended drawings that are not labeled as “New” or “Amended” or “Canceled” as required by 37 CFR 1.173(b)(3). FIG(s)
- [ ] This Design reissue application contains a drawing that is labeled as “Canceled” but is not surrounded by brackets, or a drawing that is surrounded by brackets but is not labeled as “Canceled.” See 37 CFR 1.173(b)(3). FIG(s)
- [ ] OTHER:
- [ ] COMMENTS:

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**11/03/2023 10:07:58 PM Z ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	63161923	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_312_Amendment.pdf		11	-	155 KB
NL070-14US03_312_Amendment-A.NA.pdf	(1-1)	1	Amendment after Notice of Allowance (Rule 312)	110 KB
NL070-14US03_312_Amendment-CLM.pdf	(2-7)	6	Claims	108 KB
NL070-14US03_312_Amendment-REM.pdf	(8-11)	4	Applicant Arguments/Remarks Made in an Amendment	117 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL070-14US03_312_Amendment.pdf	133B94F9C8F38E4590CA58BCA7125283F00E70A522C637C2C3EDA19FF13AB3CF6C218F18DF2758C294D5F7996CF2F81F125008D7DEE12B295267ADCD4533E1BB
NL070-14US03_312_Amendment-A.NA.pdf	1B8520D2D38312FE8584D239695D79D6207F694A5E6C8BB2CF4EA5EE4527D2CF128E9B3F220C6427A7E8438D8130B243E8C7598600F33911E0CFE31AF2E6FE24
NL070-14US03_312_Amendment-CLM.pdf	60FEAC00816902810961C52F1FAD982EBCFC98FC3036A0FC74FD94FF1EEAE796222A3BBF5DDF22B4343680F6A344950DF19CFB6EE95E6A423A4D0D772120E880
NL070-14US03_312_Amendment-REM.pdf	2DB96C19087B6CEFC3B3EFB99154EFDFE5A03204A9F4BF79CDEE7DF4776B89713555BDD1C559F5C8695C97FDEB55F8B654225CF4922C3F691536A8B01FCEC9B3

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed November 3, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated September 21, 2023, and is submitted under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals ~~being~~ to be driven by a respective first driver having a first driver size, a respective signal of the second data signals ~~being~~ to be driven by a respective second driver having a second driver size different from the first driver size.

19. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

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REMARKS

This amendment is submitted under 37 C.F.R. 1.312 and responds to the Notice of Allowance dated September 21, 2023, in which claims 1-20 are allowed.

REMARKS CONCERNING CLAIMS

Claims 1-2, 7, 12, 14-16, and 18 have been amended.

Claims 1-2, 12, and 18 have been amended to replace the recitations of "electrically coupled to data ports" with "configured to be in electrical communication with respective data ports," to be more consistent with the specification. Support for the amendment can be found throughout the specification, for example:

> "Each of these die interconnects 220 may be **coupled to, or in electrical communication with at least one data port** of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is **in electrical communication with at least one data port** from each of at least two array dies 210 without being **in electrical communication with a data port** from at least one array die 210" (Para. [0029], lines 7-12, *emphasis added*);
>
> "For example, die interconnect 220a may be **in electrical communication with a data port** from array die 210a and **a data port** from array die 210b" (Para. [0030], lines 1-2, *emphasis added*);
>
> "the die interconnect 220b may be **in electrical communication with a data port** from array die 210c and a data port from array die 210d . . . certain embodiments described herein utilize multiple die interconnects to provide **electrical communication to the corresponding data ports** of the array dies" (Para. [0031], lines 1-3 and 16-18, *emphasis added*);
>
> "a die interconnect that was in **electrical communication with at least one data port** of each of the array dies 210" (Para. [0037], lines 2-3, *emphasis added*);
>
> "Each of these die interconnects 320 may be **coupled to, or in electrical communication with at least one port** of at least one of the array dies 310" (Para. [0048], lines 6-8, *emphasis added*);
>
> . . .

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Claims 1-2, 12 and 18 are further amended to replace the recitations of "electrically isolated from data ports" with "not in electrical communication with data ports," to be more consistent with the specification. Support for the amendment can be found throughout the specification, for example:

> "For example, die interconnect 220a . . . **not in electrical communication with any data ports** from array die 210c or any data ports from array die 210d . . . These other die interconnects can be **electrically isolated from** the corresponding data ports of array dies 210c and 210d." (Para. [0030], lines 3-4 and 8-9, *emphasis added*);
>
> "the die interconnect 220b may be in electrical communication with . . . **without being in electrical communication with any data ports** from array die 210a and array die 210b . . . Despite **not being in electrical communication with any data ports** from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b" (Para. [0031], lines 1-5 and 7-11, *emphasis added*);
>
> "In addition, the die interconnects 220 may use via holes to pass through an array die that is not **configured to be in electrical communication with** the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b **using TSVs that do not enable electrical communication between the die interconnect 220b and data ports** of the array dies 210a and 210b" (Para. [0041], lines 1-5, *emphasis added*);
>
> . . .

Claim 14 has been amended to replace the recitations of "electrically isolated from memory cells" with "not configured to provide electrical communication with memory cells," to be more consistent with the specification. Support for the amendment can be found in the specification, for example:

> "in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not **configured to provide electrical communication with the memory cells** of the array die" (Para. [0041], last four lines, *emphasis added*);

Claims 7 and 15-16 have been amended to address minor issues.

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Some of claims 1-2, 12, 14 and 18 are further amended for clarity and/or to address minor issues.

Thus, the amendments do not add new matter and should not necessitate additional search or examination.

The Examiner is invited to call the undersigned attorney at (650) 521-4828 for any questions regarding this amendment and the application.

Respectfully submitted,

Date: November 3, 2023

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM array dies including at least a first plurality of DRAM array dies and a second plurality of DRAM array dies;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the stacked DRAM array dies;

first data interconnects configured to be in electrical communication with respective ~~electrically coupled to~~ data ports on the first plurality of DRAM array dies and not in electrical communication with ~~electrically isolated from~~ data ports on any of the second plurality of DRAM array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies;

second data interconnects configured to be in electrical communication with respective ~~electrically coupled to~~ data ports on the second plurality of DRAM array dies and not in electrical communication with ~~electrically isolated from~~ data ports on any of the first plurality of DRAM array dies, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is not configured to be in electrical communication with ~~electrically isolated from~~ any data port on the at least one array die; and

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of DRAM array dies via

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the second data interconnects, a respective signal of the first data signals ~~being~~ to be driven by a respective one of the first drivers configured to have ~~having~~ a first driver size, a respective signal of the second data signals ~~being~~ to be driven by a respective one of the second drivers configured to have ~~having~~ a second driver size different from the first driver size.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked DRAM array dies, the stacked DRAM array dies including a first plurality of DRAM array dies and a second plurality of DRAM array dies, the DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the stacked DRAM array dies and configurable to communicate a command/address signal to one or more DRAM array dies in the stacked DRAM array dies,

driving first data signals received at respective data terminals to the first plurality of DRAM array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive ~~a~~ one of the first data signals to the first plurality of DRAM array dies via ~~a~~ one of the first data interconnects, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including at least a first plurality of TSVs in the first plurality of DRAM array dies; and

driving second data signals received at respective data terminals to the second plurality of DRAM array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive ~~a~~ one of the second data signals to the second plurality of DRAM array dies via ~~a~~ one of the second data interconnects, each of the second data interconnects including a second respective set of TSVs, the second respective set of TSVs including at least a second plurality of TSVs in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is not configured to be in electrical communication with ~~electrically isolated from~~ any data port on the at least one array die, the second driver size being different from the first driver size;

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wherein the first data interconnects are configured to be in electrical communication with respective ~~electrically coupled to~~ data ports on the first plurality of DRAM array dies and not in electrical communication with ~~electrically isolated from~~ data ports on any of the second plurality of DRAM array dies, and wherein the second data interconnects are configured to be in electrical communication with respective data ports ~~electrically coupled to circuitry~~ on the second plurality of DRAM array dies and not in electrical communication with ~~electrically isolated from~~ data ports on any of the first plurality of DRAM array dies.

3. (Previously Presented) The DRAM package of claim 1, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

4. (Previously Presented) The DRAM package of claim 1, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

5. (Previously Presented) The DRAM package of claim 1, wherein:

each of the second plurality of DRAM array dies is stacked over at least one of the first plurality of DRAM array dies; and

the second driver size is greater than the first driver size.

6. (Previously Presented) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of DRAM array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of DRAM array dies and one of the second data interconnects.

7. (Currently Amended) The DRAM package of claim 1, wherein:

the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;

the plurality of chip select interconnects are respectively coupled to the first plurality of DRAM array dies; and

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the plurality of chip select signals are configured to select one array die among the first plurality of DRAM array dies to receive data in the first data signals.

8. (Previously Presented) The DRAM package of claim 7, further comprising a control die between the stacked DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

9. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (Previously Presented) The method of claim 2, wherein the control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of DRAM array dies, the method further comprising:

driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects, to select one array die among the first plurality of DRAM array dies to receive the first data signals.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

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a plurality of stacked DRAM array dies;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more DRAM array dies in the plurality of stacked DRAM array dies and configurable to communicate a control or address signal to one or more DRAM array dies in the plurality of stacked DRAM array dies, the control interconnects including a plurality of chip select interconnects; and

data interconnects, wherein:

each of the data interconnects is configured to be in electrical communication with a corresponding data port on each of ~~electrically coupled to data ports on~~ a subset of the plurality of stacked DRAM array dies and is not configured to be in electrical communication with any data port ~~electrically isolated from data ports~~ on any other array die of the plurality of stacked DRAM array dies that is not in the subset of the plurality of stacked DRAM array dies;

the data interconnects include first data interconnects configured to be in electrical communication with ~~electrically coupled to~~ a first subset of DRAM array dies in the plurality of stacked DRAM array dies, the first subset of DRAM array dies including a first plurality of DRAM array dies;

each respective array die of the first plurality of DRAM array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of DRAM array dies and at least one second TSV in at least one second array die of the plurality of stacked DRAM array dies that is not in the first subset of DRAM array dies;

a respective TSV [[in]] of the first subset of TSVs is configured to be in electrical communication with ~~coupled to~~ a corresponding data port on a respective array die in the first subset of DRAM array dies; and

the at least one second TSV is not configured to be in electrical communication with ~~electrical isolated from~~ any data port on the at least one second array die.

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13. (Previously Presented) The DRAM package of claim 12, wherein each of the plurality of stacked DRAM array dies includes a DRAM integrated circuit (IC) ~~chip~~, the DRAM IC ~~chip~~ including a number of memory cells.

14. (Currently Amended) The DRAM package of claim 13, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is not configured to provide electrical communication with ~~electrically isolated from~~ memory cells on the corresponding array die.

15. (Currently Amended) The DRAM package of claim 14, wherein the each of the at least one second TSV includes a conducting material in [[a]]the corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

16. (Currently Amended) The DRAM package of claim 14, wherein the each of the at least one second TSV in [[~~a~~]]the corresponding array die of the at least one second array die is connected to a stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (Previously Presented) The DRAM package of claim 13, further comprising a control die between the stack of DRAM array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of DRAM array dies via respective ones of the plurality of chip select interconnects.

18. (Currently Amended) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects configured to be in electrical communication with ~~electrically coupled to~~ a second subset of DRAM array dies in the plurality of stacked DRAM array dies, the second subset of DRAM array dies including a second plurality of DRAM array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of DRAM array dies via the first data interconnects and second

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drivers configurable to drive second data signals to the second plurality of DRAM array dies via the second data interconnects, a respective signal of the first data signals ~~being~~ to be driven by a respective first driver having a first driver size, a respective signal of the second data signals ~~being~~ to be driven by a respective second driver having a second driver size different from the first driver size.

19. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

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Ex. 1002, p. 280

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 11/14/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/694,649	Lee, Hyun	
	Examiner	Art Unit	AIA (FITF) Status
	HUAN HOANG	2827	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 03 November 2023 under 37 CFR 1.312 has been considered, and has been:

a) ☑ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;

☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);

☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/HUAN HOANG/
Primary Examiner, Art Unit 2827

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Ex. 1002, p. 282

Receipt date: 11/03/2023

OK TO ENTER: /H.H/

11/07/2023

Electronically filed November 3, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated September 21, 2023, and is submitted under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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Ex. 1002, p. 283

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 17694649 Document Date: 12/04/2023

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

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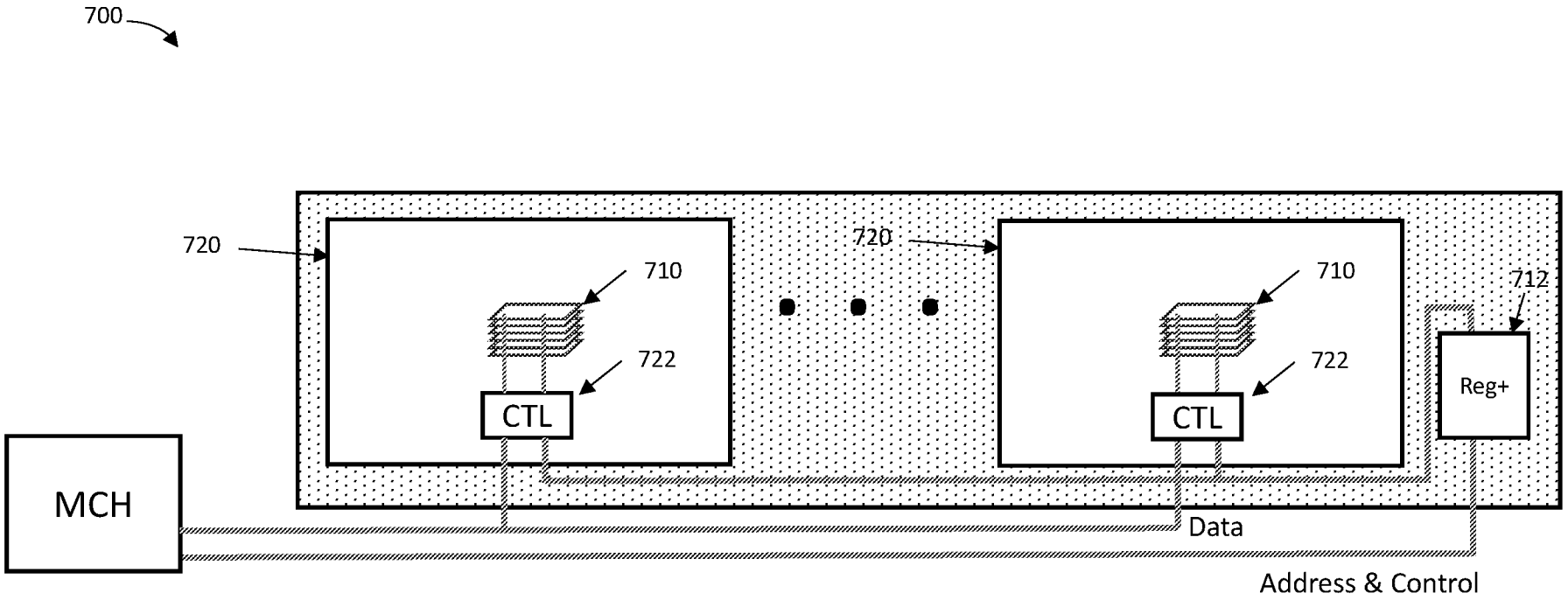

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FIG. 7

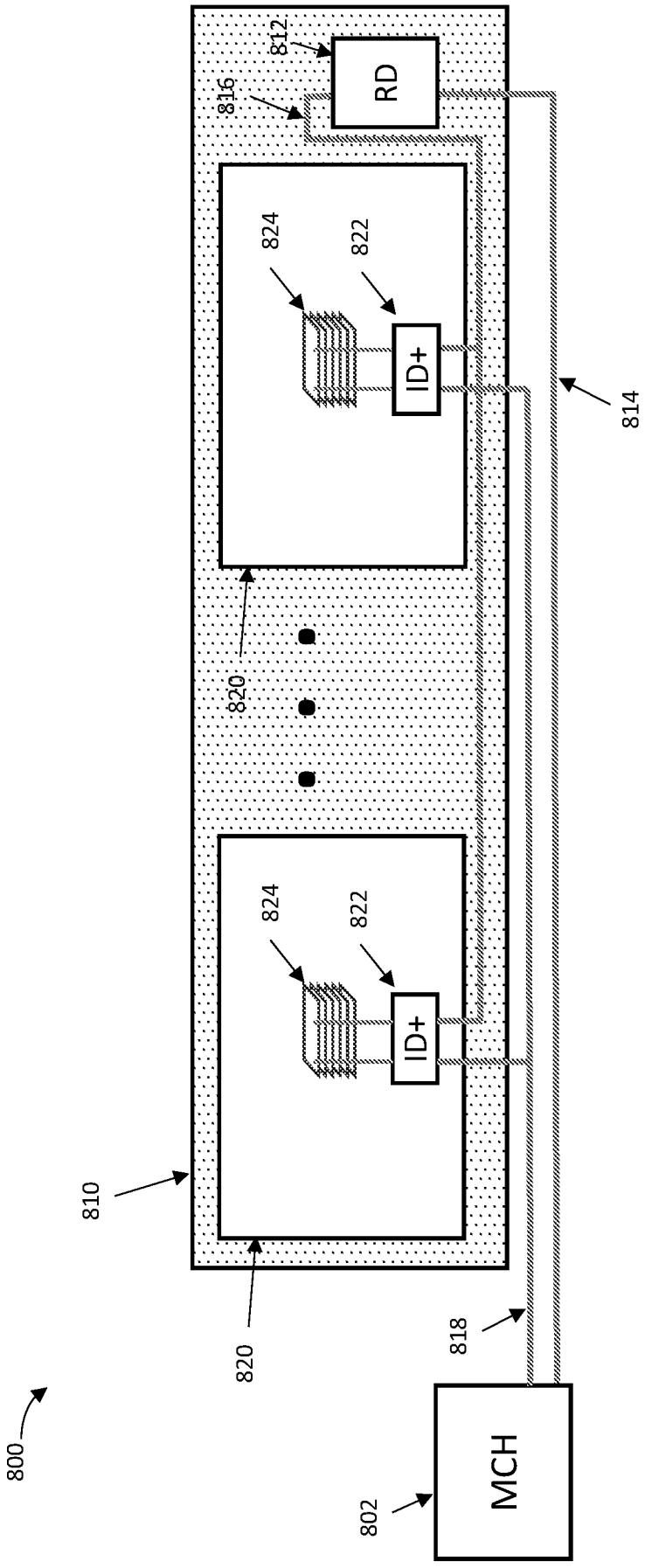


FIG. 8

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**12/04/2023 07:42:24 PM Z ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	63484074	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_Corrected_Drawings.pdf	2	Drawings-only black and white line drawings	85 KB
NL070-14US_Replacement_Drawing_Sheets.pdf	2	Drawings-only black and white line drawings	86 KB
NL070-14US03_M327_2023-10-04.pdf	3	Miscellaneous Incoming Letter	222 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL070-14US03_Corrected_Drawings.pdf	E6F560F3CE7EE1AE0B69E3D70367C8397F762EE6C0F7F6F8228DF5E7A55D4E52169C76A949FF3F588AAE5A42A98A2B2BB4805F0C5A7B6737B1F497B31932A3DD
NL070-14US_Replacement_Drawing_Sheets.pdf	C00E8598463099D039FCFBEE8A1C048C48997C2134FF853AF0C0F5CFD00BAEC5873849F55EAB4BAD6BF348E5C3AA77088DD1B0404960360F818383ACC275668D
NL070-14US03_M327_2023-10-04.pdf	D8EA9D12AF7BA82BADDA8F91E25FD0B283448A3BAA81ADEC388E1BBA036B96F7FE2E5833ACA7256BB79C99FDCDB567CEC5677FCD115196C3551AD330489F9640

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed December 4, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This submission is in response to the Notice to File Corrected Application Papers dated October 4, 2023 (the "Notice"), in the above-referenced patent application. A copy of the Notice is attached hereto. The Notice requires correction of informalities in FIGS. 7 and 8, where the character of the lines, numbers, and letters is poor.

Applicant submits herewith two (2) sheets of replacement drawings containing FIGS. 7 and 8, respectively, in compliance with 37 CFR 1.121(d). FIGS. 7 and 8 in the replacement drawing sheets are the same as FIGS. 7 and 8, respectively, submitted with the above-referenced application, except for the improved clarity in the replacement drawing sheets. Thus, no new matter is added.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 289

The undersigned attorney can be reached at (650) 521-4828 for any question regarding this submission or the present application.

Respectfully submitted,

Date: December 4, 2023

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

Samsung Electronics Co., Ltd.
Ex. 1002, p. 290

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 10/04/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/04/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 291

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 17694649
Applicant : Lee
Filing Date : 03/14/2022
Date Mailed : 10/04/2023

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Kam Sin/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 17694649 **Drawings filed: 03/14/2022**

IDENTIFICATION OF DRAWING DEFICIENCIES

- [ ] There is a hole or the image thereof within the illustration. FIG(s)
- [ ] The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- [ ] An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- [ ] The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- [ ] Figure numbers are duplicated or missing. FIG(s)
- [ ] Drawing sheet or figure is missing. FIG(s)
- [ ] Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- [X] The character of the lines, numbers, and letters is poor. FIG(s) 7-8
- [ ] The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- [ ] The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- [ ] Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s)
- [ ] The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- [ ] This utility application contains a photograph of a view that is capable of being illustrated as a line drawing. FIG(s)
- [ ] A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iii).
- [ ] This reissue application contains added and/or amended drawings that are not labeled as “New” or “Amended” or “Canceled” as required by 37 CFR 1.173(b)(3). FIG(s)
- [ ] This Design reissue application contains a drawing that is labeled as “Canceled” but is not surrounded by brackets, or a drawing that is surrounded by brackets but is not labeled as “Canceled.” See 37 CFR 1.173(b)(3). FIG(s)
- [ ] OTHER:
- [ ] COMMENTS:

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/694,649	Filing Date 03/14/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	12/21/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JAMES T WASHINGTON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**12/21/2023 11:46:43 PM Z ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	63718336	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 16

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_Amendment_RCE.pdf		10	-	156 KB
NL070-14US03_Amendment_RCE-AMSB.pdf	(1-1)	1	Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE)	103 KB
NL070-14US03_Amendment_RCE-CLM.pdf	(2-9)	8	Claims	123 KB
NL070-	(10-10)	1	Applicant Arguments/Remarks	98 KB

14US03_Amendment_RCE-REM.pdf		Made in an Amendment	
NL070-14US03_RCE_SB30PC_20231221.pdf	3	Request for Continued Examination (RCE)	1642 KB
NL070-14US03_IDS_Transmittal_2023-12-21.pdf	4	Transmittal Letter	120 KB
NL070-14US03_IDS_List_2023-12-21.pdf	1	Information Disclosure Statement (IDS) Form (SB08)	177 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
IPR2022-01428_Brogioli_Deposition.pdf	383	Non Patent Literature	1011 KB
IPR2022-01428_Exh1063_Dictionary.pdf	1	Non Patent Literature	291 KB
IPR2022-01428_Exh1064_Dictionary.pdf	1	Non Patent Literature	296 KB
Netlist_Tutorial.pdf	11	Non Patent Literature	1284 KB
IPR2022-00639_Subramanian_Depo.pdf	357	Non Patent Literature	1357 KB
Micron_Claim_Construction_Order.pdf	45	Non Patent Literature	836 KB
IPR2022-	34	Non Patent Literature	882 KB

00639_Reply_POPR.pdf

Warning: The attached file contains comments or annotations. Comments are not recommended and may cause processing problems with the document.

IPR2022-01428_Sur_Reply.pdf	46	Non Patent Literature	3285 KB
IPR2022-01428_Reply_POR.pdf	58	Non Patent Literature	4232 KB
IPR2022-00639_Reply_POR.pdf	70	Non Patent Literature	7207 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL070-14US03_Amendment_RCE.pdf	EEA1208FE66282D3DB44A39A1EA605B59674BD4CEFA1AAB53135AC09D1278AD12E6D4322D1FC25054083EF6F0E80D1A362298BF611500CBFB988CD4B21B9214D
NL070-14US03_Amendment_RCE-AMSB.pdf	B70460E8A34E7DDDE63D36D049393431BC36C5B4F95B4748FA081AA1AABF92F7A8F315E844735FC68AF731802464D7AC7F6EDDC53962BA8198D6863E0476C17
NL070-14US03_Amendment_RCE-CLM.pdf	13039D87D3BCF874D13484F9887329312F9C7C1DE2977BF1F379D432BAB8A025FCAD03FD9C377778390DAFCD1B92518161449E4901218993955CC186786F81F2
NL070-14US03_Amendment_RCE-REM.pdf	94C265B65ADF7CC1C544DA56193F84AB01E822540219083E02EA8C0C5206E94D9BC3F8AE83368BA5D9D1744AD97D49BD792AE747DFC9E0CB8C8C55086EEA9F0D
NL070-14US03_RCE_SB30PC_20231221.pdf	E72F6E32F78562D791335CCF17AD7CBA12379C06106438CD837A5D1304C25437DD4E07C09F5B258DBEFB7703E56788E270097A7165211E11F16A5EDED516B6FF

NL070-14US03_IDS_Transmittal_2023-12-21.pdf	B770AAAEC159E3CBBB3E40005002B0F688A08CCCCD78F978F490CE20AD2DB74FB69C45C8D83A0122E2DE2F68F3A3999672836DD46E760B4D43C9CF954EC02CF3
NL070-14US03_IDS_List_2023-12-21.pdf	63CBB883DC63C4B35EDBB19CFDE48C6651AB1C653E353C938566C6A3CFE7D16963BED7E012E622A840D492C5E1CC250C089B918988496C6529B6704226714 6E6
IPR2022-01428_Brogioli_Deposition.pdf	19341BC009F8C2804CD5A04F9578C311ECA96EBAB9F2BA5690E448BC02A3EC8BB9414C4F1499918ABA752F6C402EF7CA0B45DD02E94C0C9A8A2D466D3F9882C2
IPR2022-01428_Exh1063_Dictionary.pdf	AFDD24364604623F93AF2FE85C47FC9202144E668B8C86F5AEAF330AB974080F007150F3B8427F95871DB38E8BE40F7298CDE28DA63E50296455BC23CDEB51DB
IPR2022-01428_Exh1064_Dictionary.pdf	A6D2C0EAF58DA87E956DB9653C994D4D734D0FC8DFC8B7361FEA3528B9C584ED7A1B6355AB4CD0DEAB424FAFEA24F17135BC1178FC3633A4C2F85598A3D71230
Netlist_Tutorial.pdf	18EC51EA4EFF8B5632D9DAB86A17AAF61B9E92179B657EE6A95CA5DF7A79A7CD2951787D82667476C50A7B998D1B229919D3BFB62EE4EAAC3F679214566DC20B
IPR2022-00639_Subramanian_Depo.pdf	BA0819EFA25DD8B58100052520E92989D7D59488D82871431FE3802E0C9F2326C42C8B9BC32E7F9AB1D37D7F220567C174B3C608BFCDE6DC15BEA5B5BFCFAC5D
Micron_Claim_Construction_Order.pdf	D8F20094D901055FC4B78FF4A51E6AA285EEB1D080558A6AAC2E69D1B269D77A9B06A59EB48BCE95152B46F4A1B96EF333CE5190E48E88AE634BF61026C847D2
IPR2022-00639_Reply_POPR.pdf	B5B6A0D40C3CF4DBB54C7B8B964E6FDF2AEEA67CE10D771D00D5EA0F5093A956D445AF7E01A009A46076DB552B9A3BAAF6C2FA7A810AD55C4F4CE69AB0D0F8E6
IPR2022-01428_Sur_Reply.pdf	DD23F6C6314D11909A93E0FA1D3A28D1C37CF4E11FADE0A0327F94BD05DD45A6E9DA513036CC1710E6E58ADA4B82789963F06F5ECFFA2CDE324FD194FFF1E622

IPR2022-01428_Reply_POR.pdf	C4F18CC2845FC06FABF217F1F86308EA166F4718F9F8115CF09FC9CCB5CE89952BA62FE7D68CF0A42B836CBFF05A968C4AE142B731F7FF1BB4D0F158AFDD0934
IPR2022-00639_Reply_POR.pdf	B12E997DB7A9634A2963194140E252B8ACD6EF92DD51A52631DC2920B4504A0C4ACC0CF2D4B30B36E0AD77DB8B6C360D4FA1C68E766F87FB5B0DEA56953642D

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17/694,649	Filing Date	2022-03-14	Docket Number (if applicable)	NL070-14US03	Art Unit	2827
First Named Inventor	Hyun LEE			Examiner Name	Huan HOANG		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 603916

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jamie J. Zheng/	Date (YYYY-MM-DD)	2023-12-21
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed December 21, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	1	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Loh		2010/0110748	05/06/2010	Best, Scott C.	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed August 26, 2022
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, Petitioner's Reply to Patent Owner's Response, filed May 1, 2023
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, EX2015 - Subramanian Supplemental Declaration IPR2022-00063, filed January 26, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Brogioli Deposition, September 27, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, EX1063 – Dictionary Deposition for "electrical", filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, EX1064 – Dictionary Deposition for "communication", filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Reply to Patent Owner Response, filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Patent Owner's Sur Reply, filed November 21, 2023
		USDC for Eastern District of Texas, Marshall Division, Civil Action No. 2:22-CV-00203-JRG-RSP, Claim Construction Order, issued October 21, 2023
		Inter Partes Review of US Patent No.8787060, Case No. IPR2022-01428, Exhibit 1053 - Netlist's Technology Tutorial, filed October 19, 2023

Examiner Signature		Date Considered	

Electronically filed December 21, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Notice of Allowance dated September 21, 2023, and is submitted with a Request for Continued Examination (RCE), for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked ~~DRAM~~ array dies including at least a first plurality of ~~DRAM~~ array dies and a second plurality of ~~DRAM~~ array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more ~~DRAM~~ array dies in the stacked ~~DRAM~~ array dies and ~~configurable to communicate~~ configured to conduct a control or address signal to one or more ~~DRAM~~ array dies in the stacked ~~DRAM~~ array dies;

first data interconnects configured to conduct first data signals to ~~be in electrical communication with~~ respective data ports on the first plurality of ~~DRAM~~ array dies and not ~~in electrical communication with~~ to data ports on any of the second plurality of ~~DRAM~~ array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including ~~at least~~ a first plurality of TSVs, the first plurality of TSVs including a TSV in each of the first plurality of ~~DRAM~~ array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die;

second data interconnects configured to ~~be in electrical communication with~~ conduct second data signals to respective data ports on the second plurality of ~~DRAM~~ array dies and not ~~in electrical communication with~~ to any data ports on any of the first plurality of ~~DRAM~~ array dies, each of the second data interconnects including ~~a second respective set of TSVs, the second respective set of TSVs including at least~~ a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the

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at least one second array die does not conduct any data signal to any data port on the at least one second array die ~~in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is not configured to be in electrical communication with any data port on the at least one array die~~; and

drivers coupled to the data terminals and including first drivers configurable to drive the first data signals to the first plurality of ~~DRAM~~ array dies via the first data interconnects and second drivers configurable to drive the second data signals to the second plurality of ~~DRAM~~ array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective one of the first drivers configured to have a first driver size, a respective signal of the second data signals to be driven by a respective one of the second drivers configured to have a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the first drivers, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the second drivers;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of a respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of a respective second data interconnect and not to any data port on any of the first plurality of array dies.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked ~~DRAM~~ array dies, the stacked ~~DRAM~~ array dies including a first plurality of ~~DRAM~~ array dies and a second plurality of ~~DRAM~~ array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells, the DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more ~~DRAM~~ array

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dies in the stacked ~~DRAM~~ array dies and ~~configurable to communicate~~ configured to conduct a command/address signal to one or more ~~DRAM~~ array dies in the stacked ~~DRAM~~ array dies,

driving first data signals received at respective data terminals to the first plurality of ~~DRAM~~ array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive ~~one~~ a respective signal of the first data signals to the first plurality of ~~DRAM~~ array dies via ~~one~~ a respective first data interconnect of the first data interconnects, each of the first data interconnects including ~~a first respective set of TSVs, the first respective set of TSVs including at least~~ a first plurality of TSVs, the first plurality of TSVs including a TSV in each of in the first plurality of ~~DRAM~~ array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; and

driving second data signals received at respective data terminals to the second plurality of ~~DRAM~~ array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a respective signal ~~one~~ of the second data signals to the second plurality of ~~DRAM~~ array dies via a respective second data interconnect ~~one~~ of the second data interconnects, each of the second data interconnects including ~~a second respective set of TSVs, the second respective set of TSVs including at least~~ a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die ~~in the second plurality of DRAM array dies and at least one TSV in at least one array die of the first plurality of DRAM array dies, wherein the at least one TSV in the at least one array die is not configured to be in electrical communication with any data port on the at least one array die~~, the second driver size being different from the first driver size;

wherein the first data interconnects are configured to ~~be in electrical communication with~~ conduct the first data signals to respective data ports on the first plurality of ~~DRAM~~ array dies and not ~~in electrical communication with~~ to data ports on any of the second plurality of ~~DRAM~~ array dies, and wherein the second data interconnects are configured to conduct the second data signals to ~~be in electrical communication with~~ respective data ports on the second plurality of

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~~DRAM~~ array dies and not ~~in electrical communication with~~ to data ports on any of the first plurality of ~~DRAM~~ array dies;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of the respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of the respective second data interconnect and not to any data port on any of the first plurality of array dies; and

wherein the first driver size corresponds to a transistor size and/or a number of transistors included in the first driver, and the second driver size corresponds to a transistor size and/or a number of transistors included in the second driver.

3. (Currently Amended) The DRAM package of claim 1, wherein the respective one of the first drivers includes at least one first transistor having a first transistor size and the respective one of the second drivers includes at least one second transistor having a second transistor size that is different from the first transistor size.

4. (Currently Amended) The DRAM package of claim 1, wherein the respective one of the first drivers includes a first number of transistors and the respective one of the second drivers includes a second number of transistors, the second number being different from the first number.

5. (Currently Amended) The DRAM package of claim 1, wherein:

each of the second plurality of ~~DRAM~~ array dies is stacked over at least one of the first plurality of ~~DRAM~~ array dies; and

the second driver size is greater than the first driver size.

6. (Currently Amended) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of ~~DRAM~~ array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of ~~DRAM~~ array dies and one of the second data interconnects.

7. (Currently Amended) The DRAM package of claim 1, wherein:

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the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;

the plurality of chip select interconnects are respectively coupled to the first plurality of ~~DRAM~~ array dies; and

the plurality of chip select signals are configured to select one array die among the first plurality of ~~DRAM~~ array dies to receive data in the first data signals.

8. (Currently Amended) The DRAM package of claim 7, further comprising a control die between the stacked ~~DRAM~~ array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of ~~DRAM~~ array dies via respective ones of the plurality of chip select interconnects.

9. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (Currently Amended) The method of claim 2, wherein the control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of ~~DRAM~~ array dies, the method further comprising:

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driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of ~~DRAM~~ array dies via respective ones of the plurality of chip select interconnects, to select one array die among the first plurality of ~~DRAM~~ array dies to receive the first data signals.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked ~~DRAM~~ array dies, each array die of the plurality of stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more ~~DRAM~~ array dies in the plurality of stacked ~~DRAM~~ array dies and configurable to ~~communicate~~ conduct a control or address signal to one or more ~~DRAM~~ array dies in the plurality of stacked ~~DRAM~~ array dies, the control interconnects including a plurality of chip select interconnects; and

data interconnects, wherein:

each of the data interconnects is configured to be in electrical communication with a corresponding data port on each of a subset of the plurality of stacked ~~DRAM~~ array dies and is not configured to be in electrical communication with any data port on any other array die of the plurality of stacked ~~DRAM~~ array dies that is not in the subset of the plurality of stacked ~~DRAM~~ array dies;

the data interconnects include first data interconnects configured to be in electrical communication with a first subset of ~~DRAM~~ array dies in the plurality of stacked ~~DRAM~~ array dies, the first subset of ~~DRAM~~ array dies including a first plurality of ~~DRAM~~ array dies;

each respective array die of the first plurality of ~~DRAM~~ array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of ~~DRAM~~ array dies and at least one second TSV in at least one second array die

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of the plurality of stacked ~~DRAM~~ array dies ~~that~~, wherein the at least one second array die is not in the first subset of ~~DRAM~~ array dies;

a respective TSV of the first subset of TSVs in a respective array die of the first subset array dies is ~~configured to be~~ in electrical communication with a corresponding data port on [[a]] the respective array die in the first subset of ~~DRAM~~ array dies; and

the at least one second TSV is not ~~configured to be~~ in electrical communication with any data port on the at least one second array die.

13. (Cancelled)

14. (Currently Amended) The DRAM package of claim 13, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is not ~~configured to provide electrical communication with~~ coupled to conducting data signals to memory cells on the corresponding array die.

15. (Previously Presented) The DRAM package of claim 14, wherein the each of the at least one second TSV includes a conducting material in the corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

16. (Previously Presented) The DRAM package of claim 14, wherein the each of the at least one second TSV in the corresponding array die of the at least one second array die is connected to a stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (Currently Amended) The DRAM package of claim 13, further comprising a control die between the stack of ~~DRAM~~ array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of ~~DRAM~~ array dies via respective ones of the plurality of chip select interconnects.

18. (Currently Amended) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects configured to be in electrical communication with a

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second subset of ~~DRAM~~ array dies in the plurality of stacked ~~DRAM~~ array dies, the second subset of ~~DRAM~~ array dies including a second plurality of ~~DRAM~~ array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of ~~DRAM~~ array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of ~~DRAM~~ array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective first driver having a first driver size, a respective signal of the second data signals to be driven by a respective second driver having a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective first driver, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective second driver.

19. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

21. (New) The DRAM package of claim 1, wherein the at least one TSV in the at least one first array die is not in electrical communication with memory cells on the at least one first array die, and the at least one TSV in the at least one second array die is not in electrical communication with memory cells on the at least one second array die.

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REMARKS

This amendment responds to the Notice of Allowance dated September 21, 2023, in which the Examiner allowed 1-20. This amendment is submitted with a request for continued examination (RCE).

Claims 1-8, 11-12, 14, and 17-18 have been amended.

Claim 13 has been cancelled.

New claim 21 has been added.

Support for the amendment can be found in at least paragraphs [0004], [0027]-0028], [0040]-[0041], and [0082] of Specification as filed.

No new matter has been added.

After entry of this amendment, the pending claims are: claims 1-12 and 14-21.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: December 21, 2023

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Electronically filed December 21, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,

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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: December 21, 2023

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	12/21/2023 11:46:43 PM Z ET	NL070-14US03

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	63718336	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	03/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2172	E2023BKN47175100	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1801	REQUEST FOR CONTINUED EXAMINATION (RCE) - 1ST REQUEST (SEE 37 CFR 1.114)	1360.00	1	1360.00
			TOTAL AMOUNT:	$1,360.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	09/28/2022	HH
Above Updated	07/07/2023	HH
Above Updated	09/18/2023	HH
Above Updated	01/13/2024	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/28/2022	HH
Above	Updated	07/07/2023	HH
Above	Updated	09/18/2023	HH
Aove	Updated	01/13/2024	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

Search Notes		
Search Notes	**Date**	**Examiner**
PE2E Search	09/28/2022	HH
Assignee and Inventor search	09/28/2022	HH
PE2E Search	07/07/2023	HH
IPR2022-01427 Reviewed Inter Partes Review of U.S. Patent No. 9,318,160 on 07/05/23	07/05/2023	HH
IPR2022-01428 Reviewed Inter Partes Review of U.S. Patent No. 8,787,060 on 07/06/23	07/06/2023	HH
PE2E Search	09/18/2023	HH
PE2ESearch	01/13/2024	HH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	PE2E Search (US-PGPUB)	09/18/2023	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC						
Symbol					**Type**	**Version**
G11C	/	5	/	066	F	2013-01-01
G11C	/	5	/	06	I	2013-01-01
G11C	/	7	/	1057	I	2013-01-01
G11C	/	7	/	1084	I	2013-01-01
G11C	/	7	/	12	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	13 January 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20240113

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G11C	/	5	/	06	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	13 January 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20240113

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/694,649	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	11	10	20	20										
9	2	12	11	8	21										
2	3	13	12												
3	4	14	14												
4	5	15	15												
5	6	16	16												
6	7	17	17												
7	8	18	18												
10	9	19	19												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	13 January 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office

Part of Paper No.: 20240113

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed December 21, 2023	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	1	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Loh		2010/0110748	05/06/2010	Best, Scott C.	

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed August 26, 2022
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, Petitioner's Reply to Patent Owner's Response, filed May 1, 2023
		Inter Partes Review of US Patent No.10949339, Case No. IPR2022-00639, EX2015 - Subramanian Supplemental Declaration IPR2022-00063, filed January 26, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Brogioli Deposition, September 27, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, EX1063 – Dictionary Deposition for "electrical", filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, EX1064 – Dictionary Deposition for "communication", filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Reply to Patent Owner Response, filed October 19, 2023
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Patent Owner's Sur Reply, filed November 21, 2023
		USDC for Eastern District of Texas, Marshall Division, Civil Action No. 2:22-CV-00203-JRG-RSP, Claim Construction Order, issued October 21, 2023
		Inter Partes Review of US Patent No.8787060, Case No. IPR2022-01428, Exhibit 1053 - Netlist's Technology Tutorial, filed October 19, 2023

Examiner Signature	/HUAN HOANG/	Date Considered	01/13/2024

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	67359	(G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:13 PM
L2	282	1 AND stack$3 WITH (dies dice chip integrated ADJ circuit ic) WITH (second another different) adj2 (set group plurality)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:15 PM
L3	214	2 AND (dram dynamic ADJ ram dynamic ADJ random)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:16 PM
L5	13	3 AND (data bit information) near5 port	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:18 PM
L6	4	"20080025137".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:24 PM
L7	44	3 AND interconnect$4 WITH (tsv through ADJ silicon ADJ vias)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:35 PM
L8	3	3 AND interconnect$4 WITH (tsv through ADJ	(US-PGPUB; USPAT; USOCR; FIT (AP, AT,	OR	ON	ON	2024/01/13 12:36 PM

		silicon ADJ vias) WITH (control$ address$3)	AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L9	5	3 AND data WITH (tsv through ADJ silicon ADJ vias) WITH port	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:37 PM
L10	3925	(memory storage) AND stack$3 WITH (dies dice chip integrated ADJ circuit ic) WITH (second another different) adj2 (set group plurality)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:38 PM
L11	1899	10 AND (dram dynamic ADJ ram dynamic ADJ random)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:38 PM
L12	81	11 AND (data bit information) near5 port	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:38 PM
L13	18	12 AND (tsv through ADJ silicon ADJ vias) WITH (control$4 address$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:39 PM
L14	333	11 AND (tsv through ADJ silicon ADJ vias) WITH (control$4 address$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:45 PM
L15	211	14 AND data WITH (tsv	(US-PGPUB; USPAT;	OR	ON	ON	2024/01/13

		through ADJ silicon ADJ vias) WITH (second another different)	USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				12:47 PM
L16	0	15 AND driv$3 WITH data WITH (size number) WITH transistor	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:48 PM
L17	2	15 AND driv$3 WITH data WITH (size number)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 12:49 PM
L18	170	data adj2 signal WITH (die dice chip ic integrated ADJ circuit) WITH (tsv through ADJ silicon ADJ vias) WITH (second another different)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 01:01 PM
L19	2	18 AND driv$3 WITH size	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 01:02 PM
L20	4	"20100110748".pn.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 01:04 PM
L22	0	15 AND chip adj2 select$3 WITH interconnect$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/01/13 01:17 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	1	"20100110748".pn.	(US-PGPUB; USPAT)	OR	ON	ON	2024/01/13 01:07 PM

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 01/22/2024

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/22/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/22/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 01/22/2024
USCH Law, PC
3790 El Camino Real #1147
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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/22/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 01/22/2024

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/22/2024

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).
https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to:

1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;
3) a contractor of the USPTO having need for the information in order to perform a contract;
4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
9) the Office of Personnel Management (OPM) for personnel research purposes; and
10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/694,649	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the RCE filed on 12/21/23.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 and 14-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

REASONS FOR ALLOWANCE

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "first data interconnects configured to conduct first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a first plurality of TSVs, the first plurality of TSVs including a TSV in each of the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; second data interconnects configured to conduct second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies, each of the second data interconnects including at least a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die; and drivers coupled to the data terminals and including first drivers

configurable to drive the first data signals to the first plurality of array dies via the first data interconnects and second drivers configurable to drive the second data signals to the second plurality of array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective one of the first drivers configured to have a first driver size, a respective signal of the second data signals to be driven by a respective one of the second drivers configured to have a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the first drivers, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the second drivers; wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of a respective first data interconnect and not to any data port on any of the second plurality of array dies; and wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of a respective second data interconnect and not to any data port on any of the first plurality of array dies." in combination with the other limitations thereof as is recited in the claim. Claims 3-8 and 21 depend on claim 1.

Regarding claim 2, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "driving first data signals received at respective data terminals to the first plurality of array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive a respective signal of the first data signals to the first plurality of array dies via a respective first data interconnect of the first data interconnects, each of the first data

interconnects including a first plurality of TSVs, the first plurality of TSVs including a TSV in each of in the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; and driving second data signals received at respective data terminals to the second plurality of array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a respective signal of the second data signals to the second plurality of array dies via a respective second data interconnect of the second data interconnects, each of the second data interconnects including a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die, the second driver size being different from the first driver size; wherein the first data interconnects are configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and wherein the second data interconnects are configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to data ports on any of the first plurality of array dies; wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of the respective first data interconnect and not to any data port on any of the second plurality of array dies; and wherein the respective signal of the second data signals is driven to corresponding data

ports on the second plurality of array dies through TSVs of the respective second data interconnect and not to any data port on any of the first plurality of array dies; and wherein the first driver size corresponds to a transistor size and/or a number of transistors included in the first driver, and the second driver size corresponds to a transistor size and/or a number of transistors included in the second driver." in combination with the other limitations thereof as is recited in the claim. Claims 9-11 depend on claim 2.

Regarding claim 12, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the plurality of stacked array dies and configurable to conduct a control or address signal to one or more array dies in the plurality of stacked array dies, the control interconnects including a plurality of chip select interconnects; and data interconnects, wherein: each of the data interconnects is configured to be in electrical communication with a corresponding data port on each of a subset of the plurality of stacked array dies and is not configured to be in electrical communication with any data port on any other array die of the plurality of stacked array dies that is not in the subset of the plurality of stacked array dies; the data interconnects include first data interconnects configured to be in electrical communication with a first subset of array dies in the plurality of stacked array dies, the first subset of array dies including a first plurality of array dies; each respective array die of the first plurality of array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective

chip select signal of a plurality of chip select signals; each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of array dies and at least one second TSV in at least one second array die of the plurality of stacked array dies that , wherein the at least one second array die is not in the first subset of array dies; a respective TSV of the first subset of TSVs in a respective array die of the first subset array dies is in electrical communication with a corresponding data port on the respective array die in the first subset of array dies; and the at least one second TSV is not in electrical communication with any data port on the at least one second array die." in combination with the other limitations thereof as is recited in the claim. Claims 14-20 depend on claim 12.

Therefore, the application is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Electronically filed March 22, 2024

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated January 22, 2024, and is submitted under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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Ex. 1002, p. 341

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked array dies including at least a first plurality of array dies and a second plurality of array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the stacked array dies and configured to conduct a ~~control or address~~ command/address signal to one or more array dies in the stacked array dies;

first data interconnects configured to conduct first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including ~~a first plurality of TSVs, the first plurality of TSVs including~~ a TSV in each of the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die;

second data interconnects configured to conduct second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies, each of the second data interconnects including ~~a second plurality of TSVs, the second plurality of TSVs including~~ a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die; and

drivers coupled to the data terminals and including first drivers configurable to drive the first data signals received via the data terminals to the first plurality of array dies via the first data

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interconnects and second drivers configurable to drive the second data signals received via the data terminals to the second plurality of array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective one of the first drivers configured to have a first driver size, a respective signal of the second data signals to be driven by a respective one of the second drivers configured to have a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the first drivers, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the second drivers;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of a respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of a respective second data interconnect and not to any data port on any of the first plurality of array dies.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked array dies, the stacked array dies including a first plurality of array dies and a second plurality of array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells, the DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the stacked array dies and configured to conduct a command/address signal to one or more array dies in the stacked array dies,

driving first data signals received at respective data terminals to the first plurality of array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive a respective signal of the first data signals receive via a respective data terminal to the first plurality of array dies via a respective first data interconnect of the first data interconnects, each of the first data interconnects including a first plurality of TSVs, the first

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plurality of TSVs including a TSV in each of in the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; and

driving second data signals received at respective data terminals to the second plurality of array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a respective signal of the second data signals receive via the respective data terminal to the second plurality of array dies via a respective second data interconnect of the second data interconnects, each of the second data interconnects including a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die, the second driver size being different from the first driver size;

wherein the first data interconnects are configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and wherein the second data interconnects are configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to data ports on any of the first plurality of array dies;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of the respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of the respective second data interconnect and not to any data port on any of the first plurality of array dies; and

wherein the first driver size corresponds to a transistor size and/or a number of transistors included in the first driver, and the second driver size corresponds to a transistor size and/or a number of transistors included in the second driver.

3. (Previously Presented) The DRAM package of claim 1, wherein the respective one of the first drivers includes at least one first transistor having a first transistor size and the respective

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one of the second drivers includes at least one second transistor having a second transistor size that is different from the first transistor size.

4. (Previously Presented) The DRAM package of claim 1, wherein the respective one of the first drivers includes a first number of transistors and the respective one of the second drivers includes a second number of transistors, the second number being different from the first number.

5. (Previously Presented) The DRAM package of claim 1, wherein:

each of the second plurality of array dies is stacked over at least one of the first plurality of array dies; and

the second driver size is greater than the first driver size.

6. (Previously Presented) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of array dies and one of the second data interconnects.

7. (Previously Presented) The DRAM package of claim 1, wherein:

the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;

the plurality of chip select interconnects are respectively coupled to the first plurality of array dies; and

the plurality of chip select signals are configured to select one array die among the first plurality of array dies to receive data in the first data signals.

8. (Previously Presented) The DRAM package of claim 7, further comprising a control die between the stacked array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects.

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9. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (Previously Presented) The method of claim 2, wherein the control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of array dies, the method further comprising:

driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects, to select one array die among the first plurality of array dies to receive the first data signals.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked array dies, each array die of the plurality of stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the plurality of stacked array dies and configurable to conduct a command/address ~~control~~

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~~or address~~ signal to one or more array dies in the plurality of stacked array dies, the control interconnects including a plurality of chip select interconnects; and

data interconnects, wherein:

each of the data interconnects is configured to be in electrical communication with a corresponding data port on each of a subset of the plurality of stacked array dies and is not configured to be in electrical communication with any data port on any other array die of the plurality of stacked array dies that is not in the subset of the plurality of stacked array dies;

the data interconnects include first data interconnects configured to be in electrical communication with a first subset of array dies in the plurality of stacked array dies, the first subset of array dies including a first plurality of array dies;

each respective array die of the first plurality of array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of array dies and at least one second TSV in at least one second array die of the plurality of stacked array dies, wherein the at least one second array die is not in the first subset of array dies;

a respective TSV of the first subset of TSVs in a respective array die of the first subset array dies is in electrical communication with a corresponding data port on the respective array die in the first subset of array dies; and

the at least one second TSV is not in electrical communication with any data port on the at least one second array die.

13. (Cancelled)

14. (Currently Amended) The DRAM package of claim [[~~13~~]] 12, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is not coupled to ~~conducting~~ conduct data signals to memory cells on the corresponding array die.

15. (Previously Presented) The DRAM package of claim 14, wherein the each of the at least one second TSV includes a conducting material in the corresponding array die of the at least one

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second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

16. (Previously Presented) The DRAM package of claim 14, wherein the each of the at least one second TSV in the corresponding array die of the at least one second array die is connected to a stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (Previously Presented) The DRAM package of claim 13, further comprising a control die between the stack of array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects.

18. (Previously Presented) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects configured to be in electrical communication with a second subset of array dies in the plurality of stacked array dies, the second subset of array dies including a second plurality of array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective first driver having a first driver size, a respective signal of the second data signals to be driven by a respective second driver having a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective first driver, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective second driver.

19. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size.

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20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

21. (Currently Amended) The DRAM package of claim 1, wherein each of the at least one TSV in the at least one first array die is connected to a stub on a corresponding first array die of the at least one first array die and is not in electrical communication with memory cells on the ~~at least one~~ corresponding first array die, and wherein each of the at least one TSV in the at least one second array die is connected to a stub on a corresponding second array die of the at least one second array die and is not in electrical communication with memory cells on the ~~at least one~~ corresponding second array die.

22. (New) The DRAM package of claim 1, wherein each of the at least one TSV in the at least one first array die includes a first conducting material in a corresponding first array die of the at least one first array die and an insulator or air gap between the first conducting material and a data port on the corresponding first array die, and wherein each of the at least one TSV in the at least one second array die includes a second conducting material in a corresponding second array die of the at least one second array die and an insulator or air gap between the second conducting material and a data port on the corresponding second array die.

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REMARKS

This amendment is submitted under 37 C.F.R. 1.312 and responds to the Notice of Allowance dated January 22, 2022, in which claims 1-12 and 14-21 are allowed.

REMARKS CONCERNING CLAIMS

Claims 1-2, 12, 14, and 21 are amended. New dependent claim 22 is added and depends from claim 1. The amendments do not add new matter and should not necessitate additional search or examination, as discussed below.

Claim 1 is amended to clarify that "the DRAM package receives or outputs data signals in response to the command/address signals." This is described throughout the specification and shown in the drawings. For example, paragraph [0004] states: "The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects." FIGS. 7-8 also shows the memory packages 710 and 820 communicating data with the MCH (memory control hub) in response to Address & Control signals from the MCH.

Claim 1 is further amended to replace "control or address signal" in the third paragraph after the preamble to "command/address signal" to be consistent with the terminology used in the specification (e.g., para. [0006] and [0044]).

Claim 1 is further amended to delete the recitation of "a first plurality of TSVs, the first plurality of TSVs including" in the fourth paragraph after the preamble because the recitation is superfluous. So, instead of the claim reciting "the first respective set of TSVs including a first plurality of TSVs, the first plurality of TSVs including . . . ," claim 1 as amended simply recites "the first respective set of TSVs including . . ." This amendment does not change the meaning of the claim. It only makes the claim easier to read. -Similar amendment is also made in the fifth paragraph under the preamble to address the same issue of superfluous wording.

Claim 1 is further amended to recite "first drivers configurable to drive the first data signals received via the data terminals" and "second drivers configurable to drive the second data signals received via the data terminals." Support for the amendment can be found throughout the

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specification (e.g., para. [0072]: "Signals received at the input/output port 402 can be provided to the drivers 404a and 404b. In turn, these drivers 404a and 404b can drive the signal to conduits 406a and 406b respectively, which are in electrical communication with corresponding die interconnects.")

Corresponding amendments are made in claims 2 and 12, where appropriate.

Claim 14 is amended to correct a dependency error and a typographical error.

Claim 21 is amended to correspond with claim 16. That is, the subject matter of claim 16 is added to claim 21. Support for the amendment can be found in claim 16 and in para. [0041] of the specification starting on the 8th line from the bottom of the paragraph, as quoted below (emphasis added for easy review):

> "In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be **stubs**. These **stubs** are not configured to provide electrical communication with the memory cells of the array die."

Claim 22 is added to correspond with claim 15. That is, claim 22 includes similar subject matter as claim 15 but depends from independent claim 1, while claim 15 depends from independent claim 12. Support for the amendment can be found in para. [0041] of the specification, starting on line 9, as quoted below (emphasis added for easy review):

> "In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include **an insulator or an air gap** between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry."

Therefore, no new matter has been added, and the amendments should not necessitate additional search or examination.

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After entry of this amendment, the pending claims are: claims 1-12 and 14-21.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: March 22, 2024

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**03/22/2024 11:28:25 PM Z ET**	**NL070-14US03**

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	64809566	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NL070-14US03_312_Amendment_2024-03-22.pdf		12	-	164 KB
NL070-14US03_312_Amendment_2024-03-22-A.NA.pdf	(1-1)	1	Amendment after Notice of Allowance (Rule 312)	105 KB
NL070-14US03_312_Amendment_2024-03-22-CLM.pdf	(2-9)	8	Claims	114 KB
NL070-14US03_312_Amendment_2024-03-22-REM.pdf	(10-12)	3	Applicant Arguments/Remarks Made in an Amendment	117 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL070-14US03_312_Amendment_2024-03-22.pdf	ACE3E7AFF02EBF3FA93947A71584A4B58CE26C910E29CB98B48352A82C75B11BD1566FA7B8579B9680633CDB1A5384A2661EA70FEC07DA9DFBD95FB0F2370468
NL070-14US03_312_Amendment_2024-03-22-A.NA.pdf	DCA7EB694A5F0BCF209DBD93D9FF4DDD2826631EDF0E9AE0ACEBA7A6DB36596DB07CBAE2620DB543DCF91BECC149BFE436272439FC675A80E7FF78BA028BA18C
NL070-14US03_312_Amendment_2024-03-22-CLM.pdf	3FBCF2AB6D07F5C78A8191FC3EE54D036023394DE049873D65DCC378401459E712DE9D65411DAFA4DCDA9B770AC269746D23F35545673FB05F9BCF1477C521A8
NL070-14US03_312_Amendment_2024-03-22-REM.pdf	DA860E7A3709024C13F1A1094F6DB14C4250AD9616DE74CE548ED32A55EAF5D71B07A9A3F65BC6C8E280217B9A055EAB8F7BC56C632FAD8A3A65E430742745F9

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 04/01/2024

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
04/01/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/694,649	Lee, Hyun	
	Examiner	Art Unit	AIA (FITF) Status
	HUAN HOANG	2827	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 22 March 2024 under 37 CFR 1.312 has been considered, and has been:

a) ☑ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;

☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);

☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/HUAN HOANG/
Primary Examiner, Art Unit 2827

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Ex. 1002, p. 356

Receipt date: 03/22/2024

OK TO ENTER: /H.H/

03/26/2024

Electronically filed March 22, 2024

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated January 22, 2024, and is submitted under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	04/07/2024 10:53:29 PM Z ET	NL070-14US03

Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3889	FILED BY	Jamie Zheng
PATENT CENTER #	64995824	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	03/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2172	E202447M54076300	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	$260.00

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 7, 2024	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	1	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Hearing Transcript, February 5, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Patent Owner's Corrected Objections to Petitioner's Demonstratives, filed January 9, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Demonstratives for Oral Arguments, filed January 8, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Objections to Patent Owner's Demonstratives, filed January 8, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Netlist's Demonstratives, filed January 8, 2024
		USDC Eastern District of Texas Marshall Division, Civil Action No. 2:22-cv-203-JRG-RSP, Netlist, Inc. v. Micron Technology, Inc. et al., Report & Recommendation, filed January 11, 2024

Examiner Signature		Date Considered	

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/694,649	**04/07/2024 10:53:29 PM Z ET**	**NL070-14US03**

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MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

Application Information

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PATENT CENTER #	64995824	FILING DATE	03/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 7

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
IPR2022-01428_Hearing_Transcript.pdf	89	Non Patent Literature	548 KB
USDC_ED_TX_Report_Recommendation.pdf	10	Non Patent Literature	284 KB
NL070-14US03_IDS_List_2024-04-08.pdf	1	Information Disclosure Statement (IDS) Form (SB08)	173 KB

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IPR2022-01428_PO_Corrected_Objection_Petitioner_Demonstratives.pdf	29	Non Patent Literature	2768 KB
NL070-14US03_IDS_Transmittal_2024-04-07.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	120 KB

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IPR2022-01428_Objection_PO_Demonstratives.pdf	63	Non Patent Literature	10850 KB
IPR2022-01428_Petitioner_Demonstratives.pdf	159	Non Patent Literature	15958 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)
IPR2022-01428_Hearing_Transcript.pdf	7E3B4EC6FC7855114848D5AF71CA759BD50A78828172102713E516AB901132B9BCBB2830C441CAF38E3C39D1027C15BF4D913F7543D023C8CBA9FAC728CE090C
USDC_ED_TX_Report_Recommendation.pdf	224E7722CBD9BCF84834540E1C54CB187FBBDD1F77499C9378EDBFE75335A127863B71A88391030FC1653BC7F06578FB05865CF8BC8413267B6ACA5588AF2E6F
NL070-14US03_IDS_List_2024-04-08.pdf	A6CCB46B35E6A4C082AE784166E5A4D2EA9F34052CD4FD5EAA5DF38B24F5DC694386ED598999BFCB49F43D1D69BFDD90C947A3D99948711934DE34188B10A55F
IPR2022-01428_PO_Corrected_Objectio	87D8545476B9D417F07FBF68080E70D7E7D40A982F3BE99DC7F9247F6A491A64165F2AD3065BBF77F4299A7E621D776B614

n_Petitioner_Demonstratives.pdf	F933FC677D8B8CA7054169DA22F3D
NL070-14US03_IDS_Transmittal_2024-04-07.pdf	1CC42F95F248ACCBCA32195D8F07F13B81796F694920931E73814358D49A783C55790C24EDED61D1EB8ED85166F494AAA914AE777BF8ADD0E74B94717F7F83F1
IPR2022-01428_Objection_PO_Demonstratives.pdf	1292C469CDFF166F2FB44E88C1EEA54F8565A0ED55382B1997FB38EAC3CE94C9C62CB3D9CE794F5531A18C0A5AE6BC5316A4ED7B9A4C40686C20CBFD75B05D6B
IPR2022-01428_Petitioner_Demonstratives.pdf	1B8A4578DEFAE50ABFD40D61C05E64DCEA4C574117DE55BE66DD1BE81970C3452D6F12FDF7FB753C3EF0D5E62C3695EFF7CB15DFE1827C848F46B4CB2E897DC3

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Electronically filed April 7, 2024

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3889
Serial No.:	17/694,649	Group Art Unit:	2827
Filed:	March 14, 2022	Examiner:	Huan HOANG
For:	*MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD*	Attorney Docket No.:	NL070-14US03

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☒ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no.).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,

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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: April 7, 2024

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/694,649	03/14/2022	Hyun Lee	NL070-14US03	3889

79141 7590 04/15/2024

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
04/15/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Supplemental ***Notice of Allowability***	**Application No.** 17/694,649	**Applicant(s)** Lee, Hyun	
	Examiner HUAN HOANG	**Art Unit** 2827	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 04/04/24.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 and 14-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 7, 2024	
				Application Number	17/694,649
				Filing Date	March 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2827
				Examiner Name	Huan HOANG
Sheet	1	of	1	Attorney Docket Number	NL070-14US03

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Hearing Transcript, February 5, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Patent Owner's Corrected Objections to Petitioner's Demonstratives, filed January 9, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Demonstratives for Oral Arguments, filed January 8, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Petitioner's Objections to Patent Owner's Demonstratives, filed January 8, 2024
		Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Netlist's Demonstratives, filed January 8, 2024
		USDC Eastern District of Texas Marshall Division, Civil Action No. 2:22-cv-203-JRG-RSP, Netlist, Inc. v. Micron Technology, Inc. et al., Report & Recommendation, filed January 11, 2024

Examiner Signature	/HUAN HOANG/	Date Considered	04/09/2024

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/