PTO/SB/06 (09-11)
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| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>17/694,649 | Filing Date<br>03/14/2022 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY:** ☑ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED - PART I

| FOR | (Column 1)<br>NUMBER FILED | (Column 2)<br>NUMBER EXTRA | | RATE ($) | FEE ($) |
|---|---|---|---|---|---|
| ☐ BASIC FEE<br>(37 CFR 1.16(a), (b), or (c)) | N/A | N/A | | N/A | |
| ☐ SEARCH FEE<br>(37 CFR 1.16(k), (i), or (m)) | N/A | N/A | | N/A | |
| ☐ EXAMINATION FEE<br>(37 CFR 1.16(o), (p), or (q)) | N/A | N/A | | N/A | |
| TOTAL CLAIMS<br>(37 CFR 1.16(i)) | minus 20 = | * | | x $100 = | |
| INDEPENDENT CLAIMS<br>(37 CFR 1.16(h)) | minus 3 = | * | | x $480 = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | 04/23/2024 | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * 21 | Minus | ** 20 | = 1 | | x $100 = | 100 |
| | Independent<br>(37 CFR 1.16(h)) | * 3 | Minus | *** 3 | = 0 | | x $480 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | 100 |

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * | Minus | ** | = | | x $0 = | |
| | Independent<br>(37 CFR 1.16(h)) | * | Minus | *** | = | | x $0 = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | |

| | |
|---|---|
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. | LIE |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". | /RENEE D HAWKINS/ |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". | |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. | |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

Electronically filed April 22, 2024

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION**

**Mail Stop: Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated January 22, 2024, and is submitted with a Request for Continued Examination (RCE).

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).


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## Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Previously Presented) A dynamic random access memory (DRAM) package, comprising:

stacked array dies including at least a first plurality of array dies and a second plurality of array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals;

control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the stacked array dies and configured to conduct a command/address signal to one or more array dies in the stacked array dies;

first data interconnects configured to conduct first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each of the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die;

second data interconnects configured to conduct second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies, each of the second data interconnects including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die; and

drivers coupled to the data terminals and including first drivers configurable to drive the first data signals received via the data terminals to the first plurality of array dies via the first data interconnects and second drivers configurable to drive the second data signals received via the



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data terminals to the second plurality of array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective one of the first drivers configured to have a first driver size, a respective signal of the second data signals to be driven by a respective one of the second drivers configured to have a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the first drivers, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the second drivers;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of a respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of a respective second data interconnect and not to any data port on any of the first plurality of array dies.

2. (Previously Presented) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked array dies, the stacked array dies including a first plurality of array dies and a second plurality of array dies, each array die of the stacked array dies including data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells, the DRAM package further including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals, the DRAM package further including control interconnects coupled to respective ones of the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the stacked array dies and configured to conduct a command/address signal to one or more array dies in the stacked array dies,

driving first data signals received at respective data terminals to the first plurality of array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive a respective signal of the first data signals receive via a respective data terminal to the first plurality of array dies via a respective first data interconnect of the first data interconnects, each of the first data interconnects including a first plurality of TSVs, the first plurality of TSVs including a TSV in each of in the first plurality of array dies and at least one


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TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; and

driving second data signals received at respective data terminals to the second plurality of array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a respective signal of the second data signals receive via the respective data terminal to the second plurality of array dies via a respective second data interconnect of the second data interconnects, each of the second data interconnects including a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die, the second driver size being different from the first driver size;

wherein the first data interconnects are configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and wherein the second data interconnects are configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to data ports on any of the first plurality of array dies;

wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of the respective first data interconnect and not to any data port on any of the second plurality of array dies; and

wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of the respective second data interconnect and not to any data port on any of the first plurality of array dies; and

wherein the first driver size corresponds to a transistor size and/or a number of transistors included in the first driver, and the second driver size corresponds to a transistor size and/or a number of transistors included in the second driver.

3. (Previously Presented) The DRAM package of claim 1, wherein the respective one of the first drivers includes at least one first transistor having a first transistor size and the respective one of the second drivers includes at least one second transistor having a second transistor size that is different from the first transistor size.


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4. (Previously Presented) The DRAM package of claim 1, wherein the respective one of the first drivers includes a first number of transistors and the respective one of the second drivers includes a second number of transistors, the second number being different from the first number.

5. (Previously Presented) The DRAM package of claim 1, wherein:

each of the second plurality of array dies is stacked over at least one of the first plurality of array dies; and

the second driver size is greater than the first driver size.

6. (Currently Amended) The DRAM package of claim 1, wherein the first driver size corresponds to a first load associated with the first plurality of array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of array dies and one of the second data interconnects, and wherein the first load and the second load are balanced by the first data interconnects being configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and by the second data interconnects being configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies.

7. (Currently Amended) The DRAM package of claim 1, wherein:

~~the control interconnects include a plurality of chip select interconnects corresponding to respective ones of a plurality of chip select signals;~~

~~the plurality of chip select interconnects are respectively coupled to the first plurality of array dies; and~~

the first data signals are associated with first command/address signals received via the control terminals, the first command/address signals including one or more signals ~~plurality of chip select signals are configured~~ to select one array die among the first plurality of array dies to receive data in the first data signals.

8. (Currently Amended) The DRAM package of claim 7, further comprising a control die between the stacked array dies and the terminals, wherein the control die is configured to control timing of command/address signals driven to the stacked array dies and/or timing of data signals


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communicated between the stacked array dies and the data terminals to prevent signal collisions ~~the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects~~.

9. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size.

10. (Previously Presented) The method of claim 2, wherein each of the first driver and the second driver includes a set of transistors, wherein enabling the first driver having the first driver size includes enabling a first number of transistors coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling a second number of transistors coupled to the second data interconnect, the second number being different from the first number.

11. (Currently Amended) The method of claim 2, wherein the first data signals are associated with first command/address signals received via the control terminals, ~~control interconnects include a plurality of chip select interconnects respectively coupled to the first plurality of array dies, the method further comprising:~~

~~driving respective ones of a plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects,~~ the first command/address signals including one or more signals to select one array die among the first plurality of array dies to receive the first data signals.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:


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a plurality of stacked array dies, each array die of the plurality of stacked array dies including command/address ports, data ports and DRAM memory cells, wherein the each array die is configurable to transfer data between the data ports and the DRAM memory cells in response to command/address signals received via the command/address ports;

terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals in response to the command/address signals;

control interconnects coupled to ~~respective ones of~~ the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the plurality of stacked array dies and configurable to conduct a command/address signal received at a respective control terminal of the control terminals to one or more array dies in the plurality of stacked array dies~~, the control interconnects including a plurality of chip select interconnects~~; and

data interconnects, wherein:

each of the data interconnects is configured to be in electrical communication with a corresponding data port on each of a subset of the plurality of stacked array dies and is not configured to be in electrical communication with any data port on any other array die of the plurality of stacked array dies that is not in the subset of the plurality of stacked array dies;

the data interconnects include first data interconnects configured to be in electrical communication with a first subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies, the first subset of array dies including a first plurality of array dies;

the command/address signals received via the control terminals include one or more signals to select an array die in the first subset of array dies to respond to the command/address signals~~each respective array die of the first plurality of array dies is coupled to a respective chip select interconnect of the plurality of chip select interconnects to receive a respective chip select signal of a plurality of chip select signals;~~

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective array dies in the first subset of array dies and at least one second TSV in at least one second array die of the plurality of stacked array dies, wherein the at least one second array die is not in the first subset


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of array dies, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is not in electrical communication with any active circuitry on the corresponding array die;

a respective TSV of the first subset of TSVs in a respective array die of the first subset array dies is in electrical communication with a corresponding data port on the respective array die in the first subset of array dies; and

the at least one second TSV is not in electrical communication with any data port on the at least one second array die.

13. (Cancelled)

14. (Currently Amended) The DRAM package of claim 12, wherein the data interconnects further include second data interconnects configured to be in electrical communication with a second subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies, the second subset of array dies including a second plurality of array dies, the DRAM package further comprising first drivers, second drivers, and pre-drivers, wherein a respective first driver of the first drivers is configurable to drive a first data signal to the first plurality of array dies via a respective one of the first data interconnects, a respective second driver of the second drivers is configurable to drive a second data signal to the second plurality of array dies via a respective one of the second data interconnects, and a respective pre-driver is coupled between a respective data terminal of the date terminals and one or more of the respective first driver and the respective second driver ~~each of the at least one second TSV in a corresponding array die of the at least one second array die is not coupled to conduct data signals to memory cells on the corresponding array die~~.

15. (Currently Amended) The DRAM package of claim 12[[14]], wherein the each of the at least one second TSV includes a conducting material in the corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die.

16. (Currently Amended) The DRAM package of claim 12[[14]], wherein the each of the at least one second TSV in the corresponding array die of the at least one second array die is connected


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to a stub on the corresponding array die, and wherein the stub is not configured to provide any electrical communication with memory cells on the corresponding array die.

17. (Currently Amended) The DRAM package of claim 12[[13]], further comprising drivers coupled to the control terminals and configured to drive the command/address signals to the plurality of stacked array dies ~~a control die between the stack of array dies and the terminals, the control die including the drivers coupled to the data terminals and further including drivers coupled to the control terminals, the drivers coupled to the control terminals including a plurality of chip select drivers configurable to drive respective ones of the plurality of chip select signals to respective array dies of the first plurality of array dies via respective ones of the plurality of chip select interconnects~~.

18. (Currently Amended) The DRAM package of claim 17[[12]], wherein the data interconnects further include second data interconnects configured to be in electrical communication with a second subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies, the second subset of array dies including a second plurality of array dies, the DRAM package further comprising:

drivers coupled to the data terminals and including first drivers configurable to drive first data signals to the first plurality of array dies via the first data interconnects and second drivers configurable to drive second data signals to the second plurality of array dies via the second data interconnects, wherein loads on the first drivers and the second drivers are substantially balanced by the first data interconnects being configured to be in electrical communication with a first subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies, and by the second data interconnects being configured to be in electrical communication with a second subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies~~a respective signal of the first data signals to be driven by a respective first driver having a first driver size, a respective signal of the second data signals to be driven by a respective second driver having a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective first driver, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective second driver~~.


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19. (Currently Amended) The DRAM package of claim 18, further comprising a control die between the stacked array dies and the terminals, wherein the control die is configured to control timing of command/address signals driven to the plurality of stacked array dies and/or timing of data signals between the data terminals and the plurality of stacked array dies to prevent data collisions~~wherein the respective first driver includes at least one first transistor having a first transistor size and the respective second driver includes at least one second transistor having a second transistor size that is different from the first transistor size~~.

20. (Previously Presented) The DRAM package of claim 18, wherein the respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number.

21. (Currently Amended) The DRAM package of claim 1, wherein each of the at least one TSV in the at least one first array die is connected to a stub on a corresponding first array die of the at least one first array die and the stub on the corresponding first array die is not in electrical communication with memory cells on the corresponding first array die, and wherein each of the at least one TSV in the at least one second array die is connected to a stub on a corresponding second array die of the at least one second array die and the stub on the corresponding second array die is not in electrical communication with memory cells on the corresponding second array die.

22. (Previously Presented) The DRAM package of claim 1, wherein each of the at least one TSV in the at least one first array die includes a first conducting material in a corresponding first array die of the at least one first array die and an insulator or air gap between the first conducting material and a data port on the corresponding first array die, and wherein each of the at least one TSV in the at least one second array die includes a second conducting material in a corresponding second array die of the at least one second array die and an insulator or air gap between the second conducting material and a data port on the corresponding second array die.


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*REMARKS*

This amendment is submitted after the Notice of Allowance dated January 22, 2022, in which claims 1-12 and 14-21 are allowed, and is submitted with a Request for Continued Examination (RCE).

REMARKS CONCERNING CLAIMS

Claims 6-8, 11-12, 14-19 and 21 are amended. Support for the amendment can be found in the specification and drawings as filed (e.g., paragraphs [0056], [0069], [0072], [0073]-[0074], [0080], [0102]). Therefore, no new matter is added.

After entry of this amendment, the pending claims are: claims 1-12 and 14-21.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 22, 2024

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

**Customer No. 79141**



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UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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# ELECTRONIC PAYMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| 17/694,649 | 04/23/2024 02:24:41 AM Z ET | NL070-14US03 |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 65200323 | AUTHORIZED BY | - |
| CUSTOMER # | 79141 | FILING DATE | 03/14/2022 |
| CORRESPONDENCE ADDRESS | - | FIRST NAMED INVENTOR | Hyun Lee |

## Payment Information

| PAYMENT METHOD | PAYMENT TRANSACTION ID | PAYMENT AUTHORIZED BY |
|---|---|---|
| CARD / 2172 | E20244M325229300 | Jamie Zheng |

| FEE CODE | DESCRIPTION | ITEM PRICE($) | QUANTITY | ITEM TOTAL($) |
|---|---|---|---|---|
| 1820 | REQUEST FOR CONTINUED EXAMINATION (RCE)- 2ND AND SUBSEQUENT REQUEST (SEE 37 CFR 1.114) | 2000.00 | 1 | 2000.00 |
| | | | TOTAL AMOUNT: | $2,000.00 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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# REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
## (Submitted Only via EFS-Web)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Application Number | 17/694,649 | Filing Date | 2022-03-14 | Docket Number (if applicable) | NL070-14US03 | Art Unit | 2827 |
| First Named Inventor | Hyun LEE | | | Examiner Name | Huan HOANG | | |

**This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.**
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

### SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

### MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

### FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 603916

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
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| Signature of Registered U.S. Patent Practitioner | | | |
|---|---|---|---|
| Signature | /Jamie J. Zheng/ | Date (YYYY-MM-DD) | 2024-04-22 |
| Name | Jamie J. Zheng | Registration Number | 51167 |

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

# Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **04/23/2024 02:24:41 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 65200323 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 8**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| Certificate_Transmission_sb0092.pdf | 2 | Transmittal Letter | 630 KB |
| NL070-14US03_RCE_SB30PC_20240422.pdf | 3 | Request for Continued Examination (RCE) | 1642 KB |
| NL070-14US03_IDS_List_2024-04-22.pdf | 1 | Information Disclosure Statement (IDS) Form (SB08) | 160 KB |

Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.

| | | | | |
|---|---|---|---|---|
| IPR2022-01428_FWD.pdf | | 75 | Non Patent Literature | 1059 KB |
| NL070-14US03_IDS_Transmittal_2024-04-22.pdf | | 4 | Information Disclosure Statement (IDS) Form (SB08) | 120 KB |
| Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems. | | | | |
| NL070-14US03_Amendment_RCE2.pdf | | 11 | - | 156 KB |
| NL070-14US03_Amendment_RCE2-AMSB.pdf | (1-1) | 1 | Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE) | 104 KB |
| NL070-14US03_Amendment_RCE2-CLM.pdf | (2-10) | 9 | Claims | 123 KB |
| NL070-14US03_Amendment_RCE2-REM.pdf | (11-11) | 1 | Applicant Arguments/Remarks Made in an Amendment | 99 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| Certificate_Transmission_sb0092.pdf | CBE0FB9885579E0FEEBD84CFE2D31ABC0B3F0A60A37C182B9FEFF4392F179A285480877C2B0A7A0D89E2FF9DCEE206B6FBCB8EDF28A8D4C1FA638D722FCB879F |
| NL070-14US03_RCE_SB30PC_20240422.pdf | 260C33449BCD8A9111987C186AFF1F2308303FA2FBD1FFD0DDB822F39AC99A76E3E863A2A36816777D83101B6AF269007F89BC82F393380875D0A64EF17ACA51 |

| | |
|---|---|
| NL070-14US03_IDS_List_2024-04-22.pdf | 25A7A8BC996857A0FB164C97479704DA7A02F89F451B9DCE7715BF15E8C54C416369F5EA014D93ACB13F1405E8F9B1D79BD3FA121F8E39EC8D9F71173E289952 |
| IPR2022-01428_FWD.pdf | E918B54480F735098AFFB7FEA37487D7A1B2A0FC9298684002C0F064280A378FC1123D6E95FE4E6FE9EAEF299FEA448DB19DAF8559A9F9861865B62DD562C011 |
| NL070-14US03_IDS_Transmittal_2024-04-22.pdf | 74F305B374F7BA22C3F04C37C5AFB74A269759DA458F5AF16E39F78D840B2A0F8C8E7D5B2C8996D9603DAB26DBD5BA8DF3F472191C3F45F52DBAB7322177566A |
| NL070-14US03_Amendment_RCE2.pdf | E0C4E62F186E54CA278105F56696EC7F56EC4C82566CC69A25060A0C0A512E010D98E776CD7EA9BD2D56A366A2E8745DF11C975834D15A76D5ED35A339937EC5 |
| NL070-14US03_Amendment_RCE2-AMSB.pdf | 6BA3868A1F1C3B0FDA9F1B0F7A22C21A7E9921CED7B7098945FD950C5278FB1233AA7F883F02580AB7DF3E0FC87B5372D067AA66EF3ABA48087BA3FA541FD022 |
| NL070-14US03_Amendment_RCE2-CLM.pdf | E5BB8AC99F9271196643F801EE43AD5D8C56794EFE2D75C82A052AC670D2B3E8F90C806A3430C45C7C27106E2B0F2C6CB7121020B6C856C00FFD332C1B531941 |
| NL070-14US03_Amendment_RCE2-REM.pdf | 48979E26F8D538974166E9D8D0F9F4007FBFA8208B91EA4D1A3DEA82ECA02086C42C6F07C4E6C740EE6F6F3CA11A527F597BC803773AB14E55B2ACE7CD6352FD |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an

international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>Substitute for Form 1449-PTO | | | | Electronically filed April 22, 2024 | |
|---|---|---|---|---|---|
| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 1 | of | 1 | Attorney Docket Number | NL070-14US03 |

| U.S. PATENT DOCUMENTS | | | | | |
|---|---|---|---|---|---|
| Examiner Initials | Cite No. | Document Number<br>Number - Kind Code | Publication Date<br>MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
| | | | | | |

| NON PATENT LITERATURE DOCUMENTS | | |
|---|---|---|
| Examiner Initials | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published |
| | | Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Final Written Decision, April 1, 2024 |
| | | |
| | | |

| Examiner Signature | | Date Considered | |
|---|---|---|---|

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   on _____ ,
   Date

2. ☐ Facsimile transmitted to the United States Patent and Trademark Office, or

   OR

3. ☑ Transmitted via the USPTO's patent electronic filing system (Patent Center or EFS-Web).

| /Jamie J. Zheng/ | April 22, 2024 |
|---|---|
| Signature | Date |
| Jamie J. Zheng | 51167 |
| Typed or printed name | Telephone number |

Note: Each paper must have its own certificate of mailing or transmission, or this certificate must identify each submitted paper:

US Pat. Appl. No. 17/694,649 - Request for Continued Examination (RCE)

US Pat. Appl. No. 17/694,649 - Information Disclosure Statement and Reference

US Pat. Appl. No. 17/694,649 - Amendment

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Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

**Additional Uses**

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

Electronically filed April 22, 2024

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☐ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);


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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

*(Check either Item 3a, 3b, 3c or 3d)*

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

*(Items 3b or 3c to be checked if any reference known for more than 3 months)*

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

*(Check Item 4a, and 4b, 4c or 4d)*

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

*(Check either Item 5a, 5b, 5c or 5d)*


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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

*(Check appropriate Items 7a, 7b and/or 7c)*

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,


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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

*(Check Item 9a, 9b, or 9c)*

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: April 22, 2024

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828


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# United States Patent and Trademark Office

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Document Code:WFEE

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Sale Accounting Date:04/29/2024

| Sale Item Reference Number | Effective Date |
|---|---|
| 17694649 | 04/23/2024 |

| Document Number | Fee Code | Fee Code Description | Amount Paid | Payment Method |
|---|---|---|---|---|
| I20244QN15159407 | 1202 | CLAIMS IN EXCESS OF 20 | $100.00 | Deposit Account |

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENTS** Remove

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|---|---|---|
| | Application Number | 17694649 |
| | Filing Date | 2022-03-14 |
| | First Named Inventor | Hyun LEE |
| | Art Unit | 2827 |
| | Examiner Name | Huan HOANG |
| | Attorney Docket Number | NL070-14US03 |

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| Application Number | 17694649 |
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| | Filing Date | 2022-03-14 |
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

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| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**CERTIFICATION STATEMENT**

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

**SIGNATURE**

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

| | | | |
|---|---|---|---|
| Signature | /Jamie J. Zheng/ | Date (YYYY-MM-DD) | 2024-05-02 |
| Name/Print | Jamie J. Zheng | Registration Number | 51167 |

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| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **05/02/2024 11:36:21 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 65361010 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

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**TOTAL DOCUMENTS: 16**

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| Johnson-2011.pdf | 6 | Non Patent Literature | 534 KB |
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| XiaoxiaWu-Dissertation-dvi.pdf | 3 | Non Patent Literature | 328 KB |
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| Notice of References Cited | Application/Control No. 17/694,649 | Applicant(s)/Patent Under Reexamination Lee, Hyun | |
|---|---|---|---|
| | Examiner HUAN HOANG | Art Unit 2827 | Page 1 of 1 |

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| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | Examiner | Art Unit |
| | HUAN HOANG | 2827 |

| CPC - Searched* | | |
|---|---|---|
| **Symbol** | **Date** | **Examiner** |
| G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12 | 09/28/2022 | HH |
| Above Updated | 07/07/2023 | HH |
| Above Updated | 09/18/2023 | HH |
| Above Updated | 01/13/2024 | HH |
| Above Updated | 06/06/2024 | HH |

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| 365 | 63 | 09/28/2022 | HH |
| Above | Updated | 07/07/2023 | HH |
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| Above | Updated | 01/13/2024 | HH |
| Above | Updated | 06/06/2024 | HH |

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|---|---|
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |


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Ex. 1002, p. 411

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | Examiner | Art Unit |
| | HUAN HOANG | 2827 |

| Search Notes | | |
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| **Search Notes** | **Date** | **Examiner** |
| PE2E Search | 09/28/2022 | HH |
| Assignee and Inventor search | 09/28/2022 | HH |
| PE2E Search | 07/07/2023 | HH |
| IPR2022-01427 Reviewed Inter Partes Review of U.S. Patent No. 9,318,160 on 07/05/23 | 07/05/2023 | HH |
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| PE2E Search | 09/18/2023 | HH |
| PE2ESearch | 01/13/2024 | HH |
| PE2E Search | 06/06/2024 | HH |

| Interference Search | | | |
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| **US Class/CPC Symbol** | **US Subclass/CPC Group** | **Date** | **Examiner** |
| | PE2E Search (US-PGPUB) | 09/18/2023 | HH |

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| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |


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| Index of Claims | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | Examiner | Art Unit |
| | HUAN HOANG | 2827 |

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| = | Allowed | ÷ | Restricted | I | Interference | O | Objected |

**CLAIMS**

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

| CLAIM | | DATE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Final | Original | 09/28/2022 | 07/07/2023 | 06/06/2024 | | | | | | |
| | 1 | ✓ | ✓ | ✓ | | | | | | |
| | 2 | ✓ | ✓ | ✓ | | | | | | |
| | 3 | | ✓ | ✓ | | | | | | |
| | 4 | | ✓ | ✓ | | | | | | |
| | 5 | | ✓ | ✓ | | | | | | |
| | 6 | | ✓ | ✓ | | | | | | |
| | 7 | | ✓ | ✓ | | | | | | |
| | 8 | | ✓ | ✓ | | | | | | |
| | 9 | | ✓ | ✓ | | | | | | |
| | 10 | | ✓ | ✓ | | | | | | |
| | 11 | | ✓ | ✓ | | | | | | |
| | 12 | | ✓ | ✓ | | | | | | |
| | 13 | | ✓ | - | | | | | | |
| | 14 | | ✓ | ✓ | | | | | | |
| | 15 | | ✓ | ✓ | | | | | | |
| | 16 | | ✓ | ✓ | | | | | | |
| | 17 | | ✓ | ✓ | | | | | | |
| | 18 | | ✓ | ✓ | | | | | | |
| | 19 | | ✓ | ✓ | | | | | | |
| | 20 | | ✓ | ✓ | | | | | | |
| | 21 | | | ✓ | | | | | | |
| | 22 | | | ✓ | | | | | | |
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## PE2E SEARCH - Search History (Prior Art)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | British Equivalents | Time Stamp |
|---|---|---|---|---|---|---|---|
| L1 | 66252 | (G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:35 PM |
| L2 | 11134 | (dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3 | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:38 PM |
| L3 | 1351 | 2 AND (terminal pad pin) WITH control$4 WITH (data information bit) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:39 PM |
| L4 | 1777 | 2 AND (terminal pad pin) WITH (control$4 command address) WITH (data information bit) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:40 PM |
| L5 | 380 | 4 AND (through ADJ silicon tsv) WITH (die dice ic chip integrated ADJ circuit) WITH (control$4 address) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:43 PM |
| L6 | 32 | 5 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:44 PM |
| L7 | 0 | 6 AND (second another different) WITH (data bit information) near5 port | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, | OR | ON | ON | 2023/09/18 04:45 PM |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | WITH (die dice ic chip integrated ADJ circuit) WITH (through ADJ silicon tsv) | DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L8 | 142 | 1 AND package WITH (dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3 | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:48 PM |
| L9 | 0 | 8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv) WITH driv$3 WITH size | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:51 PM |
| L10 | 268 | 5 AND chip near3 (select$3 enabl$3) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:54 PM |
| L11 | 31 | 10 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:54 PM |
| L12 | 754 | 1 AND (dynamic ADJ ram dram dynamic ADJ random) near5 (die dice ic chip integrated ADJ circuit) WITH stack$3 | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:57 PM |
| L13 | 283 | 12 AND (terminal pad pin) WITH control$4 WITH (data information bit) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:58 PM |
| L14 | 333 | 12 AND (terminal pad pin) WITH (control$4 command address) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, | OR | ON | ON | 2023/09/18 04:58 PM |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | WITH (data information bit) | DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L15 | 67 | 14 AND (through ADJ silicon tsv) WITH (die dice ic chip integrated ADJ circuit) WITH (control$4 address) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:59 PM |
| L16 | 5 | 15 AND (data bit information) near5 port WITH (die dice ic chip integrated ADJ circuit) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 04:59 PM |
| L17 | 0 | 8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv) WITH driv$3 | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:00 PM |
| L18 | 1 | 8 AND (data information bit) WITH (terminal pad node) WITH (through ADJ silicon tsv) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:01 PM |
| L19 | 12579 | stack$3 WITH dram WITH (die dice chip) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:03 PM |
| L20 | 1019 | 19 AND (command address) WITH terminal | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:03 PM |
| L21 | 915 | 20 AND data WITH terminal | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, | OR | ON | ON | 2023/09/18 05:04 PM |


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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L22 | 61 | 20 AND (command address) WITH terminal WITH (through ADJ silicon tsv) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:05 PM |
| L23 | 0 | 22 AND data WITH port WITH (die dice chip) WITH (through ADJ silicon tsv) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/09/18 05:07 PM |

## PE2E SEARCH - Search History (Interference)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | British Equivalents | Time Stamp |
|---|---|---|---|---|---|---|---|
| N1 | 0 | (dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND respective AND port AND driver AND size AND different).clm. | (US-PGPUB; USPAT) | OR | ON | ON | 2023/09/18 05:09 PM |
| N2 | 0 | (dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND enabl$3 AND driver AND isolat$3 AND size AND different).clm. | (US-PGPUB; USPAT) | OR | ON | ON | 2023/09/18 05:12 PM |
| N3 | 0 | (dram AND stack$3 AND package AND command AND address AND data AND terminal AND die AND interconnect AND tsv AND chip AND select AND port).clm. | (US-PGPUB; USPAT) | OR | ON | ON | 2023/09/18 05:14 PM |

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>Substitute for Form 1449-PTO | | | | Electronically filed April 22, 2024 | |
|---|---|---|---|---|---|
| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 1 | of | 1 | Attorney Docket Number | NL070-14US03 |

| U.S. PATENT DOCUMENTS | | | | | |
|---|---|---|---|---|---|
| Examiner Initials | Cite No. | Document Number<br>Number - Kind Code | Publication Date<br>MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
| | | | | | |

| NON PATENT LITERATURE DOCUMENTS | | |
|---|---|---|
| Examiner Initials | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published |
| | | Inter Partes Review of US Patent No. 8787060, Case No. IPR2022-01428, Final Written Decision, April 1, 2024 |
| | | |
| | | |

| Examiner Signature | /HUAN HOANG/ | Date Considered | 06/06/2024 |
|---|---|---|---|

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENTS** Remove

| Examiner Initial* | Cite No | Patent Number | Kind Code[1] | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | 1 | 9,502,345 | B2 | 2016-11-22 | SUNPIL YOUN, et al. | |
| | 2 | 8,582,373 | B2 | 2013-11-12 | TIMOTHY HOLLIS | |
| | 3 | 9,087,555 | B2 | 2015-07-21 | KEISUKE NOMOTO, et al. | |
| | 4 | 8,179,737 | B2 | 2012-05-15 | SANG JIN BYEON | |
| | 5 | 6,611,459 | B2 | 2003-08-26 | TATSUYA SHIROMOTO, et al. | |
| | 6 | 9,177,609 | B2 | 2015-11-03 | MANUEL ANTONIO D'ABREAU, et al. | |
| | 7 | 8,743,582 | B2 | 2014-06-03 | UK-SONG KANG, et al. | |
| | 8 | 8,437,163 | B2 | 2013-05-07 | TAKUYA NAKANISHI, et al. | |



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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT ( Not for submission under 37 CFR 1.99) | | |
|---|---|---|
| | Application Number | 17694649 |
| | Filing Date | 2022-03-14 |
| | First Named Inventor | Hyun LEE |
| | Art Unit | 2827 |
| | Examiner Name | Huan HOANG |
| | Attorney Docket Number | NL070-14US03 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | 9 | 8,295,070 | B2 | 2012-10-23 | GOU FUKANO | |
| | 10 | 8,476,767 | B2 | 2013-07-02 | HO CHEOL LEE | |
| | 11 | 5,398,210 | | 1995-03-14 | MISAO HIGUCHI | |
| | 12 | 8,473,653 | B2 | 2013-06-25 | CHIKARA KONDO, et al. | |
| | 13 | 8,654,593 | B2 | 2014-02-18 | TAE-YOUNG OH, et al. | |
| | 14 | 7,830,706 | B2 | 2010-11-09 | SATORU HANZAWA, et al. | |
| | 15 | 8,341,336 | B2 | 2012-12-25 | YUAN-HAO CHANG, et al. | |
| | 16 | 5,991,192 | | 1999-11-23 | JINN-SHYAN WANG, et al. | |

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**U.S.PATENT APPLICATION PUBLICATIONS** Remove

| Examiner Initial* | Cite No | Publication Number | Kind Code[1] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | 1 | 20120106229 | A1 | 2012-05-03 | CHIKARA KONDO | |

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

( **Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**FOREIGN PATENT DOCUMENTS** Remove

| Examiner Initial* | Cite No | Foreign Document Number[3] | Country Code[2] | Kind Code[4] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear | T[5] |
|---|---|---|---|---|---|---|---|---|
| | 1 | | | | | | | ☐ |

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| Examiner Initials* | Cite No | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published. | T[5] |
|---|---|---|---|
| | 1 | YIRAN LI, et al., Exploiting Three-Dimensional (3D) Memory Stacking to Improve Image Data Access Efficiency for Motion Estimation Accelerators, Preprint submitted to Signal Processing: Image Communication, March 31, 2010 | ☐ |
| | 2 | LI JIANG, et al., Modeling TSV Open Defects in 3D-Stacked DRAM, IEEE INTERNATIONAL TEST CONFERENCE, Paper 6.1, 2010 | ☐ |
| | 3 | XIAOXIA WU, Design Exploration for Three-dimensional Integrated Circuits (3D ICs), Doctor of Philosophy Dissertation, October 25, 2010, pages 30-32 | ☐ |
| | 4 | PAUL FALKENSTERN, Electronic Design Automation Challenges in Three Dimensional Integrated Chips (3D ICs), Master of Science Master Thesis, November 11, 2008, pages 1-2 | ☐ |
| | 5 | R. COLIN JOHNSON, Multidimensional Efforts Push Toward 3-D Chips, Electronic Engineering Times, October 10, 2011, pages 26-32 | ☐ |
| | 6 | RAKESH ANIGUNDI, et al., Architecture Design Exploration of Three-Dimensional (3D) Integrated DRAM, 10th International Symposium on Quality Electronic Design, 2009 | ☐ |
| | 7 | KATSUYUKI SAKUMA, et al., 3D Chip-Stacking Technology With Through-Silicon Vias And Low-Volume Lead-free Interconnections, IBM Journal of Research and Development Vol. 52 No. 6, November 2008, pages 611-622 | ☐ |



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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT ( Not for submission under 37 CFR 1.99) | | |
|---|---|---|
| | Application Number | 17694649 |
| | Filing Date | 2022-03-14 |
| | First Named Inventor | Hyun LEE |
| | Art Unit | 2827 |
| | Examiner Name | Huan HOANG |
| | Attorney Docket Number | NL070-14US03 |

| | | | |
|---|---|---|---|
| | 8 | QI WU, et al., Impacts of Though-DRAM Vias in 3D Processor-DRAM Integrated Systems, 2009 | ☐ |
| | 9 | WANGYUAN ZHANG, et al., Exploring Phase Change Memory and 3D Die-Stacking for Power/Thermal Friendly, Fast and Durable Memory Architectures, 2009 18th International Conference on Parallel Architectures and Compilation Techniques, 2009 | ☐ |
| | 10 | CHRISTIAN WEIS, et al., Design Space Exploration for 3D-stacked DRAMs, 2011 Design, Automation & Test in Europe, 2011 | ☐ |
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| | 14 | IGOR LOI, et al., An Efficient Distributed Memory Interface For Many-Core Platform With 3D Stacked DRAM, 2010 Design, Automation & Test in Europe Conference & Exhibition, 2010 | ☐ |
| | 15 | JUNG-SIK KIM, et al., A 1.2 v 12.8 GB/s 2 Gb mobile wide-I/O DRAM with 4 × 128 I/Os using TSV Based Stacking, IEEE Journal of Solid-State Circuits Vol. 47 No. 1, January 2012, Pages 107-116 | ☐ |

If you wish to add additional non-patent literature document citation information please click the Add button Add

**EXAMINER SIGNATURE**

| Examiner Signature | /HUAN HOANG/ | Date Considered | 06/06/2024 |
|---|---|---|---|

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.



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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

## CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

**OR**

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

## SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

| | | | |
|---|---|---|---|
| Signature | /Jamie J. Zheng/ | Date (YYYY-MM-DD) | 2024-05-02 |
| Name/Print | Jamie J. Zheng | Registration Number | 51167 |

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**



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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



Samsung Electronics Co., Ltd.
Ex. 1002, p. 424

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

79141 7590 06/11/2024

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER |
|---|
| HOANG, HUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 06/11/2024 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com



Samsung Electronics Co., Ltd.
Ex. 1002, p. 425

| Office Action Summary | Application No. 17/694,649 | Applicant(s) Lee, Hyun | |
|---|---|---|---|
| | Examiner HUAN HOANG | Art Unit 2827 | AIA (FITF) Status No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☑ Responsive to communication(s) filed on 23 April 2024.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5) ☑ Claim(s) 1-12 and 14-22 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 and 14-22 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 14 March 2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

## DETAILED ACTION

### *Notice of Pre-AIA or AIA Status*

1. The present application is being examined under the pre-AIA first to invent provisions.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-12 and 14-22 are ejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

The recitation of "the first respective set of TSVs including a TSV in each of the first plurality of array dies and **at least one TSV in at least one first array die of the**

**second plurality of array dies,** wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die." in claims 1, lines 15-19, claim 2, lines 17-21 and claim 12, lines 30-35 is neither disclosed in the specification nor shown in any of the drawings.

According to Fig. 2, the first interconnects are 220a, 252a and 252b for the first plurality memory array dies 210a and 210b, each of the first data interconnects comprises set of TSVs (210a has two TSVs, 252a has one TSV and 252b has one TSV). Fig. 2 does not show the first respective set of TSVs including a TSV in each of the first plurality of array dies and at least one at least one TSV in at least one first array die of the second plurality of array dies. In fact, the first respective set of TSVs only includes a TSV in each of the first plurality of array dies.

According to Fig. 3, the first interconnects are 320a, 320b and 320c for the first plurality memory array dies 310a, 310b, 310c, 310d and 310e, each of the first data interconnects comprises set of TSVs (320a has two TSVs, 320b has four TSVs, 320c has 5 TSVs). The first respective set of TSVs include a TSV in each of the first plurality of array dies, but do not include at least one TSV in at least one first array die of the second plurality of array dies.

## *Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoko et al. discloses a semiconductor device, semiconductor testing method and data processing system.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

| **AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS** | | |
|---|---|---|
| | Application No. | 17/694,649 |
| | Filing Date | 2022-03-14 |
| | First Named Inventor | Hyun LEE |
| | Art Unit | 2827 |
| | Examiner Name | Huan HOANG |
| | Practitioner Docket No. | NL070-14US03 |

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**I. To authorize permission for Internet Communications.**

☑ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

**II. To withdraw authorization for Internet Communications.**

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 51167.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Jamie J. Zheng/ — Signature

September 9, 2024 — Date

Jamie J. Zheng — Typed or printed name

650-521-4828 — Telephone Number

**NOTE:** This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

# Privacy Act Statement

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **09/09/2024 03:32:33 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 67089998 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 1**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| NL070-14US03_USPTO_SB439_20240909.pdf | 2 | Internet Communications Authorization | 101 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| NL070-14US03_USPTO_SB439_20240909.pdf | A736F92E155817771769991A5F7064D6272304211DA0814000B74E479D514F4BFE4F026B321DD2A338FC0257C7CC5D267914A76866E3367E4FED915DBAB83410 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

WO201021410A1

# Stacked memory chip, semiconductor integrated circuit device using same, and manufacturing method therefor


## Abstract

Memory areas that operate independently for each logic macro of a semiconductor chip cannot be reserved with the memory configuration required by the logic macros. A stacked memory chip stacked on the semiconductor chip comprises a plurality of memory elements arranged in a two-dimensional array, wherein each of the memory elements is provided with an inter-chip I/O section for transmitting a signal between the stacked memory chip and the semiconductor chip, a memory macro capable of writing and reading data, and first wiring for transmitting the data, an address signal, and a command between the adjacent memory elements, and wherein the write data from the semiconductor chip is transferred to the memory macros of the memory elements via the inter-chip I/O sections to perform the write operation, and the data read from the memory macros is transferred to the semiconductor chip via the inter-chip I/O sections.


## Description

TECHNICAL FIELD

[0001] The present invention relates to a stacked memory chip stacked on a semiconductor chip that is a system on chip provided with a plurality of logical macros, a semiconductor integrated circuit device in which the semiconductor chip and the stacked memory chip are stacked, and a method for manufacturing the same.

BACKGROUND ART

[0002] Information terminal devices such as mobile phones are becoming more multifunctional, such as voice processing functions and image processing functions, so it is desirable that a large number of logical macros be mounted on a semiconductor chip used in the information terminal device. With miniaturization of semiconductor processes, it becomes possible to integrate many logical macros on chips, and the number of logical macros exceeds 10. A semiconductor chip that integrates multiple functions on a single chip in this manner is referred to as a System On Chip (System on Chip ; SoC). Many logical macros consist of CMOS (Complementary Metal Oxide Semiconductor) logic circuits. Each logical macro requires a memory for temporary storage of programs and data, and includes a memory for temporary storage of programs and data, such as SRAM (Static Random Access Memory), DRAM (Dynamic Random Access Memory), and the like. A memory, such as MRAM (Magnetoresistive Random Access Memory), is located near the logical macro. Since the memory needs to have an analog circuit configuration, optimized transistors and storage elements are used separately from logic circuits. Fig.49 is a plan view illustrating the configuration of logic macros and

on-chip memory in an SoC chip. In the SoC chip 300 of Fig.49, on-chip memory is disposed for each logical macro. Logic macro 301 A accesses memory 302 a, logic macro 301 B accesses memory 302 b, logic macro 301 C accesses memory 302 c, and logic macro 301 D accesses memory 302 d. 303 is an I/O port of the logic macro 301 A connected to the memory 302 a, 304 is an I/O port of the memory 302 a connected to the logic macro 301 A, 305 is an I/O port of the logic macro 301 A connected to the logic macro 301 B, and 306 is an I/O port of the logic macro 301 B connected to the logic macro 301 A. The total on-chip memory area occupies near 1/2 of the chip as a whole. Compared to digital logic circuits, memory has low noise resistance and is difficult to follow miniaturization of a semiconductor process, so the area occupied by the memory in a chip is increased. Increasing the amount of data handled also increases the memory area. In a process with a gate length of 90 nm generation, the percentage of memory occupied in the chip is half. In the past, the number of installed logical macros can be increased by miniaturization, but in the future, the area in which the logical macros can be used in an SoC chip is reduced, making it difficult to increase the number of macros. In addition, when the occupied area of the memory is increased, arranging a large number of logic macros and the memory in the chip causes a problem in that a delay in transmission of a signal between the logic macros and the memory or a delay in transmission of a signal between the logic macros and other logic macros increases. For example, in a case where logic macros and memories are gathered and arranged, for logic macros arranged far from the memory, the wiring distance between the logic macros and the memory accessed may extend to half or more of the chip size, increasing the transmission delay between the logic macros and the memory. On the other hand, in a case where the memory accessed by each of the logical macros is disposed near each of the logical macros, the distance between the logical macros and the memory decreases, but the memory having a large area is disposed between the logical macros, the wiring distance between the logical macros increases, and the transmission delay between the logical macros increases. In order to reduce the memory area in the chip, it is conceivable to turn off the memory of the logical macros off chip. However, in off-chip memory typified by a general-purpose DRAM, the input/output unit (inter-chip I / O unit) is limited to one or several, so it is not possible to secure a plurality of memory regions that operate independently for each of a large number of logical macros in a single off-chip memory. Although it is possible to operate the memory independently for each logical macro using a plurality of off-chip memories, it is necessary to use a number of memory chips in accordance with the number of logical macros. Furthermore, because the required memory capacity differs for each logical macro, a memory chip having an excessive capacity must be used in general purpose products having a fixed memory configuration. Stacked memory devices with a large capacity by stacking memories have been proposed as technologies other than general purpose DRAM chips (see Patent Document 1). In this stacked memory device, the entire memory chip constitutes one memory region or four memory regions. In addition, it has a plurality of data input/output sections to/from the outside of the chip, and the

number of input/output bits of data can be changed by the interface chip stacked with the memory chip. Patent Document 2 proposes an integrated device in which a memory and a logic macro are stacked using different dies. The memory of this integrated device includes a plurality of memory banks, and is capable of exchanging data with a plurality of logical macros.

PATENT CITATIONS

Japanese Unexamined Patent Application Publication No.2006-012337 (paragraphs "0020"~ "0026"~ Fig. 1)

Japanese Unexamined Patent Application Publication No.2008-047079 (paragraphs "0026"~ "0050"~ Fig. 4)

DISCLOSURE

TECHNICAL PROBLEM

[0003] In the stacked memory device disclosed in Patent Document 1 described above, the memory configuration is fixed, so there is a problem in that it is not possible to secure a large number of memory regions having different capacities for each of the plurality of logical macros from a single memory chip and to operate the memory regions independently. Also, in the integrated device disclosed in Patent Document 2 described above, the number of I / O connections is increased or decreased after the memory chip is manufactured for the input/output ports (I / O) between the dies (between chips), and Because the connection position cannot be selected or the like, there is a problem in that one type of memory chip cannot be stacked on SoC chips of different logical macro configurations. An object of the present invention is to provide a stacked memory chip that solves the above-described problem in that a memory region that operates independently for each logic macro of the semiconductor chip cannot be secured with a memory configuration required by the logic macro, a semiconductor integrated circuit device using the stacked memory chip, and a method for manufacturing the stacked memory chip.

TECHNICAL SOLUTION

[0004] A stacked memory chip of the present invention is a stacked memory chip stacked on a semiconductor chip, the stacked memory chip including a plurality of memory elements arranged in a two-dimensional array, each memory element including: A semiconductor device comprising: an inter-chip I / O portion that transmits signals to and from a semiconductor chip; a memory macro capable of writing and reading data; and a memory macro capable of writing and reading data to and from an adjacent memory element, And first wiring that transmits address signals and commands, wherein writing data from the semiconductor chip is transferred to a memory macro of the memory element via the inter-chip I / O portion to perform a writing operation, and reading data read from the memory macro is transferred to the semiconductor chip via the inter-chip I / O portion. A semiconductor integrated circuit device of the present invention includes a stacked memory chip and a semiconductor chip that includes a plurality of logical macros

stacked on the stacked memory chip, wherein the stacked memory chip includes: A stacked memory chip stacked on a semiconductor chip, comprising: a plurality of memory elements arranged in a two-dimensional array, wherein each of the memory elements includes: an inter-chip I / O portion that transmits signals to and from the semiconductor chip; A memory macro capable of writing and reading data, and a first interconnect for transmitting data, address signals, and commands to and from adjacent memory elements, wherein write data from a semiconductor chip is transmitted to and from an inter-chip I / O portion, and read data read from the memory macro is transferred to the semiconductor chip via the inter-chip I / O portion. A method for manufacturing a semiconductor integrated circuit device according to the present invention includes the steps of: forming, on a semiconductor chip having a multilayer wiring structure, a first bonding electrode layer formed from a portion of an electrode layer constituting the multilayer wiring structure included in the semiconductor chip; A method for manufacturing a semiconductor device, comprising the steps of: forming, on a stacked memory chip stacked on a semiconductor chip and provided with a multi-layer wiring structure, a second electrode layer for joining that is formed from a portion of an electrode layer constituting the multi-layer wiring structure included in the stacked memory chip; and joining the first electrode layer for joining and the second electrode layer for joining, wherein the stacked memory chip is a stacked memory chip stacked on the semiconductor chip; A memory device comprising: a plurality of memory elements arranged in a two-dimensional array, wherein each of the memory elements includes an inter-chip I / O portion that transmits signals to and from stacked semiconductor chips, a memory macro capable of writing and reading data, and a plurality of memory elements including data to and from adjacent memory elements, And first wiring that transmits address signals and commands, wherein writing data from the semiconductor chip is transferred to a memory macro of the memory element via the inter-chip I / O portion to perform a writing operation, and reading data read from the memory macro is transferred to the semiconductor chip via the inter-chip I / O portion.

ADVANTAGEOUS EFFECTS

[0005] According to the present invention, a memory region that operates independently for each logic macro of a semiconductor chip can be secured with a memory configuration required by the logic macro.

DESCRIPTION OF DRAWINGS

[0006] Fig. 1 A is a plan view illustrating the configuration of an SoC chip and a stacked memory chip according to the embodiment of the present invention. Fig. 1 B is a cross-sectional view schematically illustrating the SoC chip and the stacked memory chip after flip chip mounting. Fig.2 is a plan view illustrating the configuration of a stacked memory chip according to a first embodiment of the present invention, and is an enlarged plan view illustrating the configuration of a memory element of the stacked memory chip. Fig.3 is a block diagram illustrating a

circuit configuration of an SRAM macro of the memory element according to the first embodiment of the present invention. Fig.4 is a circuit diagram illustrating the configuration of the switch fabric of the memory element according to the first embodiment of the present invention. Fig.5 is a block diagram illustrating the configuration of a configuration register of the memory element according to the first embodiment of the present invention. Fig.6 illustrates the connection between configuration registers between a plurality of memory elements in the first embodiment of the present invention. Fig.7 is a connection diagram illustrating a case where each memory element is operated as a 16-bit 1 k-word independent memory region in the first embodiment of the present invention. Fig.8 is a connection diagram illustrating a case where four memory elements are combined and operated as a 16-bit 4 k-word memory region in the first embodiment of the present invention. Fig.9 is a plan view illustrating the configuration of the SoC chip and the stacked memory chip when the memory region accessed by the logical macros is 32-bit 4 k word in the first embodiment of the invention. Fig.10 is a connection diagram illustrating a case where eight memory elements are combined and operated as a 32-bit 4 k-word memory region in the first embodiment of the present invention. Fig. 11 A illustrates the interconnection of clocks in the logic macro of the SoC chip in the first embodiment of the invention. Fig. 11 B is a diagram illustrating clock wiring within a memory element of the stacked memory chip. Fig.12 is a plan view illustrating an example in which the number and positions of memory regions and inter-chip I / O are configured according to the SoC chip in the first embodiment of the present invention. Fig.13 is a plan view illustrating another example of configuring the number and position of the memory region and inter-chip I / O according to the SoC chip in the first embodiment of the present invention. Fig.14 is a plan view illustrating another example of configuring the number and position of the memory region and inter-chip I / O according to the SoC chip in the first embodiment of the present invention. Fig.15 is a plan view illustrating another example of configuring the number and position of the memory region and inter-chip I / O according to the SoC chip in the first embodiment of the present invention. Fig.16 is a plan view illustrating the configuration of an SoC chip and a stacked memory chip in which the logical macros of the SoC chip are mixed with operating and inactive macros in the first embodiment of the present invention. Fig.17 is a plan view illustrating the configuration of an SoC chip and a stacked memory chip in which the logical macros of the SoC chip are mixed with operating and inactive macros in the first embodiment of the present invention. Fig.18 is a plan view illustrating the configuration of a stacked memory chip that includes a memory region in opposition to the inactive logic macro. Fig.19 is a plan view illustrating another stacked memory chip configuration that includes a memory region in opposition to the inactive logic macro. Fig.20 is a plan view illustrating the configuration of yet another stacked memory chip that includes a memory region in opposition to the inactive logic macro. Fig.21 is a plan view illustrating the configuration of a stacked memory chip in which different types of SRAM macros are arranged. Fig.22 is a plan view illustrating the configuration of a stacked

memory chip in which different types of SRAM macros are arranged, and a plan view illustrating the configuration of a corresponding SoC chip. Fig.23 is a plan view illustrating the configuration of a stacked memory chip provided with functional circuits. Fig.24 is a plan view of a stacked memory chip in which scribe lines are provided between memory elements in the first embodiment of the present invention. Fig.25 is a plan view illustrating the configuration of a stacked memory chip according to a second embodiment of the present invention. Fig.26 is a cross-sectional view illustrating a configuration in which stacked memory chips are stacked in multiple stages in the third embodiment of the present invention. Fig.27 is a plan view illustrating the configuration of a stacked memory chip according to a fourth embodiment of the present invention. Fig.28 is a plan view illustrating the configuration of an SoC chip and a plan view illustrating the configuration of a stacked memory chip according to a fourth embodiment of the present invention. Fig.29 is a plan view illustrating a schematic configuration of another stacked memory chip according to the fourth embodiment of the present invention. Fig.30 is a plan view of a stacked memory chip for explaining the data transfer path in the stacked memory chip according to the first embodiment of the present invention. Fig.31 is a plan view illustrating a schematic configuration of a stacked memory chip according to a fifth embodiment of the present invention. Fig.32 is a plan view schematically illustrating a stacked memory chip for explaining the data transfer path in the stacked memory chip according to the fifth embodiment of the present invention. Fig.33 is a schematic plan view of the stacked memory chip according to the fifth embodiment of the present invention when the memory region is divided and used. Fig.34 is a plan view schematically illustrating a stacked memory chip according to a fifth embodiment of the present invention, in which the stacked memory chip has a hybrid structure in which a two-dimensional mesh structure and a tree-like structure are combined. Fig.35 is a plan view schematically illustrating a stacked memory chip according to a fifth embodiment of the present invention in which the switch fabrics are arranged in multiple layers. Fig.36 is a plan view illustrating the configuration of a stacked memory chip according to a sixth embodiment of the present invention. Fig.37 is a plan view illustrating the configuration of a stacked memory chip according to a seventh embodiment of the present invention. Fig.38 is a cross-sectional view schematically illustrating a stacked memory chip and ROM according to an eighth embodiment of the present invention. Fig.39 is a plan view illustrating a configuration of an SoC chip according to a ninth embodiment of the present invention. Fig.40 is a plan view illustrating a configuration of a control signal generating unit of an SoC chip according to a ninth embodiment of the present invention. Fig.41 is a cross-sectional view schematically illustrating the configuration in which the wiring member according to the 10 th embodiment of the present invention is disposed, a plan view illustrating the configuration of the stacked memory chip, and a plan view illustrating the configuration of the SoC chip and the wiring member. Fig.42 is a plan view illustrating the configuration of the SoC chip and the wiring member according to the 10 th embodiment of the present invention. Fig.43 is a cross-sectional view of a

semiconductor integrated circuit device according to a 11-th embodiment of the present invention. Fig.44 is a process diagram for explaining the method for forming bump electrodes in the semiconductor integrated circuit device according to the 11 th embodiment of the present invention. Fig.45 is a cross-sectional view for explaining a method for manufacturing a semiconductor integrated circuit device according to a 12-th embodiment of the present invention. Fig.46 is a cross-sectional view for explaining a method for manufacturing a semiconductor integrated circuit device according to a 13-th embodiment of the present invention. Fig.47 is a cross-sectional view of another semiconductor integrated circuit device according to a 11-th embodiment of the present invention. Fig.48 is a cross-sectional view of yet another semiconductor integrated circuit device according to a 11-th embodiment of the present invention. Fig.49 is a plan view illustrating a configuration of a related SoC chip.

REFERENCE SIGNS LIST

[0007] 1 SoC chip 2 stacked memory chip 3 A ~ 3 D logic macro 4 a ~ 4 h memory region 5 memory element 6 A , 6 B , 6 C , 8 a inter-chip I / O portion 7 A , 7 B input/output port 9 scribe line 10 through-wiring 30 clock supply source 31 clock output portion 50 SRAM macro 51 inter-chip I / O unit 52 switch fabric 53 configuration register 54 clock input unit 55 ~ 60 wiring 61 ~ 64 connection network 65 crossbar switch 70 control signal input Unit 80 ROM81 Electrode 82 Bonding wire 83 substrate 100 Control signal generator 101 Configuration Request Signal 102 Configuration Control Signal 103 Configuration Acquisition Signal No.110 Configuration request arbitration unit 120 control signal processing unit 130 control signal output unit 200 interposer 210 SoC in-chip wiring 220 in-interposer arrangement Line 500 SRAM Memory Cell 501 Address Decoder 502 Word Line Driver 503 Write Buffer 504 Read Buffer 505 sense amplifier 520 n , 520 s , 520 w , 520 e , 520ram , 520io transfer gate switch 530 ~ 532 register 533 selectors 600 and 700, 710 semiconductor integrated circuit device 601, 602 multilayer wiring layer 603, 604 electrode pad 605, 606 bump electrode 607 LOR resist 608 PMMA resist 609 gold (Au) 610 mounting stage 620 mounting head 630 sealing resin 701 inductor 702 insulating material 711 capacitance pad

BEST MODE

[0008] Embodiments of the present invention will be described below with reference to the drawings. [principle of invention] Fig. 1 A is a plan view illustrating a representative example of the configuration of an SoC chip and a stacked memory chip according to an embodiment of the invention, and Fig. 1 B is a cross-sectional view schematically illustrating the SoC chip and stacked memory chip after flip chip mounting. Note that in Fig. 1 A, the stacked memory chip 2 is illustrated with the face facing the SoC chip 1 facing upward when flip chip mounting. A logic macro 3 A , 3 B , 3 C , 3 D is disposed within the SoC chip 1, and a memory region 4 a , 4 b , 4 c , 4 d is disposed within the stacked memory chip 2. Chip surfaces of the SoC chip 1 and the stacked memory chip 2 are connected by

wires by flip chip mounting. In this flip chip implementation, the logic macro 3 A and the memory area 4 a face to face, the logic macro 3 B and the memory area 4 b face to face, the logic macro 3 C and the memory area 4 c face to face, and the logic macro 3 D and the memory area 4 d face to face. In this way, the inter-chip I / O portion 6 A of the logic macro 3 A is connected to the inter-chip I / O portion 8 a of the memory region 4 a. In a representative example of the present invention, by making the SoC chip 1 and the stacked memory chip 2 separate chips, memory is not disposed between the logical macros in the SoC chip 1, and the logical macros approach each other, so it is possible to reduce the transmission delay between the logical macros. In Fig. 1 A, 7 A is an I/O port of logic macro 3 A connected to I/O port 7 B of logic macro 3 B. A plurality of memory elements 5, each provided with a memory macro having a small memory capacity and an inter-chip I / O portion, are two-dimensionally arranged within the stacked memory chip 2. Between the memory macro in one memory element 5 and the memory macro in another memory element 5, between the memory macro in the memory element 5 and the same inter-chip I / O portion in the memory element 5, And wiring for transmitting write data, read data, address signals, and commands is connected between the memory in the memory element 5 and the inter-chip I / O portion in another memory element 5, but the connections can be disconnected by a switch described below. Therefore, from among the multiple inter-chip I / O units two-dimensionally arranged within the stacked memory chip 2, it is possible to select the inter-chip I / O unit of the logic macro to which the SoC chip 1 is to be connected, so it is also possible to reduce the transmission delay between the logic macro and the memory region. In the example of Fig. 1 A, the inter-chip I / O portion 8 a of the stacked memory chip 2 is disposed directly above and connected to the inter-chip I / O portion 6 A of the logic macro 3 A at the time of flip chip mounting. The memory region that can be accessed from the inter-chip I / O portion of the stacked memory chip 2 can be selected to have an arbitrary number of bits, words, and ports depending on the combination of the memory elements 5 arranged two-dimensionally. Also, the memory region 4 a , 4 b , 4 c , 4 d is configured by combining a plurality of memory elements 5. In the present invention, even if the function of the SoC has changed, it is not necessary to newly reconstruct the stacked memory chip 2, and it is possible to change the configuration of the memory region by changing the combination of the memory elements 5, so it is possible to accommodate changes in the function of the SoC. [First Embodiment] Next, embodiments of the present invention will be described in detail with reference to the drawings. Fig.2 is a plan view illustrating the configuration of a stacked memory chip 2 according to the first embodiment of the present invention, and is an enlarged plan view illustrating the configuration of one memory element 5 in the stacked memory chip 2. In the example illustrated in Fig.2, a total of 64 memory elements 5, eight vertical x eight horizontal, are two-dimensionally arranged within the stacked memory chip 2. As illustrated in Fig.2, each of the memory elements 5 includes an SRAM macro 50, which is a 16-bit and 1 k-word memory macro, an inter-chip I / O unit 51, a switch fabric 52 that

switches data wiring between the memory elements, and A configuration register 53 for storing a configuration of a memory region in advance and for switching wiring switches of the switch fabric 52; and a clock input section 54 for inputting a synchronization clock from a logical macro of the SoC chip 1. Also, each of the memory elements 5 has interconnections 55 ~ 58 for transferring signals to and from adjacent memory elements 5 in four directions. In the example of Fig.2, the interconnection 55 is an interconnection connected to the adjacent memory element 5 in the upper direction, the interconnection 56 is an interconnection connected to the adjacent memory element 5 in the lower direction, the interconnection 57 is an interconnection connected to the adjacent memory element 5 in the left direction, and the interconnection 58 is an interconnection connected to the adjacent memory element 5 in the right direction. Further, wiring 59 connects the SRAM macro 50 and the switch fabric 52, and wiring 60 connects the inter-chip I / O unit 51 and the switch fabric 52. The signals transferred between the memory elements 5 include 16-bit write data WD, 16-bit read data RD, and A total 16-bit address signal ADR of a 6-bit memory element address signal for specifying a memory element 5 to be accessed from among all the 64 memory elements 5 and a 10-bit word address signal for specifying a word address in the SRAM macro 50; There is a 1-bit command CE for instructing a read operation and a write operation, and a 1-bit command WE for specifying either a read operation or a write operation, and a total of 50 bits are required. Hereinafter, the signals exchanged with the adjacent memory element 5 in the upper direction are denoted by "n" as an index, the signals exchanged with the adjacent memory element 5 in the lower direction are denoted by "s" as an index, and the signals exchanged with the adjacent memory element 5 in the left direction are denoted by "w" as an index, Signals exchanged between adjacent memory elements 5 to the right are denoted by "e" as subscripts, and signals exchanged between SRAM macro 50 and switch fabric 52 are denoted by "ram" as subscripts; The signal exchanged between the inter-chip I / O unit 51 and the switch fabric 52 is denoted by "io" as an index. These signals are transferred via the switch fabric 52 to other memory elements 5 adjacent to each other in the up, down, left, and right directions, as well as the SRAM macro 50 and inter-chip I / O unit 51 within the memory elements 5. Fig.3 is a block diagram illustrating a circuit configuration of the SRAM macro 50. Within the SRAM macro 50 are provided SRAM memory cells 500 in a 1 k word 16 bit configuration. Also, in the SRAM macro 50, an address decoder 501 and a word line driver 502 are provided for controlling access to a memory cell 500 corresponding to a write operation to the memory cell 500 and a read operation from the memory cell 500, Furthermore, a write buffer 503 for transmitting write data to the memory cell 500, a read buffer 504 for transmitting read data from the memory cell 500, and a sense amplifier 505 for amplifying data are provided. As described above, the address signal ADR includes a total of 16 bits of a 6-bit memory element address signal for specifying the memory element 5 to be accessed from among a total of 64 memory elements 5, eight vertical by eight horizontal columns, and a 10-bit word address signal for specifying the word

address in the SRAM macro 50. Among these, when the 6-bit memory element address matches its own memory element address preset in the control unit 506, all circuits at a later stage than the control unit 506, In other words, address decoder 501, word line driver 502, write buffer 503, read buffer 504, and sense amplifier 505 are activated. Then, a 10-bit word address signal included in address signal ADR is output to address decoder 501. Address decoder 501 causes word line driver 502 to select the word line corresponding to the specified word address. As a result, the memory cell 500 corresponding to the specified word address is selected, and a write operation or a read operation is performed on the selected memory cell 500. Fig.4 is a circuit diagram illustrating a configuration of the switch fabric 52. However, in Fig.4, only a circuit portion of a switch configured to control the read data RD is illustrated. The circuit of the switch that controls the writing data WD, the address signal ADR, the command CE, and the command WE can also be configured in the same manner as in Fig.4. The 520 n , 520 s , 520 w , 520 e , 520ram , 520io is a transfer gate switch including a transistor. The transfer gate switch 520 n turns the transmission of the read data RDn to and from the upper adjacent memory element 5 in Fig. 2 (B) on the basis of the selection signal CINn. The transfer gate switch 520 s turns on and off the transmission of the read data RDs to and from the adjacent memory element 5 on the lower side in Fig. 2 (B) in response to the selection signal CINs. The transfer gate switch 520 w turns the transmission of the read data RDw to and from the adjacent memory element 5 to the left in Fig. 2 (B) on the basis of the selection signal CINw. The transfer gate switch 520 e turns the transmission of the read data RDw to and from the adjacent memory element 5 to the right in Fig. 2 (B) on the basis of the selection signal CINe. The transfer gate switch 520ram turns on and off the transmission of the read data RDram to and from the SRAM macro 50 in the same memory element 5 in accordance with the selection signal CINram. The transfer gate switch 520io turns on and off the transmission of the read data RDio to and from the inter-chip I / O unit 51 in the same memory element 5 in response to the selection signal CINio. In this way, the connection can be turned on or off between the memory element 5, the SRAM macro 50, and the inter-chip I / O portion 51 in all directions using the transfer gate switch 520 n , 520 s , 520 w , 520 e , 520ram , 520io. The selection signal CINn , CINs , CINe , CINw , CINram , CINio is sent from the configuration register 53. Fig.5 is a block diagram illustrating a configuration of the configuration registers 53, and Fig.6 is a diagram illustrating a connection between the configuration registers 53 among a plurality of memory elements 5. However, in the example illustrated in Fig.6, a case is illustrated in which there are a total of 16 memory elements 5 in the stacked memory chip 2, namely 4 vertical x 4 horizontal. The SoC chip 1 sends a configuration control signal corresponding to the memory configuration to be used, specifically the 6-bit selection signal CINn , CINs , CINe , CINw , CINram , CINio described with reference to Fig.4, to each of the memory elements 5 of the stacked memory chip 2. In this embodiment, as illustrated in Fig.6, the input part of the configuration control signal from the SoC chip 1 to the stacked memory chip 2 is set as a single location, and the

configuration control signal is transmitted to the first memory element 5 therefrom. hereinafter, the configuration control signal is sequentially transmitted to the adjacent memory element 5 for each cycle of the configuration register clock Cclk. After each of the configuration control signals is sent to all of the memory elements 5, the configuration control signals are stored in the configuration register 53. The control signal output means (not illustrated) of the SoC chip 1 sends a configuration control signal corresponding to the desired memory configuration to the corresponding memory element 5 of the stacked memory chip 2. In this way, it is possible to store an independent configuration control signal for each memory element 5 in the configuration register 53 of each memory element 5, and configure a desired memory region within the stacked memory chip 2. In order to switch the memory configuration of the stacked memory chip 2, the configuration control signal from the SoC chip 1 can be converted to a new configuration and re-sent. In a case where a register is provided in the configuration register 53 so that several types of configuration control signals set in the configuration register 53 can be stored for each memory element, the memory configuration can be immediately switched by switching a plurality of types of configuration control signals. In the example illustrated in Fig.5, three sets of 6-bit registers 530 ~ 532 (storage means) are provided in one configuration register 53. Accordingly, three types of configuration control signals corresponding to the three patterns of memory configurations can be stored, and the memory configurations can be switched by switching the configuration control signals output to the switch fabric 52 with the selector 533 (selection unit) in the subsequent stage. The control signal of the selector 533 can be given for each memory element 5 from the control signal output means of the SoC chip 1. Note that Fig.5 illustrates only a circuit portion configured to switch a configuration control signal supplied to a switch configured to control the read data RD among the switches of the switch fabric 52. A circuit configured to switch a configuration control signal supplied to a switch configured to control the writing data WD, the address signal ADR, the command CE, and the command WE can also be configured in the same manner as in Fig.5. The inter-chip I / O unit 51 inputs and outputs communication data between the logical macros of the SoC chip 1 and the memory elements 5 of the stacked memory chip 2. The inter-chip I / O unit 51 includes 16 input buffers for 16-bit write data WDio, 16 output buffers for 16-bit read data RDio, an input buffer for a total of 16-bit address signals ADRio of 6-bit memory element address signals and 10-bit word address signals; A total of 50 buffers are provided: one input buffer for a 1-bit command CEio for instructing a read operation and a write operation; and one input buffer for a 1-bit command WEio for specifying either a read operation or a write operation. The inter-chip wiring of the inter-chip I / O portion 51 connects the pads between the SoC chip 1 and the stacked memory chip 2 using the vias of the normal chip in-plane wiring as pads. Examples of the method of connecting pads to each other include a method of thermocompression bonding with solder balls interposed therebetween, or a method of forming and crimping a metal bump of gold or the like. The clock input unit 54 is an inter-chip input buffer for receiving a

clock transmitted from a logic macro for synchronization with the logic macro of the SoC chip 1. The received clock is sent to the SRAM macro 50 in the memory element 5. Next, the configuration of the memory region using the memory element 5 will be described. Each memory element 5 can operate as an independent memory region using the SRAM macro 50 and inter-chip I / O portion 51 inside the memory element 5. When the interconnection to all the memory elements 5 adjacent to each other in the up, down, left, and right directions is turned off, each of the memory elements 5 becomes an independent memory region 4 a ~ 4 h of 16 bits and 1 k words, as illustrated in Fig.7. However, in Fig.7, of the 64 memory elements 5, only 8 memory elements 5 are illustrated. In Fig.7, the wiring line in which the connection is turned on by the switch fabric 52 is represented by a solid line, and the wiring line in which the connection is turned off by the switch fabric 52 is represented by a dashed line. As is clear from Fig.7, in each of the memory elements 5, the interconnection 55 between the upper adjacent memory element 5, the interconnection 56 between the lower adjacent memory element 5, and the interconnection 57 between the left adjacent memory element 5; All of the transfer gate switches of the interconnection 58 to and from the adjacent memory element 5 to the right are off, and the transfer gate switches of the interconnection 59 to and from the SRAM macro 50 and the interconnection 60 to and from the inter-chip I / O portion 51 are on. When all of the memory elements 5 of the stacked memory chip 2 are operated independently in this manner, it is possible to access 64 memory regions to the maximum 64 logical macros of the SoC chip 1 to operate in parallel. By combining the memory elements 5, it is possible to increase the memory capacity of one memory region. Turning on the switch fabric 52 to combine the four memory elements 5, for example, as shown in Fig.8, results in a 16-bit, 4 k-word memory region 4 a , 4 b. Among the four memory elements 5-1,5-2,5-5,5-6 constituting the memory region 4 a, the transfer gate switch of the interconnection 56,57 is turned off, and the transfer gate switch of the interconnection 55,58,59,60 is turned on. In the memory element 5-2 on the lower right, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In the upper left memory element 5-5, the transfer gate switch of the interconnection 55,57,60 is off, and the transfer gate switch of the interconnection 56,58,59 is on. In the upper right memory element 5-6, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In this way, all the SRAM macros 50 of the four memory elements 5-1,5-2,5-5,5-6 are connected to form one memory region 4 a. Of these memory elements 5-1,5-2,5-5,5-6, the inter-chip I / O portion 51 used is only the inter-chip I / O portion 51-1 of the memory element 5-1. Similarly, among the four memory elements 5-3,5-4,5-7,5-8 that constitute the memory region 4 b, in the lower left memory element 5-3, the transfer gate switch of the interconnection 56,57 is off, and the transfer gate switch of the interconnection 55,58,59,60 is on. In the memory element 5-4 on the lower right, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on.

In the upper left memory element 5-7, the transfer gate switch of the interconnection 55,57,60 is off, and the transfer gate switch of the interconnection 56,58,59 is on. In the upper right memory element 5-8, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. Of these memory elements 5-3,5-4,5-7,5-8, the inter-chip I / O unit 51 is only the inter-chip I / O unit 51-3 of the memory element 5-3. It is also possible to change the number of input and output bits of the memory region. Fig.9 is a plan view illustrating the configuration of the SoC chip 1 and the stacked memory chip 2 when the memory region 4 a accessed by the logical macros 3 A is 32-bit 4 k word. Note that in Fig.9, the stacked memory chip 2 is illustrated with the face facing the SoC chip 1 facing upward when flip chip mounting. As in the case of Fig. 1 A, the chip surfaces of the SoC chip 1 and the stacked memory chip 2 are connected by wires by flip chip mounting. In this flip chip implementation, the logic macro 3 A and the memory area 4 a face to face, and the inter-chip I / O portion 6 A of the logic macro 3 A is connected with two inter-chip I / O portions 8 a of the memory area 4 a. When the memory region 4 a that accesses the logic macro 3 A of the SoC chip 1 is set to 32-bit and 4 k words as illustrated in Fig.9, eight 16-bit and 1 k-word memory elements 5 are combined to form one memory region 4 a as illustrated in Fig.10. The memory region 4 a includes memory regions 4 a-1 and 4 a-2. The memory region 4 a-1 is constituted of memory elements 5-1 ~ 5-3,5-5, and the memory region 4 a-2 is constituted of memory elements 5-4,5-6 ~ 5-8. Of the four memory elements 5-1 ~ 5-3,5-5 constituting the 16-bit and 4 k-word memory region 4 a-1, the transfer gate switch of the interconnection 55,57,60 is turned off, and the transfer gate switch of the interconnection 56,58,59 is turned on. In the memory element 5-2, the transfer gate switch of the interconnection 55,66,60 is off, and the transfer gate switch of the interconnection 57,58,59 is on. In the memory element 5-3, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In the memory element 5-5, the transfer gate switch of the interconnection 56,57,58 is off, and the transfer gate switch of the interconnection 55,59,60 is on. In this way, all the SRAM macros 50 of the four memory elements 5-1 ~ 5-3,5-5 are connected to form one memory region 4 a-1. Of these memory elements 5-1 ~ 5-3,5-5, the inter-chip I / O portion used is only the inter-chip I / O portion 51-5 of the memory element 5-5. This inter-chip I / O portion 51-5 constitutes one of the two inter-chip I / O portions 8 a in Fig.9. Similarly, of the four memory elements 5-4,5-6 ~ 5-8 that constitute the 16-bit and 4 k-word memory region 4 a-2, the transfer gate switch of the interconnection 55,57,58,60 is off and the transfer gate switch of the interconnection 56,59 is on in the memory element 5-4. In the memory element 5-6, the transfer gate switch of the interconnection 55,56,57 is off, and the transfer gate switch of the interconnection 58,59,60 is on. In the memory element 5-7, the transfer gate switch of the interconnection 55,56,60 is off, and the transfer gate switch of the interconnection 57,58,59 is on. In the memory element 5-8, the transfer gate switch of the interconnection 56,58,60 is off, and the transfer gate switch of the

interconnection 55,57,59 is on. In this way, all the SRAM macros 50 of the four memory elements 5-4,5-6 ~ 5-8 are connected to form one memory region 4 a-2. Of these memory elements 5-4,5-6 ~ 5-8, the inter-chip I / O portion used is only the inter-chip I / O portion 51-6 of the memory element 5-6. This inter-chip I / O portion 51-6 constitutes the other one of the two inter-chip I / O portions 8 a in Fig.9. Of the eight memory elements 5-1 ~ 5-8, the inter-chip I / O unit 51-5,51-6 of the memory element 5-5,5-6 is selected because the inter-chip I / O unit 51-5,51-6 is positioned directly above the inter-chip I / O unit 6 A of the logic macro 3 A at the time of flip chip mounting. Thus, by combining the 16-bit, 4 k-word memory regions 4 a-1,4 a-2, it is possible to configure the 32-bit, 4 k-word memory region 4 a. Next, the write operation and read operation performed between the SoC chip 1 and the stacked memory chip 2 will be described. When writing data into the memory, a memory element address signal, a word address signal, and a writing command CE , WE are input from the logic macro of the SoC chip 1 to the inter-chip I / O portion of the stacked memory chip 2. One of the 64 memory elements 5 is specified by the memory element address signal, and the switch fabric 52 is routed at each memory element 5 so that the write data WD is transferred to the SRAM macro 50 of the specified memory element 5. In the selected memory element 5, the write data WD is written to the SRAM memory cell 500 at the word address specified by the word address signal. When reading data from the memory, a memory element address signal, a word address signal, and a read command CE , WE are input from the logic macro of the SoC chip 1 to the inter-chip I / O portion of the stacked memory chip 2. Read data RD is output from the memory element 5 selected by the memory element address signal to the logic macro of the SoC chip 1 via the inter-chip I / O portion via the path opposite to the writing. Next, a clock synchronization method between the memory of the stacked memory chip 2 and the logic macro of the SoC chip 1 will be described. In the SoC chip 1, there are a large number of flip-flop circuits, which are register memories, and synchronous clocks are distributed by a clock tree having a uniform delay from a clock supply source to all of the flip-flop circuits. An equal delay wiring is realized by adding up to the clock input of the SRAM macro 50 in the memory element 5 of the stacked memory chip 2 to this configuration of the clock tree. In other words, as shown in FIGS. 11 A and 11 B, the transfer delay T (FF) from the clock source 30 of the logic macro 3 of the SoC chip 1 to the clock input of the flip-flop FF; The transmission delay T (SRAM) from the clock supply source 30 of the SoC chip 1 to the clock input of the SRAM macro 50 via the clock input unit 54 of the memory element 5 of the stacked memory chip 2 may be equal. A clock is supplied to the clock input 54 of the memory element 5 via the clock output 31 of the logic macro 3. In other words, during flip chip mounting, the clock input unit 54 is connected to the clock output unit 31 located directly below. The equal delay wiring is realized by adjusting a transmission delay T (SOC _ OUT) from the clock supply source 30 to the clock output unit 31 of the SoC chip 1. In other words, the transmission delay T (CHIP _ CHIP) between the SoC chip 1 and the stacked memory chip 2, and the transmission delay T (RAM _ IN) from the clock input unit 54 within the memory

element 5 of the stacked memory chip 2 to the clock input of the SRAM macro 50 are known unique to the memory chip. The transmission delay T (SOC _ OUT) is adjusted when generating the clock tree for the SoC chip 1 so that the following equation is satisfied: T (FF) = T (SRAM) = T (SOC _ OUT) + T (CHIP _ CHIP) + T (RAM _ IN) (1) T (SOC _ OUT) = T (FF)-{T (CHIP _ CHIP) + T (RAM _ IN)} · (2) The clock input to the clock input unit 54 of the memory element 5 can have a different frequency in accordance with the logical macro. In other words, on the stacked memory chip 2, it is also possible for synchronization clocks of different frequencies to exist for each memory element 5 or for each memory region. The memory region within the stacked memory chip 2 can be reconfigured by the SoC chip 1 in combination. In this case, only one memory configuration may be configured once by the SoC chip 1, so the configuration register 53 of the memory element 5 illustrated in Fig.5 may include only one set of 6-bit registers. Next, after the manufacture of the stacked memory chip 2, the number and position of the memory region and inter-chip I / O are configured according to the SoC chip 1 will be described using FIGS.12, 13, 14, and 15. In Fig.12, Fig.13, Fig.14, and Fig.15, the stacked memory chip 2 is illustrated with the face facing the SoC chip 1 facing up during flip chip mounting, the same as in Fig. 1 A. Additionally, in FIGS.12, 13, 14, and 15, similar to Fig.7, wiring lines in each of the memory elements 5 turned on by the switch fabric 52 are represented by solid lines, and wiring lines in which the connection is turned off by the switch fabric 52 are represented by dashed lines. Fig.12 illustrates a case in which one memory region 4 a of the stacked memory chip 2 is constituted by memory elements 5-1,5-2,5-5,5-6, and another memory region 4 b is constituted by memory elements 5-3,5-4,5-7,5-8. The configuration of the memory region 4 a , 4 b of the stacked memory chip 2 of Fig.12 is the same as that illustrated in Fig.8. The logic macro 3 A of the SoC chip 1 accesses the memory region 4 a via the inter-chip I / O portion 6 A, and the logic macro 3 B accesses the memory region 4 b via the inter-chip I / O portion 6 B. In the case of Fig.12, the inter-chip I / O portion 51-1 in the memory element 5-1 located directly above the inter-chip I / O portion 6 A during flip chip mounting is selected as the inter-chip I / O portion of the memory area 4 a that exchanges data with the logic macro 3 A. Also, as the inter-chip I / O unit of the memory area 4 b that exchanges data with the logic macro 3 B, the inter-chip I / O unit 51-3 in the memory element 5-3 positioned directly above the inter-chip I / O unit 6 B is selected during flip chip mounting. On the other hand, in the SoC chip 1 that combines with the stacked memory chip 2, as illustrated in Fig.13, it is conceivable that the region of the logic macro 3 A is large and the region of the logic macro 3 B is small. When the memory region 4 a requires a larger capacity than the capacity of the memory region 4 a required by the logic macro 3 A and the capacity of the memory region 4 b required by the logic macro 3 B, As illustrated in Fig.13, the memory region 4 a is constituted by memory elements 5-1,5-2,5-3,5-5,5-6,5-7, and the memory region 4 b is constituted by memory elements 5-4,5-8. Of the six memory elements 5-1,5-2,5-3,5-5,5-6,5-7 constituting the memory region 4 a, the transfer gate switch of the interconnection 56,57 is off and the transfer gate switch

of the interconnection 55,58,59,60 is on in the memory element 5-1. In the memory element 5-2,5-6, the transfer gate switch of the interconnection 55,56,60 is off, and the transfer gate switch of the interconnection 57,58,59 is on. In the memory element 5-3,5-7, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. Of the two memory elements 5-4,5-8 constituting the memory region 4 b, in the memory element 5-4, the transfer gate switch of the interconnection 56,57,58 is off, and the transfer gate switch of the interconnection 55,59,60 is on. In the memory element 5-8, the transfer gate switch of the interconnection 55,57,58,60 is off, and the transfer gate switch of the interconnection 56,59 is on. As a result, the memory region 4 a has three times the memory capacity of the memory region 4 b. However, the ratio of the number of memory elements 5 constituting the memory region 4 a , 4 b is not limited to 3: 1 of Fig.13, and can be set in accordance with the SoC chip 1. The inter-chip I / O portion of the memory region 4 a that exchanges data with the logic macro 3 A may be the inter-chip I / O portion 51-1 within the same memory element 5-1 as in Fig. 12 (A). The inter-chip I / O portion of the memory region 4 b that exchanges data with the logic macro 3 B is selected from the inter-chip I / O portion of the memory element 5-4 or the memory element 5-8. In Fig.13, the inter-chip I / O portion 51-4 of the memory element 5-4 is selected. In addition, instead of Fig.13, as illustrated in Fig.14, the memory region 4 a may be constituted by memory elements 5-1,5-2,5-3,5-4,5-5,5-6, and the memory region 4 b may be constituted by memory elements 5-7,5-8. Of the six memory elements 5-1,5-2,5-3,5-4,5-5,5-6 constituting the memory region 4 a, the transfer gate switch of the interconnection 56,57 is off and the transfer gate switch of the interconnection 55,58,59,60 is on in the memory element 5-1. In the memory element 5-2,5-3,5-6, the transfer gate switch of the interconnection 55,56,60 is off, and the transfer gate switch of the interconnection 57,58,59 is on. In the memory element 5-4, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In the memory element 5-5, the transfer gate switch of the interconnection 55,57,60 is off, and the transfer gate switch of the interconnection 56,58,59 is on. Of the two memory elements 5-7,5-8 constituting the memory region 4 b, in the memory element 5-7, the transfer gate switch of the interconnection 55,56,57 is off, and the transfer gate switch of the interconnection 58,59 is on. In the memory element 5-8, the wiring line 55,56,58 transfer gate switch is off, and the wiring line 57,59,60 transfer gate switch is on. The memory capacity of the memory region 4 a , 4 b in Fig.14 is the same as the memory capacity of the memory region 4 a , 4 b in Fig.13. The inter-chip I / O portion of the memory region 4 a that exchanges data with the logic macro 3 A may be the inter-chip I / O portion 51-1 within the same memory element 5-1 as in Fig.13. Also, the inter-chip I / O portion of the memory region 4 b that exchanges data with the logic macro 3 B can be selected from the inter-chip I / O portions of the memory element 5-7 and the memory element 5-8. However, the inter-chip I / O portion 51-8 of the memory element 5-8 positioned directly above the logic macro 3 B shortens the inter-chip wiring and can

reduce the delay in inter-chip transmission, so the inter-chip I / O portion 51-8 of the memory element 5-8 is selected as the inter-chip I / O portion of the memory region 4 b that exchanges data with the logic macro 3 B. In this way, in this embodiment, by disposing a plurality of interchip I / O portions in two dimensions within the stacked memory chip 2, it is possible to select an interchip I / O portion near the logical macro of the SoC chip 1 to which it is connected. Also, as illustrated in Fig.15, when the logic macro 3 C of the SoC chip 1 is added, it is possible to reconfigure the memory region of the stacked memory chip 2 so as to add the memory region 4 c. The logic macro 3 C accesses the memory region 4 c via the inter-chip I / O portion 6 C. In Fig.15, the memory region 4 a is constituted by memory elements 5-1,5-2,5-5,5-6, the memory region 4 b is constituted by memory elements 5-3,5-4, and the memory region 4 c is constituted by memory elements 5-7,5-8. Of the four memory elements 5-1,5-2,5-5,5-6 constituting the memory region 4 a, the transfer gate switch of the interconnection 56,57 is off, and the transfer gate switch of the interconnection 55,58,59,60 is on. In the memory element 5-2,5-6, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In the memory element 5-5, the transfer gate switch of the interconnection 55,57,60 is off, and the transfer gate switch of the interconnection 56,58,59 is on. Of the two memory elements 5-3,5-4 constituting the memory region 4 b, in the memory element 5-3, the transfer gate switch of the interconnection 55,56,57 is off, and the transfer gate switch of the interconnection 58,59,60 is on. In the memory element 5-4, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. Of the two memory elements 5-7,5-8 constituting the memory region 4 c, in the memory element 5-7, the transfer gate switch of the interconnection 55,56,57,60 is off, and the transfer gate switch of the interconnection 58,59 is on. In the memory element 5-8, the transfer gate switch of the interconnection 55,56,58 is off, and the transfer gate switch of the interconnection 57,59,60 is on. The inter-chip I / O portion of the memory region 4 a that exchanges data with the logic macro 3 A may be the inter-chip I / O portion 51-1 within the same memory element 5-1 as in Fig.14. Also, the inter-chip I / O unit 51-3 of the memory element 5-3 is selected as the inter-chip I / O unit of the memory region 4 b that exchanges data with the logic macro 3 B, and the inter-chip I / O unit 51-8 of the memory element 5-8 is selected as the inter-chip I / O unit of the memory region 4 c that exchanges data with the logic macro 3 C. Also, in this embodiment, several patterns of the configuration control signals stored in the configuration register 53 of each memory element 5 of the stacked memory chip 2 are prepared in advance and switched during chip use, making it possible to dynamically re-configure the memory region. FIGS.16 and 17 are plan views illustrating the configuration of the SoC chip 1 and the stacked memory chip 2 in the case where the logical macros of the SoC chip 1 include both operating and inactive macros. In FIGS.16 and 17, similar to Fig. 1 A, the stacked memory chip 2 is illustrated with the face facing the SoC chip 1 facing upward at the time of flip chip mounting. Also, Fig.16 illustrates a case where the logic macro 3 A is in

operation and the logic macro 3 B is in suspension, and Fig.17 illustrates a case where the logic macro 3 A is in suspension and the logic macro 3 B is in operation. When the logic macro 3 A is in operation and the logic macro 3 B is inactive as in the example of Fig.16, by causing the configuration register 53 of each memory element 5 to select a configuration control signal in accordance with an instruction from the control signal output means of the SoC chip 1, The number of memory elements 5 constituting the memory region 4 b is reduced, and the number of memory elements 5 constituting the memory region 4 a is increased. This makes it possible to increase the memory capacity of the memory region 4 a accessed by the logical macros 3 A during operation. On the other hand, when the logic macro 3 A is inactive and the logic macro 3 B is active as in the example of Fig.17, by causing the configuration register 53 of each memory element 5 to select the corresponding configuration control signal in accordance with an instruction from the control signal output means of the SoC chip 1, The number of memory elements 5 constituting the memory region 4 a is reduced, and the number of memory elements 5 constituting the memory region 4 b is increased. This makes it possible to increase the memory capacity of the memory region 4 b accessed by the logical macros 3 B during operation. In this way, in this embodiment, by switching the configuration control signal in accordance with the operating conditions of the logical macro of the SoC chip 1, it is possible to dynamically change the memory configuration of the stacked memory chip 2, and it is possible to efficiently use limited memory resources. Also, at this time, by turning off the power of the SRAM macros in the memory region allocated corresponding to the inactive logical macros, it is possible to save power in the stacked memory chip 2. Fig.18 illustrates an example of a configuration of a stacked memory chip 2 that includes a memory region 4 a that opposes the inactive logic macro 3 A. As illustrated in the figure, a power supply connection switch circuit is provided for each SRAM macro 50 of each memory element 5. As a result, the SRAM macro 50 can be powered off individually, and the SRAM macro in the memory region corresponding to the inactive logic macro can be powered off. Note that in the SRAM macro, when the SRAM is powered off, the stored data is erased. If it is necessary to retain data even when inactive, the power supply voltage of the SRAM macro 50 in the inactive memory region can be lowered to a voltage lower than normal, for example, as shown in Fig.19. Further, as illustrated in Fig.20, leakage current may be suppressed by increasing the substrate bias of the transistors configuring the SRAM. Furthermore, by lowering the clock operating frequency of the SRAM macro corresponding to the inactive logic macro, power saving may be achieved. In this embodiment, the SRAM macro 50 in each of the memory elements 5 has a 1 k word and 16 bit configuration, but the present invention is not limited thereto, and any word and bit configuration may be employed. Also, in this embodiment, all of the SRAM macros 50 of the memory element 5 illustrated in Fig.2 are described as 16-bit and 1 k-word SRAM macros of the same type. However, the configuration is not limited to this, and several types of SRAM macros may be mapped. Fig.21 illustrates an example of a stacked memory chip in which different types of SRAM macros (A, B, C, and D) are disposed

in a mixed manner. The SRAM macro (A) can be an underlying SRAM macro with, for example, 16 bits, 1 k words, 1 port, read delay of 4 ns. As the SRAM macro (B), for example, a SRAM macro having different numbers of bits and words of 32 bits, 2 k words, 1 port, and a read delay of 4 ns can be used. The SRAM macro (C) can be, for example, a SRAM macro with a different read delay of 16 bits, 1 k words, 1 port, and a read delay of 2 ns. Furthermore, a SRAM macro with 16 bits, 1 k words, two ports, and a read delay of 4 ns can be used as the memory macro with a different number of ports for the SRAM macro (D). The stacked memory chip 2 in which different types of SRAM macros are arranged will be described in more detail. As illustrated in Fig.22, the SoC chip 1 is provided with, for example, a logical macro of 16-bit processing, along with a logical macro of 32-bit processing, for example, a 32-bit CPU. If the CPU requires a memory region of 32 bits and 8 k words as the memory, 16 SRAM macros are required if the memory region is configured from only the basic SRAM macros (A). In contrast, if the SRAM macro (B) is used, four SRAM macros can be configured. If the number of SRAM macros constituting a single memory region can be reduced, the number of switch fabrics in the memory region can be reduced, so the area of the memory region can be reduced. Also, when a logical macro at a normal operating speed and a logical macro requiring high-speed memory access, for example, an image processing accelerator, are disposed in the SoC chip 1, the memory region can be configured using the SRAM macro (C) having a reading delay of 2 ns as the memory for the accelerator. Furthermore, when a logical macro that needs to be frequently switched between reading and writing to the memory is disposed on the SoC chip 1, such as in a switch router, for example, the memory region can be constituted by the SRAM macro (D). As described above, by using the stacked memory chip 2 in which different types of SRAM macros are arranged, it is possible to ensure a memory region without impairing the memory access performance required by the SoC chip 1. Also, in this embodiment, the memory macro in the memory element 5 was SRAM, but the memory macro may be DRAM. Because the circuit area of the DRAM is smaller than that of the SRAM, the DRAM can be equipped with a larger capacity of memory. Flash memory, non-volatile memory such as MRAM (Magnetoresistive Random Access Memory), ReRAM (Resistive Random Access Memory), or the like may be used as the memory macro in the memory element 5. By using non-volatile memory, it is possible to power down a memory region that is not temporarily used within the stacked memory chip 2, and to enter a power-saving mode. In this embodiment, each of the memory elements 5 that constitute the stacked memory chip 2 was described as including the SRAM macro 50, but this is not a limitation, and functional circuits other than the SRAM macro 50 may be included. Fig.23 illustrates an example of a stacked memory chip 2 provided with a function circuit. A general-purpose CPU, a peripheral circuit, or the like can be used as the functional circuit. The peripheral circuits include, for example, an external memory interface, a serial interface for external high-speed communication, an external wireless interface, a digital-to-analog converter, a power supply controller, a clock generation circuit, and the like. These functional circuits are coupled to

wiring in the memory element 5. These functional circuits are widely used even if the type of SoC chip 1 varies, so they can be formed in advance in the stacked memory chip 2 and mass-produced. As a result, the effect of reducing manufacturing costs can be obtained. Also, in this embodiment, the memory elements 5 are arranged in a two-dimensional array of eight vertical x eight horizontal in the stacked memory chip 2, but the array size may be any other configuration. Also, in this embodiment, wiring between adjacent memory elements is electrically turned on and off by the switch fabric 52 in each of the memory elements 5. In contrast, as illustrated in Fig.24, if scribe lines 9 are provided between the memory elements 5, and it is possible to physically separate the memory elements 5 along the scribe lines 9, it is also possible to arrange the array of memory elements 5 on the entire surface of the wafer, and cut out a memory chip having an array size that corresponds to the required memory capacity from the wafer. [Second Embodiment] Next, a second embodiment of the present invention will be described. Fig.25 is a plan view illustrating the configuration of a stacked memory chip according to a second embodiment of the present invention. In Fig.25, similar to Fig.7, the wiring line in each of the memory elements 5 turned on by the switch fabric 52 is represented by solid lines, and the wiring line in which the connection is turned off by the switch fabric 52 is represented by dashed lines. In this embodiment, the stacked memory chip 2 is a two-port memory having one writing port and two reading ports in a pseudo manner. Of the eight memory elements 5-1 ~ 5-8, in the memory element 5-1, the transfer gate switch of the interconnection 56,57 is off, and the transfer gate switch of the interconnection 55,58,59,60 is on. In the memory element 5-2,5-3,5-6,5-7, the transfer gate switch of the interconnection 55,56,60 is off, and the transfer gate switch of the interconnection 57,58,59 is on. In the memory element 5-4,5-8, the transfer gate switch of the interconnection 55,56,58,60 is off, and the transfer gate switch of the interconnection 57,59 is on. In the memory element 5-5, the transfer gate switch of the interconnection 55,57 is off, and the transfer gate switch of the interconnection 56,58,59,60 is on. When writing data to the stacked memory chip 2, the inter-chip I / O unit 51-1 of the memory element 5-1 is used. In other words, the same writing data WD is written from the SoC chip 1 to the memory element 5-1 ~ 5-8 via the inter-chip I / O unit 51-1. When reading data from the stacked memory chip 2, the inter-chip I / O unit 51-1 of the memory element 5-1 and the inter-chip I / O unit 51-5 of the memory element 5-5 are used. In other words, the read data RD can be read from the memory element 5-1 ~ 5-4 via the inter-chip I / O unit 51-1, and the read data RD can be read from the memory element 5-5 ~ 5-8 via the inter-chip I / O unit 51-5. In this way, the read data RD can be read independently from the memory elements 5-1 ~ 5-4 and 5-5 ~ 5-8. As a result, in this embodiment, a high-speed memory reading operation, such as reading the next memory data without waiting for one memory data to be read, is possible. [Third Embodiment] Next, a third embodiment of the present invention will be described. Fig.26 is a cross-sectional view illustrating a configuration in which the stacked memory chips 2 are stacked in multiple stages in the third embodiment of the

present invention. This embodiment illustrates a configuration in which stacked memory chips 2 are stacked in multiple stages. As illustrated in Fig.26, through wiring 10 that passes through the plurality of stacked memory chips 2 is used so that the plurality of stacked memory chips 2 can be accessed from the SoC chip 1. In this embodiment, the memory region directly above the functional macro of the SoC chip 1 can be extended, so the memory capacity accessed by the functional macro can be increased. [Fourth Embodiment] Next, a fourth embodiment of the present invention will be described. In the first embodiment, as illustrated in Fig.2, the interconnection that couples each of the two-dimensionally arranged memory elements is a connection network having a two-dimensional mesh structure. However, the configuration is not limited thereto, and the connection network 61 having the two-dimensional torus structure illustrated in Fig.27 may also be used. In this case, the memory elements 5 disposed at the left and right ends or the memory elements 5 disposed at the top and bottom ends in Fig.27 can be mutually coupled. Fig.27 illustrates a case where a total of 16 memory elements 5, four vertical by four horizontal, are disposed in the stacked memory chip. By adopting the two-dimensional torus structure, for example, as illustrated in Fig.28, it is possible for the logic macro 3 A located at the edge of the SoC chip 1 to use a memory element that configures a memory region 4 b that is not continuous with the memory region 4 a located at a position opposite the logic macro 3 A, in other words, the memory region 4 b located at the opposite edge. Therefore, unused memory area can be reduced, and a large capacity memory area can be efficiently ensured. Note that the connection network having the two-dimensional torus structure is not limited to that illustrated in Fig.27, and as illustrated in Fig.29, for example, the connection network 62 may be provided with wiring that bypasses and connects one adjacent memory element. In Fig.29, only the switch fabric 52 and the wiring therebetween are illustrated in order to make the wiring between the memory elements 5 easier to see. Referring to the numbers shown in Fig.29, each memory element is coupled 1 and 2, 2 and 3, 3 and 4, or 4 and 1 in both the horizontal and vertical directions. By adopting the connection network 62 having such a two-dimensional torus structure, the wiring distance between the memory elements can be doubled or less than the case where a connection network having a two-dimensional mesh structure is adopted. Therefore, compared to the case in which the memory elements at both ends are coupled to each other as illustrated in Fig.27, delay in signal transmission due to an increase in wiring distance can be suppressed. [Fifth Embodiment] Next, a fifth embodiment of the present invention will be described. In the first embodiment, as illustrated in Fig.2, the interconnection that couples each of the two-dimensionally arranged memory elements is a connection network having a two-dimensional mesh structure. Here, when data is transmitted from the memory element disposed at one end of one memory region to the memory element disposed at the other end, the data is transferred via the switch fabric 52 of each of the memory elements 5. For example, as illustrated in Fig.30, in a case where a memory region constituted by 4 × 4 memory elements is formed, when data is sent from the SRAM macro 50 of the

upper left memory element 5 to the inter-chip I / O portion 51 of the lower right memory element 5, the data passes through seven switch fabrics 52. When switch fabric 52 has the configuration shown in Fig.4, a delay occurs when data passes through the transfer gate switch. Therefore, when the memory region is large, it is desirable to reduce the number of switch fabrics through which data passes. Therefore, in this embodiment, as illustrated in Fig.31, the interconnection network 63 having a tree-like structure is used as the interconnection network 63 that couples each of the memory elements two-dimensionally arranged. In Fig.31, only the switch fabric 52 and the wiring connections therebetween are illustrated in order to make the wiring between the memory elements 5 easier to see. The total number of switch fabrics 52 increases by five, but the increased switch fabric 52 is connected only to the switch fabric 52 and is not directly connected to SRAM macros or inter-chip I / O sections. According to this embodiment, as illustrated in Fig.32, in a case where the memory region constituted by 4 × 4 memory elements is formed, when data is transmitted from the SRAM macro 50 of the upper left memory element 5 to the inter-chip I / O portion 51 of the lower right memory element 5, it is sufficient for the data to only pass through the five switch fabrics 52. Therefore, even when the memory area is large, the delay time when transferring data in the memory area can be shortened. On the other hand, as illustrated in Fig.33, in a case where the memory region is divided into upper and lower portions of the tree-like structure of the connection network 63 and used, when the switch fabric 52 is constituted by a single channel switch, a location where coupling between the memory elements cannot be ensured occurs. For example, in the center switch fabric of Fig.33, connecting wires from the upper left switch fabric and the upper right switch fabric will not connect wires from the lower left switch fabric and the lower right switch fabric. In this case, as illustrated in Fig.34, for example, a connection network 64 having a hybrid structure in which a two-dimensional mesh structure and a tree-like structure are combined can be used. In addition, as illustrated in Fig.35, the switch fabrics 52 may be arranged in multiple in a connection network 63 having a tree-like structure. By adopting such a configuration, even when the memory region is divided above and below the tree-like structure constituting the connection network and used, the connection of all the wiring lines can be ensured. [Sixth Embodiment] Next, a sixth embodiment of the present invention will be described. In the first embodiment, as illustrated in Fig.2, each of the two-dimensionally arranged memory elements is connected by the wiring 55 ~ 60 via the switch fabric 52. In contrast, in this embodiment, as illustrated in Fig.36, a crossbar switch 65 is provided, and each of the memory elements 5 is crossbar coupled. As a result, data can be transmitted and received between all the memory elements 5 by simply passing through a single crossbar switch 65. In the stacked memory chip of the first embodiment, a switch fabric is provided for each memory element, but according to this embodiment, a switch fabric is unnecessary, so the configuration of each memory element can be simplified. Note that a commonly used crossbar switch circuit can be used as the crossbar switch 65, which makes it possible to form a plurality of connections

between two memory elements. [Seventh embodiment] Next, a seventh embodiment of the present invention will be described. In the first embodiment, as illustrated in Fig.6, the configuration control signal sent from the SoC chip is input from one location of the stacked memory chip. In contrast, in this embodiment, the configuration control signals are input from a plurality of locations on the stacked memory chip. Fig.37 illustrates a configuration in which a control signal input section 70 connected to the configuration register 53 is provided for each memory element 5. In the stacked memory chip according to this embodiment, the configuration control signal can be sent from the SoC chip to each of the memory elements 5 in parallel, making it possible to set the configuration control signal in the configuration register 53 of each of the memory elements 5 in a short period of time. Accordingly, even in a case where the configuration register 53 includes only one set of registers, switching of the memory configuration can be completed in a short period of time, and thus the configuration of the configuration register 53 can be simplified. [Eighth Embodiment] Next, an eighth embodiment of the present invention will be described. In the first embodiment, the configuration control signal is sent from the SoC chip to the stacked memory chip, but this is not a limitation, and the configuration control signal may be sent from an external device other than the SoC chip to the stacked memory chip. In this embodiment, as illustrated in Fig.38, an ROM (Read Only Memory) 80 is provided outside the stacked memory chip 2, and the stacked memory chip 2 is configured to read configuration control signals from the ROM80. The connection of the stacked memory chip 2 and the ROM80 can be made by providing electrodes 81 that connect to the stacked memory chip 2 and the ROM80, and connecting the electrodes 81 using bonding wires 82. In this embodiment, first, a device was manufactured in which the stacked memory chip 2 and the SoC chip 1 were configured on the substrate 83. Then, at the time of manufacturing the device or before the device user uses the device, the configuration control signal is written to the ROM80. Next, when starting to use the device, the configuration control signal recorded in the ROM80 is transmitted to the stacked memory chip 2, and a memory region is formed in the stacked memory chip 2 on the basis of the configuration control signal. In this way, according to the present embodiment, the memory region can be directly constituted by a device manufacturer or a device user. Fig.38 illustrates a case where the ROM80 is disposed on the same substrate 83 as the device, but a configuration where the ROM80 is stacked on the device may be employed. In the present embodiment, the configuration control signal is transmitted from the ROM80. however, the configuration control signal is not limited thereto, and a semiconductor device such as an FPGA (Field Programmable Gate Array), an CPU (Central Processing Unit), or another SoC chip may be used. [Ninth embodiment] Next, a ninth embodiment of the present invention will be described. As illustrated in Fig.39, the SoC chip 1 according to the present embodiment includes a control signal generation unit 100. The control signal generation unit 100 generates a control signal for configuring the memory region in accordance with the operating status of the logical macro. The plurality of logical macros 3 mounted on the SoC

chip 1 transmit a configuration request signal 101 to the control signal generation unit 100 in accordance with an operating status of each logical macro 3. The configuration request signal 101 indicates the number of memory elements, which are the size of the memory region required by each logical macro 3. for example, when the number of memory elements is 16 in total, the configuration request signal 101 is a 4-bit signal. As illustrated in Fig.40, the control signal generation unit 100 includes a configuration request arbitration unit 110, a control signal processing unit 120, and a control signal output unit 130. The configuration request arbitration unit 110 receives the configuration request signal 101 from the plurality of logical macros 3, and determines the size of the memory area allocated to each of the logical macros 3, that is, the number of memory elements, in accordance with the priority order of the requests. The control signal processing unit 120 generates the configuration control signal 102 for each memory element necessary to reconfigure the memory region in the stacked memory chip 2 on the basis of the determined size of the memory region. The configuration control signal 102 is sent to the stacked memory chip 2 via the control signal output unit 130. Here, the configuration control signal 102 is a 6-bit signal of CINn, CINe, CINs, CINw, CINram, and CINio serving as a selection signal of the switch fabric of each memory element. For example, in a case where the total number of memory elements is 16, 16 6-bit configuration control signals are required to correspond to the number of memory elements. In this case, the generated configuration control signal can be stored in a register having a 6 × 16-bit configuration, taken out from the register 6-bit at a time in one cycle of the clock, and sent to the stacked memory chip 2 via the control signal output unit 130. The control signal processing unit 120 sends the configuration control signal 102 to the stacked memory chip 2 via the control signal output unit 130, and sends, to each logical macro 3, a configuration acquisition signal 103 indicating the number of memory elements acquired by each logical macro 3 in the memory region of the stacked memory chip 2. The configuration acquisition signal 103 is also a 4-bit signal when the total number of memory elements is 16. To determine the priority order of requests from each logical macro 3, a fixed priority order method, a round robin type method in which the priority order is switched each time, or the like can be used. Also, when assigning the memory regions according to the priorities, a method in which the 100 % of the memory region is assigned to the logical macro having the highest priority, or a method in which the ratio of the memory regions is determined according to the priorities and assigned to each logical macro can be used. Also, for example, a certain amount of memory regions may be constantly occupied by each logical macro, and the rest of the memory regions may be allocated according to priority. [Fourth Embodiment] Next, a twelfth embodiment of the present invention will be described. In this embodiment, as illustrated in Fig.41, a wiring member is disposed between the stacked memory chip 2 and the SoC chip 1. In this embodiment, the interposer 200 is used as a wiring member. The interposer is a substrate in which only a wiring layer is formed separately from the manufacturing process of a semiconductor chip, and is manufactured using a resin substrate, a silicon (Si)

substrate, or the like. According to this embodiment, even if the size of the stacked memory chip 2 is larger than that of the SoC chip 1 and there is a region on the stacked memory chip 2 that does not overlap with the SoC chip 1, it is possible to distribute clocks to the memory elements disposed in that region via the interposer 200. Accordingly, in this case as well, the delay difference between the clocks in the clock input unit 54 of each memory element can be reduced. In other words, by passing through both the wiring in the SoC chip 1 and the wiring in the interposer 200, a uniform delay wiring can be formed from the clock supply source 30 in the SoC chip 1 to the clock input unit 54 of the stacked memory chip 2. More specifically, for example, as illustrated in Fig.41, if the memory region is constituted by the four memory elements 5 on the upper left of the stacked memory chip 2, three of the four memory elements other than the lower right memory element do not overlap with the SoC chip 1. According to this embodiment, as illustrated in Fig.42, in the clock distribution path, the intra-interposer wiring 220 can be used to connect to the intra-SoC chip wiring 210, so even if there is a region on the stacked memory chip 2 that does not overlap with the SoC chip 1, it is possible to realize a uniform delay wiring. Fig.41 illustrates a case where the stacked memory chip 2 is larger in size than the SoC chip 1 and covers the entirety of the SoC chip 1, but this is not a limitation, and if there is a region that does not overlap with the SoC chip 1 in a portion of the stacked memory chip 2, a uniform delay wiring including the region that does not overlap with the SoC chip 1 is possible by applying this embodiment. In addition, here, description has been given of a case in which interposer wiring is used as part of wiring for clock distribution, but this is not a limitation, and interposer wiring may be used as part of wiring for transmitting data, address signals, or command signals. In this case, according to this embodiment, by connecting the interposer wiring to the inter-chip I / O portion of the memory element, it is possible to interconnect the memory element formed in the region on the stacked memory chip 2 that does not overlap with the SoC chip 1. Therefore, it is possible to increase the number of selectable memory elements when configuring the memory region. [Fourth Embodiment] Next, a twelfth embodiment of the present invention will be described. Fig.43 is a cross-sectional view of a semiconductor integrated circuit device 600 according to this embodiment. Multi-layer wiring layers 601 and 602 are formed on the SoC chip 1 and the stacked memory chip 2, respectively. Bonding electrode layers constituted by a portion of the electrode layers constituting the multilayer wiring structures 601, 602 are formed in predetermined positions on the surface layers of the SoC chip 1 and the stacked memory chip 2, respectively. In this embodiment, the electrode pad 603 on the SoC chip side and the electrode pad 604 on the stacked memory chip side are each formed as the bonding electrode layers. Here, the material used for the multilayer interconnections 601, 602 and the electrode pads 603, 604 is not particularly limited, and Cu, Al, or the like that are commonly used in semiconductor integrated circuit devices can be used. Bump electrodes 605 on the SoC chip side are formed on the electrode pads 603 on the SoC chip side as bonding members, and bump electrodes 606 on the stacked memory chip side are

formed on the electrode pads 604 on the stacked memory chip side as bonding members. When manufacturing the semiconductor integrated circuit device 600, these bump electrodes are positioned at corresponding positions, and the bump electrodes are electrically connected to each other. As a result, signal transmission between the SoC chip 1 and the stacked memory chip 2 is possible. The material used for the bump electrodes 605 and 606 is not particularly limited, and materials commonly used in semiconductor integrated circuit devices can be used. For example, a metal such as Au, Cu, solder, or the like can be used. Examples of solder bump materials include Sn / Pb, Sn / Ag, Sn / Cu, Sn / Zn, and Sn / Bi, as well as materials in which certain additional elements are further added to these materials, and these materials can be used as appropriate. When Au bumps are used as the method of electrically connecting the bump electrodes, metal diffusion bonding by applying heat and pressure at the time of mounting is suitable. As another method, a method of maintaining contact between the bump surfaces and ensuring conduction can be used. As a method of maintaining the bump surfaces in contact with each other, a method can be used in which the gap between the SoC chip 1 and the stacked memory chip 2 is sealed with resin, and the contractive force of the resin used for sealing and the heat and pressure applied during mounting are used. When solder is used for the bump electrode, fusion bonding can be used in which the solder is heated to a melting temperature of approximately 200 °C ~ 250 °C, which is the melting temperature of the solder, thereby wetting and connecting the solder to the other bump surface. In this case, pressurization at the time of mounting can be reduced. In the case of an Cu bump, in addition to the method of ensuring electrical continuity by contact described above, a method of mounting in a state where the surface of the Cu bump is activated by plasma treatment or the like and obtaining an electrical connection can be used. Furthermore, solder may be formed on the surface of the Au bump or the Cu bump, and melt-connected at the surface portion of the bump. Next, a first method for forming the bump electrodes 606 on the electrode pads 604 on the stacked memory chip side according to this embodiment will be described using Fig.44. First, a stacked memory chip 2 is prepared in which the electrode pads 604 as illustrated in Fig. 44 A are formed. Next, as illustrated in Fig. 44 B, resist coating is performed. A LOR (Lift-Off Resist) resist 607 is applied by spin coating, and a PMMA (Poly methyl methacrylate) resist 608, which is a positive electron beam resist, is applied thereon. Baking is performed after the resist is applied. The film thickness of the LOR resist 607 is preferably greater than or equal to the film thickness of the subsequently formed electrode. Next, as illustrated in Fig. 44 C, the PMMA resist 608 is used to form an electrode pattern using an electron beam exposure method. A mixed solution of MIBK (Methyl Isobutyl Ketone) and IPA (Isopropyl Alcohol) can be used to develop the PMMA resist 608. Using the patterned PMMA resist 608 as a mask, the LOR resist 607 is etched and removed with an TMAH (Tetra Methyl Ammonium Hydroxide) solution to form a resist pattern (Fig. 44 D). At this time, the LOR resist 607 covered with the PMMA resist 608 is also partially etched away, and overhangs of the PMMA resist 608 are formed around the pattern. This

overhang provides the benefit of facilitating the subsequent lift-off step. A residue may remain at the location where the LOR resist 607 was removed using the TMAH solution. This residue causes a decrease in adhesion of the gold (Au) electrode to the substrate and an increase in electrical resistance, so it is desirable to remove this residue. The residue of the resist can be removed by ashing in oxygen plasma. In addition, copper oxide on the surface generated during the ashing process or by exposure to the atmosphere may be removed by performing etching with dilute hydrofluoric acid or the like after ashing. Next, an electrode formation step is performed as illustrated in Fig. 44 E. Gold (Au) 609 is deposited as the bump electrode 606 using an electron beam vapor deposition method. To ensure adhesion with the substrate, titanium may be deposited prior to vapor deposition of the gold (Au) 609, and gold (Au) 609 may be deposited to a predetermined thickness. After electron beam deposition, the resist is dissolved in a solution such as acetone, and the gold (Au) deposited on the resist is removed by lift-off to complete the bump electrode 606 (Fig. 44 F). Thereafter, acetone is removed using ethanol or the like, and washed with water. As described above, in the present embodiment, the electron beam vapor deposition method is used for the deposition of the gold (Au) 609, but other deposition methods such as sputtering and pulse laser deposition may be used instead. Next, a second method for forming the bump electrodes 606 on the electrode pads 604 on the stacked memory chip side will be described. In the first method, the electrode pattern was formed by lift-off, but this is not a limitation, and the electrode pattern may be formed by etching after metal is deposited, as described below. First, oxides on the copper surface produced by exposure to the atmosphere are removed by etching using dilute hydrofluoric acid. Next, gold (Au) is deposited to a predetermined thickness using an electron beam deposition method. To ensure adhesion with the substrate, titanium may be deposited prior to vapor deposition of the gold (Au). Next, after a negative-working electron beam resist is applied, baking is performed, and an electrode pattern is formed in the resist using an electron beam exposure method. Next, the gold (Au) other than the electrode pattern portion covered with the resist is removed by etching using a potassium iodide solution. Furthermore, titanium is removed by etching using an etching solution in which hydrogen peroxide and hydrofluoric acid are diluted with pure water. Finally, oxygen plasma ashing is used to remove the negative-working electron beam resist, thereby completing the bump electrode 606. [Fourth Embodiment] Next, a twelfth embodiment of the present invention will be described. FIGS. 45 A and 45 B are cross-sectional views for explaining the method of manufacturing the semiconductor integrated circuit device according to this embodiment. Multi-layer wiring layers 601 and 602 are formed on the SoC chip 1 and the stacked memory chip 2, respectively. Bonding electrode layers constituted by a portion of the electrode layers constituting the multilayer wiring structures 601, 602 are formed in predetermined positions on the surface layers of the SoC chip 1 and the stacked memory chip 2, respectively. In this embodiment, the electrode pad 603 on the SoC chip side and the electrode pad 604 on the stacked memory chip side are each formed as the bonding electrode layers, and the

electrode pad 603 on the SoC chip side is provided with: The bump electrodes 605 on the SoC chip side were formed as bonding members, and the bump electrodes 606 on the stacked memory chip side were formed on the electrode pads 604 on the stacked memory chip side. Next, the SoC chip 1 is fixed to the mounting stage 610 of the mounting apparatus by suction or the like. The rear face of the SoC chip 1 is in contact with the mounting stage 610, and the front face of the bump electrode 605 faces upward in Fig. 45 A. Note that it is desirable that the mounting stage 610 be provided with a suction fixing function, a planar (x-y) drive function, a heating function, and a joining surface height adjustment function. Next, the stacked memory chip 2 is fixed by suction to the mounting head 620 of the mounting apparatus. At this time, the mounting head 620 is in contact with the back surface of the stacked memory chip 2, and the front surfaces of the bump electrodes 606 face downward in Fig. 45 A. Note that the mounting head 620 preferably includes a chip suction fixing function, a θ driving function, a heating function, and a bonding height adjustment function. As illustrated in Fig. 45 A, the surfaces of the bump electrodes 605, 606 of the SoC chip 1 and the stacked memory chip 2 face each other. In the process of positioning the SoC chip 1 and the stacked memory chip 2, first, an image of alignment marks necessary for positioning the chips is captured. It is preferable that the alignment marks be produced in a process for producing an electrode pad or a process for producing a bump electrode. In general, it is desirable to provide the chip at two locations in the vicinity of corners on diagonal lines of the chip. At this time, in cases where the thermal expansion coefficients of the SoC chip 1 and the stacked memory chip 2 are the same, the temperatures of the mounting head 620 and the mounting stage 610 are the same, making it possible to prevent recognition coordinate positional skew caused by differences in the thermal expansion coefficients. Next, the SoC chip 1 and the stacked memory chip 2 are aligned from the alignment mark coordinate data of the two recognized points. Next, as illustrated in Fig. 45 B, the stacked memory chip 2 is mounted on the SoC chip 1, and the bump electrodes 606 on the stacked memory chip side and the bump electrodes 605 on the SoC chip side are electrically connected by applying heat and pressure. When each bump electrode is made from gold (Au) material, electrical connection between the SoC chip 1 and the stacked memory chip 2 is made possible by carrying out Au diffusion bonding by applying heat and pressure during mounting. At this time, by sealing the gap between the SoC chip 1 and the stacked memory chip 2, in other words, the periphery of the connection portion between the bump electrodes 605, 606, it is possible to improve the connection reliability and the like during practical use. An epoxy resin, a polyimide resin, a silicone resin, or the like can be used as the resin used for sealing, but the present invention is not limited thereto. one type of these resins may be used in combination, or two or more types of these resins may be mixed with an inorganic filler such as silica or the like. When an epoxy resin is used, the semiconductor integrated circuit device according to this embodiment is completed by curing the resin after filling at approximately 100 ~ 200 °C. A normally commonly used method can be used for resin sealing, for example, a

method in which the gap between the SoC chip 1 and the stacked memory chip 2 is filled with a liquid resin using the capillary phenomenon, and then the resin is hardened. As the resin used in this case, an epoxy resin can be suitably used in consideration of the viscosity physical properties of the resin, which are important at the time of filling. Here, resin wettability can be improved by modifying the surface of the resin-filled region of the SoC chip 1 or the stacked memory chip 2 by plasma treatment or the like prior to filling with the resin to increase the resin wettability. The present invention is not limited thereto, and resin fillability can be improved by a method of accelerating resin filling using atmospheric pressure after resin filling in a vacuum, a method of curing resin while pressurizing, or the like. [Fourth Embodiment] Next, a twelfth embodiment of the present invention will be described. FIGS. 46 A and 46 B are cross-sectional views for explaining the method of manufacturing the semiconductor integrated circuit device according to this embodiment. Multi-layer wiring layers 601 and 602 are formed on the SoC chip 1 and the stacked memory chip 2, respectively. Bonding electrode layers constituted by a portion of the electrode layers constituting the multilayer wiring structures 601, 602 are formed in predetermined positions on the surface layers of the SoC chip 1 and the stacked memory chip 2, respectively. In this embodiment, the electrode pad 603 on the SoC chip side and the electrode pad 604 on the stacked memory chip side are each formed as the bonding electrode layers, and the electrode pad 603 on the SoC chip side is provided with: The bump electrodes 605 on the SoC chip side were formed as bonding members, and the bump electrodes 606 on the stacked memory chip side were formed on the electrode pads 604 on the stacked memory chip side. As illustrated in Fig. 46 A, unlike the 12 embodiment, in this embodiment, a sealing resin 630 is formed in advance on the surfaces of the SoC chip 1 and the stacked memory chip 2 as a sealing material prior to mounting. Fig. 46 A illustrates a case in which the sealing resin 630 is formed on both the SoC chip 1 and the stacked memory chip 2. After forming the sealing resin 630, excess resin during formation is removed, and the surfaces of the connection between the bump electrodes 605 on the SoC chip side and the bump electrodes 606 on the stacked memory chip side are exposed, thereby making it possible to improve the connection characteristics of the bump electrodes 605, 606. As in the 12 embodiment, an epoxy resin, a polyimide resin, a silicone resin, or the like can be used as the material of the sealing resin 630. In addition, the present invention is not limited thereto, and one type or two or more types of these resins may be used in combination, or an inorganic filler such as silica may be mixed therein. Examples of the method of supplying the resin to the surface of the SoC chip 1 or the stacked memory chip 2 include a method of supplying the resin processed on the film to the chip surface using a laminator, a method of supplying and temporarily curing a liquid resin using spin coating or printing methods, and the like. Also, as a method for removing excess resin and exposing the surface of the bump electrode, for example, a method by machining using a byte capable of precision machining can be used. Note that if it is not necessary to expose the surfaces of the bump electrodes, the sealing resin 630 may be formed on only one

of the SoC chip 1 and the stacked memory chip 2. Also, immediately prior to mounting the SoC chip 1 and the stacked memory chip 2, the sealing resin 630 can be formed by applying an appropriate amount of liquid resin to the surface of the SoC chip 1. Next, as illustrated in Fig. 46 B, the stacked memory chip 2 is mounted on the SoC chip 1 and subjected to heating and pressure treatment. In this way, the bump electrodes 606 on the stacked memory chip side and the bump electrodes 605 on the SoC chip side are electrically connected and, at the same time, the sealing resin 630 is cured, thereby completing the semiconductor integrated circuit device according to this embodiment. Gold (Au) can be used as the material of the bump electrodes, and Au diffusion bonding can be performed under the same conditions as in the 12-th embodiment. In the present embodiment, bump connection and resin sealing are performed simultaneously, so even in cases where the electrical connection of the bump electrodes is only in contact, the electrical connection can be favorably maintained due to the pressure applied during mounting and the stress applied when the sealing resin 630 is cured and shrunk. In the 11 st embodiment described above, a case is described in which the SoC chip 1 and the stacked memory chip 2 are electrically connected by bump electrodes, and signals are transmitted between the chips. However, the present invention is not limited thereto, and signal transmission may be performed in a state in which no electrical connection is made between the chips. For example, as in the semiconductor integrated circuit device 700 illustrated in Fig.47, the inductors 701 may be formed on the surfaces of the SoC chip 1 and the stacked memory chip 2, and signals may be transmitted by magnetic field coupling between the inductors 701 with the insulating material 702 interposed between the chips. Alternatively, as in the semiconductor integrated circuit device 710 illustrated in Fig.48, the capacitive pads 711 may be formed on the respective surfaces of the SoC chip 1 and the stacked memory chip 2, and signals may be transmitted by capacitive coupling between the capacitive pads 711 with the insulating material 702 interposed between the chips. In the semiconductor integrated circuit devices 700, 710 that use these transmission schemes, electrical connections are not made between the chips, making it possible to avoid the risk of circuit damage in the chip caused by static electricity. The present invention is not limited to the embodiments described above, and various modifications are possible within the scope of the invention described in the claims. it goes without saying that these modifications are also included within the scope of the present invention. This application claims priority based on Japanese Patent Application No.2008-213670 filed August 22, 2008 and Japanese Patent Application No.2009-024501 filed February 5, 2009, the entire disclosures of which are incorporated herein by reference.

INDUSTRIAL APPLICABILITY

[0009] The present invention can be applied to a memory chip accessed by a semiconductor chip, which is a system-on-chip provided with a large number of logical macros.

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# Semiconductor memory module and method of testing operating margin thereof, and semiconductor memory apparatus

Abstract
translated from Korean
The present invention discloses a semiconductor memory module, a test method thereof, and a semiconductor memory device. The semiconductor memory module of the present invention includes a circuit board having a plurality of external input / output terminals, an interface circuit provided on the circuit board, a plurality of semiconductor memory chips, and a nonvolatile memory chip. The interface circuit interfaces the signal transmission between the plurality of external input terminals and the internal circuit. The plurality of semiconductor memory chips are connected to an interface circuit and input an external address signal having the mode setting information to decode the input mode setting information to generate a mode setting control signal. In the test mode, the mode setting control signal is provided to the test operation circuit unit. The nonvolatile memory chip stores the initial value to provide initial values of the semiconductor memory chips to the outside through the interface circuit during initial system boot. Therefore, in the present invention, various tests can be performed by mode setting the chips in the memory module, thereby improving test efficiency in the test process.

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Description
translated from Korean
Semiconductor Memory Module and Method of Testing Operating Margin, and Semiconductor Memory Apparatus
The present invention relates to a semiconductor memory module, a test method, and a semiconductor memory device capable of operating margin testing, and more particularly, to a semiconductor memory module and a test method capable of testing an operation margin by allowing a mode setting to be programmed during a test operation. ,
In order to improve the performance of the central processing unit of the computer system and to process a large amount of data at high speed, large-capacity main memories of high speed operation are used. In particular, as a main memory of a personal computer system, a memory module including a double data rate (DDR) or rambus DRAM chips as one package is commercially provided.
The memory module configures a plurality of unit memory chips on a circuit board and mounts the configured module to a motherboard to connect to the system.
The computer system requires that initialization information for initializing the memory module is stored in the memory module in order to speed up the system booting operation.
In order for a computer system to boot properly, it must be able to recognize the configuration of the memory modules. Parallel Presence Detect (PPD) is a general method of using registers to connect necessary information. It is mainly used in SIMM (Single-In-Line Memory Module) type modules and Serial Presence Detect (SPD). -Serial Configuration Recognition Device) is a method used by a module of a dual-in-line memory module (DIMM) type and uses EEPROM to store information about the module.
The test range of such a memory module is limited according to the configuration of the unit memory chip. Typically, synchronous DRAMs have a mode register inside the chip and are configured to set to test mode. In other words, the setting in the unit chip is given only the mode setting in which the chip is simply set to the test mode or the normal mode.
However, in the case of configuring such unit chips as modules, data input / output operation margins among the plurality of chips may be different from each other, and there may be a difference in minute operation parameter differences depending on a mounting environment or a module. Therefore, after module mounting, these parameters had to be measured to find the most appropriate margin for the entire module and to set each memory chip inside the module. That is, since it is not possible to know which margin is most suitable at the time of producing the first module, a test sample module having various operating margins was manufactured and then tested in a mounted state to find an optimal margin.
However, since each individual memory chip does not have a function for testing an operating margin by changing parameter values in a test mode, a separate test module has to be prepared and tested for each change value, which is expensive.
This process adds time and cost, increasing module production costs.
SUMMARY OF THE INVENTION An object of the present invention is to provide a semiconductor memory module and a test method thereof capable of testing an optimal operating

margin among a plurality of memory chips in order to solve the problems of the prior art.
Another object of the present invention is to provide a semiconductor memory device capable of programming a plurality of operation margin tests.
In order to achieve the above object, the memory module of the present invention includes a circuit board having a plurality of external input / output terminals, an interface circuit provided on the circuit board, a plurality of semiconductor memory chips, and a recognition unit.
The interface unit interfaces a signal transmission between the memory chips and the input / output terminal. The interface section includes a timing register. Each of the semiconductor memory chips is connected to an interface circuit and inputs an external address signal having mode setting information to decode the input mode setting information to generate a mode setting control signal. In the test mode, the mode setting control signal is provided to the test operation circuit unit. Here, the semiconductor memory chips may be composed of DDR SDRAM or Rambus DRAM, respectively. The recognition unit stores the initial value in order to provide the initial values of the semiconductor memory chips to the outside through the interface circuit during initial system booting. Here, the recognition unit is composed of a serial input / output EEPROM.
The test method of the present invention for achieving the object of the present invention comprises the following steps.
a) mounting a test memory module to the memory test equipment;
b) reading initial value information from the mounted test memory module;
c) initializing the test memory module in response to the read initial value information;
d) providing test mode setting information to the initialized test memory module;
e) setting a plurality of memory chips mounted inside the memory module to a corresponding test mode in response to provided test mode setting information;
f) testing the memory module in the set test mode; And
g) detecting the mode setting information of the optimum operation by repeating steps d to f while changing the test mode setting information provided to the memory module.
In the present invention, the test memory module further includes programming a plurality of memory chips mounted in the test mode by electric fusing.
In order to achieve the above object, the semiconductor memory device of the present invention includes a mode register for inputting and storing an external address signal having mode setting information, and a mode setting connected to the mode register and decoding the mode setting information stored in the mode register. A mode setting decoder for generating a control signal, and a fuse circuit unit which is fused to provide the mode setting control signal to the normal operation circuit unit in the normal mode and to provide the mode setting control signal to the test operation circuit unit in the test mode.
Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. This embodiment is described in sufficient detail to enable those skilled in the art to practice the invention.
1 shows a configuration diagram of a semiconductor memory module according to the present invention.
In FIG. 1, the memory module 100 of the present invention is provided by installing an interface

unit 120, a plurality of SDRAMs 130, and a recognition unit 140 on a circuit board 110. Specific examples are disclosed in the data manual of the DDR SDRAM Registered Module published by the applicant in August 2003. The circuit board 110 is provided with 184 pin input / output terminals 112 for inputting and outputting data, data strobe signals, address signals, timing signals, power signals, and the like.

The interface unit 120 is composed of an address and a timing register. Input the bank address BA0 ~ BA1, address signals A0 ~ A12, timing signals CS0 ~ CS1, RAS, CAS, CKE0, CKE1, WE, etc., so that the internal chip selection signal, internal bank address signal, internal address signal, internal timing signal, etc. Occurs.

The SDRAM 130 may be configured as 512M, 1G, 2G, etc. according to the memory capacity.

The recognition unit 140 is configured as an EEPROM and inputs and outputs serial data in response to the serial clock signal.

FIG. 2 is a circuit block diagram of the internal memory chip of FIG. 1. 2, the SDRAM 130 according to the present invention includes an address register 202, a timing register 204, a mode register 206, a mode setting circuit 207, a row decoder 208, A column decoder 210, a memory cell array 212, a data input buffer and a data input register 214, a data output buffer 216, a data strobe output buffer 218, a DLL 220, and the like.

The address register 202 inputs and buffers a bank address signal and an address signal ADD to provide a row address, a column address, a mode set address, and the like in response to a timing control signal.

The timing register 204 inputs and buffers external timing control signals such as CKE, CS, RAS, CAS, and WE to generate internal timing control signals.

The mode register 206 latches a mode set address in response to a timing control signal, eg, a mode set command, to store mode set information.

The mode setting circuit 207 includes a mode setting decoder MRD, a first fuse circuit FS1, a second fuse circuit FS2, a normal operation circuit NC, and a test operation circuit TC.

Referring to FIG. 3, the mode setting decoder MRD decodes the MRS command MRSCMD signal and the mode setting address bits Ai and Aj through the gates of G1 to G4 to output four mode setting control signals MRS1 to MRS4. Output each of them.

In the first fuse circuit FS1 and the second fuse circuit FS2, the output is converted from a state of '0' or '1' to a state of '1' or '0' by cutting a fuse through a transient current. It consists of a fuse circuit.

In a normal memory chip, all of FS2 is turned off and all of FS1 are turned on so that the MRS1 to MRS4 signals are applied to the normal operation circuit. Therefore, in the normal operation, the mode setting control signals MRS1 to MRS4 are generated when the address bits Ai and Aj are changed externally, and the normal operation circuit is programmed by the corresponding mode setting.

In the test memory chip, all of FS1 is turned off and FS2 is all turned on. Therefore, during the test operation, the mode setting control signals MRS1 to MRS4 are generated when the address bit Ai and Aj values are changed externally, and the test operation circuit is programmed by the corresponding mode setting.

4 shows an example of a mode register setting code table according to the present invention.
That is, four test modes can be set by the address bits Ai and Aj. As shown in the drawing, the access time (tAC) value of the DRAM can be programmed to be set while changing the operating margin little by little, such as + 100ps, + 200ps, -100ps, -200ps, and the like.
5 is a flowchart for describing a test operation of the semiconductor memory module of FIG. 1.
First, the test memory module (TMM) is mounted on the module test equipment (S10). Here, the test memory module TMM refers to a memory module including the above-described test mode programmable memory chips, and refers to a module in which internal chips are fused in a test mode.
The SPD read command is transmitted to the memory module mounted in the test equipment, and the initial value information of the mounted memory module is interpreted by receiving the SPD code value read from the recognition unit of the module (S12).
The TMM is initialized according to the analyzed initial value information (S14).
Subsequently, mode set address information is provided to the initialized TMM, and an MRS command is issued to set the mode in the first test mode (S16).
Subsequently, the memory module is tested according to the given test pattern, and the test result is analyzed (S18).
If the optimal operating margin is not determined by the test result analysis, the mode change is performed (S20), and the steps S16 and S18 are repeated.
When the optimum operating margin is detected by the test, the test result is stored (S22).
For example, in this manner, the optimum access time can be set while changing the access time of the memory chip from the initial value to four steps from + 200ps to -200ps.
Although described with reference to the examples, those skilled in the art can understand that the present invention can be variously modified and changed without departing from the spirit and scope of the invention described in the claims below. There will be.
As described above, the present invention can be tested while changing the operation margin little by little in the test of the memory module so that one test memory module can be used to easily detect the optimum operating margin. Therefore, since all four conventional test memory modules can be tested by one test module, test costs can be reduced and test work efficiency can be improved.
1 is a block diagram of a semiconductor memory module according to the present invention.
FIG. 2 is a circuit block diagram of the internal memory chip of FIG. 1. FIG.
FIG. 3 is a diagram illustrating one mode setting circuit of the semiconductor memory chip of FIG. 2. FIG.
4 is a diagram showing an example of a mode register setting code table according to the present invention;
5 is a flowchart for describing a test operation of the semiconductor memory module of FIG. 1.
* Brief description of the main parts of the drawing *
100: memory module 110: circuit board
120: interface unit 130: memory chip, SDRAM
140: recognition unit, EEPROM 206: mode register

207: mode setting circuit MRD: mode setting decoder
FS1, FS2: Fusing circuit part NC: Normal operation circuit part
TC: test operation circuit

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심사청구 : 없음

# (54) 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트방법과 반도체 메모리 장치

요약

본 발명은 반도체 메모리 모듈 및 그 테스트 방법과 반도체 메모리 장치를 개시한다. 본 발명의 반도체 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스회로, 복수의 반도체 메모리 칩들, 및 불휘발성 메모리 칩을 포함한다. 인터페이스회로는 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스 한다. 복수의 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 모드세팅 제어신호를 테스트동작회로부에 제공한다. 불휘발성 메모리 칩은 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 따라서, 본 발명에서는 메모리 모듈 내부의 칩들을 모드세팅에 의해 다양한 테스트를 수행할 수 있어서, 테스트 과정에서 테스트 효율을 향상시킬 수 있다.

대표도

도 2

명세서

도면의 간단한 설명

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도.

도 2는 도 1의 내부 메모리 칩의 회로 블록도.

도 3은 도 2의 반도체 메모리 칩의 모드세팅회로의 일예를 나타낸 도면.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸 도면.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도.

* 도면의 주요 부분에 대한 간단한 부호설명*

100 : 메모리 모듈 110 : 회로기판

120 : 인터페이스부 130 : 메모리 칩, SDRAM



Samsung Electronics Co., Ltd.
Ex. 1002, p. 470

140 : 인식부, EEPROM 206 : 모드 레지스터

207 : 모드 세팅회로 MRD : 모드 세팅 디코더

FS1, FS2 : 퓨징회로부 NC : 정상 동작 회로부

TC : 테스트 동작 회로부

## 발명의 상세한 설명

### 발명의 목적

#### 발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트 방법과 반도체 메모리 장치에 관한 것으로서, 특히 테스트 동작시 모드 세팅을 프로그램할 수 있도록 함으로써 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 테스트 방법에 관한 것이다,

컴퓨터 시스템의 중앙처리장치의 성능 향상과 더불어 많은 양의 데이터를 고속으로 처리하기 위하여 고속동작의 대용량 메인 메모리들이 사용되고 있다. 특히 퍼스널 컴퓨터 시스템의 메인 메모리로는 DDR(Double Data Rate) 또는 램버스 디램 칩들을 하나의 패키지로 구성한 메모리 모듈이 상품화되어 제공되고 있다.

이러한 메모리 모듈은 복수의 단위 메모리 칩들을 회로기판 상에 구성하고 구성된 모듈을 마더보드에 장착하여 시스템에 연결한다.

컴퓨터 시스템에서는 시스템 부팅 동작을 고속으로 하기 위하여 메모리 모듈을 초기화하기 위한 초기화 정보를 메모리 모듈 내부에 저장하도록 요구하고 있다.

컴퓨터 시스템이 부팅을 할 때 제대로 작동하기 위해서는 메모리 모듈의 구성형태를 인식할 수 있어야 한다. PPD(Parallel Presence Detect - 병렬 구성 인식장치)는 필요로 하는 정보를 연결시키기 위해 레지스터를 사용하는 일반적인 방법으로 주로 SIMM(Single-In-Line Memory Module)방식의 모듈에서 사용하고, SPD(Serial Presence Detect - 직렬 구성 인식장치)란 DIMM(Dual-In-Line Memory Module)방식의 모듈에서 사용하는 방식으로 모듈에 관한 정보 저장시 EEPROM을 이용하는 것이다.

이와 같은 메모리 모듈의 테스트 범위는 단위 메모리 칩의 구성에 따라 제한된다. 통상적으로 동기형 DRAM의 경우 칩 내부에 모드 레지스터를 구비하고 테스트 모드로 세팅하도록 구성되어 있다. 즉, 단위 칩에서 세팅은 단순히 칩을 테스트 모드로 세팅할 것인지 아니면 노말 모드로 할 것인지를 선택하는 정도의 모드 세팅만 주어진 상태이다.

그러나, 이러한 단위 칩들을 모듈로 구성할 경우 복수의 칩들 간의 데이터 입출력 동작 마진이 서로 차이가 있을 수 있으며, 실장환경이나 모듈에 따라 미세한 동작 파라미터들의 차이가 형성될 우려가 있었다. 그러므로 모듈 실장 후에 이들 파라미터들을 측정하여 모듈 전체의 가장 적합한 마진을 찾아서 모듈 내부의 각 메모리 칩들을 세팅하지 않으면 안되었다. 즉 처음 모듈 생산시에 가장 적당한 마진이 어느 것인지 알 수 없으므로 다양한 동작 마진을 가진 테스트용 샘플 모듈들을 제작한 다음에 실장된 상태에서 테스트하여 최적의 마진을 찾아내는 과정이 요구되었다.

그러나, 각 개별적인 메모리 칩들에는 테스트 모드시 파라미터 값들을 변경하면서 동작 마진을 테스트하기 위한 기능이 없으므로 각 변경값들 마다 각각 별도의 테스트용 모듈을 마련하여 테스트하여야 하기 때문에 많은 비용과 시간이 소요되었다.

이와 같은 작업과정은 시간과 비용을 증가시키므로 모듈 생산 코스트를 상승시킨다.

#### 발명이 이루고자 하는 기술적 과제

본 발명의 목적은 이와 같은 종래 기술의 문제점을 해결하기 위하여 복수의 메모리 칩들 사이의 최적 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 그 테스트 방법을 제공하는 데 있다.

본 발명의 다른 목적은 복수의 동작마진 테스트를 프로그램할 수 있는 반도체 메모리 장치를 제공하는 데 있다.

#### 발명의 구성 및 작용

상기 목적을 달성하기 위하여 본 발명의 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스 회로, 복수의 반도체 메모리 칩들 및 인식부를 포함한다.

인터페이스부는 메모리 칩들과 입출력단자 사이의 신호전송을 인터페이스 한다. 인터페이스부는 타이밍 레지스터를 포함한다. 각 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회



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로부에 제공하고, 테스트 모드에서는 모드세팅 제어신호를 테스트동작회로부에 제공한다. 여기서 반도체 메모리 칩들은 각각 DDR SDRAM 또는 램버스 디램으로 구성될 수 있다. 인식부는 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 여기서 인식부는 직렬 입출력방식의 EEPROM으로 구성한다.

본 발명의 목적을 달성하기 위한 본 발명의 테스트 방법은 다음 단계들을 포함한다.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리드하는 단계;

c) 상기 리드된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 세팅정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 세팅정보에 응답하여 대응하는 테스트 모드로 세팅하는 단계;

f) 상기 세팅된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계; 및

g) 메모리 모듈에 제공되는 테스트 모드 세팅정보를 변경하면서 상기 d 내지 f단계를 반복하여 최적 동작의 모드 세팅정보를 검출하는 단계.

본 발명에서 테스트용 메모리 모듈은 전기적 퓨징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램하는 단계를 더 포함한다.

상기 다른 목적을 달성하기 위하여 본 발명의 반도체 메모리 장치는 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터와, 모드 레지스터에 연결되고, 상기 모드 레지스터에 저장된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하는 모드세팅 디코더와, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하기 위해 퓨징되는 퓨즈회로부를 구비한다.

이하, 첨부한 도면을 참조하여 본 발명의 바람직한 실시예를 구체적으로 설명하고자 한다. 이 실시예는 이 기술에 숙련된 자들이 본 발명을 실시할 수 있게 충분히 상세하게 기술한다.

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도를 나타낸다.

도1에서 본 발명의 메모리 모듈(100)은 회로기판(110) 상에 인터페이스부(120), 복수의 SDRAM(130), 인식부(140)를 설치하여서 된 것이다. 구체적인 예는 본 출원인이 2003년 8월에 공개한 DDR SDRAM Registered Module의 데이터 매뉴얼에 개시되어 있다. 회로기판(110)에는 데이터, 데이터 스트로브신호, 어드레스신호, 타이밍신호, 전원신호 등을 입출력하기 위한 184핀의 입출력단자들(112)이 형성된다.

인터페이스부(120)는 어드레스 및 타이밍 레지스터로 구성한다. 뱅크어드레스 BA0~BA1, 어드레스신호 A0~A12, 타이밍신호들 CS0~CS1, RAS, CAS, CKE0, CKE1, WE 등을 입력하여 내부칩선택신호, 내부 뱅크어드레스신호, 내부 어드레스신호, 내부 타이밍신호 등을 발생한다.

SDRAM(130)은 메모리 용량에 따라 512M, 1G, 2G 등으로 구성할 수 있다.

인식부(140)는 EEPROM으로 구성하고 시리얼 클럭신호에 응답하여 시리얼 데이터를 입출력한다.

도 2는 도 1의 내부 메모리 칩의 회로 블록도를 나타낸다. 도 2에서 본 발명에 의한 SDRAM(Synchronous Dynamic Random Accesses Memory)(130)은 어드레스 레지스터 (202), 타이밍 레지스터(204), 모드 레지스터(206), 모드세팅회로(207), 로우 디코더(208), 컬럼 디코더(210), 메모리 셀어레이(212), 데이터 입력버퍼 및 데이터 입력 레지스터(214), 데이터 출력버퍼(216), 데이터 스트로브 출력버퍼(218), DLL(220) 등을 포함한다.

어드레스 레지스터(202)는 뱅크 어드레스신호 및 어드레스신호(ADD) 등을 입력하여 버퍼링하여 타이밍 제어신호에 응답하여 로우 어드레스, 컬럼 어드레스, 모드세트 어드레스 등을 제공한다.

타이밍 레지스터(204)는 CKE, CS, RAS, CAS, WE 등의 외부 타이밍 제어신호를 입력하여 버퍼링하여 내부 타이밍 제어신호를 발생한다.

모드 레지스터(206)는 타이밍 제어신호, 예컨대 모드 세트 커맨드에 응답하여 모드 세트 어드레스를 래치하여 모드세트 정보를 저장한다.

모드세팅회로(207)는 모드세팅 디코더(MRD), 제1퓨즈회로(FS1), 제2퓨즈회로(FS2), 정상동작 회로부(NC), 테스트동작 회로부(TC)를 포함한다.



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도 3을 참조하면, 모드세팅 디코더(MRD)는 MRS 커멘드(MRSCMD)신호와 모드세팅 어드레스 비트(Ai, Aj)를 G1 내지 G4의 게이트를 통하여 디코딩하여 4개의 모드세팅 제어신호(MRS1~MRS4)를 각각 출력한다.

제1 퓨즈회로(FS1) 및 제2 퓨즈회로(FS2)는 과도전류를 흘려서 퓨즈를 절단시킴으로써 '0' 또는 '1'의 상태에서 '1' 또는 '0'의 상태로 출력이 변환되는 통상적인 퓨즈회로로 구성한다.

정상적인 메모리 칩에서는 FS2는 모두 턴오프되고 FS1는 모두 턴온되어 MRS1~MRS4 신호가 정상동작회로에 인가되도록 퓨징된다. 따라서, 정상동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 정상동작회로가 프로그램된다.

테스트용 메모리 칩에서는 FS1은 모두 턴오프되고 FS2는 모두 턴온되도록 퓨징된다. 따라서, 테스트 동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 테스트 동작회로가 프로그램된다.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸다.

즉, 어드레스 비트 Ai, Aj값에 의해 4가지 테스트 모드의 설정이 가능하다. 도시한 바와 같이, 디램의 억세스 타임(tAC) 값을 + 100ps, + 200ps, -100ps, -200ps 등으로 동작마진을 조금씩 변경하면서 설정할 수 있도록 프로그램할 수 있다.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도를 나타낸다.

먼저 모듈 테스트 장비에 테스트용 메모리 모듈(TMM)을 장착한다(S10). 여기서 테스트용 메모리 모듈(TMM)은 상술한 테스트 모드 프로그램이 가능한 메모리 칩들로 구성한 메모리 모듈을 칭하며, 내부 칩들이 테스트모드로 퓨징된 모듈을 말한다.

테스트 장비에서 장착된 메모리 모듈에 SPD 리드명령을 전달하여 모듈의 인식부로부터 읽혀진 SPD 코드 값을 전송받아 장착된 메모리 모듈의 초기값 정보를 해석한다(S12).

해석된 초기값 정보에 따라 TMM을 초기화시킨다(S14).

이어서, 초기화된 TMM에 모드세트 어드레스 정보를 제공하고 MRS 커멘드를 내려서 제1테스트 모드로 모드세팅시킨다(S16).

이어서 주어진 테스트 패턴에 의해 메모리 모듈을 테스트하고, 테스트 결과를 분석한다(S18).

테스트 결과 분석에 의해 최적 동작마진이 아닐 경우에는 모드변경을 수행하여(S20) S16, S18 단계를 반복 수행한다.

상기 테스트에 의해 최적 동작마진이 검출되면 그 테스트 결과를 저장한다(S22).

예컨대 이와 같은 방식에 의해 메모리 칩의 억세스 타임을 초기치에서부터 + 200ps 로부터 -200ps로 4단계로 바꾸어가면서 최적의 억세스 타임을 세팅할 수 있게 된다.

실시예를 참조하여 설명하였지만, 해당 기술 분야의 숙련된 당업자는 하기의 특허 청구의 범위에 기재된 본 발명의 사상 및 영역으로부터 벗어나지 않는 범위 내에서 본 발명을 다양하게 수정 및 변경시킬 수 있음을 이해할 수 있을 것이다.

## 발명의 효과

상술한 바와 같이 본 발명에서는 메모리 모듈의 테스트시 동작마진을 조금씩 변경하면서 테스트 할 수 있으므로 하나의 테스트 메모리 모듈을 사용하여 최적의 동작마진을 손쉽게 검출할 수 있게 된다. 그러므로, 종래의 4개의 테스트 메모리 모듈을 하나의 테스트 모듈로 모두 테스트 할 수 있으므로 테스트 비용을 절감할 수 있고 테스트 작업 효율을 향상시킬 수 있다.

## (57) 청구의 범위

### 청구항 1.

모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터;

상기 모드 레지스터에 연결되고, 상기 모드 레지스터에 저장된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하는 모드세팅 디코더;

정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하기 위해 퓨징되는 퓨즈회로부를 구비한 것을 특징으로 하는 반도체 메모리 장치.



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## 청구항 2.

복수의 외부 입출력단자들을 가지는 회로기판;

상기 회로기판 상에 설치되고, 상기 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스 하기 위한 인터페이스 회로;

상기 회로기판 상에 설치되고, 상기 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하는 복수의 반도체 메모리 칩들; 및

상기 회로기판 상에 설치되고, 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한 인식부를 구비한 것을 특징으로 하는 메모리 모듈.

## 청구항 3.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리드하는 단계;

c) 상기 리드된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 세팅정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 세팅정보에 응답하여 대응하는 테스트 모드로 세팅하는 단계;

f) 상기 세팅된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계;

g) 메모리 모듈에 제공되는 테스트 모드 세팅정보를 변경하면서 상기 d 내지 f단계를 반복하여 최적 동작의 모드 세팅정보를 검출하는 단계를 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

## 청구항 4.

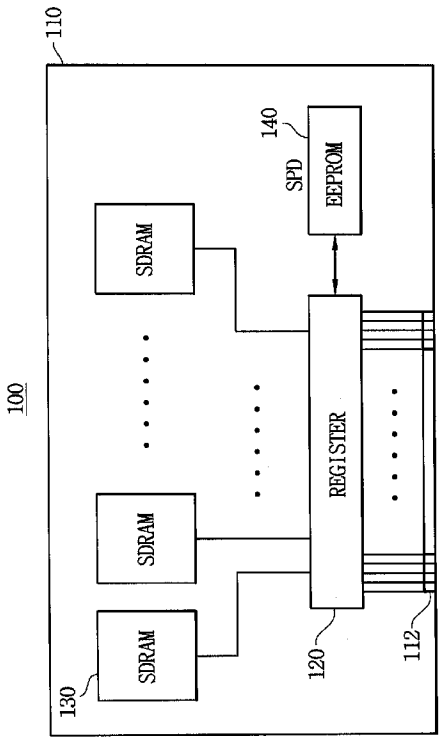
제3항에 있어서, 상기 테스트용 메모리 모듈은 퓨징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램하는 단계를 더 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

도면



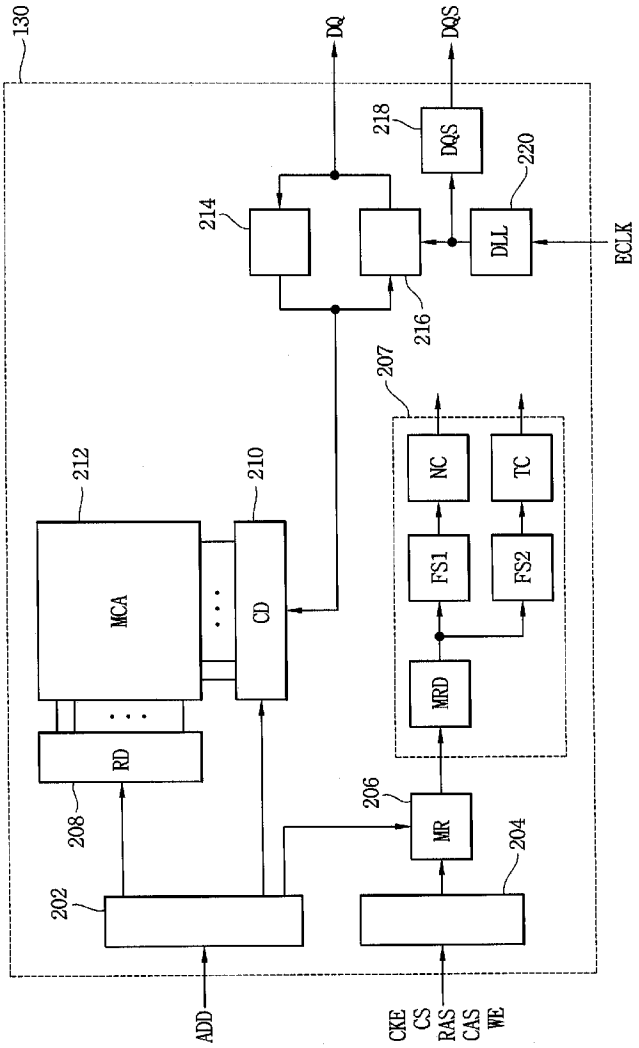
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도면1




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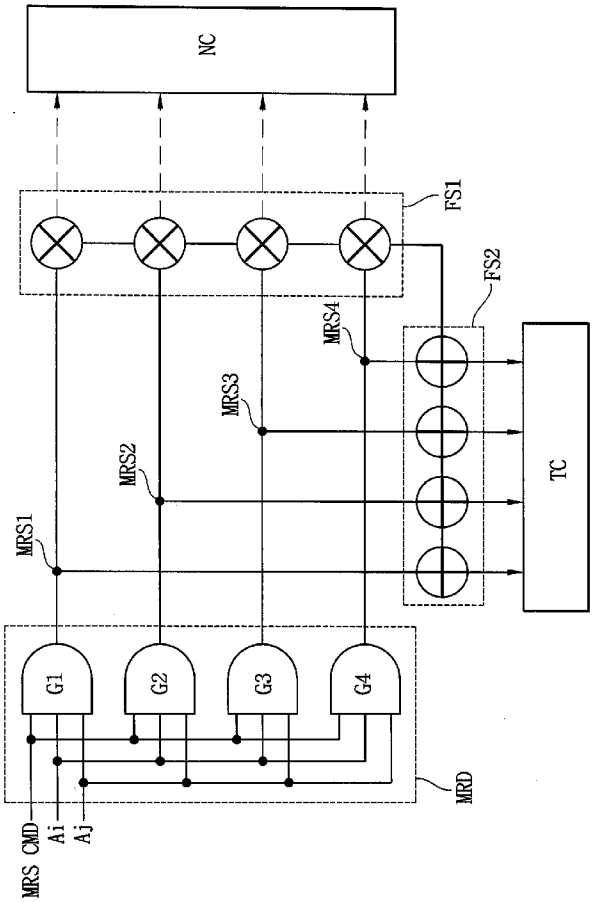
도면2






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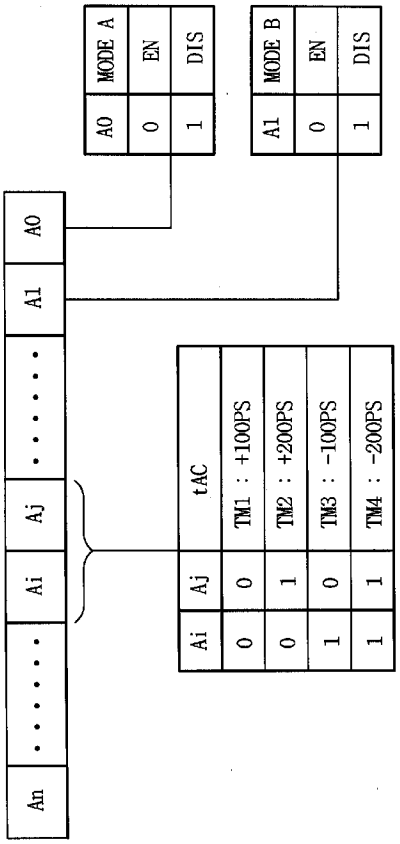
도면3



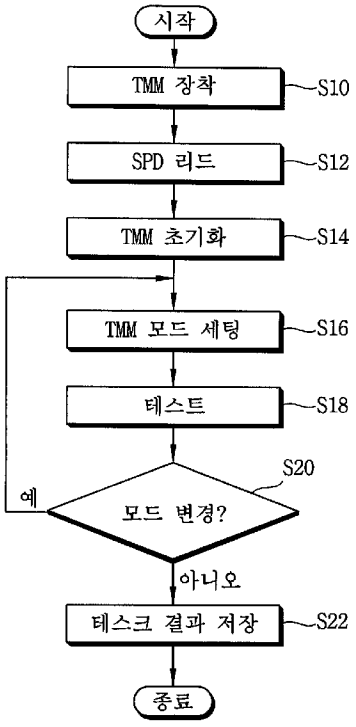



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도면4




도면5






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[続葉有]

(54) **Title**: STACKED MEMORY CHIP, SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING SAME, AND MANUFACTURING METHOD THEREFOR

(54) 発明の名称: 積層メモリチップ、それを用いた半導体集積回路装置及びその製造方法

図1A

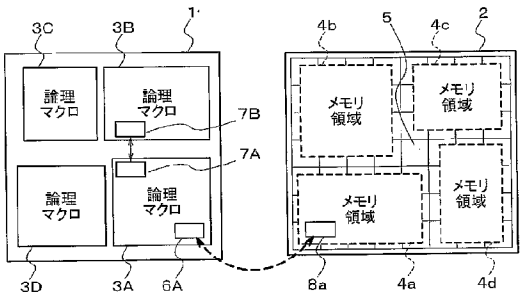
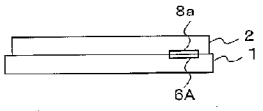



図1B




3C LOGIC MACRO
3D LOGIC MACRO
3B LOGIC MACRO
3A LOGIC MACRO

4b MEMORY AREA
4a MEMORY AREA
4c MEMORY AREA
4d MEMORY AREA

(57) **Abstract**: Memory areas that operate independently for each logic macro of a semiconductor chip cannot be reserved with the memory configuration required by the logic macros. A stacked memory chip stacked on the semiconductor chip comprises a plurality of memory elements arranged in a two-dimensional array, wherein each of the memory elements is provided with an inter-chip I/O section for transmitting a signal between the stacked memory chip and the semiconductor chip, a memory macro capable of writing and reading data, and first wiring for transmitting the data, an address signal, and a command between the adjacent memory elements, and wherein the write data from the semiconductor chip is transferred to the memory macros of the memory elements via the inter-chip I/O sections to perform the write operation, and the data read from the memory macros is transferred to the semiconductor chip via the inter-chip I/O sections.

(57) 要約: 半導体チップの論理マクロごとに独立に動作するメモリ領域を論理マクロが必要とするメモリ構成で確保することができない。 積層メモリチップは、半導体チップ上に積層される積層メモリチップであって、２次元アレイ状に配置された複数のメモリエレメントを備え、各メモリエレメントは、半導体チップとの間で信号を伝送するチップ間Ｉ／Ｏ部と、データの書き込みと読み出しが可能なメモリマクロと、隣接するメモリエレメントとの間でデータ、アドレス信号およびコマンドを伝送する第１の配線とを有し、半導体チップからの書き込みデータを、チップ間Ｉ／Ｏ部を経由してメモリエレメントのメモリマクロへ転送して書き込み動作を行い、メモリマクロから読み出された読み出しデータを、チップ間Ｉ／Ｏ部を経由して半導体チップへ転送する。

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LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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添付公開書類:

— 国際調査報告（条約第 21 条(3)）

# 明細書

## 発明の名称

積層メモリチップ、それを用いた半導体集積回路装置及びその製造方法

## 技術分野

本発明は、論理マクロを複数備えたシステム・オン・チップである半導体チップ上に積層される積層メモリチップ、および半導体チップと積層メモリチップとを積層した半導体集積回路装置及びその製造方法に関するものである。

## 背景技術

携帯電話機などの情報端末機器は音声処理機能や画像処理機能など多機能化が進んでいることから、情報端末機器に使用される半導体チップには多数の論理マクロを搭載することが望まれている。半導体プロセスの微細化に伴い、チップ上に多くの論理マクロを集積することが可能になり、論理マクロの数は多いもので10を超えている。このように多機能を1つのチップ上に集積した半導体チップはシステム・オン・チップ(System on Chip;SoC)と呼ばれている。

論理マクロの多くはCMOS(Complementary Metal Oxide Semiconductor)のロジック回路からなる。それぞれの論理マクロはプログラムやデータの一時記憶用のメモリが必要であり、SRAM(Static Random Access Memory)やDRAM(Dynamic Random Access Memory)、MRAM(Magnetoresistive Random Access Memory)といったメモリを論理マクロの近くに配置している。メモリはアナログ的な回路構成が必要なことから、論理回路とは別に最適化されたトランジスタや記憶素子を用いる。

図49はSoCチップ内の論理マクロとオンチップメモリの構成を示す平面図である。図49のSoCチップ300では、論理マクロごとにオンチップメモリが配置されている。論理マクロ301Aはメモリ302aにアクセスし、論理マクロ301Bはメモリ302bにアクセスし、論理マクロ301Cはメモリ302cにアクセスし、論理マクロ301Dはメモリ302dにアクセスする。303はメモリ302aと接続される論理マクロ301Aの入出力ポート、304は論理マクロ301Aと接続されるメモリ302aの入出力ポート、305は論理マクロ301Bと接続される論理マクロ301Aの入出力ポート、306は論理マクロ301Aと接続される論

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理マクロ301Bの入出力ポートである。オンチップメモリの総面積はチップ全体の1／2近くを占めている。

デジタルの論理回路に比べて、メモリはノイズ耐性が小さく、半導体プロセスの微細化に追従することが難しいためにチップに占めるメモリの面積が増大している。また、扱うデータ量が増加していることも、メモリ面積を増大させている。ゲート長90nm世代のプロセスでは、チップ内に占めるメモリの割合が半分に達している。今までは微細化によって搭載する論理マクロの数を増やせたが、今後はSoCチップ内で論理マクロが使える面積が減少して、マクロ数を増やすことが困難になる。

また、メモリの占有面積が大きくなった場合、多数の論理マクロとメモリをチップ内に配置することで、論理マクロとメモリ間の信号の伝送遅延、あるいは論理マクロと他の論理マクロ間の信号の伝送遅延が大きくなるという問題が生じる。例えば、論理マクロ同士、メモリ同士を集めて配置した場合、メモリから遠いところに配置された論理マクロについては、この論理マクロとアクセスするメモリとの配線距離がチップサイズの半分以上に及ぶことが起こり、論理マクロとメモリ間の伝送遅延が大きくなる。一方、各論理マクロの近傍にそれぞれの論理マクロがアクセスするメモリを配置した場合には、論理マクロとメモリの距離は近くなるが、論理マクロ間に面積が大きいメモリを配置することになり、論理マクロ間の配線距離が長くなって、論理マクロ間の伝送遅延が大きくなる。

チップ内のメモリ面積を削減するために、論理マクロのメモリをオフチップにすることが考えられる。しかし、汎用DRAMに代表されるオフチップメモリでは、入出力部（チップ間I／O部）が一個もしくは数個に限られるので、一個のオフチップメモリで多数の論理マクロごとに独立に動作する複数のメモリ領域を確保することはできない。複数のオフチップメモリを使って論理マクロごとにメモリを独立に動作させることは可能であるが、論理マクロ数に応じたメモリチップ数が必要となる。さらに、論理マクロごとに必要なメモリ容量が異なるために、メモリ構成が固定である汎用品では、過大な容量のメモリチップを使わざるを得ない。

汎用DRAMチップ以外の技術としては、メモリを積層することで大容量化した積層型メモリ装置が提案されている（特許文献1参照）。この積層型メモリ装置はメモリチップ全体で1つのメモリ領域あるいは4つのメモリ領域を構成している。また、チップ外部との複数のデータ入出力部を持っており、データの入出力ビット数を、メモリチップが積層

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されるインターフェースチップで変更可能にしている。

また、メモリと論理マクロを別ダイで積層する集積装置が、特許文献2に提案されている。この集積装置のメモリはメモリバンクを複数持ち、複数の論理マクロとデータのやり取りが可能なようになっている。

特許文献1:特開2006－012337号公報(段落「0020」～「0026」、図1)

特許文献2:特開2008－047079号公報(段落「0026」～「0050」、図4)

## 発明の開示

### 発明が解決しようとする課題

上述した特許文献1に開示された積層型メモリ装置では、メモリの構成が固定されているため、複数の論理マクロのそれぞれに応じて異なる容量の大きさのメモリ領域を1つのメモリチップから多数確保して、メモリ領域を独立に動作させることはできないという問題点があった。

また、上述した特許文献2に開示された集積装置では、ダイ間(チップ間)の入出力ポート(I／O)について、メモリチップ製造後にI／Oの接続数を増減したり、接続位置を選択したりすることができないために、1つの品種のメモリチップを異なる論理マクロ構成のSoCチップに積層することはできないという問題点があった。

本発明の目的は、上述した課題である、半導体チップの論理マクロごとに独立に動作するメモリ領域を論理マクロが必要とするメモリ構成で確保することができないという問題を解決する積層メモリチップ、それを用いた半導体集積回路装置及びその製造方法を提供することにある。

### 課題を解決するための手段

本発明の積層メモリチップは、半導体チップ上に積層される積層メモリチップであって、2次元アレイ状に配置された複数のメモリエレメントを備え、各メモリエレメントは、半導体チップとの間で信号を伝送するチップ間I／O部と、データの書き込みと読み出しが可能なメモリマクロと、隣接するメモリエレメントとの間でデータ、アドレス信号およびコマンドを伝送する第1の配線とを有し、半導体チップからの書き込みデータを、チップ間I／O部を経由してメモリエレメントのメモリマクロへ転送して書き込み動作を行い、メモリマクロから読み出された読み出しデータを、チップ間I／O部を経由して半導体チップへ転

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送する。

本発明の半導体集積回路装置は、積層メモリチップと、積層メモリチップに積層される複数の論理マクロを有する半導体チップとを備え、積層メモリチップは、半導体チップ上に積層される積層メモリチップであって、2次元アレイ状に配置された複数のメモリエレメントを備え、各メモリエレメントは、半導体チップとの間で信号を伝送するチップ間I／O部と、データの書き込みと読み出しが可能なメモリマクロと、隣接するメモリエレメントとの間でデータ、アドレス信号およびコマンドを伝送する第1の配線とを有し、半導体チップからの書き込みデータを、チップ間I／O部を経由してメモリエレメントのメモリマクロへ転送して書き込み動作を行い、メモリマクロから読み出された読み出しデータを、チップ間I／O部を経由して半導体チップへ転送する。

本発明の半導体集積回路装置の製造方法は、多層配線構造を有する半導体チップに、半導体チップに含まれる多層配線構造を構成する電極層の一部からなる第1の接合用電極層を形成し、半導体チップ上に積層され多層配線構造を備えた積層メモリチップに、積層メモリチップに含まれる多層配線構造を構成する電極層の一部からなる第2の接合用電極層を形成し、第1の接合用電極層と第2の接合用電極層とを接合する工程を含み、積層メモリチップは、半導体チップ上に積層される積層メモリチップであって、2次元アレイ状に配置された複数のメモリエレメントを備え、各メモリエレメントは、積層される半導体チップとの間で信号を伝送するチップ間I／O部と、データの書き込みと読み出しが可能なメモリマクロと、隣接するメモリエレメントとの間でデータ、アドレス信号およびコマンドを伝送する第1の配線とを有し、半導体チップからの書き込みデータを、チップ間I／O部を経由してメモリエレメントのメモリマクロへ転送して書き込み動作を行い、メモリマクロから読み出された読み出しデータを、チップ間I／O部を経由して半導体チップへ転送する。

## 発明の効果

本発明によれば、半導体チップの論理マクロごとに独立に動作するメモリ領域を論理マクロが必要とするメモリ構成で確保することができる。

## 図面の簡単な説明

図1Aは本発明の実施形態に係るSoCチップと積層メモリチップの構成を示す平面図である。

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図1Bはフリップチップ実装後のSoCチップと積層メモリチップを模式的に表す断面図である。

図2は本発明の第1の実施形態に係る積層メモリチップの構成を示す平面図、および積層メモリチップのメモリエレメントの構成を示す拡大平面図である。

図3は本発明の第1の実施形態におけるメモリエレメントのSRAMマクロの回路構成を示すブロック図である。

図4は本発明の第1の実施形態におけるメモリエレメントのスイッチファブリックの構成を示す回路図である。

図5は本発明の第1の実施形態におけるメモリエレメントの構成レジスタの構成を示すブロック図である。

図6は本発明の第1の実施形態において複数のメモリエレメント間の構成レジスタ同士の接続を示す図である。

図7は本発明の第1の実施形態において各メモリエレメントを16ビット1kワードの独立のメモリ領域として動作させる場合の接続図である。

図8本は発明の第1の実施形態において4個のメモリエレメントを組み合わせて16ビット4kワードのメモリ領域として動作させる場合の接続図である。

図9は本発明の第1の実施形態において論理マクロとアクセスするメモリ領域が32ビット4kワードの場合の、SoCチップおよび積層メモリチップの構成を示す平面図である。

図10は本発明の第1の実施形態において8個のメモリエレメントを組み合わせて32ビット4kワードのメモリ領域として動作させる場合の接続図である。

図11Aは本発明の第1の実施形態においてSoCチップの論理マクロ内のクロックの配線を示す図である。

図11Bは積層メモリチップのメモリエレメント内のクロックの配線を示す図である。

図12は本発明の第1の実施形態においてメモリ領域およびチップ間I／Oの数や位置をSoCチップに応じて構成する例を示す平面図である。

図13は本発明の第1の実施形態においてメモリ領域およびチップ間I／Oの数や位置をSoCチップに応じて構成する他の例を示す平面図である。

図14は本発明の第1の実施形態においてメモリ領域およびチップ間I／Oの数や位置をSoCチップに応じて構成する他の例を示す平面図である。

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図15は本発明の第1の実施形態においてメモリ領域およびチップ間I／Oの数や位置をSoCチップに応じて構成する他の例を示す平面図である。

図16は本発明の第1の実施形態においてSoCチップの論理マクロに動作中のものと休止中のものが混在する場合のSoCチップと積層メモリチップの構成を示す平面図である。

図17は本発明の第1の実施形態においてSoCチップの論理マクロに動作中のものと休止中のものが混在する場合のSoCチップと積層メモリチップの構成を示す平面図である。

図18は休止中の論理マクロに対向するメモリ領域を含む積層メモリチップの構成を示す平面図である。

図19は休止中の論理マクロに対向するメモリ領域を含む別の積層メモリチップの構成を示す平面図である。

図20は休止中の論理マクロに対向するメモリ領域を含むさらに別の積層メモリチップの構成を示す平面図である。

図21は種類の異なるSRAMマクロを配置した積層メモリチップの構成を示す平面図である。

図22は種類の異なるSRAMマクロを配置した積層メモリチップの構成を示す平面図、およびそれに対応するSoCチップの構成を示す平面図である。

図23は機能回路を備えた積層メモリチップの構成を示す平面図である。

図24は本発明の第1の実施形態においてメモリエレメント間にスクライブ線を設けた場合の積層メモリチップの平面図である。

図25は本発明の第2の実施形態に係る積層メモリチップの構成を示す平面図である。

図26は本発明の第3の実施形態において積層メモリチップを多段に積層した場合の構成を示す断面図である。

図27は本発明の第4の実施形態に係る積層メモリチップの構成を示す平面図である。

図28は本発明の第4の実施形態に係るSoCチップの構成を示す平面図および積層メモリチップの構成を示す平面図である。

図29は本発明の第4の実施形態に係る別の積層メモリチップの概略の構成を示す平

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面図である。

図30は本発明の第1の実施形態に係る積層メモリチップにおけるデータの転送経路を説明するための積層メモリチップの平面図である。

図31は本発明の第5の実施形態に係る積層メモリチップの概略の構成を示す平面図である。

図32は本発明の第5の実施形態に係る積層メモリチップにおけるデータの転送経路を説明するための積層メモリチップの概略の平面図である。

図33は本発明の第5の実施形態に係る積層メモリチップにおいて、メモリ領域を分割して使用する場合の概略の平面図である。

図34は本発明の第5の実施形態に係る積層メモリチップにおいて、2次元メッシュ構造とツリー状構造を合わせた混成構造からなる接続網とした場合の概略の平面図である。

図35は本発明の第5の実施形態に係る積層メモリチップにおいて、スイッチファブリックを多重に配置した構成とした場合の概略の平面図である。

図36は本発明の第6の実施形態に係る積層メモリチップの構成を示す平面図である。

図37は本発明の第7の実施形態に係る積層メモリチップの構成を示す平面図である。

図38は本発明の第8の実施形態に係る積層メモリチップとROMを模式的に表す断面図である。

図39本発明の第9の実施形態に係るSoCチップの構成を示す平面図である。

図40は本発明の第9の実施形態に係るSoCチップの制御信号生成部の構成を示す平面図である。

図41は本発明の第10の実施形態に係る配線部材を配置した構成を模式的に表す断面図、積層メモリチップの構成を示す平面図、およびSoCチップと配線部材の構成を示す平面図である。

図42は本発明の第10の実施形態に係るSoCチップと配線部材の構成を示す平面図である。

図43は本発明の第11の実施形態に係る半導体集積回路装置の断面図である。

図44は本発明の第11の実施形態に係る半導体集積回路装置におけるバンプ電極

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の形成方法を説明するための工程図である。

図45は本発明の第12の実施形態に係る半導体集積回路装置の製造方法を説明するための断面図である。

図46は本発明の第13の実施形態に係る半導体集積回路装置の製造方法を説明するための断面図である。

図47は本発明の第11の実施形態に係る別の半導体集積回路装置の断面図である。

図48は本発明の第11の実施形態に係るさらに別の半導体集積回路装置の断面図である。

図49は関連するSoCチップの構成を示す平面図である。

## 符号の説明

1 SoCチップ

2 積層メモリチップ

3A～3D 論理マクロ

4a～4h メモリ領域

5 メモリエレメント

6A, 6B, 6C, 8a チップ間I／O部

7A, 7B 入出力ポート

9 スクライブ線

10 貫通配線

30 クロック供給源

31 クロック出力部

50 SRAMマクロ

51 チップ間I／O部

52 スイッチファブリック

53 構成レジスタ

54 クロック入力部

55～60 配線

61～64 接続網

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65　クロスバースイッチ

70　制御信号入力部

80　ROM

81　電極

82　ボンディングワイヤ

83　基板

100　制御信号生成部

101　構成リクエスト信号

102　構成制御信号

103　構成獲得信号

110　構成リクエスト調停部

120　制御信号処理部

130　制御信号出力部

200　インターポーザ

210　SoCチップ内配線

220　インターポーザ内配線

500　SRAMメモリセル

501　アドレスデコーダ

502　ワード線ドライバ

503　ライトバッファ

504　リードバッファ

505　センスアンプ

520n, 520s, 520w, 520e, 520ram, 520io　トランスファーゲート・スイッチ

530～532　レジスタ

533　セレクタ

600、700、710　半導体集積回路装置

601、602　多層配線層

603、604　電極パッド

605、606　バンプ電極

607　LORレジスト

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608 PMMAレジスト
609 金(Au)
610 実装ステージ
620 実装ヘッド
630 封止樹脂
701 インダクタ
702 絶縁材料
711 容量パッド

## 発明を実施するための最良の形態

以下に、図面を参照しながら、本発明の実施形態について説明する。

[発明の原理]

図1Aは本発明の実施形態に係るSoCチップと積層メモリチップの代表的な構成例を示す平面図、図1Bはフリップチップ実装後のSoCチップと積層メモリチップを模式的に表す断面図である。なお、図1Aでは、フリップチップ実装時にSoCチップ1と向かい合う面を上にして積層メモリチップ2を記載している。SoCチップ1内には、論理マクロ3A, 3B, 3C, 3Dが配置され、積層メモリチップ2内には、メモリ領域4a, 4b, 4c, 4dが配置されている。

SoCチップ1と積層メモリチップ2とは、フリップチップ実装によってチップ表面同士が配線接続される。このフリップチップ実装では、論理マクロ3Aとメモリ領域4aとが向かい合い、論理マクロ3Bとメモリ領域4bとが向かい合い、論理マクロ3Cとメモリ領域4cとが向かい合い、論理マクロ3Dとメモリ領域4dとが向かい合うように実装される。これにより、論理マクロ3Aのチップ間I／O部6Aは、メモリ領域4aのチップ間I／O部8aと接続される。

本発明の代表的な一例では、SoCチップ1と積層メモリチップ2とを別チップ化することで、SoCチップ1内では、論理マクロ間にメモリが配置されることがなくなり、論理マクロ同士が接近するので、論理マクロ間の伝送遅延を小さくすることができる。図1Aにおいて、7Aは論理マクロ3Bの入出力ポート7Bと接続される論理マクロ3Aの入出力ポートである。

積層メモリチップ2内には、メモリ容量の小さいメモリマクロとチップ間I／O部とを備え

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た複数のメモリエレメント5が2次元状に多数配置されている。一つのメモリエレメント5内のメモリマクロと他のメモリエレメント5内のメモリマクロとの間、メモリエレメント5内のメモリマクロと同じメモリエレメント5内のチップ間I／O部との間、およびメモリエレメント5内のメモリと他のメモリエレメント5内のチップ間I／O部との間で、書き込みデータと読み出しデータとアドレス信号とコマンドとを伝送するための配線が接続されるが、後述するスイッチによって接続の切り離しが可能である。

したがって、積層メモリチップ2内に2次元状に配置された多数のチップ間I／O部の中から、SoCチップ1の接続先の論理マクロのチップ間I／O部の直上にあるものを選択できるため、論理マクロとメモリ領域間の伝送遅延も小さくすることができる。図1Aの例では、積層メモリチップ2のチップ間I／O部8aは、フリップチップ実装時に、論理マクロ3Aのチップ間I／O部6Aの直上に配置され、チップ間I／O部6Aと接続される。

積層メモリチップ2のチップ間I／O部からアクセスできるメモリ領域は、2次元状に配置されたメモリエレメント5の組み合わせによって、任意のビット数、ワード数およびポート数を有する構成を選択可能である。また、メモリ領域4a, 4b, 4c, 4dは、それぞれ複数のメモリエレメント5を組み合わせることによって構成される。本発明では、SoCの機能が変わった場合でも、積層メモリチップ2を新たに作り直す必要は無く、メモリエレメント5の組み合わせを変更することによって、メモリ領域の構成を変更することができ、SoCの機能変更に対応することができる。

[第1の実施形態]

次に、本発明の実施形態について図面を参照して詳細に説明する。図2は本発明の第1の実施形態に係る積層メモリチップ2の構成を示す平面図、および積層メモリチップ2の中の一つのメモリエレメント5の構成を示す拡大平面図である。

図2の例では、積層メモリチップ2内に縦8個×横8個の計64個のメモリエレメント5が2次元状に配置されている。

各メモリエレメント5は、図2に示すように、それぞれ16ビット、1kワードのメモリマクロであるSRAMマクロ50と、チップ間I／O部51と、メモリエレメント間のデータ配線を切り替えるスイッチファブリック52と、メモリ領域の構成をあらかじめ記憶し、スイッチファブリック52の配線スイッチを切り替えるための構成レジスタ53と、SoCチップ1の論理マクロから同期クロックを入力するためのクロック入力部54とを有する。

また、各メモリエレメント5は、4方向にある隣接メモリエレメント5との間で信号転送す

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るための配線55～58を有する。図2の例では、配線55は上方向にある隣接メモリエレメント5と接続される配線、配線56は下方向にある隣接メモリエレメント5と接続される配線、配線57は左方向にある隣接メモリエレメント5と接続される配線、配線58は右方向にある隣接メモリエレメント5と接続される配線である。また、配線59はSRAMマクロ50とスイッチファブリック52との間を接続し、配線60はチップ間I／O部51とスイッチファブリック52との間を接続している。

メモリエレメント5間で転送される信号としては、16ビットの書き込みデータWDと、16ビットの読み出しデータRDと、64個の全メモリエレメント5の中からアクセスするメモリエレメント5を指定するための6ビットのメモリエレメントアドレス信号およびSRAMマクロ50内のワードアドレスを指定するための10ビットのワードアドレス信号の合計16ビットのアドレス信号ADRと、読み出し動作と書き込み動作を指令するための1ビットのコマンドCEと、読み出しと書き込みのどちらかを指定するための1ビットのコマンドWEとがあり、合計で50ビットが必要である。

以下、上方向にある隣接メモリエレメント5との間でやり取りされる信号には添え字として「n」を付し、下方向にある隣接メモリエレメント5との間でやり取りされる信号には添え字として「s」を付し、左方向にある隣接メモリエレメント5との間でやり取りされる信号には添え字として「w」を付し、右方向にある隣接メモリエレメント5との間でやり取りされる信号には添え字として「e」を付し、SRAMマクロ50とスイッチファブリック52との間でやり取りされる信号には添え字として「ram」を付し、チップ間I／O部51とスイッチファブリック52との間でやり取りされる信号には添え字として「io」を付すことにする。

これらの信号は、スイッチファブリック52を経由して、上下左右の隣接する他のメモリエレメント5や、メモリエレメント5内のSRAMマクロ50やチップ間I／O部51に転送される。

図3はSRAMマクロ50の回路構成を示すブロック図である。SRAMマクロ50内には、SRAMメモリセル500が1kワード16ビット構成で設けられている。また、SRAMマクロ50内には、メモリセル500への書き込み動作およびメモリセル500からの読み出し動作について該当するメモリセル500へのアクセスを制御するためのアドレスデコーダ501とワード線ドライバ502とが設けられ、さらにメモリセル500への書き込みデータ伝送のためのライトバッファ503と、メモリセル500からの読み出しデータ伝送のためのリードバッファ504と、データの増幅のためのセンスアンプ505とが設けられている。

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前述のとおり、アドレス信号ADRは、縦8個×横8個の計64個の全メモリエレメント5の中からアクセスするメモリエレメント5を指定するための6ビットのメモリエレメントアドレス信号とSRAMマクロ50内のワードアドレスを指定するための10ビットのワードアドレス信号の合計16ビットある。このうち、6ビットのメモリエレメントアドレスが、制御部506にあらかじめ設定されている自分のメモリエレメントアドレスと一致した場合に、制御部506の後段にあるすべての回路、すなわちアドレスデコーダ501、ワード線ドライバ502、ライトバッファ503、リードバッファ504およびセンスアンプ505が活性化される。

そして、アドレス信号ADRに含まれる10ビットのワードアドレス信号がアドレスデコーダ501に出力される。アドレスデコーダ501は、指定されたワードアドレスに対応するワード線をワード線ドライバ502に選択させる。これにより、指定されたワードアドレスに対応するメモリセル500が選択され、選択されたメモリセル500に対して書き込み動作あるいは読み出し動作が行われる。

図4はスイッチファブリック52の構成を示す回路図である。ただし、図4では、読み出しデータRDを制御するスイッチの回路部分のみを示している。書き込みデータWD、アドレス信号ADR、コマンドCE、コマンドWEを制御するスイッチの回路についても、それぞれ図4と同様に構成することができる。520n, 520s, 520w, 520e, 520ram, 520ioは、トランジスタからなるトランスファーゲート・スイッチである。

トランスファーゲート・スイッチ520nは、図2(B)において上方向にある隣接メモリエレメント5との間で読み出しデータRDnの伝送のオンオフを選択信号CINnに応じて行う。トランスファーゲート・スイッチ520sは、図2(B)において下方向にある隣接メモリエレメント5との間で読み出しデータRDsの伝送のオンオフを選択信号CINsに応じて行う。トランスファーゲート・スイッチ520wは、図2(B)において左方向にある隣接メモリエレメント5との間で読み出しデータRDwの伝送のオンオフを選択信号CINwに応じて行う。トランスファーゲート・スイッチ520eは、図2(B)において右方向にある隣接メモリエレメント5との間で読み出しデータRDwの伝送のオンオフを選択信号CINeに応じて行う。

トランスファーゲート・スイッチ520ramは、同じメモリエレメント5内にあるSRAMマクロ50との間で読み出しデータRDramの伝送のオンオフを選択信号CINramに応じて行う。トランスファーゲート・スイッチ520ioは、同じメモリエレメント5内にあるチップ間I/O部51との間で読み出しデータRDioの伝送のオンオフを選択信号CINioに応じて行う。

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こうして、トランスファーゲート・スイッチ520n, 520s, 520w, 520e, 520ram, 520ioを使って、全ての方向のメモリエレメント5、SRAMマクロ50、チップ間I／O部51との間で接続をオンまたはオフすることが可能である。選択信号CINn, CINs, CINe, CINw, CINram, CINioは、構成レジスタ53から送られる。

図5は構成レジスタ53の構成を示すブロック図、図6は複数のメモリエレメント5間の構成レジスタ53同士の接続を示す図である。ただし、図6の例では、積層メモリチップ2内のメモリエレメント5が縦4個×横4個の計16個の場合を示している。

SoCチップ1は、使用したいメモリ構成に応じた構成制御信号、具体的には図4で説明した6ビットの選択信号CINn, CINs, CINe, CINw, CINram, CINioを積層メモリチップ2の各メモリエレメント5に送る。

本実施形態では、図6に示すように、SoCチップ1から積層メモリチップ2への構成制御信号の入力部を一箇所にして、そこから1つ目のメモリエレメント5に構成制御信号を送り、以下、構成レジスタクロックCclkの1サイクルごとに隣のメモリエレメント5へ構成制御信号を順番に送る。全てのメモリエレメント5へそれぞれの構成制御信号が送られた後に、構成制御信号は構成レジスタ53に保存される。SoCチップ1の制御信号出力手段（不図示）は、所望のメモリ構成に応じた構成制御信号を積層メモリチップ2の該当するメモリエレメント5宛に送る。これにより、メモリエレメント5ごとに独立した構成制御信号を各メモリエレメント5の構成レジスタ53に保存させて、積層メモリチップ2内に所望のメモリ領域を構成することができる。

積層メモリチップ2のメモリ構成を切り替えるには、SoCチップ1からの構成制御信号を新しい構成用にして、送り直すことでも実現できるが、構成レジスタ53に設定される構成制御信号をメモリエレメントごとに数種類保存できるように構成レジスタ53内にレジスタを備えておけば、複数種類の構成制御信号を切り替えることで即座にメモリ構成を切り替えることが可能である。

図5の例では、1つの構成レジスタ53内に6ビットのレジスタ530～532（記憶手段）を3組備えている。これにより、3つのパターンのメモリ構成に対応する3種類の構成制御信号を保存しておくことができ、後段のセレクタ533（選択手段）でスイッチファブリック52に出力する構成制御信号を切り替えることにより、メモリ構成を切り替えることができる。セレクタ533の制御信号は、メモリエレメント5毎にSoCチップ1の制御信号出力手段から与えることができる。

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なお、図5では、スイッチファブリック52のスイッチのうち、読み出しデータRDを制御するスイッチに供給される構成制御信号を切り替える回路部分のみを示している。書き込みデータWD、アドレス信号ADR、コマンドCE、コマンドWEを制御するスイッチに供給される構成制御信号を切り替える回路についても、それぞれ図5と同様に構成することができる。

チップ間I／O部51は、SoCチップ1の論理マクロと積層メモリチップ2のメモリエレメント5との間の通信データを入出力するものである。チップ間I／O部51には、16ビットの書き込みデータWDioのための16個の入力バッファ、16ビットの読み出しデータRDioのための16個の出力バッファ、6ビットのメモリエレメントアドレス信号と10ビットのワードアドレス信号の合計16ビットのアドレス信号ADRioための入力バッファ、読み出し動作と書き込み動作を指令するための1ビットのコマンドCEioのための1個の入力バッファ、読み出しと書き込みのどちらかを指定するための1ビットのコマンドWEioのための1個の入力バッファの計50個のバッファが備えられている。

チップ間I／O部51のチップ間配線は、通常のチップ面内配線のビアをパッドとして、SoCチップ1と積層メモリチップ2間のパッド同士をつないでいる。パッド同士の接続方法としては、間に半田ボールを挟んで熱圧着する方法や、金などのメタルバンプを形成して圧着する方法で可能である。

クロック入力部54は、SoCチップ1の論理マクロと同期するために論理マクロから送信されたクロックを受信するためのチップ間入力バッファである。受信したクロックはメモリエレメント5内のSRAMマクロ50に送られる。

次に、メモリエレメント5を使ったメモリ領域の構成について説明する。個々のメモリエレメント5は、その内部にあるSRAMマクロ50とチップ間I／O部51とを使って独立のメモリ領域として動作できる。上下左右で隣接する全てのメモリエレメント5との配線接続をオフにした場合は、メモリエレメント5のそれぞれが、図7に示すように16ビット、1kワードの独立したメモリ領域4a～4hとなる。ただし、図7では64個のメモリエレメント5のうち、8個のメモリエレメント5についてのみ示している。

図7では、スイッチファブリック52によって接続がオンとなっている配線を実線で表し、接続がオフとなっている配線を破線で表している。図7から明らかなように、各メモリエレメント5において、上方向にある隣接メモリエレメント5との間の配線55、下方向にある隣接メモリエレメント5との間の配線56、左方向にある隣接メモリエレメント5との間

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の配線57、および右方向にある隣接メモリエレメント5との間の配線58のトランスファーゲート・スイッチが全てオフとなっており、SRAMマクロ50との間の配線59およびチップ間I／O部51との間の配線60のトランスファーゲート・スイッチはオンとなっている。

このように積層メモリチップ2のメモリエレメント5の全てを独立動作させると、64個のメモリ領域をSoCチップ1の最大64個の論理マクロとアクセスして並列動作させることが可能になる。

メモリエレメント5を組み合わせることで、1つのメモリ領域のメモリ容量を大きくすることが可能である。スイッチファブリック52をオンにして、例えば図8に示すように4個のメモリエレメント5を組み合わせることで、16ビット、4kワードのメモリ領域4a，4bになる。

メモリ領域4aを構成する4個のメモリエレメント5－1，5－2，5－5，5－6のうち、左下のメモリエレメント5－1においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。右下のメモリエレメント5－2においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。左上のメモリエレメント5－5においては、配線55，57，60のトランスファーゲート・スイッチがオフ、配線56，58，59のトランスファーゲート・スイッチがオンとなっている。右上のメモリエレメント5－6においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。

こうして、4個のメモリエレメント5－1，5－2，5－5，5－6のSRAMマクロ50が全て接続されて1つのメモリ領域4aを構成する。これらのメモリエレメント5－1，5－2，5－5，5－6のうち使用されるチップ間I／O部51は、メモリエレメント5－1のチップ間I／O部51－1のみである。

同様に、メモリ領域4bを構成する4個のメモリエレメント5－3，5－4，5－7，5－8のうち、左下のメモリエレメント5－3においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。右下のメモリエレメント5－4においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。左上のメモリエレメント5－7においては、配線55，57，60のトランスファーゲート・スイッチがオフ、配線56，58，59のトランスファーゲート・スイッチがオンとなっている。右上のメモリエレメント5－8においては、配線55，56，58，60のトランスファーゲート・スイ

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ッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。これらのメモリエレメント5－3，5－4，5－7，5－8のうち使用されるチップ間I／O部51は、メモリエレメント5－3のチップ間I／O部51－3のみである。

また、メモリ領域の入出力のビット数を変更することも可能である。図9は、論理マクロ3Aとアクセスするメモリ領域4aが32ビット4kワードの場合の、SoCチップ1および積層メモリチップ2の構成を示す平面図である。なお、図9では、フリップチップ実装時にSoCチップ1と向かい合う面を上にして積層メモリチップ2を記載している。図1Aの場合と同様に、SoCチップ1と積層メモリチップ2とは、フリップチップ実装によってチップ表面同士が配線接続される。このフリップチップ実装では、論理マクロ3Aとメモリ領域4aとが向かい合い、論理マクロ3Aのチップ間I／O部6Aは、メモリ領域4aの2つのチップ間I／O部8aと接続される。

図9のようにSoCチップ1の論理マクロ3Aとアクセスするメモリ領域4aを32ビット、4kワードに設定する場合は、図10に示すように16ビット、1kワードのメモリエレメント5を8つ組み合わせて1つのメモリ領域4aにする。メモリ領域4aは、メモリ領域4a－1と4a－2とから構成される。メモリ領域4a－1は、メモリエレメント5－1～5－3，5－5から構成され、メモリ領域4a－2は、メモリエレメント5－4，5－6～5－8から構成される。

16ビット、4kワードのメモリ領域4a－1を構成する4個のメモリエレメント5－1～5－3，5－5のうち、メモリエレメント5－1においては、配線55，57，60のトランスファーゲート・スイッチがオフ、配線56，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－2においては、配線55，56，60のトランスファーゲート・スイッチがオフ、配線57，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－3においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－5においては、配線56，57，58のトランスファーゲート・スイッチがオフ、配線55，59，60のトランスファーゲート・スイッチがオンとなっている。こうして、4個のメモリエレメント5－1～5－3，5－5のSRAMマクロ50が全て接続されて1つのメモリ領域4a－1を構成する。これらのメモリエレメント5－1～5－3，5－5のうち使用されるチップ間I／O部は、メモリエレメント5－5のチップ間I／O部51－5のみである。このチップ間I／O部51－5が、図9の2つのチップ間I／O部8aのうちの一方を構成する。

同様に、16ビット、4kワードのメモリ領域4a－2を構成する4個のメモリエレメント5－

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4，5－6～5－8のうち、メモリエレメント5－4においては、配線55，57，58，60のトランスファーゲート・スイッチがオフ、配線56，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－6においては、配線55，56，57のトランスファーゲート・スイッチがオフ、配線58，59，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－7においては、配線55，56，60のトランスファーゲート・スイッチがオフ、配線57，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－8においては、配線56，58，60のトランスファーゲート・スイッチがオフ、配線55，57，59のトランスファーゲート・スイッチがオンとなっている。こうして、4個のメモリエレメント5－4，5－6～5－8のSRAMマクロ50が全て接続されて1つのメモリ領域4a－2を構成する。これらのメモリエレメント5－4，5－6～5－8のうち使用されるチップ間I／O部は、メモリエレメント5－6のチップ間I／O部51－6のみである。このチップ間I／O部51－6が、図9の2つのチップ間I／O部8aのうちの他方を構成する。

8つのメモリエレメント5－1～5－8のうち、メモリエレメント5－5，5－6のチップ間I／O部51－5，51－6が選択された理由は、フリップチップ実装時にチップ間I／O部51－5，51－6が論理マクロ3Aのチップ間I／O部6Aの真上に位置するからである。こうして、16ビット、4kワードのメモリ領域4a－1，4a－2を組み合わせることにより、32ビット、4kワードのメモリ領域4aを構成することができる。

次に、SoCチップ1と積層メモリチップ2との間で行われる書き込み動作、読み出し動作について説明する。メモリへデータを書き込む場合は、SoCチップ1の論理マクロから積層メモリチップ2のチップ間I／O部へメモリエレメントアドレス信号とワードアドレス信号と書き込みのコマンドCE，WEとを入力する。メモリエレメントアドレス信号によって64個のメモリエレメント5のうちの1つが指定され、この指定されたメモリエレメント5のSRAMマクロ50まで書き込みデータWDが転送されるように各メモリエレメント5でスイッチファブリック52の経路が決められる。選択されたメモリエレメント5では、ワードアドレス信号で指定されたワードアドレスにあるSRAMメモリセル500に書き込みデータWDが書き込まれる。

メモリからデータを読み出す場合は、SoCチップ1の論理マクロから積層メモリチップ2のチップ間I／O部へメモリエレメントアドレス信号とワードアドレス信号と読み出しのコマンドCE，WEとを入力する。メモリエレメントアドレス信号によって選択されたメモリエレメント5から、書き込みの場合と逆の経路でチップ間I／O部を経てSoCチップ1の論

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理マクロへ読み出しデータRDが出力される。

次に、積層メモリチップ2のメモリとSoCチップ1の論理マクロとの間のクロック同期手法について説明する。SoCチップ1内はレジスタメモリであるフリップフロップ回路が多数あり、クロック供給源からすべてのフリップフロップ回路まで遅延が揃えられたクロックツリーによって同期クロックが配られる。このクロックツリーの構成に、積層メモリチップ2のメモリエレメント5内のSRAMマクロ50のクロック入力までを加えて、等遅延配線を実現する。

つまり、図11A、図11Bに示すように、SoCチップ1の論理マクロ3のクロック供給源30からフリップフロップFFのクロック入力までの伝送遅延T(FF)と、SoCチップ1のクロック供給源30から積層メモリチップ2のメモリエレメント5のクロック入力部54を経由してSRAMマクロ50のクロック入力までの伝送遅延T(SRAM)とが等しくなるようにすればよい。メモリエレメント5のクロック入力部54に対しては、論理マクロ3のクロック出力部31を介してクロックが供給される。すなわち、フリップチップ実装時に、クロック入力部54は、真下に位置するクロック出力部31と接続される。

等遅延配線は、SoCチップ1のクロック供給源30からクロック出力部31までの伝送遅延T(SOC__OUT)を調整することで実現される。つまり、SoCチップ1と積層メモリチップ2間の伝送遅延T(CHIP__CHIP)と積層メモリチップ2のメモリエレメント5内のクロック入力部54からSRAMマクロ50のクロック入力までの伝送遅延T(RAM__IN)がメモリチップ固有で既知のものであるので、次式が成立するように伝送遅延T(SOC__OUT)をSoCチップ1のクロックツリー生成時に調整する。

$$T(FF)=T(SRAM)$$
$$=T(SOC\_\_OUT)+T(CHIP\_\_CHIP)+T(RAM\_\_IN) \quad \cdots(1)$$

$$T(SOC\_\_OUT)=T(FF)-\{T(CHIP\_\_CHIP)+T(RAM\_\_IN)\} \quad \cdots(2)$$

メモリエレメント5のクロック入力部54へ入力するクロックを、論理マクロに合わせて異なる周波数のものにすることも可能である。つまり、積層メモリチップ2上では、メモリエレメント5毎あるいはメモリ領域毎に異なる周波数の同期クロックが存在することも可能である。

積層メモリチップ2内のメモリ領域は、組み合わせるSoCチップ1によって、再構成す

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ることが可能である。この場合は、SoCチップ1によって1つのメモリ構成を1回限りで構成すればよいので、図5で示したメモリエレメント5の構成レジスタ53は、1組の6ビットレジスタのみを備えていればよい。

次に、積層メモリチップ2の製造後に、メモリ領域およびチップ間I／Oの数や位置を、SoCチップ1に応じて構成する場合を図12、図13、図14、図15を用いて説明する。図12、図13、図14、図15では、図1Aと同様に、フリップチップ実装時にSoCチップ1と向かい合う面を上にして積層メモリチップ2を記載している。また、図12、図13、図14、図15では、図7と同様に、各メモリエレメント5においてスイッチファブリック52によって接続がオンとなっている配線を実線で表し、接続がオフとなっている配線を破線で表している。

図12は積層メモリチップ2の1つのメモリ領域4aをメモリエレメント5－1，5－2，5－5，5－6で構成し、別のメモリ領域4bをメモリエレメント5－3，5－4，5－7，5－8で構成した場合を示している。図12の積層メモリチップ2のメモリ領域4a，4bの構成は、図8に示したものと同じである。SoCチップ1の論理マクロ3Aはチップ間I／O部6Aを介してメモリ領域4aにアクセスし、論理マクロ3Bはチップ間I／O部6Bを介してメモリ領域4bにアクセスする。

図12の場合、論理マクロ3Aとデータをやり取りするメモリ領域4aのチップ間I／O部としては、フリップチップ実装時にチップ間I／O部6Aの真上に位置するメモリエレメント5－1内のチップ間I／O部51－1を選択する。また、論理マクロ3Bとデータをやり取りするメモリ領域4bのチップ間I／O部としては、フリップチップ実装時にチップ間I／O部6Bの真上に位置するメモリエレメント5－3内のチップ間I／O部51－3を選択する。

一方、積層メモリチップ2と組み合わせるSoCチップ1において、図13に示すように、論理マクロ3Aの領域が大きく、論理マクロ3Bの領域が小さい場合が考えられる。論理マクロ3Aが必要とするメモリ領域4aの容量と論理マクロ3Bが必要とするメモリ領域4bの容量を比べて、メモリ領域4aの方が大容量を必要とする場合には、図13に示すようにメモリ領域4aをメモリエレメント5－1，5－2，5－3，5－5，5－6，5－7で構成し、メモリ領域4bをメモリエレメント5－4，5－8で構成する。

メモリ領域4aを構成する6個のメモリエレメント5－1，5－2，5－3，5－5，5－6，5－7のうち、メモリエレメント5－1においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。

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メモリエレメント5－2，5－6においては、配線55，56，60のトランスファーゲート・スイッチがオフ、配線57，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－3，5－7においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。

メモリ領域4bを構成する2個のメモリエレメント5－4，5－8のうち、メモリエレメント5－4においては、配線56，57，58のトランスファーゲート・スイッチがオフ、配線55，59，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－8においては、配線55，57，58，60のトランスファーゲート・スイッチがオフ、配線56，59のトランスファーゲート・スイッチがオンとなっている。

これにより、メモリ領域4aはメモリ領域4bの3倍のメモリ容量を持つ。ただし、メモリ領域4a，4bを構成するメモリエレメント5の数の比は図13の3:1に限定されず、SoCチップ1に応じて設定できる。論理マクロ3Aとデータをやり取りするメモリ領域4aのチップ間I／O部としては、図12（A）と同じメモリエレメント5－1内のチップ間I／O部51－1でよい。また、論理マクロ3Bとデータをやり取りするメモリ領域4bのチップ間I／O部は、メモリエレメント5－4もしくはメモリエレメント5－8のチップ間I／O部から選択する。図13では、メモリエレメント5－4のチップ間I／O部51－4を選択している。

また、図13の代わりに、図14に示すように、メモリ領域4aをメモリエレメント5－1，5－2，5－3，5－4，5－5，5－6で構成し、メモリ領域4bをメモリエレメント5－7，5－8で構成しても良い。

メモリ領域4aを構成する6個のメモリエレメント5－1，5－2，5－3，5－4，5－5，5－6のうち、メモリエレメント5－1においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－2，5－3，5－6においては、配線55，56，60のトランスファーゲート・スイッチがオフ、配線57，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－4においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－5においては、配線55，57，60のトランスファーゲート・スイッチがオフ、配線56，58，59のトランスファーゲート・スイッチがオンとなっている。

メモリ領域4bを構成する2個のメモリエレメント5－7，5－8のうち、メモリエレメント5－7においては、配線55，56，57のトランスファーゲート・スイッチがオフ、配線58，5

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9のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－8においては、配線55，56，58トランスファーゲート・スイッチがオフ、配線57，59，60のトランスファーゲート・スイッチがオンとなっている。図14のメモリ領域4a，4bのメモリ容量は、図13のメモリ領域4a，4bのメモリ容量と同じ大きさである。

論理マクロ3Aとデータをやり取りするメモリ領域4aのチップ間I／O部としては、図13と同じメモリエレメント5－1内のチップ間I／O部51－1でよい。また、論理マクロ3Bとデータをやり取りするメモリ領域4bのチップ間I／O部は、メモリエレメント5－7とメモリエレメント5－8のチップ間I／O部から選択可能である。ただし、論理マクロ3Bの直上に位置するメモリエレメント5－8のチップ間I／O部51－8の方が、チップ間配線が短くなり、チップ間伝送の遅延を小さくできるので、論理マクロ3Bとデータをやり取りするメモリ領域4bのチップ間I／O部として、メモリエレメント5－8のチップ間I／O部51－8を選択する。

このように、本実施形態では、積層メモリチップ2内にチップ間I／O部を2次元状に多数配置することで、接続先のSoCチップ1の論理マクロの近傍にあるチップ間I／O部を選択することが可能になっている。

また、図15に示すように、SoCチップ1の論理マクロ3Cが追加された場合には、メモリ領域4cを追加するように積層メモリチップ2のメモリ領域を再構成することが可能である。論理マクロ3Cは、チップ間I／O部6Cを介してメモリ領域4cにアクセスする。図15では、メモリ領域4aをメモリエレメント5－1，5－2，5－5，5－6で構成し、メモリ領域4bをメモリエレメント5－3，5－4で構成し、メモリ領域4cをメモリエレメント5－7，5－8で構成している。

メモリ領域4aを構成する4個のメモリエレメント5－1，5－2，5－5，5－6のうち、メモリエレメント5－1においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－2，5－6においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－5においては、配線55，57，60のトランスファーゲート・スイッチがオフ、配線56，58，59のトランスファーゲート・スイッチがオンとなっている。

メモリ領域4bを構成する2個のメモリエレメント5－3，5－4のうち、メモリエレメント5－3においては、配線55，56，57のトランスファーゲート・スイッチがオフ、配線58，5

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9，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－4においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファーゲート・スイッチがオンとなっている。メモリ領域4cを構成する2個のメモリエレメント5－7，5－8のうち、メモリエレメント5－7においては、配線55，56，57，60のトランスファーゲート・スイッチがオフ、配線58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－8においては、配線55，56，58のトランスファーゲート・スイッチがオフ、配線57，59，60のトランスファーゲート・スイッチがオンとなっている。

論理マクロ3Aとデータをやり取りするメモリ領域4aのチップ間I／O部としては、図14と同じメモリエレメント5－1内のチップ間I／O部51－1でよい。また、論理マクロ3Bとデータをやり取りするメモリ領域4bのチップ間I／O部としては、メモリエレメント5－3のチップ間I／O部51－3が選択され、論理マクロ3Cとデータをやり取りするメモリ領域4cのチップ間I／O部としては、メモリエレメント5－8のチップ間I／O部51－8が選択される。

また、本実施形態では、積層メモリチップ2の各メモリエレメント5の構成レジスタ53に保存する構成制御信号をあらかじめ数パターン用意してチップ使用中に切り替えることで、メモリ領域の動的な再構成が可能になる。図16、図17は、SoCチップ1の論理マクロに動作中のものと休止中のものが混在する場合のSoCチップ1と積層メモリチップ2の構成を示す平面図である。図16、図17では、図1Aと同様に、フリップチップ実装時にSoCチップ1と向かい合う面を上にして積層メモリチップ2を記載している。また、図16は論理マクロ3Aが動作中で論理マクロ3Bが休止中の場合を示し、図17は論理マクロ3Aが休止中で論理マクロ3Bが動作中の場合を示している。

図16の例のように論理マクロ3Aが動作中で論理マクロ3Bが休止中の場合には、SoCチップ1の制御信号出力手段からの指示により構成制御信号を各メモリエレメント5の構成レジスタ53に選択させることで、メモリ領域4bを構成するメモリエレメント5の個数を少なくし、メモリ領域4aを構成するメモリエレメント5の個数を多くする。これにより、動作中の論理マクロ3Aがアクセスするメモリ領域4aのメモリ容量を大きくすることができる。

一方、図17の例のように論理マクロ3Aが休止中で論理マクロ3Bが動作中の場合には、SoCチップ1の制御信号出力手段からの指示により対応する構成制御信号を

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各メモリエレメント5の構成レジスタ53に選択させることで、メモリ領域4aを構成するメモリエレメント5の個数を少なくし、メモリ領域4bを構成するメモリエレメント5の個数を多くする。これにより、動作中の論理マクロ3Bがアクセスするメモリ領域4bのメモリ容量を大きくすることができる。

このように、本実施形態では、SoCチップ1の論理マクロの動作状況に応じて構成制御信号を切り替えることにより、積層メモリチップ2のメモリ構成を動的に変えることができ、限られたメモリリソースを効率的に使用することができる。

また、このとき、休止中の論理マクロに対応して割り当てられたメモリ領域におけるSRAMマクロの電源をオフとすることによって、積層メモリチップ2の省電力化を図ることができる。図18に、休止中の論理マクロ3Aに対向するメモリ領域4aを含む積層メモリチップ2の構成の一例を示す。図に示すように、各メモリエレメント5のSRAMマクロ50ごとに電源接続スイッチ回路が設けられている。そのため、SRAMマクロ50の電源を個別にオフすることが可能となり、休止中の論理マクロに対応するメモリ領域におけるSRAMマクロの電源をオフにすることができる。

なお、SRAM マクロでは、SRAM の電源をオフにすると保存されていたデータが消去される。休止中であってもデータを保持しておく必要がある場合は、例えば、図19に示すように、休止中のメモリ領域の SRAM マクロ50の電源電圧を通常より低い電圧まで下げることとすることができる。また、図20に示すように、SRAM を構成するトランジスタの基板バイアスを上げることにより、リーク電流を抑制することとしてもよい。さらに、休止中の論理マクロに対応するSRAMマクロのクロック動作周波数を下げることにより、省電力化を図ることとしてもよい。

なお、本実施形態では、各メモリエレメント5内のSRAMマクロ50を1kワード、16ビット構成としたが、これに限るものではなく、任意のワード、ビット構成のものでよい。

また、本実施形態においては、図2に示したメモリエレメント5のSRAMマクロ50は全て、同一種類の16ビット、1kワードの SRAM マクロとして説明した。しかし、これに限らず、数種類のSRAMマクロを配置することとしてもよい。図21に、種類の異なるSRAMマクロ(A、B、C、D)を混在して配置した積層メモリチップの一例を示す。SRAM マクロ(A)は、例えば、16ビット、1kワード、1ポート、読み出し遅延が4nsである基本となる SRAM マクロとすることができる。SRAM マクロ(B)としては、例えば、ビット数とワード数の異なるSRAMマクロとして32ビット、2kワード、1ポート、読み出し遅延が4nsの

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SRAM マクロを用いることができる。また SRAM マクロ(C)は、例えば、読み出し遅延の異なるSRAMマクロとして16ビット、1kワード、1ポート、読み出し遅延が2nsの SRAM マクロとすることができる。さらに SRAM マクロ(D)には、ポート数の異なるメモリマクロとして16ビット、1kワード、2ポート、読み出し遅延が4nsの SRAM マクロを用いることができる。

種類の異なるSRAMマクロを配置した積層メモリチップ2について、さらに具体的に説明する。図22に示すように、SoCチップ1には、例えば、16ビット処理の論理マクロと、これに加えて32ビット処理の論理マクロ、例えば32ビット CPU が配置されている。この CPU がメモリとして32ビット、8kワードのメモリ領域を必要とする場合、基本となる SRAM マクロ(A)だけでメモリ領域を構成すると16個の SRAM マクロが必要となる。これに対して、SRAM マクロ(B)を用いることとすれば4個の SRAM マクロで構成することができる。一つのメモリ領域を構成する SRAM マクロの個数を少なくできれば、メモリ領域内におけるスイッチファブリック数を減らすことができるので、メモリ領域の面積の低減が可能となる。また、SoC チップ1に通常の動作速度の論理マクロと、高速なメモリアクセスが必要な論理マクロ、例えば画像処理アクセラレータとが配置されている場合、アクセラレータ用のメモリとして読み出し遅延が2nsである SRAM マクロ(C)を用いてメモリ領域を構成することができる。さらに、例えばスイッチルータのように、メモリへの読み出しと書き込みのアクセスを頻繁に切り替えることが必要な論理マクロが SoC チップ1に配置されている場合は、SRAM マクロ(D)でメモリ領域を構成することができる。以上述べたように、種類の異なるSRAMマクロを配置した積層メモリチップ2を用いることによって、SoC チップ1が必要とするメモリアクセスの性能を損なわずにメモリ領域を確保することが可能となる。

また、本実施形態では、メモリエレメント5内のメモリマクロをSRAMとしたが、メモリマクロをDRAMとしてもよい。DRAMはSRAMに比べて回路面積が小さいので、より大容量のメモリを搭載することができる。また、メモリエレメント5内のメモリマクロとして、フラッシュメモリやMRAM(Magnetoresistive Random Access Memory)やReRAM(Resistive Random Access Memory)といった不揮発メモリを用いてもよい。不揮発メモリを使うことにより、積層メモリチップ2内で一時的に使用されないメモリ領域の電源を止めて、省電力モードとすることが可能である。

本実施形態では、積層メモリチップ2を構成する各メモリエレメント5は、そえぞれSR

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AMマクロ50を備えるものとして説明したが、これに限らず、SRAMマクロ50以外の機能回路を備えることとしてもよい。図23に、機能回路を備えた積層メモリチップ2の一例を示す。機能回路として、汎用 CPU、周辺回路などを用いることができる。周辺回路には、例えば、外部メモリインターフェース、外部高速通信用シリアルインターフェース、外部無線インターフェース、デジタルーアナログ変換部、電源コントローラ、クロック生成回路などが含まれる。これらの機能回路はメモリエレメント5内の配線に結合される。これらの機能回路はSoCチップ1の品種が変わっても汎用的に使われるものであるため、積層メモリチップ2内にあらかじめ形成し、大量生産することができる。これによって、製造コストの低減を図ることができるという効果が得られる。

また、本実施形態では、積層メモリチップ2内にメモリエレメント5を縦8個×横8個の2次元アレイ状に配置したが、このアレイサイズは他の構成でもよい。

また、本実施形態では、隣接メモリエレメント間の配線を、各メモリエレメント5内のスイッチファブリック52によって電気的にオンオフする構成となっている。これに対して、図24に示すように、メモリエレメント5間にスクライブ線9を設けて、スクライブ線9でメモリエレメント5を物理的に切り離すことを可能にすれば、ウエハの全面にメモリエレメント5のアレイを並べて、必要なメモリ容量に応じたアレイサイズのメモリチップをウエハから切り出すことも可能である。

[第2の実施形態]

次に、本発明の第2の実施形態について説明する。図25は本発明の第2の実施形態に係る積層メモリチップの構成を示す平面図である。図25では、図7と同様に、各メモリエレメント5においてスイッチファブリック52によって接続がオンとなっている配線を実線で表し、接続がオフとなっている配線を破線で表している。本実施形態は、積層メモリチップ2を、擬似的に書き込みポートが1つと読み出しポートが2つあるような2ポートメモリにするものである。

8つのメモリエレメント5－1～5－8のうち、メモリエレメント5－1においては、配線56，57のトランスファーゲート・スイッチがオフ、配線55，58，59，60のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－2，5－3，5－6，5－7においては、配線55，56，60のトランスファーゲート・スイッチがオフ、配線57，58，59のトランスファーゲート・スイッチがオンとなっている。メモリエレメント5－4，5－8においては、配線55，56，58，60のトランスファーゲート・スイッチがオフ、配線57，59のトランスファ

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ーゲート・スイッチがオンとなっている。メモリエレメント5－5においては、配線55，57のトランスファーゲート・スイッチがオフ、配線56，58，59，60のトランスファーゲート・スイッチがオンとなっている。

積層メモリチップ2へデータを書き込む場合は、メモリエレメント5－1のチップ間I／O部51－1を使う。すなわち、SoCチップ1からチップ間I／O部51－1を介してメモリエレメント5－1～5－8に同じ書き込みデータWDを書き込む。

積層メモリチップ2からデータを読み出す場合は、メモリエレメント5－1のチップ間I／O部51－1とメモリエレメント5－5のチップ間I／O部51－5を使う。すなわち、チップ間I／O部51－1を介してメモリエレメント5－1～5－4から読み出しデータRDを読み出すことができ、チップ間I／O部51－5を介してメモリエレメント5－5～5－8から読み出しデータRDを読み出すことができる。このように、メモリエレメント5－1～5－4とメモリエレメント5－5～5－8とから読み出しデータRDを独立に読み出すことが可能である。これにより、本実施形態では、1つのメモリデータ読み出しを待たずに、次のメモリデータを読み出すといった、高速なメモリ読み出し動作が可能である。

[第3の実施形態]

次に、本発明の第3の実施形態について説明する。図26は、本発明の第3の実施形態において積層メモリチップ2を多段に積層した場合の構成を示す断面図である。本実施形態は、積層メモリチップ2を多段に積層した構成を示すものである。

図26に示すように、SoCチップ1から複数の積層メモリチップ2にアクセスできるように、複数の積層メモリチップ2を貫通した貫通配線10を用いる。本実施形態では、SoCチップ1の機能マクロの直上にメモリ領域を拡張することができるので、機能マクロがアクセスするメモリ容量を増加させることができる。

[第4の実施形態]

次に、本発明の第4の実施形態について説明する。第1の実施形態においては、図2に示すように、2次元状に配置された各メモリエレメント間を結合する配線は、2次元メッシュ構造を有する接続網とした。しかし、これに限らず、図27に示す2次元トーラス構造を有する接続網61を用いることもできる。この場合には、図27の左右の端に配置されたメモリエレメント5同士、または上下の端に配置されたメモリエレメント5同士を互いに結合することができる。図27では積層メモリチップ内に縦4個×横4個の計16個のメモリエレメント5が配置されている場合を示す。2次元トーラス構造を採用するこ

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とにより、例えば、図28に示すように、SoCチップ1の端に位置する論理マクロ3Aは、論理マクロ3Aと対向する位置に配置されたメモリ領域4aと連続していないメモリ領域4b、すなわち逆の端に位置するメモリ領域4bを構成するメモリエレメントも使用することが可能となる。そのため、未使用のメモリ領域を減らすことができ、大容量のメモリ領域を効率よく確保することが可能となる。

なお、2次元トーラス構造を有する接続網は図27に示したものに限られず、例えば図29に示すように、隣接する一つのメモリエレメントを跳び越して接続する配線を設けた接続網62としてもよい。図29ではメモリエレメント5同士の配線を見やすくするため、スイッチファブリック52とその間の配線のみを示した。図29に記載した番号を参照すると、各メモリエレメントは、横方向、縦方向ともに1と2、2と3、3と4、4と1が結合している。このような2次元トーラス構造を有する接続網62を採用することにより、メモリエレメント間の配線距離は、2次元メッシュ構造を有する接続網を採用した場合の2倍以下とすることができる。したがって、図27に示した両端のメモリエレメント同士を結合した場合に比べ、配線距離の増加による信号伝送の遅延を抑制することができる。

[第5の実施形態]

次に、本発明の第5の実施形態について説明する。第1の実施形態においては、図2に示すように、2次元状に配置された各メモリエレメント間を結合する配線は、2次元メッシュ構造を有する接続網とした。ここで、一つのメモリ領域の一端に配置されたメモリエレメントから他端に位置するメモリエレメントへデータを送出する場合、データは各メモリエレメント5のスイッチファブリック52を経由して転送される。例えば、図30に示すように、4×4個のメモリエレメントからなるメモリ領域を形成した場合、左上のメモリエレメント5のSRAMマクロ50から右下のメモリエレメント5のチップ間I／O部51にデータを送出するとき、データは7個のスイッチファブリック52を経由する。スイッチファブリック52を図4に示した構成とした場合、データがトランスファーゲート・スイッチを通過する時に遅延が生じる。したがってメモリ領域が大きい場合には、データが経由するスイッチファブリックの数を少なくすることが望ましい。

そこで、本実施形態では図31に示すように、2次元状に配置された各メモリエレメント間を結合する配線は、ツリー状構造を有する接続網63とした。図31ではメモリエレメント5同士の配線を見やすくするため、スイッチファブリック52とその間の配線接続のみを示した。スイッチファブリック52の総数は5個増加するが、増加したスイッチファブリッ

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ク52はスイッチファブリック52とだけ接続され、SRAMマクロやチップ間I／O部と直接接続されることはない。

本実施形態によれば、図32に示すように、4×4個のメモリエレメントからなるメモリ領域を形成した場合、左上のメモリエレメント5のSRAMマクロ50から右下のメモリエレメント5のチップ間I／O部51にデータを送出するとき、データは5個のスイッチファブリック52を経由するだけで足りる。そのため、メモリ領域が大きい場合であっても、メモリ領域内でデータを転送するときの遅延時間を短縮することができる。

一方、図33に示すように、メモリ領域を接続網63のツリー状構造の上下で分割して使用する場合、スイッチファブリック52が1チャンネルのスイッチで構成されているときは、メモリエレメント間の結合が確保できない箇所が生じる。例えば、図33の中央のスイッチファブリックでは4つの方向からの接続のうち、左上のスイッチファブリックと右上のスイッチファブリックからの配線を接続すると、左下と右下のスイッチファブリックからの配線は接続されないことになる。その場合には、例えば図34に示すように、2次元メッシュ構造とツリー状構造を合わせた混成構造からなる接続網64とすることができる。また、図35に示すように、ツリー状構造を有する接続網63にスイッチファブリック52を多重に配置した構成としてもよい。このような構成を採用することにより、メモリ領域を接続網を構成するツリー状構造の上下で分割して使用する場合であっても、全ての配線の接続を確保することができる。

[第6の実施形態]

次に、本発明の第6の実施形態について説明する。第1の実施形態においては、図2に示すように、2次元状に配置された各メモリエレメントはスイッチファブリック52を介して配線55～60により接続する構成とした。それに対して本実施形態では、図36に示すように、クロスバースイッチ65を備え、各メモリエレメント5間をクロスバー結合する構成とした。これにより、一つのクロスバースイッチ65を経由させるだけで、すべてのメモリエレメント5間のデータの送受信が可能となる。第1の実施形態における積層メモリチップにおいては、各メモリエレメント毎にスイッチファブリックを備えた構成としたが、本実施形態によればスイッチファブリックは不要になるので、各メモリエレメントの構成を簡潔にすることができる。なお、クロスバースイッチ65としては、一般に使用されているクロスバースイッチ回路を用いることができ、これにより、2つのメモリエレメント間の接続を複数個形成することができる。

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[第7の実施形態]

次に、本発明の第7の実施形態について説明する。第1の実施形態においては、図6に示したように、SoCチップから送出された構成制御信号は、積層メモリチップの一カ所から入力する構成とした。それに対して本実施形態では、積層メモリチップの複数箇所から構成制御信号を入力する構成とした。図37に、各メモリエレメント5毎に、構成レジスタ53と接続した制御信号入力部70を設けた構成を示す。本実施形態による積層メモリチップにおいては、構成制御信号をSoCチップから各メモリエレメント5に対して並列的に送出できるので、各メモリエレメント5の構成レジスタ53に構成制御信号を短時間でセットすることができる。これにより、構成レジスタ53が1組のレジスタしか備えていない場合であっても、メモリ構成の切り替えを短時間に完了することができるので、構成レジスタ53の構成を簡略化することができる。

[第8の実施形態]

次に、本発明の第8の実施形態について説明する。第1の実施形態においては、構成制御信号はSoCチップから積層メモリチップに送られることとしたが、これに限らず、SoCチップ以外の外部装置から積層メモリチップに構成制御信号を送出することとしてもよい。本実施形態では、図38に示すように、積層メモリチップ2の外部にROM(Read Only Memory)80を設け、積層メモリチップ2はROM80から構成制御信号を読み込む構成とした。積層メモリチップ2とROM80の接続は、それぞれと接続する電極81を設け、電極81間をボンディングワイヤ82を用いて接続することにより行うことができる。

本実施形態では、まず、積層メモリチップ2とSoCチップ1を基板83上に構成したデバイスを製造した。そして、このデバイスの製造時、あるいはデバイス使用者がデバイスを使用する前に、構成制御信号をROM80に書き込む。次に、このデバイスの使用を開始する時に、ROM80に記録された構成制御信号を積層メモリチップ2へ送信させ、構成制御信号に基づいて積層メモリチップ2にメモリ領域を構成する。このように本実施形態によれば、デバイス製造者あるいはデバイス使用者が直接、メモリ領域を構成することができる。図38は、ROM80をデバイスと同一の基板83上に配置した場合を示しているが、ROM80をデバイスの上に積層する構成としてもよい。また本実施形態では、構成制御信号はROM80から送信することとしたが、これに限らず、FPGA(Field Programmable Gate Array)、CPU(Central Processing Unit)あるい

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は別のSoCチップなどの半導体装置を用いることとしてもよい。

[第9の実施形態]

次に、本発明の第9の実施形態について説明する。図39に示すように、本実施形態におけるSoCチップ1は制御信号生成部100を備えている。制御信号生成部100は、論理マクロの動作状況に応じて、メモリ領域を構成するための制御信号を生成する。SoCチップ1に複数搭載された論理マクロ3は、各論理マクロ3の動作状況に応じて構成リクエスト信号101を制御信号生成部100に送る。構成リクエスト信号101は、各論理マクロ3が必要とするメモリ領域の大きさであるメモリエレメント数を示すものであり、例えば、メモリエレメント数が全部で16ある場合は4ビットの信号となる。

図40に示すように、制御信号生成部100は、構成リクエスト調停部110と、制御信号処理部120と、制御信号出力部130を備えている。構成リクエスト調停部110は、複数の論理マクロ3から構成リクエスト信号101を受け取り、リクエストの優先順位にしたがって、各論理マクロ3に割り当てられるメモリ領域の大きさ、つまりメモリエレメント数を決定する。制御信号処理部120は、決定したメモリ領域の大きさに基づいて、積層メモリチップ2におけるメモリ領域の再構成を行うために必要なメモリエレメント毎の構成制御信号102を生成する。構成制御信号102は制御信号出力部130を介して積層メモリチップ2に送出される。

ここで、構成制御信号102は各メモリエレメントのスイッチファブリックの選択信号となるCINn、CINe、CINs、CINw、CINram、CINioの6ビット信号である。例えば、メモリエレメント数が全部で16ある場合は、6ビットの構成制御信号がメモリエレメント数に対応して16個必要となる。この場合、生成された構成制御信号を6×16ビット構成のレジスタに保存しておき、クロックの1サイクルで6ビットずつレジスタから取り出し、制御信号出力部130を介して積層メモリチップ2に送出することができる。

制御信号処理部120は、構成制御信号102を制御信号出力部130を介して積層メモリチップ2へ送出するとともに、各論理マクロ3が積層メモリチップ2のメモリ領域に獲得できたメモリエレメント数を示す構成獲得信号103を各論理マクロ3に送信する。構成獲得信号103もメモリエレメント数が全部で16ある場合は4ビットの信号となる。

各論理マクロ3からのリクエストの優先順位の決定には、固定優先順位とする方式、またはラウンドロビン型で優先順位が毎回入れ替わる方式などを用いることができる。また、優先順位にしたがってメモリ領域を割り当てるときに、優先順位の最も高い論理

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マクロにメモリ領域の100%を割り当てる方法、あるいは、優先順位に従ってメモリ領域の比率を決定し各論理マクロに割り当てる方法などを用いることができる。また例えば、ある一定量の大きさのメモリ領域はそれぞれの論理マクロが常に占有し、それ以外のメモリ領域について優先順位にしたがって割り当てることとしてもよい。

[第10の実施形態]

次に、本発明の第10の実施形態について説明する。本実施形態では図41に示すように、積層メモリチップ2とSoCチップ1の間に配線部材を配置した構成とした。本実施形態では配線部材としてインターポーザ200を用いた。インターポーザは半導体チップの製造プロセスとは別に配線層だけを形成した基板であり、樹脂基板あるいはシリコン(Si)基板などを用いて製造される。本実施形態によれば、積層メモリチップ2のサイズがSoCチップ1よりも大きく、積層メモリチップ2上にSoCチップ1と重ならない領域が存在する場合であっても、その領域に配置されたメモリエレメントに対してはインターポーザ200を介してクロックを分配することができる。したがって、この場合でも各メモリエレメントのクロック入力部54におけるクロックの遅延差を小さくすることができる。すなわち、SoCチップ1内の配線とインターポーザ200の配線の両方を経由させることによって、SoCチップ1内のクロック供給源30から積層メモリチップ2のクロック入力部54までを等遅延配線とすることができる。

さらに具体的に説明すると、例えば、図41に示すように、積層メモリチップ2の左上の4個のメモリエレメント5からメモリ領域を構成するとした場合、その4個の中の右下のメモリエレメント以外の3つのメモリエレメントは、SoCチップ1と重なっていない。本実施形態によれば図42に示すように、クロック分配の経路において、SoCチップ内配線210に接続してインターポーザ内配線220を用いることができるので、積層メモリチップ2上にSoCチップ1と重ならない領域が存在する場合であっても、等遅延配線を実現することができる。

図41には、積層メモリチップ2のサイズがSoCチップ1よりも大きく、SoCチップ1の全体を覆っている場合を示したが、これに限らず、積層メモリチップ2の一部にSoCチップ1と重ならない領域が存在する場合であれば、本実施形態を適用することにより重なっていない領域を含めた等遅延配線が可能である。また、ここでは、クロック分配の配線の一部にインターポーザ配線を用いる場合について説明したが、これに限らず、データ、アドレス信号、またはコマンド信号を伝送する配線の一部としてインターポーザ配線を

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用いることとしてもよい。この場合、本実施形態によれば、インターポーザ配線をメモリエレメントのチップ間I／O部に接続することにより、SoCチップ1と重ならない積層メモリチップ2上の領域に形成されたメモリエレメントに対しても配線が可能となる。そのため、メモリ領域を構成する時に選択可能なメモリエレメントの数を増大させることができる。

[第11の実施形態]

次に、本発明の第11の実施形態について説明する。図43に、本実施形態による半導体集積回路装置600の断面図を示す。SoCチップ1および積層メモリチップ2には、それぞれ多層配線層601、602が形成されている。そして、この多層配線構造601、602を構成する電極層の一部からなる接合用電極層が、SoCチップ1および積層メモリチップ2の表層の所定の位置にそれぞれ形成されている。本実施形態では、接合用電極層としてSoCチップ側の電極パッド603および積層メモリチップ側の電極パッド604をそれぞれ形成した。ここで、多層配線601、602及び電極パッド603、604に用いる材料は特に限定されることはなく、半導体集積回路装置において一般的に使用されているCu、Al等を用いることができる。

SoCチップ側の電極パッド603の上には、接合部材としてSoCチップ側のバンプ電極605が、積層メモリチップ側の電極パッド604には、積層メモリチップ側のバンプ電極606がそれぞれ形成されている。これらのバンプ電極は、半導体集積回路装置600の製造時に、それぞれが対応する位置に位置合わせされ、バンプ電極同士が電気的に接続された状態となっている。その結果、SoCチップ1と積層メモリチップ2間の信号伝送が可能となっている。バンプ電極605、606に用いる材料は特に限定されることはなく、半導体集積回路装置において一般的に用いられている材料を使用することができる。例えば、Au、Cu、半田等の金属を用いることができる。半田バンプ材料の例としては、Sn／Pb、Sn／Ag、Sn／Cu、Sn／Zn、Sn／Biおよびこれらの材料に特定の添加元素をさらに加えた材料であってもよく、これらを適宜用いることができる。

バンプ電極同士の電気的接続方法としては、Auバンプを用いる場合、実装時の加熱加圧による金属拡散接合が適している。その他の方法として、それぞれのバンプ表面を接触状態に保ち、導通を確保する方法を用いることもできる。このバンプ表面同士を接触状態に保つ方法としては、SoCチップ1と積層メモリチップ2との隙間を樹脂封止し、封止に用いた樹脂の収縮力および実装時の加熱加圧を利用する方法を用いることができる。バンプ電極に半田を使用する場合は、半田の溶融温度である200℃～

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250℃程度まで加熱し、半田を溶融することにより他方のバンプ表面に濡らして接続する融着接続を用いることができる。この場合は、実装時の加圧を低減することができる。Cuバンプの場合、上述した接触により導通を確保する方法の他、プラズマ処理等によりCuバンプ表面を活性化した状態で実装し、電気的接続を得る方法を用いることができる。また、AuバンプやCuバンプの表面に半田を形成し、バンプの表面部分において溶融接続させることとしてもよい。

次に、図44を用いて、本実施形態における積層メモリチップ側の電極パッド604の上にバンプ電極606を形成する第1の方法について説明する。まず、図44Aに示すような電極パッド604が形成された積層メモリチップ2を準備する。

次に図44Bに示すように、レジスト塗布を行う。LOR(Lift－Off Resist)レジスト607をスピンコート法により塗布し、この上にポジ型電子ビームレジストであるPMMA(Poly methyl methacrylate)レジスト608を塗布する。レジスト塗布後にベーキングを行う。LORレジスト607の膜厚は、この後に形成する電極の膜厚以上であることが望ましい。

続いて図44Cに示すように、電子ビーム露光法を用いてPMMAレジスト608により電極用のパターンを形成する。PMMAレジスト608の現像にはMIBK(Methyl Isobutyl Ketone)とIPA(Isopropyl Alcohol)の混合溶液を用いることができる。パターニングされたPMMAレジスト608をマスクとしてLORレジスト607をTMAH(Tetra Methyl Ammonium Hydroxide)溶液でエッチング除去し、レジストパターンを形成する(図44D)。このとき、PMMAレジスト608で被覆されたLORレジスト607も一部エッチング除去され、PMMAレジスト608のオーバーハングがパターンの周囲に形成される。このオーバーハングにより、この後のリフトオフ工程が容易になるという効果が得られる。

TMAH溶液を用いてLORレジスト607を除去した箇所には、残渣が残る場合がある。この残渣は金(Au)電極の基板への密着性を下げ、また、電気抵抗を増加させる原因となるため、除去することが望ましい。このレジストの残渣は酸素プラズマ中でアッシング処理を行うことにより取り除くことができる。また、アッシングの後に希フッ酸等でエッチングを行うことにより、アッシング処理中または大気中への暴露によって生じた表面上の銅酸化物を除去することとしてもよい。

次に図44Eに示すように電極形成工程を行う。電子ビーム蒸着法によりバンプ電極

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606として金(Au)609を堆積する。基板との密着性を確保するために、金(Au)609の蒸着前に、チタンを堆積し、さらに、金(Au)609を所定の厚さで堆積することとしてもよい。電子ビーム蒸着後、アセトン等の溶液にレジストを溶解させ、レジスト上に堆積した金(Au)をリフトオフを用いて除去することにより、バンプ電極606が完成する(図4F)。その後、エタノール等を用いてアセトンを取り除き、水洗を行う。上述したように本実施形態では、金(Au)609の堆積には電子ビーム蒸着法を用いることとしたが、これに替えてスパッタ法やパルスレーザー蒸着法など他の堆積方法を用いることとしてもよい。

次に、積層メモリチップ側の電極パッド604の上にバンプ電極606を形成する第2の方法について説明する。第1の方法においては、リフトオフにより電極パターンを形成することとしたが、これに限らず、以下に述べるように金属を堆積させた後に、エッチング法により電極パターンを形成することとしてもよい。

まず、大気中への暴露によって生じる銅表面の酸化物を希フッ酸を用いたエッチングにより除去する。続いて、電子ビーム蒸着法により金(Au)を所定の厚さで堆積する。基板との密着性を確保するため、金(Au)の蒸着前にチタンを堆積することとしてもよい。次に、ネガ型電子ビームレジストを塗布した後にベーキングを行い、電子ビーム露光法を用いてレジストに電極パターンを形成する。

続いて、ヨウ化カリウム溶液を用いてレジストで覆われた電極パターン部分以外の金(Au)をエッチングにより除去する。さらに、過酸化水素とフッ酸を純水で希釈したエッチング液を用いてチタンをエッチングにより除去する。最後に、酸素プラズマアッシングを用いてネガ型電子ビームレジストを除去し、バンプ電極606が完成する。

[第12の実施形態]

次に、本発明の第12の実施形態について説明する。図45A、45Bは、本実施形態による半導体集積回路装置の製造方法を説明するための断面図である。SoCチップ1および積層メモリチップ2には、それぞれ多層配線層601、602が形成されている。そして、この多層配線構造601、602を構成する電極層の一部からなる接合用電極層が、SoCチップ1および積層メモリチップ2の表層の所定の位置にそれぞれ形成されている。本実施形態では、接合用電極層としてSoCチップ側の電極パッド603および積層メモリチップ側の電極パッド604をそれぞれ形成し、SoCチップ側の電極パッド603の上には、接合部材としてSoCチップ側のバンプ電極605を、積層メモリチップ側の

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電極パッド604の上には、積層メモリチップ側のバンプ電極606をそれぞれ形成した。

次に、SoCチップ1を実装装置の実装ステージ610に吸着等により固定する。SoCチップ1の裏面は実装ステージ610に接しており、バンプ電極605の表面が図45A中の上方向を向いている。なお、実装ステージ610は吸着固定機能、平面(x−y)駆動機能、加熱機能、接合面高さ調整機能を備えていることが望ましい。

続いて、積層メモリチップ2を実装装置の実装ヘッド620に吸着固定する。このとき実装ヘッド620は積層メモリチップ2の裏面に接しており、バンプ電極606の表面が図45A中の下方向を向いている。なお、この実装ヘッド620はチップ吸着固定機能、θ駆動機能、加熱機能、接合高さ調整機能を備えていることが望ましい。

図45Aに示すように、SoCチップ1と積層メモリチップ2は、それぞれのバンプ電極605、606の表面が対面している。SoCチップ1と積層メモリチップ2の位置合わせ工程では、まず、それぞれのチップの位置合わせに必要なアライメントマークの撮像を行う。アライメントマークは電極パッドの作製工程またはバンプ電極の作製工程において作製することが望ましい。一般的には、チップの対角線上の角部付近の2箇所に設けることが望ましい。このとき、SoCチップ 1 と積層メモリチップ2の熱膨張係数が等しい場合は、実装ヘッド620と実装ステージ610の温度を同等にすることで、熱膨張係数の相違による認識座標位置ずれを防止することができる。続いて、認識した2点のアライメントマーク座標データから、SoCチップ1と積層メモリチップ2の位置合わせを行う。

次に、図45Bに示すように、積層メモリチップ2をSoCチップ1上に搭載し、加熱加圧により、積層メモリチップ側のバンプ電極606とSoCチップ側のバンプ電極605の電気的接続を行う。それぞれのバンプ電極が金(Au)材料からなる場合、実装時の加熱加圧によりAu拡散接合を行うことにより、SoCチップ1と積層メモリチップ2間の電気的接続が可能となる。

このとき、SoCチップ1と積層メモリチップ2の隙間、すなわちバンプ電極605、606の接続部周囲を絶縁樹脂等で封止することにより、実用時における接続信頼性等を向上させることができる。封止に使用する樹脂としては、エポキシ樹脂、ポリイミド樹脂、シリコーン樹脂等を用いることができるが、これに限らず、これらの樹脂を1種あるいは2 種以上組み合わせて用いることとしてもよいし、シリカ等の無機充填剤等を混合することもできる。エポキシ樹脂を用いる場合、充填後の樹脂を約100～200℃程度で硬化させることにより、本実施形態による半導体集積回路装置が完成する。

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樹脂封止には、通常一般的に使用される方法、例えば、SoCチップ1と積層メモリチップ2の隙間に毛細管現象を利用して液状の樹脂を充填し、充填後に樹脂を硬化させる方法等を用いることができる。この場合に使用する樹脂としては、充填時に重要となる樹脂の粘度物性等を考慮すると、エポキシ樹脂を好適に用いることができる。ここで、樹脂を充填する前に、SoCチップ1または積層メモリチップ2の樹脂充填領域の表面をプラズマ処理等により改質し、樹脂濡れ性を高めておくことにより、樹脂充填性を向上させることができる。これに限らず、真空中で樹脂充填した後に大気圧を利用して樹脂充填を促進させる方法、加圧しながら樹脂硬化を行う方法等によっても、樹脂充填性を向上させることができる。

[第13の実施形態]

次に、本発明の第13の実施形態について説明する。図46A、46Bは、本実施形態による半導体集積回路装置の製造方法を説明するための断面図である。SoCチップ1および積層メモリチップ2には、それぞれ多層配線層601、602が形成されている。そして、この多層配線構造601、602を構成する電極層の一部からなる接合用電極層が、SoCチップ1および積層メモリチップ2の表層の所定の位置にそれぞれ形成されている。本実施形態では、接合用電極層としてSoCチップ側の電極パッド603および積層メモリチップ側の電極パッド604をそれぞれ形成し、SoCチップ側の電極パッド603の上には、接合部材としてSoCチップ側のバンプ電極605を、積層メモリチップ側の電極パッド604の上には、積層メモリチップ側のバンプ電極606をそれぞれ形成した。

図46Aに示すように、本実施形態では第12の実施形態と異なり、SoCチップ1と積層メモリチップ2の表面に、実装前にあらかじめ封止材料として封止樹脂630が形成されている。図46Aでは、SoCチップ1および積層メモリチップ2の両方のチップに封止樹脂630を形成した場合を示す。封止樹脂630を形成した後に、形成時の余剰な樹脂を除去し、SoCチップ側のバンプ電極605および積層メモリチップ側のバンプ電極606の接続部表面を露出させることにより、バンプ電極605、606の接続特性を向上させることができる。封止樹脂630の材料には、第12の実施形態と同様に、エポキシ樹脂、ポリイミド樹脂、シリコーン樹脂等を用いることができる。また、これに限らず、これらの樹脂を1種あるいは2種以上組み合わせて用いることとしてもよいし、シリカ等の無機充填剤等を混合することもできる。

SoCチップ1または積層メモリチップ2の表面への樹脂供給方法としては、フィルム上

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に加工した樹脂をラミネータによりチップ表面に供給する方法、液状の樹脂をスピンコート法や印刷法により供給し仮硬化する方法などを用いることができる。また、余剰の樹脂を除去し、バンプ電極の表面を露出させる方法としては、例えば、精密加工が可能なバイトを使用した機械加工による方法を用いることができる。なお、バンプ電極の表面を露出させる必要がない場合には、SoCチップ1または積層メモリチップ2のいずれか一方にのみ封止樹脂630を形成することとしてもよい。また、SoCチップ1と積層メモリチップ2を実装する直前に、適正量の液状樹脂をSoCチップ1の表面上に塗布することによっても封止樹脂630を形成することができる。

次に、図46Bに示すように、積層メモリチップ2をSoCチップ1上に搭載し、加熱・加圧処理を施す。これにより、積層メモリチップ側のバンプ電極606とSoCチップ側のバンプ電極605が電気的に接続され、同時に封止樹脂630が硬化することによって本実施形態による半導体集積回路装置が完成する。バンプ電極の材料には金(Au)を用いることができ、第12の実施形態の場合と同様の条件でAu拡散接合を行うことができる。本実施形態では、バンプ接続と樹脂封止を同時に行うこととしたので、バンプ電極の電気的接続が接触だけの場合であっても、搭載時の加圧および封止樹脂630の硬化収縮時の応力により、電気的接続を良好に保持することができる。

上述した第11の実施形態においては、SoC チップ1と積層メモリチップ2とがバンプ電極によって電気的に接続され、チップ間の信号伝送を行う場合について説明した。しかし、これに限らず、チップ間で電気的な接続を行わない状態で信号伝送を行うこととしてもよい。

例えば、図47に示す半導体集積回路装置700のように、SoC チップ1と積層メモリチップ2のそれぞれの表面にインダクタ701を形成し、チップ間に絶縁材料702を挟んでインダクタ701同士の磁界結合によって信号を伝送することとしてもよい。また、図48に示す半導体集積回路装置710のように、SoC チップ1と積層メモリチップ2のそれぞれの表面に容量パッド711を形成し、チップ間に絶縁材料702を挟んで容量パッド711同士の容量結合によって信号を伝送することとしてもよい。これらの伝送方式を用いた半導体集積回路装置700、710においては、チップ間で電気的な接続を行わないため、静電気によるチップ内の回路破壊が生じる危険を回避することができる、という効果が得られる。

本発明は上記実施形態に限定されることなく、特許請求の範囲に記載した発明の範

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囲内で、種々の変形が可能であり、それらも本発明の範囲内に含まれるものであることはいうまでもない。

この出願は、２００８年８月２２日に出願された日本出願特願２００８－２１３６７０および２００９年２月５日に出願された日本出願特願２００９－０２４５０１を基礎とする優先権を主張し、その開示の全てをここに取り込む。

## 産業上の利用可能性

本発明は、多数の論理マクロを備えたシステム・オン・チップである半導体チップがアクセスするメモリチップに適用することができる。

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# 請求の範囲

[請求項1] 半導体チップ上に積層される積層メモリチップであって、

2次元アレイ状に配置された複数のメモリエレメントを備え、

各メモリエレメントは、前記半導体チップとの間で信号を伝送するチップ間I／O部と、データの書き込みと読み出しが可能なメモリマクロと、隣接するメモリエレメントとの間でデータ、アドレス信号およびコマンドを伝送する第1の配線とを有し、

前記半導体チップからの書き込みデータを、前記チップ間I／O部を経由して前記メモリエレメントのメモリマクロへ転送して書き込み動作を行い、前記メモリマクロから読み出された読み出しデータを、前記チップ間I／O部を経由して前記半導体チップへ転送することを特徴とする積層メモリチップ。

[請求項2] 請求項1記載の積層メモリチップにおいて、

さらに、各メモリエレメントは、前記第1の配線、この第1の配線と前記チップ間I／O部との間の第2の配線、および前記第1の配線と前記メモリマクロとの間の第3の配線を個別にオンオフ可能なスイッチファブリックと、

このスイッチファブリックを制御する制御信号を出力するレジスタとを有することを特徴とする積層メモリチップ。

[請求項3] 請求項2記載の積層メモリチップにおいて、

前記スイッチファブリックは、前記レジスタから出力される制御信号に応じて前記第1、第2、第3の配線を配線毎およびメモリエレメント毎にオンオフして、前記メモリエレメントを組み合わせることにより、前記半導体チップが前記チップ間I／O部を経由してアクセスするメモリ領域を所望のビット数、ワード数、ポート数で構成することを特徴とする積層メモリチップ。

[請求項4] 請求項2記載の積層メモリチップにおいて、

前記スイッチファブリックは、前記レジスタから出力される制御信号に応じて前記第1、第2、第3の配線を配線毎およびメモリエレメント毎にオンオフすることにより、各メモリエレメントの前記チップ間I／O部のうち、積層メモリチップにアクセスする半導体チップの論理マクロの近傍に存在するものを、この論理マクロと接続されるチップ間I／O部として選択することを特徴とする積層メモリチップ。

[請求項5] 請求項2記載の積層メモリチップにおいて、

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前記制御信号は、論理マクロを複数備えたシステム・オン・チップである前記半導体チップから出力されて前記レジスタに保持されるものであり、

それぞれの前記論理マクロがアクセスするメモリ領域が1つ以上の前記メモリエレメントの組み合わせで構成され、かつそれぞれのメモリ領域が独立に動作することを特徴とする積層メモリチップ。

[請求項6] 請求項2記載の積層メモリチップにおいて、

前記レジスタは、

複数種類の前記制御信号を保持する複数の記憶手段と、

前記複数種類の制御信号のうちいずれか1つを選択して前記スイッチファブリックに出力する選択手段とからなることを特徴とする積層メモリチップ。

[請求項7] 請求項2記載の積層メモリチップにおいて、

さらに、各メモリエレメントは、メモリエレメント毎に前記半導体チップの論理マクロと前記メモリマクロとを同期させるクロックを前記半導体チップから受信するクロック入力部を有することを特徴とする積層メモリチップ。

[請求項8] 請求項3記載の積層メモリチップにおいて、

前記スイッチファブリックは、前記半導体チップの論理マクロの構成に従って前記半導体チップから出力される前記制御信号に応じて前記第1、第2、第3の配線を配線毎およびメモリエレメント毎にオンオフして、前記メモリエレメントを組み合わせることにより、前記メモリ領域を構成するメモリエレメントの組み合わせを変更することを特徴とする積層メモリチップ。

[請求項9] 請求項8記載の積層メモリチップにおいて、

前記制御信号は、前記半導体チップの論理マクロの動作状況に応じて出力されることを特徴とする積層メモリチップ。

[請求項10] 請求項2記載の積層メモリチップにおいて、

前記スイッチファブリックは、前記レジスタから出力される制御信号に応じて前記第1、第2、第3の配線を配線毎およびメモリエレメント毎にオンオフすることにより、前記メモリエレメントを組み合わせてメモリ領域を構成すると共に、このメモリ領域を構成するメモリエレメントの2つのチップ間I／O部を使用可能とするものであり、

前記半導体チップからの書き込みデータを、使用可能な前記2つのチップ間I／O部のうち一方のチップ間I／O部を経由して前記メモリ領域を構成する各メモリエレメン

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トのメモリマクロへ転送して書き込み動作を行い、前記メモリ領域を構成する一部のメモリエレメントのメモリマクロから読み出された読み出しデータを、使用可能な前記2つのチップ間I／O部のうち一方のチップ間I／O部を経由して前記半導体チップへ転送すると共に、前記メモリ領域を構成する残りのメモリエレメントのメモリマクロから読み出された読み出しデータを、使用可能な前記2つのチップ間I／O部のうち他方のチップ間I／O部を経由して前記半導体チップへ転送することを特徴とする積層メモリチップ。

[請求項11] 請求項1記載の積層メモリチップにおいて、

前記メモリエレメントを物理的に切り離すことが可能なスクライブ領域が、前記メモリエレメント間に設けられることを特徴とする積層メモリチップ。

[請求項12] 請求項1記載の積層メモリチップにおいて、

2次元アレイ状に配置された前記メモリエレメントを多段に積層することを特徴とする積層メモリチップ。

[請求項13] 積層メモリチップと、前記積層メモリチップに積層された半導体チップとを備え、前記半導体チップは複数の論理マクロを有し、前記積層メモリチップは請求項1に記載の積層メモリチップであることを特徴とする半導体集積回路装置。

[請求項14] 請求項13記載の半導体集積回路装置において、

さらに、前記半導体チップは、前記論理マクロの構成に応じた所望のメモリ構成に対応する制御信号を前記積層メモリチップに出力する制御信号出力手段を備えることを特徴とする半導体集積回路装置。

[請求項15] 請求項14記載の半導体集積回路装置において、

前記制御信号出力手段は、前記論理マクロの動作状況に応じて前記制御信号を出力することを特徴とする半導体集積回路装置。

[請求項16] 請求項14記載の半導体集積回路装置において、

前記制御信号出力手段は、前記メモリエレメントの組み合わせによりメモリ領域が構成され、このメモリ領域を構成するメモリエレメントの2つのチップ間I／O部が使用可能となるように前記制御信号を出力し、

前記論理マクロは、書き込みデータを、使用可能な前記2つのチップ間I／O部のうち一方のチップ間I／O部を経由して前記メモリ領域を構成する各メモリエレメントのメモリマクロへ転送して書き込み動作を行い、前記メモリ領域を構成する一部のメモリエレメントのメモリマクロから読み出された読み出しデータを、使用可能な前記2つのチッ

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プ間I／O部のうち一方のチップ間I／O部を経由して受け取ると共に、前記メモリ領域を構成する残りのメモリエレメントのメモリマクロから読み出された読み出しデータを、使用可能な前記2つのチップ間I／O部のうち他方のチップ間I／O部を経由して受け取ることを特徴とする半導体集積回路装置。

[請求項17] 請求項2記載の積層メモリチップにおいて、

前記第1の配線は前記スイッチファブリックを相互に接続する接続網を構成していることを特徴とする積層メモリチップ。

[請求項18] 請求項17記載の積層メモリチップにおいて、

前記接続網は、2次元メッシュ構造、2次元トーラス構造、またはツリー構造のいずれかの構造、または、前記構造の組み合わせからなる構造を有することを特徴とする積層メモリチップ。

[請求項19] 請求項1記載の積層メモリチップにおいて、

クロスバースイッチをさらに備え、前記各メモリエレメントは、前記クロスバースイッチと前記第1の配線により相互に接続されることを特徴とする積層メモリチップ。

[請求項20] 請求項2記載の積層メモリチップにおいて、

前記メモリエレメントの少なくとも一つは、制御信号入力部を有し、

前記制御信号入力部は、前記半導体チップまたは前記半導体チップとは異なる半導体装置から前記制御信号を受信し、前記制御信号を前記レジスタに出力することを特徴とする積層メモリチップ。

[請求項21] 請求項13記載の半導体集積回路装置において、

前記半導体チップは、前記論理マクロの構成に応じた所望のメモリ構成に対応する制御信号を生成する制御信号生成部を有し、

前記制御信号生成部は、前記論理マクロが必要とするメモリ領域の大きさの情報からなる構成リクエスト信号を前記各論理マクロから受け取り、前記構成リクエスト信号に基づいて前記各論理マクロに割り当てるメモリ領域の大きさを決定する構成リクエスト調停部と、前記決定に基づいて制御信号を生成する制御信号処理部と、前記制御信号を前記積層メモリチップに送出する制御信号出力部を備えることを特徴とする半導体集積回路装置。

[請求項22] 請求項13記載の半導体集積回路装置において、

前記半導体チップと前記積層メモリチップとの間に配線部材を有することを特徴と

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する半導体集積回路装置。

[請求項23] 請求項22記載の半導体集積回路装置において、

前記半導体チップは、クロック供給源を有し、

前記積層メモリチップは、クロック入力部を有し、

前記配線部材は、前記クロック供給源から前記クロック入力部までが等遅延配線となるように形成された配線層を備えている

ことを特徴とする半導体集積回路装置。

[請求項24] 複数の論理マクロを有する半導体チップと、

前記半導体チップ上に積層される、請求項1に記載の積層メモリチップとを有し、

前記半導体チップおよび前記積層メモリチップは多層配線構造を備え、

前記半導体チップに含まれる多層配線構造を構成する電極層の一部からなる第1の接合用電極層と、前記積層メモリチップに含まれる多層配線構造を構成する電極層の一部からなる第2の接合用電極層を有し、前記第1の接合用電極層と第2の接合用電極層とが接合していることを特徴とする半導体集積回路装置。

[請求項25] 請求項24記載の半導体集積回路装置において、

少なくとも前記第1の接合用電極層と前記第2の接合用電極層の周辺領域に封止材料を有することを特徴とする半導体集積回路装置。

[請求項26] 多層配線構造を有する半導体チップに、前記半導体チップに含まれる前記多層配線構造を構成する電極層の一部からなる第1の接合用電極層を形成し、

前記半導体チップ上に積層され多層配線構造を備えた、請求項1に記載の積層メモリチップに、前記積層メモリチップに含まれる前記多層配線構造を構成する電極層の一部からなる第2の接合用電極層を形成し、

前記第1の接合用電極層と前記第2の接合用電極層とを接合する

ことを特徴とする半導体集積回路装置の製造方法。

[請求項27] 請求項26記載の半導体集積回路装置の製造方法において、

少なくとも前記第1の接合用電極層と前記第2の接合用電極層の周辺領域に封止材料を形成することを特徴とする半導体集積回路装置の製造方法。

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図1A

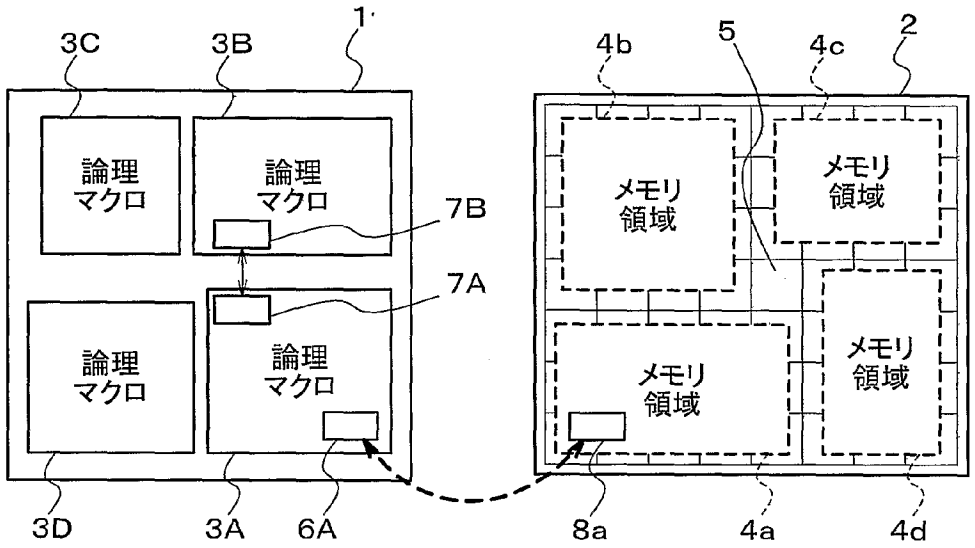

1
3C
3B
4b
5
4c
2
論理
マクロ
論理
マクロ
7B
7A
論理
マクロ
論理
マクロ
メモリ
領域
メモリ
領域
メモリ
領域
メモリ
領域
3D
3A
6A
8a
4a
4d

図1B

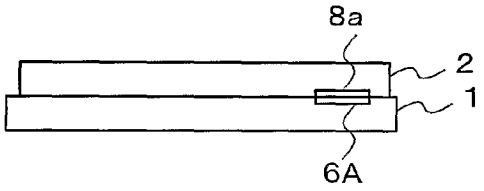
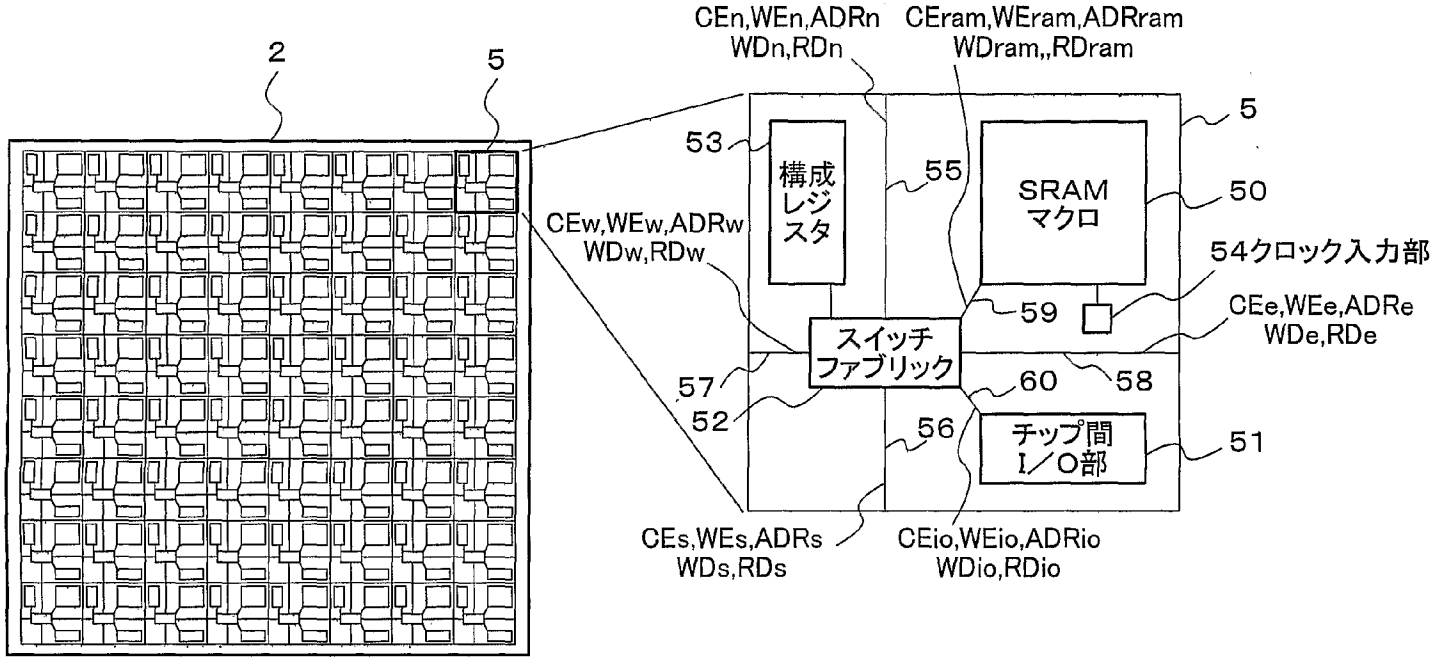

8a
2
1
6A

図2




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図3

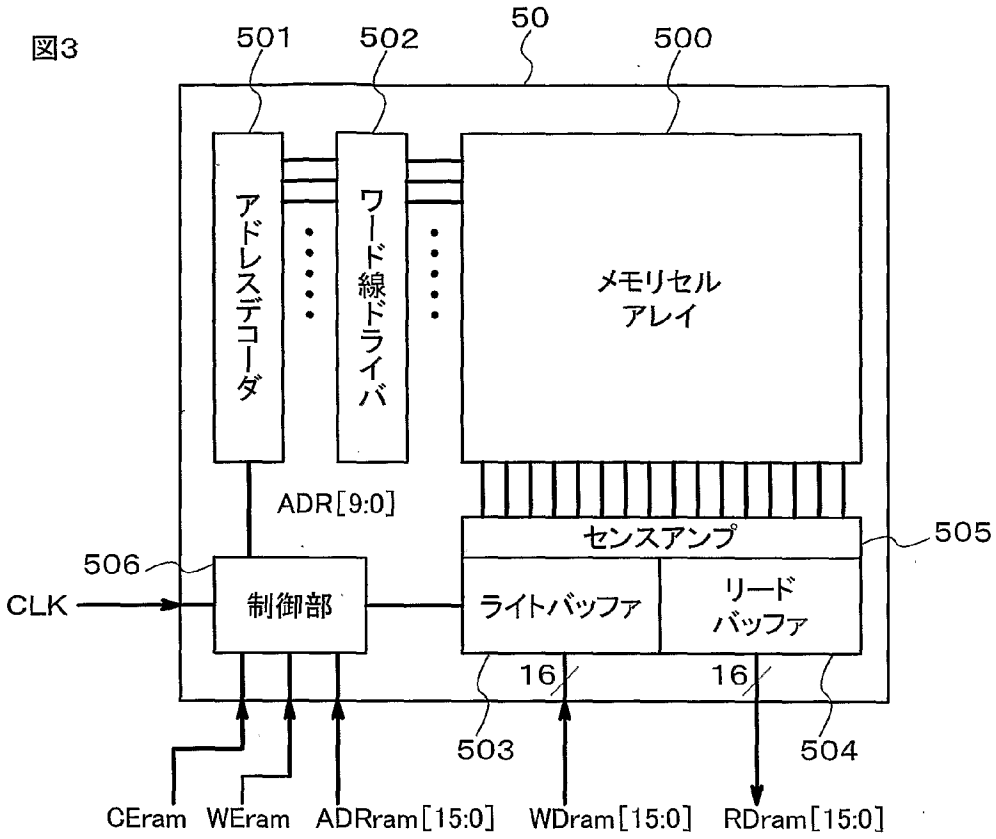

501
502
50
500
アドレスデコーダ
ワード線ドライバ
メモリセル
アレイ
ADR[9:0]
センスアンプ
505
506
CLK
制御部
ライトバッファ
リード
バッファ
16
16
503
504
CEram
WEram
ADRram[15:0]
WDram[15:0]
RDram[15:0]

図4

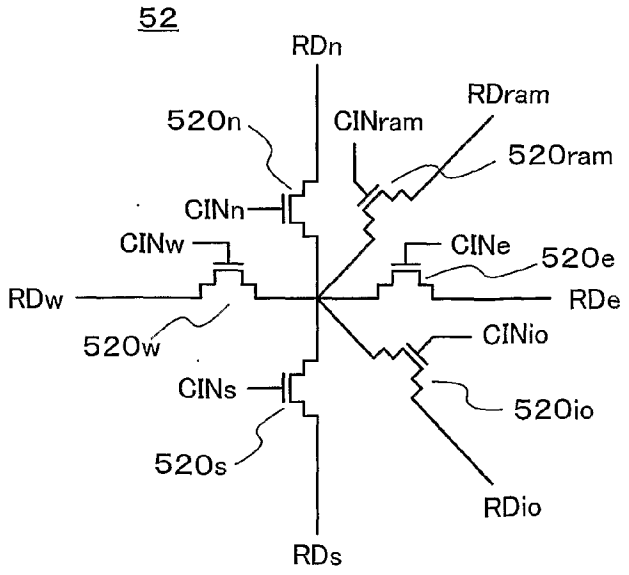

52
RDn
520n
CINram
RDram
520ram
CINn
CINw
CINe
520e
RDw
RDe
520w
CINio
CINs
520io
520s
RDio
RDs

図5

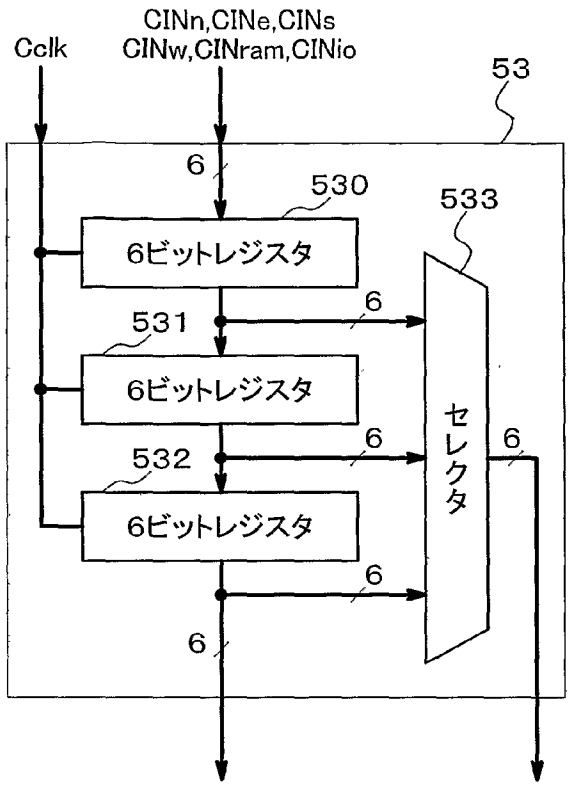
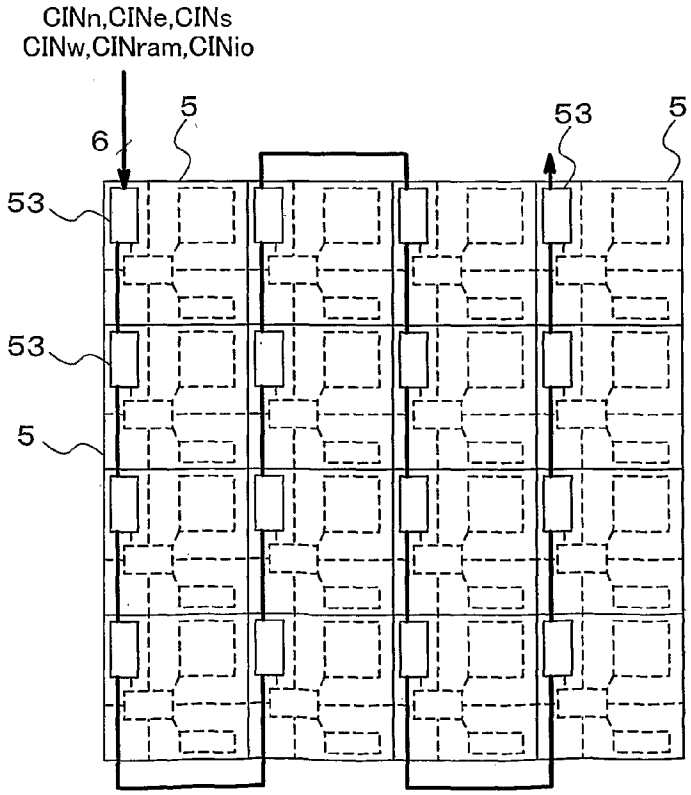



図6




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図7

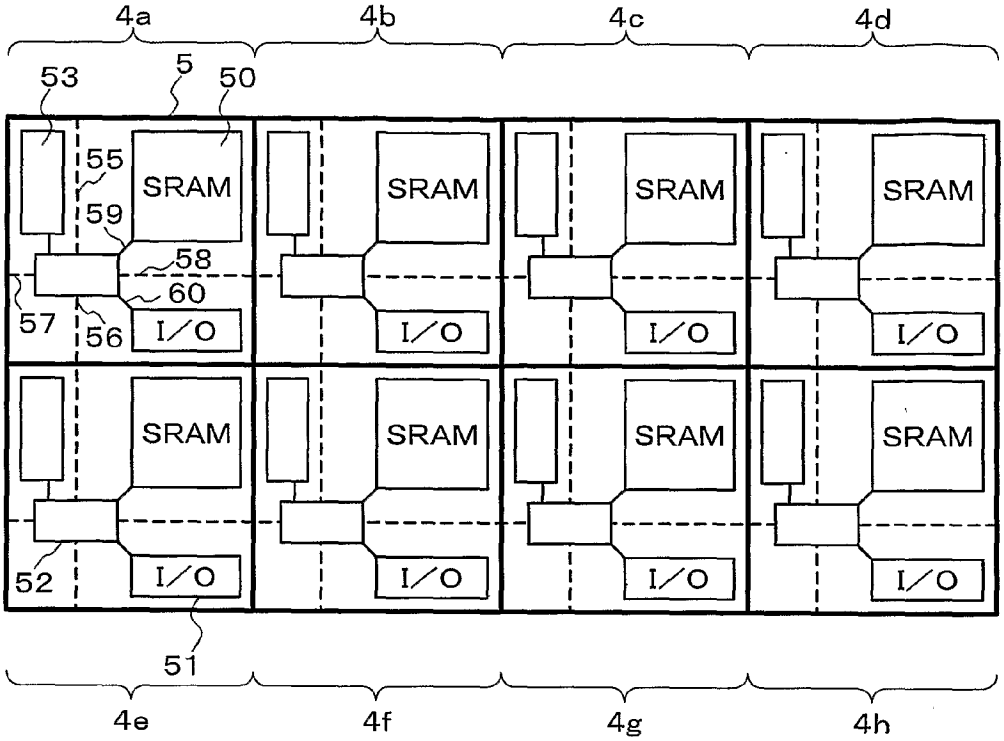
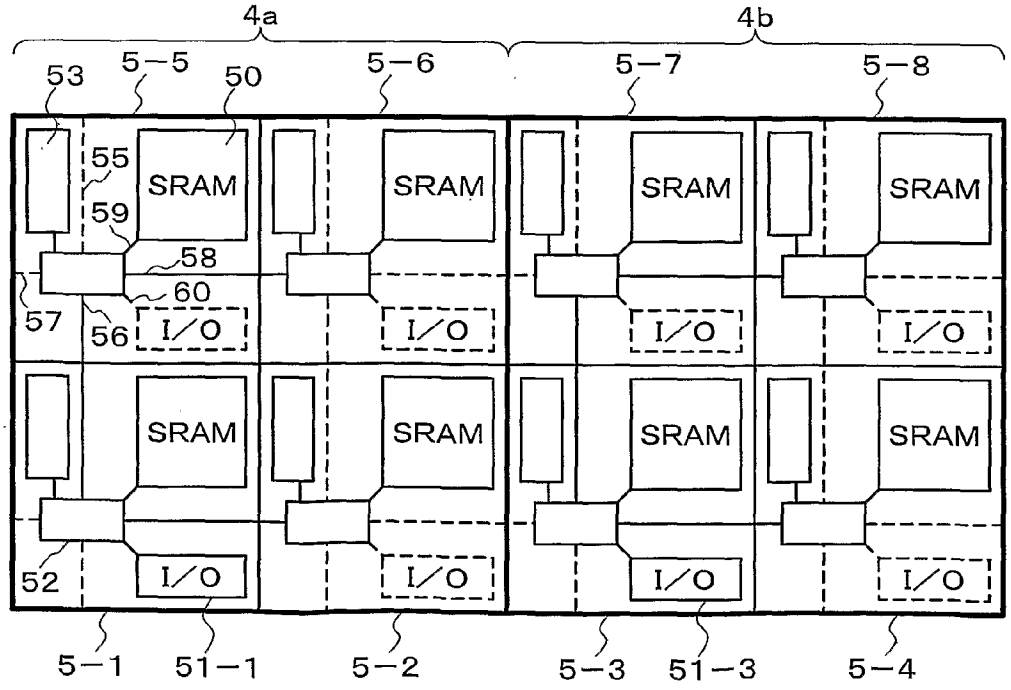



図8




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図9

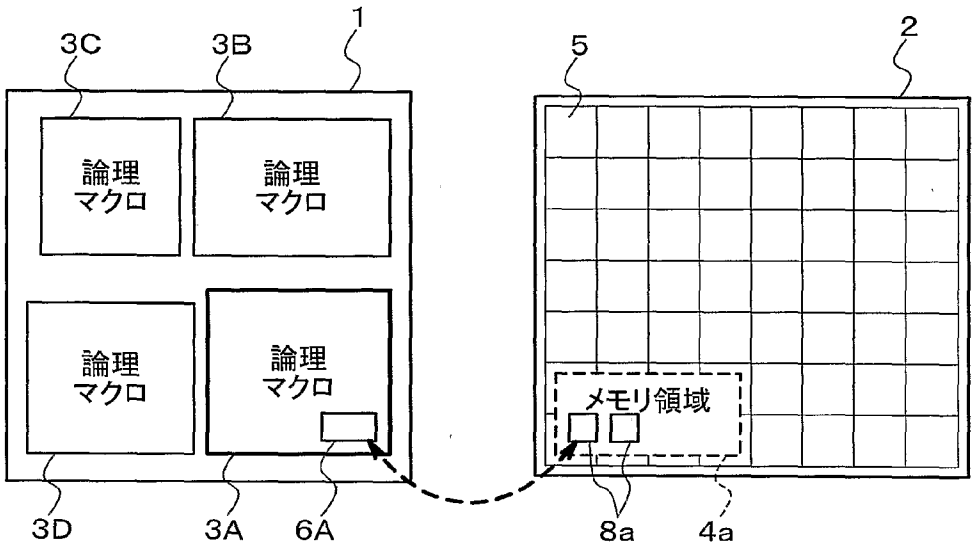
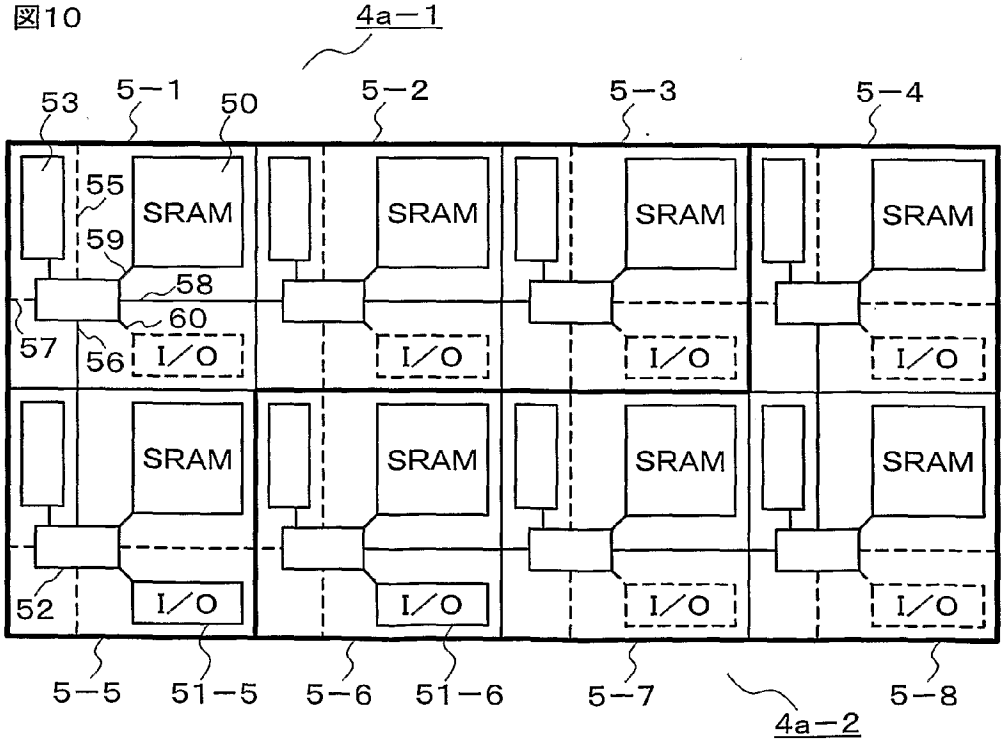



図10




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図11A

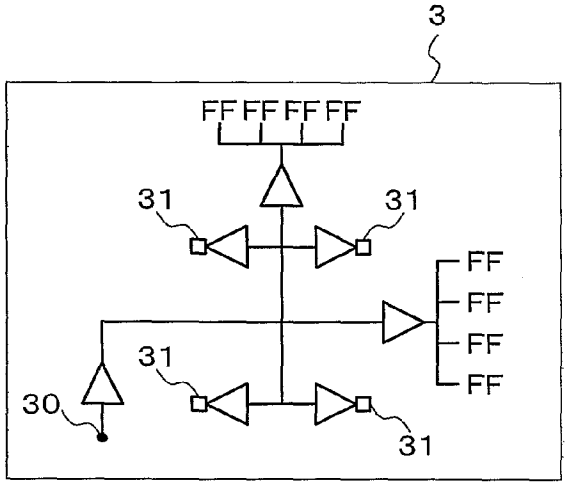



図11B

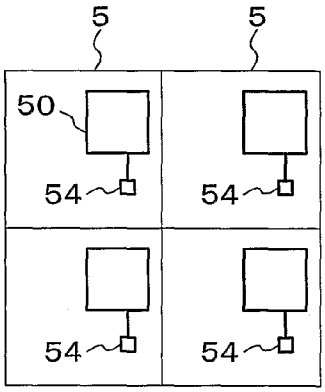


図12

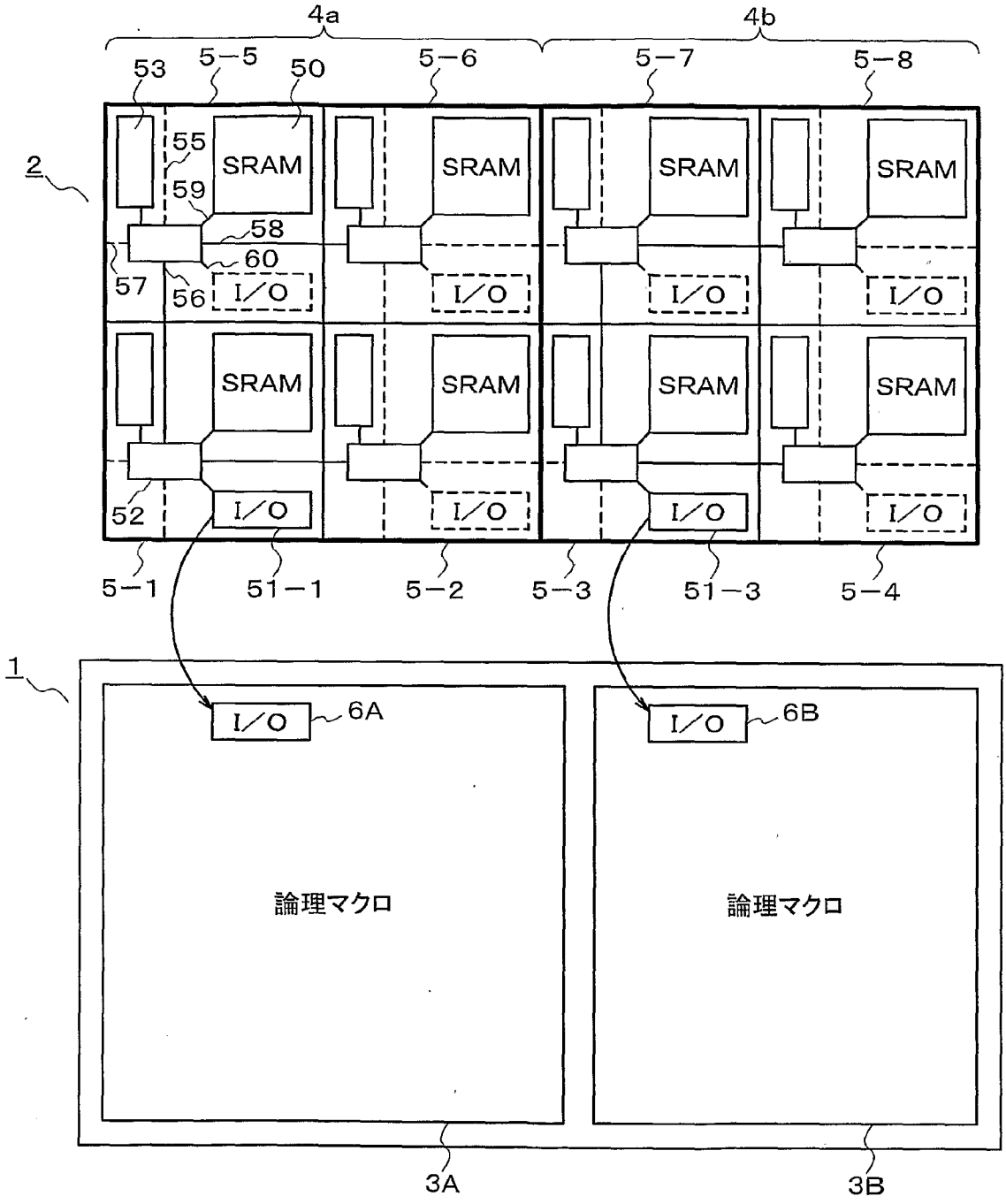

4a
4b
53
5−5
50
5−6
5−7
5−8
2
55
SRAM
59
58
60
57
56
I／O
52
5−1
51−1
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5−3
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1
6A
6B
論理マクロ
3A
3B

図13

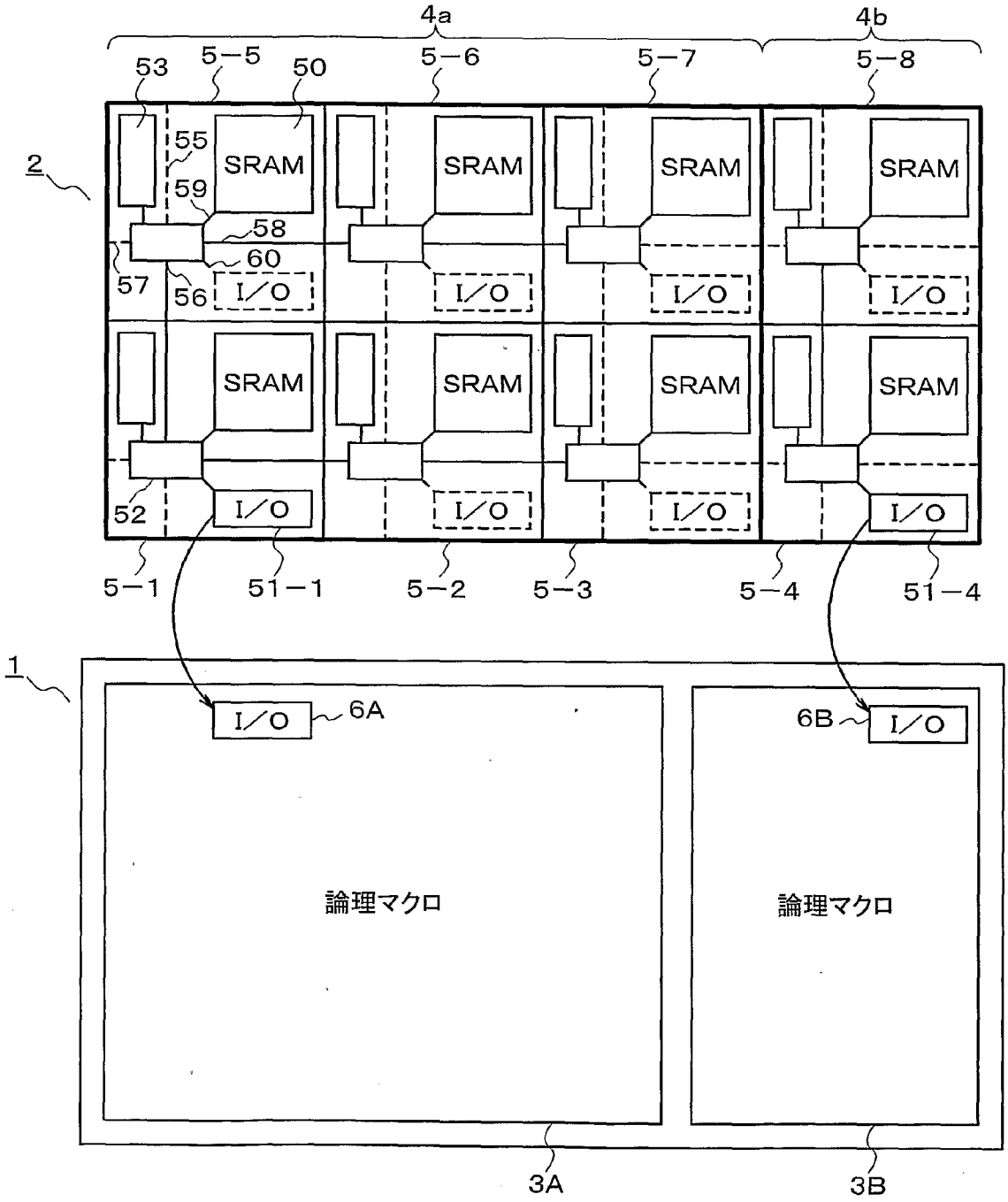

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5−4
51−4
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6A
6B
論理マクロ
3A
3B

図14

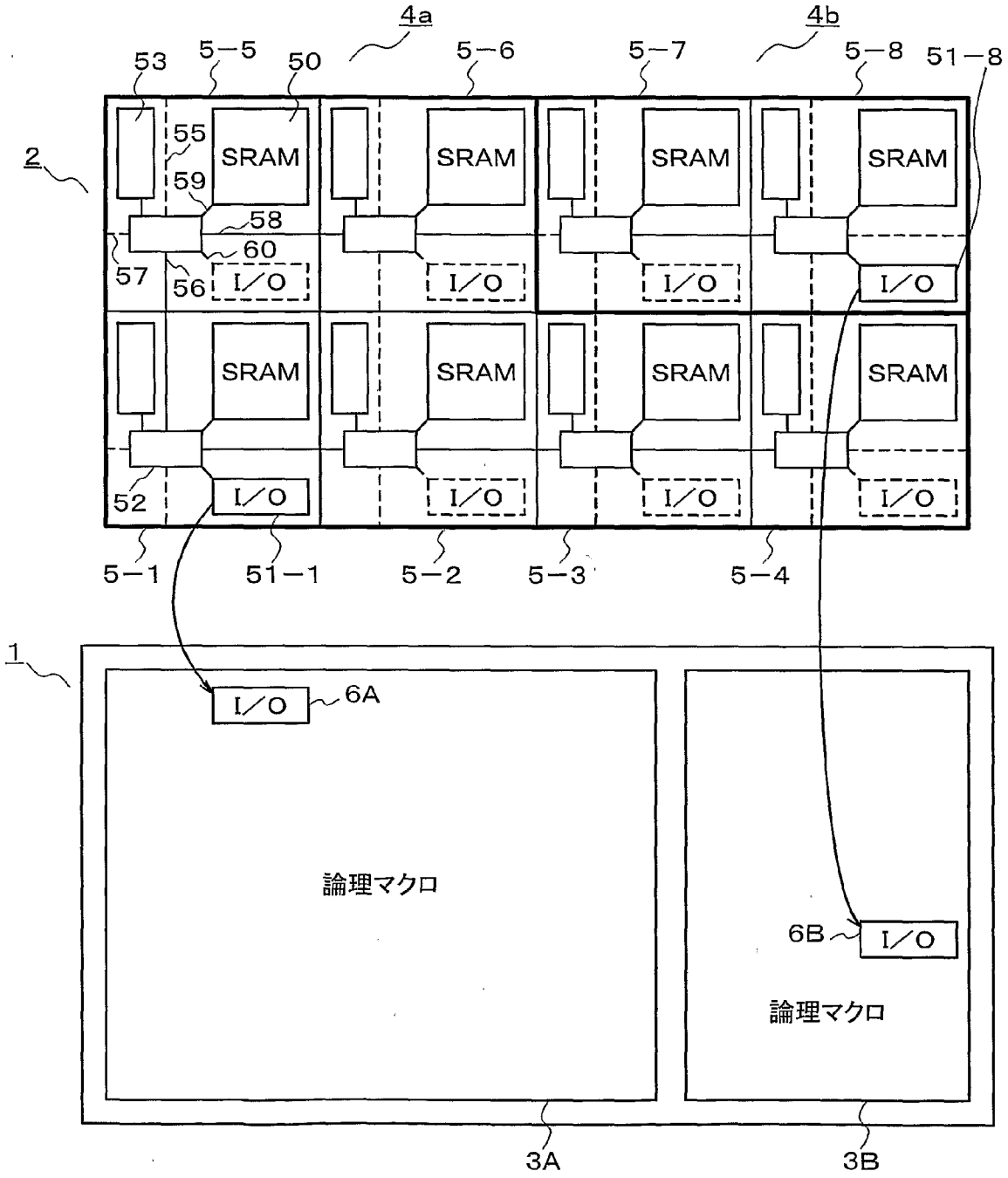

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5−8
51−8
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SRAM
I／O
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51−1
5−2
5−3
5−4
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6A
論理マクロ
6B
3A
3B

図15

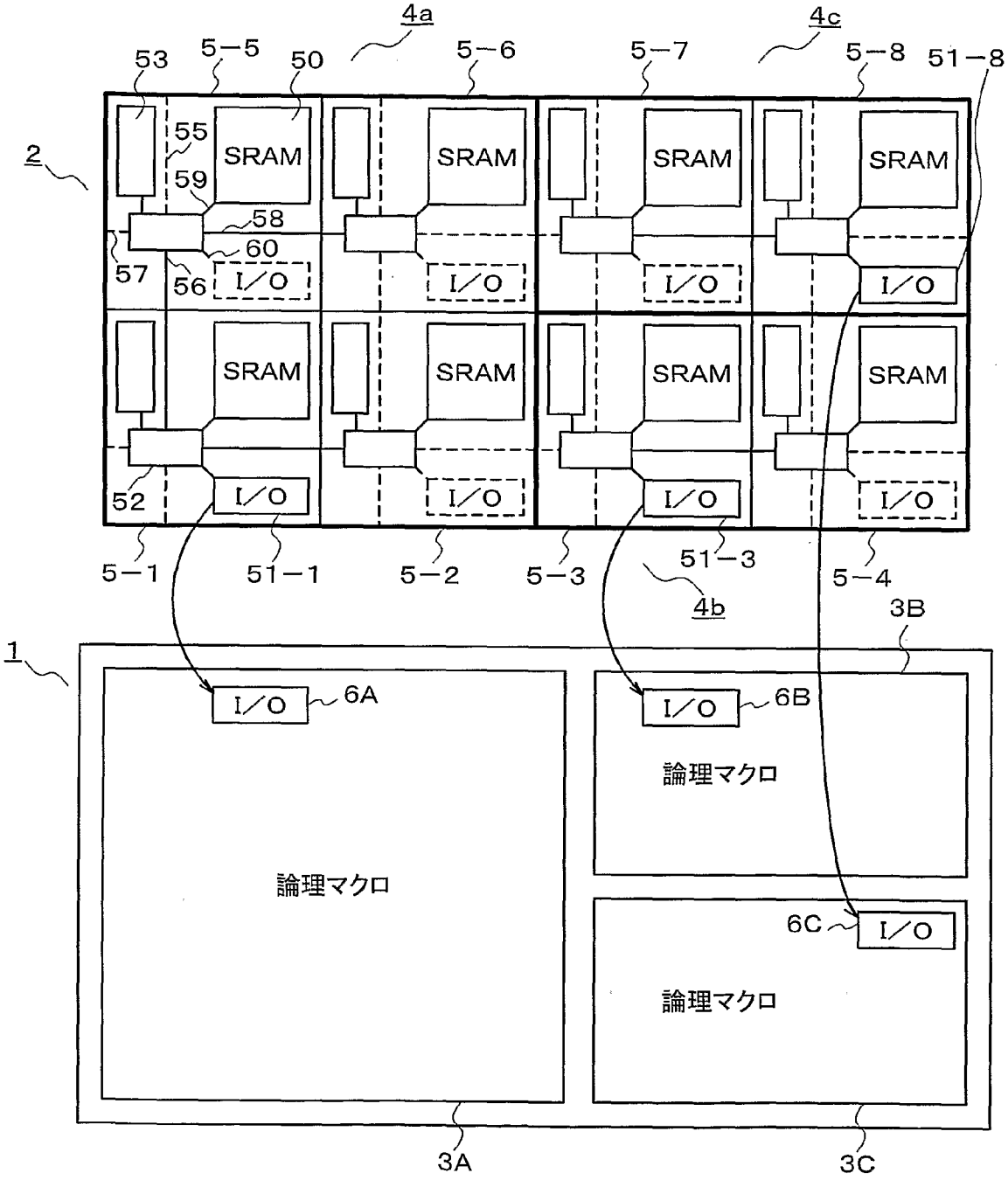

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5−8
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SRAM
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I／O
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5−1
51−1
5−2
5−3
51−3
4b
5−4
3B
1
6A
6B
論理マクロ
6C
3A
3C

図16

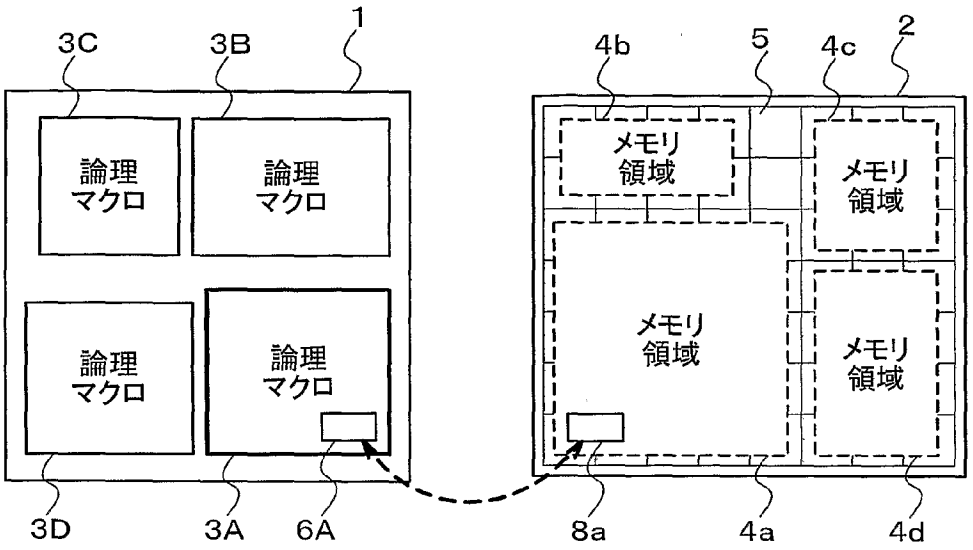
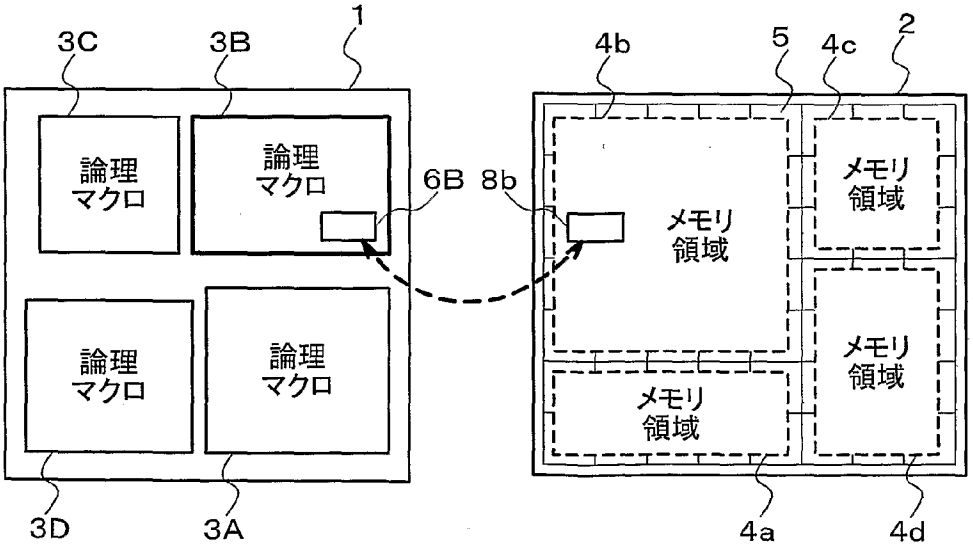



図17




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図18

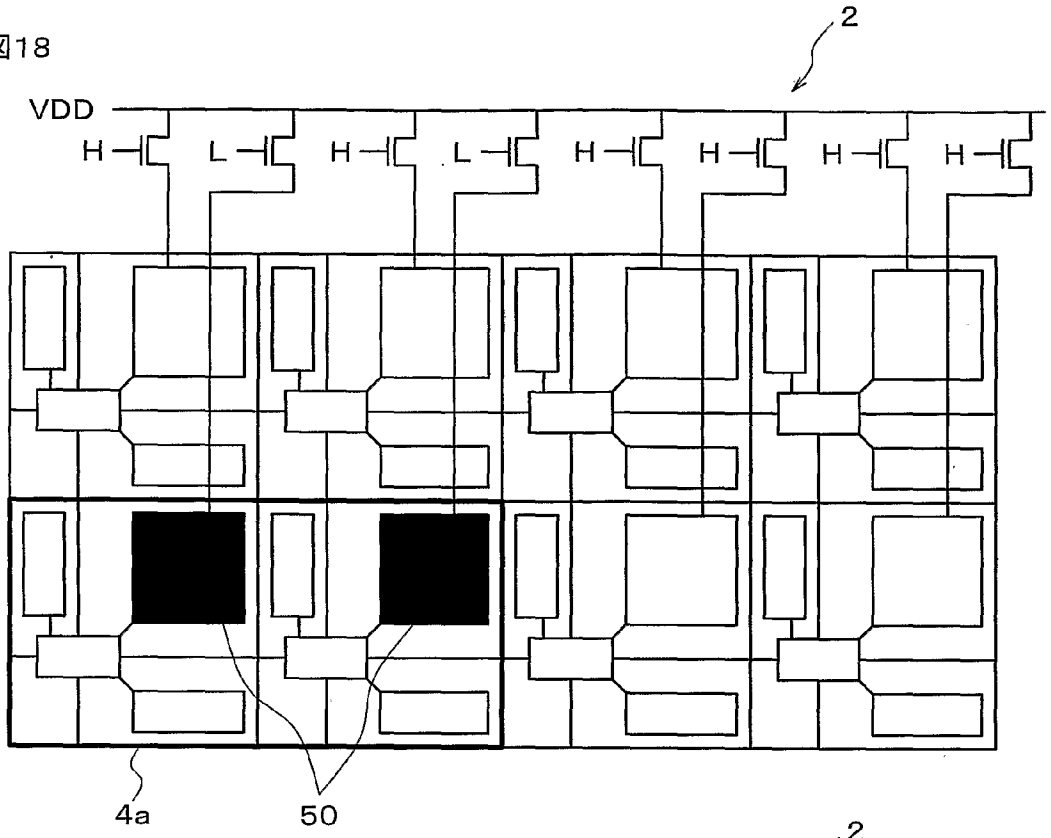



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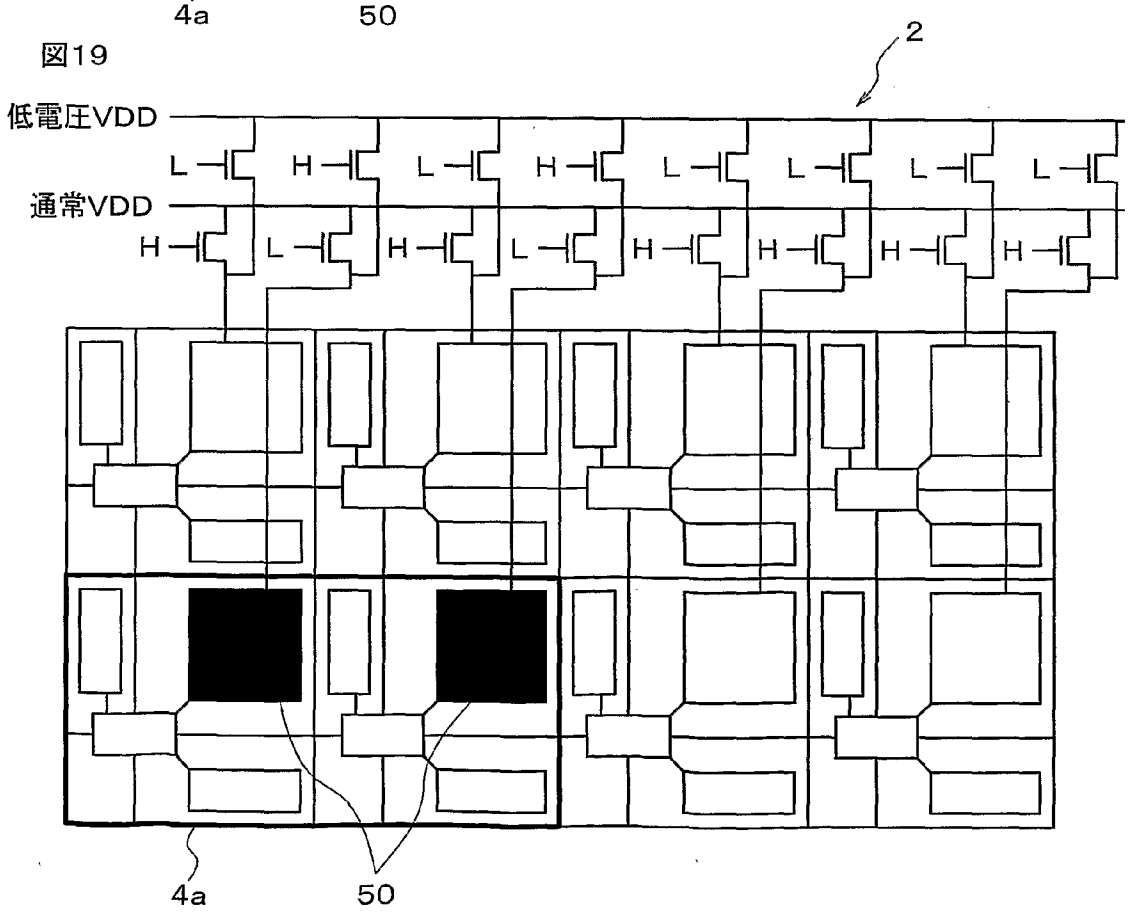


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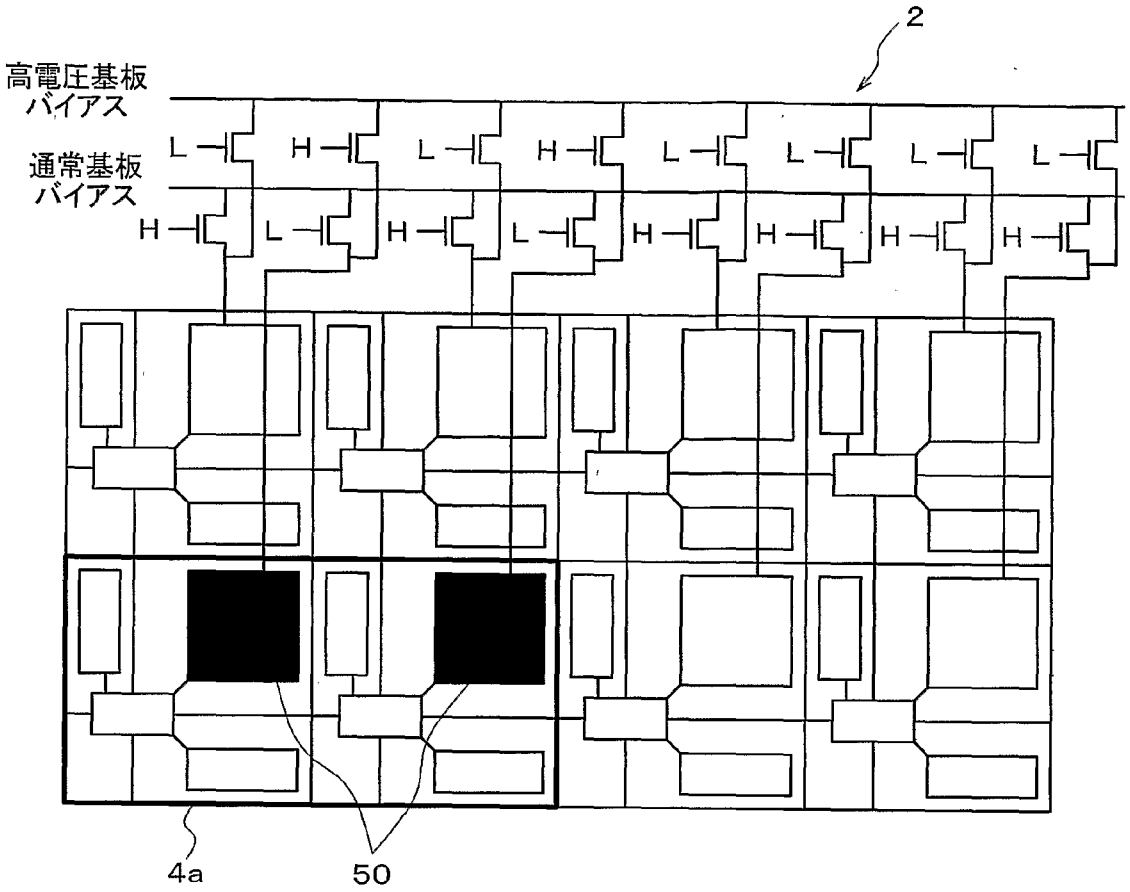


図21

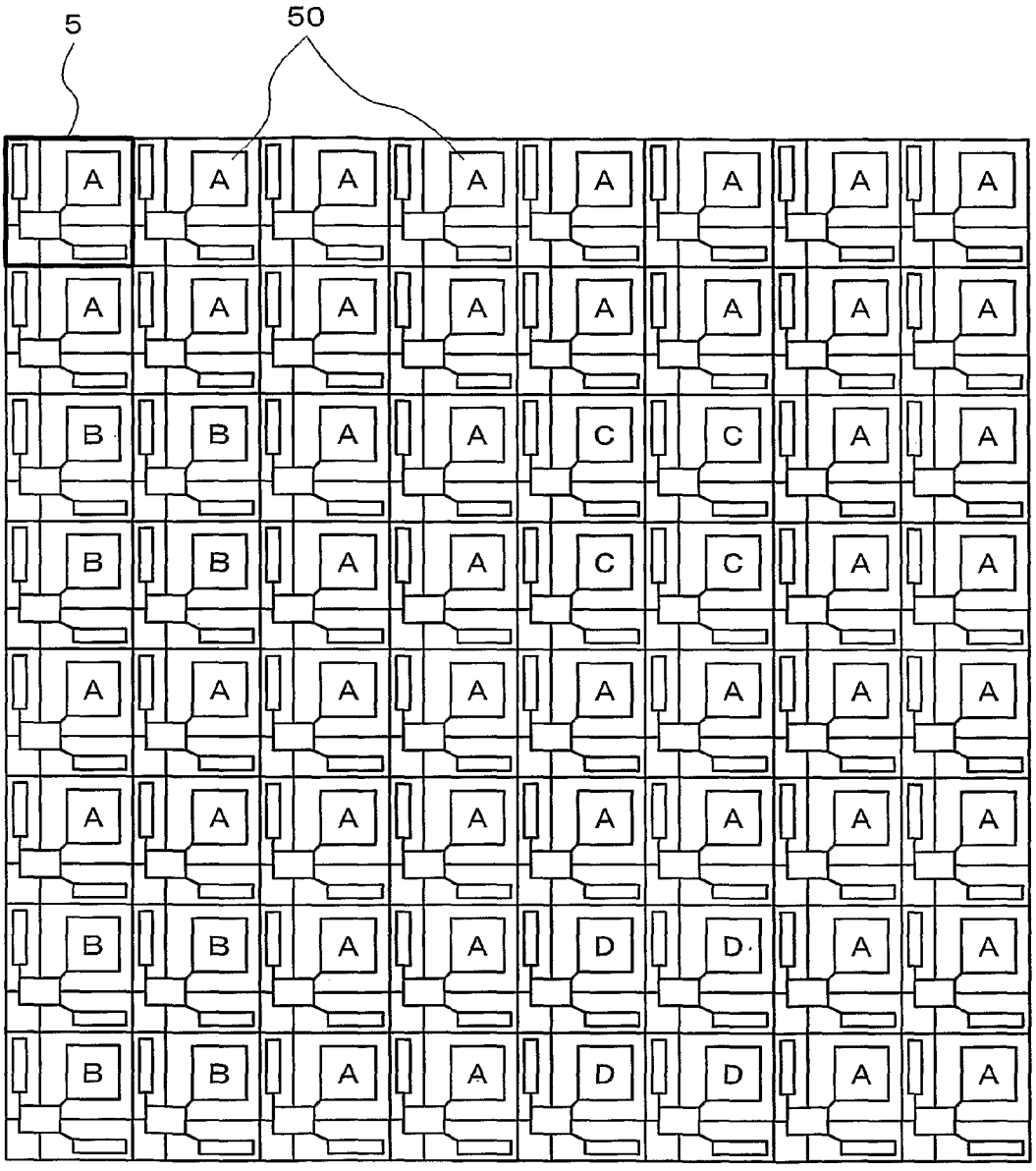
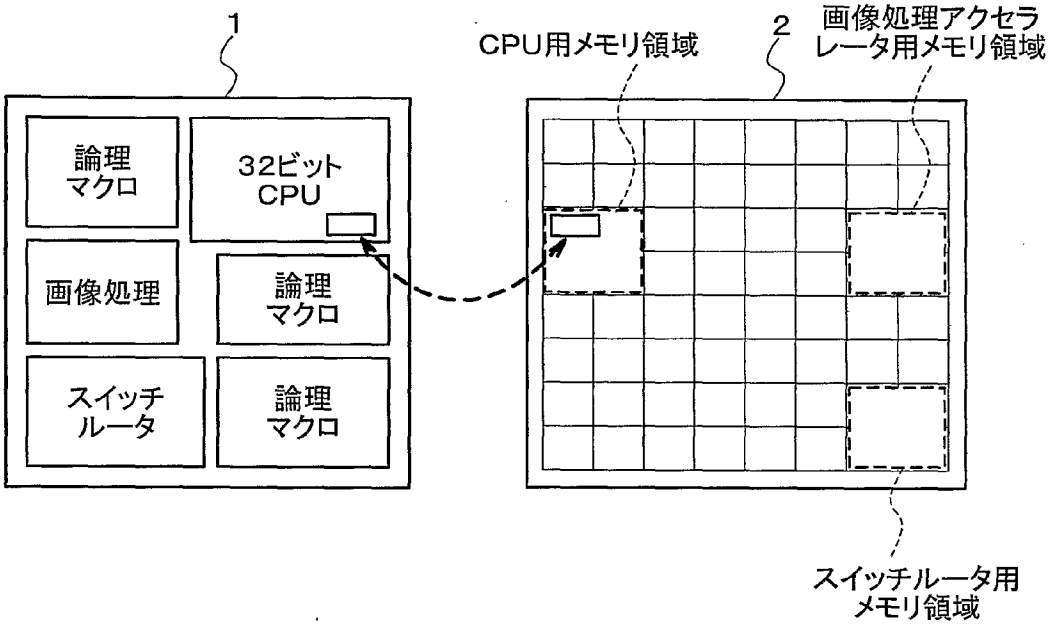

5
50
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図22




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図24

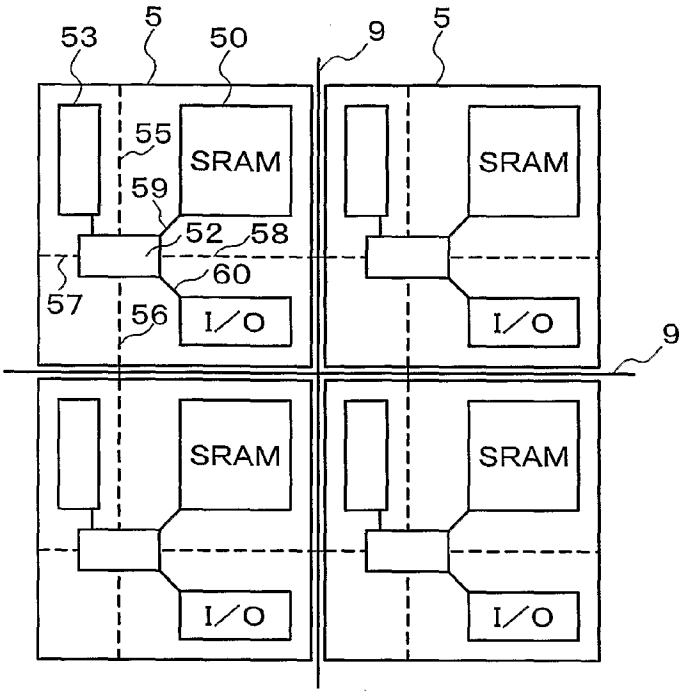
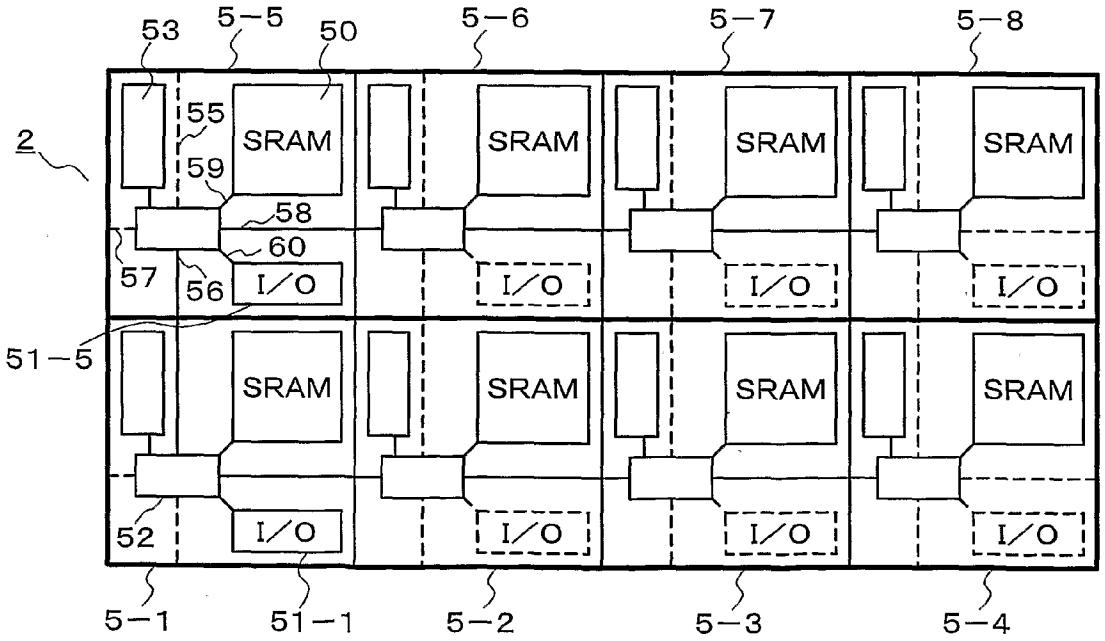
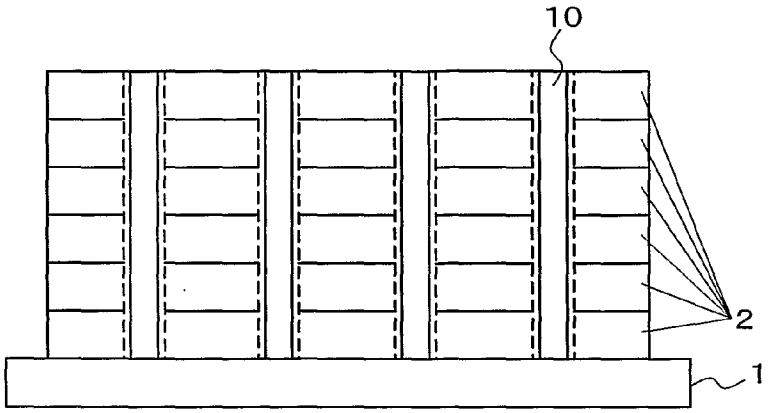



図25




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図26




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図27

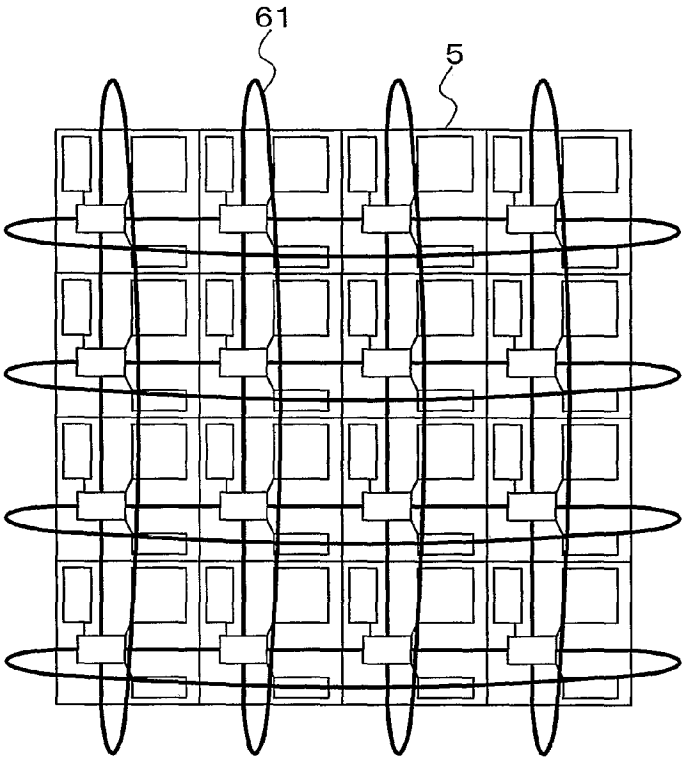
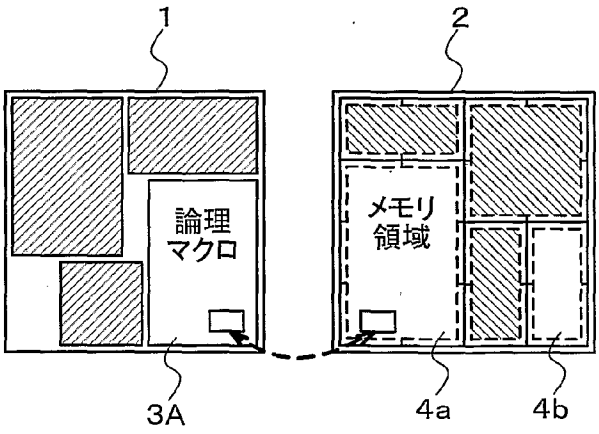



図28




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図29

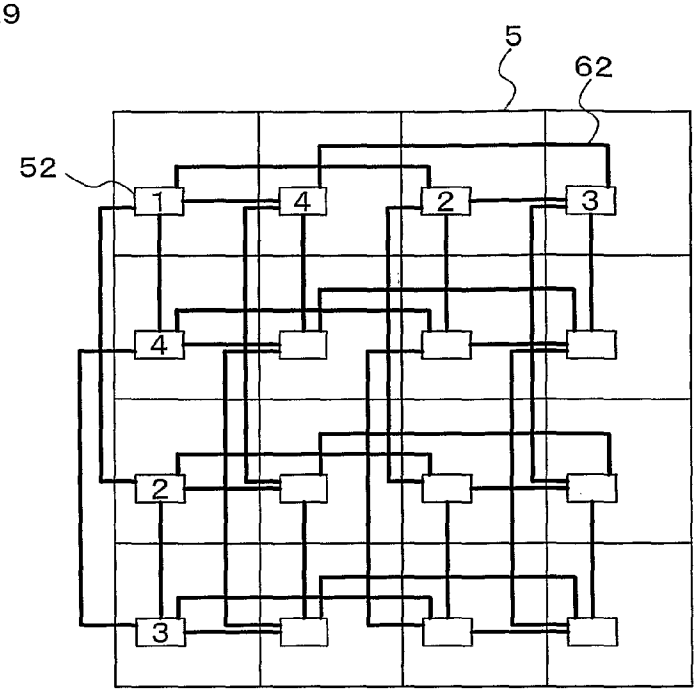



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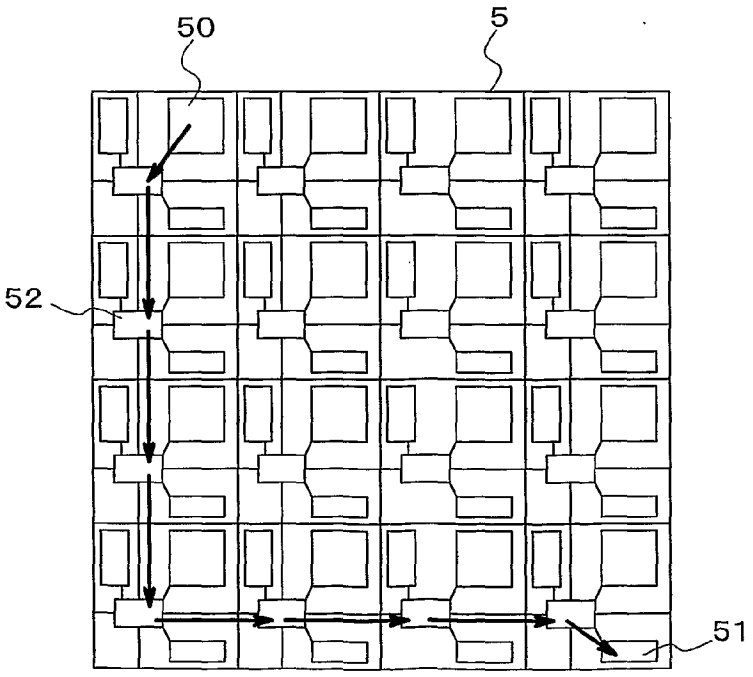


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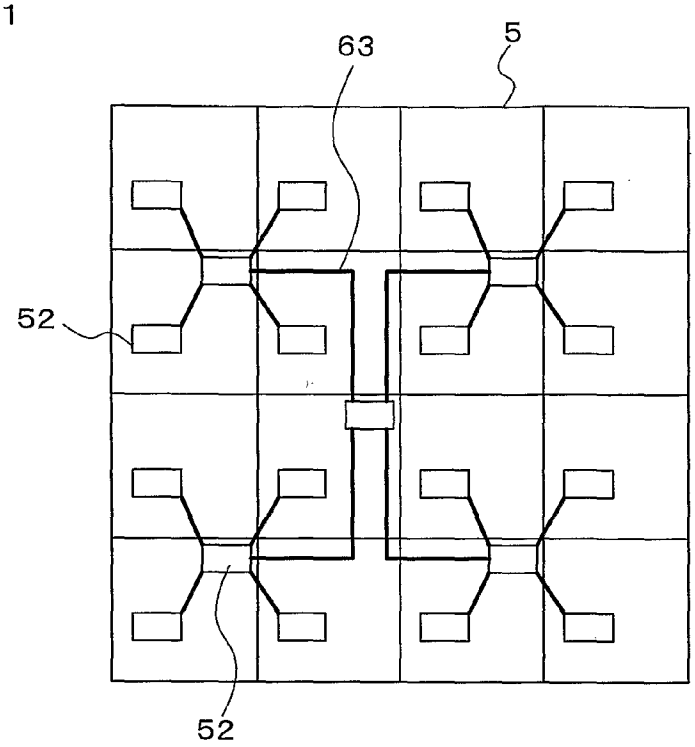



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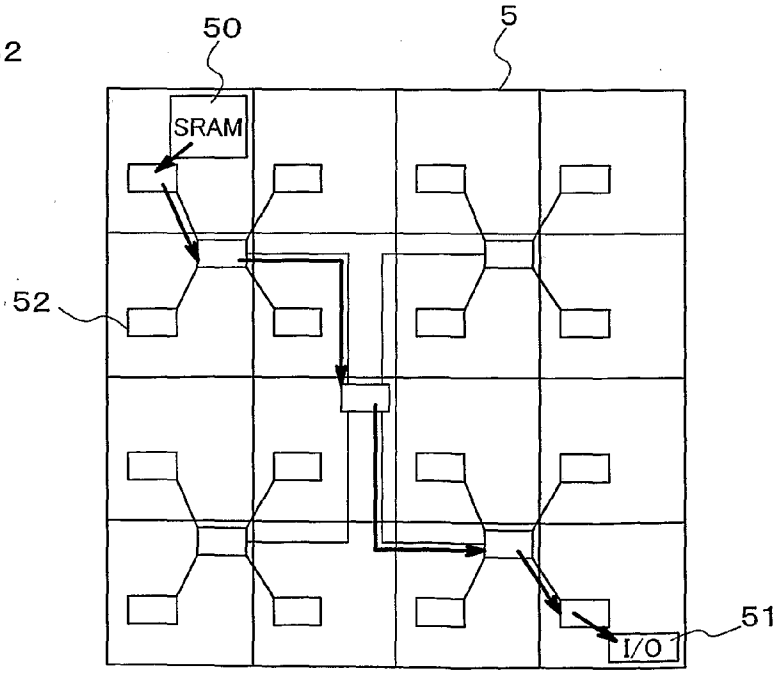


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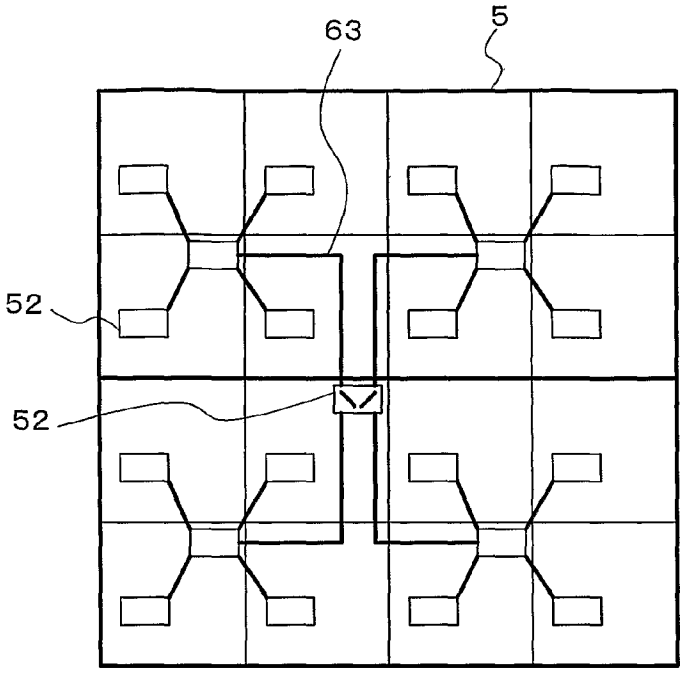



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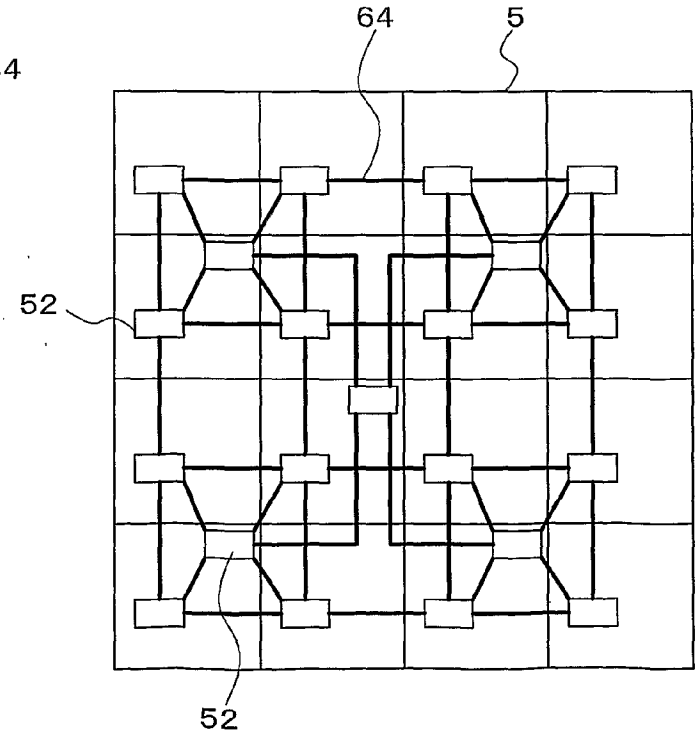


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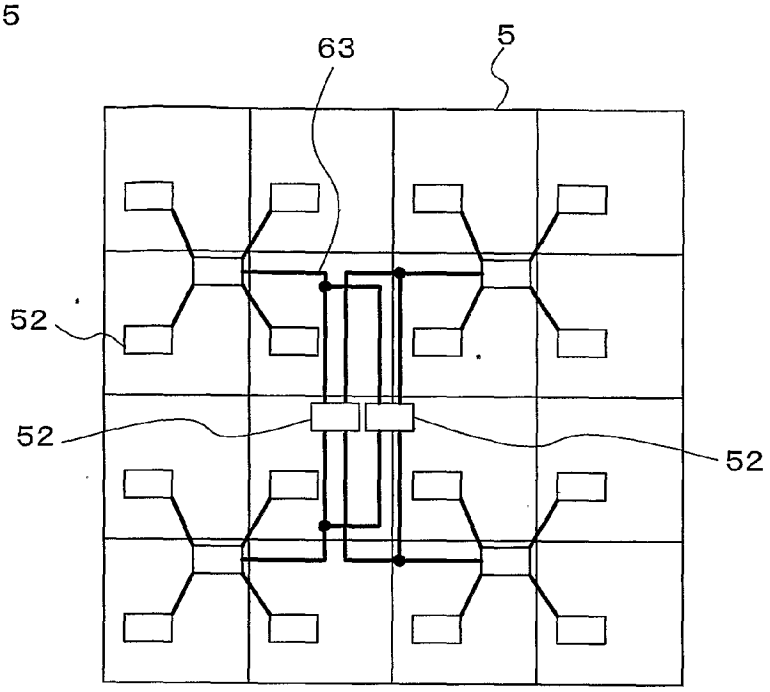



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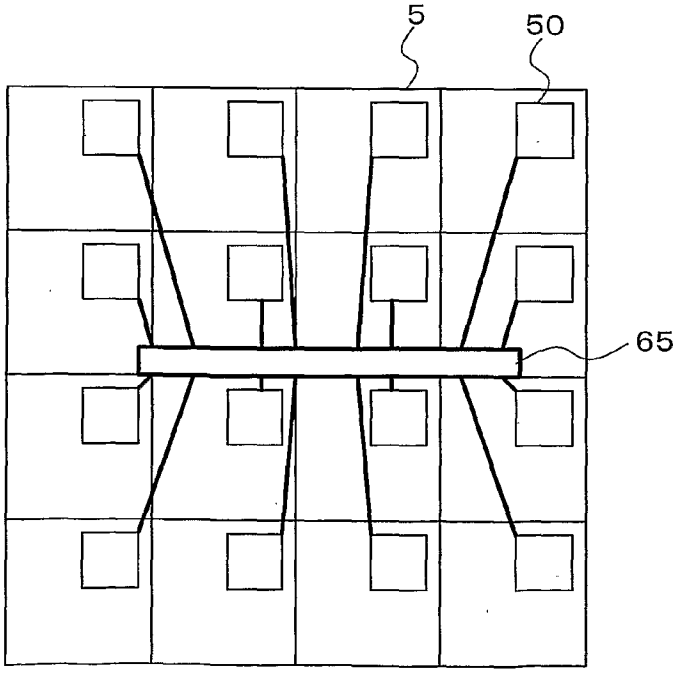


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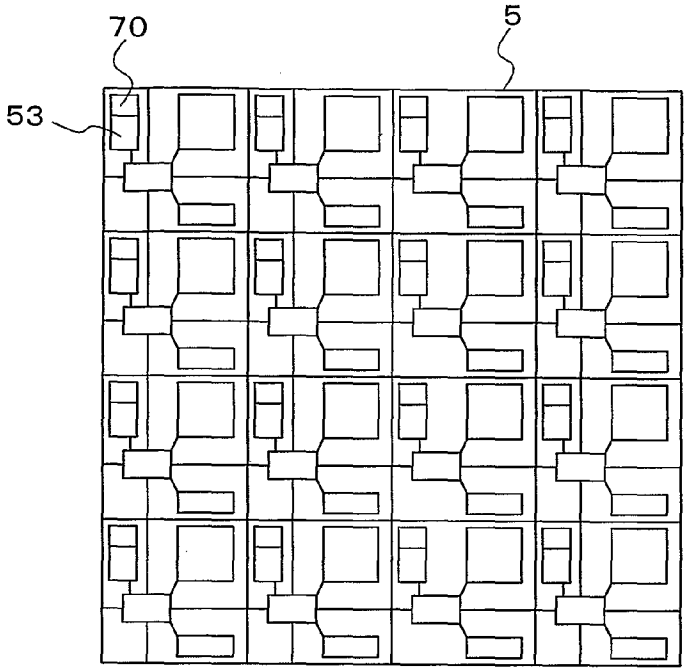
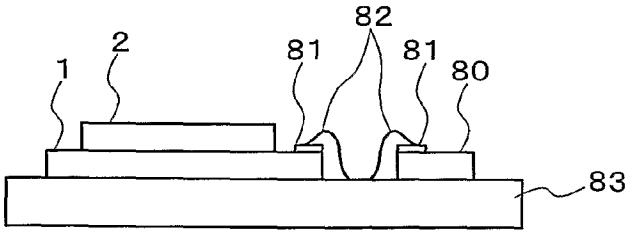



図38




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図39

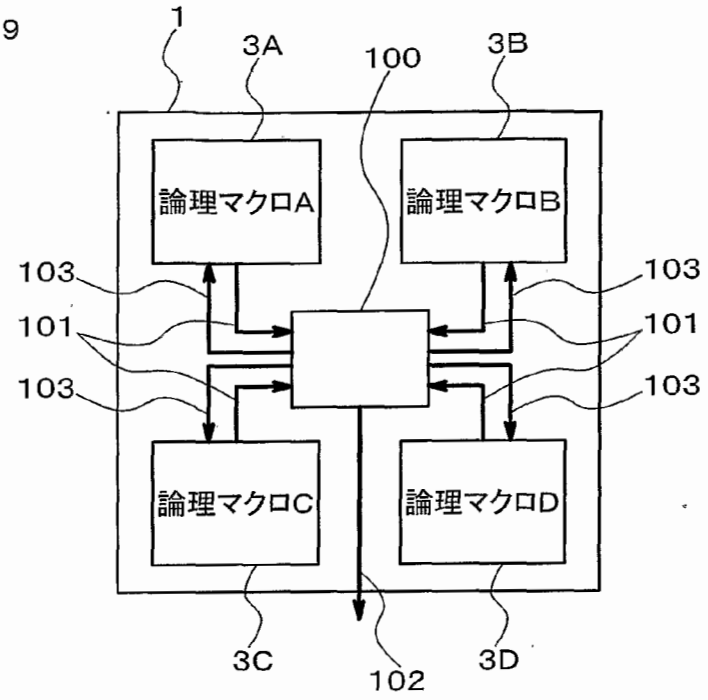
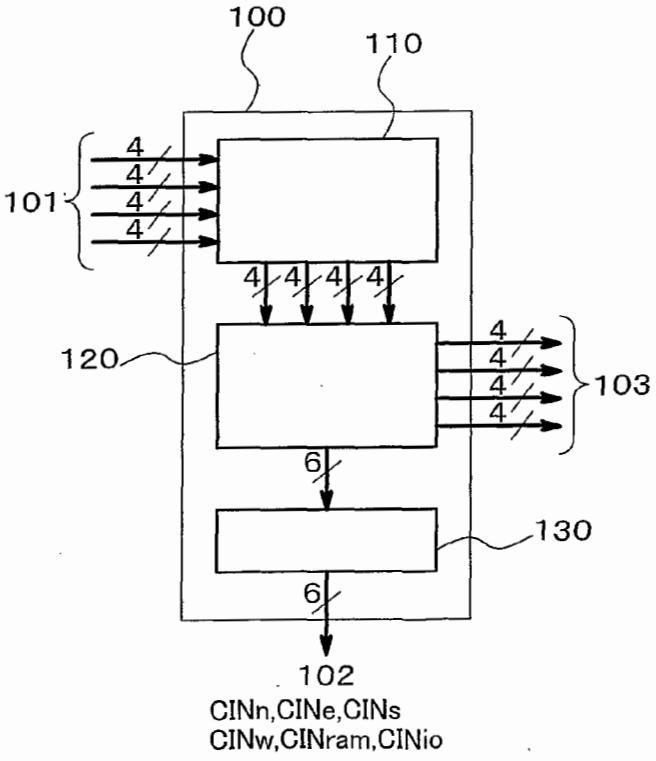



図40




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図41

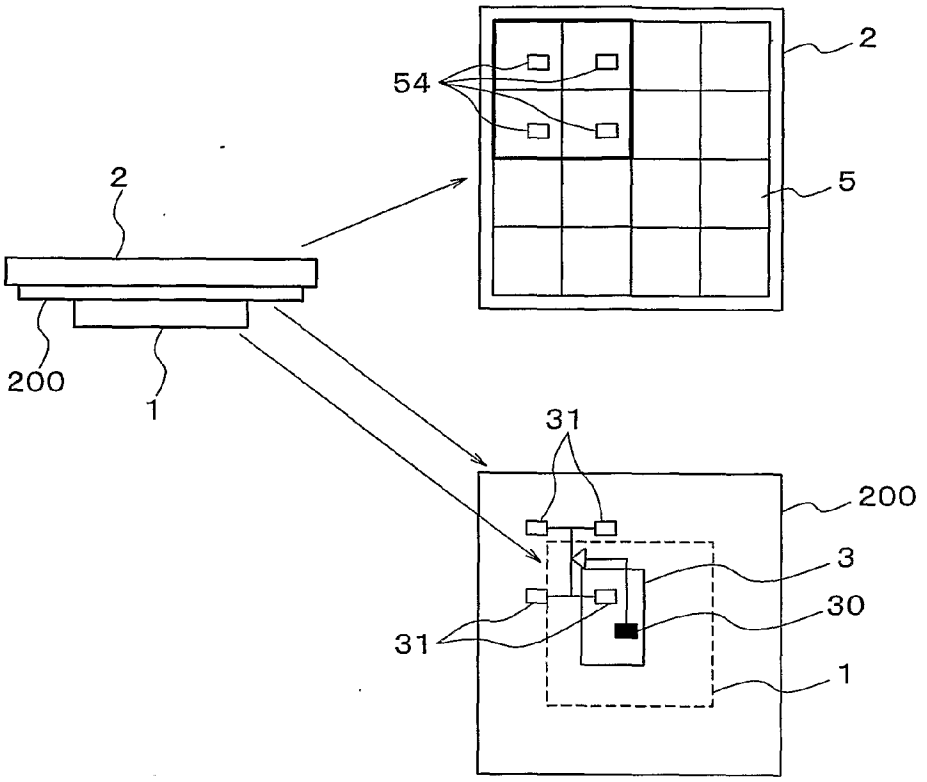



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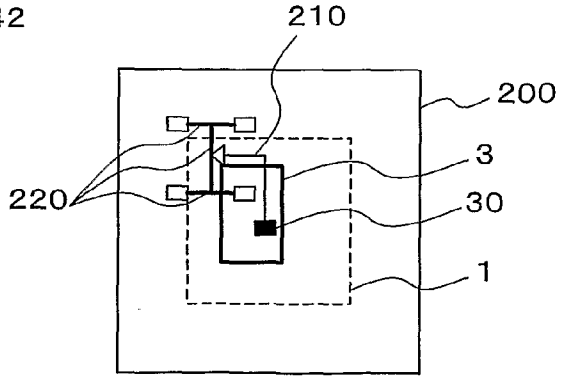
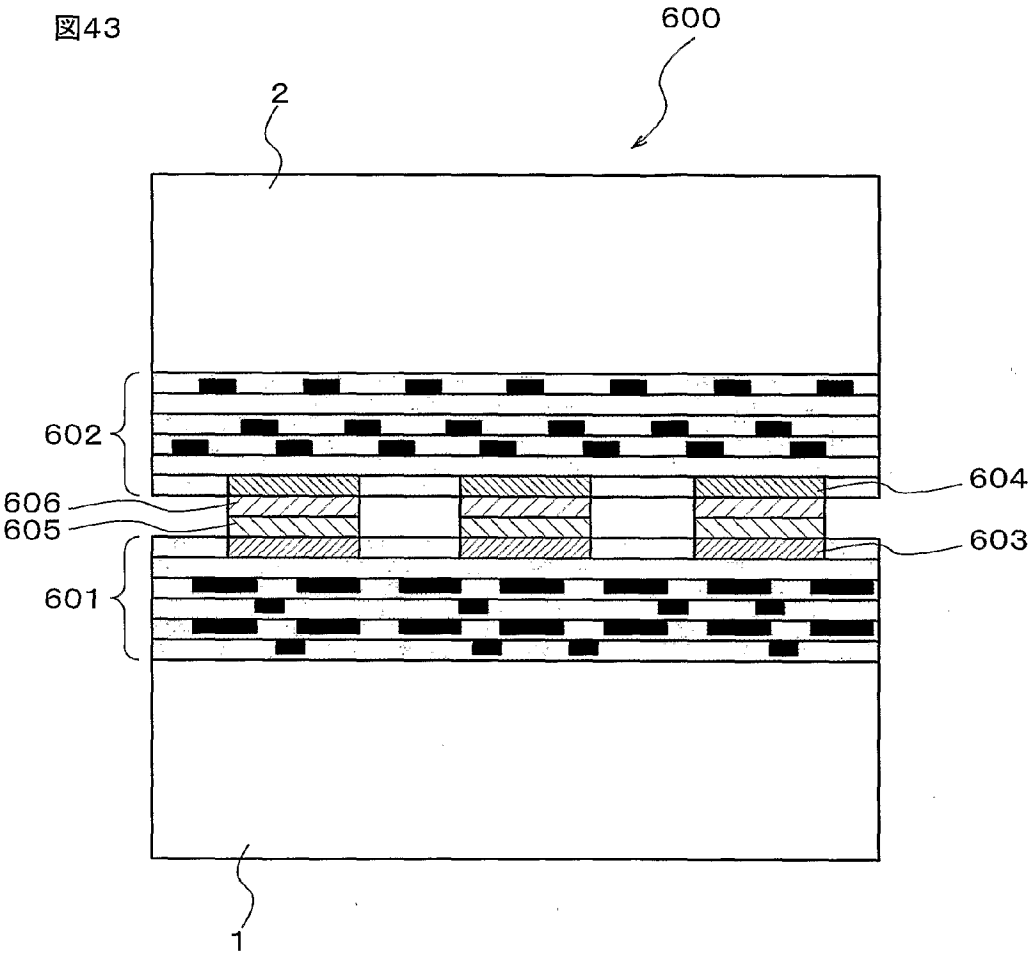


図43




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図44A

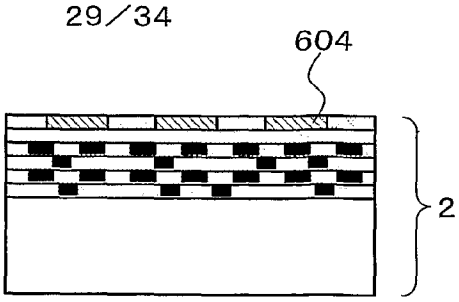



図44B

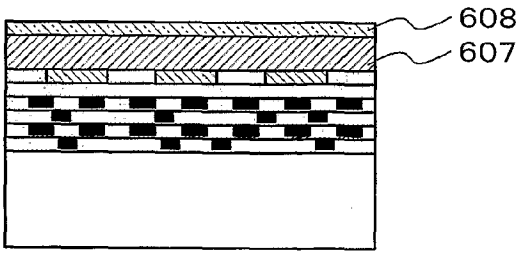



図44C

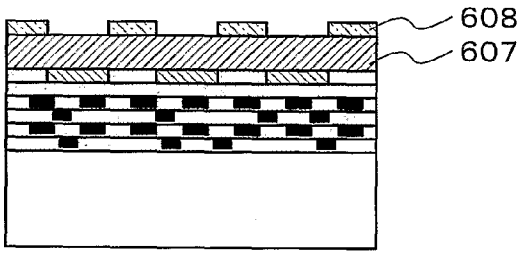



図44D

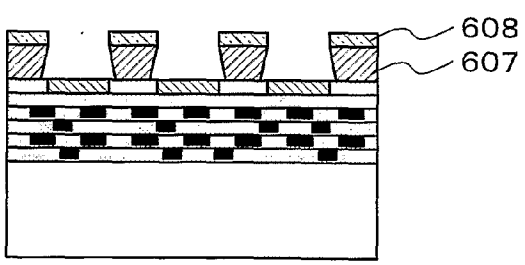



図44E

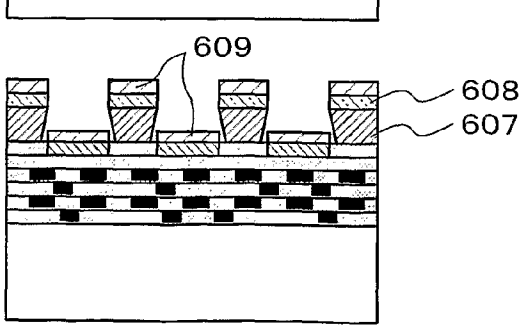



図44F

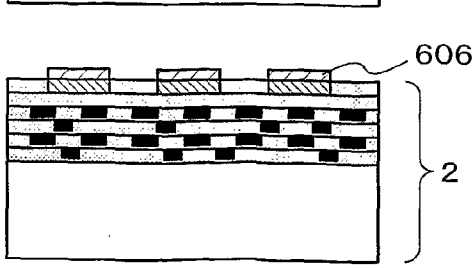


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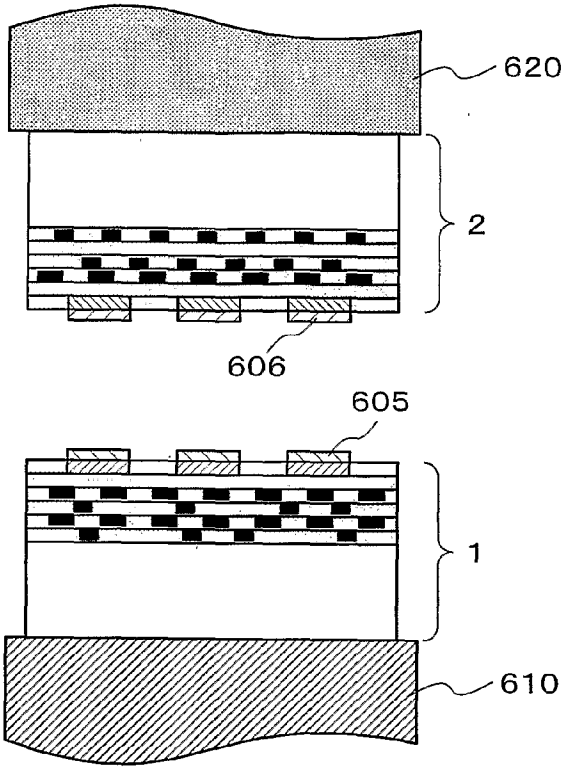



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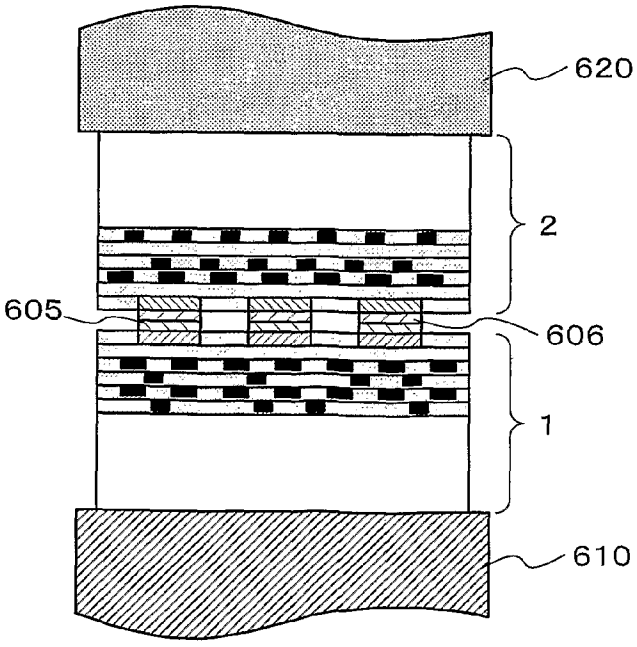


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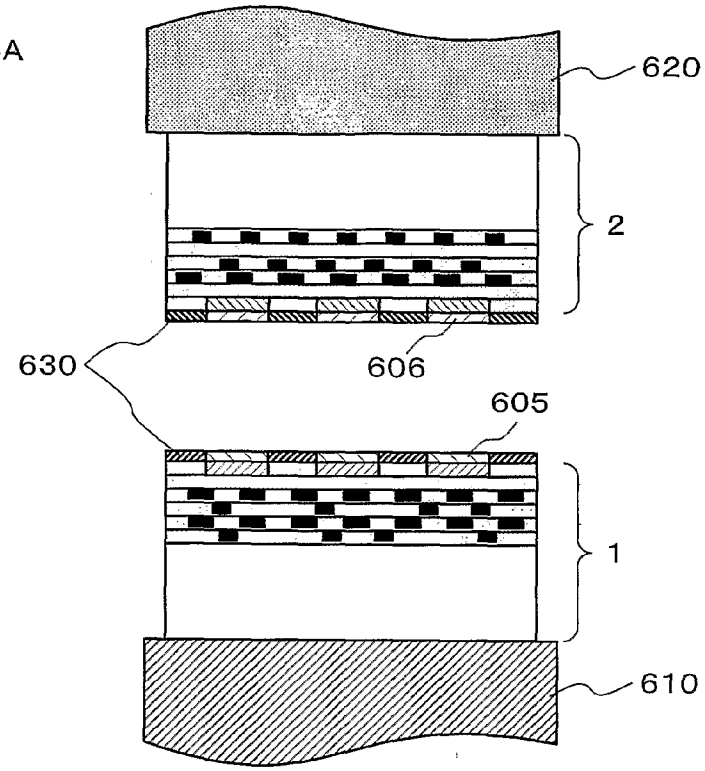



図46B

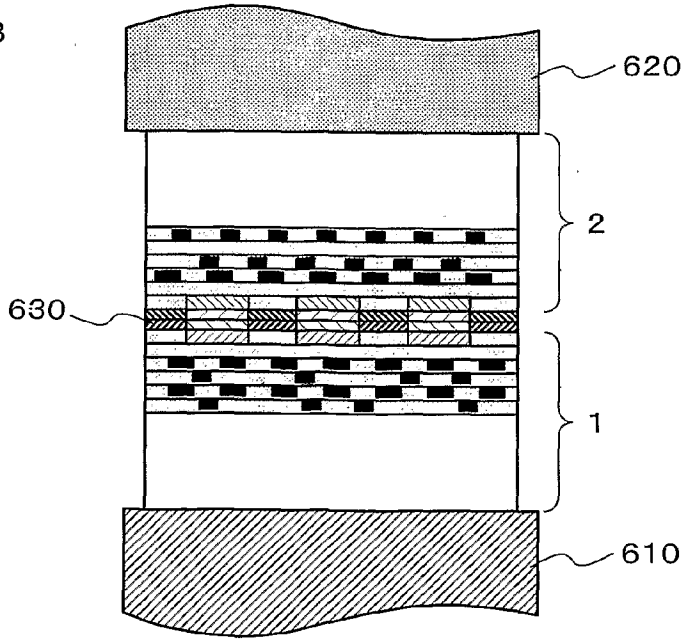
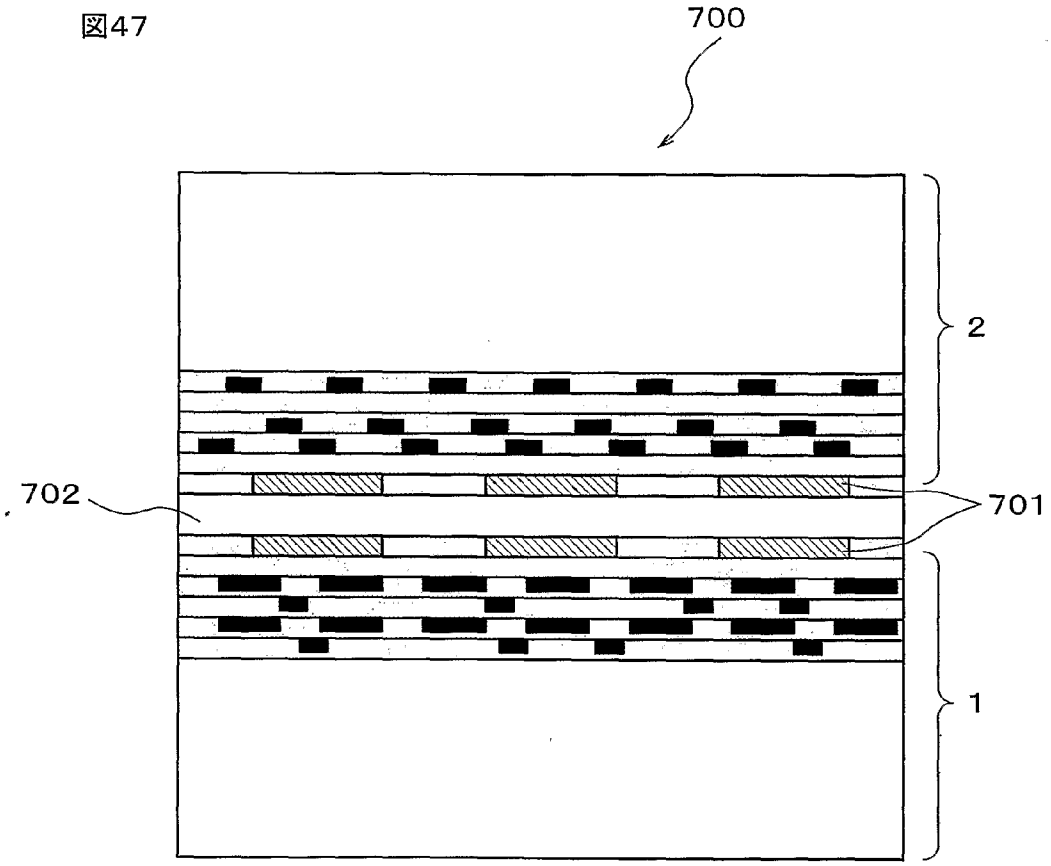
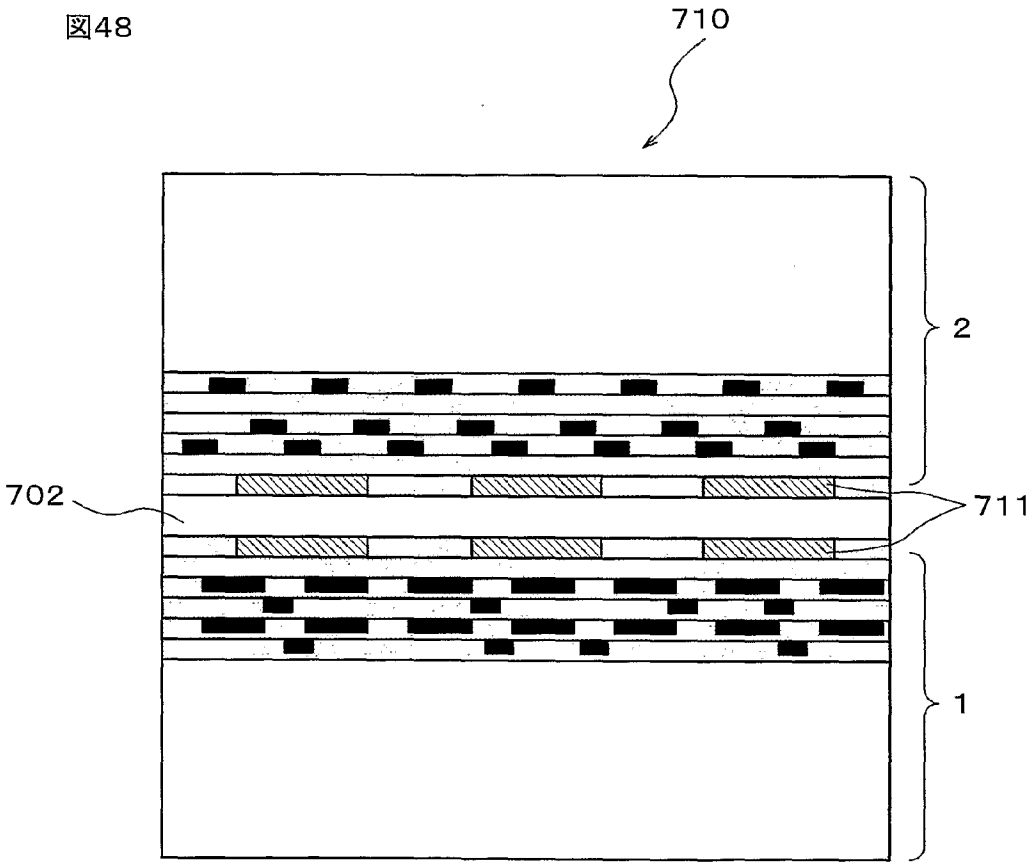


図47



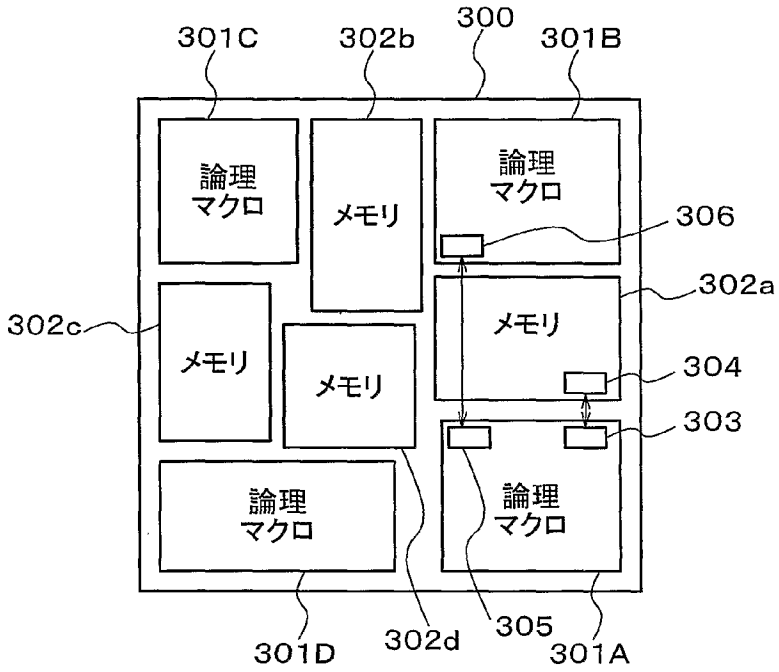

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**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/JP2009/065016

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/822(2006.01)i, G11C5/00(2006.01)i, H01L25/065(2006.01)i, H01L25/07(2006.01)i, H01L25/18(2006.01)i, H01L27/04(2006.01)i, H01L27/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L21/822, G11C5/00, H01L25/065, H01L25/07, H01L25/18, H01L27/04, H01L27/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009
Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | JP 2000-223661 A (Mitsubishi Electric Corp.), 11 August, 2000 (11.08.00), Full text & US 6208547 B1 & US 2001/0012231 A1 & US 2002/0048182 A1 | 1-27 |
| A | JP 2003-023138 A (Toshiba Corp.), 24 January, 2003 (24.01.03), Full text & US 2003/0015792 A1 & US 2004/0164425 A1 & US 2006/0148130 A1 & KR 10-2003-0007076 A & CN 1463036 A | 1-27 |
| A | JP 2000-076865 A (Kawasaki Steel Corp.), 14 March, 2000 (14.03.00), Full text (Family: none) | 1-27 |

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 14 September, 2009 (14.09.09) | 06 October, 2009 (06.10.09) |
| Name and mailing address of the ISA/ Japanese Patent Office | Authorized officer |
| Facsimile No. | Telephone No. |

Form PCT/ISA/210 (second sheet) (April 2007)

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/JP2009/065016

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | JP 2004-054993 A (Matsushita Electric Industrial Co., Ltd.), 19 February, 2004 (19.02.04), Full text (Family: none) | 1-27 |
| P,A | JP 2009-032857 A (Hitachi, Ltd.), 12 February, 2009 (12.02.09), Fig. 38 (Family: none) | 1-27 |



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国際調査報告

国際出願番号　ＰＣＴ／ＪＰ２００９／０６５０１６

Ａ．　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Int.Cl.　H01L21/822(2006.01)i, G11C5/00(2006.01)i, H01L25/065(2006.01)i, H01L25/07(2006.01)i, H01L25/18(2006.01)i, H01L27/04(2006.01)i, H01L27/10(2006.01)i

Ｂ．　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Int.Cl.　H01L21/822, G11C5/00, H01L25/065, H01L25/07, H01L25/18, H01L27/04, H01L27/10

最小限資料以外の資料で調査を行った分野に含まれるもの

| | |
|---|---|
| 日本国実用新案公報 | １９２２－１９９６年 |
| 日本国公開実用新案公報 | １９７１－２００９年 |
| 日本国実用新案登録公報 | １９９６－２００９年 |
| 日本国登録実用新案公報 | １９９４－２００９年 |

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

Ｃ．　関連すると認められる文献

| 引用文献のカテゴリー＊ | 引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示 | 関連する請求項の番号 |
|---|---|---|
| A | JP 2000-223661 A (三菱電機株式会社) 2000.08.11, 全文<br>& US 6208547 B1 & US 2001/0012231 A1 & US 2002/0048182 A1 | 1-27 |
| A | JP 2003-023138 A (株式会社東芝) 2003.01.24, 全文<br>& US 2003/0015792 A1 & US 2004/0164425 A1 & US 2006/0148130 A1<br>& KR 10-2003-0007076 A & CN 1463036 A | 1-27 |
| A | JP 2000-076865 A (川崎製鉄株式会社) 2000.03.14, 全文<br>(ファミリーなし) | 1-27 |

☑　Ｃ欄の続きにも文献が列挙されている。

☐　パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
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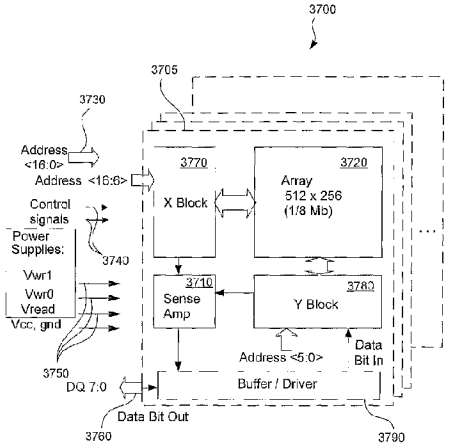
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*[Continued on next page]*

(54) Title: NON-VOLATILE PROGRAMMABLE MEMORY




(57) Abstract: A memory (3700) is provided. The memory includes an array of non-volatile memory cells (3720), each memory cell including a two terminal memory plug that switches from a first resistance state to a second resistance state upon application of a first write voltage pulse and reversibly switches from the second resistance state to the first resistance state upon application of a second write voltage pulse.

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# NON-VOLATILE PROGRAMMABLE MEMORY

## BACKGROUND OF THE INVENTION

Field of the Invention

**[0001]** The present invention relates generally to memory, and more specifically to re-writable non-volatile memory.

Description of the Related Art

**[0002]** Memory can either be classified as volatile or nonvolatile. Volatile memory is memory that loses its contents when the power is turned off. In contrast, non-volatile memory does not require a continuous power supply to retain information. Most non-volatile memories use solid-state memory devices as memory elements.

**[0003]** Certain conductive metal oxides (CMOs), for example, can be used as solid-state memory devices. The CMOs can retain a resistive state after being exposed to an electronic pulse, which can be delivered through two terminals. U.S. Pat. No. 6,204,139, issued March 20, 2001 to Liu et al. describes some perovskite materials that exhibit such characteristics. The perovskite materials are also described by the same researchers in "Electric-pulse-induced reversible resistance change effect in magnetoresistive films," Applied Physics Letters, Vol. 76, No. 19, 8 May 2000, and "A New Concept for Non-Volatile Memory: The Electric-Pulse Induced Resistive Change Effect in Colossal Magnetoresistive Thin Films," in materials for the 2001 Non-Volatile Memory Technology Symposium. However, the materials described in the 6,204,139 patent are not generally applicable to RAM memory because the resistance of the material, when scaled to small dimensions, is considered to be too large to make a memory with fast access times.

**[0004]** In US Pat. No. 6,531,371 entitled "Electrically programmable resistance cross point memory" by Hsu et al. resistive cross point memory devices are disclosed along with methods of manufacture and use. The memory device comprises an active layer of perovskite material interposed between upper electrodes and lower electrodes.

**[0005]** Similarly, the IBM Zurich Research Center has also published three technical papers that discuss the use of metal oxide material for memory applications: "Reproducible switching effect in thin oxide films for memory applications," Applied



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Physics Letters, Vol. 77, No. 1, 3 July 2000, "Current-driven insulator-conductor transition and nonvolatile memory in chromium-doped $SrTiO_3$ single crystals," Applied Physics Letters, Vol. 78, No. 23, 4 June 2001, and "Electric current distribution across a metal-insulator-metal structure during bistable switching," Journal of Applied Physics, Vol. 90, No. 6, 15 September 2001.

**[0006]** The discovery of the resistance-changing property of certain CMOs, however, is relatively recent and has not yet been implemented in a commercial memory product. There are continuing efforts to bring a true non-volatile RAM (nvRAM) to market.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a perspective view of an exemplary cross point memory array employing a single layer of memory;

FIG. 2 depicts a plan view of selection of a memory cell in the cross point array depicted in FIG. 1;

FIG. 3 depicts a perspective view of the boundaries of the selected memory cell depicted in FIG. 2;

FIG. 4A depicts a perspective view of an exemplary stacked cross point memory array employing a four memory layers;

FIG. 4B depicts a schematic diagram of the exemplary stacked cross point memory array depicted in FIG. 4A;

FIG. 5 depicts a schematic diagram of an exemplary stacked cross point memory array employing eight memory layers;

FIG. 6A depicts a schematic diagram of x-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A;

FIG. 6B depicts a schematic diagram of y-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A;

FIG. 7A depicts the general layout of the x-direction and y-direction driver sets depicted in FIG. 6A and FIG. 6B in relation to the stacked cross point array depicted in FIG. 4A;

FIG. 7B depicts an abstracted representation of FIG. 7A;

FIG. 8A depicts the general layout of interdigitated x-direction and y-direction driver in relation to the single layer cross point array depicted in FIG. 1;



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FIG. 8B depicts an abstracted representation of FIG. 8A;

FIG. 9A depicts the general layout of interdigitated x-direction and y-direction driver in relation to the stacked cross point array depicted in FIG. 4A;

FIG. 9B depicts an abstracted representation of FIG. 9A;

FIG. 10A and FIG. 10B depicts a schematic diagram of alternating x-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A;

FIGs. 11A through 11C depict various layouts of the x-direction and y-direction driver sets that have some drivers underneath the single-layer cross point array depicted in FIG. 1;

FIG. 12 depicts a layout of the x-direction and y-direction driver sets that interdigitate some drivers but not others such that some drivers are underneath the single-layer cross point array depicted in FIG. 1;

FIG. 13A depicts a layout of an x-direction driver set and a y-direction driver set that completely fits underneath the single-layer cross point array depicted in FIG. 1;

FIG. 13B depicts another layout of an x-direction driver set and a y-direction driver set that completely fits underneath the single-layer cross point array depicted in FIG. 1;

FIG. 14A depicts a layout of x-direction driver sets and a y-direction driver sets that completely fits underneath the stacked cross point array depicted in FIG. 4A;

FIG. 14B depicts a layout of x-direction driver sets and a y-direction driver sets that leaves empty gaps underneath the single-layer cross point array depicted in FIG. 4A;

FIG. 15A depicts a schematic diagram of x-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A;

FIG. 15B depicts a schematic diagram of y-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A;

FIG. 16 depicts an alternative schematic diagram of x-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A that uses separate drivers that operate on identical logic;

FIG. 17 depicts an alternative schematic diagram of y-direction driver sets in conjunction with the stacked cross point memory of FIG. 4A that eliminates the need for additional metal layers;

FIG. 18A depicts a layout of an x-direction driver set and a y-direction driver set that connects to the single-layer cross point array depicted in FIG. 1;



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FIG. 18B depicts a layout of multiple x-direction driver sets and y-direction driver sets that connects to the stacked cross point array depicted in FIG. 4A;

FIG. 19 depicts a layout of the X0 driver set that fit within the necessary line pitch;

FIG. 20A depicts a driver schematic in which the driver requires access to a primary decoder, a secondary decoder, and a reference voltage;

FIG. 20B depicts a layout of the three transistors depicted in FIG. 20A;

FIG. 21A depicts the driver depicted in FIG. 20B after a first metal layer is deposited;

FIG. 21B depicts the driver depicted in FIG. 21A after a second metal layer is deposited;

FIG. 22 depicts a layout of the last stage of drivers;

FIG. 23A depicts the driver depicted in FIG. 22 after a first metal layer is deposited;

FIG. 23B depicts the driver depicted in FIG. 23A after a second metal layer is deposited;

FIG. 24 depicts a cross section of the stacked cross point array of FIG. 4A;

FIG. 25A depicts a block diagram depicting the logical connections of various systems that contribute to selecting a memory plug;

FIG. 25B depicts a block diagram depicting the physical connections of the various systems that contribute to selecting a memory plug;

FIG. 26A depicts a block diagram depicting one mechanism for preventing the unselected conductive array lines from floating to an undesired voltage;

FIG. 26B depicts a block diagram depicting another mechanism for preventing the unselected conductive array lines from floating to an undesired voltage;

FIG. 26C depicts a block diagram depicting an improvement on the mechanism for preventing the unselected conductive array lines from floating to an undesired voltage depicted in FIG. 26B;

FIG. 26D depicts a block diagram depicting an improvement on the mechanism for preventing the unselected conductive array lines from floating to an undesired voltage depicted in FIG. 26C;

FIG. 26E depicts a block diagram depicting yet another mechanism for preventing the unselected conductive array lines from floating to an undesired voltage by using a 3-output driver;

FIG. 27 depicts a block diagram depicting one possible configuration of a 3-output driver;



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FIG. 28 depicts a timing diagram showing the falling edge of the write select signal being used to discharge the array lines;

FIG. 29 depicts a timing diagram showing the falling edge of the write select signal being used to discharge the conductive array lines;

FIG. 30 depicts a timing diagram showing the conductive array lines being discharged at the end of a write operation;

FIG. 31 depicts a timing diagram showing the array lines being discharged both as the write mode is selected and at the end of the write operation, as defined by an internal write timer pulse;

FIG. 32 depicts a timing diagram showing the array lines being discharged by the write select signal falling edge, data or address transitions;

FIG. 33 depicts a timing diagram with multiple addresses switching at different times;

FIG. 34A depicts an exemplary schematic of a detection circuit;

FIG. 34B depicts the timing of the detection circuit of FIG. 34A;

FIG. 35 depicts a schematic representation of memory cells laid out in a two-dimensional transistor memory array;

FIG. 36 depicts a diagrammatic cross sectional representation of a memory cell that can be used in the transistor memory array of FIG. 35;

FIG. 37A depicts a block diagram of a representative implementation of an exemplary 1 MB memory;

FIG. 37B depicts a block diagram of an exemplary memory that includes sensing circuits that are capable of reading multiple bits;

FIG. 38A depicts a page latch circuit for writing information in page mode and burst mode in accordance with an embodiment of the invention;

FIG. 38B depicts write command signals for writing information in page mode and burst mode in accordance with an embodiment of the invention;

FIG. 38C depicts a diagram of write signal input and corresponding output when writing information in page mode and burst mode in accordance with an embodiment of the invention;

FIG. 39A depicts input and data signals for reading information in page or burst mode;

FIG. 39B depicts input and data signals for writing information in page or burst mode;

FIG. 40 depicts a high-level conceptual diagram of an adaptive programming circuit of the present invention;



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FIG. 41A depicts a first more detailed embodiment of the adaptive programming circuit using a comparator;

FIG. 41B depicts a second more detailed embodiment of the adaptive programming circuit using a comparator;

FIG. 42 depicts a third circuit schematic level embodiment of the adaptive programming circuit with a bipolar voltage drive, a current comparison circuitry and an activating logic;

FIG. 43 depicts an exemplary timing diagram of signals and device currents during an application of the present invention in a re-writable memory array;

FIG. 44 depicts another embodiment of the adaptive programming circuit that can be used with a multi-level memory;

FIG. 45 depicts yet another embodiment of the adaptive programming circuit;

FIG. 46 depicts a simplified representation of a cross point memory array;

FIG. 47 depicts an exemplary cross point array where each memory cell includes a diode;

FIG. 48 depicts an exemplary cross point memory array where each memory cell includes a back to back diode;

FIG. 49 depicts the current-voltage, or "IV" characteristic of a back to back diode device;

FIG. 50 depicts the IV characteristic of one type of linear memory element;

FIG. 51 depicts the typical IV characteristics of both a memory element and a back to back diode in series;

FIG. 52 depicts an representative IV curve of a stack that exhibits non-ohmic behavior;

FIG. 53 depicts a cross sectional view of a partially processed integrated circuit up to the completion of a bottom front end of line section;

FIG. 54 depicts a cross sectional view of a further processed integrated circuit from FIG. 53 after the formation of a plurality of conductive plugs;

FIG. 55 depicts a cross sectional view of a further processed integrated circuit from FIG. 54 after the partial formation of a middle memory plug section atop the front end of line section;

FIG. 56 depicts a cross sectional view of a further processed integrated circuit from FIG. 55 after the complete formation of a middle memory plug section atop the front end of line section;



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FIG. 57 depicts a cross sectional view of a completely processed integrated circuit from FIG. 56 after the complete formation of a top metallization section atop the middle memory plug section;

FIG. 58 depicts a cross sectional view of a completely processed integrated circuit wherein the middle memory plug section further include features of a hard mask layer and a spacer;

FIG. 59A through FIG. 59E depict an exemplary sequence of various processing steps that could be used for the creation of the hard mask and spacer features of FIG. 58;

FIG. 60 depicts a cross sectional view of a completely processed integrated circuit wherein the middle memory plug section further include an optional undercut feature;

FIG. 61 depicts a cross-section of a prior art FET;

FIG. 62A depicts a section of a resistive memory material with charge traps;

FIG. 62B depicts an energy band diagram of the section of resistive memory material in FIG. 62A;

FIG. 63 depicts energy band diagrams of a Schottky barrier without and with a charged trap;

FIG. 64 depicts energy band diagrams of trap to trap conduction without and with trapped charge;

FIG. 65 depicts energy band diagrams of Frenkel-Poole conduction without and with charged trap; and

FIG. 66 depicts energy band diagrams of tunneling conduction through a Schottky junction without and with a charged trap.

It is to be understood that, in the drawings, like reference numerals designate like structural elements. Also, it is understood that the depictions in the figures are not necessarily to scale.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0007]** In the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order to avoid unnecessarily obscuring the present invention.



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*Cross Point Memory Array*

**[0008]** Conventional nonvolatile memory requires three terminal MOSFET-based devices. The layout of such devices is not ideal, usually requiring an area of at least $8f^2$ for each memory cell, where f is the minimum feature size. However, not all memory elements require three terminals. If, for example, a memory element is capable of changing its electrical properties (e.g., resistivity) in response to a voltage pulse, only two terminals are required. With only two terminals, a cross point array layout that allows a single cell to be fabricated to a size of $4f^2$ can be utilized.

**[0009]** FIG. 1 depicts a perspective view of an exemplary cross point memory array 100 employing a single layer of memory. A bottom layer of x-direction conductive array lines 105 is orthogonal to a top layer of y-direction conductive array lines 110. The x-direction conductive array lines 105 act as a first terminal and the y-direction conductive array lines 110 act as a second terminal to a plurality of memory plugs 115, which are located at the intersections of the conductive array lines 105 and 110. The conductive array lines 105 and 110 are used to both deliver a voltage pulse to the memory plugs 115 and carry current through the memory plugs 115 in order to determine their resistive states.

**[0010]** Conductive array line layers 105 and 110 can generally be constructed of any conductive material, such as aluminum, copper, tungsten or certain ceramics. Depending upon the material, a conductive array line would typically cross between 64 and 8192 perpendicular conductive array lines. Fabrication techniques, feature size and resistivity of material may allow for shorter or longer lines. Although the x-direction and y-direction conductive array lines can be of equal lengths (forming a square cross point array) they can also be of unequal lengths (forming a rectangular cross point array), which may be useful if they are made from different materials with different resistivities.

**[0011]** FIG. 2 illustrates selection of a memory cell 215 in the cross point array 100. The point of intersection between a single x-direction conductive array line 205 and a single y-direction conductive array line 210 uniquely identifies the single memory cell 215. FIG. 3 illustrates the boundaries of the selected memory cell 215. The memory cell is a repeatable unit that can be theoretically extended in one, two or even three dimensions. One method of repeating the memory cells in the z-direction (orthogonal to the x-y plane) is to use both the bottom and top surfaces of conductive array lines 105 and 110, creating a stacked cross point array.



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**[0012]** The repeatable cell that makes up the cross point array 100 can be considered to be a memory plug 305, plus 1/2 of the space around the memory plug, plus 1/2 of an x-direction conductive array line 205 and 1/2 of a y-direction conductive array line 210. Of course, 1/2 of a conductive array line is merely a theoretical construct, since a conductive array line would generally be fabricated to the same width, regardless of whether one or both surfaces of the conductive array line was used. Accordingly, the very top and very bottom layers of conductive array lines (which use only one surface) would typically be fabricated to the same size as all other layers of conductive array lines.

***Stacked Cross Point Memory Array***

**[0013]** FIGs. 4A and 4B depict an exemplary stacked cross point array 400 employing four memory layers 405, 410, 415, and 420. The memory layers, $ML_0$ 405, $ML_1$ 410, $ML_2$ 415 and $ML_3$ 420, are sandwiched between alternating layers of x-direction conductive array lines, $X_0$ layer 425, $X_1$ layer 430, and $X_2$ 435, and y-direction conductive array lines, $Y_0$ layer 440 and $Y_1$ layer 445. Stacking allows for the memory device to increase its memory capacity without increasing the footprint of the cross point array 400. A "memory layer," as the term is used herein, is not necessarily a homogenous layer of material, but a layer of memory plugs. Memory plugs are described below, and can be made up of several different layers of materials. The term "plug" is meant to be generally applicable to any stack or formation between complementary conductive array lines, and not intended to be limited to any manufacturing process.

**[0014]** Each memory layer 405, 410, 415, and 420 is associated with one layer 425, 430, or 435 of x-direction conductive array lines and one layer 440 or 445 of y-direction conductive array lines. Although the top conductive array line layers 435 and bottom conductive array line layer 425 are only used to supply voltage to a single memory layer 420 and 405, the other conductive array line layers 430, 440, and 445 can be used to supply voltage to both a top and a bottom memory layer 405, 410, 415, or 420.

**[0015]** Generally speaking, if each middle conductive array line layer were used for two memory layers, $N$ memory layers would require $N + 1$ layers of conductive array lines. However, although every memory plug in a cross point array would need to have two conductive lines, not every conductive line layer would need to have its own separate circuitry. Since selection of a memory plug requires both an x-direction



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conductive array line and a y-direction conductive array line to be active, multiple conductive array lines in both directions can be activated as long as only one memory layer can be activated.

**[0016]** For example, in the stacked cross point array 400, the top and bottom x-direction layers of conductive array lines (the $X_0$ layer 425 and the $X_2$ layer 435) can be logically related for accessing memory elements, and, in addition to sharing the same selection logic, may even share the same circuitry. Table 1 shows the combinations of x-direction conductive array lines and y-direction conductive array lines that can be used to activate a memory element on a specific memory layer.

| $X_0$, $X_2$ | $X_1$ | $Y_0$ | $Y_1$ | Memory Layer |
|---|---|---|---|---|
| x | | x | | $ML_0$ |
| | x | x | | $ML_1$ |
| | x | | x | $ML_2$ |
| x | | | x | $ML_3$ |

**TABLE 1**

**[0017]** Therefore, in order to access a memory cell on $ML_1$ 410, for example, one conductive array line from the $X_1$ layer 430 and one conductive array line from the $Y_0$ layer 440 would need to be selected.

**[0018]** Similarly, FIG. 5 depicts a configuration of a stacked cross point array 500 that uses eight memory layers 505, 510, 515, 520, 525, 530, 535, and 540. All of the x-direction conductive array line layers 545, 550, 555, 560, and 565 are connected to one of two thrus 570 or 575, and, therefore, share decoding logic. A thru, as used herein, is generally defined as a vertical conductive pathway between multiple metal layers that bypasses layers of memory plugs, but is otherwise very similar in function to vias and contacts. Each of the y-direction conductive array line layers 580, 585, 590, and 595, however, are driven by their own decoding logic. Table 2 shows the combinations of x-direction conductive array lines and y-direction conductive array lines that can be used to activate a memory element on a specific memory layer.



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| $X_0, X_2, X_4$ | $X_1, X_3$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | Memory Layer |
|---|---|---|---|---|---|---|
| x | | x | | | | $ML_0$ |
| | x | x | | | | $ML_1$ |
| | x | | x | | | $ML_2$ |
| x | | | x | | | $ML_3$ |
| x | | | | x | | $ML_4$ |
| | x | | | x | | $ML_5$ |
| | x | | | | x | $ML_6$ |
| x | | | | | x | $ML_7$ |

**TABLE 2**

***The Peripheral Circuitry***

**[0019]** One benefit of the cross point array is that the active circuitry that drives the cross point array (e.g., 100, 400, or 500) can be placed beneath the cross point array, therefore reducing the footprint required on a semiconductor substrate. FIG. 6A depicts x-direction driver sets 605, 610, and 615 that are used to select specific x-direction conductive array lines in the $X_0$ layer 425, $X_1$ layer 430, and $X_2$ layer 435 of the four memory layer stacked cross point array 400. Although the $X_0$ driver 605 and the $X_2$ driver 615 can use identical logic (as described in table 1), separate drivers are shown because of the difficulty in routing the single $X_0$ driver 605 around a thru 640 connecting the $X_1$ layer 430 to the $X_1$ driver 610.

**[0020]** FIG. 6B depicts y-direction driver sets 620 and 625 that are used to select specific y-direction conductive array lines in the y-direction conductive array line layers 440 and 445. The $Y_0$ driver set 620 uses a thru 630 that traverses one memory layer 405 in order to connect with the $Y_0$ layer 440. The $Y_1$ driver set 625 uses a thru 635 that traverses three memory layers 405, 410, and 415 in order to connect with the $Y_1$ layer 445.

**[0021]** FIG. 7A depicts the general layout of the x-direction and y-direction driver sets 605, 610, 615, 620, and 625 in relation to the stacked cross point array 400. FIG. 7B is a more abstracted representation of FIG. 7A. Since each driver set is on the same side the entire layout forms a non-symmetrical L-shape.



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**[0022]** However, certain designs may interdigitate the driver circuitry so that the driver that controls one conductive array line comes from one side and the driver that controls the next conductive array line comes from the opposite side.

***Interdigitated Driver Sets***

**[0023]** FIGs. 8A and 8B depict a layout of an interdigitated x-direction driver 805 and an interdigitated y-direction driver 810 that drive a single-layer cross point array 100. Interdigitating the drivers 805 and 810 not only allows for greater symmetry in a single-layer cross point array 100, but also permits the drivers to be fabricated to larger dimensions.

**[0024]** Drivers can be considered to be interdigitated when alternating lines in the same conductive array line layer are driven from different locations. Such oppositely driven lines may be alternate, i.e. even numbered lines are driven from one side and odd numbered lines are driven from the opposite side, or grouped by pair where 2 lines driven from one side are adjacent and two lines driven from the other side are next to them, or grouped in any arrangement which allows the use of a driver which is laid out in the pitch of 2 x $N$ cells, and drives $N$ lines. By extension, we call "interdigitated driver set" a set of drivers driving interdigitated lines even though the drivers themselves need not be interdigitated.

**[0025]** FIGs. 9A and 9B depict a layout of driver sets 605, 610, 620, and 625 for the stacked cross point array 400 that are interdigitated. The configuration of the x-direction driver sets 605 and 610 are depicted in FIGs. 10A and 10B. The configuration of FIG. 10A is alternated with the configuration of FIG. 10B for each x-direction conductive array line so that both the $X_0$ driver 605 and the $X_1$ driver 610 alternate sides.

**[0026]** Additionally, by placing the thru 640 that connects the $X_1$ layer 430 to the $X_1$ driver 610 and thru 645 that connects the $X_2$ layer 435 to the $X_0$ driver 605 on opposite sides, the bottom $X_0$ layer 425 can be directly tied to the $X_2$ layer 435. Therefore, a single $X_0$ driver 605 can be used for both the bottom $X_0$ layer 425 and the top $X_2$ layer 435.

**[0027]** The layouts shown in FIGs. 7B, 8B and 9B assume that the drivers 605, 610, 615, 620, 625, 805, and 810 all lay outside the cross point array 100 or 400. However, if the substrate underneath a cross-point array is used to draw the peripheral circuitry, the footprint of the entire memory chip can be reduced.



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**[0028]** FIGs. 11A through 11C depict various layouts of the x and y direction driver sets 805 and 810 that have some drivers underneath the single-layer cross point array 100. In each layout, some drivers are left outside of the single-layer cross point array 100 even though there may be unused space underneath the cross point array 100. In FIG. 11A the layout forms a rectangle that extends beyond the cross point array 100 in the x-direction. In FIG. 11B the layout forms an H-shape that extends beyond the cross point array 100 in the y-direction. In FIG. 11C the layout forms an asymmetric shape that, while extending beyond the cross point array 100 in both the x-direction and y-direction, forms a more symmetrical pattern.

**[0029]** FIG. 12 depicts an alternative layout of the x and y direction driver sets 805 and 810 that interdigitate some drivers but not others. Portions of each driver set 805 and 810 are still outside the single-layer cross point array 100. However, assuming each driver is fabricated to common dimensions, a portion of the non-interdigitated driver would still extend beyond the cross point array 100 because non interdigitated drivers drive twice as many lines in the same pitch, and therefore necessitate more circuitry.

**[0030]** However, if none of the drivers 805 and 810 are interdigitated, then the entire peripheral circuitry might be placed underneath the single-layer cross point array 100.

***Non-Interdigitated Driver Sets***

**[0031]** FIG. 13A depicts a layout of an x-direction driver 805 and a y-direction driver 810 that completely fits underneath the single-layer cross point array 100. FIG. 13B depicts an alternate layout of the x-direction driver 805 and the y-direction driver 810 that uses a more symmetrical layout.

**[0032]** The concept of using non-interdigitated driver sets can be extended to stacked cross point arrays. FIGs. 14A and 14B depict layouts of non-interdigitated driver sets 605, 610, 620, and 625. It should be appreciated that each driver set 605, 610, 620, or 625, is not necessarily to scale, and, depending upon both the number of lines in each conductive array line layer and the circuitry used for each driver, each driver set 605, 610, 620, or 625, may completely fit underneath the stacked cross point array 400, leave empty gaps underneath the stacked cross point array 400, as shown in FIG. 14B, or extend beyond the footprint of the stacked cross point array 400.



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**[0033]** FIGs. 15A and 15B depicts one possible configuration of the driver sets 605, 610, 620 and 625 that can be used in the layout of FIGs. 14A or 14B. While the $X_0$ driver set 605 can directly connect with the $X_0$ layer 425 (and the $X_2$ layer 435 via the thru 645) and the $X_1$ and $Y_1$ driver sets 610 and 625 can be directly connected to their $X_1$ and $Y_1$ layers 430 and 445 via their respective thrus 640 and 635, the $Y_0$ driver set 620 will not be able to directly connect to the thru 630 that connects the peripheral circuitry to the $Y_0$ layer 440. Instead, the $Y_0$ driver set 620 uses an extra metal layer 1505 in the peripheral circuitry portion in order to connect to the thru 630 by going over the circuitry of the $Y_1$ driver set 625. The extra metal layer 1505 is in addition to any metal layers that may be necessary to construct the driver circuitry.

**[0034]** FIG. 16 depicts an alternate configuration for the x-direction driver sets 605, 610, and 615. Since the extra metal layer 1505 is used in connection with the y-direction drivers 620 and 625, the configuration of FIG. 15 also utilizes the extra metal layer 1505. By separating the $X_0$ driver set 605 from the $X_2$ driver set 615, the load on the $X_0$ driver is reduced even if the two drivers 605 and 615 use identical logic. This modification can improve the access time to layer 425 and 435.

**[0035]** FIG. 17 depicts yet another configuration for the y-direction driver sets 620 and 625 that can be used to eliminate the need for the extra metal layer 1505. In this configuration, one x-direction conductive array line is eliminated from the $X_0$ layer 425, creating an array cut that allows the $Y_0$ driver set 620 to directly connect with the thru 630 that connects the $Y_0$ driver set 620 to the $Y_0$ layer 440. While one line of memory plugs would be eliminated from the $ML_0$ layer 405, their absence would represent a very small percentage of the total memory plugs in the stacked cross point array 400 and may be a fair tradeoff for a peripheral circuitry design that does not use an extra metal layer 1505. Cells in layers $ML_1$ 410, $ML_2$ 415, and $ML_3$ 420 straight above the eliminated $ML_0$ array line can either be eliminated, or be kept as non-functional dummy cells. This way, the four array layers are symmetrical. Alternatively, the bottom $ML_0$ memory layer could use a redundancy line to replace the missing line.

**[0036]** Additionally, if the $Y_0$ driver set 620 is moved to the middle of the stacked cross point array 400, the access time for the $Y_0$ layer 440 is improved. If the $Y_0$ driver set 620 is at one end of the conductive array lines then current would need to travel to the opposite end in order to reach the active memory cell in the worst case scenario. However, if the $Y_0$ driver set 620 is positioned in the middle of the



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conductive array lines, the current would only need to travel half the length of the conductive array line in the worst case scenario. Access time is, therefore, improved by having the $Y_0$ driver set 620 positioned in the middle of the conductive array lines.

**[0037]** FIG. 18A depicts a layout of an x-direction driver 805 and a y-direction driver 810 that are both centered underneath the single-layer cross point array 100. The y-direction driver 810 can use the array cut to reach the middle of the y-direction conductive array lines 110 and the x-direction driver can be positioned anywhere under the x-direction conductive array lines 105 as long as it does not overlap with another driver. Moving both drivers 805 and 810 substantially to the middle of their respective conductive array lines 105 and 110 further reduces the access time to the memory plug layer 115.

**[0038]** Such a layout would be most effective for either a single layer cross point array or the bottom layer of a stacked cross point array. In the case of a stacked cross point array, while the $X_0$ driver set 605 and $Y_0$ driver set 620 are positioned substantially in the middle of cross point array 400, the other driver sets would typically connect to the ends of the conductive array lines for the upper conductive array line layers.

**[0039]** FIG. 18B depicts a layout of driver sets for a stacked cross point array 400 where the bottom memory layer has a faster access time than upper memory layers. Certain applications might require that a portion of memory be accessed faster than other portions. For example a mass storage device might want to be able to access its file allocation tables (FAT) quicker than other stored data.

***Non-Interdigitated Driver Design***

**[0040]** The designs depicted in FIGs. 13A through 18B all presume that non-interdigitated drivers are used. FIG. 19 depicts one possible layout of the $X_0$ driver set 605 that would make it possible to fit the line drivers within the line pitch necessary for non- interdigitated drivers. Each driver would be responsible for supplying voltage to a specific conductive array line (or group of conductive array lines if the driver set supplied voltage to multiple memory layers). Therefore, if there were 256 conductive array lines on the $X_0$ layer 425, there would be 256 drivers in the $X_0$ driver set 605. The drivers deliver voltage to the conductive array lines through metal interconnects 1905. Each metal interconnect 1905 would preferably be fabricated to be the same width as the conductive array lines. Since each driver in FIG. 19 spans four metal interconnects, stacking the drivers four deep ensures that the



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entire $X_0$ driver set 605 fits within the required parameters. In general terms, if a line driver group contained $N$ line drivers, and if a memory cell was fabricated to a width of $W$, then the line driver group could not have a width greater than $N \times W$ if the drivers were to fit completely underneath the cross point array.

**[0041]** It should be appreciated that additional peripheral circuitry may be needed in addition to the drivers. For example, the drivers might require access to both a primary decoder and a secondary decoder. The primary decoder is capable of selecting a single group of, for example, eight drivers (e.g., 1910), but not a specific driver, and the secondary decoder is capable of selecting a single driver (e.g., 1915), but not a specific group of eight drivers. Although the secondary decoder connections are not shown in FIG. 19, the primary decoder activates the group of eight drivers through a metal interconnect line 1920. If the primary decoder selected a group of, say, sixteen drivers, then the metal interconnect line 1920 could be tied to a metal interconnect line of another set of eight drivers. The secondary decoder would then select a single driver out of the group of sixteen drivers. More detailed information about the additional peripheral circuitry is described later. If there were room underneath the cross point array (e.g., the configuration shown in FIG. 14B), at least some of the additional peripheral circuitry required for the primary and secondary decoders could be placed underneath the cross point array.

**[0042]** FIG. 20A depicts one possible driver schematic in which the driver 1915 requires access to a primary decoder, a secondary decoder, and ground (or another reference voltage). The driver 1915 is made up of a pass device (one p-channel transistor 2005 and one n-channel transistor 2010) and a transistor 2015 to ground. The transistor to ground 2015 can be either an n-channel transistor or a p-channel transistor, depending upon how it is connected to the pass device.

**[0043]** FIG. 20B depicts one layout of the three transistors 2005, 2010, and 2015 that make up the driver 1915. Since one of the transistors 2005 of the pass device is a p-channel transistor, it must be fabricated in a portion of the semiconductor substrate that is n-doped 2020. In order to conserve space, each transistor 2005, 2010, and 2015 shares a node 2025, 2030, and 2035 with a transistor from another driver 1925 in the group of eight drivers 1910. The nodes can be shared because the entire group of eight drivers 1910 receives the same input 1920 from the primary decoder into each pass device and the third transistor in each driver is tied to ground.



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**[0044]** Making the various connections can be accomplished through well-known process steps. FIG. 21A depicts the driver 1915 after a first metal layer is deposited that provides vertical connections 2105, 2110, 2115, and 2120 from the driver to other peripheral circuitry and/or other drivers. The transistor to ground 2015 can share its vertical connection 2115 to ground with every grounded transistor in the same horizontal position as the drivers 1915 and 1925. However, in order to reduce load alternative layouts may not tie all the drivers together. Similarly, the gates of each transistor 2005, 2010 and 2015 in the driver 1915 that takes inputs from the secondary decoder can share their vertical connections 2105, 2110, and 2115 with the gates of other drivers that have the same position in relation to the group of eight drivers 1910. Although not shown in FIG. 21A, the gate of the grounded transistor 2015 and the gate of the p-channel transistor 2005 are driven by the same input from the secondary decoder as shown in FIG. 20A.

**[0045]** Although a single via 2125, 2130, 2135, and 2140 is shown connecting each of the transistors 2005, 2010, and 2015 to their corresponding vertical connections 2105, 2110, 2115, and 2120, it should be appreciated that multiple vias might be used in order to improve performance. Similarly, different designs might use vertical connections 2105, 2110, 2115, and 2120 that are wider than a single feature size in order to similarly improve performance.

**[0046]** FIG. 21B depicts the driver 1915 after a second metal layer is deposited. The second metal layer provides the horizontal connections 2145, 2150, and 1920 that make the logical connections between the three transistors 2005, 2010, and 2015. The transistors 2005 and 2010 in the pass device are tied together with two horizontal connectors 2145 and 1920. Additionally, the horizontal connector 1920 that connects the nodes 2025 and 2030 of the pass device that is common to the two drivers 1915 and 1925 extends beyond the driver 1915 boundaries to the other drivers in the group of eight drivers 1910 and carries signals from the primary decoder.

**[0047]** Horizontal connector 2150 also connects the transistor to ground 2015 to the pass device transistors 2005 and 2010. In one embodiment, connector 2145 and connector 2150 are the same line, ensuring that all three transistors 2005, 2010, and 2015 are tied together. The horizontal connector 2150 is preferably the same line pitch as the conductive array lines because the horizontal connector 2150 is the beginning of the metal interconnect that joins the driver 1915 to the appropriate conductive array line. The other metal interconnects from the other drivers in the



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group of eight drivers 1910 are also formed on the second metal layer as shown in FIG. 19. Although other embodiments could use more metal layers, such designs would typically result in a more costly fabrication process.

**[0048]** The last column 1930 of drivers uses a slightly different layout than the previous three columns 1935, 1940, and 1945. Since the circuitry is laid out in the pitch of 8 array lines, which is intended to be minimum pitch, and the circuitry drives 8 conductive array lines, there is no space left for the line 1920 that drives the common nodes of the pass device. FIG. 22 depicts the layout for the drivers in the last column 1930. The gates 2205, 2210, 2215, and 2220 of the pass devices 2225 are lengthened with extensions 2230, 2235, 2240, and 2245. Although lengthening the pass devices 2225 increases the width of the last column 1930, such lengthening allows for the first metal layer to be used for both horizontal and vertical connections within the pass devices 2225

**[0049]** FIG. 23A depicts the driver in the last column 1930 after a first metal layer is deposited. A horizontal connector 2305 can directly connect the common node of the pass devices 2225 because the vertical connections 2310, 2315, 2320, and 2325 lie on the exterior of the pass devices 2225. Additionally, the horizontal connector 2305 extends to the beginning of a via 2330, which is how the last column 1930 receives its input 1920 from the primary decoder.

**[0050]** FIG. 23B depicts the driver in the last column 1930 after the second metal layer is deposited. The input 1920 from the primary decoder delivers its signal to the pass devices 2225 through the via 2330, which connects to the horizontal connection 2305 on the first metal layer. Allowing the primary decoder input 1920 to drop to the first metal layer makes an additional line available on the second metal layer, such that all eight metal interconnects 1905 from the group of eight drivers 1910 fit on the minimum line pitch.

***Cross Point Array Design***

**[0051]** Once these front end of line (FEOL) processes are complete (which, in the previous example, includes the metallization layers that were described in FIG. 21B and FIG. 23B), the cross point array can be fabricated on top of the active circuitry. FIG. 24 depicts the exemplary stacked cross point array 400 employing thrus 2405 and 2410 for the two upper layers of x-direction conductive array lines 430 and 435. As will be appreciated by those skilled in the art, similar thrus could also be used to connect the peripheral circuitry to the y-direction conductive array lines 440 and 445.



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**[0052]** The thru 2405 that connects the $X_1$ layer 430 to the peripheral circuitry would go through at least two inter-layer dielectric (ILD) layers 2415 and 2420. ILD layers provide several functions, including isolation between conductive array lines and providing a substrate for conductive array lines that would otherwise need to span empty spaces.

**[0053]** The thru 2410 that connects the $X_2$ layer 435 to the peripheral circuitry would go through at least four ILD layers 2415, 2420, 2425, and 2430. Although the thrus 2405 and 2410 may share some of the same processing steps as the memory layers, a conductive material 2435 would need to be used to connect the conductive array lines to the peripheral circuitry. The conductive material will typically be deposited in separate processing steps that include masking the area that is to have the conductive material 2435 while the memory layers are deposited.

***Driver Designs***

**[0054]** As illustrated in the exemplary embodiments shown FIGs. 25A and 25B, each conductive array line 205, 210, 220, 225, 230, 235 and 240 is associated with a pass device 2505, 2510, 2515, 2520, 2525, 2530 and 2535 (one n-type and one p-type transistor). The gate voltages of each transistor can be adjusted such that the selected conductive array lines 205 and 210 are allowed to pass a voltage from primary decoders 2540. The voltage that is passed can either be the full voltage from the primary decoders 2540 during a write operation (e.g., a magnitude of 3 volts), a partial voltage during a read operation (e.g., a magnitude of 2 volts), or no voltage for the unselected lines in an unselect mode. Therefore, the pass devices 2505 can act as part of the decoding circuitry as a type of modulating circuit, allowing one conductive array line to be on ("selected") at either a read or write voltage and the other conductive array lines to be off ("unselected"). FIG. 25A illustrates the logical connections and FIG. 25B illustrates the same connections, but with a different physical layout (the pass devices alternating on each end of the conductive array lines).

**[0055]** Alternatively, in place of the pass devices pass device 2505, 2510, 2515, 2520, 2525, 2530 and 2535, a single transistor can be used. However, the transistor's gate voltage would need to be such that it could pass large magnitude voltages. For example, an n-channel transistor would pass the full 3V if its gate were held to 3V plus the n-channel transistor's threshold voltage. A single transistor could still act as a modulating circuit by only partially turning on the transistor.



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**[0056]** In another embodiment, the modulation is performed upstream of the gate circuit such that the input to the gate circuit would already be at an appropriate read or write voltage. In this embodiment, the gate circuit would only have a first select mode (passing substantially the full input voltage) and an unselect mode (passing substantially no voltage).

**[0057]** It should be noted that if the unselected conductive array lines 220, 225, 230, 235 and 240 were not held to a certain voltage, they would be considered floating, which is generally discouraged in circuit design. Specifically, a problem would arise if, for example, an unselected y-direction conductive array line 240 were floating at -3 volts. If the selected x-direction conductive array line 205 was at 3 volts and the selected y-direction conductive array line 210 was at -3 volts, two cells 215 and 2545 would see a 6-volt drop, potentially disturbing the resistive states of both cells.

**[0058]** FIG. 26A illustrates one mechanism for preventing the unselected conductive array lines 220, 225, 230, 235 and 240 from floating to an undesired voltage. Prior to a read or write operation, each pass device 2505, 2510, 2515, 2520, 2525, 2530 and 2535 would have both of their transistors turned on, the primary decoders 2540 would be deactivated, and voltage reference generators 2605 would be at some reference voltage (presumed to be ground). Therefore, all the conductive array lines 205, 210, 220, 225, 230, 235 and 240 would be pulled to the reference voltage. During the read or write operation, the voltage reference generator 2605 would be deactivated, the primary decoders 2540 would be activated, and only the appropriate pass devices 2505 and 2510 would be on, bringing the selected conductive array lines 205 and 210 to the driver voltage. Although the unselected conductive array lines 220, 225, 230, 235 and 240 would be floating during a read or write operation, their parasitic capacitance might keep them at the reference voltage for the time it takes to do a normal read or write cycle. However, lateral coupling capacitance will work against the parasitic capacitance, raising the voltage on the unselected conductive array lines 220, 225, 230 and 235 adjacent to the selected conductive array lines 205 and 210.

**[0059]** FIG. 26B illustrates another mechanism for preventing the unselected conductive array lines 220, 225, 230, 335 and 240 from floating to an undesired voltage. Each conductive array line 205, 210, 220, 225, 330, 235 and 240 would have an associated grounding pass device 2610, 2615, 2620, 2625, 2630, 2635 and 2640



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that allows the conductive array lines 205, 210, 220, 225, 230, 235 and 240 to be pulled to ground when activated.

**[0060]** The grounding pass devices 2610, 2615, 2620, 2625, 2630, 2635 and 2640 could be activated prior to a read or write operation (similar to the operation described in connection with FIG. 26A), could be triggered by the selection of a conductive array line, or could always be kept on. If the grounding pass devices 2610, 2615, 2620, 2625, 2630, 2635 and 2640 were always on, their relative size would need to be small in relation to the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535 so that the leakage to ground would have a small effect.

**[0061]** If the grounding pass devices 2610, 2615, 2620, 2625, 2630, 2635 and 2640 were triggered by the selection of a conductive array line, the process of selecting the x-direction conductive array line 205, would activate the decoding pass device 2505 and deactivate the grounding pass device 2610 associated with the selected conductive array line 205 while deactivating the decoding pass devices 2515 and 2520 and activating the grounding pass devices 2635 and 2640 associated with the unselected conductive array lines 220 and 225. Similarly, selecting the y-direction conductive array line 210 would activate the decoding pass device 2510 and deactivate the grounding pass device 2615 associated with the selected conductive array line 210 while deactivating the decoding pass devices 2525, 2530 and 2535 and activating the grounding pass devices 2620, 2625 and 2630 associated with the unselected conductive array lines 230, 235 and 240.

**[0062]** FIG. 26C is an improvement on FIG. 26B. However, instead of pass devices 2610, 2615, 2620, 2625, 2630, 2635 and 2640, a single transistor 2645, 2650, 2655, 2660, 2665, 2670 and 2675 is used. Assuming the transistors 2645, 2650, 2655, 2660, 2665, 2670 and 2675 were n-channel devices, they would be on only if the gate voltage were held to at least the threshold voltages of the transistors. Similarly, if the transistors were p-channel devices, they would be on if the gate voltages were held to at least the negative threshold voltages. Therefore, an appropriate gate voltage can fully discharge the conductive array lines.

**[0063]** The single n-channel (or p-channel) transistor embodiment can be used either at the beginning of a cycle or by using the inverse of the signal that activates the n-channel (or p-channel) portion of the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535. As shown in FIG. 26D, in some embodiments, the single n-channel (or p-channel) transistor's activating signal might simply use the activating



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signal of the p-channel (or n-channel) portion of the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535.

**[0064]** FIG. 26E illustrates yet another mechanism for preventing the unselected conductive array lines 220, 225, 230, 235 and 240 from floating to an undesired voltage by using a 3-output driver 2680. Since the 3-output driver 2680 would deliver a voltage to all of the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535, such a mechanism could not be used while a specific conductive array line was being selected. Therefore, the 3-output driver 2680 could either be used to discharge the floating voltages prior to a read or write operation. Alternatively, the 3-output driver 680 could be used during a read or write operation if it were only used in connection with unselected banks.

**[0065]** FIG. 27 illustrates one possible configuration of a 3-output driver 2680. A p-channel transistor 2705 and an n-channel transistor 2710 are arranged in series. The n-channel transistor may be in a separate well from the CMOS logic because its substrate is tied to a negative voltage. The source of the p-channel transistor 2705 is connected to a voltage source of $+1/2\ V_W$ (e.g., +3 V) and the source of the n-channel transistor 2710 is connected to a voltage source of $-1/2\ V_W$ (e.g., -3 V). The drains of both transistors are connected to both the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535 and transistor to ground 2715. In order to discharge the entire line, the transistor to ground 2715 would need to have an appropriate gate voltage, as described in connection with FIG. 26C, or be a pass device. The 3-output driver 2680 would function when only one transistor 2705, 2710 or 2715 was on, while the other two transistors were off.

**[0066]** Depending on the embodiment, the driver 2540 or the 3-output driver 2680, must be able to supply either $+1/2\ V_W$ or $-1/2\ V_W$ to the decoding pass devices 2505, 2510, 2515, 2520, 2525, 2530 and 2535. This is because applying a voltage pulse in one direction ($+V_W$) will decrease the resistive state of the memory cell from $R_0$ to $R_1$ and applying a voltage pulse in the opposite direction ($-V_W$) will increase the resistive state from $R_1$ to $R_0$.

**[0067]** The polarity of the voltage drop is not important during a read. The resistive state of the memory cell can be detected regardless of whether the x-direction conductive array line 205 is $V_R$ (e.g., 4 V) higher or $V_R$ lower than the y-direction conductive array line 210. However, it is desirable to alternate polarities of reads to reduce the effect of long term read disturbs on the memory elements.



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**[0068]** Additionally, a write operation could be preceded by a read operation in order to ensure a write is necessary. In other words, $+V_W$ should only be applied to a memory plug in its $R_0$ resistive state and $-V_W$ should only be applied to a memory plug in its $R_1$ resistive state. By ensuring that a voltage pulse is only used when the memory cell needs to change state, the memory cell would not either be placed in a resistive state lower than $R_1$ or higher than $R_0$ or suffer any degradation that occurs with certain memory cells. Additionally, avoiding a write operation will reduce disturbing the unselected cells and improve the endurance of the selected cell, avoiding unnecessarily stress on the cross point memory array. However, use of an adaptive programming scheme could avoid the need for a read operation before a write operation. Adaptive programming is described below.

**[0069]** If a read operation is used prior to a write operation, the polarity of the read can be the same as the polarity of the write operation that would follow, if required. For example, if the data to be written is "0" then the selected x-direction conductive array line 205 would be 3V and the selected y-direction conductive array line 210 would be -3V. If the read operation preceding the write used +2V on the selected x-direction conductive array line 205 and -2V on the selected y-direction conductive array line 210, then the circuitry would only need to switch 1V for both conductive array lines 205 and 210. This can be preferable to the alternative (-2V on the selected x-direction conductive array line 205 and +2V on the selected y-direction conductive array line 210), which would require the voltage to switch a total of 5V.

***Timing of Discharge***

**[0070]** Since the memory cell is capable of being programmed with very little current, floating conductive array lines may create disturb conditions. If an unselected conductive array line inadvertently stays charged, it may be at a high enough voltage to affect the state of unselected cells on that line.

**[0071]** Discharging the selected conductive array line after a voltage has been applied is not only useful to avoid disturb conditions, but may be necessary in certain architectures where the line drivers are not strong enough to quickly drive a conductive array line from one state to another. As previously discussed, a re-programmable memory experiences at least three different operational voltages: $-V_W$ (to be programmed into a high state) $+V_W$ (to be programmed into a low state), and $V_R$ (to read the data in the cell). Each conductive array line would typically carry half of the voltage such that only the selected cells in the array would experience the full



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voltage. In such a system, it is possible that a conductive array line be required to be driven to half $-V_W$ immediately after being held to half $+V_W$.

**[0072]** Since the most common reference voltage is ground, application of the reference voltage is referred to as "discharge." However, it should be understood that the lines could be equalized (tied together to a common node) to realize the same purpose.

**[0073]** FIG. 28 is a timing diagram showing the falling edge of the write select signal (labeled "Write Enable #") being used to discharge the array lines. The actual write operation is triggered by the rising edge of the Write Enable # signal with the address and data signals typically being latched. By using this falling edge, the conductive array lines are discharged prior to a write operation. The data and address information associated with the write operation are not applied to the memory array until after the conductive array lines are discharged.

**[0074]** FIG. 29 is a timing diagram showing the falling edge of the write select signal being used to discharge the conductive array lines. By the time the write select signal changes state, the data and address signals usually will have been applied and become stable. However, the write operation would be delayed by the discharged time, which may not be preferable in certain architectures as it would delay the write operation and slow the performance of the memory chip.

**[0075]** FIG. 30 is a timing diagram showing the conductive array lines being discharged at the end of a write operation. A prolonged write operation could saturate or damage the memory element. Accordingly, a timer is used to terminate the internal write operation. The falling edge of the internal write timer pulse is used to trigger a discharge pulse. Use of the timer ensures that the array lines are free of charge after the write operation, and ready for further operations.

**[0076]** FIG. 31 is a timing diagram showing the array lines being discharged both as the write mode is selected and at the end of the write operation, as defined by an internal write timer pulse. As will be appreciated by those skilled in the art, many of the discharge schemes can similarly be combined for improved operation.

**[0077]** FIG. 32 is a timing diagram showing the array lines being discharged by the write select signal falling edge, data or address transitions. Such discharge pulses are obtained with a signal transition detector, which will be further detailed in connection with FIG. 34. Such a scheme may be beneficial if a discharge is desired



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while the write select signal is not switching, if only one address or one data signal switches.

**[0078]** FIG. 33 is a timing diagram with multiple addresses switching at different times. The changes in the address create multiples signal transition pulses, which can be combined as a logical OR to create a transition detection pulse. The OR'd transition signal can then either act as a discharge signal or trigger a discharge signal.

**[0079]** In a first approach, the discharge signal is applied to conductive array lines while addresses are being decoded. Since the address bus has address signals switching at different times, and an internal delay may occur in the circuitry generating the discharge pulse, it is possible for some unselected array lines to switch momentarily, temporarily selecting the wrong memory cells, as is depicted by the "X, Y Lines" signal in FIG. 33. During a read operation the switching noise may disturb the following read operation.

**[0080]** In a second more preferable approach, the address signals going to the decoders of the array lines are delayed sufficiently so that the array lines would switch during the discharge pulse. Such a technique ensures a clean operation of the conductive array lines without spurious selection of unselected memory cells, therefore reducing switching noise, as depicted by the "X, Y Lines With Delayed Addresses" signal in FIG. 33. Such a scheme can be further used for continuous write operations where new data or new addresses trigger a new write while the memory chip stays in write mode. By ensuring that address transitions are clean and no intermediate lines get selected, write cycles can be accomplished without disturb to undesired memory cells.

**[0081]** The detection circuit can be made in many ways. FIG. 34A shows an exemplary schematic of a detection circuit 3400. The detection circuit is a logic AND gate 3405, which compares the input signal 3410 (whose edge is to be detected) and the same signal 3410 after it has been delayed and inverted 3415. When a transition on this signal 3410 occurs, the delayed and inverted transition 3415 will reach the AND gate 3405 later than the signal 3410 itself. During the time where the delayed signal has not reached the AND gate, the output 3420 of the gate will switch and a pulse is created. FIG. 34B shows the timing of the detection circuit

**[0082]** To detect both rising and falling edges, two such circuits can be combined, with inverted inputs and OR'ed outputs. If it is desired to trigger on only one edge (either rising or falling), only one such circuit is used.



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[0083] Such a combination can be repeated for all address and control signals, and all the outputs of these circuits can be OR'ed together, so that if any of these signals transitions, a pulse will be generated. As explained above, the resulting pulse can be used to trigger a pulse of appropriate duration for discharge of the array lines. This transition detection pulse can then be used to control different elements of the memory circuits.

***Single Transistor Array Design***

[0084] The cross point array is not the only type of memory array that can be used with a two-terminal memory element. FIG. 35 is a schematic representation of memory cells laid out in a two-dimensional transistor memory array 3500. Each memory cell in the transistor memory array 3500 is connected to one select line 3505, 3510, or 3515, one data line 3520, 3525, 3530, or 3535, and a reference line 3540 or 3545. In one embodiment, all reference lines 3540 and 3545 are held to the same voltage, and perhaps even tied together. Therefore, a single select line 3510 and a single data line 3525 uniquely define an individual memory cell 3550.

[0085] By connecting the select lines 3505, 3510, and 3515 to the gates of field effect transistors (FETs), the select lines 3505, 3510, and 3515 can control whether current from the data lines 3520, 3525, 3530, and 3535 are able to pass to the memory plugs. Although the transistor memory array 3500 depicts n-channel FETs controlling access to the memory plugs (e.g., 3555), many other semiconductor devices can be used. Such device can include p-channel FETs, pnp transistors, npn transistors, diodes, and many other devices, such as parasitic vertical bipolar transistors that consists of a p junction and an N well in a p substrate.

[0086] Additionally, the semiconductor device can either be placed in between the memory plug 3555 and the reference line 3540 or in between the memory plug 3555 and the data line 3525. In both configurations the semiconductor device is able to prevent the memory plug from experiencing a voltage drop between the data line 3525 and the reference line 3540 when the semiconductor device is turned off. However, in the former case the memory plug would still experience voltage changes associated with the changing data line 3525, but no voltage drop. In contrast, memory plug in the configuration of FIG. 35 is insulated from the voltage of the data line 3525 for as long as the semiconductor device is not activated.

[0087] The data lines 3520, 3525, 3530, and 3535 both carry the data from the memory cells during read operations and provides the memory cells with a voltage



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pulse appropriate to change the resistive state of the memory plug during write operations. Selection circuitry used to select a specific data line 3520, 3525, 3530, or 3535 would generally be placed outside the select transistor memory array 3500.

**[0088]** Table 3 shows the operational voltages that could be applied to the array in one possible embodiment of the invention.

| | Selected Data Line | Unselected Data Line | Selected Select Line | Unselected Select Line | Reference Line |
|---|---|---|---|---|---|
| READ | 1V | Floating or 0V | 3V | -2V | 0V |
| WRITE 1 | -2V | Floating or 0V | 3V | -2V | 0V |
| WRITE 0 | 2V | Floating or 0V | 3V | -2V | 0V |

**TABLE 3**

**[0089]** In the embodiment of table 3, the reference lines 3540 and 3545 stay grounded. Activating more than one cell at a time may lead to voltage drops due to parasitic resistances. One technique that can be used to avoid this problem is to tie all the reference lines (e.g., 3540 and 3545) together at regular intervals. For example, including a line parallel to the data lines every 64 cells might ameliorate any unwanted voltage drops. Regardless of the technique used, it would generally be desirable to keep the reference line at a constant voltage.

**[0090]** During the read operation, the selected memory cell experiences a voltage drop of $V_R$'. It should be noted that current also flows through the unselected memory plugs along the selected select line 3510. An unselected memory cell along the selected select line 3510 would have its n-channel FET active, allowing current to flow. However, since the decoding circuitry only reads information off of the selected data line 3525, the current that flows through the unselected data lines 3520, 3530, and 3535 is not relevant to determining the stored value in the selected memory cell 3550. The voltage of the floating unselected data lines 3520, 3530, and 3535 must not, however, exceed either the positive voltage threshold ($V_{Wth}$) or negative voltage thresholds ($-V_{Wth}$) that can alter the resistive states in the unselected memory cells. Alternatively, the unselected data lines 3520, 3530, and 3535 might be held to some voltage in between $V_{Wth}$ and $-V_{Wth}$ (such as the reference voltage) if parasitic capacitance or some other correction mechanism was not thought to be sufficient to prevent the voltage from floating too high or too low.



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**[0091]** Current does not flow through the other unselected memory plugs because their n-channel FETs do not have a gate voltage greater than the required threshold gate voltages. An unselected memory cell along the selected data line 3525 would have a gate voltage of -2V, which is lower than both the voltage of the selected data line 3525, which is 1V, and the reference voltage, which is 0V. Of course, any value of 0V or less could be used for the unselected select lines 3505 and 3515 during the read operation. As will be appreciated, the -2V value is used to allow for rapid transitions from a read to a WRITE 1 operation. Similarly, an unselected memory plug 3565 along an unselected data line 3535 and an unselected select line 3515 would have a gate voltage of -2V, which is lower than both the unselected data line, which cannot float to less than -2V, and the reference voltage, which is 0V.

**[0092]** The WRITE 1 operation puts the memory cell into the $R_1$ state. Similarly, the WRITE 0 operation puts the memory cell into the $R_0$ state. The unselected memory cells are not affected by the write operations because either their gates are not activated or the unselected data lines only float between voltages of $V_{Wth}$ and $-V_{Wth}$.

**[0093]** To generate internal write voltages, two on chip voltage converters can convert the chip power supply, typically 3V or 1.8V, to the required value. One voltage converter, for example, could produce a 2V signal, and the other might produce a -2V signal.

**[0094]** FIG. 36 is a diagrammatic cross sectional representation of the memory cell 3550 that can be used in a transistor memory array 3500. Each memory cell 3550 includes a transistor 3605 and a memory plug 3610. The transistor 3605 is used to permit current from the data line 3525 to access the memory plug 3610 when an appropriate voltage is applied to the select line 3510, which is also the transistor's gate. The reference line 3540 might span two cells if the adjacent cells are laid out as the mirror images of each other.

**[0095]** Depending upon the fabrication process (e.g., solution based spin on followed by high temperature anneal, pulsed laser deposition, sputtering, and metalorganic chemical vapor deposition) the fabrication temperature might require that substances such as polysilicon, silicide, and/or refractory metals be used for the layers that are formed below the memory plug 3610, such as the select lines 3505, 3510, and 3515 and some vias 3620 and 3625. Polysilicon and silicide have resistances of 3 to 30Ω/□ where copper metal lines typically have resistances of less



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than 0.1Ω/□. Therefore, certain embodiments employing polysilicon or silicide may have the chip be much longer in the data line-direction than the select line-direction

**[0096]** As long as no high temperature processes are required after the memory plug 3610 is deposited, a more standard conductive metal (e.g., copper or tungsten for the vias) can be used for the layers that come after, such as the reference line 3540, metal plugs 3635 and 3640, vias 3615, 3630, 3645, and 3650, and the data line 3525. The metal plugs 3635 and 3640 are one technique that can be used to connect the vias 3615, 3630, 3645, and 3650 after the memory plugs 3610 and 3655 have been deposited.

**[0097]** It should be appreciated that the memory plug 3610 and 3655 geometries that are depicted are merely one embodiment, and will not be the same for every transistor memory array 3500. For example, in certain processes, the memory plug 3610 and 3655 may be the same dimensions as the underlying vias 3620 and 3625. In yet other processes, the underlying vias 3620 and 3625 may be unnecessary, as the memory plugs 3610 and 3655 may be deposited directly on the transistor's drain.

***Memory Chip Configuration***

**[0098]** FIG. 37A is a block diagram of a representative implementation of an exemplary 1 MB memory 3700. Physical layouts might differ, but each memory bit block 3705 is typically formed on a separate portion of a semiconductor substrate. It should be appreciated that a memory chip is not the only type of chip that could use a memory array, and many other types of chips would benefit from memory formed on the same substrate. For example, a microprocessor that has access to fast non-volatile L1 cache would be beneficial for many portable applications.

**[0099]** Referring back to FIG. 37A, inputs signals into the memory 3700 can include an address bus 3730, a control bus 3740, some power supplies 3750, and a data bus 3760. The control bus 3740 typically includes signals to select the chip, to signal whether a read or write operation should be performed, and to enable the output buffers when the chip is in read mode. The address bus 3730 specifies which location in the memory array is accessed -- some addresses going to the X block 3770 (typically including a predecoder and an X-decoder) to select one line out of the horizontal array lines. The other addresses go to a Y block 3780 (typically including a predecoder and a Y-decoder) to apply the appropriate voltage on specific vertical lines. Each memory bit block 3705 operates on one line of the memory chip data bus 3760.



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**[00100]** The reading of data from a memory array 3720 is relatively straightforward: an x-line is energized, and current is sensed by the sensing circuits 3710 and converted to bits of information. FIG. 37B is a block diagram of an exemplary memory that includes sensing circuits 3715 that are capable of reading multiple bits. The simultaneous reading of multiple bits involves sensing current from multiple y-lines simultaneously.

**[00101]** During a write operation, the data is applied from the data bus 3760 to the input buffers and data drivers 3790 to the selected vertical lines, or bit lines. Specifically, when binary information is sent to the memory chip 3700, it is stored in latch circuits within the circuits 3790. Each y-line can either have an associated driver circuit 3790 or a group of y-lines can share a single driver circuit 3790 if the non-selected lines in the group are held to a constant voltage that would not cause the unselected memory plugs to experience any change in resistance. The driver circuit then writes the 1 or 0 to the appropriate memory plug during the appropriate cycle. For example, there may be 1024 y-lines in a cross point array, and the page register may include 8 latches, in which case the y-block would decode 1 out of 128 y-lines and connect this selected line to block 3790. As described below, certain memory plugs can have multiple stable distinct resistive states. With such multi-level resistance memory plugs, driver circuits could program, for example, states of 00, 01, 10 or 11 by varying write voltage magnitude or pulse length.

**[00102]** It is to be noted that such an architecture can be expanded to create a memory where one array handles all the bits of the data bus, as opposed to having multiple arrays, or memory bit blocks as described above. For example, if the data bus, or memory data organization, also called data width, is 16-bit wide, the y-block of one cross point array can be made to decode 16 lines simultaneously. By applying the techniques of simultaneous reads and 2-cycle writes, such a memory chip with only one array can read and program 16-bit words.

***Page Mode and Burst Mode***

**[00103]** There are two common techniques used to output or input data in the page, often termed "page mode" and "burst mode." In both cases these modes take advantage of the internal architecture of memory. Words that are consecutive in address can be accessed faster with such modes, as the X/Y selection is only performed once, and the data for a number of words, which constitute a "page," is read or written at once, as opposed to being read or written one word at a time. This



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number of consecutive words read together and commonly referred as a "page" or an "information set."

**[00104]** In page mode, the lower significant bits of the address can be utilized to determine the order in which individual bits are to be read or written. The words selected by these address bit combinations can thus be in any order, and some words may not be read or written.

**[00105]** In burst mode the internal read or write operation is similar to page mode, but an external clock is used to sequentially input or output the words in the page. A post-sensing decoding block can be configured to simply sequentially output its information upon receipt of a trigger signal from an external burst clock. In this manner, information is either read from the decoding block or written to the cross point array automatically upon receiving the trigger signal. The advantage of burst mode over page mode is that no address decoding is needed to input or output the subsequent words in the page; this technique thus allows for a faster access time. The disadvantage of burst mode over page mode is that the page words can only be accessed in a set order.

**[00106]** Page or burst read can be accomplished by selecting multiple y-lines, connecting them to sensing circuits, and connecting the sensing circuit outputs to a post-sensing decoding block to select the appropriate data to bring to the pins of the memory integrated circuit. The page or burst write can be accomplished by selecting multiple y-lines, connecting them to the same number of drivers and energizing the drivers in a two-cycle sequence that writes in parallel all bits of the same data polarity (e.g., all binary 1's during the first cycle, and all binary 0's during the second). A pre-driver decoding stage would ensure that the data coming from the memory integrated circuit data pins is loaded in the appropriate latches.

**[00107]** FIG. 38A illustrates an exemplary latch 3810, drivers 3830 and 3840 and sensing circuit 3850 that can be used to accomplish two-cycle write operations. The circuit includes a page latch 3810 for storing one bit of information, AND gates 3860 and 3870 that receive signals from the page latch 3810 and inputs 3880 and 3890, an inverter 3820, and two drivers 3830 and 3840. The page latch 3810 is configured to hold a signal (either high or low signal depending on whether a 1 or 0 is received). Similarly, the inputs 3880 and 3890 are configured to receive the signal sequence shown in FIG. 38B. As one skilled in the art will appreciate, the write 1 signal is only high during the portion of the cycle where a write command is received, and the write



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0 signal is only high during the portion of the cycle immediately following the write 1 cycle. It should be noted that the duty cycle of the write 0 and write 1 operations can either correspond to the system clock, some fraction or multiple thereof, or can be asynchronous.

**[00108]** On receipt of a high or low signal, the page latch 3810 then continues to emit a corresponding high or low signal for as long as is necessary to complete the two-cycle write. When it is desired to write this 1 or 0 to the appropriate memory plug, circuitry then transmits the signals of FIG. 38B to each AND gate 3860 and 3870. Specifically, a high signal is sent to the input 3880 of the AND gate 3860 attached to the 1 driver 3830 during a first cycle, followed by a high signal to the other input 3890 during a second cycle. One of skill can see that either the 1 driver 3830 or the 0 driver 3840 will then be triggered to apply a write voltage to the y-line, as shown in the table of FIG. 38C. In this manner, a bit is written to the page latch 3810, and either its 1 driver 3830 or 0 driver 3840 will apply +2V or -2V to the y-line so as to write this bit to an associated memory plug within two cycles. It can also be seen that electrically connecting each y-line of a word, or other group of memory plugs, to a group of driver circuits allows that entire word or group of data to be written in two cycles, i.e. one cycle to write the binary 1's, and one to write the binary 0's.

**[00109]** While these driver circuits allow for two-cycle write operations, it would also be desirable to conduct read and write operations in both page and burst modes, so as to further speed reads and writes. As discussed above, read operations in page mode can be accomplished by reading multiple words (or other groupings of data) from the memory cells to the sensing circuits 3850, which then output the appropriate words, possibly buffering the data so that it could be output when desired, based on receipt of an address bit or bits identifying a particular word.

**[00110]** When read operations are to be performed in burst mode, multiple words or other data are read into a buffer, and are output sequentially upon receipt of signals from a burst clock or other known device for generating a trigger signal at a particular time. Typically, the burst clock signal triggers the circuit block to output words or other data groupings in an orderly fashion, such as one at a time from left to right y-lines.

**[00111]** Write operations are performed in page mode or burst mode according to specific signals sent to the inputs 3880 and 3890. Each bit block would



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simultaneously perform either the write 1 cycle or the write 0 cycle, according to the state of the signals described in FIG. 38B. In this manner, multiple driver circuits write their information to a memory array simultaneously, in either page mode or burst mode. It is to be noted that write 1 cycle signal 3880 and write 0 cycle signal 3890 will also control the X-block 3770 (shown in FIG. 37) in order to switch the selected x-line polarity, for example from -2V in the first cycle to +2V in the second cycle.

**[00112]** FIG. 39A further exemplifies the behavior of the memory chip during a page or burst read. The write enable signal is set low, which sets the chip for a read operation. An address is asserted on the address bus and all bits within the page at the given address are internally read. The first data is output after a delay which corresponds to the first access time. The way the data is output is different in burst mode and in page mode.

**[00113]** In burst mode, no page addresses are specified, but the sense amps 3710 send their data to a set of logic circuits within the page register, the logic circuits also being connected to the data bus 3760. An external burst clock signal 3910 is used to trigger the logic circuits to sequence the output of the page data bits to the data bus 3760.

**[00114]** In page mode page addresses 3920 that specify which bits are being output within the page are given. More specifically, known decoder circuits are employed within the page register to receive page address signals and decode these address signals into an order in which bits are to be output to the data bus 3760.

**[00115]** Although both burst clock and page addresses signals are shown on FIG. 39A, only one of these signals would be used for any one given mode. Many variations can be inferred by those skilled in the art as to whether the first address may be at the boundary of a page or not, or the exact shape and timing of the burst clock. In essence these variations do not alter the scope of page or burst mode operations within the memory chip.

**[00116]** FIG 39B further exemplifies the behavior of the memory chip during a page or burst write. In burst mode, information is sent over the data bus 3760 to the logic circuits. A burst clock signal toggles repeatedly to trigger the logic circuits to latch successive bits of data. Further burst clock pulses and optional write enable pulses are used to enter further data. When the last burst clock pulse has been entered, for example the 4th pulse if the internal page is 4 words long, the internal



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write operation, which as above can be a two-cycle write, is triggered. As above, in page mode, the page register contains address circuits and decoder circuits. These circuits ensure that the data to be programmed is transmitted from the bus 3760 and loaded into the page register at the page address being input to the memory chip, according to a succession of write enable pulses while page data and page address signals are input to the memory chip. When the page register is full, or according to any other signal (such as a control signal or combination of signals), the memory chip triggers the page register/buffer/driver 3795 and decoding circuits 3770 and 3780 to select the desired memory locations and send information to their associated driver circuit according to the signal sequence of FIG. 38B.

**[00117]** Although both burst clock and page address signals are shown in FIG. 39B, only one of these signals would be used for any one given mode. Many variations in the way data and addresses as well as how the actual write operation is triggered can be contemplated without departing from the scope of this invention.

***Adaptive programming***

**[00118]** A high-level conceptual diagram of an adaptive programming circuit of the present invention is depicted in FIG. 40. The adaptive programming circuit 4000 includes a coupled detector 4010, controller 4020 and driver 4030. The detector 4010, being coupled to a memory cell, functions to detect a cell resistance $R_d$ and output an indicating signal identifying an $R_j$ within the multi-level resistance set ($R_1$, $R_2$, . . . , $R_M$) that corresponds to $R_d$, where $M \geq 2$. Identifying an $R_j$ can be accomplished by determining $R_d$'s closest neighbor out of the multi-level resistance set ($R_1$, $R_2$, . . . , $R_M$).

**[00119]** The controller 4020, being coupled to the detector 4010, functions to detect a write command with write-data and the indicating signal and to generate an activating signal when a write is desired. The driver 4030, being coupled to the re-writable memory and the controller 4020, functions to drive, only while the activating signal is in the activated state, the memory to the desired resistance. The controller 4020 can further include activating logic functions as follows:

(a) an absence of the write command (or the presence of a read command) sets the activating signal to a deactivated state, thus insuring that the memory device is not driven by the driver 4030.

(b) a presence of the write command activates a comparison of the indicating signal with the write-data; and



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(b1) a non-correspondence between the indicating signal and the write-data sets the activating signal to an activated state while continuing function (b) thus causing the driver 4030 to drive the re-writable memory device to effect a desired switching of the memory cell resistance among the multi-level resistance set; or

(b2) a correspondence between the indicating signal and the write-data sets the activating signal to a deactivated state and terminates the programming cycle.

**[00120]** Notice that logic element (b2) above, in addition to completing the adaptive aspect of the adaptive programming circuit 4000, also functions to avoid a redundant programming cycle where the resistive state of the memory cell already corresponds to the write-data before the programming cycle. Repetitive redundant programming cycles can potentially cause a shortening of the memory device operating life.

**[00121]** To deal with re-writable memory devices that either are unreasonably hard to program or would require an unreasonably long programming cycle time or simply have failed in time, the controller 4020 can further include a pre-determined maximum allowable programming time $T_{max}$ and a timer tracking an elapsed time $T_{lp}$ of the programming cycle from the moment of presence of the write command. Correspondingly, the above activating logic can be first modified to include a Logic Fault Signal (LFS). For example, LFS = 1 can mean a fault condition and LFS = 0 can mean a no-fault condition. Specifically, the activating logic can add to function (b) a logic that sets LFS = 1 if $T_{lp} > T_{max}$. The activating logic can further include the following changes:

1. logic element (a) includes an additional, unconditional initialization of LFS to 0.
2. logic element (b1) is replaced with the following two logic elements:

   (b11) a non-correspondence between the indicating signal and the write-data, while LFS = 0, sets the activating signal to an activated state while continuing function (b) thus causing the driver 4030 to drive the re-writable memory device to effect a desired switching of the resistive state of the memory cell among the multi-level resistance set; or



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(b12) a non-correspondence between the indicating signal and the write-data, but LFS = 1, sets the activating signal to a deactivated state and terminates the programming cycle.

**[00122]** For simplicity of implementation in practice, to effect the function of detecting the memory cell's resistance and outputting an indicating signal identifying an $R_j$ within the multi-level resistance set ($R_1, R_2, \ldots, R_M$) that $R_d$ corresponds to, the detector 4010 includes an equivalent-signal $S_{eq}$ generator, whose value corresponds to $R_d$ through a pre-determined function $R_d = f(S_{eq})$.

**[00123]** The detector 4010 further selects an equivalent-reference signal set ($REF_1, REF_2, \ldots, REF_M$), depending upon the write data. A base reference signal will typically be an input to the adaptive programming circuit 4000, or derived from resistive circuitry within the adaptive programming circuit 4000. Additionally, the detector 4010 compares $S_{eq}$ with an appropriate reference signal from the equivalent-reference signal set ($REF_1, REF_2, \ldots, REF_M$).

**[00124]** For one example, the driver 4030 is switchable by the activating signal voltage source with an output voltage $V_{cs}$, the equivalent-signal $S_{eq}$ generator can be a current detector, coupled to the memory device, providing the memory device current $I_d$ as the equivalent-signal $S_{eq}$. That is $S_{eq} = I_d$. Consequently, the pre-determined function $R_d = f(S_{eq})$ can simply be $R_d = V_{cs}/I_d$ by Ohm's law. Where the output voltage $V_{cs}$ is a constant voltage, of course, its magnitude must exceed each respective threshold voltage to effect a desired switching of $R_d$ among the multi-level resistance set. As a higher $V_d$ generally results in a shorter device programming cycle time, for those re-writable memory devices having high threshold voltages, the $V_{cs}$ can be set as a time-varying voltage ramp or voltage steps of increasing magnitude so as to exceed each respective threshold within a pre-determined time interval to shorten the programming cycle time. Of course, the initial value of the time-varying voltage ramp can be set at or above a corresponding threshold voltage of the re-writable memory device to further shorten the programming cycle time.

**[00125]** For another example, the driver 4030 is, by the activating signal, a switchable current source with an output current $I_{cs}$ the equivalent-signal $S_{eq}$ generator can be a voltage detector, coupled to the writable memory device, providing the memory device voltage $V_d$ as the equivalent-signal $S_{eq}$. That is $S_{eq} = V_d$. Consequently, the pre-determined function $R_d = f(S_{eq})$ can be $R_d = V_d/I_{cs}$, also by Ohm's law. Where the output current $I_{cs}$ is a constant current, of course, its



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magnitude must cause the corresponding $V_d$ to exceed each respective threshold voltage to effect a desired switching of $R_d$ among the multi-level resistance set. As a higher $V_d$ generally results in a shorter device programming cycle time, for those memory devices having high threshold voltages, the $I_{cs}$ can be set as a time-varying current ramp or steps of increasing magnitude so as to cause the corresponding $V_d$ to exceed each respective threshold within a pre-determined time interval to shorten the programming cycle time. Of course, the initial value of the time-varying current ramp can be set to cause the corresponding $V_d$ to be at or above a corresponding threshold voltage of the re-writable memory device to further shorten the programming cycle time.

**[00126]** By now it should become clear that, in addition to being an adaptive programming circuit, the adaptive programming circuit 4000 is equally applicable to a method of programming the re-writable memory device with a sequence of steps logically corresponding to the above attributes of the adaptive programming circuit. It should also be clear that, except for insuring that $V_d$ stays below each respective threshold to avoid the switching of $R_d$, essentially the same adaptive programming circuit can be adapted to effect a read operation outputting an indicating signal identifying an $R_j$ that $R_d$ corresponds to upon detection of a read-command. Additional, even more detailed embodiments of the detector 4010, the controller 4020 and the driver 4030 will be presently illustrated graphically.

**[00127]** FIG 41A depicts a first more detailed embodiment of an exemplary adaptive programming circuit 4100. In this case the multi-level resistance set $R_j$ consists of only two distinct resistance levels $R_1 < R_2$, that is $M = 2$. As part of the detector 4010, the equivalent-reference signal set selector includes a reference driver 4105 working in conjunction with a reference data source 4110 to provide an equivalent-reference signal $REF_1$ at node B of a comparator 4115. The driver 4030 includes a program supply 4120 and a data driver 4125. The program supply 4120 outputs write-data. The data driver 4125 is a voltage source with an output voltage $V_{cs}$ for effecting an actual programming of the memory device according to the write-data. The equivalent-signal $S_{eq}$ generator is a current detector 4130, coupled to the memory device, providing the equivalent-signal $S_{eq} = I_d$ at node A. Consequently, the pre-determined function $R_d = f(S_{eq})$ is $R_d = V_{cs}/I_d$. Hence, this particular embodiment essentially employs a current comparison technique and the output of the comparator 4115 is logically the indicating signal identifying an $R_j$ within the multi-level



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resistance set ($R_1$, $R_2$) that $R_d$ corresponds to. The controller 4020, in this case a single feedback signal path, functions to either activate or deactivate the data driver 4125 depending upon the correspondence between the indicating signal and the write-data.

**[00128]** The current comparison technique is further illustrated with a numerical example. Here the selected re-writable memory device to be programmed is in the low resistive state with $R_d$ corresponds to $R_1$. When a write voltage $V_W$ is initially applied to the cell $I_d = 40$ μA before any resistance switching takes place. The comparator 4115 includes a reference current set at 20 μA, a similar load circuit for the reference current and the selected memory device and a voltage comparator. The load circuits are basically resistor networks connected to the voltage source $V_{cs}$. As the reference current is 20 μA and the selected memory device current is 40 μA, the voltage on node A will be lower than that on node B causing the output of the voltage comparator to be high. Instead the comparator could be connected with a different polarity of input so that its output would be low, but this would not change the nature of this invention. In time, as the write voltage $V_W$ starts to switch the resistance of the selected memory device, its current $I_d$ decreases from 40 μA until it reaches the reference current of 20 μA. At this point node A voltage equals node B voltage. As the programming of the selected memory device progresses further, node A voltage becomes higher than node B voltage that causes the voltage comparator to trip into a state of low output voltage. Hence, the voltage comparator output can be used to deactivate the data driver 4125, thus turning off the write voltage $V_W$ applied to the selected memory device.

**[00129]** On the other hand, if the selected memory device to be programmed is already in the high resistive state with $R_d$ corresponds to $R_2$ thus, for example, $I_d = 15$ μA at start of the programming operation, the comparator output will stay low and the data driver will stay deactivated.

**[00130]** Notice that the above circuit needs to be properly initialized. If, at the beginning of the write cycle, the node A voltage starts at a value higher than the node B voltage, the output of the voltage comparator is low thus the data driver 4125 stays disabled. The consequence is that the program operation would never start. To avoid this problem a discharge circuit and an initialization pulse can be used to force node A voltage low at the beginning of each program operation.



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**[00131]** It is further remarked that, while only one reference current is needed in the above example for minimum functionality, this would not provide a more precise resolution of the actual resistance values $R_1$ and $R_2$. Thus, if so desired, additional reference current levels can be included in the adaptive programming circuitry to further improve the detection margin of the various resistance levels.

**[00132]** As already remarked before, the programming voltage pulse does not have to be a square pulse of constant amplitude. A further improvement would be to use a ramp on the programming voltage, starting at a low initial voltage value and increasing with time. The initial voltage can start somewhere at or above the read voltage and can go as high as the circuitry allows. For a cross point array, that means the voltage should not disturb unselected memory devices on the selected array lines. This technique, combined with the comparison technique, would insure that memory devices with a fast programming cycle time get programmed quickly at a relatively low voltage. On the other hand, memory devices with a slow programming cycle time can be programmed faster than if a constant voltage was applied as a write voltage. Furthermore, if a memory device has a very high write threshold voltage it may never program under a normal constant voltage drive. Here, by increasing the write voltage it may become possible to program this memory device. However, it may not be desirable to program all the memory devices of the array with the increased write voltage as this could prematurely wear out or even damage those memory devices easily programmable at lower voltage levels.

**[00133]** Figure 41B depicts a second more detailed embodiment of an exemplary adaptive programming circuit 4150. The multi-level resistance set $R_j$ still consists of only two distinct resistance levels $R_1 < R_2$, that is $M = 2$. As part of the detector 4150, the equivalent-reference signal set selector includes a reference data source 4110 providing an equivalent-reference signal $REF_1$ at node B of a comparator 4115. The driver 4030 includes the program supply 4120 and a data driver with voltage detector 4155 outputting a detected re-writable memory device voltage $V_d$ at node A. The program supply 4120 outputs write-data. The data driver with voltage detector 4155 includes a current source with an output current $I_{cs}$ for effecting an actual programming of the re-writable memory device according to the write-data. Thus, the equivalent-signal $S_{eq}$ generator is the above voltage detector, coupled to the re-writable memory device, providing the equivalent-signal $S_{eq} = V_d$, at node A. Hence, this particular embodiment essentially employs a voltage comparison technique and



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the output of the comparator 4115 is logically the indicating signal identifying an $R_j$ within the multi-level resistance set ($R_1$, $R_2$) that $R_d$ corresponds to. The controller 4020, in this case a single feedback signal path, functions to either activate or deactivate the data driver with voltage detector 4155 depending upon the correspondence between the indicating signal and the write-data.

**[00134]** FIG. 42 depicts a third circuit schematic level embodiment of an exemplary adaptive programming circuit 4200 with a bipolar voltage driver, a current comparison circuit and activating logic. This circuit schematic uses two references so that the programmed resistance states $R_1$ and $R_2$ are separated by a pre-determined margin. Correspondingly, the adaptive programming circuit 4200 includes upper half circuitry to provide the required positive voltage driver and lower half circuitry, being essentially a mirror image of the upper half circuitry, to provide the required negative voltage driver. For convenience, the upper half circuitry is also called positive drive circuitry and the lower half circuitry is also called negative drive circuitry. While both the positive drive circuitry and the negative drive circuitry are logically driven by a write command pulse 4205, the positive drive circuitry is only activated with a write-data $R_2$ signal 4210 whereas the negative drive circuitry is only activated with a write-data $R_1$ signal 4215. In this way, during a programming operation with a positive voltage drive the negative drive circuitry is deactivated in a state of high impedance to avoid any interference with the positive drive circuitry, and vice versa.

**[00135]** Focusing on the details of the positive drive circuitry, the controller 4020 includes an activating logic 4225 in turn driving both a device pre-driver 4220 and, through an $R_2$ reference pre-driver 4235, an $R_2$ reference driver 4240. The device pre-driver 4220 drives a $+V_{Wth}$ device driver 4230 whose output drives a selected re-writable memory device within the re-writable memory array. In parallel, the $+V_{Wth}$ device driver 4230 output, through a signal branch at node A, also feeds a negative terminal of a comparator 4260. The $R_2$ reference driver 4240 output, in combination with an $R_2$ reference resistance 4250, establishes an equivalent-reference signal $REF_1$ at node B that feeds a positive terminal of the comparator 4260. Except for working in a domain of negative voltage with a - $V_{Wth}$ device driver 4280, by now it should become clear that the negative drive circuitry has a similar circuit topology and functions, in a way similar to the positive drive circuitry above, to accomplish the desired function of adaptive programming. It is also instructional to note that, while FIG. 42 depicts an embodiment with a bipolar voltage drive, there is nevertheless a



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typically small drain-to-source voltage drop across the + $V_{Wth}$ device driver 4230 and the - $V_{Wth}$ device driver 4280. Furthermore, the drain-to-source voltage drop itself is dependent upon the memory device current $I_d$. Thus, the driving circuit can also be characterized as a hybrid combination of voltage and current source.

**[00136]** Lastly, for those skilled in the art, the circuit topology of FIG. 42 is used for detecting $R_d$ between two levels separated by two reference levels in between to affect a higher detection resolution of $R_d$ with a correspondingly higher margin of correct logic decision.

**[00137]** FIG. 43 depicts an exemplary timing diagram of signals and memory device currents during an application of the present invention in a re-writable memory array. In this example, a first device A within the re-writable memory array is programmed with a low resistance state, a second device B is programmed with a low resistance state and a third device C is programmed with a high resistance state. Notice the self-adapting nature of the activating signal having a variable pulse width each corresponds to an individual memory device being programmed. That is, device A exhibits a typical programming cycle time of $t_{A2}$-$t_{A1}$, cell B exhibits a fast programming cycle time of $t_{B2}$-$t_{B1}$ while cell C exhibits a slow programming cycle time of $t_{C2}$-$t_{C1}$.

**[00138]** FIG. 44 illustrates another embodiment of the adaptive programming circuit extended to a general case where the re-writable memory device exhibits a multi-level voltage switchable resistance set of more than two resistance levels. To avoid unnecessary obscuring aspects of the present invention only section-j of adaptive programming circuit 4400 is illustrated here where j = (1,2, . . ,M-1), M >= 3 and R1 < R2 < . . < RM. Furthermore, it should be understood that all similar sections are set in parallel, with a common connection at node A. First of all, the entire section-j of adaptive programming circuit 4400 is selected by a section-j selection signal 4405, where j would be the distinct state that is desired. If the j-state is higher than the initial state of the memory plug, section-j selection signal 4405, for $R_j$ programming, activates a reference $R_{jlow}$ generator 4410 to establish an equivalent-reference signal $REF_{jlow}$ at node B1 that feeds a first input terminal of a comparator 4415. The output of the comparator 4415, while in an activated state, in turn activates a low $R_d$ device driver 4420 through a feedback signal path 4425 to drive a selected memory device within the re-writable memory array causing a switching of $R_d$ into the $R_j$-state. In parallel, the low $R_d$ device driver 4420 output, through a signal branch



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at node A, also feeds a second input terminal of the comparator 4415 to complete the adaptive programming logic for resistance $R_j$. Similarly, if the j-state is lower than the initial resistance state of the memory plug, the section-j selection signal 4405, for $R_{jhigh}$ programming, activates a reference $R_j$+1 generator 4430 to establish an equivalent-reference signal $REF_{jhigh}$ at node B2 that feeds a first input terminal of a comparator 4435. The output of the comparator, while in an activated state, in turn activates a high $R_d$ device driver 4440 through a feedback signal path 4445 to drive a selected memory device within the re-writable memory array, causing a switching of $R_d$ into the $R_j$+1-state. In parallel, the high $R_d$ device driver 4440 output, through the signal branch at node A, also feeds a second input terminal of the comparator 4435 to complete the adaptive programming logic for resistance $R_j$. At the beginning of the write, if the selected cell resistance is above $R_{jhigh}$ the low $R_d$ driver 4420 will turn on. If the selected cell resistance is below $R_{jlow}$ the high $R_d$ driver 4440 will turn on. At the end of the write operation the selected cell's resistance will be between $R_{jlow}$ and $R_{jhigh}$.

**[00139]** As an alternative embodiment, FIG. 45 depicts a block diagram of yet another implementation of an exemplary adaptive programming circuit 4500. The state-j selection signal 4505, which tells the circuit which is the desired state out of M states, and includes typically k lines, so that M = 2k, can be applied to the two reference generators 4510 and 4530, and possibly also to the device drivers 4520 and 4540, to adjust these reference generators and device drivers so that their outputs equal to a respectively desired level appropriate for the state-j programming. Unlike the embodiment of FIG. 44, this approach requires only two comparators 4515 and 4535, two adjustable references 4510 and 4530 and two adjustable drivers 4520 and 4540. This is an advantage where no replication of the section-j circuit would be necessary to implement the programming of the multi-level resistance set ($R_1$, $R_2$, . . . $R_M$).

***Memory Plug***

**[00140]** Each memory plug contains layers of materials that may be desirable for fabrication or functionality. For example, one desirable function might be a non-ohmic characteristic. A non-ohmic characteristic might exhibit a very high resistance regime for a certain range of voltages ($V_{NO-}$ to $V_{NO+}$) and a very low resistance regime for voltages above and below that range. In a cross point array, a non-ohmic characteristic could prevent leakage during reads and writes if half of both voltages



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were within the range of voltages $V_{NO-}$ to $V_{NO+}$. If each conductive array line carried 1/2 $V_W$, the current path would be the memory plug at the intersection of the two conductive array lines that each carried 1/2 $V_W$. The other memory plugs would exhibit such high resistances from the non-ohmic characteristic that current would not flow through the half-selected plugs.

**[00141]** A non-ohmic device might be used to cause the memory plug to exhibit a non-linear resistive characteristic. Exemplary non-ohmic devices include three-film metal-insulator-metal (MIM) structures and back-to-back diodes in series. Separate non-ohmic devices, however, may not be necessary. Certain fabrications of the memory plug can cause a non-ohmic characteristic to be imparted to the memory cell. While a non-ohmic characteristic might be desirable in certain arrays, it may not be required in other arrays.

**[00142]** Electrodes will typically be desirable components of the memory plugs, a pair of electrodes sandwiching the memory element. If the only purpose of the electrodes is as a barrier to prevent metal inter-diffusion, then a thin layer of non-reactive metal, e.g. TiN, TaN, Pt, Au, and certain metal oxides could be used. However, electrodes may provide advantages beyond simply acting as a metal inter-diffusion barrier. Electrodes (formed either with a single layer or multiple layers) can perform various functions, including: prevent the diffusion of metals, oxygen, hydrogen and water; act as a seed layer in order to form a good lattice match with other layers; provide adhesion layers; reduce stress caused by uneven coefficients of thermal expansion; and provide other benefits.

**[00143]** For example, a conducting oxide electrode might modify the formation and migration of oxygen vacancies. Oxygen vacancies in certain embodiments can cause degradation of electrical properties in the memory plug. A conducting oxide electrode can also withstand high temperature processing. Most non-refractory metals either start oxidizing or combining with adjacent materials at temperatures above 400C. Accordingly, fabrication processes above these temperatures can be considered to be high temperature processing. Additionally, conducting oxide electrodes will not degrade during operation. Regular metal electrodes may degrade due to the electric field assisted metal migration and interaction between the metal atoms and the memory material atoms.

**[00144]** Examples of conductive oxides include $LaSrCoO_3$, $RuO_2$, $IrO_2$, $SrRuO_3$, $LaNiO_3$ and doped strontium titanate (STO). The dopant used in STO can be either



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Nb or Ta to substitute for titanium atoms, or any rare earth such as La or Pr to substitute for strontium atoms. Generally, a conducting oxide electrode is metallic with resistivity below 1 Ω-cm.

**[00145]** Conducting oxide electrodes can be fabricated directly, or can be made with a material that is not initially an oxide, but is subsequently oxidized during further processing or operation. Ru and Ir are both examples of materials that can be oxidized during processing or operation.

**[00146]** Additionally, certain materials oxidize at a finite rate and allow dual layers to form. For example, Ir might be particularly well suited for making contact to an underlying conductive array line layer. When Ir is oxidized, the top of the Ir layer becomes $IrO_2$. Since the $IrO_2$ grows at a finite rate it becomes possible to control the oxidation so that a dual layer of $Ir/IrO_2$ is formed. Such a dual layer could provide a good contact on the un-oxidized bottom while still forming an oxygen barrier on the oxidized top.

**[00147]** Furthermore, some conductive oxides electrodes form a good lattice match with other layers, and thus lower crystallization temperature for those layers. For example, if an oxide such as STO is to be deposited on top of a conductive electrode, possible conductive oxide electrodes that make a good lattice match include doped STO, $LaSrCoO_3$, and $SrRuO_3$. If the oxide is PCMO, possible conductive oxide electrodes include the STO electrodes and also $LaNiO_3$. A seed layer will often be used on top of a thin layer of metal. A seed layer will help the formation of the layer grown or deposited above it. For example, the seed layer could be on Pt, Ru, Ir or TiN. Some seed layer/metal layer matches include $LaNiO_3$ or $SrRuO_3$ on Pt, $IrO_2$ on Ir, $RuO_2$ on Ru, and Pt on TiN.

**[00148]** Another benefit to certain conductive oxide electrodes is that stress may be reduced by more closely matching the conductive oxide electrode's coefficient of thermal expansion to the oxide. The electrodes might be further improved by using a layer of metal such as thin platinum, less than 100 Å, between the oxide and the conductive oxide electrode. Such implementations advantageously provide a good Schottky barrier with the conductive oxide to minimize cell leakage current, and a good contact with an adjacent metal layer. The Schottky barrier can provide a desired non-linearity of a non-ohmic device.



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**[00149]** Barrier layers are generally helpful to prevent inter-diffusion of atoms after different materials have been deposited. For example, barrier layers can block the diffusion of metals, oxygen, hydrogen or water. Binary oxides or nitrides with 2 elements and ternary oxides or nitrides with 3 elements are particularly suited to high temperature processing. Unlike a regular electrode like titanium that oxidizes and becomes non-conductive, titanium nitride will remain conductive and will not oxidize until about 500C. Ternary nitrides oxidize at even higher temperatures, typically about 50C higher than binary nitrides. The rate of oxidation depends on the temperature and the oxygen partial pressure.

**[00150]** Examples of binary nitrides include titanium nitride, tantalum nitride and tungsten nitride. Examples of ternary nitrides include titanium silicon nitride, tantalum aluminum nitride, tantalum silicon nitride, and ruthenium titanium nitride. An example of a ternary oxide is ruthenium tantalum oxide.

**[00151]** As will be appreciated by those skilled in the art, an electrode may require other layers, in order to properly function. For example adhesion layers are sometimes necessary. An adhesion layer is used between a substrate and thin-film layer to improve adhesion of the thin-film layer to substrate. Pt does not stick well to $SiO_2$, so a glue layer, such as Ti or $TiO_2$, is used between them for better adhesion. Similarly, a sacrificial barrier layer is an oxide layer that is deposited for the sole purpose of capturing all the oxygen that could otherwise diffuse into other layers, such as the oxide. The electrode is considered to include any adhesion or sacrificial barrier layers, as required.

**[00152]** For example, an electrode may include a TiN or TiAlN layer, an Ir layer and an $IrO_2$ layer to have good metal barrier and oxygen barrier properties. However, such additional layers are only necessary to the extent they are required. Certain conductive oxide electrodes may provide multiple functions. For example, ternary nitrides and ternary oxides that have one component that is either ruthenium or iridium and another component that is either tantalum or titanium can act as both a barrier layer and a sacrificial high-temperature oxygen barrier.

**[00153]** Additionally, the choice of electrode layers can affect the memory effect properties of the memory plug and become part of the memory element.

***Memory Effect***

**[00154]** The memory effect is a hysteresis that exhibits a resistive state change upon application of a voltage while allowing non-destructive reads. A non-



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destructive read means that the read operation has no effect on the resistive state of the memory element. Measuring the resistance of a memory cell is generally accomplished by detecting either current after the memory cell is held to a known voltage, or voltage after a known current flows through the memory cell. Therefore, a memory cell that is placed in a high resistive state $R_0$ upon application of $-V_W$ and a low resistive state $R_1$ upon application of $+V_W$ should be unaffected by a read operation performed at $-V_R$ or $+V_R$. In such materials a write operation is not necessary after a read operation. It should be appreciated that the magnitude of $|-V_R|$ does not necessarily equal the magnitude of $|+V_R|$. In certain cases the details of the voltage pulse can actually affect the resistance of a memory plug. For example, the paper "New Conduction and Reversible Memory Phenomena in Thin Insulating Films" by J.G. Simmons and R.R. Verderber, 301 *Proc. Roy. Soc. A.* 77-102 (1967), describes a memory effect on certain MIM structures that are controlled by details of the voltage pulse duration and height. In such a system, bringing an MIM structure to a certain voltage, and then quickly dropping the voltage to zero would achieve a different resistance state than bringing the MIM structure to the same voltage and then slowly decreasing the voltage to zero. In such a system voltage pulses of opposite polarity are not needed.

**[00155]** The $R_1$ state of the memory plug may have a best value of 10kΩ to 100kΩ. If the $R_1$ state resistance is much less than 10kΩ, the current consumption will be increased because the cell current is high, and the parasitic resistances will have a larger effect. If the $R_1$ state value is much above 100kΩ, the RC delays will increase access time. However, workable single state resistive values may also be achieved with resistances as low as 5kΩ and as high as 1MΩ. Typically, a single state memory would have the operational voltages of $R_0$ and $R_1$ separated by a factor of 10.

**[00156]** For example, if 1 volt were used as a read voltage ($V_R$), $R_1$ might be about 100kΩ and $R_0$ might be about 1MΩ, making the current either 10μA or 1μA, depending on the resistive state. Since large currents can be destructive to semiconductors fabricated to small dimensions, no more than 100μA would be desired for a memory circuit in most cases. Once a $V_R$ is identified, a desired write voltage ($V_W$) can also be determined. Not only should $V_W$ be greater than $V_R$, but it should also be far enough away from $V_R$ to allow minor voltage fluctuations (e.g., due to fabrication imperfections) to have a negligible effect on the memory plug.



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Similarly, $V_W$ should be greater than $V_{Wth}$, the threshold at which the resistive material starts to change resistivity, for the same reason. A typical $V_W$ might be about 2 volts, and $V_{Wth}$ might be about 1.5 volts.

**[00157]** It should be noted that changes in the resistive property of the memory plugs that are greater than a factor of 10 might be desirable in multi-bit resistive memory cells. Since memory plugs can be placed into several different resistive states, multi-bit resistive memory cells are possible. For example, the memory plug might have a high resistive state of $R_{00}$, a medium-high resistive state of $R_{01}$, a medium-low resistive state of $R_{10}$ and a low resistive state of $R_{11}$. Since multi-bit memories typically have access times longer than single-bit memories, using a factor greater than a 10 times change in resistance from $R_{11}$ to $R_{00}$ is one way to make a multi-bit memory as fast as a single-bit memory. For example, a memory cell that is capable of storing two bits might have the low resistive state be separated from the high resistive state by a factor of 100. A memory cell that is capable of storing three or four bits of information might require the low resistive state be separated from the high resistive state by a factor of 1000. Typically, the intermediary resistive states in a multi-bit memory would evenly subdivide the resistive range between the high resistive state and the low resistive state on a logarithmic scale. For example, if a memory cell that held three bits of memory had a low resistive state of 10kΩ, the six intermediary states might have resistive states of about 26.8kΩ, 72.0kΩ, 193kΩ, 518kΩ, 1.39MΩ, and 3.73MΩ. The highest resistive state would then be 10MΩ, 1000 times the value of the low resistive state.

***Creating The Memory Effect***

**[00158]** Although the memory effect properties of the memory plug appear to be dominated by carrier trapping, other carrier transport mechanisms such as oxygen migration or electrolyte migration may be present. Even within carrier charge trapping, dominant factors can include space-charge limited currents, thermionic emission limited conduction, electrothermal Poole-Frenkel emission, or Fowler-Nordheim quantum tunneling. While the inventors note that experimental data is consistent with the memory effect being created primarily by carrier trapping, they do not wish to be bound by any explanation of how the memory effect is created or how any other effect that is described herein functions.



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**[00159]** Additionally, different mechanisms may be responsible for a memory effect depending upon whether the interface has been "formed." Forming, (or "electroforming") as it relates to a MIM structure, was described in "The Electroformed metal-insulator-metal structure: a comprehensive model," J. Phys. D: Appl. Phys. Vol. 35, pp. 802 - 809, 2 April 2002 by R. E. Thurstans and D. P. Oxley, and can be thought of as "the localized filamentary movement of metallic anode material through the dielectric, induced by the electric field. Here it is important to note that the evaporated dielectric may contain voids and departures from stoichiometry. When resulting filaments through the dielectric carry sufficient current, they rupture to leave a metal island structure embedded in the dielectric. Electronic conduction is possible through this structure by activating tunneling." However, the authors caution, "The forming process is complex and inherently variable. Also tunneling barriers are susceptible to changes in their characteristics when exposed to water vapour, organic species and oxygen. . . . Thus, device characteristics can never be expected to be produced consistently or be stable over long periods without passivation, effective encapsulation and a better understanding of the dynamics of the forming process."

**[00160]** Contrary to the warnings of Thurstans and Oxley, certain methodologies can be used to direct and control forming, and even obtain a memory effect without forming. For example, simply exposing a reactive metal layer to an oxide can create a memory effect without forming. It is believed that in those circumstances the memory effect is created through an interface between the oxide and the reactive metal layer.

**[00161]** A formed structure can also be approximated by depositing islands of one material within the bulk of a second, more insulating material. Islands (as opposed to a continuous thin film) can be formed by a number of different processes, including sputtering, co-sputtering, evaporation, molecular beam epitaxy, atomic layer deposition, implantation, etc, and are typically related to the surface energies of the two materials. Those skilled in the art will appreciate that a first material can form islands on the surface of a second material under some processes and not others.

**[00162]** In one specific embodiment, a portion of a non-organic semiconductive material is first deposited on an electrode. Then, conductive islands are formed on the semiconductive material. After the islands are formed, another portion of the same semiconductive material is deposited on the islands. Then, either a top electrode is



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formed or additional island/semiconductive material layers are formed prior to the top electrode.

**[00163]** As a more specific example, a damascene process could be employed where an interlayer dielectric such as $SiO_2$ is patterned on top of a bottom electrode in order to create voids over the bottom electrodes. Aluminum oxide can then be deposited and polished off the $SiO_2$ surface such that a portion of the void is filled with aluminum oxide. A small amount of conductive metal or oxide could then be formed on top of the aluminum oxide, which will preferentially nucleate into an array of island formations on the aluminum oxide. Another layer of aluminum oxide could then be sputtered fill more the void, followed by another polish and then another deposition of islands. A final layer of aluminum oxide could then be deposited to completely fill the void, followed by a final polish so that the $SiO_2$/aluminum oxide surface was smooth.

***Interfacial layer***

**[00164]** The interface layer is typically a very thin layer because the reaction that is created by placing the oxide in contact with the reactive metal only extends a short distance, typically less than 100 angstroms. The thickness of the interfacial layer can be controlled by limiting the thickness of the reactive metal. Although the interfacial layer can be placed into different resistive states, even the lowest resistive state is typically very insulating. Accordingly, a thick interfacial layer would not allow any current to pass through the memory cell in an optimal period of time. To allow rapid access times (on the order of tens of nanoseconds, typically below 100 ns) in small dimension devices (on the order of hundreds of nanometers), the entire memory plug should have a resistivity of not more than about 1 ohm-cm.

**[00165]** The oxide will generally (but not necessarily) be a conductive crystalline metal oxide -- either as a single crystalline structure or a polycrystalline structure. One class of conductive oxides are perovskites that include two or more metals, the metals being selected from the group consisting of transition metals, alkaline earth metals and rare earth metals. The perovskites (generally in the form of $ABX_3$ structures, where A has an atomic size of 1.0-1.4 Å and B has an atomic size of 0.45 – 0.75 Å for the case where X is either oxygen or fluorine) can be any number of compositions, including manganites (e.g., $Pr_{0.7}Ca_{0.3}MnO_3$, $Pr_{0.5}Ca_{0.5}MnO_3$ and other PCMOs, LCMOs using lanthanum and calcium as A, etc.), titanates (e.g., $SrTiO_3$ doped with Cr, also identified as STO:Cr), zirconates (e.g., $SrZrO_3$ doped with Cr,



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also identified as SZO:Cr), other materials such as $Ca_2Nb_2O_7$:Cr, and $Ta_2O_5$:Cr, and high Tc superconductors (e.g., yttrium barium copper oxide, also identified as YBCO). Specifically, $MnO_3$, when combined with the rare earth metals La, Pr or some combination thereof and the alkaline earth metals Ca, Sr or some combination thereof have been found to be effective for use in the memory plug.

**[00166]** Further, some oxides that may not be conductive in their pure form may be used as they become conductive through the addition of dopants, or if they are used as a very thin layer (e.g., in the order of tens of Angstroms) in which case tunneling conduction can be achieved. Therefore, as will be appreciated by those skilled in the art, oxides that are classified as insulators, but are thin enough to allow tunneling conduction, can still be considered conductive oxides. Since a memory plug will need to be able to be switched at low currents, low resistances are desirable – making conductive oxides more attractive than insulating oxides.

**[00167]** Whether a metal is a "reactive metal" is determined by its relation to the conductive metal oxide, and whether the metal is a strong enough reducing agent to reduce the conductive metal oxide and be oxidized, and whether the resulting oxidized reactive metal is insulating. For example, Al will reduce a PCMO perovskite in order to form an insulating interfacial layer having a memory effect. Other reactive metals, depending on the conductive metal oxide, can include Ta, Ti, Zr, Y, Hf, Cr and Mg.

**[00168]** In one embodiment, the interfacial layer can be considered to be between the unaltered conductive oxide and the unaltered reactive metal. If, however, only a small amount of reactive metal is deposited such that all of the reacted metal is oxidized, then the interfacial layer will be between the unaltered conductive oxide and an electrode on top of the interfacial layer.

**[00169]** However, it should be appreciated that using a reactive metal may not be the only way to create a memory effect with a conductive oxide. Insulating layers having the memory effect might be able to be created through doping, implantation or use of other techniques.

**[00170]** For example, strontium titanate (STO) or strontium zirconate (SZO) can be doped by adding an element that has a different preferred oxidation state (a different charge when ionized) when it replaces an element in the crystal matrix. Typically, the dopant would make up less than 10% molecular percentage of the total material. In SZO, chromium (Cr), with a +3 oxidation state, can replace zirconium (Zr) with a +4



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oxidation state. Charge imbalance is compensated by either creation of appropriate vacancies (e.g., oxygen vacancies), by change of valence on a matrix element, or by introduction of free carriers (electrons or holes).

**[00171]** A dopant atom usually substitutes for a matrix element based, at least partly, on the similarity of ionic radii. Thus lanthanum (La) primarily substitutes for strontium (Sr) whereas Cr primarily substitutes for Zr in SZO. In SZO, cation vacancies are rare (i.e., there are few Sr and Zr vacancies), but anion vacancies (i.e., oxygen) are common. Therefore, adding Cr to SZO generates both oxygen vacancies and free holes. However, Cr addition is usually compensated by oxygen vacancies (one vacancy for every two Cr atoms) such that the material remains essentially insulating. In contrast, free electrons primarily compensate for La in SZO. Therefore adding La drastically lowers the resistance of SZO. Similarly tantalum (Ta) or niobium (Nb) can substitute for Zr to lower SZO resistivity.

**[00172]** Further, vacancies (either anion or cation) can also act to create charge traps. The charge imbalance caused by a vacancy can be compensated by the same mechanisms that compensate for the intentional additions of a dopant. Thus, an oxygen vacancy compensated by 2 Cr atoms provides no free carriers, but if there is insufficient Cr for full compensation, oxygen vacancies lead to free electrons.

**[00173]** Some dopants create centers at deep levels in the bandgap. Such dopants create centers where a charge would need a high level of energy to exit that level, effectively creating traps with the deep levels. For example, Cr, iron (Fe),or nickel (Ni) can create traps in STO and SZO. To the contrary, yttrium (Y), La, Nb and Ta would create centers at shallow levels, which would not be traps.

**[00174]** Treatment can additionally occur through, for example, ion implantation. In ion implantation accelerated ions penetrate a solid surface up to certain depth that is determined by the ion energy. Ion implantation can be used to introduce dopants, to form buried layers, and to modify solid surfaces.

**[00175]** Another treatment method is to expose a reactive metal or a conductive oxide to either an anneal or a gas at a given temperature within a given ambient. Some anneals can be easily integrated into fabrication. For example, if the array only has a single memory plug layer, then the bottom layers might be subjected to high temperatures in order to properly form the conductive oxide. However, the top layers can then be deposited at temperatures far below what is necessary for forming the conductive oxide. Similar results can be obtained by laser treating one of the



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surfaces, or exposing one of the surfaces to a plasma process (such as plasma etching).

**[00176]** Another treatment method might be to expose the entire structure and/or a particular surface layer to a physical re-sputtering, typically by using Ar and/or $O_2$ or other inert gas plasma. Re-sputtering is a technique commonly used to clean-up surfaces. Since a new film is not deposited when the plasma hits the surface in the sputtering chamber, it can be considered to be the opposite of sputtering. Similarly, the surface can be exposed to an inert ion from an ion gun, bombarding the surface with accelerated inert ions, such as ionized Ar.

**[00177]** Typically, the goal of such treatments is to create traps. Traps can also be introduced with high energy radiation or particle beam bombardment. For example, UV and X-ray radiation induces traps in $SiO_2$. Also, neutron transmutation doping can be used to create dopant atoms in silicon. Furthermore, traps can be created by an electrical initialization process during which oxygen vacancies drift through an oxide in the presence of an applied electric field. Of course, the dominant carrier mechanisms may change depending upon the treatment of the interface layer.

**[00178]** A memory plug using an interface layer, therefore, has many similarities with a traditional MIM structure. However, it should be noted that the interface layer exhibits memory characteristics regardless of whether it has been formed. The interfacial layer may be very rough, and therefore allows many current leakage paths, which eliminates the need for forming at low currents. It should be appreciated that the term "memory element" includes all the layers that contribute to the memory effect. Such layers, depending on the specific embodiment, can include the interface layer, the conductive oxide, reactive metal layer and/or electrodes.

***Multiple Interfaces***

**[00179]** Making sandwich-type structures can create additional interfaces. Depositing layers of reactive metal/conductive oxide/reactive metal will, for example, create two separate interfaces, as will depositing layers of conductive oxide/reactive metal/conductive oxide (assuming the entire middle layer does not reactive with the top and bottom layer, which would result in only a single interfacial layer). Although multiple interfaces can be created, it is sometimes useful to subject the interfaces to dissimilar treatments in order to bias the memory plug in a single direction, thereby encouraging the desired hysteresis effect.



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**[00180]** Including dopants in only either the top or the bottom layer, or using different dopants allows the use of substantially similar materials, thus avoiding control issues while imparting enough differences between the substantially similar materials to constitute and create an active interface.

**[00181]** Thus, for example, a conductive metal oxide layer that includes a metal oxide strontium zirconate doped with chromium could be sandwiched between two substantially similar conductive metal oxide layers. The top conductive metal oxide layer can be strontium zirconate doped with iron, which results in a p-type metal oxide layer. The bottom conductive metal oxide layer is strontium zirconate doped with niobium, which results in an n-type metal oxide layer.

**[00182]** The thickness of such layers is not critical, typically 500 Å may be used, but any thickness from 100 to 1000 Å will usually be adequate. The only constraint is to ensure that the layer is thick enough that it is not completely depleted of charges when a voltage is applied across the memory element. The thickness of the middle layer is more critical, as tunneling conduction is preferred and will usually be achieved between 10 and 100 Å of thickness, depending on the voltage applied to the memory element. A typical thickness of 30 Å is adequate.

**[00183]** By causing the top metal oxide layer to have a surplus of either holes or electrons, and causing the bottom metal oxide layer to have a surplus of either electrons or holes (the opposite of the top metal oxide layer), it is possible to create an asymmetry in the electrical properties of the memory element. The asymmetry ensures that a program pulse of one polarity always changes the material to a higher resistance, and a program pulse of the other polarity changes the material to a lower resistance. If the top and bottom conductive metal oxide materials are the same, there is no asymmetry, and, at first, the memory material may switch either way. To avoid this lack of directionality, pre-conditioning techniques can be used, such as applying a high voltage pulse across the memory material. However, by using slightly different materials such an initialization step can be minimized or avoided.

**[00184]** Another way to create an asymmetry between the bottom and top metal oxide layers is to use the same type material, that is both layers being n-type (surplus of mobile electrons) or p-type (surplus of mobile holes), with a different concentration of mobile carriers.

**[00185]** Notably, the dopants included in the conductive metal oxide layers are typically used in low concentration. Generally, the amount of dopant included in the



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conductive metal oxide is less than 10% by weight and more particularly approximately 1% by weight.

**[00186]** The dopants used to create an n-type and a p-type region can be chosen with the following guidelines. An n-type dopant has a higher valence (more positive charge) than the lattice atom it replaces, therefore n-type dopants which substitute for Zr or Ti in strontium zirconate or strontium titanate include Nb and Ta. Similarly, n-type dopants which substitute for Sr include Y, La, and all of the lanthanide elements. A p-type dopant has a lower valence (less positive charge) than the lattice atom it replaces, therefore p-type dopants which substitute for Zr or Ti include Cr, Mn, Fe, Co, Ni, and Al. Another way to obtain hole conduction in strontium zirconate would be to dope with Nb on the Zr site and simultaneously with nitrogen on two adjacent oxygen sites to obtain p-type conductivity.

**[00187]** In still another embodiment of the present invention, the bottom conductive metal oxide material can be made out of praseodymium calcium manganese oxide ($Pr_xCa_{1-x}MnO_3$) with a selected ratio of $Mn_3$ or $Mn_4$ ions. The ratio of $Mn_3$ or $Mn_4$ can be adjusted by varying, during deposition, the ratio of Pr and Ca atoms. The top conductive metal oxide can be made out of $Pr_xCa_{1-x}MnO_3$with another specific ratio of $Mn_4$ or $Mn_3$ ions so that the top metal oxide layer and the bottom metal oxide layer are dissimilar.

**[00188]** In similar fashion, one skilled in the art can appreciate that only two layers of conductive metal oxides may be utilized without departing from the scope of the present invention. In particular, either the bottom conductive metal oxide layer or the top conductive metal oxide layer can be excluded from the memory device because an active interface is still present between the remaining conductive metal oxide layers and the electron or hole imbalance is sufficient to provide asymmetry. As such, the use of three layers as described above is illustrative only and not indicative of any inherent limitation of the scope of the disclosure as any of a number of conductive metal oxide layers are contemplated by the present invention.

**[00189]** As another example of the present invention, it is also possible to use different materials to form the conductive metal oxide layers, as long as these materials are compatible. Example compatible materials would have a similar crystal structure and similar lattice parameters. Strontium ruthenate (SRO) and strontium titanate STO constitute an example of such a material, where the distance between Sr-



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Ru atoms in a SRO crystal and Sr-Ti atoms in a STO crystal are within a few percentage points of each other.

**[00190]** The criteria for other compatible materials would be the same as the criteria used for a good epitaxy. For example, Si is compatible with $Al_2O_3$ (Sapphire) since one plane of $Al_2O_3$ crystal closely matches an integral multiple of Si crystal plane.

***Modifying the Electrical Properties of Various Layers***

**[00191]** The electrical properties of layers within the memory plug can be modified with several techniques. These electrical properties include, but are not limited to, the resistivity of the material as well as the temperature sensitivity of such resistance; the amount or magnitude of charge traps; and magnetic field dependence.

**[00192]** It is known that the resistivity of certain metal oxides depends upon various factors, often including some of the following: film thickness, oxygen content of the film, stoichiometry, elemental composition, deposition method and conditions, degree of crystallinity, crystallite size, crystalline orientation, and doping level and choice of dopant. Current research indicates that suitably low resistivity (less than or equal to 1 ohm-cm) materials can be achieved by judicious choice of these parameters.

**[00193]** One example of a suitable film thickness for the memory applications of this invention is approximately 100Å to 3000Å. Thinner films sometimes have higher strains, usually resulting from a slight misalignment with the seed layer, which can result in higher resistivity. Film thickness has been discussed by S.I. Khartsev, et al. in "Colossal magnetoresistance in ultrathin epitaxial $La_{0.75}Sr_{0.25}MnO_3$ films," Journal of Applied Physics, Vol. 87, No. 5, 1 March 2000.

**[00194]** Another factor that affects resistivity is the oxygen content of the film. By properly controlling the exposure to oxygen during deposition and annealing (if any) the resistivity can be controlled. It has been observed that 1500Å lanthanum manganese oxide (LMO) films deposited by pulsed laser deposition in oxygen environments have a lower resistivity than films deposited in vacuum (but otherwise identical conditions). *See* Y. G. Zhao, et al., "Effect of oxygen content on the structural, transport, and magnetic properties of $La_{1-\delta}Mn_{1-\delta}O_3$ thin films," Journal of Applied Physics, Vol. 86, No. 11, 1 December 1999. Cooling down the freshly deposited film in an oxygen-containing atmosphere further decreases film resistivity.



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**[00195]** It has been further observed that adjusting the relative amounts of the rare earths and the alkaline earth metals can modify resistivity. Higher ratios of alkaline earth to rare earth metals can, to a degree (e.g., up to about 50:50 in lanthanum calcium manganese oxides), lower resistivity. *See* Guo-Qiang Gong, et al., "Colossal magnetoresistance of 1000000-fold magnitude achieved in the antiferromagnetic phase of $La_{1-x}Ca_xMnO_3$," Applied Physics Letters, Vol. 67, No. 12, 18 September 1995.

**[00196]** Further, it has been found that some polycrystalline materials may have lower resistivities than their amorphous and single crystal counterparts. Large changes (i.e., greater than about 10x), are, however, not typically necessary for making a practical memory chip with only two resistive states (although they may be necessary for memory cells that hold multiple bits of information).

**[00197]** In addition to the above properties, certain process and design features are important. First, the seed layer or other "substrate" on which the oxide deposits impacts the resistivity of the oxide and other properties. Often the underlying crystallographic orientation of the substrate will epitaxially propagate to the upper levels the oxide element. So, for example, if the underlying substrate has a 100 orientation, then the oxide may preferentially deposit in a 100 orientation. Preferably, the underlying substrate is a conductive electrode such a noble metal (e.g., platinum) or relatively conductive oxide such as $LaNiO_3$. In polycrystalline structures, suitable crystallite sizes may range from about 100Å to about 500Å.

**[00198]** If more than one dopant is used, the dopants may serve to modify the same or different properties of the various layers. Doping the oxide, the reactive metal layer and/or the interface can cause electrical properties to be more uniform, whereby the electrical properties have a greater predictability.

**[00199]** In a particular aspect, doping alters resistivity. For example, application of an electrical pulse reversibly changes the resistivity from either a high value to a low value or from a low value to a high value; and doping the materials can modify the magnitude of the difference from the high value to the low value.

**[00200]** In another aspect, doping alters the amount or magnitude of charge traps or otherwise modifies the ability of the charge traps to capture electrons and thus, improve the data retention capability of the memory plug. In other words, the doping should facilitate electrons tunneling through the memory plug and leaving charge traps during the operation of the memory.



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**[00201]** In yet another aspect, doping additionally reduces the temperature sensitivity of its resistance. In a further aspect, doping reduces magnetic field dependence.

***Electrical Properties of the Cross Point Array***

**[00202]** FIG. 46 depicts a simplified representation of a cross point memory array. The selected X line 4605 and the selected Y line 4610 intersect at the selected cell 4615. The remaining unselected X lines 4620 and the remaining unselected Y lines 4625 are each represented as a single group for simplicity. Similarly, the unselected memory cells 4630 on the selected X line 4605, the unselected memory cells 4635 connected to the selected Y line 4610, and the unselected cells 4640 connected to neither the selected X line 4605 nor the selected Y line 4610 are also represented as groups for simplicity.

**[00203]** The combination of unselected memory cells 4630, 4635, and 4640 is set in parallel with the selected memory cell 4615, and therefore, the current that is read when applying some $V_x$ on line 4605 and some $V_y$ on line 4610 will be: $(V_x-V_y)$ x $(R_{4615}+R_{4630}+R_{4635}+R_{4640})/(R_{4615}$ x $(R_{4630}+R_{4635}+R_{4640}))$, where $R_{4630}$, $R_{4635}$, and $R_{4640}$ are the resistances of the unselected memory cells 4630, 4635, and 4640 and $R_{4615}$ is the resistance of the selected memory cells 4615. In large arrays, the combined resistance of the selected cell 4615 in parallel with the unselected cells 4630, 4635, and 4640 will be significantly less than the resistance of the selected cell 4615 alone. As such, it is not practical to read the resistance of the selected cell 4615 with floating lines and unselected cells 4630, 4635, and 4640 that allow current to flow.

**[00204]** Although clamping the unselected lines 4620 and 4625 at specific voltages reduce the effect of the unselected memory cells 4630, 4635, and 4640, such techniques result in current consumption through unselected cells. For example, if $V_y = -V_x$ and the unselected lines 4620 and 4625 are held at 0V, the unselected memory cells 4635 on the selected Y line 4610 will pass a current equal to $V_x/R_{4635}$, which can be high if there are a high number of unselected array lines.

**[00205]** As previously discussed, a higher voltage is typically applied on both selected X line 4605 and Y line 4610 during a write operation. Although the current leakage in other elements is not critical to the selected element, in a large array, the current leakage amplitude could be such that it would require impractically large currents from the line drivers. Further, unselected memory cells 4630, 4635 and 4640



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carrying unselected current could have their memory state affected by the unselected current.

**[00206]** FIG. 47 depicts an exemplary cross point array 4700 where each memory cell includes a diode. As the voltage $V_x$ is applied on selected X line 4705 and $V_y$ is applied to the selected Y line 4710, the diodes block the current flow through the unselected memory cells 4730, 4735 and 4740 in series. With unselected lines 4720 and 4725 left floating the current going from selected X line 4705 to selected Y line 4710 will pass exclusively through the selected memory cell 4715, therefore giving an accurate evaluation of the value of the resistance of the memory cell 4715.

**[00207]** During a write operation, the diodes will also block the parasitic current path through unselected memory cells 4730, 4735 and 4740. However, if the unselected lines 4720 and 4725 are floating then they will be charged by current going through the unselected memory cells 4730, 4735 and 4740. For example, one of the unselected lines that crosses the selected X line 4705 will reach $V_x - V_{fwd}$, where $V_{fwd}$ is the forward bias voltage drop across a diode, since line 4705 is at $V_x$ (which, during a write operation, might be 1/2 $V_W$) and current can flow through the unselected memory cell. If $V_x$ is high enough, the current flowing temporarily through the unselected memory cell can be high enough to disturb its resistive state. If unselected lines 4720 and 4725 are clamped to a fixed voltage, as long as $V_x$ is above a diode voltage drop, some cells will see a constant current flow, which is undesirable because it could slowly affect the state of those cells.

**[00208]** FIG. 48 depicts an exemplary cross point memory array 4800 where each memory cell includes a back to back diode. FIG. 49 depicts the current-voltage, or "IV" characteristic of a back to back diode device. At low voltages, between $-V_{NO}$ and $+V_{NO}$, the device does not conduct or conducts only slightly. The $V_{NO}$ voltage can be referred to as the non-ohmic voltage, where conduction becomes significant. Below $-V_{NO}$ and above $+V_{NO}$, the device is conductive.

**[00209]** FIG. 50 shows the IV characteristic of one type of linear memory element. As a positive voltage is applied across its terminals, the memory element has a substantially linear resistance value, as a write threshold voltage $V_W$ is reached, the resistance of the memory element rises. As the voltage across the terminals is decreased and becomes negative, the memory element characteristic exhibits a higher resistance value. When the voltage across the terminals reaches a negative write threshold, the resistance state goes back to a lower value. FIG. 51 depicts the IV



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characteristics of both a linear memory element and a back to back diode in series. A further embodiment would use two tunnel or backward diodes mounted back to back. The principal of backward diode is explained in Sze S.M., *Physics of Semiconductor Devices*, pp. 537-539, 1981, and can be realized with a N+, a P+ and another N+ layer of about 500 Å each.

**[00210]** Referring back to FIG. 48, one method of writing to the cross point memory array 4800 is to apply $V_x = (V_{NO} + V_W)/2$, and $V_y = -(V_{NO}+V_W)/2$ on the respective selected lines 4805 and 4810, and to ground the unselected lines 4820 and 4825. This will result in the voltage across the memory element of the selected memory cell 4815 to be $V_x - V_y - V_{NO}$, or $V_W$, and across the memory elements of the unselected cells 4830 and 4835 on a select line to be $(V_{NO} + V_W)/2 - V_{NO}$, or $V_W/2 - V_{NO}/2$, and across the memory elements of the unselected memory cells 4840 to be 0V, since in this case the unselected lines 4820 and 4825 are grounded. Applying the reverse polarity voltage on the selected X and Y lines 4805 and 4810 will program the opposite data in the selected cell. Therefore, if $V_W$ is set to be higher than the threshold write voltage and lower than twice the threshold write voltage, the unselected cells that see $V_W/2$ across their terminals are not affected and written during the write operation.

**[00211]** A read operation will process similarly, replacing $V_W$ by $V_R$, a lower voltage so that $V_R$ is below the threshold write voltage. In the read case, the selected memory element will see a $V_R$ voltage across its terminal and unselected memory elements will see $V_R/2 - V_{NO}/2$, or zero if this $V_R$ is less than $V_{NO}$.

**[00212]** During read another point of concern are leakage currents, since the read operation tries to ascertain the value of the selected cell's resistance by applying a voltage and reading a current. Any change in the read current may affect the read value. For example, if each unselected cell 4835 on line 4810 leaks 1 nA, and the array has 1024 cells per line, the leakage on the line would be 1023 x 1nA, or 1.023 μA. Although 1.023 μA can be tolerated in many systems, a leakage of 100 nA per cell would create more than 100 μA of leakage, which could affect the proper read of the selected cell. In such a case, a smaller array, possibly 100 cells per line, would only have a 100 x 100nA or 10 μA of leakage, and would still be workable.

**[00213]** An alternate embodiment to the memory element and the back to back diode in series is to embed the back to back diode into the memory element, and take



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advantage of the non-ohmic nature of some metal / semiconductor interfaces. FIG. 52 depicts an representative IV curve of a stack consisting of a Pt electrode, crystalline PCMO, a thin layer of Al, and another Pt electrode that exhibits a non-ohmic behavior. Although such material shows some leakage below $V_{NO}$, it is still applicable to smaller arrays, and may be improved to be of use in larger arrays.

**[00214]** To use this embodiment, the threshold write voltage of the memory element has to be adjusted. Typical non-ohmic behavior, such as Schottky effect, will result in a $V_{NO}$ below 1V. If $V_W$ is above $V_{NO}$, the unselected cells will see $(V_W - V_{NO})/2$ across the memory element, which will create an un-desirable current in the unselected memory cell. To avoid or reduce this current, it is preferable to keep $V_W$ close to or below $V_{NO}$. Therefore, the write threshold voltage will have to be adjusted, by varying the properties of the conductive metal oxide such as thickness, oxygen content, crystalline structure, stoichiometry to achieve a write threshold below $V_{NO}$.

***Methods of Manufacture***

**[00215]** FIG. 53 depicts a cross sectional view of a partially processed integrated circuit up to the completion of a bottom front end of line (FEOL) processed section 5300. A p-type substrate 5310 lies beneath an n-well 5315 that in turn lies underneath a p-well 5320. Two N+ islands 5325 and 5330 are created within the p-well 5320 to form reverse-biased p-n junctions. A first inter-layer dielectric (ILD) 5305 is formed atop the p-well 5320. A select line 5335 can be formed, within the first ILD 5305, with a standard polysilicon gate controllably turning on a field effect transistor (FET) type of conduction between the two N+ islands 5325 and 5330. For simplicity and low cost fabrication, the selected FEOL process can be any of the many standard IC processes such as Silicon, Germanium, Gallium Arsenide, Silicon-Germanium and Silicon on Insulator. FEOL processes in this embodiment can be defined as operations performed on a semiconductor wafer in the course of device manufacturing up to but just before first metallization, and might end with chemical-mechanical polishing (CMP) of the first ILD 5305. To simplify the description of the present invention, the following embodiments are generally described using a Silicon process with the understanding that the scope of our present invention is not so limited.

**[00216]** FIG. 54 depicts a cross sectional view of a further processed integrated circuit 5400 after conductive plugs are formed in the FEOL section 5300 of FIG. 53. In the process that is shown, a number of contact holes, each corresponding to the



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location of a desired conductive plug, are first formed through the first ILD 5305. Barrier/adhesion layers 5405 and 5410 can then sputtered inside the contact holes. Notice that sputtering is a form of physical vapor deposition technique. The specific sputtering composition will depend on the conductive plug material being used, and can be 100Å Ti followed by 200Å of TiN. Next, a conductive plug material can be deposited within the contact holes atop the barrier/adhesion layers 5405 and 5410. As illustrated, the conductive plug can be Tungsten (W)-plug 5415 and Tungsten (W)-plug 5420 deposited with 5000Å of W using chemical vapor deposition (CVD) followed by an etchback process or chemical-mechanical polishing (CMP) to remove excess conductive plug material atop the first ILD 5305 surface.

**[00217]** FIG. 55 depicts a cross sectional view of a further processed integrated circuit 5500 after the partial formation of a middle memory plug section atop the partially processed integrated circuit 5400 from FIG. 54. First, a bottom electrode 5505 is deposited. The bottom electrode 5505 can in turn be made of multiple layers, such as a 500Å thick barrier layer of TiAlN to prevent metal inter-diffusion followed by a 500Å $LaNiO_3$ or 1000Å Pt. These layers can be deposited by sputtering. Next, a conductive oxide 5510 is deposited on top of the bottom electrode 5505. The conductive oxide and can be 500Å of a material having a stoichiometry of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) and is preferably deposited at less than or equal to about 600°C by a physical vapor deposition technique such as sputtering, followed by annealing. The annealing step helps to recover the intended crystalline structure and material composition of the conductive oxide 5510. Next, a top electrode 5515 can be deposited using sputtering. The top electrode can have a composition similar to the bottom electrode 5505, except that a small layer of a reactive metal (e.g., 10Å of Al) is first deposited on the conductive oxide 5510. Standard photolithography and appropriate multi-step etch processes can then be used to pattern the bottom electrode/conductive oxide/top electrode layers into a memory plug. As an optional improvement, one or both of the bottom electrode 5505 and the top electrode 5515 can be made of a conductive layer and a barrier layer to prevent metal inter-diffusion.

**[00218]** Numerous sputtering techniques can be employed to further improve the formation of the middle memory plug section. In an off-axis sputtering process, the target surface, the supplier of the material to be sputtered, and the substrate surface, the receiver of the material to be sputtered, are oriented approximately orthogonal to each other, about 70 to 90 degrees. The advantage of the off-axis sputtering includes



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minimizing material damage from ion impingement during an on-axis reactive ion sputtering process. Another implementation can include two oppositely faced targets as in facing target sputtering (FTS). In a co-sputtering process, the deposited materials are sputtered from more than one target concurrently so as to create a plasma of more than one material, hence the deposition of more than one material on the substrate surface at the same time. Thus, the advantage of co-sputtering includes flexibility of material composition. In a continuous deposition process, in-situ multi-layer film deposition takes place inside the same deposition chamber without breaking the vacuum. This deposition technique is most easily accomplished, for example, in a sputtering machine by keeping the substrate at one location while switching targets or by switching deposition chambers within one system. By not breaking the vacuum, numerous contamination and oxidation problems from exposure to air are avoided.

**[00219]** Given the above discussion, the deposition of the conductive oxide 5510 can advantageously employ the co-sputtering technique. At least one of the three sputtering processes for the bottom electrode 5505, the conductive oxide 5510 and the top electrode 5515 can employ the off-axis sputtering technique. Furthermore, out of these three sputtering processes, at least two consecutive sputtering processes can advantageously use the continuous deposition technique. These layers are then patterned (photodefined) to create the stacks 5505, 5510 and 5515 on top of the contact 5420. As another option, an etch stop/diffusion barrier 5520 might then be deposited to protect the PCMO from inter-diffusion. The etch stop/diffusion barrier 5520 would surround the exposed surfaces of the bottom electrode 5505, top electrode 5515 and conductive oxide 5510 as shown. Notice that the etch stop/diffusion barrier 5520 is a dual-function layer also acting as an etch stop in the fabrication process. Notice also that the etch stop/diffusion barrier 5520 forms a sidewall layer that surrounds the side surfaces of the bottom electrode 5505, the conductive oxide 5510 and the top electrode 5515. The etch stop/diffusion barrier 5520 can be made of 250Å of $Si_3N_4$, $TiO_2$ or $Al_2O_3$. As a material improvement, the deposition of the conductive oxide 5510 can be followed by modification of the interface property between the conductive oxide 5510 and the later deposited top electrode 5515. More specifically, the modification of the interface property can be done by ion implantation, in situ plasma treatment in various gasses, or in situ annealing in various gasses. Possible gasses might include argon, oxygen or hydrogen.



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**[00220]** FIG. 56 depicts a cross sectional view of a further processed integrated circuit 5600 after the complete formation of a middle memory plug section atop the partially processed integrated circuit 5500 of FIG. 55. As a clarification while counting IC components upwards from the bottom, the middle memory plug section includes all IC components above the top surface of the first ILD 5305, as shown in FIG. 54, up to the top surface of a second ILD 5605.

**[00221]** The second ILD 5605 is deposited on top of the etch stop/diffusion barrier 5520. The second ILD 5605 can be made of a thick $SiO_2$ layer and then planarized by chemical-mechanical polishing (CMP). A plurality of via holes, locationally and geometrically corresponding to the top electrode 5515, can then be formed with standard photolithography and via etch. Barrier/adhesion layers 5610 and 5615 are then sputtered inside the via holes. The specific sputtering composition can be 100Å Ti followed by 200Å of TiN. Next, a conductive plug material is deposited within the contact holes atop the barrier/adhesion layers 5610 and 5615. The conductive plug can be W-plug 5620 and W-plug 5625 deposited with 5000Å of W using chemical vapor deposition (CVD) followed by an etchback process or CMP to remove excess conductive plug material atop the second ILD 5605 surface. As a process improvement, an annealing step can take place at this point to help in recovering the original crystalline structure and material composition of the middle memory plug section.

**[00222]** FIG. 57 depicts a cross sectional view of a completely processed integrated circuit 5700 after the complete formation of a top metallization section atop the middle memory plug section. As a clarification while counting IC components upwards from the bottom, the top metallization section includes all IC components above the middle memory plug section. Using standard processes, one or more metallization layers can be formed above the partially processed integrated circuit 5600 of FIG. 56. Two metallization layers are illustrated in this embodiment. The first metallization layer can be used to form both a reference line 5705 and a metal plug 5710 that eventually connects two W-plugs 5620 and 5715. The W-plug 5715 is used to connect a data line 5720, formed during the second metallization layer, to the metal plug 5710 through a third ILD 5725 used to support the data line 5720. The W-plug 5715 and the third ILD 5725 are respectively formed with processes similar to those described before. As a process improvement, an annealing step can take place at this point to help recovering the original crystalline structure and material



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composition of the completed IC. By now it should become clear to those skilled in the art, while the bottom front end of line section 5300 is shown with the addition of a FET with a terminal of N+ island 5325 connected to the bottom electrode 5505 of the memory device via the W-plug 5420, in general any other IC components can be implemented instead to connect the bottom electrode 5505 to suit a corresponding application. Some examples are a resistor, a capacitor or a non-ohmic device like a diode. To further clarify the spatial orientation and alignment of the memory device an X-Y-Z Cartesian coordinate system can be set in reference to FIG. 55: the interfaces between the electrodes 5505 and 5515 and the conductive oxide 5510 generally define the X-Y plane while the direction of current through the memory device is essentially parallel to the Z-axis.

**[00223]** FIG. 58 depicts a cross sectional view of another completely processed integrated circuit 5800 wherein the memory devices of the middle memory plug section further include features of a hard mask 5530 layer and a spacer 5525. Except for these features, whose fabrication process is to be presently described, the completely processed integrated circuit 5800 is otherwise the same as the completely processed integrated circuit 5700 depicted in FIG. 57. The spacer 5525 can be made of a dielectric material surrounding the top electrode 5515. Some examples of the dielectric material are $Si_3N_4$, $SiO_2$, $TiO_2$, SiON or $Al_2O_3$. The hard mask 5530 is typically made of an electrically conductive material having a similar X-Y cross section as the top electrode 5515. The hard mask 5530 is a masking material that is used as etching mask to protect the film or films underneath from etching in a plasma etch chamber. The hard mask materials can be divided into two categories, insulator or conductor. The popular insulating hard mask materials are oxide and nitride. The popular conductive hard mask materials are binary nitrided metals including TiN, TaN, WN, etc. and ternary nitrided metals including TiSiN, TiAlN, TaSiN, etc. One advantage of the hard mask over a standard photo-resist is that the hard mask can resist a dry etching process requiring elevated temperature. Usually reactive ion etching (RIE) at an elevated temperature is required to etch precious metals or complex metal oxides because of the difficulties associated with their etching, especially the etch byproduct volatility. Due to the impact of previous etch steps defining the profile of bottom electrode 5505, conductive oxide 5510 and top electrode 5515, the outer periphery of the conductive oxide 5510 is often damaged by plasma ions, causing a corresponding leakage current conduction in the Z-direction.



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This leakage current can short out the current conduction through the bulk of the conductive oxide 5510, and is therefore undesirable and detrimental to the operation of the memory device. The introduction of the spacer 5525 makes the cross sectional area, along the X-Y plane, of the top electrode 5515 smaller than that of the conductive oxide 5510. The spacer 5525 creates a resistance between the sides of the electrode 5515 and the edge of the conductive oxide 5510. Hence, the X-Y footprint of the spacer 5525 can be made large enough to make the resistance between the sides of the top electrode 5515 and the edge of the conductive oxide 5510 high enough to render the effect of the leakage current conduction negligible.

**[00224]** FIG. 59A through FIG. 59E detail an exemplary sequence of various processing steps that could be used for the creation of the hard mask 5530 and spacer 5525 features of the memory device 5800 of FIG. 58. FIG. 59A illustrates only a memory device following the steps of sputtering a bottom electrode layer 5505, sputtering a conductive oxide 5510, sputtering a top electrode layer 5515 and depositing a hard mask layer 5530. The hard mask layer can be deposited by various means such as Chemical Vapor Deposition, spin coat or sputtering. Like before, the deposition of the conductive oxide 5510 can be followed by modification of the interface property between the conductive oxide 5510 and the later deposited top electrode 5515. More specifically, the modification of the interface property can be done by ion implantation, in situ argon plasma treatment, in situ oxygen plasma treatment, in situ annealing in argon or in situ annealing in oxygen. FIG. 59B and FIG. 59C illustrate the steps of photo lithographically etching, with a photo resist 5535, the hard mask layer 5530 and the top electrode layer 5515 both having cross sections smaller than that of a later-patterned conductive oxide 5510. A dielectric material is then deposited on top to form the spacer 5525. FIG. 59D illustrates the memory device following an anisotropic dry etching, with a much higher etch rate in the Z-direction than the X- and Y-directions, of the dielectric material to create a sidewall spacer 5525 surrounding the side surfaces of the top electrode 5515 and the hard mask 5530. Finally, FIG. 59E illustrates the memory device following an etching of the conductive oxide layer 5510 and the bottom electrode layer 5505. As an optional measure to further remove the damaged outer periphery of the conductive oxide 5510, an additional clean-up step of wet etching can be applied to selectively remove 50 - 150 Å material of the conductive oxide sides, thus forming an undercut.



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**[00225]** FIG. 60 depicts a cross sectional view of yet another completely processed integrated circuit 6000 wherein the memory devices of the middle memory plug section include an undercut 5540. Geometrically, the X-Y cross section of the bottom electrode 5505 is larger than that of the conductive oxide 5510. Similarly, the X-Y cross section of the top electrode 5515 is also larger than that of the conductive oxide 5510. Except for the undercut 5540 the completely processed integrated circuit 6000 is otherwise the same as the completely processed integrated circuit 5700 depicted in FIG. 57. Referring back to FIG. 55 and its accompanying description, after patterning the bottom electrode/conductive oxide/top electrode layers into a memory plug, an optional clean-up step of wet etching can be applied to selectively remove 50 - 150 Å of the sides of the conductive oxide 5510, thus forming an undercut 5540 as shown in FIG. 60. The purpose of the undercut 5540 is to directly remove the damaged outer periphery of the multi-resistive state element 5510 that would otherwise cause an undesirable leakage current conduction in the Z-direction, as explained before.

***High Temperature Fabrication***

**[00226]** As previously described, the fabrication techniques used for the memory plug will typically dictate the requirements of the layers beneath the memory plug (e.g., the select line in a transistor memory array; and the driver circuitry and the bottom conductive lines in a cross point array). Since certain fabrication processes (e.g., solution based spin on followed by high temperature anneal, pulsed laser deposition, sputtering, and metal-organic chemical vapor deposition) might require high temperatures, refractory metals can be used for these layers so that they may withstand the temperatures.

**[00227]** Typical metal lines in integrated circuits are made out of aluminum or copper. However, these metals have a rather low melting point, and the structural integrity of the formed metal lines is damaged if they are allowed to melt. Furthermore, these materials cannot even withstand exposure to temperatures below their melting point. For example, although aluminum's melting point is 660C, it generally should not be exposed to temperatures above 400C. At such temperatures the aluminum atoms start to diffuse to other areas, possibly reacting with other semiconductor elements on the substrate, disturbing the characteristics of those



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elements. The diffusion increases with increasing temperatures, becoming largely unworkable at 450C.

**[00228]** Therefore, if typical low temperature conductive lines were used (i.e., aluminum or copper), any material above the first metal line would be limited to temperatures where they were considered to be "stable" metals. However, most manufacture processes require high temperatures to grow the crystalline or poly-crystalline structure of the multi-resistive state element. In such processes, high temperature is typically between 600C and 800C.

**[00229]** Therefore, using conductive lines that can withstand high temperatures is sometimes required. High melting point metals are usually referred to as refractory metals, and include tungsten, molybdenum, tantalum, niobium, chromium, vanadium and rhenium, as well as the less common zirconium, technetium, ruthenium, rhodium, hafnium, osmium and iridium. Some of the latter metals may, however, not be practical for use in an integrated circuit process. Refractory metals also include any compounds and alloys that have high melting points. Additionally, in many applications it is preferable to use a material with a low resistivity in order to both improve the memory access time and allow for longer array lines.

**[00230]** Additionally, any conductive material with a melting point of at least 100C above the desired process temperature can typically be used. For example, in the case of aluminum, a desired process temperature 200C below the melting point of aluminum is generally preferred. Therefore, an optimum conductive array line would be a refractory metal with a low resistivity that has a melting point at least 100C above the high temperature processing that is used.

**[00231]** Conductive lines are not the only elements that may need to withstand high temperature processing. Typically, only the layers that are deposited after the high temperature processing of the memory plug are free from those high temperatures. Since no high temperature steps are required after the memory plug's formation, the top layers of the memory do not need to have high melting points. Therefore, such layers can be made with standard metallization materials such as aluminum, copper or aluminum alloys such as aluminum-silicon, aluminum-silicon-copper or aluminum-copper.

**[00232]** The elements that may need to withstand high temperature processing can include the multi-resistive state material, a possible non-ohmic device, appropriate electrodes, bottom layers of conductive array lines, and contact plugs to connect the



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electrodes of the memory cells to the conductive array lines. Electrodes made out of noble metals, binary or ternary oxides and nitrides, and conductive metal oxides are temperature resistant. Examples of high temperature resistant materials that can act as sacrificial layers include ternary oxides such as ruthenium tantalum oxide, ruthenium titanium oxide, iridium tantalum oxide or iridium titanium oxide and ternary nitrides such as ruthenium tantalum nitride, ruthenium titanium nitride, iridium tantalum nitride or iridium titanium nitride.

***Mechanisms for Storing Resistive States***

**[00233]** The use of stored or trapped charges is the dominant mechanism for storing data in a non-volatile memory cell. During device operation, these trapped charges function to modify, for example, the silicon surface conductivity of a FET. A corresponding general device configuration is illustrated in FIG. 61. A FET 6100 includes a source 6130 and a drain 6120 separated by a control gate 6110. This FET 6100 can be of n-type or p-type. For simplicity an n-type FET will be described. Thus, the drain 6120 and the source 6130 are both made of an n-doped semiconductor material while the substrate 6140 is made of a p-doped semiconductor material. When a positive voltage is applied to the control gate 6110, electrons within the substrate 6140 are attracted toward the control gate 6110 and form an inversion layer 6150 in an area called the 'channel' that is within the substrate 6140 and under the control gate 6110. The channel then allows current conduction between the drain 6120 and the source 6130.

**[00234]** Notwithstanding the foregoing description, the presence of any trapped charges 6160 within the oxide 6170 and between the control gate 6110 and the substrate 6140 will modify the required value of the voltage applied to the control gate 6110 to create the inversion layer 6150. For a case of negative trapped charges 6160, the higher the magnitude of trapped charge the higher the required voltage would have to be. The reason is that the negative charges trapped in the oxide will repel the electrons away from the channel, necessitating the application of a higher positive voltage on the control gate 6110 to counteract this effect.

**[00235]** For each of the above devices, the magnitude of trapped charges can be altered through various mechanisms. Retrieving data can then be accomplished by sensing the voltage that is required to create the inversion layer. Similarly, the memory material in the present invention also has a resistive state that is modified with trapped charges. As previously described, the memory material can be any of a



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variety of materials, and will most commonly be an insulator or semiconductor that is treated to become conductive.

**[00236]** A current carrier can be either a negatively charged electron or a positively charged hole. The current carrier trap locations, or simply traps, are regions within the memory material causing the presence of localized energy levels within the bandgap of the memory material. These traps are thus capable of trapping, or immobilizing, current carriers within the memory material and affecting its resistance.

**[00237]** Furthermore, the degree of charging or discharging the traps are dependent upon localized energy levels within the bandgap. Also, the carrier occupancy can be affected by an electric field applied across the memory material and accompanied by a corresponding current flow. Typically, the electric field will need to be beyond a certain threshold value before it affects carrier occupancy. Consequently, the resistance of a properly designed memory plug can be switched through multiple values following a corresponding number of applied voltage thresholds. The means of creating and configuring these traps will be presently described.

**[00238]** For a crystalline memory material, the traps may be located within the crystal lattice. However, for a poly-crystalline memory material, the traps may be located within the grain boundaries or within a molecular structure.

**[00239]** To foster the creation of traps, extrinsic materials, called dopants, can be introduced into the memory material in minute quantities. Typically, the dopant would make up less than 10% molecular percentage of the total material. As a result, some dopants create trapping centers at deep energy levels within the bandgap. That is, once captured at these trapping centers, a current carrier would need to acquire a sufficient amount of energy to regain its mobility. For example, the elements Cr, Fe or Ni can create traps at deep energy levels in STO and in SZO. On the other hand, the elements Y, La, Nb and Ta primarily create centers at shallow energy levels which typically do not act as traps. See the technical papers "Photochromism in Ni-doped SrTiO3," P. Koidl et al, Physical review B, Vol. 14, No. 7, Oct. 7, 1976 PP. 2703 – 2708, and "Photoinduced Phenomina in Sr1-xCaxTiO2, 0 <= x <= 0,12," S. A. Basun et al, Ferroelectrics, 1996, Vol. 183, PP. 255 – 264.

**[00240]** Traps can also be introduced in memory material with high energy radiation or particle beam bombardment. For example, UV and X-ray radiation induces traps in $SiO_2$. Also, neutron transmutation doping has been used to create dopant atoms in silicon.



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**[00241]** Traps can also be created intrinsically within the memory material during its fabrication. Examples of such mechanisms have been previously described. Furthermore, traps can be created by an electrical initialization process during which oxygen vacancies drift through a complex metal oxide in the presence of an applied electric field. See references "DC Electrical Degradation of Perovskite-Type Titanates (Ceramics, Single Crystal, A Model of the Mechanism): I, II & III," Rainer Waser et al, J. Am. Ceram. Soc., 73 [6] 1990 PP. 1645-1663 and "New conduction and reversible memory phenomena in thin insulating films" J.G. Simmons and R. R. Verderber, Proc. Roy. Soc. A. 301, 1967 PP. 77-102.

**[00242]** The presence of the trapped charge modifies or otherwise alters the conductivity of the bulk memory material. An example is illustrated in FIG. 62A, which depicts a section of a memory material 6200 with charge traps 6210. Each charge trap 6210 is shown carrying an amount of negative charge. Here, the charge traps 6210 act to reduce the flow of electrons by repelling those electrons traveling nearby. On the other hand, the same charge traps 6210 can enhance the flow of holes by attracting those holes traveling nearby. Thus, depending upon its polarity, a trapped charge could either enhance or deplete the concentration of free current carriers in its vicinity. The corresponding energy band diagram is illustrated in FIG. 62B showing a localized elevation 6220 of both conduction band EC and valence band EV.

**[00243]** The presence of the trapped charge raises or lowers, depending upon the charge type, the height of the Schottky barrier at the top electrode to memory material contact or at the bottom electrode to memory material contact. The trapped charge would raise the Schottky barrier for free carriers of like charge polarity by introducing an opposition electric field at the contact. On the other hand, the trapped charge would lower the Schottky barrier for free carriers of the opposite polarity by introducing an enhancement electric field at the contact. Consequently, a higher Schottky barrier acts to increase the resistance of the trapped charge memory device and vice versa. The corresponding energy band diagrams of the Schottky barrier are shown in FIG. 63 wherein the left side has no charged trap but the right side has a charged trap 6300 and the free carriers are electrons.

**[00244]** The interface between a metal electrode and a CMO film can have a depletion region, like in a Schottky barrier, and traps at the interface can affect conduction. Trap to trap hopping, while allowing bipolar conduction, is affected by



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the presence of trapped charge and are illustrated in the energy band diagrams without (left hand) and with trapped charge (right hand) of FIG. 64.

**[00245]** Frenkel-Poole conduction is an electric field assisted thermionic emission from moderately deep traps. Here, charges trapped in other energy levels, while not participating in the emission of current carriers, could affect the resistance as well. Under this mechanism there are two types of traps, the traps that participate in the Frenkel-Poole conduction and the charged traps responsible for the resistance memory effect. The associated trapped charges will affect the resistance by modifying the barrier height in a way similar to the mechanism above. The corresponding energy band diagrams of Frenkel-Poole Conduction without (top) and with charged trap (bottom) are illustrated in FIG. 65.

**[00246]** Tunneling conduction can happen in which current carriers tunnel from the electrode directly to the conduction band (for electrons) or valence band (for holes) in a Schottky-like structure. Here, the trapped charge in the depletion region can affect the resistance in a way similar to the Schottky barrier mechanism described above. The corresponding energy band diagrams of tunneling conduction through a Schottky junction without (left hand) and with a charged trap (right hand) are illustrated in FIG. 66.

**[00247]** Orbital ordering is a mechanism in which the electron orbitals in a crystal lattice have a preferred direction, typically in an ordered pattern, such that the resistivity of the crystal lattice will be higher than the case wherein the ordered pattern is disrupted by the addition of charged traps.

**[00248]** Direct tunneling is a mechanism during which electrons from the conduction band in semiconductor are transferred across an insulator directly (i.e. without changing energy) into the conduction band of a conductor. The probability of direct tunneling is a very strong function of the width of the barrier electron tunnels through (i.e., the oxide thickness or the interfacial layer or other insulating structure).

**[00249]** In order for trapped-charge conductive metal oxide memories to be non-volatile, trapped charges must remain trapped until intentionally depopulated. In the case where traps are populated and depopulated by means of electric field induced tunneling processes, traps having a fixed energy level will not result in non-volatility because charges will be able to discharge (or charge) with no externally applied voltage bias. However, a non-volatile trapped-charge conductive metal oxide memory can be produced by introducing "level shifting" traps into the oxide. A level-



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shifting trap is one in which the energy required to depopulate the trap is larger than that required to populate it because of a relaxation process that takes place immediately after the trap becomes populated (or depopulated). For non-volatility, an electron level-shifting trap must have an energy level above the Fermi levels of the adjacent metal electrodes when unpopulated, and below the Fermi levels when populated.

**[00250]** There are several possible relaxation mechanisms that can lead to such level-shifting. One such mechanism is a symmetric lattice distortion which takes place as a result of the change in local electric field arising from a change in the trap charge state (electron-photon interaction). This mechanism is especially active in ionic solids. A related phenomenon is an asymmetric distortion called the Jahn-Teller effect. Also electronic processes such as bond formation can lead to shifts in trap energy levels. Polarization of dipoles can also work to shift trap energy levels.

**[00251]** For those skilled in the art, while the charges and energy band diagrams from FIG. 62A through FIG. 66 are largely illustrated for electron conduction near the conduction band EC, it should be understood that the same mechanisms above are equally applicable to hole conduction near the valence band EV as well.

**[00252]** Traps can therefore be charged and discharged in a variety of ways, each mechanism potentially changing the resistance of the memory material. For example, under a high electric field the current carriers can tunnel from an electrode to the traps or between neighboring traps. For another example, the traps can also be charged by trapping free current carriers with lower energy. Clearly, the concentration of the traps, be it by molecular counts, by weight or by volume, will also determine their net total effect on the resistance of the memory material.

**[00253]** The following analytical expressions, while not being a complete set, includes some modeling expressions that have been identified in "Physics of Semiconductor devices," 2nd Edition: S. M. Sze, Publisher: John Wiley & Sons, 1981 to explain the above emissions:

Schottky emission:

$J = A^{*}T^{2} \exp\left[\frac{-q(\phi_B - \sqrt{q\xi / 4\pi\varepsilon_i}}{kT}\right]$ with a voltage and temperature dependence of $\sim T^{2} \exp(+a\sqrt{V}/T - q\phi_B / kT)$



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Frenkel-Poole emission:

$J \sim \xi \exp\left[\frac{-q(\phi_B - \sqrt{q\xi/\pi\varepsilon_i})}{kT}\right]$ with a voltage and

temperature dependence of $\sim V \exp(+2a\sqrt{V}/T - q\phi_B/kT)$

Tunnel or field emission:

$J \sim \xi^2 \exp\left[-\frac{4\sqrt{2m^*}(2q\phi_B)^{3/2}}{3q\hbar\xi}\right]$ with a voltage and

temperature dependence of $\sim V^2 \exp(-b/V)$

Ohmic conduction:

$J \sim \xi \exp(-\Delta E_{ae}/kT)$ with a voltage and temperature dependence of $\sim V \exp(-c/T)$

Ionic conduction:

$J \sim (\xi/T) \exp(-\Delta E_{ai}/kT)$ with a voltage and temperature dependence of $\sim \frac{V}{T} \exp(-d'/T)$

Where:

$A^*$ = effective Richardson constant, $\phi_B$ = barrier height, $\xi$ = electric field, $\varepsilon_i$ = insulator dynamic permittivity, $m^*$ = effective mass, d = insulator thickness, $\Delta E_{ae}$ = activation energy of electrons, $\hbar$ = reduced Planck constant, $\Delta E_{ai}$ = activation energy of ions, and $a \equiv \sqrt{q/(4\pi\varepsilon_i d)}$. $V = \xi d$, J = current density, V = terminal voltage. Positive constants independent of V or T are b, c, and d'.

**[00254]** The fabrication of the trapped charge memory element as described, being basically a multi-layered thin film structure with each film typically of a thickness less than 10 μm, includes (1) providing a substrate on which to first form the bottom electrode material, (2) forming or depositing the memory material with any of a variety of treatments or conditioning schemes, (3) forming or depositing the top electrode material, and, optionally (4) conditioning the structure with a variety of means. Some specific fabrication processes for the memory element include: Solution



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based spin on followed by high temperature anneal, pulsed laser deposition (PLD), sputtering, and metalorganic chemical vapor deposition (MOCVD).

**[00255]** Where one or both of the top electrode-to-memory material contact and the bottom electrode-to-memory material contact are made non-ohmic with the addition of diodes, the diodes can be (i) a PN junction diode made of amorphous, microcrystalline, polycrystalline or single crystal semiconductor (e.g. Si, Ge, SiGe, GaAs, InP, etc.); (ii) a metal-semiconductor Schottky diode; (iii) a junction field-effect transistor with gate connected to source (or to drain); (iv) a MOSFET with gate either floating, or connected to source or connected to drain; (v) a Zener diode, avalanche diode, or tunnel diode; (vi) a four-layer diode (SCR); (vii) a P-I-N diode made of amorphous, microcrystalline, polycrystalline or single crystal semiconductor. Yet another implementation comprises a metal-insulator-metal (MIM) tunneling device.

***Concluding Remarks***

**[00256]** Although the invention has been described in its presently contemplated best mode, it is clear that it is susceptible to numerous modifications, modes of operation and embodiments, all within the ability and skill of those familiar with the art and without exercise of further inventive activity. For example, some techniques can be applied to other types of memories that switch fast with a relatively low current or amount of charge, such as chalcogenide, silver dendrite, molecular, polymer or organic memories. Accordingly, that which is intended to be protected by Letters Patent is set forth in the claims and includes all variations and modifications that fall within the spirit and scope of the claim.



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## CLAIMS

*What is claimed is:*

1. A memory comprising:

an array of non-volatile memory cells, each memory cell including a two terminal memory plug that switches from a first resistance state to a second resistance state upon application of a first write voltage of a first polarity and reversibly switches from the second resistance state to the first resistance state upon application of a second write voltage of polarity opposite to the first polarity;

a control bus that carries signals indicative of whether a read operation or a write operation is desired;

an address bus that carries signals indicative of a particular memory cell or a particular group of memory cells;

a data bus that carries signals indicative of information relating to the particular memory cell or the particular group of memory cells;

peripheral circuitry that decodes the signals on the address bus and,

if the control bus carries signals indicative of a write operation, places the particular memory cell or the particular group of selected memory cells into resistive states that correspond to the signals on the data bus; and

if the control bus carries signals indicative of a read operation, places signals on the data bus that correspond to the resistance states of the selected memory cell or the group of selected memory cells.

2. The memory of claim 1, wherein the peripheral circuitry includes buffers that store data signals.

3. The memory of claim 1, wherein the memory is capable of storing at least a megabit of information and having an access time of not more than 100 nanoseconds

4. The memory of claim 1, wherein the memory plug includes a conductive metal oxide.

5. The memory of claim 4, wherein the conductive metal oxide is a perovskite.

6. The memory of claim 4, wherein a reactive metal is deposited such that it comes into contact with the conductive metal oxide.

7. The memory of claim 1, wherein the array is a cross-point array.

8. The memory of claim 7, wherein the cross point array is a stacked cross point array that has multiple memory plug layers.



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9. The memory of claim 8, wherein at least two memory plug layers share a conductive array line layer.

10. The memory of claim 7, 8 or 9, wherein the memory plug exhibits a very high resistance for a range of voltages between a third voltage of a first polarity and a fourth voltage of polarity opposite to the first polarity, the first write voltage having a greater magnitude than the third voltage and the second write voltage having a greater magnitude than the fourth voltage.

11. The memory of claim 10, wherein the cross point array can be accessed in page mode.

12. The memory of claim 10, wherein the cross point array can be accessed in burst mode.

13. The memory of claim 10, wherein at least a portion of the peripheral circuitry is underneath the cross point array.

14. The memory of claim 10, wherein the peripheral circuitry includes x-direction select circuitry and y-direction select circuitry.

15. The memory of claim 14, wherein the x-direction select circuitry includes drivers that receive inputs from a primary decoder, a secondary decoder and a reference.

16. The memory of claim 15, wherein the drivers share nodes with other drivers.

17. The memory of claim 1, wherein the array is a single transistor array such that each memory cell includes a semiconductor device in series with the memory plug.

18. The memory of claim 17, wherein the semiconductor device is a transistor that controls current flow through its memory cell depending on the voltage of a select line that is controlled by decoded address bus signals.

19. The memory of claim 18, wherein one terminal of the memory plug is in electrical contact with a reference voltage.

20. The memory of claim 19, wherein two adjacent memory cells share a reference voltage.

21. A memory comprising:

an array of non-volatile memory cells capable of storing at least a megabit of information and having an access time of not more than 100 nanoseconds, each memory cell including a two terminal memory plug that switches from a first resistance state to a second resistance state upon application of a first write voltage of a first polarity and reversibly switches from the second resistance state to the first



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resistance state upon application of a second write voltage of polarity opposite to the first polarity; and

peripheral circuitry operable to deliver either the first write voltage or the second write voltage to a selected memory cell or a group of selected memory cells, the peripheral circuitry additionally being operable to determine the resistance states of a memory cell or a group of memory cells.

22. The memory of claim 21 wherein the peripheral circuitry includes buffers that store information.

23. A memory comprising:

an array of non-volatile memory cells, each memory cell including a two terminal memory plug that is capable of exhibiting a range of resistances, the memory plug operable to

undergo an increase in resistance upon application of a voltage pulse of a first polarity,

undergo a decrease in resistance upon application of a voltage pulse of a polarity opposite to the first polarity, and

experience no significant change in resistance upon application of a read voltage pulse; and

peripheral circuitry operable to

select a memory cell or a group of memory cells,

apply a read voltage pulse to the selected cell or group of cells to determine stored information, and

deliver at least one voltage pulse that is operable to change the resistance of the at least one of the selected cells if a write operation is desired and if at least one of the selected cells does not have a desired resistance,.

24. The memory of claim 23, wherein each memory cell can be written to at least four distinct resistances within the range of resistances.

25. The memory of claim 23, wherein the memory is formed on the substrate that includes microprocessor circuitry.

26. The memory of claim 23, further comprising:

a control bus that carries a write enable signal pulse when a write is desired, the write enable signal pulse having a end;

an address bus that carries signals indicative of a particular memory cell or a particular group of memory cells; and



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a data bus that carries signals indicative of information relating to the particular memory cell or the particular group of memory cells;

wherein the peripheral circuitry does not deliver the at least one voltage pulse that is operable to change the resistance of the at least one of the selected cells until after the write enable signal pulse has ended.

27. The memory of claim 23, 24, 25 or 26 wherein the memory plug includes island formations of one material within the bulk of a second, more insulating material.



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## AMENDED CLAIMS

**[Received by the International Bureau on 23 May 2005 (23.05.2005): original claims 1-27 replaced by new claims 28-54; (9 pages)]**

28. A non-volatile memory, comprising:

a plurality of x-direction conductive array lines and a plurality of y-direction conductive array lines;

a plurality of two-terminal memory plugs, wherein the conductive array lines cross one another in a substantially orthogonal orientation and the memory plugs are positioned at intersections of the conductive array lines forming a cross point memory array, each memory plug including

(i) a first electrode connected with one of the x-direction conductive array lines,

(ii) a second electrode connected with one of the y-direction conductive array lines,

(iii) at least one layer of a conductive oxide positioned between and in electrical communication with the first and second electrodes that can be written from a first state exhibiting a first I-V curve to a second state exhibiting a second I-V curve that is different from the first I-V curve by applying a first write voltage pulse of a first polarity and reversible written from the second state to the first state by applying a second write voltage pulse of a second polarity opposite to the first polarity, the conductive oxide does not experience a change in state when subjected to read voltage pulse that is lower in magnitude than either write voltage pulse, and the conductive oxide does not experience a change in state in the absence of electrical power, and

(iv) a non-ohmic device positioned between and in electrical communication with the first and second electrodes and operable to impart a high resistance for half-selected memory plugs and operable to impart a low resistance to selected memory plugs; and



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a substrate including active circuitry in electrical communication with the conductive array lines and operable to drive the cross point memory array, the cross point array being formed on the substrate, and the substrate being positioned beneath the cross point array.

29. The non-volatile memory as set forth in Claim 28, wherein the conductive oxide comprises a perovskite.

30. The non-volatile memory as set forth in Claim 28, wherein the non-ohmic device comprises a pair of back-to-back diodes.

31. The non-volatile memory as set forth in Claim 28, wherein the non-ohmic device comprises a plurality of thin film layers including at least one insulating layer and at least one conductive layer.

32. The non-volatile memory as set forth in Claim 31, wherein the plurality of thin film layers comprises a metal-insulator-metal structure including a first thin film layer of a conductive material, a thin film layer of an insulating material, and a second thin film layer of a conductive material.

33. The non-volatile memory as set forth in Claim 28, wherein the first and second electrodes comprise at least one layer of material selected from the group consisting of a metal, a refractory metal, a precious metal, and a conductive oxide.





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34. The non-volatile memory as set forth in Claim 33, wherein the at least one layer of material operatively performs a function selected from the group consisting of a diffusion barrier, an adhesion layer, a glue layer, a seed layer, and a stress relief layer.

35. The non-volatile memory as set forth in Claim 28, wherein the at least one layer of the conductive oxide comprises a first conductive metal oxide layer and a second conductive metal oxide layer that are made from the same type of material and the first and second layers are doped with different concentrations of the same type of dopant.

36. The non-volatile memory as set forth in Claim 28, wherein the at least one layer of the conductive oxide comprises a conductive metal oxide layer, a top conductive metal oxide layer, and a bottom conductive metal oxide layer that are made from substantially similar materials, the conductive metal oxide layer is positioned between the top and bottom conductive metal oxide layers, and the top and bottom conductive metal oxide layers are doped with dopants having an opposite mobile carrier type.

37. The non-volatile memory as set forth in Claim 28, wherein the active circuitry further comprises:



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an adaptive programming circuit including a detector coupled with a memory plug selected for a write operation and operative to detect a resistive state of the memory plug and to output an indicating signal indicative of the resistive state, a controller coupled with the detector and operative to detect a write command and a write-data, the controller compares the indicating signal with the write data and generates an activating signal only when there is a non-correspondence between the indicating signal and the write-data, and a driver coupled with the controller and the memory plug and operative drive the memory plug to a desired resistive state indicative of the write-data in response to the activating signal.

38. The non-volatile memory as set forth in Claim 28, wherein at least a portion of the active circuitry is positioned beneath the cross point array.

39. The non-volatile memory as set forth in Claim 38 and further comprising:

a plurality of x-direction drivers sets operable to drive specific x-direction conductive array lines;

and a plurality of y-direction drivers sets operable to drive specific y-direction conductive array lines.

40. The non-volatile memory as set forth in Claim 39, wherein the x-direction and y-direction driver sets are a selected one of interdigitated or non-interdigitated.



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41. The non-volatile memory as set forth in Claim 28, wherein the cross point array is a stacked cross point array that includes multiple memory plug layers.

42. The non-volatile memory as set forth in Claim 41, wherein at least two memory plug layers share the plurality of y-direction conductive array lines or the plurality of the y-direction conductive array lines.

43. A memory device, comprising:

a plurality of x-direction conductive array lines;

a plurality of y-direction conductive array lines;

a plurality of two-terminal memory plugs, wherein the conductive array lines cross one another in a substantially orthogonal orientation and the memory plugs are positioned at intersections of the conductive array lines forming a cross point memory array, each memory plug including

(i) a first electrode connected with one of the x-direction conductive array lines,

(ii) a second electrode connected with one of the y-direction conductive array lines,

(iii) at least one layer of a conductive oxide positioned between and in electrical communication with the first and second electrodes that can be written from a first state exhibiting a first I-V curve to a second state exhibiting a second I-V curve that is different from the first I-V curve by applying a first write voltage pulse of a first polarity and reversible written from the second state to the first state by applying a second write voltage pulse of a second polarity opposite to the first polarity, the conductive oxide does not experience a change in state when subjected to read voltage pulse that is lower in magnitude than either write voltage pulse, and the conductive oxide does not experience a change in state in the absence of electrical power, and

(iv) a non-ohmic device positioned between and in electrical communication with the first and second electrodes and operable to impart a high resistance for half-



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selected memory plugs and operable to impart a low resistance to selected memory plugs; and

a substrate including peripheral circuitry in electrical communication with the conductive array lines and operable to apply the first and second write voltage pulses and the read voltage pulse, and to select at least one memory plug, apply the read voltage pulse to the selected memory plug to determine a resistive state of the memory plug, and apply the write voltage pulses to change the resistive state of the memory plug if a write operation to the memory plug is desired and if a write-data associated with the write operation will change the resistive state of the selected memory plug, and

the cross point array is formed on the substrate and the substrate is positioned beneath the cross point array.

44. The memory device as set forth in Claim 43, wherein the substrate the cross point array is formed on includes a microprocessor fabricated on the substrate.

45. The memory device as set forth in Claim 43 and further comprising:

a control bus that carries a write enable signal pulse when a write operation to the cross point array is desired, the write enable signal pulse having an end;

an address bus that carries signals indicative of a selected memory plug or a group of selected memory plugs; and

a data bus that carries signals indicative of a write-data relating to the selected memory plug or the group of selected memory plugs, and

wherein the peripheral circuitry does not apply the first and second write voltage pulses that are operable to change the resistive state of the selected memory



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plug or the group of selected memory plugs until after the write enable signal pulse has ended.

46. The memory device as set forth in Claim 43, wherein data is read from or written to the cross point array in a mode selected from the group consisting of a page mode and a burst mode.

47. The non-volatile memory as set forth in Claim 43, wherein the conductive oxide comprises a perovskite.

48. A non-volatile re-writeable memory cell, comprising:

a memory plug including a first electrode and a second electrode,

at least one layer of a conductive oxide positioned between and in electrical communication with the first and second electrodes that can be written from a first state exhibiting a first I-V curve to a second state exhibiting a second I-V curve that is different from the first I-V curve by applying a first write voltage pulse of a first polarity and reversible written from the second state to the first state by applying a second write voltage pulse of a second polarity opposite to the first polarity, the conductive oxide does not experience a change in state when subjected to read voltage pulse that is lower in magnitude than either write voltage pulse, and the conductive oxide does not experience a change in state in the absence of electrical power, and

a non-ohmic device positioned between and in electrical communication with the first and second electrodes and operable to impart a high resistance to the memory





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plug when the memory plug is not selected for a read operation or a write operation and operable to impart a low resistance to the memory plug when the memory plug is selected for the read operation or the write operation.

49. The non-volatile memory as set forth in Claim 48, wherein the conductive oxide comprises a perovskite.

50. The non-volatile memory as set forth in Claim 48, wherein the non-ohmic device comprises a pair of back-to-back diodes.

51. The non-volatile memory as set forth in Claim 48, wherein the non-ohmic device comprises a plurality of thin film layers including at least one insulating layer and at least one conductive layer.

52. The non-volatile memory as set forth in Claim 51, wherein the plurality of thin film layers comprises a metal-insulator-metal structure including a first thin film layer of a conductive material, a thin film layer of an insulating material, and a second thin film layer of a conductive material.

53. The non-volatile memory as set forth in Claim 48, wherein the first and second electrodes comprise at least one layer of material selected from the group consisting of a metal, a refractory metal, a precious metal, and a conductive oxide.





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54. The non-volatile memory as set forth in Claim 53, wherein the at least one layer of material operatively performs a function selected from the group consisting of a diffusion barrier, an adhesion layer, a glue layer, a seed layer, and a stress relief layer.



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## STATEMENT

The prior art cited in the International Search Report and as set forth in the Written Opinion of the International Searching Authority (i.e. references D1, D2, and D3) do not identically describe or render obvious to the skilled man the features as now recited in new independent **Claims 28, 43,** and **48** or the claims that depend from those independent claims.

Accordingly, the Applicant respectfully submits that the claims of the present application are novel, non-obvious, and constitute an inventive step over the prior art as is required by **Article 33(1) PCT, Article 33(2) PCT,** and **Article 33(3) PCT.**

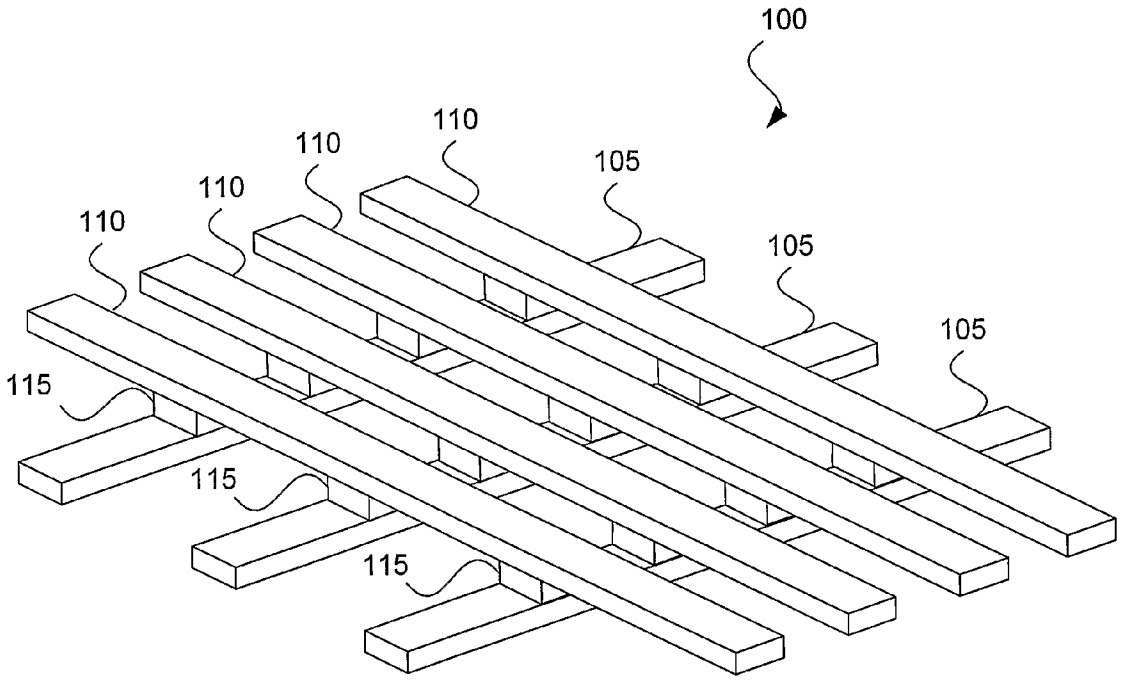



FIG. 1

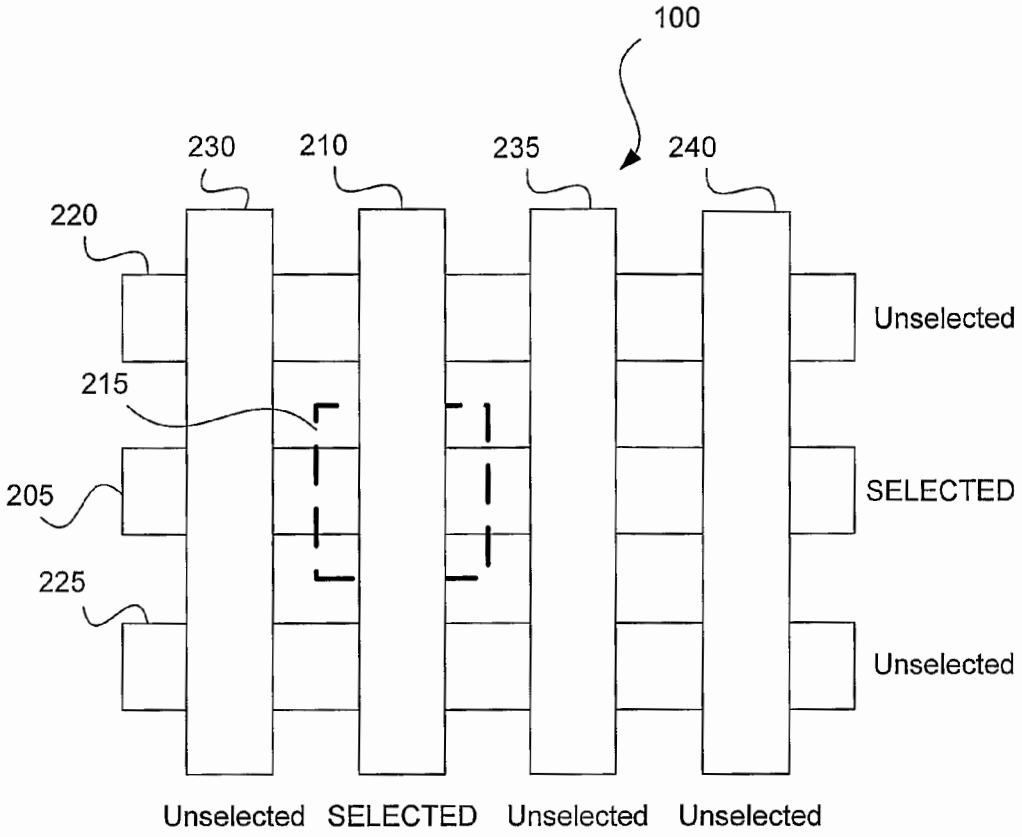
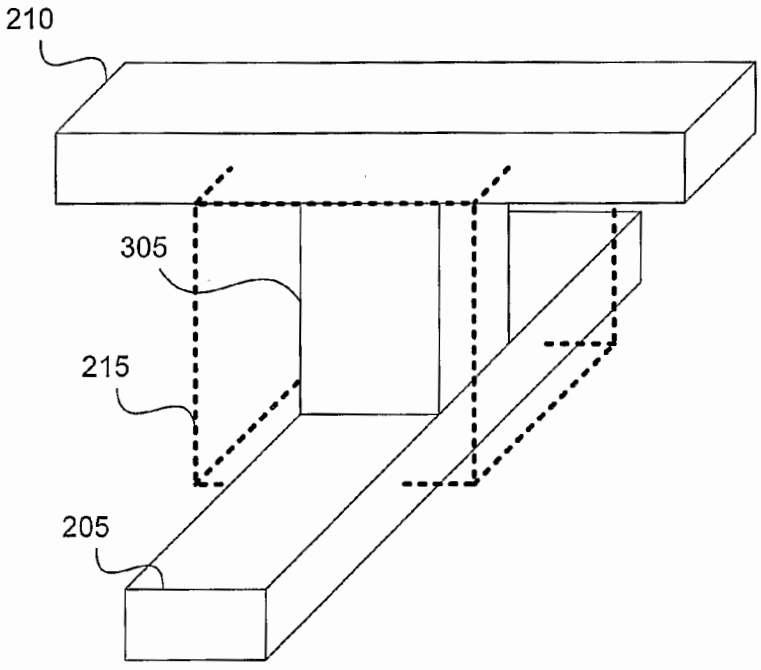

100
230
210
235
240
220
Unselected
215
205
SELECTED
225
Unselected
Unselected
SELECTED
Unselected
Unselected

FIG. 2


210
305
215
205

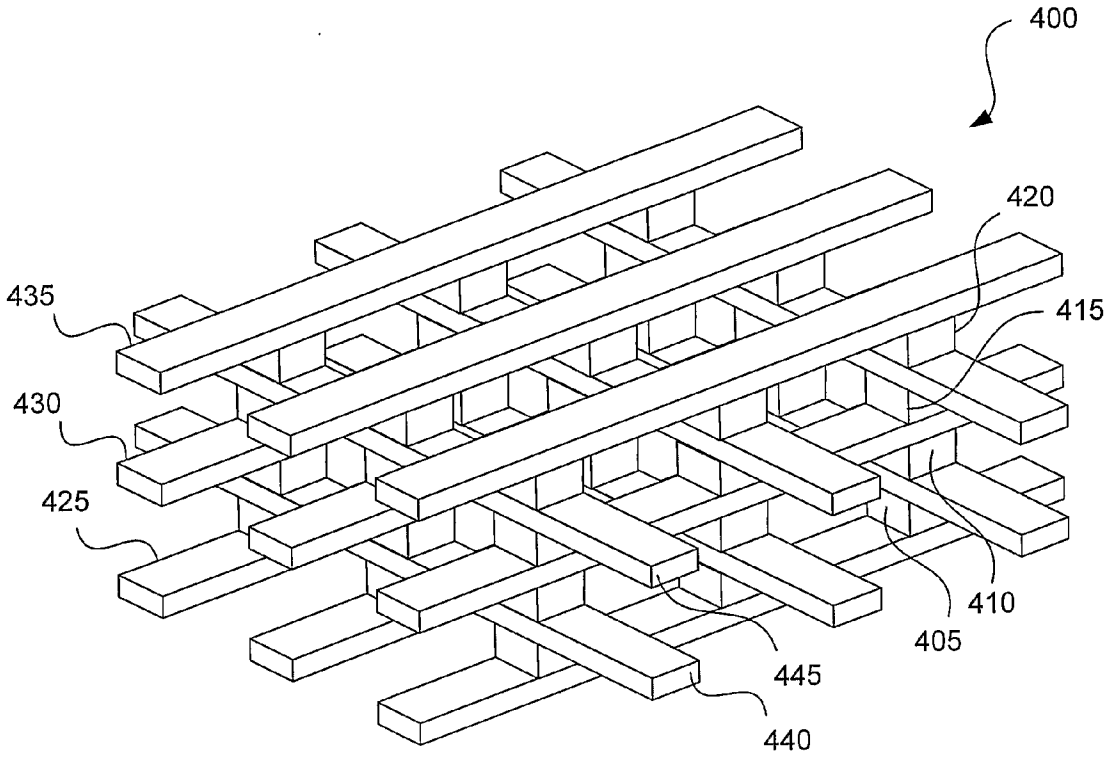

400
420
435
415
430
425
410
405
445
440

FIG. 4A

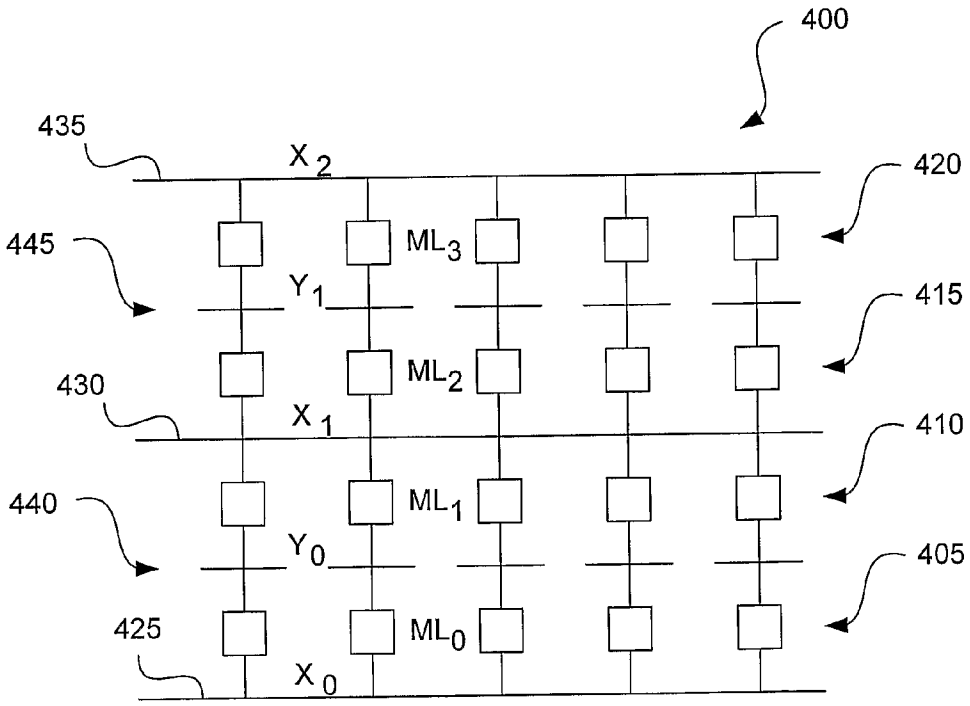

400
435
$X_2$
420
445
$ML_3$
$Y_1$
415
$ML_2$
430
$X_1$
410
440
$ML_1$
$Y_0$
405
425
$ML_0$
$X_0$

FIG. 4B

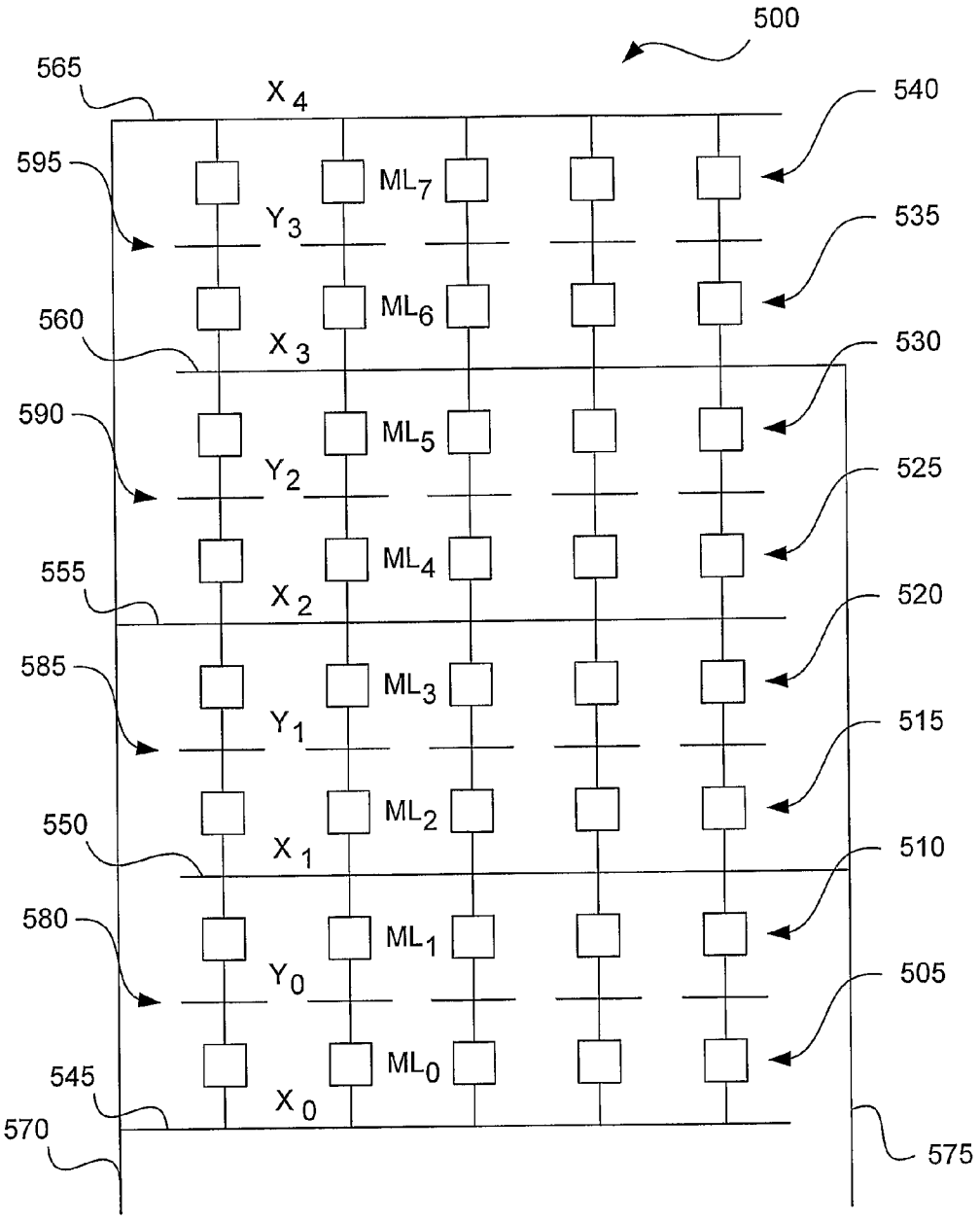

500
565
X4
540
595
ML7
Y3
535
ML6
560
X3
530
590
ML5
Y2
525
ML4
555
X2
520
585
ML3
Y1
515
ML2
550
X1
510
580
ML1
Y0
505
ML0
545
X0
570
575

FIG. 5

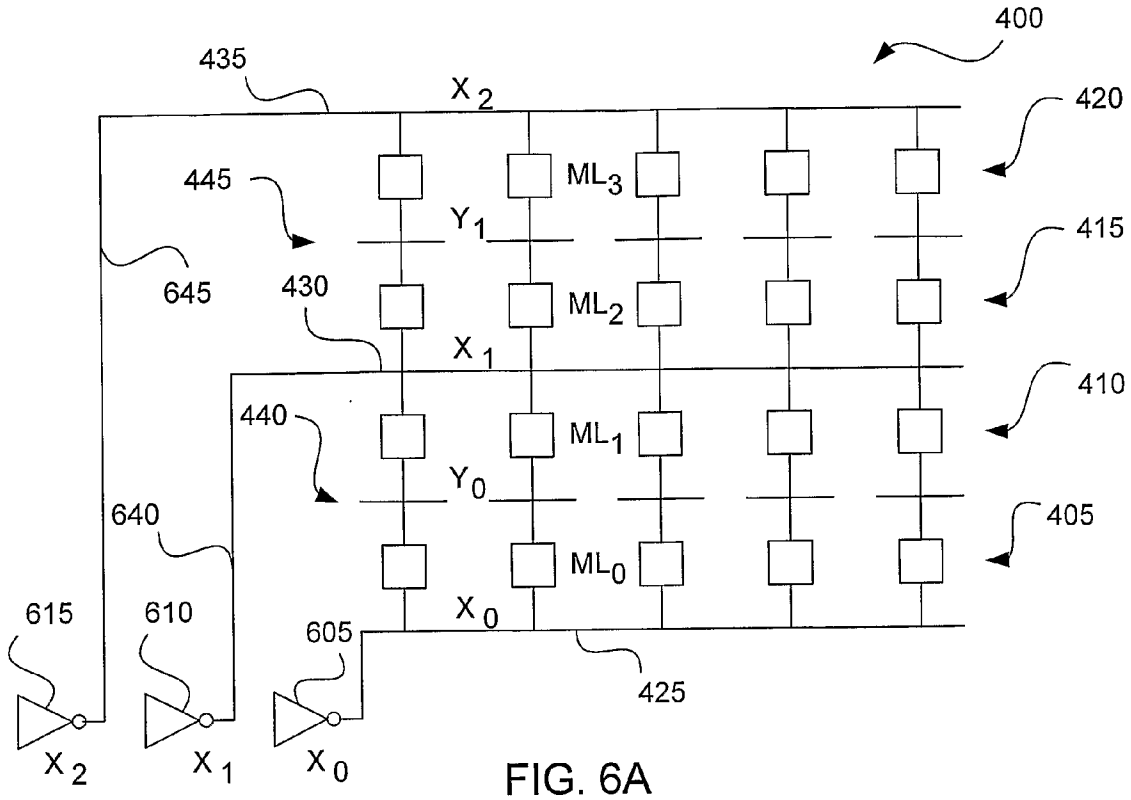

400
435
X2
420
445
ML3
Y1
415
645
430
ML2
X1
410
440
ML1
Y0
640
405
ML0
615
610
605
X0
425
X2
X1
X0

FIG. 6A

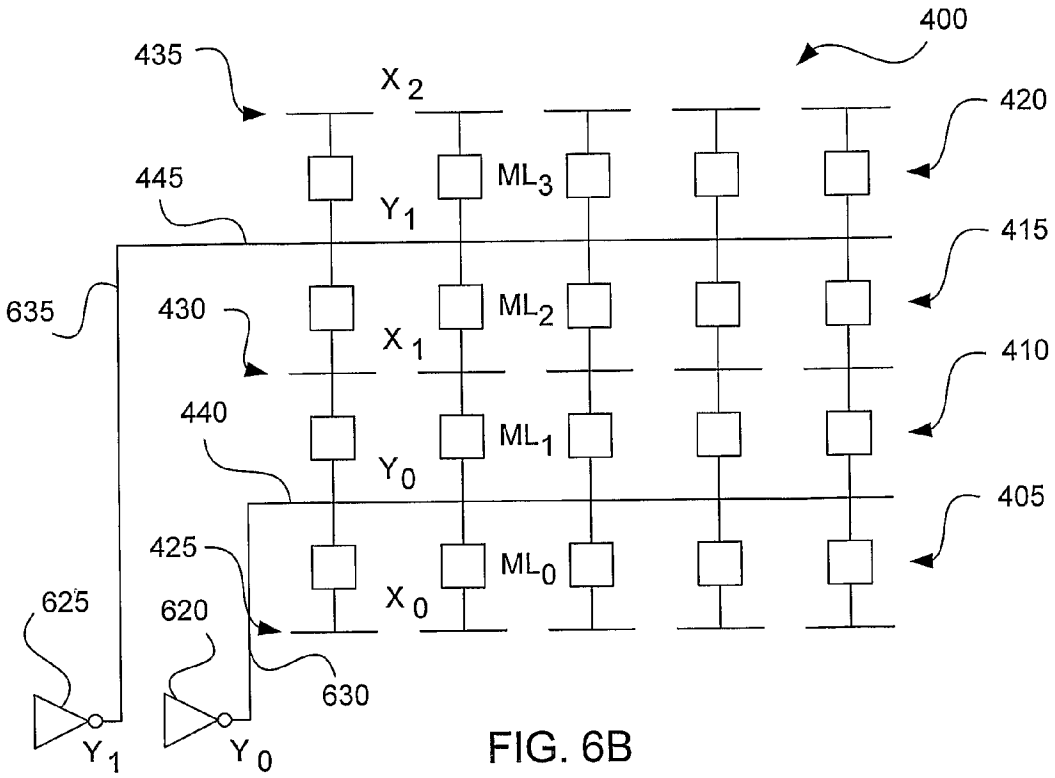

400
435
X2
420
445
ML3
Y1
415
635
430
ML2
X1
410
440
ML1
Y0
405
425
ML0
625
620
X0
630
Y1
Y0

FIG. 6B

FIG. 7B




FIG. 7A






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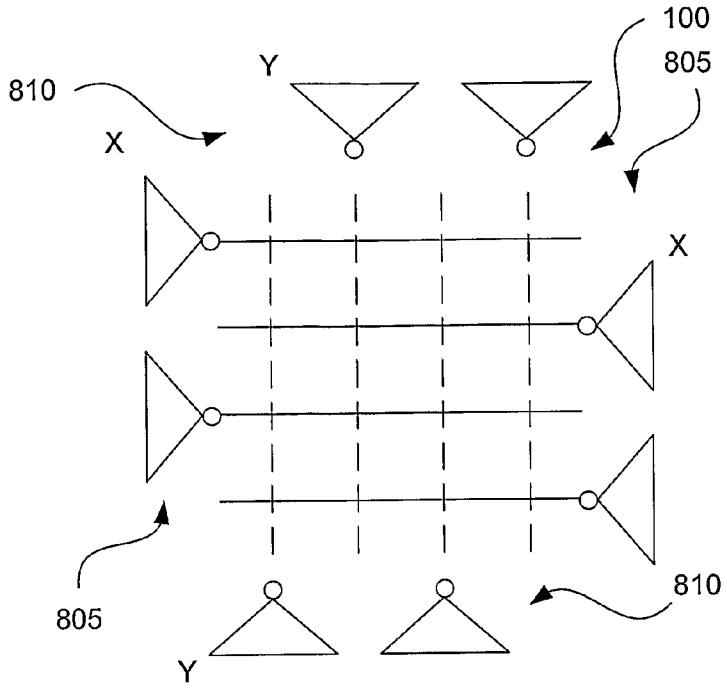



FIG. 8A

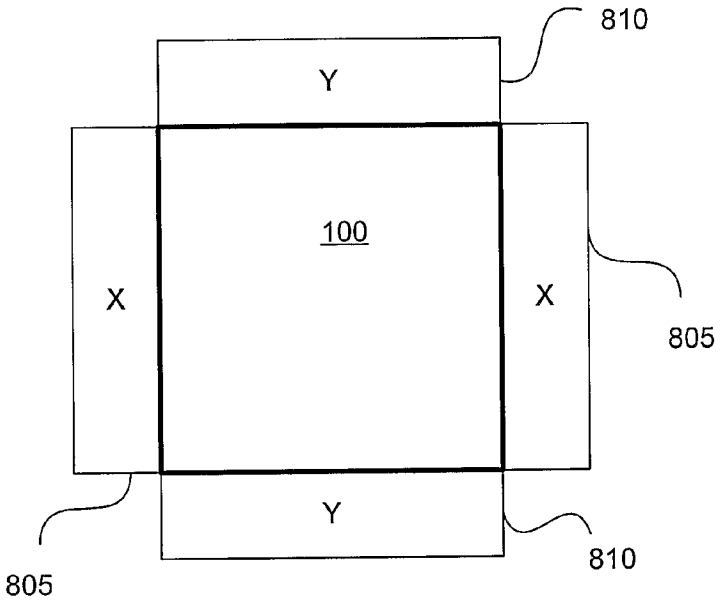



FIG. 8B

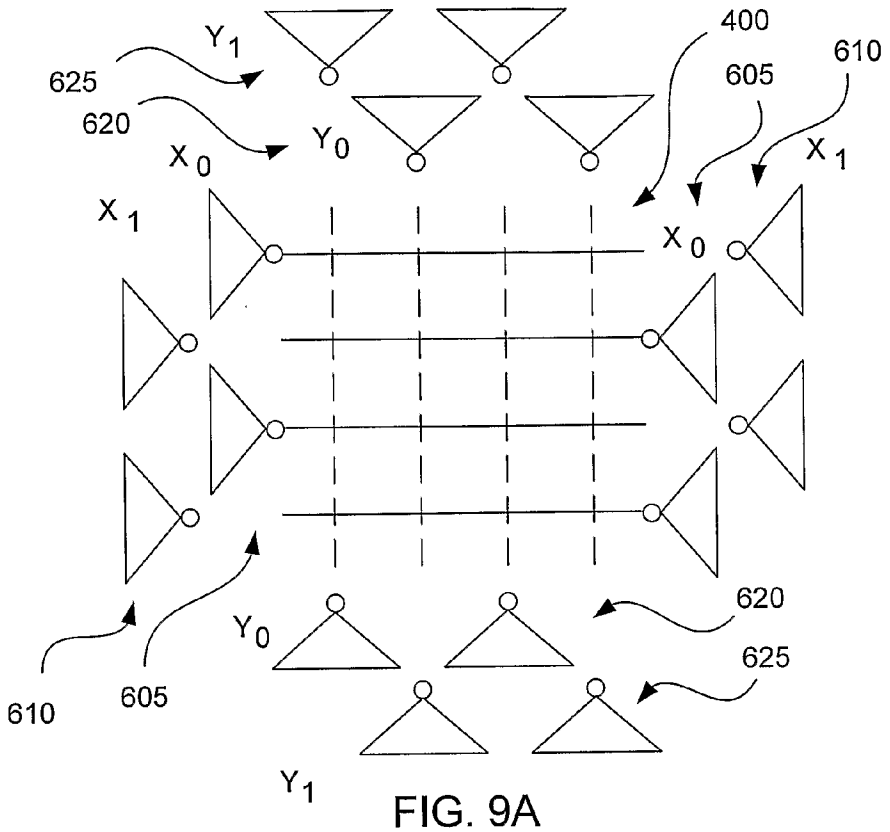

Y1
625
620
X0
Y0
400
610
605
X1
X1
X0
620
Y0
625
610
605
Y1

FIG. 9A

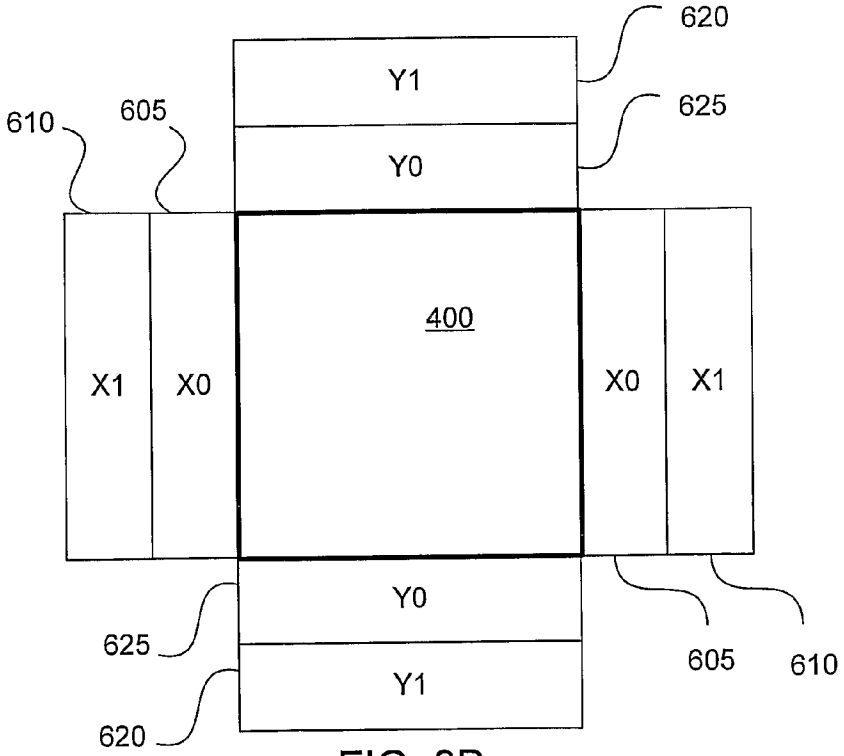

620
Y1
610
605
625
Y0
400
X1
X0
X0
X1
Y0
625
605
610
Y1
620

FIG. 9B

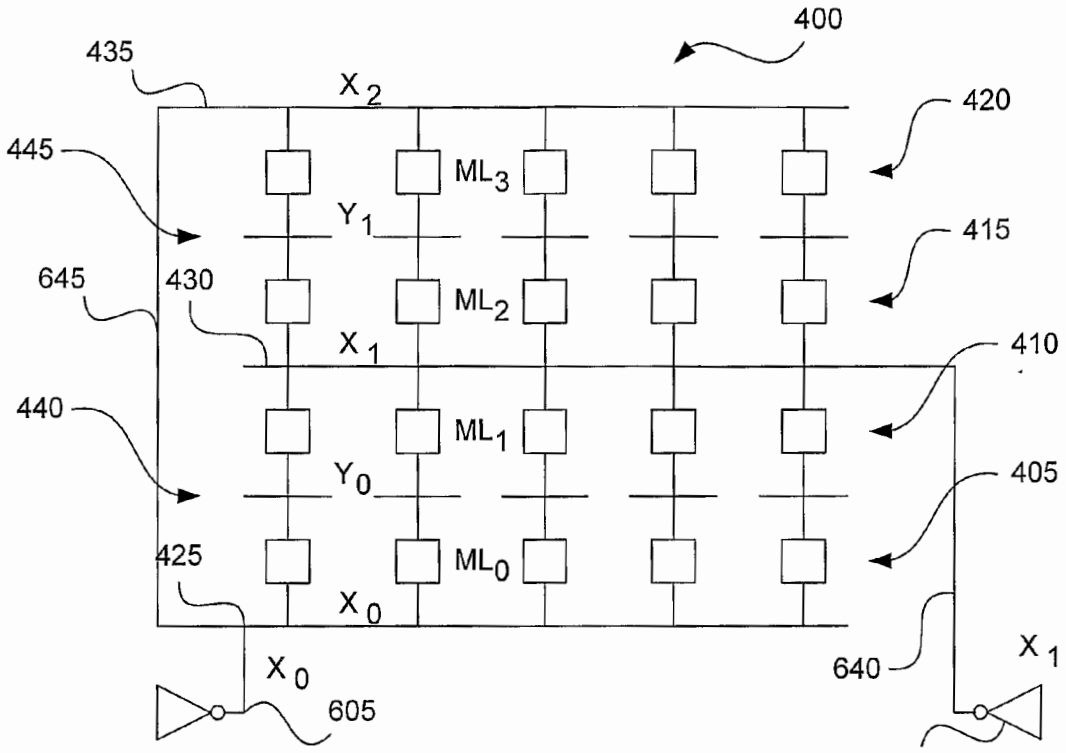



FIG. 10A

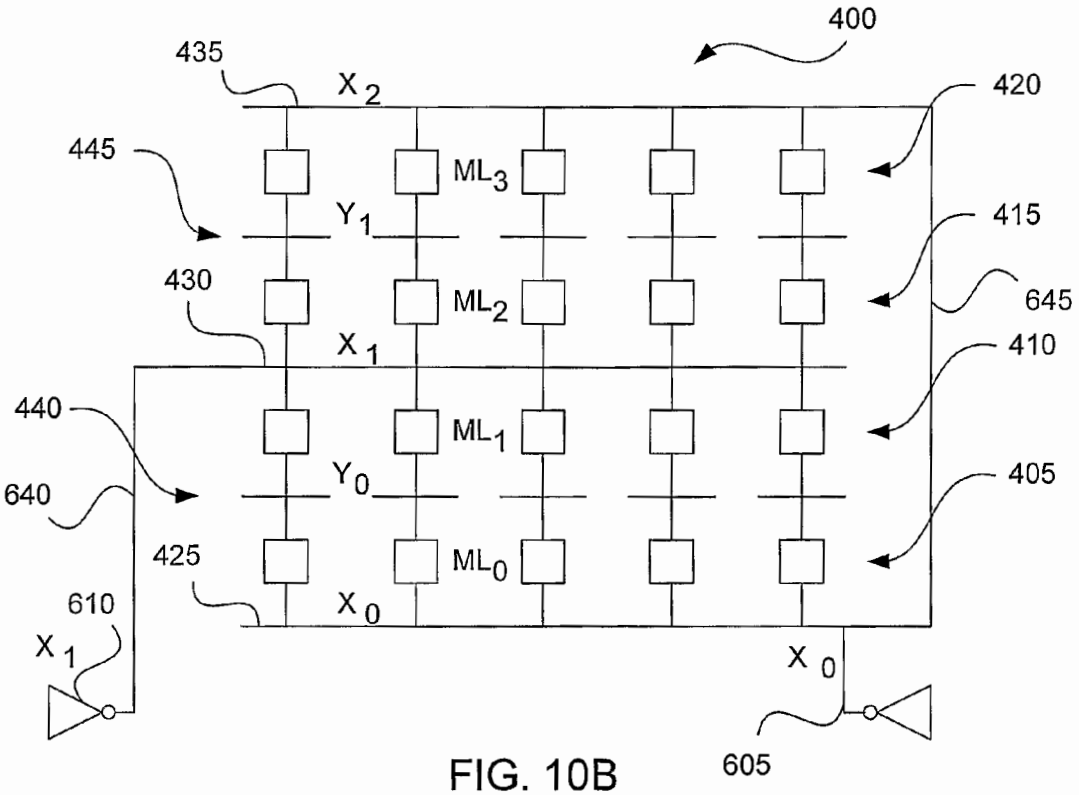



FIG. 10B

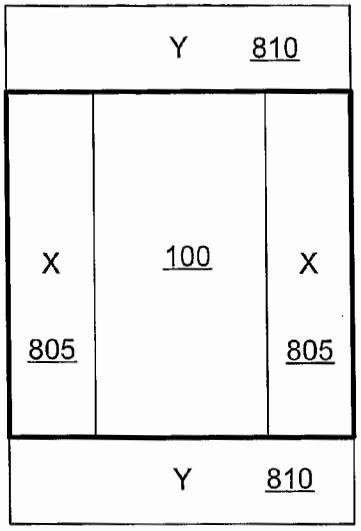



FIG. 11A

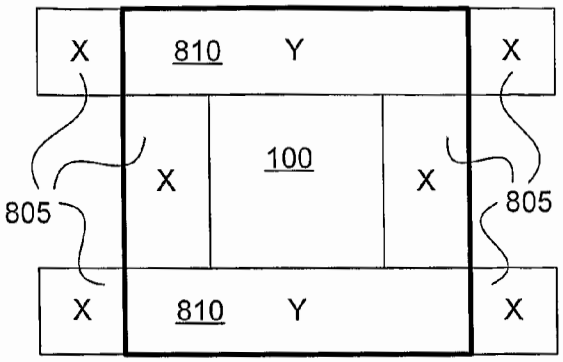



FIG. 11B

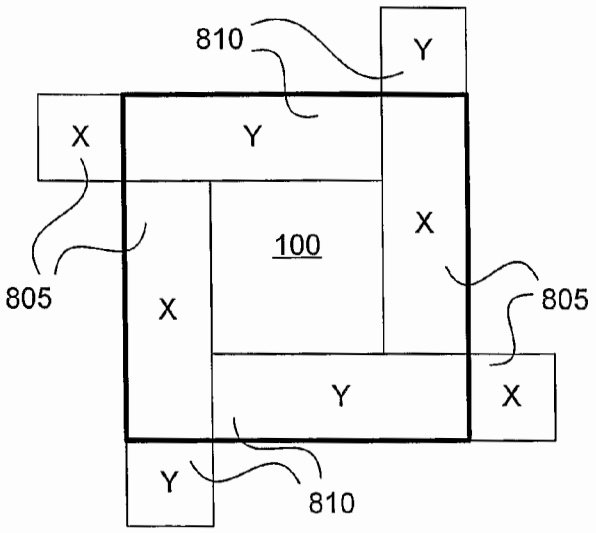



FIG. 11C

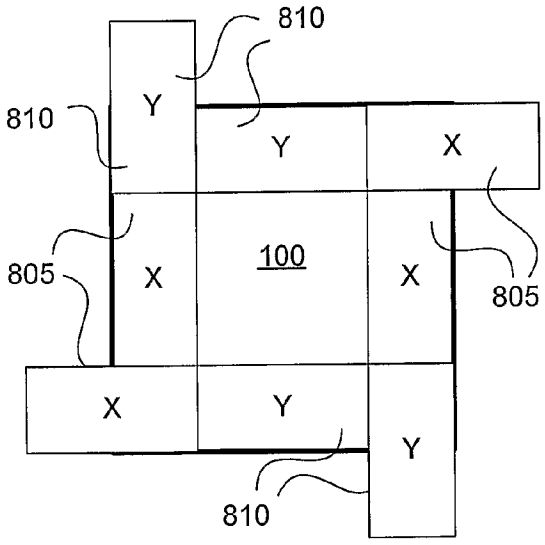



FIG. 12

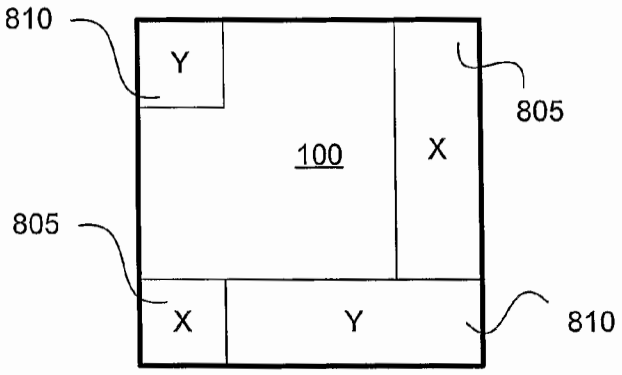



FIG. 13A

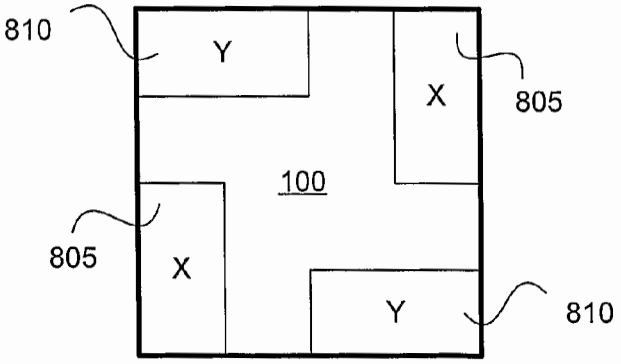



FIG. 13B

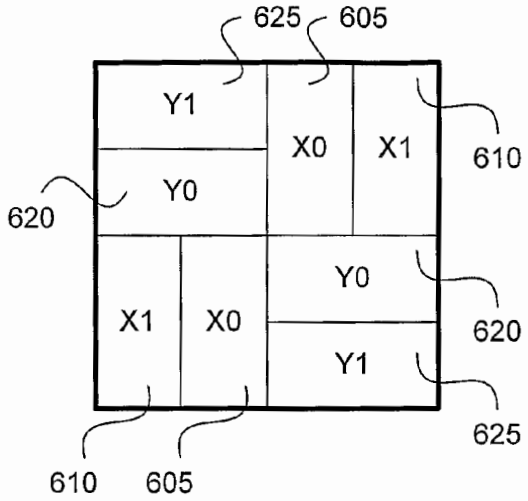



FIG. 14A

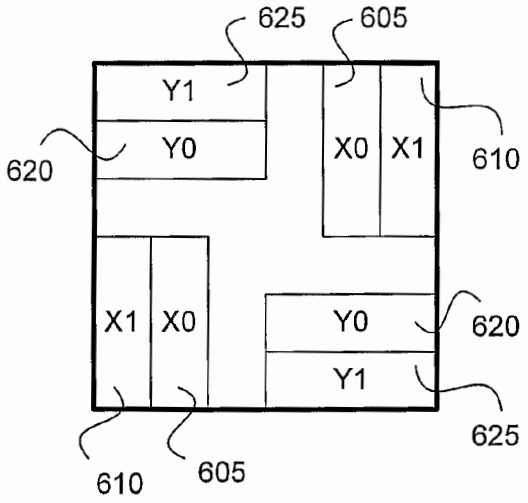



FIG. 14B

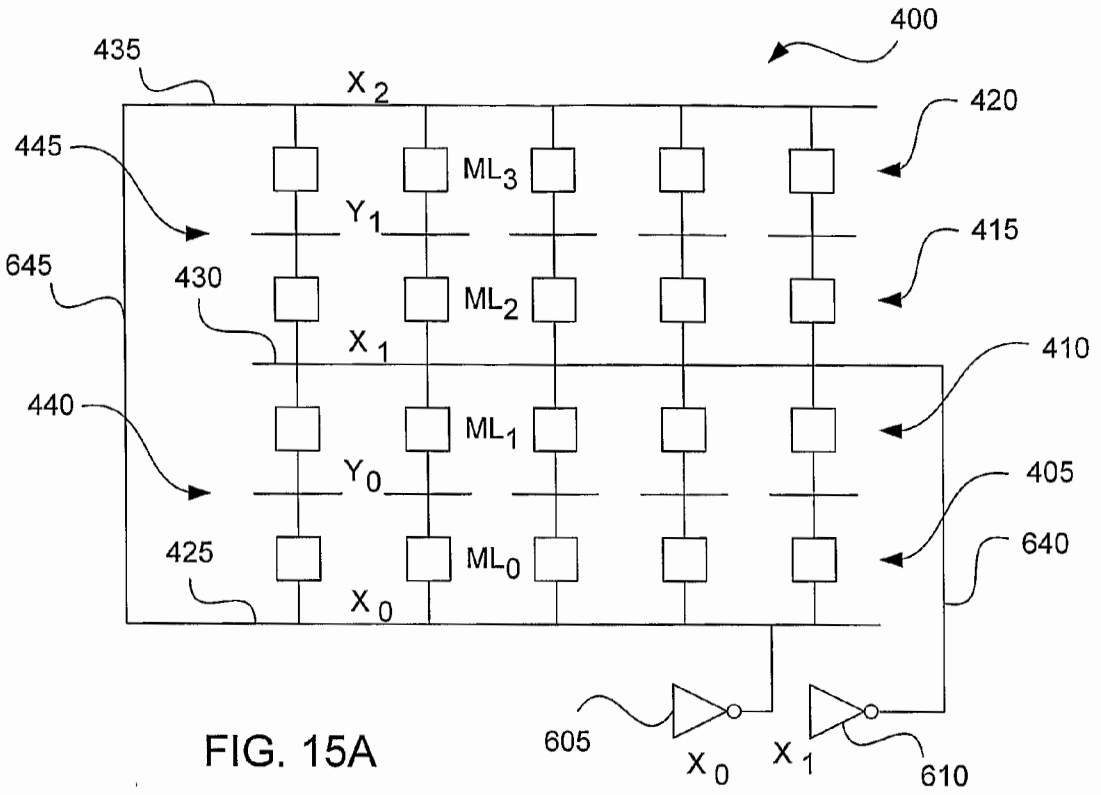



FIG. 15A

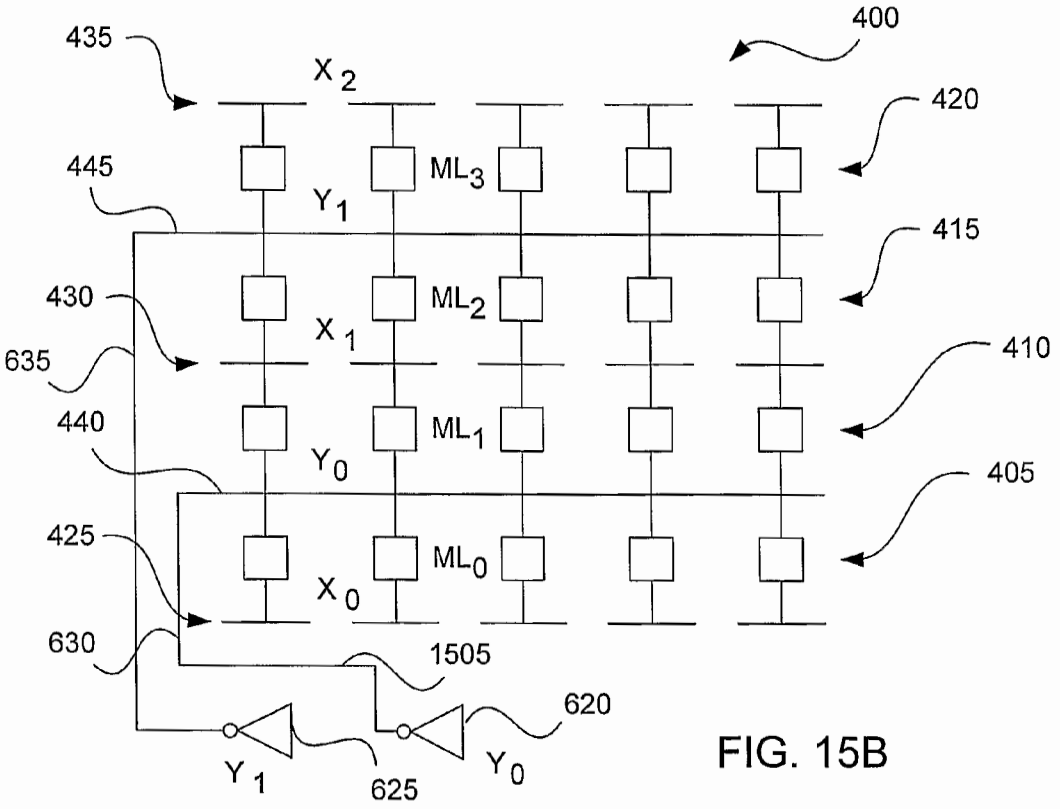



FIG. 15B

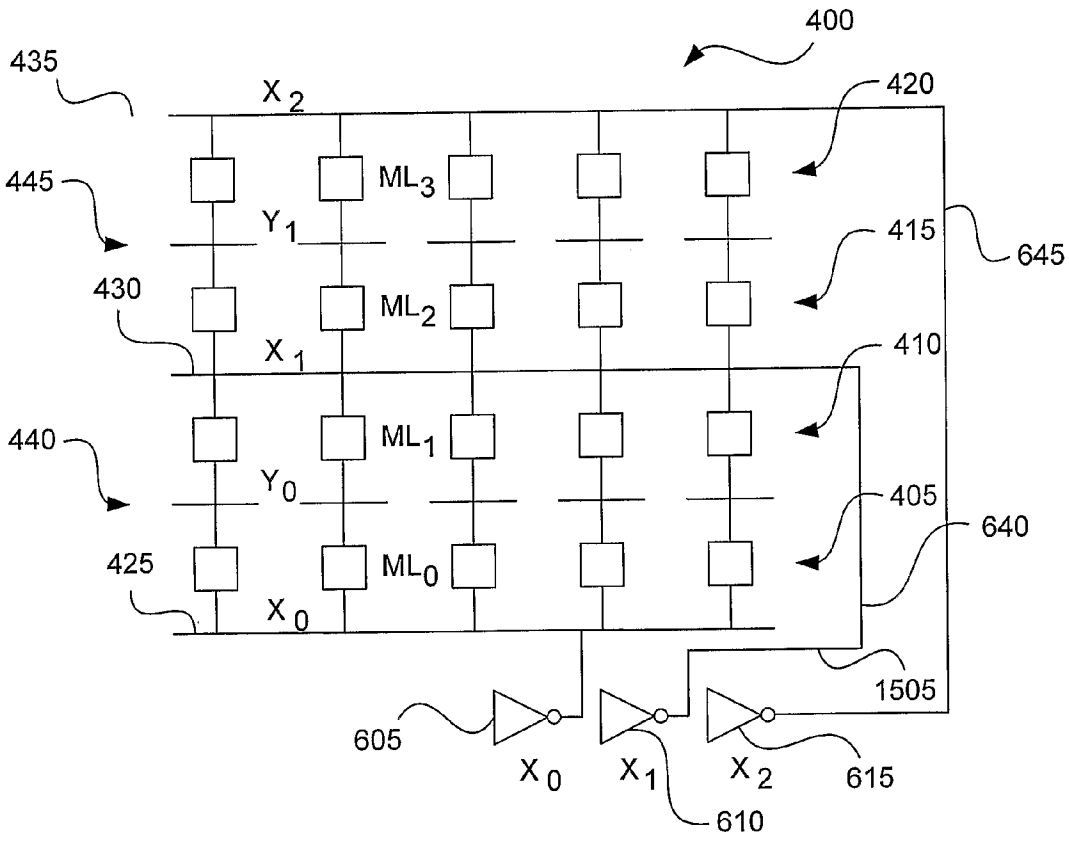

400
435
X 2
420
445
ML3
Y 1
415
645
430
ML2
X 1
410
440
ML1
Y0
405
640
425
ML0
X 0
1505
605
X 0
X 1
X 2
615
610

FIG. 16

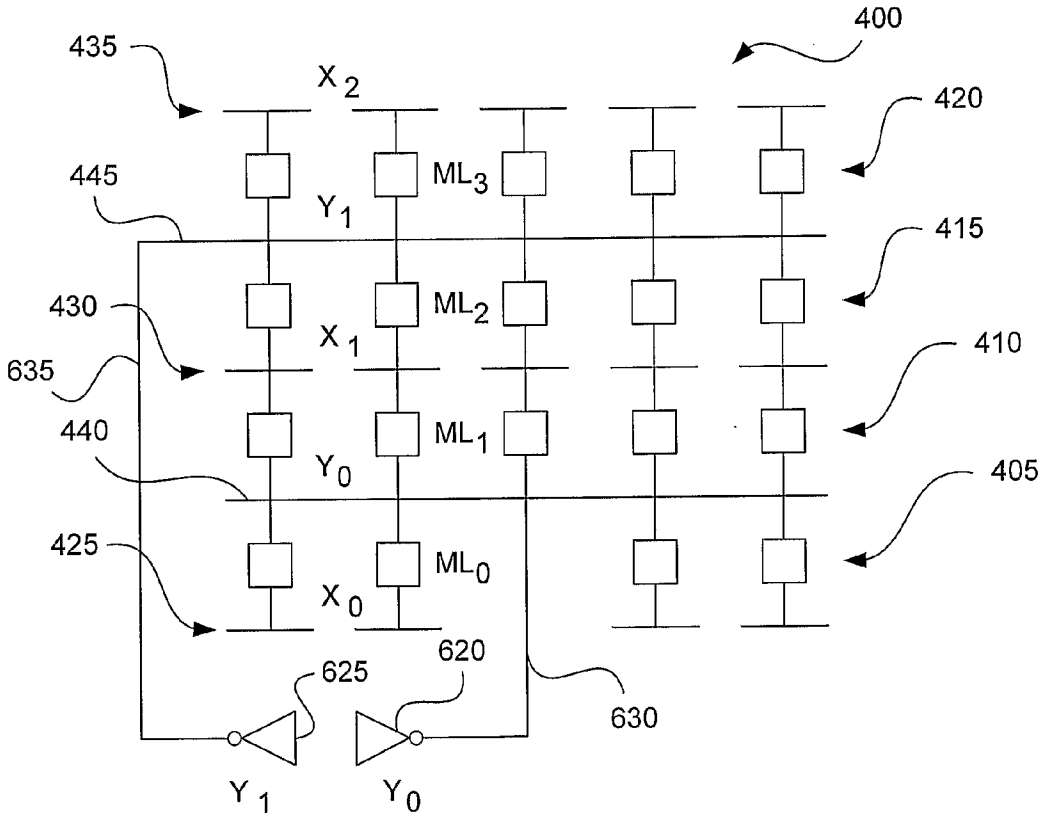

400
435
X 2
420
445
ML3
Y1
415
430
ML2
X 1
410
635
440
ML1
Y0
405
425
ML0
X 0
620
625
630
Y 1
Y 0

FIG. 17

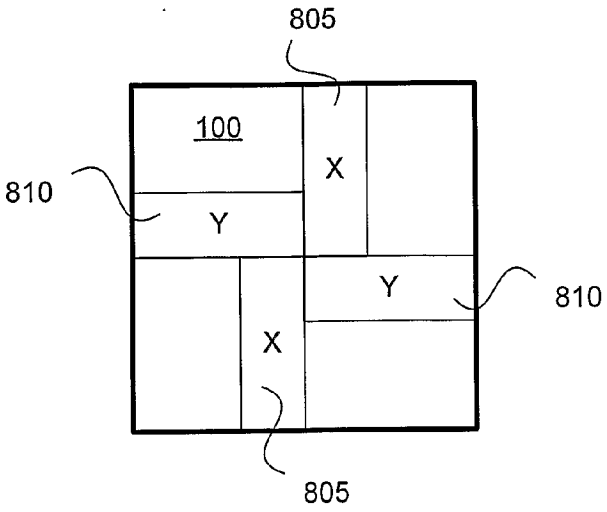



FIG. 18A

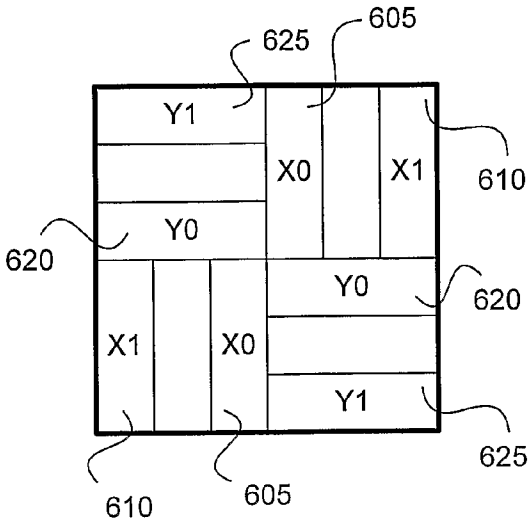



FIG. 18B

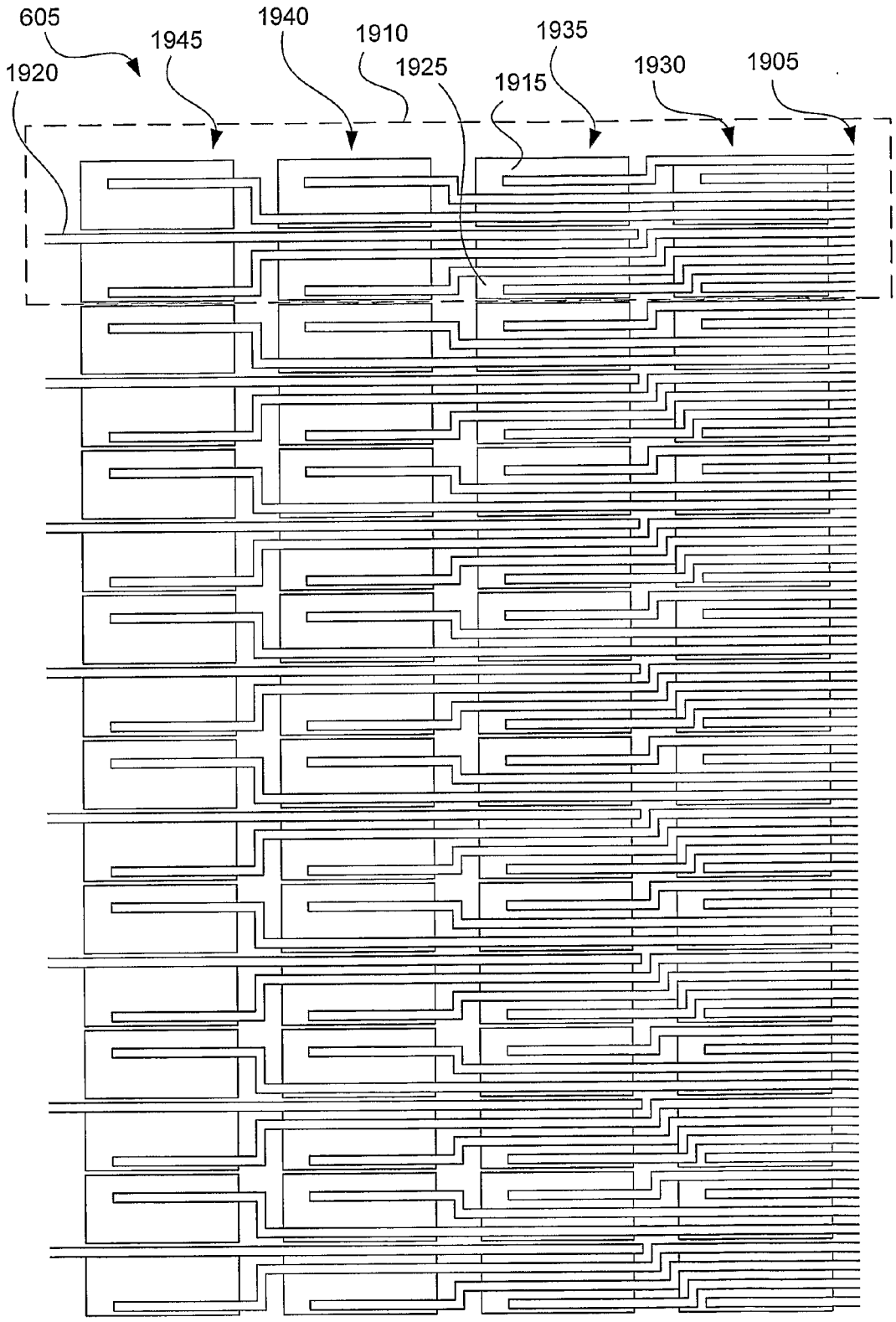



FIG. 19

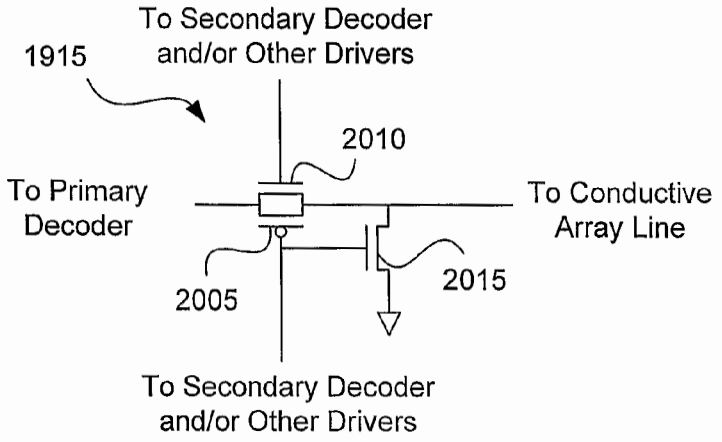



FIG. 20A

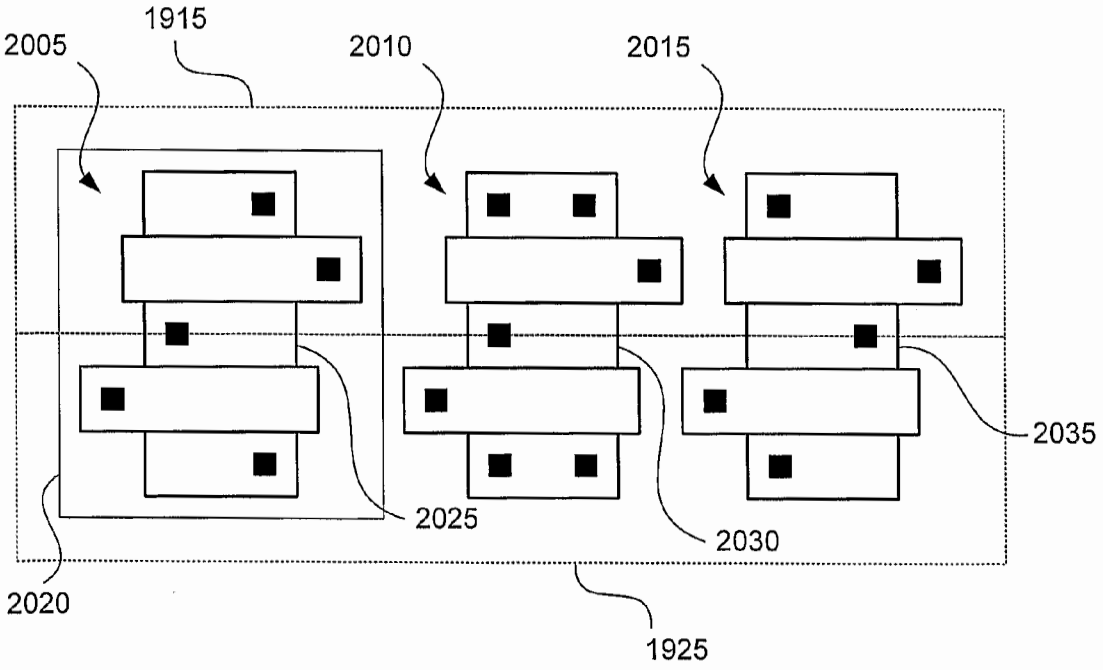



FIG. 20B

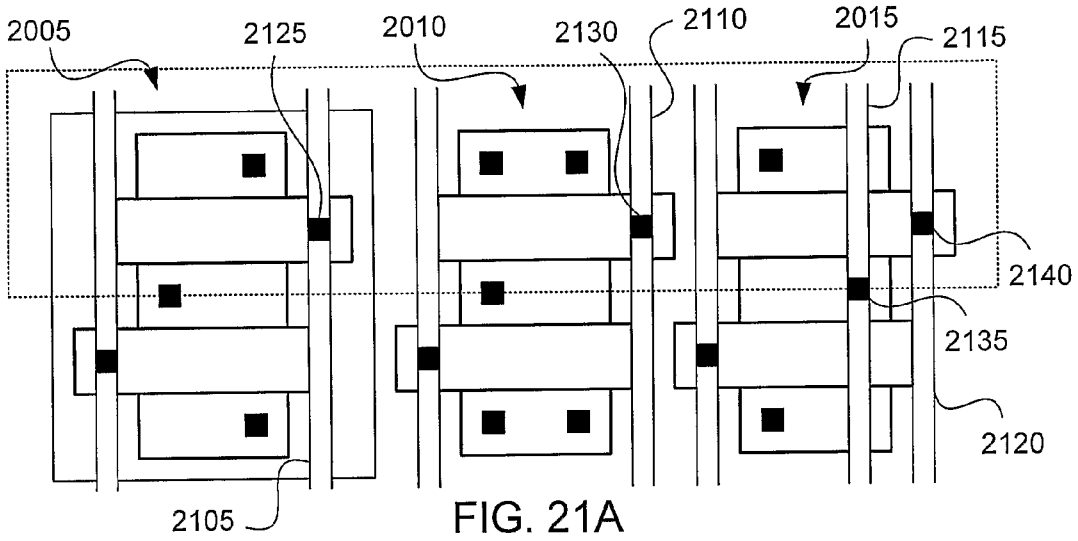



FIG. 21A

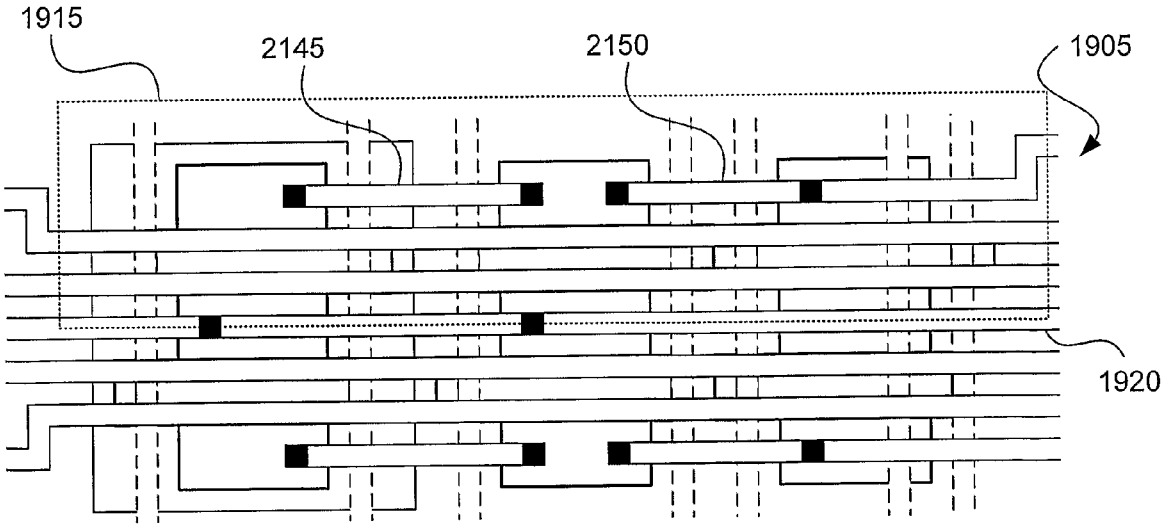



FIG. 21B

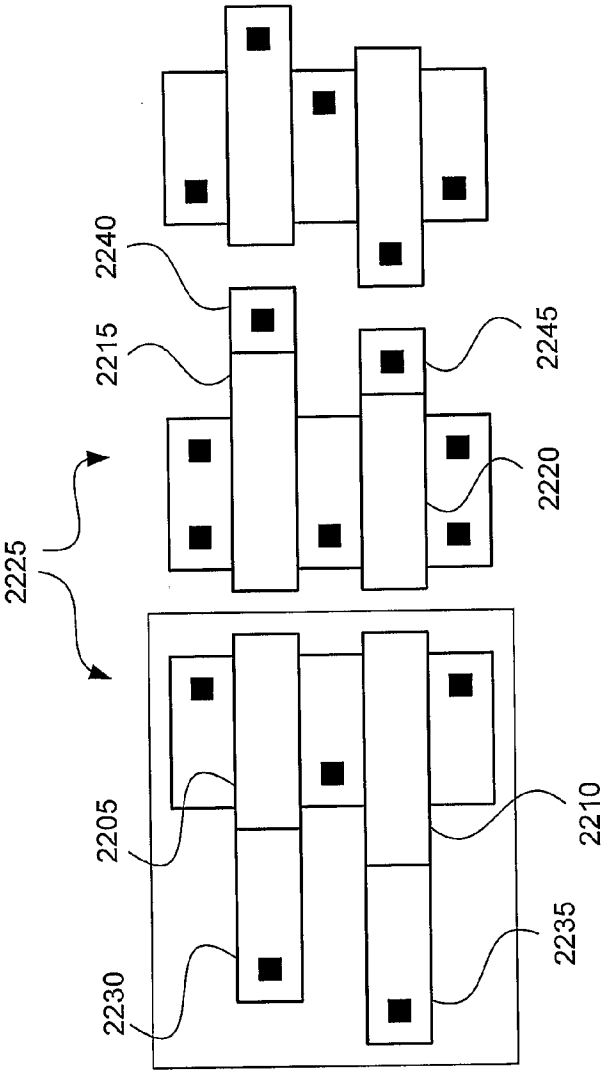



FIG. 22

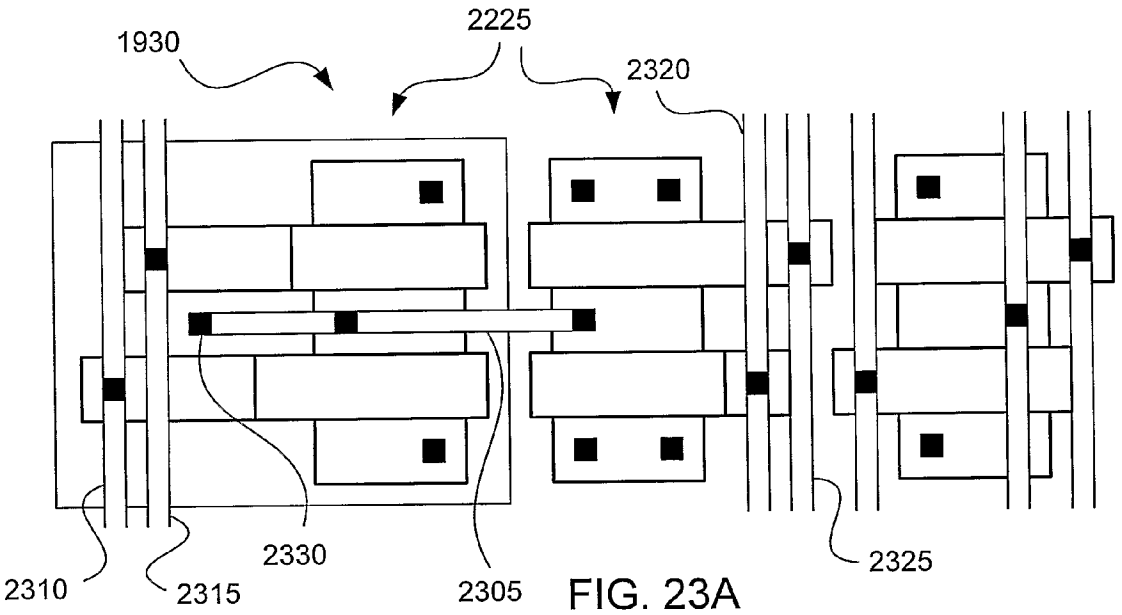



FIG. 23A

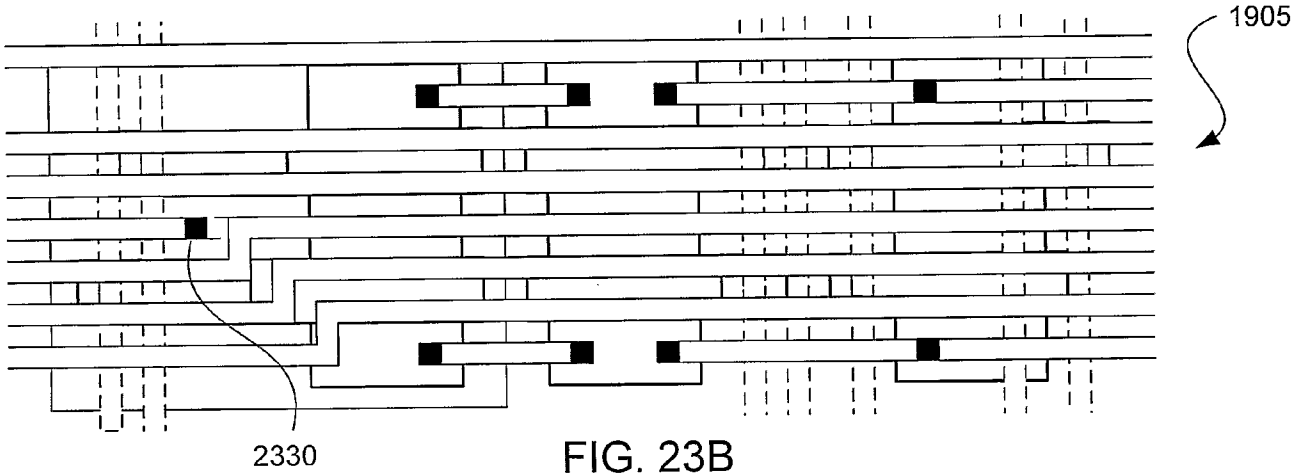



FIG. 23B

Samsung Electronics Co., Ltd.
Ex. 1002, p. 674

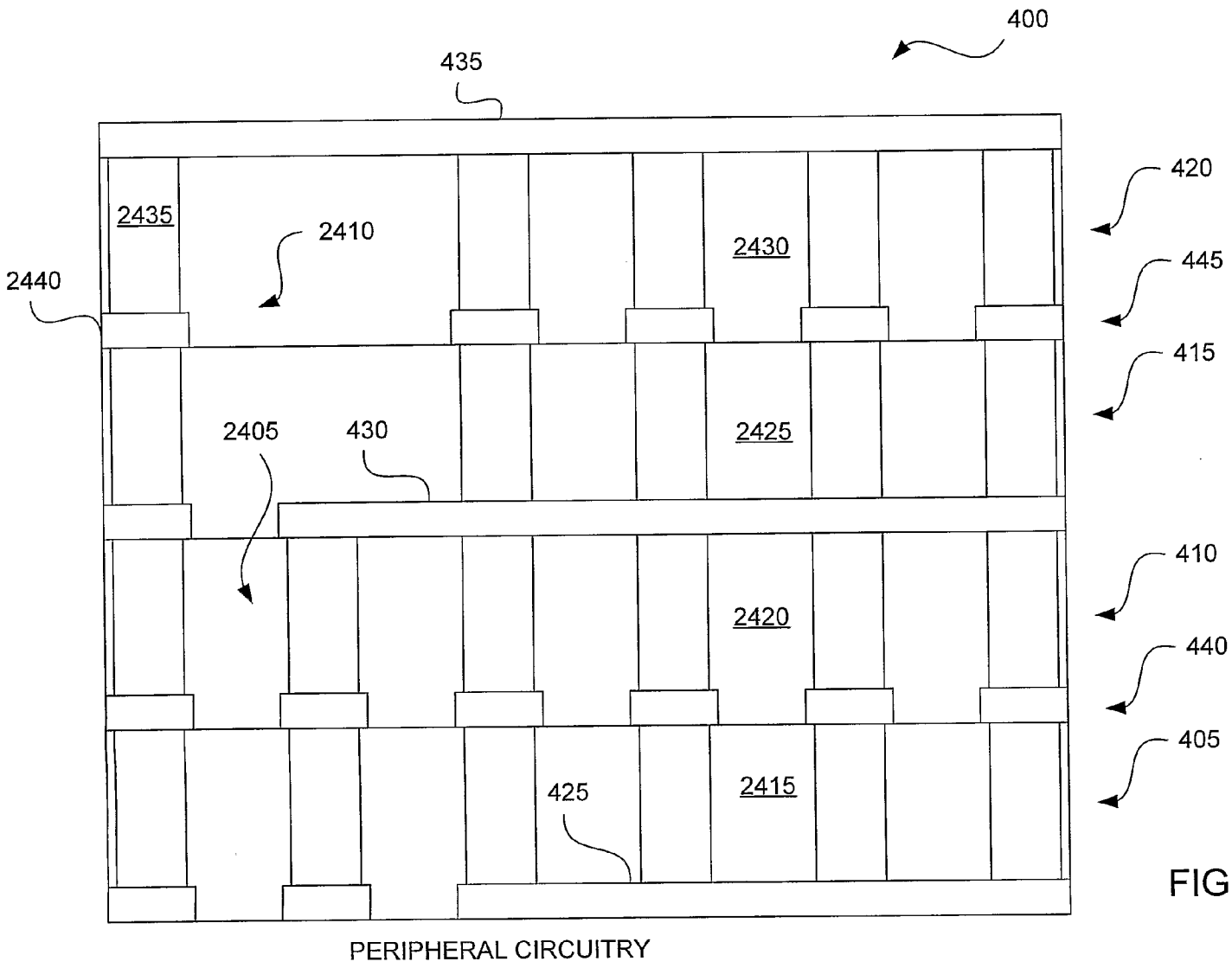

400
435
2435
2410
2430
2440
420
445
415
2405
430
2425
410
2420
440
405
425
2415
PERIPHERAL CIRCUITRY

FIG. 24

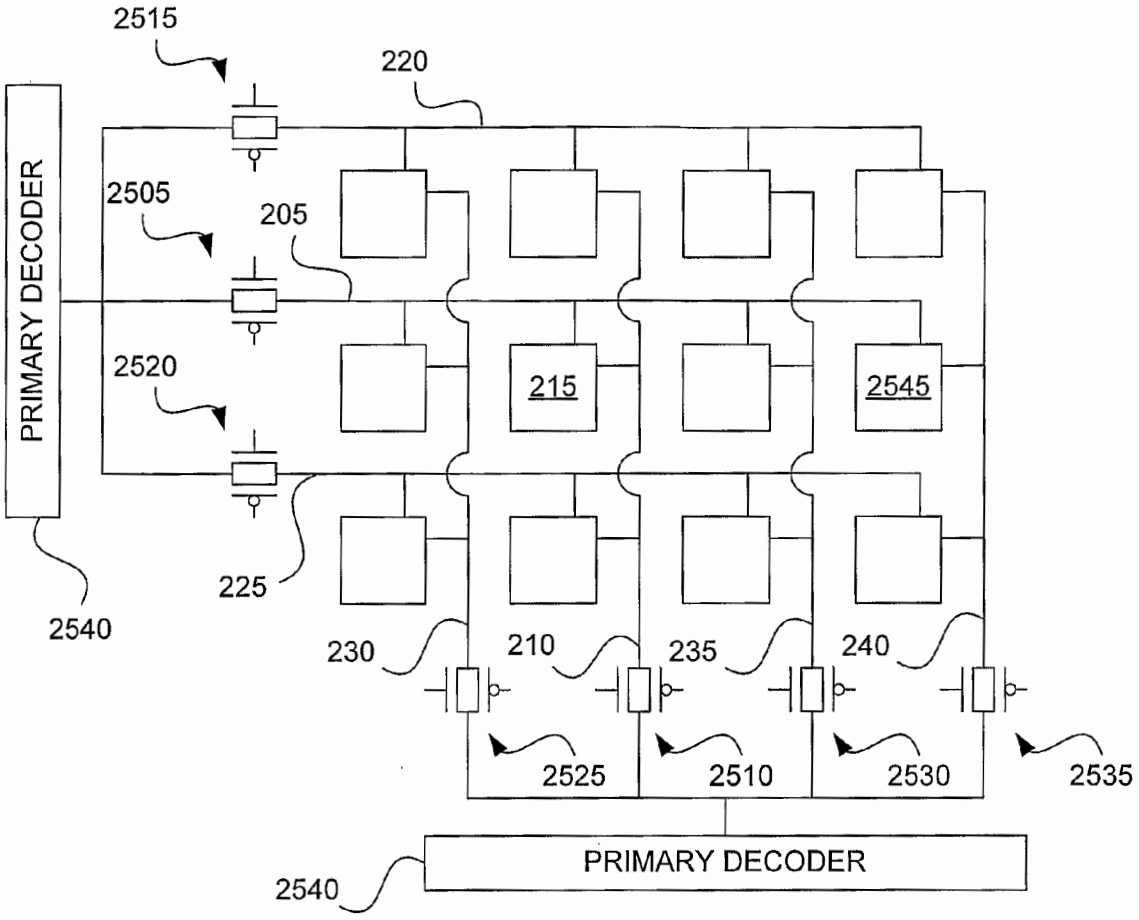

2515
220
PRIMARY DECODER
2505
205
2520
215
2545
225
2540
230
210
235
240
2525
2510
2530
2535
PRIMARY DECODER
2540

FIG. 25A

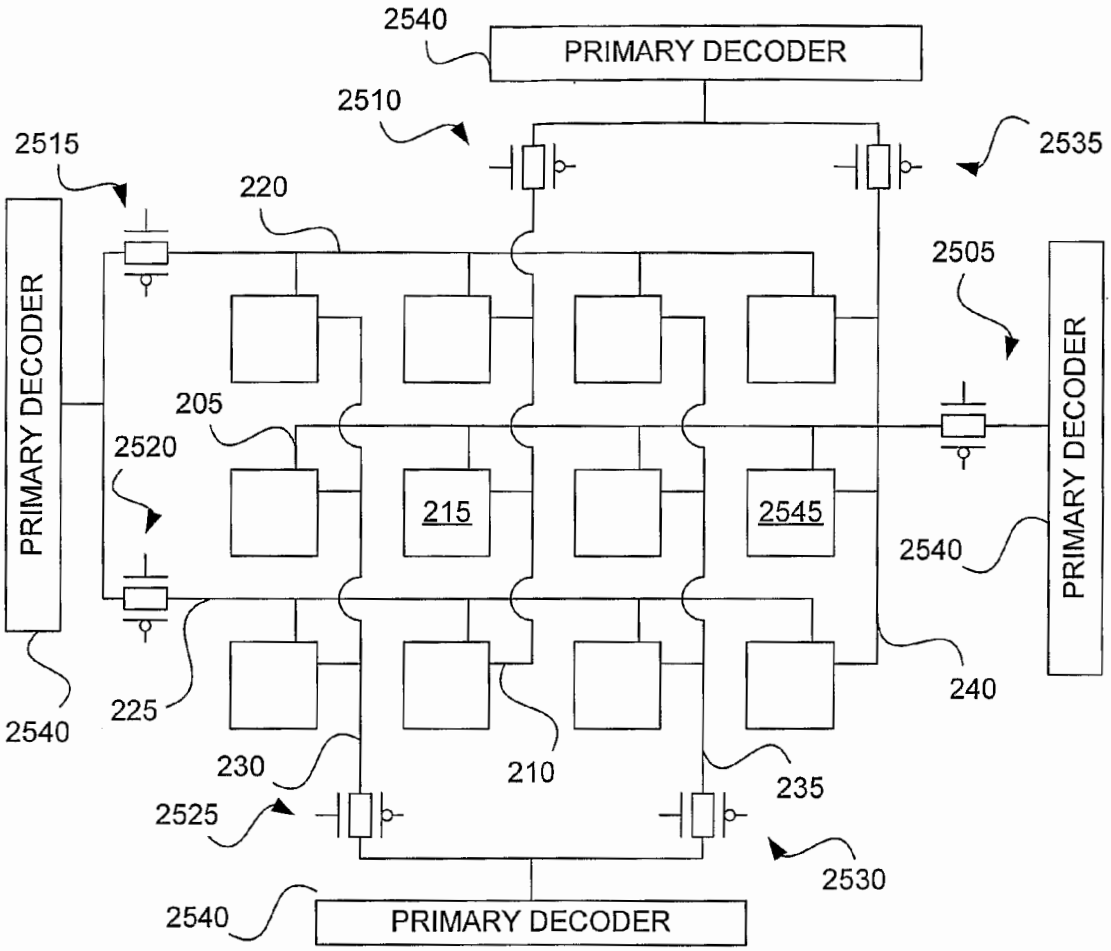

2540
PRIMARY DECODER
2510
2515
2535
220
2505
PRIMARY DECODER
205
2520
215
2545
2540
PRIMARY DECODER
2540
225
240
230
210
235
2525
2530
2540
PRIMARY DECODER

FIG. 25B

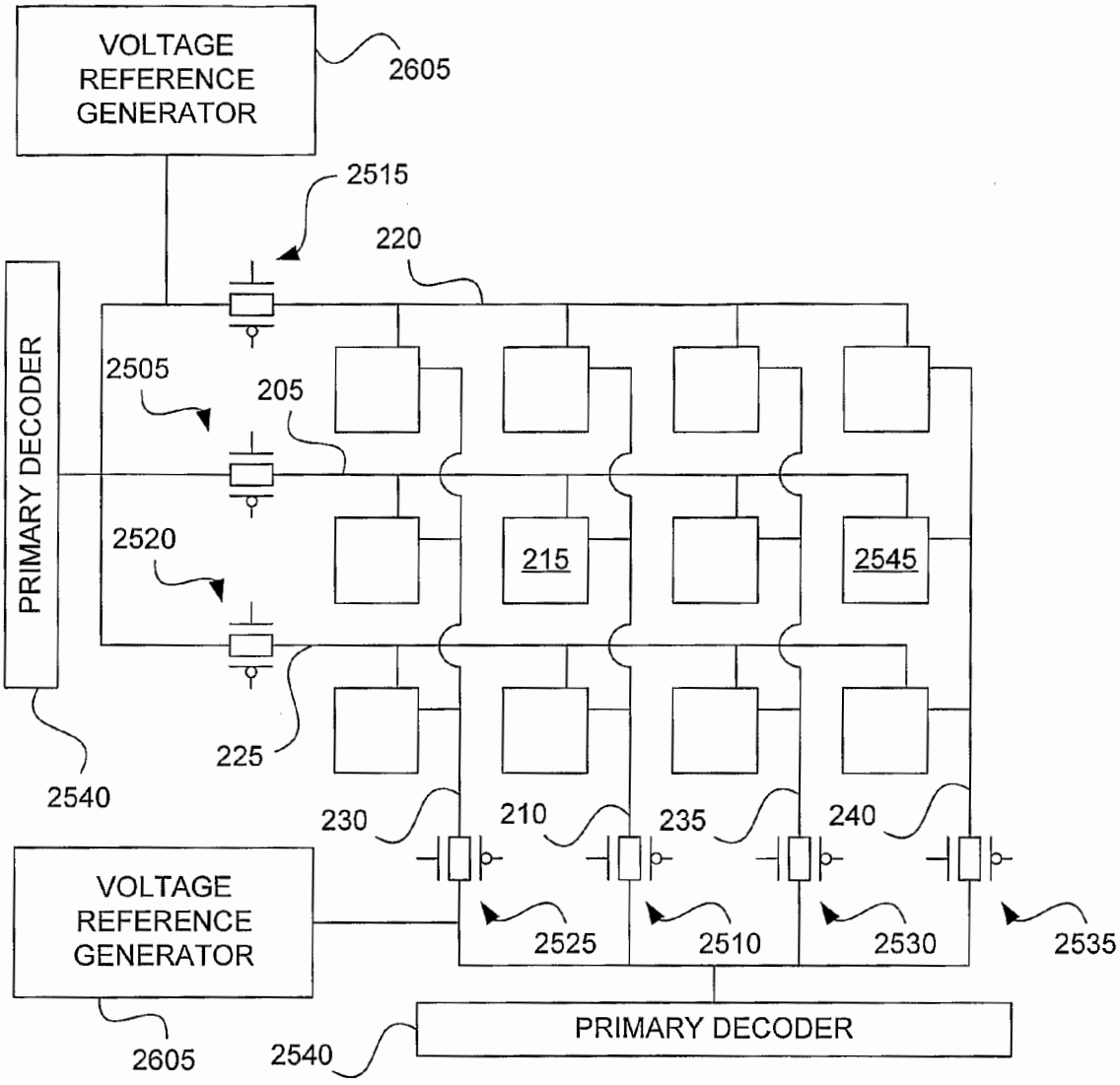

VOLTAGE REFERENCE GENERATOR
2605
2515
220
PRIMARY DECODER
2505
205
2520
215
2545
225
2540
230
210
235
240
VOLTAGE REFERENCE GENERATOR
2525
2510
2530
2535
2605
2540
PRIMARY DECODER

FIG. 26A

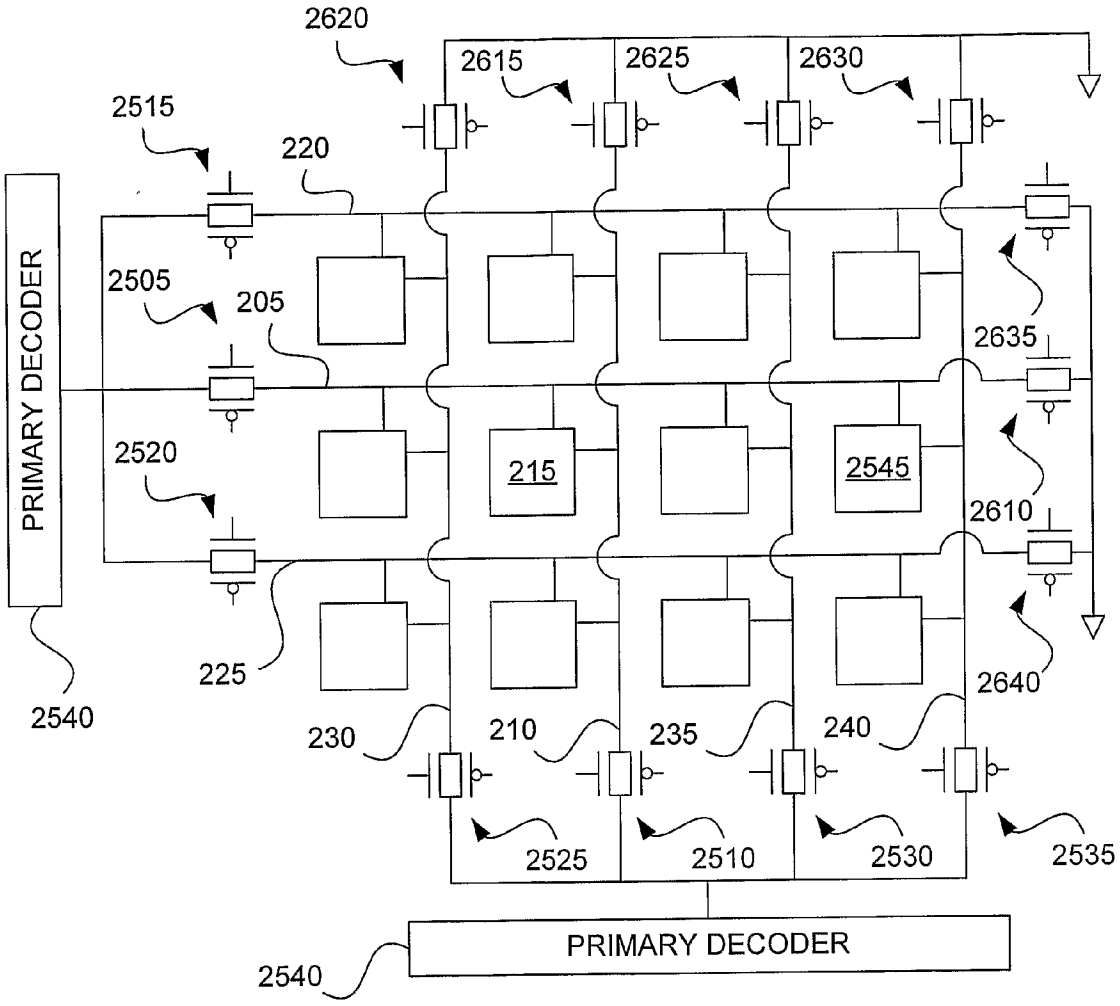

2620
2615
2625
2630
2515
220
PRIMARY DECODER
2505
205
2635
2520
215
2545
2610
225
2640
2540
230
210
235
240
2525
2510
2530
2535
PRIMARY DECODER
2540

FIG. 26B

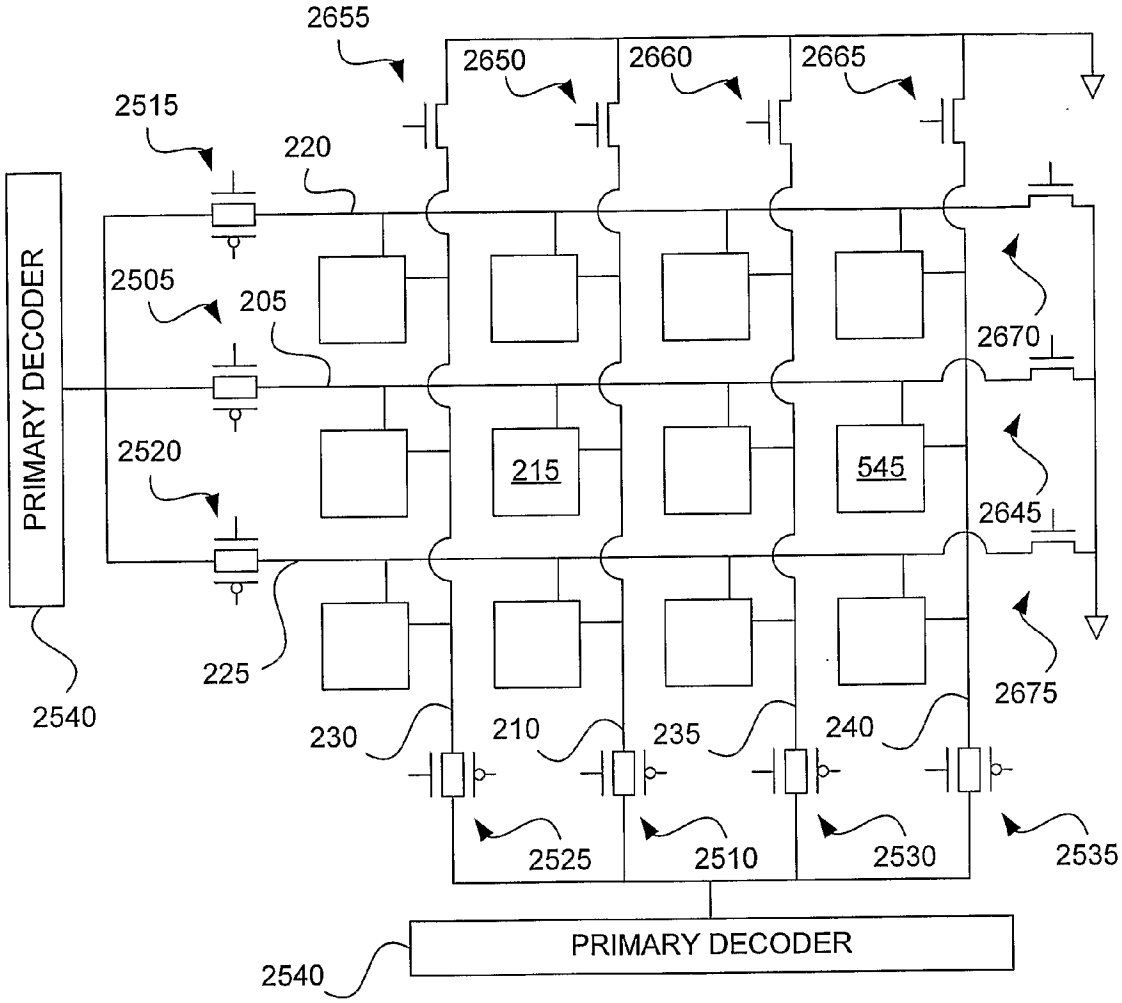

2655
2650
2660
2665
2515
220
PRIMARY DECODER
2505
205
2670
2520
215
545
2645
225
2675
2540
230
210
235
240
2525
2510
2530
2535
PRIMARY DECODER
2540

FIG. 26C

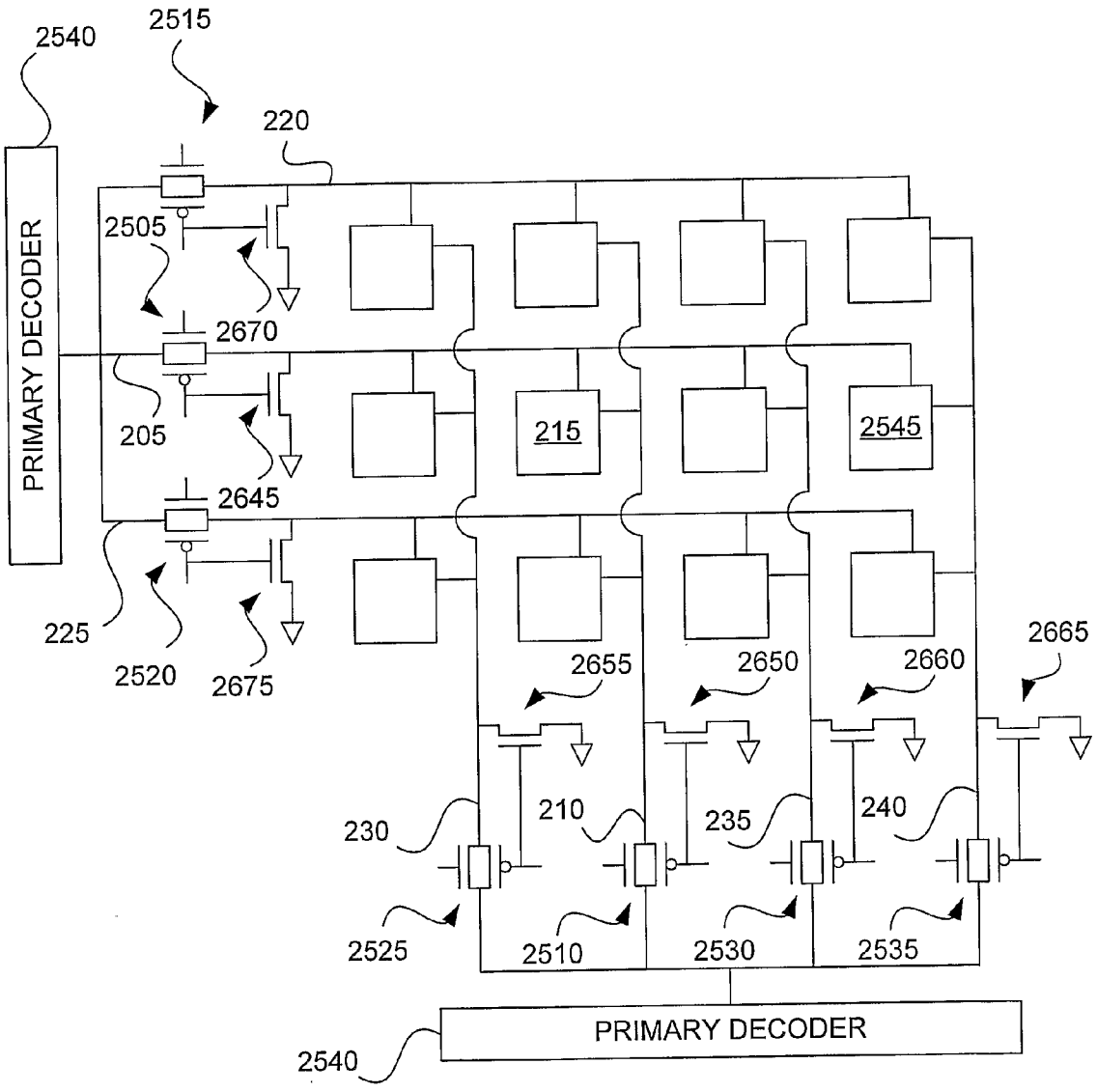

2540
2515
220
PRIMARY DECODER
2505
2670
205
215
2545
2645
225
2520
2675
2655
2650
2660
2665
230
210
235
240
2525
2510
2530
2535
PRIMARY DECODER
2540

FIG. 26D

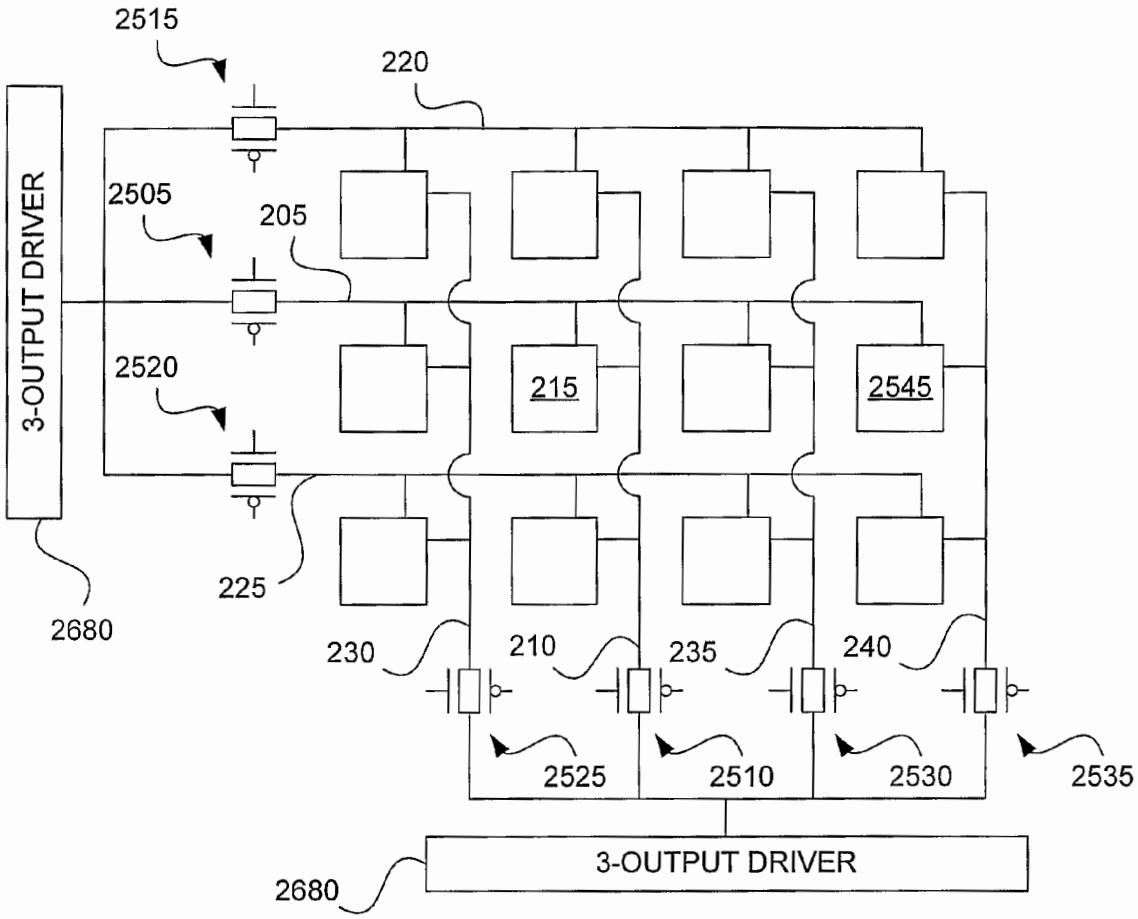

2515
220
2505
205
3-OUTPUT DRIVER
2520
215
2545
225
2680
230
210
235
240
2525
2510
2530
2535
3-OUTPUT DRIVER
2680

FIG. 26E

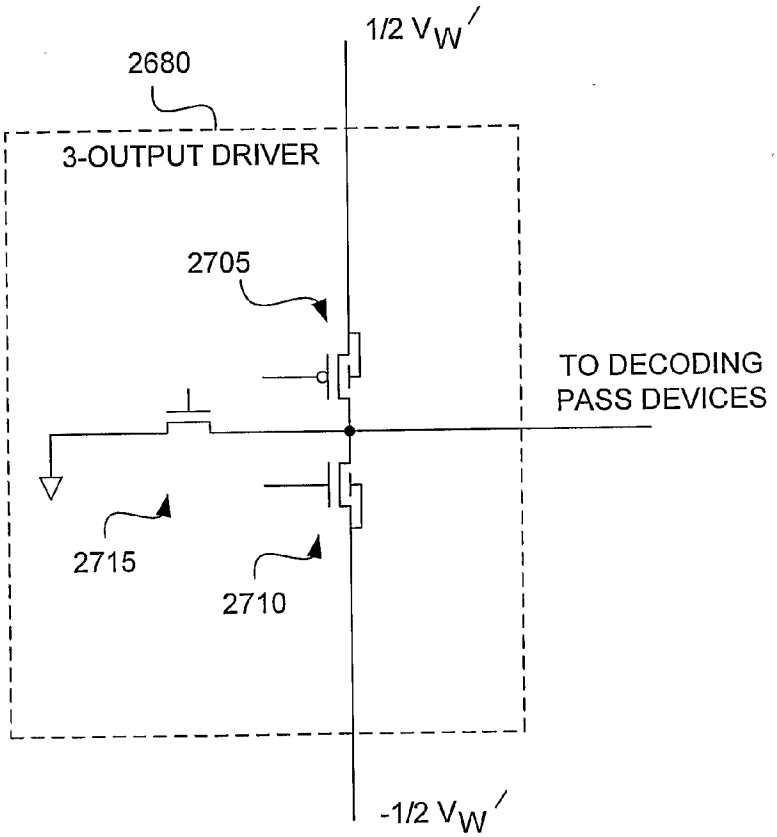

1/2 $V_W$'
2680
3-OUTPUT DRIVER
2705
TO DECODING
PASS DEVICES
2715
2710
-1/2 $V_W$'

FIG. 27

Discharge at start of write select signal

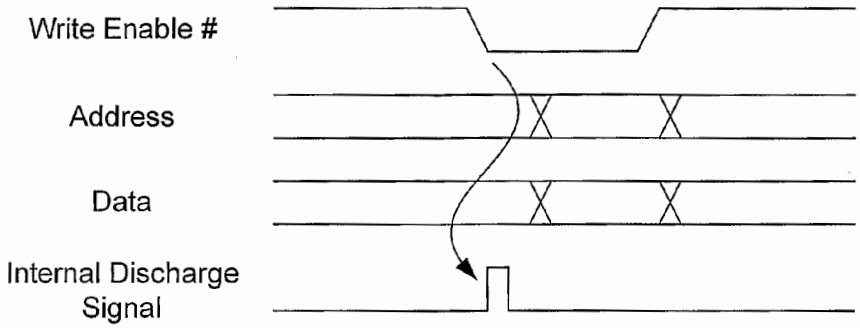



FIG. 28

Discharge at end of write select signal

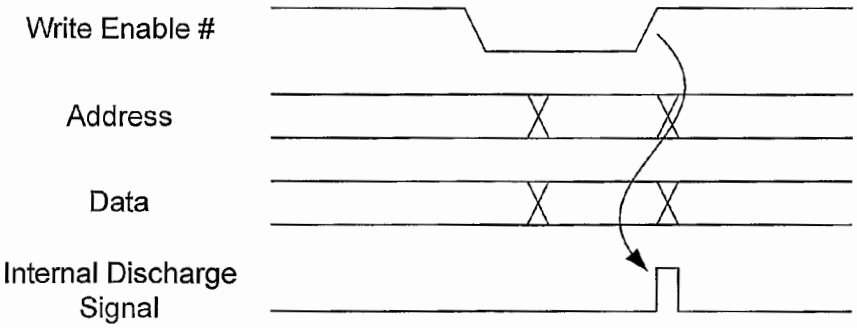



FIG. 29

Discharge at end of write operation

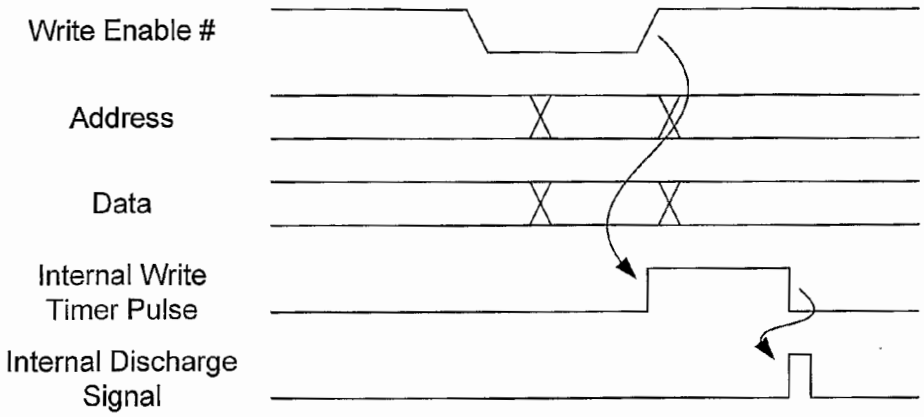



FIG. 30

Discharge at start of write select signal and end of write select operation

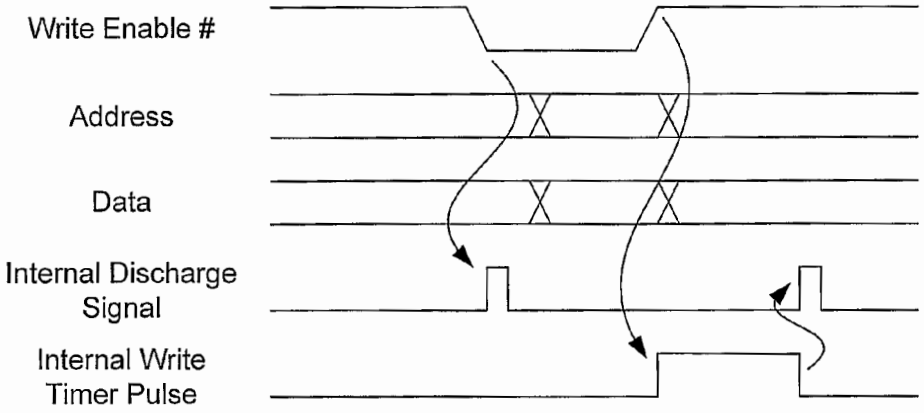



FIG. 31

Discharge during signal transitions

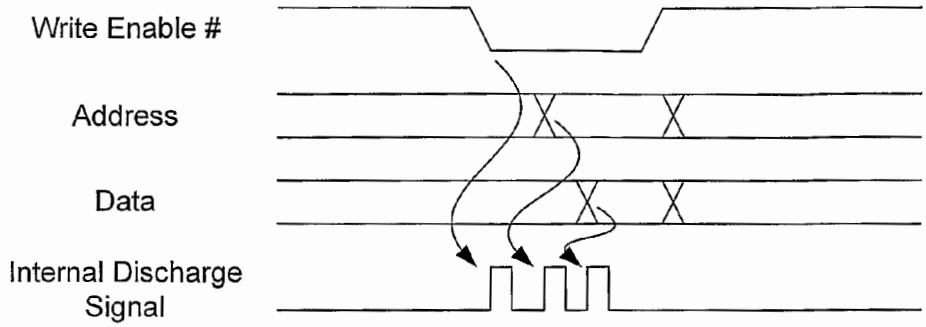



FIG. 32

Discharge with delayed addresses

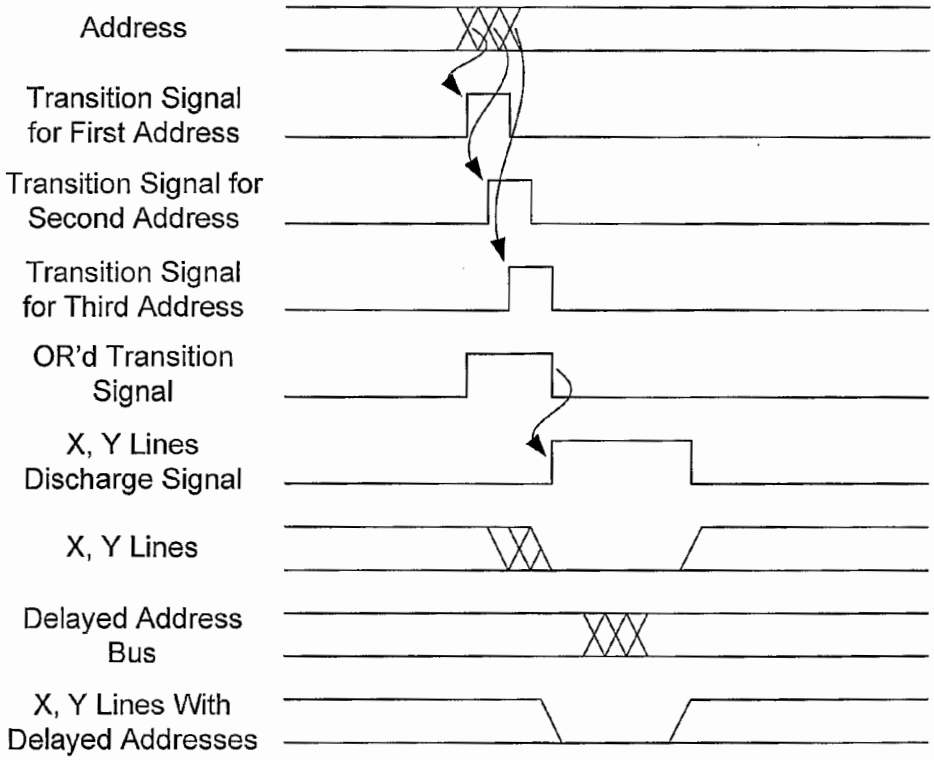



FIG. 33

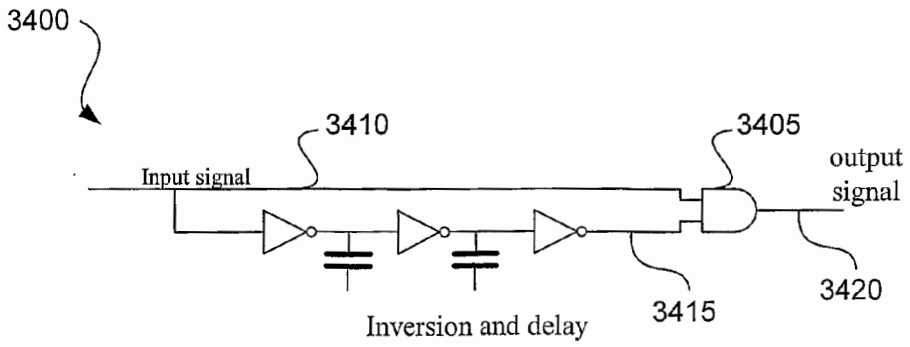



FIG. 34A

Signal Transition Detection Timing Diagram

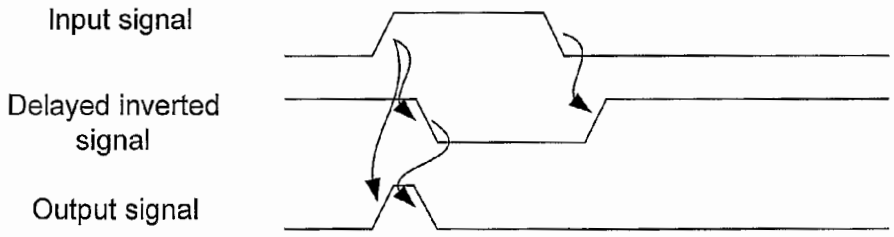



FIG. 34B

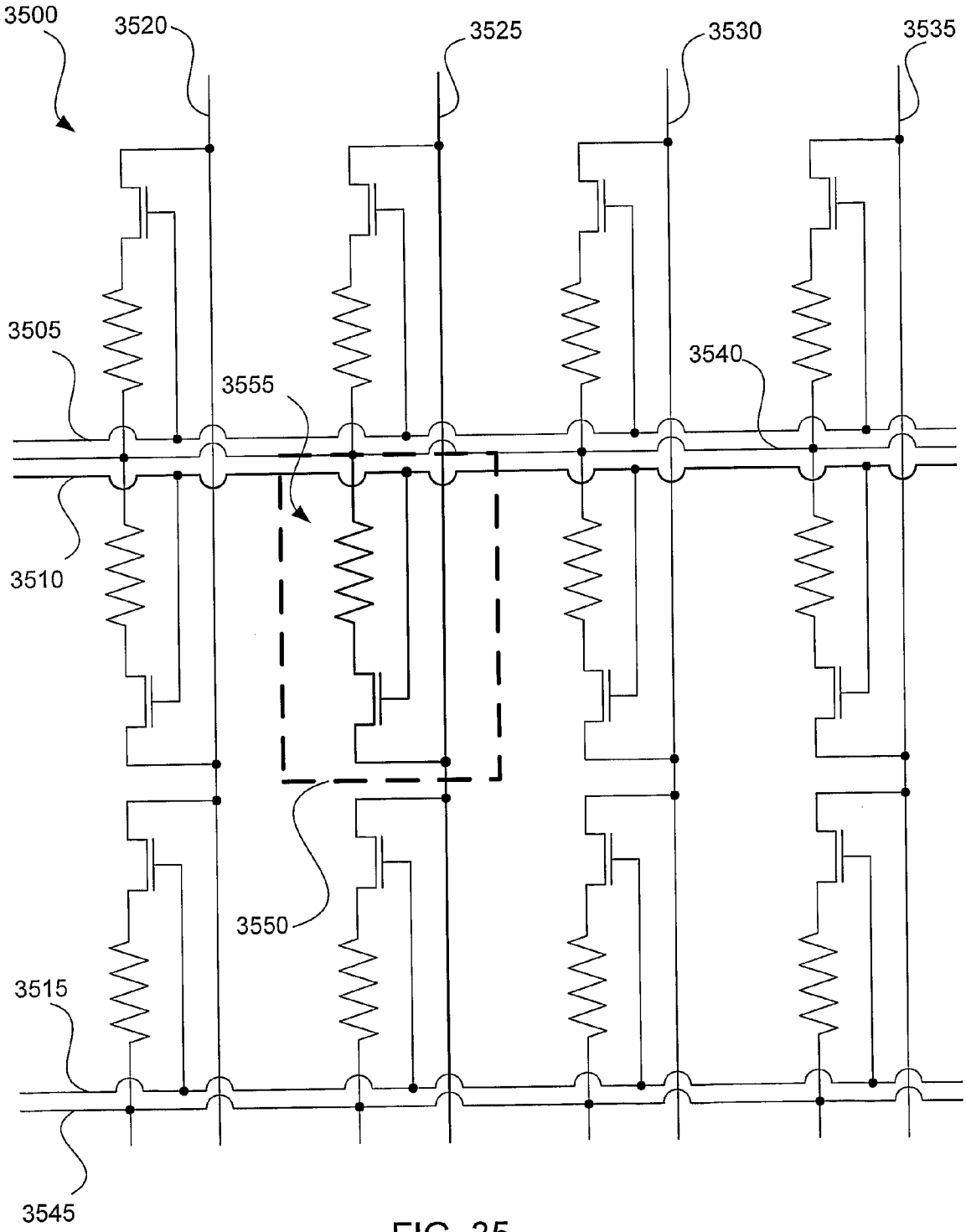



FIG. 35

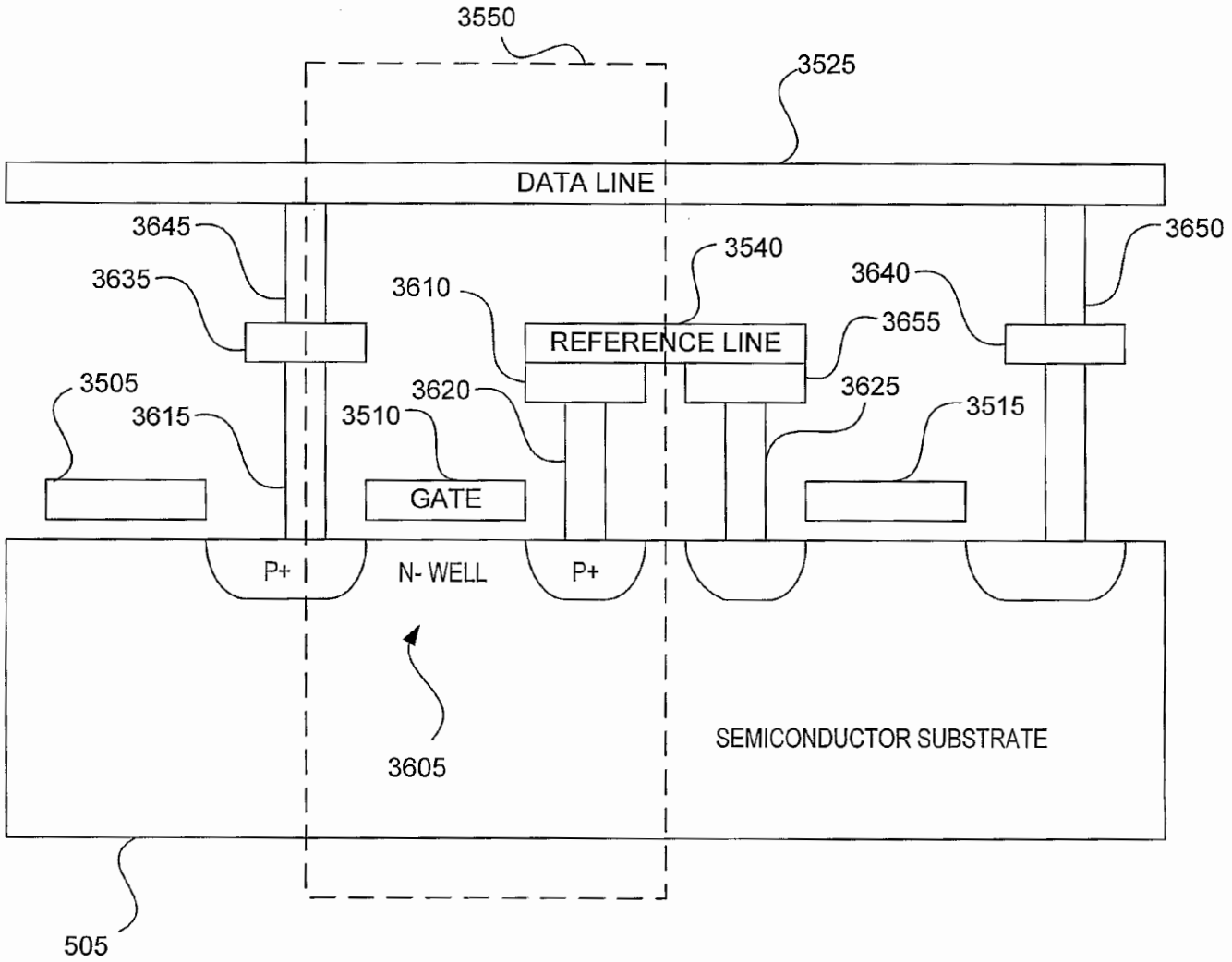

3550
3525
DATA LINE
3645
3635
3650
3540
3610
3640
REFERENCE LINE
3655
3505
3620
3625
3615
3510
3515
GATE
P+
N- WELL
P+
3605
SEMICONDUCTOR SUBSTRATE
505

FIG. 36

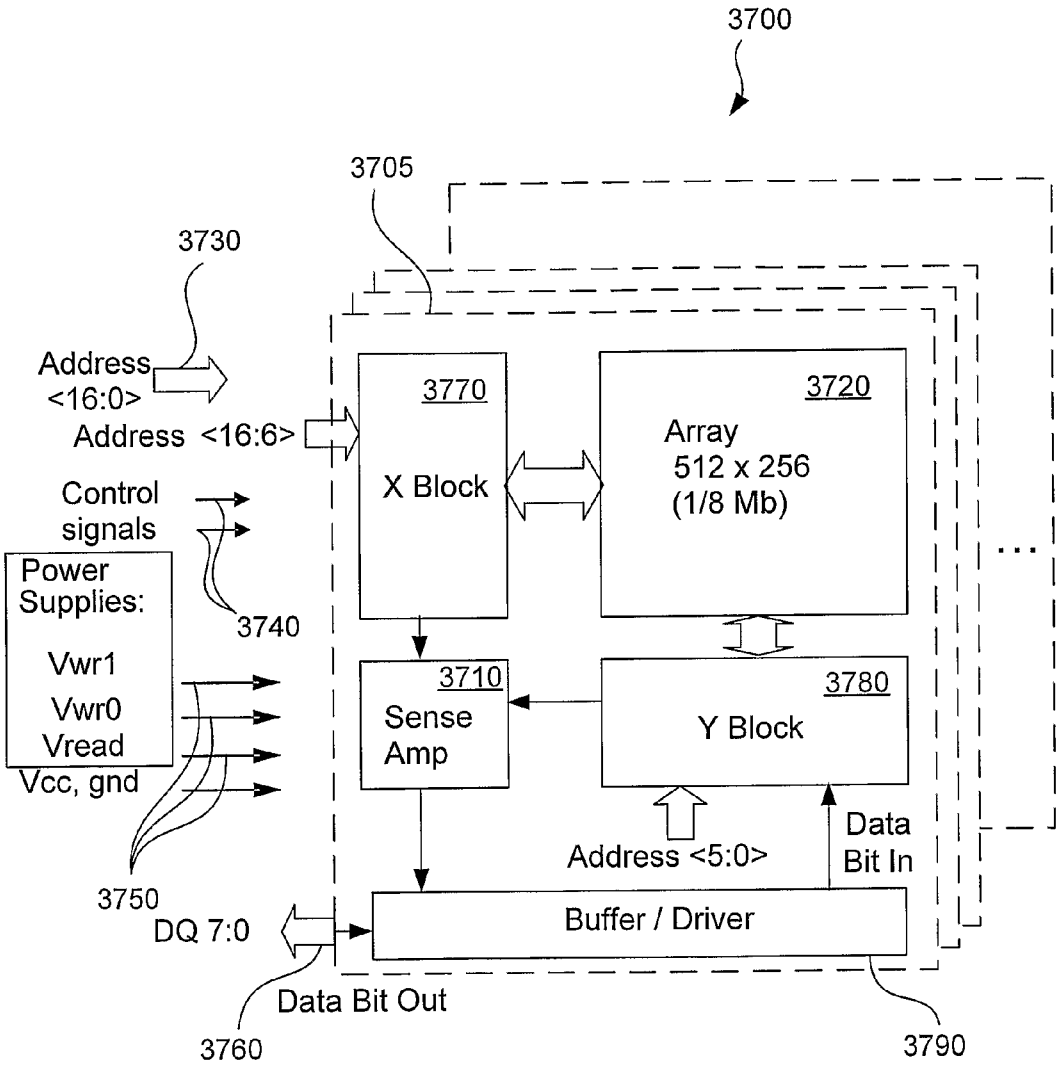

3700
3705
3730
Address
<16:0>
Address <16:6>
Control
signals
Power
Supplies:
Vwr1
Vwr0
Vread
Vcc, gnd
3740
3750
3770
X Block
3720
Array
512 x 256
(1/8 Mb)
3710
Sense
Amp
3780
Y Block
Address <5:0>
Data
Bit In
DQ 7:0
Buffer / Driver
Data Bit Out
3760
3790

FIG. 37A

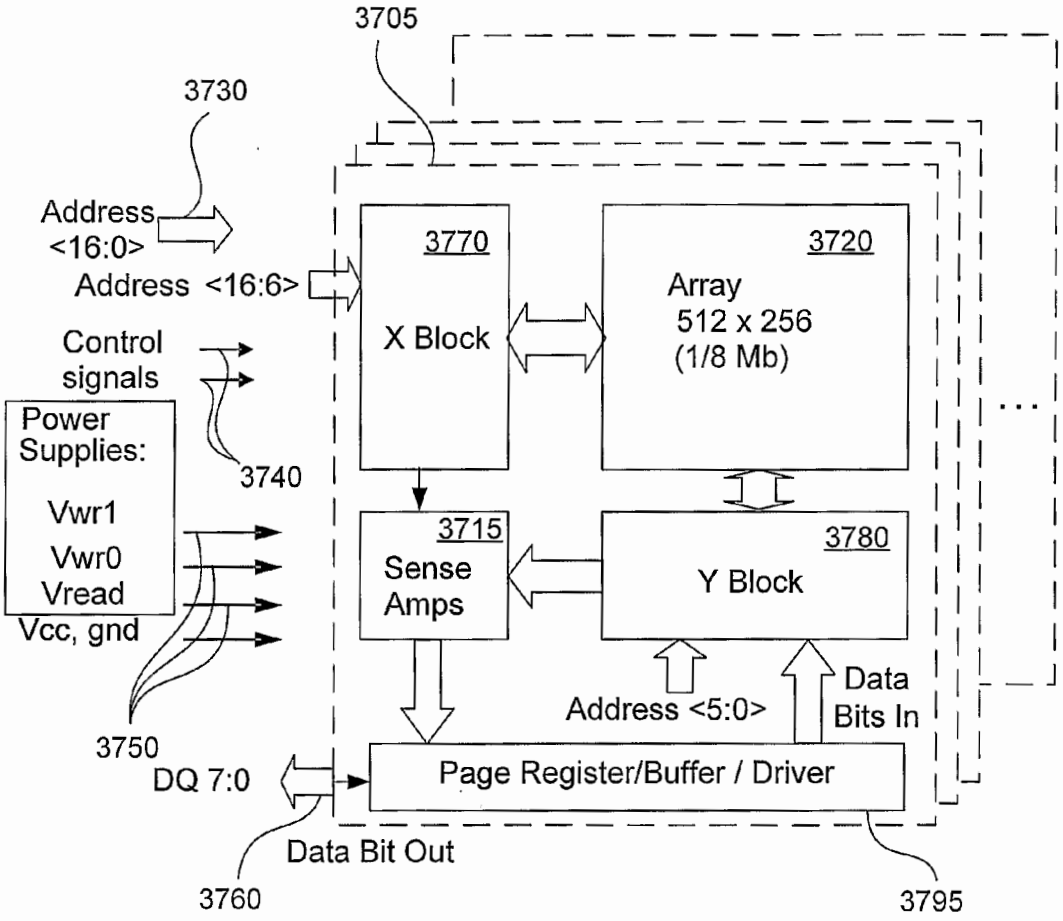

3705
3730
Address <16:0>
Address <16:6>
Control signals
Power Supplies:
Vwr1
Vwr0
Vread
Vcc, gnd
3740
3750
3770
X Block
3720
Array
512 x 256
(1/8 Mb)
3715
Sense Amps
3780
Y Block
Address <5:0>
Data Bits In
DQ 7:0
Page Register/Buffer / Driver
Data Bit Out
3760
3795

FIG. 37B

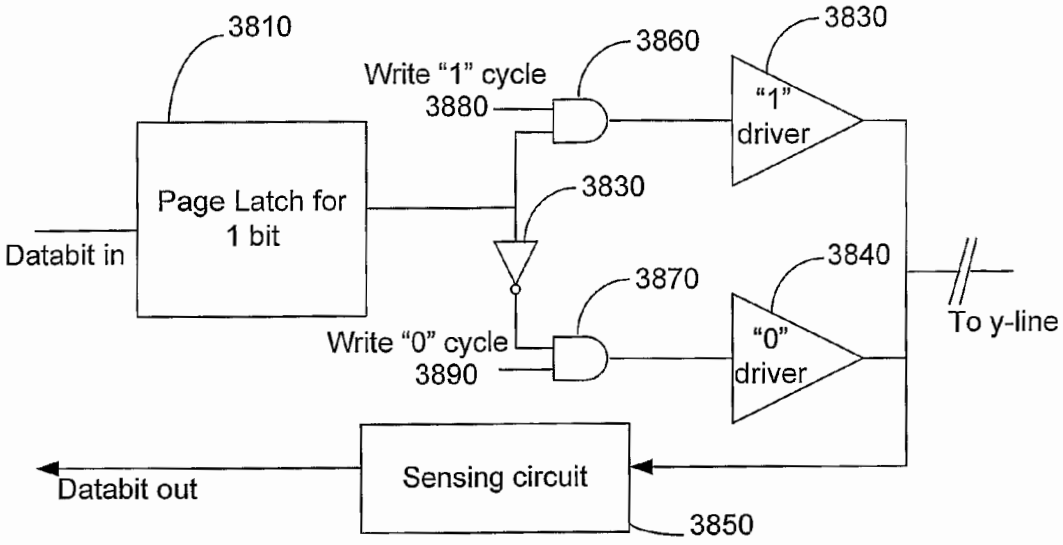



FIG. 38A

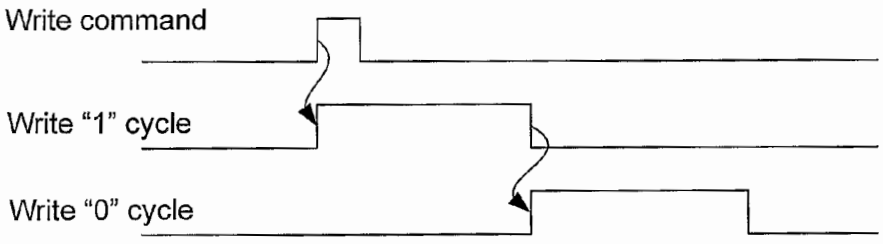



FIG. 38B

| Page latch data | | During Wr. "1" cycle | During Wr. "0" cycle |
|---|---|---|---|
| 1 | Input of "1" driver: | 1 | 0 |
| | Input of "0" driver: | 0 | 0 |
| 0 | Input of "1" driver: | 0 | 0 |
| | Input of "0" driver: | 0 | 1 |
| Where "1" on the driver input signifies that the driver is enabled. | | | |

FIG. 38C

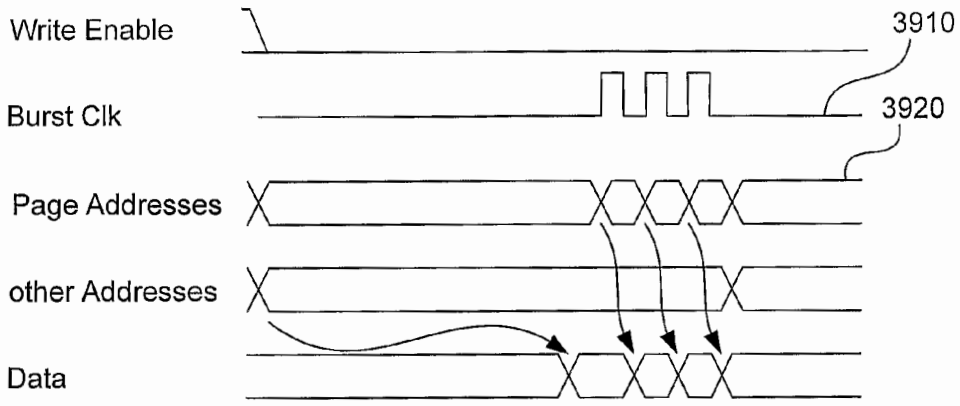



FIG. 39A

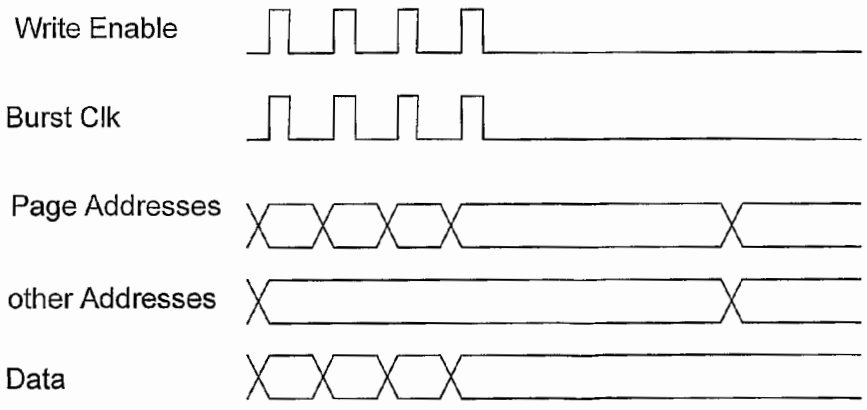



FIG. 39B

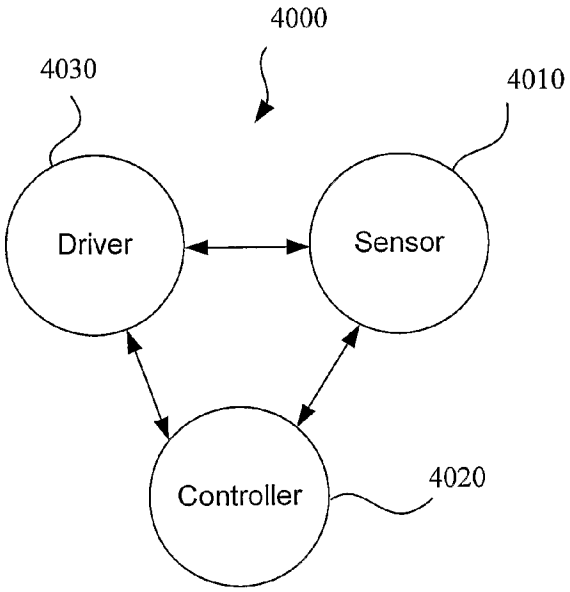



FIG. 40

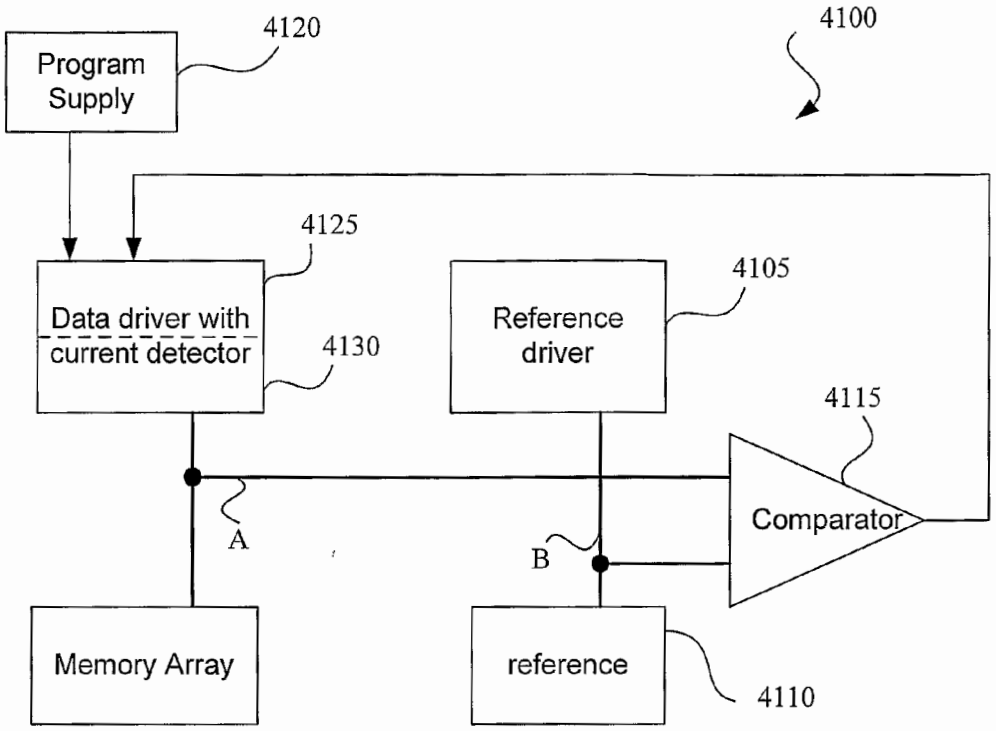



FIG. 41A

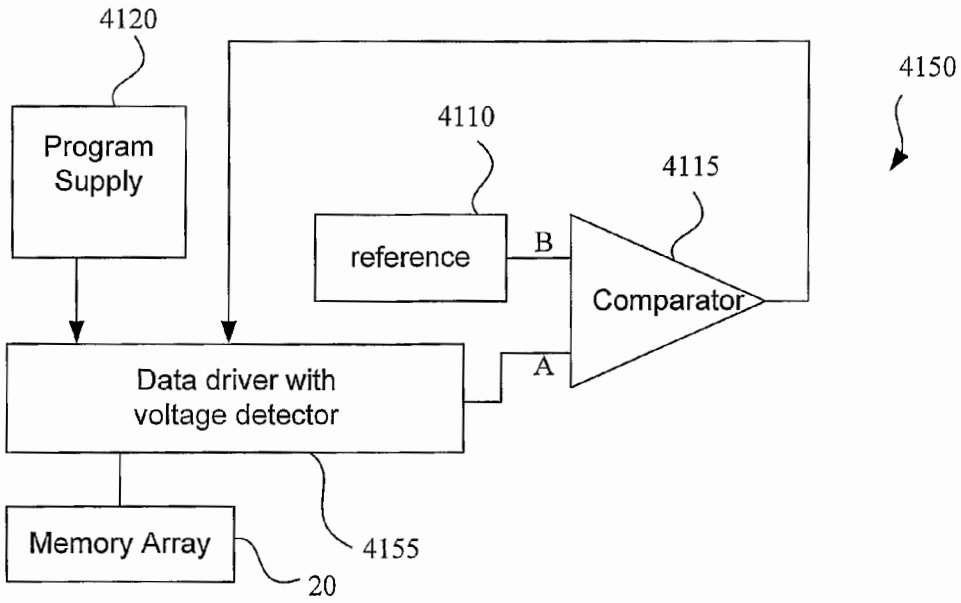



FIG. 41B

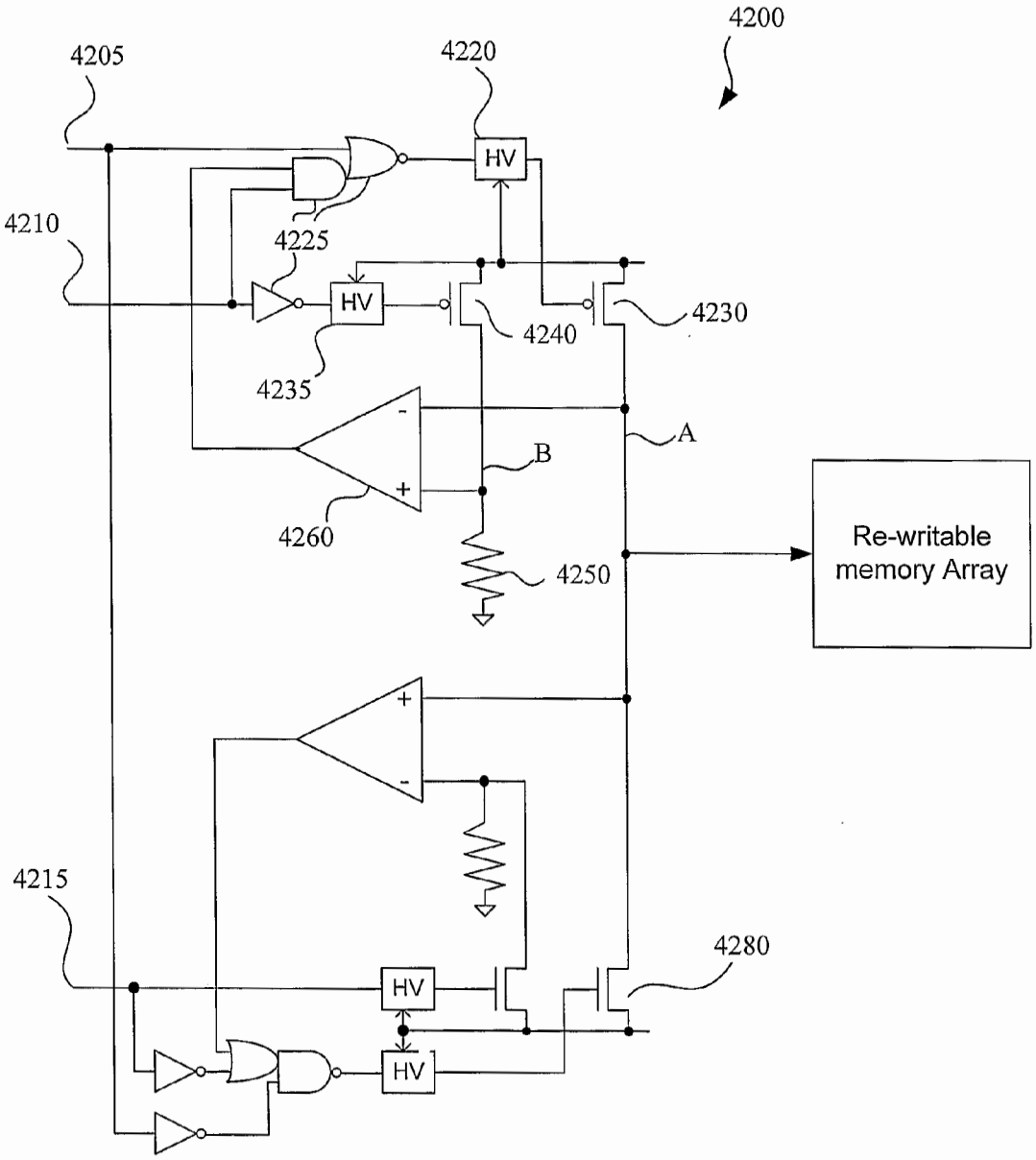

4200
4205
4220
HV
4210
4225
HV
4230
4240
4235
A
B
4260
4250
Re-writable
memory Array
4215
4280
HV
HV

FIG. 42

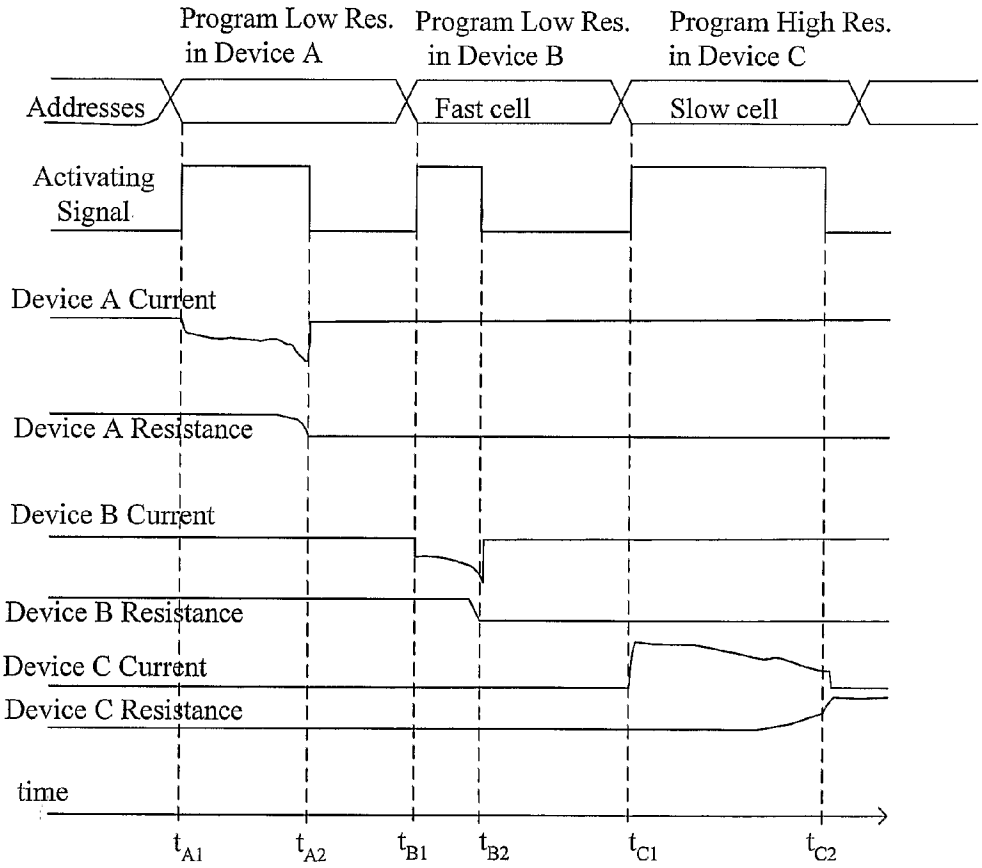

Program Low Res. in Device A
Program Low Res. in Device B
Program High Res. in Device C
Addresses
Fast cell
Slow cell
Activating Signal
Device A Current
Device A Resistance
Device B Current
Device B Resistance
Device C Current
Device C Resistance
time
$t_{A1}$
$t_{A2}$
$t_{B1}$
$t_{B2}$
$t_{C1}$
$t_{C2}$

FIG. 43

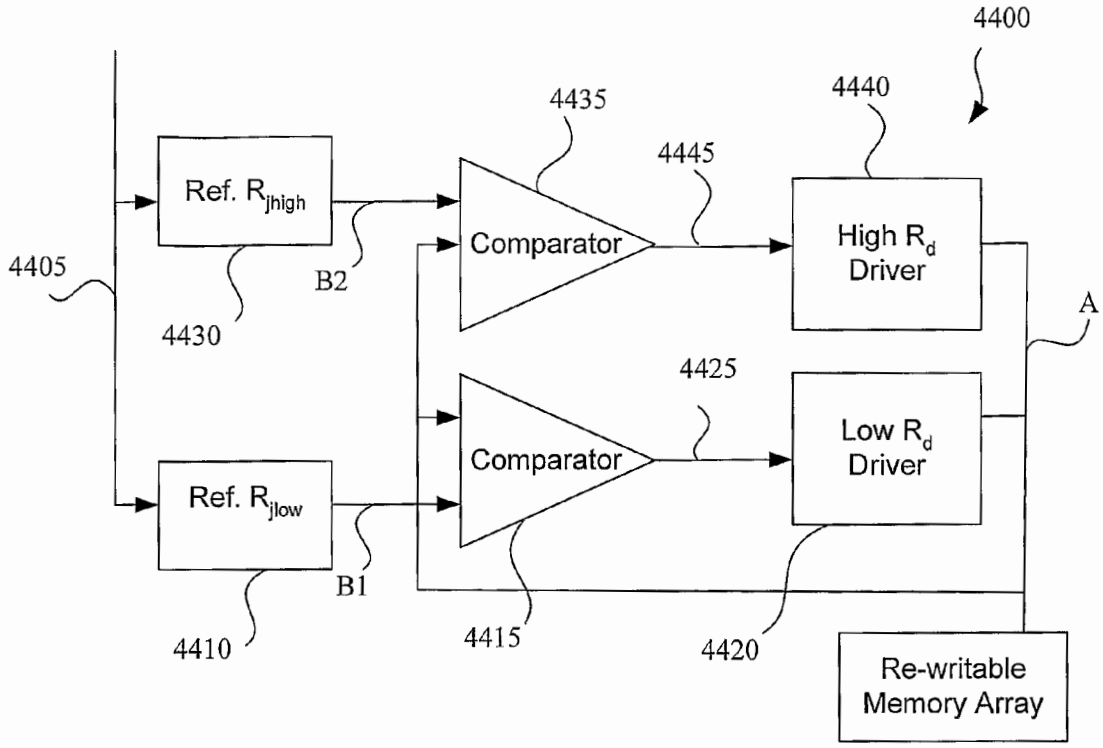

4400
4435
4440
4445
Ref. $R_{jhigh}$
Comparator
High $R_d$ Driver
4405
B2
4430
A
4425
Comparator
Low $R_d$ Driver
Ref. $R_{jlow}$
B1
4410
4415
4420
Re-writable Memory Array

FIG. 44

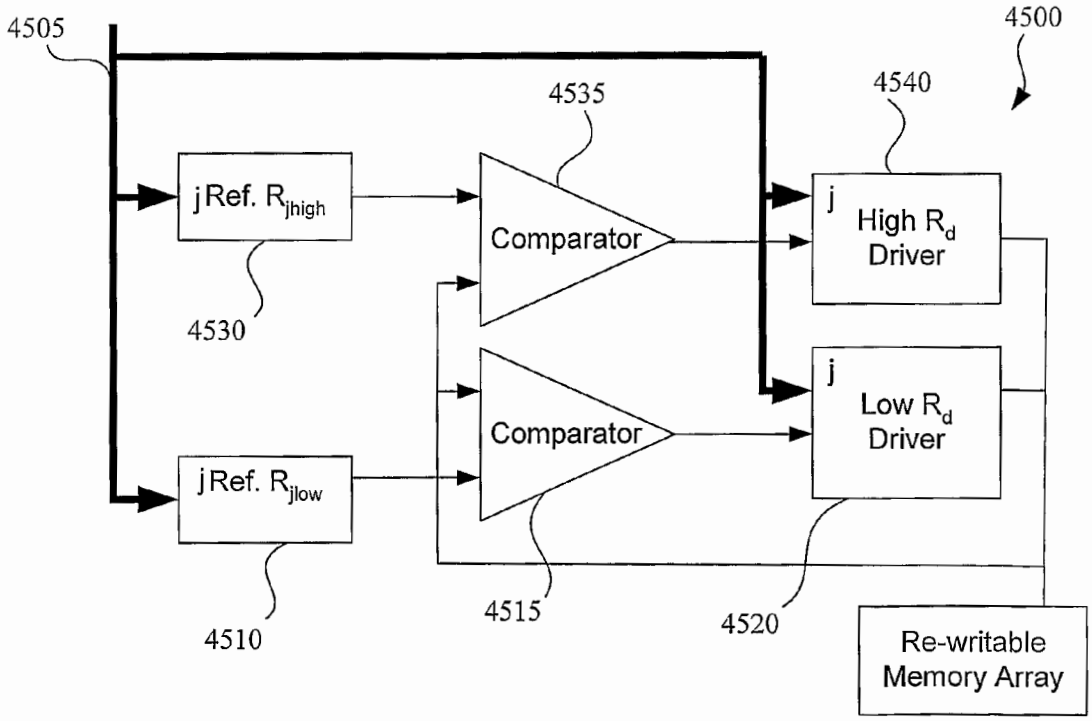

4505
4500
4535
4540
jRef. $R_{jhigh}$
Comparator
j High $R_d$ Driver
4530
Comparator
j Low $R_d$ Driver
jRef. $R_{jlow}$
4510
4515
4520
Re-writable Memory Array

FIG. 45

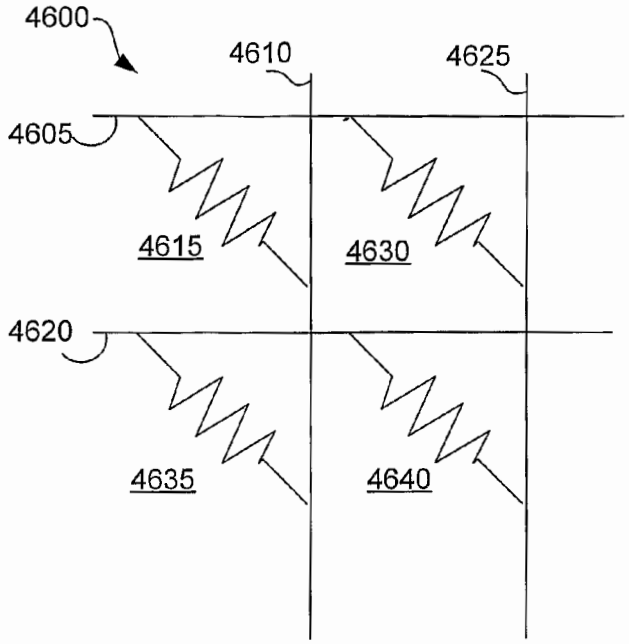

4600
4610
4625
4605
4615
4630
4620
4635
4640

FIG. 46

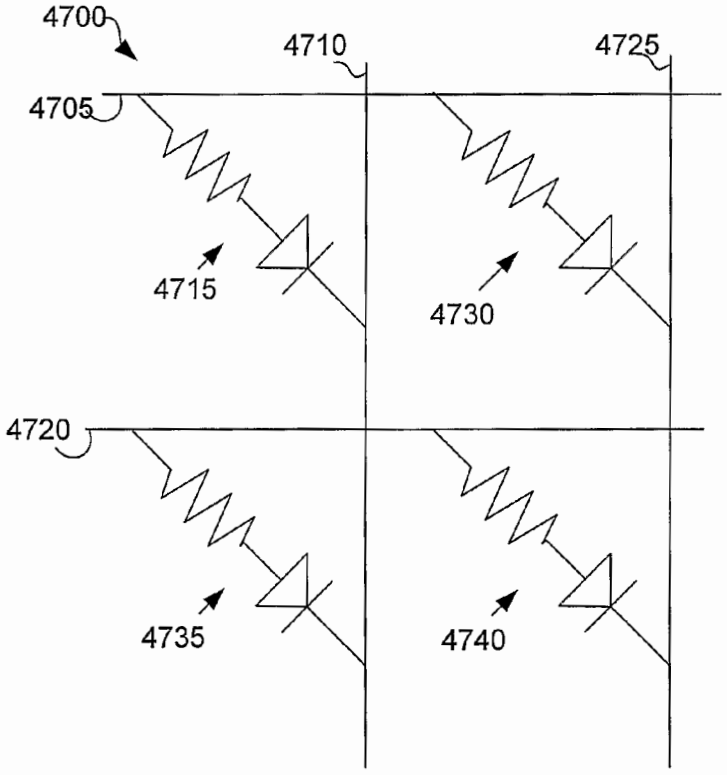

4700
4710
4725
4705
4715
4730
4720
4735
4740

FIG. 47

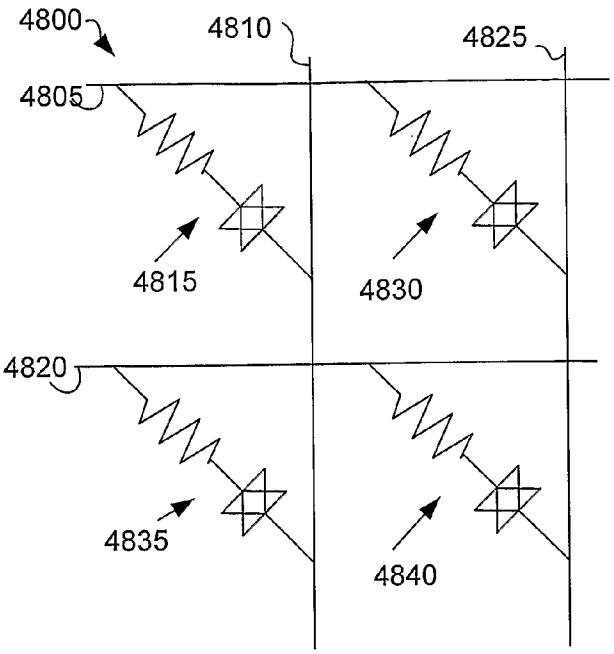



FIG. 48

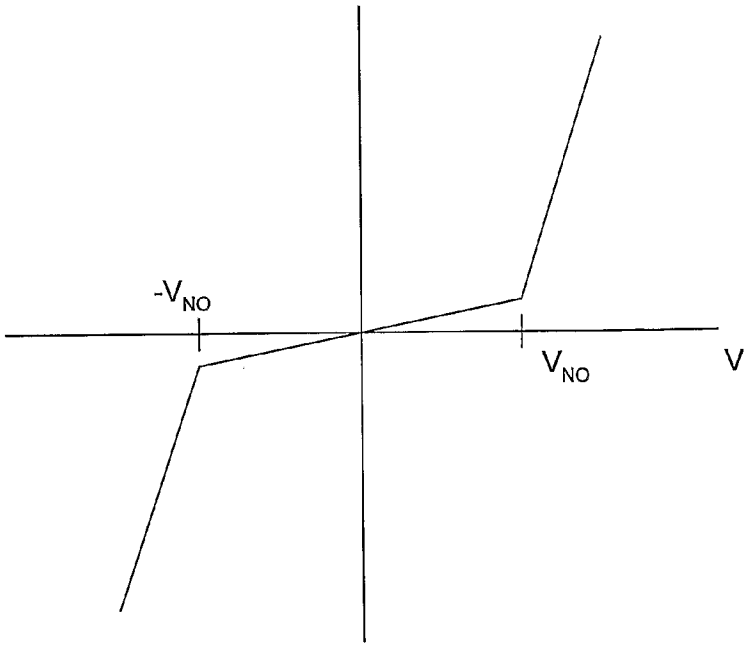



FIG. 49

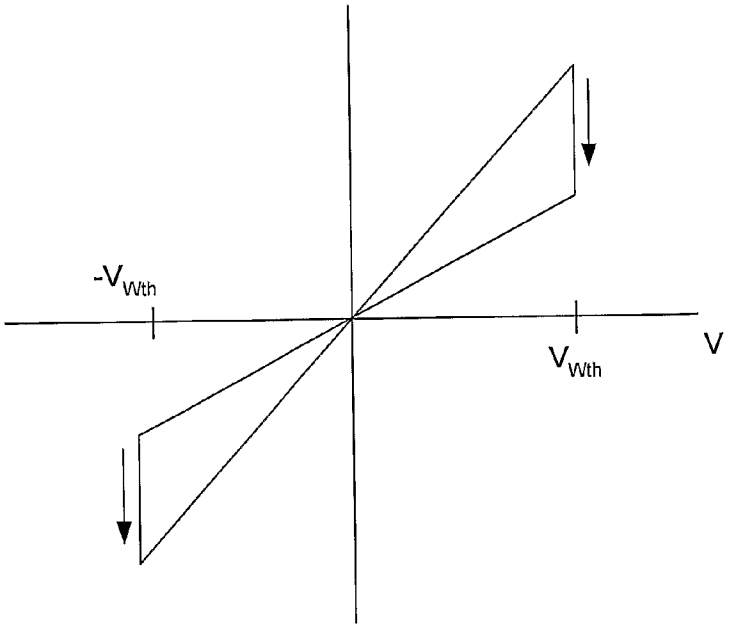



FIG. 50

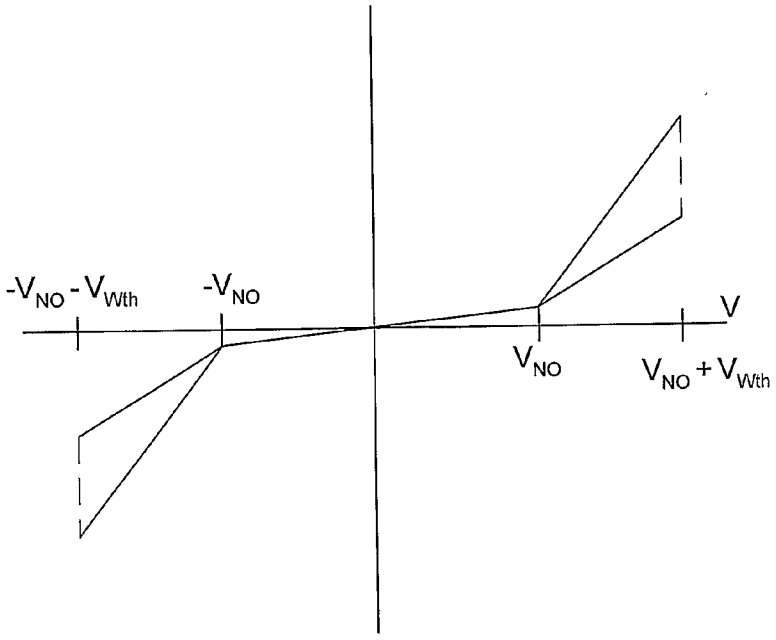



FIG. 51

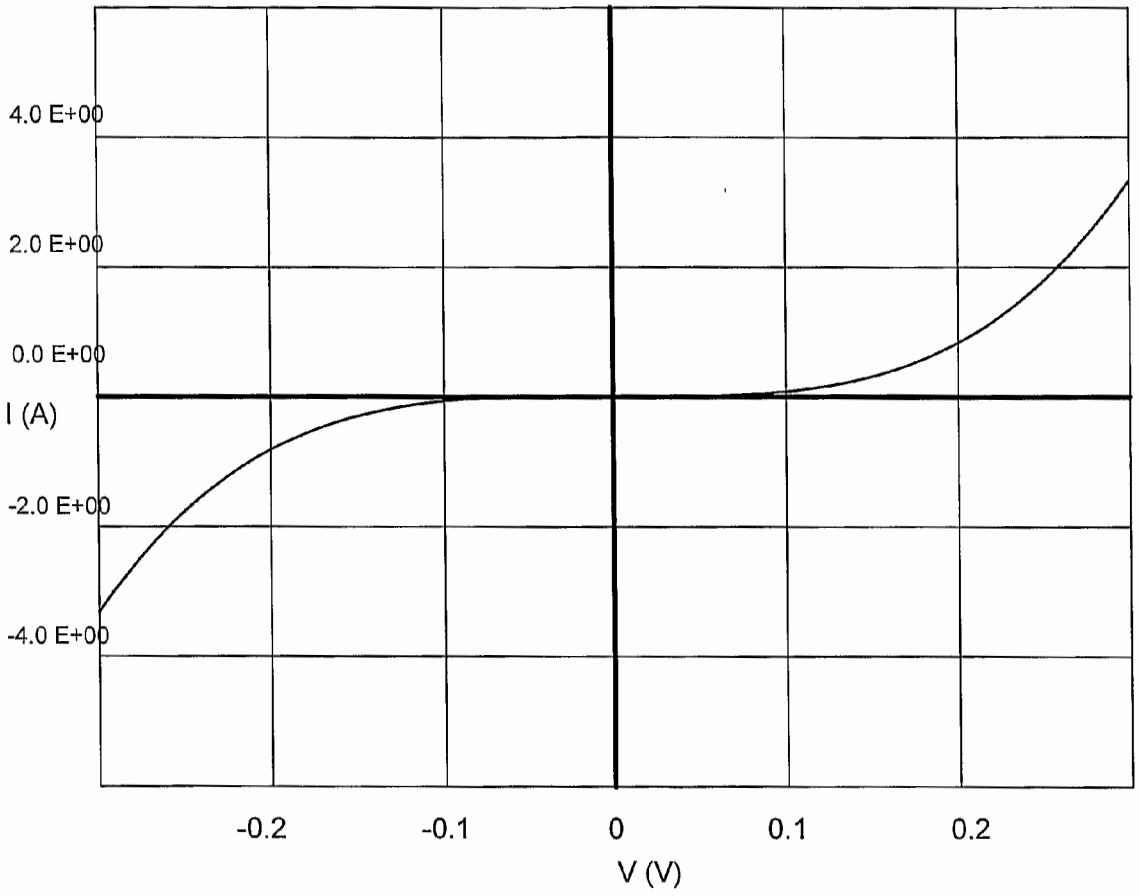



FIG. 52

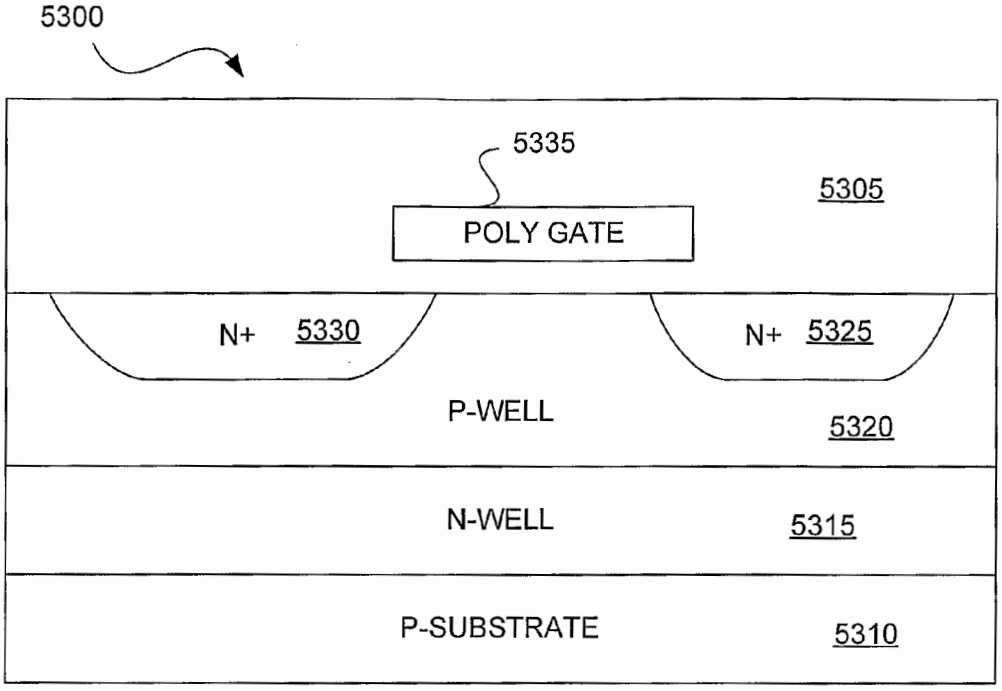

5300
5335
5305
POLY GATE
N+ 5330
N+ 5325
P-WELL
5320
N-WELL
5315
P-SUBSTRATE
5310

FIG. 53

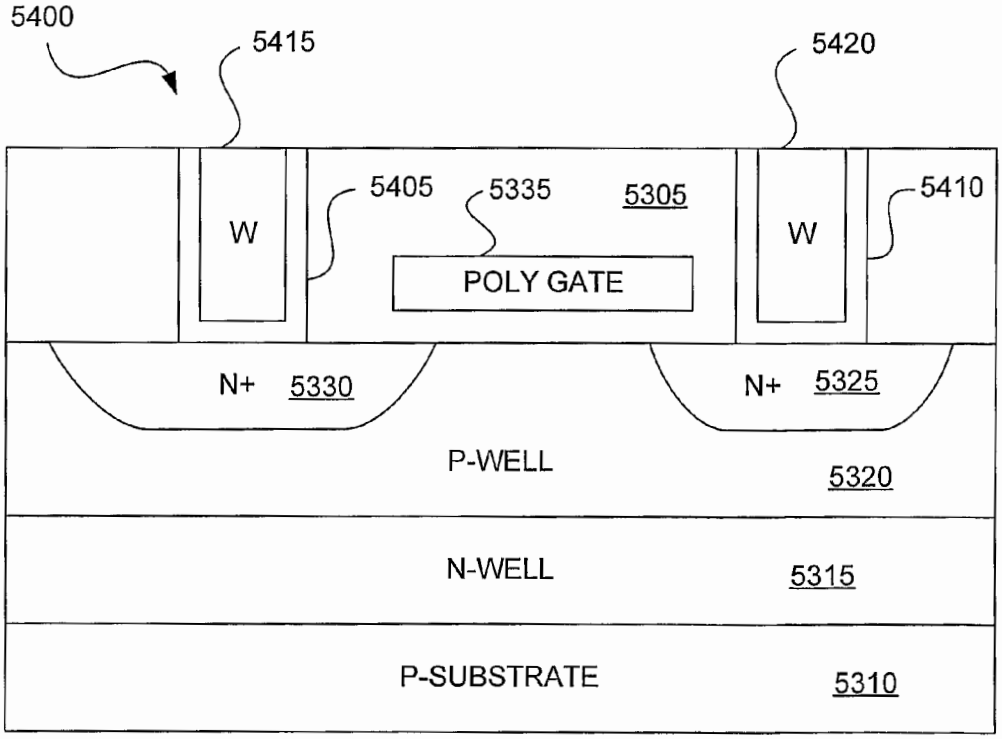

5400
5415
5420
W
5405
5335
5305
W
5410
POLY GATE
N+ 5330
N+ 5325
P-WELL
5320
N-WELL
5315
P-SUBSTRATE
5310

FIG. 54

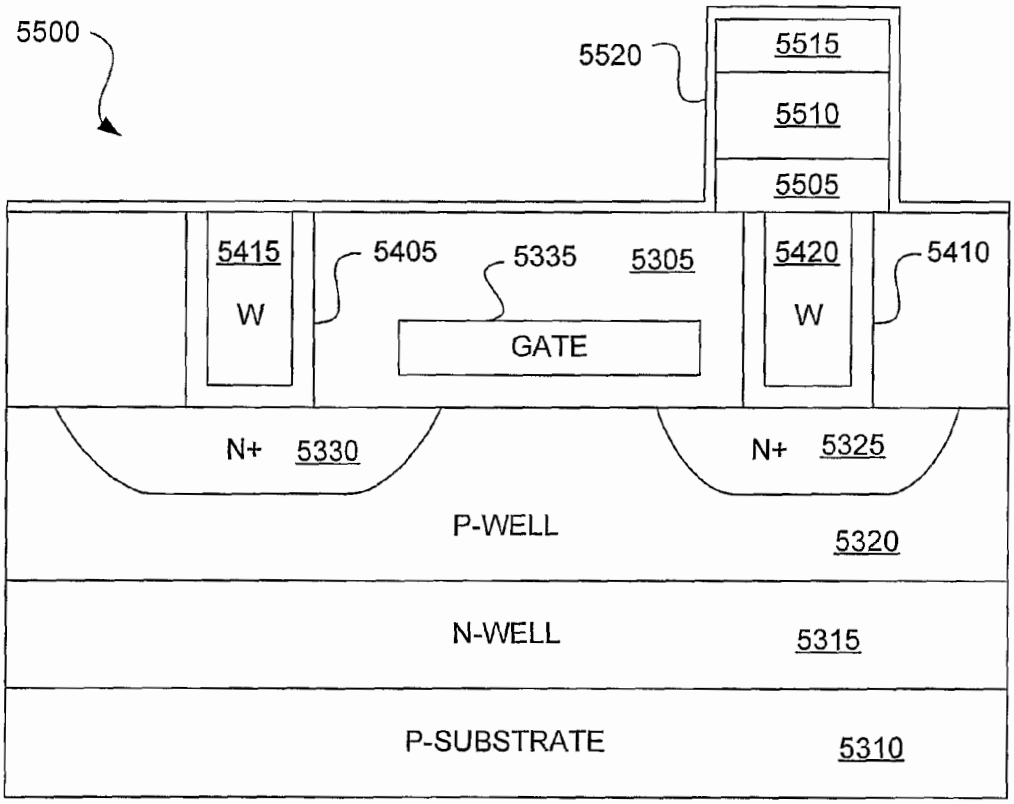

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FIG. 55

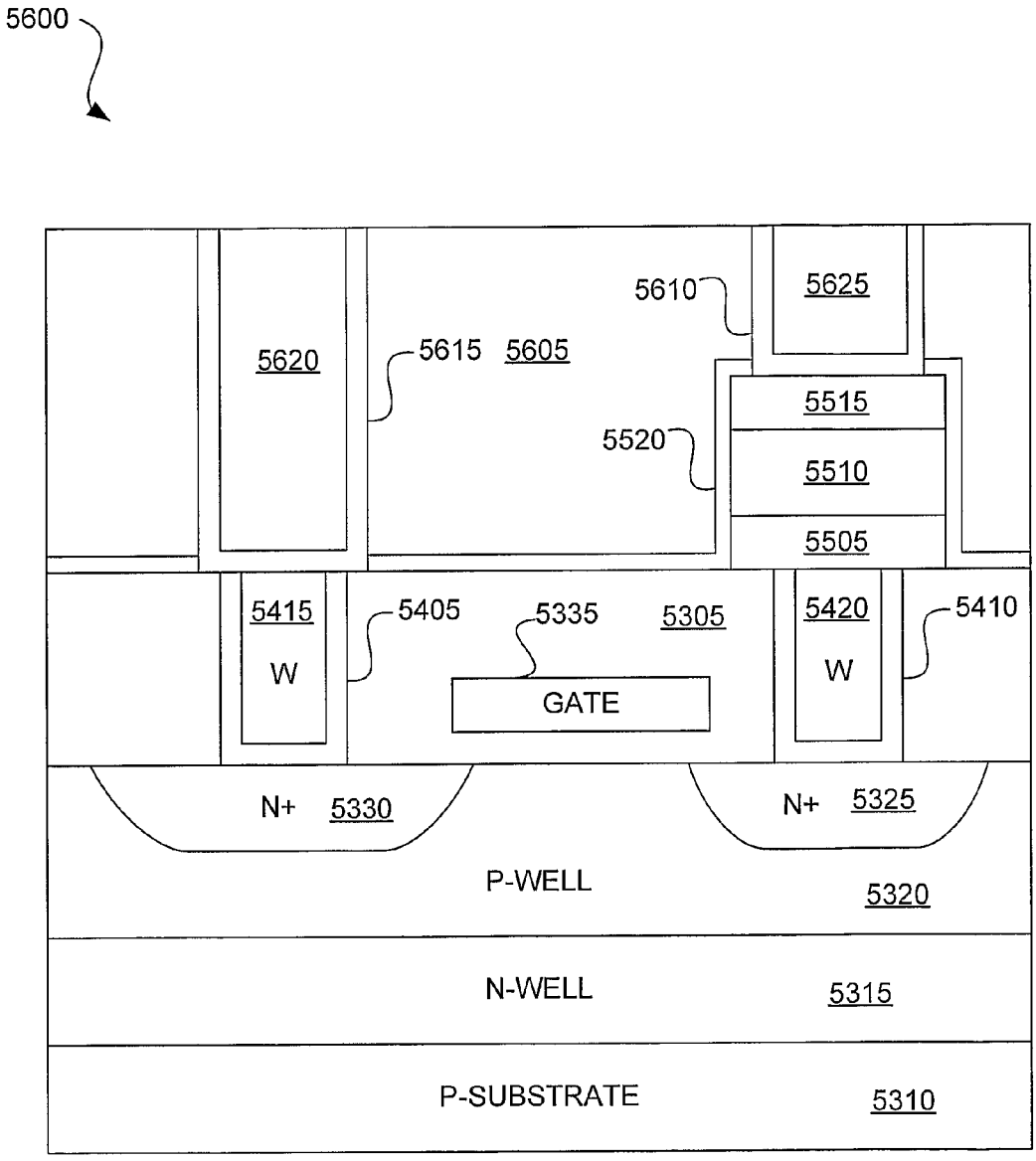

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N-WELL
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P-SUBSTRATE
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FIG. 56

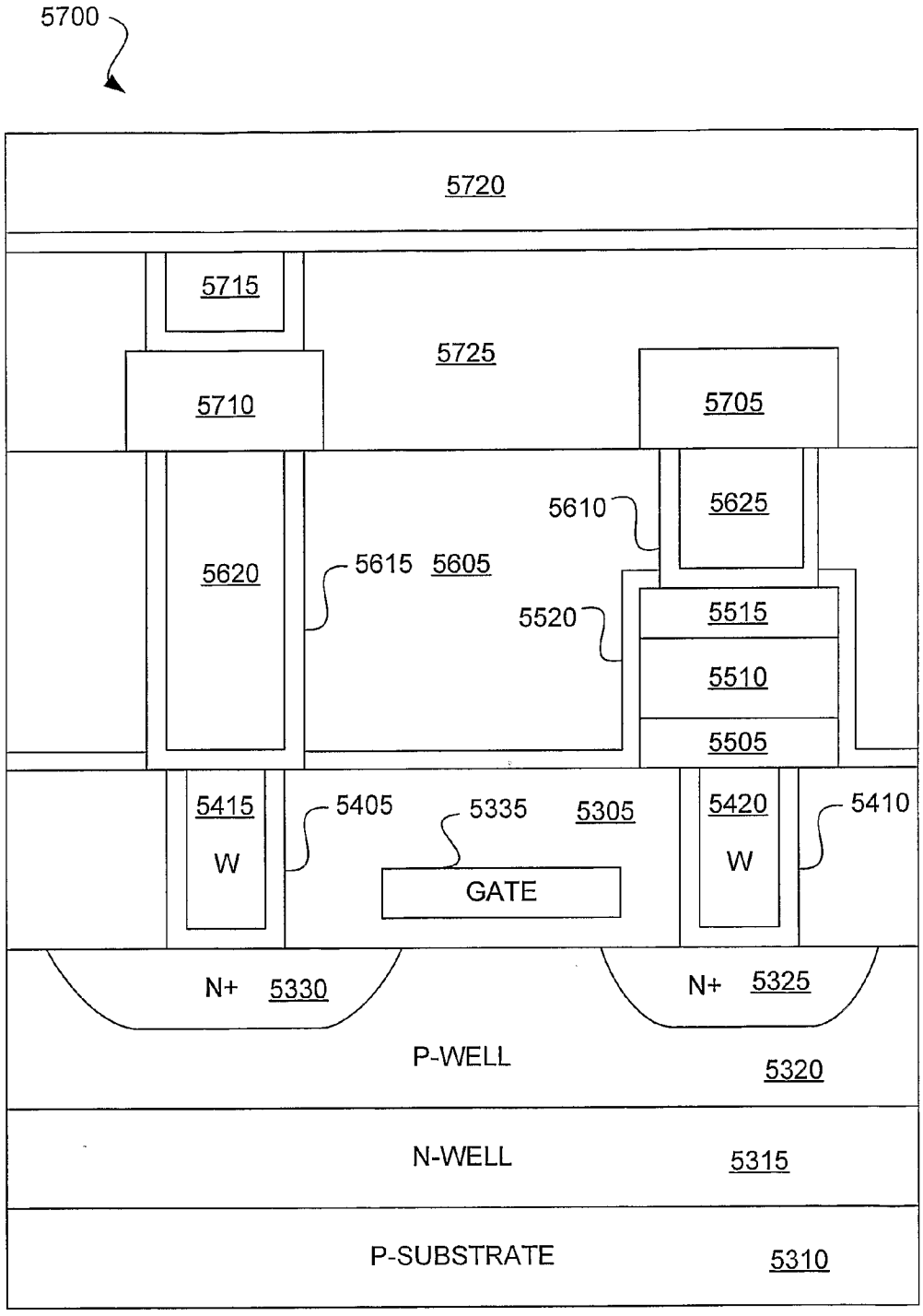

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N-WELL
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P-SUBSTRATE
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FIG. 57

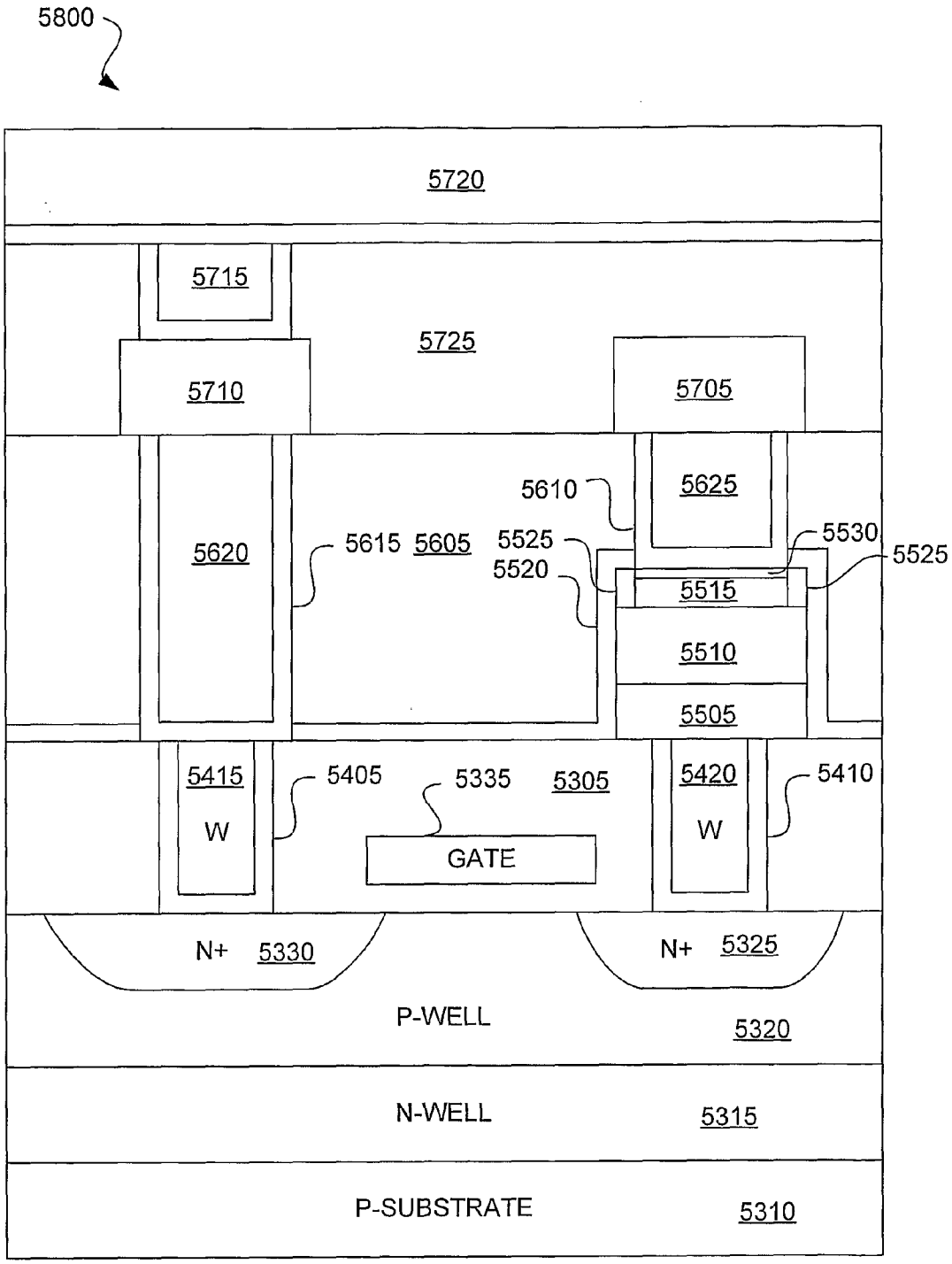

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**FIG. 58**

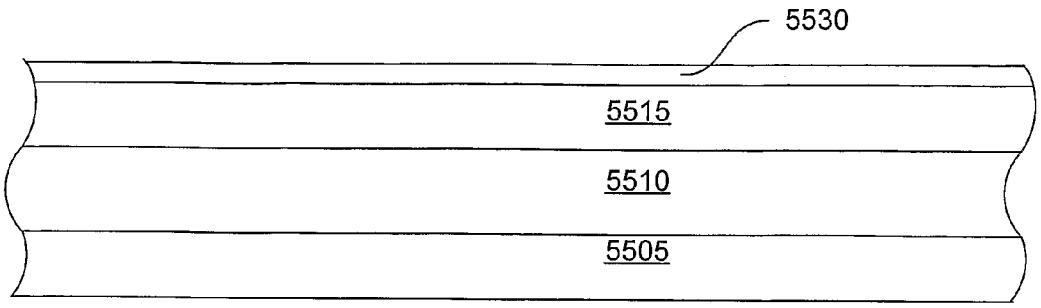



FIG. 59A

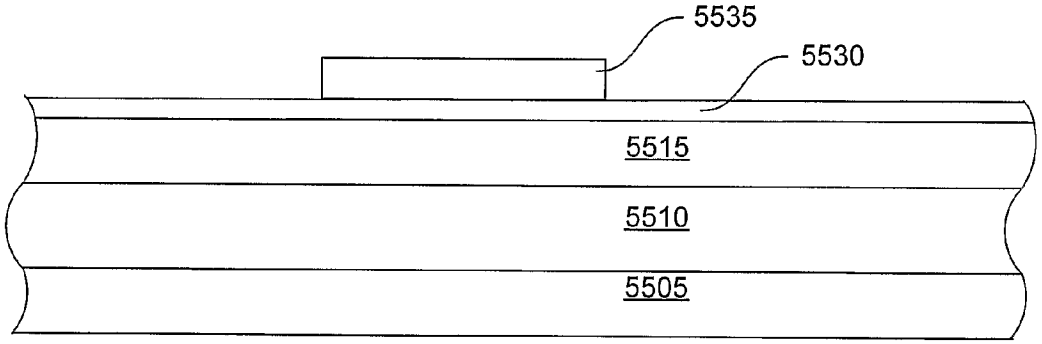



FIG. 59B

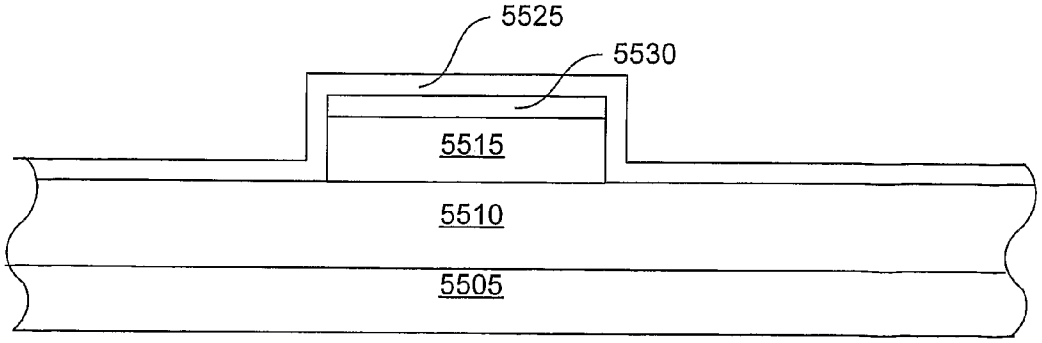



FIG. 59C

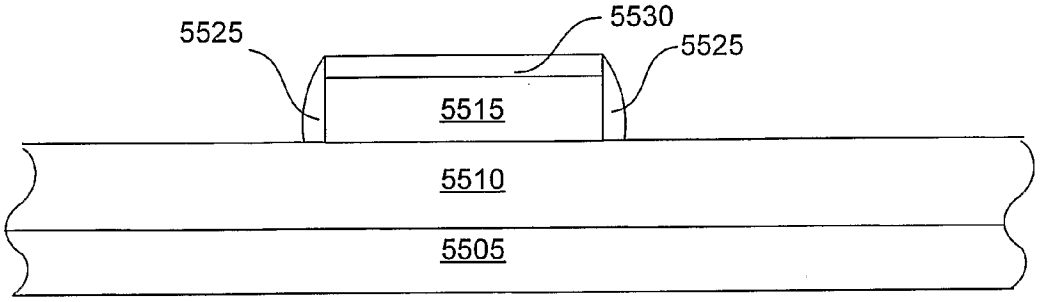



FIG. 59D

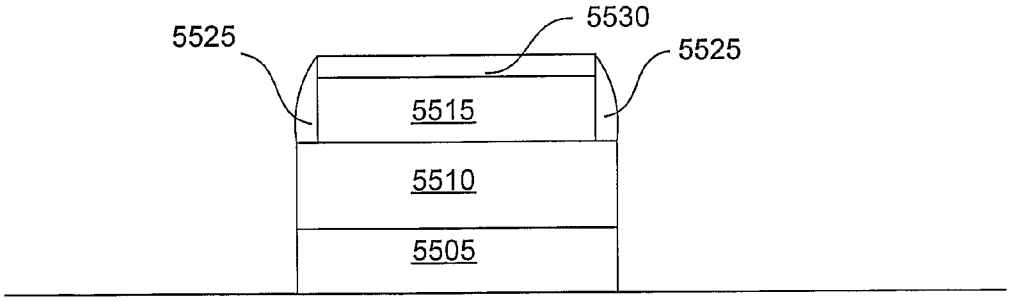



FIG. 59E

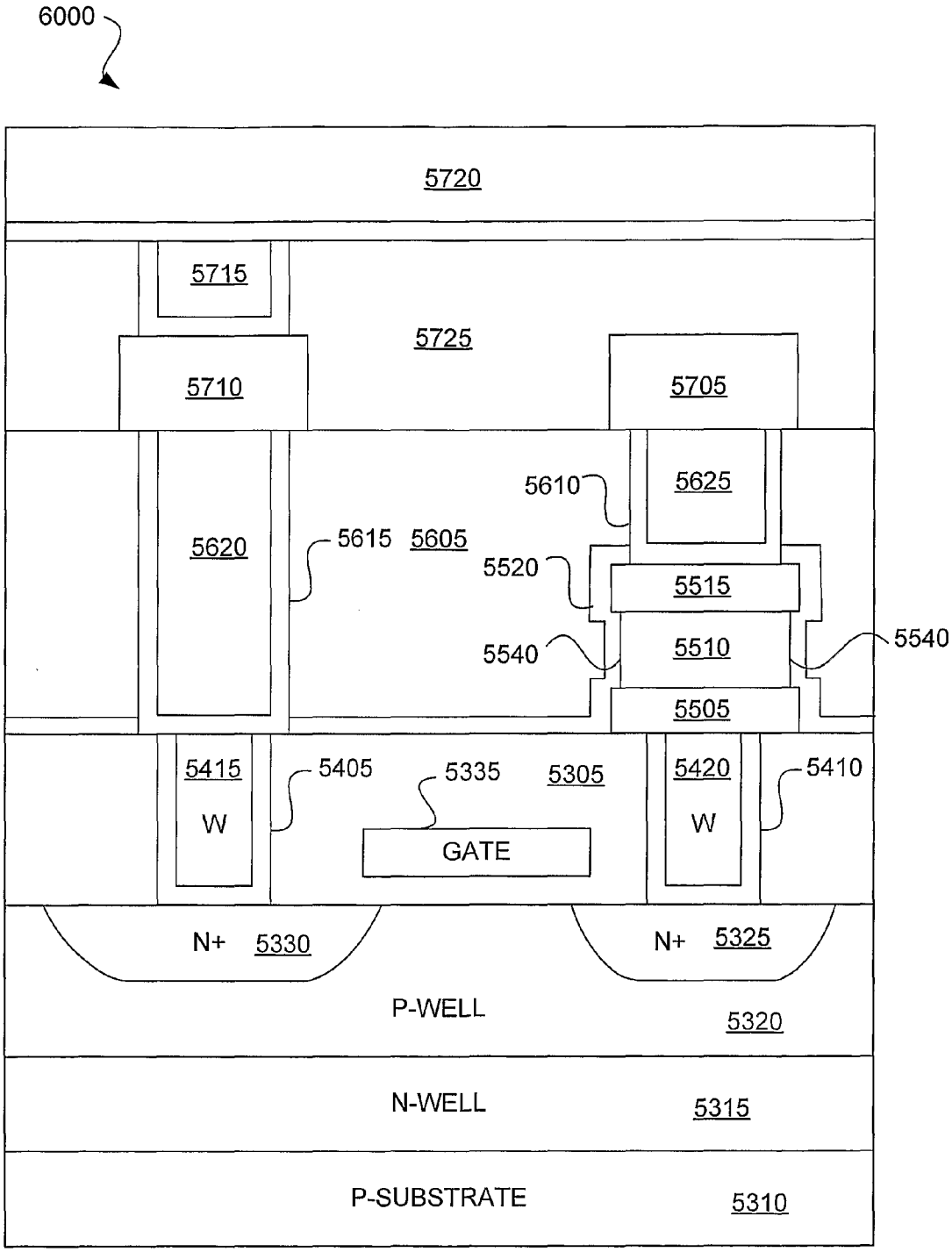

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FIG. 60

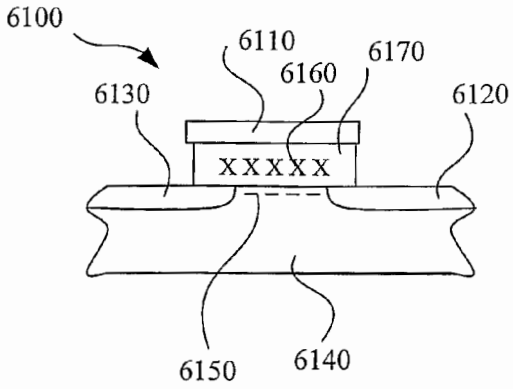



FIG. 61 (Prior Art)

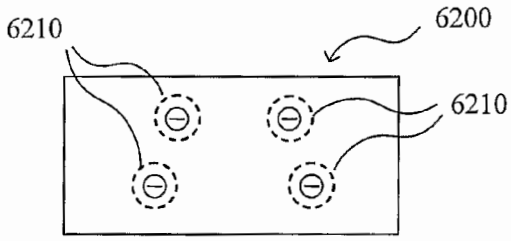



FIG. 62A

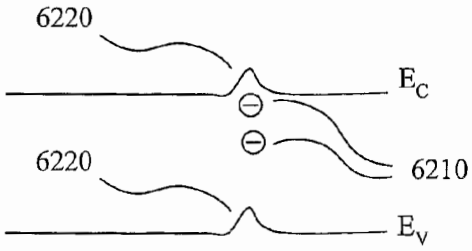



FIG. 62B

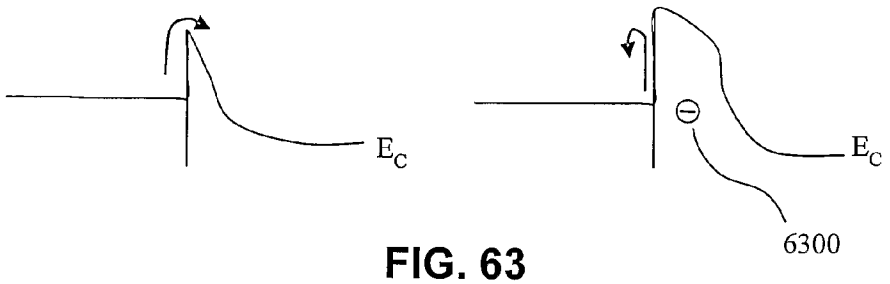



FIG. 63

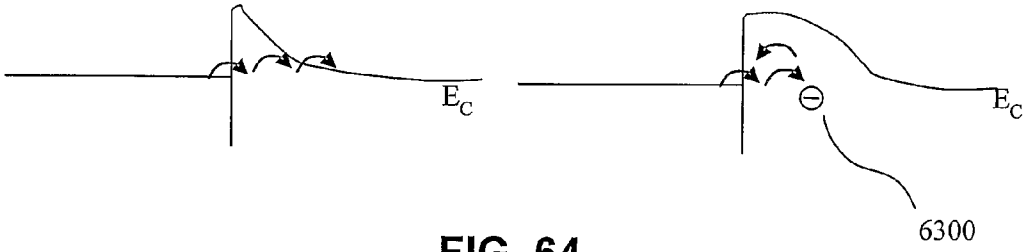



FIG. 64

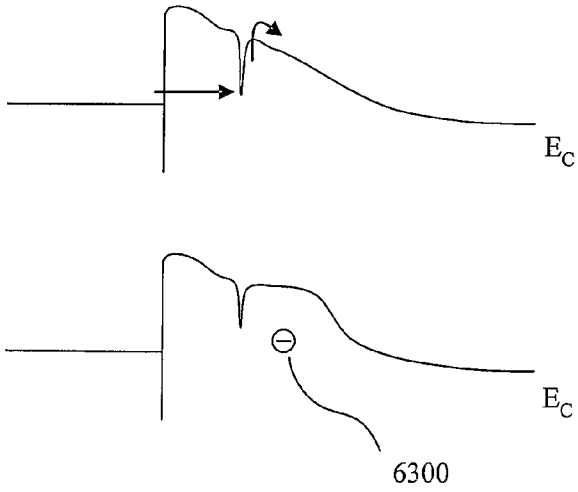



FIG. 65

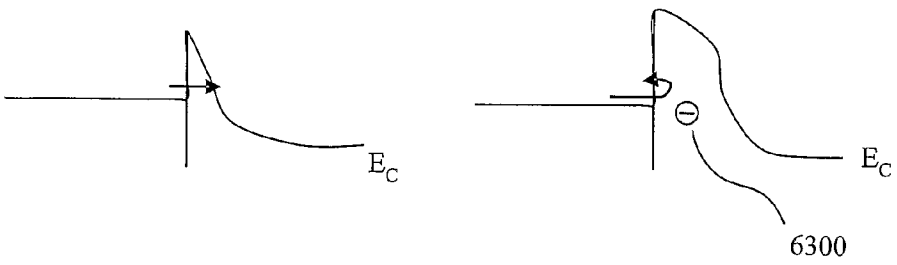



FIG. 66

# INTERNATIONAL SEARCH REPORT

PCT/US2004/013836

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | EP 1 376 598 A (SHARP KABUSHIKI KAISHA) 2 January 2004 (2004-01-02) abstract; figures 1A,2-8 paragraphs '0014! - '0022!, '0025! - '0051! | 1-7, 10-22 |
| Y | | 8,9, 23-27 |
| X | US 2003/003675 A1 (HSU SHENG TENG) 2 January 2003 (2003-01-02) abstract; figure 1 paragraphs '0006! - '0008!, '0026!, '0036! - '0039! | 1,4-9,21 |
| Y | | 8,9 |
| A | | 2,3, 10-20, 22-27 |

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 1 March 2005 | 23/03/2005 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Trifonov, A |

Form PCT/ISA/210 (second sheet) (January 2004)

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Ex. 1002, p. 713

## INTERNATIONAL SEARCH REPORT

PCT/US2004/013836

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | ZHUANG W W ET AL: "Novel colossal magnetoresistive thin film nonvolatile resistance random access memory (RRAM)" INTERNATIONAL ELECTRON DEVICES MEETING 2002. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 8 - 11, 2002, NEW YORK, NY : IEEE, US, 8 December 2002 (2002-12-08), pages 193-196, XP010626021 ISBN: 0-7803-7462-2 the whole document | 23-27 |
| A | | 1,4-6, 10,21 |

Form PCT/ISA/210 (continuation of second sheet) (January 2004)

## INTERNATIONAL SEARCH REPORT

PCT/US2004/013836

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| EP 1376598 A | 02-01-2004 | JP 2004087069 A | 18-03-2004 |
| | | EP 1376598 A1 | 02-01-2004 |
| | | US 2004036109 A1 | 26-02-2004 |
| US 2003003675 A1 | 02-01-2003 | US 2003001178 A1 | 02-01-2003 |
| | | US 2003003674 A1 | 02-01-2003 |
| | | CN 1411074 A | 16-04-2003 |
| | | JP 2003197877 A | 11-07-2003 |
| | | US 2003203585 A1 | 30-10-2003 |
| | | JP 2003068983 A | 07-03-2003 |
| | | TW 550764 B | 01-09-2003 |
| | | US 2004164332 A1 | 26-08-2004 |
| | | US 2004170048 A1 | 02-09-2004 |
| | | JP 2003068984 A | 07-03-2003 |
| | | TW 571348 B | 11-01-2004 |
| | | US 2003142578 A1 | 31-07-2003 |
| | | US 2003206481 A1 | 06-11-2003 |
| | | US 2004108528 A1 | 10-06-2004 |



Samsung Electronics Co., Ltd.
Ex. 1002, p. 715

Electronically filed September 28, 2024

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☒ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☒ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);


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Ex. 1002, p. 716

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

*(Check either Item 3a, 3b, 3c or 3d)*

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03) if it is not submitted herewith.

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

*(Items 3b or 3c to be checked if any reference known for more than 3 months)*

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

*(Check Item 4a, and 4b, 4c or 4d)*

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

*(Check either Item 5a, 5b, 5c or 5d)*


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Ex. 1002, p. 717

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

*(Check appropriate Items 7a, 7b and/or 7c)*

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,


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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

*(Check Item 9a, 9b, or 9c)*

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 28, 2024

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828


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Ex. 1002, p. 719

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

# ELECTRONIC PAYMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **09/28/2024 03:44:21 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 67363740 | AUTHORIZED BY | - |
| CUSTOMER # | 79141 | FILING DATE | 03/14/2022 |
| CORRESPONDENCE ADDRESS | - | FIRST NAMED INVENTOR | Hyun Lee |

## Payment Information

| PAYMENT METHOD | PAYMENT TRANSACTION ID | PAYMENT AUTHORIZED BY |
|---|---|---|
| **CARD / 2172** | **E20249R445018600** | **Jamie Zheng** |

| FEE CODE | DESCRIPTION | ITEM PRICE($) | QUANTITY | ITEM TOTAL($) |
|---|---|---|---|---|
| 1806 | SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT | 260.00 | 1 | 260.00 |
| | | | **TOTAL AMOUNT:** | **$260.00** |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>Substitute for Form 1449-PTO | | | | Electronically filed September 28, 2024 | |
|---|---|---|---|---|---|
| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 1 | of | 3 | Attorney Docket Number | NL070-14US03 |

| U.S. PATENT DOCUMENTS | | | | | |
|---|---|---|---|---|---|
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|---|---|---|---|---|---|
| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 2 | of | 3 | Attorney Docket Number | NL070-14US03 |

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| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **09/28/2024 03:44:21 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 67363740 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

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| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **12/07/2024 09:03:47 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 68275297 | AUTHORIZED BY | - |
| CUSTOMER # | 79141 | FILING DATE | 03/14/2022 |
| CORRESPONDENCE ADDRESS | - | FIRST NAMED INVENTOR | Hyun Lee |

## Payment Information

| PAYMENT METHOD | PAYMENT TRANSACTION ID | PAYMENT AUTHORIZED BY |
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| **CARD / 2172** | **E2024B7L04105101** | **Jamie Zheng** |

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENTS** Remove

| Examiner Initial* | Cite No | Patent Number | Kind Code[1] | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
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**( Not for submission under 37 CFR 1.99)**

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|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

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|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**CERTIFICATION STATEMENT**

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

**OR**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

**SIGNATURE**

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

| | | | |
|---|---|---|---|
| Signature | /Jamie J. Zheng/ | Date (YYYY-MM-DD) | 2024-12-07 |
| Name/Print | Jamie J. Zheng | Registration Number | 51167 |

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

# Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **12/07/2024 09:03:47 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 68275297 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 2**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| Micron_CC_Order.pdf | 45 | Non Patent Literature | 815 KB |
| CH070-14US03_IDS_SB08a_20241207.pdf | 4 | Information Disclosure Statement (IDS) Form (SB08) | 1234 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| Micron_CC_Order.pdf | 2D9CE50A237425E1CCBF2277911551CA066225B9A190F0463050E42EDE93D8D398969866E0C2B575D68C59EB76A6175D3C0F30845FE29EA6A614608153F356BD |
| CH070- | 864BA41F5F5B2555742D3B81A29A624F2A5BB80A4192B97222 |

14US03_IDS_SB08a_20241207.pdf 2B332F9AF2CF26485B951F9C1008B2984B22DF461CEFE955BA3E13D96C743EEA2310D0F2A7B767

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
**United States Patent and Trademark Office**
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www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

79141 7590 12/12/2024

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER |
|---|
| HOANG, HUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 12/12/2024 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com



Samsung Electronics Co., Ltd.
Ex. 1002, p. 737

| *Applicant-Initiated Interview Summary* | **Application No.** 17/694,649 | **Applicant(s)** Lee, Hyun | | |
|---|---|---|---|---|
| | **Examiner** HUAN HOANG | **Art Unit** 2827 | **AIA (First Inventor to File) Status** No | **Page** 1 of 1 |

| **All Participants** (applicant, applicants representative, PTO personnel) | **Title** | **Type** |
|---|---|---|
| HUAN HOANG | Primary Examiner | Video Conference |
| JAMIE ZHENG | Attorney of Record | |
| RAYMOND CHAN | Guest | |

**Date of Interview:** 09 December 2024

**Issues Discussed:**

**35 U.S.C. 112**

The Examiner agreed that the proposed amendments to the claims overcome the 112(a) rejections.

**Proposed Amendment(s)**

Applicant provided support for the amendments to the claims. The Examiner will conduct an updated search to determine patentability of the claims upon receiving the formal response.

| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |
|---|---|

**Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04**
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

**Applicant recordation instructions:** The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

**Examiner recordation instructions:** Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.



Samsung Electronics Co., Ltd.
Ex. 1002, p. 738

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>17/694,649 | Filing Date<br>03/14/2022 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY:** ☑ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED - PART I

| FOR | (Column 1)<br>NUMBER FILED | (Column 2)<br>NUMBER EXTRA | | RATE ($) | FEE ($) |
|---|---|---|---|---|---|
| ☐ BASIC FEE<br>(37 CFR 1.16(a), (b), or (c)) | N/A | N/A | | N/A | |
| ☐ SEARCH FEE<br>(37 CFR 1.16(k), (i), or (m)) | N/A | N/A | | N/A | |
| ☐ EXAMINATION FEE<br>(37 CFR 1.16(o), (p), or (q)) | N/A | N/A | | N/A | |
| TOTAL CLAIMS<br>(37 CFR 1.16(i)) | minus 20 = | * | | x $100 = | |
| INDEPENDENT CLAIMS<br>(37 CFR 1.16(h)) | minus 3 = | * | | x $480 = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | 12/12/2024 | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * 28 | Minus | ** 21 | = 7 | | x $100 = | 700 |
| | Independent<br>(37 CFR 1.16(h)) | * 6 | Minus | *** 3 | = 3 | | x $480 = | 1440 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | 2140 |

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * | Minus | ** | = | | x $0 = | |
| | Independent<br>(37 CFR 1.16(h)) | * | Minus | *** | = | | x $0 = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | |

| | |
|---|---|
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. | LIE |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". | /ANTJUAN M RIVERA/ |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". | |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. | |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

# ELECTRONIC PAYMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **12/12/2024 01:42:17 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 68336573 | AUTHORIZED BY | - |
| CUSTOMER # | 79141 | FILING DATE | 03/14/2022 |
| CORRESPONDENCE ADDRESS | - | FIRST NAMED INVENTOR | Hyun Lee |

## Payment Information

| PAYMENT METHOD | PAYMENT TRANSACTION ID | PAYMENT AUTHORIZED BY |
|---|---|---|
| **CARD / 2172** | **E2024BB242439105** | **Jamie Zheng** |

| FEE CODE | DESCRIPTION | ITEM PRICE($) | QUANTITY | ITEM TOTAL($) |
|---|---|---|---|---|
| 1202 | EACH CLAIM IN EXCESS OF 20 | 100.00 | 7 | 700.00 |
| 1201 | EACH INDEPENDENT CLAIM IN EXCESS OF THREE | 480.00 | 3 | 1440.00 |
| 1253 | EXTENSION FOR RESPONSE WITHIN THIRD MONTH | 1480.00 | 1 | 1480.00 |
| | | | **TOTAL AMOUNT:** | **$3,620.00** |

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement

Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

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PTO/SB/92 (05-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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   P.O. Box 1450
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   on _____ ,
   Date

2. ☐ Facsimile transmitted to the United States Patent and Trademark Office, or

   OR

3. ☑ Transmitted via the USPTO's patent electronic filing system (Patent Center or EFS-Web).

| /Jamie J. Zheng/ | December 11, 2024 |
|---|---|
| Signature | Date |
| Jamie J. Zheng | 51,167 |
| Typed or printed name | Telephone number |

Note: Each paper must have its own certificate of mailing or transmission, or this certificate must identify each submitted paper:

US Pat. Appl. No. 17/694,649 - Response to Non-Final Office Action

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*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

# Privacy Act Statement

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Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

**Additional Uses**

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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **12/12/2024 01:42:17 AM Z ET** | **NL070-14US03** |

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MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

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| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 68336573 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 4**

| DOCUMENT | | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|---|
| Certificate_Transmission_sb0092.pdf | | 2 | Transmittal Letter | 747 KB |
| NL070-14US03_Amendment_NFOA_aft_RCE2.pdf | | 31 | - | 298 KB |
| NL070-14US03_Amendment_NFOA_aft_RCE2-A....pdf | (1-1) | 1 | Amendment/Request for Reconsideration-After Non-Final Rejection | 106 KB |
| NL070-14US03_Amendment_NFOA_aft_RCE2-CLM.pdf | (2-22) | 21 | Claims | 208 KB |
| NL070-14US03_Amendment_NFOA_aft_RCE2-REM.pdf | (23-31) | 9 | Applicant Arguments/Remarks Made in an Amendment | 159 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| Certificate_Transmission_sb0092.pdf | 3A28B12B94969E889AB138A254C4322497ADD113D710BD8316380C449687DDA033E8A815B4B1E29CA6F6833F0E0B071F680F8CA2A18740D61DE15FBBFAE9F7AD |
| NL070-14US03_Amendment_NFOA_aft_RCE2.pdf | 1A3BA8D7691654CCC057AEF6ACE1A947C2BB446C7BFF373B8E833FBAC4BA069CDC6796CDC28B204C06868662FC602FF68A848A966C7BBB2FEFD88AE78B90EB73 |
| NL070-14US03_Amendment_NFOA_aft_RCE2-A....pdf | FE31890B642E8C33163A9807B468E811D96D8E443897013D6EA04D7FDEE8E5B000E94445374CD9F0DFB173323C970E8EB29F6DCFC2BBD81A5447E7E6DE4B5085 |
| NL070-14US03_Amendment_NFOA_aft_RCE2-CLM.pdf | B65CF528613A66125391B48B2EE2E9300E091C9953A591AEB9DD8CCF645BF392096F61C143FC312722DF1EF71BFB84C6AED8CBF28106EA76516F923F7BF82801 |
| NL070-14US03_Amendment_NFOA_aft_RCE2-REM.pdf | 62C00C29D97805E99E79A9C786D223EEF08B6AB6D72C531009B0A1A289B6AD51965FF1060D20C5624A99B5C67B41AD4790F90ACE6F7FF95DE76D8C48D162EE2D |

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed December 11, 2024

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION**

**Mail Stop: Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is submitted in response to the non-final office action dated June 11, 2024.

Applicant petitions for a three-month extension of time, which extends the due date for responding to the Office Action from September 11, 2024, to December 11, 2024.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).


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## Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked ~~array~~ DRAM dies including at least a first plurality of ~~array~~ DRAM dies and a second plurality of ~~array~~ DRAM dies, each DRAM die of the stacked ~~array~~ DRAM dies including data ports and DRAM memory cells, wherein the each ~~array~~ DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including ~~control~~ command and/or address (C/A) terminals~~, via which the DRAM package receives command/address signals,~~ and data terminals, ~~via which~~ wherein the DRAM package ~~receives or outputs~~ is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the ~~command/address~~ (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals ~~control interconnects coupled to respective ones of the control terminals~~, each of the ~~control~~ die interconnects including one or more through silicon vias (TSVs) in one or more ~~array~~ DRAM dies in the stacked ~~array~~ DRAM dies and configured to conduct signals to and/or from ~~a command/address signal to~~ the one or more ~~array~~ DRAM dies in the stacked array dies through the one or more TSVs;

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits corresponding, respectively, to the die interconnects, wherein each die interconnect is coupled to a respective one of the conduits, the conduits including CA conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects, the data conduits including at least first data conduits coupled


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to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

wherein a first data interconnect of the first data interconnects ~~configured to conduct first data signals to respective~~ is in electrically communication with data ports on the first plurality of ~~array~~ DRAM dies and not ~~to data ports~~ in electrical communication with any data port on any of the second plurality of ~~array~~DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of ~~array~~ DRAM dies and at least one TSV in at least one ~~first array~~ DRAM die of the second plurality of ~~array~~ DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is electrically connected to a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one ~~first array~~ DRAM die ~~does not conduct any data signal~~ is not electrically connected to any data port on the at least one ~~first array~~ DRAM die;

wherein a second data interconnect of the second data interconnects is in electrically communication with data ports on a second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the data conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;


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wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects;

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies

~~second data interconnects configured to conduct second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies, each of the second data interconnects including a TSVthe at least one second array die does not conduct any data signal to any data port on the at least one second array die; and~~

~~drivers coupled to the data terminals and including first drivers configurable to drive the first data signals received via the data terminals to the first plurality of array dies via the first data interconnects and second drivers configurable to drive the second data signals received via the data terminals to the second plurality of array dies via the second data interconnects, a respective signal of the first data signals to be driven by a respective one of the first drivers configured to have a first driver size, a respective signal of the second data signals to be driven by a respective one of the second drivers configured to have a second driver size different from the first driver size, the first driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the first drivers, the second driver size corresponding to a transistor size and/or a number of transistors included in the respective one of the second drivers;~~


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~~wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of a respective first data interconnect and not to any data port on any of the second plurality of array dies; and~~

~~wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of a respective second data interconnect and not to any data port on any of the first plurality of array dies~~.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked ~~array~~ DRAM dies, the stacked ~~array~~ DRAM dies including a first plurality of ~~array~~ DRAM dies and a second plurality of ~~array~~ DRAM dies, each ~~array~~ DRAM die of the stacked ~~array~~ DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each ~~array~~ DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports, the DRAM package further including an interface ~~control terminals~~, via which the DRAM package receives ~~command/address~~ C/A signals, and ~~data terminals,~~ via which the DRAM package receives or outputs data signals in response to ~~the command/address~~ C/A signals received via the interface, the interface including terminals, the DRAM package further including die interconnects, each of the die ~~control interconnects coupled to respective ones of the control terminals, each of the control~~ interconnects including one or more through silicon vias (TSVs) in one or more ~~array~~ DRAM dies in the stacked ~~array~~ DRAM dies ~~and configured to conduct a command/address signal to one or more array dies in the stacked array dies~~, the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects, the data interconnects including first data interconnects,

receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;


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in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;

wherein each of the first data interconnects is in electrically communication with data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies, each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is electrically connected to a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not electrically connected to any data port on the at least one DRAM die;

wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked array dies and second unidirectional interconnects are not configured to conduct any signals from any of the stacked array dies;

the first data signals include at least 32 signals driven in parallel; and

the second data signals include at least 32 signals driven in parallel

~~driving first data signals received at respective data terminals to the first plurality of array dies via respective first data interconnects, including enabling a first driver having a first driver size to drive a respective signal of the first data signals receive via a respective data terminal to~~


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~~the first plurality of array dies via a respective first data interconnect of the first data interconnects, each of the first data interconnects including a first plurality of TSVs, the first plurality of TSVs including a TSV in each of in the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies, wherein the at least one TSV in the at least one first array die does not conduct any data signal to any data port on the at least one first array die; and~~

~~driving second data signals received at respective data terminals to the second plurality of array dies via respective second data interconnects, including enabling a second driver having a second driver size to drive a respective signal of the second data signals receive via the respective data terminal to the second plurality of array dies via a respective second data interconnect of the second data interconnects, each of the second data interconnects including a second plurality of TSVs, the second plurality of TSVs including a TSV in each of the second plurality of array dies and at least one TSV in at least one second array die of the first plurality of array dies, wherein the at least one TSV in the at least one second array die does not conduct any data signal to any data port on the at least one second array die, the second driver size being different from the first driver size;~~

~~wherein the first data interconnects are configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and wherein the second data interconnects are configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to data ports on any of the first plurality of array dies;~~

~~wherein the respective signal of the first data signals is driven to corresponding data ports of the first plurality of array dies through TSVs of the respective first data interconnect and not to any data port on any of the second plurality of array dies; and~~

~~wherein the respective signal of the second data signals is driven to corresponding data ports on the second plurality of array dies through TSVs of the respective second data interconnect and not to any data port on any of the first plurality of array dies; and~~

~~wherein the first driver size corresponds to a transistor size and/or a number of transistors included in the first driver, and the second driver size corresponds to a transistor size and/or a number of transistors included in the second driver~~.


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3. (Currently Amended) The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies ~~the respective one of the first drivers includes at least one first transistor having a first transistor size and the respective one of the second drivers includes at least one second transistor having a second transistor size that is different from the first transistor size~~.

4. (Currently Amended) The DRAM package of claim 3[[1]], wherein the stacked DRAM dies include 16 stacked DRAM dies.

~~the respective one of the first drivers includes a first number of transistors and the respective one of the second drivers includes a second number of transistors, the second number being different from the first number.~~

5. (Currently Amended) The DRAM package of claim 1, wherein:

the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size~~each of the second plurality of array dies is stacked over at least one of the first plurality of array dies~~; and

the second driver size is ~~greater than~~ different from the first driver size.

6. (Currently Amended) The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel ~~driver size corresponds to a first load associated with the first plurality of array dies and one of the first data interconnects, and the second driver size corresponds to a second load associated with the second plurality of array dies and one of the second data interconnects, and wherein the first load and the second load are balanced by the first data interconnects being configured to conduct the first data signals to respective data ports on the first plurality of array dies and not to data ports on any of the second plurality of array dies, and by the second data interconnects being configured to conduct the second data signals to respective data ports on the second plurality of array dies and not to any data ports on any of the first plurality of array dies~~.

7. (Currently Amended) The DRAM package of claim 1, wherein:


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~~the first data signals are associated with first command/address signals received via the control terminals,~~ the first set of C/A signals include ~~command/address signals including~~ one or more signals to select one ~~array~~ DRAM die among the first plurality of ~~array~~ DRAM dies to ~~receive data in~~ output the first data ~~signals~~; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals.

8. (Currently Amended) The DRAM package of claim 1 ~~7, further comprising a control die between the stacked array dies and the terminals~~, wherein the control die is further configured to control timing of command/address signals driven to the stacked ~~array~~ DRAM dies and/or timing of data signals communicated between the stacked ~~array~~ DRAM dies and the data terminals to prevent signal collisions.

9. (Currently Amended) The method of claim 2, wherein the stacked DRAM dies include at least 8 stacked DRAM dies ~~wherein each of the first driver and the second driver includes one or more transistors, wherein enabling the first driver having the first driver size includes enabling at least one first transistor having the first transistor size and coupled to the first data interconnect, and wherein enabling the second driver having the second driver size includes enabling at least one second transistor having the second transistor size and coupled to the second data interconnect, the second transistor size being different from the first transistor size~~.

10. (Currently Amended) The method of claim 2, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel ~~each of the first driver and the second driver~~ includes ~~a set of transistors, wherein enabling the first driver having the first driver size includes enabling~~ a first number of transistors coupled to ~~the~~ a respective first data interconnect, and wherein ~~enabling~~ each of the second drivers ~~having the second driver size includes enabling~~ has a second number of transistors coupled to ~~the~~ a respective second data interconnect, the second number being different from the first number.


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11. (Currently Amended) The method of claim 2, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:

enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals; ~~the first data signals are associated with first command/address signals received via the control terminals,~~

enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals~~the first command/address signals including one or more signals to select one array die among the first plurality of array dies to receive the first data signals~~; and

maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;

wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked ~~array~~ DRAM dies, each ~~array~~ DRAM die of the plurality of stacked ~~array~~ DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each ~~array~~ DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to ~~command/address~~ C/A signals received via the ~~command/address~~ C/A ports;

~~terminals including control terminals,~~ an interface, via which the DRAM package receives command/address (C/A) signals, and ~~data terminals,~~ via which the DRAM package receives or outputs data signals ~~in response to the command/address signals~~, the interface including C/A terminals and data terminals;

~~control interconnects coupled to the control terminals, each of the control interconnects including one or more through silicon vias (TSVs) in one or more array dies in the plurality of stacked array dies and configurable to conduct a command/address signal received at a respective control terminal of the control terminals to one or more array dies in the plurality of stacked array dies; and~~

die ~~data~~ interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and


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a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;

wherein:

the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;

each of the first data interconnects is configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked ~~array~~ DRAM dies and is not configured to be in electrical communication with any data port on any ~~other array die~~ of ~~the plurality of stacked array dies that is not in the~~ a second subset of the plurality of stacked ~~array~~ DRAM dies;

each of the second data interconnects ~~include first data interconnects~~ is configured to be in electrical communication with ~~a first~~ a corresponding data port of each of the second subset of ~~array dies in~~ the plurality of stacked ~~array~~ DRAM dies and is not configured to be in electrical communication with any ~~other array die~~ data port of the first subset of the plurality of stacked ~~array~~ DRAM dies, each subset of the first subset and the second subset of the plurality of stacked DRAM ~~array~~ dies including ~~a first plurality of~~ two or more DRAM dies;

the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to at least the first subset of the plurality of stacked DRAM dies via at least the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to at least the second subset of the plurality of stacked DRAM dies via at least the second C/A interconnects;

the ~~command/address signals received via the control terminals include~~ first set of C/A signals include one or more first signals to select ~~an array~~ a first DRAM die in the first subset of the plurality of stacked ~~array~~ DRAM dies to respond to the first set of C/A ~~command/address~~ signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data


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signals associated with the second set of C/A signals between the second data interconnects and the interface;

the control die is further configurable to, in response to the first or second set of C/A signals being for a memory read operation, receive one or more signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the first or second set of C/A signals being for a memory write operation, drive one or more signals associated with the memory write operation to one or more of the second unidirectional interconnects;

the first unidirectional interconnects are configured to conduct signals from one or more DRAM dies of the plurality of stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

the second unidirectional interconnects are configured to conduct signals from the control die to one or more DRAM dies of the plurality of stacked DRAM dies and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;

the control die is configurable to receive signals from one or more DRAM dies of the plurality of stacked DRAM dies via the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

the control die is configurable to drive signals to one or more DRAM dies of the plurality of stacked DRAM dies via the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective ~~array~~ DRAM dies in the first subset of ~~array~~ DRAM dies and at least one second TSV in at least one second ~~array~~ DRAM die of the second subset of plurality of stacked ~~array~~ DRAM dies~~, wherein the at least one second array die is not in the first subset of array dies, wherein each of the at least one second TSV in a corresponding array die of the at least one second array die is not in electrical communication with any active circuitry on the corresponding array die~~;


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a respective TSV of the first subset of TSVs in a respective ~~array~~ DRAM die of the first subset of ~~array~~ DRAM dies is in electrical communication with a corresponding data port on the respective ~~array~~ DRAM die in the first subset of ~~array~~ DRAM dies; and

each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the ~~at least one second~~corresponding ~~array~~ DRAM die.

13. (Cancelled)

14. (Currently Amended) The DRAM package of claim 12, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies ~~the data interconnects further include second data interconnects configured to be in electrical communication with a second subset of array dies in the plurality of stacked array dies and not in electrical communication with any other array die of the plurality of stacked array dies, the second subset of array dies including a second plurality of array dies, the DRAM package further comprising first drivers, second drivers, and pre-drivers, wherein a respective first driver of the first drivers is configurable to drive a first data signal to the first plurality of array dies via a respective one of the first data interconnects, a respective second driver of the second drivers is configurable to drive a second data signal to the second plurality of array dies via a respective one of the second data interconnects, and a respective pre-driver is coupled between a respective data terminal of the date terminals and one or more of the respective first driver and the respective second driver~~.

15. (Currently Amended) The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies ~~each of the at least one second TSV includes a conducting material in the corresponding array die of the at least one second array die and an insulator or air gap between the conducting material and a data port on the corresponding array die~~.

16. (Currently Amended) The DRAM package of claim 12[[14]], wherein the each of the at least one second TSV in the corresponding ~~array~~ DRAM die of the at least one second ~~array~~ DRAM die is connected to one or more electrical connections leading from the at least one second TSV ~~a stub on the corresponding array die, and wherein the stub is~~, the one or more electrical


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connections are not configured to provide any electrical communication with memory cells on the corresponding ~~array~~ DRAM die.

17. (Currently Amended) The DRAM package of claim 12, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby: ~~further comprising drivers coupled to the control terminals and configured to drive the command/address signals to the plurality of stacked array dies~~

the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;

the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;

each of the first data conduits are placed in a non-driving state after driving the first data signals;

each of the second data conduits are placed in a non-driving state after driving the second data signals; and

data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.

18. (Cancelled)

19. (Currently Amended) The DRAM package of claim 12[[18]], ~~further comprising a control die between the stacked array dies and the terminals,~~ wherein the control die is configured to control timing of the first set of C/A signal, the second set of C/A signals, ~~command/address signals driven to the plurality of stacked array dies and/or timing of~~ the first data signals , and/or the second data signals between the ~~data terminals~~ interface and the plurality of stacked ~~array~~ DRAM dies to prevent data collisions.

20. (Currently Amended) The DRAM package of claim 12[[18]], wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via


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the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel ~~respective first driver includes a first number of transistors and the respective second driver includes a second number of transistors, the second number being different from the first number~~.

21. (Currently Amended) The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not ~~each of the at least one TSV in the at least one first array die is connected to a stub on a corresponding first array die of the at least one first array die and the stub on the corresponding first array die is not in electrical communication with memory cells~~ electrically connected to any data port on the at least one DRAM die ~~corresponding first array die, and wherein each of the at least one TSV in the at least one second array die is connected to a stub on a corresponding second array die of the at least one second array die and the stub on the corresponding second array die is not in electrical communication with memory cells on the corresponding second array die~~.

22. (Cancelled)

23. (New) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A


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signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and to drive signals to the one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to any of the one or more DRAM dies via any of the first unidirectional interconnects or to receive any signal from any of the one or more DRAM dies via any of the second unidirectional interconnects;


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wherein, in response to the first set of C/A signals, the control die is configured to receive first signals associated with the memory read operation from the one or more DRAM dies via the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive second signals associated with the memory write operation to the one or more DRAM dies via the second unidirectional interconnects;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM- dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

24. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a


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corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and to drive signals to the one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to any of the one or more DRAM dies via any of the first unidirectional interconnects or to receive any signal from any of the one or more DRAM dies via any of the second unidirectional interconnects;

wherein, in response to the first set of C/A signals, the control die is configured to receive first signals associated with the memory read operation from the one or more DRAM dies via the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive second signals associated with the memory write operation to the one or more DRAM dies via the second unidirectional interconnects;

wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second


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supply voltage interconnect is configured to conduct the supply voltage to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

25. (New) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;

an interface via which the DRAM package receives C/A signals and receives or outputs data signals;

a control die coupled between the interface and the stacked DRAM dies, the control die including signal conduits and logic configured to control at least some of the signal conduits; and

die interconnects, each die interconnect of the die interconnects coupled to between one corresponding conduit in the control die and one corresponding signal port in each of one or more of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;

wherein:

the conduits include first conduits, second conduits, third conduits and fourth conduits;

the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;

each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;

each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;


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each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;

the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;

in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second interconnects and to drive the first signals to the interface; and a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third interconnect and drive the one or more second signals to the interface;

in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second interconnects; and a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth interconnect;

in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second interconnects and to drive the fifth signals to the interface; and a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third interconnect and drive the one or more sixth signals to the interface;


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in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the first subset of the first interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second interconnects; and a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth interconnect;

each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;

the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;

the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;

the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

26. (New) The DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;

the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and

the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;


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a data conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.

27. (New) The DRAM package of claim 25, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, and wherein:

the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;

the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;

the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals; and

the fourth set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the seventh signals and the one or more eighth signals.

28. (New) The DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

29. (New) The DRAM package of claim 28, wherein the stacked DRAM dies include 16 stacked DRAM dies.

30. (New) The DRAM package of claim 23, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

31. (New) The DRAM package of claim 23, wherein:

the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.


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*REMARKS*

This amendment is submitted in response to the Non-Final Office Action dated June 11, 2024 (the "Office Action"). In the Office Action, the examiner:

- rejected claims 1-12 and 14-22 under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as filing to comply with the written description requirement.

REMARKS CONCERNING CLAIMS

Claims 1-12, 14-17, and 19-21 are amended.

Claims 18 and 22 are cancelled

New claims 23-31 are presented.

Support for the amendments can be found in the specification and drawings as filed (e.g., paragraph [0042], [0044], [0051], [0068], [0073], [0091], [0100], [0103], [0105]-[0108], and FIGS. 3-4 and related descriptions). Therefore, no new matter is added.

After entry of this amendment, the pending claims are: claims 1-12, 14-17, 19-21 and 23-31.

EXAMINER INTERVIEW SUMMARY

Applicant's representatives thank Examiner Hoang for the opportunity to discuss the above-referenced patent application during an examiner interview with Jamie Zheng, Tobin Hobbs, and Raymond Chan on December 9, 2024. During the interview, support for certain limitations in a proposed claim amendment is discussed. Some agreements were reached, and Examiner Hoang stated that more time would be needed to consider the proposed claim amendment.

REMARKS CONCERNING CLAIM REJECTIONS

Claims 1-12 and 14-22 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as filing to comply with the written description requirement.


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The Office Action points to FIGS. 2 and 3 for not showing that "the first respective set of TSVs including a TSV in each of the first plurality of array dies and at least one TSV in at least one first array die of the second plurality of array dies," as recited in the previously presented claims 1 and 12 (emphasis added).

Applicant respectfully submits that, although not shown in FIGS. 2 and 3, the written description supports the above-quoted limitations in previously presented claims 1 and 12. For example, the specification in para. [0041] states that "the die interconnects 220 (which is used to refer to either or both of die interconnects 220a and 220b) may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect." Further, the specification provides in the same para. [0041] that "the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same."

Nonetheless, the above limitations have been replaced in claims 1 and 12 by other limitations. Therefore, the reasons stated in the Office Action for rejecting claims 1-12 and 14-22 under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as filing to comply with the written description requirement, are now moot

Claim 1 as amended is provided in clean form below with annotations in parenthesis to show examples of support for newly introduced limitations:

> A dynamic random access memory (DRAM) package, comprising:
>
> stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
>
> terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to


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receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation; **(*para. [0044] and throughout the specification*)**

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked array dies through the one or more TSVs;

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits corresponding, respectively, to the die interconnects, wherein each die interconnect is coupled to a respective one of the conduits, the conduits including CA conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

wherein a first data interconnect of the first data interconnects is in electrically communication with data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first


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respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is electrically connected to a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die is not electrically connected to any data port on the at least one DRAM die;

wherein a second data interconnect of the second data interconnects is in electrically communication with data ports on a second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the data conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal; **(*e.g., para. [0073], [0100], [0105]*)**

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die; **(*e.g., para. [0068]*)**


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wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects;

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects; ***(e.g., para. [0068])***

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies. ***(e.g., para. [0046], [0108])***

Claim 12 as amended is provided in clean form below with annotations in parenthesis to show examples of support for newly introduced limitations:

A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports;


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an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including C/A terminals and data terminals;

die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and

a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;

wherein:

the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects; ***(e.g., para. [0051], [0068])***

each of the first data interconnects is configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;

each of the second data interconnects is configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies, each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to at least the first subset of the plurality of stacked DRAM dies via at least the first C/A interconnects, and is further configurable to drive a second set of C/A


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signals received by the DRAM package via the interface to at least the second subset of the plurality of stacked DRAM dies via at least the second C/A interconnects; **(*e.g., para. [0051]*)**

the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

the control die is further configurable to, in response to the first or second set of C/A signals being for a memory read operation, receive one or more signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the first or second set of C/A signals being for a memory write operation, drive one or more signals associated with the memory write operation to one or more of the second unidirectional interconnects; **(*e.g., para. [0068]*)**

the first unidirectional interconnects are configured to conduct signals from one or more DRAM dies of the plurality of stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

the second unidirectional interconnects are configured to conduct signals from the control die to one or more DRAM dies of the plurality of stacked DRAM dies and not configured to conduct any


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signal from any of the plurality of stacked DRAM dies to the control die;

the control die is configurable to receive signals from one or more DRAM dies of the plurality of stacked DRAM dies via the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

the control die is configurable to drive signals to one or more DRAM dies of the plurality of stacked DRAM dies via the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects; ***(e.g., para. [0068])***

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;

a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and

each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

The other independent claims recite the above annotated limitations in varied specificity. Thus, the examples of support for the above annotated limitations also apply to the similar limitations in the other independent claims.

Further, support for the following claim limitations in claim 24 can be found, for example, in para. [0051]:


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wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies.

Therefore, applicant respectfully submits that the claims presented herein comply with the written description requirement under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph.

## CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: December 11, 2024

/Jamie J. Zheng/ 51,167

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| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>17/694,649 | Filing Date<br>03/14/2022 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY:** ☑ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED - PART I

| FOR | (Column 1)<br>NUMBER FILED | (Column 2)<br>NUMBER EXTRA | | RATE ($) | FEE ($) |
|---|---|---|---|---|---|
| ☐ BASIC FEE<br>(37 CFR 1.16(a), (b), or (c)) | N/A | N/A | | N/A | |
| ☐ SEARCH FEE<br>(37 CFR 1.16(k), (i), or (m)) | N/A | N/A | | N/A | |
| ☐ EXAMINATION FEE<br>(37 CFR 1.16(o), (p), or (q)) | N/A | N/A | | N/A | |
| TOTAL CLAIMS<br>(37 CFR 1.16(i)) | minus 20 = | * | | x $100 = | |
| INDEPENDENT CLAIMS<br>(37 CFR 1.16(h)) | minus 3 = | * | | x $480 = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | 01/17/2025 | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * 27 | Minus | ** 28 | = 0 | | x $100 = | 0 |
| | Independent<br>(37 CFR 1.16(h)) | * 5 | Minus | *** 6 | = 0 | | x $480 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | 0 |

| | | (Column 1) | | (Column 2) | (Column 3) | | | |
|---|---|---|---|---|---|---|---|---|
| AMENDMENT | | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
| | Total<br>(37 CFR 1.16(i)) | * | Minus | ** | = | | x $0 = | |
| | Independent<br>(37 CFR 1.16(h)) | * | Minus | *** | = | | x $0 = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | |

| | |
|---|---|
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. | SLIE |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". | /KAREN L VESTAL/ |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". | |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. | |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronically filed January 17, 2025

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**SUPPLEMENTAL AMENDMENT**

**Mail Stop: Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Amendment is submitted to correct clerical/typographical errors and/or to address potential formality, clarity and/or antecedent basis issues in the Amendment submitted on December 11, 2024, in response to the non-final office action dated June 11, 2024.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL070-14US03).


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## Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked ~~array~~ DRAM dies through the one or more TSVs;

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits corresponding, respectively, to the die interconnects, wherein each die interconnect is coupled to a respective one of the conduits, the conduits including CA conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

wherein a first data interconnect of the first data interconnects is in electrically communication with data ports on the first plurality of DRAM dies and not in electrical



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communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is ~~electrically connected to~~ in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not ~~electrically connected to~~ in electrical communication with any data port on the at least one DRAM die;

wherein a second data interconnect of the second data interconnects is in electrically communication with data ports on [[a]]the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the data conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects;


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wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports, the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals, the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies, the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects, the data interconnects including first data interconnects,

receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;

in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first


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DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;

wherein each of the first data interconnects is in ~~electrically~~ electrical communication with data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies, each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is ~~electrically connected to~~ in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not ~~electrically connected to~~ in electrical communication with any data port on the at least one DRAM die;

wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked ~~array~~ DRAM dies and the second unidirectional interconnects are not configured to conduct any signals from any of the stacked ~~array~~ DRAM dies;

the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and

the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.

3. (Previously Presented) The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.


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4. (Previously Presented) The DRAM package of claim 3, wherein the stacked DRAM dies include 16 stacked DRAM dies.

5. (Previously Presented) The DRAM package of claim 1, wherein:

the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and

the second driver size is different from the first driver size.

6. (Previously Presented) The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.

7. (Currently Amended) The DRAM package of claim 1, wherein:

the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals.

8. (Previously Presented) The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.

9. (Previously Presented) The method of claim 2, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

10. (Currently Amended) The method of claim 2, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel ~~includes a first number of transistors coupled to a respective first data interconnect, and wherein each of the second drivers has a second~~


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~~number of transistors coupled to a respective second data interconnect, the second number being different from the first number~~.

11. (Previously Presented) The method of claim 2, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:

enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;

enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and

maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;

wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.

12. (Previously Presented) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports;

an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including C/A terminals and data terminals;

die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and

a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;

wherein:

the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;


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each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding bi-directional data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;

each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding bi-directional data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies, each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to at least the first subset of the plurality of stacked DRAM dies via at least the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to at least the second subset of the plurality of stacked DRAM dies via at least the second C/A interconnects;

the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

the control die is further configurable to, in response to the first or second set of C/A signals being for a memory read operation, receive one or more signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the first or second set of C/A signals being for a memory write operation, drive one or more signals associated with the memory write operation to one or more of the second unidirectional interconnects;


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the first unidirectional interconnects are configured to conduct signals from one or more DRAM dies of the plurality of stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

the second unidirectional interconnects are configured to conduct signals from the control die to one or more DRAM dies of the plurality of stacked DRAM dies and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;

the control die is configurable to receive signals from one or more DRAM dies of the plurality of stacked DRAM dies via the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

the control die is configurable to drive signals to one or more DRAM dies of the plurality of stacked DRAM dies via the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

each respective data interconnect of the first data interconnects includes a respective set of TSVs, the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;

a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and

each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

13. (Cancelled)

14. (Previously Presented) The DRAM package of claim 12, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.

15. (Previously Presented) The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.


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16. (Currently Amended) The DRAM package of claim 12, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.

17. (Previously Presented) The DRAM package of claim 12, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;

the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;

each of the first data conduits are placed in a non-driving state after driving the first data signals;

each of the second data conduits are placed in a non-driving state after driving the second data signals; and

data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.

18. (Cancelled)

19. (Previously Presented) The DRAM package of claim 12, wherein the control die is configured to control timing of the first set of C/A signal, the second set of C/A signals, the first data signals, and/or the second data signals between the interface and the plurality of stacked DRAM dies to prevent data collisions

20. (Previously Presented) The DRAM package of claim 12, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64


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signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel.

21. (Previously Presented) The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.

22. (Cancelled)

23. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a


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corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and to drive signals to the one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to any of the one or more DRAM dies via any of the first unidirectional interconnects or to receive any signal from any of the one or more DRAM dies via any of the second unidirectional interconnects;

wherein, in response to the first set of C/A signals, the control die is configured to receive first signals associated with the memory read operation from one of the one or more DRAM dies via the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive second signals associated with the memory write operation to the one or more DRAM dies via the second unidirectional interconnects;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM- dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

24. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:


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stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;


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wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and to drive signals to the one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to any of the one or more DRAM dies via any of the first unidirectional interconnects or to receive any signal from any of the one or more DRAM dies via any of the second unidirectional interconnects;

wherein, in response to the first set of C/A signals, the control die is configured to receive first signals associated with the memory read operation from one of the one or more DRAM dies via the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive second signals associated with the memory write operation to the one or more DRAM dies via the second unidirectional interconnects;

wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

25. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of


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the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;

an interface via which the DRAM package receives C/A signals and receives or outputs data signals;

a control die coupled between the interface and the stacked DRAM dies, the control die including signal conduits and logic configured to control at least some of the signal conduits; and

die interconnects, each die interconnect of the die interconnects coupled [[to]] between one corresponding conduit in the control die and one corresponding signal port in each of one or more of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;

wherein:

the conduits include first conduits, second conduits, third conduits and fourth conduits;

the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;

each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;

each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;

each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;

the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third


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set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;

in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second interconnects and to drive the first signals to the interface; and a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third interconnect and drive the one or more second signals to the interface;

in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second interconnects; and a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth interconnect;

in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second interconnects and to drive the fifth signals to the interface; and a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third interconnect and drive the one or more sixth signals to the interface;

in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the ~~first~~ second subset of the first interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second interconnects; and a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth interconnect;


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each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;

the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;

the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;

the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

26. (Currently Amended) The DRAM package of claim [[25]]27, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;

the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and

the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;

a [[data]] conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.

27. (Currently Amended) The DRAM package of claim 25, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second conduits is configured to be in electrical communication with a corresponding data port of each of a first subset of DRAM dies and not in electrical communication with any data port of any of the second subset of DRAM dies, wherein each of


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the second subset of the second conduits is configured to be in electrical communication with a corresponding data port of each of the second subset of DRAM dies and not in electrical communication with any data port of any of the first subset of DRAM dies, and wherein:

the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;

the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;

the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals; and

the fourth set of C/A signals include one or more signals selecting a DRAM die in the ~~first~~ second subset of DRAM dies to ~~output~~ receive the seventh signals and the one or more eighth signals.

28. (Currently Amended) The DRAM package of claim [[25]]27, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

29. (Previously Presented) The DRAM package of claim 28, wherein the stacked DRAM dies include 16 stacked DRAM dies.

30. (Previously Presented) The DRAM package of claim 23, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

31. (Previously Presented) The DRAM package of claim 23, wherein:

the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.


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*REMARKS*

This supplemental amendment supplements the amendment submitted on December 11, 2024, in response to the Non-Final Office Action dated June 11, 2024 (the "Office Action").

In this supplemental amendment, claims 1-2, 7, 10, 16, and 23-27 are amended to correct clerical/typographical errors and/or to address potential formality, clarity and/or antecedent basis issues in the Amendment submitted on December 11, 2024. No new matter is added.

Further, in the Amendment submitted on December 11, 2024, the status identifier for claim 24 was incorrectly stated as "Currently Amended." The correct status of claim 24 should be "New" in the Amendment submitted on December 11, 2024. Applicant apologizes for any confusion this error may have caused.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: January 17, 2025

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

**Customer No. 79141**



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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **01/17/2025 10:09:41 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 68817362 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 3**

| DOCUMENT | | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|---|
| NL070-14US03_Supplemental_Amendment.pdf | | 19 | - | 195 KB |
| NL070-14US03_Supplemental_Amendment-SA...pdf | (1-1) | 1 | Supplemental Response or Supplemental Amendment | 103 KB |
| NL070-14US03_Supplemental_Amendment-CLM.pdf | (2-18) | 17 | Claims | 161 KB |
| NL070-14US03_Supplemental_Amendment-REM.pdf | (19-19) | 1 | Applicant Arguments/Remarks Made in an Amendment | 98 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| NL070-14US03_Supplemental_Amendment.pdf | FBB7014929CD3A96BDA2B809A73692D0DE5F5103696A55EDB1E35628DA64061DB4E446F26629D6586EFAB0CDBC583094A671171D2FE784C234D144676ED5D7D4 |
| NL070-14US03_Supplemental_Amendment-SA...pdf | 69D9EA1566734794964354059 2FA88BED054A247794DBBAEDB48FE4A99F1A863D9C333E7CE7DDF31A7EB7C70E22223452C1862EF955D7F7FDE782D9E4E4555EE |
| NL070-14US03_Supplemental_Amendment-CLM.pdf | F9442633E469B5CA541F2CABC336FC39A8019A1E2FA480D769C125EA25A935109C02EC260D79D88FF371820D475C9B9F70884759E0A7B8B11CB4B6E1398E1253 |
| NL070-14US03_Supplemental_Amendment-REM.pdf | 69D219BB487C60A58C02E13BA6DE6E979ABA2DCA1380A73023B488D7283FAA0987C7896A772E3A66AB255614CCB19935C7736381DA9E254CE1954634FD4F914A |

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**National Stage of an International Application under 35 U.S.C. 371**

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**New International Application Filed with the USPTO as a Receiving Office**

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

79141 7590 02/20/2025

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER |
|---|
| HOANG, HUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 02/20/2025 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com



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| *Applicant-Initiated Interview Summary* | **Application No.** 17/694,649 | **Applicant(s)** Lee, Hyun | | |
|---|---|---|---|---|
| | **Examiner** HUAN HOANG | **Art Unit** 2827 | **AIA (First Inventor to File) Status** No | **Page** 1 of 1 |

| **All Participants** (applicant, applicants representative, PTO personnel) | **Title** | **Type** |
|---|---|---|
| HUAN HOANG | Primary Examiner | Telephonic |
| JAMIE ZHENG | Attorney of Record | |
| TOBIN HOBBS | Appl's representative | |
| RICHARD KIM | Appl's representatve | |

**Date of Interview:** 12 February 2025

**Issues Discussed:**

**35 U.S.C. 112**

Some 112 issues in claim 1 were discussed. Applicant clarified support for the negative limitation in claim 1 (the last three lines) and will consider to replace "at least first C/A interconnects" in claim 1, line 13 with "first C/A interconnects and second C/A interconnects" to overcome the 112(b) issue. The Examiner will decide patentability of the claims upon receiving a formal response.

| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |
|---|---|

**Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04**
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

**Applicant recordation instructions:** The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

**Examiner recordation instructions:** Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.



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| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **02/26/2025 02:54:27 AM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 69337470 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 2**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| NL070-14US03_Interview_Summary.pdf | 1 | Applicant summary of interview with examiner | 102 KB |
| Certificate_Transmission_sb0092.pdf | 2 | Transmittal Letter | 771 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| NL070-14US03_Interview_Summary.pdf | 6B2C365D5B722F3C9A6C03FF8F0435F55D3413292E27BD9BD5255D3764D6580F0EB30758B1F47A356279F6F3646E5562652BAADBAA2FC1F001FA6336BFA31EF3 |

Certificate_Transmission_sb0092.pdf

A67D6FC5E4FD1BD4F8AE48A74EDBE28728CBCA7F0FDC6453B0D7DAB454DC823D8A693506A27505DFF837F269E150B5E5E45CDEC80A98ECD03C45EB2152B06BB6

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**New International Application Filed with the USPTO as a Receiving Office**

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Electronically filed February 25, 2025

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**EXAMINER INTERVIEW SUMMARY**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant's representatives thank Examiner Hoang for the opportunity to discuss the above-referenced patent application during an examiner interview with Jamie Zheng and Richard Kim on February 12, 2025. During the interview, Examiner Hoang raised several 112 issues in claim 1. Jamie Zheng provided explanation on how the negative limitation in the last paragraph of claim 1 is supported in the specification and agreed to make changes in claim 1 to address the 112(b) issues, as suggested by Examiner Hoang. Mr. Kim suggested that Jamie Zheng would email a proposed claim amendment to Examiner Hoang to address the issues raised in the interview and any other potential 112 issues for entry as Examiner's amendment. Examiner Hoang tentatively agreed to the suggestion.

Respectfully submitted,

Date: February 25, 2025

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
**Customer No. 79141**


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PTO/SB/92 (05-22)
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| /Jamie J. Zheng/ | February 25, 2025 |
|---|---|
| Signature | Date |
| Jamie J. Zheng | 51,167 |
| Typed or printed name | Telephone number |

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| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | Examiner | Art Unit |
| | HUAN HOANG | 2827 |

| CPC - Searched* | | |
|---|---|---|
| **Symbol** | **Date** | **Examiner** |
| G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12 | 09/28/2022 | HH |
| Above Updated | 07/07/2023 | HH |
| Above Updated | 09/18/2023 | HH |
| Above Updated | 01/13/2024 | HH |
| Above Updated | 06/06/2024 | HH |
| AboveUpdated | 03/16/2025 | HH |

| CPC Combination Sets - Searched* | | |
|---|---|---|
| **Symbol** | **Date** | **Examiner** |
| | | |

| US Classification - Searched* | | | |
|---|---|---|---|
| **Class** | **Subclass** | **Date** | **Examiner** |
| 365 | 63 | 09/28/2022 | HH |
| Above | Updated | 07/07/2023 | HH |
| Above | Updated | 09/18/2023 | HH |
| Above | Updated | 01/13/2024 | HH |
| Above | Updated | 06/06/2024 | HH |
| Above | Updated | 03/16/2025 | HH |

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

| | |
|---|---|
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |


Samsung Electronics Co., Ltd.
Ex. 1002, p. 806

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | **Examiner** | **Art Unit** |
| | HUAN HOANG | 2827 |

| Search Notes | | |
|---|---|---|
| **Search Notes** | **Date** | **Examiner** |
| PE2E Search | 09/28/2022 | HH |
| Assignee and Inventor search | 09/28/2022 | HH |
| PE2E Search | 07/07/2023 | HH |
| IPR2022-01427 Reviewed Inter Partes Review of U.S. Patent No. 9,318,160 on 07/05/23 | 07/05/2023 | HH |
| IPR2022-01428 Reviewed Inter Partes Review of U.S. Patent No. 8,787,060 on 07/06/23 | 07/06/2023 | HH |
| PE2E Search | 09/18/2023 | HH |
| PE2ESearch | 01/13/2024 | HH |
| PE2E Search | 06/06/2024 | HH |
| PE2E Search | 03/16/2025 | HH |

| Interference Search | | | |
|---|---|---|---|
| **US Class/CPC Symbol** | **US Subclass/CPC Group** | **Date** | **Examiner** |
| | PE2E Search (US-PGPUB) | 09/18/2023 | HH |
| | PE2E Search (US-PGPUB) | 03/16/2025 | HH |

| | |
|---|---|
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | |


Samsung Electronics Co., Ltd.
Ex. 1002, p. 807

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | **Examiner** | **Art Unit** |
| | HUAN HOANG | 2827 |

| CPC | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | | | | | **Type** | **Version** |
| G11C | / | 5 | / | 066 | F | 2013-01-01 |
| G11C | / | 5 | / | 06 | I | 2013-01-01 |
| G11C | / | 7 | / | 1057 | I | 2013-01-01 |
| G11C | / | 7 | / | 1084 | I | 2013-01-01 |
| G11C | / | 7 | / | 12 | I | 2013-01-01 |

| CPC Combination Sets | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | | | | | **Type** | **Set** | **Ranking** | **Version** |
| | / | | / | | | | | |

| NONE | | **Total Claims Allowed:** | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 28 | |
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | 16 March 2025 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 | 2 |

U.S. Patent and Trademark Office

Part of Paper No.: 20250314



Samsung Electronics Co., Ltd.
Ex. 1002, p. 808

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | **Examiner** | **Art Unit** |
| | HUAN HOANG | 2827 |

| INTERNATIONAL CLASSIFICATION | | | | | |
|---|---|---|---|---|---|
| **CLAIMED** | | | | | |
| G11C | / | 5 | / | 06 | |

| NON-CLAIMED | | | | | |
|---|---|---|---|---|---|
| | / | | / | | |

| US ORIGINAL CLASSIFICATION | |
|---|---|
| **CLASS** | **SUBCLASS** |
| | |

| CROSS REFERENCES(S) | | | | | | |
|---|---|---|---|---|---|---|
| **CLASS** | **SUBCLASS (ONE SUBCLASS PER BLOCK)** | | | | | |
| | | | | | | |

| NONE | | **Total Claims Allowed:** | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 28 | |
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | 16 March 2025 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 | 2 |

U.S. Patent and Trademark Office

Part of Paper No.: 20250314



Samsung Electronics Co., Ltd.
Ex. 1002, p. 809

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 17/694,649 | Lee, Hyun |
| | **Examiner** | **Art Unit** |
| | HUAN HOANG | 2827 |

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

**CLAIMS**

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 11 | 10 | 8 | 21 | 22 | 31 | | | | | | | | |
| 9 | 2 | 12 | 11 | 20 | 23 | | | | | | | | | | |
| 2 | 3 | 13 | 12 | 23 | 24 | | | | | | | | | | |
| 3 | 4 | 14 | 14 | 24 | 25 | | | | | | | | | | |
| 4 | 5 | 15 | 15 | 26 | 26 | | | | | | | | | | |
| 5 | 6 | 16 | 16 | 25 | 27 | | | | | | | | | | |
| 6 | 7 | 17 | 17 | 27 | 28 | | | | | | | | | | |
| 7 | 8 | 18 | 19 | 28 | 29 | | | | | | | | | | |
| 10 | 9 | 19 | 20 | 21 | 30 | | | | | | | | | | |

| | | | |
|---|---|---|---|
| NONE | | **Total Claims Allowed:** | |
| (Assistant Examiner) | (Date) | 28 | |
| /HUAN HOANG/<br>Primary Examiner, Art Unit 2827 | 16 March 2025 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 1 | 2 |



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Ex. 1002, p. 810

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENTS** Remove

| Examiner Initial* | Cite No | Patent Number | Kind Code[1] | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | 1 | 6414904 | B2 | 2002-01-03 | So et al. | |
| | 2 | 7242635 | B2 | 2005-11-24 | Okuda | |
| | 3 | 8421237 | B2 | 2013-01-10 | Chia et al. | |
| | 4 | 8432027 | B2 | 2013-01-10 | Foster et al. | |
| | 5 | 8488399 | B2 | 2011-11-24 | Yu et al. | |
| | 6 | 8817549 | B2 | 2012-11-29 | Shin et al. | |
| | 7 | 8866303 | B2 | 2011-12-22 | Kim | |
| | 8 | 9484326 | B2 | 2016-11-01 | Keeth et al. | |

If you wish to add additional U.S. Patent citation information please click the Add button. Add



ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

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Ex. 1002, p. 811

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENT APPLICATION PUBLICATIONS** Remove

| Examiner Initial* | Cite No | Publication Number | Kind Code[1] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | 1 | | | | | |

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**FOREIGN PATENT DOCUMENTS** Remove

| Examiner Initial* | Cite No | Foreign Document Number[3] | Country Code[2] i | Kind Code[4] | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear | T[5] |
|---|---|---|---|---|---|---|---|---|
| | 1 | | | | | | | ☐ |

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**NON-PATENT LITERATURE DOCUMENTS** Remove

| Examiner Initials* | Cite No | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published. | T[5] |
|---|---|---|---|
| | 1 | USDC Easter District of Texas, Marshall Division, Netlist, Inc. v. Micron Technology, Inc. et al., Civil Action No. 2:22-CV-00203-JRG-RSP, Claim Construction Order, Filed 10/22/2023, 45 pages | ☐ |

If you wish to add additional non-patent literature document citation information please click the Add button Add

**EXAMINER SIGNATURE**

| Examiner Signature | /HUAN HOANG/ | Date Considered | 03/14/2025 |
|---|---|---|---|

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.



ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

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Ex. 1002, p. 812

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

## CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

**OR**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

## SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

| | | | |
|---|---|---|---|
| Signature | /Jamie J. Zheng/ | Date (YYYY-MM-DD) | 2024-12-07 |
| Name/Print | Jamie J. Zheng | Registration Number | 51167 |

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**



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# Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

# BIB DATA SHEET

**CONFIRMATION NO. 3889**

| SERIAL NUMBER | FILING or 371(c) DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022<br>RULE | 365 | 2827 | NL070-14US03 |

**APPLICANTS**
Netlist, Inc., Irvine, CA;

**INVENTORS**
Hyun Lee, Ladera Ranch, CA;

**** CONTINUING DATA ***************************
This application is a CON of 17/157,903 01/25/2021 ABN
which is a CON of 16/412,308 05/14/2019 PAT 10902886
which is a CON of 15/602,099 05/22/2017 PAT 10290328
which is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/17/2022

| Foreign Priority claimed | 35 USC 119(a-d) conditions met | Verified and Acknowledged | Met after Allowance | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|---|
| ❑ Yes ☑ No | ❑ Yes ☑ No | /HUAN HOANG/ Examiner's Signature | ❑ HH Initials | CA | 8 | 2 | 2 |

**ADDRESS**
USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306
UNITED STATES

**TITLE**
MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

| FILING FEE RECEIVED | | |
|---|---|---|
| 0.00 | FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following: | ❑ All Fees<br>❑ 1.16 Fees (Filing)<br>❑ 1.17 Fees (Processing Ext. of time)<br>❑ 1.18 Fees (Issue)<br>❑ Other _____<br>❑ Credit |

BIB (Rev. 05/07).

Electronically filed September 28, 2024

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Hyun LEE | Confirmation No.: | 3889 |
| Serial No.: | 17/694,649 | Group Art Unit: | 2827 |
| Filed: | March 14, 2022 | Examiner: | Huan HOANG |
| For: | *MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD* | Attorney Docket No.: | NL070-14US03 |

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☒ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☒ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);



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Ex. 1002, p. 816

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

*(Check either Item 3a, 3b, 3c or 3d)*

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03) if it is not submitted herewith.

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

*(Items 3b or 3c to be checked if any reference known for more than 3 months)*

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

*(Check Item 4a, and 4b, 4c or 4d)*

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL070-14US03).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. ).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

*(Check either Item 5a, 5b, 5c or 5d)*



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Ex. 1002, p. 817

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

*(Check appropriate Items 7a, 7b and/or 7c)*

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. 17/157,903, filed on January 25, 2021, 16/412,308, filed on May 14, 2019, 15/602,099, filed May 22, 2017, 15/095,288, filed Apr. 11, 2016, 14/337,168, filed Jul. 21, 2014, and 13/288,850, filed Nov. 3, 2011, of which this application claims priority under 35 U.S.C. §120, and in prior application Serial No. 15/470,856, filed on March 27, 2017, to which this application is related, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in the above-listed prior applications are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly,



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additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

*(Check Item 9a, 9b, or 9c)*

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL070-14US03).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 28, 2024

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

/HUAN HOANG/ 03/14/2025



Samsung Electronics Co., Ltd.
Ex. 1002, p. 819

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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>Substitute for Form 1449-PTO | | | | Electronically filed September 28, 2024 | |
|---|---|---|---|---|---|
| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 1 | of | 3 | Attorney Docket Number | NL070-14US03 |

**U.S. PATENT DOCUMENTS**

| Examiner Initials | Cite No. | Document Number<br>Number - Kind Code | Publication Date<br>YYYY-MM-DD | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
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| Examiner Signature | | Date Considered | |
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT<br>Substitute for Form 1449-PTO | | | | Electronically filed September 28, 2024 | |
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| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 2 | of | 3 | Attorney Docket Number | NL070-14US03 |

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| Examiner Initials | Cite No. | Foreign Patent Document<br>Country Code – Number - Kind Code *(if known)* | Publication Date YYYY-MM-DD | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T |
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| Examiner Initials | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published |
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| Examiner Signature | | Date Considered | |
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

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| | | | | Application Number | 17/694,649 |
| | | | | Filing Date | March 14, 2022 |
| | | | | First Named Inventor | Hyun LEE |
| | | | | Art Unit | 2827 |
| | | | | Examiner Name | Huan HOANG |
| Sheet | 3 | of | 3 | Attorney Docket Number | NL070-14US03 |

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| | | |

| Examiner Signature | /HUAN HOANG/ | Date Considered | 03/14/2025 |
|---|---|---|---|

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

## PE2E SEARCH - Search History (Prior Art)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | British Equivalents | Time Stamp |
|---|---|---|---|---|---|---|---|
| L1 | 4 | "20080025137".pn. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 11:07 AM |
| L2 | 68734 | (G11C5/066 OR G11C5/06 OR G11C7/1057 OR G11C7/1084 OR G11C7/12).cpc. 365/63,063.ccls. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:12 PM |
| L3 | 5718 | 2 AND stack$3 WITH (die chip ic integrated ADJ circuit) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:13 PM |
| L4 | 2381 | 3 AND command WITH address$3 WITH (data bit information) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:14 PM |
| L5 | 121 | 4 AND control$4 WITH (interconnect$3 tsv through ADJ silicon ADJ via) WITH command WITH address$3 WITH (data bit information) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:16 PM |
| L6 | 121 | 5 AND data WITH (interconnect$3 tsv through ADJ silicon ADJ via) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:17 PM |
| L8 | 58 | 6 AND (set group subset) WITH (tsv | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, | OR | ON | ON | 2024/06/06 04:18 PM |


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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | through ADJ silicon ADJ via) | AT, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L9 | 289591 | (memory storage) AND stack$3 WITH (die chip ic integrated ADJ circuit) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:21 PM |
| L10 | 27560 | 9 AND command WITH address$3 WITH (data bit information) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:21 PM |
| L11 | 491 | 10 AND control$4 WITH (interconnect$3 tsv through ADJ silicon ADJ via) WITH command WITH address$3 WITH (data bit information) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:22 PM |
| L12 | 482 | 11 AND data WITH (interconnect$3 tsv through ADJ silicon ADJ via) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:22 PM |
| L13 | 174 | 12 AND (set group subset) WITH (tsv through ADJ silicon ADJ via) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:22 PM |
| L14 | 116 | 13 NOT 8 | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, CA, CH, CN, DD, DE, EA, EP, ES, FR, GB, JP, KR, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2024/06/06 04:23 PM |

There are no Interference searches to show.

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# NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/20/2025

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER | |
|---|---|
| HOANG, HUAN | |
| ART UNIT | PAPER NUMBER |
| 2827 | |

DATE MAILED: 03/20/2025

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1290 | $0.00 | $0.00 | $1290 | 06/20/2025 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.**





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## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/20/2025

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3524 Waverley St.
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

| |
|---|
| (Typed or printed name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1290 | $0.00 | $0.00 | $1290 | 06/20/2025 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| HOANG, HUAN | 2827 | 365-063000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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Ex. 1002, p. 827

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|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

79141 7590 03/20/2025

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER | |
|---|---|
| HOANG, HUAN | |
| ART UNIT | PAPER NUMBER |
| 2827 | |

DATE MAILED: 03/20/2025

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.





Samsung Electronics Co., Ltd.
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## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
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10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

| Notice of Allowability | Application No. 17/694,649 | Applicant(s) Lee, Hyun | |
|---|---|---|---|
| | Examiner HUAN HOANG | Art Unit 2827 | AIA (FITF) Status No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 02/26/25 and 03/06/25.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are See Continuation Sheet . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   **Certified copies:**

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827



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Continuation of 3. The allowed claim(s) is/are: 1-12,14-17,19-21 and 23-31

## EXAMINER'S AMENDMENT

### *Notice of Pre-AIA or AIA Status*

1. The present application is being examined under the pre-AIA first to invent provisions.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Jamie J. Zheng on 03/06/25.

The application has been amended as follows:

In the claims:

1. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first

data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits ~~corresponding, respectively, to the die interconnects, wherein each die interconnect is coupled to a respective one or more of the conduits~~, the conduits including [[CA]]C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

wherein a first data interconnect of the first data interconnects is in ~~electrically~~ electrical communication with corresponding data ports on the first plurality of DRAM

dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

wherein a second data interconnect of the second data interconnects is in ~~electrically~~ electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first and second [[data]] conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not

configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects;

~~wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies~~.

2. (Currently Amended) A method, comprising:

at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports, the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals, the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies, the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including

first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects,

receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;

in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;

wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies, each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of

the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies;

wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and

wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.

3. (Previously Presented) The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

4. (Previously Presented) The DRAM package of claim 3, wherein the stacked DRAM dies include 16 stacked DRAM dies.

5. (Previously Presented) The DRAM package of claim 1, wherein:

the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and

the second driver size is different from the first driver size.

6. (Previously Presented) The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.

7. (Currently Amended) The DRAM package of claim 1, wherein:

the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

8. (Previously Presented) The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.

9. (Previously Presented) The method of claim 2, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

10. (Previously Presented) The method of claim 2, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.

11. (Previously Presented) The method of claim 2, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:

enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;

enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and

maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;

wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.

12. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;

an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals;

die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and

a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;

wherein:

the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;

each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding ~~bi-directional~~ data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;

each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding ~~bi-directional~~ data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies, each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to ~~at least~~ the first subset of the plurality of stacked DRAM dies via ~~at least~~ the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to ~~at least~~ the second subset of the plurality of stacked DRAM dies via ~~at least~~ the second C/A interconnects;

a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies;

wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;

the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to

select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

the control die is further configurable to, in response to the first ~~or second~~ set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the ~~first or~~ second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;

the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die ~~one or more DRAM dies of the plurality of stacked DRAM dies~~ to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die ~~one or more DRAM dies of the plurality of stacked DRAM dies~~ and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;

the control die is configurable to receive the one or more first signals from the first DRAM die ~~one or more DRAM dies of the plurality of stacked DRAM dies~~ via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

the control die is configurable to drive the one or more second signals to the second DRAM die ~~one or more DRAM dies of the plurality of stacked DRAM dies~~ via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;

a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and

each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

13. (Cancelled)

14. (Previously Presented) The DRAM package of claim 12, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.

15. (Previously Presented) The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.

16. (Previously Presented) The DRAM package of claim 12, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.

17. (Previously Presented) The DRAM package of claim 12, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured

to control states of the data conduits in response to C/A signals received via the interface, whereby:

the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;

the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;

each of the first data conduits are placed in a non-driving state after driving the first data signals;

each of the second data conduits are placed in a non-driving state after driving the second data signals; and

data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.

18. (Cancelled)

19. (Currently Amended) The DRAM package of claim 12, wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits, wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal. ~~is configured to control timing of the first set of C/A signal, the second set of C/A signals, the first data signals, and/or the second data signals between the interface and the plurality of stacked DRAM dies to prevent data collisions~~

20. (Previously Presented) The DRAM package of claim 12, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel.

21. (Previously Presented) The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.

22. (Cancelled)

23. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from ~~one or more DRAM dies of the stacked DRAM dies via~~ the first unidirectional interconnects and to drive signals to ~~the one or more DRAM dies of the stacked DRAM dies via~~ the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to ~~any of the one or more DRAM dies via~~ any of the first unidirectional interconnects or to receive any signal from ~~any of the one or more DRAM dies via~~ any of the second unidirectional interconnects; and

wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to

drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

24. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits coupled to respective ones of the die interconnects;

wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies

of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

wherein the control die is configured to receive signals from ~~one or more DRAM dies of the stacked DRAM dies via~~ the first unidirectional interconnects and to drive signals to ~~the one or more DRAM dies of the stacked DRAM dies via~~ the second unidirectional interconnects;

wherein the control die is not configured to drive any signal to ~~any of the one or more DRAM dies via~~ any of the first unidirectional interconnects or to receive any signal from ~~any of the one or more DRAM dies via~~ any of the second unidirectional interconnects;

wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;

wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage

interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

25. (Currently Amended) A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;

an interface via which the DRAM package receives C/A signals and receives or outputs data signals;

a control die coupled between the interface and the stacked DRAM dies, the control die including signal conduits and logic configured to control at least some of the signal conduits; and

die interconnects, each die interconnect of the die interconnects coupled between at least one corresponding conduit in the control die and one corresponding signal port in each of ~~one or more~~ a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;

wherein:

the signal conduits include first conduits, second conduits, third conduits and fourth conduits;

the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;

each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;

each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;

each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;

the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;

in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;

in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the

second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;

in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;

in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect;

each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;

the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;

the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;

the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

26. (Currently Amended) The DRAM package of claim 27, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;

the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and

the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;

a [[data]] conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.

27. (Currently Amended) The DRAM package of claim 25, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second ~~conduits~~ die interconnects is configured to be in electrical communication with a corresponding ~~data~~ signal port of each of a first subset of DRAM dies and not in electrical communication with any ~~data~~ signal port of any of the second subset of DRAM dies, wherein each of the second subset of the second ~~conduits~~ die interconnects is configured to be in electrical communication with a corresponding ~~data~~ signal port of each of the second subset of DRAM dies and not in electrical communication with any ~~data~~ signal port of any of the first subset of DRAM dies, and wherein:

the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;

the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;

the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals; [[and]]

the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals;

the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and

the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.

28. (Previously Presented) The DRAM package of claim 27, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

29. (Previously Presented) The DRAM package of claim 28, wherein the stacked DRAM dies include 16 stacked DRAM dies.

30. (Previously Presented) The DRAM package of claim 23, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

31. (Previously Presented) The DRAM package of claim 23, wherein:

the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and

the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.

## ***Reasons for Allowance***

1. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies; wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies; wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and

wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die; wherein a second data interconnect of the second data interconnects is in electrical_communication with corresponding_data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies; wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal; wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal; wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies; wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die; wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects; wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is

not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects." in combination with the other limitations thereof as is recited in the claim. Claims 3-8 and 21 depend on claim 1.

Regarding claim 1, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies; wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies; wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies; wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies; wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the

interface in parallel; and wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel." in combination with the other limitations thereof as is recited in the claim. Claims 9-11 depend on claim 2.

Regarding claim 12, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface; the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the first or second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects; the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies; the one or more of second unidirectional interconnects are configured to conduct the one or more second_signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die; the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not

configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects; the control die is configurable to drive the one or more second signals to the second DRAM die via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects; each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies; a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die." in combination with the other limitations thereof as is recited in the claim. Claims 14-17, 19 and 20 depend on claim 12

Regarding claim 23, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies, the second data interconnect configured to be

in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies; wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal; wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal; wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects; wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects; wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects; wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to

emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies." in combination with the other limitations thereof as is recited in the claim.

Regarding claim 24, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects; wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects; wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects; wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and wherein the control die does not include emulation logic that performs emulation

causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies." in combination with the other limitations thereof as is recited in the claim.

Regarding claim 25, the prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface; in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect; in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset

of the second die interconnects and to drive the fifth signals to the interface; and a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface; in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect; each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits; each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects; the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel; the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel; the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel." in

combination with the other limitations thereof as is recited in the claim. Claims 26-31 depend on claim 25.

Therefore, the application is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

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# ELECTRONIC PAYMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **04/15/2025 02:40:01 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 70015074 | AUTHORIZED BY | - |
| CUSTOMER # | 79141 | FILING DATE | 03/14/2022 |
| CORRESPONDENCE ADDRESS | - | FIRST NAMED INVENTOR | Hyun Lee |

## Payment Information

| PAYMENT METHOD | PAYMENT TRANSACTION ID | PAYMENT AUTHORIZED BY |
|---|---|---|
| **CARD / 2172** | **E20254EE40287181** | **Jamie Zheng** |

| FEE CODE | DESCRIPTION | ITEM PRICE($) | QUANTITY | ITEM TOTAL($) |
|---|---|---|---|---|
| 1501 | UTILITY ISSUE FEE | 1290.00 | 1 | 1290.00 |
| | | | **TOTAL AMOUNT:** | **$1,290.00** |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/20/2025

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

| |
|---|
| (Typed or printed name) |
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1290 | $0.00 | $0.00 | $1290 | 06/20/2025 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| HOANG, HUAN | 2827 | 365-063000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **USCH Law, PC**
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **Netlist, Inc.**

(B) RESIDENCE: (CITY and STATE OR COUNTRY): **Irvine, CA**

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. **60-3916**

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature **/Jamie J. Zheng/** Date **April 15, 2025**

Typed or printed name **Jamie J. Zheng** Registration No. **51167**



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United States Patent and Trademark Office
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www.uspto.gov

# NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/20/2025

USCH Law, PC
3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER | |
|---|---|
| HOANG, HUAN | |
| ART UNIT | PAPER NUMBER |
| 2827 | |

DATE MAILED: 03/20/2025

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

TITLE OF INVENTION: MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1290 | $0.00 | $0.00 | $1290 | 06/20/2025 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.**





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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **17/694,649** | **04/15/2025 02:40:01 PM Z ET** | **NL070-14US03** |

## Title of Invention

MEMORY PACKAGE HAVING STACKED ARRAY DIES AND REDUCED DRIVER LOAD

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 3889 | FILED BY | Jamie Zheng |
| PATENT CENTER # | 70015074 | FILING DATE | 03/14/2022 |
| CUSTOMER # | 79141 | FIRST NAMED INVENTOR | Hyun Lee |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | - |

## Documents

**TOTAL DOCUMENTS: 1**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| NL070-14US03_Issue_Fee.pdf | 2 | Issue Fee Payment (PTO-85B) | 289 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| NL070-14US03_Issue_Fee.pdf | 39A9C7110E4E67003CBB14DE52BFCC52FB0A156721BD3106 A1A40C187B9869A10E656C8A4608EE6B1A42A967D3E973E44 9E2069FBB7D681664DBA4C99A1997E8 |

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**( Not for submission under 37 CFR 1.99)**

| | |
|---|---|
| Application Number | 17694649 |
| Filing Date | 2022-03-14 |
| First Named Inventor | Hyun LEE |
| Art Unit | 2827 |
| Examiner Name | Huan HOANG |
| Attorney Docket Number | NL070-14US03 |

**U.S.PATENTS** Remove

| Examiner Initial* | Cite No | Patent Number | Kind Code[1] | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | 1 | 6414904 | B2 | 2002-01-03 | So et al. | |
| Change(s) applied to document, /J.H./ 4/21/2025 | 2 | 7242635 | B2 | 07/2007 ~~2005-11-24~~ | Okuda | |
| | 3 | 8421237 | B2 | 2013-01-10 | Chia et al. | |
| | 4 | 8432027 | B2 | 2013-01-10 | Foster et al. | |
| | 5 | 8488399 | B2 | 07/2013 ~~2011-11-24~~ | Yu et al. | |
| | 6 | 8817549 | B2 | 08/2014 ~~2012-11-29~~ | Shin et al. | |
| | 7 | 8866303 | B2 | 10/2014 ~~2011-12-22~~ | Kim | |
| | 8 | 9484326 | B2 | 2016-11-01 | Keeth et al. | |

If you wish to add additional U.S. Patent citation information please click the Add button. Add



ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

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| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 05/20/2025 | 12308087 | NL070-14US03 | 3889 |

79141 7590 05/07/2025

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# ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.



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INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

Hyun Lee, Ladera Ranch, CA;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

Netlist, Inc., Irvine, CA;

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 17/694,649 | 03/14/2022 | Hyun Lee | NL070-14US03 | 3889 |

79141 7590 05/20/2025

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3524 Waverley St.
Palo Alto, CA 94306

| EXAMINER |
|---|
| HOANG, HUAN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 05/20/2025 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@netlist.com
patents@uschlaw.com



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Ex. 1002, p. 873

| APPLICATION NO. | ISSUE DATE | PATENT NO. |
|---|---|---|
| 17/694,649 | 20-May-2025 | 12308087 |

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3524 Waverley St.
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# EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants



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