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Paper No. 38
Entered: July 18, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.
Patent Owner.

IPR2017-00667
Patent 7,532,537 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges.*

McSHANE, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc. ("Petitioner") filed a Corrected Petition requesting *inter partes* review of claims 1–17, 24–38, and 45–55 of U.S. Patent No. 7,532,537 B2 as amended by Reexamination Certificate No. 7,532,537 C1 (Ex. 1001, "the '537 patent"), pursuant to 35 U.S.C. §§ 311–319. Paper 6 ("Pet."). Netlist, Inc. ("Patent Owner") did not file a Preliminary Response to the Petition.

Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review as to claims 1–17, 24–38, and 45–55 of the '537 patent on July 21, 2017. Paper 10 ("Dec." or "Institution Decision"), 7–25. The following grounds were instituted:

Identifier	Basis	Claims	Prior Art
Ground A	§ 102[1]	1, 2, 4–10, 12–17, 24, 25, 27–32, 34–38, 45, 49–52, 54, and 55	Amidi[2]
Ground B	§ 103	3, 11, 26, and 33	Amidi
Ground C	§ 103	1–17, 24–38, and 45–55	Amidi and Klein[3]

Dec. 25; Pet. 2.

During the course of trial, Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp."), and Petitioner filed a Reply to the Patent Owner Response (Paper 19, "Pet. Reply"). Petitioner submitted the Declaration of Harold Stone, Ph.D. (Ex. 1003), and the Supplemental Declaration of Harold Stone, Ph.D. (Ex. 1031). Patent Owner submitted the Declaration of Carl Sechen, Ph.D. (Ex. 2001).

[1] Petitioner assert that Amidi is prior art to the '537 patent under § 102(e). Pet. 12.
[2] U.S. Patent No. 8,250,295 B2 (issued August 21, 2012) (Ex. 1006).
[3] U.S. Publication No. 2001/0008006 A1 (published July 12, 2001) (Ex. 1007).

Petitioner filed a Motion to Exclude Evidence (Paper 22, "Pet. Mot. Ex."), with Patent Owner filing an Opposition the Motion to Exclude (Paper 31, "Pet. Mot. Ex. Opp."), and Petitioner filing a Reply thereto (Paper 33, "Pet. Mot. Ex. Reply"). Patent Owner filed a Motion for Observations (Paper 24, "Mot. Ob.") and Petitioner filed a Response to Patent Owner's Motion for Observations (Paper 29, "Mot. Ob. Resp.). Patent Owner also filed a Submission on Propriety of Petitioner' Reply and Supplemental Stone Declaration due to alleged new arguments in Petitioner's Reply and related expert declaration (Paper 26, "PO Obj."), with Petitioner filing a Response (Paper 28, "PO Obj. Resp.").

We held a consolidated oral hearing on April 24, 2018, with the parties presenting arguments for this proceeding in combination with IPR2017-00668 ("the 668 IPR"), as well for another proceeding involving the same parties. A transcript (Paper 35, "Tr."), of the oral hearing has been entered into the record. *See* Tr. 3–45.

By Joint Motion to Limit the Petition (Paper 37), the parties move to remove two grounds from the proceeding: (1) Ground A that asserts the anticipation of certain claims by Amidi; and (2) Ground B that asserts the obviousness of certain claims by Amidi. The parties agree that Grounds A and B should be removed from this proceeding and do not need to be addressed in the final written decision. Paper 37, 2. The parties contend that limiting the proceeding would facilitate the Board's goal of resolving these proceedings in a just, speedy, and inexpensive manner pursuant to 37 C.F.R. § 42.1(b). *Id*.

We grant the Joint Motion to Limit the Petition and, accordingly, this Final Written Description addresses only the challenge brought under Ground C, that is, the obviousness challenge to claims 1–17, 24–38, and 45–55 over the combination of Amidi and Klein.

Samsung Electronics Co., Ltd.
Ex. 1032, p. 3

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6, and this Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–17, 24–38, and 45–55 of the ’537 patent are unpatentable. We deny Petitioner’s Motion to Exclude.

B. Related Proceedings

Petitioner and Patent Owner indicate related matters are *Netlist, Inc. v. Inphi Corp*., Case No. 09-cv-6900-FMO (C.D. Cal.); *Inter Partes* Reexamination No. 95/001,381 filed by Inphi Corporation on June 9, 2010, with associated Federal Circuit decision, *Inphi v. Netlist*, 805 F.3d 1350 (Fed. Circ. 2015); *inter partes* reexaminations of related U.S. Patent No. 7,619,912 (Control Nos. 95/001,339, 95/000,578, 95/000,579), U.S. Patent No. 7,864,627 (Control No. 95/001,758), and U.S. Patent No. 7,636,274 (Control No. 95/001,337); *inter partes* reviews of U.S. Patent No. 7,881,150 (Case Nos. IPR2014-00882, IPR2014-01011, and IPR2015-01020), U.S. Patent No. 8,081,536 (Case Nos. IPR2014-00883 and IPR2014-01021), U.S. Patent No. 7,532,537 (Case No. IPR2017-00668) (“the 668 IPR”), U.S. Patent No. 8,756,364 (Case No. IPR2017-00549). *See* Pet. 1–2; Paper 5, 1–3.

Another *inter partes* review was instituted in the 668 IPR, which challenges the same ’537 patent, but different claims than those at issue here. *See SK hynix Inc. v. Netlist, Inc*., Case IPR2017-00668, Papers 6 and 10. A final written decision in that proceeding issues concurrently with this decision.

Cases IPR2014-00882 (“882 IPR”), IPR2014-00883 (“883 IPR”), and IPR2014-01011 (“1011 IPR”) were directed to different patents, but the patents are related and have the same specification as the ’537 patent. Final written decisions were issued in these cases, the decisions were appealed to the Federal Circuit, and a decision issued in the appeal on July 25, 2017. *See Netlist, Inc. v. Diablo Techs.*,

Inc., 701 Fed. App'x 1001 (Fed. Cir. 2017) (Ex. 2003) ("the Federal Circuit decision"). In its decision, the Federal Circuit construed some claim terms and remanded the cases back to the Patent Trial and Appeal Board for further proceedings. *See Netlist*, 701 Fed. App'x at 1004–7. Subsequently, the Patent Trial and Appeal Board issued decisions from the remand in the 882 IPR, the 883 IPR, and the 1011 IPR, finding that under the Federal Circuit's claim construction, the respective claims challenged were unpatentable. *See Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00882, (PTAB Mar. 29, 2018) (Paper 36); *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, (PTAB Mar. 29, 2018) (Paper 36); *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-01011, (PTAB Mar. 29, 2018) (Paper 37).

C. The '537 Patent

The '537 patent is entitled "Memory Module With A Circuit Providing Load Isolation and Memory Domain Translation," and issued on May 12, 2009, from an application filed on January 19, 2006. Ex. 1001, [22], [45], [54]. The '537 patent claims priority to (1) U.S. Patent Application No. 11/173,175, filed on July 1, 2005 (now U.S. Patent No. 7,289,386); (2) U.S. Application No. 11/075,395, filed on March 7, 2005 (now U.S. Patent No. 7,286,436); (3) U.S. Provisional Application No. 60/645,087, filed on January 19, 2005; (4) U.S. Provisional Application No. 60/588,244, filed on July 15, 2004; (5) U.S. Provisional Application No. 60/550,668, filed on March 5, 2004; (6) U.S. Provisional Application No. 60/575,595, filed on May 28, 2004; and (7) U.S. Provisional Application No. 60/590,038, filed on July 21, 2004. *Id*. at [60], [63]. *Inter Partes* Reexamination No. 95/001,381 was conducted, resulting in claims 1, 7, 13, 16, 18, 21, 23, 24, 35, 39, 41 and 44 being deemed patentable as amended, claims 2–6, 8–12, 14, 15, 17, 19, 20, 22, 25–34, 36–38, 40, 42, and 43, which are dependent on amended claims,

determined to be patentable, and with new claims 45–60 added which were determined to be patentable. *See* Ex. 1001, *Inter Partes* Reexamination Certificate ("Reexam. Cert.") 1:16–22.[4]

The '537 patent is directed to a memory module system that includes memory devices and a circuit. Ex. 1001, Abstract, 2:62–63. The circuit can isolate one or more of the memory device loads from the computer system. *Id*. at Abstract, 2:67–3:1. The circuit has logic to translate between the system memory domain of the computer system and the physical memory domain of the memory module. *Id*. at Abstract, 3:2–4. The memory module has at least two memory devices arranged into ranks, and each memory device has a data signal line and data strobe line. *Id*. at 5:64–6:3, 6:27–47. Figure 4A of the '537 patent is reproduced below.

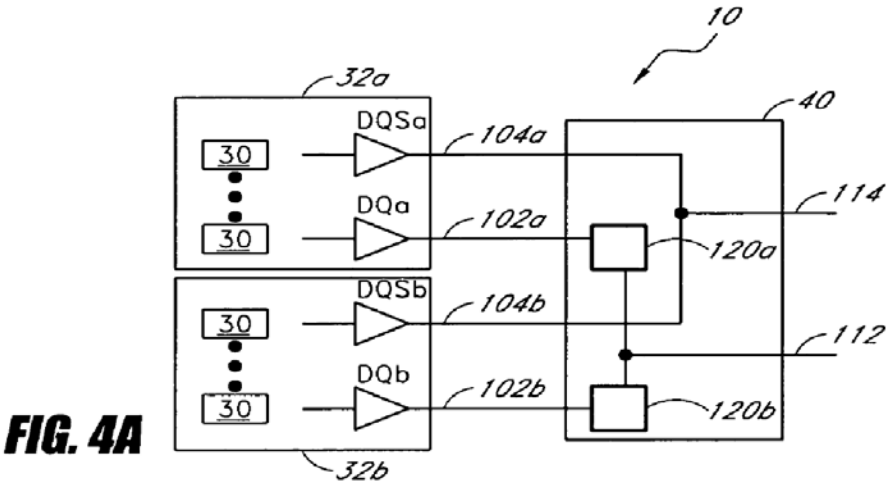

FIG. 4A

[4] The Board issued an affirmance in the Reexamination (Ex. 1005, 1947–1970, 2058–2063), of the Examiner's Action Closing Prosecution (*id*. at 1494–1525), which determined that the reexamined amended and unamended claims were patentable. On appeal to the Federal Circuit, the Board's determination was upheld. *Inphi Corp. v Netlist, Inc*., 805 F.3d 1350 (Fed. Cir. 2015). The Reexamination considered different prior art than the art at issue under this review.

Figure 4A above is a schematic illustration of example memory modules with a circuit and data signal lines. Ex. 1001, 3:48–53. Circuit 40 may selectively isolate or selectively electrically couple data signal lines 102a and 102b of memory ranks 32a and 32b with common data signal line 112. *Id*. at 7:44–8:3, Fig. 4A. The circuit receives a set of input command and address signals from the memory controller and, in response, generates a set of output address and command signals. *Id*. at 16:10–18. Figure 9A is reproduced below.

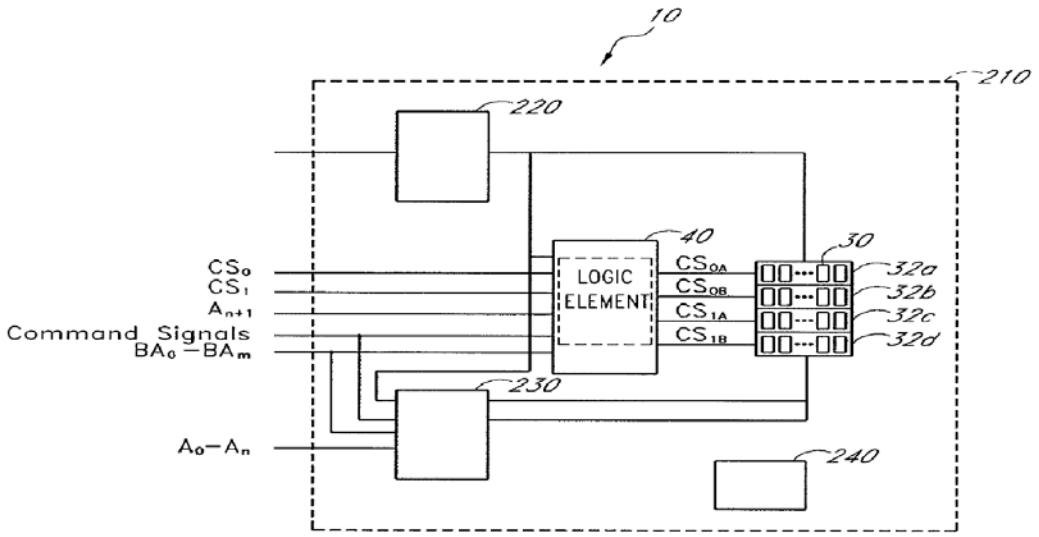

FIG. 9A

Figure 9A above is a schematic illustration of an example memory module with four ranks of memory devices. Ex. 1001, 4:5–7. Memory module 10 is connectable to memory controller 20, and comprises printed circuit board 210, memory devices 30, and circuit 40. *Id*. at 15:7–17. Circuit 40 receives a set of input address and command signals from the computer system, and generates a set of output address and command signals in response to the set of input signals. *Id*. at 15:21–23. In some embodiments, circuit 40 receives a set of input address and command signals that corresponds to a number of memory devices for which the

computer system is configured, and outputs a set of output address and command signals that correspond to a larger number of memory devices 30. *Id*. at 16:19–24. In certain embodiments, memory module 10 simulates a virtual memory module by operating as having a certain number of ranks of memory devices 30. *Id*. at 16:31–40. In certain embodiments, "the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices 30 to which it is coupled," where "the memory module 10 operates as having a data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another, from the ranks on other memory modules, and from the computer system." *Id*. at 8:48–62.

Claim 1, reproduced below, is illustrative of the challenged claims of the '537 patent, with emphasis on the limitation that is the subject of dispute between the parties.

1. A memory module comprising:

> a plurality of memory devices, each memory device having a corresponding load; and
>
> a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, *the circuit selectively isolating one or more of the loads of the memory devices from the computer system*, the circuit comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects, wherein the plurality of memory devices comprises double-data rate (DDR) dynamic random-access memory (DRAM) devices and the chip selects of the first and second number

> of chip selects are DDR chip selects that are not CAS, RAS, or bank address signals.

Ex. 1001, Reexam. Cert. 1:23–42.

II. ANALYSIS

A. The Parties' Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1–17, 24–38, and 45–55 of the '537 patent would have been unpatentable under 35 U.S.C. § 103 over Amidi and Klein. Dec. 19–24. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–17, 24–38, and 45–55 are unpatentable under 35 U.S.C. § 103(a) over Amidi and Klein. 35 U.S.C. § 316(e). We previously instructed Patent Owner that "any arguments for patentability not raised and fully briefed in the [Patent Owner Response] will be deemed waived." Paper 11, 3; *see also* 37 C.F.R. § 42.23(a) ("Any material fact not specifically denied may be considered admitted."); *In re Nuvasive, Inc*., 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board's Trial Practice Guide states that the Patent Owner Response "should identify all the involved claims that are believed to be patentable and state the basis for that belief." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive arguments and evidence presented by Petitioner regarding the manner in which the asserted prior

art teaches corresponding limitations of claims 1–17, 24–38, and 45–55. Based on the preponderance of the evidence before us, we conclude that the art identified by Petitioner teaches or suggests all of the limitations of the reviewed claims.

B. Claim Construction

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as they would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

"selectively electrically coupling/couples"

As discussed in the Institution Decision, the 882 IPR, 883 IPR, and 1011 IPR were directed to different patents, but the patents are related and have the same specification as the '537 patent. *See* Dec. 3. Here, we adopt the Federal Circuit's broadest reasonable construction from the 882, 883, and 1011 IPRs of the term "selectively electrically coupling" as "coupling in response to a selection." *See Netlist*, 701 Fed. App'x at 1004.

"selectively isolating/isolates"

The Federal Circuit decision in the 882, 883, and 1011 IPRs finds that "[t]he specification uses the terms 'coupling' and 'isolating' in a similar fashion," and directs that the term be construed in view of the construction of the term "selectively electrically coupling." *Netlist, Inc.*, 701 Fed. App'x at 1005. Accordingly, we construe the term "selectively isolating" as "isolating in response to a selection," which conforms with the Federal Circuit's direction, and also is

consistent with the Patent Owner's proposed construction for the term. PO Resp. 5.

Other Terms

The parties do not propose constructions for any additional claim terms. We determine that it is not necessary to provide an express interpretation of any other term of the claims because it is not necessary to resolve any issues or disputes. *Vivid Techs., Inc. v. Am. Sci. & Eng'g*, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999)) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.").

C. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art at the time of the '537 invention would be "someone with an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field." Pet. 3–4 (citing Ex. 1003 ¶ 48). Dr. Stone further testifies that a person of ordinary skill in the art

> would have been knowledgeable about the design and operation of computer memories, most particular DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and more low level circuits such as tri-state buffers, flip flops and registers.

Ex. 1003 ¶ 48.

Patent Owner's expert offers a proposed level of qualification to include:

> an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market.

Ex. 2001 ¶ 14. Patent Owner's expert agrees with Petitioner's proposed level of skill. Ex. 2001 ¶ 18.

We adopt and apply this assessment of the level of ordinary skill in the art articulated by Petitioner to our obviousness analysis in this proceeding. In addition, we note that the art of record in this proceeding—namely, Amidi and Klein—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Asserted Obviousness of Claims 1–17, 24–38, and 45–55 by Amidi and Klein

In support of this asserted ground of unpatentability, Petitioner explains how the combination of Amidi and Klein would have rendered obvious claims 1–17, 24–38, and 45–55. Pet. 45–64. In its Response, Patent Owner contends that impermissible hindsight was used in the obviousness challenge, that one of ordinary skill in the art would not have been motivated to combine Amidi and Klein, and that the combination would not have had a reasonable likelihood of success. *See* PO Resp. 26–60. Patent Owner directs all its arguments to claim 1. *Id*.

Having considered all of the arguments and evidence, we find that Petitioner has demonstrated by a preponderance of the evidence that the combination of Amidi and Klein would have rendered obvious claims 1–17, 24–38, and 45–55 for the reasons discussed below.

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Ex. 1032, p. 12

We begin our analysis with summaries of Amidi and Klein, and then address the arguments and evidence presented by the parties.

1. Amidi (Ex. 1006)

Amidi discloses a memory interface system with a processor, a memory controller, and a memory module. Ex. 1006, 1:21–23. According to Amidi, a memory interface system in the prior art is shown in Figure 1, reproduced below.

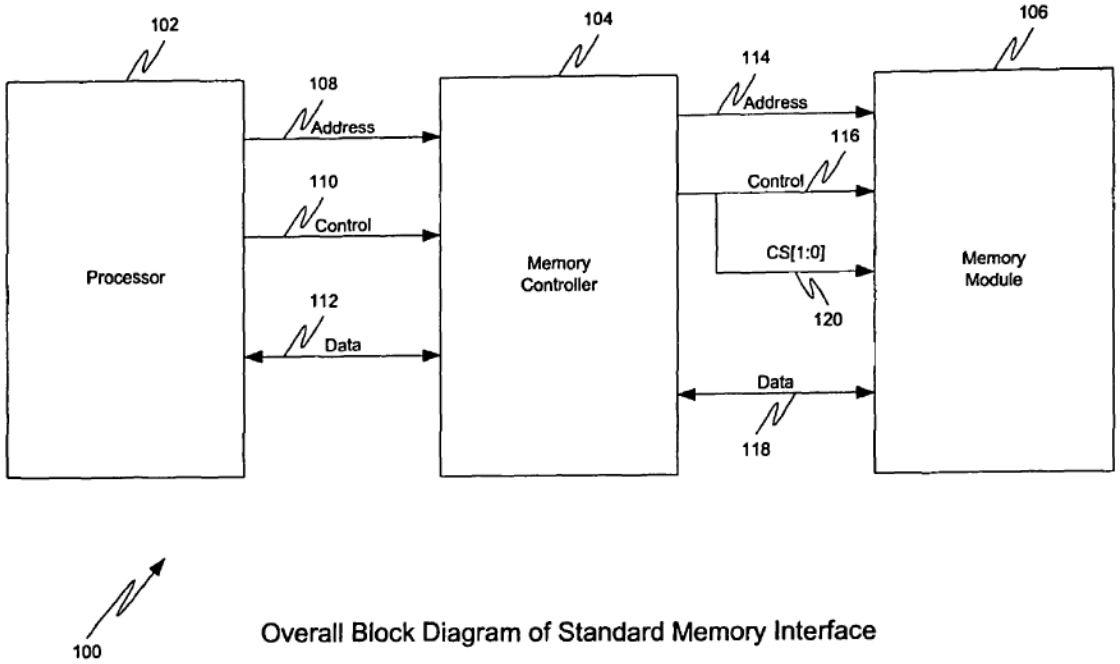
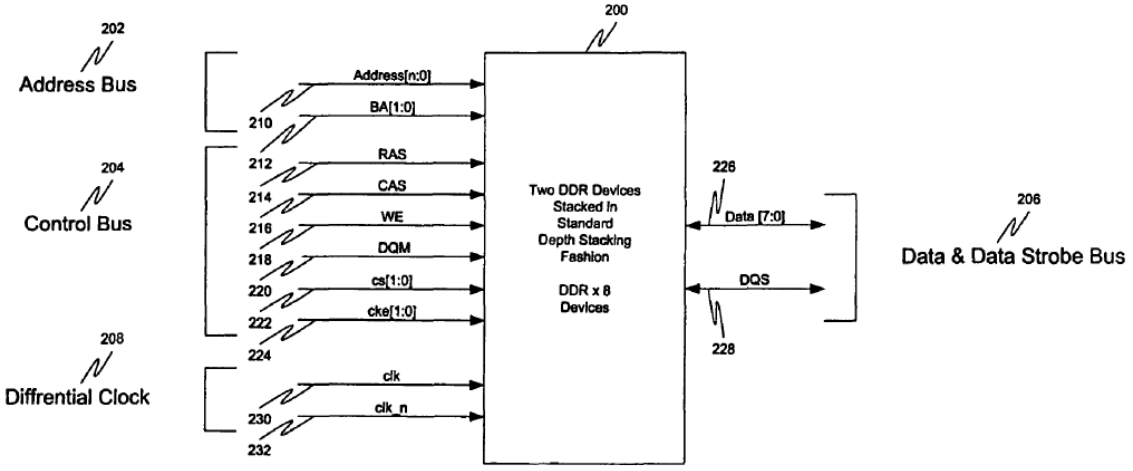


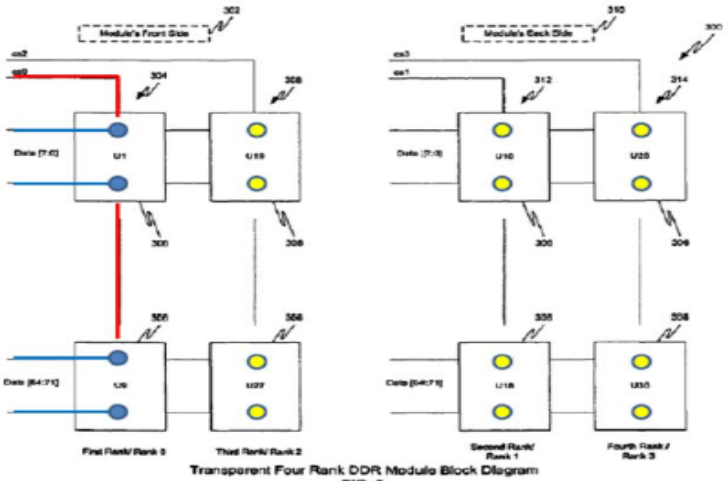
Figure 1 is a schematic of a standard prior art memory interface system with memory module 106 with controller address bus 114, controller control signal bus 116, and controller data bus 118. Ex. 1006, 1:21–29, 3:5–6, Fig. 1. As illustrated in Figure 1, memory module 106 communicates with memory controller 104 via busses 114, 116, 118. *Id*. at Fig. 1. Amidi discloses that each stack of double data rate (DDR) memory devices has a data signal line and a data strobe line (DQS), as shown in Figure 2 below. *See id*. at 4:24–30.



Standard DDR Device Depth Stacking Block Diagram

FIG. 2

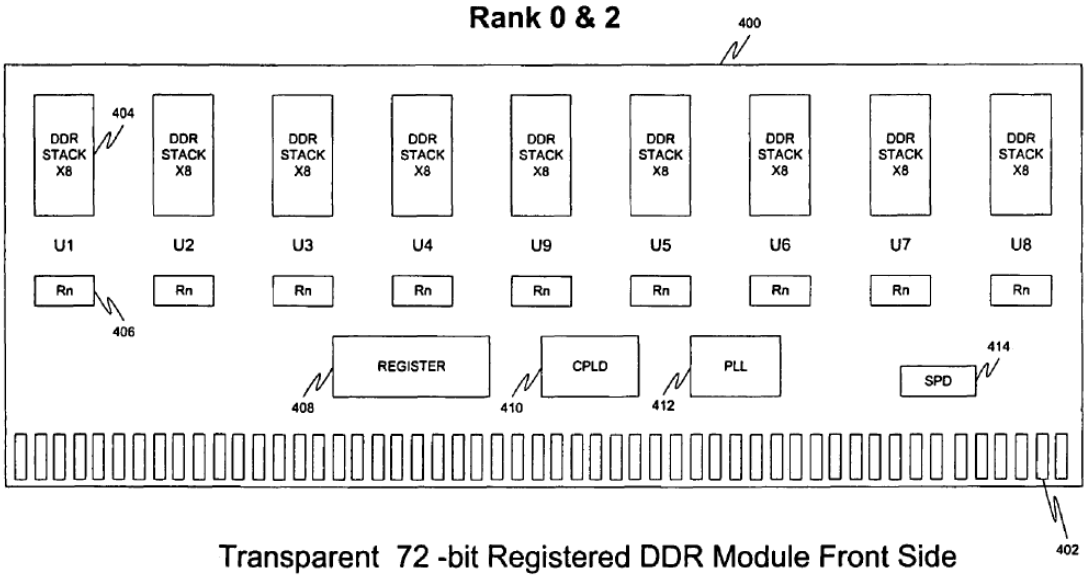
Figure 2 is a diagram illustrating a stacked DDR device. Ex. 1006, 3:7–9. Amidi discloses a four-rank memory module with logic that allows the four rank memory module "to communicate with a memory socket having only two chip select signals routed." *Id*. at 4:61–64. Figure 3 of Amidi, which is reproduced in an annotated form by Petitioner below, illustrates Amidi's four-rank memory module.



Transparent Four Rank DDR Module Block Diagram
FIG. 3

EX1006, Amidi at Fig. 3 (annotated).
Active rank selection signal, cs0, red. Active rank data path and data pin, blue. Inactive ranks data pins, yellow.

Figure 3, in annotated form above, depicts stacked 8-bit memory devices on the front and back side of memory module 300. Ex. 1006, 4:33–35. Each rank includes nine memory devices (e.g., U1 to U9 for rank 0, U19 to U27 for rank 3, etc.). *Id*. at 4:36–39. The memory devices in each rank of memory devices are coupled to a chip select signal corresponding to that rank. *Id*. at 4:43–46. Figure 4A of Amidi is reproduced below.



Transparent 72 -bit Registered DDR Module Front Side
FIG. 4A

Figure 4A is a diagram schematically illustrating the front side of transparent 72-bit registered double data rate (DDR) module 400 in an embodiment of the invention. Ex. 1006, 3:13–15, 4:65–67. Amidi's memory module includes complex programmable logic device (CPLD) 410 that

> emulates a two rank memory module on the four rank memory module 400. CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module where typically a two rank memory module couples with the memory socket. The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410.

Id. at 5:30–39.

Register 408 and phase-lock loop device (PLL) 412 provide one or more input control signals to the rank of memory devices activated by the generated chip select signals and thereby may control loading. *Id*. at 5:15–26.

2. Klein (Ex. 1007)

Klein discloses a method for bus capacitance reduction. Ex. 1007, Abstract. According to Klein, data bus capacitance is reduced by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits. *Id*. In one embodiment, memory controller 22 connects to circuitry 26 for interfacing with one or more memory circuits 28, as shown in Figure 3, reproduced below. *Id*. ¶ 28, Fig. 3.

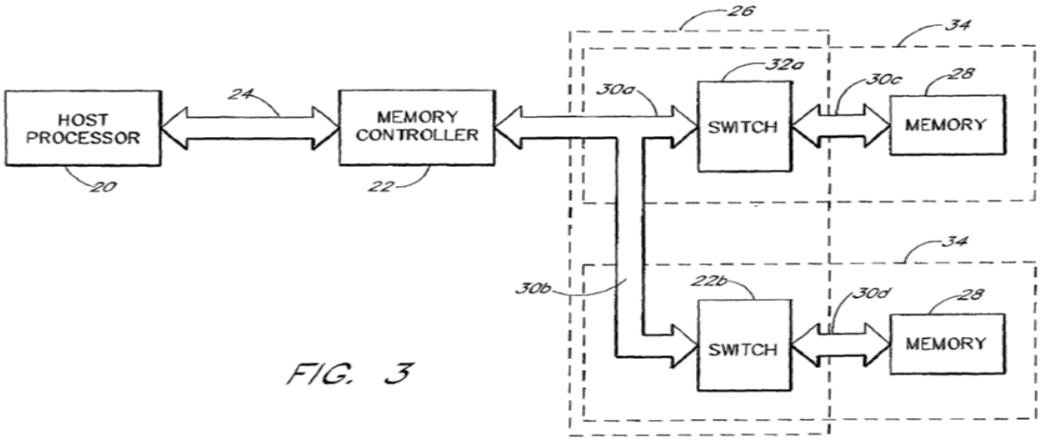


FIG. 3

Figure 3 illustrates that the data bus between memory controller 22 and memory elements 28 may comprise several branches 30a, 30b, one for each separate memory elements 28. *Id*. Each branch may include a switch, e.g., switch 32a or switch 22b, which may be used to selectively isolate a portion of the data bus, e.g., 30c or 30d, from memory controller 22. *Id*. Klein states that memory circuit 28 may be a conventional DRAM integrated circuit. *Id*. ¶ 29. The embodiment shown in Figure 3 may reduce the parasitic capacitance that the memory controller needs to charge and discharge during data transfers because a portion of the data

bus and the stray capacitance of unaccessed memory circuits are removed. *Id*. ¶ 28.

Another embodiment in Klein is illustrated in Figure 6, reproduced below.

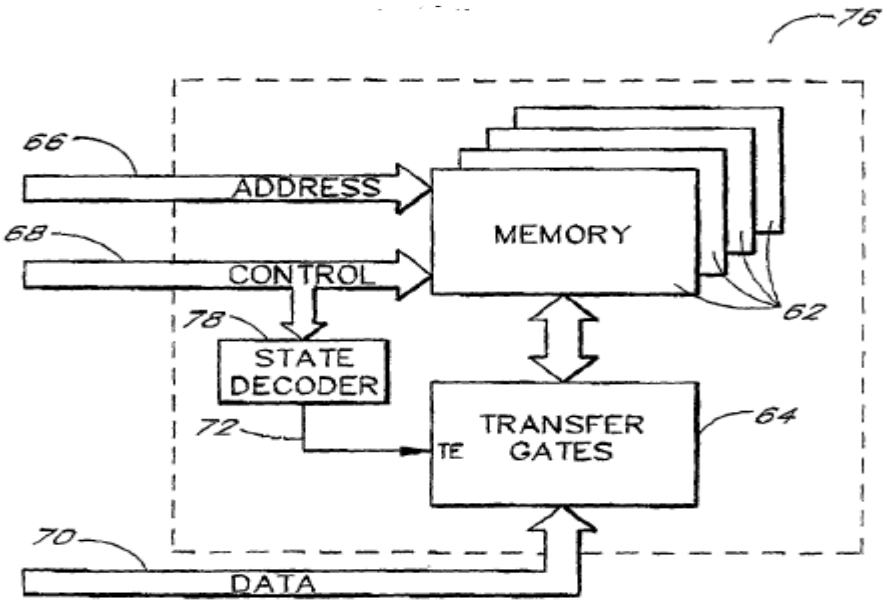


FIG. 6

As shown in Figure 6, a circuit is provided on memory module 76 that includes transfer gates 64 and state decoder 78. Ex. 1007 ¶¶ 35, 39. Klein discloses that state decoder 78 includes inverter 80 (*id*. ¶ 36), and that "state decoder 78 could comprise a state machine 84 made with a programmable gate array for example" (*id*. ¶ 37). Klein further discloses control logic circuitry, data buffer registers, and a bus switch are incorporated into memory modules. *Id*. ¶¶ 29, 39, 40, Figs. 3, 10. The integrated circuit and a transfer gate output are connected to data buffer registers. *Id*. ¶ 40, Fig. 10.

3. Analysis

To prevail on its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the

petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378–79 (Fed. Cir. 2015) (discussing the burdens of persuasion and production in *inter partes* review).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). For a determination of obviousness, there must be a showing that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (citing *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)).

[5] Patent Owner does not present arguments or evidence of objective indicia of nonobviousness in its Patent Owner Response.

a. Petitioner's Assertions

Petitioner contends that Amidi teaches a memory module with a plurality of memory devices with each memory device having a corresponding load by its disclosure of a memory module with four ranks of stacked memory devices. *See* Pet. 15–16.[6] Petitioner asserts that Amidi discloses "*a circuit electrically coupled to . . . memory devices . . . and a memory controller*" by its disclosure of the circuit formed of a complex programmable-logic device ("CPLD"), register, and phase-lock loop ("PLL") that receives signals from a memory controller and is electrically coupled to the memory devices. *Id*. at 16–17.

As to the "selectively isolate" limitation, Petitioner asserts that "[t]o the extent one might argue that Amidi does not teach '*the circuit selectively isolating one or more of the loads of the memory devices from the computer system*,' it would have been obvious to one of ordinary skill in the art to include it in the system of Amidi based on the teachings of Klein." Pet. 45–46. Petitioner contends that Klein teaches the use of a circuit that decouples memory elements from other data bus segments, with isolation of the load of the decoupled segments. *Id*. at 46 (citing Ex. 1007 ¶ 24). Petitioner alleges that the isolated memory element can be an entire memory module or a smaller memory element, such as an individual DRAM integrated circuit. *Id*. (citing Ex. 1007 ¶¶ 24, 28, 29, 32, 39, Fig. 10; Ex. 1003 ¶ 136). Petitioner refers to state decoder 78 that is electrically coupled to

[6] The evidence and argument presented in the Petition for Ground C is primarily directed "selectively isolating" limitation of claims 1, 13, 24, and 35. Pet. 45–53. From the Petition's Ground C discussion it is apparent that Grounds A and B sections are relied upon for the evidence and argument of Amidi's teachings of the other limitations of the claims, which are not in dispute. *See id.* at 15–46, 51–52. Patent Owner does not dispute the application of other portions of the Petition besides those in Ground C to other claim limitations.

memory devices and a memory controller. *Id*. (citing Ex. 1003 ¶ 137; Ex. 1007 ¶¶ 29, 33, Figs. 2, 5, and 6). Petitioner further contends that state decoder 78 and transfer gates 64 as shown in Figure 6 of Klein "selectively isolate the load of a memory element from the computer system," and, more specifically, that "state decoder 78 decouples a selected memory element from the bus when no memory access is being performed." *Id*. at 47 (citing Ex. 1003 ¶¶ 138–144; Ex. 1007 ¶¶ 22, 26, 33, 35–37, 41). Dr. Stone refers to inverter 80 of Figure 7, state decoder 78 of Figure 8, which includes state machine 84 with a programmable gate array that determines the status of memory accesses and "appropriately assert[s] the gate control signal 72 when data transfer is to occur," as well as decode circuit 86 of Figure 9 of Klein, as reproduced below. Ex. 1003 ¶¶ 140–143.

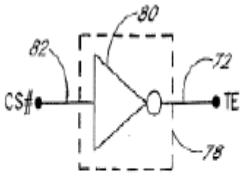


FIG. 7

EX1007, Klein at FIG. 7.

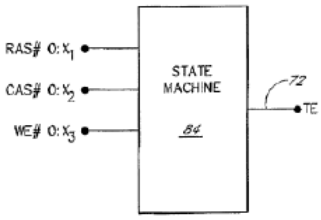


FIG. 8

EX1007, Klein FIG. 8

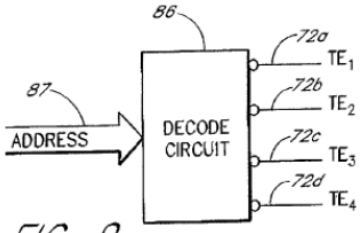


FIG. 9

EX1007, Klein FIG. 9.

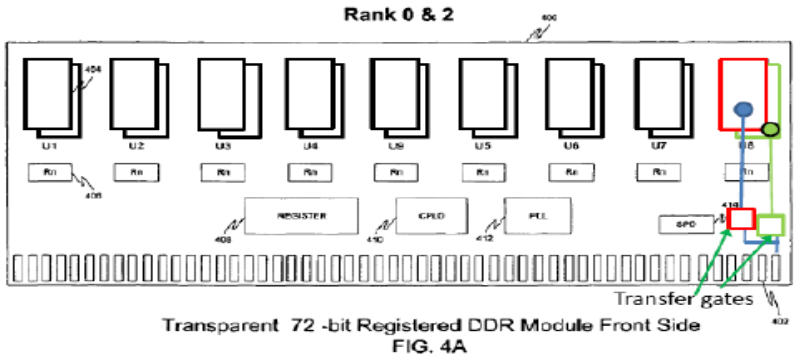
Figures 7, 8, and 9, above, are discussed in combination as teaching the control required of the claimed circuit. *Id*. Dr. Stone refers to Klein embodiments of state decoders and testifies

> It also would have been obvious to one of ordinary skill in the art that FIG. 8 . . . discloses a circuit that triggers an enable signal based on ***when*** to enable a transfer, whereas FIG. 9 discloses a circuit that triggers an enable signal based on ***what*** to enable. One of skill in the art would know that it is possible to combine FIGS. 8 and 9, to control both ***what*** to enable and ***when*** to enable it simply by enabling the decoder circuit of FIG. 9 by the output of the state machine 84 in FIG. 8. Further, Klein discloses that the embodiments are meant to be illustrative and that his teachings could be embodied "in other specific

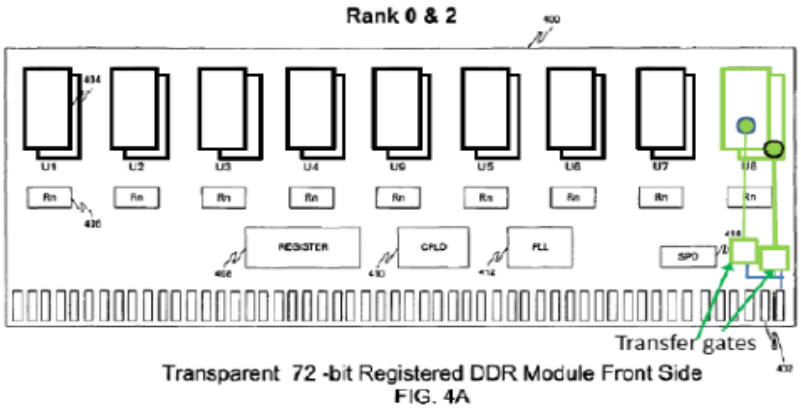
> forms without departing from its spirit or essential characteristics." EX1007 at 41. The obvious combination of Figs. 8 and 9 falls within the spirit of Klein's disclosure. Another obvious combination is to incorporate the chip select of FIG. 7 to control the decoder of FIG. 9, if such a chip select were part of the design.

Ex. 1003 ¶ 144.

Two annotated versions of Figure 4A of Amidi depict the proposed modification by Klein, including separate paths to the two data pins on the stacked memory devices. Ex. 1003 ¶ 147.



EX1006, Amidi at FIG. 4A (annotated).
The transfer gates are the transfer gates taught by Klein. In this figure, one device is selected, and one is not.



EX1006, Amidi at FIG. 4A (annotated).
The transfer gates are the transfer gates taught by Klein. In this figure, neither device is selected. The module data pin is isolated from the capacitance on the paths from the transfer gates to the unselected memory devices.

Dr. Stone testifies that the first annotated version of Figure 4A depicts the case where one of two devices is selected, and the second annotated version of Figure 4A depicts the case where the corresponding path to the module path is not selected. Ex. 1003 ¶ 149.

Dr. Stone further testifies

> Klein's circuitry consists of common, off-the shelf parts, such as transfer gate switches controlled by either state decoders or state machines, so the skilled artisan could have readily implemented a modification of Amidi that included such circuitry. Likewise, these embodiments offer the advantage that the transfer gates are controlled by commonly used chip select signals or RAS [row address strobe], CAS [column address strobe], and WE [write enable] signals. EX1007 at [0036, 0037].

Ex. 1003 ¶ 150.

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine the transfer gate switches of Klein with the circuitry of Amidi because the references are from the same field of endeavor and are at least reasonably pertinent to the problem addressed in the '537 patent. Pet. 47–48. More specifically, it is alleged that Amidi is directed to "an improved memory module having a different and increased number of ranks with cheaper, lower chip densities." *Id*. at 48 (citing Ex. 1006, 2:16–50). Petitioner describes Klein as "reduc[ing] the capacitance of the bus provided between a processor and one or more memory elements by decoupling a selected one of the memory elements from the bus when no memory access to or from the selected memory element is being performed." *Id*. (citing Ex. 1007 ¶¶ 10, 22, 28, 33). Petitioner also asserts that Klein is directed "to memory module configurations that increase the speed at which memory accesses can be performed by isolating memory devices from the full capacitive loading effects of the system memory data bus." *Id*. (citing Ex. 1007 ¶ 10; Ex. 1003 ¶ 145). With this, Petitioner contends that Klein discloses and

"explains why it is desirable to employ that technique [selective load isolation, as required by the claims] in order to avoid having the parasitic capacitance slow the speed of transfer." *Id*. (citing Ex. 1007 ¶ 7).

Petitioner also contends that Klein discloses selective load isolation and the motivation "to include [selective load isolation] in Amidi in a straightforward manner that would have been well within the level of ordinary skill in the art." Pet. 48–49 (citing Ex. 1003 ¶¶ 146, 147–150). Petitioner also relies upon the alleged flexibility of Klein's circuitry to allow one of skill in the art to isolate memory elements or segments as needed, and the reduced load in combination "provides for a potentially faster system" than Amidi. *Id*. at 49. Additionally, Petitioner argues that the combination is an arrangement of old elements performing the same known functions, and yielding not more than one would expect from such an arrangement. *Id*. at 50.

As to other remaining limitations of claim 1, Petitioner contends that Amidi teaches the limitations related to the circuit comprising logic to translate between "a system memory domain of the computer system and a physical memory domain of the memory module," with system memory domain compatibility and the memory devices being the DDR DRAM devices as claimed. Pet. 18–21.

Petitioner's obviousness analysis, as supported by Dr. Stone's Declaration, relies on testimony as to where each element of challenged claim 1 is disclosed in the combination of Amidi and Klein. Pet. 45–50; Ex. 1003 ¶¶ 136–153. After having considered Patent Owner's arguments, which we address below, we agree with and adopt Petitioner's analysis and credit Dr. Stone's testimony.

b. Patent Owner's Arguments

Patent Owner argues that Amidi and Klein are improperly combined because impermissible hindsight has been employed, the combination would be inoperable,

and the combination is beyond the level of one of ordinary skill in the art. PO Resp. 26–59. As discussed in more detail below, Patent Owner does not directly allege that the combination of Klein and Amidi fails to teach all the limitations of representative claim 1 as to the limitation of "the circuit selectively isolating one or more of the loads." Rather, Patent Owner argues the alleged use of hindsight, teaching away, inoperability of the combination, and undue experimentation required for the combination are failings of the Petition—which are related to the skilled artisan's view of the rationale to combine, as well as the reasonable expectation of success of the combination. *See id*. We find Patent Owner's arguments unpersuasive and we discuss them in turn.

i. Rationale to combine and impermissible hindsight

Patent Owner's arguments relate to Petitioner's reliance on Klein for teaching "the circuit selectively isolating . . ." limitation of claim 1, and the proposed combination with Amidi as shown in the annotated versions of Amidi's Figure 4A in Dr. Stone's declaration. PO Resp. 31–32. Patent Owner argues that the technical details concerning how the Klein transfer gates are implemented in the Amidi-Klein combination are provided only by the sentence in the Petition that states

> [a]n artisan would understand that the **transfer gate switches** could be controlled using the **decoded chip select signals from the CPLD** or the **RAS, CAS, and WE signals from Register 608** above.

PO Resp. 32–33 (quoting Pet. 50) (emphasis in PO Resp.).

Patent Owner also refers to Dr. Stone's testimony on the use of "state decoders or state machines"

> Additionally, Klein's circuitry consists of common, off-the shelf parts, such as **transfer gate switches** controlled by **either state decoders or state machines**, so the skilled artisan could have readily implemented

> a modification of Amidi that included such circuitry. Likewise, these embodiments offer the advantage that the transfer gates are controlled by **commonly used chip select signals** or **RAS, CAS, and WE signals**. EX1007 at [0036, 0037].

PO Resp. 33 (quoting Ex. 1003 ¶ 150) (emphasis in PO Resp.).

Based on these disclosures, Patent Owner asserts that the Petition limits its contentions for the control of the four Klein transfer gates to two options, which Patent Owner characterizes as:

- <u>either</u> (i) Klein's state decoder 78 of Fig. 7 using "the decoded chip select signals from the CPLD" (Pet. 50) ("sub-proposal (i)")
- <u>or</u> (ii) Klein's state machine 84 of Fig. 8 using "the RAS, CAS, and WE signals from Register 608" (*id*.) ("sub-proposal (ii)").

PO Resp. 34 (citing Ex. 2001 ¶ 66) (emphasis in PO Resp.).

Patent Owner argues that one of skill in the art would not have had a reasonable expectation of success in combining Amidi and Klein as proposed. PO Resp. 35–36. More specifically, Patent Owner alleges that Petitioner's proposed combination uses Klein's elements in a different manner in Amidi than their original use. *Id*. at 37.

Patent Owner contends that the use of Klein's state decoder (element 78 in Figure 7) or state machine (element 84 in Figure 8), is "beyond any suggestions of Amidi and Klein," and that the proposed arrangement using Amidi's output (CS or RAS, CAS, WE) "misplaces" Klein's teachings in Amidi. PO Resp. 38. Patent Owner argues that use of Amidi's output signals generated on module as input to Klein is a non-obvious implementation of Klein's transfer gate in Figure 6, which is based on signals from an off-module memory controller. *Id*. As such, Patent Owner avers, in part, that such a combination would not have been obvious to a

person of ordinary skill in the art and is based upon impermissible hindsight. *Id*. at 39.

Patent Owner also alleges that under Petitioner's depiction of annotated Figure 4A, the assertion that "one device is selected, and one is not," is in relation to the same memory module, which Patent Owner alleges is an attempt to implement Klein at a rank or device level (not module), but this is not disclosed by Amidi or Klein. PO Resp. 40–41, 43. In support, Patent Owner argues that "Klein actually teaches that its transfer gates and even other switches operate at the module-level (not rank-level nor device-level)." *Id*. at 41 (citing Ex. 1007 ¶¶ 24, 30, 33–35, 38) (emphasis in PO Resp.). Patent Owner asserts that Petitioner is implementing Klein's module-level teaching at rank or device level and is, therefore, employing impermissible hindsight. *Id*. at 43.

Petitioner responds that Patent Owner's arguments regarding on-module control rely solely on attorney argument that are unsupported by expert testimony. Pet. Reply 7.[7] Petitioner further argues that Patent Owner misreads Klein. *Id*. at 6. More specifically, Petitioner contends that Patent Owner's allegation that "[t]ransforming the off-module control scheme of Klein into the on-module control scheme" is only possible by hindsight is directly contradicted by Klein's specification, and that Patent Owner fails to consider Klein's teachings in context. *Id*. Petitioner alleges, and Dr. Stone provides supporting testimony, that Klein teaches that its switch and control circuitry can be "placed on a single IC, or may be provided in a multi-chip package" (Ex. 1007 ¶ 29), and the FET switches, as

[7] Patent Owner contends that portions of Petitioner's Reply are allegedly beyond the scope of what is considered appropriate for a reply. *See infra* Section III. As discussed below, however, we find that the disputed portions of Petitioner's Reply and associated evidence are within the scope of what is appropriate for a reply and may be considered. *See id*.

well as the control signals to activate the switch gates, can be mounted on-module (*id*. ¶¶ 29, 35, Figs. 3, 6), off-module (*id*. ¶¶ 29–30, Fig. 4), or incorporated into the memory device itself (*id*. ¶ 39–40, Fig. 10). *Id*. at 7–9.

For a finding of obviousness, there has to be a showing of a suggestion, teaching, or motivation to combine the prior art references. *C.R. Bard, Inc. v. M3 Sys. Inc*., 157 F.3d 1340, 1352 (Fed. Cir. 1998); *see also KSR*, 550 U.S. at 421. A finding of obviousness also requires that there be a reasonable expectation of success of the combination of the references. *See KSR*, 550 U.S. at 421 (discussing "predictable solutions" and "anticipated success."). As discussed in *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc*., 567 F.3d 1314, 1326 (Fed. Cir. 2009), under *KSR*, "the 'predictable result' . . . refers not only to the expectation that prior art elements are capable of being physically combined, but also that the combination would have worked for its intended purpose." The inquiry into obviousness, with the assessment of a rationale to combine and the reasonable expectation of success, is through the view of a person on ordinary skill in the art. *See KSR*, 550 U.S. at 421.

We agree with the Petitioner that Klein teaches that its switch, control circuitry, and control logic can be incorporated at device level and, therefore, Patent Owner's arguments based on the on-module versus off-module distinction is contrary to Klein's disclosures. *See* Ex. 1007 ¶¶ 29, 30, 35, 39, 40, Figs. 3, 4, 6, 10. We also agree that Patent Owner's argument is not supported by its own expert testimony from Dr. Sechen, which instead is consistent with Petitioner's arguments. *See* Ex. 1030, 137:12–138:25.

We also find the Petition's support of the rationale to combine Amidi and Klein to be sufficient to demonstrate articulated reasoning with rational underpinnings that support the legal conclusion of obviousness. *See* Pet. 48–50;

KSR, 550 at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). The prior art references are both directed to the control of memory elements, with advantages offered by the addition of Klein's circuitry to Amidi to allow isolating memory elements or segments as needed, and reduce loads to provide a potentially faster system operation. *See* Pet. 48–49. Patent Owner's argument on the "misplacement of" Klein's teachings in Amidi includes the allegation that the combination of the references is a new and non-obvious implementation of Klein. PO Resp. 38–39. We do not find that the proposed arrangement of Amidi and Klein is "beyond the suggestions of Amidi and Klein." To the contrary, the relied-upon features are the teachings of Klein's circuity, which are used in both Klein and in combination with Amidi for similar purposes, i.e. for decoupling or isolating of memory elements, and Klein's circuitry may be used in an on-module control scheme. Pet. 47–50. Patent Owner's arguments are also addressed to the alleged inoperability of the combination (PO Resp. 43–57), which we further discuss below.

ii. Sub-proposals

1. Limiting the Petition to Patent Owner's sub-proposals, generally

As identified above, Patent Owner parses and limits the Petition's contentions regarding the Amidi-Klein combination into two discrete alleged sub-proposals: sub-proposal (i) and sub-proposal (ii). *See* PO Resp. 30–35, 36–57. Patent Owner argues a limited view of the Petition relying on Petitioner's statements that identify control of transfer gate switches by "either state decoders or state machines" or "by commonly used chip select signals or RAS, CAS, and WE signals." *Id*. at 32–33 (citing Pet. 50; Ex. 1003 ¶¶ 150–151).

Petitioner argues that Klein "is not limited to Dr. Sechen's contrived embodiments," and instead Klein's embodiments, as depicted in Figures 7–9, illustrate potential decoders for creating the signals to operate the gates of the

transfer gate switches, where Klein "does not limit its teaching to these specific state decoders or to their suggested applications." Pet. Reply 11 (citing Ex. 1003 ¶¶ 144, 150; Ex. 1007 ¶¶ 27–40; Ex. 1015, 24; Ex. 2002, 168:15–172:16). Petitioner further contends that Patent Owner's reading of the Petition limiting it to only two sub-proposals is improper because this view ignores the teachings of Klein that disclose a variety of options, and improperly discounts the knowledge of one of ordinary skill in the art. *Id*. at 12–13.

The record supports a less limited view of the allegations in the Petitioner's challenge than that argued by Patent Owner. As discussed above, *supra* Section II.D.3.a, and contrary to Patent Owner's contentions, Dr. Stone testifies that Klein discloses alternative embodiments in support of the Petition, such as the state decoder depicted in Figure 8, and the state machine of Figure 9, and he further testifies that "one of skill in the art would know that it is possible to combine [them], to control both ***what*** to enable and ***when*** to enable it." Ex. 1003 ¶ 144. Dr. Stone further testifies that Klein discloses that the embodiments are meant to be illustrative and that his teachings could be embodied "in other specific forms without departing from its spirit or essential characteristics," wherein the combination of Figures 8 and 9 "falls within the spirit of Klein's disclosure." *Id*. (citing Ex. 1007 ¶ 41). Dr. Stone testifies that "an artisan would have been motivated to use the circuitry of Klein, or something very similar, in order to enjoy some of the additional benefits provided by that circuitry." *Id*. ¶ 151. Further, the Petition explains that "the flexibility of the circuitry disclosed by Klein allows one of skill in the art to isolate a variety of memory elements or memory segments as needed." Pet. 49. Moreover, in the portions of the Petition and supporting testimony that Patent Owner alleges to be limiting, we do not discern any

suggestion that one of ordinary skill in the art's view of Klein should be limited to the discussion therein.

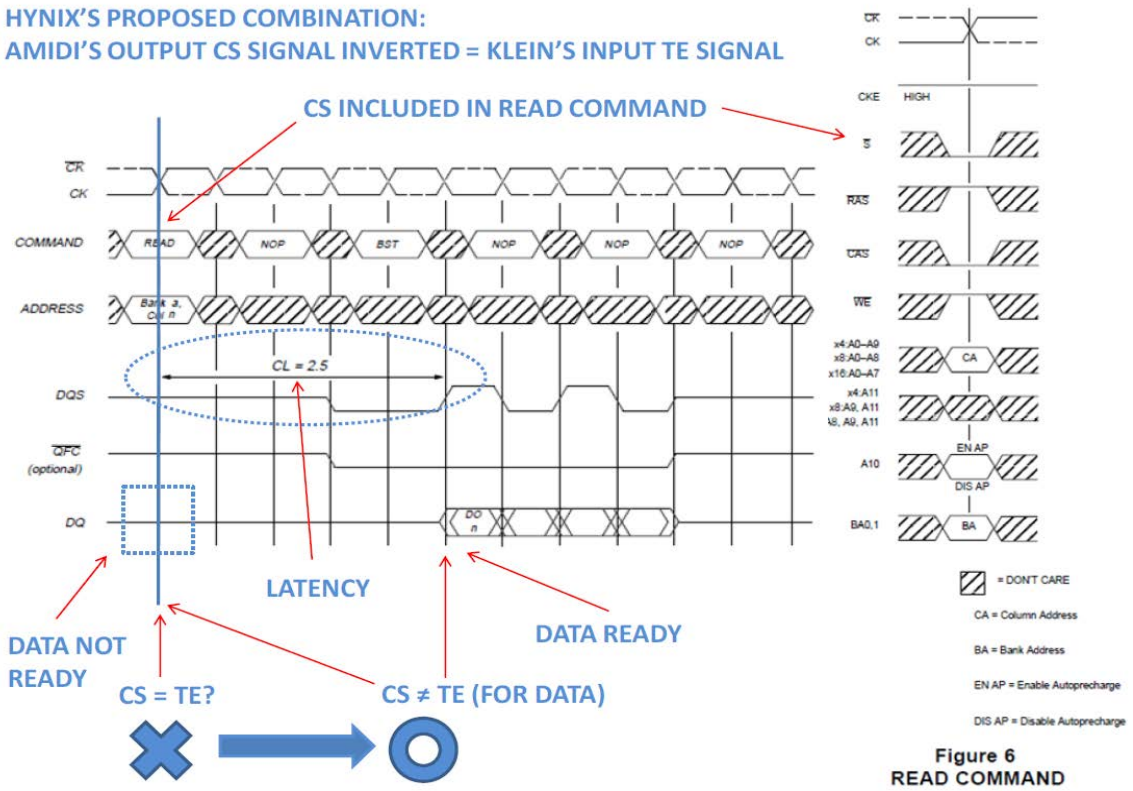
2. Alleged inoperability of sub-proposals

Although we do not find that Petitioner's challenge is limited to the sub-proposals that Patent Owner has identified, Petitioner has nonetheless argued the specifics of their alleged lack of operability. *See* Pet. Reply 43–57. We include a discussion of these issues here, not to suggest that they reflect the Petitioner's proposed combination as reflected in the Petition, but rather to address Patent Owner's allegations of inoperability in order to fully consider the arguments relating to the alleged lack of reasonable expectation of success of the combination.

Patent Owner argues that under sub-proposal (i), which is based on the use of Klein's state decoder 78 in Figure 7, a person of ordinary skill in the art would perceive inoperability, "which would direct him or her from any perception of reasonable expectation of success." PO Resp. 43. With this, Patent Owner contends that there should be no finding of obviousness for the Klein-Amidi combination because, even if there was a rationale to combine the references, one of ordinary skill in the art would not perceive a reasonable expectation of success. *Id*. at 51–52 (citing *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984); MPEP § 2143.01(V); *Broadcom Corp. v. Emulex Corp*., 732 F.3d 1325, 1335 (Fed. Cir. 2013)).

Patent Owner asserts that under sub-proposal (i), and based on Dr. Stone's testimony, "one of the possibilities is to connect Figure 7 to the input TE of Figure 2," and based upon this, "Amidi's CPLD output CS [chip select] signals inverted = Klein's input TE [transfer enable] signals." PO Resp. 44–45 (citing Ex. 2002, 167:16–169:11; Pet. 50). Patent Owner argues that under sub-proposal (i), the

combination would be inoperable due to timing problems. *Id*. at 45–49. Patent Owner relies on an annotated timing diagram of DDR command operations, reproduced below.[8] *Id*. at 46–47.



Patent Owner contends that in standardized DDR memory device operations, depicted above, there would be an improper result with no data read because the read command CS signal in Amidi would not coincide with its read data (as gated by Klein's input TE signal) because a DDR command is valid for only one clock cycle. PO Resp. 46–47 (citing Ex. 2001 ¶¶ 77–79). It is alleged that the same problem would apply to the write command. *Id*. at 47–48 (citing Ex. 2001 ¶ 79). Patent Owner further contends that using an inverted DDR chip-select signal as an input TE signal would be inoperable because the DDR chip-select signal lacks

[8] This figure is represented to be Figure 11 of Exhibit 1020, with annotations by Dr. Sechen. *See* Ex. 1031 ¶ 39; Ex. 2001 ¶ 77.

enough timing information for the proper operation of Klein's transfer gate. *Id*. at 48 (citing Ex. 2001 ¶ 82–87). Patent Owner also asserts that because Verilog code as disclosed in the '537 patent, which includes timing logic, is missing in Klein, Amidi, and the JEDEC specification, so one of ordinary skill would have insufficient information to build the timing circuit. Mot. Ob. 9 (citing Ex. 2007, 76:18–80:6).

Turning to sub-proposal (ii), Patent Owner argues that this option would also be inoperable, which would direct a person of ordinary skill away from a perception of a reasonable expectation of success. PO Resp. 52–57. Patent Owner alleges that under Klein's Figure 8 and its teachings of state machine 84 that operates based on RAS, CAS, WE signals, the command identification would be insufficient for properly controlling the four transfer gates on Amidi's memory module in combination. *Id*. at 56 (citing Ex. 2001 ¶ 93). Dr. Sechen testifies that Klein limits the teaching of Figure 8 to embodiments where the chip select is always asserted and, further, that Figure 8 is missing the critical chip select signal required to determine the correct rank for the DDR command. Ex. 2001 ¶¶ 88–95. Patent Owner asserts that the combination is based on Amidi's DDR SDRAM, which operates in accordance with the JESD79 standardized protocols, where "[e]xemplary DDR commands are in the JESD79 command table" reproduced below.

TRUTH TABLE 1a _ Commands
(Notes: 1)

NAME (Function)	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7
MODE REGISTER SET	L	L	L	L	Op–Code	2

(Ex. 1020, table of commands at 13; Ex. 2001, Sechen Decl., ¶ 92.)

PO Resp. 56.

Patent Owner argues that based on the command table above

> For instance, with a given set of RAS, CAS, WE signal values as HLH, state machine 84 might be able to have some indication that the target input DDR command is a READ command (HLH in command table above) but would be unable to determine the target rank for that READ command.

PO Resp. 56 (citing Ex. 2001 ¶ 93).

Patent Owner alleges that because the RAS, CAS, and WE signals lack any rank-identifying information, "Klein's state machine 84 in Fig. 8 would be unable to coordinate the rank-level operation of Hynix's four Klein transfer gates in the Amidi-Klein combination." PO Resp. 56–57. Patent Owner concludes by arguing "sub-proposal (ii) uses RAS, CAS, WE signals beyond their fundamental limitations, which a [person of ordinary skill in the art] POSITA would recognize as resulting in inoperability." *Id*. at 57.

We are not persuaded by Patent Owner's arguments. Figure 1 of Klein, reproduced below, depicts switch control.

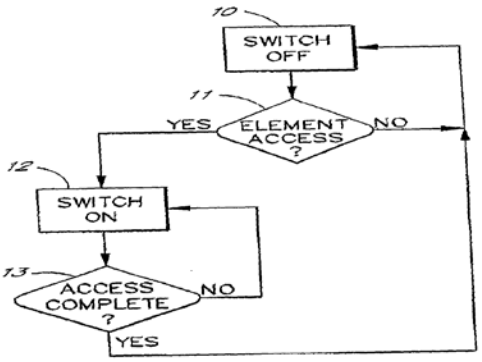


FIG. 1

Klein discloses, in reference to Figure 1 above, that

> As illustrated by block 13, once the switch is on, the system monitors whether or not the memory access has been completed. If not, the system continues to leave the switch in the on state. Once the memory access cycle has completed, the system loops back to block 10, and places the switch in the off state. Thus, the system decouples a memory element from a bus when no memory access to or from the selected memory element is being performed. It will be appreciated by those of skill in the art that the switch need not necessarily remain in the on state for the entire duration of any given memory access cycle. It will typically be sufficient to open the switch only during a portion of the memory cycle corresponding to the time during which valid information should be present on the bus which is routed through the switch.

Ex. 1007 ¶ 23.

We credit Dr. Stone's testimony that one of ordinary skill in the art would understand how to use the control logic identified in Figures 6–9 of Klein to control the switches in a combination of Klein and Amidi, with the timing taught in Klein for read/write. More specifically, Dr. Stone testifies that Klein's teachings on switch control to allow read/write to be completed for memory elements would be implementable in accordance with the JEDEC standard specifications for

memory devices and modules.[9] Ex. 1031 ¶¶ 5, 32–35. Dr. Stone refers to Truth Table 1a_Commands reproduced above, and testifies that one of ordinary skill in the art could use the control circuits of Klein in compliance with the JESD79 protocols to utilize the chip select (S), RAS, CAS, WE, and address signals to properly time the opening and closing of the transfer gate switches.[10] *Id*. ¶ 34. Dr. Stone also provides details of how to build the timing circuit in view of Klein and Amidi's teachings, thus, not requiring the use of Verilog code in the '537 patent. *See* Ex. 2007, 54:17–24, 56:2–58:3, 58:21–59:24, 145:25–146:9, 150:11–152:3, 153:15–154:16, 156:8–25, 168:9–169:22, 175:16–176:10, 183:5–185:5, 186:16–188:6. We agree with Petitioner that this testimony is consistent with the Petition, the Petitioner Reply, and the declarations of Dr. Stone. Mot. Ob. Resp. 13.

Petitioner also addresses Dr. Sechen's testimony asserting there is no teaching of the chip select signal required to determine the correct rank for the DDR command. Pet. Reply 17–18. Dr. Stone testifies that one of skill in the art would have understood that the control circuitry could be modified to include a decoded chip select from Amidi for the determination of the active rank. Ex.1031 ¶¶ 32–37. The evidence supports that Amidi's decoded chip select signal identifies a single rank for memory access, which could be used by the control circuit to determine the rank. *See* Ex. 1006, Fig. 3; Ex. 1003 ¶ 133; Ex. 1030, 94:7–21.

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[9] Dr. Sechen testified one of skill in the art in 2005 would have been familiar with the JEDEC standards, would have looked at it when designing a JEDEC compliant memory devices, and "needs to understand the JEDEC specifications and parameters for DRAM read or write accesses and the timing thereof, and needs to understand how the actual delays in specific DRAM chips relate to the JEDEC specifications." *See* Ex. 1030, 56:21–57:1, 84:3–19.

[10] As discussed above, *supra* Section II.D.3.b.ii, we do not agree with Patent Owner's attempt to limit the view of Klein to only two sub-proposals, and, therefore, the Stone testimony regarding the Klein components in combination is appropriate to consider.

In further support of operability, Dr. Stone also refers to the annotated version of the DDR command operations diagram, as annotated by Dr. Sechen (*see supra* 31), which operates in accordance with standardized protocol JESD79, and which was relied upon by Patent Owner for its assertions relating to the timing of read/write commands. Ex. 1031 ¶ 39. Dr. Stone testifies that the QFC signal, shown as "optional" in the diagram, may be used for timing the transfer enable signal as taught by Klein, with the stated purpose described below.[11] *Id*. ¶¶ 40, 41 (citing Ex. 1007 ¶ 23; Ex. 1020, 12).

$\overline{\text{QFC}}$ Enable/Disable

The $\overline{\text{QFC}}$ signal might be provided by certain vendors to control FET switches used to isolate module loads from the system memory bus at times when the given module is not being accessed.

Ex. 1020, 12.

Dr. Stone testifies that "[i]n fact, the QFC signal has exactly the timing required to identify the timing window for READ and WRITE commands." Ex. 1031 ¶ 40. Dr. Stone refers to the QFC generator logic block in the function block diagrams of the JESD79 standard and testifies that one of ordinary skill in the art could specify the logic for implementation to ensure interoperability. *Id*. at ¶¶ 42–44 (citing Ex. 1020, 4). We find this testimony to be credible.

[11] Patent Owner argues that Dr. Stone testifies that "he does not rely" on the QFC discussion in the JEDEC specification, but does, in fact, rely upon it. Mot. Ob. 8 (citing Ex. 2007, 54:17–24, 72:3–16, 185:6–15, 186:17–23; Ex. 1031 ¶ 49). This testimony is acceptably provided in reply to respond to Patent Owner's arguments (*see supra* Section III). More specifically, we agree with Petitioner that although Dr. Stone did not rely on the QFC signal in his testimony in support of the Petition, this testimony is provided to rebut Dr. Sechen's allegation that a new timing signal would have to be engineered that is beyond the skill of one in the art. *See* Mot. Ob. Resp. 11–12; Tr. 40:15–41:2.

Accordingly, we find that there is sufficient evidence to demonstrate that the Amidi-Klein sub-proposals identified by Patent Owner would be operable which lends supports to Petitioner's contention that there is a reasonable expectation of success of the combination.

iii. Undue Experimentation

Patent Owner avers that even if the Petition overcomes its inoperability arguments, the modifications would have to be within the skill of a person of ordinary skill in the art and, in this case, undue experimentation would have been required to achieve an operable combination of Amidi and Klein. PO Resp 57.

The Supreme Court has stated that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR*, 550 U.S. at 417. Further, "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id*. at 421 (2007). The inquiry into obviousness, therefore, requires that we look at the teachings of the prior art through the lens of a skilled artisan who is a person of ordinary creativity. And, in doing so, we also consider the background knowledge and common sense of the person of ordinary skill. *See Perfect Web Techs., Inc. v. InfoUSA, Inc*., 587 F.3d 1324. 1329 (Fed. Cir. 2009).

Here, there is more agreement than not between the parties concerning the qualifications of a person of ordinary skill in the art and the standards that would be known to and employed by this person in viewing the prior art combination. Patent Owner's expert, Dr. Sechen, agrees with the Dr. Stone's opinion that a person of ordinary skill would "have been knowledgeable about the design and operation of computer memories, most particular DRAM and SDRAM devices that

were compliant with various standards of the day."[12] *See supra* Section II.C. Dr. Sechen testifies that these standards include JEDEC standards. *See id.*

As discussed above, Patent Owner assumes a limited view of the relied-upon disclosures of Klein, which colors its view of the difficulty of combining the prior art to reach an operable system. For instance, Patent Owner alleges that a person of ordinary skill in the art "would need to engineer an entirely new timing signal" from Klein's Figure 7 state decoder or its Figure 8 state machine and such an attempt would be beyond the level of a person of ordinary skill and would require undue experimentation. PO Resp. 59; Ex. 2001 ¶ 96. Dr. Sechen presents additional testimony on the complexity of timing considerations, concluding that the circuit would be beyond the skill level of a person of ordinary skill in the art. Ex. 2001 ¶ 97. He also testifies that "it is unlikely" that a person of ordinary skill in the art would be able to produce an operable combination with the "invented timing signals" and it would require an effort of at least several months. *Id*. at 99. However, as discussed, some of these arguments disregard the potential use of the QFC signal under JESD79 standard that can be used to achieve the same.

Additionally, we afford more weight to Dr. Stone's testimony that a skilled artisan could have readily implemented the combination of Klein and Amidi

[12] Patent Owner alleges that Dr. Stone's testimony concerning the qualifications of one of ordinary skill varied between his initial declaration (Ex. 1003) and his supplemental declaration (Ex. 1031) concerning knowledge in the design of memory devices. *See* Tr. 29:9–19. Our view is that Dr. Stone did not vary his testimony on the required qualifications, and rather was pointing out some wording differences in Dr. Sechen's articulation. *See* Ex. 1031 ¶¶ 6–7. Moreover, when questioned on whether any differences in articulation between the two experts mattered, Dr. Sechen testified "I don't find it to be of particular significance," and he also testified that he had analyzed the prior art under both articulations, and was not aware of any different conclusions that he would have formed under either. Ex. 1030, 50:3–19.

because Dr. Sechen's opinions on undue experimentation in implementation appear to be based on a misunderstanding of legal standards. Dr. Sechen testifies that his understanding of undue experimentation is when "the procedure for how to do that . . . is not plainly described or is not . . . well known by persons of ordinary skill." Ex. 1030, 62:6–16; *see also id*. at 62:22–63:16, 64:10–65:3. Dr. Sechen's view, in other words, would deem implementation that is not plainly described in a document or well known to one of skill in the art to require undue experimentation—and this sets too low a threshold.

Under *KSR*, "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421 (2007). An obviousness determination is not limited to instances where the person of ordinary skill already well knows how to combine the specific references or has a document that plainly describes how to do so. The references can be considered together with the knowledge of ordinarily skilled artisans. *In re Paulsen*, 30 F.3d 1475, 1480–81 (Fed. Cir. 1994) (citations and internal quotation marks omitted). Cited references, therefore, do not have to explain every detail to render a claimed invention obvious because the references speak to those skilled in the art. *Id*. at 1480. As discussed, one of ordinary skill in the art would have had knowledge of the JEDEC standard for memory devices and modules, as well as knowledge on the design and operation of computer memories, and could have predictably applied that knowledge in considering the combination of the prior art.

Therefore, we are not persuaded by Patent Owner's arguments regarding alleged undue experimentation. The evidence provided by Petitioner is sufficient to show that the combination of Amidi and Klein would have had a reasonable expectation of success.

c. Summary for Claim 1

For the reasons discussed above, we are persuaded Petitioner has shown by a preponderance of the evidence that claim 1 of the ’537 patent is unpatentable as obvious over Amidi and Klein.

d. Claims 2–17, 24–38, and 45–55

Petitioner’s obviousness analysis, as supported by Dr. Stone’s Declaration, relies on testimony as to where each element of challenged claims 2–17, 24–38, and 45–55 is taught in the combination of Amidi and Klein. Pet. 51–64. Patent Owner provides no separate arguments addressing claims 2–17, 24–38, and 45–55. *See* PO Resp. 26–60. We agree with and adopt Petitioner’s analysis and credit Dr. Stone’s testimony.

We are persuaded Petitioner has shown by a preponderance of the evidence that claims 2–17, 24–38, and 45–55 of the ’537 patent are unpatentable as obvious over Amidi and Klein.

III. ALLEGED IMPERMISSIBLE NEW ARGUMENTS IN PETITIONER REPLY

Patent Owner contends that Petitioner asserts new arguments in Petitioner’s Reply that are allegedly beyond the scope of what can be considered appropriate for a reply, and identified portions of the Reply at issue. PO Obj. 1–2. Petitioner filed a response identifying portions of the Patent Owner’s Response that it alleges its Reply is responsive to or where in the Petition the argument may be found. PO Obj. Resp. 1–2. In particular, Patent Owner objects to Petitioner’s reliance on address and command signals together, alleged reliance on Figure 10 of Klein, and the inclusion of a discussion of a QFC signal for switch timing generation. *See* PO Obj. 1–2.

We have considered Patent Owner's identification of the portions of Petitioner's Reply that are alleged to be beyond the scope of a reply, and determine that the cited portions of Petitioner's Reply and associated evidence are within the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response, and in particular, the majority of identified portions of the Reply fairly respond to Patent Owner's arguments on the inoperability of the sub-proposals. *See Idemitsu Kosan Co. v. SFC Co.*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arkane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do."). Moreover, the arguments to which Petitioner responds in its Reply are directed to the details of specific implementations that could not have been reasonably anticipated by Petitioner.

IV. PETITIONER'S MOTION TO EXCLUDE

Petitioner moves to exclude Dr. Sechen's opinions under FRE 702 because it alleges that the opinions provided are not acceptable expert testimony because they "are not the product of a reliable application of the accepted principles and methods to the facts." Pet. Mot. Ex. 1–2, 7–8. Petitioner asserts that Dr. Sechen's inoperability opinions rely on an improper definition of a person of ordinary skill in the art and on a legally incorrect definition of undue experimentation. *Id*. at 1. More specifically, Petitioner argues that Dr. Sechen had assumed a skilled artisan

would have some level of skill less than that required to implement the patent at issue, and counsel's direction to not answer questions during deposition prevented Petitioner from further testing the standard used. *Id*. at 2. Petitioner also alleges that Dr. Sechen presumed a standard for undue experimentation where "if a skilled artisan wants to alter the characteristics of an embodiment found in one disclosure, does not currently know how to make that transformation, and cannot readily identify an alternative disclosure explaining how to achieve that transformation, then that transformation requires 'undue experimentation.'" *Id*. at 4–5 (citing Ex. 1030 at 62:6–16, 62:25–63:16, 64:4–65:3).

Patent Owner opposes the motion, arguing that Dr. Sechen's testimony does not suggest an understanding of an incorrect level for one of ordinary skill in the art, and that Petitioner's counsel had an opportunity to revisit questioning on the issue during deposition. Pet. Mot. Ex. Opp. 6–7, 9–11. Patent Owner also alleges that the questions directed to Dr. Sechen concerning undue experimentation were legal in nature and Petitioner misapplies FRE 702. *Id*. at 12–13.

We have reviewed the arguments and determine such arguments are insufficient to have Dr. Sechen's opinions excluded in their entirety. Rather, it is within our discretion to assign the appropriate weight to be accorded evidence. *See* 37 C.F.R. § 42.65(a); *see also, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); and *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more

weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion.”).

V. CONCLUSION

For the foregoing reasons, we are persuaded Petitioner has demonstrated by a preponderance of the evidence that challenged claims 1–17, 24–38, and 45–55 of the ’537 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Amidi and Klein.

VI. ORDER

Accordingly, it is

ORDERED that claims 1–17, 24–38, and 45–55 of the ’537 patent are determined to be *unpatentable*;

FURTHER ORDERED that the Joint Motion to Limit the Petition is *granted*;

FURTHER ORDERED that Petitioner’s Motion to Exclude is *denied*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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