1Gb (32Mx32) GDDR5 SGRAM

H5GQ1H24AFR

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Revision History

Revision No.	History	Draft Date	Remark
0.1	Defined target spec.	Dec. 2008	Preliminary
0.2	Updated tRTPS / tRTW / tFAW / t32AW / Thermal Characteristics	Mar. 2009	Preliminary
0.3	Updated tCKE / Pin Cap / CRCWL / CRCRL/ IDD / PLL Value	April. 2009	Preliminary
0.4	Updated tRRDL / Revision ID/ Density ID Removed tFLK / tSTDBYLK	May. 2009	Preliminary
0.5	Updated tCKE / tCKSRE / tCKSRX (@ 6Gbps only)	May. 2009	Preliminary
0.6	Updated CRCWL / VREFD Selection Coding Updated Auto VREFD Training Updated tCKE & tPD Updated Leakage Current Updated x16 Mode IDD Value & 1.35V Timing Parameters Updated Ordering Information	July. 2009	Preliminary
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FEATURES

- Single ended interface for data, address and command
- Quarter data-rate differential clock inputs CK/CK# for ADR/CMD
- Two half data-rate differential clock inputs WCK/WCK#, each associated with two data bytes (DQ, DBI#, EDC)
- Double Data Rate (DDR) data (WCK)
- Single Data Rate (SDR) command (CK)
- Double Data Rate (DDR) addressing (CK)
- 16 internal banks
- 4 bank groups for t_{CCDL} = 3 t_{CK}
- 8n prefetch architecture: 256 bit per array read or write access
- Burst length: 8 only
- Programmable CAS latency: 5 to 20 t_{CK}
- Programmable WRITE latency: 1 to 7 t_{CK}
- WRITE Data mask function via address bus (single/double byte mask)
- Data bus inversion (DBI) & address bus inversion (ABI)
- Input/output PLL on/off mode
- Address training: address input monitoring by DQ pins
- WCK2CK clock training with phase information by EDC pins
- Data read and write training via READ FIFO
- READ FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO by WRTR command
- Consecutive read of READ FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic redundancy check (CRC-8)
- READ/WRITE EDC on/off mode
- Programmable EDC hold pattern for CDR
- Programmable CRC READ latency = 0 to 3 t_{CK}
- Programmable CRC WRITE latency = 7 to 14 t_{CK}
- Low Power modes
- RDQS mode on EDC pin
- Optional on-chip temperature sensor with read-out
- Auto & self refresh modes
- Auto precharge option for each burst access
- 32ms, auto refresh (8k cycles)
- Temperature sensor controlled self refresh rate
- On-die termination (ODT); nominal values of 60 ohm and 120 ohm
- Pseudo open drain (POD-15) compatible outputs (40 ohm pulldown, 60 ohm pullup)
- ODT and output drive strength auto-calibration with external resistor ZQ pin (120 ohm)
- Programmable termination and driver strength offsets
- Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
- Separate external VREF for address / command inputs
- Vendor ID, FIFO depth and Density info fields for identification
- x32/x16 mode configuration set at power-up with EDC pin
- Mirror function with MF pin
- Boundary scan function with SEN pin
- 1.6V / 1.5V +/- 0.045V supply for device operation (VDD)
- 1.6V / 1.5V +/- 0.045V supply for I/O interface (VDDQ)
- 170 ball BGA package

FUNCTIONAL DESCRIPTION

The GDDR5 SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. GDDR5 devices contain the following number of bits:

1 Gb has 1,073,741,824 bits and sixteen banks

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n-prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.

The GDDR5 SGRAM operates from a differential clock CK and CK#. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of CK#.

GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK/WCK#) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the GDDR5 SGRAM are burst oriented; an access starts at a selected location and consists of a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising CK# edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK# edge are used to select the bank and the column location for the burst access.

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ORDERING INFORMATION

Part No	Power Supply	CK Frequency	WCK Frequency	Max Data Rate	Interface
H5GQ1H24AFR-R0C	VDD/VDDQ = 1.6V	1.50GHz	3.00GHz	6.0Gbps/pin	POD_15
H5GQ1H24AFR-T3C	VDD/VDDQ = 1.5V	1.375GHz	2.75GHz	5.5Gbps/pin	
H5GQ1H24AFR-T2L (Note1)		1.25GHz	2.50GHz	5.0Gbps/pin	
H5GQ1H24AFR-T2C		1.25GHz	2.50GHz	5.0Gbps/pin	
H5GQ1H24AFR-T1C		1.125GHz	2.25GHz	4.5Gbps/pin	
H5GQ1H24AFR-T0C		1.00GHz	2.00GHz	4.0Gbps/pin	

Above Hynix P/N's are Leead-free, RoHS Compliant and Halogen-free.

Note.1)It supports not only 5Gbps @ 1.5V, but also 3.2Gbps @ 1.35V.

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0.1. DEFINITION OF SIGNAL STATE TERMINOLOGY

GDDR5 SGRAM will be operated in both ODT Enable (terminated) and ODT Disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT Enable mode. ODT Disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT Enable mode can not be guaranteed for a short period of time, i.e. during power up.

Following are four terminologies defined for the state of a device (GDDR5 SGRAM or controller) pin during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example in GDDR5 it is possible for the SGRAM pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled. For details on the GDDR5 SGRAM pins and their function see "PACKAGE SPECIFICATION" on page 156 and "SIGNALS" on page 158 in the section entitled "PACKAGE SPECIFICATION" on page 156.

Device pin signal level:

- High: A device pin is driving the Logic "1" state.
- Low: A device pin is driving the Logic "0" state.
- Hi-Z: A device pin is tristate.
- ODT: A device pin terminates with ODT setting, which could be terminating or tristate depending on Mode Register setting.

Bus signal level:

- High: One device on bus is High and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VDDQ
- Low: One device on bus is Low and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VOL(DC) if ODT was enabled, or VSSQ if Hi-Z.
- Hi-Z: All devices on bus are Hi-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: At least one device on bus is ODT and all others are Hi-Z. The voltage level on the bus would be nominally VDDQ.

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0.2. CLOCKING

The GDDR5 SGRAM operates from a differential clock CK and CK#. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of CK#.

GDDR5 uses a DDR data interface and an 8n-prefetch architecture. The data interface uses two differential forwarded clocks (WCK/WCK#). DDR means that the data is registered at every rising edge of WCK and rising edge of WCK#. WCK and WCK# are continuously running and operate at twice the frequency of the command/address clock (CK/CK#).

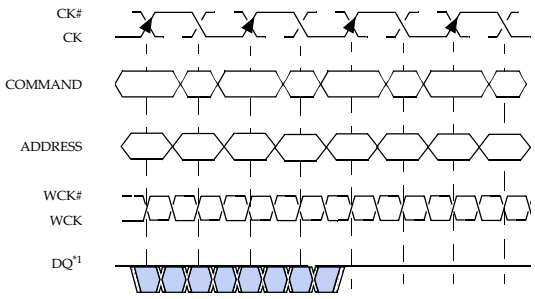


Figure 1: GDDR5 Clocking and Interface Relationship

Note : Figure.1 shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.

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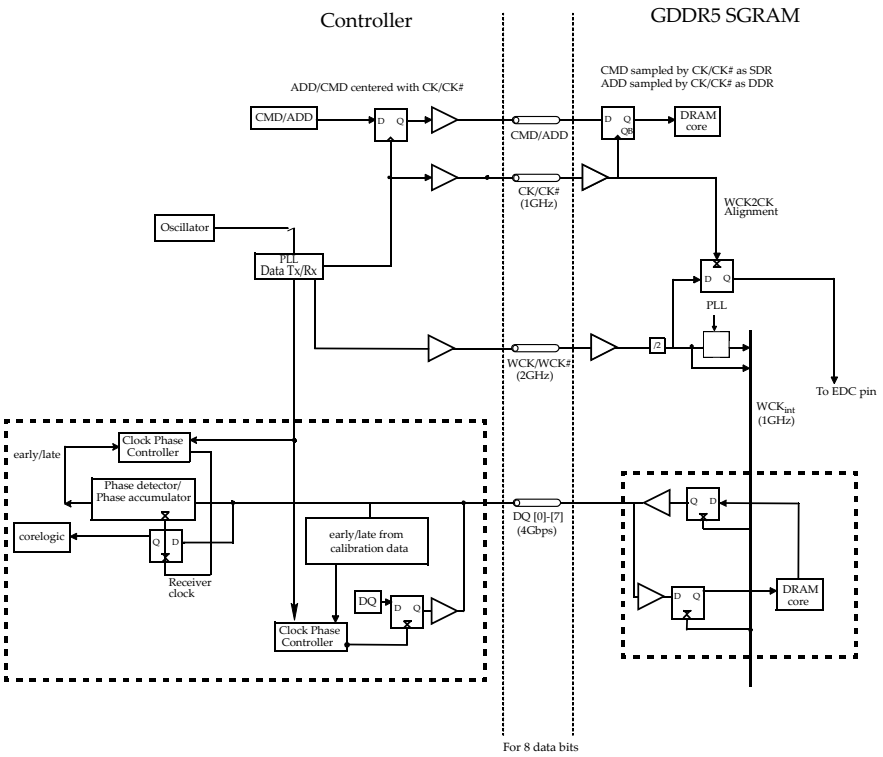


Figure 2: Block Diagram of an example clock system

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1. INITIALIZATION

1.1. POWER-UP SEQUENCE

GDDR5 SGRAMs must be powered up and initialized in a predefined manner as shown in <Link>Figure . Operational procedures other than those specified may result in undefined operation. The Mode Registers do not have RESET default values, except for ABI#, ADR/CMD termination, and the EDC hold pattern. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

Step	
1	Apply power to VDD
2	Apply power to VDDQ at same time or after power is applied to VDD
3	Apply VREFC and VREFD at same time or after power is applied to VDDQ
4	After power is stable, provide stable clock signals CK/CK#
5	Assert and hold RESET# low to ensure all drivers are in Hi-Z and all active terminations are off. Assert and hold NOP command.
6	Wait a minimum of 200µs.
7	If boundary scan mode is necessary, SEN can be asserted HIGH to enter boundary scan mode. Boundary scan mode must be entered directly after power-up while RESET# is low. Once boundary scan is executed, power-up sequence should be followed.
8	Set CKE# for the desired ADR/CMD ODT settings, then bring RESET# High to latch in the logic state of CKE#, t_{ATS} and t_{ATH} must be met during this procedure. See <Link>Table 1 for the values and logic states for CKE#. The rising edge of RESET# will determine x32 mode or x16 mode depending on the state of EDC1(EDC2 when MF=1). In normal x32 mode, EDC1 has to be sustained HIGH until RESET# is HIGH. See <Link>Table for the values and logic states for EDC1(EDC2 when MF=1).
9	Bring CKE# Low after t_{ATH} is satisfied
10	Wait at least 200µs referenced from the beginning of t_{ATS}
11	Issue at least 2 NOP commands
12	Issue a PRECHARGE ALL command followed by NOP commands until t_{RP} is satisfied
13	Issue MRS command to MR15. Set GDDR5 SGRAM into address training mode (optional)
14	Complete address training (optional)
15	Issue MRS command to read the Vendor ID
16	Issue MRS command to set WCK01/WCK01# and WCK23/WCK23# termination values
17	Provide stable clock signals WCK01/WCK01# and WCK23/WCK23#
18	Issue MRS commands to use PLL or not and select the position of a WCK/CK phase detector. The use of PLL and the position of a phase detector should be issued before WCK2CK training. Issue MRS commands including PLL reset to the mode registers in any order. t_{MRD} must be met during this procedure. WLmrs, CLmrs, CRCWL and CRCRL must be programmed before WCK2CK training.
19	Issue two REFRESH commands followed by NOP until t_{RFC} is satisfied
20	After any necessary GDDR5 training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for operation.

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Table 1 Address and Command Termination

VALUE (OHMS)	CKE# at RESET# high transition
ZQ/2	Low
ZQ	High

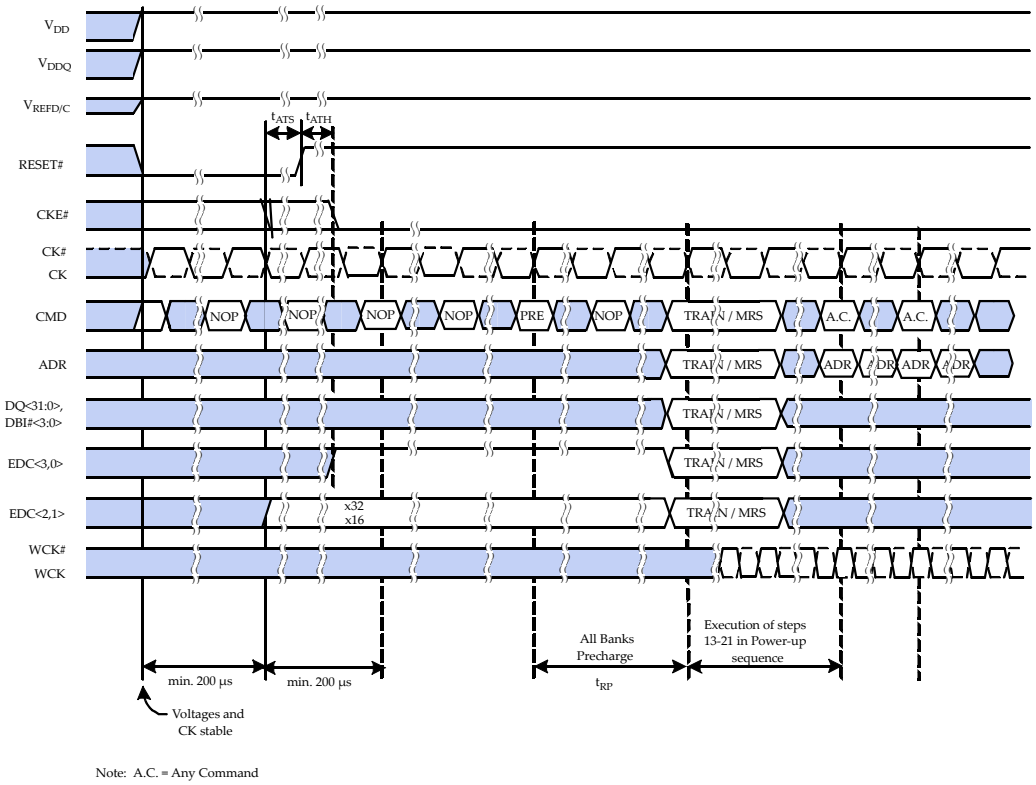


Figure 3: GDDR5 SGRAM Power-up Initialization

1.2. Initialization with Stable Power

The following sequence is required for reset subsequent to power-up initialization. This requires that the power has been stable within the specified VDD and VDDQ ranges since power-up initialization (See Figure 4)

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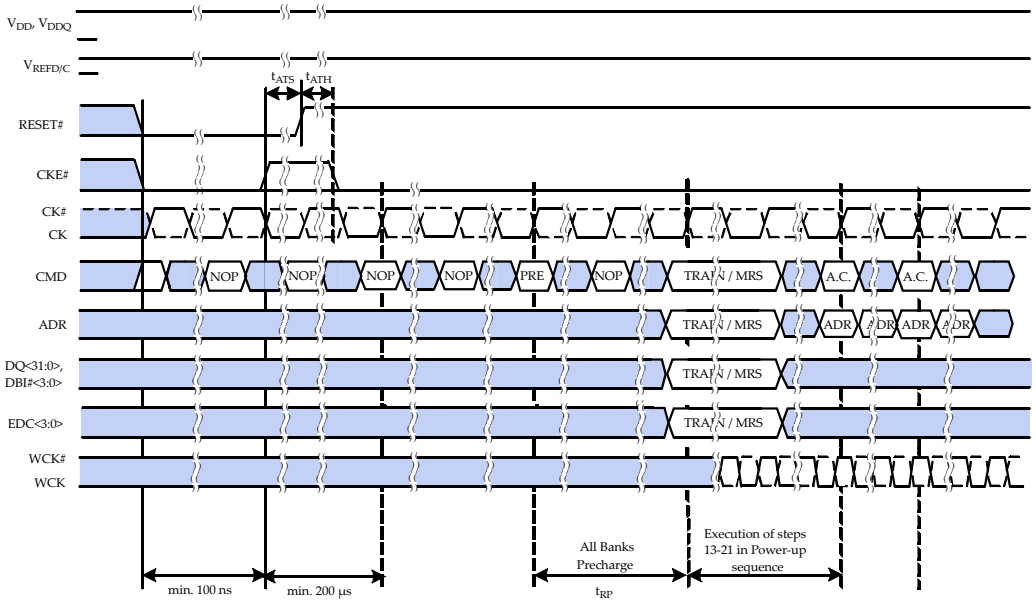
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1) Assert RESET# Low anytime when reset is needed.

2) Hold RESET# Low for minimum 100ns. Assert and hold NOP command.

3) Set CKE# for the desired ADR/CMD ODT settings, then bring RESET# High to latch in the logic state of CKE#; tATS and tATH must be met during this procedure. Keep EDC1 (MF=0) / EDC2 (MF=1) at the same logic level as during power-up initialization as device functionality is not guaranteed if the I/O width has changed.

4) Continue with step 9 of the power-up initialization sequence.



Notes: 1. A.C. = Any Command
2. Device functionality is not guaranteed if x32/x16 mode is not the same as during power-up initialization.

Figure 4: Initialization with Stable Power

1.2. VENDOR ID

GDDR5 SGRAMs are required to include a Vendor ID feature that allows the controller to receive information from the GDDR5 SGRAM to differentiate between different vendors and different devices using a software algorithm.

When the Vendor ID function is enabled the GDDR5 SGRAM will provide its Manufacturers Vendor Code on bits [3:0] as shown in Table 2; Revision Identification on bits [7:4]; Density on bits [9:8] ; FIFO Depth on bits [11:10] as shown in Table 3 & Table4. Bits [15:12] are RFU.

Vendor ID is part of the INFO field of Mode Register 3 (MR3) and is selected by issuing a MODE REGISTER SET command with MR3 bit A6 set to 1, and bit A7 set to 0. MR3 bits A0-A5 and A8-A11 are set to the desired values.

The Vendor ID will be driven onto the DQ bus after the MRS command that sets bits A6 to 1 and A7 to 0. The DQ bus will be continuously driven until an MRS command sets MR3 A6 and A7 back to 0 to disable the INFO field or to another valid state for the INFO field if the INFO field includes support for additional vendor specific information. The DQ bus will be in ODT state after $t_{WRIDOFF}$ (max). The code can be sampled by the controller after waiting t_{WRIDON} (max) and before $t_{WRIDOFF}$ (min). DBI is not enabled or ignored during all Vendor ID operations. Table 4 shows the mapping of the Vendor ID info to the physical DQs. The 16 bits of Vendor ID are sent on Byte 0 and 2 when MF=0. When MF=1 the 16 bits are sent on Byte 1 and 3. Optionally the vendor may replicate the data on the other 2 bytes when in x32 mode. Byte 0 would be replicated on Byte 1 and Byte 2 would be replicated on Byte 3 when MF=0. When MF=1, Byte 1 would be replicated on Byte 0 and Byte 3 would be replicated on Byte 2.

TABLE 2. Manufacturers Vendor Code

Manufacturers ID	Bit 3	Bit 2	Bit 1	Bit 0	Name of Company
0	0	0	0	0	Reserved
1	0	0	0	1	Samsung
2	0	0	1	0	Qimonda
3	0	0	1	1	Elpida
4	0	1	0	0	Etron
5	0	1	0	1	Nanya
6	0	1	1	0	Hynix
7	0	1	1	1	ProMOS
8	1	0	0	0	Winbond
9	1	0	0	1	ESMT
A	1	0	1	0	Reserved
B	1	0	1	1	Reserved
C	1	1	0	0	Reserved
D	1	1	0	1	Reserved
E	1	1	1	0	Reserved
F	1	1	1	1	Micron

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Table 3 Revision ID & Density & FIFO Depth

Revision ID				Density		FIFO	
Bit 7	**Bit 6**	**Bit 6**	**Bit 4**	**Bit 9**	**Bit 8**	**Bit 11**	**Bit 10**
0	0	0	1	0	1	1	0

Table 4 Vendor ID to DQ mapping

Bit	7	6	5	4	3	2	1	0
MF=0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
MF=1	DQ31	DQ30	DQ29	DQ28	DQ27	DQ26	DQ25	DQ24
Feature	Revision Identification				Manufacturers Vendor Code			

Bit	15	14	13	12	11	10	9	8
MF=0	DQ23	DQ22	DQ21	DQ20	DQ19	DQ18	DQ17	DQ16
MF=1	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Feature	RFU				FIFO Depth		Density	

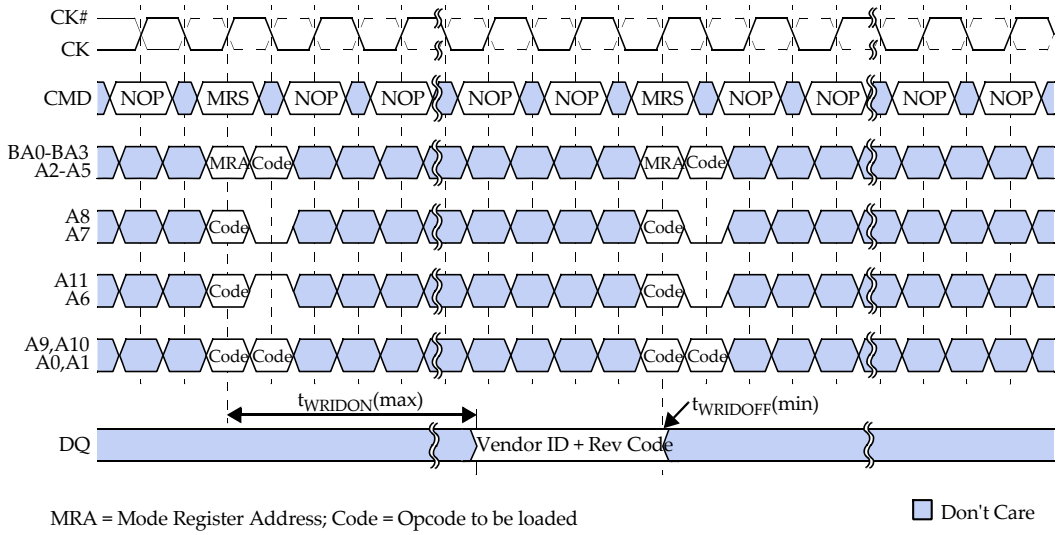


Figure 5: Vendor ID Timing Diagram

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2. ADDRESS

2.1. ADDRESSING

GDDR5 SGRAMs use a double data rate address scheme to reduce pins required on the GDDR5 SGRAM as shown in Table 5. The addresses should be provided to the GDDR5 SGRAM in two parts; the first half is latched on the rising edge of CK along with the command pins such as RAS#, CAS# and WE#; the second half is latched on the next rising edge of CK#.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 5 Address Pairs

Clock									
Rising CK	BA3	BA2	BA1	BA0	(A12)	A11	A10	A9	A8
Rising CK#	A3	A4	A5	A2	(RFU)	A6	A0	A1	A7

Note: Address pin A12 is required only for 2G density.

GDDR5 addressing includes support for 1G density. For all densities two modes are supported (x32 mode or x16 mode). x32 and x16 modes differ only in the number of valid column addresses, as shown in Table6.

Table 6 Addressing Scheme

	1G	
	x32 mode	**x16 mode**
Row address	A0~A11	A0~A11
Column address	A0~A5	A0~A6
Bank address	BA0~BA3	BA0~BA3
Autoprecharge	A8	A8
Page Size	2K	2K
Refresh	8K/32ms	8K/32ms
Refresh period	3.9us	3.9us

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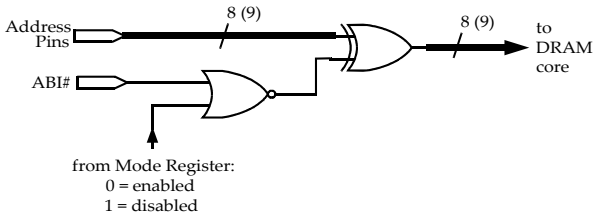
2.2. ADDRESS BUS INVERSION (ABI)

Address Bus Inversion (ABI) reduces the power requirements on address pins, as the no. of address lines driving a low level can be limited to 4 (in case A12/RFU is not wired) or 5 (in case A12/RFU is wired).

The Address Bus Inversion function is associated with the electrical signalling on the address lines between a controller and the GDDR5 SGRAM, regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a data mask, or any other pattern.

The ABI# input is an active Low double data rate (DDR) signal and sampled by the GDDR5 SGRAM at the rising edge of CK and the rising edge of CK# along with the address inputs.

Once enabled by the corresponding ABI Mode Register bit, the GDDR5 SGRAM will invert the pattern received on the address inputs in case ABI# was sampled Low, or leave the pattern non-inverted in case ABI# was sampled High, as shown in Figure 6.



Note: bus width is 8 when A12/RFU pin is not present, and 9 when A12/RFU pin is present

Figure 6: Example of Address Bus Inversion Logic

The flow diagram in Figure 7 illustrates the ABI operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The GDDR5 SGRAM has to perform the reverse operation based on the level of the ABI# pin. Address input timing parameters are only valid with ABI being enabled and a maximum of 4 address inputs driven Low.

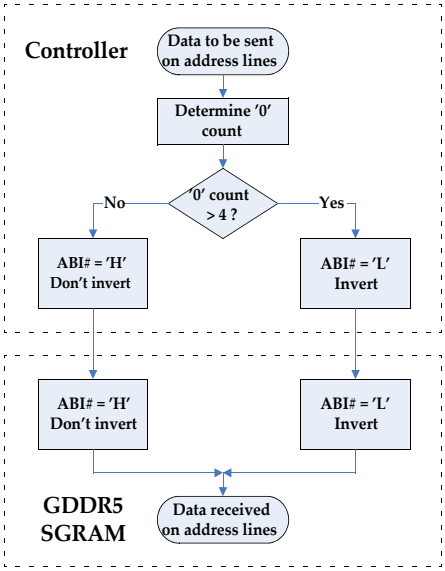


Figure 7: Address Bus Inversion (ABI) Flow Diagram

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2.3. BANK GROUPS

For GDDR5 SGRAM devices operating at frequencies above a certain threshold, the activity within a bank group must be restricted to ensure proper operation of the device. The 8 or 16 banks in GDDR5 SGRAMs are divided into four bank groups. The bank groups feature is controlled by bits A10 and A11 in Mode Register 3 (MR3). The assignment of the banks to the bank groups is shown in Table 7.

Table 7 Bank Groups

Bank	Addressing				1G
	BA3	BA2	BA1	BA0	16 banks
0	0	0	0	0	Group A
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	Group B
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	Group C
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	Group D
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 8.

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Table 8 Command Sequences Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter			Notes
	Bank Groups Disabled	Bank Groups Enabled		
		Accesses to different bank groups	Accesses within the same bank group	
ACTIVE to ACTIVE	t_{RRDS}	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS}	t_{CCDS}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	t_{RTPS}	1 tck	t_{RTPL}	1

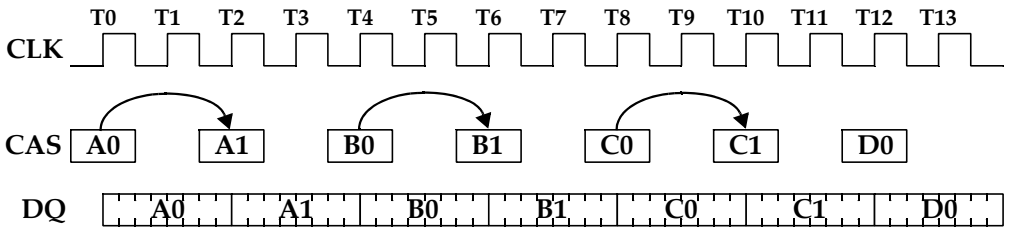
Note.1 : Parameters tRTPS and tRTPL apply only when READ and PRECHARGE go to the same bank; use tRTPS when BG are disabled, and tRTPL when BG are enabled.

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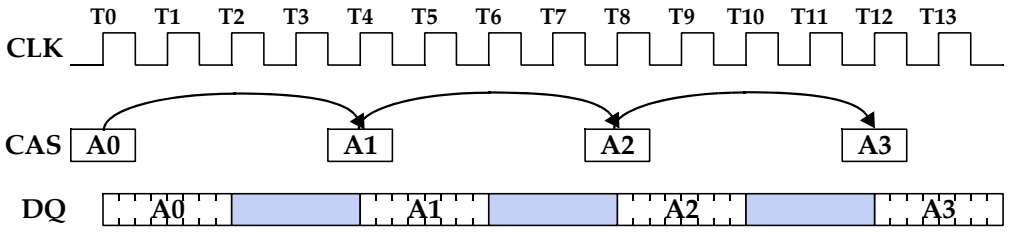
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Back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

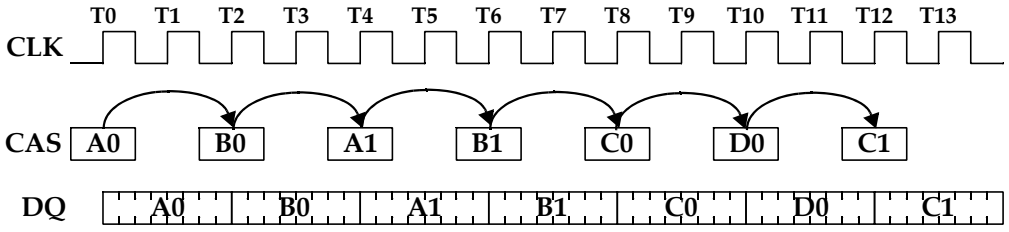
Example 1 (Bank Groups disabled): $t_{CCDS} = 2 * t_{CK}$



Example 2: (Bank Groups enabled): $t_{CCDL} = 4 * t_{CK}$



Example 3: (Bank Groups enabled): $t_{CCDS} = 2 * t_{CK}$



Notes:
1) Column accesses are to open banks, and t_{RCD} has been met.
2) CL = 0 assumed
3) Ax, Bx, Cx, Dx: accesses to bank groups A, B, C or D, respectively
4) With bank groups enabled, t_{CCDL} is $3t_{CK}$, as programmed in MR3.

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3. TRAINING

3.1. INTERFACE TRAINING SEQUENCE

Due to the high data rates of GDDR5, it is recommended that the interfaces be trained to operate with the optimal timings. GDDR5 SGRAM has features defined which allow for complete and efficient training of the I/O interface without the use of the GDDR5 SGRAM array. The interface trainings are required for normal DRAM functionality unless running in lower frequency modes as described in the low frequency section. Interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences has been chosen based on the following criteria:

The address training must be done first to allow full access to the Mode Registers. (MRS for address training is a special single data rate mode register set guaranteed to work without training). Address input timing shall function without training as long as $t_{AS/H}$ are met at the GDDR5 SGRAM.

WCK2CK training should be done before read training because a shift in WCK relative CK will cause a shift in all READ timings relative to CK.

READ training should be done before WRITE training because optimal WRITE training depends on correct READ data.

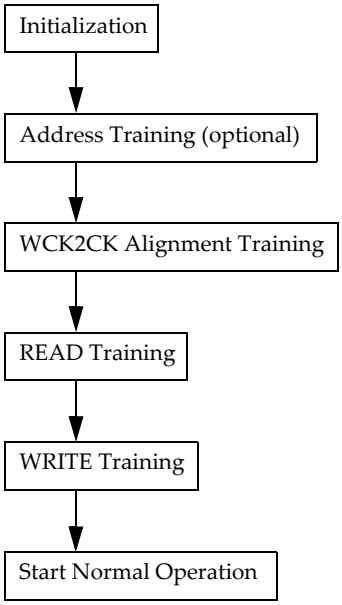


Figure 8: Interface Training Sequence

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3.2. ADDRESS TRAINING

The GDDR5 SGRAM provides means for address bus interface training. The controller may use the address training mode to improve the timing margins on the address bus.

Address training mode is entered and exited via the ADT bit in Mode Register 15 (MR15). Mode Register 15 supports the same setup and hold times on the address pins as for commands to allow a safe entry into address training mode.

Address training mode uses an internal bridge between the GDDR5 SGRAM's address inputs and DQ/DBI# outputs. It also uses a special READ command for address capture that is encoded using the SDR command pins only (CS#,RAS#,CAS#,WE# = L,H,L,H). The address values normally used to encode the commands will not be interpreted. Once the address training mode has been entered, the address values registered coincident with this special READ command will be transmitted to the controller on the DQ/DBI# pins. The controller is then expected to compare the address pattern received to the expected value and to adjust the address transmit timing accordingly. The procedure may be repeated using different address pattern and interface timings.

No WCK clock is required for this special READ command operation during address training mode. The latched addresses are driven out asynchronously.

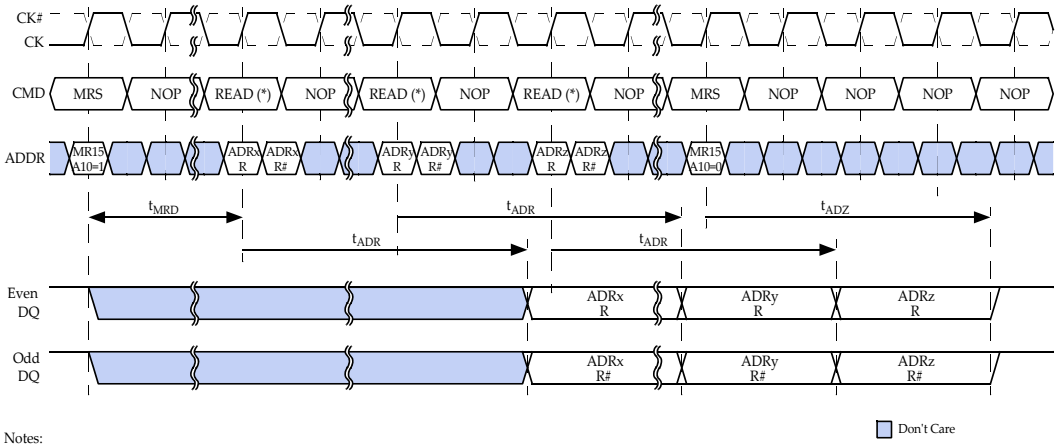
The only commands allowed during address training mode are this special READ, MRS (e.g. to exit address training mode) and NOP / DESELECT.

When enabled by the ABI bit in Mode Register 1, address bus inversion (ABI) is effective during address training mode. It is suggested to train the ABI# pin's interface timing together with the other address lines.

The timing diagram in Figure 9 illustrates the typical command sequence in address training mode. The DQ/DBI# output drivers are enabled as long as the ADT bit is set. The minimum spacing between consecutive special READ commands is 2 t_{CK}.

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Notes:
1) READ command encoding: CS# = L, RAS# = H, CAS# = L, WE# = H
2) ADRxR = 1st half of address x, sampled on rising edge of CK;
ADRxR# = 2nd half of address x, sampled on rising edge of CK#
3) Addresses sampled on rising edge of CK are returned on even DQ after tADR;
addresses sampled on rising edge of CK# are returned on odd DQ simultaneously with even DQ
4) DQs are enabled when ADT bit in Mode Register 15 set to 1 (Enter Address Training Mode)
DQs are disabled after t_{ADZ} when ADT bit in Mode Register 15 set to 0 (Exit Address Training Mode)

Figure 9: Address Training Timing

Table 9 AC timings in Address Training Mode

Parameter	Symbol	Min	Max	Unit
READ command to data out delay	t_{ADR}	0.5*tCK+0	0.5*tCK+10	ns
ADT off to DQ/DBI# in ODT state delay	t_{ADZ}	--	0.5*tCK+10	ns

Table 10 defines the correspondence between address bits and DQ/DBI#. Devices configured to x16 mode reflect the address on the two bytes being enabled in that mode, which are bytes 0 and 2 for MF=0 and bytes 1 and 3 for MF=1 configurations. Devices configured to x32 mode reflect the address on the same DQ as in x16 mode; in addition they are allowed but not required to reflect the address on those bytes that are disabled in x16 mode, thus reflecting each address twice.

Devices not supporting an A12/RFU pin shall drive a logic High on the DBI# pins.

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Table 10 Address to DQ Mapping in Address Training Mode

Output	Address bits registered at rising edge of CK								
	A12	**A8**	**A11**	**BA1**	**BA2**	**BA3**	**BA0**	**A9**	**A10**
DQ	DBI0#	DQ22	DQ20	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0
	DBI1#	DQ30	DQ28	DQ26	DQ24	DQ14	DQ12	DQ10	DQ8
Output	**Address bits registered at rising edge of CK#**								
	RFU	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
DQ	DBI2#	DQ23	DQ21	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1
	DBI3#	DQ31	DQ29	DQ27	DQ25	DQ15	DQ13	DQ11	DQ9

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3.3. WCK2CK TRAINING

The purpose of WCK2CK training is to align the data WCK clock with the command CK clock to aid in the GDDR5 SGRAM's internal data synchronization between the logic clocked by CK/CK# and WCK/WCK#. This will help to define both Read and Write latencies between the GDDR5 SGRAM and memory controller. WCK2CK training mode is controlled via MRS.

Before starting WCK2CK training, the following conditions must be met:

- CK/CK# clock is stable and toggling
- The timing of all address and command pins must be guaranteed
- PLL on/off(MR1 bit A7) and PLL delay compensation enable(MR7 bit A2) are set to desired mode before WCK to CK training is started
- The desired WCK2CK alignment point (MR6, bit A0) is selected
- The EDC hold pattern (MR4, bits A0-A3) must be programmed to '1111'
- 2 Mode Register bits for internal WCK01 and WCK23 inversion (MR3, bits A2-A3) must be set to a known state
- All banks are idle and no other command execution is in progress

WCK2CK training must be done after any of the following conditions:

- Device initialization
- Any CLmrs, WLmrs, CRCRL or CRCWL latency change
- CK and WCK frequency changes
- PLL on/off(MR1 bit A7) and PLL delay compensation mode(MR7 bit A2) changes
- Change of the WCK2CK alignment point (MR6, bit A0)
- WCK state change from off to toggling, including self refresh exit or exit from power-down when bit A1 (LP2) in MR5 is set

Figure 10 and Figure 11 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting bit A4 in MR3. This will initiate the WCK divide-by-2 circuits associated with WCK01 and WCK23 clocks in the GDDR5 SGRAM. In case the divide-by-2 circuits are at opposite output phases, which is indicated by opposite "early/late" phases on the EDC pins associated with WCK01 and WCK23 (see below), they may be put in phase by using the WCK01 and WCK23 inversion bits. Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in <Link>Figure 11. The challenge of this method is to restart the WCK clocks in a way that even their first clock edges meet the WCK clock input specification. Otherwise, divide-by-2 circuits for both WCK01 and WCK23 might again have opposite phase alignment.

Figure 12 illustrates how the WCK phase information is derived. The phase detectors (PD) sample the internally divided-by-2 WCK clocks. Only one sample point is shown in the figure for clarity. In reality, when WCK2CK training mode is enabled, a sample will occur every t_{CK} and will be translated to the EDC pins accordingly. If the divided-by-2 WCK clock arrives early, then the EDC pin outputs the EDC hold pattern during the time interval specified in Figure 12. If the divided-by-2 WCK clock arrives late, then the EDC pin outputs the inverted EDC hold pattern during the time interval specified in Figure 12. This is shown in Table 11.

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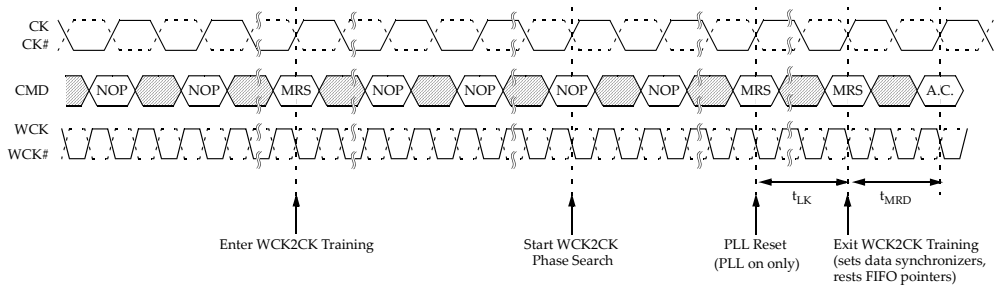


Figure 10: Example WCK2CK Training Sequence

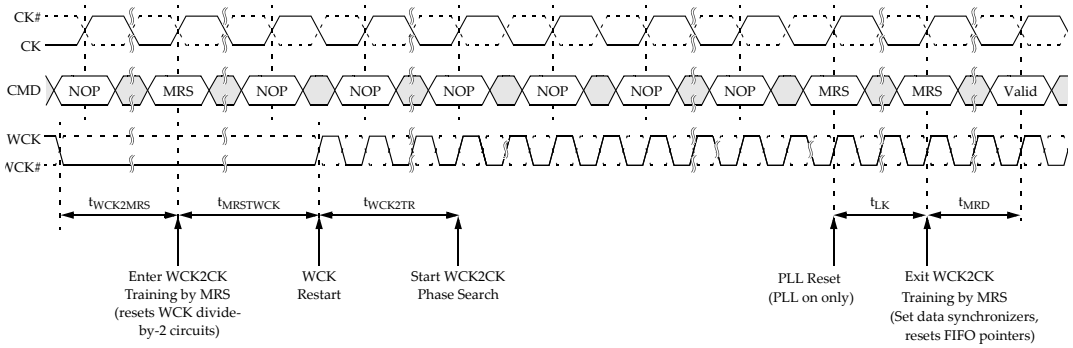


Figure 11: Example WCK2CK Training Sequence with WCK Stopping

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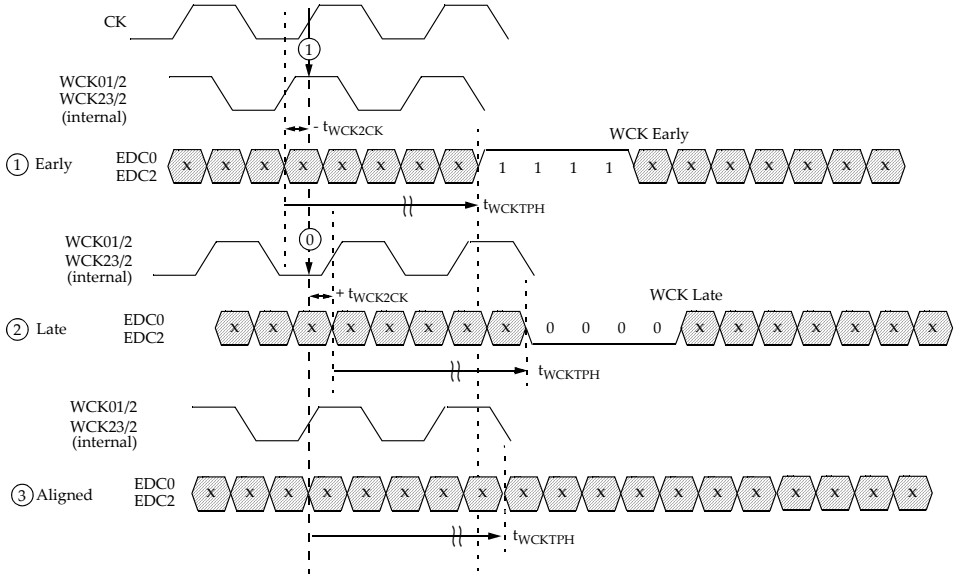


Figure 12: EDC pin Behaviour for WCK2CK Training (assumes '1111' as EDC Hold Pattern)

Table 11 Phase Detector and EDC Pin behavior

WCK/2 value sampled by CK	WCK2CK Phase	Data on EDC Pin	Action
'1'	'Early'	EDC hold ('1111')	Increase Delay on WCK
'0'	'Late'	Inverted EDC Hold ('0000')	Decrease Delay on WCK

The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$; the value(s) vary with the PLL mode (on or off) and the selected alignment point.

If enabled, the PLL shall not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL. It is required to perform a PLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL is in lock such that the GDDR5 SGRAM data synchronizers are set upon WCK2CK training exit.

WCK2CK training is exited via MRS by resetting bit A4 in MR3. For proper reset of the data synchronizers it is required that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ at the time of the WCK2CK training exit.

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After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK} (e.g. due to voltage and temperature variation). Once this WCK phase drift exceeds t_{WCK2CK}(min) or t_{WCK2CK}(max), it is required to repeat the WCK2CK training and realign the clocks.

WCK2CK alignment at PIN Mode

The WCK and CK phase alignment point can be changed via MRS by setting bit A0 in MR6. In normal mode, when MR6 A0 is set to '0', the phases of CK and WCK are aligned at CK pins and the end of WCK tree as shown in Figure 13. On the other hand, when MR6 A0 is set to '1', the phases of CK and WCK are aligned at the pin as shown in Figure 14. PIN mode is supported up to the max CK clock frequency of f_{CKPIN}, and is an option to reduce the time of WCK2CK training at low frequency.

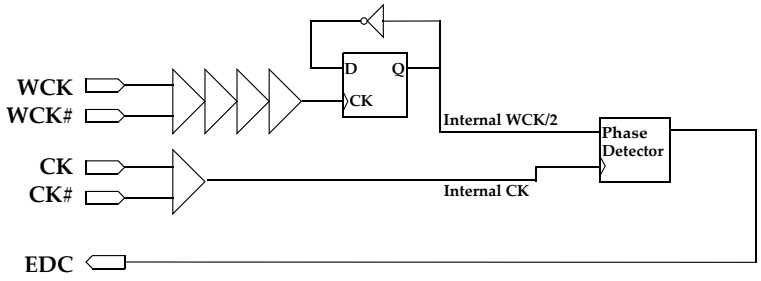


Figure 13: Normal Mode

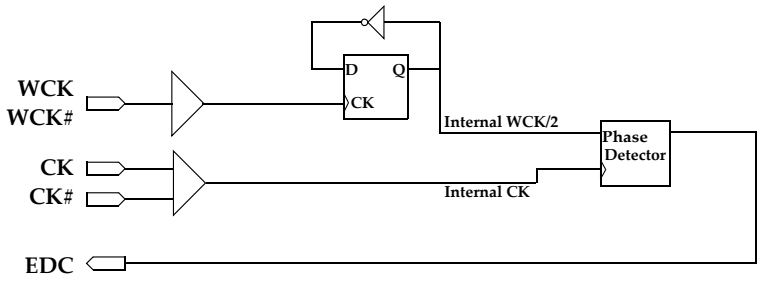


Figure 14: Pin Mode

WCK2CK Auto Synchronization

GDDR5 SGRAMs support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit. This mode is controlled by the autosync bit (MR7, bit A4), and is effective when the LP2 bit (MR5, bit A1) is set and the WCK clocks are stopped during power-down.

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Also, this mode works for both normal and PIN mode. When WCK2CK automatic synchronization mode is enabled, a full WCK2CK training including Phase search is not required after power-down exit, although WCK2CK MRS must be issued momentarily for setting the data synchronizers. However, WCK and CK clocks must meet the $t_{WCK2CKSYNC}$ specification upon power-down exit. Any allowed command may be issued after t_{XPN} or after t_{LK} in case the PLL had been enabled upon power-down entry. The PLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to lower operating frequencies up to $f_{CKAUTOSYNC}$ as described in the datasheets.

Table 12 describes WCK2CK training methods for different frequency ranges. Each Frequency range is vendor specific. Normal and PIN mode of WCK2CK training are described in Table 12. Each frequency range is DRAM vendor specific. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stopping, or WCK2CK auto-sync. If the user wants to use WCK2CK stop for divider initialization instead of WCK2CK auto-sync, the user must not set the WCK2CK auto-sync. Low frequency, the combined use of PIN and WCK2CK auto-sync modes can minimize WCK2CK training time.

Table 12 WCK2CK training simplified for Normal mode and PIN mode

	High Frequency		Low Frequency	
Frequency	≥ 2Gbps		< 2Gbps	
WCK2CK alignment mode	**Normal**	**PIN**	**Normal**	**PIN**
Phase Search	Required	Required	No*	No*

* Note: The divided WCK/WCK# should be aligned CK/CK# by WCK2CK Auto Synchronization or WCK stop mode

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:

1) Enable training mode via MRS and wait t_{MRD}
2) Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phase use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits
3) Adjust the WCK phase independently for WCK01 and WCK23 to the optimal point ("ideal alignment")
4) Issue a PLL reset and wait for t_{LK} (PLL on mode only)
5) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
6) Wait t_{MRD} for the reset of data synchronizers

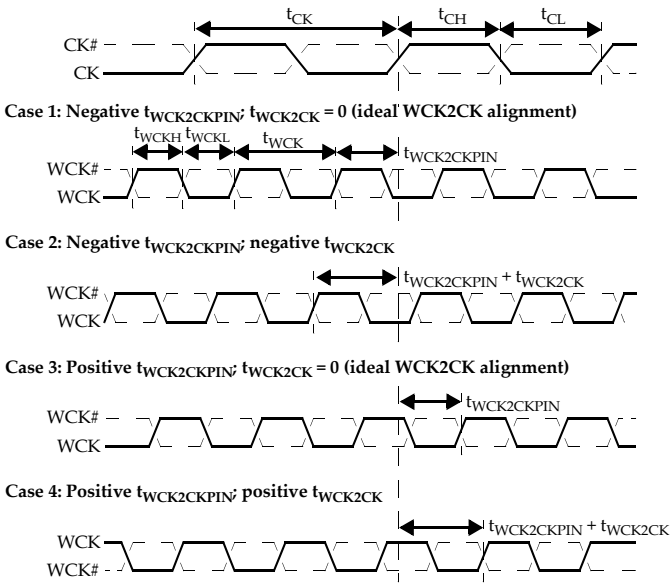
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Example 2: outline of a basic WCK2CK training sequence with optional WCK clock stop:

1) Stop WCK clocks with WCK01/WCK23 LOW and WCK01#/WCK23# HIGH
2) Wait $t_{WCK2MRS}$ for internal WCK clocks to settle
3) Enable training mode via MRS and wait t_{MRD} for divide-by-2 circuits to reset
4) Start WCK clocks without glitches (both divide-by-2 circuits remain in sync)
5) Wait t_{WCK2TR} for internal WCK clocks to stabilize
6) Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; adjust the WCK phase to the optimal point ("ideal alignment")
7) Issue a PLL reset and wait t_{LK} (PLL on mode only)
8) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
9) Wait t_{MRD} for the reset of data synchronizers

READ and WRITE latency timings are defined relative to CK. Any offset in WCK and CK at the pins and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 6. For more details on the impact on READ and WRITE timings see the OPERATIONS section.



Note: $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 15: WCK2CK Timings

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GDDR5 WCK2CK Training in x16 mode

For configurations with WCK clocks not shared between two GDDR5 SGRAMs it is suggested to set the WCK phase to the ideal alignment point. However, for configurations where two GDDR5 SGRAMs (x16) share their WCK clocks as in a x16 clamshell, an offset given by the midpoint of both DRAM's ideal WCK positions may be required. The maximum allowed offset in this case is specified by parameter $t_{WCK2CKSYNC}$: it defines the WCK offset range from the ideal alignment which still guarantees a GDDR5 SGRAM device to internally synchronize its WCK and CK clocks upon training exit.

Example: outline of training sequence for x32 and x16 configurations with 2 GDDR5 SGRAMs sharing their WCK clocks (e.g. clamshell):

1) Enable training mode for both DRAMs via MRS and wait t_{MRD}
2) For both DRAMs sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phases use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits; in case of shared CS# signals use MREMF0 and MREMF1 bits in MR15 to explicitly direct the MRS command for this phase flipping to either DRAM1 or DRAM2 ("soft chip select");
3) Sweep and observe the phase on DRAM1 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
4) Sweep and observe the phase on DRAM2 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
5) Sweep WCK01 and WCK23 phase to midpoint of DRAM1 and DRAM2 optimal settings
6) Issue a PLL reset and wait for t_{LK} (PLL on mode only)
7) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
8) Wait t_{MRD} for the reset of data synchronizers

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3.4. READ TRAINING

Read training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed output of the GDDR5 SGRAM. Each pin (DQ0-DQ31, DBI0#-DBI3#, EDC0-EDC3) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include the DBI# pins. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC pins.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 16 shows an example of the internal data paths used with LDFF and RDTR. Table 13 lists AC timing parameters associated with Read Training.

Table 13 LDFF and RDTR TIMINGS

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to LDFF command delay	t_{RCDLTR}	10	–	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}	10	–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}	10	–	ns	
RDTR to RDTR command delay	t_{CCDS}	2	–	t_{CK}	
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF(111) to LDFF command cycle time	t_{LTL7TR}	4	–	t_{CK}	a
LDFF(111) to RDTR command delay	t_{LTRTR}	4	–	t_{CK}	
READ or RDTR to LDFF command delay	t_{RDTLT}	4	–	t_{CK}	

a. The min. value does not exceed 8 t_{CK}.

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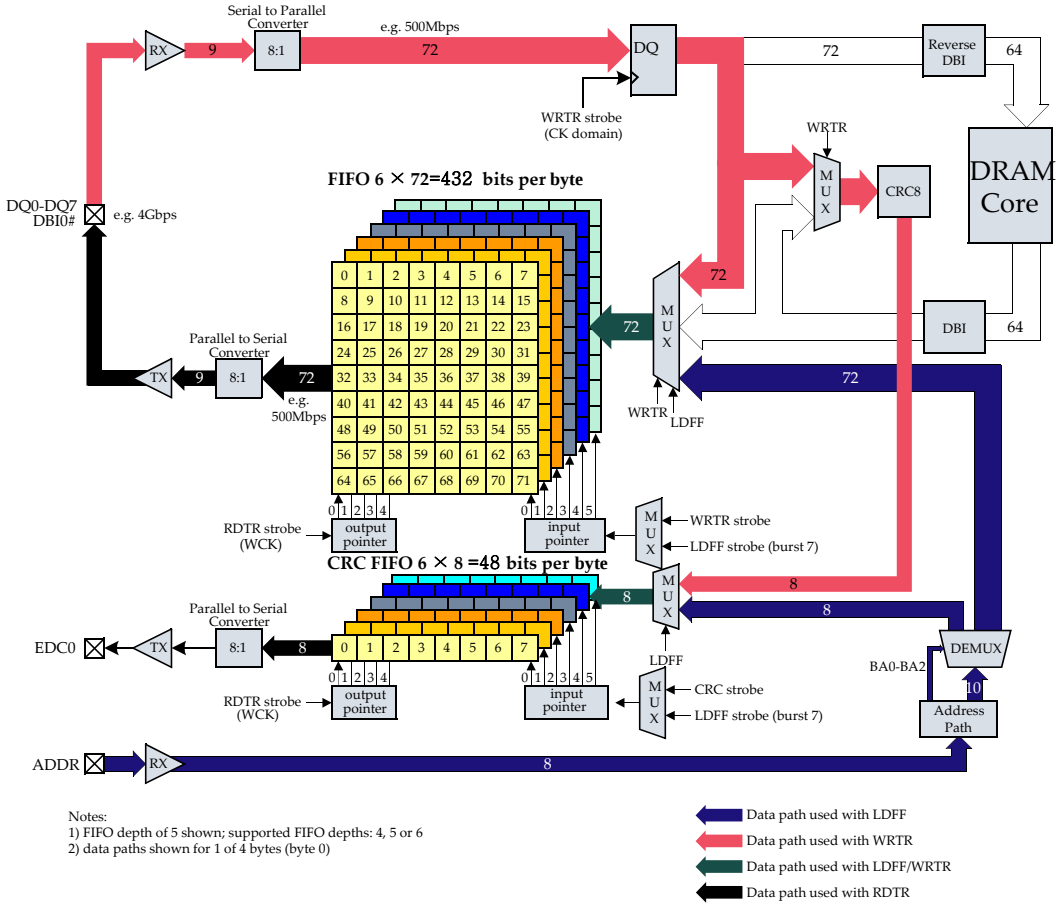


Figure 16: Data Paths used for Read and Write Training

LDFF Command

The LDFF command (Figure 17) is used to securely load data to the GDDR5 SGRAM Read FIFOs via the address bus. Depending on the GDDR5 SGRAM READ FIFO depth nFIFO 6, any bit pattern of length 32-48 can be loaded uniquely to every DQ, DBI# and EDC pin within a byte. The FIFO depth is fixed by design and can be read via the Vendor ID function.

Eight LDFF commands are required to fill one FIFO stage; each LDFF command loads one burst position, and the bank addresses BA0-BA2 select the burst position from 0 to 7.

The data pattern is conveyed on address pins A0-A7 for DQ0-DQ7, A9 for DBI0#, and BA3 for EDC0; the data are internally replicated to all 4 bytes, as shown in Figure 18.

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LDFF loads the DBI FIFO regardless of the WDBI and RDBI Mode Register bits. It also loads the EDC FIFO regardless of the WRCRC and RDCRC Mode Register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command.

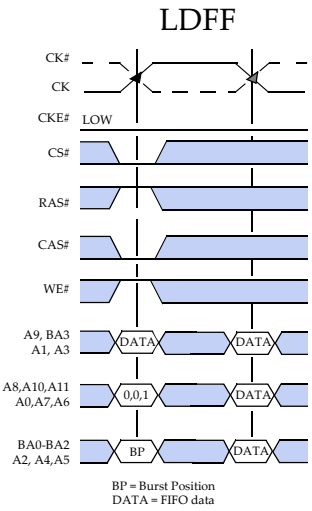


Figure 17: LDFF Command

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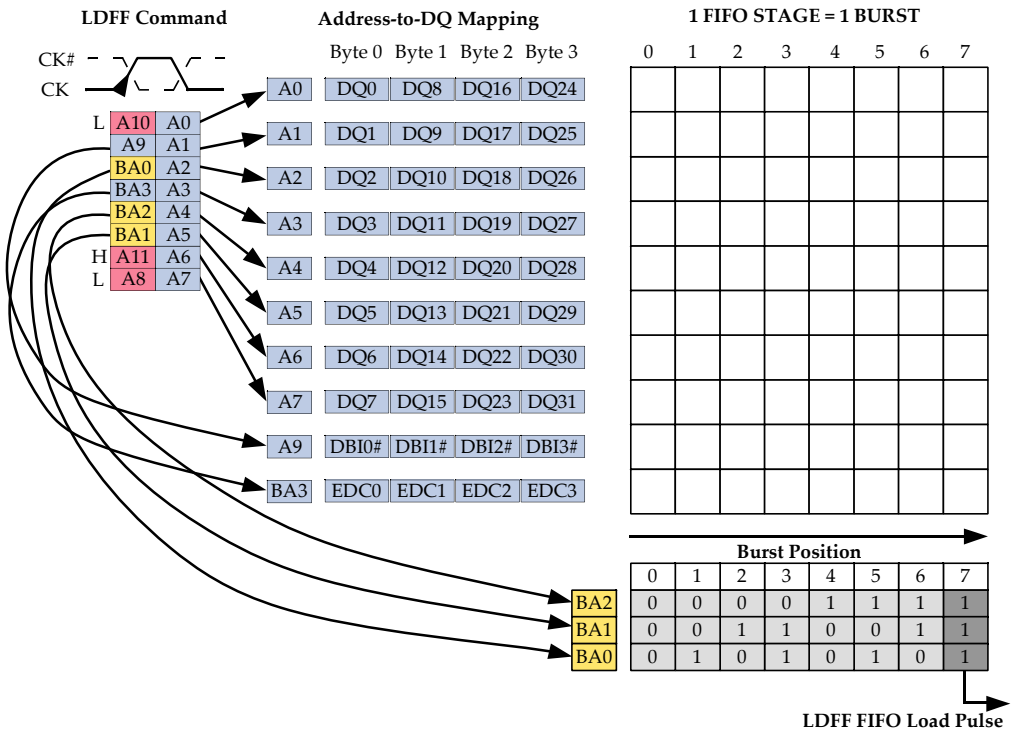


Figure 18: LDFF Command Address to DQ/DBI#/EDC Mapping

All burst addresses 0 to 7 must be loaded; LDFF commands to burst address 0 to 6 may be issued in random order; the LDFF command to burst address 7 (LDFF7) must be the last of 8 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least t_{LTLTR}, and at least t_{LTL7TR} cycles are required after each LDFF command to burst address 7.

LDFF pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFF commands to burst address 7 (with identical data pattern). The data pattern in the scratch memory for LDFF will be available until the first RDTR command.

The DQ/DBI# output buffers remain in ODT state during LDFF.

An amount of LDFF commands to burst address 7 greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

The total number of LDFF commands to burst address 7 modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

The EDC hold pattern is driven on the EDC pins during LDFF (provided RDQS mode is not enabled).

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RDTR Command

A RDTR burst is initiated with a RDTR command as shown in Figure 19. No bank or column addresses are used as the data is read from the internal READ FIFO, not the array. The length of the burst initiated with a RDTR command is eight. There is no interruption nor truncation of RDTR bursts.

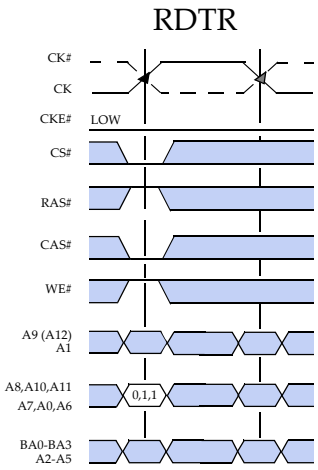


Figure 19: RDTR Command

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. If not set, the DBI# pins will remain in ODT state, and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. The DBI# pin behaves like a DQ, and no encoding with DBI is performed.

An amount of RDTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data output. The FIFO depth from which the RDTR data is read must be a number between 4-6 and must be specified by the DRAM vendor. The FIFO depth is read via the Vendor ID function.

During RDTR bursts, the first valid data-out element will be available after the CAS latency (CL). The latency is the same as for READ. The data on the EDC pins comes with additional CRC latency (t_{CRCRD}) after the CL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQ and DBI# pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

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Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the t_{CCDS} timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time t_{RTW} is met.

The total number of RDTR commands modulo FIFO depth must be equal to total number of WRTR commands modulo FIFO depth when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.

The total number of RDTR commands modulo FIFO depth must be equal to the total number of LDFF commands to burst position 7 modulo FIFO depth when used in conjunction with LDFF. No READ or WRITE commands are allowed between LDFF and RDTR.

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3.5. WRITE TRAINING

Write training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed input of the GDDR5 SGRAM. Each pin (DQ0-DQ31, DBI0#-DBI3#) can be individually trained during this sequence.

For Write Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- the PLL must be locked, if enabled.
- WCK2CK training should be complete
- Read training should be complete
- RDBI and WDBI must be enabled prior to and during Write Training if the training shall include the DBI# pins. RDCRC and WRCRC must be enabled prior to and during Write Training if the training shall include the EDC pins.

The following commands are associated with Write Training:

- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory core. No MRS is required to enter Write Training.

Figure 16 shows an example of the internal data paths used with WRTR and RDTR. Figure 21 shows a typical Write training command sequence using WRTR and RDTR. Table 14 lists AC timing parameters associated with WRITE Training.

Table 14 WRTR and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to WRTR command delay	t_{RCDWTR}	10	–	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}	10	–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}	10	–	ns	
RD/WR bank A to RD/WR bank B command delay different bank groups	t_{CCDS}	2	–	t_{CK}	a
WRTR to RDTR command delay	t_{WTRTR}	WL-tWLmin	–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}	WL+CRCWL+2	–	t_{CK}	
READ or RDTR to WRITE or WRTR command delay	t_{RTW}	1	–	ns	b

a. t_{CCDS} is either for gapless consecutive READ or RDTR (any combination), gapless consecutive WRITE, or gapless consecutive WRTR commands.

b. t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.

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WRTR Command

A WRTR burst is initiated with a WRTR command as shown in Figure 20. No bank or column addresses are used as the data is written to the internal READ FIFO, not the array. The length of the burst initiated with a WRTR command is eight. There is no interruption nor truncation of WRTR bursts.

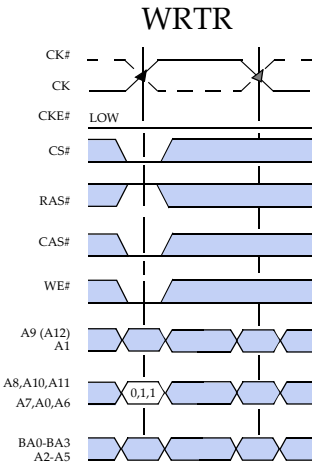


Figure 20: WRTR Command

A WRTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

WDBI and WRCRC must be enabled to write the DBI and EDC bits, respectively, with the WRTR command. If WDBI is not set, a '1' will be written to the DBI FIFO, and a '1' will be assumed for the DBI# input in the CRC calculation. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

An amount of WRTR commands equal to the FIFO depth is required to fully load the FIFO; any number of WRTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input. The FIFO depth to which the WRTR data is written must be 6. The FIFO depth is read via the Vendor ID function.

During WRTR bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is the same as for WRITE.

Upon completion of a burst, assuming no other WRTR data is expected on the bus the GDDR5 SGRAM DQ and DBI# pins will be driven according to the ODT state. Any additional input data will be ignored.

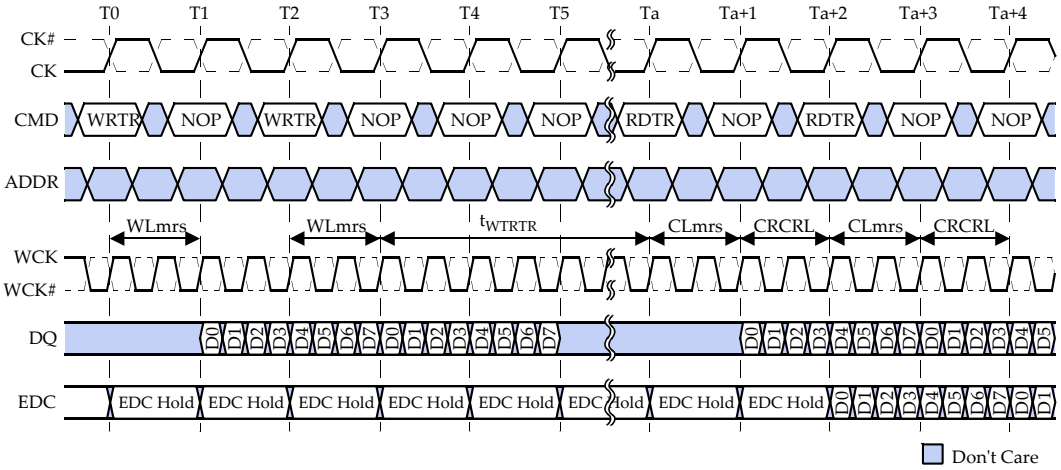
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Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the t_{CCDS} timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time t_{RTWTR} is met.

The total number of WRTR commands modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.



1. WLmrs, CLmrs and CRCRL set to 1 for ease of illustration; check Mode Register definition for supported settings
2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

Figure 21: Write Training using WRTR and RDTR Commands

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4. MODE REGISTERS

GDDR5 specifies 10 Mode Registers to define the specific mode of operation. MR0 to MR7 and MR15 are defined as shown in the overview in Figure 22. MR8 to MR13 are not defined and may be used by DRAM vendors for vendor specific features. Reprogramming the Mode Registers will not alter the contents of the memory array.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed or the device loses power. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values e.g. upon power-up.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0. Bit A12 is not used for any mode register programming as this address input is not defined for 1G density.

	BA3	BA2	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0	0	Write Recovery (WR)				TM	CAS Latency (CLmrs)				Write Latency (WLmrs)		
MR1	0	0	0	1	0	PLL Reset	ABI	WDBI	RDBI	PLL	Cal Upd	ADR/CMD Termination		Data Termination		Driver Strength	
MR2	0	0	1	0	0	ADR/CMD Termination Offset			Data and WCK Termination Offset			OCD Pullup Driver Offset			OCD Pulldown Driver Offset		
MR3	0	0	1	1	0	Bank Groups		WCK Termination		Info		RDQS Mode	WCK 2CK	WCK 23Inv	WCK 01Inv	Self Refresh	
MR4	0	1	0	0	0	EDC 13Inv	WR CRC	RD CRC	CRC Read Latency (CRCRL)		CRC Write Latency (CRCWL)			EDC Hold Pattern			
MR5	0	1	0	1	0	RFU						PLL Bandwidth (PLLBW)		LP3	LP2	RFU	
MR6	0	1	1	0	0	VREFD Offset Upper 2 bytes				VREFD Offset Lower 2 bytes			VREFD	Auto VREFD	VREFD Merge	WCK PIN	
MR7	0	1	1	1	0	DCC		RFU		Half VREFD	Temp Sense	DQ PreA	Auto Sync	LF Mode	RFU		
MR14	RFU																
MR15	1	1	1	1	0	RFU	ADT	MRE MF1	MRE MF0	X	X	X	X	X	X	X	X

Figure 22. Mode Registers Overview

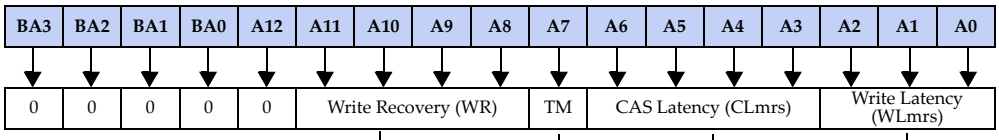
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4.1. MODE REGISTER 0 (MR0)

Mode Register 0 controls operating modes such as Write Latency, CAS latency, Write Recovery and Test Mode as shown in Figure 23.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=0.



A11	A10	A9	A8	Write Recovery (WR)
0	0	0	0	4
0	0	0	1	5
0	0	1	0	6
0	0	1	1	7
0	1	0	0	8
0	1	0	1	9
0	1	1	0	10
0	1	1	1	11
1	0	0	0	12
1	0	0	1	13
1	0	1	0	14
1	0	1	1	15
1	1	0	0	16
1	1	0	1	17
1	1	1	0	18
1	1	1	1	19

A7	Test Mode
0	Normal
1	Test Mode

A2	A1	A0	Write Latency (WLmrs)
0	0	0	RFU
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

A6	A5	A4	A3	CAS Latency (CLmrs)
0	0	0	0	5
0	0	0	1	6
0	0	1	0	7
0	0	1	1	8
0	1	0	0	9
0	1	0	1	10
0	1	1	0	11
0	1	1	1	12
1	0	0	0	13
1	0	0	1	14
1	0	1	0	15
1	0	1	1	16
1	1	0	0	17
1	1	0	1	18
1	1	1	0	19
1	1	1	1	20

Figure 23. Mode Register 0 (MR0) Definition

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WRITE Latency (WLmrs)

The WRITE latency (WLmrs) is the delay in clock cycles used in the calculation of the total WRITE latency (WL) between the registration of a WRITE command and the availability of the first piece of input data. DRAM vendor specifications should be checked for value(s) of WLmrs supported. The full WRITE latency definition can be found in the section entitled OPERATION.

When the WRITE latencies are set to small values (i.e. 1,2,... clocks), the input receivers never turn off, in turn, raising the operating power. When the WRITE latency is set to higher values (i.e. .. 6, 7 clocks) the input receivers turn on when the WRITE command is registered. Refer to vendor datasheets for value(s) of WLmrs where the input receivers are always on or only turn on when the WRITE command is registered

Speed	Allowable Operating Frequency (Gbps)						
	WL7	WL6	WL5	WL4	WL3	WL2	WL1
6.0Gbps							
5.5Gbps							
5.0Gbps							
4.5Gbps							
4.0Gbps							

CAS Latency (CLmrs)

The CAS latency (CLmrs) is the delay in clock cycles used in the calculation of the total READ latency (CL) between the registration of a READ command and the availability of the first piece of output data.

By default CLmrs is specified by bits A3-A6, defining a CLmrs range of 5 to 20 tCK.

DRAM vendor specifications should be checked for value(s) of CLmrs supported. The full READ latency definition can be found in the section entitled OPERATION

Speed	RDBI ON/OFF	Allowable Operating Frequency (Gbps)								
		CL20	CL19	CL18	CL17	CL16	CL15	CL14	CL13	CL12
6.0Gbps	OFF									
	ON									
5.5Gbps	OFF									
	ON									
5.0Gbps	OFF									
	ON									
4.5Gbps	OFF									
	ON									
4.0Gbps	OFF									
	ON									

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WRITE Recovery (WR)

The programmed WR value is used for the auto precharge feature along with t_{RP} to determine t_{DAL}. The WR register bits are not a required function and may be implemented at the discretion of the DRAM manufacturer.

WR must be programmed with a value greater than or equal to RU{t_{WR}/t_{CK}}, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time.

By default WR is specified by bits A8-A11, defining a WR range of 4 to 19 tCK.

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to '0', and bits A0-A6 and A8-A11 set to the desired values. Programming bit A7 to '1' places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

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4.2. MODE REGISTER 1 (MR1)

Mode Register 1 controls functions like drive strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL as shown in Figure 24.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=0 and BA3=0. Bits A0-A1, A4-A6 and A10 of this register are initialized with'0's.

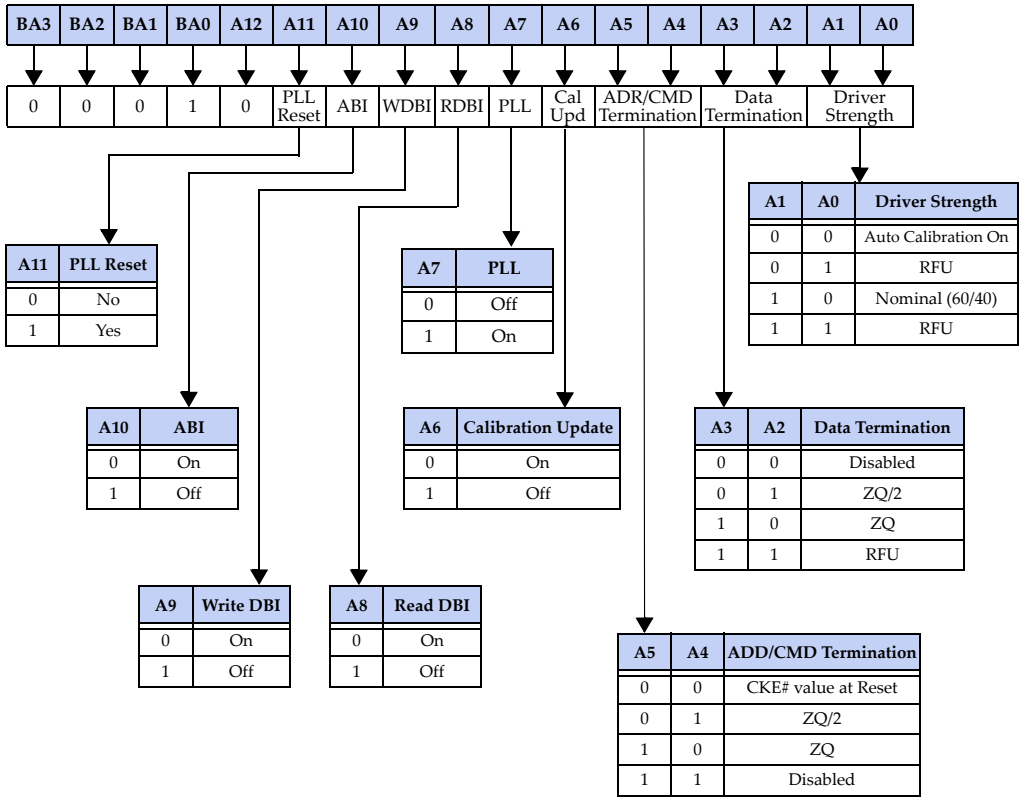


Figure 24. Mode Register 1 (MR1) Definition

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5 SGRAMs offer autocalibrating impedance output buffers and on-die terminations. This enables a user to match the driver impedance and terminations to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and V_{SSQ}. A nominal resistor

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value of 120 Ohms is equivalent to the 40 Ohms Pulldown and 60 Ohms Pullup nominal impedances of GDDR5 SGRAMs. RESET#, CK and CK# are not internally terminated. CK and CK# shall be terminated on the system using external 1% resistors to V_{DDQ}.

The output driver and on-die termination impedances are updated during all REFRESH commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

Driver Strength

Bits A0 and A1 define the driver strength. The Auto Calibration setting enables the Auto-Calibration functionality for the Pulldown, Pullup and Termination over process, temperature and voltage changes. The design target for the factory setting is 40 Ohm Pulldown, 60 Ohm Pullup driver strength with nominal process, voltage and temperature conditions.

The nominal option enables the factory setting for the Pulldown, Pullup driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with Auto Calibration.

Data Termination

Bits A2 and A3 define the data termination value for the on-die termination (ODT) for the DQ and DBI# pins in combination with the driver strength setting.

The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for a weaker termination used in a lower power or frequency applications. The data termination may also be turned off.

ADR/CMD Termination

Bits A4 and A5 define the address/command termination. The default setting ('00') provides that the address/command termination is determined by latching CKE# on the rising edge of RESET#.

The address/command termination can also be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double loaded configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

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Calibration Update

The Calibration Update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled upon power-up to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling Calibration Update (A6=1).

The calibration updates can occur with any REFRESH command. The update is not complete for a time t_{KO} after the latching of the REFRESH command. During this t_{KO} time, only NOP or DESELECT commands may be issued

PLL and PLL Reset

If a PLL is to be used, it must be enabled for normal operation by setting bit A7 to '1'.

A PLL reset is done by turning the PLL off then on, or by use of the PLL Reset bit A11. The PLL Reset bit is self clearing meaning that it returns back to the value '0' after the PLL reset function has been issued.

RDBI and WDBI

Bit A8 controls Data Bus Inversion (DBI) for READs (RDBI), and bit A9 controls Data Bus Inversion for WRITEs (WDBI). For more details on DBI see READ and WRITE Data Bus Inversion (DBI) in the section entitled OPERATION.

ABI

Address Bus Inversion (ABI) is selected independently from DBI using bit A10. When enabled any data sent over the address bus (whether opcode, addresses, LDFF data or DM) is inverted or not inverted based on the state of ABI# signal. For more details on ABI see Address Bus Inversion (ABI) in the section entitled OPERATION.

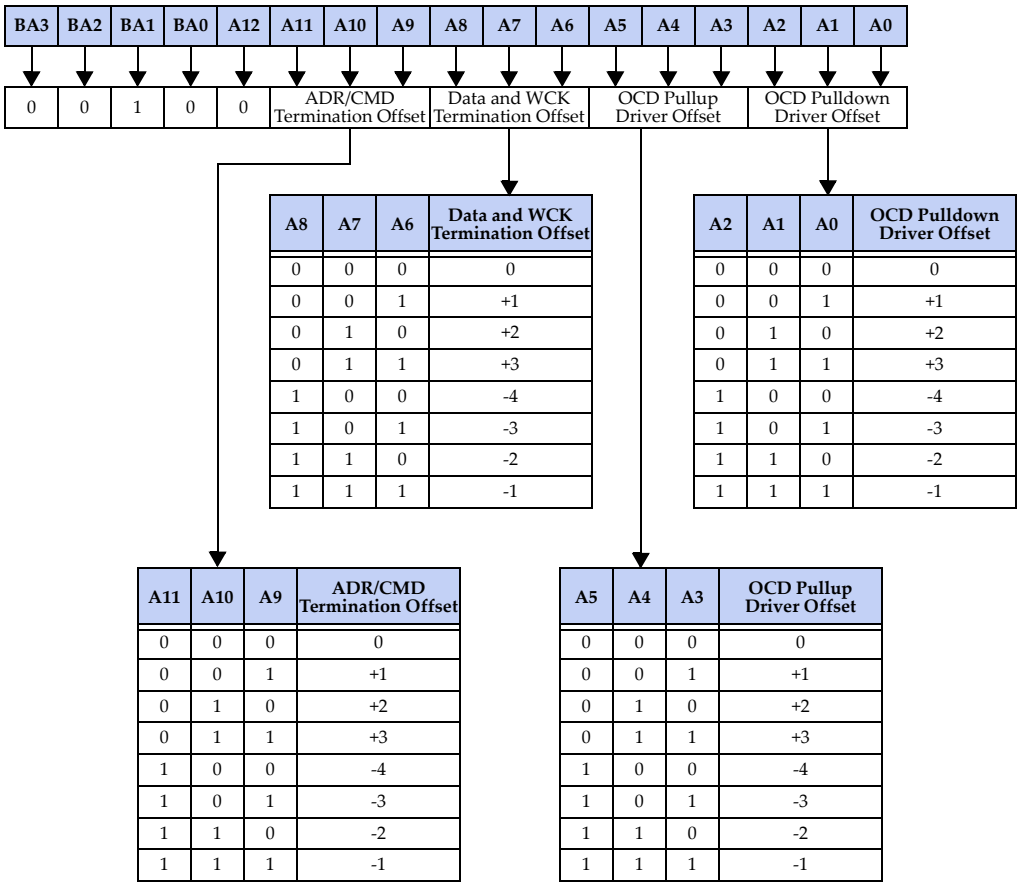
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4.3. MODE REGISTER 2 (MR2)

Mode Register 2 defines the output driver (OCD) and termination offsets as shown in Figure 25.

Mode Register 2 is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=0 and BA3=0.



A8	A7	A6	Data and WCK Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A2	A1	A0	OCD Pulldown Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A11	A10	A9	ADR/CMD Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A5	A4	A3	OCD Pullup Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Figure 25. Mode Register 2 (MR2) Definition

Impedance Offsets

The driver and termination impedances may be offset individually for PD driver, PU driver, DQ/DBI#/WCK termination and address/command termination. The offset impedance step values may be non-linear and will vary across PVT. With negative offset steps the drive strengths will be decreased and Ron

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will be increased. With positive offset steps the drive strengths will be increased and Ron will be decreased. With negative offset steps the termin-ation value will be increased. With positive offset steps the termination value will be decreased.

IV curves and AC timings are only guaranteed with zero offset.

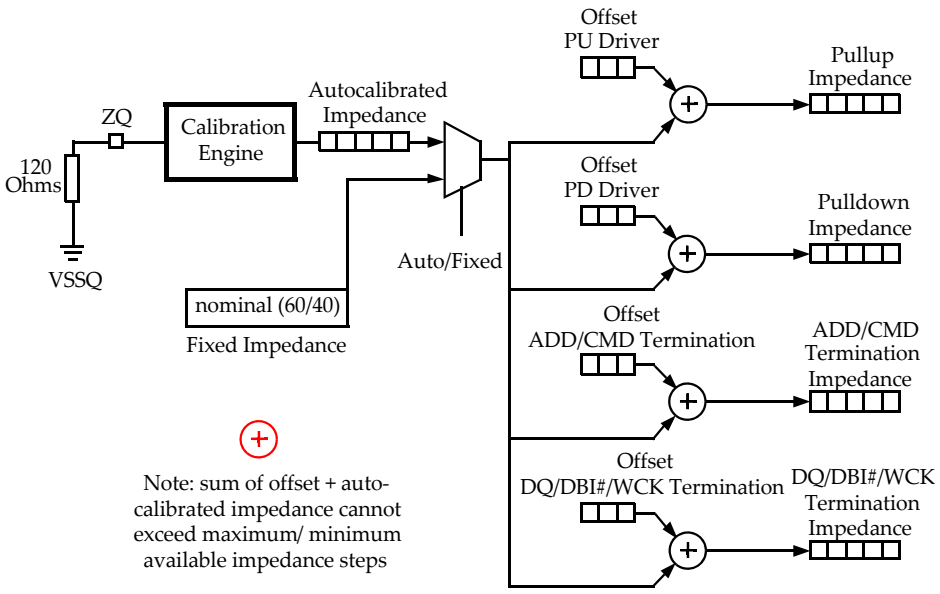


Figure 26. Impedance Offsets

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4.4. MODE REGISTER 3 (MR3)

Mode Register 3 controls functions including Bank Groups, WCK termination, self refresh, RDQS mode, DRAM Info and WCK2CK training as shown in Figure 27.

Mode Register 3 is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=0 and BA3=0.

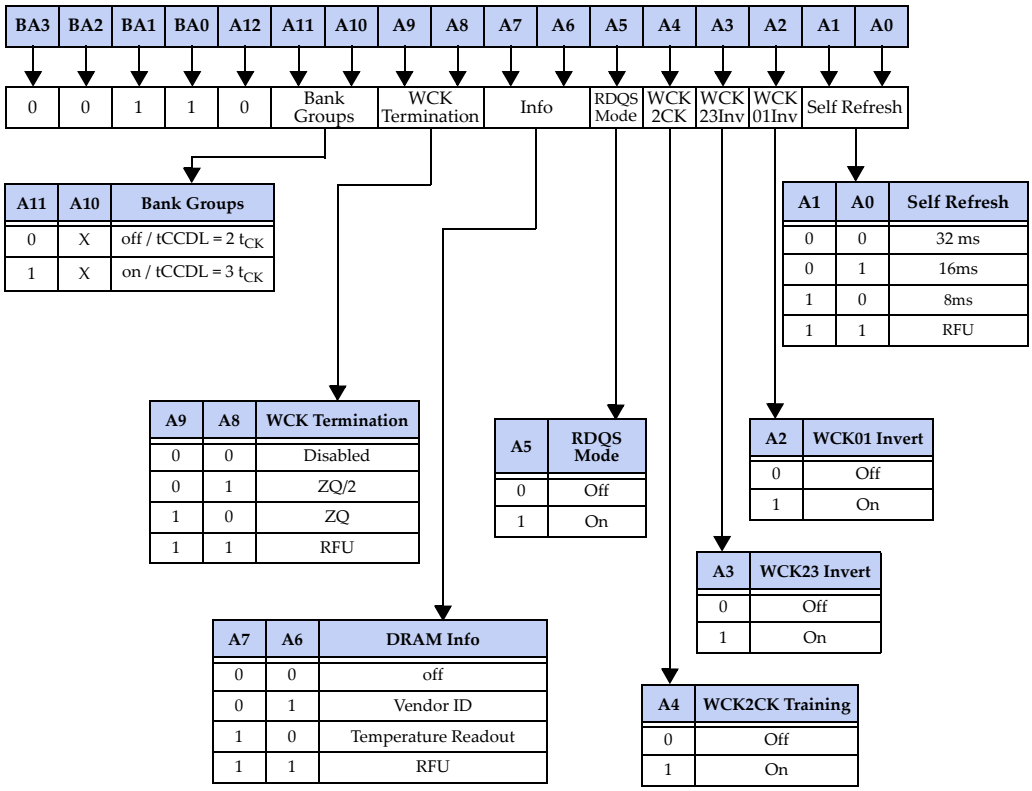


Figure 27. Mode Register 3 (MR3) Definition

Self Refresh

The refresh interval in self refresh mode may be set to 32ms, 16ms and 8ms.

WCK2CK

Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the section on TRAINING.

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WCK01 / WCK23 Inversion

Bits A2 and A3 control whether the internal phase of the WCK01 and WCK23 clock inputs after internal divide-by-2 shall be inverted, corresponding to a 2 U.I. phase shift. The bits are used in conjunction with WCK2CK training mode.

RDQS Mode

Bit A5 enables the RDQS mode of the GDDR5 SGRAM. In this mode the EDC pins will act as a READ strobe (RDQS). No CRC is supported in RDQS mode, and all related bits in MR4 will be ignored. A detailed description of the RDQS mode can be found in the section entitled OPERATION.

DRAM Info

Bits A6 and A7 enable the DRAM Info mode which is provided to output the Vendor ID, or the current junction temperature.

The Vendor ID identifies the manufacturer of the GDDR5 SGRAM, and provides the die revision, memory density and FIFO depth.

The Temperature Readout provides the SGRAM's junction temperature. The on-chip temperature sensor is enabled in advance by bit A6 in MR7.

WCK Termination

Bits A8 and A9 define the termination value for the on-die termination (ODT) for the WCK01, WCK01#, WCK23 and WCK23# pins in combination with the driver strength setting.

The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double load configurations with two devices sharing the WCK clocks. The WCK termination may also be turned off.

Bank Groups

Bit A11 enables the bank groups feature. With A11 set to '1', the bank groups feature is enabled and t_{CCDL} is 3tCK.

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4.5. MODE REGISTER 4 (MR4)

Mode Register 4 defines the Error Detection Code (EDC) features of GDDR5 SGRAMs as shown in Figure 28.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=1 and BA3=0. Bits A0-A3 (EDC Hold Pattern) of this register are initialized with '1111'.

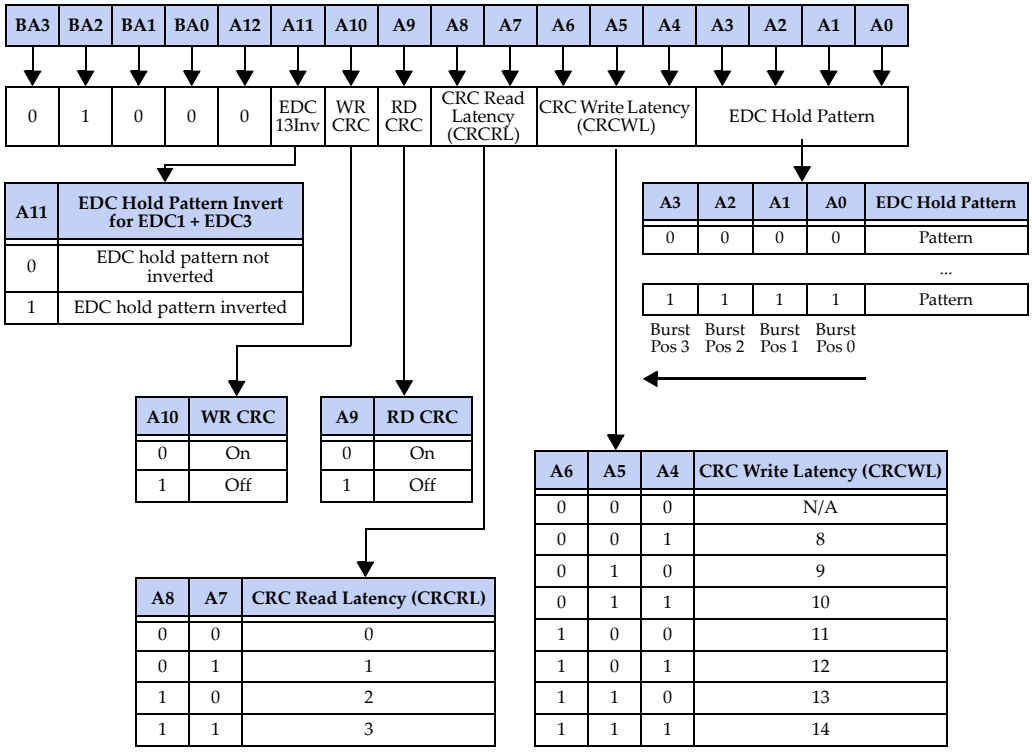


Figure 28. Mode Register 4 (MR4) Definition

EDC Hold pattern / EDC13 Invert

The 4-bit EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register is initialized with all '1's. The pattern is shifted from right to left and repeated with every clock cycle. The output timing is the same as of a READ burst.

CRC bursts calculated from WRITEs or READs will replace the EDC hold pattern for the duration of those bursts, provided CRC is enabled for those bursts.

With each MRS command to MR4 that changes bits A0-A3 or A9-A11, the EDC hold pattern will be undefined for t_{MRD}.

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The EDC hold pattern will not be transmitted when the device is in address training mode, in WCK2CK training mode, in RDQS mode, in self refresh mode, in reset state, in power-down state with the LP2 bit set, or in scan mode.

With register bit A11 set High, EDC1 and EDC3 will transmit the inverted EDC hold pattern, resulting in a pseudo-differential pattern. Please note that this function is not available in x16 configuration. Bit A11 is ignored for READ, WRITE and RDTR CRC bursts and the clock phase information in WCK2CK training mode.

CRC Write Latency (CRCWL)

The value of the CRC write latency is loaded into register bits A4-A6. If the DRAM vendor does not support the Mode Register definition of CRCWL, the Mode Register settings will be ignored. In that case the valid fixed latency is given with the DRAM vendor's specification. The user must set the CRCWL Mode Register bits.

Speed	Allowable Operating Frequency (Gbps)						
	CRCWL14	CRCWL13	CRCWL12	CRCWL11	CRCWL10	CRCWL9	CRCWL8
6.0Gbps							
5.5Gbps							
5.0Gbps							
4.5Gbps							
4.0Gbps							

CRC Read Latency (CRCRL)

The value of the CRC read latency is loaded into register bits A7-A8. If the DRAM vendor does not support the Mode Register definition of CRCRL, the Mode Register settings will be ignored. In that case the valid fixed latency is given with the DRAM vendor's specification. The user must set the CRCRL Mode Register bits.

Speed	RDBI ON/OFF	Allowable Operating Frequency (Gbps)			
		CRCRL3	CRCRL2	CRCRL1	CRCRL0
6.0Gbps	OFF				
	ON				
5.5Gbps	OFF				
	ON				
5.0Gbps	OFF				
	ON				
4.5Gbps	OFF				
	ON				
4.0Gbps	OFF				
	ON				

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Read CRC

Bit A9 controls the CRC calculation for READ bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCRL field of this register. With Read CRC being off, no CRC will be calculated for READ bursts, and the EDC hold pattern will be transmitted instead.

Write CRC

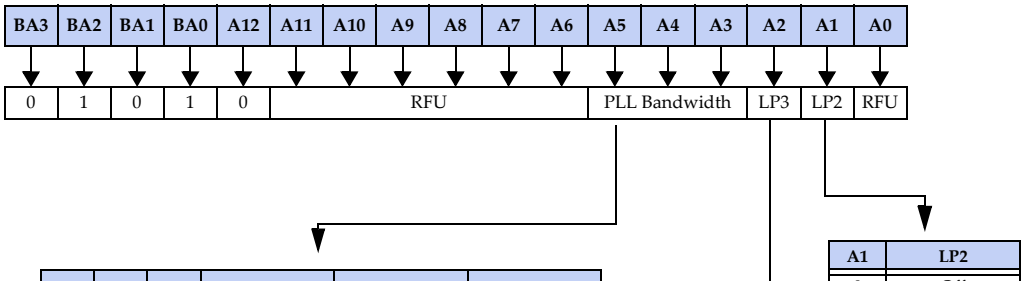
Bit A10 controls the CRC calculation for WRITE bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCWL field of this register. With Write CRC being off, no CRC will be calculated for WRITE bursts, and the EDC hold pattern will be transmitted instead.

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4.6. MODE REGISTER 5 (MR5)

Mode Register 5 defines digital RAS, PLL band-width and low power modes as shown in Figure 29.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=1 and BA3=0.



A5	A4	A3	-3dB [MHz] BW_{3dBLL}	Peak [MHz] BW_{PKLL}	Peak [dB] PK_{LL}
0	0	0	13	2	< 1.2
0	0	1	18	4	< 1.1
0	1	0	22	5	< 1.1
0	1	1	28	7	< 1.2
1	0	0	36	10	< 1.2
1	0	1	44	13	< 1.2
1	1	0	54	15	< 1.7
1	1	1	69	20	< 1.5

A1	LP2
0	Off
1	On

A2	LP3
0	Off
1	On

Note 1) PLL BW characteristics is extracted at 4Gbps
Note 2) PLL BW is linearly proportional to the data rate

Figure 29. Mode Register 5 (MR5) Definition

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Low Power Modes (LP2, LP3)

Bits A1-A2 control several low power modes of the GDDR5 SGRAM. The modes are independent of each other.

When bit A1 (LP2) is set, the WCK receivers may be turned off during power-down.

When bit A2 (LP3) is set, RDTR, WRTR and LDFF commands are not allowed while a REF command is being executed.

PLL Bandwidth

The PLL bandwidth may optionally be configured to match system characteristics. Each setting defines a unique combination of -3dB corner frequency, peaking frequency and peaking magnitude.

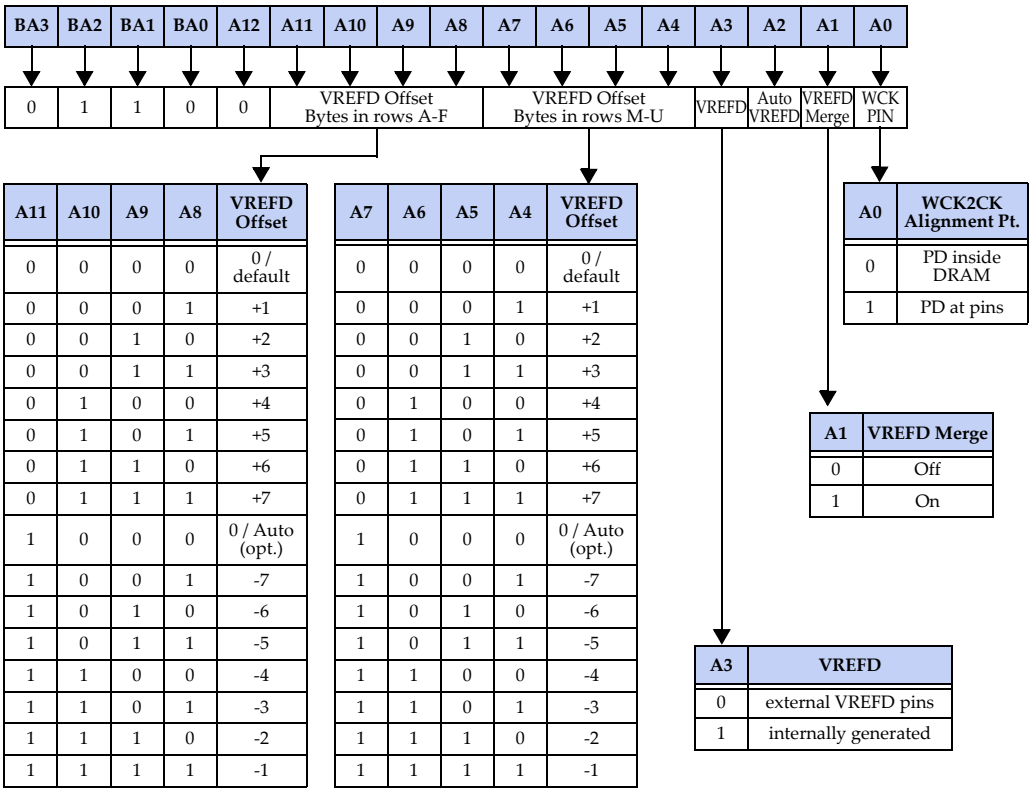
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4.7. MODE REGISTER 6 (MR6)

Mode Register 6 controls the WCK2CK alignment point and defines VREFD related features such as source, level, offsets, VREFD Merge and VREFD Auto Calibration mode, as shown in Figure 30.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=1 and BA3=0.



A11	A10	A9	A8	VREFD Offset
0	0	0	0	0 / default
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	0 / Auto (opt.)
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

A7	A6	A5	A4	VREFD Offset
0	0	0	0	0 / default
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	0 / Auto (opt.)
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

A0	WCK2CK Alignment Pt.
0	PD inside DRAM
1	PD at pins

A1	VREFD Merge
0	Off
1	On

A3	VREFD
0	external VREFD pins
1	internally generated

Figure 30. Mode Register 6 (MR6) Definition

WCK2CK Alignment Point (WCKPIN)

Bit A0 defines the position of the alignment point between CK and WCK. When set to '0', the alignment point will be at the phase detector inside the GDDR5 SGRAM. When set to '1', the alignment point will be at the CK and WCK pins.

Input Reference Voltage for DQ and DBI# Pins

GDDR5 SGRAMs offer multiple options for the input reference voltage (Vref) for the DQ and DBI# pins, as shown in Figure 31.

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Separate Vref circuits are associated with the bytes in rows A to F and the bytes in rows M to U, with separate VREFD pins for the required external Vref.

The only mandatory mode is that Vref will be supplied externally at the VREFD pins. This mode is configured with bits A1-A3 and bit A7 in MR7 all set to '0'.

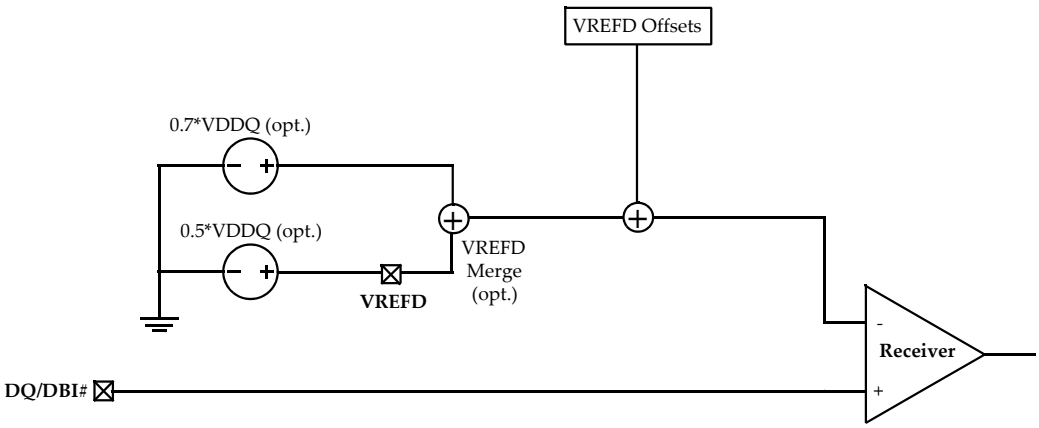


Figure 31. VREFD Options

VREFD Merge

The VREFD Merge mode is enabled when bit A1 is set to'1'. The externally supplied VFRED and the internally generated Vref will be merged, resulting in the average value of both. DRAM vendor specifications should be checked for values of external resistors that may be connected to VREFD pins in this VREF Merge mode.

Auto VREFD Training

When Auto is set for VREFD offsets, the internal Vref generator must be trained. Bit A2 enables this training; the bit is self-clearing, meaning that it returns back to the value '0' after the training has completed.

Once the training mode is enabled, the GDDR5 SGRAM drives the EDC pins Low to indicate to the controller that the training has started. The controller is now expected to send the specified PRBS pattern to the GDDR5 SGRAM. Upon completion of the training, the GDDR5 SGRAM stops driving the EDC pins Low, and the EDC pins will resume transmitting the EDC hold pattern.

But, it is not supported.

VREFD

Bit A3 selects between external and internal Vref. The bit is "Don't Care" when VREF Merge mode is selected.

VREFD Offsets and VREFD Auto Mode

It supports the capability to offset Vref independently for the upper 2 bytes and the lower 2 bytes. The offset step values may be non-linear and will vary across PVT.

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The vendors may optionally support the offset capability to be applied to the external Vref (not shown in Figure 31).

The optional Auto setting for VREFD enables the GDDR5 SGRAM to search for its own optimal internal Vref. There is no offset from this internally determined value (see also Auto VREFD Training).

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4.8. MODE REGISTER 7 (MR7)

Mode Register 7 controls features like PLL Standby, PLL Fast-Lock, PLL Delay Compensation, Low Frequency mode, Auto Synchronization, Data Preamble, Temperature Sensor operation, Half VREFD, VDD Range and DCC as shown in Figure 32.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=0.

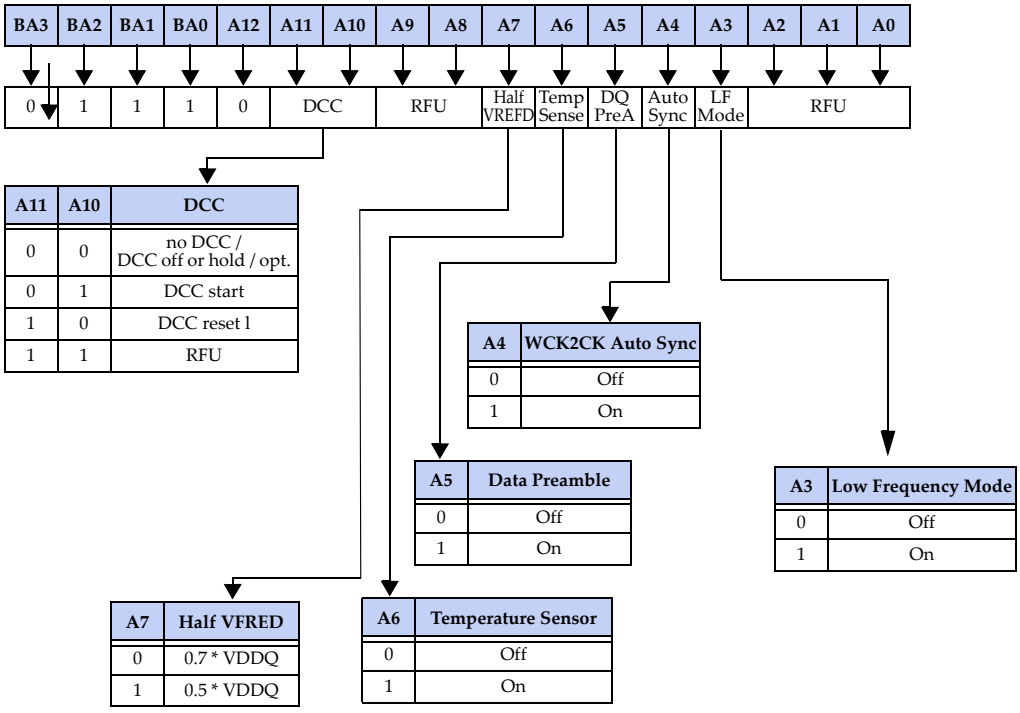


Figure 32. Mode Register 7 (MR7) Definition

Low Frequency Mode

When Low Frequency Mode is enabled by bit A3, the power consumption of input receivers and clock trees is reduced. The maximum operating frequency for this low frequency mode is given in the vendor's datasheet.

WCK2CK Auto Synchronization

GDDR5 SGRAMs support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit or for reducing WCK2CK training time at low frequency. This mode is controlled by bit A4. For a detailed description see WCK2CK Auto Synchronization in the section entitled WCK2CK Training.

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Data Preamble

When enabled by bit A5, non-gapless READ bursts will be preceded by a fixed data preamble on the DQ and DBI# pins of 4 U.I. duration. The programmed READ latency does not change when the Data Preamble is enabled. The pattern is not encoded with RDBI, however, if RDBI is disabled, the DBI# pins will not toggle and drive a HIGH.

Temperature Sensor

The on-chip temperature sensor is enabled by bit A6.

A detailed description of the Temperature Sensor can be found in the VENDOR ID, TEMP SENSOR and SCAN section.

Half VREFD

This mode allows users to adjust the Vref level in case the GDDR5 SGRAM is operated without termination: when bit A7 is set to'1', a Vref level of nominally 0.5 * VDDQ is expected at the VREFD pin or being generated internally (see Figure 31).

Duty Cycle Correction (DCC)

Bits A10 and A11 control the operation of the duty cycle corrector (DCC). The DCC can be used to cancel out a static duty cycle error on the WCK clocks. For more details see Duty Cycle Correction (DCC) in the section entitled OPERATION.

VREFD Selection Options Summary

The following table summarizes the complete set of VREFD selection options.

Table 15 VREFD Selection Options

MR6	MR7	Description
A3 Internal VREFD	A7 Half VREFD	
0	0	External
0	1	External
1	0	Internal 0.7 * VDDQ
1	1	Internal 0.5 * VDDQ

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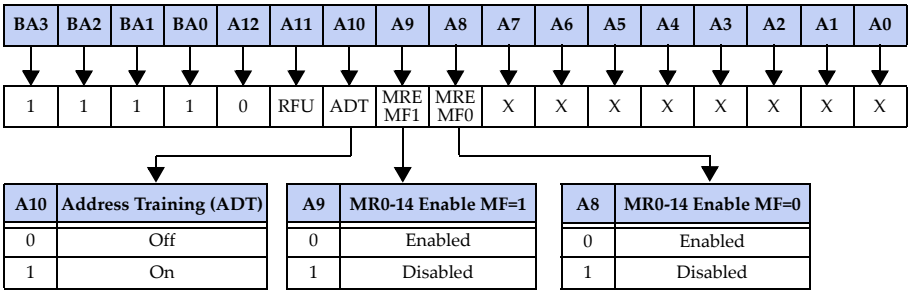
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4.9. MODE REGISTER 15 (MR15)

Mode Register 15 controls address training mode (ADT) and access to Mode Registers 0 to 14 (MRE) as shown in Figure 33.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=1.

Mode Register 15 is a special register that operates in SDR addressing mode. Increased setup and hold times as for command inputs are assumed to ensure the MRS command to this register is successful while address training (ADT) has not taken place and the integrity of DDR addresses may not be guaranteed. This is indicated by setting bits A0-A7 to Don't Care ("X") which are paired with the usable bits (A8-A11) and the Mode Register address (BA0-BA3).



A10	Address Training (ADT)
0	Off
1	On

A9	MR0-14 Enable MF=1
0	Enabled
1	Disabled

A8	MR0-14 Enable MF=0
0	Enabled
1	Disabled

Figure 33. Mode Register 15 (MR15) Definition

Address Training (ADT)

Address training mode is enabled and disabled with bit A10.

Mode Register 0-14 Enable

When disabled by bit A8 (for SGRAMs configured to MF=0) or bit A9 (for SGRAMs configured to MF=1), the GDDR5 SGRAM will ignore any MODE REGISTER SET command to Mode Registers 0 to 14. If enabled, MODE REGISTER SET commands function as normal. MODE REGISTER SET commands to Mode Register 15 (this register) are not affected and will always be executed.

This functional allows for individual configuration of two GDDR5 SGRAMS on a common address bus without the use of a CS# pin.

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5. OPERATION

5.1. COMMANDS

Table 16 Truth Table - Commands

Operation	Symbol	CKE#		CS#	RAS#	CAS#	WE#	BA	A11	A10	A8	A6, A7, A9, (A12)	A0-A5 (A6)	Notes
		Previous cycle	Current cycle											
DESELECT (NOP)	DES	L	X	H	X	X	X	X	X	X	X	X	X	1, 2, 8
NO OPERATION (NOP)	NOP	L	X	L	H	H	H	X	X	X	X	X	X	1, 2, 8
MODE REGISTER SET	MRS	L	L	L	L	L	L	MRA	Opcode					1, 2, 3
ACTIVE (Select bank & activate row)	ACT	L	L	L	L	H	H	BA	RA					1, 2, 4
READ (Select bank and column, & start burst)	RD	L	L	L	H	L	H	BA	L	L	L	X	CA	1, 2, 5, 9
READ with Autoprecharge	RDA	L	L	L	H	L	H	BA	L	L	H	X	CA	1, 2, 5
Load FIFO	LDFF	L	L	L	H	L	H	X	H	L	L	X	X	1, 2, 7
READ Training	RDTR	L	L	L	H	L	H	X	H	H	L	X	X	1, 2
WRITE without Mask (Select bank and column, & start burst)	WOM	L	L	L	H	L	L	BA	L	L	L	X	CA	1, 2, 5
WRITE without Mask with Autoprecharge	WOMA	L	L	L	H	L	L	BA	L	L	H	X	CA	1, 2, 5
WRITE with single-byte mask	WSM	L	L	L	H	L	L	BA	L	H	L	X	CA	1, 2, 5
WRITE with single-byte mask with Autoprecharge	WSMA	L	L	L	H	L	L	BA	L	H	H	X	CA	1, 2, 5
WRITE with double-byte mask (WDM)	WDM	L	L	L	H	L	L	BA	H	L	L	X	CA	1, 2, 5
WRITE with double-byte mask with Autoprecharge	WDMA	L	L	L	H	L	L	BA	H	L	H	X	CA	1, 2, 5
WRITE Training	WRTR	L	L	L	H	L	L	X	H	H	L	X	X	1, 2
PRECHARGE (Deactivate row in bank or banks)	PRE	L	L	L	L	H	L	BA	X	X	L	X	X	1, 2
PRECHARGE ALL	PREALL	L	L	L	L	H	L	X	X	X	H	X	X	1, 2
REFRESH	REF	L	L	L	L	L	H	X	X	X	X	X	X	1, 6
POWER DOWN ENTRY	PDE	L	H	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H	X	X	X	X	X	X	1
POWER DOWN EXIT	PDX	H	L	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H							
SELF REFRESH ENTRY	SRE	L	H	L	L	L	H	X	X	X	X	X	X	1, 6
SELF REFRESH EXIT	SRX	H	L	H	X	X	X	X	X	X	X	X	X	1
				L	H	H	H							

Notes:
1) H = Logic High Level; L = Logic Low Level; X = Don't care: signal may be H or L, but not floating
2) Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and ABI#=L
3) BA0-BA3 provide the Mode Register address (MRA), A0-A11 the opcode to be loaded
4) BA0-BA3 provide the bank address (BA), A0-A11 (A12) provide the row address (RA).
5) BA0-BA3 provide the bank address, A0-A5 (A6) provide the column address (CA); no sub-word addressing within a burst of 8.
6) The command is Refresh when CKE#(n) = L and Self Refresh Entry when CKE#(n) = H.
7) BA0-BA3 and CA are used to select burst location and data respectively
8) DESELECT and NOP are functionally interchangeable
9) In address training mode READ is decoded from the commands pins only with RAS# = H, CAS# = L, WE# = H

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Figure 34 and Figure 35 illustrate the timings associated with the Command and Address input as well as Data input.

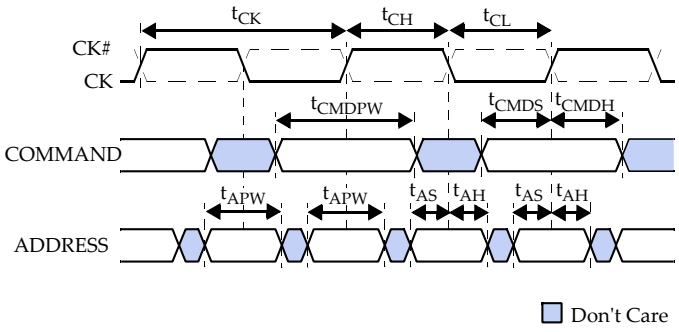


Figure 34. Command and Address Input Timings

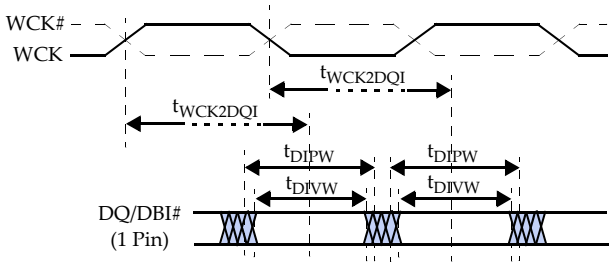


Figure 35. Data Input Timings

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5.2. DESELECT (NOP)

The DESELECT function (CS# HIGH) prevents new commands from being executed by the GDDR5 SGRAM. The GDDR5 SGRAM is effectively deselected. Operations already in progress are not affected.

5.3. NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR5 SGRAM to perform a NOP (CS# LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

5.4. MODE REGISTER SET

The MODE REGISTER SET command is used to load the Mode Registers of the GDDR5 SGRAM. The bank address inputs BA0-BA3 select the Mode Register, and address puts A0-A11(A12) determine the op-code to be loaded. See MODE REGISTER for a register definition. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until t_{MRD} is met.

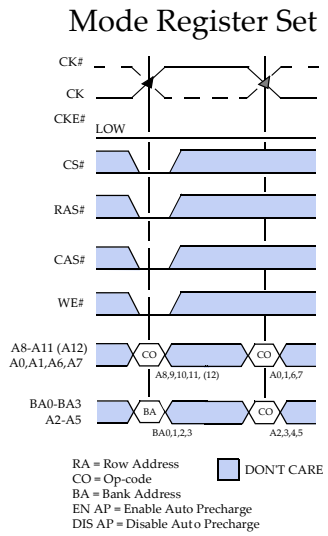
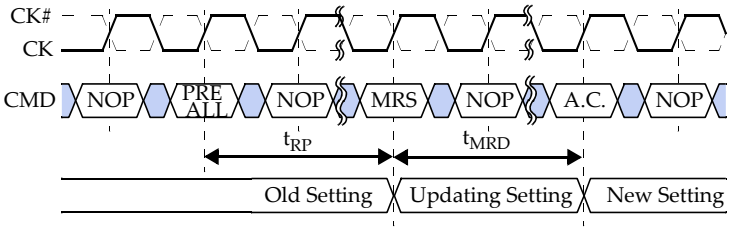


Figure 36. MRS Command

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A.C. = any command allowed in bank idle state

Figure 37. Mode Register Set Timings

5.5. ACTIVATION

Before any READ or WRITE commands can be issued to a bank in the GDDR5 SGRAM, a row in that bank must be "opened". This is accomplished by the ACTIVE command (see Figure 38): BA0 -BA3 select the bank, and A0-A11 (A12) select the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed (precharged). The minimum time interval between two successive ACTIVE commands on the same bank is defined by t_{RC}. A minimum time, t_{RAS}, must have elapsed between opening and closing a row.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks to different bank groups is defined by t_{RRDS}. With bank groups enabled, the minimum time interval between two successive ACTIVE commands to different banks in the same bank group is defined by t_{RRDL}. In all other cases the interval is defined by t_{RRDS}. <Link>Figure shows the t_{RCD} and t_{RRD} definition.

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The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Pre-charge) is issued to the bank.

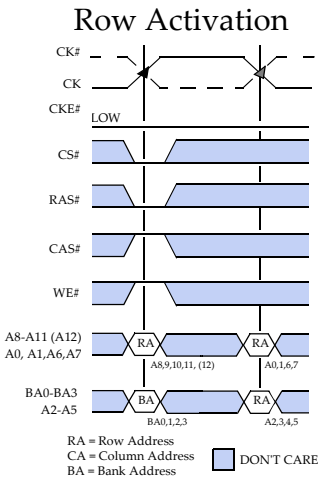


Figure 38. Active Command

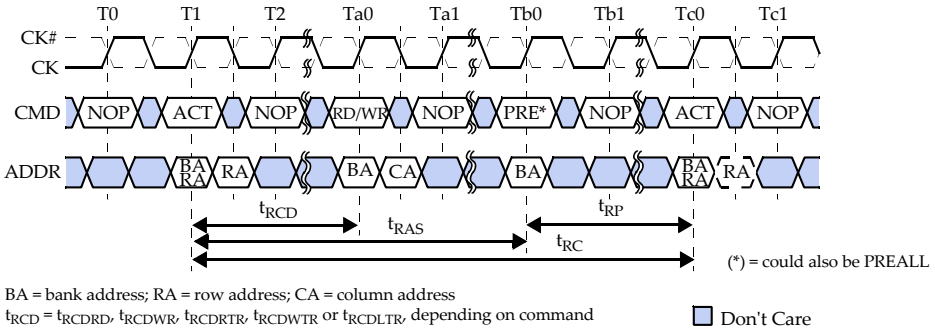


Figure 39. Bank Activation Command Cycle

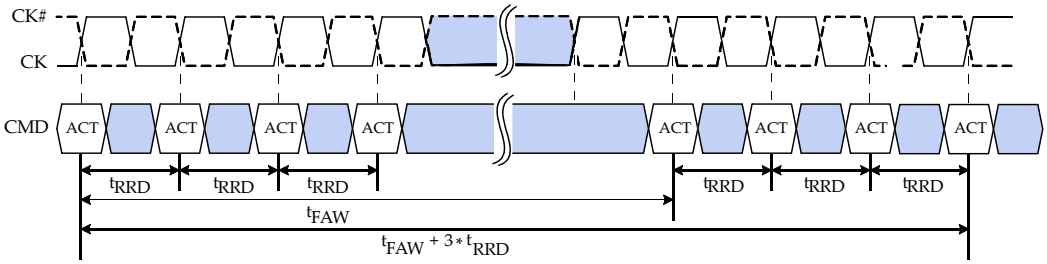
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5.6. BANK RESTRICTIONS

There may be a need to limit the number of activates in a rolling window to ensure that the instantaneous current supplying capability of the devices is not exceeded. To reflect the short term capability of the GDDR5 SGRAM current supply, the parameter t_{FAW} (four activate window) is defined. No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 10 clocks, and an activate command is issued at clock N, no more than three further activate commands may be issued at clocks N+1 through N+9 as illustrated in Figure 40.

To reflect a longer term GDDR5 SGRAM current supply capability, the parameter t_{32AW} (thirty-two activate window) is defined. No more than 32 banks may be activated in a rolling t_{32AW} window. Converting to clocks is done by dividing t_{32AW} (ns) by t_{CK} (ns) and rounding up to next integer value. The use of a shorter and longer rolling activation window allows the GDDR5 SGRAM design to be optimized to handle higher instantaneous currents within a shorter window while still limiting the current strain over a longer period of time. This means that in general t_{32AW} will be greater than or equal to 8* t_{FAW} as shown in Figure41.

It is preferable that GDDR5 SGRAMs have no rolling activation window restrictions (t_{FAW} = 4 * t_{RRD}).



t_{RRD} = t_{RRDL} or t_{RRDS} depending on Bank Groups on/off setting and accessed banks

Figure 40. t_{RRD} and t_{FAW}

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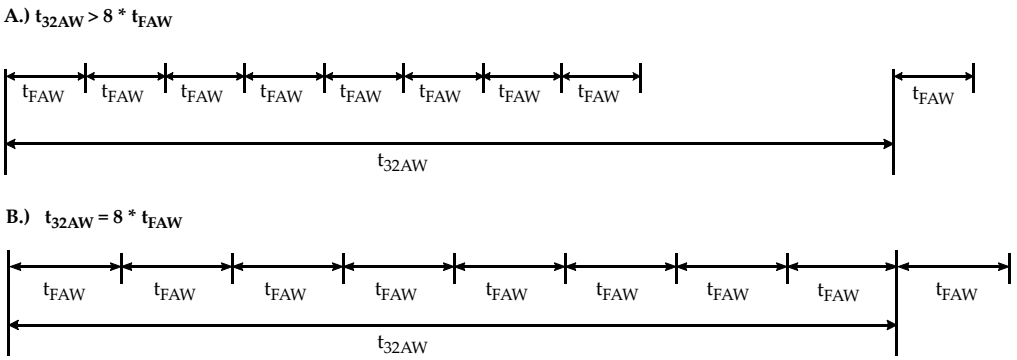


Figure 41. t_{32AW}

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5.7. WRITE (WOM)

WRITE bursts are initiated with a WRITE command as shown in Figure 42. The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met. The length of the burst initiated with a WRITE command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of WRITE bursts.

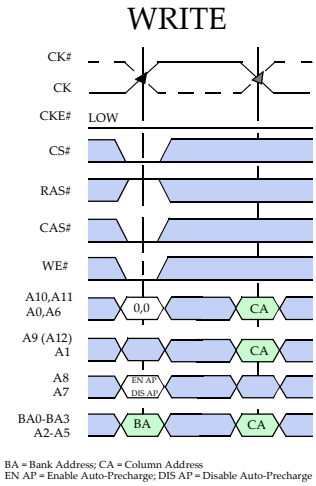


Figure 42. WRITE Command

During WRITE bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is defined as WLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQI}$, where WLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the GDDR5 SGRAM phase detector, and $t_{WCK2DQI}$ is the WCK to DQ/DBI# offset as measured at the DRAM pins to ensure concurrent arrival at the latch. The total delay is relative to the data eye center averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQI}.

The data input valid window, t_{DIVW}, defines the time region when input data must be valid for reliable data capture at the receiver for any one worst-case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (i.e. within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL mode and bandwidth. t_{DIVW} is measured at the pins. t_{DIVW} is defined for the PLL off and on mode separately. In the case of PLL on, t_{DIVW} must be specified for each supported bandwidth. In general t_{DIVW} is smaller than t_{DIPW}.

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The data input pulse width, t_{DIPW}, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. t_{DIPW} is measured at the pins. t_{DIPW} is independent of the PLL mode. In general t_{DIPW} is larger than t_{DIVW}.

Upon completion of a burst, assuming no other WRITE data is expected on the bus the GDDR5 SGRAM DQ and DBI# pins will be driven according to the ODT state. Any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command.

Data from any WRITE burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the t_{CCD} timing. If that WRITE command is to another bank then an ACTIVE command must precede the WRITE command and t_{RCDWR} also must be met.

A READ can be issued any time after a WRITE command as long as the internal turn around time t_{WTR} is met. If that READ command is to another bank, then an ACTIVE command must precede the READ command and t_{RCDRD} also must be met.

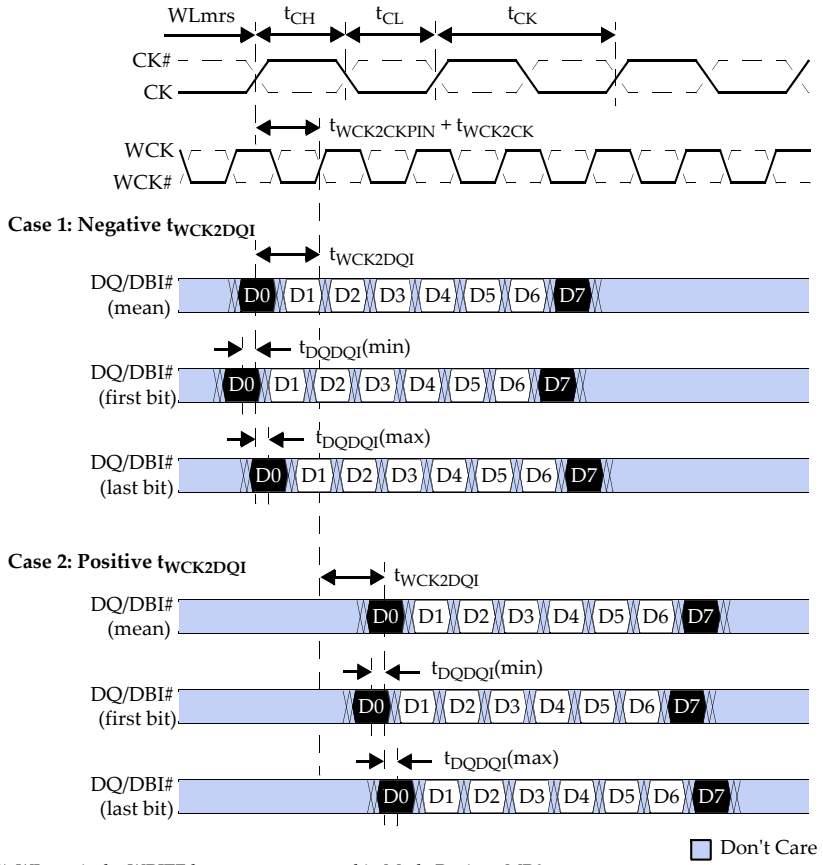
A PRECHARGE can also be issued to the GDDR5 SGRAM with the same timing restriction as the new WRITE command if t_{RAS} is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag is received on the DBI# pin to identify whether to store the true or inverted data. If DBI# is LOW, the data will be stored after inversion inside the GDDR5 SGRAM and not inverted if DBI# is HIGH. WRITE Data Inversion can be enabled (A9=0) or disabled (A9=1) using WDBI in MR1.

When enabled by the WRCRC flag in MR4, EDC data are returned to the controller with a latency of (WLmrs + CRCWL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCWL is the CRC Write latency programmed in MR4 and $t_{WCK2DQO}$ is the WCK to DQ/DBI#/EDC phase offset at the DRAM pins.

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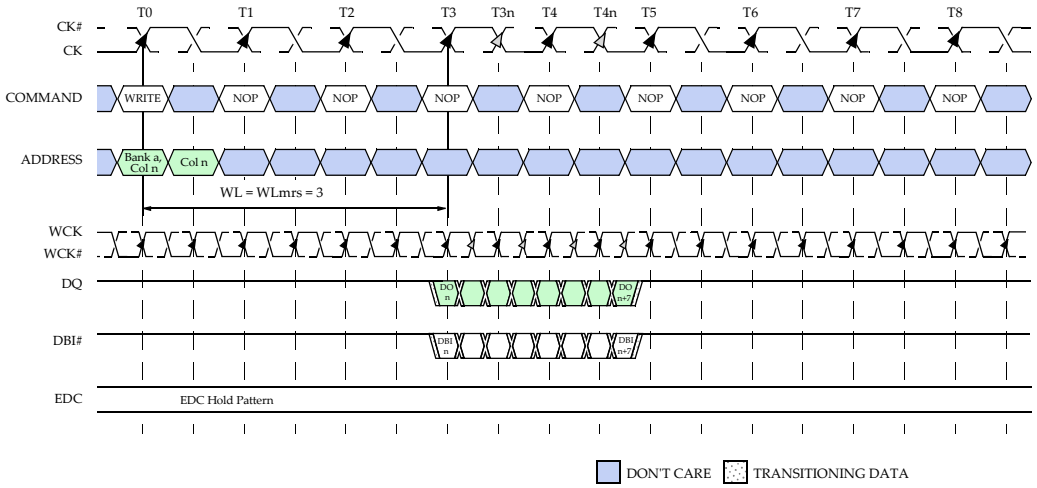


1) WLmrs is the WRITE latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK2CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQI}$ parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQI}$ value for stable WRITE operation.
4) t_{DQDQI} defines the minimum to maximum variation of $t_{WCK2DQI}$ within a double byte (x32 mode) or a single byte (x16 mode).
5) Data Read timings are used for CRC return timing from WRITE commands with CRC enabled.

Figure 43. WRITE Timings

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Notes: 1. WLmrs = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

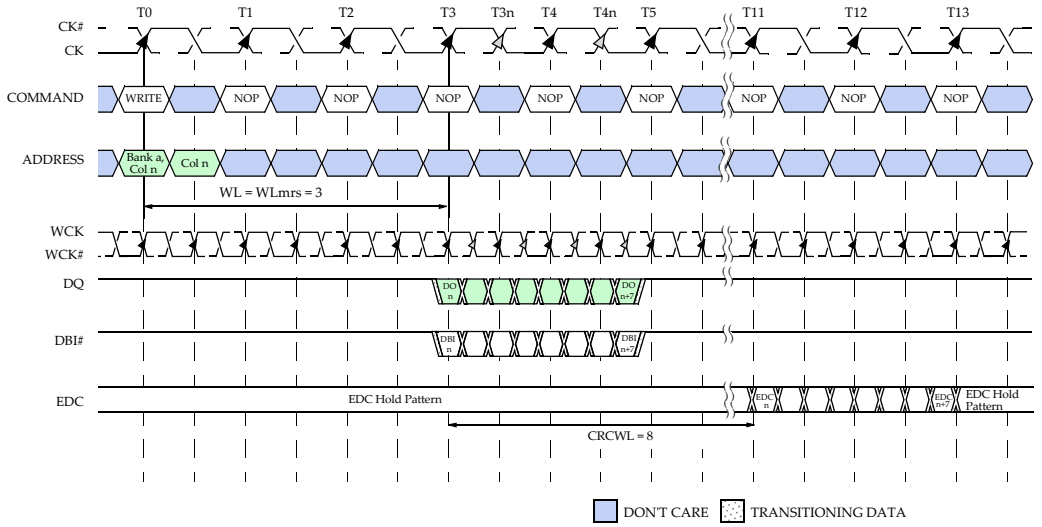
3. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

4. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

5. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 44. Single WRITE without EDC

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Notes: 1. WLmrs = 3 and CRCWL = 8 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

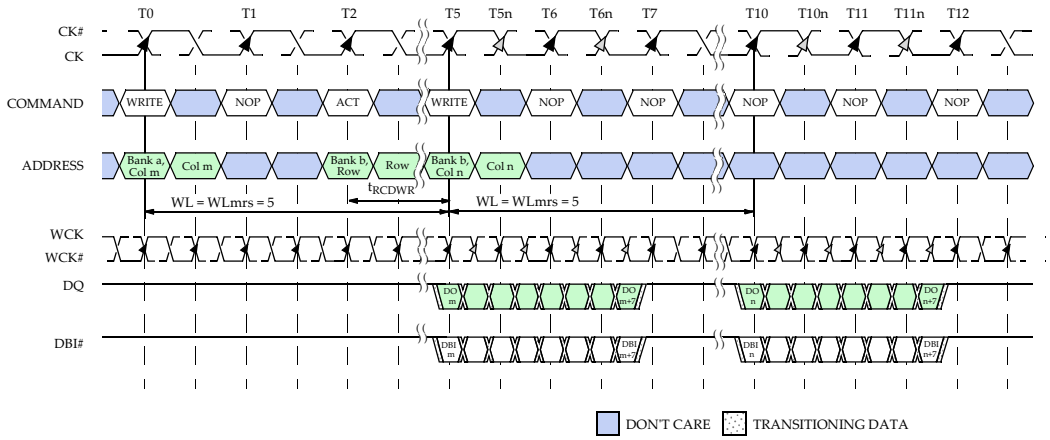
3. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

4. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

5. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 45. Single WRITE with EDC

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Notes: 1. WLmrs = 5 and t_{RCDWR} = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

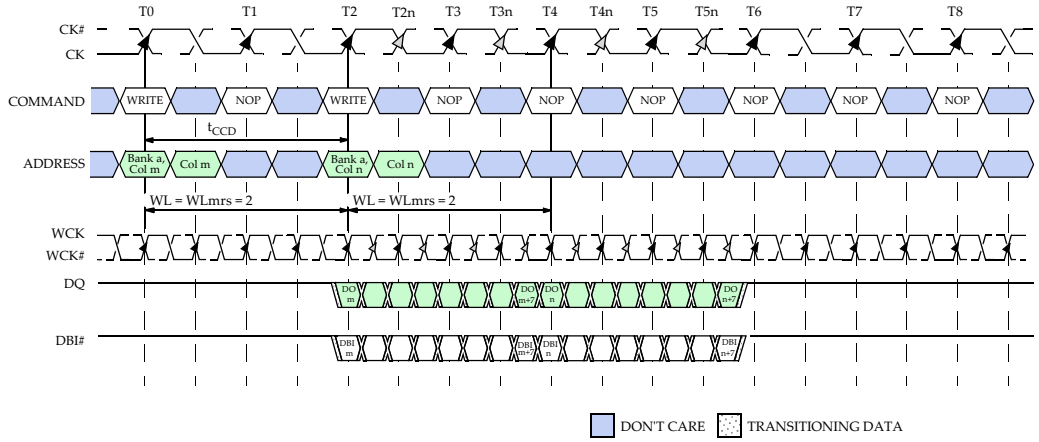
4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 46. Non-Gapless WRITEs

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Notes: 1. WLmrs = 2 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. t_{CCD} = t_{CCDS} when bank groups is disabled or the second WRITE is to a different bank group, otherwise t_{CCD}=t_{CCDL}.

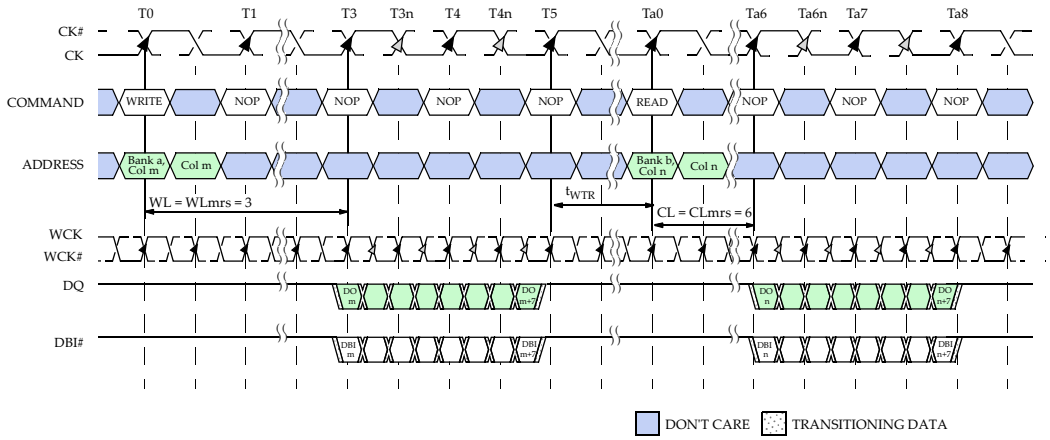
5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

6. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

7. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 47. Gapless WRITEs

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Notes: 1. WLmrs = 3 and CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. t_{WTR} = t_{WTRL} when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise t_{WTR}=t_{WTRS}.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

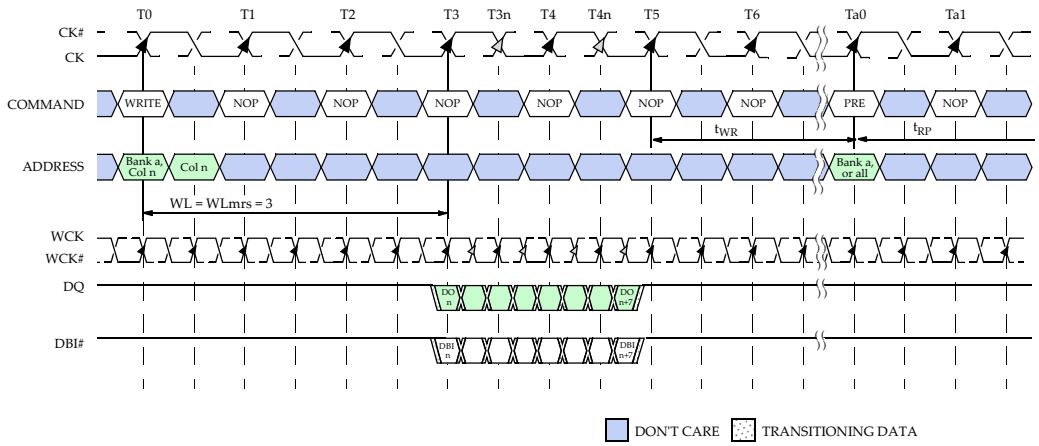
6. Before the READ and WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} or t_{RCDWR} respectively must be met.

7. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 48. WRITE to READ

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Notes: 1. WLmrs = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE command, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 49. WRITE to PRECHARGE

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5.8. WRITE DATA MASK (DM)

The traditional method of using a DM pin for WRITE data mask must be abandoned for a new method. Due to the high data rate of GDDR5 SGRAMs, bit errors are expected on the interface and are not recoverable when they occur on the traditional DM pin.

In GDDR5 the DM is sent to the SGRAM over the address following the bank/column address cycle associated with the command, during the NOP/DESELECT commands between the WRITE command and the next command. The DM is used to mask the corresponding data according to the following table.

Table 17: DM State

FUNCTION	DM Value	DQ
Write Enable	0	Valid
Write Inhibit	1	X

Two additional WRITE commands that augment the traditional WRITE Without Mask (WOM) are required for proper DM support:

- WDM: WRITE-With-Doublebyte-Mask:

2 cycle command where the 1st cycle carries address information and the 2nd cycle carries data mask information (2 byte granularity);

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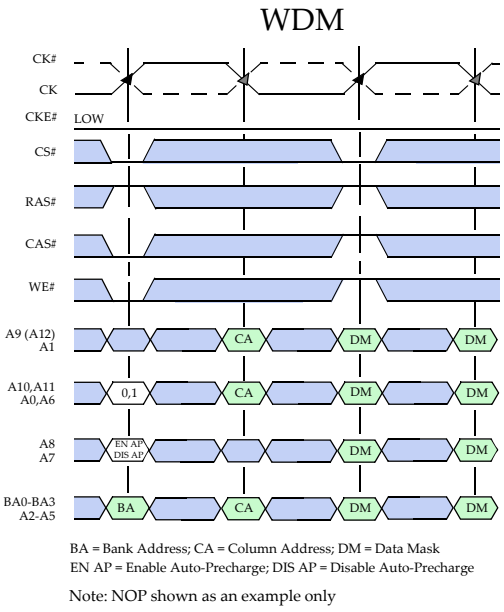
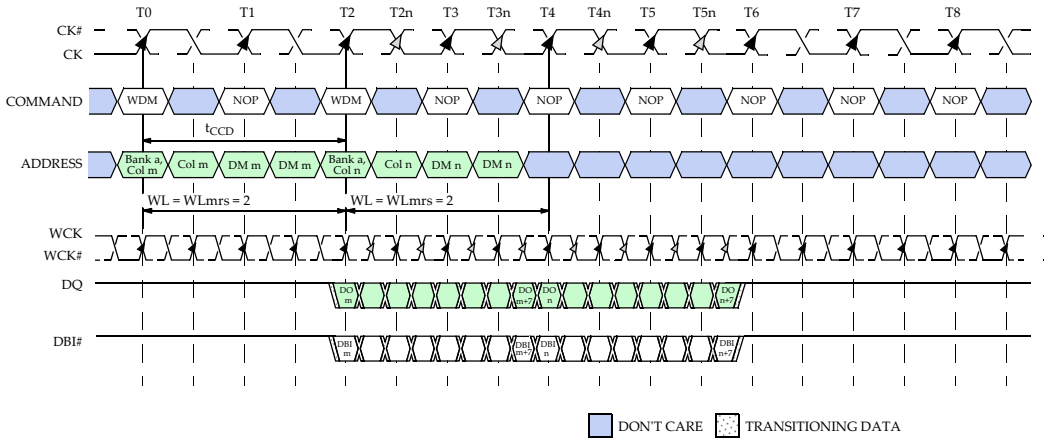


Figure 50. WRITE-With-Doublebyte-Mask Command



Notes: 1. WLmrs = 2 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
3. EDC may be on or off. See Figure 4 for EDC Timing.
4. t_{CCD} = t_{CCDS} when bank groups is disabled or the second WRITE is to a different bank group, otherwise t_{CCD}=t_{CCDL}.
5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.
6. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.
7. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

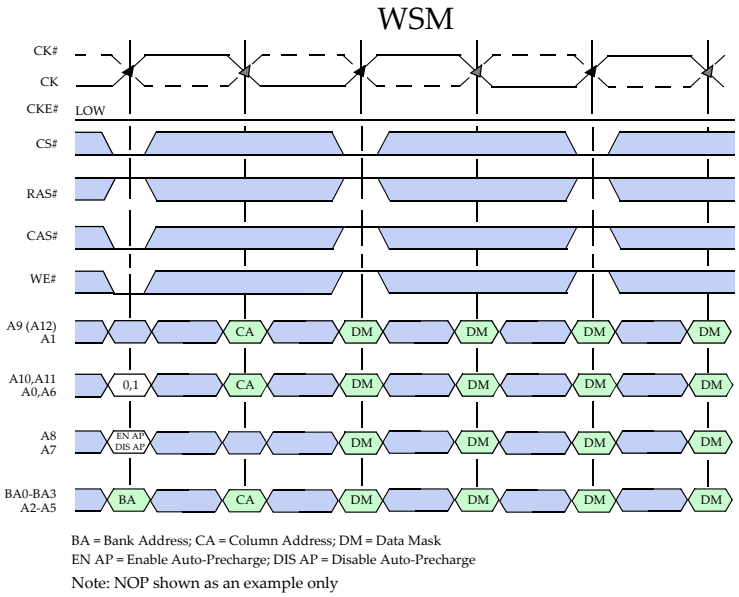
Figure 51. WDM Timing

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- WSM: WRITE-With-Singlebyte-Mask:

3 cycle command where the 1st cycle carries address information, the 2nd and 3rd cycle carry data mask information

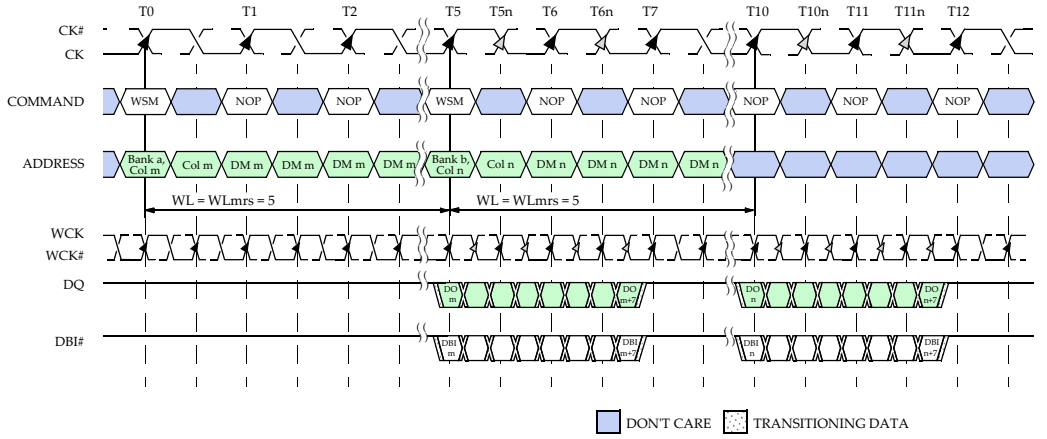


BA = Bank Address; CA = Column Address; DM = Data Mask
EN AP = Enable Auto-Precharge; DIS AP = Disable Auto-Precharge
Note: NOP shown as an example only

Figure 52. WRITE-With-Singlebyte-Mask Command

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Notes: 1. WLmrs = 5 and t_{RCDWR} = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDWR} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 53. WSM Timing

Table 18 WDM Mapping for mirrored & non-mirrored x32 Mode

Byte and Burst Position Masked during WDM					
ADR	ADR CK Rising Edge		ADR	ADR CK# Rising Edge	
	Byte	Burst		Byte	Burst
A10	DQ[15:0]	0	A0	DQ[15:0]	4
A9	DQ[15:0]	1	A1	DQ[15:0]	5
BA0	DQ[15:0]	2	A2	DQ[15:0]	6
BA3	DQ[15:0]	3	A3	DQ[15:0]	7
BA2	DQ[31:16]	0	A4	DQ[31:16]	4
BA1	DQ[31:16]	1	A5	DQ[31:16]	5
A11	DQ[31:16]	2	A6	DQ[31:16]	6
A8	DQ[31:16]	3	A7	DQ[31:16]	7

Table 19 WDM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked during WDM					
	ADR CK Rising Edge		ADR	ADR CK# Rising Edge	
ADR	Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7

Table 20 WDM Mapping for mirrored x16 Mode

Byte and Burst Position Masked during WDM					
	ADR CK Rising Edge		ADR	ADR CK# Rising Edge	
ADR	Byte	Burst		Byte	Burst
A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[31:24]	3	A7	DQ[31:24]	7

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Table 21 WSM Mapping for mirrored and non-mirrored x32 Mode

Byte and Burst Position Masked During WSM												
ADR CK 1st rising Edge			ADR CK# 1st rising Edge			ADR CK 2nd rising Edge			ADR CK# 2nd rising Edge			
ADR	Byte	Burst	ADR	Byte	Burst	ADR	Byte	Burst	ADR	Byte	Burst	
A10	DQ[7:0]	0	A0	DQ[7:0]	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4	
A9	DQ[7:0]	1	A1	DQ[7:0]	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5	
BA0	DQ[7:0]	2	A2	DQ[7:0]	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6	
BA3	DQ[7:0]	3	A3	DQ[7:0]	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7	
BA2	DQ[23:16]	0	A4	DQ[23:16]	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4	
BA1	DQ[23:16]	1	A5	DQ[23:16]	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5	
A11	DQ[23:16]	2	A6	DQ[23:16]	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6	
A8	DQ[23:16]	3	A7	DQ[23:16]	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7	

Table 22 WSM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked During WSM											
ADR CK 1st rising Edge			ADR CK# 1st rising Edge			ADR CK 2nd rising Edge			ADR CK# 2nd rising Edge		
ADR	Byte	Burst	ADR	Byte	Burst		Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4		-	0		-	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5		-	1		-	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6		-	2		-	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7		-	3		-	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4		-	0		-	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5		-	1		-	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6		-	2		-	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7		-	3		-	7

Table 23 WSM Mapping for mirrored x16 Mode

Byte and Burst Position Masked During WSM											
ADR CK 1st rising Edge			ADR CK# 1st rising Edge			ADR CK 2nd rising Edge			ADR CK# 2nd rising Edge		
	Byte	Burst		Byte	Burst	ADR	Byte	Burst	ADR	Byte	Burst
	-	0		-	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4
	-	1		-	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5
	-	2		-	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6
	-	3		-	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7
	-	0		-	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4
	-	1		-	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5
	-	2		-	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6
	-	3		-	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7

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5.9. READ

A READ burst is initiated with a READ command as shown in Figure 54. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access with the A8 address. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met. The length of the burst initiated with a READ command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of READ bursts.

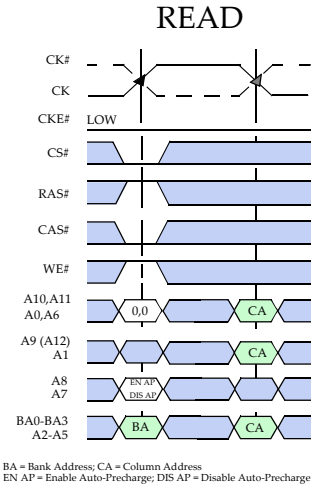


Figure 54. READ Command

During READ bursts, the first valid data-out element will be available after the CAS latency (CL). The CAS Latency is defined as CLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the GDDR5 SGRAM phase detector, and $t_{WCK2DQO}$ is the WCK to DQ/DBI#/EDC offset as measured at the DRAM pins. The total delay is relative to the data eye initial edge averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQO}.

Upon completion of a burst, assuming no other READ command has been initiated, all DQ and DBI# pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t_{CCD} timing. If that READ command is to another bank then an ACTIVE command must precede the READ command and t_{RCDRD} also must be met.

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A WRITE can be issued any time after a READ command as long as the bus turn around time t_{RTW} is met. If that WRITE command is to another bank, then an ACTIVE command must precede the second WRITE command and t_{RCDWR} also must be met.

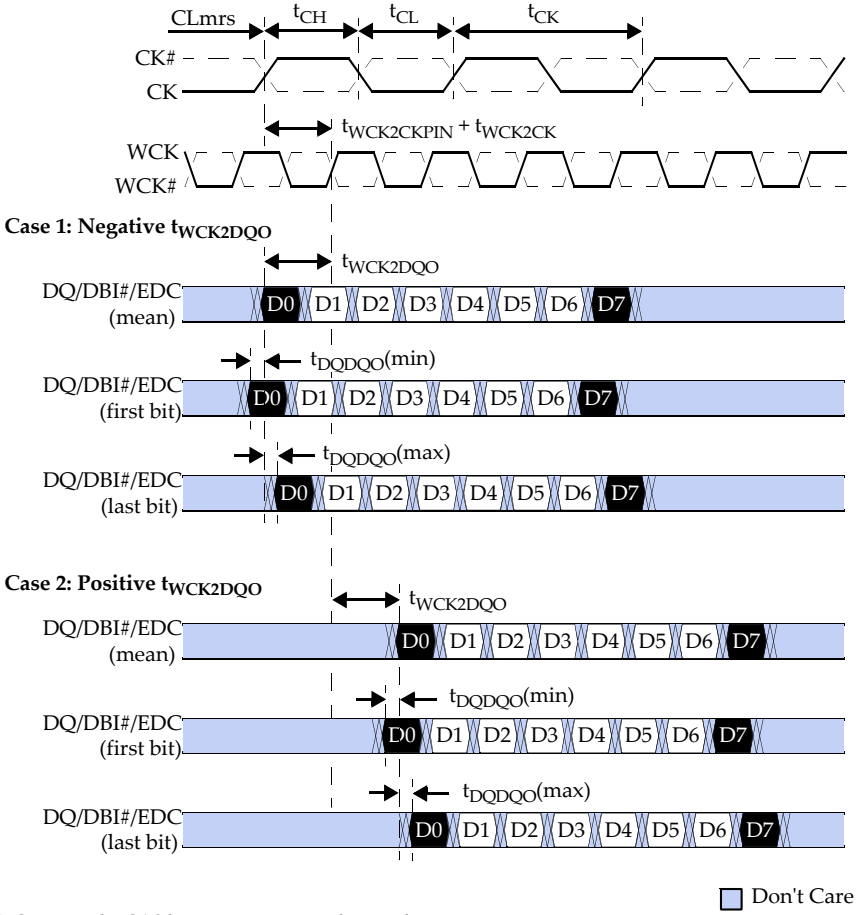
A PRECHARGE can also be issued to the GDDR5 SGRAM with the same timing restriction as the new READ command if t_{RAS} is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag is driven on the DBI# pin to identify whether the data is true or inverted data. If DBI# is HIGH, the data is not inverted, and if LOW it is inverted. READ Data Inversion can be enabled (A8=0) or disabled (A8=1) using RDBI in MR1.

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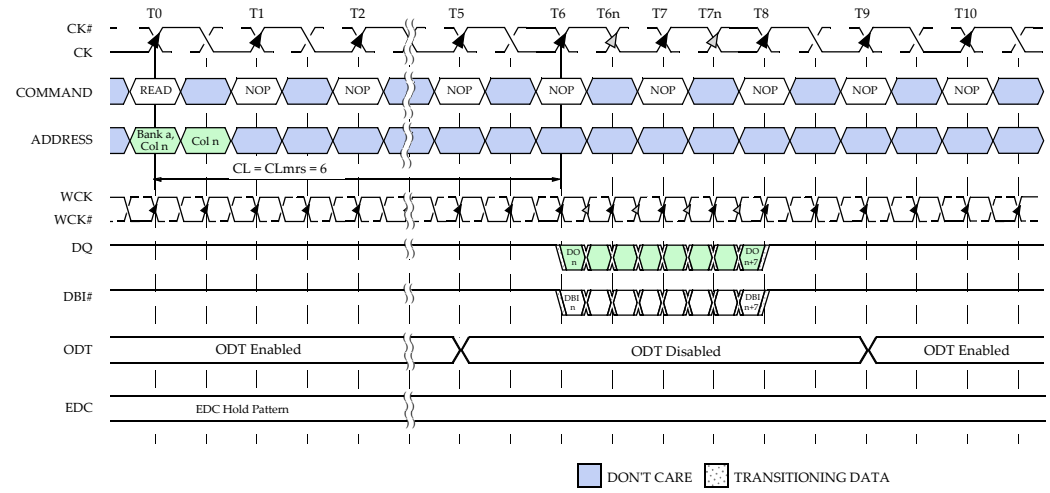
When enabled by the RDCRC flag in MR4, EDC data is returned to the controller with a latency of (CLmrs + CRCRL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCRL is the CRC Read latency programmed in MR4.



1) CLmrs is the CAS latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK2CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQO}$ parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQO}$ value for stable READ operation.
4) t_{DQDQO} defines the minimum to maximum variation of $t_{WCK2DQO}$ within a double byte (x32 mode) or a single byte (x16 mode).
5) t_{DQDQO} also applies for CRC data from WRITE and READ commands with CRC enabled, the EDC hold pattern, and the data strobe in RDQS mode.

Figure 55. READ Word Lane Timing

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Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

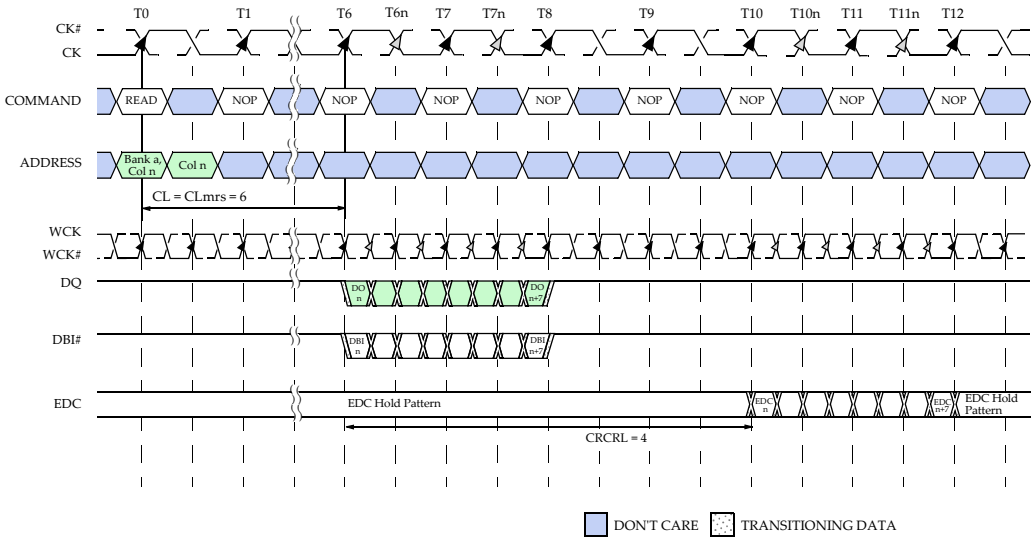
3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

4. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 56. Single READ without EDC

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Notes: 1. CLmrs = 6 and CRCRL = 4 are shown as examples. Actual supported values will be found in the MR and AC timings sections.

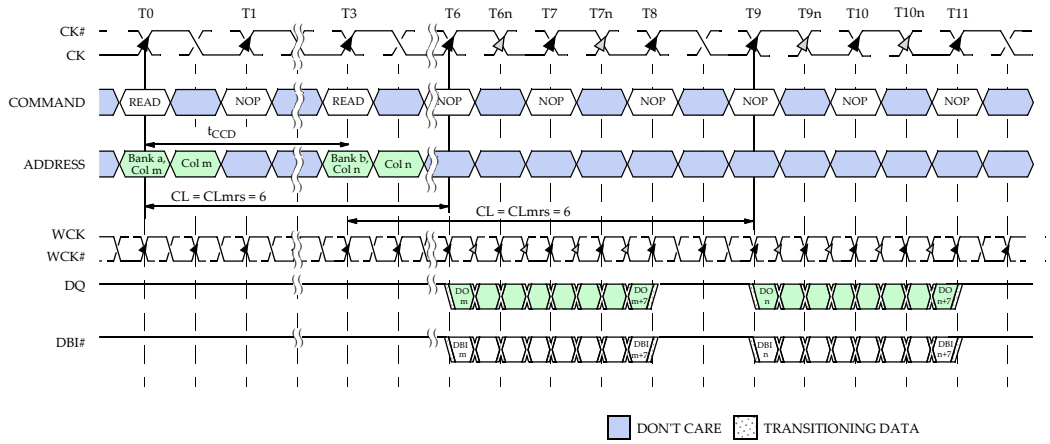
2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

4. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 57. Single READ with EDC

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Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

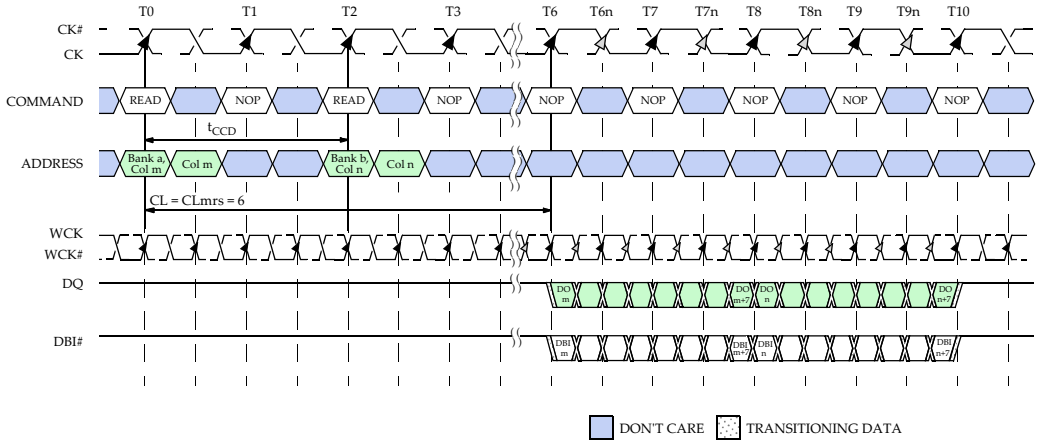
4. t_{CCD} = t_{CCDL} when bank groups are enabled and both READs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 58. Non-Gapless READs

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Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

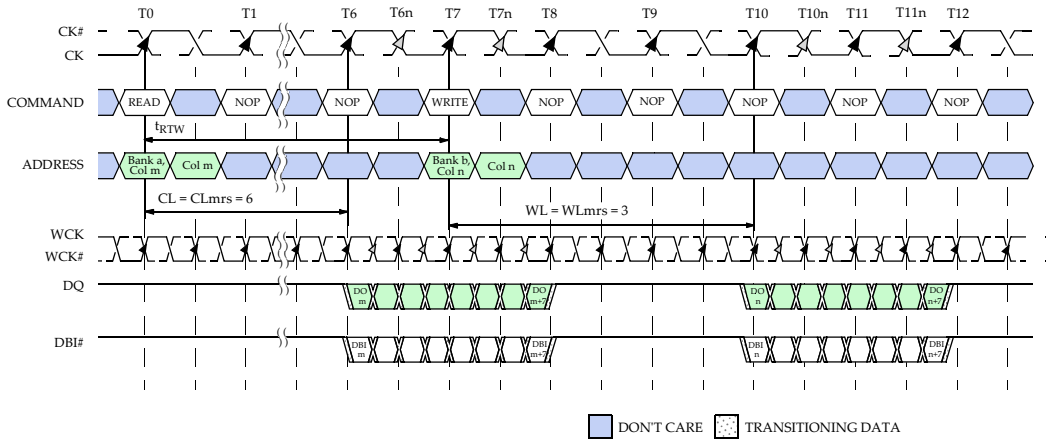
4. $t_{CCD} = t_{CCDS}$ when bank groups are disabled or the second READ is to a different bank group; otherwise $t_{CCD}=t_{CCDL}$.

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 59. Gapless READs

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Notes: 1. WLmrs = 3 and CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. $t_{WTR} = t_{WTRL}$ when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise $t_{WTR}=t_{WTRS}$.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

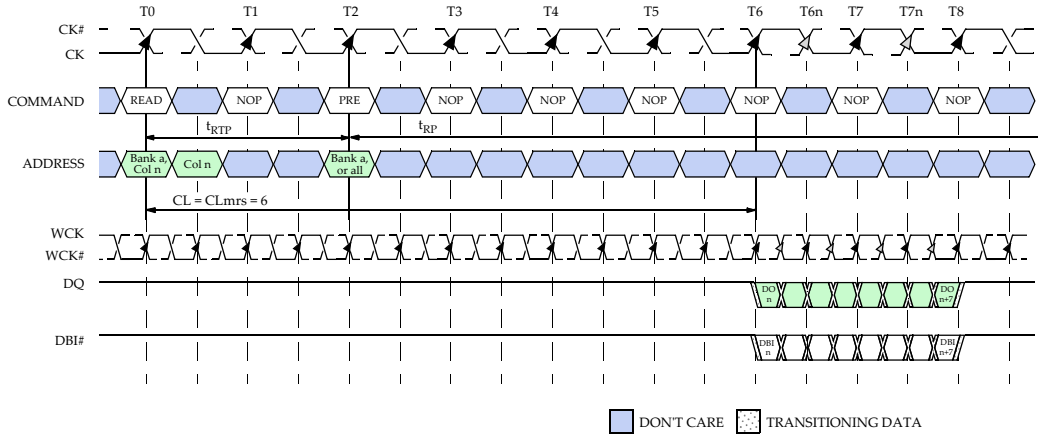
6. Before the READ and WRITE commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} or t_{RCDWR} respectively must be met.

7. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 60. READ to WRITE

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Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. $t_{RTP} = t_{RTPL}$ when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise $t_{RTP} = t_{RTPS}$.

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

6. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 61. READ to PRECHARGE

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5.10. DQ PREAMBLE

DQ preamble is a feature for GDDR5 SGRAMs that is used for READ data. DQ preamble conditions the DQs for better signal integrity on the initial data of a burst.

Once enabled by bit 5 in MR7, the DQ preamble will precede all READ bursts, including non-consecutive READ bursts with a minimum gap of 1 t_{CK}, as shown in Figure 58. When enabled, the DQ preamble pattern applies to all DQ and DBI# pins in a byte, and the same pattern is used for all bytes as shown in Figure62. DQ preamble is enabled or disabled for all bytes. The EDC pin in each byte is not included in the DQ preamble. If ODT is enabled, the ODT is disabled 1 t_{CK} before the start of the preamble pattern as shown in Figure 63.

The preamble pattern on the DBI# pin is only enabled if the MR for RDBI is enabled (MR1 A8 bit). During the preamble the DBI# pin is treated as another DQ pin and the preamble pattern on the DQs is not encoded with RDBI. If RDBI is disabled, then the DBI# pin drives ODT.

Byte 0	Byte 1	Byte 2	Byte 3	Idle				Preamble				Burst							
DQ7	DQ15	DQ23	DQ31	1	1	1	1	0	1	0	1	x	x	x	x	x	x	x	x
DQ6	DQ14	DQ22	DQ30	1	1	1	1	1	0	1	0	x	x	x	x	x	x	x	x
DQ5	DQ13	DQ21	DQ29	1	1	1	1	0	1	0	1	x	x	x	x	x	x	x	x
DQ4	DQ12	DQ20	DQ28	1	1	1	1	1	0	1	0	x	x	x	x	x	x	x	x
DQ3	DQ11	DQ19	DQ27	1	1	1	1	0	1	0	1	x	x	x	x	x	x	x	x
DQ2	DQ10	DQ18	DQ26	1	1	1	1	1	0	1	0	x	x	x	x	x	x	x	x
DQ1	DQ9	DQ17	DQ25	1	1	1	1	0	1	0	1	x	x	x	x	x	x	x	x
DQ0	DQ8	DQ16	DQ24	1	1	1	1	1	0	1	0	x	x	x	x	x	x	x	x
DBI0#	DBI1#	DBI2#	DBI3#	1	1	1	1	0	1	0	1	x	x	x	x	x	x	x	x
			Max 0's	0	0	0	0	5	4	5	4	4	4	4	4	4	4	4	4

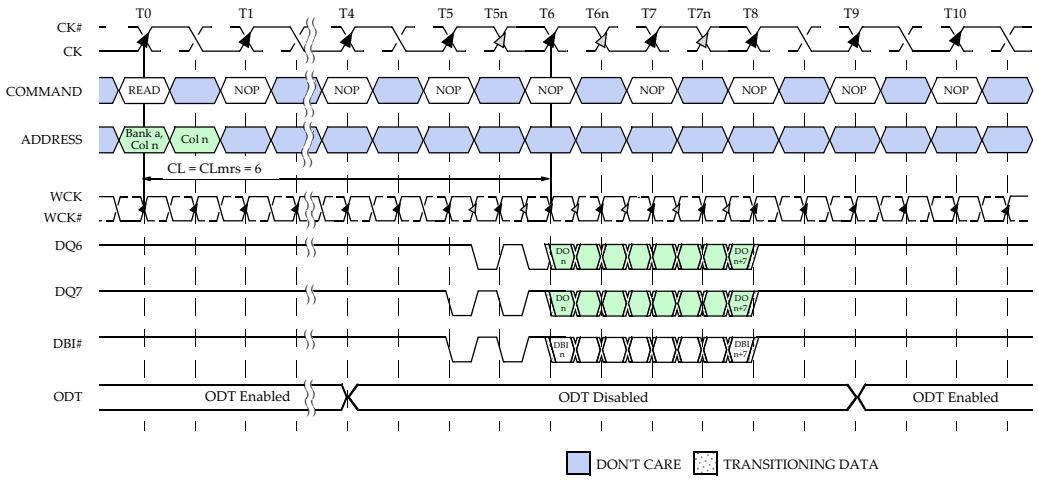
Time →

Notes:
1) The number of Max 0's in the burst is 4 only if RDBI is enabled. Max 0's is on a per byte basis and does not include the EDC pin.
2) x = Valid Data

Figure 62. DQ Preamble Pattern

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Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 4 for EDC Timing.

4. DQ6, DQ7 and the DBI# pin are shown to illustrate the DQ preamble pattern. RDBI is Enabled (MR1 A8=0).

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.

6. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 63. Preamble Timing Diagram

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5.11. READ and WRITE DATA BUS INVERSION (DBI)

The GDDR5 SGRAM Data Bus Inversion (DBIdc) reduces the DC power consumption on data pins, as the number of DQ lines driving a low level can be limited to 4 within a byte. DBIdc is evaluated per byte.

There is one DBI# pin per byte: DBI0# is associated with DQ0-DQ7, DBI1# with DQ8-DQ15, DBI2# with DQ16-DQ23 and DBI3# with DQ24-DQ31.

The DBI# pins are bidirectional active Low double data rate (DDR) signals. For Writes, they are sampled by the GDDR5 SGRAM along with the DQ of the same byte. For Reads, they are driven by the GDDR5 SGRAM along with the DQ of the same byte.

Once enabled by the corresponding RDBI Mode Register bit, the GDDR5 SGRAM inverts read data and sets DBI# Low, when the number of '0' data bits within a byte is greater than 4; otherwise the GDDR5 SGRAM does not invert the read data and sets DBI# High, as shown in Figure 64.

Once enabled by the corresponding WDBI Mode Register bit, the GDDR5 SGRAM inverts write data received on the DQ inputs in case DBI# was sampled Low, or leaves the data non-inverted in case DBI# was sampled High, as shown in Figure 65.

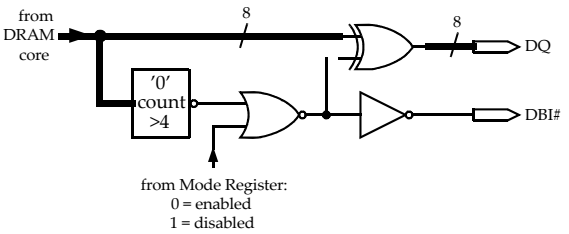


Figure 64. Example of Data Bus Inversion Logic for READs

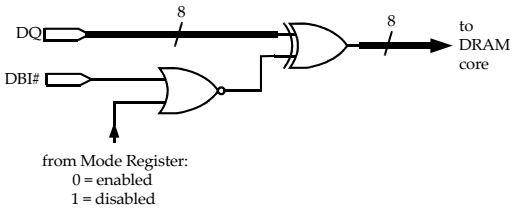


Figure 65. Example of Data Bus Inversion Logic for WRITEs

The flow diagram in Figure 66 illustrates the DBIdc operation. In any case, the transmitter (the controller for WRITEs, the GDDR5 SGRAM for READs) decides whether to invert or not invert the data conveyed on the DQs. The receiver (the GDDR5 SGRAM for WRITEs, the controller for READs) has to perform the reverse operation based on the level on the DBI# pin. Data input and output timing parameters are only valid with DBI being enabled and a maximum of 4 data lines per byte driven Low.

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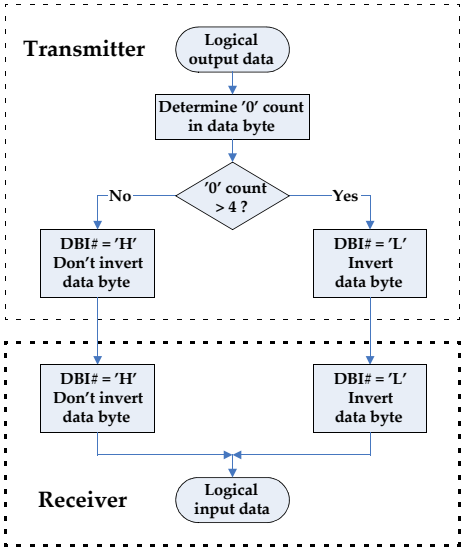


Figure 66. DBI Flow Diagram

DBI# Pin Special Function Overview

The DBI# pin has special behavior compared to DQ pins because of the ability to enable and disable it via MRS. For either WRITE or READ DBI# pin training, both DBI READ and DBI WRITE in MRS must be enabled. The behavior of the DBI# pin in various mode register settings is summarized below:

If both DBI READ and DBI WRITE are enabled:

- Pin drives DBI FIFO data with RDTR command
- DBI# pin FIFO accepts WRTR data with the WRTR command

If only DBI READ is enabled:

- DBI# pin drives ODT when not READ or RDTR

If only DBI WRITE is enabled:

- Pin always drives ODT (unless RESET)

If both DBI READ and DBI WRITE are disabled:

- DBI# pin drives ODT (unless RESET)

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5.12. ERROR DETECTION CODE (EDC)

The GDDR5 SGRAM provides error detection on the data bus to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The GDDR5 SGRAM itself does not perform any error correction. The features of the EDC are:

- 8 bit checksum on 72 bits (9 channels x 8 bit burst)
- dedicated EDC transfer pin per 9 channels (4x per GDDR5 SGRAM)
- asymmetrical latencies on EDC transfer for Reads and Writes

The CRC polynomial used by the GDDR5 SGRAM is an ATM-8 HEC, X^8+X^2+X^1+1. The starting seed value is set in hardware at "zero". Table 24 shows the error types that are detectable and the detection rate.

Table 24 Error Correction Details

Error Type	Detection Rate
Random Single Bit	100%
Random Double Bit	100%
Random Odd Count	100%
Burst <= 8	100%

The bit ordering calculation for the CRC error detection is optimized for errors in the time burst direction. Figure 67 shows the bit orientation on a byte lane basis.

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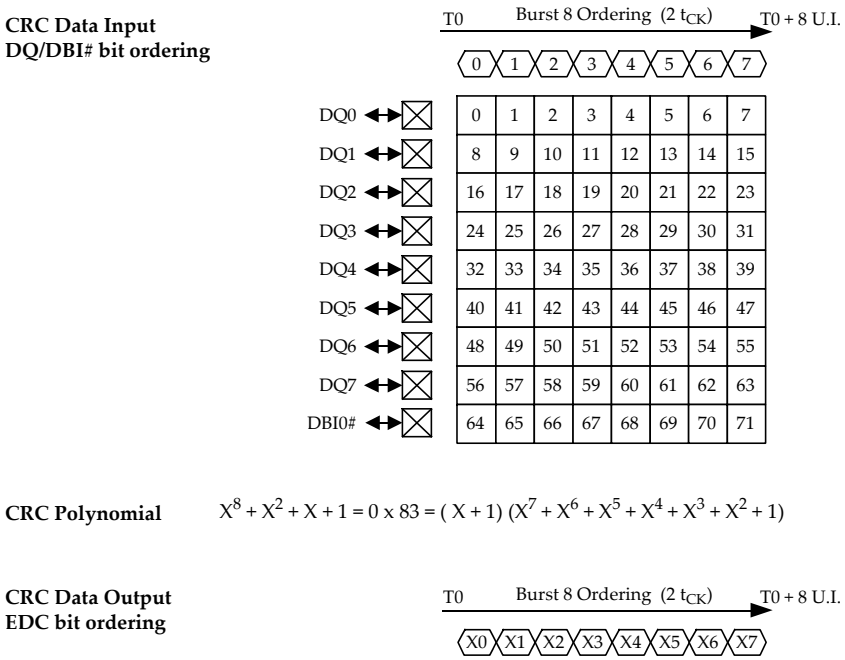


Figure 67. EDC Calculation matrix

The CRC calculation is embedded into the WRITE and READ data stream as shown in Figure 16:

- for WRITEs, the CRC checksum is calculated on the DQ and DBI# input data before decoding with DBI
- for READs, the CRC checksum is calculated on the DQ and DBI# output data after encoding with DBI

The bit ordering is optimized for errors in the time burst direction. Figure 67 shows the bit orientation on a byte lane basis. All '1s' are assumed in the calculation for the DBI# in burst in case DBI is disabled for WRITEs or READs in the Mode Register.

The CRC calculation is also not affected by any data mask sent along with WDM, WDMA, WSM or WSMA commands.

The EDC latency is based on the CAS latency for READ data and the WRITE latency for WRITE data. Table 25 shows the 2 timing parameters associated with the EDC scheme.

Mode Register 4 is used to determine the functionality of the EDC pin. Register bits A9 and A10 control the GDDR5 SGRAM's CRC calculation independently for READs and WRITEs. With EDC off, the calculated CRC pattern will be replaced by the EDC hold pattern defined in Mode Register bits A0 - A3. See "Mode Registers on page 39" section for more details.

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Table 25 EDC Timing

Description	Parameter	Value	Units
EDC READ Latency	t_{EDCRL}	CL + CRCRL	t_{CK}
EDC WRITE Latency	t_{EDCWL}	WL + CRCWL	t_{CK}

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EDC Pin Special Function Overview

The EDC pin is used for many different functions. The behavior of the EDC pin in various modes is summarized in Table 26.

Table 26 EDC Pin Behavior

Device Status	Condition	EDC0-EDC3 Pin Status
Device Power-up	RESET# = LOW	Hi-Z
	RESET# = HIGH; no WCK clocks	High
	RESET# = HIGH; stable WCK clocks	EDC hold pattern (default = '1111')
WCK2CK Training	WCK is sampled High	EDC hold pattern ('1111')
	WCK is sampled Low	Inverted EDC hold pattern ('0000')
Idle	EDC13inv MR4 A11=0	EDC hold pattern
	EDC13inv MR4 A11=1	EDC0, EDC2: EDC hold pattern EDC1, EDC3: inverted EDC hold pattern
WRITE Burst	WRCRC on	CRC data
	WRCRC off	EDC hold pattern
READ or RDTR burst	RDCRC on	CRC data
	RDCRC off	EDC hold pattern
LDFF	WRCRC + RDCRC both on or both off	EDC hold pattern
WRTR burst	-	EDC hold pattern
Power-Down	WCK enabled (MR5 A1=0)	EDC hold pattern
	WCK disabled during Power-Down using MR5 A1=1	High
Self Refresh	-	High
Read Burst in RDQS Mode	MR3 A5=1	Fixed '1010' strobe pattern with 4 U.I. preamble
READ burst in RDQS Mode with RDQS pseudo-differential	MR3 A5=1; EDC13inv MR4 A11=1	EDC0, EDC2: Fixed '1010' strobe pattern with 4 U.I. preamble EDC1, EDC3: Fixed '0101' strobe pattern with 4 U.I. preamble

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5.13. PRECHARGE

The PRECHARGE command (see Figure 68) is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREALL). The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued as illustrated in Figure 39.

Input A8 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0-BA3 select the bank. Otherwise BA0-BA3 are treated as "Don't Care".

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging. Sequences of PRECHARGE commands must be spaced by at least t_{PPD} as shown in Figure 69.

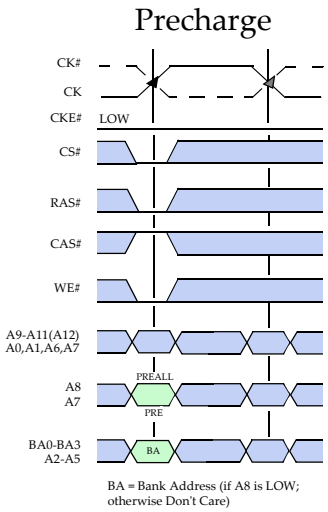


Figure 68. PRECHARGE command

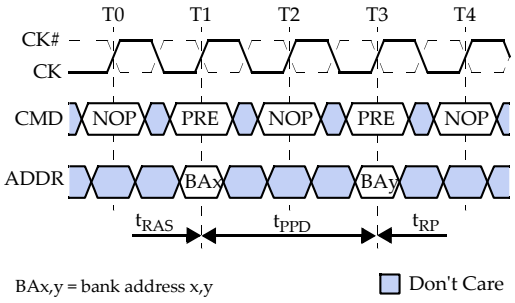


Figure 69. Precharge to Precharge Timings

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5.14. AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A8 (A8 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the OPERATION section of this specification.

5.15. REFRESH

The REFRESH command is used during normal operation of the GDDR5 SGRAM. The command is non persistent, so it must be issued each time a refresh is required. A minimum time t_{RFC} is required between two REFRESH commands. The same rule applies to any access command after the refresh operation. All banks must be precharged prior to the REFRESH command.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a REFRESH command. The GDDR5 SGRAM requires REFRESH cycles at an average periodic interval of t_{REFI}(max). The values of t_{REFI} for different densities are listed in Table 6. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to the GDDR5 SGRAM, and the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * t_{REFI}.

During REFRESH, and when bit A2 in MR5 is set to 0, WRTR, RDTR, and LDFF commands are allowed at time t_{REFTR} after the REFRESH command, which enable (incremental) data training to occur in parallel with the internal refresh operation and thus without loss of performance on the interface. See READ Training and WRITE Training for details.

As impedance updates from the auto-calibration engine may occur with any REFRESH command, it is safe to only issue NOP commands during t_{KO} period to prevent false command, address or data latching resulting from impedance updates.

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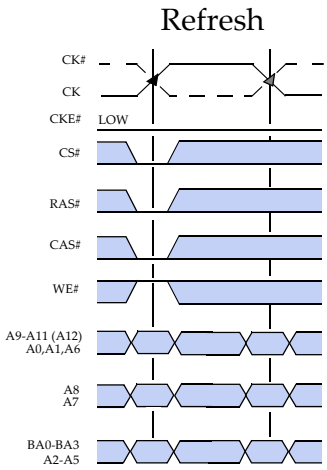
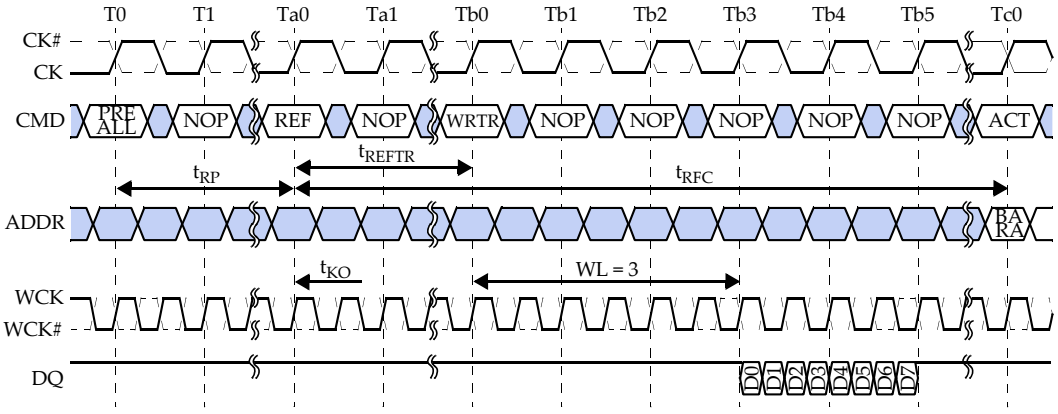


Figure 70. REFRESH command



BA = bank address; RA = row address

WRTR and RDTR commands are allowed during refresh unless disabled in the Mode Register

WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

Figure 71. Refresh Timings

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5.16. SELF-REFRESH

Self-Refresh can be used to retain data in the GDDR5 SGRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the GDDR5 SGRAM retains data without external clocking. The SELF REFRESH ENTRY command (see Figure 72) is initiated like a REFRESH command except that CKE# is pulled HIGH. SELF REFRESH ENTRY is only allowed when all banks are precharged with t_{RP} satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command have been pushed out (t_{RDSRE}). NOP commands are required until t_{CKSRE} is met after the entering Self-Refresh. The PLL is automatically disabled upon entering Self-Refresh and is automatically enabled and reset upon exiting Self-Refresh. If the GDDR5 SGRAM enters Self-Refresh with the PLL disabled, it will exit Self-Refresh with the PLL disabled.

Once the SELF REFRESH ENTRY command is registered, CKE# must be held HIGH to keep the device in Self-Refresh mode. When the device has entered the Self-Refresh mode, all external control signals, except CKE# and RESET# are "Don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFC, VREFD) must be at valid levels. The GDDR5 SGRAM initiates a minimum of one internal refresh within t_{CKE} period once it enters Self-Refresh mode. The address, command, data and WCK pins are in ODT state, and the EDC pins drive a HIGH.

The clock is internally disabled during Self-Refresh operation to save power. The minimum time that the GDDR5 SGRAM must remain in Self-Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external CK and WCK clocks t_{CKSRE} after Self-Refresh entry is registered. However, the clocks must be restarted and stable t_{CKSRX} before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the CK and WCK clocks must be stable prior to CKE# going back LOW. A delay of at least t_{XSNRW} must be satisfied before a valid command not requiring a locked PLL can be issued to the device to allow for completion of any internal refresh in progress. Before a command requiring a locked PLL can be applied, a delay of at least t_{XSRW} must be satisfied.

During Self-Refresh the on-die termination (ODT) and driver will not be auto-calibrated. Therefore, it is recommended that the ODT and driver be recalibrated by the controller upon exiting Self-Refresh. Alternatively, if changes in voltage and temperature are tracked or known to be bounded then the provided Voltage and Temperature Variation tables may be consulted to determine if recalibration is necessary.

Upon exit from Self-Refresh, the GDDR5 SGRAM can be put back into Self-Refresh mode after waiting at least t_{XSNRW} period and issuing one extra REFRESH command.

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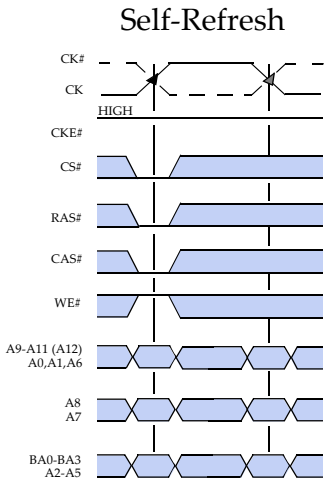
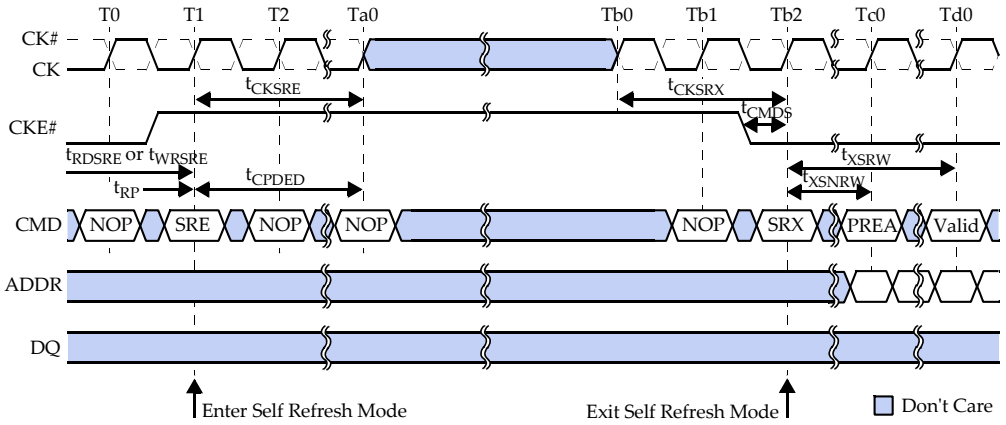


Figure 72. SELF REFRESH Entry Command



Self refresh exit requires WCK2CK training prior to any WRITE or READ operation
At least one REFRESH command shall be issued after t_{XSNRW} for output driver and termination impedance updates.

Figure 73. Self Refresh Entry and Exit

Note:
1. Clock(CK and CK#) must be stable before exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. t_{XSNRW} is required before any non-READ or WRITE command can be applied, and t_{XSRW} is required before a READ or WRITE command can be applied.
4. REF = REFRESH command.

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Table 27 Pin States During Self Refresh

Pin	State
EDC	High
DQ/DBI#	ODT
ADR/CMD	ODT
CKE#	ODT (Driven High by Controller)
WCK/WCK#	ODT

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5.17. POWER-DOWN

GDDR5 SGRAMs requires CKE# to be LOW at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined as when the last data element including CRC has been transmitted on the DQ outputs, for WRITEs, a burst completion is defined as when the last data element has been written to the memory array and CRC data has been returned to the controller.

POWER-DOWN is entered when CKE# is registered HIGH. If POWER-DOWN occurs when all banks are idle, this mode is referred to as precharge POWER-DOWN; if POWER-DOWN occurs when there is a row active in any bank, this mode is referred to as active POWER-DOWN. Entering POWER-DOWN deactivates the input and output buffers, excluding CK, CK#, WCK, WCK#, EDC pins and CKE#.

For maximum power savings, the user has the option of disabling the PLL prior to entering POWER-DOWN. In that case, on exiting POWER-DOWN, WCK2CK training is required to set the internal synchronizers which will include the enabling of the PLL, PLL reset, and t_{LK} clock cycles must occur before any READ or WRITE command can be issued.

While in power-down, CKE# HIGH and stable CK and WCK signals must be maintained at the device inputs. The EDC pins continuously drive the EDC hold pattern; if the controller does not require CDR, users may program the EDC hold pattern to '1111' prior to entering power-down mode. POWER-DOWN duration is limited by the refresh requirements of the device.

The POWER-DOWN state is synchronously exited when CKE# is registered LOW (in conjunction with a NOP or DESELECT command). A valid executable command may be applied t_{XPN} cycles later. The min. power-down duration is specified by t_{PD}.

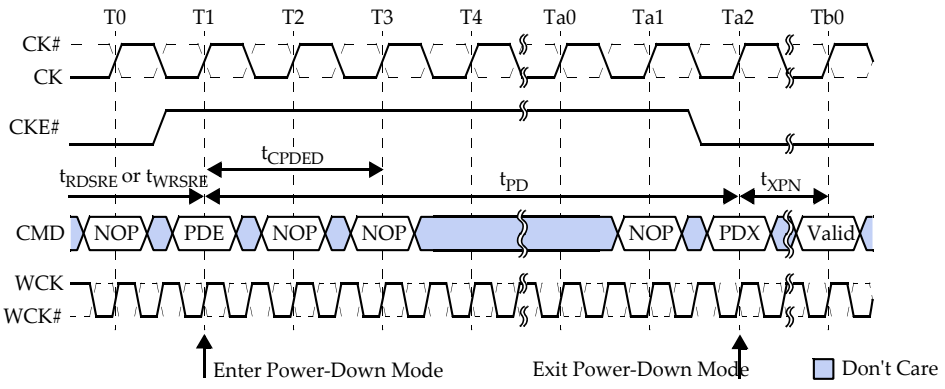


Figure 74. Power-Down Entry and Exit

Note:
1. Minimum CKE# pulse width must satisfy t_{CKE}.
2. After issuing Power-Down command, two more NOPs should be issued.

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Table 28 Pin States During Power Down

Pin	LP2	State
EDC	WCK	'Hold'
	no WCK	High
DQ/DBI#	x	ODT
ADR/CMD	x	ODT
CKE#	x	ODT (Driven High by Controller)
WCK/WCK#	x	ODT

5.18. COMMAND TRUTH TABLES

Table 29 Truth Table – CKE#

CKE#*n-1*	CKE#*n*	CURRENT STATE	COMMAND*n*	ACTION*n*	NOTES
H	H	Power-Down	X	Maintain Power-Down	
H	H	Self Refresh	X	Maintain Self Refresh	
H	L	Power-Down	DESELECT or NOP	Exit Power-Down	
H	L	Self Refresh	DESELECT or NOP	Exit Self Refresh	5
L	H	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
L	H	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
L	H	All Banks Idle	REFRESH	Self Refresh Entry	
L	L		See <Link>Table 30 and <Link>Table 31		1, 2, 3

Notes:
1. CKE#*n* is the logic state of CKE# at clock edge *n*; CKE#*n-1* was the state of CKE# at the previous clock edge.
2. Current state is the state of the GDDR5 SGRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge *n*, and ACTION*n* is a result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSRW} period. A minimum of t_{LK} is needed for the PLL to lock before applying a READ or WRITE command if the PLL was disabled.

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Table 30 Truth Table – Current State Bank *n* – Command To Bank *n*

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH	4
	L	L	L	L	MODE REGISTER SET	4
Row Active	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	5
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	6, 8
	L	L	H	L	PRECHARGE (only after the READ burst is complete	5
Write (Auto Precharge Disabled) (WOM, WSM or WDM)	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE (only after the WRITE burst is complete)	5, 7

Notes
1. This table applies when CKE#*n-1* was LOW and CKE#*n* is LOW (see <Link>Table 29) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled.
   Write: A WRITE burst has been initiated, with auto precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and <Link>Table 30, and according to <Link>Table 31.
   Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the "row active" state.
   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of a REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the GDDR5 SGRAM will be in the all banks idle state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the GDDR5 SGRAM will be in the all banks idle state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.
   READ or WRITE: Starts with the registration of the ACTIVE command and ends the last valid data nibble.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.

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9. Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.
10. A WRITE command may be applied after the completion of the READ burst

Table 31 Truth Table – Current State Bank *n* – Command To Bank *m*

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE	
Read (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE	
Write (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	6
	L	L	H	L	PRECHARGE	

Notes
1. This table applies when CKE#*n-1* was LOW and CKE#*n* is LOW (see <Link>Table 30) and after t_{XSNR} has been met (if the previous state was self refresh).
2. WRITE in this table refers to both WOM/WOMA, WSM/WSMA and WDM/WDMA commands
3. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
4. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled.
   Write: A WRITE burst has been initiated, with auto precharge disabled.
   Read with Auto Precharge Enabled: See following text
   Write with Auto Precharge Enabled: See following text

4a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was

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executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

4b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

5. REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

Table 32 Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE with AUTO PRECHARGE (WOMA)	READ or READ with AUTO PRECHARGE	[WLmrs + (BL/4)] t_{CK} + t_{WTRL} ***
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	2 * t_{CK}
	PRECHARGE	1 t_{CK}
	ACTIVE	1 t_{CK}
WRITE with AUTO PRECHARGE (WDMA)	READ or READ with AUTO PRECHARGE	[WL + (BL/4)] t_{CK} + t_{WTR} ***
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	2 * t_{CK}
	PRECHARGE	2 t_{CK}
	ACTIVE	2 t_{CK}
WRITE with AUTO PRECHARGE (WSMA)	READ or READ with AUTO PRECHARGE	[WL + (BL/4)] t_{CK} + t_{WTR} ***
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	3 * t_{CK}
	PRECHARGE	3 t_{CK}
	ACTIVE	3 t_{CK}
READ with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	2 * t_{CK}
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/ WDMA)	[CLmrs + (BL/4) + 2 - WL] * t_{CK} ***
	PRECHARGE	1 t_{CK}
	ACTIVE	1 t_{CK}

*** CL = CAS latency (CL)
BL = Burst length
WL = WRITE latency
t_{WTR} = t_{WTRL} if Bank Groups enabled and access to the same bank otherwise t_{WTR}=t_{WTRS}

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5.19. RDQS MODE

For device operation at lower clock frequencies the GDDR5 SGRAM may be set into RDQS mode in which a READ DATA STROBE (RDQS) in the style of GDDR4 will be sent on the EDC pins along with the READ data. The controller will use the RDQS to latch the READ data.

RDQS mode is entered by setting the RDQS Mode bit A5 in Mode Register 3 (MR3). When the bit is set, the GDDR5 SGRAM will asynchronously terminate any EDC hold pattern and drive a logic HIGH after t_{MRD} at the latest. All features controlled by MR4 are ignored by RDQS mode.

READ commands are executed as in normal mode regarding command to data out delay and programmed READ latencies. A fixed clock-like pattern as shown in Figure 75 is driven on EDC pins in phase (edge aligned) with the DQ. Prior to the first valid data element, this fixed clock-like pattern or READ preamble is driven for 2 t_{WCK}.

No CRC is calculated in RDQS mode, neither for READs nor for WRITEs. The CRC engine is effectively disabled, and the corresponding WRCRC and RDCRC Mode Register bits are ignored. The PLL may be on or off with RDQS mode, depending on system considerations and the PLL's minimum clock frequency.

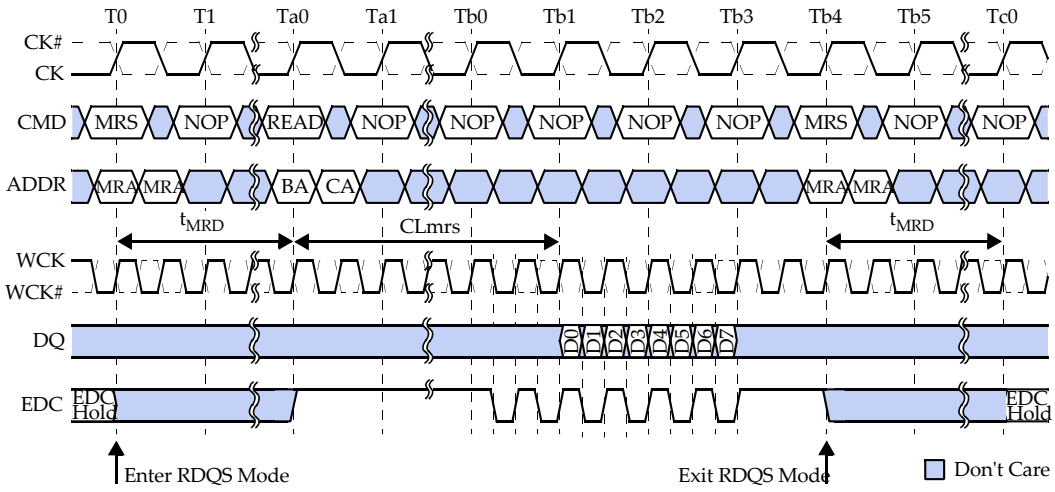
There is no equivalent WDQS mode; WRITE commands to the GDDR5 SGRAM are not affected by RDQS mode.

RDQS mode is exited by resetting the RDQS Mode bit. In this case the GDDR5 SGRAM will asynchronously start driving the EDC hold pattern after t_{MRD}.

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The WCK2CK training should be performed prior to entering RDQS mode. No WCK2CK training can be done when the RDQS mode is active.



1. MRA = Mode Register address and opcode; BA = bank address; CA = column address
2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the GDDR5 SGRAM and t_{RCDRD} must be met.
4. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 75. RDQS Mode Timings

EDC1 and EDC3 can be treated as pseudo-differential to EDC0 and EDC2 respectively, by setting the EDC13Inv field, bit A11 in MR4, as shown in Table 34.

Table 33 EDC pin behavior in RDQS mode including pseudo-differential RDQS

MRS Set			READ/RDTR		NOP (except RD/RDTR/ PDN/SRF)	POWER-DOWN/SELF REFRESH
RDQS Mode	WCK2CK Training	EDC13 Invert	EDC02 Output	EDC13 Output	EDC0123 Output	EDC0123 Output
On	Off	Off	RDQS	RDQS	1111	High
		On	RDQS	Inverted RDQS	1111	High

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5.20. CLOCK FREQUENCY CHANGE SEQUENCE

Step 1) Wait until all commands have finished, all banks are idle.

Step 2) Send NOP or DESELECT (must meet setup/hold relative to clock while clock is changing) to GDDR5 SGRAM for the entire sequence unless stated to do otherwise. The user must take care of refresh requirements.

Step 3) If the new desired clock frequency is below the min frequency supported by PLL-on mode, turn the PLL off via an MRS command.

Step 4) Change the clock frequency and wait until clock is stabilized.

Step 5) If the new clock frequency is within the PLL on range and the PLL on state is desired, enable the PLL via an MRS Command if it is not already enabled.

Step 6) Perform address training if required.

Step 7) Perform WCK2CK training. As defined in the WCK2CK training process, if the PLL is enabled, then complete steps 7a and 7b:

7a) Reset the PLL by writing to the MRS register.

7b) Wait t_{LK} clock cycles before issuing any commands to the GDDR5 SGRAM.

Step 8) Exit WCK2CK training.

Step 9) Perform READ and WRITE training, if required.

Step 10) GDDR5 SGRAM is ready for normal operation after any necessary interface training.

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5.21. DYNAMIC VOLTAGE SWITCHING (DVS)

GDDR5 SGRAM's allow the supply voltage to be changed during the course of normal operation using the GDDR5 Dynamic Voltage Switching (DVS) feature. By using DVS the GDDR5 SGRAM's power consumption can be reduced whenever only a fraction of the maximum available bandwidth is required by the current work load.

DVS requires the GDDR5 SGRAM to be properly placed into self refresh before the voltage is changed from the exising stable voltage, $V_{original}$ to the new desired voltage V_{new} . The DVS procedure may also require changes to the VDD Range mode register using MR7 bits A8 and A9, depending on whether the feature is supported. The datasheet shall be consulted regarding the supported supply voltages for DVS, and any dependencies of AC timing parameters on the selected supply voltage.

Clock frequency changes can also take place before or after entering self refresh mode using the standard Clock Frequency Change procedure. A clock frequency change in conjunction with DVS is required if t_{CK} is less than t_{CK}min supported by V_{new} . In this case normal device operation including self refresh exit is not guaranteed without a frequency change. Changing the frequency while in self refresh is the most safe procedure.

Once self refresh is entered, t_{CKSRE} must be met before the supply voltage is allowed to transition from $V_{original}$ to V_{new}. After VDD and VDDQ are stable at V_{new}, t_{VS} must be met to allow for internal voltages in the GDDR5 SGRAM to stabilize before self refresh mode may be exited. During the voltage transition the voltage must not go below V_{min} of the lower voltage of either $V_{original}$ or V_{new} in order to prevent false chip reset. V_{min} is the minimum voltage allowed by VDD or VDDQ in the DC operating conditions table. VREF shall continue to track VDDQ.

DVS Procedure

Step 1) Complete all operations and precharge all banks.

Step 2) Issue an MRS command to set VDD Range to proper values for V_{new}. This step is only required when the VDD Range mode register field is supported by the GDDR5 SGRAM.

Step 3) Enter self refresh mode. Self refresh entry procedure must be met.

Step 4) Wait required time t_{CKSRE} before changing voltage to V_{new}.

Step 5) Change VDD and VDDQ to V_{new}.

Step 6) Wait required time t_{VS} for voltage stabilization.

Step 7) Exit self refresh. The self refresh exit procedure must be met.

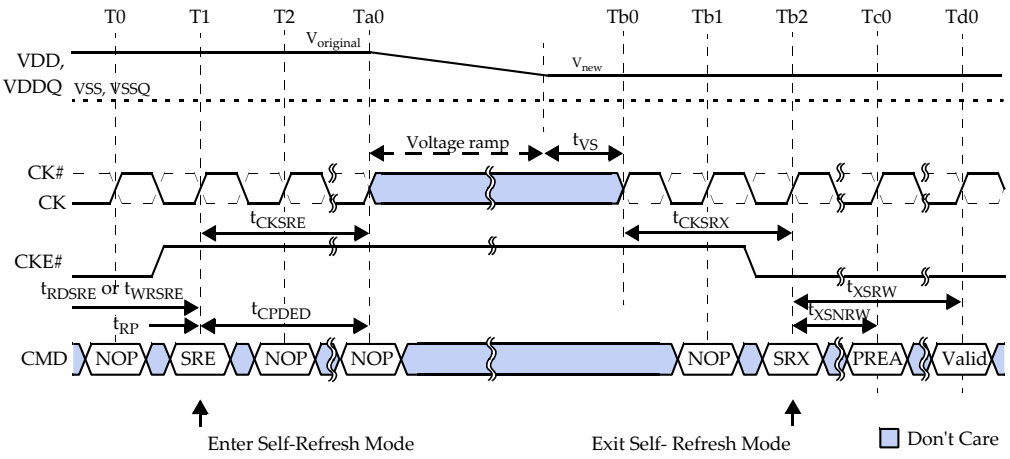
Step 8) Issue MRS commands to adjust mode register settings as desired (e.g. latencies, PLL on/off, CRC on/off, RDQS mode on/off).

Step 9) Perform any interface training as required.

Step 10) Continue normal operation.

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Self refresh exit requires WCK2CK training prior to any WRITE or READ operation
At least one REFRESH command shall be issued after t_{XSNRW} for output driver and termination impedance updates
$V_{original} > V_{new}$ shown as an example of a voltage change

Figure 76. DVS Sequence

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5.22. TEMPERATURE SENSOR

GDDR5 SGRAMs incorporate a temperature sensor with digital temperature readout function. This function allows the controller to monitor the GDDR5 SGRAM die's junction temperature and use this information to make sure the device is operated within the specified temperature range or to adjust interface timings relative to temperature changes over time.

The temperature sensor is enabled by bit A6 in Mode Register 7 (MR7). In this case the temperature readout is valid after t_{TSEN}. Hynix applies 10us to t_{TSEN}.

The temperature readout uses the DRAM Info mode feature. The digital value is driven asynchronously on the DQ bus following the MRS command to Mode Register 3 (MR3) that sets bit A7 to 1 and bit A6 to 0. The temperature readout will be continuously driven until an MRS command sets both bits to 0.

The GDDR5 SGRAM's junction temperature is linearly encoded as shown in Table 35. Hynix has the readout to a subset of six digital codes out of Table 35, corresponding to six temperature thresholds.

Table 34 Temperature Sensor Readout Pattern

Temperature [°C]	Binary Temperature Readout MF=0: DQ[5:0] MF=1: DQ[31:26]
< 45	000000
55	000001
65	000011
75	000111
85	001111
95	011111
> 95	111111

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5.23. DUTY CYCLE CORRECTOR (DCC)

As GDDR5 SGRAMs can operate with the PLL off during normal operation, the use of a Duty Cycle Corrector (DCC) can correct for the duty cycle of the WCK. DCC can be used at any time, however, rising and falling edges of WCK can be shifted according to the DCC type. The DCC should be enabled before WCK training and should be run for t_{DCC} in order to effectively correct any error.

Table 35 DCC Timings

Parameter	Symbol	Min	Max	Unit
Required time for duty cycle corrector	t_{DCC}	150	-	tCK

DCC can correct the duty cycle error within the range of ± 100ps.

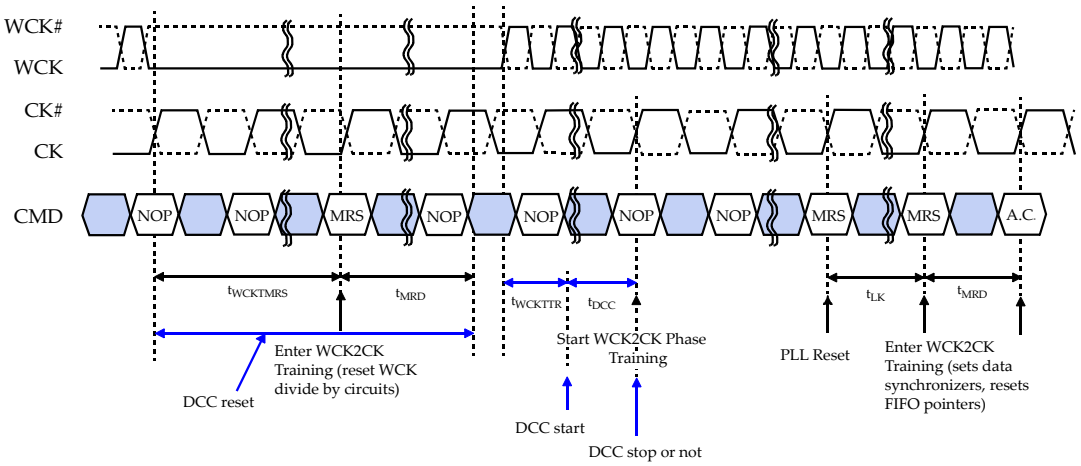


Figure 77. Timing Diagram of DCC Control Signals

DCC control signals

- DCC reset : The DCC reset is used to initialize the DCC code and should be issued anytime before the WCK enables (MRS7 A11:1, A10:0)
- DCC start : The DCC start is used to update the DCC code and should be issued anytime after the WCK is stable (MRS7 A11:0, A10:1)
- DCC stop : The DCC stop is used to make it stop to update the DCC code while the DCC code is held. This should be issued after enough time from DCC start if needs (MRS7 A11:0, A10:0)

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Table 36 DCC Control Signals

A11	A10	DCC
0	0	no DCC & DCC stop
0	1	DCC start
1	0	DCC reset
1	1	RFU

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6. OPERATING CONDITIONS

6.1. ABSOLUTE MAXIMUM RATINGS

Voltage on Vdd Supply
Relative to Vss..... -0.5V to +2.0V
Voltage on VddQ Supply
Relative to Vss ..... -0.5V to +2.0V
Voltage on Vref and Inputs
Relative to Vss ..... -0.5V to +2.0V
Voltage on I/O Pins
Relative to Vss ..... -0.5V to VddQ +0.5V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 37 Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DBI#, EDC, WCK, WCK#	DCio	0	0.5	pF	
Delta Input Capacitance: Command and Address	DCi1	0	0.5	pF	
Delta Input Capacitance: CK, CK#	DCi2	0	0.3	pF	
Input/Output Capacitance: DQs, DBI#, EDC, WCK, WCK#	Cio	1.2	1.9	pF	
Input Capacitance: Command and Address	Ci1	0.9	1.6	pF	
Input Capacitance: CK, CK#, WCK, WCK#	Ci2	0.9	1.6	pF	
Input Capacitance: CKE#	Ci3	0.9	1.6	pF	

Table 38 Thermal Characteristics

Parameter		Description	Value	Units	Notes
Theta_JA	1s	Thermal resistance junction to ambient	45	°C/W	1,2,4,5
			33	°C/W	1,4,5 (at Tc 115°C)
	2s2p		30	°C/W	1,2,4,5
Theta_JB		Thermal resistance junction to board	12	°C/W	1,3
Theta_JC		Thermal resistance junction to case	3	°C/W	1,6

Notes:
1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA measured with the low and high thermal conductivity test board defined in JESD51-9

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3. Theta_JB measured with the special boundary condition defined in JESD51-8
4. Theta_JA should only be used for comparing the thermal performance of single package and not for system related junction.
5. Theta_JA is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure as decribed in JESD 51-2.
   The environment is sometimes refered to as "still-air" although natural convection causes the air to move.
6. Theta_JC case surface is defined as the "outside surface of the package (case) closest to the chip mounting area when that same surface is properly hear sunk" so as to minimize temperature variation across that surface.

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6.2. AC & DC CHARACTERISTICS

All GDDR5 SGRAMs are designed for 1.5V typical voltage supplies. The interface of GDDR5 with 1.5V VDDQ will follow the POD15 specification. All AC and DC values are measured at the ball.

Table 39 DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply Voltage	VDD	1.452	1.6	1.648	V	1
Output Supply Voltage	VDDQ	1.452	1.6	1.648	V	1
Device Supply Voltage	VDD	1.455	1.5	1.545	V	2
Output Supply Voltage	VDDQ	1.455	1.5	1.545	V	2
Reference Voltage for DQ and DBI# pins	VREFD	0.69 * VDDQ		0.71 * VDDQ	V	3, 4
Reference Voltage for DQ and DBI# pins	VREFD2	0.49 * VDDQ		0.51 * VDDQ	V	3, 4, 5
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	V	6
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 0.15			V	
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.15	V	
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD	VIHD (DC)	VREFD + 0.10			V	
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD	VILD (DC)			VREFD - 0.10	V	
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD2	VIHD2 (DC)	VREFD2 + 0.30			V	
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD2	VILD2 (DC)			VREFD2 - 0.30	V	
Input Logic HIGH Voltage for RESET#, SEN, MF	VIHR	VDDQ - 0.50			V	
Input Logic LOW Voltage for RESET#, SEN, MF	VILR			0.30	V	
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3			V	9
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			0.30	V	9
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	II			10	µA	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz			10	µA	
Output Logic LOW Voltage	VOL (DC)			0.62	V	

Notes:
1. VDD/VDDQ 1.6V is for 6Gbps
2. GDDR5 SGRAMs are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.
3. AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
4. Source of Reference Voltage and control of Reference Voltage for DQ and DBI# pins is determined by VREFD, Half VREFD, Auto VREFD, VREFD MERGE and VREFD Offsets mode registers.
5. VREFD Offsets are not supported with VREFD2.
6. External VREFC is to be provided by the controller as there is no other alternative supply.
7. DQ/DBI# input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
8. ADR/CMD input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
9. VIHX and VILX define the voltage levels for the receiver that detects x32 or x16 mode with RESET# going High.

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Table 40 AC Operating Conditions

Parameter	Symbol	POD15			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	VREFC + 0.20			V	
AC Input Logic LOW Voltage for address and command	VILA (AC)			VREFC - 0.20	V	
AC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD	VIHD (AC)	VREFD + 0.15			V	
AC Input Logic LOW Voltage for DQ and DBI# pins with VREFD	VILD (AC)			VREFD - 0.15	V	
AC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD2	VIHD2 (AC)	VREFD2 + 0.40			V	
AC Input Logic LOW Voltage for DQ and DBI# pins with VREFD2	VILD2 (AC)			VREFD2 - 0.40	V	

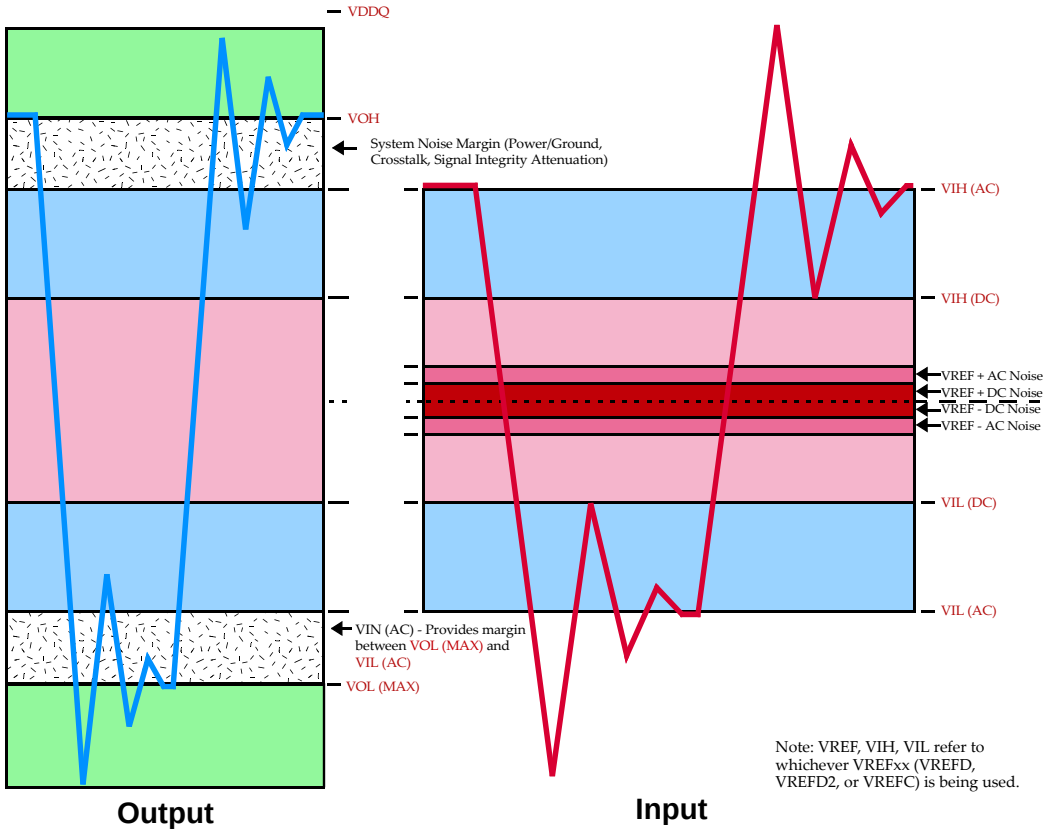


Figure 78. Voltage Waveform

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Table 41 Clock Input Operating Conditions

Parameter	Symbol	POD15		Unit	Note
		Min	Max		
Clock Input Mid-Point Voltage; CK and CK#	VMP (DC)	VREFC - 0.10	VREFC + 0.10	V	1, 6
Clock Input Differential Voltage; CK and CK#	VIDCK (DC)	0.22		V	4, 6
Clock Input Differential Voltage; CK and CK#	VIDCK (AC)	0.40		V	2, 4, 6
Clock Input Differential Voltage; WCK and WCK#	VIDWCK (DC)	0.20		V	5, 7
Clock Input Differential Voltage; WCK and WCK#	VIDWCK (AC)	0.30			2, 5, 7
Clock Input Voltage Level; CK, CK#, WCK and WCK# single ended	VIN	-0.30	VDDQ + 0.30		
CK/CK# Single ended slew rate	CKslew	3		V/ns	9
WCK/WCK# Single ended slew rate	WCKslew	3		V/ns	10
Clock Input Crossing Point Voltage; CK and CK#	VIXCK (AC)	VREFC - 0.12	VREFC + 0.12	V	2, 3, 6
Clock Input Crossing Point Voltage; WCK and WCK#	VIXWCK (AC)	VREFD - 0.10	VREFD + 0.10	V	2, 3, 7, 8
Allowed time before ringback of CK/WCK below VIDCK/WCK(AC)	t_{DVAC}			ps	11, 12, 13

Notes:
1. This provides a minimum of 0.9V to a maximum of 1.2V, and is nominally 70% of VDDQ with POD15. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
4. VIDCK is the magnitude of the difference between the input level in CK and the input level on CK#. The input reference level for signals other than CK and CK# is VREFC.
5. VIDWCK is the magnitude of the difference between the input level in WCK and the input level on WCK#. The input reference level for signals other than WCK and WCK# is either VREFD, VREFD2 or the internal VREFD.
6. The CK and CK# input reference level (for timing referenced to CK and CK#) is the point at which CK and CK# cross. Please refer to the applicable timings in the AC timings table (Table 44).
7. The WCK and WCK# input reference level (for timing referenced to WCK and WCK#) is the point at which WCK and WCK# cross. Please refer to the applicable timings in the AC Timings table (Table 44).
8. VREFD is either VREFD, VREFD2 or the internal VREFD.
9. The slew rate is measured between VREFC crossing and VIXCK(AC).
10. The slew rate is measured between VREFD crossing and VIXWCK(AC).
11. Figure illustrates the exact relationship between (CK-CK#) or (WCK-WCK#) and VID(AC), VID(DC) and tDVAC
12. Ringback below VID(DC) is not allowed.
13. t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.

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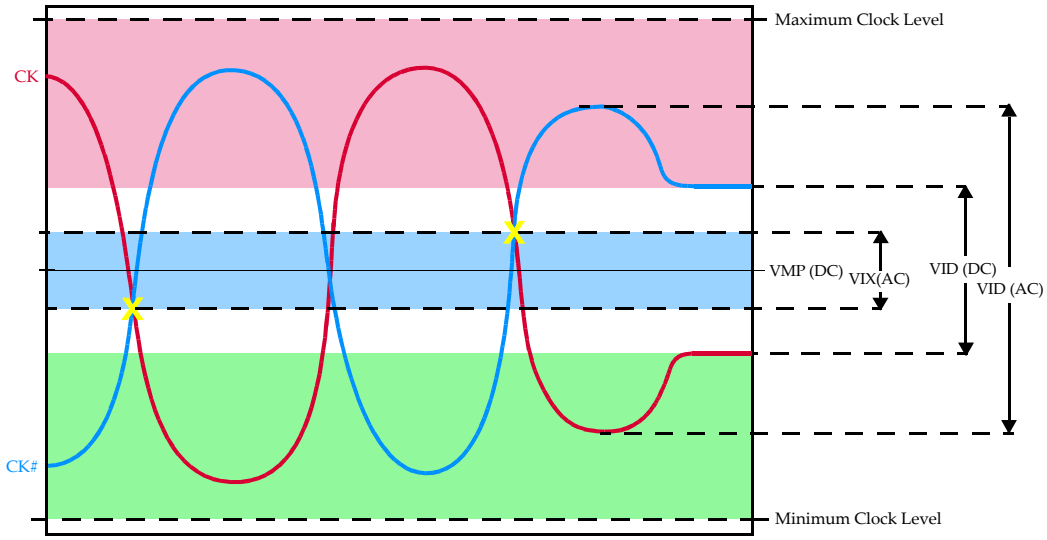


Figure 79. Clock Waveform

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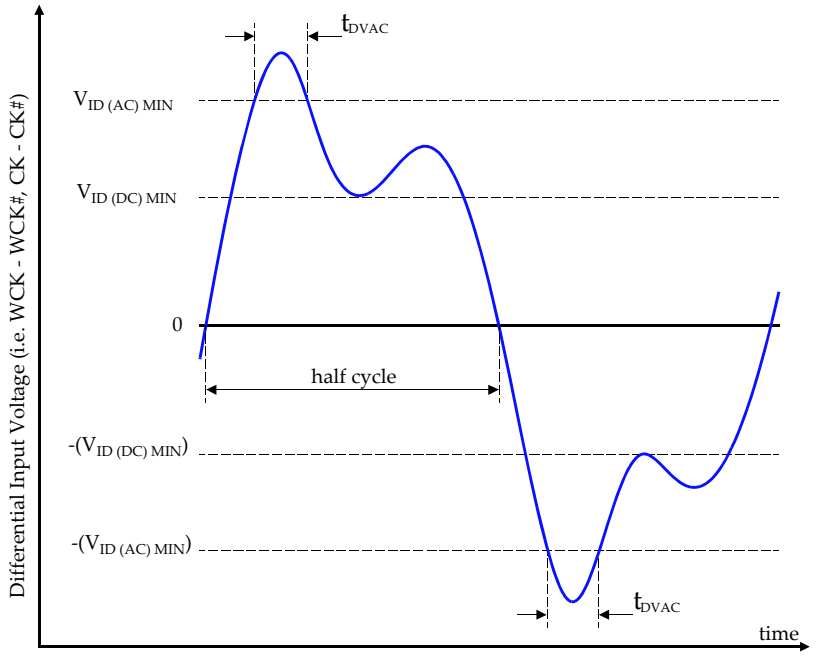


Figure 80. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

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Table 42 IDD Specifications and Test Conditions

PARAMETER/CONDITION	SYMBOL	NOTES
One Bank Activate Precharge Current: $t_{CK} = t_{CK}(min)$; $t_{WCK} = t_{WCK}(min)$; $t_{RC} = t_{RC}(min)$; CKE# = LOW; DQ, DBI# are HIGH; random bank and row addresses (4 address inputs set LOW) with ACT command	IDD0	1
One Bank Activate Read Precharge Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; $t_{RC} = t_{RC}(min)$; CKE# = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, DBI# are HIGH; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ commands; I_{OUT} = 0mA	IDD1	1
Precharge Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; all banks idle; CKE# = HIGH; all other inputs are HIGH; PLLs are off	IDD2P	
Precharge Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; all banks idle; CKE# = LOW; all other inputs are HIGH	IDD2N	
Active Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; one bank active; CKE# = HIGH; all other inputs are HIGH	IDD3P	
Active Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; one bank active; CKE# = LOW; all other inputs are HIGH	IDD3N	
Read Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; CKE# = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank and column addresses (4 address inputs set LOW) with READ command; I_{OUT} = 0mA	IDD4R	
Write Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; CKE# = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; random bank and column addresses (4 address inputs set LOW) with WRITE command; no data mask	IDD4W	
Refresh Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; $t_{RFC} = t_{RFC}(min)$; CKE# = LOW; DQ, DBI# are HIGH; address inputs are HIGH	IDD5	1
Self Refresh Current: CKE# = HIGH; all other inputs are HIGH	IDD6	
Four Bank Interleave Read Current: $t_{CK} = t_{CK}(min)$; $t_{WCK} = t_{WCK}(min)$; CKE# = LOW; one bank in each of the 4 bank groups activated and precharged at $t_{RC}(min)$; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; random bank, row and column addresses (4 address inputs set LOW) with ACT and READ/ READA commands; I_{OUT} = 0mA	IDD7	

NOTE: Min t_{RC} or t_{RFC} for IDD measurements is the smallest multiple of t_{CK} that meets the minimum of the absolute value for the respective parameter.

Common Test conditions:

1) Device is configured to x32 mode
2) ABI and DBI are enabled
3) All ODTs are enabled with ZQ/2
4) PLLs are enabled unless otherwise noted
5) CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to'1010'
6) Bank groups are enabled if required for device operation at $t_{CK}(min)$
7) Address inputs include ABI# pin
8) Each data byte consists of eight DQs and one DBI# pin
9) DESELECT condition during idle command cycles

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Table 43. IDD SPECIFICATIONS AND CONDITIONS

1. × 32 Mode IDD

Symbol	4.0Gbps	4.5Gbps	5.0Gbps	5.5Gbps	6.0Gbps	Units
IDD0	550	590	630	670	710	mA
IDD1	590	630	670	710	750	mA
IDD2P	240	260	280	300	320	mA
IDD2N	260	280	300	320	340	mA
IDD3P	385	405	425	445	465	mA
IDD3N	540	580	620	660	700	mA
IDD4W	1300	1430	1560	1690	1820	mA
IDD4R	1370	1500	1630	1760	1890	mA
IDD5	545	580	615	650	685	mA
IDD6	60	60	60	60	60	mA
IDD7	900	1000	1100	1200	1300	mA

2. × 16 Mode IDD

Symbol	4.0Gbps	4.5Gbps	5.0Gbps	5.5Gbps	6.0Gbps	Units
IDD0	370	400	420	450	490	mA
IDD1	390	420	450	480	520	mA
IDD2P	170	175	185	195	210	mA
IDD2N	190	200	210	230	250	mA
IDD3P	250	260	275	290	310	mA
IDD3N	350	370	390	420	450	mA
IDD4W	830	910	990	1070	1160	mA
IDD4R	850	930	1010	1090	1080	mA
IDD5	350	370	390	420	450	mA
IDD6	60	60	60	60	60	mA
IDD7	660	710	770	840	910	mA

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	6.0Gbps		5.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
CK and WCK Timings								
CK Clock cycle time	PLL on	tCK	0.667	2	0.727	2	ns	
	PLL off		0.667	20	0.727	20		
CK Clock high-level width		tCH	0.470	0.530	0.470	0.530	tCK	C
CK Clock low-level width		tCL	0.470	0.530	0.470	0.530	tCK	C
Min CK Clock half period		tHP	0.470	-	0.470	-	tCK	
Max CK Clock frequency with bank groups disabled		fCKBG	-	1500	-	1375	MHz	d
Max CK Clock frequency with bank groups enabled and tCCDL=3tCK		fCKBG4	-	1500	-	1375	MHz	d
Max CK Clock frequency with WCK2CK alignment at pins		fCKPIN	-	1500	-	1375	MHz	e
Max CK Clock frequency in RDQS Mode		fCKRDQS	-	TBD	-	TBD	MHz	f
Max CK Clock frequency for device operation with VREFD2		fCKVREFD2	-	TBD	-	TBD	MHz	g
Max CK Clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode		fCKAUTOSYNC	-	1500	-	1375	MHz	h
Max CK Clock frequency for device operation with Low Frequency Mode enabled		fCKLF	-	900	-	900	MHz	i
WCK Clock cycle time	PLL on	tWCK	0.333	1	0.364	1	ns	j
	PLL off		0.333	10	0.364	10		
WCK Clock high-level width		tWCKH	0.470	0.530	0.470	0.530	tWCK	k,l
WCK Clock low-level width		tWCKL	0.470	0.530	0.470	0.530	tWCK	k,l
Min WCK Clock half period		tWCKHP	0.470	-	0.470	-	tWCK	
Command and Address Input Timings								
Command input setup time		tCMDS	0.25	-	0.25	-	ns	m,n
Command input hold time		tCMDH	0.25	-	0.25	-	ns	m,n
Command input pulse width		tCMDPW	0.60	-	0.65	-	ns	m,n,o
Address input setup time		tAS	0.1	-	0.1	-	ns	m,n,p
Address input hold time		tAH	0.1	-	0.1	-	ns	m,n,p
Address input pulse width		tAPW	0.3	-	0.32	-	ns	m,n,o,p

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	6.0Gbps		5.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
WCK2CK Timings								
WCK stop to MRS delay for entering WCK2CK training		tWCK2MRS	3	-	3	-	ns	
MRS to WCK restart delay after entering WCK2CK training		tMRSTWCK	10	-	10	-	ns	q
WCK start to WCK phase movement delay		tWCK2TR	10	-	10	-	tCK	
WCK phase change to phase detector out delay		tWCK2PH	5	-	5	-	ns	
WCK Clock high-level width during WCK2CK training		tWCKHTR	0.42	0.58	0.42	0.58	tWCK	k,l,r
WCK Clock low-level width during WCK2CK training		tWCKLTR	0.42	0.58	0.42	0.58	tWCK	k,l,r
WCK2CK offset when zero offset at phase detector or at pins	PLL on;MR6A0=0 (at phase detector)	tWCK2CKPIN	-0.2	0.2	-0.2	0.2	ns	s
	PLL on;MR6A0=1 (at pins)		-0.2	0.2	-0.2	0.2		
	PLL off;MR6A0=0 (at phase detector)		-0.2	0.2	-0.2	0.2		
	PLL off;MR6A0=1 (at pins)		-0.2	0.2	-0.2	0.2		
WCK2CK phase offset upon WCK2CK training exit	MR6A0=0 (at phase detector)	tWCK2CKSYNC	-0.25	0.25	-0.25	0.25	tCK	t
	MR6A0=1 (at pins)		-0.25	0.25	-0.25	0.25	ns	
WCK2CK phase offset	MR6A0=0 (at phase detector)	tWCK2CK	-0.4	0.4	-0.4	0.4	tCK	u
	MR6A0=1 (at pins)		-0.4	0.4	-0.4	0.4	ns	
PLL Input and Output Timings								
WCK to DQ/DBI# offset for input data	PLL on	tWCK2DQI	0.7	1.7	0.7	1.7	ns	v
	PLL off		0.7	1.7	0.7	1.7		
WCK to DQ/DBI#/EDC/ offset for output data	PLL on	tWCK2DQO	1.1	2.2	1.1	2.2	ns	w,x
	PLL off		1.1	2.2	1.1	2.2		
DQ/DBI# input pulse width		tDIPW	0.15	-	0.164	-	ns	y,z,aa

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	6.0Gbps		5.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
DQ/DBI# data input valid window	PLL on	tDIVW	0.1	-	0.11	-	ns	y,z,ab
	PLL off		0.1	-	0.11	-		
DQ/DBI# input skew within double byte		tDQDQI	-0.1	0.1	-0.1	0.1	ns	ac
DQ/DBI#/EDC output skew within double byte		tDQDQO	-0.125	0.125	-0.125	0.125	ns	ad
Row Access Timings								
Active to Active command period		tRC	40	-	40	-	ns	
Active to PRECHARGE command period		tRAS	28	9*tREFI	28	9*tREFI	ns	ae
Active to READ command delay		tRCDRD	12	-	12	-	ns	
Active to WRITE command delay		tRCDWR	10	-	10	-	ns	
Active to RDTR command delay		tRCDRTR	10	-	10	-	ns	
Active to WRTR command delay		tRCDWTR	10	-	10	-	ns	
Active to LDFF command delay		tRCDLTR	10	-	10	-	ns	
REFRESH to RDTR or WRTR command delay		tREFTR	10	-	10	-	ns	
Active bank A to Active bank B command delay same bank group		tRRDL	5.5	-	5.5	-	ns	af
Active bank A to Active bank B command delay different bank groups		tRRDS	5.5	-	5.5	-	ns	ag
Four bank activate window		tFAW	23	-	23	-	ns	ah
Thirty two bank activate window		t32AW	184	-	184	-	ns	ai
READ to PRECHARGE command delay same bank with bank groups enabled		tRTPL	2	-	2	-	tCK	aj
READ to PRECHARGE command delay same bank with bank groups disabled		tRTPS	2	-	2	-	tCK	ak
PRECHARGE to PRECHARGE command delay		tPPD	1	-	1	-	ns	
PRECHARGE command period		tRP	12	-	12	-	ns	
WRITE recovery time		tWR	12	-	12	-	ns	
Auto precharge write recovery + precharge time		tDAL	24	-	24	-	tCK	al
Column Access Timings								
RD/WR bank A to RD/WR bank B command delay same bank group		tCCDL	3	-	3	-	tCK	af,am
RD/WR bank A to RD/WR bank B command delay different bank groups		tCCDS	2	-	2	-	tCK	ag,an

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	6.0Gbps		5.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
LDFF to LDFF command cycle time		tLTLTR	4	-	4	-	tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	4	-	4	-	tCK	ao
LDFF(111) to RDTR command cycle delay		tLTRTR	4	-	4	-	tCK	
READ or RDTR to LDFF command delay		tRDTLT	4	-	4	-	tCK	
WRITE to LDFF command delay		tWRTLT	WL+5	-	WL+5	-	tCK	
WRTR to RDTR command delay		tWTRTR	WL-tWLmin	-	WL-tWLmin	-	tCK	
WRITE to WRTR command delay		tWRWTR	WL+tCR CWL+2	-	WL+tCR CWL+2	-	tCK	
Internal WRITE to READ command delay same bank group		tWTRL	5	-	5	-	ns	af
Internal WRITE to READ command delay different bank groups		tWTRS	5	-	5	-	ns	ag
READ or RDTR to WRITE or WRTR command delay		tRTW	[CLmrs+(BL/4)+2-WLmrs]*tCK	-	[CLmrs+(BL/4)+2-WLmrs]*tCK	-	tCK	ap
Write Latency		tWL	4	7	4	7	tCK	aq
Power-Down and Refresh Timings								
CKE# min high and low pulse width		tCKE	16	-	14	-	tCK	
Valid CK Clock required after self refresh entry		tCKSRE	16	-	14	-	tCK	
Valid CK Clock required before self refresh exit		tCKSRX	16	-	14	-	tCK	
READ to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tRDSRE	CL+2tCK	-	CL+2tCK	-	tCK	ar
WRITE to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tWRSRE	TBD	-	TBD	-	tCK	as
REFRESH command period		tRFC	65	-	65	-	ns	
Exit self refresh to non-READ/WRITE command delay		tXSNRW	tRFC	-	tRFC	-	ns	
Exit self refresh to READ/WRITE command delay		tXSRW	tRFC+tRCD	-	tRFC+tRCD	-	tCK	at
Refresh period		tREF	-	32	-	32	ms	
Average periodic refresh interval	8k rows	tREFI	-	3.9	-	3.9	us	au
	16k rows		-	1.9	-	1.9		
Min Power down entry to exit time		tPD	16		14		tCK	

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Table 44. AC Timings (@1.5V)

PARAMETER a, b	SYMBOL	6.0Gbps		5.5Gbps		UNIT	NOTES
		MIN	MAX	MIN	MAX		
NOP/DESELECT commands required upon power-down and self refresh entry	tCPDED	4	-	3	-	tCK	
Power down exit time	tXPN	17	-	15	-	tCK	
Miscellaneous Timings							
MODE REGISTER SET command period	tMRD	4	-	4	-	tCK	
PLL enabled to PLL lock delay	tLK	-	5000	-	5000	tCK	
PLL standby time	tSTDBTY	-	TBD	-	TBD	us	ax
DVS voltage stabilization time	tVS	TBD	-	TBD	-	us	
REFRESH to calibration update complete delay	tKO	-	40	-	40	ns	
Active termination setup time	tATS	10	-	10	-	ns	
Active termination hold time	tATH	10	-	10	-	ns	
READ to data out delay in address training mode	tADR	0.5*tCK+0	0.5*tCK+10	0.5*tCK+0	0.5*tCK+10	tCK	q
Address training exit to DQ in ODT state delay	tADZ	-	0.5*tCK+10	-	0.5*tCK+10	ns	
Vendor ID on	tWRIDON	-	11	-	11	ns	
Venodr ID off	tWRIDOFF	-	11	-	11	ns	
Temperature sensor enable delay	tTSEN	10	-	10	-	us	

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	5.0Gbps		4.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
CK and WCK Timings								
CK Clock cycle time	PLL on	tCK	0.8	2	0.89	2	ns	
	PLL off		0.8	20	0.89	20		
CK Clock high-level width		tCH	0.470	0.530	0.470	0.530	tCK	C
CK Clock low-level width		tCL	0.470	0.530	0.470	0.530	tCK	C
Min CK Clock half period		tHP	0.470	-	0.470	-	tCK	
Max CK Clock frequency with bank groups disabled		fCKBG	-	1250	-	1125	MHz	d
Max CK Clock frequency with bank groups enabled and tCCDL=3tCK		fCKBG4	-	1250	-	1125	MHz	d
Max CK Clock frequency with WCK2CK alignment at pins		fCKPIN	-	1250	-	1125	MHz	e
Max CK Clock frequency in RDQS Mode		fCKRDQS	-	TBD	-	TBD	MHz	f
Max CK Clock frequency for device operation with VREFD2		fCKVREFD2	-	TBD	-	TBD	MHz	g
Max CK Clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode		fCKAUTOSYNC	-	1250	-	1125	MHz	h
Max CK Clock frequency for device operation with Low Frequency Mode enabled		fCKLF	-	900	-	900	MHz	i
WCK Clock cycle time	PLL on	tWCK	0.4	1	0.444	1	ns	j
	PLL off		0.4	10	0.444	10		
WCK Clock high-level width		tWCKH	0.470	0.530	0.470	0.530	tWCK	k,l
WCK Clock low-level width		tWCKL	0.470	0.530	0.470	0.530	tWCK	k,l
Min WCK Clock half period		tWCKHP	0.470	-	0.470	-	tWCK	
Command and Address Input Timings								
Command input setup time		tCMDS	0.25	-	0.25	-	ns	m,n
Command input hold time		tCMDH	0.25	-	0.25	-	ns	m,n
Command input pulse width		tCMDPW	0.7	-	0.7	-	ns	m,n,o
Address input setup time		tAS	0.1	-	0.125	-	ns	m,n,p
Address input hold time		tAH	0.1	-	0.125	-	ns	m,n,p
Address input pulse width		tAPW	0.36	-	0.4	-	ns	m,n,o,p

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	5.0Gbps		4.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
WCK2CK Timings								
WCK stop to MRS delay for entering WCK2CK training		tWCK2MRS	3	-	3	-	ns	
MRS to WCK restart delay after entering WCK2CK training		tMRSTWCK	10	-	10	-	ns	q
WCK start to WCK phase movement delay		tWCK2TR	10	-	10	-	tCK	
WCK phase change to phase detector out delay		tWCK2PH	5	-	5	-	ns	
WCK Clock high-level width during WCK2CK training		tWCKHTR	0.42	0.58	0.42	0.58	tWCK	k,l,r
WCK Clock low-level width during WCK2CK training		tWCKLTR	0.42	0.58	0.42	0.58	tWCK	k,l,r
WCK2CK offset when zero offset at phase detector or at pins	PLL on;MR6A0=0 (at phase detector)	tWCK2CKPIN	-0.2	0.2	-0.2	0.2	ns	s
	PLL on;MR6A0=1 (at pins)		-0.2	0.2	-0.2	0.2		
	PLL off;MR6A0=0 (at phase detector)		-0.2	0.2	-0.2	0.2		
	PLL off;MR6A0=1 (at pins)		-0.2	0.2	-0.2	0.2		
WCK2CK phase offset upon WCK2CK training exit	MR6A0=0 (at phase detector)	tWCK2CKSYNC	-0.25	0.25	-0.25	0.25	tCK	t
	MR6A0=1 (at pins)		-0.25	0.25	-0.25	0.25	ns	
WCK2CK phase offset	MR6A0=0 (at phase detector)	tWCK2CK	-0.4	0.4	-0.4	0.4	tCK	u
	MR6A0=1 (at pins)		-0.4	0.4	-0.4	0.4	ns	
PLL Input and Output Timings								
WCK to DQ/DBI# offset for input data	PLL on	tWCK2DQI	0.7	1.7	0.7	1.7	ns	v
	PLL off		0.7	1.7	0.7	1.7		
WCK to DQ/DBI#/EDC/ offset for output data	PLL on	tWCK2DQO	1.1	2.2	1.1	2.2	ns	w,x
	PLL off		1.1	2.2	1.1	2.2		
DQ/DBI# input pulse width		tDIPW	0.18	-	0.197	-	ns	y,z,aa

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	5.0Gbps		4.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
DQ/DBI# data input valid window	PLL on	tDIVW	0.12	-	0.13	-	ns	y,z,ab
	PLL off		0.12	-	0.13	-		
DQ/DBI# input skew within double byte		tDQDQI	-0.1	0.1	-0.1	0.1	ns	ac
DQ/DBI#/EDC output skew within double byte		tDQDQO	-0.125	0.125	-0.125	0.125	ns	ad
Row Access Timings								
Active to Active command period		tRC	40	-	40	-	ns	
Active to PRECHARGE command period		tRAS	28	9*tREFI	28	9*tREFI	ns	ae
Active to READ command delay		tRCDRD	12	-	12	-	ns	
Active to WRITE command delay		tRCDWR	10	-	10	-	ns	
Active to RDTR command delay		tRCDRTR	10	-	10	-	ns	
Active to WRTR command delay		tRCDWTR	10	-	10	-	ns	
Active to LDFF command delay		tRCDLTR	10	-	10	-	ns	
REFRESH to RDTR or WRTR command delay		tREFTR	10	-	10	-	ns	
Active bank A to Active bank B command delay same bank group		tRRDL	5.5	-	5.5	-	ns	af
Active bank A to Active bank B command delay different bank groups		tRRDS	5.5	-	5.5	-	ns	ag
Four bank activate window		tFAW	23	-	23	-	ns	ah
Thirty two bank activate window		t32AW	184	-	184	-	ns	ai
READ to PRECHARGE command delay same bank with bank groups enabled		tRTPL	2	-	2	-	tCK	aj
READ to PRECHARGE command delay same bank with bank groups disabled		tRTPS	2	-	2	-	tCK	ak
PRECHARGE to PRECHARGE command delay		tPPD	1	-	1	-	ns	
PRECHARGE command period		tRP	12	-	12	-	ns	
WRITE recovery time		tWR	12	-	12	-	ns	
Auto precharge write recovery + precharge time		tDAL	24	-	24	-	tCK	al
Column Access Timings								
RD/WR bank A to RD/WR bank B command delay same bank group		tCCDL	3	-	3	-	tCK	af,am
RD/WR bank A to RD/WR bank B command delay different bank groups		tCCDS	2	-	2	-	tCK	ag,an

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	5.0Gbps		4.5Gbps		UNIT	NOTES
			MIN	MAX	MIN	MAX		
LDFF to LDFF command cycle time		tLTLTR	4	-	4	-	tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	4	-	4	-	tCK	ao
LDFF(111) to RDTR command cycle delay		tLTRTR	4	-	4	-	tCK	
READ or RDTR to LDFF command delay		tRDTLT	4	-	4	-	tCK	
WRITE to LDFF command delay		tWRTLT	WL+5	-	WL+5	-	tCK	
WRTR to RDTR command delay		tWTRTR	WL-tWLmin	-	WL-tWLmin	-	tCK	
WRITE to WRTR command delay		tWRWTR	WL+tCR CWL+2	-	WL+tCR CWL+2	-	tCK	
Internal WRITE to READ command delay same bank group		tWTRL	5	-	5	-	ns	af
Internal WRITE to READ command delay different bank groups		tWTRS	5	-	5	-	ns	ag
READ or RDTR to WRITE or WRTR command delay		tRTW	[CLmrs+(BL/4)+2-WLmrs]*tCK	-	[CLmrs+(BL/4)+2-WLmrs]*tCK	-	tCK	ap
Write Latency		tWL	3	7	3	7	tCK	aq
Power-Down and Refresh Timings								
CKE# min high and low pulse width		tCKE	12	-	11	-	tCK	
Valid CK Clock required after self refresh entry		tCKSRE	12	-	11	-	tCK	
Valid CK Clock required before self refresh exit		tCKSRX	12	-	11	-	tCK	
READ to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tRDSRE	CL+2tCK	-	CL+2tCK	-	tCK	ar
WRITE to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tWRSRE	TBD	-	TBD	-	tCK	as
REFRESH command period		tRFC	65	-	65	-	ns	
Exit self refresh to non-READ/WRITE command delay		tXSNRW	tRFC	-	tRFC	-	ns	
Exit self refresh to READ/WRITE command delay		tXSRW	tRFC+tRCD	-	tRFC+tRCD	-	tCK	at
Refresh period		tREF	-	32	-	32	ms	
Average periodic refresh interval	8k rows	tREFI	-	3.9	-	3.9	us	au
	16k rows		-	1.9	-	1.9		
Min Power down entry to exit time		tPD	12		11		tCK	

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Table 44. AC Timings (@1.5V)

PARAMETER a, b	SYMBOL	5.0Gbps		4.5Gbps		UNIT	NOTES
		MIN	MAX	MIN	MAX		
NOP/DESELECT commands required upon power-down and self refresh entry	tCPDED	3	-	3	-	tCK	
Power down exit time	tXPN	13	-	11	-	tCK	
Miscellaneous Timings							
MODE REGISTER SET command period	tMRD	4	-	4	-	tCK	
PLL enabled to PLL lock delay	tLK	-	5000	-	5000	tCK	
PLL standby time	tSTDBTY	-	TBD	-	TBD	us	ax
DVS voltage stabilization time	tVS	TBD	-	TBD	-	us	
REFRESH to calibration update complete delay	tKO	-	40	-	40	ns	
Active termination setup time	tATS	10	-	10	-	ns	
Active termination hold time	tATH	10	-	10	-	ns	
READ to data out delay in address training mode	tADR	0.5*tCK+0	0.5*tCK+10	0.5*tCK+0	0.5*tCK+10	tCK	q
Address training exit to DQ in ODT state delay	tADZ	-	0.5*tCK+10	-	0.5*tCK+10	ns	
Vendor ID on	tWRIDON	-	11	-	11	ns	
Venodr ID off	tWRIDOFF	-	11	-	11	ns	
Temperature sensor enable delay	tTSEN	10	-	10	-	us	

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	4.0Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
CK and WCK Timings								
CK Clock cycle time	PLL on	tCK	1	2			ns	
	PLL off		1	20				
CK Clock high-level width		tCH	0.470	0.530			tCK	C
CK Clock low-level width		tCL	0.470	0.530			tCK	C
Min CK Clock half period		tHP	0.470	-			tCK	
Max CK Clock frequency with bank groups disabled		fCKBG	-	1000			MHz	d
Max CK Clock frequency with bank groups enabled and tCCDL=3tCK		fCKBG4	-	1000			MHz	d
Max CK Clock frequency with WCK2CK alignment at pins		fCKPIN	-	1000			MHz	e
Max CK Clock frequency in RDQS Mode		fCKRDQS	-	TBD			MHz	f
Max CK Clock frequency for device operation with VREFD2		fCKVREFD2	-	TBD			MHz	g
Max CK Clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode		fCKAUTOSYNC	-	100			MHz	h
Max CK Clock frequency for device operation with Low Frequency Mode enabled		fCKLF	-	800			MHz	i
WCK Clock cycle time	PLL on	tWCK	0.5	1			ns	j
	PLL off		0.5	10				
WCK Clock high-level width		tWCKH	0.470	0.530			tWCK	k,l
WCK Clock low-level width		tWCKL	0.470	0.530			tWCK	k,l
Min WCK Clock half period		tWCKHP	0.470	-			tWCK	
Command and Address Input Timings								
Command input setup time		tCMDS	0.25	-			ns	m,n
Command input hold time		tCMDH	0.25	-			ns	m,n
Command input pulse width		tCMDPW	0.7	-			ns	m,n,o
Address input setup time		tAS	0.125	-			ns	m,n,p
Address input hold time		tAH	0.125	-			ns	m,n,p
Address input pulse width		tAPW	0.45	-			ns	m,n,o,p

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	4.0Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
WCK2CK Timings								
WCK stop to MRS delay for entering WCK2CK training		tWCK2MRS	3	-			ns	
MRS to WCK restart delay after entering WCK2CK training		tMRSTWCK	10	-			ns	q
WCK start to WCK phase movement delay		tWCK2TR	10	-			tCK	
WCK phase change to phase detector out delay		tWCK2PH	5	-			ns	
WCK Clock high-level width during WCK2CK training		tWCKHTR	0.42	0.58			tWCK	k,l,r
WCK Clock low-level width during WCK2CK training		tWCKLTR	0.42	0.58			tWCK	k,l,r
WCK2CK offset when zero offset at phase detector or at pins	PLL on;MR6A0=0 (at phase detector)	tWCK2CKPIN	-0.2	0.2			ns	s
	PLL on;MR6A0=1 (at pins)		-0.2	0.2				
	PLL off;MR6A0=0 (at phase detector)		-0.2	0.2				
	PLL off;MR6A0=1 (at pins)		-0.2	0.2				
WCK2CK phase offset upon WCK2CK training exit	MR6A0=0 (at phase detector)	tWCK2CKSYNC	-0.25	0.25			tCK	t
	MR6A0=1 (at pins)		-0.25	0.25			ns	
WCK2CK phase offset	MR6A0=0 (at phase detector)	tWCK2CK	-0.4	0.4			tCK	u
	MR6A0=1 (at pins)		-0.4	0.4			ns	
PLL Input and Output Timings								
WCK to DQ/DBI# offset for input data	PLL on	tWCK2DQI	0.7	1.7			ns	v
	PLL off		0.7	1.7				
WCK to DQ/DBI#/EDC/ offset for output data	PLL on	tWCK2DQO	1.1	2.2			ns	w,x
	PLL off		1.1	2.2				
DQ/DBI# input pulse width		tDIPW	0.225	-			ns	y,z,aa

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	4.0Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
DQ/DBI# data input valid window	PLL on	tDIVW	0.15	-			ns	y,z,ab
	PLL off		0.15	-				
DQ/DBI# input skew within double byte		tDQDQI	-0.1	0.1			ns	ac
DQ/DBI#/EDC output skew within double byte		tDQDQO	-0.125	0.125			ns	ad
Row Access Timings								
Active to Active command period		tRC	40	-			ns	
Active to PRECHARGE command period		tRAS	28	9*tREFI			ns	ae
Active to READ command delay		tRCDRD	12	-			ns	
Active to WRITE command delay		tRCDWR	10	-			ns	
Active to RDTR command delay		tRCDRTR	10	-			ns	
Active to WRTR command delay		tRCDWTR	10	-			ns	
Active to LDFF command delay		tRCDLTR	10	-			ns	
REFRESH to RDTR or WRTR command delay		tREFTR	10	-			ns	
Active bank A to Active bank B command delay same bank group		tRRDL	5.5	-			ns	af
Active bank A to Active bank B command delay different bank groups		tRRDS	5.5	-			ns	ag
Four bank activate window		tFAW	23	-			ns	ah
Thirty two bank activate window		t32AW	184	-			ns	ai
READ to PRECHARGE command delay same bank with bank groups enabled		tRTPL	2	-			tCK	aj
READ to PRECHARGE command delay same bank with bank groups disabled		tRTPS	2	-			tCK	ak
PRECHARGE to PRECHARGE command delay		tPPD	1	-			ns	
PRECHARGE command period		tRP	12	-			ns	
WRITE recovery time		tWR	12	-			ns	
Auto precharge write recovery + precharge time		tDAL	24	-			tCK	al
Column Access Timings								
RD/WR bank A to RD/WR bank B command delay same bank group		tCCDL	3	-			tCK	af,am
RD/WR bank A to RD/WR bank B command delay different bank groups		tCCDS	2	-			tCK	ag,an

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Table 44. AC Timings (@1.5V)

PARAMETER a, b		SYMBOL	4.0Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
LDFF to LDFF command cycle time		tLTLTR	4	-			tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	4	-			tCK	ao
LDFF(111) to RDTR command cycle delay		tLTRTR	4	-			tCK	
READ or RDTR to LDFF command delay		tRDTLT	4	-			tCK	
WRITE to LDFF command delay		tWRTLT	WL+5	-			tCK	
WRTR to RDTR command delay		tWTRTR	WL-tWLmin	-			tCK	
WRITE to WRTR command delay		tWRWTR	WL+tCRCWL+2	-			tCK	
Internal WRITE to READ command delay same bank group		tWTRL	5	-			ns	af
Internal WRITE to READ command delay different bank groups		tWTRS	5	-			ns	ag
READ or RDTR to WRITE or WRTR command delay		tRTW	[CLmrs+(BL/4)+2-WLmrs]*tCK	-			tCK	ap
Write Latency		tWL	3	7			tCK	aq
Power-Down and Refresh Timings								
CKE# min high and low pulse width		tCKE	10	-			tCK	
Valid CK Clock required after self refresh entry		tCKSRE	10	-			tCK	
Valid CK Clock required before self refresh exit		tCKSRX	10	-			tCK	
READ to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tRDSRE	CL+2tCK	-			tCK	ar
WRITE to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tWRSRE	TBD	-			tCK	as
REFRESH command period		tRFC	65	-			ns	
Exit self refresh to non-READ/WRITE command delay		tXSNRW	tRFC	-			ns	
Exit self refresh to READ/WRITE command delay		tXSRW	tRFC+tRCD	-			tCK	at
Refresh period		tREF	-	32			ms	
Average periodic refresh interval	8k rows	tREFI	-	3.9			us	au
	16k rows		-	1.9				
Min Power down entry to exit time		tPD	10				tCK	

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Table 44. AC Timings (@1.5V)

PARAMETER a, b	SYMBOL	4.0Gbps		-		UNIT	NOTES
		MIN	MAX	MIN	MAX		
NOP/DESELECT commands required upon power-down and self refresh entry	tCPDED	2	-			tCK	
Power down exit time	tXPN	10	-			tCK	
Miscellaneous Timings							
MODE REGISTER SET command period	tMRD	4	-			tCK	
PLL enabled to PLL lock delay	tLK	-	5000			tCK	
PLL standby time	tSTDBTY	-	TBD			us	ax
DVS voltage stabilization time	tVS	TBD	-			us	
REFRESH to calibration update complete delay	tKO	-	40			ns	
Active termination setup time	tATS	10	-			ns	
Active termination hold time	tATH	10	-			ns	
READ to data out delay in address training mode	tADR	0.5*tCK+0	0.5*tCK+10			tCK	q
Address training exit to DQ in ODT state delay	tADZ	-	0.5*tCK+10			ns	
Vendor ID on	tWRIDON	-	11			ns	
Venodr ID off	tWRIDOFF	-	11			ns	
Temperature sensor enable delay	tTSEN	10	-			us	

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Table 44. AC Timings (@1.35V)

PARAMETER a, b		SYMBOL	3.2Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
CK and WCK Timings								
CK Clock cycle time	PLL on	tCK	1.25	2			ns	
	PLL off		1.25	20				
CK Clock high-level width		tCH	0.470	0.530			tCK	C
CK Clock low-level width		tCL	0.470	0.530			tCK	C
Min CK Clock half period		tHP	0.470	-			tCK	
Max CK Clock frequency with bank groups disabled		fCKBG	-	800			MHz	d
Max CK Clock frequency with bank groups enabled and tCCDL=3tCK		fCKBG4	-	800			MHz	d
Max CK Clock frequency with WCK2CK alignment at pins		fCKPIN	-	800			MHz	e
Max CK Clock frequency in RDQS Mode		fCKRDQS	-	TBD			MHz	f
Max CK Clock frequency for device operation with VREFD2		fCKVREFD2	-	TBD			MHz	g
Max CK Clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode		fCKAUTOSYNC	-	800			MHz	h
Max CK Clock frequency for device operation with Low Frequency Mode enabled		fCKLF	-	700			MHz	i
WCK Clock cycle time	PLL on	tWCK	0.625	1			ns	j
	PLL off		0.625	10				
WCK Clock high-level width		tWCKH	0.470	0.530			tWCK	k,l
WCK Clock low-level width		tWCKL	0.470	0.530			tWCK	k,l
Min WCK Clock half period		tWCKHP	0.470	-			tWCK	
Command and Address Input Timings								
Command input setup time		tCMDS	0.3	-			ns	m,n
Command input hold time		tCMDH	0.3	-			ns	m,n
Command input pulse width		tCMDPW	1.0	-			ns	m,n,o
Address input setup time		tAS	0.15	-			ns	m,n,p
Address input hold time		tAH	0.15	-			ns	m,n,p
Address input pulse width		tAPW	0.55	-			ns	m,n,o,p

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Table 44. AC Timings (@1.35V)

PARAMETER a, b		SYMBOL	3.2Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
WCK2CK Timings								
WCK stop to MRS delay for entering WCK2CK training		tWCK2MRS	3	-			ns	
MRS to WCK restart delay after entering WCK2CK training		tMRSTWCK	10	-			ns	q
WCK start to WCK phase movement delay		tWCK2TR	10	-			tCK	
WCK phase change to phase detector out delay		tWCK2PH	5	-			ns	
WCK Clock high-level width during WCK2CK training		tWCKHTR	0.42	0.58			tWCK	k,l,r
WCK Clock low-level width during WCK2CK training		tWCKLTR	0.42	0.58			tWCK	k,l,r
WCK2CK offset when zero offset at phase detector or at pins	PLL on;MR6A0=0 (at phase detector)	tWCK2CKPIN	-0.2	0.2			ns	s
	PLL on;MR6A0=1 (at pins)		-0.2	0.2				
	PLL off;MR6A0=0 (at phase detector)		-0.2	0.2				
	PLL off;MR6A0=1 (at pins)		-0.2	0.2				
WCK2CK phase offset upon WCK2CK training exit	MR6A0=0 (at phase detector)	tWCK2CKSYNC	-0.25	0.25			tCK	t
	MR6A0=1 (at pins)		-0.25	0.25			ns	
WCK2CK phase offset	MR6A0=0 (at phase detector)	tWCK2CK	-0.4	0.4			tCK	u
	MR6A0=1 (at pins)		-0.4	0.4			ns	
PLL Input and Output Timings								
WCK to DQ/DBI# offset for input data	PLL on	tWCK2DQI	0.7	1.7			ns	v
	PLL off		0.7	1.7				
WCK to DQ/DBI#/EDC/ offset for output data	PLL on	tWCK2DQO	1.1	2.2			ns	w,x
	PLL off		1.1	2.2				
DQ/DBI# input pulse width		tDIPW	0.295	-			ns	y,z,aa

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Table 44. AC Timings (@1.35V)

PARAMETER a, b		SYMBOL	3.2Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
DQ/DBI# data input valid window	PLL on	tDIVW	0.19	-			ns	y,z,ab
	PLL off		0.19	-				
DQ/DBI# input skew within double byte		tDQDQI	-0.1	0.1			ns	ac
DQ/DBI#/EDC output skew within double byte		tDQDQO	-0.125	0.125			ns	ad
Row Access Timings								
Active to Active command period		tRC	48	-			ns	
Active to PRECHARGE command period		tRAS	32	9*tREFI			ns	ae
Active to READ command delay		tRCDRD	16	-			ns	
Active to WRITE command delay		tRCDWR	14	-			ns	
Active to RDTR command delay		tRCDRTR	16	-			ns	
Active to WRTR command delay		tRCDWTR	14	-			ns	
Active to LDFF command delay		tRCDLTR	14	-			ns	
REFRESH to RDTR or WRTR command delay		tREFTR	14	-			ns	
Active bank A to Active bank B command delay same bank group		tRRDL	12	-			ns	af
Active bank A to Active bank B command delay different bank groups		tRRDS	7	-			ns	ag
Four bank activate window		tFAW	30	-			ns	ah
Thirty two bank activate window		t32AW	245	-			ns	ai
READ to PRECHARGE command delay same bank with bank groups enabled		tRTPL	2	-			tCK	aj
READ to PRECHARGE command delay same bank with bank groups disabled		tRTPS	2	-			tCK	ak
PRECHARGE to PRECHARGE command delay		tPPD	1	-			ns	
PRECHARGE command period		tRP	16	-			ns	
WRITE recovery time		tWR	16	-			ns	
Auto precharge write recovery + precharge time		tDAL	32	-			tCK	al
Column Access Timings								
RD/WR bank A to RD/WR bank B command delay same bank group		tCCDL	3	-			tCK	af,am
RD/WR bank A to RD/WR bank B command delay different bank groups		tCCDS	2	-			tCK	ag,an

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Table 44. AC Timings (@1.35V)

PARAMETER a, b		SYMBOL	3.2Gbps		-		UNIT	NOTES
			MIN	MAX	MIN	MAX		
LDFF to LDFF command cycle time		tLTLTR	4	-			tCK	
LDFF(111) to LDFF command cycle time		tLTL7TR	4	-			tCK	ao
LDFF(111) to RDTR command cycle delay		tLTRTR	4	-			tCK	
READ or RDTR to LDFF command delay		tRDTLT	4	-			tCK	
WRITE to LDFF command delay		tWRTLT	WL+5	-			tCK	
WRTR to RDTR command delay		tWTRTR	WL-tWLmin	-			tCK	
WRITE to WRTR command delay		tWRWTR	WL+tCRCWL+2	-			tCK	
Internal WRITE to READ command delay same bank group		tWTRL	5	-			ns	af
Internal WRITE to READ command delay different bank groups		tWTRS	5	-			ns	ag
READ or RDTR to WRITE or WRTR command delay		tRTW	[CLmrs+(BL/4)+2-WLmrs]*tCK	-			tCK	ap
Write Latency		tWL	3	7			tCK	aq
Power-Down and Refresh Timings								
CKE# min high and low pulse width		tCKE	11	-			tCK	
Valid CK Clock required after self refresh entry		tCKSRE	11	-			tCK	
Valid CK Clock required before self refresh exit		tCKSRX	11	-			tCK	
READ to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tRDSRE	CL+2tCK	-			tCK	ar
WRITE to SELF REFRESH ENTRY or POWER DOWN ENTRY command delay		tWRSRE	TBD	-			tCK	as
REFRESH command period		tRFC	120	-			ns	
Exit self refresh to non-READ/WRITE command delay		tXSNRW	tRFC	-			ns	
Exit self refresh to READ/WRITE command delay		tXSRW	tRFC+tRCD	-			tCK	at
Refresh period		tREF	-	32			ms	
Average periodic refresh interval	8k rows	tREFI	-	3.9			us	au
	16k rows		-	1.9				
Min Power down entry to exit time		tPD	11				tCK	

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Table 44. AC Timings (@1.35V)

PARAMETER a, b	SYMBOL	3.2Gbps		-		UNIT	NOTES
		MIN	MAX	MIN	MAX		
NOP/DESELECT commands required upon power-down and self refresh entry	tCPDED	2	-			tCK	
Power down exit time	tXPN	10	-			tCK	
Miscellaneous Timings							
MODE REGISTER SET command period	tMRD	4	-			tCK	
PLL enabled to PLL lock delay	tLK	-	5000			tCK	
PLL standby time	tSTDBTY	-	TBD			us	ax
DVS voltage stabilization time	tVS	TBD	-			us	
REFRESH to calibration update complete delay	tKO	-	40			ns	
Active termination setup time	tATS	10	-			ns	
Active termination hold time	tATH	10	-			ns	
READ to data out delay in address training mode	tADR	0.5*tCK+0	0.5*tCK+10			tCK	q
Address training exit to DQ in ODT state delay	tADZ	-	0.5*tCK+10			ns	
Vendor ID on	tWRIDON	-	11			ns	
Venodr ID off	tWRIDOFF	-	11			ns	
Temperature sensor enable delay	tTSEN	10	-			us	

a. All parameters assume proper device initialization.
b. Tests for AC timing may be considered at norminal supply voltage levels, but the related specification and device operation are guaranteed for the full voltage and temperature range specified.
c. CK and CK# single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between V_{REFC} crossing and $V_{IXCK(AC)}$
d. Parameter fCKBG4 is required for those devices supporting both 3*tCK and 4*tCK setting for bank groups. Devices supporting only 3*tCK or 4*tCK need only to specify fCKBG.
e. Parameter fCKPIN applies when the alignment point in MR6, bit A0 is set to “at pins”, the phase difference between the WCK and CK clocks at the DRAM pins is within tWCK2CKSYNC or tWCK2CK for pin mode and no phase search in WCK2CK training is performed.
f. Parameter fCKRDQS applies when RDQS mode is enabled in AR3, bit A5.
g. Parameter fCKBREFD2 applies when the data input reference voltage in MR7, bit A7 (Half VREFD) is set to VREFD2.
h. Parameter fCKAUTOSYNC applies when WCK2CK Auto Synchronization is enabled in MR7, bit A4.
i. Parameter fCKLF applies when Low Frequency Mode is enabled in MR7, bit A3.
j. By definition the norminal WCK clock cycle time always is 1/2 of the CK clock cycle time (not including jitter).
k. WCK and WCK# single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between V_{REFD} crossing and $V_{IXWCK(AC)}$.

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l. The phase relationship between WCK/WCK# and CK/CK# clocks must meet the tWCK2CK specification.
m. Command and address input timings are referenced to V_{REFC}.
n. Command and address input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between V_{REFC} crossing and $V_{IHA(AC)}$ or $V_{ILA(AC)}$.
o. Command and address input pulse widths are design targets. The value will be characterized but not tested on each device.
p. Address input timings are only valid with ABI beging enabled and a maximum of 4 address input driven LOW.
q. Parameter may be specified as a combination of tCK and ns.
r. Parameters tWCKHTR and tWCKLTR specify the max. allowed WCK clock-to-clock phase shift during WCK2CK training. For READ and WRITE bursts use tWCKH and tWCKL.
s. Parameter tWCK2CKPIN defines the WCK2CK phase offset range at the CK and WCK pins for ideal (phase=0°) clock alignment at the GDDR5 SGRAM's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment in MR6, bit A0 is set to "at pins"). The minimum and maximum values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on or PLL-off mode and design implementation.
t. Parameter tWCK2CKSYNC defines the max. phase offset from the ideal (phase = 0°) clock alignment at the GDDR5 SGRAM's phase detector (when the alignment point in MR6, bit A0 is set to "at the phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), where the internal logic synchronizes the CK and WCK clocks; it is expected to be a fraction of tWCK2CK.
u. Parameter tWCK2CK defines the max. phase offset from the ideal (phase = 0°) clock alignment at the GDDR5 SGRAM's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector") or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), for stable device operation.
v. Parameter tWCK2DQI defines the WCK to DQ/DBI# time delay range for WRITEs for PLL-on and PLL-off mode. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual tWCK2DQI value for reliable WRITE operation.
w. Parameter tWCK2DQO defines the WCK to DQ/DBI# time delay range for READs for PLL-on and PLL-off mode. The minimum and maxium values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determind the actual tWCK2DQO value for reliable READ operation.
x. Outputs measured with equivalent load terminated with 60 Ohms to VDDQ
y. DQ/DBI# input timings are valid only with DBI being enabled and a maximum of 4 data inputs per byte driven LOW.
z. Data input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between V_{REFD} crossing and $V_{IHD(AC)}$ or $V_{ILD(AC)}$.
aa. The data input pulse width, tDIPW, defines the minimum positive or negative input pulse width for any worst-case channel required for proper propagation of an external signal to the receiver. tDIPW is measured at the pins. tDIPW is independent of the PLL mode. In general tDIPW is larger than tDIVW
ab. The data input valid width, tDIVW, defines the time region where input data must be valid for reliable data capture at the receiver for any one worst case channel. It accounts for jitter between data and clock at the latching point introduced in the path between DARM pads and the latching point. Any additional jitter introduced into the source signals (e.g. within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL mode and bandwidth. tDIVW is measured at the pins. tDIVW is defined for PLL off and on mode separately. In the case of PLL on, tDIVW must be specified for each supported bandwidth. In general, tDIVW is smaller than tDIPW.
ac. tDQDQI defines the maximum skew among all DQ/DBI# inputs of a double byte (when configured to × 32 mode) or a single byte (when configured to × 16 mode) under worst case conditions. Parameter tWCK2DQI defines the mean value of the earliest and latest DQ/DBI# pin, tDQDQI(min) the negative offset to tWCK2DQI for the earliest DQ/DBI# pin and tDQDQI(max) the positive offset to tWCK2DQI for the latest DQ/DBI# pin.
ad. tDQDQO defines the maximum skew among all DQ/DBI# outputs of a double byte (when configured to × 32mode) or a single byte (when configured to × 16 mode) under worst case conditions. Parameter tWCK2DQO defines the mean value of of the earliest and latest DQ/DBI# /EDC pin, tDQDQO(min) the negative offset to tWCK2DQO for earliest DQ/DBI#/EDC pin and tDQDQO(max) the positive offset to tWCK2DQO for the latest DQ/DBI#/EDC pin.
ae. For READs and WRITEs with AUTO PRECHARGE enabled the device will hold off the internal PRECHARGE until tRAS(min) has been satisfied.
af. Parameter applies when bank groups are enabled and consecutive commands access the same bank group.
ag. Parameter applies when bank groups are disabled or consecutive commands access different bank group.
ah. Not more than 4 ACTIVE commands are allowed within period.
ai. Not more than 32 ACTIVE commands are allowed within t32AW period. The parameter need not to be specified in case t32AW(min) would not be greater than 8*tFAW(min).
aj. Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.
ak. Parameter applies when bank groups are disabled or READ and PRECHARGE commands access the same bank.
al. tDAL = (tWR/tCK) + (tRP/tCK). For each of the terms, if not already an integer, round up to the next integer.
am. tCCDL is either for gapless consecutive READ or gapless consecutive WRITE commands
an. tCCDS is either for gapless consecutive READ or RDTR (any combination), gapless consecutive WRITE, or gapless consecutive WRTR commands.
ao. The min. value does not exceed 8 tCK
ap. tRTW is not a device limit but determined by the system bus turnaround time. The difference between tWCK2DQO and tWCK2DQI shall be considered in the calculation of the bus turnaround time.

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aq. The WRITE latency WLmrs cna be set to 3 to 7 clocks. When the WRITE latency is set to small values (3 ~ 4 clocks), the input buffers are always on, reducing the latency but adding power. When the WRITE latency is set to larger values (5 ~ 7 clocks), the input buffers are turned on with the WRITE command, thus saving power.

ar. Read data including CRC data must have been clocked out before entering self refresh or power down mode.

as. Write data must have been written to the memory core and CRC data must have been clocked out before entering self refresh or power down mode.

at. Time for WCK2CK training and data training not included.

au. A maximum of 8 consecutive REFRESH commands can be posted to a GDDR5 SGRAM device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9*tREFI.

av. Replaces parameter tLK when PLL Fast Lock has been neabled prior to the PLL enable or reset.

aw. Replaces parameter tLK when PLL Standby has been enabed and the WCK clock frequency has not charged while in standby mode.

ax. The PLL standby time tSTDBY ismeasured from self refresh entry until after self refresh exit a subsequent PLL reset is given (with PLL Standby enabled)

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6.3 CLOCK-TO-DATA TIMING SENSITIVITY

The availability of clock-to-data (WCK2DQ) timing sensitivity information provides the controller the opportunity to anticipate the impact to timings from variations in environmental conditions (such as changes in voltage or temperature) allowing the controller to take corrective action if necessary (e.g. realigning WCK and DQ).

Variations in relative timing between WCK and data are reported for READ and WRITE paths. This specification calls out one zone each for VDDQ, VDD, and Tcase temperature over a specified range. Vendors may choose to provide information for additional zones covering, in total, a wider range or a finer granularity or both.

However, within a given zone if an approximated value (i.e. the specified slope) deviates from the characterized slope to such a degree that the approximated WCK-to-DQ time delay would be in error by more than 5% of one UI relative to the characterized delay then the splitting of this zone into more than one zone is required.

All zones and their associated specified slopes must form a continuous piece-wise-linear curve such that, after calibration during normal operation, traversing the approximated curve (i.e. the set of specified slopes) does not lead to time delay errors in excess of the 5% of one UI.

Tables 45, 46, and 47 below describe the minimum set of defined zones.

Table 45. VDDQ Voltage Zone

	VDDQ High	VDDQ Low	Notes
Zone_VQ1	VDDQmax	VDDQmin	a

a. VDDQ(max) is the maximum specified operating voltage. VDDQ(min) is the minimum specified operating voltage.

Table 46. VDD Voltage Zone

	VDD High	VDD Low	Notes
Zone_VD1	VDDmax	VDDmin	a

a. VDD(max) is the maximum specified operating voltage. VDD(min) is the minimum specified operating voltage.

Table 47. Tcase Temperature Zone

	Tcase High	Tcase Low	Notes
Zone_T1	Tcasemax	10°C	a

a. Tcase(max) is the maximum specified operating temperature.

As noted, variations in relative timing are reported for READ and WRITE paths. Tables 48,49 and 50 below provide information for READ timings while Tables 51,52 and 53 provide information for WRITE timings

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Table 48. WCK-to-Data READ Timing Sensitivity to VDDQ

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in VDDQ for zone_VQ1	PLL on	$t_{O2VQSensZ1}$	TBD	ps/V	a,b
	PLL off		TBD		

a. Calculation of tO2VQSensZ1 is performed as follows:
tO2VQSensZ1 equals the quantity (tWCK2DQO(Zone_VQ1(max)) - tWCK2DQO(Zone_VQ1(min)))
divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
= (tWCK2DQO(VDDQ(max)) - tWCK2DQO(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
b. VDD(typ), Tcase = 85°C, worst-case process corner.

Table 49. WCK-to-Data READ Timing Sensitivity to VDD

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in VDD for zone_VD1	PLL on	$t_{O2VDSensZ1}$	TBD	ps/V	a,b
	PLL off		TBD		

a. Calculation of tO2VDSensZ1 is performed as follows:
tO2VDSensZ1 equals the quantity (tWCK2DQO(Zone_VD1(max)) - tWCK2DQO(Zone_VD1(min)))
divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
= (tWCK2DQO(VDD(max)) - tWCK2DQO(VDD(min))) / (VDD(max) - VDD(min)).
b. VDDQ(typ), Tcase = 85°C, worst-case process corner.

Table 50. WCK-to-Data READ Timing Sensitivity to Tcase

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in Tcase for zone_T1	PLL on	$t_{O2TSensZ1}$	TBD	ps/°C	a,b
	PLL off		TBD		

a. Calculation of tO2TSensZ1 is performed as follows:
tO2TSensZ1 equals the quantity (tWCK2DQO(Zone_T1(max)) - tWCK2DQO(Zone_T1(min)))
divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
= (tWCK2DQO(Tcase(max)) - tWCK2DQO(Tcase(min))) / (Tcase(max) - Tcase(min)).
b. VDDQ(typ), VDD(typ), worst-case process corner.

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Tables 51, 52 and 53 below provide information for WRITE timings.

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Table 51. WCK-to-Data WRITE Timing Sensitivity to VDDQ

Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in VDDQ for zone_VQ1	PLL on	$t_{I2VQSensZ1}$	TBD	ps/V	a,b
	PLL off		TBD		

a. Calculation of tI2VQSensZ1 is performed as follows:
tI2VQSensZ1 equals the quantity (tWCK2DQI(Zone_VQ1(max)) - tWCK2DQI(Zone_VQ1(min)))
divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
= (tWCK2DQI(VDDQ(max)) - tWCK2DQI(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
b. VDD(typ), Tcase = 85°C, worst-case process corner.

Table 52. WCK-to-Data WRITE Timing Sensitivity to VDD

Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in VDD for zone_VD1	PLL on	$t_{I2VDSensZ1}$	TBD	ps/V	a,b
	PLL off		TBD		

a. Calculation of tO2VDSensZ1 is performed as follows:
tI2VDSensZ1 equals the quantity (tWCK2DQI(Zone_VD1(max)) - tWCK2DQI(Zone_VD1(min)))
divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
= (tWCK2DQI(VDD(max)) - tWCK2DQI(VDD(min))) / (VDD(max) - VDD(min)).
b. VDDQ(typ), Tcase = 85°C, worst-case process corner.

Table 53. WCK-to-Data WRITE Timing Sensitivity to Tcase

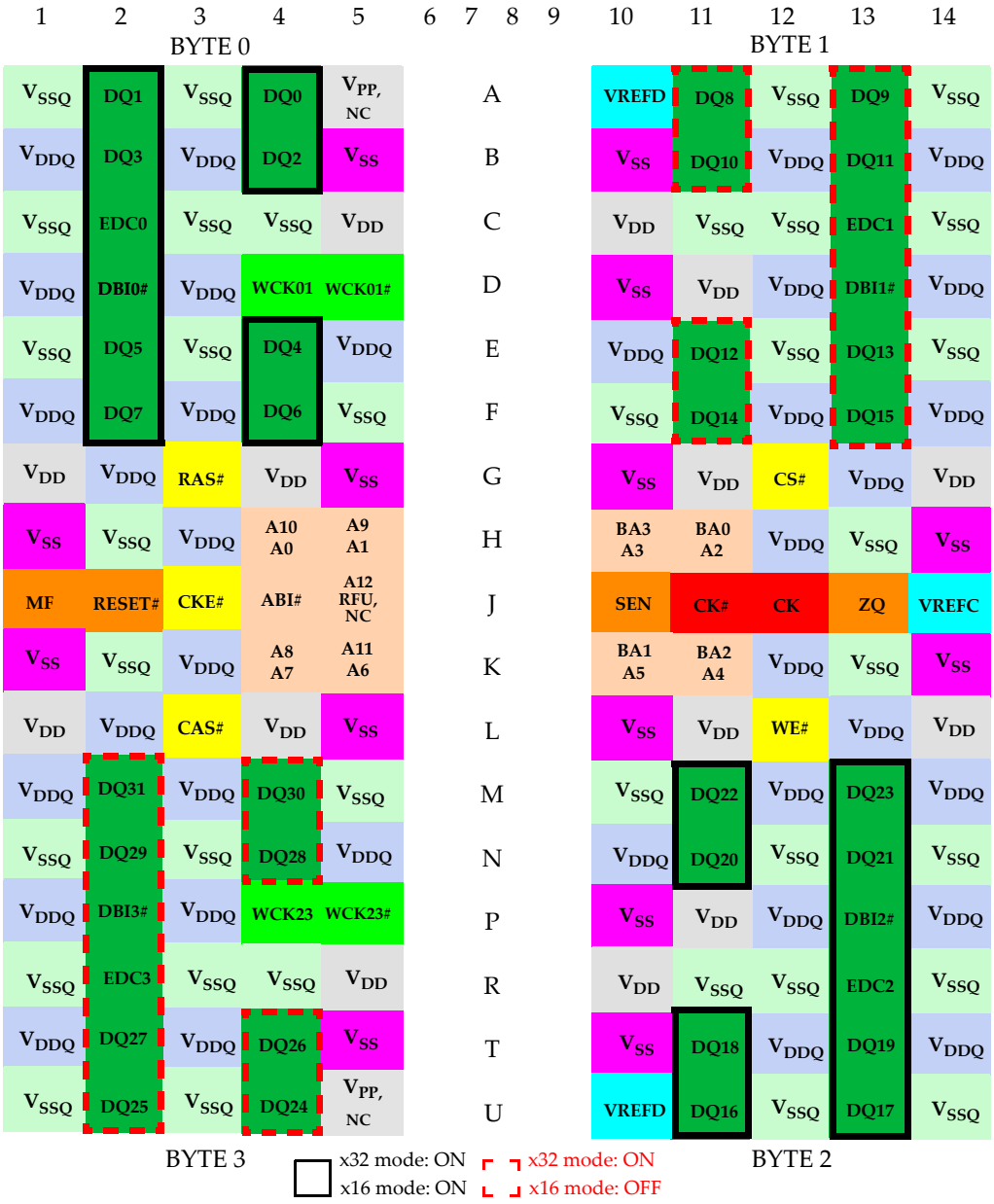
Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in Tcase for zone_T1	PLL on	$t_{I2TSensZ1}$	TBD	ps/°C	a,b
	PLL off		TBD		

a. Calculation of tI2TSensZ1 is performed as follows:
tI2TSensZ1 equals the quantity (tWCK2DQI(Zone_T1(max)) - tWCK2DQI(Zone_T1(min)))
divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
= (tWCK2DQI(Tcase(max)) - tWCK2DQI(Tcase(min))) / (Tcase(max) - Tcase(min)).
b. VDDQ(typ), VDD(typ), worst-case process corner.

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7. PACKAGE SPECIFICATION

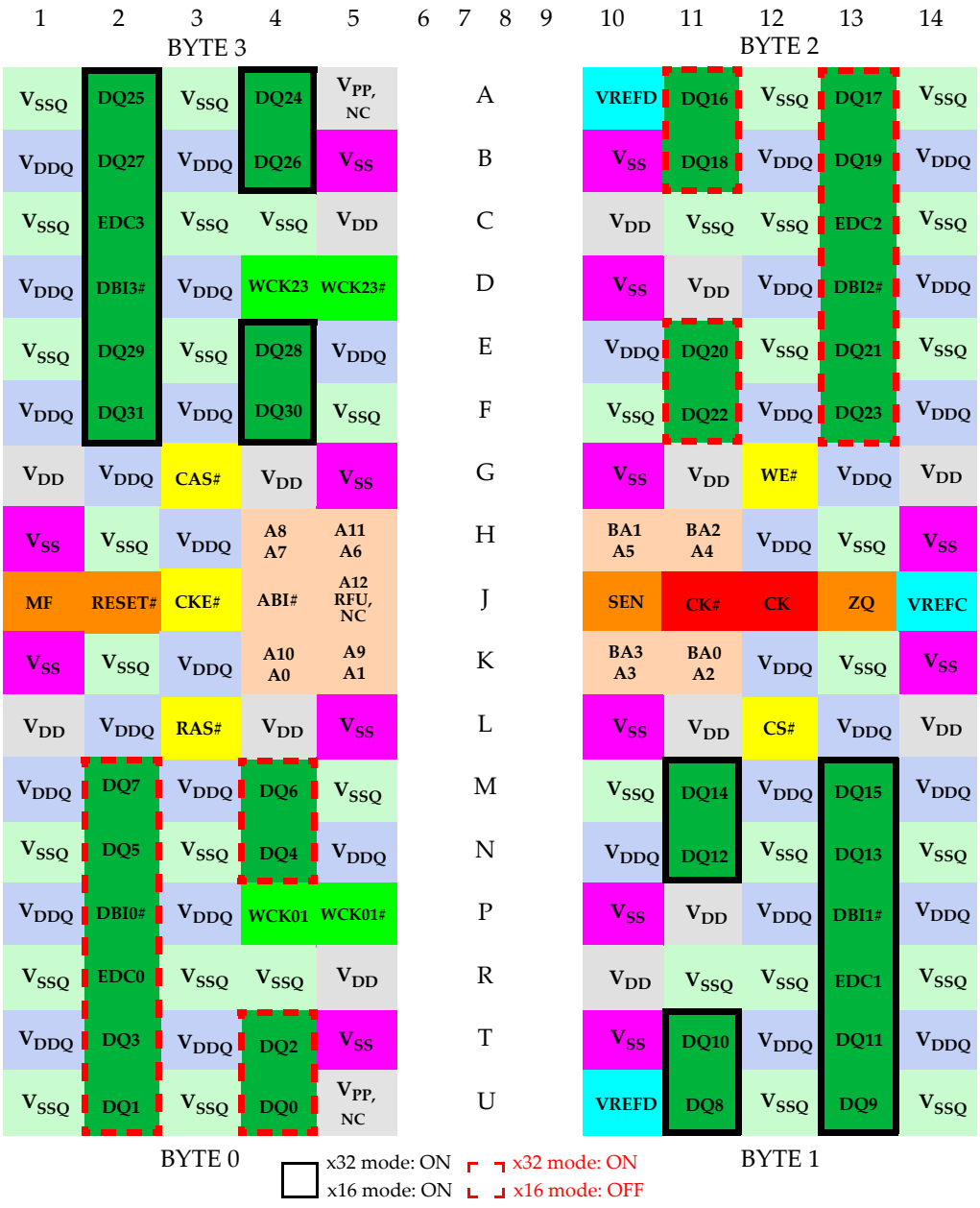


Note) Top View (as seen thru package), MF = LOW (MF = 0)

Figure 81. GDDR5 SGRAM 170ball BGA Ball-out MF=0

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Note) Top View (as seen thru package), MF = HIGH (MF = 1)

Figure 82. GDDR5 SGRAM 170ball BGA Ball-out MF=1

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7.1. SIGNALS

Table 54. Ball-out Description

SYMBOL	TYPE	DESCRIPTION
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. Command inputs are latched on the rising edge of CK. Address inputs are latched on the rising edge of CK and the rising edge of CK#. All latencies are referenced to CK. CK and CK# are externally terminated.
WCK01, WCK01#, WCK23, WCK23#	Input	Write Clocks: WCK and WCK# are differential clocks used for WRITE data capture and READ data output. WCK01/WCK01# is associated with DQ0-DQ15, DBI0#, DBI1#, EDC0 and EDC1. WCK23/WCK23# is associated with DQ16-DQ31, DBI2#, DBI3#, EDC2 and EDC3.
CKE#	Input	Clock Enable: CKE# LOW activates and CKE# HIGH deactivates the internal clock, device input buffers, and output drivers. Taking CKE# HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE# must be maintained LOW throughout read and write accesses. The value of CKE# latched at power-up with RESET# going High determines the termination value of the address and command inputs.
CS#	Input	Chip Select: CS# LOW enables and CS# HIGH disables the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code.
RAS#, CAS#,WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
BA0–BA3	Input	Bank Address Inputs: BA0 - BA3 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0-BA3 also determine which Mode Register is accessed with an MODE REGISTER SET command. BA0-BA3 are sampled with the rising edge of CK.
A0–A11 (A12)	Input	Address Inputs: A0-A11 (A12) provide the row address for ACTIVE commands, A0-A5 (A6) provide the column address and A8 defines the auto precharge function for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0-BA3) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during a LDFF command. A8-A11(A12) are sampled with the rising edge of CK and A0-A7 are sampled with the rising edge of CK#.
DQ0–31	I/O	Data Input/Output: 32-bit data bus
DBI#0-3	I/O	Data Bus Inversion. DBI#0 is associated with DQ0-DQ7, DBI#1 is associated with DQ8-DQ15, DBI#2 is associated with DQ16-DQ23, DBI#3 is associated with DQ24-DQ31.
EDC0-3	Output	Error Detection Code. The calculated CRC data is transmitted on these pins. In addition these pins drive a 'hold' pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ0-DQ7, EDC1 is associated with DQ8-DQ15, EDC2 is associated with DQ16-DQ23, EDC3 is associated with DQ24-DQ31.
ABI#	Input	Address Bus Inversion
VddQ	Supply	I/O Power Supply. Isolated on the die for improved noise immunity.
VssQ	Supply	I/O Ground: Isolated on the die for improved noise immunity.
Vdd	Supply	Power Supply
Vss	Supply	Ground
Vrefd	Supply	Reference Voltage for DQ, DBI#, and EDC pins.
Vrefc	Supply	Reference Voltage for address and command pins.
Vpp	Supply	Pump Voltage
MF	Reference	Mirror Function: VDDQ CMOS input. Must be tied to power or ground.
ZQ	Reference	External Reference Pin for autocalibration

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Table 54. Ball-out Description

SYMBOL	TYPE	DESCRIPTION
RFU		Reserved for Future Use
NC		Not connected
SEN	Input	Scan enable. VDDQ CMOS input. Must be tied to the ground when not in use.
RESET#	Input	Reset Pin. VDDQ CMOS input. RESET# Low asynchronously initiates a full chip reset. With RESET# Low all ODTs are disabled.

Figure clarifies the use of the MF=0 and MF=1 ball-outs in x16 mode and why the bytes are renumbered to give the controller the view of the same bytes that a controller sees with a single x32 device. This is important for Address Training, DM and EDC functionality. For more details see the x16 enable and MF enable section.

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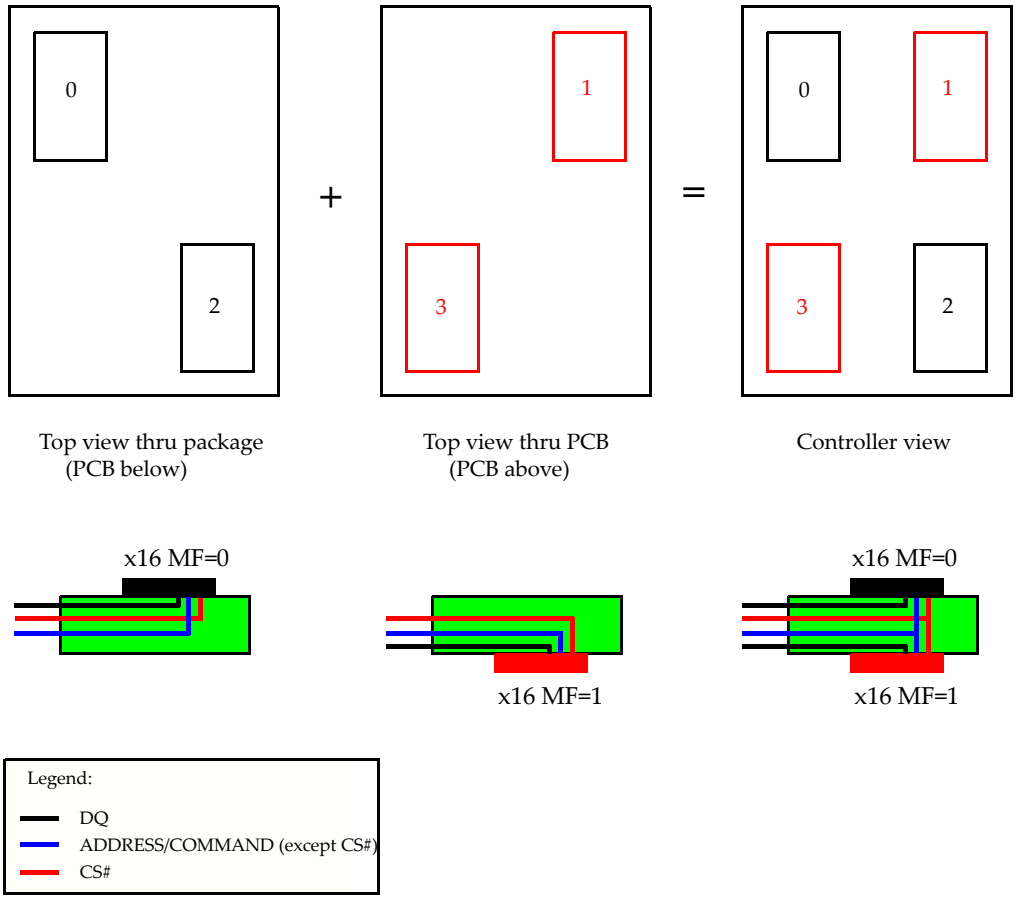


Figure 83. Byte Orientation in Clamshell Topology

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7.2. ON DIE TERMINATION (ODT)

GDDR5 SGRAMs support multiple termination modes for its high speed input signals. When the termination is enabled for a receiver, an impedance defined for that termination mode is applied between that input receiver and the VDDQ supply rail. This is commonly referred to as VDDQ termination. Registers have been defined to control the termination modes. ADD/CMD Termination is controlled using MR1 bits A4 and A5. Data termination is controlled using MR1 bits A2 and A3. WCK termination is controlled using MR3 bits A8 and A9.

Table 55 includes all the high speed GDDR5 SGRAM signals whose receivers include on die termination to VDDQ and whether their termination can be disabled by ADD/CMD Term, DQ Term, or WCK Term. A "Yes" indicates whether the mode register field controls termination for the signal.

Table 55. Signals Affected by Termination Control Registers

	ADD/CMD Term MR1 (A4,A5)		DQ Term MR1 (A2,A3)		WCK Term MR3 (A8,A9)	
Signal	**x32**	**x16**	**x32**	**x16**	**x32**	**x16**
RAS#, CAS#, WE, CS#, CKE#	Yes	Yes	No	No	No	No
A10/A0, A9/A1, BA0/A2, BA3/A3, BA2/A4, BA1/A5, A11/A6, A8/A7, A12/RFU/(NC), ABI#	Yes	Yes	No	No	No	No
DQ[7:0], DBI0#	No	No	Yes	Yes	No	No
DQ[15:8], DBI1#	No	Disabled	Yes	Disabled	No	Disabled
DQ[23:16], DBI2#	No	No	Yes	Yes	No	No
DQ[31:24], DBI3#	No	Disabled	Yes	Disabled	No	Disabled
WCK01, WCK01#, WCK23, WCK23#	No	No	No	No	Yes	Yes

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7.3. PACKAGE OUTLINE

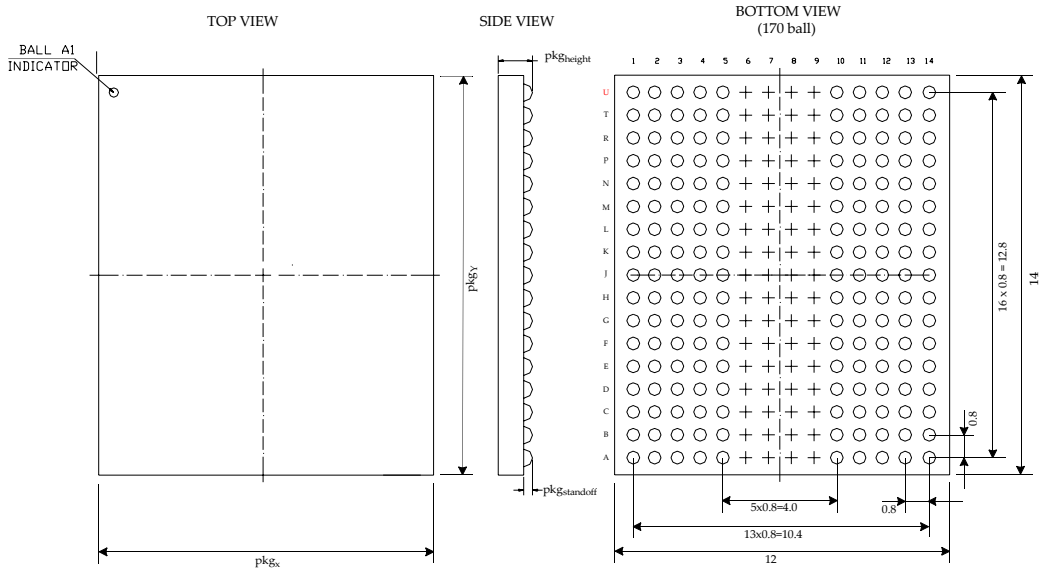


Figure 84. Package Dimensions

Table 56. Package Height Parameters

	Nominal	Variation
$pkg_{standoff}$	0.350	+/- 0.050
pkg_{height}	1.100	+/- 0.100

Notes:
1) GDDR5 package height specification is compliant to MO-207 Rev L, variation DAA-z

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7.4. MIRROR FUNCTION (MF) ENABLE and x16 MODE ENABLE

The GDDR5 SGRAM provides a mirror function (MF) pin to change the physical location of the command, address, data, and WCK pins assisting in routing devices back to back. The MF ball should be tied directly to VSSQ or VDDQ depending on the control line orientation desired.

The GDDR5 SGRAM can operate in a x32 mode or a x16 mode to allow a clamshell configuration with a point to point connection on the high speed data signal. The disabled pins in x16 mode should all be in a Hi-Z state, non-terminating.

The x16 mode is detected at power up on the pin at location C-13 which is EDC1 when configured to MF=0 and EDC2 when configured to MF=1. For x16 mode this pin is tied to VSSQ; the pin is part of the two bytes that are disabled in this mode and therefore not needed for EDC functionality. For x32 mode this pin is active and always terminated to VDDQ in the system or by the controller. The configuration is set with RESET# going High. Once the configuration has been set, it cannot be changed during normal operation. Usually the configuration is fixed in the system. Details of the x16 mode detection are depicted in Figure . A comparison of x32 mode and x16 mode systems is shown in Figure .

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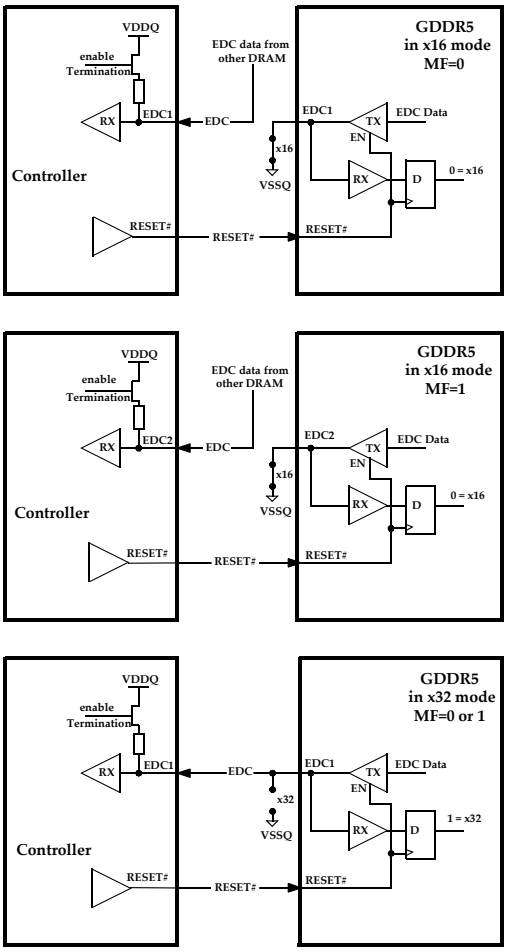


Figure 85. Enabling x16 mode

Table 57. x16 mode and MF

MODE	MF	EDC1 (MF=0) or EDC2 (MF=1)
x16 non-mirrored	VSSQ	VSSQ
x32 non-mirrored	VSSQ	VDDQ (terminated by the system or controller)
x16 mirrored	VDDQ	VSSQ
x32 mirrored	VDDQ	VDDQ (terminated by the system or controller)

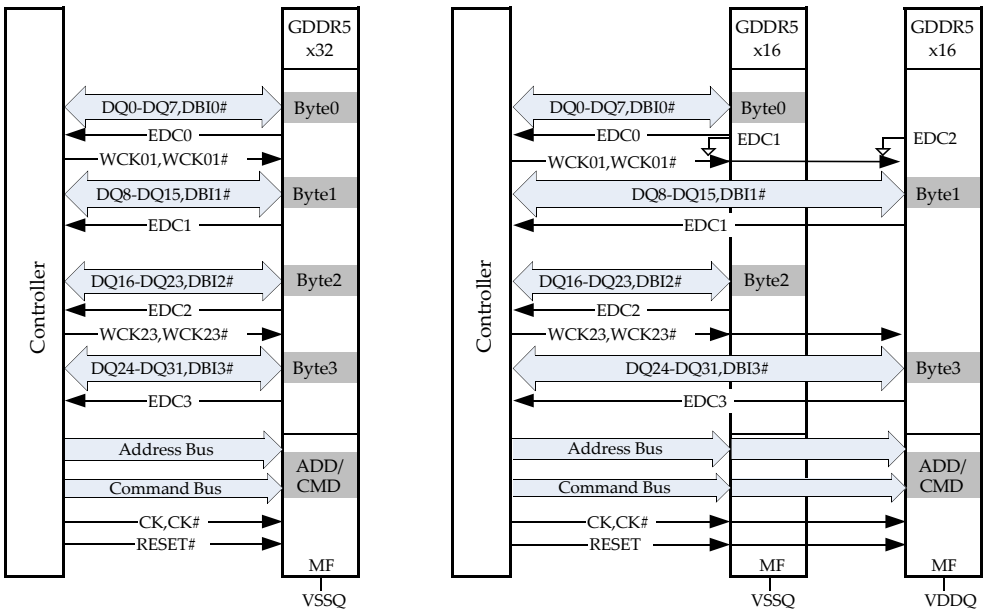


Figure 86. System view for x32 mode vs. x16 mode

Figure 86 and Figure 87 show examples of the board channels and topologies that are supported in GDDR5 in order to illustrate the expected usage of x16 mode and the MF pin.

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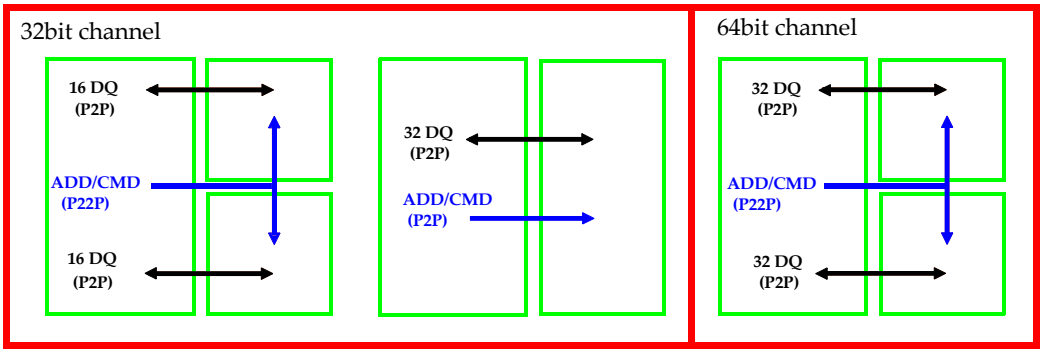
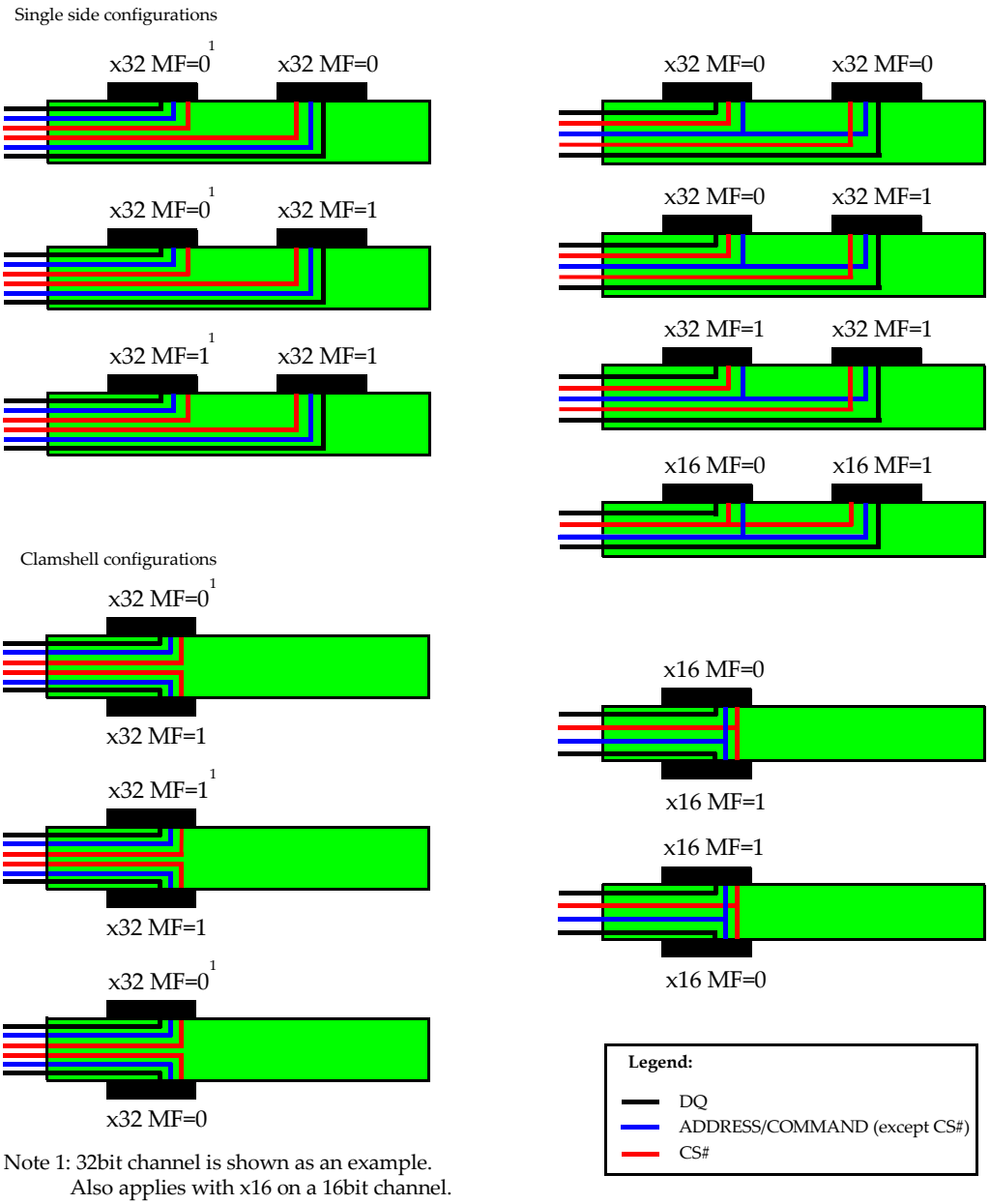


Figure 87. Example Channel Topologies

For flexibility of PCB routing GDDR5 SGRAM devices, the ball-out includes definition of both MF=0 and MF=1. The following simple block diagrams in Figure 88 demonstrate some of the flexibility of PCB routing.

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Note 1: 32bit channel is shown as an example.
Also applies with x16 on a 16bit channel.

Figure 88. Example GDDR5 PCB Layout Topologies

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BOUNDARY SCAN

The GDDR5 SGRAM incorporates a modified boundary scan test mode. This mode does not operate in accordance with IEEE Standard 1149.1-1990. To save the current GDDR5 SGRAM's ball-out, this mode will scan the parallel data input and output the scanned data on EDC0 located at C-2 controlled by an add-on pin, SEN which is located at J-10 of the 170 ball package.

Scan mode is entered directly after power-up while the device is in reset state. This ensures that no unwanted access commands are being executed prior to scan mode.

Boundary scan does not distinguish between x16 and x32 modes, and data is captured on all pins. The user has to make sure to mask those bits in the test program which are not wired in the system.

For normal device operation, i.e. after scan mode operation, it is required that device re-initialization occurs through device power-down and then power-up.

It is possible to operate the GDDR5 SGRAM without using the boundary scan feature. SEN should be tied Low to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode (RESET#, MF, EDC0 and CS#) will be operating as normal when SEN is deasserted.

Table 58. Boundary Scan Exit Order

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-5	13	J-3	25	T-2	37	M-11	49	E-13
2	D-4	14	K-4	26	T-4	38	M-13	50	E-11
3	D-2	15	K-5	27	U-2	39	L-12	51	D-13
4	E-4	16	L-3	28	U-4	40	K-10	52	C-13
5	E-2	17	M-2	29	U-11	41	K-11	53	B-13
6	F-4	18	M-4	30	U-13	42	J-13	54	B-11
7	F-2	19	N-2	31	T-11	43	J-12	55	A-13
8	G-3	20	N-4	32	T-13	44	J-11	56	A-11
9	H-5	21	P-2	33	R-13	45	H-11	57	A-4
10	H-4	22	P-4	34	P-13	46	H-10	58	A-2
11	J-5	23	P-5	35	N-11	47	F-13	59	B-4
12	J-4	24	R-2	36	N-13	48	F-11	60	B-2

Note: When the device is in scan mode, mirror function is disabled (MF=0) and none of the pins are remapped.

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Table 59. Scan Pin Description

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
J-2	SSH	RESET#	Input	Scan Shift: capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
G-12	SCK	CS#	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to the rising edge of the scan clock.
C-2	SOUT	EDC0	Output	Scan Output.
J-10	SEN	RFU	Input	Scan Enable: logic HIGH enables scan mode. Scan mode is disabled at logic LOW. Must be tied to VSSQ when not in use.
J-1	SOE#	MF	Input	Scan Output Enable: enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDDQ or GND through a resistor (typically 1K Ohm) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

Notes:
1. When SEN is asserted, no commands are to be executed by the GDDR5 SGRAM. This applies to both user commands and manufacturing commands which may exist while RESET# is deasserted.
2. All scan functionality is valid only after the appropriate power-up (Steps 1-4 of initialization sequence).
3. In scan mode, all ODT will be disabled.

Table 60. Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock					
Clock cycle time	t_{SCK}	40	-	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	-	ns	1
Scan enable hold time	t_{SEH}	20	-	ns	1
Scan command setup time for SSH, SOE# and SOUT	t_{SCS}	14	-	ns	1
Scan command hold time for SSH, SOE# and SOUT	t_{SCH}	14	-	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	-	ns	1
Scan capture hold time	t_{SDH}	10	-	ns	1

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Table 60. Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	-	6	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	-	ns	1

Notes:
1. The parameter applies only when SEN is asserted.

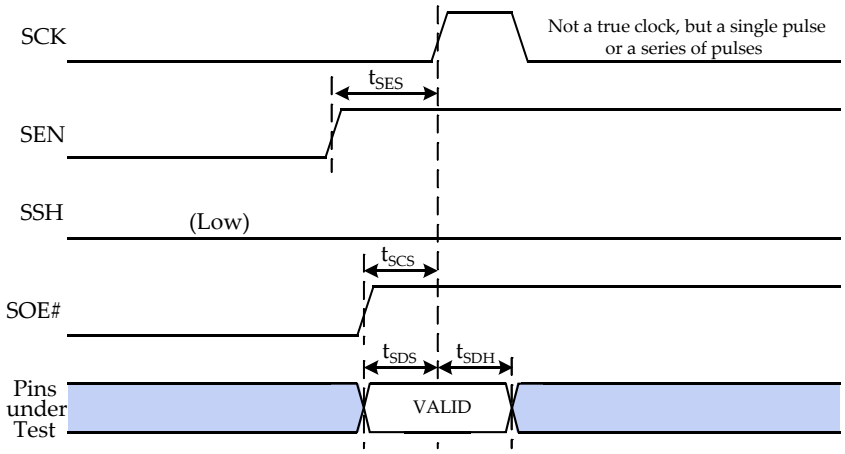


Figure. 89 Scan Capture Timing

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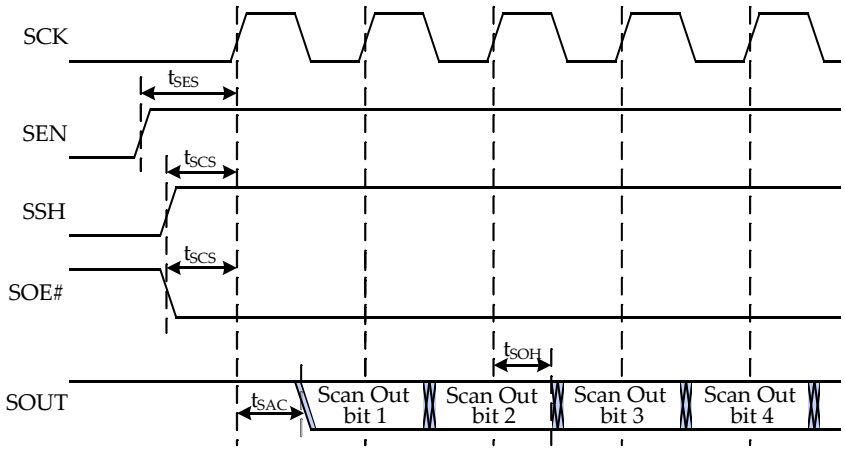


Figure. 90 Scan Shift Timing

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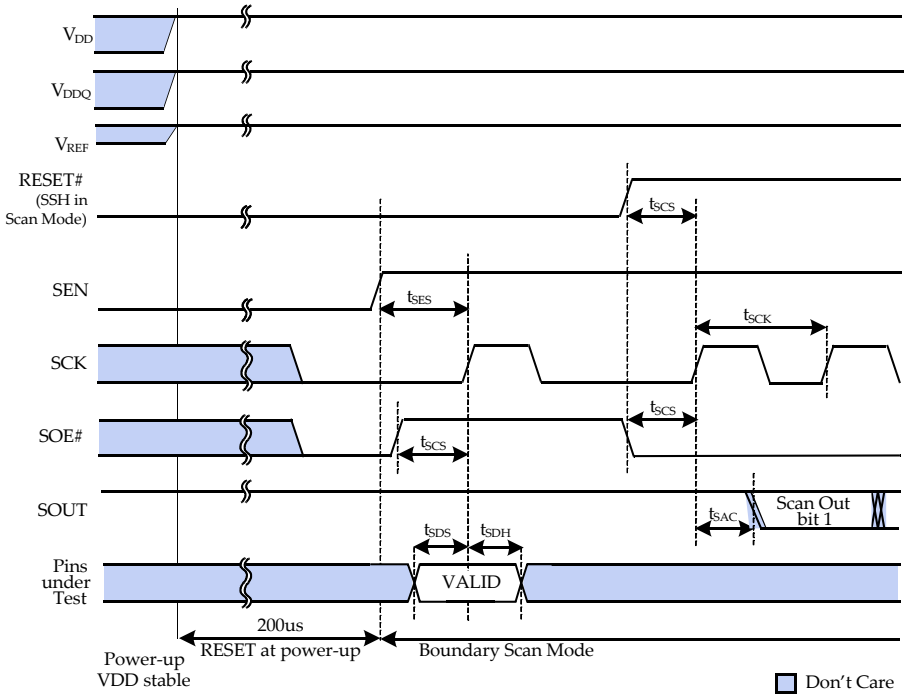


Figure 91. Scan Initialization Sequence

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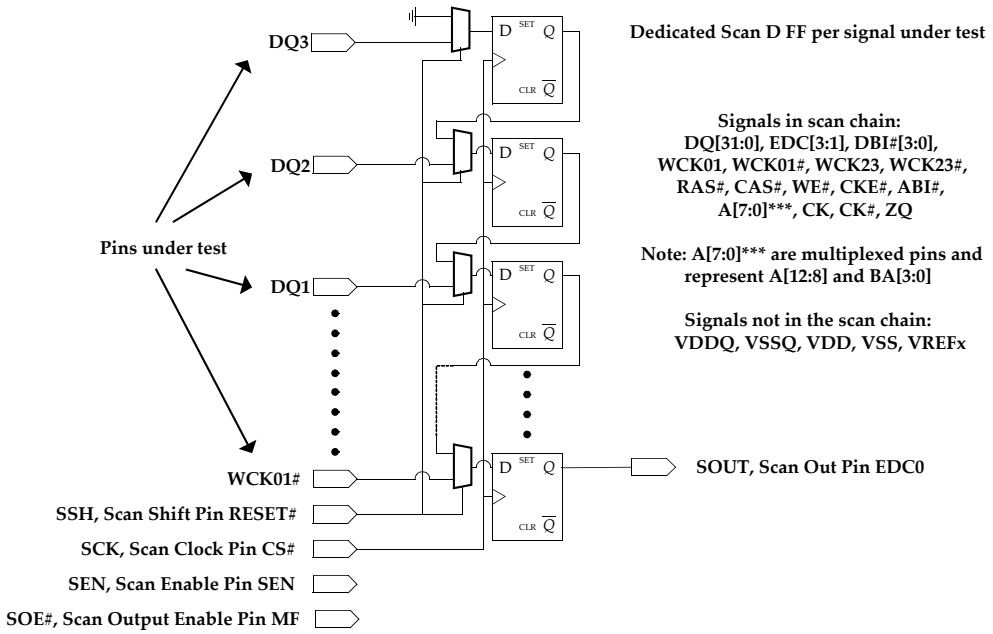


Figure. 92 Internal Block Diagram

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