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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co. Ltd.	Case No. IPR2022-01427
Petitioner,	Patent No. 9,318,160
vs.	
Netlist, Inc.,	Case No. IPR2022-01428
Patent Owner.	Patent No. 8,787,060

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VIDEOCONFERENCE DEPOSITION OF ANDREW WOLFE, Ph.D.

Tuesday, June 27, 2023

Volume I (Pages 1 - 191)

Reported Remotely and Stenographically by:
JANIS JENNINGS, CSR No. 3942, CLR, CCRR
Job No. 5965315

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DEPOSITION OF ANDREW WOLFE, Ph.D.,
appearing remotely, located in Santa Clara,
California, taken on behalf of the Petitioner,
beginning at 8:58 a.m., on Tuesday, June 27,
2023, sworn remotely by Janis Jennings, Certified
Shorthand Reporter No. 3942, CCRR, located in the
City of Walnut Creek, County of Contra Costa,
State of California.

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1 Tuesday, June 27, 2023; 9:00 a.m.

2

3 ANDREW WOLFE,

4 the witness herein, was sworn and

5 testified as follows:

6

7 EXAMINATION

8

9 BY MS. ZHONG: 08:58

10 Q. Good morning, Dr. Wolfe. Can you please 08:58

11 state your name for the record. 08:58

12 A. Andrew Wolfe. 08:58

13 Q. Okay. Dr. Wolfe, you submitted two 08:58

14 declarations, one for patent number ending with '060 08:58

15 and the other for patent number ending with '160; is 08:58

16 that correct? 08:58

17 A. Correct. 08:58

18 Q. Do you have all the exhibits that's already 08:58

19 in the record with you, at least electronically? 08:58

20 A. No. I have printed a small subset of the 08:58

21 exhibits and I have access to your Exhibit Share, 08:58

22 which also has a subset of exhibits. 08:58

23 Q. Okay. Do you have Exhibit 1016, which is US 08:58

24 publication 2011/0026293 Riho, with you? 08:59

25 A. Yes. 08:59

Page 6

1 Q. Okay. Can you please pull up that exhibit. 08:59
2 A. I don't seem to have the ability to download 08:59
3 the exhibits. 08:59
4 Q. What about from the Exhibit Share? It 08:59
5 should be -- 08:59
6 A. Oh, yes, I do. I just have to use a 08:59
7 different set of clicks than I was. Okay. 08:59
8 Q. Let me know when you have the exhibit. 08:59
9 A. I do. 08:59
10 Q. Okay. 08:59
11 A. No, actually -- 08:59
12 Q. Do you have --
13 A. Sorry. Give me the exhibit number again. 08:59
14 Q. 1016. Exhibit 1016. 09:00
15 A. Okay. Sorry. I downloaded the wrong Riho. 09:00
16 Give me one second. 09:00
17 Q. Okay. 09:00
18 A. Okay. 09:00
19 Q. Do you have it? 09:00
20 A. Yes. 09:00
21 Q. Okay. You have reviewed this application 09:00
22 before; correct? 09:00
23 A. Yes. 09:00
24 Q. And you are pretty familiar with the content 09:00
25 of this particular reference; correct? 09:00

1	A. Yes.	09:00
2	Q. Can you please turn to Figure 4 and 5 of	09:00
3	Riho.	09:00
4	A. Okay.	09:00
5	Q. In Riho, as shown in Figure 4, there are	09:00
6	16 stacked SDRAMs; is that correct?	09:01
7	A. In this particular example in Figure 4,	09:01
8	there are 16 stacked SDRAM dies and what Riho calls,	09:01
9	I believe, a master die model.	09:01
10	Q. Okay. And there are multiple TSVs going --	09:01
11	each one of them going through 16 of the dies; is	09:01
12	that correct?	09:01
13	MR. CHANDLER: Objection. Form.	09:01
14	THE WITNESS: Riho teaches that there are	09:01
15	more than 300 and gives us some -- a breakdown, but	09:01
16	I think -- I believe four of them are illustrated in	09:01
17	Figure 4.	09:01
18	BY MS. ZHONG:	09:01
19	Q. Okay. And each of the TSVs goes through	09:01
20	each of the SDRAMs; correct?	09:01
21	MR. CHANDLER: Object to form.	09:02
22	THE WITNESS: Each physically penetrates	09:02
23	through each of the chips, but they are only	09:02
24	electrically connected to, depending on the	09:02
25	embodiment, one or two of the chips.	09:02

Page 8

1 BY MS. ZHONG:

2 Q. Okay. So let's take a look at Figure 5 to 09:02
3 see the electrical connection of one of the TSVs to 09:02
4 each of the array dies. 09:02

5 So in Figure 5, it shows a connection with 09:02
6 TSV 715 to each of the array dies -- SDRAM dies; is 09:02
7 that correct? 09:02

8 A. No. No. What it is showing is that -- 09:02

9 Q. Okay.

10 A. -- in a certain embodiment, TSV 715 is 09:02
11 electrically connected to the D15 die and it's 09:02
12 electrically connected to the D17 die -- I'm sorry, 09:02
13 the D7 die, but it is disconnected from the 09:03
14 remaining SDRAM die. 09:03

15 Q. Okay. So in the circuitry in each of the 09:03
16 SDRAMs, the chip internal circuit in each of the 09:03
17 SDRAMs are identical; is that correct? 09:03

18 MR. CHANDLER: Objection. Form. 09:03

19 BY MS. ZHONG: 09:03

20 Q. Take a look at paragraph 76 of Riho. 09:03

21 A. No. That 76 says they have the same 09:03
22 equivalent circuit. That equivalent circuit is 09:03
23 talking about what's in the small box of D15 in 09:03
24 Figure 5 showing L1, R2 and C2, and it's meant to 09:04
25 represent the AC and DC load that is presented when 09:04

1 an electrical connection is present. 09:04

2 Q. Okay. And in each of the die, there are two 09:04

3 switches, sa and sb; is that correct? 09:04

4 A. That's exemplary. There are an sa and an sb 09:04

5 for each through silicon via and, as I mentioned, 09:04

6 there are more than 300 of those. 09:04

7 Q. Okay. And the TSV that is shown in Figure 5 09:04

8 is a TSV 715; is that correct? 09:04

9 A. Yes. That is the example that's illustrated 09:05

10 in Figure 5. 09:05

11 Q. Okay. And there is an R1C1 circuit that is 09:05

12 shown as part of TSV 715; is that correct? 09:05

13 A. I don't think "circuit" is the best word. 09:05

14 It is an equivalent to a circuit. 09:05

15 Q. Okay.

16 A. It is a model used to illustrate what the 09:05

17 effective resistant capacitive load would be of that 09:05

18 portion of the through silicon via. 09:05

19 Q. Okay. So --

20 A. It's not intended to represent the actual 09:05

21 physical circuit. 09:05

22 Q. Okay. So each segment of the TSV in the -- 09:05

23 in one of the SDRAMs is represented by a C1R1 09:05

24 circuit? 09:05

25 MR. CHANDLER: Objection. Form. 09:05

1 THE WITNESS: Each portion of the through 09:05
2 silicon via interconnect is modeled by a C1R1 09:06
3 circuit in Figure 5 to represent -- 09:06
4 BY MS. ZHONG:
5 Q. Okay.
6 A. -- the effective resistance and capacitance 09:06
7 that that physical structure would contribute to the 09:06
8 circuit behavior. 09:06
9 DEPOSITION REPORTER: Excuse me, Miss Zhong. 09:06
10 Can I please go off the record. 09:06
11 MS. ZHONG: Sure. 09:06
12 (Off the record.) 09:06
13 BY MS. ZHONG: 09:09
14 Q. So, Dr. Wolfe, each of the C1R1 equivalent 09:09
15 circuit is shown in Figure 5 Riho as connected to 09:09
16 the switch circuit A, sa and switch circuit B, sb; 09:09
17 is that correct? 09:09
18 MR. CHANDLER: Object to form. 09:09
19 THE WITNESS: No, that's incorrect. 09:09
20 DEPOSITION REPORTER: Excuse me one moment, 09:09
21 Miss Zhong. Can you adjust your camera down a
22 little bit. I need to see your mouth when you're
23 looking at the exhibits. It helps between "D" and
24 "B." Thank you.
25 / / / 09:09

1 BY MS. ZHONG: 09:09
2 Q. Why is it incorrect? 09:09
3 A. Because R1 and C1 don't physically exist. 09:09
4 Q. I said the "equivalent circuit" is shown as 09:09
5 connected to the sa and sb circuits. 09:10
6 MR. CHANDLER: Objection. Form. 09:10
7 THE WITNESS: Can I hear the entire question 09:10
8 again? 09:10
9 BY MS. ZHONG: 09:10
10 Q. So in Figure 5, the C1R1 equivalent circuit 09:10
11 in each of the portions is shown as connected to 09:10
12 switch circuits A and B; is that correct? 09:10
13 MR. CHANDLER: Objection. Form. 09:10
14 THE WITNESS: Again, I don't know what it 09:10
15 means to say that it's connecting when it doesn't 09:10
16 physically exist. 09:10
17 That is an illustration that's provided in 09:10
18 Figure 5 that -- that on one side of the switch, 09:10
19 there is an equivalent load that is modeled as R1 09:10
20 and C1, and depending on how the switch is set, the 09:10
21 switch can either electrically connect the MOS 09:11
22 driver or not electrically connect the MOS driver. 09:11
23 BY MS. ZHONG: 09:11
24 Q. But there are physical connections between 09:11
25 the circuits and the load of the TSV; is that 09:11

1 correct? 09:11

2 MR. CHANDLER: Objection. Form. 09:11

3 THE WITNESS: I don't know what circuits 09:11

4 you're talking about. 09:11

5 BY MS. ZHONG: 09:11

6 Q. So you said C1R1 is representing the load on 09:11

7 each portion of the PSD; is that correct? 09:11

8 A. TSV -- yeah, the R1C1 is representative of 09:11

9 the load that the physical portion of the 09:11

10 through-silicon via 715 would provide if it were 09:11

11 connected to -- electrically to a driver circuit. 09:12

12 Q. Okay. And what is shown here is that the 09:12

13 load would be connected to each of the circuits sa 09:12

14 and sb. So they are physical connections to it, but 09:12

15 those circuits might be turned off digitally by the 09:12

16 control signal; is that correct? 09:12

17 MR. CHANDLER: Objection. Form. 09:12

18 THE WITNESS: No. I don't think that's 09:12

19 right. So that's a representation of the load that 09:12

20 would be provided to a driver. There's really no 09:12

21 load that's provided to an off switch so that would 09:12

22 no longer be the appropriate model. 09:12

23 BY MS. ZHONG: 09:13

24 Q. So in each of the SDRAMs, there are two 09:13

25 switch circuits, sa and sb; correct? 09:13

1 MR. CHANDLER: Objection. Form. 09:13

2 THE WITNESS: Well, again, I don't want 09:13

3 there to be a misunderstanding. There are in fact 09:13

4 over 700 switch circuits, but two of them for each 09:13

5 SDRAM are illustrated in Figure 5. 09:13

6 BY MS. ZHONG: 09:13

7 Q. Okay. So for each TSV -- let me put it this 09:13

8 way. 09:13

9 In each of the SDRAMs, for each TSV, there 09:13

10 are two switch circuits, sa and sb; is that correct? 09:13

11 MR. CHANDLER: Objection. Form. 09:13

12 THE WITNESS: For each TSV and each die in 09:13

13 the stack, there are two switches, sa and sb. 09:14

14 BY MS. ZHONG: 09:14

15 Q. And does the on and off state of those 09:14

16 switches -- are controlled by control signals, chip 09:14

17 select signals and the D715 signals from ROM1 and 09:14

18 ROM2; is that correct? 09:14

19 MR. CHANDLER: Objection. Form. 09:14

20 THE WITNESS: It depends on the embodiment, 09:14

21 but they are all controlled by some type of control 09:14

22 signal. 09:14

23 BY MS. ZHONG: 09:14

24 Q. Okay. So what I just wanted to establish is 09:14

25 that as shown in Figure 5, for each of the portion 09:14

1 of the TSV in each die, there are two circuits whose 09:14
2 on and off states are determine by control signals? 09:15
3 A. It depends what your definition of a circuit 09:15
4 is, but there are definitely two transistor switches 09:15
5 that can be turned on or off based on control 09:15
6 signals that come from ROMs. 09:15
7 Q. You seem to be having some problem with 09:15
8 my use of the word "circuit." What is your 09:15
9 understanding of the term "circuit"? 09:15
10 A. There are different definitions that are 09:15
11 used in different contexts. 09:15
12 Q. Okay. 09:15
13 A. The most common one that I use in this kind 09:15
14 of a context is that it is simply an interconnection 09:15
15 of electronic components, but there are some times 09:15
16 in some context where people use the word "circuit" 09:16
17 to mean something that has a complete electrical 09:16
18 path. And that -- 09:16
19 Q. Okay. 09:16
20 A. -- the common dictionary definition and 09:16
21 these switches don't meet that definition. 09:16
22 Q. Okay. So do you see the word "C1R1 09:16
23 Circuit," "Chip Internal Circuit," "Selection 09:16
24 Control Circuit" in Figure 5? 09:16
25 A. Yes. 09:16

1 Q. What's the meaning of the circuit here? 09:16
2 A. I think it's the first one that I gave you. 09:16
3 It's simply a collection of electronic components 09:16
4 that are interconnected. 09:16
5 Q. Okay. So why is the switch -- why doesn't 09:16
6 the -- let me withdraw and ask. 09:16
7 Why doesn't the sa and sb meet that 09:16
8 definition? 09:17
9 A. They do meet that definition. They may not 09:17
10 meet the other definition. 09:17
11 MR. CHANDLER: There is an objection to 09:17
12 form. 09:17
13 BY MS. ZHONG: 09:17
14 Q. Okay. So what you are saying is sa and sb 09:17
15 does meet your first definition, but it might not 09:17
16 meet your second definition that's used less 09:17
17 commonly; is that right? 09:17
18 A. Correct. 09:17
19 Q. Okay. And the sa and sb switch circuits 09:17
20 connect the MOS driver to the load; is that correct? 09:17
21 To the TSV load? 09:17
22 MR. CHANDLER: Objection to form. 09:17
23 THE WITNESS: When they are turned on, they 09:17
24 connect them. When they are turned off, they do not 09:17
25 connect them. 09:17

1 BY MS. ZHONG: 09:18

2 Q. Okay. And when the -- when switch sa and sb 09:18

3 are both turned off, does the TSV experience the 09:18

4 load from the SDRAM memory arrays? 09:18

5 MR. CHANDLER: Objection. Form. 09:18

6 THE WITNESS: No. 09:18

7 BY MS. ZHONG: 09:18

8 Q. Does the driver -- does the driver in the 09:18

9 L1R1C2 equivalent circuit impose a load on the TSV? 09:19

10 MR. CHANDLER: Objection. Form. 09:19

11 THE WITNESS: It's not a normal way we would 09:19

12 phrase that discussion. The load gets -- 09:19

13 DEPOSITION REPORTER: Excuse me, Dr. Wolfe.

14 Can you start your answer again. "The load..." 09:19

15 THE WITNESS: So that would not be the 09:19

16 normal way we would phrase that question. The load 09:19

17 is presented to the driver, not to the TSV -- 09:19

18 BY MS. ZHONG:

19 Q. Okay. 09:20

20 A. -- and, therefore, the question of interest 09:20

21 essentially is does the driver on another die 09:20

22 present a load to another driver that's trying to 09:20

23 drive through the TSV, and the answer here would be 09:20

24 that when the switch is on, connected to a 09:20

25 particular driver, it does add to the load; and when 09:20

1 the switch is off, connected to a particular driver, 09:20
2 it does not add to the load. 09:20
3 Q. Okay. Can you please pull up Exhibit -- let 09:20
4 me see which one it is -- the Ellsberry exhibit. I 09:20
5 believe it is 1026. 09:20
6 A. Okay. 09:21
7 Q. Tell me when you have it. 09:21
8 A. I do. 09:21
9 Q. Okay. Can you go to Figure 4 of Ellsberry. 09:21
10 A. Sure. I haven't looked at Ellsberry for 09:21
11 some time, but I will do my best to answer 09:21
12 questions. 09:21
13 Q. Okay. In Ellsberry, do you see that there 09:21
14 are -- there's a flip-flop -- two flip-flops and two 09:21
15 read drivers -- 09:22
16 (Clarification requested by Reporter.)
17 MS. ZHONG: Let me just withdraw and ask. 09:22
18 BY MS. ZHONG:
19 Q. Do you see that in Figure 4 of Ellsberry, 09:22
20 there are two boxes numbered 402 and 404? 09:22
21 A. I see that. 09:22
22 Q. Okay. And in each of the boxes, there is a 09:22
23 triangle with the word "Read" in it. 09:22
24 What is that? 09:22
25 A. That is a read driver that is used to 09:22

1 propagate signals from Port A or Port B to the DQ 09:22
2 port. 09:22
3 Q. Okay. And there is also a square with the 09:22
4 word "Write" in it. Is that a flip-flop? 09:22
5 A. It is a flip-flop. One would understand 09:22
6 there to be a driver there as well, either not 09:23
7 illustrated or built into the flip-flop. 09:23
8 Q. Okay. So if the -- both the read driver and 09:23
9 the flip-flop, including the drivers, are turned 09:23
10 off, is there a load presented -- let's just say 09:23
11 like the read driver and the write drivers in box 09:23
12 402 are both turned off. 09:23
13 MR. CHANDLER: Objection. Form. 09:23
14 BY MS. ZHONG: 09:23
15 Q. Is there a load from the memory dies that's 09:23
16 connected to that box on path 234? 09:23
17 MR. CHANDLER: Objection. Form. 09:23
18 THE WITNESS: What do you mean by turned 09:23
19 off? 09:24
20 BY MS. ZHONG: 09:24
21 Q. Try to save it, for example. 09:24
22 DEPOSITION REPORTER: Miss Zhong, can we go 09:24
23 off the record, please. 09:24
24 MS. ZHONG: Yes. 09:24
25 (Off the record.) 09:24

1 THE WITNESS: So the tri-stating of the read 09:25
2 buffer in 402 would have no impact on the load on a 09:26
3 driver that was driving Port A because it's on the 09:26
4 output and it would be the input of the driver that 09:26
5 is connected to Port A. So that would have no 09:26
6 impact. 09:26
7 If the write driver that is driving to 09:26
8 Port A were tri-stated, it already contributes only 09:26
9 a little bit to the load. The load primarily comes 09:26
10 from the transistor gates which are used in the 09:26
11 input direction of the circuits. 09:26
12 But if those were tri-stated -- well, 09:26
13 actually they would have to be tri-stated. They 09:26
14 would always be tri-stated if someone else was 09:26
15 driving Port A, so that's the only situation where 09:26
16 we would ever measure the load, otherwise, the 09:26
17 flip-flop would be driving Port A and the capacitive 09:26
18 load would be irrelevant because the two drivers 09:27
19 would be fighting each other. 09:27
20 You would have to look at it in some very 09:27
21 special cases. It wouldn't be the normal case you 09:27
22 would analyze. 09:27
23 BY MS. ZHONG: 09:27
24 Q. Sorry. I'm not clear. 09:27
25 So if both drivers in box 402 are disabled, 09:27

1 how many loads would the memory controller on bus 09:27
2 230 experience? Would it experience both loads from 09:27
3 Port A and Port B or only the load from Port B? 09:27
4 MR. CHANDLER: Objection. Form. 09:27
5 THE WITNESS: How many loads would what 09:27
6 experience? 09:27
7 BY MS. ZHONG: 09:27
8 Q. So at 230, bus 230, which is connected to 09:27
9 the memory driver -- memory controller. Sorry. 09:27
10 A. So the load gets analyzed based on who's 09:28
11 driving it -- 09:28
12 Q. Uh-huh.
13 A. -- but if it were being driven from an 09:28
14 external source, then the load, then that can only 09:28
15 happen when the read driver in 402 and the read 09:28
16 driver in 404 are disabled, and then the write 09:28
17 drivers would each produce essentially one load, one 09:28
18 input load, whether they were disabled or not. 09:28
19 Because this is a different configuration than -- 09:28
20 then in the other system. This doesn't use the same 09:28
21 kind of switches. These are unswitched loads. 09:28
22 Q. So what you are saying is if there is a 09:28
23 switch before the write driver, then if the driver 09:29
24 is disabled, there would only be a single load? 09:29
25 MR. CHANDLER: Objection. Form. 09:29

1 THE WITNESS: If there is a transmission 09:29
2 gate switch, like we saw in Riho, between the 09:29
3 external bus 230 and a driver 402, and that switch 09:29
4 were turned off, that would disconnect the write 09:29
5 flip-flop and remove its load from the circuit if 09:29
6 one were to build that. 09:29
7 BY MS. ZHONG: 09:29
8 Q. So why is -- so what you are saying that the 09:30
9 difference is whether it's -- the driver is 09:30
10 connected directly to the bus or whether it is 09:30
11 connected to the transmission gate that can be 09:30
12 switched on and off, that makes a difference on the 09:30
13 load? 09:30
14 A. Again, I find your question a little bit 09:30
15 vague. 09:30
16 But, in general, if a driver's input or 09:30
17 driver -- again, it depends which end you are 09:30
18 looking at. But if a driver is connected directly 09:30
19 to a bus, it will provide -- it will increase the 09:30
20 load on that bus. If a driver is disconnected by 09:30
21 having a transmission gate switch between it and the 09:30
22 bus, then it will decouple that load from the bus 09:30
23 and it will remove it. 09:31
24 Q. But if the driver is connected directly to 09:31
25 the bus without a transmission gate, the load is not 09:31

1 removed even when the driver is turned off; is that 09:31
2 right? 09:31
3 MR. CHANDLER: Objection. Form. 09:31
4 THE WITNESS: That's correct, as I 09:31
5 understand the question. Generally, when you talk 09:31
6 about whether or not a driver contributes to the 09:31
7 load on a bus, you're assuming that it's turned off 09:31
8 and there are other drivers trying to drive that 09:31
9 bus. 09:31
10 BY MS. ZHONG: 09:31
11 Q. Can you elaborate on that a little bit. 09:32
12 A. I can try. When we're doing a load analysis 09:32
13 on a bus, ordinarily, that's what we call a 09:32
14 multidrop bus, which means that there is more than 09:32
15 one driver that is capable of driving that bus, but 09:32
16 in ordinary operation, they take turns. 09:32
17 That can be done either through a technique 09:32
18 where drivers use something like a tri-state output 09:32
19 stage or it can be done through having switches to 09:32
20 decouple the drivers or it can be done using 09:32
21 techniques like open collector and open drain in 09:32
22 which -- where the drivers don't interfere with each 09:32
23 other. 09:32
24 In all those cases, the normal operation is 09:33
25 that one driver is driving current onto the bus in 09:33

1 order to change its voltage. And in order to do 09:33
2 that, it needs to overcome the electrical impedance 09:33
3 of the bus. And primarily in modern systems, that 09:33
4 means overcoming the capacitance. It needs to use 09:33
5 current to charge up the capacitance of the bus 09:33
6 before the voltage level will change. 09:33
7 Because of that, we try to determine the 09:33
8 capacitive load on the bus, which is a combination 09:33
9 of a number of things. But predominantly the 09:33
10 capacitance of the physical interconnect, the 09:33
11 capacitance of any inputs connected to that bus, and 09:33
12 the capacitance of the output stages of any disabled 09:34
13 drivers that are currently connected to that bus. 09:34
14 And all of those would contribute and the lower that 09:34
15 total number is, the faster the bus can operate. 09:34
16 Q. Okay. You mentioned a word, a "multidrop 09:34
17 bus." So in Riho, are the TSVs connected to the 09:34
18 16 array that -- 16 SDRAM dies in a multidrop 09:34
19 fashion? 09:34
20 MR. CHANDLER: Objection. Form. 09:34
21 THE WITNESS: It depends which ones. 09:34
22 Certainly, the data TSVs are because they can be 09:34
23 driven by the logic LSI chip, and then depending on 09:35
24 the embodiment, they can also be driven by one or 09:35
25 two of the memory die. Actually, I think they can 09:35

1 always possibly be driven by two of the memory die 09:35
2 depending on the switch configuration at the time. 09:35
3 Some of the control signals may not be 09:35
4 multidrop. But we would do a similar analysis, only 09:35
5 we would only include the input circuits and not 09:35
6 both the input circuits and the output circuits in 09:35
7 the case where it was not a multidrop bus. 09:35
8 BY MS. ZHONG: 09:35
9 Q. So for -- let's look at TSV 715. Is it 09:36
10 connected to SDRAM D14 in a multidrop fashion? 09:36
11 MR. CHANDLER: Objection. Form. 09:36
12 BY MS. ZHONG: 09:36
13 Q. Because the circuits -- the switch circuits 09:36
14 are there, it's just that they are turned off by the 09:36
15 control signals. 09:36
16 A. We are talking about Figure 5 -- 09:36
17 Q. Yes. 09:36
18 A. -- of Riho? 09:36
19 Q. Yes. 09:36
20 MR. CHANDLER: Objection. Form. 09:36
21 THE WITNESS: Figure 5 of Riho, the purpose 09:36
22 of the switch is to disconnect D14's circuitry from 09:36
23 TSV 715. It is configured to disconnect it and to 09:36
24 remove the capacitive load. 09:36
25 / / / 09:36

1 BY MS. ZHONG: 09:36

2 Q. Okay. But the physical circuities are 09:36

3 there? So the physical connections are there, they 09:36

4 are just turned off digitally by the control 09:36

5 circuit -- control signals? 09:37

6 MR. CHANDLER: Objection. Form. 09:37

7 THE WITNESS: Well, the interior of the 09:37

8 switch I would not describe as a connection because, 09:37

9 in its operating mode as configured, it's designed 09:37

10 to insulate and not to connect. So it's not an 09:37

11 electrical connection. It may be a physical 09:37

12 connection, but it's not an electrical connection. 09:37

13 BY MS. ZHONG: 09:37

14 Q. But would you consider that to be a 09:37

15 multidrop connection though? Part of the multidrop 09:37

16 connection? 09:37

17 MR. CHANDLER: Objection. Form. 09:37

18 THE WITNESS: No, in the configuration of 09:37

19 Figure 5, D14 has been disconnected from TSV 715. 09:37

20 The connected circuits are on the logic LSI chip D15 09:37

21 and D7. 09:37

22 BY MS. ZHONG: 09:37

23 Q. So when you say like there is a multidrop 09:37

24 configuration, you are saying that it's only with 09:38

25 respect to D15, D7 and LSI chip as far as TSV 715 is 09:38

1 concerned, but do not include any of the other 09:38
2 chips? 09:38
3 MR. CHANDLER: Objection. Form. 09:38
4 THE WITNESS: That's correct with respect 09:38
5 to Figure 5. The other 14 die are disconnected from 09:39
6 TSV 715. 09:39
7 BY MS. ZHONG: 09:39
8 Q. And as far as TSV 715 is concerned, what 09:39
9 contributes to the capacitive load the MOS driver in 09:40
10 the logic LSI chip experiences? 09:40
11 MR. CHANDLER: Objection. Form. 09:40
12 THE WITNESS: So from a perfectly -- a 09:40
13 purely theoretical perspective, everything in the 09:40
14 world contributes. So we always ask the question of 09:40
15 what contributes significantly in a meaningful way. 09:40
16 BY MS. ZHONG: 09:40
17 Q. Okay. 09:40
18 A. And in this case, it would be the MOS 09:40
19 drivers in D15 and D7 that connect through a switch 09:40
20 that is on, in addition to the physical capacitance 09:40
21 of the TSV 715 interconnect itself. 09:40
22 Q. And why I see in Riho -- 09:40
23 MR. CHANDLER: I didn't hear -- I am going 09:41
24 to object. I didn't hear the beginning of any of 09:41
25 that. 09:41

1 BY MS. ZHONG: 09:41

2 Q. Okay. So why is it that in Riho only one of 09:41

3 the die in each of the rank is -- let me withdraw 09:41

4 and ask. 09:41

5 So look at TSV 715. You said that only the 09:41

6 switch circuits for D15 and D7 are enabled and 09:41

7 connected to the respective drivers in those SDRAM 09:42

8 dies; right? 09:42

9 MR. CHANDLER: Objection. Form. 09:42

10 THE WITNESS: Yes, in the Figure 5 09:42

11 embodiment. 09:42

12 BY MS. ZHONG: 09:42

13 Q. Okay. So why does Riho design it that way? 09:42

14 In other words, why -- 09:42

15 DEPOSITION REPORTER: Ms. Zhong, I'm having 09:42

16 trouble with your audio. I don't know what 09:42

17 happened. 09:42

18 MR. CHANDLER: It got muffled. It may have 09:42

19 been your hand on your mouth. 09:42

20 BY MS. ZHONG: 09:42

21 Q. Why is it that in Riho, Figure 5, the 09:42

22 TSV 715 is not connected to, for example, SDRAM D14 09:42

23 or SDRAM D6 in addition to SDRAM D15 and SDRAM D7? 09:42

24 A. Because in operation, the Riho system only 09:43

25 interacts over TSV 715 with D7 and D15. It uses 09:43

1 another set of vias to interact with D6 and D14. It 09:43
2 does that primarily so that it can operate D15 and 09:43
3 D14 simultaneously. 09:43
4 And since D14 does not communicate through 09:43
5 TSV 715, in order to reduce the capacitive load and 09:43
6 allow this system to operate faster, Riho expresses 09:43
7 that he wants an extraordinarily high bandwidth at 09:43
8 the time out of this system. He has made the design 09:43
9 decision to not enact D14's driver circuits or D14's 09:44
10 memory array at all to TSV 715 since that would 09:44
11 offer no benefit and would needlessly slow down the 09:44
12 circuit and consume more power. 09:44
13 Q. Okay. So why can't D15 and D14 connect to 09:44
14 both TSV 715 and offer it simultaneously? 09:44
15 MR. CHANDLER: Objection. Form. 09:44
16 THE WITNESS: Because TSV 715 can only carry 09:44
17 one bit of data at a time, not one from D15 and one 09:44
18 from D14. 09:44
19 BY MS. ZHONG: 09:44
20 Q. Why can't it do that? 09:44
21 A. It's only one wire. In this configuration, 09:44
22 it can only be high or low. It can't carry values 09:45
23 at the same time from two different DRAM arrays. 09:45
24 Q. Are you saying that there could potentially 09:45
25 be data collision if the two memory dies outputs 09:45

1 different bit values? 09:45

2 MR. CHANDLER: Objection. Form. 09:45

3 BY MS. ZHONG: 09:45

4 Q. For example, one is outputting 1, the other 09:45

5 is outputting 0, then the signal can't be 09:45

6 transmitted correctly, there is going to be 09:45

7 collision? 09:45

8 MR. CHANDLER: Objection. Form. 09:45

9 THE WITNESS: Again, that is not the actual 09:45

10 configuration of Riho, but that would be one of the 09:45

11 possible problems that could occur if you were to 09:45

12 try to connect D15 and D14 both to the same TSV and 09:45

13 allow them to output at the same time. But again -- 09:45

14 BY MS. ZHONG: 09:46

15 Q. What other problems -- okay. 09:46

16 What other problems would there be if you 09:46

17 connected D15 and D14 to the same TSV and allow them 09:46

18 to output data simultaneously? 09:46

19 MR. CHANDLER: Objection. I don't think he 09:46

20 finished his previous answer. 09:46

21 THE WITNESS: I did. 09:46

22 But one of the problems, there could be 09:46

23 speed-related problems. There could be 09:46

24 current-related problems. There could be damage to 09:46

25 circuits. Again, that's not the way Riho is 09:46

1 designed. So -- 09:46

2 BY MS. ZHONG:

3 Q. I understand. 09:46

4 When you say there could be "speed-related 09:46

5 problems," what problems are you referring to in 09:46

6 specific? 09:46

7 A. Again, that's not the way Riho was designed 09:46

8 and it's not a design that makes any sense. So if 09:46

9 one were to do it in practice, one would make other 09:46

10 changes as well to make it work. 09:47

11 But Riho treats D14 and D15 as two parts of 09:47

12 the same data work. Each one supplies 32 bits. 09:47

13 They are operated at the same time and each of one 09:47

14 requires 32 wires to communicate those 32 bits. 09:47

15 That's its mode of operation. 09:47

16 If you were to redesign it, you would have 09:47

17 to make some substantial changes to -- to change the 09:47

18 way that it operates to make sure that it operates 09:47

19 correctly and effectively. You couldn't just only 09:47

20 connect D14 and D15 to the same set of vias without 09:47

21 any other changes and expect it to operate 09:47

22 correctly. 09:47

23 Q. What if D14 and D15 belonged to two 09:47

24 different ranks, so they don't operate 09:48

25 simultaneously but belong, say, for example, to the 09:48

1 same logic rank? Can you do that? 09:48
2 MR. CHANDLER: Objection. Form. 09:48
3 THE WITNESS: I don't know. That's not -- 09:48
4 BY MS. ZHONG:
5 Q. Not really -- okay. Not can you do that, 09:48
6 but would a POSITA do that? 09:48
7 MR. CHANDLER: Objection. Form. 09:48
8 DEPOSITION REPORTER: Can you repeat your 09:48
9 question, please. 09:48
10 BY MS. ZHONG: 09:48
11 Q. What if D14 and D15 belonged to two 09:48
12 different ranks so they don't operate 09:48
13 simultaneously, would a POSITA make such a 09:48
14 configuration? 09:48
15 A. I don't think they would start with Riho to 09:48
16 do that. Again, there are lots of different kinds 09:49
17 of memory configurations that a POSITA knows how to 09:49
18 do and can make work properly. 09:49
19 I would have to look at a complete design to 09:49
20 understand what the impact would be of making that 09:49
21 kind of a change, but you wouldn't make that change 09:49
22 without making other changes as well. 09:49
23 Q. What other change would you make? 09:49
24 MR. CHANDLER: Objection. Form. 09:49
25 Incomplete. 09:49

1 THE WITNESS: I don't know. I would have to 09:49
2 think it through. 09:49
3 Again, I'm not going to try to design a 09:49
4 complete working memory system based on a 09:49
5 hypothetical sitting here today. But you would make 09:49
6 sure you had the appropriate control signals and the 09:49
7 appropriate bus switching and you would analyze the 09:49
8 timing and the electrical operation and you would 09:49
9 make it work. 09:49
10 BY MS. ZHONG: 09:49
11 Q. Would that involve substantial redesign or 09:49
12 just a little bit of work? 09:49
13 MR. CHANDLER: Objection. Form. 09:50
14 THE WITNESS: I don't know until I try it. 09:50
15 Again, I wouldn't start from Riho and make that 09:50
16 particular change because it really doesn't seem to 09:50
17 be something that Riho was contemplating. There are 09:50
18 lots of other modifications one can make to Riho, 09:50
19 but making D14 and D15 not operate simultaneously 09:50
20 would not be one that I would use Riho as a starting 09:50
21 point for. 09:50
22 BY MS. ZHONG: 09:50
23 Q. And you said you would not start with Riho. 09:50
24 Is it because in Riho, D15, D14, et cetera, belong 09:50
25 to the same rank and they are intended to operate 09:51

1 simultaneously? 09:51

2 MR. CHANDLER: Objection. Form. 09:51

3 THE WITNESS: In Riho's preferred 09:51

4 embodiment, D0 through D7 are part of the same rank 09:51

5 and D8 through D15 are part of a second rank, and 09:51

6 that's the way his preferred embodiment works. 09:51

7 BY MS. ZHONG: 09:51

8 Q. Okay. What's the significance of belonging 09:51

9 to the same rank? 09:51

10 A. I'm not sure I understand the question. 09:51

11 Q. You said in Riho's preferred embodiment, 09:51

12 D0 through D7 are part of the same rank, and D8 09:51

13 through D15 are part of the second rank, and that's 09:51

14 the way his preferred embodiment works. 09:51

15 So my question to you is: What is 09:52

16 significant that D8 -- for example, D8 through D15 09:52

17 are part of one rank and D0 through D7 belongs to 09:52

18 another rank? 09:52

19 A. Again, I don't understand the question. I 09:52

20 was answering your previous question about how the 09:52

21 ranks were organized. 09:52

22 Q. Okay. So if the dies belong to the same 09:52

23 rank, what would happen if a read command is sent to 09:52

24 the stack array? Does that mean all eight of the 09:52

25 dies in the same rank is going to output data 09:52

1 simultaneously? 09:52

2 MR. CHANDLER: Objection. Form. 09:52

3 THE WITNESS: In the Figure 5 embodiment of 09:52

4 Riho, if you issue a read operation, all of the DRAM 09:52

5 die in a single rank will send data to the logic LSI 09:53

6 chip simultaneously. 09:53

7 BY MS. ZHONG: 09:53

8 Q. Is that how DRAMs are supposed to operate, 09:53

9 all the dies in the rank is supposed to respond to a 09:53

10 read signal and operate output data simultaneously? 09:53

11 MR. CHANDLER: Objection. Form. 09:53

12 THE WITNESS: It depends on the particular 09:53

13 design. 09:53

14 BY MS. ZHONG: 09:53

15 Q. So there are ranks -- there are embodiments 09:53

16 in which the dies in a rank do not respond to a read 09:53

17 operation -- a read command and output data 09:53

18 simultaneously? 09:53

19 MR. CHANDLER: Objection. Form. 09:53

20 THE WITNESS: Conceptually one could build 09:53

21 a DRAM system where either the entirety of a rank 09:53

22 could respond or a portion of a rank could respond 09:54

23 depending on the size of the read request. There 09:54

24 are lots of different ways that one could build a 09:54

25 memory system. 09:54

1 BY MS. ZHONG: 09:54

2 Q. Okay. I thought a rank is a collection of 09:54

3 DRAMs that respond to a common memory command 09:54

4 simultaneously. That's not your understanding of 09:54

5 what rank is? 09:54

6 MR. CHANDLER: Objection. Form. 09:54

7 THE WITNESS: That is my understanding. 09:54

8 But I think in common usage, one would still call 09:54

9 something a rank if it had that capability but also 09:54

10 had the capability to do a partial read. 09:54

11 BY MS. ZHONG: 09:54

12 Q. Where does that definition come from? 09:54

13 MR. CHANDLER: Objection. Form as to the 09:54

14 question there. 09:55

15 THE WITNESS: I just think that's common 09:55

16 usage, right? If a -- if a rank can provide data 09:55

17 simultaneously from each DRAM chip, I don't think it 09:55

18 has to in every instance for a person of ordinary 09:55

19 skill to refer to it as a rank. 09:55

20 BY MS. ZHONG: 09:55

21 Q. So you think "rank" can refer to a set of 09:55

22 family devices that read or write less than a full 09:56

23 bit width of the memory module in response to 09:56

24 command signals? 09:56

25 MR. CHANDLER: Objection. Form. 09:56

1 THE WITNESS: I don't think that's quite 09:56
2 what I said. 09:56
3 BY MS. ZHONG: 09:56
4 Q. Okay. Then can you further explain what you 09:56
5 meant? 09:57
6 A. I think I gave a pretty clear explanation, 09:57
7 but I will try one more time. 09:57
8 A rank of memory in the way that we 09:57
9 ordinarily use that term is capable of providing an 09:57
10 output on a read from every memory die or every 09:57
11 memory element in the rank simultaneously, but we 09:57
12 would still in normal usage still call it a rank if 09:57
13 it also had the capability of only providing a 09:57
14 portion of the memory word. 09:57
15 Q. So what you are saying is half a rank is 09:57
16 still referred to a rank? 09:57
17 MR. CHANDLER: Objection. Form. 09:58
18 THE WITNESS: No. I think I gave a clear 09:58
19 explanation of what I was saying. 09:58
20 BY MS. ZHONG: 09:58
21 Q. Okay. Let me see if I understand it. 09:58
22 So let's say that 8 memory dies in a rank to 09:58
23 output 64 bits, which is the bit width of the memory 09:58
24 module, and if now only one of the die is outputting 09:58
25 8 of the bits, you are still saying that the -- that 09:58

1 single die constitutes the rank; is that right? 09:59

2 A. No. I didn't -- there are no memory modules 09:59

3 really that I can recall in this IPR at all. But 09:59

4 even in that case, that was not what my testimony 09:59

5 was. 09:59

6 Q. Okay. So let's say 8 dies are outputting 09:59

7 64 bits from the memory system. Okay? And if for 09:59

8 one of the operation, only 8 bits are output. How 09:59

9 many -- how many dies are there in the rank? Still 09:59

10 8 or only 1? 09:59

11 A. 8. If the 8 dies normally operate together 09:59

12 and output 64 bits, the fact that there is an 10:00

13 additional operation in which only one operates does 10:00

14 not make the 8s stop being a rank. 10:00

15 Q. You said it normally outputs 64 bits, but 10:00

16 what if there are no what you call the normal -- 10:00

17 each operation is of variable length -- 10:00

18 MR. CHANDLER: Objection. 10:00

19 BY MS. ZHONG: 10:00

20 Q. -- then what would be -- what would 10:00

21 constitute a rank? 10:00

22 MR. CHANDLER: Objection. Form. 10:00

23 THE WITNESS: I can't recall ever seeing 10:00

24 such a situation, so I don't know what a person of 10:00

25 ordinary skill would call it. I would have to look 10:00

1 at the details. 10:00

2 BY MS. ZHONG: 10:00

3 Q. So let's say in the read operation, 10:00

4 sometimes it's 16 bits, sometimes it's 32 bits, 10:00

5 sometimes it's 64 bits. How many dies would you say 10:00

6 would make up a rank if each of the die is by 8? 10:00

7 MR. CHANDLER: Objection. Form. 10:01

8 THE WITNESS: Again, I would have to look at 10:01

9 the particulars, the particular situation. You 10:01

10 know, it would really depend on how that particular 10:01

11 system was configured. 10:01

12 But ordinarily we would refer to the 10:01

13 complete set of die that can operate concurrently, 10:01

14 that can output at the exact same time in a single 10:01

15 data word as a rank, whether or not it's possible to 10:01

16 use a portion of the rank. 10:01

17 BY MS. ZHONG: 10:01

18 Q. So if two dies belong to the same physical 10:02

19 rank, would you connect them with a single TSV and 10:02

20 have them output data simultaneously? 10:02

21 MR. CHANDLER: Objection. Form. Incomplete 10:02

22 hypothetical. 10:02

23 THE WITNESS: These are Riho's dies? 10:02

24 BY MS. ZHONG: 10:02

25 Q. It doesn't have to be. 10:02

1 A. I'd have to look at the specifics. I think 10:02
2 it would generally be difficult to have two die both 10:02
3 output simultaneously to the same TSV and have it 10:02
4 operate correctly. 10:02
5 Q. Because of potential data collision? 10:02
6 A. There could be a data collision. There 10:03
7 could be an electrical problem. I mean, that's just 10:03
8 not the way a wire in a memory circuit normally 10:03
9 operates. In a memory circuit, a wire with TSV is 10:03
10 just a specific kind of a wire. In normal 10:03
11 operation, it is usually driven by one driver at a 10:03
12 time. 10:03
13 Q. Okay. When you say "TSV is just a wire," 10:03
14 by "wire" you're not really -- it doesn't really 10:03
15 have the same meaning as the wire in wire bonding, 10:03
16 does it? 10:03
17 A. What I said was that TSV is a kind of a 10:03
18 wire. A wire bond is -- 10:03
19 Q. Okay.
20 A. -- a kind of a wire. 10:03
21 Q. Okay. When you say "wire," what do you 10:03
22 mean? Just electrical, a conducting trace or like 10:03
23 conductor? 10:03
24 A. A metallic conductor. 10:03
25 Q. So when you use the word "wire," you mean 10:03

1 metallic conductor? 10:04

2 MR. CHANDLER: Objection. Form. 10:04

3 THE WITNESS: That would be most commonly. 10:04

4 Again, there can be different contexts, but most 10:04

5 commonly that is what I would mean. 10:04

6 BY MS. ZHONG: 10:04

7 Q. What if the two dies don't belong to the 10:04

8 same physical rank but belong to a logical rank, 10:04

9 can you connect them to the same wire? 10:04

10 A. I'm so out of context here that I can't even 10:04

11 answer your question. I don't know what dies we are 10:04

12 talking about. I don't know what definition you are 10:04

13 using for physical rank and logical rank. I'd have 10:04

14 to look at an actual block diagram or circuit. 10:04

15 Q. Okay. So by logical rank -- and you are 10:05

16 familiar with the concept of rank multiplication; 10:05

17 right? 10:05

18 (Clarification requested by Reporter.) 10:05

19 BY MS. ZHONG:

20 Q. Rank multiplication. 10:05

21 A. Yes. Although there are many varieties. 10:05

22 Q. Okay. So in rank multiplication, you are 10:05

23 presenting -- on a high level, you are presenting 10:05

24 two physical ranks of memory dies as a single rank 10:05

25 to the memory controller; is that right? 10:05

1 A. Again, depending on your context, right. 10:05
2 These patents don't even have a memory controller. 10:05
3 But there are some situations -- yes, there 10:05
4 are some situations in rank multiplication where you 10:05
5 would represent to a memory controller that two 10:05
6 physical ranks are actually one logical rank. 10:06
7 Q. So does Riho involve the concept of rank 10:06
8 multiplication? 10:06
9 MR. CHANDLER: Objection. Form. 10:06
10 THE WITNESS: Riho is applicable with or 10:06
11 without rank multiplication. 10:06
12 BY MS. ZHONG: 10:06
13 Q. Okay. So in the context of Riho or the 10:06
14 reference Kim, what does "rank multiplication" mean 10:06
15 to you? 10:06
16 A. I just want to make sure I understand the 10:06
17 question. You asked me about Riho or Kim? 10:06
18 Q. Yes. 10:06
19 A. I think it just has the ordinary meaning. 10:06
20 Q. Which is? 10:06
21 A. That the system uses more physical memory 10:07
22 devices than the memory controller is aware of and 10:07
23 combines them in some way. 10:07
24 Q. Okay. So, basically, it's presenting 10:07
25 multiple physical ranks as a single logical rank to 10:07

1 the host? 10:07

2 MR. CHANDLER: Objection. 10:07

3 BY MS. ZHONG: 10:07

4 Q. Is that a fair description? 10:07

5 MR. CHANDLER: Objection. Form. 10:07

6 THE WITNESS: Again, in the abstract, it may 10:07

7 be broader than that. We'd have to look at how any 10:07

8 particular document uses the term. But in the 10:07

9 abstract, I think it can even be broader than that. 10:07

10 BY MS. ZHONG: 10:07

11 Q. Okay. And so in the context of, for 10:07

12 example, the memory system is presenting two 10:08

13 physical ranks as a single logical rank to the host, 10:08

14 can a single TSV be used to connect it to the two 10:08

15 physical ranks that belong to the same logical rank? 10:08

16 A. I think that depends on the specific 10:08

17 configuration, but neither Riho or Kim attempt to 10:08

18 do that. 10:08

19 Q. But would it be obvious for you to modify 10:08

20 to do that? 10:09

21 MR. CHANDLER: Objection. Form. 10:09

22 THE WITNESS: It would be obvious to use 10:09

23 rank multiplication with either reference, but I 10:09

24 don't know that you would necessarily have to use 10:09

25 that particular technique, but you could. 10:09

1 BY MS. ZHONG: 10:09

2 Q. How would you do rank multiplication in 10:09

3 Riho? 10:09

4 A. In the normal way. But, for example, you 10:09

5 could have the logic LSI chip represent that there 10:09

6 was a single rank that had a word length that was 10:09

7 twice as large as the physical ranks. 10:09

8 Q. What about in Kim then? 10:09

9 MR. CHANDLER: Object to form. 10:10

10 BY MS. ZHONG: 10:10

11 Q. And Kim is Exhibit 1014. 10:10

12 A. You can do the same. 10:10

13 Q. So in Kim, Kim's preferred embodiment shows 10:10

14 two ranks of memory dies; right? 10:10

15 A. Yes. 10:10

16 Q. Okay. So in Kim, if you want to have a 10:10

17 third rank, how would you modify Kim's Figure 3 or 10:11

18 Figure 5 to accommodate that third rank? 10:11

19 A. There would be a number of possible ways 10:11

20 to -- you are using three ranks or four ranks? 10:11

21 Q. Three. If four is easier, you can do four. 10:11

22 A. Yeah. Three ranks is just generally 10:11

23 difficult and complicated. 10:11

24 Q. Okay. Why? 10:11

25 A. Because you have to divide addresses by 10:11

1 three or you have to have word sizes that are not a 10:11
2 power of 2, so those are just generally hard -- 10:11
3 Q. Okay. 10:11
4 A. -- in any system. Not impossible, but hard. 10:11
5 But if you went from 2 to 4, you could do 10:11
6 it two different ways. And, in fact, Ellsberry 10:11
7 essentially illustrates some of those. But you 10:12
8 could -- you could either have four GIOs and four 10:12
9 chip selects and expand the read and write selecting 10:12
10 units to each select 1 of 4, then you would have 4 10:12
11 ranks. Or you could have 4 ranks sharing 2 ports 10:12
12 where you could operate only one of those ranks at a 10:12
13 time. 10:12
14 Q. When you say -- in the second option when 10:13
15 you say it shared 2 ports, are you saying like -- 10:13
16 let's just take a look at the GIO_Rank0, that path 10:13
17 there. 10:13
18 A. Yes. 10:13
19 Q. Are you saying you are going to split the 10:13
20 LIO_Rank0 after the box 100 into two different 10:13
21 branches? 10:13
22 MR. CHANDLER: Objection. Form. 10:13
23 THE WITNESS: No. You could have a Rank0 10:13
24 and a Rank2 both connected to GIO_Rank0 and simply 10:13
25 have the appropriate control signals to have one at 10:13

1 a time drive those wires. 10:13

2 BY MS. ZHONG: 10:13

3 Q. So like the Rank0 is also going to be added 10:13

4 to the GIO_Rank0 line, basically just a duplicate -- 10:13

5 A. One option would be to add -- to connect 10:14

6 Rank2 to the GIO_Rank0 line and to connect Rank3 to 10:14

7 the GIO_Rank1 line, and create the appropriate 10:14

8 control signals so that only one rank would drive 10:14

9 each of those I/O lines at a time or only one rank 10:14

10 would respond to write operations on them. There 10:14

11 are lots of different ways to make rank 10:14

12 multiplication work. 10:14

13 MS. ZHONG: Okay. Why don't we take a break 10:14

14 right now. 10 minutes. 10:14

15 MR. CHANDLER: Okay. 10:14

16 DEPOSITION REPORTER: We are off the record. 10:14

17 (Off the record.) 10:14

18 BY MS. ZHONG: 10:32

19 Q. So, Dr. Wolfe, can we go back to Figure 5 on 10:32

20 Riho, which is Exhibit 1016. Okay. 10:32

21 A. I have it. 10:32

22 Q. Okay. So I think we discussed earlier, I 10:32

23 think you said when the transmission gates in the 10:32

24 switch circuits sa and sb are off, it isolates the 10:32

25 load from the driver circuits on the right from the 10:32

1 TSV; correct? 10:32

2 A. Correct. 10:32

3 Q. Okay. 10:32

4 A. When they are both off. If either one is 10:32

5 on, then it is not isolated. 10:32

6 Q. Okay. But do the transmission gates 10:32

7 themselves have capacitive loads on them? 10:32

8 A. Everything in the universe has a capacitive 10:32

9 load on it. But the transmission gates have a very 10:33

10 tiny capacitive load compared to the drivers, enough 10:33

11 that we would typically ignore it. 10:33

12 Q. But isn't it the case that in order to 10:33

13 accommodate a current from the driver circuit, the 10:33

14 transistor had to be built large enough in order to 10:33

15 accommodate that current? 10:33

16 MR. CHANDLER: Objection. Form. 10:33

17 THE WITNESS: It has to be large enough, but 10:33

18 that doesn't mean it's very large. That could be 10:33

19 quite minimal. 10:33

20 Also, the bulk -- the way that a 10:33

21 transmission gate is configured and biased, it has 10:33

22 a very minimal capacitive load. It is designed that 10:33

23 way. We use them, for example, in capacitive touch 10:33

24 sensors because they have a very tiny capacitive 10:34

25 load and don't impact the capacitances that you are 10:34

1	trying to measure.	10:34
2	BY MS. ZHONG:	
3	Q. But we can agree that whether it's turned	10:34
4	off or it's turned on, the -- there is going to be	10:34
5	some capacitive load that's imposed on a --	10:34
6	experienced by the TSVs; right?	10:34
7	MR. CHANDLER: Objection. Form.	10:34
8	THE WITNESS: As I said, every --	10:34
9	BY MS. ZHONG:	
10	Q. Let me put it this -- let me put it this	10:34
11	way.	10:34
12	When the MOS driver in the logic side, when	10:34
13	it's trying to drive the signal up to D15, it has to	10:34
14	overcome the capacitive load attributable to the	10:34
15	switch circuits sa and sb from D0 to D14 if both --	10:34
16	even if both of them are turned off; is that -- is	10:34
17	that right?	10:34
18	MR. CHANDLER: Objection. Form.	10:35
19	THE WITNESS: It's technically correct	10:35
20	because everything in the universe has a capacitive	10:35
21	load on everything else, but as I mentioned, the	10:35
22	capacitive load is typically considered to be	10:35
23	trivial.	10:35
24	BY MS. ZHONG:	10:35
25	Q. Okay. So we agree that there are capacitive	10:35

1 loads from the transmission gates even if they are 10:35
2 turned off, it's just that you believe that the 10:35
3 contribution or the value of those capacitive loads 10:35
4 are insignificant. Is that a fair description? 10:35
5 MR. CHANDLER: Objection. Form. 10:35
6 THE WITNESS: As I mentioned, everything in 10:35
7 the universe provides a capacitive load on 10:35
8 everything else. 10:35
9 When we do the analysis and the teaching 10:35
10 from Riho is that the capacitive load of the 10:35
11 turned-off transmission gates is negligible. It can 10:35
12 be ignored. And that if -- their purpose is to 10:35
13 isolate the capacitive load from the driver 10:36
14 circuits, which is much more substantial. 10:36
15 BY MS. ZHONG: 10:36
16 Q. Okay. But the transmission gate will have 10:36
17 to accommodate a current from the driver circuit; 10:36
18 right? 10:36
19 MR. CHANDLER: Objection. Form. 10:36
20 THE WITNESS: Current from the driver 10:36
21 circuit does pass through the transmission gate, but 10:36
22 it is limited by the characteristics of the TSV so 10:36
23 it needs to be the appropriate size, but not 10:36
24 anything that would be abnormally large. 10:36
25 / / / 10:36

1 BY MS. ZHONG: 10:36

2 Q. Okay. They would be -- is it fair to say 10:36

3 that the transmission gates in D0 through D14 would 10:36

4 be sized similarly to those in D7 and D15? 10:37

5 MR. CHANDLER: Objection. Form. 10:37

6 THE WITNESS: That would be the case in 10:37

7 Riho's preferred embodiment. 10:37

8 BY MS. ZHONG: 10:37

9 Q. Okay. And each of the circuits would decide 10:37

10 appropriately in order to accommodate the expected 10:37

11 maximum load coming from the driver circuit; is that 10:37

12 right? 10:37

13 MR. CHANDLER: Objection. Form. 10:37

14 THE WITNESS: Not necessarily. They would 10:37

15 be sized appropriately to support the designer 10:37

16 current. 10:37

17 BY MS. ZHONG: 10:37

18 Q. Okay. So each of the circuits -- let me 10:37

19 withdraw it. 10:37

20 Each of the switch circuits in SDRAM D0 10:37

21 through D15 would be designed or sized appropriately 10:38

22 in order to accommodate the desired current from the 10:38

23 driver circuit; is that right? 10:38

24 MR. CHANDLER: Objection. Form. 10:38

25 THE WITNESS: From the driver circuit on 10:38

1 that particular chip, right. Remember, in many 10:38
2 cases they're being driven by the driver circuit on 10:38
3 the logic LSI chip as well. That's the one that we 10:38
4 are really concerned about. 10:38
5 BY MS. ZHONG: 10:38
6 Q. Okay. So each of the switch circuit in D0 10:38
7 through D15 would be sized appropriately to 10:38
8 accommodate the expected or desired drive current 10:38
9 from the L1C2R2 driver circuits on that -- 10:38
10 (Clarification requested by Reporter.) 10:39
11 BY MS. ZHONG: 10:39
12 Q. So each of the switch circuits in SDRAM D0 10:39
13 through D15 would be sized appropriately to 10:39
14 accommodate the expected current from the associated 10:39
15 driver circuit on that die; is that correct? 10:39
16 MR. CHANDLER: Objection. Form. 10:39
17 THE WITNESS: It depends what you mean by 10:39
18 "expected current." One would determine what the 10:39
19 desired current is from the driver on the die to the 10:39
20 TSV and would size -- 10:39
21 BY MS. ZHONG:
22 Q. Okay.
23 A. -- sa and sb appropriately to match the
24 desired current. 10:40
25 (Clarification requested by Reporter.) 10:40

1 THE WITNESS: -- size sa and sb 10:40
2 appropriately to match the desired current. 10:40
3 BY MS. ZHONG: 10:40
4 Q. And is it fair to assume that in the 10:40
5 preferred embodiment of Riho, each of those 10:40
6 circuits, switch circuits, are sized similarly or 10:40
7 substantially the same? 10:40
8 A. Yes. In the preferred embodiment, that 10:40
9 would be the case. 10:40
10 Q. How would you estimate the capacitive load 10:40
11 of the transmission gate associated with one of the 10:40
12 L1C2R2 circuit? 10:40
13 MR. CHANDLER: Objection to form. 10:41
14 THE WITNESS: In the context of Riho, I 10:41
15 mean, I guess you could do an analysis using a 10:41
16 simulation tool based on your IC process, but, 10:41
17 essentially, the teaching of Riho is that it is 10:41
18 insubstantial and you don't need to take it into 10:41
19 account. 10:41
20 BY MS. ZHONG: 10:41
21 Q. Okay. When you say the "simulation tool," 10:41
22 what kind of tool are you talking about? What are 10:41
23 the input parameters? 10:41
24 A. It depends on your specific implementation 10:41
25 technology. There are tools available from people 10:41

1 like Synopsys and Cadence that do 3D semiconductor 10:41
2 simulation to determine what the parasitic 10:42
3 capacitances are of individual devices using 10:42
4 techniques like find an element analysis, and that's 10:42
5 what would be done in the industry by those tools, 10:42
6 and you put in the parameters that you get back from 10:42
7 your manufacturing process. 10:42
8 But, again, those details aren't really 10:42
9 relevant to Riho's teachings. Riho's teaching is 10:42
10 that by disconnecting the L1C2R2 circuit, that you 10:42
11 reduce the capacitance and that's the important 10:42
12 teaching. 10:42
13 Q. Okay. Did you yourself do any simulation to 10:42
14 see whether Riho's assumption was correct on that? 10:42
15 A. It would depend on the exact parameters of 10:42
16 the memory system. But from my experience, I can 10:43
17 tell you that it's generally correct. 10:43
18 Q. Okay. 10:43
19 A. I mean, obviously, one could do a terrible 10:43
20 design, but if -- in normal designs, this kind of 10:43
21 technique is used all the time to reduce capacitive 10:43
22 load by using a transmission gate. 10:43
23 Q. Is that the same -- is that the kind of 10:43
24 design that's used being stacked with DDR4 or DDR5 10:43
25 dies? 10:43

1 MR. CHANDLER: Objection. Outside the scope 10:43
2 of direct. 10:43
3 THE WITNESS: I don't know. I haven't seen 10:43
4 a circuit level design for DDR4 or DDR5 die. 10:43
5 BY MS. ZHONG: 10:44
6 Q. Okay. So when you say it is a normal 10:44
7 design, in what context have you seen this kind of 10:44
8 design [indiscernible] or it's more horizontal 10:44
9 designs? 10:44
10 (Clarification requested by Reporter.) 10:44
11 BY MS. ZHONG: 10:44
12 Q. So when you say, like in your experience, 10:44
13 it's pretty normal for you to have a transmission 10:44
14 gate to reduce a capacitive load, is that -- let me 10:44
15 ask you, do you have experience designing stacked 10:44
16 dies with TSVs connected -- using TSVs to 10:44
17 interconnect those stacks? 10:45
18 A. No, I do not. But the electrical 10:45
19 considerations in this case would be the same. 10:45
20 Q. Okay. And when you say it's normal design, 10:45
21 in what context have you used that design? 10:45
22 A. I've seen this design used for all 10:45
23 kinds of computer buses, using memories, using 10:45
24 microprocessors, and various kinds of low power 10:45
25 systems over decades. It's just a normal way to 10:45

1 isolate the capacitance of a circuit. 10:45
2 Personally, I've used it in capacitance 10:45
3 measurement circuits, but I have seen it used in 10:46
4 many other ways. 10:46
5 Q. Can you please go to the Exhibit Share and 10:46
6 download Exhibit 2100. 10:46
7 A. It's not there unless you've introduced -- 10:46
8 let me refresh. 10:46
9 Q. Yeah, if you --
10 A. Oh, it's there now. Okay. 10:46
11 MS. ZHONG: Okay. 10:46
12 MR. CHANDLER: Just one moment, please. I'm 10:46
13 still trying to get it myself. I'm making progress, 10:46
14 but just one second, if you will. 10:46
15 Okay. I think -- I've got Exhibit 2100 that 10:46
16 has Figure 3 on it. 10:47
17 BY MS. ZHONG: 10:47
18 Q. Okay. So Exhibit 2100 is a modification of 10:47
19 Kim Figure 3. 10:47
20 Dr. Wolfe, do you recall our discussion in 10:47
21 the last session on how you would modify Figure 3 to 10:47
22 accommodate four ranks in Kim; do you recall that 10:47
23 discussion? 10:47
24 A. I do. I recall saying there were a number 10:47
25 of different ways one could -- in which one could do 10:47

1 it following what was known in the art at the time. 10:47

2 Q. Okay. And I'm showing this to try to 10:47

3 understand -- like you said one of the ways is to 10:48

4 have Rank2 connected to the GIO_Rank0 line and Rank1 10:48

5 connected to the GIO_Rank1 line. 10:48

6 Do you recall that discussion? 10:48

7 A. I do. There are a number of things here. 10:48

8 One is, it appears here that you have two Rank1s, 10:48

9 which I'm not sure why you would do -- 10:48

10 Q. Okay. Sorry. 10:48

11 A. But also my testimony was and is that you 10:48

12 would also have to make a number of additional 10:48

13 routine modifications that are not illustrated here. 10:48

14 Q. Okay. I just want to understand when you 10:48

15 say to connect from GIO_Rank2 to GIO_Rank0, is 10:48

16 that -- what do you have in mind? 10:48

17 MR. CHANDLER: Objection. Form. 10:48

18 THE WITNESS: No. This is incomplete. 10:48

19 BY MS. ZHONG: 10:48

20 Q. Okay. How would you modify it? How would 10:48

21 you further modify it? 10:49

22 A. As I said, I'm not -- I'm not going to do a 10:49

23 complete memory system design sitting here. It's 10:49

24 complicated, although it's routine. 10:49

25 But for one, you would connect the read 10:49

1 sense amplifier to the bus as well. You would have 10:49
2 four chip selects instead of two, and you would need 10:49
3 to go through and analyze all of the timing and all 10:49
4 of the driver control to make it all work. 10:49
5 Again, there are many examples out there 10:49
6 where a person of ordinary skill in the art could 10:49
7 have solved it themselves using their general 10:49
8 knowledge as of 2010, but there's a large number of 10:49
9 routine steps. 10:49
10 Q. Okay. So one of the things you mentioned is 10:49
11 you would need to evaluate the timing. What do you 10:49
12 mean by that? 10:49
13 A. Every memory system design, you need to 10:49
14 evaluate the timing. You need to make sure that the 10:50
15 right signals show up on the right wires, the right 10:50
16 time, and when you make a change in a memory system, 10:50
17 you may need to go back and confirm or modify that 10:50
18 timing. 10:50
19 Q. Let's assume that Rank2 is connect -- has 10:50
20 audio probe signals and the wires and are connected 10:50
21 to the GIO_Rank0; right? What would be the timing 10:50
22 issue? 10:50
23 A. It's a -- it's a multistep analysis that 10:50
24 involves a lot of details. You have to look at all 10:50
25 of the timing diagrams for those particular 10:50

1 memories. Again, it's routine, but nontrivial. 10:50
2 And you would have to analyze the input 10:50
3 control signals, the input data, the output data to 10:51
4 make sure that the right data shows up at the right 10:51
5 time so there are no collisions, and so that data 10:51
6 arrives at the time that the controller chip is 10:51
7 expecting it. It's something that's been done tens 10:51
8 of thousands of times. It's very routine, but it's 10:51
9 more complex than one can do sitting in front of a 10:51
10 camera. 10:51
11 Q. Okay. When you say two routines being done 10:51
12 tens of thousands of times, is it by you or it's by 10:51
13 someone just out of the college? 10:51
14 A. Not necessarily someone right out of 10:51
15 college, but someone with a limited amount of 10:51
16 experience in designing memory systems and a basic 10:51
17 college education would be able to do that. 10:51
18 Again, it's a routine engineering task. It 10:51
19 is an entry-level engineering task. It is not 10:51
20 something that one requires advanced education to 10:52
21 do, but there are many details to chase down, each 10:52
22 one of which is routine, but you would have to do 10:52
23 them all. 10:52
24 Q. And who provides all those design parameters 10:52
25 to the entry-level engineers? You need to have a 10:52

1 senior person to direct the low-level engineer or 10:52
2 junior engineer to do those simulation or study; is 10:52
3 that right? 10:52
4 A. No, I wouldn't think so. You would need to 10:52
5 provide them with documentation of the components 10:52
6 that they are given so the various memory 10:52
7 components, the various controller components, or 10:52
8 you would give them the freedom to redesign them. 10:52
9 Obviously, designing a complete memory 10:52
10 system, if you didn't start with anything would take 10:52
11 a substantial amount of time for a single person to 10:53
12 do, but that's not usually the situation. Usually 10:53
13 the situation is one can choose from many different 10:53
14 pre-existing components and any undergraduate 10:53
15 electrical engineer would know how to read timing 10:53
16 diagrams and to determine compatibility and to 10:53
17 adjust and compensate for incompatibilities, 10:53
18 especially by 2010. 10:53
19 Q. Now, Kim designed the Figure 3 configuration 10:53
20 to overcome a perceived problem in what Kim 10:53
21 describes as a typical semiconductor configuration 10:54
22 in Figure 1; is that right? 10:54
23 MR. CHANDLER: Objection. Form. 10:54
24 BY MS. ZHONG: 10:54
25 Q. Why don't we take one step back. 10:54

1	A. I believe --	10:54
2	Q. Go ahead.	10:54
3	A. I believe that the problem that was	10:54
4	perceived...	10:54
5	Q. Paragraph 42 and 43?	10:55
6	A. Yes. So there was a problem in certain	10:55
7	kinds of memories in which there could be a data	10:55
8	collision in a two-rank system.	10:55
9	Q. And that is specific to the Figure 1	10:55
10	configuration?	10:56
11	A. The Figure 1 configuration, if certain	10:56
12	particular memory chips, memory components are used.	10:56
13	Q. What kind of a memory chip components are	10:56
14	used that would cause this problem?	10:56
15	MR. CHANDLER: I apologize, was the answer	10:57
16	"gate collection" or "gate collision"?	10:57
17	MS. ZHONG: Gate collision.	10:57
18	THE WITNESS: Data collision.	10:57
19	MR. CHANDLER: Data collision. All right.	10:57
20	I got it.	10:57
21	THE WITNESS: The prior art operation	10:58
22	occurred -- problem occurred when a read immediately	10:59
23	followed a write operation. Not all memories allow	10:59
24	that to happen. So sometimes one can simply specify	10:59
25	that there's a time delay between a write operation	10:59

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1 and a read operation to separate banks. So there 10:59
2 are -- 10:59
3 BY MS. ZHONG:
4 Q. [Indiscernible - simultaneous talking]
5 Sorry. 10:59
6 A. -- but again, the very -- the specific 10:59
7 problem is separate from the Figure 5 teachings of 10:59
8 how TSVs would be connected. 10:59
9 Q. Okay. So how does -- let me put it this 10:59
10 way. 10:59
11 Do JEDECs provide for -- allow for a 10:59
12 read-to-write operation within the same rank? 11:00
13 MR. CHANDLER: Object to form. 11:00
14 THE WITNESS: Well, first let's put this in 11:00
15 perspective. Kim doesn't require that the actual 11:00
16 ranks be JEDEC-compliant memory. In fact, Kim 11:00
17 doesn't specify that there is any memory type at
18 all, doesn't even specify that it's DRAM. It's for 11:00
19 any semiconductor memory. 11:00
20 But given that, we'd have to dig into each 11:00
21 individual JEDEC spec to look at the details of read 11:00
22 versus write timing. 11:00
23 But, again, even if it's permitted by the 11:00
24 memory, it doesn't have to be permitted by the 11:00
25 memory system. 11:00

1 BY MS. ZHONG: 11:00

2 Q. As far as you know, does NAND allow for read 11:00

3 after write immediately? 11:00

4 (Clarification requested by Reporter.) 11:00

5 MR. CHANDLER: Yeah, I didn't hear that word

6 either.

7 BY MS. ZHONG:

8 Q. NAND, N-A-N-D, do NAND/memories allow for 11:01

9 read after write? 11:01

10 MR. CHANDLER: Objection. Form. 11:01

11 THE WITNESS: There are lots of protocols 11:01

12 for NAND memories. Again, they don't all operate 11:01

13 exactly the same way. NANDs all allow for read 11:01

14 after write. There just may be a specified time 11:01

15 delay between them. 11:01

16 BY MS. ZHONG: 11:01

17 Q. Okay. Are you aware of any NAND systems 11:01

18 that perform as described in paragraph 42 and 43 of 11:01

19 Kim at the time of the invention? 11:01

20 A. I don't know one way or the other. 11:01

21 Q. Okay. What about SRAM systems? 11:02

22 A. I am familiar with pipelined SRAM systems 11:02

23 that have this problem, synchronous SRAMs. 11:02

24 Q. Okay. So the synchronous SRAM -- by "SRAM," 11:02

25 I mean static RAM; is that what you have in mind? 11:02

1	A. Yes.	11:02
2	Q. Okay. So SRAMs allow for read immediately	11:02
3	after write.	11:02
4	MR. CHANDLER: Objection. Form.	11:02
5	THE WITNESS: No. I said that I am familiar	11:02
6	with synchronous SRAM systems that do not permit a	11:02
7	read immediately after a write. There would be a	11:02
8	collision.	11:02
9	BY MS. ZHONG:	11:02
10	Q. Okay. Are you aware of any SRAMs that allow	11:02
11	for immediate read after write as described in	11:02
12	paragraph 42?	11:03
13	A. I am not sure if that is a correct	11:03
14	characterization of paragraph 42. Paragraph 42 says	11:03
15	that you could send those commands, but that it	11:03
16	wouldn't work in that particular configuration.	11:03
17	So there are a lot of chips that would allow	11:03
18	you to send commands that wouldn't work, but I	11:03
19	wouldn't describe that as saying that they allow	11:03
20	that memory operation.	11:03
21	Q. So are you aware of SRAM systems that allow	11:03
22	a read operation after a write operation as	11:03
23	described in 42?	11:03
24	MR. CHANDLER: Objection. Form.	11:03
25	THE WITNESS: That's the same question. I	11:03

1 just don't think that there's a clear way to answer 11:03
2 it. I am aware of SRAM systems that can operate 11:04
3 correctly if a read immediately follows a write, and 11:04
4 I'm aware of SRAM systems that will operate 11:04
5 incorrectly if a read immediately follows a write. 11:04
6 BY MS. ZHONG: 11:04
7 Q. Okay. Which SRAM system would allow for a 11:04
8 correct operation with a read after write? 11:04
9 A. There are specific chips that do that. I 11:04
10 can't recite a part number off the top of my head. 11:04
11 Q. And do those SRAMs belong to different 11:04
12 ranks? 11:04
13 A. It depends how you assemble them into a 11:04
14 system. 11:04
15 Q. I'm asking you for that system that you are 11:04
16 aware of that allows a read right after write. Are 11:04
17 those organized -- do those involve SRAMs in two 11:05
18 different ranks? 11:05
19 A. I'm aware of the components. A person of 11:05
20 ordinary skill could assemble them in lots of 11:05
21 different ways with multiple ranks or single ranks. 11:05
22 Again, these are all very ordinary things by 11:05
23 2010, but I can't point you to a particular design 11:05
24 that's configured that way. 11:05
25 Q. So I am asking you: Are you aware of a read 11:05

1 where an SRAM in Rank1 following immediately a write 11:05
2 operation of an SRAM in Rank0? 11:05
3 A. That would be something a person of ordinary 11:05
4 skill could build, but I'm not familiar with a 11:05
5 particular implementation of that off the top of my 11:05
6 head, no. 11:06
7 Q. Okay. Are you aware of an implementation in 11:06
8 2010 and before in which a NAND memory -- 11:06
9 DEPOSITION REPORTER: Excuse me.
10 Miss Zhong, can you try to move your camera down a
11 little bit. I'm losing your mouth again.
12 MS. ZHONG: I think that's as down as
13 possible.
14 DEPOSITION REPORTER: Can you get closer
15 up to the screen maybe? Maybe that will help.
16 MS. ZHONG: I don't think so. I'm already
17 against the edge of the table.
18 DEPOSITION REPORTER: Okay. Just try to
19 sit up a little more if you can would be helpful.
20 Thank you. Sorry about that. 11:06
21 BY MS. ZHONG: 11:06
22 Q. Are you aware of an implementation in 2010 11:06
23 in which a NAND in the second rank performs a read 11:06
24 operation after a write operation of the first rank? 11:06
25 MR. CHANDLER: Objection. Form. 11:07

1 THE WITNESS: Again, I can't point you to a 11:07
2 specific design at the moment, but any multiple-rank 11:07
3 NAND system would have that characteristic. 11:07
4 BY MS. ZHONG: 11:07
5 Q. And do you have any references that 11:07
6 describes organizing NAND dies in ranks? 11:07
7 A. Yes, both Riho and Rajan. Also -- 11:07
8 Q. Where does Riho say -- mention organizing 11:07
9 DRAMs -- NANDs in ranks? 11:07
10 A. Well, Riho is all about having ranks, 11:07
11 including the preferred embodiment with two ranks. 11:08
12 And then in paragraph 136, he explains that you can 11:08
13 either have a mix of DRAM and NAND, or you can have 11:08
14 a NAND controlled by the same chip. 11:08
15 And I believe -- let me see if I can find 11:08
16 it. It says that it's applicable to the whole 11:08
17 range of semiconductor products. Let me look. I 11:08
18 thought -- that's Riho. Yeah. 11:08
19 And then Rajan in column 15, starting around 11:09
20 line 3 says it can be implemented with NAND flash. 11:09
21 Q. Okay. Does it describe using the word 11:09
22 "rank" expressly whereas the word NAND -- 11:09
23 DEPOSITION REPORTER: I'm sorry,
24 Miss Zhong. I can't see your mouth at all. It's
25 hard for me to make out exactly what you're saying.

1 Can we go off the record for a moment.

2 MR. CHANDLER: Okay. 11:09

3 MS. ZHONG: Yes. 11:09

4 (Off the record.) 11:10

5 BY MS. ZHONG: 11:10

6 Q. Now, in Riho, the preferred embodiment when 11:10

7 they discuss rank, that's in reference to an SDRAM 11:10

8 system; correct? 11:10

9 MR. CHANDLER: Objection. Form. 11:10

10 THE WITNESS: The illustrated preferred 11:10

11 embodiment is, but again, it also goes on to 11:10

12 describe that the NAND can be substituted in the 11:10

13 same invention. So a person of ordinary skill would 11:10

14 understand that the SDRAM is exemplary and that the 11:11

15 same design could be done with other kinds of 11:11

16 memory. 11:11

17 BY MS. ZHONG: 11:11

18 Q. I understood that. 11:11

19 But does it describe use of the word "rank" 11:11

20 in connection with NAND expressly? 11:11

21 A. Yes. To a person of ordinary skill, it does 11:11

22 because it talks about using NAND in the invention, 11:11

23 the invention that's described in terms of ranks. 11:11

24 Q. So I have tried to do a search in JEDEC 11:11

25 specs and in general IEEE paper, and I have not seen 11:11

1 anyone have used the word "rank" together with 11:11
2 "NAND." 11:12
3 Are you aware of any such papers or JEDEC 11:12
4 specification? 11:12
5 A. Most of the JEDEC specifications are not 11:12
6 about NAND, so that wouldn't necessarily be the 11:12
7 right place to look. I haven't done a search so I 11:12
8 don't know one way or the other. 11:12
9 Q. Who puts out the NAND specifications? 11:12
10 A. Again, there are a number of them. One of 11:12
11 them is called ONFI, but -- 11:12
12 Q. OFI? 11:12
13 A. ONFI, I believe. 11:12
14 Q. ONFI. Okay. Okay. 11:12
15 A. I don't recall other names off the top of my 11:12
16 head, but it wouldn't impact my opinion at all that 11:12
17 these references disclose the use of memories beyond 11:12
18 SDRAMs. My recollection, again, with Riho is there 11:13
19 was another place that it was discussed. Let me see 11:13
20 if I can find it. 11:13
21 It's in paragraph 135. And it specifically 11:13
22 says the controlled chips, the slave chips are not 11:13
23 limited to the SDRAM and may be, for example, SRAMs 11:13
24 or nonvolatile memories. Further, the circuit types 11:13
25 are not limited to those disclosed in the 11:13

1	embodiments.	11:13
2	Q. I think we're talking about two things. I'm	11:13
3	trying to figure out what kind of memory system is	11:13
4	at issue in Kim.	11:13
5	A. Oh, in Kim?	11:14
6	Q. I think -- yeah. And I think we started	11:14
7	discussing in which memory systems the problems in	11:14
8	paragraph 42 -- described in Kim 42 would appear.	11:14
9	So I was asking you, are you aware of any	11:14
10	NAND memory systems in which the NAND memories	11:14
11	are all 9 and ranked and one NAND -- and the	11:14
12	memory -- the NAND memory in Rank1 would perform a	11:14
13	read operation after a write operation on Rank1 is	11:14
14	performed?	11:15
15	MR. CHANDLER: Objection. Form.	11:15
16	THE WITNESS: Both Riho and Rajan disclosed	11:15
17	NAND memories or nonvolatile memories, which one	11:15
18	would equate at that time with NAND flash memory.	11:15
19	BY MS. ZHONG:	11:15
20	Q. Okay.	11:15
21	A. And they are organized in ranks and they	11:15
22	would be able to perform a read following a write or	11:15
23	a write following a read.	11:15
24	Q. Okay. And in those systems, is data	11:15
25	collision avoidable as described in 42?	11:15

1 A. Data collision is always avoidable. The 11:15
2 question is what constraints the system designer 11:15
3 wants to place on time. If one carefully reads 42, 11:15
4 paragraph 42 and 43 of Kim, they're not saying that 11:15
5 that problem is unavoidable, but merely that they 11:16
6 think that they have an improvement. 11:16
7 Q. Okay. So I don't understand. Why would 11:16
8 there be a data collision problem when you do a read 11:16
9 operation after a write operation across the rank? 11:16
10 MR. CHANDLER: Objection. Incomplete. 11:16
11 THE WITNESS: Because in this one very 11:16
12 narrow circumstance that is being discussed, these 11:16
13 are burst operations and burst operations require 11:17
14 multiple data transfers. And in this one particular 11:17
15 example, the command to data delays have not been 11:17
16 properly selected for optimal performance on a 11:17
17 two-rank system. But there are many, many known 11:17
18 solutions to that problem. 11:17
19 BY MS. ZHONG: 11:17
20 Q. Okay. Do SRAMs output data in bursts? 11:17
21 A. Some do. 11:17
22 Q. What about NAND? 11:17
23 A. Most do. 11:17
24 Q. Okay. And when you say they output a data 11:17
25 in burst, what do you mean exactly? 11:17

1 A. That means that for any individual read or 11:17
2 write command, there are multiple cycles 11:18
3 consecutively in which data is transmitted, usually 11:18
4 of a fixed size. 11:18

5 Q. Does it have anything to do with -- say, for 11:18
6 example, you have an SRAM that is by 4. 11:18

7 Does that mean it outputs bursts of by 4 or 11:18
8 that has nothing to do with the bits that's been 11:18
9 output by the -- 11:18

10 (Clarification requested by Reporter.) 11:18

11 BY MS. ZHONG: 11:18

12 Q. -- by the memory? 11:18

13 A. Normally when we say that an SRAM is 11:18
14 by 4, we are talking about the width of each data 11:18
15 transfer. 11:18

16 Q. Okay. 11:18

17 A. Burst lengths are typically in JEDEC 11:18
18 compliant DRAMs. They are specified by the 11:19
19 particular generation. In SRAMs and NAND, they're 11:19
20 usually specific to each individual chip design. 11:19

21 Q. So for the SRAMs with the bursting data 11:19
22 output, were those available in 2010 -- 2009, 2010 11:19
23 time period? 11:19

24 A. They were known. Whether they were -- they 11:19
25 predate that by quite a bit. Whether they were 11:19

1 still available, I would expect the answer is yes. 11:20
2 I don't know of any reason why they wouldn't have 11:20
3 still been available, but I don't know that as a 11:20
4 fact. But they were certainly known and their 11:20
5 functionality had been published. 11:20
6 Q. And do you use chip select signals with 11:20
7 SRAMs? 11:20
8 A. Normally, yes. 11:20
9 Q. What about with NAND memory devices? 11:20
10 A. Often, yes. 11:20
11 Q. And when you use a chip select signal with 11:20
12 NAND, does it select a single chip or all the chips 11:20
13 in that rank? 11:20
14 MR. CHANDLER: Objection. Form. 11:20
15 THE WITNESS: It depends how you have 11:20
16 designed your memory system. It would be a design 11:20
17 choice. 11:20
18 BY MS. ZHONG: 11:20
19 Q. And how is it supposed to operate in Kim's 11:21
20 Figures 1 and 3? 11:21
21 MR. CHANDLER: Objection. Form. 11:21
22 THE WITNESS: Chip selects aren't 11:21
23 illustrated in Figure 1. In Figure 3, chip 11:21
24 select 0 operates the entirety of Rank0 or 11:21
25 enables the entirety of Rank0, and chip select 1 11:21

1 enables the entirely -- entirety of Rank1 in that 11:21
2 particular embodiment. 11:21
3 BY MS. ZHONG: 11:21
4 Q. What about the SRAM, do the chip selects 11:21
5 select an entire rank or just a single chip? 11:21
6 MR. CHANDLER: Objection. Form. 11:22
7 THE WITNESS: Again, it's a design choice. 11:22
8 A person of ordinary skill would know how to 11:22
9 implement either. 11:22
10 BY MS. ZHONG: 11:22
11 Q. Is that specified by JEDEC? 11:22
12 MR. CHANDLER: Objection. Form. 11:22
13 THE WITNESS: JEDEC does not specify the 11:22
14 design of SRAM memory systems. They specify 11:22
15 interfaces for various things. 11:22
16 Again, JEDEC has lots of specifications, but 11:22
17 there would not be one that I don't think would tell 11:22
18 you exactly how to connect up the chip selects on an 11:22
19 SRAM memory system. That would be a trivial 11:22
20 engineering task. 11:22
21 BY MS. ZHONG: 11:22
22 Q. Does JEDEC specify the chip select signals 11:22
23 in DRAM system or SDRAM systems? 11:22
24 MR. CHANDLER: Objection. Form. 11:23
25 THE WITNESS: In certain systems it does, 11:23

1 but it doesn't restrict what you can do in other 11:23
2 systems. 11:23
3 BY MS. ZHONG: 11:23
4 Q. Does JEDEC require that in a SDRAM system, 11:23
5 the chip select to be sent to all the dies in the 11:23
6 rank? 11:23
7 MR. CHANDLER: Objection. Form. 11:23
8 THE WITNESS: We'd have to look at 11:23
9 particular specifications. Some JEDEC standards 11:23
10 don't have anything to do with ranks and other JEDEC 11:23
11 standards do. 11:23
12 BY MS. ZHONG:
13 Q. What kind of specification would have 11:23
14 something to do with ranks? Does it have to be a 11:23
15 memory module level specification? 11:23
16 MR. CHANDLER: Objection. Form. 11:23
17 THE WITNESS: I don't remember the details 11:23
18 of every JEDEC specification, but I would think that 11:23
19 memory module specifications would be the most 11:23
20 likely to describe the supported features of ranks. 11:23
21 BY MS. ZHONG: 11:24
22 Q. Are SDRAM memory modules required to receive 11:24
23 chip select signals? 11:24
24 MR. CHANDLER: Objection. Form. 11:24
25 THE WITNESS: Required by who? No. You can 11:24

1 build an SDRAM memory module however you'd like. 11:24
2 There are no regulations or laws. 11:25
3 BY MS. ZHONG: 11:25
4 Q. So if you have -- you are building a memory 11:25
5 module using DDR4, DDR3, SDRAMs, does the host have 11:25
6 to provide a chip select signal, or can the chip 11:25
7 select signal be generated internally on the module? 11:25
8 MR. CHANDLER: Objection. Outside the scope 11:25
9 of direct and form. 11:25
10 THE WITNESS: I'd have to refer to those 11:25
11 specifications. Again, I'm sure there are lots of 11:25
12 things that are theoretically possible, but in a 11:25
13 typical JEDEC compliant DDR3 or DDR4 memory module, 11:25
14 there are chip selects that come from the host, but 11:25
15 that does not prevent you from generating local chip 11:25
16 selects on the module as well. 11:25
17 BY MS. ZHONG: 11:25
18 Q. But if you are not building a JEDEC 11:25
19 compliant memory module, does that memory module 11:26
20 have to receive a chip select signal? 11:26
21 MR. CHANDLER: Objection. Form. 11:26
22 THE WITNESS: It would depend on the purpose 11:26
23 that you were designing the module for and what 11:26
24 capabilities you wanted it to have. There may be 11:26
25 ways to not have a chip select signal externally in 11:26

1 very specific circumstances. 11:26

2 BY MS. ZHONG: 11:26

3 Q. Are you familiar with a Rambus system? 11:26

4 A. There were more than one Rambus system, but 11:26

5 I'm familiar with some of the ones that existed 20, 11:26

6 25 years ago. 11:27

7 Q. Okay. In those Rambus memory modules, do 11:27

8 they involve chip select signals? 11:27

9 MR. CHANDLER: Objection. Outside the scope 11:27

10 of direct. 11:27

11 THE WITNESS: I don't remember the details. 11:27

12 There was -- there was some communication related to 11:27

13 selection, but I don't remember the actual form. 11:27

14 BY MS. ZHONG:

15 Q. When you say "there was some communication 11:27

16 related to selection," selecting of a particular 11:27

17 chip, a group of chips, or what is the selection? 11:27

18 MR. CHANDLER: Objection. Outside the scope 11:27

19 of direct. 11:27

20 THE WITNESS: I don't recall. 11:27

21 BY MS. ZHONG: 11:27

22 Q. And let's go back to Kim. 11:28

23 Why does Kim believe that Figure 1 has a 11:28

24 problem that is described in paragraph 42, but 11:28

25 Figure 3 overcomes that issue? 11:28

1 A. In Figure 1, both reads and writes to the 11:28
2 first rank, Rank0, have to go through the same set 11:28
3 of stages, which then combine at the bus DQ0 and 11:29
4 DQ1. 11:29
5 In Figure 3, there is one set of write 11:29
6 stages shared between Rank0 and Rank1, and one set 11:29
7 of read is shared between Rank0 and Rank1. And in 11:29
8 the very particular circumstance that Kim is 11:29
9 concerned about in that portion of his disclosure, 11:29
10 this can resolve the problem. 11:29
11 Q. Why? 11:29
12 A. Because the -- let me see if I can see why. 11:30
13 It's because the assumption in Figure 1 is 11:32
14 that write data is sent out on both GI01 and GI02 at 11:32
15 the same time, and in Figure 3, because of the 11:32
16 selecting unit, it's only sent out on one or the 11:32
17 other and that solves the problem. 11:32
18 Q. Why is the assumption -- let's focus on 11:32
19 Figure 1. 11:33
20 A. I'm sorry. I missed a few words. 11:33
21 Q. Let's just focus on Figure 1. 11:33
22 A. Yes. 11:33
23 Q. Okay. So why is the assumption that if 11:33
24 write data is sent on both GI01 and GI02 in Figure 1 11:33
25 would cause a read-after-write collision? 11:33

1	A. Well, that's what's illustrated in	11:33
2	Figure 4A.	11:33

3	Q. Okay.	11:33
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4	A. And I think that the idea is that even	11:33
5	though the -- is that one of those is performing a	11:33
6	read and the other one is performing a write, and	11:33
7	the write data is going to be sent out on the same	11:33
8	wire.	11:33

9	So, for example, Rank0 is reading and then a	11:33
10	write operation happens, and the Figure 1 system is	11:33
11	not smart enough to know that it only needs to write	11:34
12	to Rank1 and it tries to write to both of them and	11:34
13	that's what causes the collision.	11:34

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14      Q.    But the read would happen after the write is 11:34
15 done because by that time --                                11:34

```

16	A. No. Because Figure A shows that that's not	11:34
17	what happens.	11:34

18	Q. But isn't that what's supposed to happen	11:34
19	though? When you have a read after write, you wait	11:34
20	until the read is done before you start to read the	11:34
21	data?	11:34

22 MR. CHANDLER: Objection. Form. 11:34

23	THE WITNESS: I'm sorry. I don't	11:34
24	understand. You wait until the read is done before	11:34
25	you start to read out the data?	11:34

1 BY MS. ZHONG: 11:34

2 Q. No. You wait until the write is done before 11:34

3 you do the read operation. 11:34

4 A. That would be a good solution, but it's not 11:34

5 the one in Figure 4A. 11:34

6 Q. When does the Figure 4A scenario happen? 11:35

7 A. When you do a write operation to Rank0 11:35

8 immediately followed by a read operation to Rank1. 11:35

9 And the reason is because Rank1 is not receiving the 11:35

10 write operation even though it is receiving the 11:35

11 write data and it, as a result, doesn't know that a 11:35

12 write is in progress. 11:35

13 Q. Okay. So now let's look at Figure 3, and 11:35

14 assume that now you have four ranks, with two ranks 11:35

15 connected to GIO_Rank0 and two ranks connected to 11:35

16 GIO_Rank1. 11:35

17 Do you have that in mind? 11:35

18 A. Understood. 11:35

19 Q. Okay. So in that scenario, if I -- and 11:35

20 let's assume that it is Rank0 and Rank2 connected to 11:36

21 Rank0 GIO and Rank1 and Rank3 connected to Rank1 11:36

22 GIO. 11:36

23 A. Yes. 11:36

24 Q. So now, if you do a read operation from 11:36

25 Rank0, immediately after a write operation to Rank2, 11:36

1 would the read-after-write collision that is 11:36
2 described in Figure 1 occur? 11:36
3 MR. CHANDLER: Objection. Form. 11:36
4 THE WITNESS: It would occur if you designed 11:36
5 it in an extraordinarily naive way. A person of 11:36
6 ordinary skill would add additional mechanisms 11:37
7 routinely to prevent that, either by telling the 11:37
8 memory controller that that was not permitted or by 11:37
9 adding some additional control logic to either the 11:37
10 memory ranks or the interface chip that would delay 11:37
11 one operation to avoid those collisions. 11:37
12 BY MS. ZHONG: 11:37
13 Q. But couldn't those be done to the Figure 1 11:37
14 configuration as well to prevent that collision? 11:37
15 A. Absolutely. There is no suggestion that 11:37
16 Kim's solution is the only way to solve this 11:37
17 problem. 11:37
18 Q. Okay. So if you just do -- collect Rank0 -- 11:37
19 Rank2 to the GIO line -- so if you just connect 11:37
20 Rank0 and Rank2 to the same GIO lines, and if -- let 11:38
21 me see -- if you have all the right control signals 11:38
22 or the right electrical connection and the right 11:38
23 timing, can the read and the write collision be 11:38
24 avoided? 11:38
25 MR. CHANDLER: Objection. Form and 11:38

1 incomplete. 11:38

2 THE WITNESS: Yes. If you get all the 11:38

3 control signals and control state machines correct, 11:38

4 the read-after-write collision can be avoided. 11:38

5 BY MS. ZHONG: 11:38

6 Q. And can the read-after-write collision be 11:38

7 avoided with Figure 1 with a different timing 11:38

8 mechanism? 11:38

9 MR. CHANDLER: Objection. Form. 11:38

10 THE WITNESS: Yes. Kim's is not the only 11:38

11 solution to this problem. There are others. 11:38

12 BY MS. ZHONG: 11:39

13 Q. But it requires additional design changes. 11:39

14 Simply connecting a Rank2 device to the common 11:39

15 GIO_Rank0 line may still cause a data collision 11:39

16 between Rank0 and Rank2; is that right? 11:39

17 MR. CHANDLER: Objection. Form. 11:39

18 Incomplete. 11:39

19 THE WITNESS: It could, but a person of 11:39

20 ordinary skill would recognize that that is an 11:39

21 inappropriate design. They would make the 11:39

22 appropriate routine changes to accommodate the 11:39

23 addition of more ranks. 11:39

24 BY MS. ZHONG: 11:39

25 Q. Okay. 11:39

1 A. Also, that's not the only way to add more 11:39
2 ranks, right. Two more ranks could be added by just 11:39
3 adding more ports to the write-selecting unit and 11:39
4 the read-selecting unit. 11:39
5 Q. Understood. 11:39
6 If that is the way you are -- let's say 11:39
7 the way that you're adding additional branches or 11:40
8 additional GIO lines to accommodate additional 11:40
9 ranks, how would that translate to a stacked 11:40
10 configuration similar to Figure 5 then -- 11:40
11 (Clarification requested by Reporter.) 11:40
12 BY MS. ZHONG: 11:40
13 Q. -- a stacked configuration shown in 11:40
14 Figure 5? 11:40
15 MR. CHANDLER: Objection. Form. 11:40
16 THE WITNESS: If you were to add to the 11:40
17 stack in Figure 5, you would have a design choice. 11:40
18 You could either add additional die sharing one of 11:40
19 the TSVs, or you could add additional die with their 11:40
20 own TSVs. Either one would be obvious. 11:41
21 BY MS. ZHONG: 11:41
22 Q. Okay. What would be the design advantage of 11:41
23 having a separate GIO design for each rank of die? 11:41
24 A. It could have a slightly reduced load and it 11:41
25 could have very minor simplifications to the control 11:41

1 circuit, but there would be a tradeoff in that it 11:41
2 would require larger circuitry in the write-selecting 11:41
3 unit and read-selecting unit and it would take up 11:41
4 more space on each die. So the low-cost solution 11:41
5 would be to share the TSVs. 11:41
6 Q. Okay. And when you share a TSV, for 11:41
7 example, like for GIO_Rank0 TSV 1, you would share, 11:42
8 for example, Rank2 with that TSV. And when you do 11:42
9 that, what additional modifications do you need in 11:42
10 order to make sure that there are no data collisions 11:42
11 across a TSV 1 wire? 11:42
12 MR. CHANDLER: Object to form. 11:42
13 THE WITNESS: You would use the same 11:42
14 ordinary techniques that you would normally use in 11:42
15 building a multirank memory system. You would look 11:42
16 at the timing of each operation, and you would make 11:42
17 sure that any sequence of operations that would 11:42
18 cause a data collision is disallowed or rescheduled 11:42
19 in exactly the ordinary way as when you combine 11:42
20 multiple memory die without stacking. It's exactly 11:43
21 equivalent. 11:43
22 BY MS. ZHONG: 11:43
23 Q. So you have to do additional modifications? 11:43
24 For example, you have to make sure that the timing 11:43
25 is correct when the data is read out or transmitted 11:43

1 to the dies in different ranks; is that right? 11:43

2 MR. CHANDLER: Objection. Form. 11:43

3 THE WITNESS: If you change the number of 11:43

4 ranks, you do need to make routine changes to the 11:43

5 control circuitry as well in exactly the way it was 11:43

6 done for nonstacked systems at the time and the way 11:43

7 that was described in earlier published patents. 11:43

8 BY MS. ZHONG: 11:43

9 Q. Okay. What would be the advantage of using 11:43

10 the Figure 1 configuration compared to Figure 3? 11:44

11 MR. CHANDLER: Objection. Form. 11:44

12 THE WITNESS: I don't know. I haven't 11:44

13 thought about it. 11:44

14 BY MS. ZHONG: 11:44

15 Q. Well, Kim describes the Figure 1 11:44

16 configuration as a typical semiconductor memory 11:44

17 apparatus; right? 11:44

18 A. Yes. 11:44

19 Q. There must be some reason why people are 11:44

20 using it as a typical design. 11:45

21 MR. CHANDLER: Object to form. 11:45

22 THE WITNESS: I'm sure there are. I just 11:45

23 haven't thought about what that is. 11:45

24 BY MS. ZHONG:

25 Q. So do you know of any advantage of the 11:45

1 Figure 1 configuration compared to Figure 3? 11:45

2 A. Again, I haven't thought about it. 11:45

3 Q. And in the Figure 1 configuration, why are 11:45

4 there two different DQ pads? The DQ0 and the DQ1 11:45

5 are connected; correct? 11:45

6 A. Yes. 11:45

7 Q. So electrically, they can be collapsed into 11:45

8 a single pad; is that correct? 11:45

9 MR. CHANDLER: Objection. Form. 11:46

10 THE WITNESS: I think that the suggestion -- 11:46

11 let me look here. 30 and 40. 11:46

12 The assumption here is that in Figure 1, 11:46

13 there are two different input and output sections 11:46

14 that include separate pads, so that is simply an 11:46

15 assumption in that design. Sure, one could do it 11:46

16 differently. 11:46

17 BY MS. ZHONG: 11:46

18 Q. Would there be any performance difference if 11:46

19 you used a single DQ output that is connected to the 11:46

20 two GIO lines? 11:46

21 A. Well, the DQ outputs are not connected to 11:46

22 the GIO lines. 11:47

23 Q. Okay. So -- sorry, that was put badly. 11:47

24 So what if you have a single DQ line that is 11:47

25 connected to both circuit 30 and circuit 40? 11:47

1 MR. CHANDLER: Objection. Form. 11:47

2 THE WITNESS: You would have to analyze the 11:47

3 particular circumstances. It is not even clear that 11:47

4 30 and 40 are on the same chip in all situations. 11:47

5 BY MS. ZHONG: 11:47

6 Q. So you think that in Figure 1, the circuitry 11:47

7 above the dashed line may be on one chip and the 11:47

8 circuitry below the dashed line may be on another 11:47

9 chip? 11:47

10 A. I think that would certainly be consistent 11:47

11 with the description in -- yeah. 11:48

12 Q. And then you tie the data output pins from 11:48

13 the two chips together? 11:48

14 A. Sure. We do that all the time. We tie the 11:48

15 data output chips from multiple chips together. 11:48

16 Q. Why would you do that? 11:48

17 A. So that they can share communication wires. 11:48

18 Q. And those two chips have to belong to two 11:48

19 different ranks; right? They can't belong to the 11:48

20 same rank? 11:48

21 A. I'm not sure what you mean by "belong to." 11:48

22 But in Figure 1, they are illustrated as being 11:48

23 associated with two different ranks. 11:49

24 Q. Can they belong to the same rank -- 11:49

25 MR. CHANDLER: Objection. Form. 11:49

1 BY MS. ZHONG: 11:49

2 Q. -- and have this configuration? 11:49

3 MR. CHANDLER: Objection. Form. 11:49

4 THE WITNESS: That's not what's described 11:49

5 in Figure 1. I mean, again, people of skill in 11:49

6 memory design can make all kinds of modifications. 11:49

7 It's a very rich space for design, but that's not 11:49

8 what's described in Figure 1. 11:49

9 BY MS. ZHONG: 11:49

10 Q. But would a POSITA make such a change that 11:49

11 both chips are -- both chips belong to the same rank 11:49

12 and their DQ lines -- their DQ pads are connected 11:49

13 together? 11:49

14 A. I don't know. I haven't done an evaluation 11:49

15 for Figure 1. 11:49

16 Q. Would that be a problem when you receive a 11:49

17 single read and write command and the data from the 11:49

18 two chips belonging to the same rank would be 11:50

19 outputting the data together? 11:50

20 A. I haven't done the analysis of that modified 11:50

21 Figure 1. 11:50

22 Q. Okay. Have you done an analysis for 11:50

23 Figure 3, if the chip 100 and chip 200 belonged to 11:50

24 the same rank, the same physical rank instead of 11:50

25 different ranks? 11:50

1 MR. CHANDLER: Objection. Form. 11:50

2 THE WITNESS: No. I have not considered a 11:50

3 case where 100 and 200 belong to the same rank. 11:50

4 BY MS. ZHONG: 11:50

5 Q. Do you think that the system would work if 11:50

6 100 and 200 are not the same physical rank? 11:50

7 A. I think a person of ordinary skill could 11:51

8 make that system work, but it would be very unusual 11:51

9 in a memory system to be able to make a change 11:51

10 without having to make changes to the control signal 11:51

11 timing. You would always have to go through routine 11:51

12 steps to make all the parts compatible with each 11:51

13 other. 11:51

14 Q. And can you tell me where in your 11:51

15 declaration you specified the changes that is 11:51

16 required when you make a modification to Kim 11:51

17 Figure 5? 11:51

18 MR. CHANDLER: Objection. Form. 11:51

19 THE WITNESS: There may be a number of 11:51

20 discussions with respect to very specific claims, 11:52

21 but generally, paragraphs 150 through 168 describe 11:52

22 the modifications, if necessary. 11:53

23 They include looking to Rajan to get the 11:53

24 specifics of the host interface, even though there 11:53

25 is clearly one in Kim. And to the extent that the 11:53

1 claims require more than one die per group, Rajan 11:53
2 provides guidance as to how to connect more than one 11:53
3 die per group. 11:53
4 MR. CHANDLER: Which exhibit of which IPR 11:53
5 are we talking about? 11:53
6 THE WITNESS: Well, it's Exhibit 1003 11:53
7 because they are both 1003, but I am looking at 11:53
8 Exhibit 3 of the 1428. Exhibit 1003 of 1428. 11:53
9 BY MS. ZHONG: 11:54
10 Q. The Exhibit 1003, Wolfe declaration for the 11:54
11 '160. 11:54
12 A. Yes. 11:54
13 Q. So in Rajan, let's just look at the Figure 4 11:54
14 you excerpted on page 67 of your declaration, 11:54
15 Exhibit 103 from the '160 proceeding. 11:54
16 A. Yes. 11:54
17 MR. CHANDLER: I just need one minute to get 11:54
18 the exhibit here you are talking about. So this is 11:54
19 IPR 1428, Exhibit 1003 is what we are looking at? 11:54
20 MS. ZHONG: Yes. 11:55
21 MR. CHANDLER: All right. And then you said 11:55
22 page 67? 11:55
23 MS. ZHONG: Yes. 11:55
24 MR. CHANDLER: All right. I am with you 11:55
25 guys. 11:55

1 BY MS. ZHONG: 11:55

2 Q. Okay. So you see an annotated Figure 4 from 11:55

3 Rajan? 11:55

4 A. Yes. 11:55

5 Q. And so you are grouping the two bottom dies, 11:55

6 417C and 417B, as one group and the two top dies, 11:55

7 417A and the 417B, as another group; correct? 11:55

8 A. That would be one embodiment that would be 11:55

9 obvious, yes. 11:56

10 Q. Okay. And are the two dies 417A and 417B in 11:56

11 the same rank or different ranks? 11:56

12 A. Either would be obvious. 11:56

13 Q. Okay. And what about 417C and 417D, do they 11:56

14 belong to the same rank or different ranks? 11:56

15 A. You would configure them in a corresponding 11:56

16 manner to 417A and 417B. So you could either have 11:56

17 two ranks -- well, let's see. 11:56

18 What would make sense -- you could either 11:56

19 have -- well, no. In this implementation, you would 11:56

20 have two ranks, one rank would be 417A and 417C, and 11:57

21 the other rank would be 417B and 417D. 11:57

22 Q. So why wouldn't you have 417A and 417B in 11:57

23 the same rank? 11:57

24 A. Because they're connected to the same TSV. 11:57

25 You could do that in different parts of the address 11:57

1 space -- 11:57

2 Q. Okay. 11:57

3 A. -- but that's not what I'm relying on. 11:57

4 Q. So if 417A and 417B belonged to the same 11:57

5 rank and they're connected to the same data wire, 11:57

6 there potentially can be collision issues and 11:57

7 current issues if they output data at the same time; 11:58

8 is that right? 11:58

9 A. That is a big if. You would never let them 11:58

10 output data at the same time if you made them in the 11:58

11 same rank. You would -- you would put them in 11:58

12 different places of the address space so only one or 11:58

13 the other was operable. 11:58

14 Q. But if they are in the same rank, then they 11:58

15 would be responding to the chip selection or read 11:58

16 commands and output data simultaneously, wouldn't 11:58

17 they? Isn't that what a rank of memory does? 11:58

18 A. I guess that's right. So you wouldn't put 11:58

19 them in the same rank, then, unless you had some 11:58

20 local modification to be able to do -- yeah. So you 11:58

21 wouldn't put them in the same rank. Again, that is 11:58

22 not what I relied on. 11:58

23 Q. What did you rely on? Did you rely on 417A 11:58

24 and 417C be in one rank, and 417B and 417D in 11:59

25 another rank? 11:59

1	A. Yes.	11:59
2	Q. And so how would your modification for Kim	11:59
3	be then?	11:59
4	A. So -- let me start over again here.	11:59
5	So that is one embodiment that I rely on for	11:59
6	all the claims. It's also possible to have four	11:59
7	separate ranks here, right. That doesn't cover all	11:59
8	the claims, but it covers many of the claims.	11:59
9	The modification to Kim is just as we talked	11:59
10	about. To the extent that the claims require more	11:59
11	than one die in a rank, it would be obvious to	11:59
12	connect them in the manner that is shown in	11:59
13	Figure 4, which is a well-known way to do rank	12:00
14	multiplication.	12:00
15	Q. And is it your opinion that Rajan discloses	12:00
16	TSV connection?	12:00
17	MR. CHANDLER: I think it is R-a-j-a-n,	12:01
18	Rajan.	12:01
19	THE WITNESS: No. Rajan -- let me look at	12:01
20	one more thing.	12:01
21	Rajan discloses a stacked configuration, but	12:02
22	doesn't express any preference as to how the wiring	12:02
23	occurs in the stack. Kim teaches to use TSVs as a	12:02
24	preferential wiring mechanism.	12:02
25	/ / /	12:02

1	BY MS. ZHONG:	12:02
2	Q. So how does Rajan's DRAM circuits differ	12:02
3	from Riho's SDRAM dies?	12:02
4	MR. CHANDLER: Objection. Form.	12:03
5	THE WITNESS: Both Rajan and Riho don't	12:03
6	restrict their embodiments to DRAM at all. They	12:03
7	both incorporate many different kinds of memories.	12:03
8	Both give exemplary configurations.	12:03
9	I haven't compared the similarities or	12:03
10	differences between Riho and Rajan's exemplary	12:03
11	configurations, but in either case, they're	12:03
12	applicable to DRAM, SRAM and flash memory, and a	12:03
13	person of ordinary skill could adapt them in either	12:03
14	way.	12:03
15	Rajan in his own implementation doesn't	12:03
16	require the transmission gate switches. Riho in his	12:03
17	preferred embodiment does include the transmission	12:04
18	gate switches. But other than that, they are both	12:04
19	applicable to a wide range of memories.	12:04
20	BY MS. ZHONG:	12:04
21	Q. So Riho's SDRAM dies can be different than	12:04
22	Rajan's DRAM circuits even though both comprises	12:04
23	DRAM cells; is that correct?	12:04
24	MR. CHANDLER: Objection. Form.	12:04
25	THE WITNESS: If by "difference," you mean	12:04

1	that they do not need to be identical in every	12:04
2	aspect in all embodiments, then they could be	12:04
3	different.	12:04
4	BY MS. ZHONG:	12:04
5	Q. What's your interpretation of Samsung's	12:04
6	claim construction that array dies are different	12:05
7	than DRAM circuits?	12:05
8	MR. CHANDLER: Objection. Form.	12:05
9	BY MS. ZHONG:	12:05
10	Q. When would a SDRAM die be different than a	12:05
11	DRAM circuit?	12:05
12	A. I don't believe an SDRAM die is ever	12:05
13	different than a DRAM circuit. I think all SDRAM	12:05
14	dies within this claim construction would be DRAM	12:05
15	circuits.	12:05
16	That's why I focused on the fact that both	12:05
17	Rajan and Riho and Kim and Wyman are not restricted	12:05
18	to DRAM dies or SDRAM dies.	12:05
19	Q. Okay. Can you take a look at your	12:05
20	paragraph 196.	12:06
21	A. This is in the 1428 declaration?	12:06
22	Q. Correct. Correct. Page 89.	12:06
23	A. Okay. Give me a second to read it.	12:06
24	Okay.	12:07
25	Q. Are the citations here specific for the	12:07

1 SDRAMs? 12:07

2 A. No. They're specific to a SDRAM-compatible 12:07

3 external interface. But Rajan, in particular, is 12:07

4 clear in its teachings that the internal memory type 12:07

5 does not need to be the same as the external 12:07

6 interface. 12:07

7 And Kim, as well, is clear that the external 12:07

8 interface is distinct from the internal chip level 12:07

9 interface. So these have to do with the external 12:07

10 interface, but not -- are not specific to any 12:07

11 particular type or generation of stacked memory 12:08

12 dies. 12:08

13 Q. So you can use these for NAND chips, as 12:08

14 well, even though those are JEDEC specifications for 12:08

15 DDR3 memories? 12:08

16 A. Yes. That's among the teachings that are in 12:08

17 Rajan in particular, is that you can build an 12:08

18 interface in which you adopt an external 12:08

19 communication standard, but use a different type of 12:08

20 memory internally. 12:08

21 Q. So, basically, you are saying you are going 12:08

22 to use NAND chips with DRAM communication protocols? 12:08

23 A. Yes. That is contemplated by this 12:08

24 combination. 12:08

25 Q. And what would that entail? Is that easily 12:08

1	doable?	12:08
2	A. It's routinely doable. I mean, nothing in	12:08
3	designing a memory system is easy in the sense that	12:09
4	it can be done in a few minutes, but it does not	12:09
5	require any experimentation or invention. It would	12:09
6	simply be converting one memory interface to	12:09
7	another. It's done all the time.	12:09
8	Q. You are saying that people routinely use a	12:09
9	NAND chip with a DRAM interface and the vice versa?	12:09
10	A. No. I'm saying that people would know how	12:09
11	to do that. So some of the examples are a little	12:09
12	bit different. For example, it is very, very common	12:09
13	to use DRAM with an SRAM interface. That's been	12:09
14	very, very common for decades.	12:09
15	But there also are a number of people who	12:09
16	over the years have designed nonvolatile DIMMs that	12:09
17	would use a DRAM-type interface to connect to a	12:09
18	nonvolatile memory such as flash to prevent data	12:10
19	loss in a power failure, for example.	12:10
20	Q. And where in Rajan is that taught, aside	12:10
21	from the general reference that the memory -- the	12:10
22	type of memory is not limited? Where does it say it	12:10
23	is going to use one type of memory and different	12:10
24	interface?	12:10
25	A. There are a number of citations in my	12:10

1 declaration. I can go through and try to find them 12:10
2 all for you. 12:10
3 Q. Okay. 12:10
4 A. So Rajan talks in a number of places about 12:10
5 "emulated interfaces." One of the places is in 12:12
6 column 3. In this particular example, he talks 12:12
7 about emulating one JEDEC DDR3 memory standard using 12:12
8 DDR2 memory chips, in column 3 at lines 52 to 61. 12:12
9 As we discussed, he talks about how his 12:12
10 invention can be built with any kind of memory 12:13
11 technology, including flash and SRAM, and other 12:13
12 kinds of memory. But also in column 4, starting at 12:13
13 line 20, he talks about how you can have a JEDEC 12:13
14 compliant host interface. He doesn't limit that to 12:13
15 any particular kind of memory. 12:13
16 I think there are some more things. 12:13
17 Figure 18 shows this kind of emulation strategy, and 12:13
18 there's a section in column 12, starting at line 14, 12:13
19 describing Figure 16 that involves changing the 12:13
20 interface to represent a different size of DRAM. 12:13
21 There's also a description of doing that at 12:14
22 the bottom of column 12 in the last paragraph there. 12:14
23 And then in column 14, there is a 12:14
24 description of Figure 18 where it describes that the 12:14
25 host interface and the physical memory can have 12:14

1 different attributes and that the attributes of one 12:14
2 may be emulated in the other. 12:14
3 And let's see. 51... So I think when you 12:14
4 take that together with the disclosure in 15, where 12:14
5 it lists all the memory types, and then says that as 12:15
6 physical memory circuits including NAND flash, NOR 12:15
7 flash, SRAM, and then it says the physical memory 12:15
8 circuits may be coupled to any type of memory 12:15
9 module, such as DIMM, RDIMM, SO-DIMM, those are 12:15
10 particular JEDEC types, so I think it makes the 12:15
11 connection there as well. 12:15
12 MR. CHANDLER: What exhibit are you looking 12:15
13 at? 12:15
14 THE WITNESS: I am looking at 12:15
15 Exhibit 1026 -- no, 1016. 12:15
16 MR. CHANDLER: You mean 1015? 12:15
17 MS. ZHONG: 1015. I think it's 1015. 12:15
18 THE WITNESS: 1015. Yes. 12:15
19 MR. CHANDLER: All right. 12:15
20 THE WITNESS: The '881 patent. 12:15
21 There is also a useful disclosure in 1015 at 12:17
22 column 8, line 6 through 15. 12:17
23 BY MS. ZHONG: 12:18
24 Q. Have you personally designed a system where 12:18
25 you emulate NAND with a DRAM interface? 12:18

1 of a DRAM circuit, but when read in the context of 12:21
2 those specifications as a whole, I think a person 12:21
3 of ordinary skill would understand that there is 12:21
4 nothing that limits the teaching of Figure 4 or that 12:21
5 embodiment to DRAM. 12:21
6 BY MS. ZHONG: 12:21
7 Q. Okay. And the teachings for a DRAM circuit 12:21
8 design can be readily applied to NAND memory design 12:21
9 systems, SRAM designs; correct? 12:22
10 A. The teachings that I relied on in Rajan can. 12:22
11 MS. ZHONG: Okay. Why don't we take a lunch 12:22
12 break. An hour? 12:22
13 DEPOSITION REPORTER: Why don't we go off 12:22
14 the record. 12:22
15 MR. CHANDLER: Okay. 12:22
16 (Lunch recess.) 12:22
17 BY MS. ZHONG: 13:12
18 Q. Dr. Wolfe, do you have Exhibit 1024 with you 13:13
19 which is Ruckerbauer? 13:13
20 A. I will load it from the site. 13:13
21 Q. Are you familiar with Ruckerbauer? 13:13
22 A. In a limited sense, I used Figure 5 of 13:13
23 Ruckerbauer to be -- simply be exemplary of some of 13:13
24 the opinions that I had. 13:13
25 Q. Okay. So can you go to Figure 5A of 13:13

1 Ruckerbauer. 13:13

2 A. Okay. 13:14

3 Q. You have seen this figure before; right? 13:14

4 A. I've seen it, but I don't recall what 13:14

5 Ruckerbauer said about it. As I said, I used this 13:14

6 in a very limited sense. 13:14

7 Q. Okay. Can you perhaps read Ruckerbauer, 13:14

8 column 9, line 66 and 8. 13:14

9 A. I'm sorry. The lines one more time. 13:14

10 Q. Actually, how about 10, 2 to 10, 8, column 13:14

11 10 line 2 to 8? 13:15

12 A. I need to read some earlier portions to 13:15

13 understand what this is referring to. 13:15

14 Okay. I read it. Again, I didn't rely on 13:16

15 this portion of this reference so I'm just getting 13:16

16 familiar with it. 13:16

17 Q. Okay. I just have a couple of questions for 13:16

18 you. Let's just focus on the two TSVs, 112a and 13:16

19 112b, on the left-hand side. 13:16

20 Are you there? 13:16

21 A. Yes. 13:16

22 Q. And do you also see that in each of the dies 13:16

23 110a to 110b associated with the TSVs 112a and 112b, 13:17

24 each of the die has two bidirectional buffers, 10a 13:17

25 and 10b? 13:17

1 A. I see that for the two masters. I don't see 13:17
2 the numbering for the slaves. 13:17

3 Q. The masters and slaves are identical so they 13:17
4 are just discussing like using 110a and 110b as the 13:17
5 example. 13:17

6 A. Okay. 13:17

7 MR. CHANDLER: Objection. Form. And I 13:17
8 guess outside the scope of direct. 13:17

9 BY MS. ZHONG: 13:17

10 Q. So if you just read column 9, lines 52 to 13:17
11 55, and satisfy yourself that the slave and the 13:18
12 master are organized the same. 13:18

13 DEPOSITION REPORTER: Miss Zhong, are you 13:18
14 able to get your phone a little closer to you. 13:18
15 Thank you. 13:18

16 MS. ZHONG: Yeah. 13:18

17 THE WITNESS: It appears that way based on 13:18
18 what I see right now. 13:18

19 BY MS. ZHONG: 13:18

20 Q. Okay. So each of the dies 110a and -- to 13:18
21 110b has two -- 13:18

22 DEPOSITION REPORTER: I need that again,
23 each of the dies 110a and 110b have...

24 BY MS. ZHONG:

25 Q. Sorry. Each of the dies 110a through 110D, 13:19

1 D as in dog, has two bidirectional buffers 10a and 13:19
2 10b associated with TSVs 112a and 112b; correct? 13:19
3 DEPOSITION REPORTER: D or B?
4 MS. ZHONG: B. 13:19
5 MR. CHANDLER: B as in boy. 13:19
6 THE WITNESS: It depends on what you mean by 13:19
7 "associated with." 13:19
8 BY MS. ZHONG: 13:19
9 Q. So take a look at die 110a and the segment 13:19
10 of TSV112A in 110a. 13:19
11 Are you there? 13:20
12 A. Yes. 13:20
13 Q. It is physically coupled to buffer 10a; is 13:20
14 that correct? 13:20
15 MR. CHANDLER: Objection. Form. 13:20
16 THE WITNESS: I don't know at the moment. 13:20
17 There's a -- let's see, dash lines indicate physical 13:20
18 connections which are not used for electrical 13:20
19 coupling. 13:20
20 So, yeah, that appears to be a physical 13:20
21 connection that is not used for an electrical 13:20
22 coupling. 13:20
23 BY MS. ZHONG:
24 Q. Okay. So one of the ways that there is no 13:20
25 electrical coupling is by basically switching the 13:20

1 buffer off; correct? According to Ruckerbauer, 13:20
2 column 10, 2 through 5. 13:20
3 MR. CHANDLER: Objection. Form. And also 13:20
4 outside the scope of direct. 13:21
5 THE WITNESS: It might be. I'm reading this 13:21
6 out of context, but it seems to indicate that one 13:21
7 way of achieving connectivity is to use an enabled 13:21
8 signal. It says or by any other appropriate 13:21
9 measure. 13:21
10 BY MS. ZHONG: 13:21
11 Q. Okay. So one of the ways to turn off the 13:21
12 buffer to decouple electrically, does buffer 10a for 13:21
13 the 112a TSV [indiscernible] -- 13:22
14 (Clarification requested by Reporter.) 13:22
15 BY MS. ZHONG: 13:22
16 Q. -- electrically is by disabling the 13:22
17 bidirectional buffering? 13:22
18 MR. CHANDLER: Objection. Form. Also 13:22
19 outside the scope of the direct. 13:22
20 THE WITNESS: What buffer are we talking 13:22
21 about? 13:22
22 BY MS. ZHONG: 13:22
23 Q. 10a. 13:22
24 A. 10a? 10a is not a buffer. 13:22
25 Q. 10a. It is. If you look at column 9, line 13:22

1	67.	13:22
2	A. Oh, yes. In this particular embodiment, it	13:22
3	appears that one of the ways disclosed to decouple	13:22
4	the electrical connection for buffer 10a is through	13:22
5	an enable signal.	13:23
6	Q. Okay. So when the buffer --	13:23
7	A. I'm not sure that that's -- I'm not sure	13:23
8	what the structure of that buffer is. I have to --	13:23
9	I believe that that is a structure similar to	13:23
10	Figure 8, but I'd have to do some more analysis.	13:23
11	Q. So if the buffer is turned off through a	13:23
12	disable signal, does the TSV 112a experience a load	13:23
13	from the buffer nevertheless?	13:23
14	(Clarification requested by Reporter.)	13:23
15	THE WITNESS: So this is a different	13:23
16	configuration than is found in Riho, a different	13:24
17	circuit.	13:24
18	BY MS. ZHONG:	
19	Q. Okay.	13:24
20	A. And it is a bidirectional buffer, which	13:24
21	means it has both an input and an output.	13:24
22	Q. Okay.	
23	A. And, yes, in this particular situation, even	13:24
24	if that particular kind of buffer was disabled, it	13:24
25	would still provide a capacitive load on 112a, if	13:24

1 the method of disabling -- well, again, it depends 13:24
2 on the structure. It depends on the structure of 13:24
3 the particular buffer circuit. 13:24
4 But it would still probably provide a 13:24
5 significant capacitive load. That's one of the 13:24
6 reasons why Riho doesn't use this configuration. It 13:24
7 uses a different one. 13:24
8 Q. Understood. 13:24
9 And that would be -- your answer would you 13:24
10 say for buffer 10b with respect to TSV 112b; 13:25
11 correct? 13:25
12 MR. CHANDLER: Objection. Form. 13:25
13 THE WITNESS: Yes. Understanding that 13:25
14 Exhibit 1024 contemplates a variety of different 13:25
15 embodiments. If the embodiment were to disable the 13:25
16 tristate buffer directly, it would still provide a 13:25
17 capacitive load. Again, that is why Riho uses a 13:25
18 different configuration. 13:25
19 BY MS. ZHONG: 13:25
20 Q. Okay. Would the answer be different if the 13:25
21 disablement is through by switching the buffers to 13:25
22 be used to the supply voltage -- by switching only 13:25
23 the buffers to be used to the supply voltage, that 13:25
24 is --
25 DEPOSITION REPORTER: I'm sorry, it's sort

1 of unclear. By switching only the buffers to be
2 used to the supply voltage, that is -- are you
3 saying tristate? 13:26
4 MR. CHANDLER: I couldn't hear the beginning 13:26
5 either, Anita. I think your phone connection 13:26
6 is somehow more muffled. 13:26
7 MS. ZHONG: You know what. Let me change 13:26
8 my -- can we just go off the record and I will 13:26
9 change the piece. 13:26
10 (Off the record.) 13:26
11 BY MS. ZHONG: 13:29
12 Q. Dr. Wolfe, let's go back to Figure 5A of 13:30
13 Ruckerbauer. 13:30
14 What would -- would the 112a experience a 13:30
15 significant capacitive load if buffer 10a is turned 13:30
16 off by not providing it with supply voltage? 13:30
17 A. Again, you would need the details of any 13:30
18 particular system to know the significance, but it 13:30
19 is likely it would. Again, that is why Riho uses a 13:30
20 different approach. I'm sorry, Rajan uses a 13:30
21 different approach. 13:30
22 Q. Okay. You mean. Riho. 13:30
23 A. Riho, Riho, that's right.
24 Q. Riho is the one with the transmission gauge. 13:30
25 A. Yeah. 13:30

1 Q. So in Ruckerbauer's configuration, as you 13:30
2 understand, as a POSITA would understand, even if 13:30
3 the buffer 10a and 10b are turned off, it is likely 13:30
4 the TSVs will experience some significant capacitive 13:31
5 loads from those buffers; is that right? 13:31
6 A. If they are turned off using the simplest 13:31
7 techniques. Again, Exhibit 1024 contemplates any 13:31
8 other appropriate measure and the transmission gates 13:31
9 in Riho would be another appropriate measure. 13:31
10 Q. Okay. Is there any indication that the 13:31
11 buffer includes a transmission gate? 13:31
12 A. As I said, I'm not familiar with the 13:31
13 entirety of this reference. I haven't really relied 13:31
14 on much more -- I haven't relied on anything other 13:31
15 than Figure 5 so I don't know the answer. 13:31
16 Q. Okay. Does Figure 8 show transmission 13:31
17 gates? 13:31
18 A. From what I can tell, Figure 8 shows the 13:32
19 slave units physically not connected. They are 13:33
20 described as floating and the wires on the 13:33
21 right-hand side appear to not be physically 13:33
22 connected to anything. 13:33
23 Again, I'm not sure what the context for 13:33
24 that is. 13:33
25 Q. Okay. But do they show transmission gates 13:33

1	though?	13:33
2	MR. CHANDLER: Objection. Form.	13:33
3	THE WITNESS: I don't see any from looking	13:33
4	at the figure alone, but again, I don't understand	13:33
5	all the context right now.	13:33
6	BY MS. ZHONG:	13:33
7	Q. Okay. Let's look at Figure 5 in steps 1	13:33
8	that you say you have relied on.	13:34
9	A. Uh-huh.	13:34
10	Q. I'm a little bit confused.	13:34
11	How can the TSVs be floating on their own	13:34
12	without any silicons or array dies supporting them	13:34
13	to go through?	13:34
14	A. Because it's a conceptual drawing, not a	13:34
15	physical drawing. It's just showing what's	13:34
16	connected. It's not trying to show physically where	13:34
17	the TSVs would be located.	13:34
18	Q. Okay. So it's not showing that TSVs are	13:34
19	located outside of the -- the dies and floating in	13:34
20	space?	13:34
21	A. No. The TSVs would be through the middle of	13:34
22	the die. This is just an illustration to make it	13:34
23	easier for one to understand which TSVs connect to	13:34
24	which die.	13:34
25	Q. Okay. And that is also not showing that the	13:34

1 TSVs are located on the edge of the dies. It's just 13:34
2 trying to show like logically which die is connected 13:35
3 to which TSV? 13:35
4 A. Right. It's logical. It's not supposed to 13:35
5 be a physically accurate representation. 13:35
6 Q. Okay. That's all I need to know. 13:35
7 And let's go back to Figure 5A. So in 13:35
8 Figure 5A, would you say that each of the TSVs 112a 13:35
9 and 112b are a multidrop configuration with each of 13:35
10 the dies? 13:35
11 MR. CHANDLER: Object to form. 13:35
12 THE WITNESS: Again, I'm not completely 13:35
13 familiar with this disclosure, but from what I can 13:36
14 see in the figure, it appears that they are. 13:36
15 Although, obviously, there -- there's something -- 13:36
16 there are things that aren't shown in this figure as 13:36
17 well. 13:36
18 BY MS. ZHONG: 13:36
19 Q. Understood. As shown, I'm just talking 13:36
20 about the portion that's shown in the figure. 13:36
21 Or let me put it this way. Based on your 13:37
22 review and your knowledge, is it your opinion that 13:37
23 it appears that 112a and 112b are each in 13:37
24 communication with each of the array dies; is that 13:37
25 right? 13:37

1	A. Oh, no. That's --	13:37
2	MR. CHANDLER: Object to form.	13:37
3	THE WITNESS: -- certainly not the case. I	13:37
4	mean, it's very clear that that's not true.	13:37
5	BY MS. ZHONG:	13:37
6	Q. Each of the 112a -- let's just look at 112a.	13:37
7	112a is experiencing electrical capacitive	13:37
8	loads from 10a in each of the dies; correct?	13:37
9	MR. CHANDLER: Objection. Form.	13:37
10	THE WITNESS: As I said, everything	13:37
11	experiences a capacitive load with everything else	13:37
12	in the universe, so that would always be --	13:38
13	BY MS. ZHONG:	
14	Q. Okay. And 112a is experiencing a	13:38
15	significant load from buffer 10a in each of the	13:38
16	load; is that right?	13:38
17	MR. CHANDLER: Object to form.	13:38
18	THE WITNESS: It would depend on what	13:38
19	embodiment. Again, the main teaching here is that	13:38
20	we're taught that the dashed lines are not used for	13:38
21	electrical coupling. So I would read that to	13:38
22	understand that there is no electrical communication	13:38
23	along the dashed lines.	13:38
24	BY MS. ZHONG:	13:38
25	Q. Okay. What is your understanding of whether	13:38

1	there is electrical communication or not?	13:38
2	A. In general, when signals are being	13:38
3	communicated from one place to another electrically	13:38
4	through a voltage or a current.	13:38
5	Q. Okay. So let's say there is a driver	13:39
6	connected to the TSV, and the driver is disabled	13:39
7	such that the signals from the memory array is not	13:39
8	being driven from the TSV.	13:39
9	In your opinion, is there electrical	13:39
10	communication between the TSV and the memory array?	13:39
11	MR. CHANDLER: Objection. Form.	13:39
12	THE WITNESS: Again, we'd have to look at	13:39
13	specific situations. But in both of -- both in the	13:39
14	Riho reference and in the Ruckerbauer reference,	13:39
15	they are both very explicit that the point of the	13:39
16	configuration is to eliminate the electrical	13:39
17	communication with some of the die while supporting	13:39
18	the electrical communication with other die.	13:40
19	BY MS. ZHONG:	13:40
20	Q. Okay. Let me -- can you please refresh your	13:40
21	Exhibit Share. And looking at Exhibit 2101, which	13:41
22	is an IEEE paper.	13:41
23	MR. CHANDLER: I will need a moment, but I	13:41
24	will let you know when I have it.	13:41
25	MS. ZHONG: Yep. So, it's an IEEE paper, a	13:41

1 conference paper, with the title "A 1.2V 64Gb 341 13:41
2 GB/s HBM2 Stacked DRAM with Spiral Point-to-Point 13:41
3 TSV Structure and Improved Bank Group Data Control" 13:41
4 by SK Hynix. 13:41
5 MR. CHANDLER: Annita, I have got a question 13:42
6 for you. Is it any different from Exhibit 2007 that 13:42
7 you already marked? 13:42
8 MS. ZHONG: Maybe not. 13:42
9 MR. CHANDLER: If not, it might be easier to 13:42
10 stick with Exhibit 2007. 13:42
11 MS. ZHONG: Okay. Yeah. It's the same 13:42
12 paper. So if you can just go to the second page, 13:42
13 Exhibit 12.3.1. 13:42
14 THE WITNESS: Okay. 13:42
15 BY MS. ZHONG: 13:42
16 Q. Okay. Do you see the proposed spiral 13:42
17 configuration? 13:42
18 A. I see it. I haven't read the paper, but I 13:42
19 see it. 13:42
20 Q. Okay. And do you see that there are six 13:42
21 core dies plus a base die in that configuration? 13:43
22 MR. CHANDLER: Objection. Outside the scope
23 of direct. 13:43
24 THE WITNESS: That's what the labels say. 13:43
25 Again, I haven't read the paper. 13:43

1 BY MS. ZHONG:

2 Q. Okay. And do you see the nine purple 13:43

3 highlighted cylinders that forms a spiral kind of a 13:43

4 pathway? 13:43

5 MR. CHANDLER: Object to form. Outside the 13:43

6 direct. 13:43

7 THE WITNESS: I do. One of them is faded 13:43

8 and, again, without reading the specifications, I 13:43

9 don't know what the lines mean. 13:43

10 BY MS. ZHONG: 13:43

11 Q. Okay. So why don't we start from the first 13:43

12 one at the bottom for the base die. 13:43

13 Do you see that one is connected to a set of 13:43

14 receiver and driver? 13:43

15 MR. CHANDLER: Objection. Outside the scope 13:43

16 of direct. 13:43

17 THE WITNESS: Again, I haven't -- haven't 13:44

18 read it, so I don't know what it says about that 13:44

19 drawing. 13:44

20 BY MS. ZHONG: 13:44

21 Q. What's your understanding of those symbols? 13:44

22 MR. CHANDLER: Objection. Outside the scope 13:44

23 of the direct. 13:44

24 THE WITNESS: Without reading the paper, 13:44

25 they appear to be a bidirectional driver. 13:44

1 BY MS. ZHONG: 13:44

2 Q. Okay. So the bottom cylinder, or like the 13:44

3 TSV segment, is connected to a bidirectional driver 13:44

4 as a POSITA would understand, right, with those 13:44

5 electrical symbols -- 13:44

6 A. So this is a 2018 paper. You're asking me 13:44

7 what a POSITA would understand in 2018? 13:44

8 Q. Yes. 13:44

9 MR. CHANDLER: And, Annita, just to be 13:44

10 clear, given that this Exhibit 2101 is the same as 13:44

11 2007, we have the same objections that we already 13:44

12 filed as to 2007. We have those to 2101 as well. 13:44

13 MS. ZHONG: That's fine. 13:45

14 BY MS. ZHONG: 13:45

15 Q. So the first TSV segment in the base is 13:45

16 connected to a bidirectional driver; correct? 13:45

17 A. I don't know. As I'm reading the paper, it 13:45

18 doesn't seem to identify exactly what those things 13:45

19 are at all. One might use that symbol for a 13:45

20 bidirectional driver. 13:45

21 Q. You agree that those will be typically 13:45

22 understood as drivers; right? 13:45

23 MR. CHANDLER: Objection. Outside the scope 13:45

24 of direct. 13:45

25 THE WITNESS: It really depends on context. 13:45

1 BY MS. ZHONG: 13:45

2 Q. So you mean that symbol could mean different 13:45

3 things in 2010 than in 2018? 13:46

4 A. No. It can mean different things in 13:46

5 different drawings, in different papers and subject 13:46

6 matters. It very well could be a bidirectional 13:46

7 driver. 13:46

8 Q. Okay. So if the TSV is connected to 13:46

9 the bidirectional driver in the base, then let's 13:46

10 move up to the second TSV segment corresponding 13:46

11 to the core 0. 13:46

12 Assuming that there are no drivers connected 13:46

13 to that segment of the TSV, can that TSV be in 13:46

14 communication with core die 0? 13:46

15 MR. CHANDLER: Objection. Form and outside 13:47

16 the scope of direct. 13:47

17 THE WITNESS: I'm not following you at all. 13:47

18 On the left-hand drawing, I don't see the dies 13:47

19 labeled with names and I also don't see a driver 13:47

20 that's not connected. 13:47

21 BY MS. ZHONG: 13:47

22 Q. I'm talking about the one in the proposed 13:47

23 spiral P2P. 13:47

24 MR. CHANDLER: Same objection. 13:47

25 / / / 13:47

1 BY MS. ZHONG: 13:47

2 Q. So the segment, the purple segment in the 13:47

3 second segment, that's in the core 0 die. 13:47

4 Do you see that one? 13:47

5 A. Which one are you calling the "second 13:47

6 segment"? 13:47

7 Q. Okay. Let me see that I can share the 13:47

8 screen. 13:47

9 Can you see my screen now? 13:47

10 A. I can, but I can't see the text right now if 13:47

11 you are sharing the screen. Okay. 13:47

12 Q. So here is the one -- here is a segment that 13:48

13 has a bidirectional driver and that's in the base 13:48

14 now. And now let's look at this one.

15 DEPOSITION REPORTER: I need clarification.

16 And that's in the...

17 BY MS. ZHONG:

18 Q. In the core -- let me withdraw and ask. 13:48

19 Do you see the TSV segment that I'm pointing 13:48

20 to that's in the core 0 die? 13:48

21 A. The purple one? 13:48

22 Q. Yes. 13:48

23 A. I see it. 13:48

24 Q. Okay. So this one doesn't have any drivers 13:48

25 connected to it; correct? 13:48

1 MR. CHANDLER: Objection. Form and outside 13:48
2 the scope of direct. 13:48
3 BY MS. ZHONG: 13:48
4 Q. At least as drawn. 13:48
5 MR. CHANDLER: Same objection. 13:48
6 THE WITNESS: Again, I don't understand all 13:48
7 the context of this drawing, but if the purple is 13:48
8 intended to be wiring, then the lower drivers would 13:49
9 be connected to that segment. 13:49
10 BY MS. ZHONG: 13:49
11 Q. Okay. But this one is not connected to any 13:49
12 drivers in the core 0 die; correct? 13:49
13 MR. CHANDLER: Object to form and outside 13:49
14 the scope of direct. 13:49
15 THE WITNESS: I don't know if it is or 13:49
16 isn't. I don't see it being illustrated that way -- 13:49
17 BY MS. ZHONG: 13:49
18 Q. Okay. 13:49
19 A. -- in this particular drawing. 13:49
20 Q. Okay. So if it's not illustrated, it's not 13:49
21 there, and if this TSV segment does not have a 13:49
22 driver in the core 0 die, can it communicate with 13:49
23 core 0 die nevertheless? 13:49
24 MR. CHANDLER: Objection to form and outside 13:49
25 the scope of direct. 13:49

1 THE WITNESS: I don't have nearly enough 13:49
2 information right now to answer that question. 13:49
3 BY MS. ZHONG: 13:50
4 Q. Can any signals be transferred from a memory 13:50
5 cell to this array drive if there are no drivers 13:50
6 connecting the two together? 13:50
7 MR. CHANDLER: Objection to form and outside 13:50
8 the scope of direct. 13:50
9 THE WITNESS: Again, based on what I know 13:50
10 right now, I don't even know if or where there is a 13:50
11 memory die here, and I don't know what else is 13:50
12 connected, so I don't have nearly enough information 13:50
13 to answer that. 13:50
14 BY MS. ZHONG: 13:50
15 Q. Okay. Each of the core die is a memory die. 13:50
16 A. Where does it say that? 13:50
17 Q. Just take my representation that each of the 13:50
18 core die is a DRAM die. 13:50
19 So if this TSV segment doesn't have a driver 13:50
20 associated with it, is it still in communication 13:50
21 with the core 0 die? 13:51
22 MR. CHANDLER: Objection. Form and outside 13:51
23 the scope of direct. 13:51
24 THE WITNESS: It could be. I would need 13:51
25 more information. 13:51

1 BY MS. ZHONG: 13:51

2 Q. When would it be in communication with the 13:51

3 core 0 die? 13:51

4 A. I would have to look at exactly what it is 13:51

5 connected to and how it communicates. There is very 13:51

6 little information here. 13:51

7 Q. It's not connected to any drivers. It's 13:51

8 basically just a pass-through segment, just acting 13:51

9 as a wire. 13:51

10 A. Again, it would depend on the specifics. If 13:51

11 it's not connected through any type of coupling or 13:51

12 anything on the die, then I don't think it can 13:51

13 communicate with anything on the die, but that's a 13:51

14 huge assumption to make based on what I see here. 13:51

15 Q. If the only thing it connects to on the die 13:51

16 is a dummy pad, is it in communication with that

17 die?

18 MR. CHANDLER: Object to form. And

19 outside --

20 DEPOSITION REPORTER: I'm sorry. I need the

21 end of that question. The only thing it connects

22 to...

23 MS. ZHONG: Is a dummy pad. D-u-m-m-y,

24 dummy.

25 THE WITNESS: Again, I -- you know, I don't 13:52

1 know that you are giving me an accurate 13:52
2 representation here. You know, I would want to look 13:52
3 at a circuit before I knew the difference. 13:52
4 BY MS. ZHONG:
5 Q. Okay. So let's go back to Ruckerbauer, look 13:53
6 at 112a and die 110a. 13:53
7 A. In which Figure? 13:53
8 Q. Figure 5A. 13:53
9 A. Okay. 13:53
10 Q. If there isn't even an electrical connect -- 13:53
11 a physical connection between 10a and 112a, is 112a 13:53
12 in electrical communication with die 110a? 13:54
13 MR. CHANDLER: Objection. Form. 13:54
14 THE WITNESS: Ruckerbauer tells us that it 13:54
15 is not. Ruckerbauer tells us that the things that 13:54
16 he's represented with a dotted line are not an 13:54
17 electrical communication, so we don't need to go 13:54
18 past that. 13:54
19 BY MS. ZHONG: 13:54
20 Q. And what about 112b and 10b, if there is no 13:54
21 electrical -- there's no -- that solid line is not 13:54
22 there, is there electrical communication between 13:54
23 112b and 110a? 13:54
24 MR. CHANDLER: Objection. Form. 13:54
25 THE WITNESS: If the solid line was not 13:54

1 there? 13:54

2 BY MS. ZHONG: 13:54

3 Q. Yes. 13:54

4 A. I guess you wouldn't know for sure. I guess 13:54

5 if there was no other connection, then probably not. 13:55

6 Q. What other connections can there be? 13:55

7 A. I don't know. I mean, again, 13:55

8 you're modifying the design. Ruckerbauer has told 13:55

9 us that they are connected over that solid line, so 13:55

10 he doesn't have to tell us one way or another 13:55

11 whether or not there are other connections because 13:55

12 it's irrelevant. 13:55

13 Q. Ruckerbauer also didn't say other than the 13:55

14 dashed line, there are no connections between 110a 13:55

15 and 112a; correct? 13:55

16 MR. CHANDLER: Objection. Form. 13:55

17 THE WITNESS: Ruckerbauer told us that the 13:55

18 solid line in is that they are connected in his 13:55

19 design. 13:55

20 BY MS. ZHONG: 13:55

21 Q. And the dashed line means they are 13:55

22 physically connected but not electrically coupled; 13:55

23 correct? 13:56

24 A. Correct. In Figure 5A, that is the case. 13:56

25 Q. Okay. And what does "electrically coupled" 13:56

1 mean? 13:56

2 MR. CHANDLER: Objection. Form. 13:56

3 THE WITNESS: In this context in 13:56

4 Ruckerbauer, it means capable of reliably 13:56

5 communicating signals from one place to another. 13:56

6 BY MS. ZHONG: 13:56

7 Q. So if there is a physical wire between 112a 13:56

8 and the buffer, there will be electrical waves 13:56

9 traveling between those two parts; right? It could 13:57

10 be signals that's being driven along 112a that gets 13:57

11 side channeled into 10a and is being bounced back. 13:57

12 Wouldn't that happen? 13:57

13 MR. CHANDLER: Objection to form. 13:57

14 THE WITNESS: Except that Ruckerbauer tells 13:57

15 us that it doesn't. So, clearly, it is not used for 13:57

16 electrical coupling. Could there be a tiny stub of 13:57

17 wire or something? Maybe, but Ruckerbauer tells us 13:57

18 to disregard it. 13:57

19 BY MS. ZHONG: 13:57

20 Q. What do you mean by "stub wire"? 13:57

21 A. It's not enough to electrically couple in 13:57

22 a -- in a functional way. He tells us that it is 13:57

23 not electrically coupled. It's very clear. 13:57

24 Q. What is a stub wire? 13:57

25 A. A stub wire would be a little piece of wire 13:57

1 that's not connected to anything or not functionally 13:58
2 connected. 13:58
3 Q. Why would someone use a stub wire? 13:58
4 MR. CHANDLER: Objection. Form. 13:58
5 THE WITNESS: There are various reasons. It 13:58
6 could just be an artifact of disconnecting 13:58
7 something, right. In other words, if you have a 13:58
8 wire that connects two things and you cut it, you 13:58
9 may still have a little piece of the wire there, but 13:58
10 it's not performing a connection function anymore. 13:58
11 BY MS. ZHONG: 13:58
12 Q. Okay. Is a dummy pad a stub wire? 13:58
13 MR. CHANDLER: Objection. Form. And 13:58
14 outside the scope of direct. 13:58
15 THE WITNESS: Again, I don't know what you 13:58
16 mean by "dummy pad," but I wouldn't -- I wouldn't 13:58
17 normally characterize it that way. 13:58
18 BY MS. ZHONG: 13:59
19 Q. But unless 10a has a transmission gate, even 13:59
20 if 10a is disabled, TSV 112a is still going to 13:59
21 experience a significant load from 10a; is that 13:59
22 right? 13:59
23 MR. CHANDLER: Objection. Form. 13:59
24 THE WITNESS: It could be the case, 13:59
25 depending on the particular geometry. Again, that's 13:59

1	why Riho does it differently.	14:00
2	BY MS. ZHONG:	14:00
3	Q. Well, if he uses a circuit shown in	14:00
4	Figure 8B, would the TSV 112a experience a	14:00
5	significant load from 10a even when it's turned off?	14:00
6	MR. CHANDLER: Objection. Form.	14:00
7	THE WITNESS: I haven't done a detailed	14:00
8	analysis. I never suggested that anyone use the	14:00
9	circuit for 5A in any of the combinations that I put	14:00
10	forth in the IPR.	14:00
11	BY MS. ZHONG:	14:00
12	Q. Okay. So you're not suggesting anyone	14:00
13	modifying Kim, Kim's TSV connection in light of	14:01
14	Figure 5A of Ruckerbauer; is that correct?	14:01
15	MR. CHANDLER: Objection. Form.	14:01
16	THE WITNESS: No. I don't think I've ever	14:01
17	suggested that anyone use Figure 5A in Ruckerbauer	14:02
18	to modify Kim.	14:03
19	BY MS. ZHONG:	14:03
20	Q. Okay. Can you pull up Wyman, which I	14:03
21	believe is Exhibit 1017.	14:03
22	A. Okay.	14:03
23	Q. Can you please take a look at Figure 8 and	14:03
24	Figure 5, and the associated disclosure.	14:03
25	A. Okay. I'm pretty familiar with this.	14:04

1 Q. Okay. So in Wyman for the different 14:04
2 segments shown in Figures 8A through 8B, are they 14:04
3 all using the same driver circuit 500 shown in 14:04
4 Figure 5? 14:04
5 A. They can all use that circuit, but Wyman 14:04
6 suggests that it might be most appropriate to 14:04
7 connect figure -- the various stub figures in 14:04
8 Figure 8 to a circuit 500 in different ways. 14:05
9 Q. Wyman is suggesting to connect the TSVs to 14:05
10 different paths of the circuits Figure 5 -- in 14:05
11 Figure 5; isn't that correct? 14:05
12 MR. CHANDLER: Objection. Form. 14:05
13 THE WITNESS: It's different taps in this 14:05
14 particular example. If you read more broadly, Wyman 14:05
15 suggests that one would analyze the load necessary 14:05
16 for any particular wiring configuration and select 14:05
17 one or more taps to connect to. 14:05
18 BY MS. ZHONG: 14:05
19 Q. Okay. So is it a single Figure 5 driver 14:05
20 that's connected to all four, or is each one of the 14:05
21 tap is connected to a separate driver circuitry as 14:06
22 shown in Figure 5? 14:06
23 MR. CHANDLER: Objection. Form. And, 14:06
24 Annita, it's a little unclear if you are saying
25 "paths," p-a-t-h-s, or "taps," t-a-p-s. The two of 14:06

1 you have been using both of those words in your 14:06
2 questions and answers. 14:06
3 MS. ZHONG: Let me see. I'm talking about 14:06
4 t-a-p, t-a-p-s. 14:06
5 MR. CHANDLER: Okay.
6 DEPOSITION REPORTER: And, Mr. Wolfe, were 14:06
7 you saying p-a-p or t-a-p? 14:06
8 THE WITNESS: T-a-p, as in tap a keg of 14:06
9 beer. 14:06
10 MS. ZHONG: Yeah, I'm talking about t-a-p as
11 well, not p-a-p. 14:06
12 MR. CHANDLER: And I -- I was wondering if 14:06
13 anyone was saying paths, p-a-t-h-s. 14:07
14 MS. ZHONG: No. No. Sorry. 14:07
15 THE WITNESS: So to answer your question, 14:07
16 there is a complete range of embodiments that are 14:07
17 described in Wyman. And in particular, if you 14:07
18 combine Figure 5 with column 5, lines 26 through 33, 14:07
19 what it explains is that you could have one driver 14:07
20 with one tap, one driver with multiple taps, or 14:07
21 multiple drivers for one tap, and that those are all 14:07
22 being disclosed. 14:07
23 BY MS. ZHONG: 14:07
24 Q. Okay. But the circuit is the same. If the 14:07
25 circuit is through the driver 500, where's the four 14:07

1 drive circuits but with different taps; correct? 14:07

2 MR. CHANDLER: Objection. 14:07

3 BY MS. ZHONG: 14:07

4 Q. It is just that, for example, for the TSV 14:07

5 shown in Figure 8A, Wyman is suggesting that it's 14:08

6 connected to either tap T0 or tap T1; isn't that 14:08

7 correct? 14:08

8 MR. CHANDLER: Objection. 14:08

9 THE WITNESS: No. I disagree with both 14:08

10 parts of it. 14:08

11 BY MS. ZHONG: 14:08

12 Q. Okay. 14:08

13 A. One, the suggestions also include taps T2 14:08

14 and taps T3 for the particular example in Figure 8, 14:08

15 but also the taps that I identified previously 14:08

16 explains that Figure 5 can be embodied or 14:08

17 implemented in many different ways, including one 14:08

18 driver supporting multiple taps, one driver 14:08

19 supporting one tap, or multiple drivers supporting 14:08

20 each tap. So all of those are contemplated by 14:08

21 Wyman. 14:08

22 Q. Okay. But when the circuit -- what is a 14:08

23 driver that's being provided to, for example, 14:08

24 Figure 8A tap? Is it an entire 500, like the driver 14:09

25 portion shown in 500, or it's only a portion of that 14:09

1 circuit that's being provided? 14:09

2 A. Again, understanding that there are many 14:09

3 variations disclosed of circuit 500, the particular 14:09

4 examples indicate that you can use the taps 14:09

5 independently, or you can provide a separate copy of 14:09

6 circuit 500 for each thing that needs to be driven 14:09

7 after you analyze the current requirements. 14:09

8 And there are a number of examples given 14:09

9 where you can use just a portion of the total 14:09

10 current and you can disable other portions of 500, 14:09

11 or you can aggregate taps to get a larger current, 14:10

12 or you can supply portions of the current to 14:10

13 different wiring networks if they both need to see 14:10

14 the same signal. 14:10

15 Q. Okay. But the circuit size for the 500, 14:10

16 that is set; right? The silicon -- the space it 14:10

17 occupies on the silicon, that is the same regardless 14:10

18 of which path you happen to be using or which of the 14:10

19 multiple combination taps you will be using; right? 14:10

20 MR. CHANDLER: Objection to form. 14:10

21 BY MS. ZHONG: 14:10

22 Q. It is still going to take the entire space 14:10

23 for the 500, isn't it? 14:10

24 MR. CHANDLER: Objection. 14:10

25 THE WITNESS: Yes. But there's also the 14:10

1 teaching in Wyman that you can make 500 at various 14:10
2 different sizes based on how you want to balance out 14:11
3 the currents and how your analysis indicates that 14:11
4 the currents are to be used. 14:11
5 So the teaching of Wyman teaches you how to 14:11
6 make 500 in many different sizes based on what any 14:11
7 particular net uses. 14:11
8 BY MS. ZHONG: 14:11
9 Q. So how is that different than, say, I make 14:11
10 many different driver circuits for different loads? 14:11
11 A. It's a minor improvement. What this says 14:11
12 essentially is that you can change the capability 14:11
13 over time. So, for example, one could connect taps 14:11
14 T2 and T3 together, and then enable T2 or T3 or both 14:11
15 if somehow you had different current requirements at 14:11
16 different times. 14:12
17 Also, this is not limited to a hardwired 14:12
18 system. It is contemplated that you could change 14:12
19 from one tap to another in a reasonably easy way. 14:12
20 And also, there is kind of -- there's a 14:12
21 teaching here that perhaps you may want to just 14:12
22 build this circuit at an estimated size and then 14:12
23 make a decision later as to which tap to use after 14:12
24 you have done some more analysis. So all those 14:12
25 teachings are present. 14:12

1 Q. Okay. But in order to do that, you have to 14:12
2 have all the -- all the possible combinations there; 14:12
3 right? 14:12

4 So, for example, if you want to accommodate 14:12
5 a range of the load -- a range of possible loads, 14:12
6 then you need to have all four of the drivers in 500 14:13
7 there. You can't just build three of them and hope 14:13
8 that somehow you will be able to accommodate a load 14:13
9 that requires four taps; correct? 14:13

10 MR. CHANDLER: Objection. Form. 14:13

11 THE WITNESS: That is correct for a 14:13
12 particular wire. But there is a clear teaching that 14:13
13 you can make a determination for one wire that you 14:13
14 might require two taps, like Figure 3, and for 14:13
15 another wire, you might require a three-buffer 14:13
16 system like Figure 4, and for another wire, you 14:13
17 might require a system like Figure 5, and even 14:13
18 within each of those, you can make them in different 14:13
19 sizes. 14:13

20 So for different wires, there's a teaching 14:13
21 that you can have different sized drivers within. 14:13
22 There is also a teaching as to how to determine what 14:13
23 to choose, and certainly to the extent that the 14:14
24 claim only requires that you have a different 14:14
25 current capability, that's disclosed even within an 14:14

1 already implemented version of 500. 14:14

2 So all those things are taught. Again, as 14:14

3 you mentioned, everywhere in the prior art, it was 14:14

4 known to be able to select the proper size driver 14:14

5 for a particular current load. That part in itself 14:14

6 was not new. 14:14

7 BY MS. ZHONG: 14:14

8 Q. Okay. So if you have two driver circuits as 14:14

9 shown in Figure 5, one uses only taps 0 through 2, 14:14

10 and the other uses all four of the drivers, do they 14:14

11 take up the same or different silicon space? 14:14

12 MR. CHANDLER: Objection. Form. 14:15

13 THE WITNESS: If you were to make up that -- 14:15

14 make that choice, they would use the same silicon 14:15

15 space. But, of course, if you used any commonsense 14:15

16 and you were only -- and you knew you were only 14:15

17 going to use T0, T1 and T2, you could instead 14:15

18 implement Figure 4, which would use less silicon 14:15

19 space. 14:15

20 BY MS. ZHONG: 14:15

21 Q. Okay. But if you implement, say, Figure 5, 14:15

22 even if you use only a subset of the drivers shown 14:15

23 here, would the size of the driver portion 500 14:15

24 differ or they would remain the same? 14:15

25 MR. CHANDLER: Objection. Form. 14:15

1 THE WITNESS: The physical size doesn't 14:15
2 depend on how many taps you use. But as I 14:15
3 mentioned, there are many teachings about how many 14:15
4 taps you implement and the size of the individual 14:16
5 taps. 14:16
6 BY MS. ZHONG: 14:16
7 Q. Okay. That's what I'm trying to understand. 14:16
8 So once you have implemented the circuit 14:16
9 shown on 500, the size of the driver doesn't really 14:16
10 change based on the number of taps you use; is that 14:16
11 correct? 14:16
12 MR. CHANDLER: Objection. Form. 14:16
13 THE WITNESS: I think that's correct. But, 14:16
14 again, you -- because you've already established the 14:16
15 size. It's because you've already chosen a size. I 14:16
16 think that that would be true of any circuit is, 14:16
17 after you decide what size it should be and build 14:16
18 it, then the size just doesn't change. But the size 14:16
19 has still been calculated based on the load. 14:16
20 BY MS. ZHONG: 14:16
21 Q. Okay. I understand where you're coming 14:16
22 from. I just want to confirm that once you have 14:16
23 built a four-driver circuit as shown in Figure 5, 14:17
24 the size of the driver circuit doesn't really change 14:17
25 based on whether you choose one of the drivers, two 14:17

1 of the drivers, or all the drivers were used; is 14:17
2 that correct? 14:17
3 MR. CHANDLER: Objection. Form. 14:17
4 THE WITNESS: Once you implement it in 14:17
5 silicon, the size of the driver has already been 14:17
6 selected and will not change. 14:17
7 BY MS. ZHONG: 14:17
8 Q. Okay. 14:17
9 A. But the current output could change. 14:17
10 Q. Understood. So if you -- 14:17
11 DEPOSITION REPORTER: Clarification. Did
12 you say "could change" or "would change"? 14:17
13 THE WITNESS: Could change. 14:17
14 BY MS. ZHONG: 14:17
15 Q. So if you want to change the size of the 14:17
16 driver, you cannot do so by programming the driver 14:17
17 circuitry by selecting a subset of the active 14:18
18 transistors that were used; is that right? 14:18
19 A. There is a little bit of a judgment call 14:18
20 there in terms of semantics. Right. So there 14:18
21 definitely are programmable drivers. They were 14:18
22 known well before this. 14:18
23 Q. Okay. 14:18
24 A. The size of the driver being used changes, 14:18
25 as it does in Figure 5. 14:18

1 Q. Okay. Uh-huh. 14:18

2 A. But not the size that the total circuit 14:18

3 takes up on the silicon. Right. So it's very 14:18

4 common to use not only this design, but also to use 14:18

5 designs where you had multiple transistors in 14:18

6 parallel. And then if you went from using four 14:18

7 transistors, eight transistors, it would be very 14:18

8 common there to say that the size of the driver had 14:18

9 changed because -- 14:18

10 Q. Okay. 14:18

11 A. -- the amount of silicon that's driving has 14:18

12 changed, but the physical space at the eight 14:19

13 transistors, or in this case, these would be four 14:19

14 transistors each, so the sixteen transistors take up 14:19

15 doesn't change. 14:19

16 So the physical space of the entire circuit 14:19

17 doesn't change after you've built it, but the 14:19

18 portion of it that is being used as a driver can 14:19

19 change. 14:19

20 Q. Okay. So the silicon space doesn't change, 14:19

21 but the portion that you use may change in the 14:19

22 programmable driver; is that right? 14:19

23 MR. CHANDLER: Objection. Form. 14:19

24 THE WITNESS: The silicon used by all the 14:19

25 transistors doesn't change after it's been built, 14:19

1 but the portion of that silicon that's being used as 14:19
2 a driver can, in some cases, be programmed during 14:19
3 use. And that is true both in the previous 14:19
4 technologies and in the Wyman technology. 14:20
5 BY MS. ZHONG: 14:20
6 Q. Okay. So in order to reduce the silicon 14:20
7 space, basically, you do have to make sure to know 14:20
8 like what would be the maximum load you can expect 14:20
9 to drive and choose the appropriate size; is that 14:20
10 right? 14:20
11 MR. CHANDLER: Objection. Form. 14:20
12 THE WITNESS: If you want to optimize the 14:20
13 silicon space that's used, you would need to -- in 14:20
14 the simplest cases, you would need to know the load 14:20
15 at the time that you chose the transistors. 14:20
16 There are very -- there are more complicated 14:20
17 designs where you could have a whole bunch of 14:20
18 transistors and you could allocate them at runtime 14:20
19 into a group of drivers, but that's a little bit 14:20
20 fancier than what's disclosed here. 14:21
21 BY MS. ZHONG: 14:21
22 Q. So the advantage of Weiman's approach than 14:21
23 the traditional approach is that it offers a little 14:21
24 bit more design tolerance; is that right? 14:21
25 MR. CHANDLER: Objection. Form. 14:21

1 THE WITNESS: It's not clear to me that 14:21
2 there is an advantage of Wyman over the traditional 14:21
3 approaches. 14:21
4 BY MS. ZHONG: 14:21
5 Q. Okay. 14:21
6 A. It's slightly different, but I don't know 14:21
7 that it's better. Also, if you look at Figures 10, 14:21
8 11 and 12 of Wyman, those basically are the 14:21
9 traditional approach. 14:22
10 Q. So how does Wyman differ from the 14:22
11 traditional approach then? 14:22
12 A. In Figures 3, 4 and 5, he uses this serial 14:22
13 architecture as opposed to the parallel architecture 14:22
14 that's shown in Figures 10, 11 and 12. 14:22
15 Q. Okay. 14:22
16 A. They both work. Again, I didn't rely on 14:22
17 Wyman as being a substantial improvement over the 14:22
18 prior art, simply as something that teaches how to 14:22
19 size buffers. 14:22
20 Q. Does relying on Wyman teach you about the 14:22
21 correlation between the load size and the driver 14:23
22 size; is that right? 14:23
23 A. Yes, and how to take that into account -- 14:23
24 Q. [Indiscernible - simultaneous talking.]
25 A. -- it is required by the claim. I also 14:23

1 relied on Wyman to show that multiple drivers can be 14:23
2 used for a single output. 14:23
3 Q. When you say "multiple drivers can be used," 14:23
4 what do you mean? 14:23
5 A. You can connect two or more drivers to drive 14:23
6 a single TSV. 14:23
7 Q. But 500 is a single driver circuit. 14:23
8 A. It's a single driver circuit, but it's 14:23
9 comprised of multiple drivers, and Wyman clearly 14:24
10 says that taps can be combined. It also says that 14:24
11 any one tap can have multiple drivers, and that's 14:24
12 shown in Figures 10, Figures 11 and Figures 12. 14:24
13 Q. And to which claim limitation is that 14:24
14 relevant? 14:24
15 A. I think probably none of them, but -- you 14:24
16 did not make the '160 patent an exhibit, but I have 14:24
17 it here. 14:24
18 So Claim 1 of the '160 patent says a first 14:25
19 data conduit including first driver, each having a 14:25
20 first driver size. 14:25
21 In the overall context of the claims, it's 14:25
22 not clear to me that that really needs -- was 14:25
23 intended to be plural, but to the extent that it was 14:25
24 intended to be plural, that's disclosed by Wyman. 14:25
25 Q. So you are saying that someone can use, say, 14:25

1 circuit 500 with multiple drivers in connection with 14:25
2 driving the TSV? 14:26
3 A. Yes. And it says that right in Wyman. 14:26
4 Q. Okay. Are you aware of any designs in which 14:26
5 the driver size are the same regardless of the mode? 14:26
6 MR. CHANDLER: Objection. Form. 14:27
7 THE WITNESS: Overall, there are designs 14:27
8 like that, but they're not very good designs. 14:27
9 BY MS. ZHONG: 14:27
10 Q. When would people use such design? 14:27
11 MR. CHANDLER: Objection. Objection to 14:27
12 form. 14:27
13 THE WITNESS: They would use it when they 14:27
14 don't have the technology to choose the driver size, 14:27
15 or when they don't have the technology to control 14:27
16 the loads, or if they're doing something that's so 14:27
17 quick and dirty that they just don't care how well 14:27
18 it operates as long as it does something. 14:27
19 BY MS. ZHONG: 14:27
20 Q. Would you use driver size of different sizes 14:27
21 if the loads are about the same? 14:28
22 MR. CHANDLER: Objection. Form. 14:28
23 THE WITNESS: It depends what you mean 14:28
24 "about the same." 14:28
25 If you have the ability to adjust for any 14:28

1 variation in the loads, such as might happen from 14:28
2 manufacturing variations, if you have the ability to 14:28
3 do that, it would certainly be a good idea to try. 14:28
4 BY MS. ZHONG: 14:28
5 Q. So if the loads on each of the TSVs are die 14:28
6 interconnects, are the designs the same but due to 14:28
7 manufacturing variances there are differences, would 14:28
8 you design a drive circuit with different driver 14:28
9 sizes or the same driver size? 14:29
10 A. To the extent that you can predict the 14:29
11 variations, you would -- you would make those 14:29
12 changes at design time. Otherwise, you would make 14:29
13 the adjustments at runtime probably in the way that 14:29
14 I described before, where you modify the effective 14:29
15 size of the driver by changing the number of 14:29
16 transistors that participate. 14:29
17 Q. Is it easy to predict what would be the 14:29
18 variances on loads on TSVs at design stage? 14:29
19 A. Sometimes it is, and sometimes it is not. 14:29
20 Q. And when is it easy to do that? 14:29
21 A. When you have models of manufacturing 14:29
22 variance or whether -- when there are geometric 14:29
23 differences, those kinds of situations. 14:29
24 Q. When they are symmetric, is it easy -- 14:30
25 A. When they are symmetric, then you would 14:30

1 probably try to determine whether or not your 14:30
2 manufacturing capabilities are also symmetric. 14:30
3 Often they're not. 14:30
4 Q. Yes. Okay. 14:30
5 A. But if you were predicting that everything 14:30
6 would end up perfect and then it didn't, then you 14:30
7 would need some way to make a post manufacturing 14:30
8 adjustment. 14:30
9 Q. In those situations, doesn't it make sense 14:30
10 to incur the additional cost to size the drivers 14:30
11 differently? 14:30
12 A. I'm sorry. I don't understand the question. 14:30
13 I proposed a situation where you're -- predicted 14:30
14 that the loads would be identical, so I don't know 14:30
15 what would size the drivers differently in advance. 14:31
16 But if, as is normal, you had a 14:31
17 manufacturing process that induced variations, then 14:31
18 you would adjust the driver size and current 14:31
19 capability after you characterized the manufactured 14:31
20 chip. 14:31
21 Q. So you basically have to have programmable 14:31
22 drivers then in that case? 14:31
23 A. It depends on what you mean by 14:31
24 "programmable." You would have to have an 14:31
25 adjustable one. But sometimes those adjustments 14:31

1 are made with lasers or other post-manufacturing 14:31
2 techniques. 14:31
3 Q. Do you need to have those adjustments or 14:31
4 can you just go with the design's driver size? 14:32
5 A. It depends what level of quality you're 14:32
6 trying to achieve. 14:32
7 Q. The normal DRAM mass manufacturing quality? 14:32
8 DEPOSITION REPORTER: I'm sorry, Miss Zhong,
9 the normal...
10 MR. CHANDLER: Objection. Form.
11 MS. ZHONG: DRAM mass production quality. 14:32
12 MR. CHANDLER: Same objection. 14:32
13 THE WITNESS: Historically, there's always 14:32
14 been at least some of the DRAM that are at the 14:32
15 leading edge of speed capabilities, and those are 14:32
16 the most valuable. So certainly, there would be 14:32
17 motivations to adjust driver sizes. That 14:32
18 accomplishes a number of things, and not only does 14:32
19 it optimize speed and power, but it also minimizes 14:32
20 the amount of electromagnetic interference 14:33
21 emissions, which are a big deal to computer system 14:33
22 manufacturers. 14:33
23 BY MS. ZHONG: 14:33
24 Q. Are you talking of the drivers on the DRAM 14:33
25 dies themselves or on the interface die? 14:33

1	A. Either/or both.	14:33
2	Q. Have you designed -- have you been involved	14:33
3	in the design of adjusting the drivers in such	14:33
4	situations?	14:33
5	A. Yes. Definitely for memory controllers, I	14:33
6	have.	14:34
7	Q. So that's for memory controllers. I'm	14:34
8	talking about memory themselves.	14:34
9	A. Well, they are connected to the same wires	14:34
10	so they're adjusted for the same reasons. For the	14:34
11	memories themselves, no, I have not designed	14:34
12	commercial memory chips myself --	14:34
13	Q. Okay.	
14	A. -- I have seen them designed, but I haven't	14:34
15	designed them myself.	14:34
16	Q. So if you already made an adjustment on the	14:34
17	memory controller side, why do you need to make	14:34
18	further adjustment on the memory device's side?	14:34
19	A. Because they each control the communications	14:34
20	in one direction. Ideally, you would want them to	14:34
21	be both controlled and both matched.	14:34
22	Q. So the memory controller controls the write	14:34
23	direction and the memory device controls the read	14:35
24	direction?	14:35
25	A. From the perspective of controlling the	14:35

1 characteristics of the signals that are communicated 14:35
2 in that direction. Obviously, the memory controller 14:35
3 is overall in control, but each individual chip has 14:35
4 control over the characteristics of the signal that 14:35
5 it drives onto the memory communication bus. 14:35
6 MS. ZHONG: Can we take a 10-minute break? 14:36
7 MR. CHANDLER: Sure. 14:36
8 DEPOSITION REPORTER: We are off the record. 14:36
9 (Off the record.) 14:36
10 BY MS. ZHONG: 14:58
11 Q. Dr. Wolfe, do you mind pulling up 14:58
12 Exhibit 1016, Riho again. 14:58
13 A. 1016? 14:58
14 Q. Yes. 1016, Riho. 14:58
15 A. Okay. 14:58
16 Q. Okay. Figure 5, please. 14:58
17 A. Yes. 14:58
18 Q. So you described the switch circuits sa and 14:58
19 sb as comprising transmission gates; correct? 14:58
20 A. Yes. You can see those in Figure 6C, for 14:59
21 example. 14:59
22 Q. Okay. What are "transmission gates"? Are 14:59
23 they made up of transistors? 14:59
24 A. Yes. In this particular technology, as I 14:59
25 mentioned, you can see one in Figure 6C, and it's 14:59

1	comprised of a PMOS transistor and an NMOS	14:59
2	transistor connected drain to source with each	14:59
3	other, and the appropriate control circuits to	14:59
4	control their gates.	14:59

5	Q. And I think we discussed earlier that	14:59
6	transmission gates will be sized according to the	15:00
7	desired current of the associated driver circuit; is	15:00
8	that right?	15:00

9 MR. CHANDLER: Object to form. 15:00

10	THE WITNESS: They would be appropriately	15:00
11	sized to support the necessary currents. Oftentimes	15:00
12	that is simply the minimum size.	15:00

13	BY MS. ZHONG:	15:00
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14	Q. Okay. So if the driver circuit to the	15:00
15	right of the transmission gate you need, say,	15:00
16	10 transistors in order to drive the appropriate	15:00
17	current or the desired current, don't you also need,	15:00
18	say, 10 transistors in the transmission gate in	15:00
19	order to drive that current onto the TSV?	15:01

20 MR. CHANDLER: Objection to form. 15:01

21	THE WITNESS: Not necessarily. The number	15:01
22	of transistors may be irrelevant.	15:01

23	BY MS. ZHONG:	15:01
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24	Q. Okay. But they will have similar size as a	15:01
25	driver size in the L1C2R2 circuit; right?	15:01

1 MR. CHANDLER: Object to form. 15:01

2 THE WITNESS: Not necessarily. They are 15:01

3 connected in different ways, so you would have to do 15:01

4 an analysis in each case. 15:01

5 BY MS. ZHONG: 15:01

6 Q. What do you mean by "they are connected in 15:01

7 different ways"? 15:01

8 A. The circuit topology is different so, 15:01

9 therefore, you would -- you would have to separately 15:01

10 analyze them. 15:01

11 Q. So is it your testimony that the driver 15:02

12 transistors would operate differently than the 15:02

13 transmission gates --

14 (Clarification requested by Reporter.)

15 BY MS. ZHONG:

16 Q. So is it your opinion that the transistors

17 in the driver circuit would operate differently than 15:02

18 the transistors in the transmission gates? 15:02

19 MR. CHANDLER: Objection. Form. 15:02

20 THE WITNESS: There would be some 15:02

21 differences because they are connected differently 15:02

22 and controlled differently. 15:02

23 BY MS. ZHONG: 15:02

24 Q. Okay. Would the size of the transmission 15:02

25 gates -- let me withdraw it. 15:02

1	Would the size of the transistors in the	15:02
2	transmission gates -- let me withdraw and ask it	15:02
3	this way.	15:03
4	Would the total size of the transistors in	15:03
5	the transmission gates be in order of magnitude	15:03
6	smaller than the transistors in the driver circuit?	15:03
7	MR. CHANDLER: Objection to form.	15:03
8	THE WITNESS: They can be under some	15:03
9	circumstances.	15:03
10	BY MS. ZHONG:	15:03
11	Q. Under what circumstances?	15:03
12	A. Depending how you are trying to operate	15:03
13	them. The primary difference is that the driver	15:03
14	transistors are being turned on and off and need to	15:03
15	drive currents as quickly as possible, where the	15:03
16	transmission gates in a system, like the one in	15:03
17	Figure 6, A, B and C of Riho, the transmission gates	15:03
18	can be turned on well in advance, presumably at	15:04
19	power-up time.	15:04
20	So, therefore, they're in their maximum	15:04
21	transmission state of their minimum resistance at	15:04
22	all times, so they're going to have a different	15:04
23	in-circuit behavior. So you would do again a	15:04
24	routine but specific analysis to make that	15:04
25	determination.	15:04

1 Q. So what you are saying is at the charge-up 15:04
2 time, you can ignore the charge-up time in the 15:04
3 design of the transmission gates in Riho's 15:04
4 configuration? 15:04

5 A. In the configuration that's on Figure 6, you 15:04
6 can. Plus, again, because the transistors are 15:04
7 connected in a different topology, you would get 15:04
8 different results in terms of a -- of an analysis. 15:04
9 So you would have to actually perform those 15:04
10 calculations. 15:04

11 Q. If you used small transistors, wouldn't the 15:05
12 resistance of the -- on the transistor goes up? 15:05

13 MR. CHANDLER: Objection to form. 15:05

14 THE WITNESS: I don't know what you mean by 15:05
15 "goes up." A small transistor will have a higher 15:05
16 resistance than a large transistor. 15:05

17 BY MS. ZHONG: 15:05

18 Q. Okay. And if the transmission gates use a 15:05
19 small transistor which has a high resistance, would 15:05
20 that cause -- would that translate to more power in 15:05
21 order to drive the data signals across the TSV? 15:05

22 MR. CHANDLER: Objection. Form. 15:05

23 THE WITNESS: I want to make sure I 15:05
24 understood your question. Was the question whether 15:06
25 a small transistor with a large resistance would 15:06

1 require more power? 15:06

2 BY MS. ZHONG: 15:06

3 Q. So like if you -- in the transmission gate, 15:06

4 if you use a small transistor, would you say like 15:06

5 the resistance would go up? How would that affect 15:06

6 the operation? 15:06

7 A. It would reduce the maximum current but, 15:06

8 again, depending on the resistance of other portions 15:06

9 of the system and the capacitance of other portions 15:06

10 of the system, that may or may not be significant. 15:06

11 It is also important to understand that both 15:06

12 Figure 6A and Figure 6B include an input circuit as 15:06

13 well. The capacitance of the input circuit is 15:07

14 usually substantially more than the capacitance of 15:07

15 the output circuit, and that's part of what's being 15:07

16 isolated. 15:07

17 Q. When you say "the input circuit," which one 15:07

18 are you referring to? 15:07

19 A. The one that has the words "input circuit" 15:07

20 on it. 15:07

21 Q. Let me see that I can understand you. 15:07

22 So if the driver circuit has to go through a 15:09

23 transmission gate with a small transistor, does that 15:09

24 mean that you have to -- I mean, would it be -- the 15:09

25 transmission gate with its high capacitance then 15:10

1 affect the speed, slow down the speed at which the 15:10
2 data signals are transferred? 15:10
3 MR. CHANDLER: Objection. Form. 15:10
4 THE WITNESS: I don't understand why a 15:10
5 transmission gate with small transistors would have 15:10
6 higher capacitance. 15:10
7 BY MS. ZHONG: 15:10
8 Q. Sorry. I mean, small transistors with high 15:10
9 resistance and when the current goes through it, 15:10
10 wouldn't that affect the speed at which the data 15:10
11 signals are transferred? 15:10
12 MR. CHANDLER: Objection. Form. 15:10
13 THE WITNESS: It would. But you would have 15:10
14 to look at all the resistances to see whether or not 15:10
15 that difference is meaningful. It could be a 15:10
16 thousandth of a percent. 15:11
17 BY MS. ZHONG: 15:11
18 Q. Can you just remind me, why do you think 15:11
19 that the transmission gate would be at its maximum 15:11
20 charge when the driving circuits begin to operate? 15:11
21 A. Because in the Figure 6 embodiment, the 15:12
22 signals ROM1 and ROM2 are permanent. They are 15:12
23 unchanging. They turn on when the power turns on. 15:12
24 Q. But when a CS0 or CS1, that would change, 15:12
25 wouldn't it? 15:12

1 A. In the Figure 6 embodiment, those don't 15:12
2 control the transmission gates. And even in the -- 15:12
3 and even in the embodiments -- go ahead. 15:12
4 Q. ROM1 -- but if you look at Figure 5, those 15:12
5 CS1 and CS0 are the two outputs from ROM1 that go 15:12
6 into the transmission gates. 15:13
7 A. Yes. And they do not change in operation in 15:13
8 that embodiment. 15:13
9 Q. Do they change the operation in Figure 8? 15:13
10 A. No. But there is another control signal in 15:13
11 Figure 8. But even so, that control signal switches 15:13
12 well in advance of the data transmission so it would 15:13
13 not be the speed-limiting portion of the circuit. 15:13
14 Q. So if it's not in this configuration, but 15:13
15 you have to switch those things instantaneously, 15:14
16 would it be better to use a large transistor or 15:14
17 smaller transistors in order to charge up to the 15:14
18 voltage needed for the transmission? 15:14
19 A. It would be better not to build it that way 15:14
20 and to build it the way that Riho tells you to build 15:14
21 it. 15:14
22 Q. Can you just answer my question. 15:14
23 MR. CHANDLER: Objection. Form. 15:15
24 THE WITNESS: I'm trying to understand your 15:15
25 hypothetical. 15:15

1 So if -- you're saying if the transmission 15:15
2 gates were turned on at the exact time that data 15:15
3 needs to be input or output to the die? 15:15
4 BY MS. ZHONG: 15:15
5 Q. I'm saying like if they are not, as you say, 15:15
6 switched on or off well in advance of when data 15:15
7 transmission occurs, in that situation, would you -- 15:15
8 would a POSITA use a larger transistor size or a 15:15
9 smaller transistor size in order for it -- for the 15:15
10 transmission gates to reach the voltage needed for 15:15
11 operation? 15:16
12 MS. ZHONG: Objection. Form. 15:16
13 THE WITNESS: It would depend on exactly 15:16
14 when they're turned on and it would depend on the 15:16
15 design tradeoff that one would make between load 15:16
16 reduction and speed. 15:16
17 BY MS. ZHONG: 15:16
18 Q. So in general, does a large transistor 15:16
19 charge up more quickly or a smaller transistor would 15:16
20 charge up more quickly? 15:16
21 A. These transistors aren't charging up in the 15:16
22 way that a logic gate does. They are what we call 15:16
23 "pass transistors." They are charged by their own 15:16
24 control circuit. Normally, a small transistor can 15:16
25 turn on faster. 15:16

1 Q. Now, in Riho's Figure 5 and 6 configuration, 15:19
2 how would a POSITA design the transmission gates? 15:19
3 MR. CHANDLER: Objection. Form. 15:20
4 BY MS. ZHONG: 15:20
5 Q. Would they design the transmission gates to 15:20
6 operate significantly differently than the 15:20
7 transistors -- let me withdraw and ask. 15:20
8 How would a POSITA design the transmission 15:20
9 gates in Riho's Figure 5 and 6? In particular, 15:20
10 would they design the transistors to be sized 15:20
11 completely differently than the transistors in the 15:20
12 L1C2R2 circuit? 15:20
13 MR. CHANDLER: Objection. Form. 15:20
14 THE WITNESS: They would design them just 15:20
15 like is shown in Figure 6C. The transistor sizing 15:20
16 would be based on a routine analysis. But I would 15:20
17 expect that they would often be minimum sized, 15:20
18 because remember, the goal in Riho is to minimize 15:21
19 the capacitance of the TSVs so they want to isolate 15:21
20 the input buffer which is highly capacitive, and 15:21
21 they also want to isolate the output buffer. So 15:21
22 they would use the minimum acceptable size. 15:21
23 And, again, you would have to do the actual 15:21
24 analysis at various voltages and speeds, but I would 15:21
25 not at all be surprised if a minimum size transistor 15:21

1 was sufficient. 15:21

2 BY MS. ZHONG: 15:21

3 Q. How would the size of a minimum size 15:21

4 transistor in the transmission gate compare to the 15:21

5 size of the transistors in the drive circuit? 15:21

6 MR. CHANDLER: Objection. Form. 15:22

7 THE WITNESS: Again, that would be a design 15:22

8 choice. It would typically be smaller. But what's 15:22

9 most important is that it's not just the drive 15:22

10 circuit, it's the drive circuit and the receiver 15:22

11 circuit because these are all bidirectional vias. 15:22

12 And the gates in the receiving circuit represent the 15:22

13 bulk of the capacitance. 15:22

14 BY MS. ZHONG: 15:22

15 Q. So how would the size of a minimum-sized 15:23

16 transistor in the transmission gate compare to the 15:23

17 size of the transistors in the R1 -- in the L1R1C1 15:23

18 circuitry, which would include both a receiver and 15:23

19 a driver circuitry? 15:23

20 A. Well, one, it would be a design choice. 15:23

21 They would typically be much smaller for all the 15:24

22 reasons that I've already explained. The 15:24

23 transmission gate transistors would typically be 15:24

24 smaller. 15:24

25 Also, the question for a designer would not 15:24

1 really be the size as much as it would be the 15:24
2 capacitance. And as I mentioned before, the gate to 15:24
3 the receiver contributes far more to the capacitance 15:24
4 than the output of the driver. 15:24
5 Q. Is it the case a smaller -- doesn't the 15:24
6 capacitance of the transmission gate decrease with 15:24
7 the increasing size of the transistor? 15:24
8 MR. CHANDLER: Objection. Form. 15:24
9 BY MS. ZHONG: 15:24
10 Q. Sorry -- 15:24
11 A. A smaller transistor [indiscernible - 15:24
12 simultaneous talking] capacitance.
13 Q. What I'm saying is doesn't the capacitance 15:24
14 for the transmission gate decrease with the 15:24
15 increasing size of the transistor? 15:25
16 MR. CHANDLER: Objection to form. 15:25
17 THE WITNESS: A transmission gate with small 15:25
18 transistors will have less capacitance than a 15:25
19 transmission gate with large transistors. 15:25
20 BY MS. ZHONG: 15:25
21 Q. But a small transmission gate will have a 15:25
22 higher resistance? 15:25
23 MR. CHANDLER: Objection to form. 15:25
24 THE WITNESS: As compared to a large 15:25
25 transmission gate? 15:25

1 BY MS. ZHONG: 15:25

2 Q. Yes. 15:25

3 A. It will have a higher resistance, but it's 15:25

4 unlikely to make any difference. 15:25

5 Q. Why is that? Because of the other 15:25

6 resistance in the system? 15:25

7 A. Because of the other resistances in the TSV 15:25

8 and because during the point at which the resistance 15:26

9 is meaningful, it's been turned on a hundred 15:26

10 percent, which is its lowest -- excuse me -- which 15:26

11 is its lowest point of resistance so it's quite low. 15:26

12 And also because Riho represents that 15:26

13 there's a tradeoff between reduced loading and 15:26

14 performance and he is encouraging reduced loading. 15:26

15 Q. And when people talk about "load," are they 15:26

16 referring to capacitive load? 15:26

17 A. In this context, generally. When you're 15:26

18 talking about CMOS integrated circuits and you talk 15:27

19 about load, while there are technically resistive 15:27

20 inductive and capacitance components, the 15:27

21 capacitance is very dominant, so people typically 15:27

22 talk about capacitive loads. And we saw that in 15:27

23 the -- in the examined patents as well. They focus 15:27

24 on the capacitive load. 15:27

25 MS. ZHONG: Can we take a break? 15:29

1	MR. CHANDLER: Okay.	15:29
2	(Off the record.)	15:29
3	BY MS. ZHONG:	15:50
4	Q. Can we please go back to Riho, 1060,	15:50
5	Figure 5.	15:50
6	A. 1060?	15:50
7	Q. Yeah. 1060, Figure 5.	15:50
8	A. Okay.	15:50
9	Q. Can we go through what would be happening	15:50
10	during a write operation onto SDRAM D15 die through	15:50
11	TSV 715. Okay.	15:51
12	So assume that the LSI logic chip at the	15:51
13	bottom is driving a bit 1 up the TSV 715 to be	15:51
14	written into the memory die.	15:51
15	Are you with me?	15:51
16	A. Yes.	15:51
17	Q. Okay. And in that case, when you're trying	15:51
18	to write bit 1 into the memory die, is what happens	15:51
19	is you're trying to push current through the	15:51
20	transmission gate in sa onto a receiver circuit in	15:51
21	D15?	15:52
22	MR. CHANDLER: Objection. Form.	15:52
23	THE WITNESS: So remember that there are	15:52
24	hundreds of TSVs that are participating in a write	15:52
25	operation and --	15:52

1 BY MS. ZHONG:

2 Q. Yeah. 15:52

3 A. -- [indiscernible - simultaneous talking] -- 15:52

4 in the embodiment of Riho. And Riho also describes 15:52

5 a variety of protocols at this point in the circuit, 15:52

6 SDRAM, SRAM and nonvolatile RAM. 15:52

7 But it would go through that normal 15:52

8 protocol, just as if this had not been in TSVs, just 15:52

9 as if -- 15:52

10 Q. Okay.

11 A. -- the circuit chips were laid out on a 15:52

12 board. The logic LSI chip, at the proper point in 15:52

13 time, would drive a data value, a 0 or a 1, into 15:52

14 TSV 715, that current would change the voltage in 15:53

15 the entire net from a 0 to a 1, and because switch 15:53

16 sa is on, that net would include the input receiver 15:53

17 that is on D15 that corresponds to this particular 15:53

18 bit, and that, again, for most memory plates would 15:53

19 then buffer that signal and drive it into some type 15:53

20 of a register or flip-flop. 15:53

21 Q. Okay. And in that process, basically, 15:53

22 power is needed to push the current through the 15:53

23 transmission gate into the receiver circuit for this 15:53

24 receiver circuit to be charged up to register that 15:53

25 bit -- the bit 1; is that correct? 15:54

1 MR. CHANDLER: Object to form. 15:54

2 THE WITNESS: The current is used to 15:54

3 overcome all of the capacitance, the output 15:54

4 capacitance of the driver, the interconnect 15:54

5 capacitance, and the capacitance in the receiver 15:54

6 circuit. The portion of the current that's used to 15:54

7 charge the receiver circuit would pass through the 15:54

8 transmission gate sa. 15:54

9 BY MS. ZHONG: 15:54

10 Q. So in that write operation, the receiver 15:54

11 circuit would be charged up as part of the process? 15:54

12 A. If it was switching from a 0 to a 1, it 15:54

13 would be charged up. If it was switching from a 1 15:54

14 to a 0, it would be discharged. 15:54

15 Q. Okay. And that circuit, the receiver 15:54

16 circuit was not -- there is a charge and discharge 15:54

17 part during that transmission; is that correct? 15:55

18 MR. CHANDLER: Object to form. 15:55

19 BY MS. ZHONG: 15:55

20 Q. In other words, it is not the transmission 15:55

21 gate that stays on; there is switching for that 15:55

22 receiver? 15:55

23 A. The output of the receiver would switch 15:55

24 based on the input. The input would change assuming 15:55

25 that the drive signal changes and -- 15:55

1 Q. Okay. 15:55

2 A. -- at some point, there would be a threshold 15:55

3 that's crossed and that would cause the output to 15:55

4 switch. 15:55

5 Q. Okay. And in order for that output to 15:55

6 switch, for that switching to occur, a charge 15:55

7 basically needs to be put on to the receiver 15:55

8 circuit. You either charge it or you discharge it. 15:55

9 Fair? 15:55

10 A. Yes. 15:55

11 MR. CHANDLER: Object to form. 15:55

12 THE WITNESS: That's the normal operation of 15:55

13 a MOS circuit. 15:55

14 BY MS. ZHONG: 15:56

15 Q. Okay. And charge is basically current over 15:56

16 time or -- 15:56

17 A. Current charge time -- 15:56

18 Q. -- [indiscernible - simultaneous talking]

19 Yeah.

20 A. -- it is times time. Current is charge -- 15:56

21 DEPOSITION REPORTER: Excuse me. I need one 15:56

22 at a time, please. 15:56

23 MS. ZHONG: Sorry. 15:56

24 BY MS. ZHONG:

25 Q. So current is charge per unit time; correct? 15:56

1	A. Correct.	15:56
2	Q. Okay. And you need a certain amount of	15:56
3	charge in order to charge up the receiver circuit	15:56
4	for it to switch from 0 to 1 and, conversely, you	15:56
5	need to discharge the amount of charge for it to	15:56
6	switch from 1 to 0; correct?	15:56
7	A. Correct.	15:56
8	Q. Okay. And for a given circuit, those	15:56
9	charge -- it will be a predetermined amount of	15:56
10	charge in order for that switching to occur. Agree?	15:56
11	MR. CHANDLER: Object to form.	15:57
12	THE WITNESS: It depends on what you mean by	15:57
13	"predetermined." It is impacted by variations in	15:57
14	supply voltage and temperature and other kinds of	15:57
15	things.	15:57
16	BY MS. ZHONG:	15:57
17	Q. Okay. For a given operating condition,	15:57
18	there will be -- a certain amount will be required	15:57
19	for you to charge up or to charge up the receiver	15:57
20	circuit; correct?	15:57
21	A. That's a model that we use. I mean, there	15:57
22	are statistical variations, but there's a -- there's	15:57
23	a typical amount or an average amount that one would	15:57
24	use to switch.	15:57
25	Q. Okay. So the larger the amount of charge,	15:57

1 the higher the current it needs to be if you want 15:57
2 the charge to occur within the given period of time; 15:57
3 correct? 15:57
4 MR. CHANDLER: Object to form. 15:57
5 THE WITNESS: Yes. When measured exactly at 15:57
6 the capacitance. In real circuits, you can't 15:57
7 necessarily increase the current. The current is 15:58
8 established by the circuit parameters and all you 15:58
9 can control is the voltage typically in a MOS 15:58
10 circuit. 15:58
11 BY MS. ZHONG: 15:58
12 Q. Okay. And so if you have a small 15:58
13 transistor, then less current can be passed through 15:58
14 it. Fair? 15:58
15 A. No. 15:58
16 Q. No? 15:58
17 A. There would be less maximum current without 15:58
18 damaging it, but if your circuit was designed so 15:58
19 that it needed 10 milliamps of current, it could 15:58
20 perform identically with a large transistor and a 15:58
21 small transistor because either one would be big 15:58
22 enough. 15:58
23 Q. So if the receiver circuit is made up, say, 15:59
24 of 10 transistors of a given size and the amount of 16:00
25 charge needed to charge up those transistors, let's 16:00

1 say, it's Q. 16:00

2 Do you have that? 16:00

3 A. Uh-huh. 16:00

4 Q. Okay. What would be the size of the 16:00

5 transmission transistor in order for you to charge 16:00

6 up the receiver circuit within the allowed -- like 16:01

7 within the permitted time for the operation to 16:01

8 occur? 16:01

9 MR. CHANDLER: Objection. Form. It's 16:01

10 unclear if you said "Q" like queen or the number "2" 16:01

11 that comes after number 1. 16:01

12 MS. ZHONG: "Q" as in queen. 16:01

13 THE WITNESS: I'm assuming you want to 16:01

14 charge the gates of these transistors? 16:01

15 BY MS. ZHONG: 16:01

16 Q. When you say "charge up the receiver 16:01

17 circuit," what do people mean by that? 16:01

18 A. It means charge the gates. 16:01

19 Q. Okay. 16:01

20 A. You would have to perform a full network 16:01

21 analysis of all of the capacitances, resistances, 16:02

22 and inductances, and you would need a transistor 16:02

23 model to figure that out. That's very routine. 16:02

24 Theoretically, it can be done by hand. 16:02

25 Nobody has done it by hand very often since the 16:02

1 1970s because we have software that does it for us, 16:02
2 once you make all those decisions. 16:02
3 Q. Okay. But the charge that's coming off the 16:02
4 TSV that's being pushed up, those would be the 16:03
5 charge that needs to be pushed onto or used to 16:03
6 charge up the receiver circuit; is that correct? 16:03
7 MR. CHANDLER: Objection. Form. 16:03
8 THE WITNESS: A portion of it will. Other 16:03
9 portions will charge C3, other portions will charge 16:03
10 the 16 copies of C1. And again, remember, these 16:03
11 don't physically exist. These are lumped 16:03
12 approximation models. 16:03
13 BY MS. ZHONG: 16:03
14 Q. When you say "C3," which circuit are you 16:03
15 referring to? Oh, the one down on the bottom? 16:03
16 A. Uh-huh. Yes. 16:03
17 Q. Okay. But the amount of charge that's 16:03
18 available to charge up the receiver circuit, that is 16:04
19 fixed; is that correct? 16:04
20 MR. CHANDLER: Objection to form. 16:04
21 THE WITNESS: No. It is constantly time 16:04
22 varying. 16:04
23 BY MS. ZHONG: 16:04
24 Q. For a given transaction, it's still varying? 16:04
25 A. I guess eventually it will hit some 16:04

1 asymptotic level, but at that point you don't care 16:04
2 anymore. It's a time varying curve. Again, that's 16:04
3 why we would need software to model it. 16:04
4 Q. Okay. So you want the receiver circuit to 16:04
5 be charged up as fast as possible; is that correct? 16:05
6 MR. CHANDLER: Objection. Form. 16:05
7 THE WITNESS: No, that's generally wrong. 16:05
8 BY MS. ZHONG: 16:05
9 Q. How would you like it to be charged up? 16:05
10 A. Fast enough to meet the specifications of 16:05
11 your product. Any faster and it probably uses more 16:05
12 power and generates more electromagnetic 16:05
13 interference, so you would pick a target speed and 16:05
14 you would try to match that. 16:05
15 And in fact, if you read Riho in its 16:05
16 entirety, you can see that in figures like Figure 6, 16:05
17 there are additional resistances that are added to 16:05
18 slow it down to try to match all the various signals 16:05
19 so that they all operate at the same speed rather 16:05
20 than as fast as possible. 16:05
21 Q. When you say they all operate at the same 16:05
22 speed, what is the "they" referring to? 16:06
23 A. So there is an attempt to try to make all of 16:06
24 the signals in the 384 or whatever TSVs -- let's see 16:06
25 if I have the actual number here. 382 TSVs. To try 16:06

1 and make them all operate at approximately the same 16:07
2 speed absent manufacturing variations. And then 16:07
3 there is a recognition that manufacturing variations 16:07
4 will happen. 16:07
5 But there is an attempt to compensate for 16:07
6 the fact that the capacitive load from the SDRAM 16:07
7 driver and receiver is at a different spot in the 16:07
8 overall TSV circuit network for different layers 16:07
9 and, therefore, since that could lead to some 16:07
10 variation in speed, there is a resistive adjustment 16:08
11 that's explained with respect to Figure 6 that is 16:08
12 used to compensate for those variations among 16:08
13 layers, again, with a goal of trying to minimize the 16:08
14 differences between the loads. 16:08
15 Q. And for you to charge up the receiver 16:08
16 circuit in Riho's DRAM dies, does it take more time 16:09
17 for that -- the charging up to occur if the current 16:09
18 through the transmission gate is lower? 16:09
19 MR. CHANDLER: Objection. Form. 16:09
20 THE WITNESS: Yes. But that depends on a 16:09
21 number of factors, only one of which is the size of 16:09
22 the transmission gate transistors and the difference 16:09
23 may be very minor. 16:09
24 BY MS. ZHONG:
25 Q. And when you say "that depends on a number 16:09

1 of factors," what factors are you referring to? 16:10

2 A. Among other things, the capacitances C1 and 16:10

3 C3, the resistances R1 and R3, and the resistance 16:10

4 R2. 16:10

5 Q. Why would those matter? 16:10

6 A. Because they're all in between the driver 16:10

7 and the receiver, and the circuit current is 16:10

8 determined by the operation as a whole. It's not 16:10

9 independently determined by each individual element. 16:10

10 Q. The C1R1 circuitry and the C3 and C2, those 16:10

11 values are independent of whether the -- are 16:10

12 independent of the size of the transmission gates; 16:11

13 right? 16:11

14 MR. CHANDLER: Objection. Form. 16:11

15 THE WITNESS: I'd have to look very 16:11

16 carefully. It's possible that the transmission gate 16:11

17 resistance and capacitance could be lumped into one 16:11

18 of those values, but it's probably not significantly 16:11

19 different. 16:11

20 BY MS. ZHONG: 16:11

21 Q. And when you say that a small transistor, 16:11

22 the resistance of it is not going to change 16:11

23 significantly -- let me withdraw and ask. 16:12

24 Do I understand it correctly when you say 16:12

25 that even for a small transistor, its resistance is 16:12

1 pretty low when it is fully on? 16:12

2 A. Yes. As compared to a larger transistor 16:12

3 when it is starting to turn on. 16:12

4 Q. What about as compared to a larger 16:12

5 transistor when it is fully on? 16:12

6 MR. CHANDLER: Objection. Form. 16:12

7 THE WITNESS: Normally after they're fully 16:12

8 on, a large transistor on the same technology would 16:12

9 have lower resistance than a small transistor. But 16:12

10 that may not affect the performance of the circuit 16:13

11 overall. 16:13

12 BY MS. ZHONG: 16:13

13 Q. I understand. Just do an orange-to-orange 16:13

14 comparison. 16:13

15 So if a large transistor is three times the 16:13

16 size of a small transistor, how would the resistance 16:13

17 change? 16:13

18 MR. CHANDLER: Objection. Form. 16:13

19 THE WITNESS: Approximately proportionately. 16:13

20 But again, that doesn't necessarily impact the way 16:13

21 it performs in a given circuit. 16:13

22 BY MS. ZHONG: 16:13

23 Q. Okay. So if you just look at the electrical 16:13

24 path, the SDRAM D15, the TSV 715 to say I receive a 16:13

25 circuit -- 16:14

1 (Clarification requested by Reporter.) 16:14

2 BY MS. ZHONG:

3 Q. In SDRAM D15, and the electrical path 16:14

4 between TSV 715 and the receiver circuit is only 16:14

5 intersected by the switch circuit sa; correct? 16:14

6 MR. CHANDLER: Objection. Form. 16:14

7 THE WITNESS: I'm sorry. I missed a word 16:14

8 there. It's only what? 16:14

9 BY MS. ZHONG: 16:14

10 Q. It's the only circuit element separating the 16:14

11 receiver circuit and the TSV is the transmission 16:14

12 gate; is that right? 16:14

13 MR. CHANDLER: Objection. Form. 16:14

14 THE WITNESS: I guess if you mean by 16:14

15 "separating" in between, that would be true, but 16:15

16 there are other circuit elements that impact the 16:15

17 behavior. So, for example, resistance R2, which 16:15

18 isn't a circuit element -- 16:15

19 BY MS. ZHONG:

20 Q. Uh-huh.

21 A. -- it's a model and would be present --

22 (Clarification requested by Reporter.) 16:15

23 THE WITNESS: It's not a circuit element. 16:15

24 It's a model and it would be present. 16:15

25 / / / 16:15

1 BY MS. ZHONG: 16:15

2 Q. Okay. So when you charge up the receiver 16:15

3 circuit in SDRAM D15 using the charge that is coming 16:15

4 off TSV 715, that charge goes through the 16:15

5 transmission gate and then maybe R2 to charge up the 16:15

6 transistors, the gates of the transistors of the 16:16

7 receiver circuit; is that right? 16:16

8 MR. CHANDLER: Objection. Form. 16:16

9 THE WITNESS: It does. But there are other 16:16

10 circuit elements that determine the magnitude of 16:16

11 that charge. 16:16

12 BY MS. ZHONG: 16:16

13 Q. When you say "the magnitude of the charge," 16:16

14 you mean the final charge that will be received by 16:16

15 the receiver circuit? 16:16

16 A. No. I mean the rate at which the charge 16:16

17 accumulates in the capacitance of the receiver 16:16

18 circuit. 16:16

19 Q. But the L1R2 and C2 are fixed for the SDRAM 16:16

20 D15 die; correct? 16:17

21 MR. CHANDLER: Objection. Form. 16:17

22 THE WITNESS: No. We talked about that 16:17

23 already. They are temperature variant and can be 16:17

24 voltage variant. 16:17

25 BY MS. ZHONG: 16:17

1 Q. But let's just say for a given operating 16:17
2 condition, they are fixed. 16:17
3 MR. CHANDLER: Object to form. 16:17
4 THE WITNESS: To a reasonable approximation, 16:17
5 they do vary over the -- they vary based on the age 16:17
6 of the component as well. 16:17
7 BY MS. ZHONG: 16:17
8 Q. Okay. 16:17
9 A. But for, you know, a reasonably short time 16:17
10 interval at the identical operating conditions, they 16:17
11 would be fixed. 16:17
12 Q. Okay. So the time that it takes for you to 16:17
13 charge up the receiver circuit, where is the charge 16:17
14 that is coming off TSV 715 in D15 that would only 16:18
15 depend on the current that the transmission gate in 16:18
16 sa can pass; is that correct? 16:18
17 MR. CHANDLER: Objection. Form. 16:18
18 THE WITNESS: No, that's wrong. We have 16:18
19 been over this many times. It depends on the 16:18
20 entirety of the network model between the driver and 16:18
21 the receiver. 16:18
22 BY MS. ZHONG: 16:18
23 Q. What I mean is that the driver has already 16:18
24 driven the charge up to the segment of TSV 715 on 16:18
25 D15, so the charge is just being pushed through the 16:18

1 transmission gate onto the receiver circuit in that? 16:18

2 A. It doesn't work that way. 16:18

3 Q. Why not? 16:18

4 A. Because that's not the way electromagnetics 16:18

5 works. If one studies the fundamental physics laws 16:19

6 of electromagnetics, things don't happen 16:19

7 independently. They happen as part of the network, 16:19

8 and there's a set of laws that govern that, and 16:19

9 those laws are in place here and they tell us that 16:19

10 the instantaneous current at any spot in a connected 16:19

11 network of components like this depends on the 16:19

12 voltage and the values of all of the elements of the 16:19

13 network. 16:19

14 Q. So if you change the size of the 16:19

15 transmission gate transistors, say you triple the 16:20

16 size, how would that change the charge time of the 16:20

17 receiver circuit? 16:20

18 A. You would need to model the entire circuit. 16:20

19 In many cases, it would be a trivial change, but 16:20

20 there could be circumstances where it was a 16:20

21 significant change that typically one would avoid 16:20

22 those. But, again, you would have to model it. 16:20

23 It's very similar to if I made all the wires 16:21

24 in my house a hundred times larger, the light bulbs 16:21

25 really wouldn't turn on any faster because the 16:21

1 originals were big enough. 16:21

2 Q. But can you use a one-gate transistor to 16:21

3 charge up, say, a 100 transistor's receiver circuit 16:21

4 fast enough? 16:21

5 MR. CHANDLER: Objection to form. 16:21

6 THE WITNESS: Yes, depending on how fast 16:21

7 "fast enough" is. 16:21

8 BY MS. ZHONG: 16:21

9 Q. For SDRAMs. 16:21

10 MR. CHANDLER: Objection. Form. 16:22

11 THE WITNESS: Again, you have to model the 16:22

12 entirety of the circuit. 16:22

13 BY MS. ZHONG: 16:22

14 Q. Have you done that modeling to see whether 16:22

15 that could be done? 16:22

16 MR. CHANDLER: Object to form. 16:22

17 THE WITNESS: No, I did not rely on -- on a 16:22

18 model at that level of detail in my analysis and, in 16:22

19 part, I didn't have to because Riho tells me that 16:22

20 having the transmission gates reduces the capacitive 16:22

21 load. 16:22

22 BY MS. ZHONG: 16:23

23 Q. But you still have to -- but the 16:23

24 transmission -- the transmission gate transistor 16:23

25 still has to be powerful enough to allow enough -- 16:23

1 sufficient current to pass through it in order to 16:23
2 charge up the receiver circuit in time, doesn't it? 16:23
3 MR. CHANDLER: Objection. Form. 16:23
4 THE WITNESS: It does. There would be no 16:23
5 reason to doubt that that is true in Riho. But even 16:23
6 so, Riho doesn't specify that it has to run at some 16:23
7 particular speed. One could implement Riho at a 16:23
8 very slow speed and it would still contain the 16:23
9 teachings. But there is no indication whatsoever in 16:23
10 Riho that it could not operate as disclosed at 16:23
11 commercially viable speeds. 16:23
12 BY MS. ZHONG: 16:24
13 Q. Okay. So in order for you to charge up the 16:24
14 receiver circuit through the transmission gate, 16:24
15 doesn't the capacitance -- the input capacitance of 16:24
16 the transmission gate need to be comparable to the 16:24
17 capacitance of the receiver circuit? 16:24
18 MR. CHANDLER: Objection. Form. 16:24
19 THE WITNESS: No. 16:24
20 BY MS. ZHONG: 16:24
21 Q. Why not? 16:24
22 A. It doesn't. There's no reason for that and 16:24
23 there's no reason to expect that it would be. 16:24
24 Again, there are a number of reasons to suspect that 16:24
25 it wouldn't. 16:24

1 One is that it's a drain capacitance rather 16:24
2 than a gate capacitance, which is generally one to 16:24
3 be lower in this kind of circuit. 16:24
4 Two, it has been turned on in advance so, 16:25
5 therefore, the differential between the two sides of 16:25
6 the -- in between the drain and the source is 16:25
7 minimal. And it only has a very small load on the 16:25
8 right side as compared to the driver and receiver 16:25
9 which connect to an entire memory array. 16:25
10 So there's no reason to doubt that it would 16:25
11 behave exactly the way Riho represents it, that it 16:25
12 would substantially reduce the capacitive load and 16:25
13 that it would run at satisfactory speeds. 16:25
14 Q. So Riho's transmission gates are turned on 16:25
15 in advance, but not the receiver circuit. Those are 16:28
16 charged up and discharged in time when transmission 16:28
17 occurs; correct? 16:28
18 MS. ZHONG: Objection. Form. 16:29
19 THE WITNESS: In Riho in the Figure 6 16:29
20 embodiment, the transmission gates are turned on or 16:29
21 off in advance, and the receiver circuit charges and 16:29
22 discharges whenever there's a write operation to 16:29
23 that particular DRAM die. 16:29
24 BY MS. ZHONG: 16:29
25 Q. Okay. So the fact that the transmission 16:29

1 gates are charged in advance doesn't really mean 16:29
2 that the receiver circuit's transistors can be 16:30
3 charged up sufficiently fast, does it? 16:30
4 MR. CHANDLER: Object to form. 16:30
5 THE WITNESS: Not in and of itself. It 16:30
6 means that it won't interfere with it being charged 16:30
7 sufficiently fast, but you still have to design the 16:30
8 rest of the circuit appropriately. 16:30
9 BY MS. ZHONG: 16:30
10 Q. So the transmission gates have to be 16:30
11 designed to pass through an amount of the current 16:30
12 that can charge up the receiver circuit in time; is 16:30
13 that correct? 16:30
14 MR. CHANDLER: Objection. Form. 16:30
15 THE WITNESS: Yes. I think we've been over 16:30
16 that, but that's not difficult to do. In fact, it 16:30
17 would often be possible to do with a minimum size 16:30
18 transistor transmission gate. 16:30
19 BY MS. ZHONG: 16:31
20 Q. Okay. But you have not really calculated 16:31
21 what would be that minimum size transmission gate 16:31
22 for Riho's configuration preferred embodiment; 16:31
23 correct? 16:31
24 MR. CHANDLER: Objection. Form. 16:31
25 THE WITNESS: It would be different 16:31

1 depending on all of the details, but it would be a 16:31
2 routine calculation. 16:31
3 BY MS. ZHONG: 16:31
4 Q. But you have not found that for the 16:31
5 preferred embodiments in Riho; correct? 16:31
6 MR. CHANDLER: Object to form. 16:31
7 THE WITNESS: No. Because Riho has done it 16:31
8 and he has already told us that it operates at a 16:31
9 reasonable speed. In fact, he's willing to slow it 16:31
10 down a little bit, and he's already told us that 16:31
11 using the transmission gates reduces the 16:31
12 capacitance. In fact, when he talks about the 16:31
13 Figure 8 embodiment where there are two transmission 16:31
14 gates that could be turned on, he represents that 16:31
15 turning one of them off reduces the capacitance 16:32
16 approximately in half. 16:32
17 BY MS. ZHONG: 16:32
18 Q. Now, in Riho, if there is significant 16:32
19 capacitive loading or input capacitance in switch 16:35
20 circuit sa or sb that can be experienced by a TSV, 16:35
21 is it your opinion that TSV 715 would be -- let me 16:35
22 withdraw and ask this question. 16:35
23 Let's assume that SDRAM D14 in Figure 5 of 16:36
24 Riho, in that particular circuit, the -- even though 16:36
25 the switch circuit sa and sb are turned off, the 16:36

1 TSV 715 will still experience -- will still 16:36
2 experience a significant capacitive load from either 16:36
3 switch circuit A or switch circuit B. 16:36
4 In that circumstance, would you consider the 16:36
5 TSV 715 to be in communication, in electrical 16:36
6 communication with SDRAM D14 or not? 16:36
7 MR. CHANDLER: Object to form. 16:36
8 THE WITNESS: So Riho tells us that the 16:36
9 capacitive load of sa and sb on D14 in TSV 715 is 16:36
10 not insignificant. But even if we were to ignore 16:37
11 that, it would not be in electrical communication 16:37
12 with D14. 16:37
13 In the first place, Riho specifically tells 16:37
14 us that it is not in electrical communication, that 16:37
15 it is not electrically coupled. But, again, even if 16:37
16 we were to ignore all those teachings, there is no 16:37
17 information being communicated. 16:37
18 BY MS. ZHONG: 16:37
19 Q. So for a TSV to be in electrical 16:37
20 communication with die array, that requires data to 16:37
21 be transferred from the memory cells to the TSV? 16:37
22 MR. CHANDLER: Object to form. 16:37
23 THE WITNESS: No. 16:37
24 BY MS. ZHONG: 16:37
25 Q. Then when you say "there is no information 16:38

1 being communicated," what information are you 16:38
2 referring to? 16:38
3 A. Any signal whatsoever. The teaching in Riho 16:38
4 is that the signals are all blocked from 16:38
5 communicating with any of the circuits on the die. 16:38
6 The first transistor that is encountered blocks the 16:38
7 communication. That's its intent. 16:38
8 Q. But the signal wave is due to the bouncing 16:38
9 off the transistors, reflected off the transistors; 16:38
10 correct? 16:38
11 MR. CHANDLER: Objection. Form. 16:38
12 THE WITNESS: In some sense, yeah, at a 16:38
13 minimal level. But, again, that's not the ordinary 16:38
14 meaning of electrical communication. The claims 16:38
15 could have said "physically disconnected" if they 16:38
16 wanted to claim that. They said not in electrical 16:39
17 communication. 16:39
18 And I think any person of ordinary skill 16:39
19 would understand that if there is a disconnected 16:39
20 switch directly adjacent to the TSV, that it's not 16:39
21 an electrical communication. And even if they 16:39
22 didn't understand that on their own, once Riho told 16:39
23 them that, they would accept it. 16:39
24 BY MS. ZHONG: 16:39
25 Q. So it's your opinion that if the TSV is not 16:40

1 connected to a switch or is connected to a 16:40
2 disconnect switch, then there is no electrical 16:40
3 communication between the TSV and the -- and the 16:40
4 DRAM die; is that right? 16:40
5 MR. CHANDLER: Object to form. 16:40
6 THE WITNESS: Not really. 16:40
7 BY MS. ZHONG: 16:40
8 Q. Okay. 16:40
9 A. If the TSV is not connected to the -- to 16:40
10 the DRAM die, then there would be no electrical 16:40
11 communication unless it were somehow using something 16:40
12 unusual like radio or light, and if the only 16:40
13 connection is to a turned-off switch, then there is 16:40
14 no electrical communication. And that's the 16:41
15 situation we have here. 16:41
16 You can see that in D15, it is connected to 16:41
17 a turned-off switch and a turned-on switch. There 16:41
18 is electrical communication there. 16:41
19 Q. So if the switches are turned on by default 16:41
20 but can be programmed to be turned off during the -- 16:41
21 during normal operation, is there still electrical 16:41
22 communication? 16:41
23 MR. CHANDLER: Objection. Form. 16:41
24 THE WITNESS: I'm sorry. Is the question if 16:41
25 you had a hypothetical system where there's a switch 16:41

1 between the DRAM die and the through hole via that 16:41
2 is on by default but can be turned off, is it an 16:42
3 electrical communication? 16:42
4 BY MS. ZHONG: 16:42
5 Q. Yes. 16:42
6 A. It's an electrical communication when it's 16:42
7 on, and it is not an electrical communication when 16:42
8 it's off. Assuming, of course, that there is 16:42
9 something on the other side of the switch to 16:42
10 communicate with. 16:42
11 Q. And if you have a TSV that's only connected 16:42
12 to a stub in a memory die, is there electrical 16:43
13 communication? 16:43
14 MR. CHANDLER: Objection. Form. 16:43
15 THE WITNESS: I would think a person of 16:43
16 ordinary skill would say no because there's nothing 16:43
17 being communicated with. 16:43
18 BY MS. ZHONG: 16:43
19 Q. If the TSV goes through a memory die and is 16:43
20 connected to nothing but another wire and that wire 16:44
21 connects to the die above it or -- above it, is the 16:44
22 TSV in communication -- let me withdraw and ask. 16:44
23 So assume that TSV 715 in Riho, it goes 16:44
24 through, for example, D14, and the segment of the 16:44
25 TSV that goes through D14 is connected to another 16:44

1 wire and that wire is not connected to any other 16:45
2 circuit in D14, but is connected to, say, SDRAM D6, 16:45
3 is SDRAM D14 in communication with TSV 715? 16:45
4 MR. CHANDLER: Objection. Form. Outside 16:45
5 the scope of direct and incomplete hypothetical. 16:45
6 THE WITNESS: I don't have an opinion on 16:45
7 that. That's just not a situation that I had to 16:45
8 consider as part of this case. 16:45
9 BY MS. ZHONG: 16:45
10 Q. So you have no opinion whether that involves 16:45
11 an electrical communication between D14 and TSV 715? 16:45
12 A. Right. I have no opinion on that because 16:45
13 it's just not a -- not a situation that was 16:45
14 disclosed in any of the art that I looked at. 16:45
15 Q. Okay. In that situation, what kind of 16:46
16 information can be exchanged before D14 and TSV 715? 16:46
17 MR. CHANDLER: Objection. Form. And 16:46
18 outside the scope of direct. 16:46
19 THE WITNESS: I don't know. Again, I didn't 16:46
20 consider that situation. I don't have an opinion on 16:46
21 it. 16:46
22 BY MS. ZHONG: 16:46
23 Q. What's the relevant -- 16:47
24 (Clarification requested by Reporter.) 16:47
25 / / / 16:47

1	BY MS. ZHONG:	16:47
2	Q. What is the relevant contribution of the	16:47
3	capacitor load from a segment of the TSV versus the	16:47
4	contribution from a memory die?	16:48
5	MR. CHANDLER: Objection. Form.	16:48
6	THE WITNESS: In Riho?	16:48
7	BY MS. ZHONG:	16:48
8	Q. We can start with Riho.	16:48
9	A. It would depend on the particular embodiment	16:48
10	and a variety of implementation details. But Riho	16:48
11	teaches us that the -- there is substantial benefit	16:48
12	in reduced capacitance by using the transmission	16:48
13	gate switches to isolate the memory die capacitance.	16:48
14	Q. So take D15, for example, do you know what	16:48
15	is the relevant contribution of the capacitive load	16:49
16	from TSV 715 itself versus from the memory die?	16:49
17	A. Same answer.	16:49
18	Q. In D15, the gate is not -- is not turned	16:49
19	off, so there is capacitive load from the array	16:49
20	die -- from the memory die; correct?	16:49
21	MR. CHANDLER: Objection. Form.	16:49
22	THE WITNESS: In Figure 5, there would be a	16:49
23	capacitive load on TSV 715 from components on the	16:49
24	memory die for D15.	16:50
25	/ / /	16:50

1 BY MS. ZHONG: 16:50

2 Q. Okay. So what's the relevant contribution 16:50

3 of the capacitive load from the memory die as 16:50

4 compared to the contribution from C1R1 in the 16:50

5 TSV 715? 16:50

6 MR. CHANDLER: Objection. Form. 16:50

7 THE WITNESS: It would depend on the 16:50

8 specific implementation parameters, but Riho teaches 16:50

9 us that there is a substantial benefit from turning 16:50

10 it off. And in fact, in the Figure 8 embodiment, 16:50

11 tells us that if we were to turn off one of D7 and 16:50

12 D15, we would approximately cut the capacitance in 16:50

13 half. 16:50

14 BY MS. ZHONG: 16:50

15 Q. I'm asking you specifically for D15, that 16:50

16 segment, how much of a contribution there is from 16:50

17 the SDRAM die versus from the TSV segment. 16:51

18 MR. CHANDLER: Objection. Form. 16:51

19 THE WITNESS: I answered that already. 16:51

20 BY MS. ZHONG:

21 Q. No, you have not. What's the relevant 16:51

22 contribution? 16:51

23 A. I don't have a different answer. It 16:51

24 depends on the implementation parameters, but we 16:51

25 are taught by Riho that it is a substantial amount 16:51

1 of capacitance. There's a substantial benefit from 16:51
2 isolating it. And that in, for example, the 16:51
3 Figure 8 embodiment, that if one of D15 or D7, 16:51
4 either one, is disconnected, that it is 16:51
5 approximately half the capacitance that is 16:51
6 removed from the capacitive load. 16:51
7 Q. What is the difference between a DRAM 16:51
8 circuit and a DRAM die? 16:52
9 MR. CHANDLER: Objection. Form. 16:52
10 THE WITNESS: It would depend on context in 16:52
11 some cases, but a circuit -- a DRAM circuit would 16:52
12 ordinarily be any interconnection of electronic 16:52
13 components that's used to implement a DRAM, where a 16:52
14 DRAM die would be one physical piece of silicon that 16:52
15 contains DRAM circuits. 16:52
16 BY MS. ZHONG: 16:52
17 Q. So is DRAM die the same as DRAM circuit? 16:53
18 MR. CHANDLER: Objection. Form. 16:53
19 THE WITNESS: Not exactly, but by my 16:53
20 experience, a DRAM die would include one or more 16:53
21 DRAM circuits on it. 16:53
22 BY MS. ZHONG: 16:53
23 Q. So is a DRAM die different than a DRAM 16:53
24 circuit? 16:53
25 MR. CHANDLER: Objection. Form. 16:53

1 THE WITNESS: It could be, but in ordinary 16:53
2 usage, a DRAM die would contain one or more DRAM 16:53
3 circuits. 16:53
4 I could have, for example, the system on a 16:53
5 chip that was in the Xbox that was not something 16:53
6 that would normally be called a DRAM die because it 16:53
7 had a CPU and a bunch of other things on it, but it 16:53
8 included a DRAM circuit. 16:53
9 But in my experience, a DRAM die would 16:53
10 include one or more DRAM circuits. 16:53
11 BY MS. ZHONG: 16:53
12 Q. Okay. So a DRAM die that includes one or 16:53
13 more DRAM circuits are the same as the DRAM circuit 16:54
14 itself? 16:54
15 MR. CHANDLER: Objection. Form. 16:54
16 THE WITNESS: No. I already explained. 16:54
17 BY MS. ZHONG: 16:54
18 Q. Okay. So a DRAM die that includes one or 16:54
19 more DRAM circuits are different than a DRAM circuit 16:54
20 cell? 16:54
21 MR. CHANDLER: Objection. Form. 16:54
22 BY MS. ZHONG: 16:54
23 Q. Sorry. 16:54
24 A DRAM die that includes one or more DRAM 16:54
25 circuits is different than the DRAM circuit itself? 16:54

1 MR. CHANDLER: Objection. Form. 16:54

2 THE WITNESS: I would think that that would 16:54

3 be a misleading statement. Not every DRAM circuit 16:54

4 is on what would normally be called a DRAM die, but 16:54

5 an ordinary DRAM die includes one or more DRAM 16:54

6 circuits. 16:54

7 BY MS. ZHONG: 16:54

8 Q. Okay. So does that make the DRAM circuit 16:55

9 the same as the DRAM die -- let me put it this way. 16:55

10 Does that make the DRAM die the same as the 16:55

11 DRAM circuit? 16:55

12 MR. CHANDLER: Objection. Form. 16:55

13 THE WITNESS: It depends what purpose you 16:55

14 are using the terms for. I would think that they 16:55

15 would be interchangeable in many instances. But the 16:55

16 die refers to some -- to the -- to the physical 16:55

17 piece of silicon and the circuit refers to the 16:55

18 contents of that physical piece of silicon. 16:55

19 There are circumstances where one might want 16:55

20 to make a distinction, but they would be unusual 16:55

21 circumstances. 16:55

22 BY MS. ZHONG:

23 Q. Does the fact that the DRAM die includes 16:56

24 more than the DRAM circuit make it different than 16:56

25 the DRAM circuit? 16:56

1 MR. CHANDLER: Object to form. 16:56

2 THE WITNESS: Again, it would depend on 16:56

3 context. It would not be at all unusual for 16:56

4 somebody to refer to a DRAM die as a DRAM circuit 16:56

5 because it includes -- it is a collection of 16:56

6 electronic components that implements a DRAM. 16:56

7 It always depends on context, but from the 16:56

8 perspective of something like the '060 or the '160 16:56

9 patent, I don't think there is any reason to make a 16:56

10 distinction between the two. 16:56

11 BY MS. ZHONG: 16:56

12 Q. What is the meaning of DRAM circuit in 16:56

13 Rajan? 16:57

14 MR. CHANDLER: Object to form. 16:57

15 THE WITNESS: It would be the ordinary 16:57

16 meaning; a collection of electronic components that 16:57

17 implement a DRAM to the extent that that phrase is 16:57

18 used. 16:57

19 By "Rajan," I assume you mean Exhibit 1015 16:57

20 and not 1011? 16:57

21 BY MS. ZHONG: 16:57

22 Q. Yes. Well, they're the same. 16:57

23 MR. CHANDLER: Objection. Form. 16:57

24 BY MS. ZHONG: 16:57

25 Q. Let's put it this way. Does the term "DRAM 16:57

1 circuit" have a different meaning in Exhibit 1011 16:57
2 than in Exhibit 1015? 16:57
3 MR. CHANDLER: Objection. Form. 16:57
4 THE WITNESS: I don't believe so. In both 16:58
5 cases, it is the ordinary meaning. It is a 16:58
6 collection of interconnected electronic components 16:58
7 that implement DRAM. 16:58
8 DEPOSITION REPORTER: Miss Zhong, is it okay 17:01
9 if we go off the record? 17:01
10 MS. ZHONG: Sure. 17:01
11 (Ending time: 5:02 p.m.) 17:02
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I, ANDREW WOLFE, do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this ____ day of _____,
2023, at _____, - _____.
(City) (State)

ANDREW WOLFE

1 I, JANIS JENNINGS, CSR No. 3942, Certified
2 Shorthand Reporter, certify:

3 That the foregoing proceedings were taken
4 before me at the time and place therein set forth, at
5 which time the witness was duly sworn by me;

6 That the testimony of the witness, the
7 questions propounded, and all objections and statements
8 made at the time of the examination were recorded
9 stenographically by me and were thereafter transcribed;

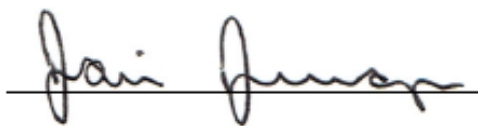
10 That the foregoing pages contain a full, true
11 and accurate record of all proceedings and testimony.

12 Pursuant to F.R.C.P. 30(e)(2) before
13 completion of the proceedings, review of the transcript
14 [X] was [] was not requested.

15 I further certify that I am not a relative or
16 employee of any attorney of the parties, nor financially
17 interested in the action.

18 I declare under penalty of perjury under the
19 laws of California that the foregoing is true and
20 correct.

21 Dated this 5th day of July 2023.

22
23 

24 JANIS JENNINGS, CSR NO. 3942

25 CLR, CCRR

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co. Ltd. Case No. IPR2022-01427
 Petitioner, Patent No. 9,318,160
 vs.
 Netlist, Inc., Case No. IPR2022-01428
 Patent Owner. Patent No. 8,787,060

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CONTINUED VIDEOCONFERENCE DEPOSITION OF
ANDREW WOLFE, Ph.D.
Volume II (Pages 192 - 229)
Wednesday, June 28, 2023

Reported Remotely and Stenographically by:
JANIS JENNINGS, CSR No. 3942, CLR, CCRR
Job No. 5965317

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CONTINUED DEPOSITION OF ANDREW WOLFE, Ph.D.,
appearing remotely, located in Santa Clara,
California, taken on behalf of the Petitioner,
beginning at 9:00 a.m., on Wednesday, June 28, 2023,
sworn remotely by Janis Jennings, Certified Shorthand
Reporter No. 3942, CCRR, located in the City of
Walnut Creek, County of Contra Costa, State of
California.

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1 Wednesday, June 28, 2023; 9:00 a.m.

2

3 ANDREW WOLFE, Ph.D.,

4 having been previously sworn, resumed

5 testifying as follows:

6

7 EXAMINATION (Resumed) 08:54

8 BY MS. ZHONG: 08:54

9 Q. Good morning, Dr. Wolfe. Do you mind 09:01
10 pulling up Exhibit 1016, Riho, Figure 4. 09:01

11 A. Okay. 09:02

12 Q. Okay. So in Figure 4 do you see that there 09:02
13 are -- as shown there are four TSVs shown in 09:02
14 Figure 4? 09:02

15 A. There are four that are illustrated, yes. 09:02

16 Q. Okay. And for the TSV annotated as TSV 08, 09:02
17 they are two -- the TSV basically have switch 09:02
18 circuits with SDRAM D0 and D8; correct? 09:02

19 A. Let's look at the text for the Figure 4 09:02
20 embodiment. Yes, I believe that's correct. 09:02

21 Q. Okay. And for TSV 15 the two array dies 09:03
22 with switch on switch circuits as D7 and D15 at the 09:03
23 top of the stack; correct? 09:03

24 A. Yes, that's my understanding. 09:03

25 Q. Okay. So when you drive a data bit up 09:03

1 TSV 08, what is the load that it needs to overcome? 09:03
2 MR. CHANDLER: Objection. Form. 09:03
3 THE WITNESS: The specific load can't be 09:03
4 calculated with the information that's available. I 09:03
5 mean there are a lot of teachings in this 09:03
6 specification about how this reduces the load, but 09:03
7 you would need more information to quantitatively 09:04
8 compute the specific load for a specific -- 09:04
9 BY MS. ZHONG:
10 Q. Okay.
11 A. -- for a specific TSV.
12 Q. I'm not -- sorry. I'm not looking for a 09:04
13 number. What I want to understand is when you drive 09:04
14 data up to TSV 08, it seems that data are likely -- 09:04
15 ae only going to be written into either D0 or D8 at 09:04
16 the bottom. Do you care about the load that's 09:04
17 imposed by the segment of TSVs from D1 through D15 09:04
18 when you drive the data bits? 09:04
19 A. I'm finding the question "do you care" to be 09:04
20 very ambiguous. 09:04
21 Q. Okay. Do you have to overcome the loads 09:04
22 that's imposed by the segments, basically the unused 09:04
23 segments of the TSVs -- 09:05
24 A. Yes. 09:05
25 Q. -- from D1 through D15? 09:05

1 A. Yes. As we discussed yesterday, you need to 09:05
2 look at the entirety of the resistance capacitance, 09:05
3 inductance network in order to understand the load 09:05
4 on the driver that is driving that TSV and that's 09:05
5 what's illustrated in Figure 5. 09:05

6 There are minor differences in what the 09:05
7 network topology is, depending on whether or not a 09:05
8 top set of die are turned on as in TSV715 which is 09:05
9 how that last one should be labeled or TSV 08. The 09:05
10 topologies are a little bit different because the 09:05
11 turned on transmission gates are in a different 09:05
12 place. 09:06

13 Q. Uh-huh. 09:06

14 A. But the patent explains in quite a bit of 09:06
15 detail that there are resistors that are used to 09:06
16 compensate for some of that difference, and that 09:06
17 this is a good approach for trying to make the loads 09:06
18 reasonably close to each other. 09:06

19 Q. So you're saying like when you drive data up 09:06
20 TSV 08 versus TSV 15, as far as a load attributable 09:06
21 to the TSV segment themselves, they will be 09:06
22 relatively close to each other? 09:06

23 A. Yes. Although in practice you can never 09:06
24 look at the load just attributable to the TSV 09:06
25 segments themselves because the loads all work 09:06

1 together, whether they're from the TSV segments or 09:07
2 from other things. 09:07
3 Q. Okay. What about -- why don't we switch to 09:07
4 Kim which is Exhibit 1014, Figure 5. 09:07
5 A. Yes. 09:07
6 Q. Okay. So in Figure 5 of Kim are the loads 09:07
7 from the TSV 1 and TSV2 more like [indiscernible] -- 09:07
8 (Clarification requested by Reporter.) 09:07
9 MS. ZHONG: I'm trying to figure out where 09:07
10 did you get -- I can't get the real time. Sorry. 09:08
11 DEPOSITION REPORTER: Okay. Why don't we go 09:08
12 off the record. 09:08
13 (Off the record.) 09:08
14 BY MS. ZHONG: 09:08
15 Q. So take a look at Figure 5. In Figure 5 of 09:09
16 Kim there are two TSVs shown, TSV 1 and TSV 2; 09:09
17 correct? 09:09
18 A. Yes. 09:09
19 Q. Okay. TSV 1 only goes up to the die 100 or 09:09
20 the C1 die; correct? 09:09
21 A. As literally illustrated, that's true. 09:09
22 Q. Okay. And TSV 2, as illustrated, goes up to 09:09
23 the C2 die. 09:09
24 A. From the C0 die, that's correct. 09:09
25 Q. Okay. And TSV 2 is longer than TSV 1; 09:09

1 correct? 09:09

2 A. In this specific example, it is. 09:09

3 Q. Okay. And so the load attributable from 09:09

4 TSV 2, is it larger than that of TSV 1? 09:09

5 A. In the unmodified example of Figure 5, as 09:10

6 illustrated, the load of TSV 2 would be greater than 09:10

7 the load on TSV 1. 09:10

8 Q. Okay. And do you know what is the relative 09:10

9 contribution of the load from TSV versus the array 09:10

10 die in Kim? 09:10

11 A. No. That would be a design choice based on 09:10

12 a number of ordinary considerations. One would just 09:10

13 simply simulate them or measure them for a 09:10

14 particular design. 09:10

15 Q. Okay. But do you know what's the range of 09:10

16 the contributions due to the TSV segment versus the 09:10

17 array die? 09:10

18 A. No. It would vary from embodiment to 09:10

19 embodiment, but it's an easy calculation to do once 09:10

20 you have the details of the design. 09:10

21 Q. Okay. And why don't we go to Figure 3 of 09:11

22 Kim. 09:11

23 A. Okay. 09:11

24 Q. So in Figure 3 there are only two ranks 09:11

25 shown; correct? 09:11

1 A. Yes. As illustrated in Figure 3, there are 09:11
2 only two ranks shown. 09:11

3 Q. Okay. And yesterday we discussed what -- 09:11
4 how a POSITA would modify Kim in order to 09:11
5 accommodate four ranks, and one of the accommodation 09:11
6 is to have, for example, Rank2 also connect to the 09:11
7 GIO_Rank0 line and Rank3 connected to GIO_Rank1 09:11
8 line. 09:11

9 Do you remember that discussion? 09:11

10 A. That would be one possible way to do it. 09:11

11 Q. Okay. So in that configuration, and let's 09:11
12 say the host wants to write or read from Rank0, do 09:12
13 the write driver and the read sense amplifiers in 09:12
14 the other three ranks need to be switched off? 09:12

15 A. They don't need to be switched off, but they 09:12
16 need to be not driving in the same way as any four 09:12
17 rank -- or any four rank system with two buses that 09:12
18 would be known in the prior art. 09:12

19 Q. How can you not turn them -- disable them -- 09:12

20 A. Well, you don't -- 09:12

21 Q. Okay. Sorry. Go ahead. 09:12

22 MR. CHANDLER: Object to form. 09:12

23 THE WITNESS: You don't have to fully 09:13
24 disable them. You simply have to block them from 09:13
25 driving the bus. The bus can only be driven by one 09:13

1 rank at a time and that's something that is not at 09:13
2 all unique to Kim. It's something that's a general 09:13
3 principle in that type of rank multiplication and 09:13
4 that a person of ordinary skill would know how to 09:13
5 implement from the prior art. 09:13

6 BY MS. ZHONG:

7 Q. And how can you block the driver from 09:13
8 driving the data to the bus without disabling the 09:13
9 driver circuit? 09:13

10 A. There are a number of ways to do that. One 09:13
11 is you can simply tri-state the output stage of the 09:13
12 driver circuit without disabling the driver circuit 09:13
13 as a whole. You could also put some type of a 09:13
14 multiplexer between the bus and the driver. You can 09:13
15 also put separate tri-state buffers in to build a 09:13
16 multiplexer, or you can use transmission gate 09:13
17 switches to build a multiplexing function. 09:14

18 There are lots of ways to select between two 09:14
19 different circuits that are both capable of driving 09:14
20 a bus in a way that only one of them does. There's 09:14
21 also a technique using what is called open drain 09:14
22 drivers as well, and they are all common and known 09:14
23 in the art. 09:14

24 Again rank multiplication was known by this 09:14
25 time and nothing in Kim indicates that it needs to 09:14

1 be done in any special way. The ordinary techniques 09:14
2 can be adapted to work with Kim. 09:14
3 Q. Okay. So assume that if you are not 09:14
4 disabling a driver circuit but block the driver from 09:14
5 driving the data onto the data bus, is there 09:14
6 communication between the GIO_Rank0 and the memory 09:14
7 dies -- 09:15
8 MR. CHANDLER: Object to form. 09:15
9 BY MS. ZHONG: 09:15
10 Q. -- to which the data has been blocked by the 09:15
11 driver circumstances? 09:15
12 MR. CHANDLER: Object to form. 09:15
13 THE WITNESS: There certainly could be 09:15
14 because you could still be connected to the read 09:15
15 sense amplifiers. I'm sorry, the other way around. 09:15
16 You could still be selected to -- it's the 09:15
17 read sense amplifiers that would -- you know, let me 09:15
18 clarify everything that we said here. 09:15
19 It's the read sense amplifiers that would be 09:15
20 driving the GIO, not the write driver. 09:15
21 BY MS. ZHONG:
22 Q. Okay.
23 A. Right? So that's the one that needs to be 09:15
24 blocked. The write driver can still remain 09:15
25 connected and in communication with GIO_rank0 or 09:15

1	GIO_Rank1, that's not a problem.	09:15
2	Q. But if you are just writing to Rank2 or	09:15
3	Rank0, and you have the write driver for Rank2 on,	09:15
4	wouldn't the data be written into Rank2 memory cells	09:16
5	as well?	09:16
6	A. No. Because you would use the appropriate	09:16
7	chip select or write enables to stop that from	09:16
8	happening.	09:16
9	Q. You're saying the data is driven by the	09:16
10	write driver to the corresponding memory die [cell	09:16
11	phone interruption] --	09:16
12	DEPOSITION REPORTER: Counsel, can we go off	09:16
13	the record, please.	09:16
14	(Off the record.)	09:19
15	BY MS. ZHONG:	09:19
16	Q. Dr. Wolfe, how would the chip select signal	09:19
17	or write enable signal stop data from being written	09:20
18	into Rank2 if both Rank1 and Rank2 write drivers are	09:20
19	enabled or active?	09:20
20	MR. CHANDLER: Object to form.	09:20
21	THE WITNESS: Well, again you're talking	09:20
22	about a modified design and one would modify it in a	09:20
23	sensible way as is taught in the prior art.	09:20
24	So each of the ranks that is connected to	09:20
25	GIO_Rank0 would have its own chip select and its own	09:20

1 write enabled, and in the ordinary course, that's 09:20
2 what those two signals are intended to do. They're 09:20
3 intended to tell the memory, each memory rank 09:20
4 whether to pay attention to the incoming signals or 09:20
5 to ignore the incoming signals. 09:20

6 The whole point of a write enable is that it 09:20
7 has two possible states, one saying that you should 09:21
8 write and one saying you should not write. 09:21

9 BY MS. ZHONG:

10 Q. Now, if you leave the Rank2 as well as Rank1 09:21
11 write drivers on all the time instead of just having 09:21
12 them on during the write operation, would that 09:21
13 consume so much power that a POSITA would not pursue 09:21
14 such a design? 09:21

15 MR. CHANDLER: Objection. Form. 09:21

16 THE WITNESS: You'd have to do the analysis. 09:21
17 Again it depends whether or not the load from the 09:21
18 write driver is separately blocked. It depends on 09:21
19 the design of the write driver. And it depends on 09:21
20 whether or not a POSITA has a choice. A POSITA may 09:21
21 have to use existing memory die and not have an 09:22
22 option there. 09:22

23 So again it's -- rank multiplication is well 09:22
24 known. It's -- the trade-offs are well known. And 09:22
25 a person of ordinary skill could make the same 09:22

1 engineering design decisions in the context of Kim 09:22
2 that they could make in the prior art. 09:22
3 BY MS. ZHONG: 09:22
4 Q. What do you mean by whether or not the load 09:22
5 from the write driver is separately blocked? 09:22
6 Blocked by what and from what? 09:22
7 A. A modern memory chip has billions of 09:22
8 circuits. So even if the write driver is on, there 09:22
9 may not be just -- the write driver may not be 09:22
10 connected directly to the memory array. There may 09:22
11 be a write enable stage that follows it. And if the 09:22
12 write enable stage is blocking the write driver 09:22
13 signals from going to the memory array, then the 09:22
14 write driver would use less power than if it were 09:23
15 connected to the memory array. 09:23
16 So you need to do a case-by-case analysis. 09:23
17 But also, again, if -- you know, engineers have 09:23
18 commonsense. If the write driver was using too much 09:23
19 power, they would disable it when write enable is 09:23
20 not asserted or when chip select is not asserted. 09:23
21 Q. Now, based on your knowledge, how much -- 09:23
22 what is the common way of enabling and disabling 09:23
23 write drivers at the time of the invention? If it's 09:23
24 at a default those write drivers are off and only 09:23
25 turned on or whether as default they're usually on? 09:23

1 MR. CHANDLER: Objection. Form. 09:24

2 THE WITNESS: It's a design choice depending 09:24

3 on the trade-offs between speed and power and chip 09:24

4 complexity. I'm sure throughout the industry both 09:24

5 techniques have been used and both are well within 09:24

6 the skill of a person of ordinary skill. 09:24

7 In my experience typically write drivers are 09:24

8 only turned on -- again it also depends on the 09:24

9 memory type as well. It would be different for a 09:24

10 SRAM than it would be for a DRAM than it would be 09:24

11 for a flash. 09:24

12 In a DRAM and in a flash, in particular, the 09:24

13 write drivers, there's one write driver to the page 09:24

14 register, there's a different write driver to the 09:24

15 array. Typically the write driver to the array 09:24

16 would only be turned off using and during a page 09:24

17 refresh operation. The write driver to the page 09:24

18 register would typically be turned on when chip 09:25

19 select and write enable have the appropriate values 09:25

20 to turn it on. 09:25

21 But actually, again, in a modern memory 09:25

22 there's typically more than one bank and there would 09:25

23 typically be more than one write driver in practice. 09:25

24 And, in fact, address bits would be used to select 09:25

25 one of them to turn on and not all of them, or one 09:25

1 set of them to turn on and not all of them. 09:25
2 BY MS. ZHONG: 09:25
3 Q. What about the write drivers that's in 09:25
4 block 1000? 09:26
5 MR. CHANDLER: Object to form. 09:26
6 THE WITNESS: I don't see anything called a 09:26
7 write driver in block 1000. 09:26
8 BY MS. ZHONG: 09:26
9 Q. Well, in order for you to write the data 09:26
10 from the D2 line into to the Rank0, does there need 09:26
11 to be a driver in block 1000? 09:26
12 MR. CHANDLER: Objection. Form. 09:26
13 BY MS. ZHONG: 09:26
14 Q. Does the write sense amplifier serve as the 09:26
15 write driver? 09:26
16 A. I mean it depends how you're driving the 09:26
17 write driver. The write sense amplifier will 09:26
18 provide signals to the write selecting unit. 09:26
19 Q. Is it driving the data? 09:26
20 A. In the abstract everything that sends data 09:27
21 from one place to another is driving the data. But 09:27
22 we usually reserve the word "driver" for things that 09:27
23 have to drive with high levels of power. 09:27
24 Q. So how can the data go from D2 to the rank 09:27
25 to 100 without a driver? 09:27

1 MR. CHANDLER: Objection. Form. 09:27

2 THE WITNESS: Again it depends how you're 09:27

3 defining the word "driver." There are circuits. A 09:27

4 data buffer is a logic circuit. The data aligning 09:27

5 unit is a logic circuit. The write sense amplifier 09:27

6 is a logic circuit. The write selecting unit is a 09:27

7 logic circuit. Logic circuits can propagate signals 09:27

8 on wires. 09:28

9 BY MS. ZHONG: 09:28

10 Q. So in your experience are those circuits 09:28

11 turned on only when there are data signals or are 09:28

12 they left on as a default? 09:28

13 MR. CHANDLER: Objection. Form. 09:28

14 THE WITNESS: It's a design choice. People 09:28

15 choose based on what their priorities are for a 09:28

16 particular limitation. Both are very well known in 09:28

17 the art. 09:28

18 BY MS. ZHONG: 09:28

19 Q. When will they choose to leave them on? 09:28

20 MR. CHANDLER: Object to form.

21 THE WITNESS: When will they choose to 09:28

22 leave them on? Was that the question? 09:28

23 BY MS. ZHONG: 09:28

24 Q. Correct. 09:28

25 A. If they have determined that leaving them on 09:28

1 will improve speed and they have decided that they 09:28
2 prioritize speed over power. 09:29
3 Q. And when will they turn it off? 09:29
4 A. They will turn it off if they have either 09:29
5 determined that they can turn them off without 09:29
6 impacting speed or that they prioritize power 09:29
7 savings over ultimate speed. But, again, these are 09:29
8 choices. People can take other factors into 09:29
9 consideration as well. 09:29
10 Q. Okay. 09:29
11 A. Sometimes also things are turned on and off 09:29
12 at certain times to limit noise emissions and 09:29
13 interference with other circuits. 09:29
14 Q. And in Kim does it say that when you have 09:30
15 more than two ranks, the write drivers would be left 09:30
16 on, even when the corresponding rank is not written 09:30
17 to? 09:30
18 MR. CHANDLER: Object to form. 09:30
19 THE WITNESS: No. It's a design choice. 09:30
20 There's nothing in Kim that says that one needs to 09:30
21 make those decisions in any particular way. A 09:30
22 person reading Kim would have knowledge of the scope 09:30
23 of the prior art at the time. It includes a wide 09:30
24 range of designs and they could either leave the 09:30
25 write drivers on or they could turn them on and off. 09:30

1 The same way as it has been done in the prior art. 09:30
2 BY MS. ZHONG: 09:30
3 Q. And you mentioned that for DRAMs, at least 09:30
4 in your design, it's pretty typical to leave the 09:30
5 write drivers off unless there are data, active data 09:31
6 being driven to the corresponding rank; is that 09:31
7 right? 09:31
8 A. In my experience that's typical but not the 09:31
9 only way that it's done. 09:31
10 Q. Okay. What about for SRAMs? 09:31
11 A. Again I've seen both implemented. Sometimes 09:31
12 SRAMs are used in very low power systems and the 09:31
13 write drivers are turned on and off. Or sometimes 09:31
14 the write drivers -- because a SRAM is sometimes not 09:31
15 that big, write drivers can be turned on and off 09:31
16 very quickly. Or they can be left on and some other 09:31
17 circuit can disconnect them from buses. 09:31
18 So both approaches are very well known. 09:31
19 Again this is just ordinary stuff. 09:31
20 Q. What is a more typical one? 09:32
21 MR. CHANDLER: Objection. Form. 09:32
22 THE WITNESS: I couldn't say. 09:32
23 BY MS. ZHONG: 09:32
24 Q. What about NAND? 09:32
25 MR. CHANDLER: Objection. Form. 09:32

1 THE WITNESS: So there are a lot of 09:32
2 different write drivers in NAND. Again people use 09:32
3 different approaches depending on what their 09:32
4 priorities are; both powering on and off write 09:32
5 drivers and not powering on and off write drivers 09:32
6 are known at various points in the NAND chip. 09:32
7 BY MS. ZHONG: 09:32
8 Q. Okay. When you -- you say that there are 09:32
9 many write drivers in NAND, I'm talking about the 09:32
10 write driver as shown in Figure 100, assuming if 09:32
11 Figure 3 applies to NAND memory systems as well. 09:32
12 So for that particular write driver 11, would that 09:32
13 driver be typically turned on or off? 09:32
14 MR. CHANDLER: Objection. Form. 09:33
15 THE WITNESS: There is no reason to make an 09:33
16 assumption one way or another. Both are well known 09:33
17 in the art. 09:33
18 BY MS. ZHONG: 09:33
19 Q. In Kim's system do you know whether it will 09:33
20 be turned on as a default or turned off as a 09:33
21 default? 09:33
22 A. Kim doesn't express a preference either way. 09:33
23 Q. Would a read after write -- the cross rank 09:33
24 read after write collision that Kim mentions in 09:33
25 paragraph 42 and 43, depend on whether the write 09:33

1 driver is left on as a default or whether it's only 09:33
2 turned on during the read and -- during the write 09:33
3 operation? 09:34
4 A. Well, in the first place, that text in 09:34
5 paragraph 42 refers to Figure 1 and not to Figure 3. 09:34
6 But in that case, I don't think it matters whether 09:34
7 or not the write driver is turned on when it's being 09:34
8 used or whether it's turned on all the time because 09:34
9 the collision happens when the write operation 09:34
10 occurs so it is being used. 09:34
11 Q. Okay. And in -- regardless whether its 09:34
12 SRAM, DRAM or NAND, the read sense amplifier would 09:34
13 be -- would only be driving data when there is read 09:34
14 data for a particular rank; is that right? 09:34
15 MR. CHANDLER: Objection. Form. 09:35
16 THE WITNESS: This is in Figure 3 or 09:35
17 Figure 1? 09:35
18 BY MS. ZHONG: 09:35
19 Q. Does it matter? 09:35
20 A. So I think a simple answer would be 09:35
21 misleading. 09:35
22 Q. Okay. 09:35
23 A. The read sense amplifier drives data at most 09:35
24 when read data is available. 09:35
25 Q. Okay.

1	A. But it also only does it when that	09:35
2	particular rank receives the proper control signals	09:35
3	telling it to perform a read operation at a	09:35
4	particular time.	09:35

5	Q. So if the particular rank is not receiving a	09:35
6	command for a particular read operation, is a read	09:36
7	sense amplifier typically left on or they are	09:36
8	usually switched off during that period?	09:36

9	A. Again, it's a design choice. Certainly it	09:36
10	can be left on. This is also, you know, a very	09:36
11	simplified design here shown in Kim. A person of	09:36
12	ordinary skill would certainly know how to leave a	09:36
13	read sense amplifier on and also have a driver that	09:36
14	is being a buffer on the other side of the read	09:36
15	sense amplifier. That would be a common design that	09:36
16	controls whether or not the line is being driven.	09:36

17	But even if those were combined, the	09:36
18	amplifier itself can be left on separately from the	09:36
19	question of whether or not it's driving.	09:36

20	Q. So in the typical design you have been	09:37
21	involved with, is the read sense amplifier left on	09:37
22	or off when there's no read operation?	09:37

23	MR. CHANDLER: Objection. Form.	09:37
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24	THE WITNESS: Both are well known in the	09:37
25	art. Again, it depends on a variety of tradeoffs.	09:37

1 BY MS. ZHONG: 09:37

2 Q. At the time of the invention in the 09:37

3 2009-2010 period, what was the typical practice? 09:37

4 MR. CHANDLER: Objection. Form. 09:37

5 THE WITNESS: I don't know that any practice 09:37

6 can be characterized as typical. I'm aware of 09:37

7 people doing it both ways. 09:37

8 BY MS. ZHONG: 09:37

9 Q. What about you? What is your typical 09:37

10 design? 09:37

11 A. I did not design memory chips in that time 09:37

12 frame. 09:37

13 Q. If both the read-write driver and the read 09:37

14 sense amplifiers are turned off, is a GIO_Rank0 line 09:38

15 in the electrical communication with rank -- let me 09:39

16 withdraw and ask. 09:39

17 Just focus on the write driver and the read 09:39

18 sense amplifier in box 100 that's connected to 09:39

19 Rank0. 09:39

20 A. Okay. 09:39

21 Q. Okay. If both the write driver and the read 09:39

22 sense amplifiers are turned off, they're disabled, 09:39

23 is a GIO_Rank0 line still in communication with the 09:39

24 Rank0 memory devices? 09:39

25 MR. CHANDLER: Objection. Form. 09:39

1 THE WITNESS: So in the first place, there's 09:39
2 nothing in Kim that would indicate there's any 09:39
3 reason to turn those both off. So that's a -- this 09:39
4 is a complete hypothetical. 09:40
5 But even so, would it be in electrical 09:40
6 communication with Rank0? The chip selects and the 09:40
7 control signals would still be going there. The 09:40
8 GIO_Rank0 signal would be communicating with -- 09:40
9 still be communicating with the write driver and the 09:40
10 read sense amplifier in 100. It never communicates 09:40
11 directly with Rank0. It always communicates with 09:40
12 the write driver and the read sense amplifier which 09:40
13 are part of the memory subsystem. 09:40
14 BY MS. ZHONG: 09:40
15 Q. Are they still communicating with the write 09:40
16 driver and read sense amplifier if they're turned 09:40
17 off? 09:40
18 A. Yes, they're still communicating. Sure. 09:40
19 Certainly with the write driver because it's the 09:40
20 output of the write driver that would be turned off, 09:41
21 not its input. 09:41
22 Now, if there was an intervening switch, as 09:41
23 I had suggested a person skilled in the art would 09:41
24 know how to do, then they would not be in 09:41
25 communication. But if there is no intervening 09:41

1 switch, then they are in electrical communication. 09:41

2 Q. Okay. So if you have a transmission gate 09:41

3 between the GIO_Rank0 and the write driver, is the 09:41

4 GIO_Rank0 in communication with that transmission 09:41

5 gate then? 09:41

6 MR. CHANDLER: Objection. Form. 09:41

7 THE WITNESS: No. It's -- a transmission 09:41

8 gate is a pass through. So, no, it's not. I mean 09:41

9 the point of the gate is to permit or disable 09:41

10 communications, right. I mean we have to use the 09:41

11 words in the way that a person of ordinary skill in 09:42

12 the art would use them and the way that they were 09:42

13 intended to be used in these documents. 09:42

14 BY MS. ZHONG: 09:42

15 Q. Can you explain what's the difference 09:42

16 between the GIO_Rank0's coupling to transmission 09:42

17 gate versus its coupling to write drivers which is 09:42

18 also a set of transistors? 09:42

19 MR. CHANDLER: Objection. Form. 09:42

20 THE WITNESS: Sure. The idea is that we 09:42

21 need to use these words in a way that a person of 09:42

22 ordinary skill in the art would. And the 09:42

23 transistors in the write driver are configured to 09:42

24 receive communications. Where the transistors in 09:42

25 the transmission gate are configured as a 09:42

1 pass-through switch to allow communications or 09:43
2 disallow communications, and that's the way they're 09:43
3 presented in the references that I have spoken about 09:43
4 in this matter and that's the way that a person of 09:43
5 ordinary skill would interpret them. 09:43
6 And as we discussed yesterday, none of this 09:43
7 is theoretical because the references that use the 09:43
8 transmission gate switches specifically tell us that 09:43
9 they're there to remove the electrical coupling 09:43
10 between the things on the two sides. 09:43
11 BY MS. ZHONG: 09:43
12 Q. So what you're saying, the difference is the 09:46
13 transmission gates are not designed to match the 09:46
14 data, they are only designed to either pass through 09:46
15 the data or block the data. Is that the difference? 09:46
16 MR. CHANDLER: Objection. Form. 09:46
17 THE WITNESS: That is not what I said. 09:46
18 BY MS. ZHONG: 09:46
19 Q. Then can you elaborate what really is the 09:46
20 difference? 09:46
21 MR. CHANDLER: Object to form. 09:46
22 BY MS. ZHONG: 09:46
23 Q. When you say the drivers are designed to 09:46
24 receive the communication, it is also designed on 09:46
25 the pathway to the memory cells; so in that sense it 09:46

1 is also designed to either allow the data to be 09:46
2 transmitted to the memory cells or designed to block 09:46
3 that data from being transmitted. 09:46
4 MR. CHANDLER: Objection. Form. 09:47
5 BY MS. ZHONG: 09:47
6 Q. So I'm trying to understand the difference 09:47
7 you are trying to draw. 09:47
8 A. There's a difference between the 09:47
9 configuration of transistors in a transmission gate 09:47
10 which is not processing the inputs and producing an 09:47
11 output, but simply connecting the two sides or not 09:47
12 connecting the two sides; and the input stage of a 09:47
13 write driver which is designed to receive an input 09:47
14 signal and then through logic produce an output 09:47
15 signal rather than simply pass electricity through 09:47
16 it. 09:47
17 Those are two different things and a person 09:47
18 of ordinary skill in the art would treat them 09:47
19 differently. It would treat one as receiving a 09:47
20 signal and another one as a pass-through switch. 09:47
21 And as I mentioned, the art that I've relied 09:47
22 on is extremely explicit in the way that it applies 09:48
23 the two different circuits in that the transmission 09:48
24 gate is used to allow or disallow electronic 09:48
25 communications and a receiving circuit like a write 09:48

1 driver does not have that function, and that's 09:48
2 consistent with the understanding of a person of 09:48
3 ordinary skill in the art at the time. 09:48
4 Q. Then can you please take a look at 09:48
5 Ruckerbauer Figure 5 which is Exhibit 1024, 5A, 09:48
6 Figure 5A of Ruckerbauer. 09:49
7 A. Okay. 09:49
8 Q. I think that yesterday we discussed the fact 09:49
9 that TSV112A and die 110A is physically coupled to 09:49
10 buffer 10a but is electrically decoupled from that 09:49
11 particular buffer. 09:49
12 Do you remember that discussion? 09:49
13 A. Yes. Again, I didn't rely on Figure 5A in 09:49
14 any way in my opinions. 09:49
15 Q. Okay. Understood. 09:49
16 So if Figure 10 the buffer is disabled by 09:49
17 signaling; right? Is there an electrical 09:50
18 communication between the TSV 112a and that buffer 09:50
19 circuit -- 09:50
20 MR. CHANDLER: Objection. 09:50
21 BY MS. ZHONG: 09:50
22 Q. -- given that the buffer is designed also to 09:50
23 receive an input signal and output signal if it is 09:50
24 enabled; right? 09:50
25 MR. CHANDLER: Objection. Form. 09:50

1 THE WITNESS: Well, I think we have to look 09:50
2 at that in the context of the disclosure where 09:50
3 Exhibit 1024 tells us specifically at column 10, 09:50
4 line 6 through 8, the dash lines are not used for an 09:51
5 electrical coupling. 09:51
6 BY MS. ZHONG: 09:51
7 Q. Understood. 09:51
8 But electrical communication doesn't come 09:51
9 from either Ruckerbauer or Riho or Kim, it comes 09:51
10 from the '060 patent. And you gave me your 09:51
11 interpretation of what that term means in the 09:51
12 context of the '060 patent. 09:51
13 I'm asking you to apply that understanding 09:51
14 to Ruckerbauer and you gave an explanation to me 09:51
15 just now as to why in the Kim circuit, even if the 09:51
16 write driver and the read sense amplifiers are 09:51
17 disabled, there would still be communication between 09:51
18 the GIO_Rank0 and the write driver and the read 09:51
19 sense amplifier. And I'm trying to understand why 09:51
20 that same rationale would not apply to Ruckerbauer 09:52
21 112a and 10a coupling. 09:52
22 A. Because Ruckerbauer doesn't give us the same 09:52
23 level of circuit detail and he tells us that there 09:52
24 is no electrical coupling. So when I take his 09:52
25 teaching as a whole, I would accept them. 09:52

1 Q. Well, it tells you that it's a buffer 09:52
2 circuit; right? 09:52
3 MR. CHANDLER: Objection. Form. 09:52
4 BY MS. ZHONG: 09:52
5 Q. What is a buffer circuit? 09:52
6 A. Where does it tell us that what is the 09:52
7 buffer circuit? 09:52
8 Q. Column 9, the last line, it says, 09:52
9 "Bi-directional buffers 10a or 10b." 09:52
10 A. Yes. But it doesn't tell us how it's 09:52
11 physically connected. 09:52
12 Q. What do you mean it doesn't tell you how 09:52
13 it's physically connected? 09:53
14 A. It tells us that there is a bi-directional 09:53
15 buffer but it doesn't -- and there is a physical 09:53
16 connection, but it doesn't give us more details 09:53
17 about that physical connection and it does tell us 09:53
18 that they're not electrically coupled. 09:53
19 Q. Why don't you take a look at Figure 3A. 09:53
20 Do you see the circle on the right -- 09:53
21 there's a dash with a circle on the right with 10a? 09:53
22 A. Okay. 09:53
23 Q. Does that give you the circuitry detail? 09:54
24 A. I'd have to do some more reading, but I can 09:54
25 certainly see that there are some intervening things 09:54

1 there that -- yeah, I would have to look at the 09:54
2 drawing. Although, again, I didn't rely on 3A for 09:54
3 my opinions so I'm not all that familiar with it. 09:54
4 Q. So your conclusion regarding the Figure 3A 09:54
5 is that there's a direct connection between the 09:54
6 write driver and the GIO_Rank0 line? 09:54
7 MR. CHANDLER: Objection. Form. 09:54
8 THE WITNESS: I haven't reached any 09:54
9 conclusions about Figure 3A. 09:54
10 BY MS. ZHONG: 09:54
11 Q. I'm talking about Kim. 09:54
12 MR. CHANDLER: Objection. Form. 09:54
13 THE WITNESS: Can I hear the question again? 09:54
14 There is no Figure 3A in Kim. 09:55
15 BY MS. ZHONG: 09:55
16 Q. Sorry. 09:55
17 So your conclusion regarding Kim's Figure 3 09:55
18 is it based on the fact that the GIO_Rank0 line is 09:55
19 connected directly with the write driver 11 and read 09:55
20 sense amplifier 12? 09:55
21 MR. CHANDLER: Objection. Form. 09:55
22 THE WITNESS: I don't understand the 09:55
23 question. 09:55
24 BY MS. ZHONG: 09:55
25 Q. Didn't you conclude that even if the write 09:55

1 driver 11 and read sense amplifier 12 are turned 09:55
2 off, there would still be electrical communication 09:55
3 between the GIO_Rank0 and Rank0 because, in your 09:55
4 opinion, there would still be signal going into the 09:55
5 write driver and the read sense amplifier -- going 09:55
6 into the write driver, even if it's disabled or 09:56
7 turned off? 09:56

8 A. So you asked me to make a number of 09:56
9 hypothetical assumptions there that are not in Kim, 09:56
10 and based on the Kim disclosure that doesn't show 09:56
11 any intervening circuits or any further details, 09:56
12 yes, that would be my conclusion is that Kim teaches 09:56
13 that there is an electrical coupling there, and 09:56
14 adding some hypothetical assumptions about things 09:56
15 being turned on and off would not in my mind 09:56
16 overcome that teaching. 09:56

17 Q. Okay. So your conclusion is based on the 09:56
18 fact that there are no intervening circuit elements 09:56
19 between the write driver and the GIO_Rank0; is that 09:57
20 correct? 09:57

21 MR. CHANDLER: Objection. Form. 09:57

22 THE WITNESS: No. My conclusion is based on 09:57
23 the teachings of Kim as a whole which teaches that 09:57
24 the intent is that the write selecting unit 09:57
25 communicates electrically over GIO_Rank0 with the 09:57

1 write driver and the read sense amplifier. 09:57
2 BY MS. ZHONG: 09:57
3 Q. And if the write driver includes a 09:57
4 transmission gate that's not shown, does your 09:57
5 conclusion still remain the same? 09:57
6 A. I don't have any opinion on that. Again, 09:57
7 that's an incomplete hypothetical and it's not 09:57
8 something that I considered. 09:57
9 Q. Okay. And does your conclusion change if 09:57
10 Kim's write driver or read sense amplifier includes 09:57
11 a transmission gate that can be switched off? 09:58
12 A. Again, I don't have an opinion on that. I 09:58
13 think that's an incomplete hypothetical. 09:58
14 Q. Okay. And would your conclusions change if 09:58
15 the write driver and the read sense amplifier 09:58
16 includes a transmission gate and the transmission 09:58
17 gates are disabled as in Riho? 09:58
18 A. If it were done as in Riho, then when Riho's 09:58
19 transmission gates are turned off, they stop 09:58
20 electrical communication. So that would change my 09:59
21 opinion, yes. 09:59
22 I mean it would be a different opinion but 09:59
23 not a changed opinion. But that's a different 09:59
24 combined circuit, it's a modified circuit, and in 09:59
25 that case when Riho's transmission gates are on, 09:59

1	there would be electrical communication; and when	09:59
2	Riho's transmission gates are off, there would not	09:59
3	be electrical communication.	09:59
4	MS. ZHONG: Give me a second. Let me just	09:59
5	turn off the phone.	09:59
6	BY MS. ZHONG:	10:00
7	Q. Does Kim provide any circuit details	10:00
8	regarding what --	10:00
9	(Clarification requested by Reporter.)	10:00
10	BY MS. ZHONG:	10:00
11	Q. Does Kim provide any circuit level detail as	10:00
12	to any of the blocks shown in Figure 3?	10:00
13	A. No. Those are all common blocks that a	10:00
14	person of ordinary skill in the art would know how	10:00
15	to implement.	10:00
16	MS. ZHONG: Okay. Why don't we take a	10:00
17	10 minute break.	10:00
18	MR. CHANDLER: Okay.	10:00
19	(Off the record.)	10:00
20	MS. ZHONG: Thank you very much,	10:19
21	Dr. Wolfe, and I will pass the witness.	10:19
22	MR. CHANDLER: Let's take a break. Maybe	10:19
23	15 minutes.	10:19
24	MS. ZHONG: Okay.	10:19
25	(Off the record.)	10:19

1 MR. CHANDLER: Thank you. I have no 10:31
2 questions so that will conclude the deposition. 10:31
3 We would like an opportunity to review the 10:31
4 transcript and make corrections if needed, and to 10:31
5 that end we would request a final version of the 10:31
6 transcript by Thursday, July 6th, on our end with 10:32
7 the understanding that the patent owner may want a 10:32
8 copy earlier than that. But we only need it by 10:32
9 Thursday July 6th. 10:32
10 MS. ZHONG: Thursday the July 6th is fine 10:32
11 with us as well. 10:32
12 DEPOSITION REPORTER: And, Counsel, do you 10:32
13 both want a rough transcript of this morning? 10:32
14 MS. ZHONG: Yes, please. 10:32
15 MR. CHANDLER: Yes. 10:32
16 DEPOSITION REPORTER: Okay. Thank you very 10:32
17 much. We are off the record. 10:32
18 (Ending time: 10:32 a.m.) 10:32
19
20
21
22
23
24
25

1 I, ANDREW WOLFE, do hereby declare under
2 penalty of perjury that I have read the foregoing
3 transcript; that I have made corrections as appear
4 noted, in ink, initialed by me, or attached hereto; that
5 my testimony as contained herein, as corrected, is true
6 and correct.

7 EXECUTED this ____ day of _____,
8 2023, at _____, - _____.
9 (City) (State)

10
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13 _____
14 ANDREW WOLFE
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1 I, JANIS JENNINGS, CSR No. 3942, Certified
2 Shorthand Reporter, certify:

3 That the foregoing proceedings were taken
4 before me at the time and place therein set forth, at
5 which time the witness was duly sworn by me;

6 That the testimony of the witness, the
7 questions propounded, and all objections and statements
8 made at the time of the examination were recorded
9 stenographically by me and were thereafter transcribed;

10 That the foregoing pages contain a full, true
11 and accurate record of all proceedings and testimony.

12 Pursuant to F.R.C.P. 30(e)(2) before
13 completion of the proceedings, review of the transcript
14 [X] was [] was not requested.

15 I further certify that I am not a relative or
16 employee of any attorney of the parties, nor financially
17 interested in the action.

18 I declare under penalty of perjury under the
19 laws of California that the foregoing is true and
20 correct.

21 Dated this 5th day of July 2023.

22
23 

24 JANIS JENNINGS, CSR NO. 3942

25 CLR, CCRR

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-01427

Patent 9,318,160 B2

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (JUNE 27–28, 2023)**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-01428

Patent 8,787,060 B2

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (JUNE 27–28, 2023)**

I, ANDREW WOLFE, have read the transcript of my deposition taken on June 27–28, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
5:7	<u>Ranjan</u>	<u>Rajan</u>	Typographical error
10:16–:18	It is a model used to illustrate what the effective <u>resistant capacitive</u> load would be of that portion of the through silicon via.	It is a model used to illustrate what the effective <u>resistive and capacitive</u> load would be of that portion of the through silicon via.	Typographical error
13:7	each portion of the <u>PSD</u>	each portion of the <u>TSV</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
15:13--:21	A. The most common one that I use in this kind of a context is that it is simply an interconnection of electronic components, but there are some times in some context where people use the word "circuit" to mean something that has a complete electrical path. <u>And that --</u> <u>Q. Okay.</u> <u>A. -- the</u> common dictionary definition and these switches don't meet that definition.	A. The most common one that I use in this kind of a context is that it is simply an interconnection of electronic components, but there are some times in some context where people use the word "circuit" to mean something that has a complete electrical path. <u>And that --</u> <u>Q. Okay.</u> <u>A. -- is the</u> common dictionary definition and these switches don't meet that definition.	Typographical error
17:8--:12	Q. Does the driver -- does the driver in the L1R1C2 equivalent circuit impose a load on the TSV? THE WITNESS: It's not a normal way we would phrase that <u>discussion.</u>	Q. Does the driver -- does the driver in the L1R1C2 equivalent circuit impose a load on the TSV? THE WITNESS: It's not a normal way we would phrase that <u>question.</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
19:18–:21	THE WITNESS: What do you mean by turned off? Q. <u>Try to save it</u> , for example.	THE WITNESS: What do you mean by turned off? Q. <u>Tri-stated</u> , for example.	Typographical error
29:8–:14	He has made the design decision to <u>not enact</u> D14's driver circuits or D14's memory array at all to TSV 715 since that would offer no benefit and would needlessly slow down the circuit and consume more power. Q. Okay. So why can't D15 and D14 connect to both TSV 715 and <u>offer it</u> simultaneously?	He has made the design decision to <u>not connect</u> D14's driver circuits or D14's memory array at all to TSV 715 since that would offer no benefit and would needlessly slow down the circuit and consume more power. Q. Okay. So why can't D15 and D14 connect to both TSV 715 and <u>operate it</u> simultaneously?	Typographical errors
31:11–:15	But Riho treats D14 and D15 as two parts of the same <u>data work</u> . Each one supplies 32 bits. They are operated at the same time and <u>each of one</u> requires 32 wires to communicate those 32 bits. That's its mode of operation.	But Riho treats D14 and D15 as two parts of the same <u>data word</u> . Each one supplies 32 bits. They are operated at the same time and <u>each one</u> requires 32 wires to communicate those 32 bits. That's its mode of operation.	Typographical errors

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
34:22–35:1	So if the dies belong to the same rank, what would happen if a read command is sent to the <u>stack</u> array? Does that mean all eight of the dies in the same rank is going to output data simultaneously?	So if the dies belong to the same rank, what would happen if a read command is sent to the <u>stacked</u> array? Does that mean all eight of the dies in the same rank is going to output data simultaneously?	Typographical error
36:21–:24	So you think "rank" can refer to a set of <u>family</u> devices that read or write less than a full bit width of the memory module in response to command signals?	So you think "rank" can refer to a set of <u>DRAM</u> devices that read or write less than a full bit width of the memory module in response to command signals?	Typographical error
38:11–:14	If the 8 dies normally operate together and output 64 bits, the fact that there is an additional operation in which only one operates does not make the <u>8s</u> stop being a rank.	If the 8 dies normally operate together and output 64 bits, the fact that there is an additional operation in which only one operates does not make the <u>8</u> stop being a rank.	Typographical error
47:24–48:1	they have a very tiny capacitive load and don't impact the <u>capacitives</u> that you are trying to measure	they have a very tiny capacitive load and don't impact the <u>capacitance</u> that you are trying to measure	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
50:9–:16	Q. Okay. And each of the circuits would <u>decide</u> appropriately in order to accommodate the expected maximum load coming from the driver circuit; is that right? THE WITNESS: Not necessarily. They would be sized appropriately to support the <u>designer</u> current.	Q. Okay. And each of the circuits would <u>be sized</u> appropriately in order to accommodate the expected maximum load coming from the driver circuit; is that right? THE WITNESS: Not necessarily. They would be sized appropriately to support the <u>desired</u> current.	Typographical errors
53:4	techniques like <u>find an</u> element analysis	techniques like <u>finite</u> element analysis	Typographical error
57:19–:21	Let's assume that Rank2 is connect -- has <u>audio probe</u> signals and the wires and are connected to the GIO_Rank0; right?	Let's assume that Rank2 is connect -- has <u>appropriate</u> signals and the wires and are connected to the GIO_Rank0; right?	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
59:4–:8	You would need to provide them with documentation of the components that they are given <u>so</u> the various memory components, the various controller components, or you would give them the freedom to redesign them.	You would need to provide them with documentation of the components that they are given <u>for</u> the various memory components, the various controller components, or you would give them the freedom to redesign them.	Typographical error
69:9–:14	are you aware of any NAND memory systems in which the NAND memories are <u>all 9 and ranked</u> and one NAND -- and the memory -- the NAND memory in Rank1 would perform a read operation after a write operation on Rank1 is performed?	are you aware of any NAND memory systems in which the NAND memories are <u>organized in ranks</u> and one NAND -- and the memory -- the NAND memory in Rank1 would perform a read operation after a write operation on Rank1 is performed?	Typographical error (see 69:21)
86:14–:15	We do that all the time. We tie the data output <u>chips</u> from multiple chips together.	We do that all the time. We tie the data output <u>pins</u> from multiple chips together.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
88:2--:8	THE WITNESS: No. I have not considered a case where 100 and 200 belong to the same rank. Q. Do you think that the system would work if 100 and 200 are <u>not</u> the same physical rank? A. I think a person of ordinary skill could make that system work	THE WITNESS: No. I have not considered a case where 100 and 200 belong to the same rank. Q. Do you think that the system would work if 100 and 200 are <u>in</u> the same physical rank? A. I think a person of ordinary skill could make that system work	Typographical error
90:5--:9	Q. And so you are grouping the two bottom dies, 417C and <u>417B</u>, as one group and the two top dies, 417A and the 417B, as another group; correct? A. That would be one embodiment that would be obvious, yes.	Q. And so you are grouping the two bottom dies, 417C and <u>417D</u>, as one group and the two top dies, 417A and the 417B, as another group; correct? A. That would be one embodiment that would be obvious, yes.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
90:19–:21 91:23–92:1	In this implementation, you would have two ranks, one rank would be 417A and 417C, and the other rank would be 417B and 417D. Q. What did you rely on? Did you rely on 417A and 417C be in one rank, and 417B and 417D in another rank? A. Yes.	[see note]	No change, but this was further clarified at 92:5–:14.
104:5–:8	I'm reading this out of context, but it seems to indicate that one way of achieving connectivity is to use an <u>enabled</u> signal.	I'm reading this out of context, but it seems to indicate that one way of achieving connectivity is to use an <u>enable</u> signal.	Typographical error
107:24	Riho is the one with the transmission <u>gauge</u> .	Riho is the one with the transmission <u>gates</u> .	Typographical error
122:17–:19	Ruckerbauer told us that the solid line <u>in</u> <u>is</u> that they are connected in his design.	Ruckerbauer told us that the solid line <u>means</u> that they are connected in his design.	Typographical error
126:9–:11	Wyman is suggesting to connect the TSVs to different <u>paths</u> of the circuits Figure 5 - - in Figure 5	Wyman is suggesting to connect the TSVs to different <u>taps</u> of the circuits Figure 5 - - in Figure 5	Typographical error (see 127:3–:9)

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
127:24– 128:1	But the circuit is the same. If the circuit is through the driver 500, <u>where's</u> the four drive circuits but with different taps; correct?	But the circuit is the same. If the circuit is through the driver 500, <u>there's</u> the four drive circuits but with different taps; correct?	Typographical error
128:13–:21	One, the suggestions also include taps T2 and taps T3 for the particular example in Figure 8, but also the <u>taps</u> that I identified previously explains that Figure 5 can be embodied or implemented in many different ways, including one driver supporting multiple taps, one driver supporting one tap, or multiple drivers supporting each tap. So all of those are contemplated by Wyman.	One, the suggestions also include taps T2 and taps T3 for the particular example in Figure 8, but also the <u>passage</u> that I identified previously explains that Figure 5 can be embodied or implemented in many different ways, including one driver supporting multiple taps, one driver supporting one tap, or multiple drivers supporting each tap. So all of those are contemplated by Wyman.	Typographical error (see 127:15–:22)

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
129:15–:19	But the circuit size for the 500, that is set; right? The silicon -- the space it occupies on the silicon, that is the same regardless of which <u>path</u> you happen to be using or which of the multiple combination taps you will be using; right?	But the circuit size for the 500, that is set; right? The silicon -- the space it occupies on the silicon, that is the same regardless of which <u>tap</u> you happen to be using or which of the multiple combination taps you will be using; right?	Typographical error (see 127:3–:9)
136:22	<u>Weiman</u>	<u>Wyman</u>	Typographical error
138:18–:20	So Claim 1 of the '160 patent says a first data conduit including first <u>driver</u> , each having a first driver size.	So Claim 1 of the '160 patent says a first data conduit including first <u>drivers</u> , each having a first driver size.	Typographical error
139:4–:5	Are you aware of any designs in which the driver size are the same regardless of the <u>mode</u> ?	Are you aware of any designs in which the driver size are the same regardless of the <u>load</u> ?	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
140:5–:9	So if the loads on each of the TSVs are die interconnects, <u>are</u> the designs the same but due to manufacturing variances there are differences, would you design a drive circuit with different driver sizes or the same driver size?	So if the loads on each of the TSVs are die interconnects, <u>and</u> the designs <u>are</u> the same but due to manufacturing variances there are differences, would you design a drive circuit with different driver sizes or the same driver size?	Typographical error
158:12–:20	The logic LSI chip, at the proper point in time, would drive a data value, a 0 or a 1, into TSV 715, that current would change the voltage in the entire net from a 0 to a 1, and because switch sa is on, that net would include the input receiver that is on D15 that corresponds to this particular bit, and that, again, for most memory <u>plates</u> would then buffer that signal and drive it into some type of a register or flip-flop.	The logic LSI chip, at the proper point in time, would drive a data value, a 0 or a 1, into TSV 715, that current would change the voltage in the entire net from a 0 to a 1, and because switch sa is on, that net would include the input receiver that is on D15 that corresponds to this particular bit, and that, again, for most memory <u>states</u> would then buffer that signal and drive it into some type of a register or flip-flop.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
169:3–:5	In SDRAM D15, <u>and</u> the electrical path between TSV 715 and the receiver <u>circuit is only intersected</u> by the switch circuit sa; correct?	In SDRAM D15, <u>in</u> the electrical path between TSV 715 and the receiver <u>circuit, it's only separated</u> by the switch circuit sa; correct?	Typographical errors
171:12–:16	So the time that it takes for you to charge up the receiver circuit, <u>where</u> is the charge that is coming off TSV 715 in D15 that would only depend on the current that the transmission gate in sa can pass; is that correct?	So the time that it takes for you to charge up the receiver circuit, <u>there</u> is the charge that is coming off TSV 715 in D15 that would only depend on the current that the transmission gate in sa can pass; is that correct?	Typographical error
178:8–:10	So Riho tells us that the capacitive load of sa and sb on D14 in TSV 715 is not <u>insignificant</u> .	So Riho tells us that the capacitive load of sa and sb on D14 in TSV 715 is not <u>significant</u> .	Typographical error
181:2–:8	is it <u>an</u> electrical communication?....It's <u>an</u> electrical communication when it's on, and it is not <u>an</u> electrical communication when it's off.	is it <u>in</u> electrical communication?....It's <u>in</u> electrical communication when it's on, and it is not <u>in</u> electrical communication when it's off.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
197:13--:16	What I want to understand is when you drive data up to TSV 08, it seems that data are likely -- <u>ae</u> only going to be written into either D0 or D8 at the bottom.	What I want to understand is when you drive data up to TSV 08, it seems that data are likely -- <u>are</u> only going to be written into either D0 or D8 at the bottom.	Typographical error
201:16	They don't need to be switched off, but they need to be <u>not driving in the same way</u> as any four rank -- or any four rank system with two buses that would be known in the prior art.	They don't need to be switched off, but they need to be <u>not driving, in the same way</u> as any four rank -- or any four rank system with two buses that would be known in the prior art.	Typographical error
205:1	write <u>enabled</u>	write <u>enable</u>	Typographical error
207:15--:17	Typically the write driver to the array would only be turned off <u>using and</u> during a page refresh operation.	Typically the write driver to the array would only be turned off <u>usually</u> during a page refresh operation.	Typographical error
208:16--:17	I mean it depends how you're <u>driving</u> the write driver.	I mean it depends how you're <u>defining</u> the write driver.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
218:12-:15	So what you're saying, the difference is the transmission gates are not designed to <u>match</u> the data, they are only designed to either pass through the data or block the data. Is that the difference?	So what you're saying, the difference is the transmission gates are not designed to <u>catch</u> the data, they are only designed to either pass through the data or block the data. Is that the difference?	Typographical error

I hereby certify that the transcript of my deposition on June 27–28, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: July 26, 2023



 Andrew Wolfe