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Respectfully submitted,

By 

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PTO/SB/14 (06-07)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	R-RA0764.P.US
	Application Number	
Title of Invention	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL	

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Title of the Invention	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL		
Attorney Docket Number	R-RA0764.P.US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
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Prior Application Status	Pending		Remove
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First Name	Anthony P.	Last Name	Jones	Registration Number	59521

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PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

Inventors: Ian Shaeffer and Thomas J. Giovannini

RELATED CASES

[0001] This application claims priority to U.S. Provisional Application No. 61/366,806, Attorney Docket Number R-RA0764.Prov1.US, entitled "Protocol Including a Command-Specified Timing Reference Signal," by inventors Ian Shaeffer and Thomas J. Giovannini, filed 22 July 2010, the contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present embodiments generally relate to techniques for communicating data between integrated circuit devices. More specifically, the present embodiments relate to a method, apparatus and protocol for high speed signaling between a memory device and a memory controller.

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BRIEF DESCRIPTION OF THE FIGURES

[0003] FIG. 1A presents a block diagram illustrating a system which performs timing updates between a memory controller and at least one memory device.

[0004] FIG. 1B presents a block diagram illustrating an exemplary system which performs fast timing updates between a memory controller and a set of memory ranks.

[0005] FIG. 2 presents a simplified timing diagram illustrating preamble-based fast timing updates between a memory controller and a rank.

[0006] FIG. 3 presents a timing diagram illustrating preamble-based fast timing updates during read memory transactions on multiple ranks.

[0007] FIG. 4A presents a timing diagram illustrating preamble-based fast timing updates during both write and read memory transactions on multiple ranks.

[0008] FIG. 4B presents a timing diagram illustrating preamble-based fast timing updates during read memory transactions using a dedicated signaling resource for TRS/EDC modes.

[0009] FIG. 5 presents a block diagram illustrating an embodiment of a memory system, which includes at least one memory controller and one or more memory devices.

DETAILED DESCRIPTION

[0010] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular example application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention.

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Thus, the present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the claims.

[0011] For computer systems, such as servers which contain numerous ranks of memory, idle power may be an issue. At any given time at most one rank is actively accessed, while all other ranks are idle but still consuming idle power. In some servers, this idle power can exceed active power if there are a large number of idle ranks. In such systems, power can be saved by moving timing control components, such as phase-locked loop (PLL) or delay-locked loop (DLL), from the ranks to the memory controller (which typically controls multiple ranks). In such designs, timing information can be provided to the memory controller from individual ranks to make timing updates to compensate for the noise and drift of the ranks. Such timing information can be conveyed via data signaling resources, for example, as a timing preamble that precedes a data burst received by the controller via the data signaling resources. Other signaling resources that are common to a given rank of memory devices and the controller may also be used to transfer the timing information between the rank and the controller.

[0012] Timing information received by the memory controller for a given rank is available when the rank is actively accessed (e.g., through a read or write command). By utilizing certain common timing reference/data resources for multiple ranks, when accessing a given rank, no timing information may be received from other ranks in the memory system. During this time, supply voltage and temperature may drift, which can cause the delay of the circuitry in the individual ranks to change. Moreover, high-frequency power supply noise can also shift the timing of the ranks. Hence, if a rank has not been accessed for some period of time, it is necessary to first perform a timing update for the rank before the rank can be accessed.

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[0013] The following description presents various exemplary methods, protocols and apparatus for performing timing updates for memory transactions between a memory controller and a memory device (e.g., in a multi-rank system). In some embodiments, at the beginning of accesses to memory devices in a memory rank (or a "rank"), for example, after the rank has been idle for a time period, the memory controller transmits, to a memory device, a read command containing information which specifies whether the memory device is to output a timing reference signal ("TRS") prior to outputting of data in response to the read command. In an embodiment, the information is a digital bit or a special flag and is referred to as a preamble request flag. When the memory device, upon condition that the information specifies a TRS, outputs the TRS to the controller, the controller will receive the TRS before receiving a first bit of the subsequent data. The controller, upon receipt of the TRS, can use the TRS for the sampling of the data. For example, the TRS is used to sample the data or, as is described in more detail below, the controller can derive phase information from the TRS to optimize a sampling point for the data at the input sampler of the controller device. For example, the controller can update the phase of an internal sampling clock based on phase information derived from the TRS, where the internal sampling clock is an internal timing reference provided to an input sampler, in the controller, used to sample incoming read data output by the memory device.

[0014] In an embodiment, the TRS is a calibration preamble and in response to the information specifying a calibration preamble, the memory device transmits the calibration preamble from the memory device to the memory controller. The memory controller subsequently uses the calibration preamble to adjust receive timing for sampling, at the memory controller, the data output from the memory device. The receive timing at the memory controller may be adjusted to compensate for low-frequency timing drifts and timing jitter.

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[0015] In some embodiments, the TRS has a burst length which is determined in part by the duration of an idle period for the rank. The burst length of the timing reference signal may be set to be the same as the burst length of the data (output in response to the read command). The TRS, in an embodiment, is conveyed from the memory device, to the memory controller via a signaling resource (i.e., signal traces, pins etc.,) that is also used to transfer error detection and correction information (EDC). Over the signaling resource, the timing reference signal may be conveyed in a time shifted manner relative to the data burst being transferred over a separate signaling resource.

[0016] In some embodiments, the calibration preamble is only requested when the first transaction to a newly accessed rank is a read access. In the discussion below, the terms "timing updates" and "phase updates" are used interchangeably, and the terms "timing reference signal (TRS)", "calibration preamble" and "preamble" may also be considered as being used interchangeably. In addition, "ranks" are used to refer to 1 or more memory devices which are accessed and (collectively in the case of more than 1 memory device) transfers data for a given data access operation.

[0017] FIG. 1A presents a block diagram illustrating a system 100 which performs timing updates between a memory controller 102 and a set of memory ranks (such as DRAM ranks) 104. Memory controller 102 includes a PLL circuit 106 and an edge tracking circuit 108. Memory ranks 104 include two or more ranks, such as a rank 110. In an embodiment, each rank 110 includes one or more memory devices 111 and a clock distribution circuit 112, and each memory device 111 is a single chip having a memory core 113.

[0018] During a memory access to an active rank 110, memory controller 102 transmits command/address (C/A) 114 and command (CA) clock 116 to rank 110 over a chip-to-chip interconnect 118. Memory controller 102 can also

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transmit data 120 and data clock 122 to rank 110 over chip-to-chip interconnect118. In some embodiments, data clock 122 is a full-bit-rate differential data clock (DCLK) for the data interface on rank 110, which provides a clock edge per bit, whereas CA clock 116 is a differential clock operating at one-quarter the rate of data clock 122, which is used for timing on the CA interface and for memory core 111. Note that the memory device CA input samplers (not shown) on rank 110 are directly clocked by CA clock 116, while write data 120 is directly clocked on rank 110 by data clock 122.

[0019] Memory rank 110 also receives data 120 and data clock 122, and distributes data clock 122 through clock distribution circuit 112 to both an input/output (I/O) data slicer 124 and an error detection and correction (EDC) circuit 126. I/O data slicer 124 includes a transmitter circuit to transmit data 128 and EDC circuit 126 includes a transmitter circuit to transmit an EDC signal 130 back to memory controller 102. Note that both data 128 and EDC signal 130 contain phase information regarding the memory transactions taking place on rank 110. In some embodiments, EDC signal 130 contains CRC codes, which are interspersed with a toggling idle pattern to achieve a minimum or predetermined number of EDC signal edge transitions (edge density).

[0020] Edge tracking circuit 108 on memory controller 102 receives both data 128 and EDC signal 130, and subsequently uses clock-data-recovery (CDR)-like circuits to extract phase information from the received data for rank 110. This phase information is then sent to PLL circuit 106, which uses the phase information to perform phase updates for data clock 122 to compensate for timing drift and timing jitter for rank 110. PLL circuit 106 also updates CA clock 116 based on the same phase information from edge tracking circuit 108.

[0021] In an embodiment, to facilitate the memory controller switching between servicing read operations directed to different ranks, phase information

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for each individual rank can be stored at the memory controller. For example, in the embodiment illustrated in FIG. 1A, memory controller 102 includes a rank-tracking circuit 132 coupled to edge-tracking circuit 108, which stores phase information for each of the memory ranks 104. Hence, the phase information for a new rank to be accessed is first loaded into a phase mixer after a rank switch occurs. At the same time, the most recently updated phase information for a previously accessed rank is stored into rank-tracking circuit 132.

[0022] When a new rank is accessed after an idle period for the rank, data and an EDC signal eventually become available from the new rank. It is possible to use the EDC signal to perform timing updates for the new rank using the above-described timing update loop in FIG. 1A. However, this timing update loop involves feedback and a long path delay which may not be sufficiently fast to track high-frequency timing jitter, such as power supply induced jitter (PSIJ). Moreover, the EDC signal only captures timing errors for preceding transactions, and therefore trails behind the data used to produce the EDC signal. Hence, during read transactions, the memory controller only receives the EDC signal after read data has already been received without associated clock phase updates.

[0023] Some of the presently described techniques enable rapid phase updates for a rank which is being accessed for the first time after an idle period. This is accomplished by initially transmitting a timing reference signal (TRS) from the rank to the memory controller before the first read data packet and the corresponding EDC packet are transmitted. In some embodiments, the timing reference signal may be added to the head of the first available read data burst being transmitted from a newly accessed rank to the memory controller. Upon receiving the TRS, the memory controller may perform fast phase updates within the duration of the TRS to correct a substantial portion of the timing drift and

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jitter for the rank. In some embodiments, this TRS comprises a toggling pattern which provides a predetermined number of timing edges.

[0024] FIG. 1B presents an example embodiment illustrating system 129 which performs fast timing updates between a memory controller 102 and a set of memory ranks 104. As illustrated in FIG. 1B, a fast edge tracking circuit 136 is included in memory controller 102's clock architecture to provide fast phase updates within a received calibration preamble. For example, assume fast edge tracking circuit 136 receives data 128 from the new rank being accessed. If data 128 contains a calibration preamble, fast edge tracking circuit 136 uses the toggling pattern in the calibration preamble to make fast phase updates to a data clock used to capture the actual read data in data 128 following the calibration preamble. In this embodiment, after the initial updates based on the calibration preamble have been made, edge tracking circuit 108 performs subsequent phase updates during data transactions following the calibration preamble. In some embodiments, fast edge tracking circuit 136 operates at a significantly faster clock rate than edge tracking circuit 108, which allows the phase update to complete within a preamble duration, before the actual read data arrives at the memory controller. Furthermore, to ensure their independent operation without interfering with each other, fast edge tracking circuit 136 and edge tracking circuit 108 can be gated by different control signals, namely fast lock enable 138 and EDC lock enable 140 in FIG. 1B.

[0025] The additional phase adjustment capability provided by fast edge tracking circuit 136 in the clock architecture of memory controller 102 facilitates additional noise tracking and can relax the design requirements for the clock distribution circuit 112 on memory ranks 104. Moreover, fast edge tracking circuit 136 can have a shorter adjustment range for accommodating the timing drift expected from the idle period between accesses to a given rank. This amount

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of drift may also be bounded by specifying a maximum allowable idle period between accesses to a given rank.

[0026] FIG. 2 presents a simplified timing diagram illustrating preamble-based fast timing updates between a memory controller and a rank in accordance with an embodiment. As illustrated in FIG. 2, a data signal DQ[n] 202 comprises the beginning of a data pattern received at a memory controller from a new rank [n] being accessed after an idle period. DQ[n] 202 begins with a calibration preamble 204 comprising a toggling pattern which contains a predetermined number of edges. Preamble 204 is immediately followed by a data burst 206 which has a predetermined burst length for example, 4, 8, 16, 32 bits or 64 bits. An EDC signal 208 associated with data burst 206 is also received by the memory controller from the same rank. Note that EDC signal 208 trails both preamble 204 and data burst 206.

[0027] EDC signal 208 contains EDC codes 210 interspersed with toggling idle patterns 212 to achieve a minimum edge density (i.e., a predetermined number of signal transitions during a given time interval) in EDC signal 208. EDC codes 210 can include any type of EDC code, such as a CRC code. Note that EDC codes 210 can be of different lengths and can occur in different orders with the idle patterns or without the idle patterns at all. While the edge density in EDC codes 210 can be guaranteed by using the idle patterns, other techniques (e.g., various coding styles on top of the EDC codes) can be used to accomplish the same. In some embodiments, no special technique is used in EDC codes 210, and the system relies on probability to provide enough edges. .

[0028] Upon receiving DQ[n] 202, the memory controller uses preamble 204 to perform a fast phase update without using a time-consuming feedback mechanism. A fast lock enable signal 214, which has an enable window 216 substantially time-aligned with preamble 204, is used to gate the fast updates at a

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fast clock rate. After completing the fast phase updates, normal phase updates can be performed based on EDC signal 208. More specifically, an EDC lock enable 218 which has an enable window 220 substantially time-aligned with EDC code 210 is used to gate the normal phase updates at a normal slow clock rate which may involve a feedback loop. In some embodiments, however, the enable window 216 of fast lock enable 214 may be extended (as shown by the dotted line) to the beginning of enable window 220 in EDC lock enable 218. In this embodiment, the initial phase updates (before the EDC-based update) include not only the fast-lock adjustments from preamble 204, but also some phase adjustments based on the first portion of data burst 206.

[0029] FIG. 3 presents a timing diagram illustrating preamble-based fast timing updates during read memory transactions on multiple ranks according to an embodiment. As illustrated in FIG. 3, a memory controller issues memory commands (CA), which include two consecutive read commands RD[A0] and RD[A1] directed to a rank 0. Note that RD[A0] is the first memory access request issued to rank 0 after an idle period for rank 0 transpires. In response, a memory device in rank 0 prepends a calibration preamble 302 to read data Q[A0].

[0030] After the controller issues read command RD[A1], a rank switch occurs from rank 0 to idle rank 1. More specifically, immediately after issuing a precharge command PRE to close off the access to rank 0, two consecutive read commands RD[A2] and RD[A3] are issued to rank 1, wherein RD[A2] is the first memory access request on rank 1 after the idle period on rank 1. In response, rank 1 prepends a calibration preamble to read data Q[A2].

[0031] Some embodiments use a "read with preamble" command to support timing updates in the controller clock architecture when the memory controller accesses a rank of memory that has not been accessed for some period of time. More specifically, the memory controller is configured to identify a

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condition when a rank is to be accessed for the first time after an idle period, and the first memory access to the rank is a read. For example, this condition occurs immediately before RD[A0] and RD[A2] in FIG. 3. When this condition is identified, the memory controller issues the read command containing a preamble request flag to the rank. Upon receiving the read command at the rank, the preamble request flag causes the rank to send a calibration preamble before transmitting the requested read data to the memory controller. The memory controller then uses the calibration preamble to update the read clock phase at the memory controller.

[0032] In one embodiment, the preamble request flag is a 1-bit field in the read command. For example, a '1' provided in the 1-bit field provides for a "read with preamble" command, and a '0' provided in the 1-bit field provides for a "read without preamble" command. In other embodiments, the preamble request flag is encoded in a multi-bit field in the read command and could be combined with other command variants of the read command, for example, a read with/without auto precharge bit that specifies whether sense amplifiers of the memory device should be automatically precharged following the read operation. Another command variant of the "read with preamble" command is a "preamble without data" command that specifies that the memory device output a timing reference signal to the controller device with no succeeding data burst being accessed during the transaction with memory. This command option provides that after a predetermined idle period to an idle rank, the memory controller flexibly has the option to schedule a receive timing update to that idle rank by specifying that a memory device of the rank transmit a timing reference signal with no accompanying data burst.

[0033] Generally, the TRS is predetermined to provide enough edges to perform the required timing updates before the read data is captured. The length

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of the TRS may be specified by a field in the read with preamble command or "statically" programmed to accommodate a given memory controller architecture and can be stored in registers on target memory devices of a rank and/or the memory controller. For example, some preamble burst lengths can be programmed to be 4, 8, 16, and 32 clock cycles. In one embodiment, two or more length values are programmed in registers on the targeted memory device and a field in the command selects from the two or more length values.

[0034] In some embodiments, a preamble request command includes a command field (one or more bits long) specifying the length of the TRS to allow the memory controller to specify the length of the preamble as needed based on various factors, such as the amount of elapsed time since the last rank access. In some embodiments, the memory controller can determine the length of the preamble based at least in part on the idle time of a given rank since the last access (i.e., an idle time-based length). It selects a shorter length for a shorter idle time and a longer length for a longer idle time. For example, the controller can use a one-bit command field to determine whether to send a long (e.g., 32 cycles) preamble or a short (e.g., 16 cycles) preamble. In another embodiment, the controller can simply use a bit of the command field to specify whether to perform a fine adjustment with a long preamble, or a fast adjustment with a short preamble based on run-time factors associated with the operation of the memory system.

[0035] The calibration preamble may be only needed for the first read transaction after an idle period; once the timing updates have been completed, any further transactions to the active rank will use EDC edges to maintain phase updates. Note that if the first memory transaction to a previously idle rank is a write transaction, the read timing can be automatically updated through the edges returned on the EDC line. We describe this situation in more detail below.

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[0036] FIG. 4A presents a timing diagram illustrating preamble-based fast timing updates during both write and read memory transactions on multiple ranks. As illustrated in FIG. 4A, a memory controller issues a memory command (CA), which includes four consecutive memory access requests: A0-A1, which are directed to rank 0, and A2-A3, which are directed to rank 1. The first memory access command RD[A0] is issued to rank 0, wherein RD[A0] is the first memory access request on rank 0 after an idle period for rank 0. In response, rank 0 prepends a calibration preamble 402 to read data Q[A0] returned for RD[A0].

[0037] Next, a write command WR[A1] is issued to rank 0 which causes a bus turnaround 404. Moreover, WR[A1] is the first write to rank 0 after the memory controller switches rank to rank 0. In this embodiment, rank 0 does not send another calibration preamble prior to receiving write data D[A1] from the memory controller. As illustrated in FIG. 4A, while D[A1] is being transmitted, EDC data EDC[A0] associated with read data Q[A0] is being received by the memory controller. Hence, the memory controller can use EDC[A0] to perform phase updates both during bus turnaround 404 and at the beginning of transmitting write data D[A1] to rank 0. Also, note that since there is not a rank switch between the read to A0 and write to A1, the EDC signal may alternatively continue to toggle or otherwise provide an "idle pattern" during the bubble period between A0 and A1 as is illustrated by the arrow in FIG. 4A. This idle pattern could be pre-defined or register programmable. It may also be command driven. For example, an extra command on the CA bus may actually be used to signal the DRAM that it will continue to be the rank that "owns" the data bus. (The DRAM could determine this itself based on its internal state machine, given that the write command has already been received by the DRAM prior to the "bubble" period.)

[0038] After issuing write command WR[A1], the memory controller switches ranks from rank 0 to idle rank 1. More specifically, immediately after

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issuing a precharge command PRE to close off the access to rank 0,, a write command WR[A2] is issued to rank 1, wherein WR[A2] is the first memory access request on rank 1 after the idle period on rank 1. In the embodiment of FIG. 4A, rank 1 does not send a calibration preamble before receiving write data D[A2] from the memory controller.

[0039] In an alternative embodiment to FIG. 4A, before issuing the write command WR[A2] to rank 1 after the rank switch, the memory controller can send a "preamble only" command to rank 1. This preamble only command causes rank 1 to send only a calibration preamble with a predetermined number of edges to the memory controller. The memory controller subsequently uses the calibration preamble to determine the amount of timing drift (due to voltage, temperature, etc.) that has occurred on rank 1. The memory controller can then compensate for the timing drift prior to transmitting the write data D[A2] to rank 1.

[0040] In a variation to the preamble only command technique, before issuing the write command WR[A2] to rank 1, the memory controller can issue an "addressless" or "data-less" read command to trigger a calibration preamble to be generated by rank 1 (because this is the first read command after the memory controller starts accessing rank 1). As a result, the calibration preamble is sent to the memory controller without causing any read data to be sent.

[0041] Note that, similar to the read with preamble command, the data-less preambles can have their length specified by a field in the "data-less" read command or "statically" programmed in a register on the targeted memory device. In one embodiment, two or more length values are programmed in registers on the targeted memory device and a field in the command selects from the two or more length values.

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[0042] Referring back to FIG. 4A, note that after sending write command WR[A2] to rank 1, a read command RD[A3] is subsequently issued to rank 1, which causes another bus turnaround 406. In this case, RD[A3] is the first read command directed to rank 1 after the memory controller switched to rank 1. In this situation, rank 1 does not send a calibration preamble before sending read data Q[A3] to the memory controller. This is because if the first memory transaction is a write (e.g., WR[A2]), the memory controller will already have received phase information from the EDC signal (e.g., EDC[A2]) during the write transaction, thereby allowing an update to the read clock phase, before a subsequent read transaction (e.g., RD[A3]) is initiated. As illustrated in FIG. 4A, while WR[A2] is in progress, EDC data EDC[A2] (associated with write data D[A2]) is received by the memory controller. Hence, the memory controller can use EDC[A2] to perform phase updates both during bus turnaround 406, and at the beginning of read data Q[A3] from rank 1.

[0043] Note that, while the embodiments illustrated in FIGs. 3 and 4 only illustrate two memory transactions on a given rank, subsequent memory transactions to the same rank do not require a calibration preamble. For exemple, a series of accesses to the same rank can commence with a read with preamble command (i.e. the first memory access after an idle period on the rank) followed by a write command, which is then followed by a read without preamble command.

[0044] In one embodiment, the memory controller can detect ranks that have not been accessed for a long period time. To prevent a large timing drift, which may be difficult to correct with a reasonable length preamble, the controller can periodically "talk" to a rank if the rank has been idle longer than a predetermined maximum time by sending a read with preamble command or a data-less read command to that rank. By sending such commands periodically, the

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memory controller avoids the need to perform later calibration operations that would necessitate longer calibration preambles, or a more exhaustive calibration process, such as one performed upon initialization of the system.

[0045] The above-described techniques and apparatus can be used in different systems having chips that that communicate with one another via chip-to-chip interfaces. Examples of such systems include front-side buses, and systems employing different types of memory devices and memory controllers that control the operation of these memory devices. Examples of these systems include, but are not limited to, mobile systems, desktop computers, servers, and/or graphics applications. The memory devices can include dynamic random access memory (DRAM). Moreover, the DRAM may be, e.g., graphics double data rate (GDDR, GDDR2, GDDR3, GDDR4, GDDR5, and future generations) and double data rate (DDR2, DDR3 and future memory types).

[0046] The techniques and apparatus described may be applicable to other types of memory, for example, flash and other types of non-volatile memory and static random access memory (SRAM). Moreover, throughout this description, a clock signal is described; it should be understood that a clock signal in the context of the instant description may be embodied as a strobe signal or, generally, as a signal that conveys timing information, and is not limited to a signal that is strictly periodic. For example, a timing reference may be a clock signal, which is periodic (however, it may be gated), or may be a strobe signal (that is aperiodic in the sense that it indicates when to sample data)

[0047] In several embodiments of the instant description, the error detection and correction (EDC) and timing reference signal (TRS) are illustrated, with the TRS signal sharing a signaling resource (pin, interconnect etc.) with data and with the EDC signal conveyed over a dedicated EDC signal line between the memory controller and a memory device. In other embodiments, the EDC signal

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and the TRS signal can each be conveyed, over respective dedicated signaling resources, between the memory controller and a memory device. For example, during a read operation, the TRS signal is transmitted by a memory device over a first signal line and is to be received by the memory controller before the read data is received (over separate signal lines) so that the memory controller can adjust its timing alignment to properly receive the read data. For the EDC operation corresponding to the memory read operation, the EDC signal is provided from the memory device over a second signal line and is skewed to be later in time than the resulting read data output since the EDC codes must be calculated before being transmitted from the memory device to the memory controller.

[0048] To prevent the EDC and/or TRS signals provided from different ranks from interfering with each other, additional spacing may be introduced between reads operations from different ranks. In an embodiment, to improve system bandwidth that may be otherwise consumed as a result of the additional spacing, the memory device limits the duration of the TRS and EDC signals for each transaction to be equal to the data burst length for the transaction (either read or write.) The TRS and EDC signals and read data have the same burst length and are skewed in time for their particular operation. For example, the TRS signal associated with a read operation is skewed to be earlier than the corresponding data in order to provide sufficient time for the memory controller to acquire timing information from the TRS signal before the data burst of the read operation begins. In this embodiment, the memory device begins sending the TRS signal between the time when it receives the read command ("read with TRS") and the time at which the memory device transmits the first bit of data of the corresponding read data. In addition, the memory device skews the timing of

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the EDC transmission corresponding to the read data to commence later than the time at which the memory device transmits the first bit of data.

[0049] In an embodiment, both the EDC and TRS are conveyed (either in TRS mode or in EDC mode) over the same signal line between the memory device and the memory controller. FIG. 4B presents a timing diagram illustrating preamble-based fast timing updates during read memory transactions using a dedicated signaling resource for TRS/EDC modes. Specifically, FIG. 4B illustrates memory read transactions with a TRS/EDC signaling resource configured in TRS mode, where a TRS signal is output by the memory device, prior to a corresponding first bit of data being output by the memory device. A transmitter circuit on the memory device provides the TRS/EDC to the memory controller via the TRS/EDC signaling resource in accordance with the mode programmed by the memory controller, or specified by the memory controller on a per read transaction basis.

[0050] In an embodiment, a register on the memory device stores a value which specifies either TRS mode or EDC mode. In this example, the timing of when each of the TRS and EDC signals are transmitted is shifted depending on which signal is being transmitted. For example, in TRS mode, the TRS signal burst would be shifted to commence before the corresponding read data burst commences, for example, as is illustrated in FIG. 4B, and in EDC mode, the EDC signal would be shifted to commence after corresponding read data burst commences. In this embodiment and in embodiments described above, the memory device may set the burst length of the TRS and EDC signals for each transaction to be equal to the data burst length for the memory transaction (either read or write). The burst length for the memory transaction is stored as a representative value in a programmable register on the memory device.

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[0051] In various embodiments, registers disposed on the memory device store values that represent time intervals between TRS/EDC and data transmission. In more detail a first register, disposed on the memory device, may be programmed by the controller via a set register command accompanied by a first value that the memory device receives and stores in the first register. The first value represents a first time interval that transpires between a referenced point of the timing reference signal (e.g., a first toggle of the TRS burst, or last toggle of the TRS burst) and the beginning, or first bit of the data burst. The first time interval may be, for example, be expressed as a number of clock cycles or a number of nano seconds that transpire.

[0052] For a data to EDC time interval, a second register, disposed on the memory device, may be programmed by the controller via the set register command accompanied by a second value that the memory device receives and stores in the second register. The second value represents a first time interval that transpires between a referenced point of the data burst (e.g., launching of the first bit of data) and, for example, the beginning, or first bit of the EDC burst. The second time interval may, for example, be expressed as a number of clock cycles or a number of nanoseconds that transpire.

[0053] In another embodiment, the functionality of the first and second registers is served by a single register that specifies a time interval that is applied, depending on which mode the memory device is programmed to be in. For example, a single register, in this embodiment, contains a value that represents a timing interval that separates TRS and data output for TRS mode, and specifies a timing interval that separates data and EDC output for EDC mode.

[0054] In another embodiment, the controller can specify individual burst lengths for the TRS and EDC signals via corresponding programmable registers on the memory device. These registers may be programmed via a register

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program command in which values that represent burst lengths for the TRS and EDC signals are conveyed from the controller and stored in their respective registers. Alternatively, the EDC and TRS burst lengths may be specified by information that is provided with the memory access commands (e.g., Read and Write commends) for a corresponding memory access. In another embodiment, multiple sets of programmable registers are implemented on a memory device. Each set of programmable registers stores values that are representative of respective different selectable EDC burst lengths and TRS burst lengths. Information provided with a memory access command specifies which register is selected to provide the burst length for the EDC and TRS signals.

[0055] Additional embodiments of memory systems that may use one or more of the above-described apparatus and techniques are described below with reference to FIG. 5. FIG. 5 presents a block diagram illustrating an embodiment of a memory system 500, which includes at least one memory controller 510 and one or more memory devices 512 arranged in each rank. Memory controller 510 and each memory device 512 are individual integrated circuit devices, which may be included in a single chip-package. For example, memory controller 510 may be stacked with one or more memory devices 512 in a through-silicon via (TSV) stack. Alternatively, multiple memory devices 512 may be integrated in a TSV stack, such that one of them may act like a "memory controller" which requests TRS from other memory devices 512 in the stack.

[0056] In some embodiments, memory controller 510 is a local memory controller (such as a DRAM memory controller) and/or is a system memory controller (which may be implemented in a microprocessor, an application-specific integrated circuit (ASIC), a system-on-a-chip (SoC) or a field-programmable gate array (FPGA)).

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[0057] Memory controller 510 may include an I/O interface 518-1 and control logic 520-1. In some embodiments, one or more of memory devices 512 include control logic 520 and at least one of interfaces 518. However, in some embodiments some of the memory devices 512 may not have control logic 520. Moreover, memory controller 510 and/or one or more of memory devices 512 may include more than one of the interfaces 518, and these interfaces may share one or more control logic 520 circuits. In some embodiments one or more of the memory devices 512 is configured as a memory rank 516.

[0058] As discussed in conjunction with FIGs. 1A, 1B, 2, 3 and 4, control logic 520-1 on memory controller 510 may be used to issue "read with preamble" commands to ranks within memory devices 512 to request timing reference signals for fast timing updates when these ranks are being accessed for the first time after having been idle. Memory controller 510 can also determine a suitable length for each TRS being requested. Note that the techniques described in conjunction with FIGs. 1A, 1B, 2, 3 and 4 may also be applied in systems with only one rank of memory, when this single rank has not been accessed for some period of time, thus requiring the same timing update as described for a multi-rank system.

[0059] Memory controller 510 and memory devices 512 are coupled by one or more links 514, such as multiple wires, in a channel 522. While memory system 500 is illustrated as having three links 514, other embodiments may have fewer or more links 514. Moreover, these links may provide: wired, wireless and/or optical communication. Furthermore, links 514 may be used for bi-directional and/or uni-directional communication between the memory controller 510 and one or more of the memory devices 512. For example, bi-directional communication between the memory controller 510 and a given memory device may be simultaneous (full-duplex communication). Alternatively, the memory

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controller 510 may transmit information (such as a data packet which includes a command) to the given memory device, and the given memory device may subsequently provide the requested data to the memory controller 510, e.g., a communication direction on one or more of the links 514 may alternate (half-duplex communication). Also, one or more of the links 514 and corresponding transmit circuits and/or receive circuits may be dynamically configured, for example, by one of the control logic 520 circuits, for bi-directional and/or uni-directional communication.

[0060] Signals corresponding to data and/or commands (such as request-for-data commands) may be communicated on one or more of the links 514 using either or both edges in one or more timing signals. These timing signals may be generated based on one or more clock signals, which may be generated on-chip (for example, using a phase-locked loop and one or more reference signals provided by a frequency reference) and/or off-chip. Note that the CA bus on links 514 may be used to convey signals having predetermined functional definitions (e.g. Bank address, Write enable, Chip select, etc.) or it may be packetized on a smaller set of pins.

[0061] In some embodiments, commands are communicated from the memory controller 510 to one or more of the memory devices 512 using a separate command link, i.e., using a subset of the links 514 which communicate commands. However, in some embodiments commands are communicated using the same portion of the channel 522 (i.e., the same links 514) as data. Moreover, communication of commands: may have a lower data rate than the data rates associated with communication of data between the memory controller 510 and one or more of the memory devices 512; may use different carrier frequencies than are used to communicate data; and/or may use a different modulation technique than is used to communicate data.

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[0062] Devices and circuits described herein may be implemented using computer-aided design tools available in the art, and embodied by computer-readable files containing software descriptions of such circuits. These software descriptions may be: behavioral, register transfer, logic component, transistor and layout geometry-level descriptions. Moreover, the software descriptions may be stored on storage media or communicated by carrier waves.

[0063] Data formats in which such descriptions may be implemented include, but are not limited to: formats supporting behavioral languages like C, formats supporting register transfer level (RTL) languages like Verilog and VHDL, formats supporting geometry description languages (such as GDSII, GDSIII, GDSIV, CIF, and MEBES), and other suitable formats and languages. Moreover, data transfers of such files on machine-readable media may be done electronically over the diverse media on the Internet or, for example, via email. Note that physical files may be implemented on machine-readable media such as: 4 mm magnetic tape, 8 mm magnetic tape, 3-1/2 inch floppy media, CDs, DVDs, and so on.

[0064] The foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.

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What Is Claimed Is:

1. A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data accessed from a memory core, the read command containing information which specifies whether the memory device is to commence outputting of a timing reference signal prior to commencing outputting of the data; and

receiving the timing reference signal if the information specified that the memory device output the timing reference signal, wherein the memory controller samples the data output from the memory device based on information provided by the timing reference signal output from the memory device.

2. The method of claim 1, wherein the memory controller samples the data output from the memory device using the timing reference signal if the information specified that the memory device output the timing reference signal.

3. The method of claim 1, wherein the memory controller samples the data output from the memory device using a sampling clock wherein, the method further comprising adjusting the sampling clock based on phase information derived from the timing reference signal.

4. The method of claim 3, further comprising:

after receiving the timing reference signal, receiving an error detection and correction (EDC) signal from the memory device, wherein a first bit of the EDC signal is received after a first bit of the read data; and

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using the EDC signal to further update the phase of the internal receive clock after the timing reference signal.

5. The method of claim 1, wherein the read command further includes information that specifies a burst length of the timing reference signal.

6. The method of claim 5, wherein the method further comprises:

determining a duration of an idle period that transpires prior to transmitting the read command to the memory device; and

selecting the information that specifies the burst length based on the duration of the idle period.

7. The method of claim 1, further comprising transmitting a command, to the memory device, that specifies storing a value in a register of the memory device, the value being representative of a burst length of the timing reference signal.

8. The method of claim 1, wherein a burst length of the timing reference signal is the same as a burst length of the data.

9. The method of claim 1, wherein transmitting the read command further comprises:

determining whether the memory device is to be accessed after a predetermined idle period for the memory device transpires; and

specifying that the memory device output the timing reference signal associated with the read command based on the predetermined idle period transpiring.

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10. The method of claim 9, wherein the predetermined idle period is of a first duration, the method further comprising:

detecting that the memory device is to be accessed after an idle period transpires that includes a duration longer than the first duration; and

specifying that the memory device output a subsequent timing reference signal having a burst length that is longer than a burst length of the timing reference signal associated with the read command based on the predetermined idle period transpiring.

11. The method of claim 1, wherein the information identifies a selected programmable register from a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal.

12. The method 1, further comprising:

detecting that a predetermined time period has transpired in which an operational state of a memory device is idle;

transmitting a command which specifies that the memory device output a timing reference signal having a predetermined burst length; and

receiving the timing reference signal, wherein the memory controller uses phase information provided by the timing reference signal output from the memory device to adjust a phase of an internal sampling clock used to sample data provided by the memory device.

13. The method of claim 12, wherein the predetermined time period is detected directly prior to transmitting a write command to the memory device.

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14. A memory controller, comprising:

a transmitter circuit to provide a read command which specifies that a memory device output data accessed from a memory core, the read command containing information which specifies whether the memory device is to commence output of a timing reference signal prior to outputting of the data; and

a receiver circuit to receive the timing reference signal wherein the timing reference signal is used to adjust memory controller receive timing of the data output from the memory device.

15. The memory controller of claim 14, further comprising a circuit, coupled to the receiver circuit, to generate a sampling clock used to sample the data output from the memory device, the circuit to adjust the sampling clock based on phase information derived from the timing reference signal.

16. The memory controller of claim 15, further comprising:

a receiver circuit to receive an error detection and correction (EDC) signal from the memory device; and

a circuit to update the sampling clock based on information derived from the EDC signal.

17. The memory controller of claim 14, wherein the read command further includes information that specifies a burst length of the timing reference signal.

18. The memory controller of claim 14, wherein the transmitter circuit transmits a command that specifies storing a value in a register of the memory

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device, the value being representative of a burst length of the timing reference signal.

19. The memory controller of claim 14, wherein the information identifies a selected programmable register from a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal.

20. The memory controller of claim 14, wherein the transmitter circuit provides a command which specifies that the memory device output a timing reference signal having a predetermined burst length.

21. A method for operation of a memory device, the method comprising:

receiving a read command which specifies that the memory device output data accessed from a memory core, the read command containing information which specifies whether the memory device is to commence output of a timing reference signal prior to commencing outputting of the data; and

transmitting the timing reference signal if the information specified that the memory device output the timing reference signal, wherein a memory controller samples the data output from the memory device based on information provided by the timing reference signal output from the memory device.

22. The method of claim 21, further comprising:

generating an error detection and correction signal; and

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after transmitting the timing reference signal, transmitting the EDC signal, wherein a first bit of the EDC signal is transmitted after a first bit of the read data is output.

23. The method of claim 21, wherein the read command further includes information that specifies a burst length of the timing reference signal.

24. The method of claim 21, further comprising receiving a command that specifies storing a value in a register of the memory device, the value being representative of a burst length of the timing reference signal.

25. The method of claim 21, wherein the information identifies a selected programmable register from a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal.

26. The method of claim 21, further comprising:

detecting that a predetermined time period has transpired in which an operational state of a memory device is idle; and

transmitting a timing reference signal after detecting that the predetermined time period has transpired.

27. The method of claim 21, further comprising:

receiving a command which specifies that the memory device output a timing reference signal having a predetermined burst length; and

transmitting the timing reference signal in response to the command which specifies that the memory device output the timing reference signal.

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28. The method of claim 21, wherein the memory controller uses phase information provided by the timing reference signal output from the memory device to adjust a phase of an internal sampling clock used to sample data provided by the memory device.

29. The method of claim 21, further comprising transmitting a timing reference signal based on a state of an internal state machine.

30. A memory device, comprising:

a receiver circuit to receive a read command, wherein the read command includes information that specifies whether to precede outputting of data associated with the read command with a timing reference signal; and

a transmitter circuit to output the timing reference signal according to the information.

31. The memory device of claim 30, further comprising a first register to store a value that is representative of a first burst length of the timing reference signal.

32. The memory device of claim 31, further comprising a second register to store a value that is representative of a second burst length of the timing reference signal, wherein the information specifies at least one of the first and second burst lengths for the timing reference signal output by the transmitter, by selecting at least one of the first and second registers, wherein the transmitter circuit outputs the timing reference signal having a burst length as selected by at least the first and second register.

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33. The memory device of claim 30, further comprising a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal wherein the information further selects a burst length value for the timing reference signal by addressing a corresponding register of the plurality of registers.

34. The memory device of claim 30, further comprising:

a first transmitter circuit to output the data; and

a second transmitter circuit to output an error detection and correction signal after a first bit of the read data is output by the first transmitter circuit.

35. The memory device of claim 30, wherein the read command further includes information that specifies a burst length of the timing reference signal.

36. The memory device of claim 30, further comprising a register, wherein the receiver circuit receives a command that specifies storing a value in the register, the value being representative of a burst length of the timing reference signal.

37. The memory device of claim 21, further comprising:

a circuit to detect that a predetermined time period has transpired in which an operational state of a memory device is idle, wherein the transmitter circuit transmits a timing reference signal after detecting that the predetermined time period has transpired.

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38. The memory device of claim 30, wherein the receiver circuit receives a command which specifies that the memory device output a timing reference signal having a predetermined burst length.

39. The memory device of claim 30, further comprising a register that specifies whether the transmitter circuit provides one of the timing reference signal in a first mode and an error detection code in a second mode.

40. The memory device of claim 30, further comprising:

a register that specifies a timing interval between the outputting of the timing signal and outputting a first bit of the data.

41. The memory device of claim 30, further comprising a register that specifies a timing interval to occur between outputting a first bit of the data and transmitting an error detection code, the error detection code corresponding to the data.

42. A memory system, comprising:

a memory device and a memory controller;

a first interconnect to carry a read command from the memory controller to the memory device, the read command including information which specifies whether the memory device is to commence output of a timing reference signal prior to commencing outputting of the data; and

a second interconnect to convey the timing reference signal from the memory device to the memory controller, wherein the timing reference signal is

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used to adjust memory controller receive timing of the data output from the memory device.

43. The system of claim 42, further comprising a plurality of ranks, wherein the memory device is disposed a rank in the plurality of ranks, wherein the memory controller specifies that the memory device output the timing reference signal associated with the read command after a predetermined idle period transpires for the rank.

44. The system of claim 43, wherein the memory controller specifies that a memory device from each rank of the plurality of ranks output a timing signal periodically in accordance with a corresponding predetermined idle duration for each rank of the plurality of ranks.

45. The system of claim 44, wherein the memory controller schedules read accesses to the plurality of ranks such that a memory device from each rank of the plurality of ranks outputs a timing signal, during each read access, such that a predetermined threshold idle period for each rank is not exceeded.

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PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

ABSTRACT

Apparatus and methods for operation of a memory controller, memory device and system are described. During operation, the memory controller transmits a read command which specifies that a memory device output data accessed from a memory core. This read command contains information which specifies whether the memory device is to commence outputting of a timing reference signal prior to commencing outputting of the data. The memory controller receives the timing reference signal if the information specified that the memory device output the timing reference signal. The memory controller subsequently samples the data output from the memory device based on information provided by the timing reference signal output from the memory device.

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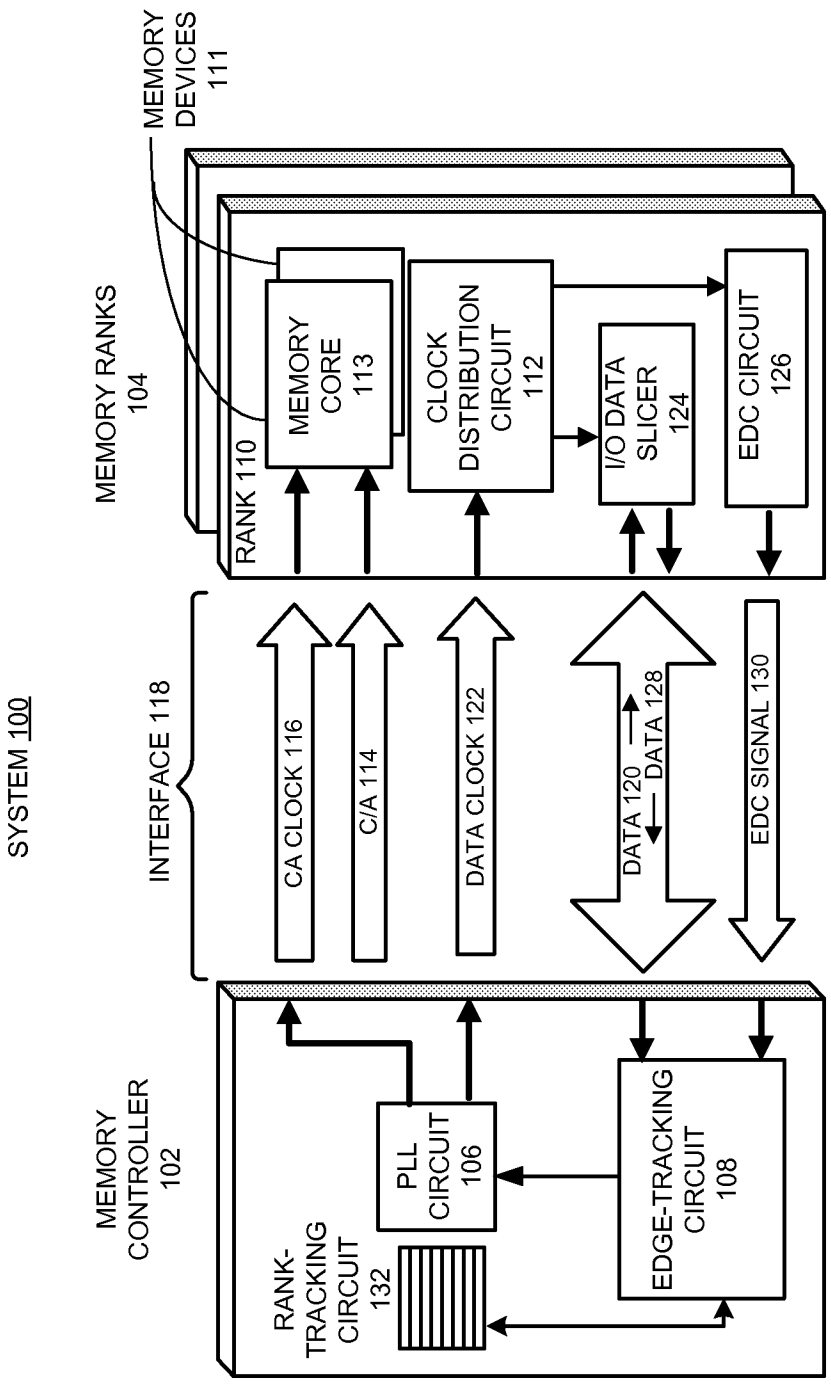


FIG. 1A

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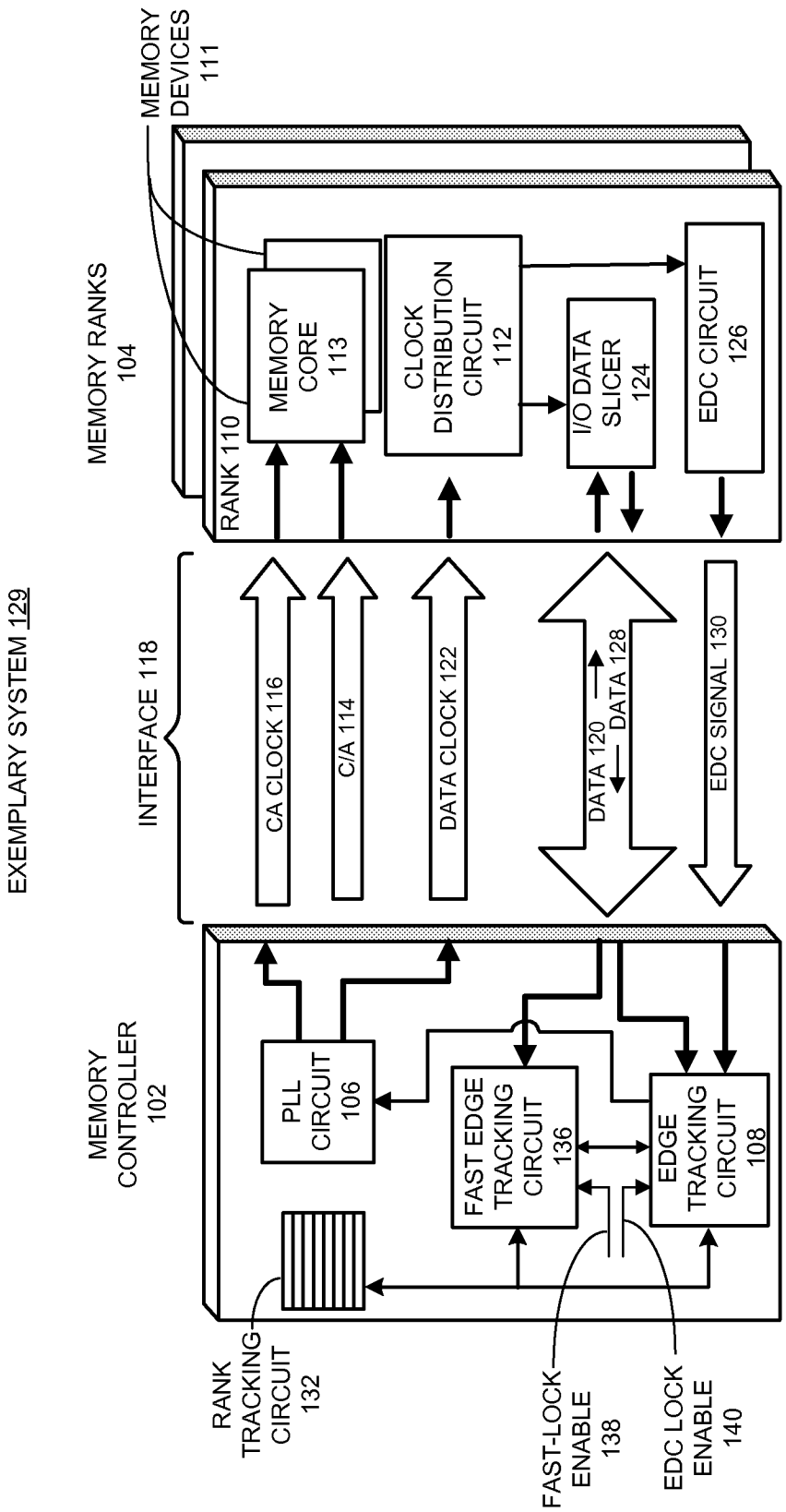


FIG. 1B

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Ex. 1050, p. 41

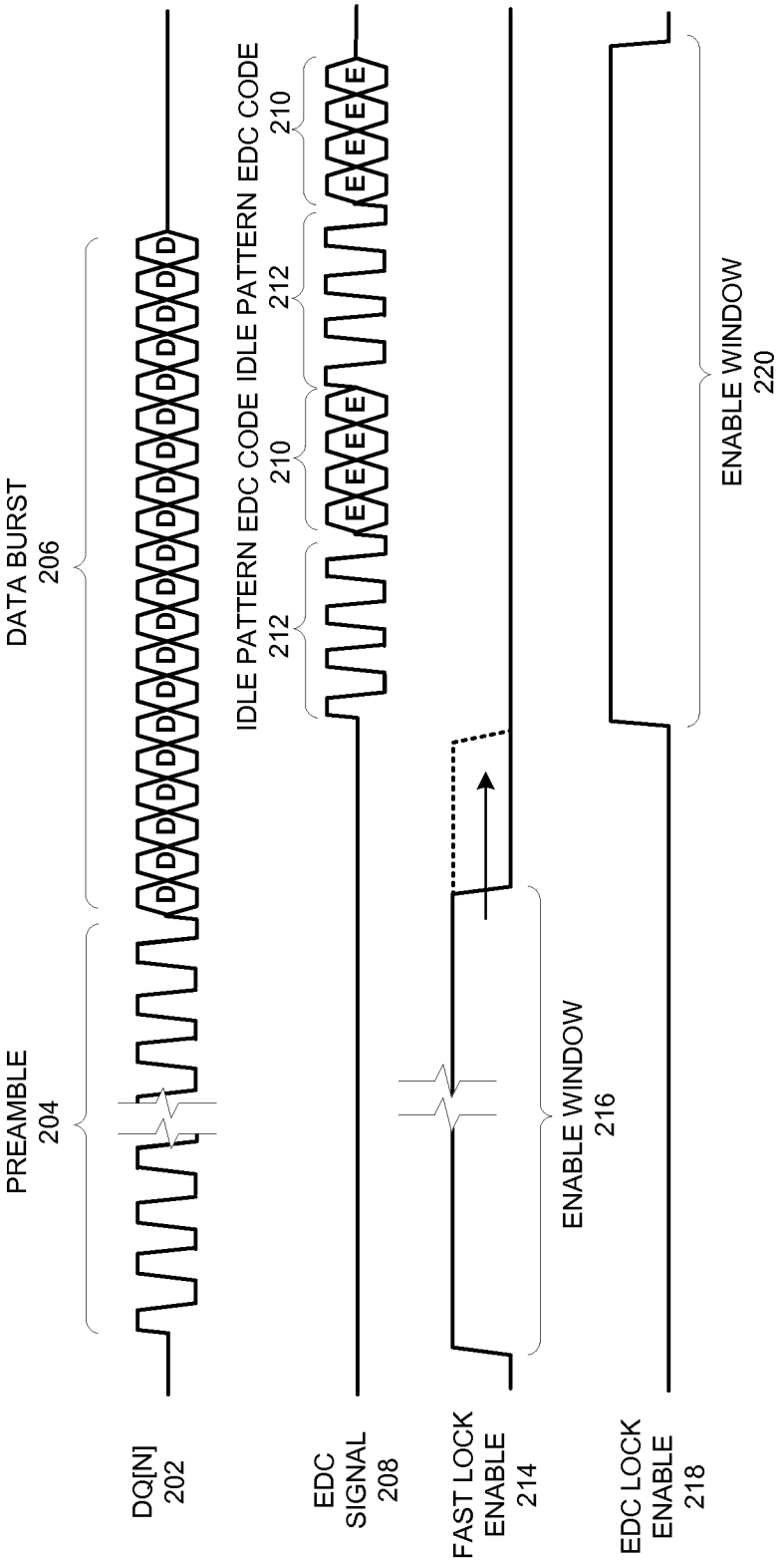


FIG. 2

Samsung Electronics Co., Ltd.
Ex. 1050, p. 42

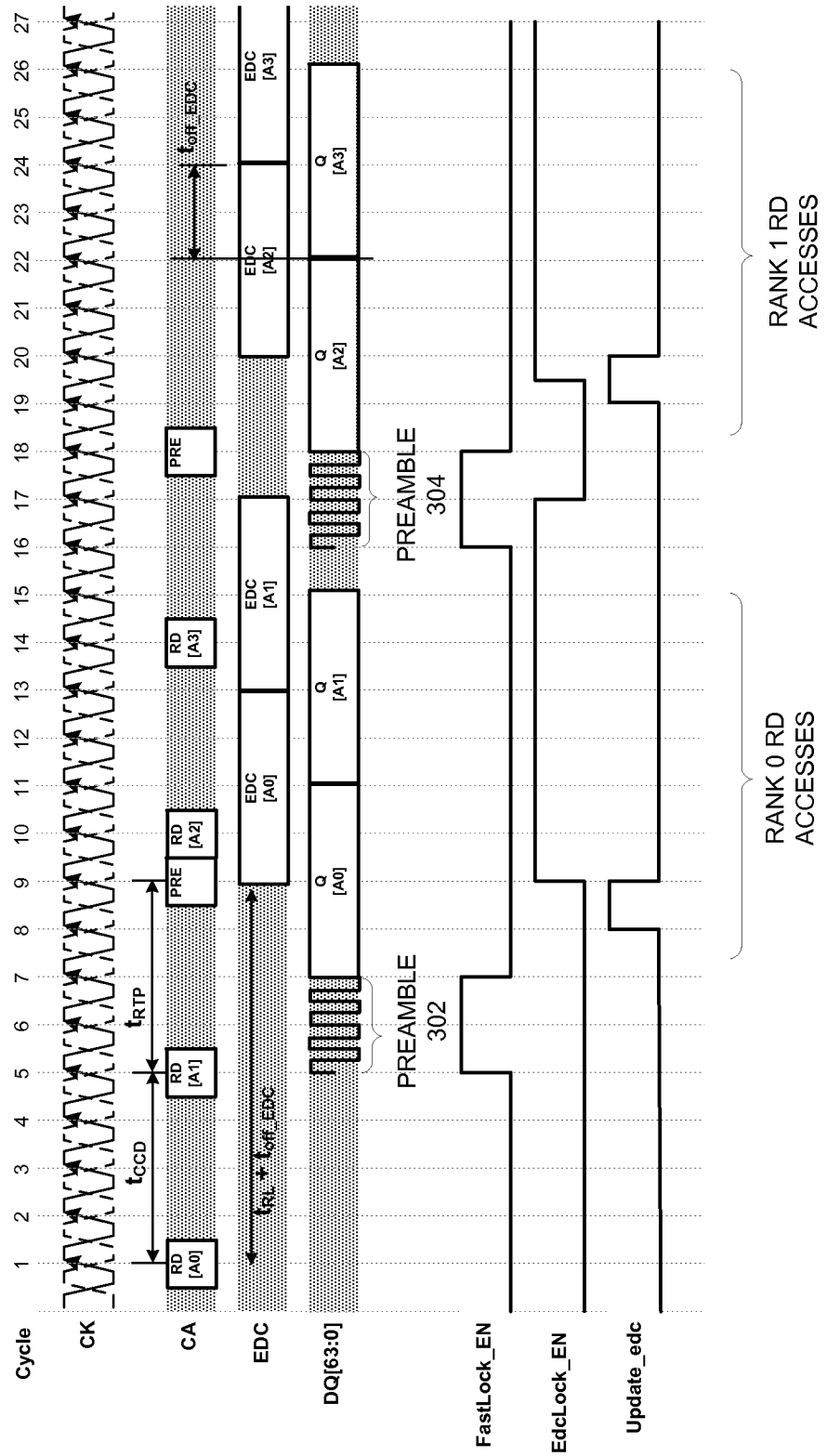


FIG. 3

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Ex. 1050, p. 43

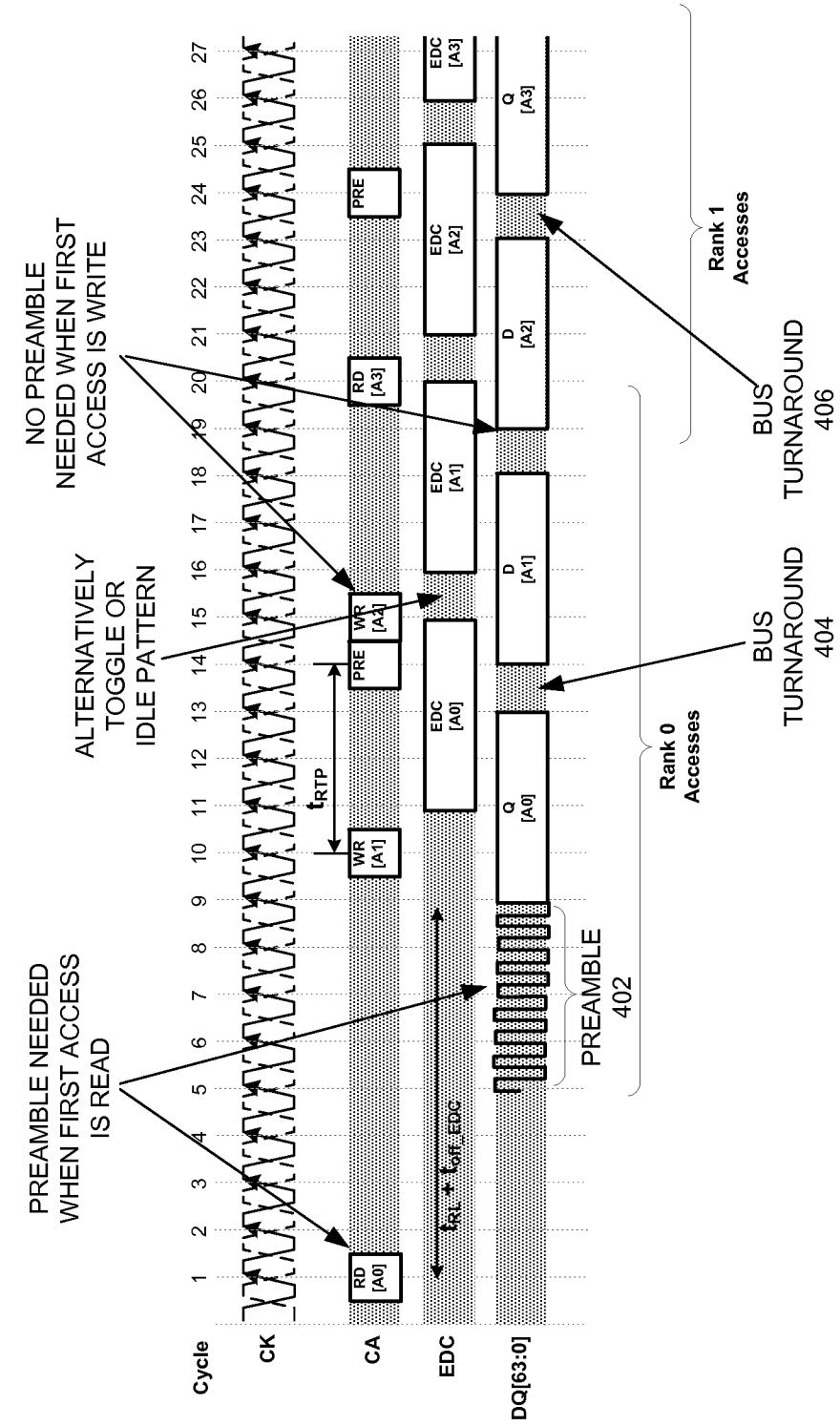


FIG. 4A

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Ex. 1050, p. 44

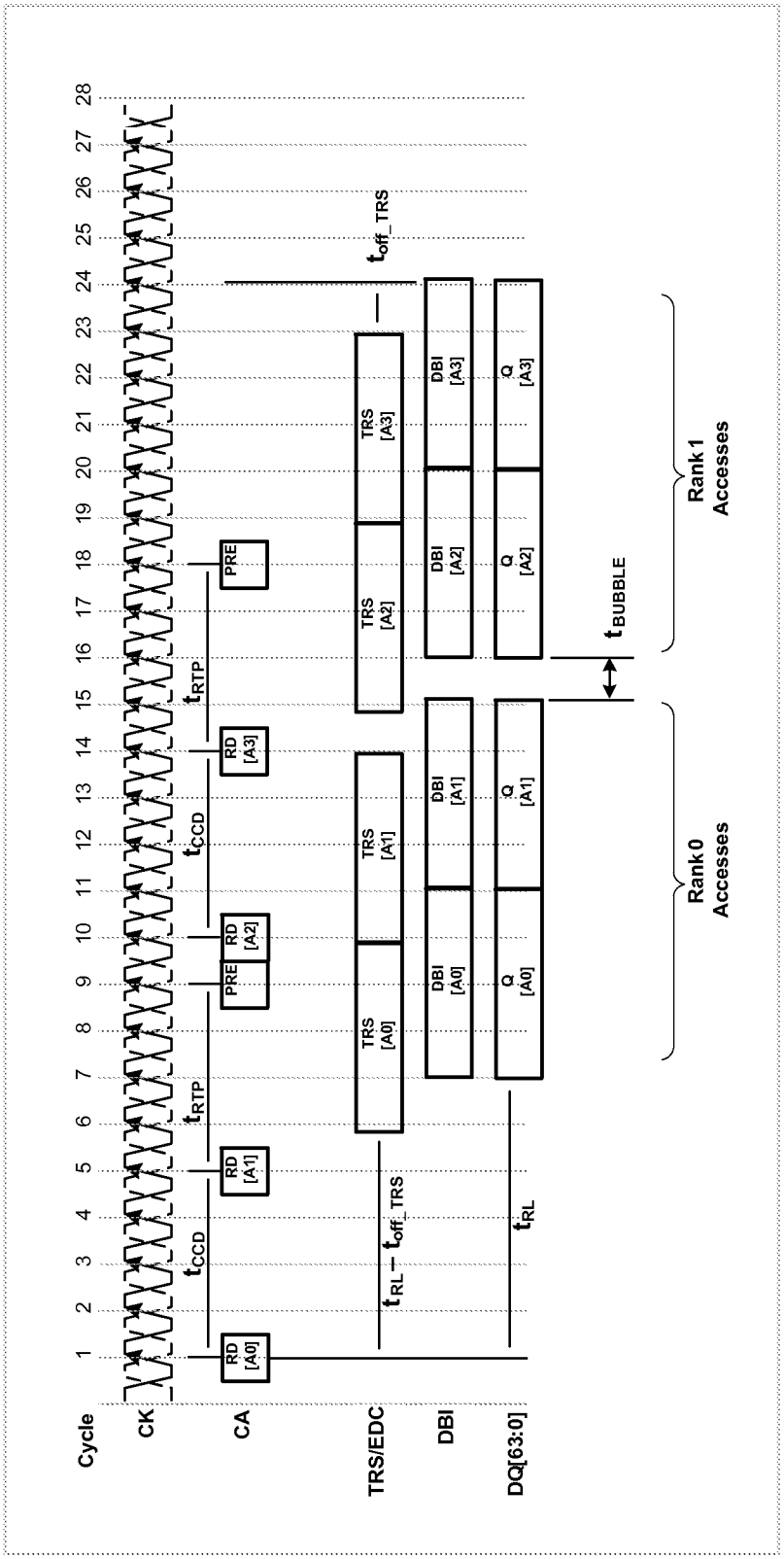


FIG. 4B

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Ex. 1050, p. 45

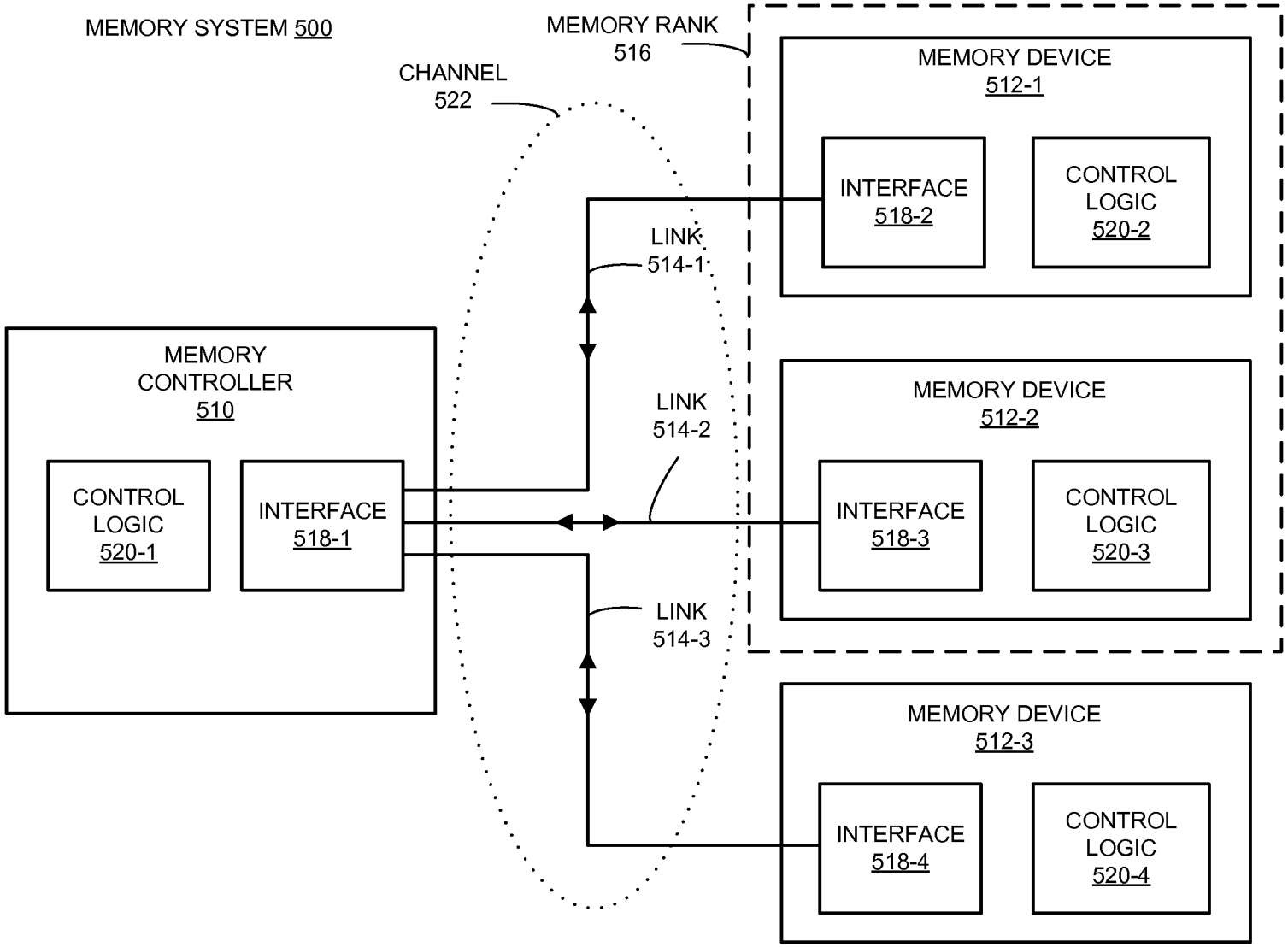

MEMORY SYSTEM 500
MEMORY RANK
516
CHANNEL
522
MEMORY DEVICE
512-1
INTERFACE
518-2
CONTROL
LOGIC
520-2
LINK
514-1
MEMORY
CONTROLLER
510
LINK
514-2
MEMORY DEVICE
512-2
CONTROL
LOGIC
520-1
INTERFACE
518-1
INTERFACE
518-3
CONTROL
LOGIC
520-3
LINK
514-3
MEMORY DEVICE
512-3
INTERFACE
518-4
CONTROL
LOGIC
520-4

FIG. 5

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below by my name;

I believe I am the original, first and sole inventor, if only one name is listed below, or an original, first and joint inventor if multiple names are listed below, of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

for which a patent application:

☒ is attached hereto.

☐ was filed in the United States on _ as Application No. ____;

☐ with amendment(s) filed on _____ *(if applicable)*.

I hereby state that I have reviewed and understand the contents of the application identified above, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56, which states in relevant part:

> Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section.... The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office....

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d), of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (Day, Month, Year)	PRIORITY CLAIMED
			YES ☐ NO ☐

I hereby claim the benefit under Title 35, United States Code, §119(e), of any United States provisional application(s) listed below:

APPLICATION NUMBER	DATE OF FILING
61/366,806	22 July 2010

I hereby claim the benefit under Title 35, United States Code, §120, of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information that is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	DATE OF FILING	STATUS		
		PATENTED	PENDING	ABANDONED

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I hereby appoint the Patent Practitioners associated with the Customer Number 68325 to prosecute this application and transact all business in the Patent and Trademark Office connected therewith, and to file, prosecute and transact all business in connection with international applications directed to said invention.

Address correspondence to:	CUSTOMER NUMBER	Direct telephone calls to:
Park, Vaughan, Fleming & Dowler LLP **2820 Fifth Street** **Davis, CA 95618-7759**	68325 PATENT TRADEMARK OFFICE	Anthony P. Jones (530) 759-1666

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, §1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1	Name and Citizenship	Ian Shaeffer	United States
	Residence Address	23 Jackson Street, Los Gatos, CA 95030	
	Postal Address *(if different from Residence)*		
	Signature and Date		Date 5/10/11
2	Name and Citizenship	Thomas J. Giovannini	United States
	Residence Address	3614 Deedham Drive, San Jose, CA 95148	
	Postal Address *(if different from Residence)*		
	Signature and Date		Date 5/9/11
3	Name and Citizenship		
	Residence Address		
	Postal Address *(if different from Residence)*		
	Signature and Date		Date
4	Name and Citizenship		
	Residence Address		
	Postal Address *(if different from Residence)*		
	Signature and Date		Date
5	Name and Citizenship		
	Residence Address		
	Postal Address *(if different from Residence)*		
	Signature and Date		Date

Additional inventor name(s) and signature(s) attached?: YES ☐ NO ☒

Samsung Electronics Co., Ltd.
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PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: RAMBUS INC.

Application No./Patent No.: 61/366,806 Filed/Issue Date: 22 July 2010

Titled: PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

RAMBUS INC. , a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. [X] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Ian Shaeffer et al. To: RAMBUS INC.

The document was recorded in the United States Patent and Trademark Office at Reel 024948, Frame 0654, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Anthony P. Jones/ — Signature

11 May 2011 — Date

Anthony P. Jones (Reg. No. 59,521) — Printed or Typed Name

Attorney of Record — Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

TO:EDWARD J. GRUNDLER COMPANY:PARK, VAUGHAN & FLEMING, LLP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

SEPTEMBER 08, 2010 *50128322A*

PTAS

EDWARD J. GRUNDLER
PARK, VAUGHAN & FLEMING, LLP
2820 FIFTH STREET
DAVIS, CA 95618

UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 571-272-3350. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, MAIL STOP: ASSIGNMENT SERVICES BRANCH, P.O. BOX 1450, ALEXANDRIA, VA 22313.

RECORDATION DATE: 09/07/2010 REEL/FRAME: 024948/0654
NUMBER OF PAGES: 5

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).
DOCKET NUMBER: R-RA0764.PROV1.US

ASSIGNOR:
SHAEFFER, IAN DOC DATE: 08/20/2010

ASSIGNOR:
GIOVANNINI, THOMAS J. DOC DATE: 08/19/2010

ASSIGNEE:
RAMBUS INC.
4440 EL CAMINO REAL
LOS ALTOS, CALIFORNIA 94022

SERIAL NUMBER: 61366806 FILING DATE: 07/22/2010
PATENT NUMBER: ISSUE DATE:
TITLE: PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

TO:EDWARD J. GRUNDLER COMPANY:PARK, VAUGHAN & FLEMING, LLP

ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

09/07/2010
501283522

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Ian Shaeffer	08/20/2010
Thomas J. Giovannini	08/18/2010

RECEIVING PARTY DATA

Name:	RAMBUS INC.
Street Address:	4440 El Camino Real
City:	Los Altos
State/Country:	CALIFORNIA
Postal Code:	94022

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	61366806

CORRESPONDENCE DATA

Fax Number: (530)759-1665
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 530-759-1663
Email: edward@parklegal.com
Correspondent Name: Edward J. Grundler
Address Line 1: Park, Vaughan & Fleming, LLP
Address Line 2: 2820 Fifth Street
Address Line 4: Davis, CALIFORNIA 95618

ATTORNEY DOCKET NUMBER:	R-RA0764.PROV1.US
NAME OF SUBMITTER:	Edward J. Grundler, Reg. No. 47,815

Total Attachments: 3
source=R-RA0764.Prov1.US_Assignment#page1.tif
source=R-RA0764.Prov1.US_Assignment#page2.tif

TO:EDWARD J. GRUNDLER COMPANY:PARK, VAUGHAN & FLEMING, LLP



CORPORATE ASSIGNMENT

WHEREAS, the undersigned,

Ian Shaeffer	23 Jackson Street, Los Gatos, CA 95030
Thomas J. Giovannini	3614 Deedham Drive, San Jose, CA 95148

hereinafter termed "Inventor(s)", have invented certain new and useful improvements in

PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

and have executed a declaration or oath for an application for a United States patent disclosing and identifying the invention:

___ On the ___ day of _____, 20___;

Or

X Said application having Application Number 61/366,806 and filed on 22 July 2010 ; and

WHEREAS, RAMBUS INC. a corporation of the State of Delaware, having a place of business at 4440 El Camino Real, Los Altos, CA 94022, (hereinafter termed "Assignee"), is desirous of acquiring the entire right, title and interest in and to said application and the invention disclosed therein, and in and to all embodiments of the invention, heretofore conceived, made or discovered jointly or severally by said Inventor(s) (all collectively hereinafter termed "said invention"), and in and to any and all patents, inventor's certificates and other forms of protection (hereinafter termed "patents") thereon granted in the United States and foreign countries.

NOW, THEREFORE, in consideration of good and valuable consideration acknowledged by said Inventor(s) to have been received in full from said Assignee:

1. Said Inventor(s) do hereby sell, assign, transfer and convey unto said Assignee the entire right, title and interest (a) in and to said application and said invention; (b) in and to all rights to apply for foreign patents on said invention pursuant to the International Convention for the Protection of Industrial Property or otherwise; (c) in and to any and all applications filed and any and all patents granted on said invention in the United States or any foreign country, including each and every application filed and each and every patent granted on any application which is a divisional, substitution, continuation, or continuation-in-part of any of said applications; and (d) in and to each and every reissue or extensions of any of said patents.

2. Said Inventor(s) hereby jointly and severally covenant and agree to cooperate with said Assignee to enable said Assignee to enjoy to the fullest extent the right, title and interest herein conveyed in the United States and foreign countries. Such cooperation by said Inventor(s) shall include prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, specifications, declarations or other papers, and other assistance all to the extent deemed necessary or desirable by said Assignee (a) for perfecting in said Assignee the right, title and interest herein conveyed; (b) for prosecuting any of said applications; (c) for filing and prosecuting substitute, divisional, continuing or additional applications covering said invention; (d) for filing and prosecuting applications for reissuance of any said patents; (e) for interference or other priority proceedings involving said invention; and (f) for legal proceedings involving said invention and any applications therefor and any patents granted thereon, including without limitation reissues and reexaminations, opposition proceedings, cancellation proceedings, priority contests, public use proceedings, infringement actions and court actions; provided, however, that the expense incurred by said

Samsung Electronics Co., Ltd.
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Inventor(s) in providing such cooperation shall be paid for by said Assignee.

3. The terms and covenants of this assignment shall inure to the benefit of said Assignee, its successors, assigns and other legal representatives, and shall be binding upon said Inventor(s), their respective heirs, legal representatives and assigns.

4. Said Inventor(s) hereby jointly and severally warrant and represent that they have not entered and will not enter into any assignment, contract, or understanding in conflict herewith.

IN WITNESS WHEREOF, said Inventors have executed and delivered this instrument to said Assignee as of the dates written below.

Ian Shaeffer

8/20/10
Date

State of California)
)
County of Santa Clara)

On 8-20-10, before me, Dorothy L. Levin, Notary Public personally appeared Ian Shaeffer,
who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/~~her/their~~ authorized capacity(ies), and that by his/~~her/their~~ signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

(Signature of Notary Public)

DOROTHY L. LEVIN
Commission # 1835908
Notary Public - California
Santa Clara County
My Comm. Expires Mar 10, 2013

Thomas J. Giovannini

8/18/2010
Date

DOROTHY L LEVIN
Commission # 1835908
Notary Public - California
Santa Clara County
My Comm. Expires Mar 10, 2013

State of California)
)
County of Santa Clara)

On Aug 18, 2010 before me, Dorothy L Levin, Notary Public
personally appeared Thomas J. Giovannini,
who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

(Signature of Notary Public)

Date

State of)
)
County of)

On_____, before me, _____,
personally appeared ,
who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

(Signature of Notary Public)

Samsung Electronics Co., Ltd.
Ex. 1050, p. 57

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Filer:	A.Richard Park
Attorney Docket Number:	R-RA0764.P.US

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	25	52	1300
Independent claims in excess of 3	1201	2	220	440
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2830**

Electronic Acknowledgement Receipt

EFS ID:	10062475
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	68325
Filer:	A.Richard Park
Filer Authorized By:	
Attorney Docket Number:	R-RA0764.P.US
Receipt Date:	11-MAY-2011
Filing Date:	
Time Stamp:	19:47:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2830
RAM confirmation Number	7753
Deposit Account	505066
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Samsung Electronics Co., Ltd.
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Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Authorization-deposit-account-RAMBUS.pdf	22189 25901cfb1e9eb606d09bd995520588b7b0097922	no	1
Warnings:					
Information:					
2	Application Data Sheet	Application_Data_Sheet_RAMBUSsb0014_fill.pdf	837357 420704b8e6af614846f6dd1eef5657b2580f7492	no	4
Warnings:					
Information:					
3		R-RA0764_Prov1_US_Application.pdf	165482 ce9f50160be6700eab05050fbc590b9aff5c2d4e	yes	34

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	23
Claims	24	33
Abstract	34	34

Warnings:					
Information:					
4	Drawings-only black and white line drawings	Visio-R-RA0764_Prov1_Figures.pdf	251615 94dcc9ca43ab40256196c1d9317a1b81e72540e3	no	7
Warnings:					
Information:					
5	Oath or Declaration filed	Oath.pdf	1075734 5ffa5b5f6c767796e7825d87a3b9760a588b73cd	no	2
Warnings:					
Information:					
6	Assignee showing of ownership per 37 CFR 3.73(b).	Assignee.pdf	352544 5456f860ee6a46d39b7f615e519fb4e54f8cdbf7	no	9
Warnings:					

Information:					
7	Fee Worksheet (PTO-875)	fee-info.pdf	37621 f01f82a3a901a7b04a72403ed5f23fca8b70a a04	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2742542	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 13105798 Document Date: 5/11/2011

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: February 8, 2006

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/105,798	05/11/2011	2189	2830	R-RA0764.P.US	45	5

CONFIRMATION NO. 3982

68325
PVF -- RAMBUS, INC.
c/o PARK, VAUGHAN, FLEMING & DOWLER LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

FILING RECEIPT

OC000000047961051

Date Mailed: 06/01/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Ian Shaeffer, Los Gatos, CA;
Thomas J. Giovannini, San Jose, CA;

Assignment For Published Patent Application

RAMBUS INC., Los Altos, CA

Power of Attorney: The patent practitioners associated with Customer Number 68325

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/366,806 07/22/2010

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 05/31/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/105,798**

Projected Publication Date: 01/26/2012

Non-Publication Request: No

Early Publication Request: No

Samsung Electronics Co., Ltd.
Ex. 1050, p. 64

Title

PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

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Ex. 1050, p. 65

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/105,798

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	45 minus 20 =	* 25			OR	x 52 =	1300
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5 minus 3 =	* 2				x 220 =	440
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2830

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080205187	A1	2008-08-28	Hong Beom PYEON	Abstract, claim 1 and figures 4-5
	2	20060203548	A1	2006-09-14	Byoung Sung YOU	Abstract, claims 1-2 and figure 4
	3	20050240838	A1	2005-10-27	Hitoshi IWAI	Abstract, claim1 and figure 1

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13105798
	Filing Date	2011-05-11
	First Named Inventor	Ian Shaeffer
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	R-RA0764.P.US

If you wish to add additional Foreign Patent Document citation information please click the Add button			Add
NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐
If you wish to add additional non-patent literature document citation information please click the Add button			Add

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13105798
	Filing Date	2011-05-11
	First Named Inventor	Ian Shaeffer
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	R-RA0764.P.US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	A. Richard Park	Date (YYYY-MM-DD)	2011-12-14
Name/Print	/A. Richard Park/	Registration Number	41,241

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Inventor:	Ian Shaeffer et al.
Title:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
Filing Date:	11 May 2011
Serial Number:	13/105,798
Group Art Unit:	2189
Examiner:	To be Assigned

Listed below or on an attached Form PTO/SB/08a is information known to applicant(s) and submitted pursuant to 37 C.F.R. §1.56. A copy of each listed publication and foreign patent, except for pending U.S. Patents and published U.S. Applications, is being submitted herewith, along with a concise explanation of information in a foreign language, if any, pursuant to 37 C.F.R. §1.97-1.98.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. If form PTO/SB/08a is enclosed, the Examiner is requested to initial and return it in accordance with MPEP §609.

This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56.

_X_ This statement qualifies under 37 C.F.R. §1.97, subsection (b) because (check all that apply):

__ (1) It is being filed within 3 months of the application filing date.
-- OR --

__ (2) It is being filed within 3 months of entry of a national stage.
-- OR --

_X_ (3) It is being filed before the mail date of the first Office Action on the merits.
-- OR --

__ (4) It is being filed before the mail date of a first Office action after the filing of a request for continued examination under 37 C.F.R. §1.114.

__ This statement qualifies under 37 C.F.R. §1.97, subsection (c), because this statement is being filed after the latest of: (1) three months beyond the filing date of a national application; (2) three months beyond the date of entry of the national stage as set forth in §1.491 in an international application; (3) the mailing date of a first Office action on the merits; or (4) the mail date of a first Office action after the filing of a request for continued examination, but before the mailing date of the earlier of a final office action

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Ex. 1050, p. 72

under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, and this statement is accompanied by one of:

__ a certification as specified in §1.97(e) is provided below; **or**

__ a fee of $180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

__ This statement qualifies under 37 C.F.R. §1.97, subsection (d), because this statement is being filed after the mailing date of the earlier of a final office action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution, but is filed on or before payment of the issue fee, and this statement is accompanied by:

__ a certification as specified in §1.97(e) is completed below; **and**

__ a fee of $180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

__ This statement is being filed after the payment of the issue fee but before issuance of the patent.

__ Statement under 37 C.F.R. 1.97(e) - I hereby certify that either:

(1) That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

(2) That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement.

Signature: _____

Respectfully submitted,

By: /A. Richard Park/
A. Richard Park
Reg. No. 41,241

PARK, VAUGHAN, FLEMING and DOWLER LLP
2820 Fifth Street
Davis, CA 95618-7759
Tel: (530) 759-1660
Fax: (530) 759-1665
Email: richard@parklegal.com
Date: 14 December 2011

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Ex. 1050, p. 73

Electronic Acknowledgement Receipt

EFS ID:	11616081
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	68325
Filer:	A.Richard Park/Joanne Swedlow
Filer Authorized By:	A.Richard Park
Attorney Docket Number:	R-RA0764.P.US
Receipt Date:	15-DEC-2011
Filing Date:	11-MAY-2011
Time Stamp:	13:23:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Authorization-deposit-account.pdf	22256 63612c2bcd3913978f7c648062b088855e94c0b9	no	1

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Form (SB08)	IDS_Form__SB_08a.pdf	612334 c70c8f109c1d499e4f960c4b947fb98c8c244f75	no	4
Warnings:					
Information:					
3	Transmittal Letter	IDS_Certification_Statement.pdf	100991 291ce09edc0a9c06a49adc067ef57d2987b531e4	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	735581	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13105798
	Filing Date	2011-05-11
	First Named Inventor	Ian Shaeffer
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	R-RA0764.P.US

	1	"1Gb(32Mx32) GDDR5 SGRAM H5GQ1H24AFR", Hynix Semiconductor, Rev. 1.0, Nov. 2009	☐
	2	"GDDR5 SGRAM", JESD212, JEDEC Solid State Technology Association, December 2009	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13105798
	Filing Date	2011-05-11
	First Named Inventor	Ian Shaeffer
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	R-RA0764.P.US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	A. Richard Park	Date (YYYY-MM-DD)	2012-01-10
Name/Print	/A. Richard Park/	Registration Number	41,241

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Inventor:	Ian Shaeffer et al.
Title:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
Filing Date:	11 May 2011
Serial Number:	13/105,798
Group Art Unit:	2189
Examiner:	To be Assigned

Listed below or on an attached Form PTO/SB/08a is information known to applicant(s) and submitted pursuant to 37 C.F.R. §1.56. A copy of each listed publication and foreign patent, except for pending U.S. Patents and published U.S. Applications, is being submitted herewith, along with a concise explanation of information in a foreign language, if any, pursuant to 37 C.F.R. §1.97-1.98.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. If form PTO/SB/08a is enclosed, the Examiner is requested to initial and return it in accordance with MPEP §609.

This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in §1.56.

_X_ This statement qualifies under 37 C.F.R. §1.97, subsection (b) because (check all that apply):

__ (1) It is being filed within 3 months of the application filing date.
-- OR --

__ (2) It is being filed within 3 months of entry of a national stage.
-- OR --

_X_ (3) It is being filed before the mail date of the first Office Action on the merits.
-- OR --

__ (4) It is being filed before the mail date of a first Office action after the filing of a request for continued examination under 37 C.F.R. §1.114.

__ This statement qualifies under 37 C.F.R. §1.97, subsection (c), because this statement is being filed after the latest of: (1) three months beyond the filing date of a national application; (2) three months beyond the date of entry of the national stage as set forth in §1.491 in an international application; (3) the mailing date of a first Office action on the merits; or (4) the mail date of a first Office action after the filing of a request for continued examination, but before the mailing date of the earlier of a final office action

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Ex. 1050, p. 80

under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application, and this statement is accompanied by one of:

__ a certification as specified in §1.97(e) is provided below; **or**

__ a fee of $180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

__ This statement qualifies under 37 C.F.R. §1.97, subsection (d), because this statement is being filed after the mailing date of the earlier of a final office action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution, but is filed on or before payment of the issue fee, and this statement is accompanied by:

__ a certification as specified in §1.97(e) is completed below; **and**

__ a fee of $180.00 as set forth in §1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.

__ This statement is being filed after the payment of the issue fee but before issuance of the patent.

__ Statement under 37 C.F.R. 1.97(e) - I hereby certify that either:

(1) That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

(2) That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement.

Signature: _____

Respectfully submitted,

By: /A. Richard Park/
A. Richard Park
Reg. No. 41,241

PARK, VAUGHAN, FLEMING and DOWLER LLP
2820 Fifth Street
Davis, CA 95618-7759
Tel: (530) 759-1660
Fax: (530) 759-1665
Email: richard@parklegal.com
Date: 10 January 2012

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Electronic Acknowledgement Receipt

EFS ID:	11800455
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	68325
Filer:	A.Richard Park/Joanne Swedlow
Filer Authorized By:	A.Richard Park
Attorney Docket Number:	R-RA0764.P.US
Receipt Date:	13-JAN-2012
Filing Date:	11-MAY-2011
Time Stamp:	14:06:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Authorization-deposit-account.pdf	22256 63612c2bcd3913978f7c648062b088855e94c0b9	no	1

Warnings:	
Information:	

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2	Information Disclosure Statement (IDS) Form (SB08)	IDS_Form__SB_08a.pdf	612243 01afbf43e5651f8584a6c1cdd84d3c288b89796b	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
3	Transmittal Letter	IDS_Certification_Statement.pdf	101204 eca4c4347d6ca43a368a6a5a528ad85eab52f4e9	no	2
Warnings:					
Information:					
4	Non Patent Literature	H5GQ1H24AFRoptimized.pdf	3240748 93af92b8af72bceb3a00512c905e91375580a1e2	no	173
Warnings:					
Information:					
5	Non Patent Literature	JedecStandardoptimized.pdf	2669808 e1d09bfd0f8b29e259fb187ec22b2b59275d8eff	no	136
Warnings:					
Information:					
			Total Files Size (in bytes):	6646259	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/105,798	05/11/2011	Ian Shaeffer	R-RA0764.P.US

CONFIRMATION NO. 3982

68325
PVF -- RAMBUS, INC.
c/o PARK, VAUGHAN, FLEMING & DOWLER LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

PUBLICATION NOTICE

OC000000052213903

Title:PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

Publication No.US-2012-0023363-A1
Publication Date:01/26/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 78408

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 78408

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Rambus Inc.
1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	3/22/11
Name	Wayne Sobon, Esq.	Telephone	408 462-8000
Title	Vice-President, Corporate Counsel, Rambus Inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	13491976
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	68325
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	R-RA0764.P.US
Receipt Date:	14-AUG-2012
Filing Date:	11-MAY-2011
Time Stamp:	14:10:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73(b).	sb0096-RA764.pdf	45524 b4b22849fb36a1fd127b7411e2519bc73d71e6b5	no	1

Warnings:	
Information:	

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2	Power of Attorney	4-2011-07-22-Rambus-General-POA-Customer-No-78408.pdf	369569 c41e0c2b4c551970e1e8517c946c243151de941f	no	1

Warnings:	
Information:	
Total Files Size (in bytes):	415093

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/96 (10-07)
Approved for use through 10/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Ian Shaeffer et al.

Application No./Patent No.: 13/105798 Filed/Issue Date: 11 May 2011

Entitled: PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

Rambus Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is_____ %)

in the patent application/patent identified above by virtue of either:

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 024949, Frame 0654, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☑ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.,* a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Marc P. Schuyler/	14 August 2012
Signature	Date
Marc P. Schuyler, Reg. No. 35675	4086556375
Printed or Typed Name	Telephone Number
Attorney for Applicants	
Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/105,798	05/11/2011	Ian Shaeffer	R-RA0764.P.US

CONFIRMATION NO. 3982

78408
MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

POA ACCEPTANCE LETTER

OC000000056029760

Date Mailed: 08/17/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/14/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tpetros/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Samsung Electronics Co., Ltd.
Ex. 1050, p. 89

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/105,798	05/11/2011	Ian Shaeffer	R-RA0764.P.US

CONFIRMATION NO. 3982

POWER OF ATTORNEY NOTICE

68325
PVF -- RAMBUS, INC.
c/o PARK, VAUGHAN, FLEMING & DOWLER LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

OC000000056029722

Date Mailed: 08/17/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/14/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/tpetros/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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Ex. 1050, p. 90

Substitute for form 1449/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	**Application Number**	13/105,798
	Filing Date	05/11/2011
	First Inventor	SHAEFFER, Ian
	Art Unit	2189
	Examiner	
Sheet 1 of 1	**Atty Docket #**	
	Rambus #	RA764.P.US

US Patent Documents						
Examiner Initials*	Cite No.	Document No.	Date (MM-DD-YYYY)	Patentee	Class	Subclass
	0023208	2004-0022088	02/05/2004	Schaefer, Scott	G11C	8/00
	0027357	2004-0052151	03/18/2004	Jacobs et al.	365	233
	0027358	2006-0015683	01/19/2006	Ashmore et al.	711	113
	0027359	2006-0083081	04/20/2006	Park et al.	365	191
	0027360	2007-0042758	02/22/2007	Bozzone, Stephen	455	413
	0027355	5566203	10/15/1996	Brief et al.	375	211
	0009607	6600681	07/29/2003	Korger et al.	365	193
	0027356	6819599	11/16/2004	Schaefer, Scott	365	189.07
	0023211	7606089	10/20/2009	Joo, Yong Suk	365	193
	0027354	8054928	11/08/2011	Macri et al.	375	356

Non-Patent Literature Documents			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T**
	0022821	PCT Search Report and the Written Opinion dated 11/30/2011 re Int'l. Application No. PCT/US2011/040690. 9 Pages	

Examiner Signature:		**Date Considered:**	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. **Applicant is to place a check mark here if English language Translation is attached.			

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

SAHASRABUDDHE LAXMAN

2820 FIFTH STREET DAVIS CA 95618 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference RA0764FPCT	Date of mailing *(day/month/year)* 30 NOVEMBER 2011 (30.11.2011) **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2011/040690**	International filing date *(day/month/year)* **16 JUNE 2011 (16.06.2011)**
Applicant **RAMBUS INC. et al**	

DEC 12 2011 BY:

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8752

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **9DY4RNJR**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
RA0764FPCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/040690	**16 JUNE 2011 (16.06.2011)**	22 JULY 2010 (22.07.2010)

Applicant

RAMBUS INC. et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. **1A**
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/040690

A. CLASSIFICATION OF SUBJECT MATTER

G11C 7/22(2006.01)i, G11C 7/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC : G11C, H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: read, command, prior, contain, timing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0205187 A1 (PYEON) 28 August 2008 See abstract, claim 1 and figures 4-5.	1-45
A	US 2006-0203548 A1 (YOU) 14 September 2006 See abstract, claims 1-2 and figure 4.	1-45
A	US 2005-0240838 A1 (IWAI) 27 October 2005 See abstract, claim 1 and figure 1.	1-45

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 NOVEMBER 2011 (30.11.2011)	**30 NOVEMBER 2011 (30.11.2011)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 189 Cheongsa-ro,
Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

YOON, Nan Young

Telephone No. 82-42-481-8188

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/040690

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0205187 A1	28.08.2008	US 7796462 B2	14.09.2010
US 2006-0203548 A1	14.09.2006	JP 2006-252747 A	21.09.2006
		JP 2011-192385 A	29.09.2011
		KR 10-0590388 B1	08.06.2006
		US 2009-0238005 A1	24.09.2009
US 2005-0240838 A1	27.10.2005	JP 2005-310313 A	04.11.2005

Samsung Electronics Co., Ltd.
Ex. 1050, p. 96

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
SAHASRABUDDHE LAXMAN

2820 FIFTH STREET DAVIS CA 95618 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**30 NOVEMBER 2011 (30.11.2011)**
Applicant's or agent's file reference: RA0764FPCT	**FOR FURTHER ACTION**: See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/040690	**16 JUNE 2011 (16.06.2011)**	22 JULY 2010 (22.07.2010)

International Patent Classification (IPC) or both national classification and IPC

G11C 7/22(2006.01)i, G11C 7/10(2006.01)i

Applicant

RAMBUS INC. et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [x] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	30 NOVEMBER 2011 (30.11.2011)	YOON, Nan Young Telephone No.82-42-481-8188

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/040690

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/040690

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-45	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-45	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-45	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0205187 A1 (PYEON) 28 August 2008
D2: US 2006-0203548 A1 (YOU) 14 September 2006
D3: US 2005-0240838 A1 (IWAI) 27 October 2005

1. Novelty and Inventive Step

The subject matters of claims 1, 14, 21, 30 and 42 differ from these prior art documents in that they comprise a read command containing information which specifies whether the memory device is to commence outputting of a timing reference signal prior to commencing outputting of the data. And they are not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claims 1, 14, 21, 30 and 42 meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

Claims 2-13, 15-20, 22-29, 31-41 and 43-45 are dependent on claim 1, 14, 21, 30 and 42 respectively, and therefore meet the requirements of PCT Article 33(2) and (3).
(It is considered that claim 12 is dependent on claim 1, and claim 37 is dependent on claim 30.)

2. Industrial Applicability

Claims 1-45 are industrially applicable under PCT Article 33(4).

Samsung Electronics Co., Ltd.
Ex. 1050, p. 99

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2011/040690

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim 21 relates to a method for operation of a memory device, but claim 37 dependent on claim 21 relates to a memory device. As claim 37 does not clearly define the matter for which protection is sought, this claim does not meet the requirement of PCT Article 6.

Claim 12 does not meet the requirements of PCT Article 6 because there is a writing error, and the term of "The method 1" of claim 12 is considered to be replaced with "The method of claim 1" for clarity.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 100

Electronic Acknowledgement Receipt

EFS ID:	14181414
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	08-NOV-2012
Filing Date:	11-MAY-2011
Time Stamp:	14:31:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	RA764PIDS-2012-11-08.pdf	41870 8a7cf64dfaa176e47691a1d00dfd78620137a1c9	no	1

Warnings:	
Information:	

Samsung Electronics Co., Ltd.
Ex. 1050, p. 101

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	0022821.pdf	372196 29775f6b12f8c17d4258acd89550a99c3c3f9c0e	no	9
Warnings:					
Information:					
			Total Files Size (in bytes):	414066	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 06/06/2013

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
06/06/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/105,798	Applicant(s) SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8 November 2012*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-45* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-45* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/15/2011, 01/13/2012, 11/08/2012*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 104

DETAILED ACTION

Claim Objections

1. Claim 37 is objected to because of the following informalities: Claim 37 is recited as "memory device of claim 21." Examiner assumes this is a typographic error and believed to be device of claim 30. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 14-17, 21-23, 28-30, 35, and 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (US 20100220536, filed Feb. 27, 2009) in view of Best (US 20100091537, published Apr. 15, 2010)

Claims 1 and 14, Coteus (20100220536) discloses a method of operation in a memory controller (e.g., memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device, see para 0057), the method comprising:

transmitter circuit, transmitting a read command which specifies that a memory device output data accessed from a memory core (e.g., memory controller 602 generates a core clock 604 for distribution to all memory devices 610 to capture information sent to memory devices, para 0068-0069; reading data from ranks, para 0058, 0069), the read command containing information which specifies whether the memory device is to commence outputting of a timing

reference signal prior to commencing outputting of the data (e.g., adjust the vernier or passively controlled delay line within memory device(s) periodically to permit data transfers to be completed between different ranks by controlling the time which each memory device transfers data, 0058; variable delay lines VDLs 702 cause data to be returned from each rank at a specific time relative to core clock 604 where controller 602 adjusts the amount of delay to synchronize to clock 604 with delay value to capture read data from each rank, see para 0069; Coteus' DQS strobe 1808 is interpreted as corresponding to the claimed 'timing reference signal', see para 0076); and

receiver circuit, receiving the timing reference signal if the information specified that the memory device output the timing reference signal (e.g., data receiver 212, para 0064; receiving a clock signal at a receiving device, and data strobe signals in response to read command, see para 0089, Fig. 22; adjusting data strobe preamble time for adjusting data transfer speed, 0059),

Coteus does not expressly disclose, but Best discloses wherein the memory controller samples the data output from the memory device based on information provided by the timing reference signal output from the memory device (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 2. Coteus does not expressly disclose, but Best discloses wherein the memory controller samples the data output from the memory device using the timing reference signal if the information specified that the memory device output the timing reference signal (e.g., interface die 421 outputs demand signal to storage die 423 and timing reference for initiating data transmission ... delayed timing signal output yields a sampling signal (s) that triggers

sampling operation within data receiver 432 to sample read data from storage-die transmitter 430, para 0060, Fig. 11).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 3. Coteus does not expressly disclose, but Best discloses wherein the memory controller samples the data output from the memory device using a sampling clock wherein, the method further comprising adjusting the sampling clock based on phase information derived from the timing reference signal (e.g., internal clock signal is used to sample command signals conveyed via command path 108 in conjunction with read data. timing circuitry includes phase adjustment to enable phase offset between internal clock signal and reference clock corresponding to incoming data strobe signals, see para 0038, Fig. 1).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of providing source-synchronous timing reference (para 0038) for scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 4. Coteus discloses after receiving the timing reference signal, receiving an error detection and correction (EDC) signal from the memory device, wherein a first bit of the EDC signal is received after a first bit of the read data; and using the EDC signal to further update the phase of the internal receive clock after the timing reference signal (e.g., transferring cyclical redundancy code CRC bits 2402 during preamble time 1810 of data strobe 1808 read from memory device to determine if error is present in received data, see para 0091, Fig. 24; error detection information is transferred in addition to data, para 0059; preamble time 1810 will vary based on factors (like EDC bits), see para 0087, Fig. 20).

Claim 5. Coteus discloses wherein the read command further includes information that specifies a burst length of the timing reference signal (e.g., effective burst length 3102 during preamble time 1810, see para 0096, Fig. 29-31).

Claim 6. Coteus discloses determining a duration of an idle period that transpires prior to transmitting the read command to the memory device (e.g., preamble time 1810 is required prior to completing read transfer, para 0086, Fig. 19); and
selecting the information that specifies the burst length based on the duration of the idle period (e.g., preamble bits are transferred during preamble time 1810, Fig. 21, para 0088, 0089, Figs 21 and 22).

Claim 15. Coteus does not expressly disclose, but Best discloses a circuit, coupled to the receiver circuit, to generate a sampling clock used to sample the data output from the memory device, the circuit to adjust the sampling clock based on phase information derived from the timing reference signal (e.g., internal clock signal used to sample command signals via command path 108 and generate strobe signals in conjunction with read data, see para 0038).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 16. Coteus discloses a receiver circuit to receive an error detection and correction (EDC) signal from the memory device; and a circuit to update the sampling clock based on information derived from the EDC signal (e.g., transferring cyclical redundancy code CRC bits 2402 during preamble time 1810 of data strobe 1808 read from memory device to determine if error is present in received data, see para 0091, Fig. 24; error detection information is transferred in addition to data, para 0059; preamble time 1810 will vary based on factors (like EDC bits), see para 0087, Fig. 20).

Coteus does not expressly disclose, but Best discloses a circuit, sampling clock (e.g., internal clock signal used to sample command signals via command path 108 and generate strobe signals in conjunction with read data, see para 0038).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 17 is rejected for reasons similar to Claim 5 (see above).

Claims 21 and 30. Coteus discloses a memory device (e.g., memory devices 610 Rank A, Rank B, see Fig. 7), comprising:

a receiver circuit to receive a read command (e.g., memory controller sends read commands 804 to memory devices 610 and core clock 604, data clock 606A, 606B, directed to data on a memory device rank 610, para 0070, Fig. 8), wherein the read command includes information that specifies whether to precede outputting of data associated with the read command with a timing reference signal (e.g., controller 602 sends time relationships of data clock 606A to core clock 604, para 0070); and

a transmitter circuit to output the timing reference signal (e.g., a preamble state from a transmitting device via a data bus, para 0005, where preamble time 1810 is required prior to completing read transfers to allow the data strobe 1808 to achieve stable switching state, para 0086, Fig. 19).

Coteus does not expressly disclose, but Best discloses according to the information; wherein a memory controller samples data output from memory device based on information provided by timing reference signal output from memory device (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 22. Coteus discloses generating an error detection and correction signal; and after transmitting the timing reference signal, transmitting the EDC signal, wherein a first bit of the EDC signal is transmitted after a first bit of the read data is output (e.g., transferring cyclical redundancy code CRC bits 2402 during preamble time 1810 of data strobe 1808 read from memory device to determine if error is present in received data, see para 0091, Fig. 24; error detection information is transferred in addition to data, para 0059; preamble time 1810 will vary based on factors (like EDC bits), see para 0087, Fig. 20).

Claim 23 is rejected for reasons similar to Claim 5 (see above).

Claim 28. Coteus does not expressly disclose, but Best discloses wherein the memory controller uses phase information provided by the timing reference signal output from the memory device to adjust a phase of an internal sampling clock used to sample data provided by the memory device (e.g., phase adjustment circuitry to enable desired phase offsets between internal clock signal and reference clock signal or between data signal sampling times in corresponding incoming data strobe signals, see para 0038, Fig. 1).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 29. Coteus discloses transmitting a timing reference signal based on a state of an internal state machine (e.g., data strobe signal driven by transmitting device in a preamble state, para 0005; state diagram showing various states for a memory device, para 0098, Fig. 32).

Claim 35 is rejected for reasons similar to Claim 5 (see above).

Claim 40. Coteus discloses a register that specifies a timing interval between the outputting of the timing signal and outputting a first bit of the data (e.g., output data at a time responsive to delayed clock, para 0004, Fig. 40).

Claim 41. Coteus discloses a register that specifies a timing interval to occur between outputting a first bit of the data and transmitting an error detection code, the error detection code corresponding to the data (e.g., mode register 1408 generates digital bits in response to MRS command to delay clock, para 0080, Fig. 14).

Claim 42. Coteus discloses a memory system (e.g., memory system, Fig 6, para 0014), comprising:
a memory device (e.g., memory device 610 Rank A, Rank B, Fig. 6, 0068) and a memory controller (e.g., memory controller 602, 0068, Fig. 6);
a first interconnect to carry a read command from the memory controller to the memory device, the read command including information which specifies whether the memory device is to commence output of a timing reference signal
prior to commencing outputting of the data (e.g., memory controller 602 controls and adjusts time relationship of data clock 606A to core clock 604 for read commands, para 0070, Fig. 7, 8; MRS commands 1418 from memory controller 1420 to memory device 1402 to adjust the data delay, para 0080, Fig. 14); and
a second interconnect to convey the timing reference signal from the memory device to the memory controller (e.g., data bus 608 including clocking circuitry and data received from memory rank A and rank B with variations in time, para 0068, Fig. 6)(e.g., synchronizing output on data bus 608 to core clock by adjusting timing of data clocks 606 where transmission of burst of four data bits from rank A is started on data bus 608 at a time determined by data clock A 606A, adjusted by memory controller 602, para 0070, Fig. 8).

Coteus does not expressly disclose, but Best discloses

wherein the timing reference signal is used to adjust memory controller receive timing of the data output from the 10 memory device (e.g., sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of providing a source-synchronous timing reference for establishing a read-data sampling time with external memory controller (see best , para 0038) and scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 43. Coteus discloses a plurality of ranks, wherein the memory device is disposed a rank in the plurality of ranks wherein the memory controller specifies that the memory device output the timing reference signal associated with the read command after a predetermined idle period transpires for the rank (e.g., memory devices 610 where memory controller 602 generates core clock to all memory devices in rank A and rank B... to adjust timing of data clocks to each memory device rank to avoid data contention, as data bus 608 sends data to memory controller 602, see para 0068, Fig. 6),

Claim 44. Coteus discloses wherein the memory controller specifies that a memory device from each rank of the plurality of ranks output a timing signal periodically in accordance with a corresponding predetermined idle duration for each rank of the plurality of ranks (e.g., controller adjust vernier or passively controlled delay line within memory devices periodically to permit data transfer between different ranks of memory devices by controlling time at which each memory device transfers data, para 0058).

Claim 45. Coteus discloses wherein the memory controller schedules read accesses to the plurality of ranks such that a memory device from each rank of the plurality of ranks outputs a timing signal, during each read access, such that a predetermined threshold idle period for each rank is not exceeded (e.g., dead time (preamble time) increases or decreases due to data valid

time, para 0059; preamble time is time it takes certain amount of time for the data strobe to go from idle state to stable switching state, para 0085, Fig. 18).

4. Claims 7, 8, 18, 20, 24, 27, 31, 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (cited above) in view of Best (cited above), and further in view of Park (US 2006/0083081, published Apr. 20, 2006)

Claim 7. Coteus in view of Best does not expressly disclose, but Park discloses transmitting a command, to the memory device, that specifies storing a value in a register of the memory device, the value being representative of a burst length of the timing reference signal (e.g., register 14-3 receives signal to generate preamble cycle signal PREC2 in response to read signal RD2 which may be enabled after three cycles and the burst length BL, para 0076, Fig. 4B, 5).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 8. Coteus in view of Best does not expressly disclose, but Park discloses wherein a burst length of the timing reference signal is the same as a burst length of the data (e.g., delay of a cycle corresponding to the burst length (2 cycles), see para 0076) .
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 18 is rejected for reasons similar to Claim 7 (see above).

Claim 20. Coteus in view of Best does not expressly disclose, but Park discloses wherein the transmitter circuit provides a command which specifies that the memory device output a timing reference signal having a predetermined burst length (e.g., burst length is fixed, see para 0082). It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 24. Coteus in view of Best does not expressly disclose, but Park discloses receiving a command that specifies storing a value in a register of the memory device, the value being representative of a burst length of the timing reference signal (e.g., register 14-3 receives signal to generate preamble cycle signal PREC2 in response to read signal RD2 which may be enabled after three cycles and the burst length BL, para 0076, Fig. 4B, 5).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 27. Coteus in view of Best does not expressly disclose, but Park discloses receiving a command which specifies that the memory device output a timing reference signal having a predetermined burst length; and transmitting the timing reference signal in response to the command which specifies that the memory device output the timing reference signal (e.g., generating a preamble cycle signal based on calculated preamble cycle number where the burst length was set, in response to mode setting signal, para 0018; set the burst length signal to a high level or low level, para 0038; fixed burst length and generating a delay corresponding to fixed burst length, para 0082).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of

Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 31. Coteus in view of Best does not expressly disclose, but Park discloses comprising a first register to store a value that is representative of a first burst length of the timing reference signal (e.g., register 14-3 may receive signal 0001 to generate preamble cycle, where burst length BL may be corresponding to two cycles, para 0076).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

Claim 36 is rejected for reasons similar to Claim 24 (see above).
Claim 37 is rejected for reasons similar to Claim 27 (see above).

Claim 38. Coteus in view of Best does not expressly disclose, but Park discloses wherein the receiver circuit receives a command which specifies that the memory device output a timing reference signal having a predetermined burst length (e.g., burst length is fixed, see para 0082).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Park providing the benefit of reducing or preventing collisions between strobe signal and preamble signal during read operation (see Park, para 0010).

5. Claims 9, 12, 13, 26, 34, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (cited above) in view of Best (cited above), and further in view of Kim (US 2011/00556671, filed Sep. 3, 2009)

Claim 9. Coteus in view of Best does not expressly disclose, but Kim discloses determining whether the memory device is to be accessed after a predetermined idle period for the memory

device transpires (e.g., determining that memory device is in an idle state, and if determined that a command has been received and is a memory access command, then memory operation is performed, para 0085, Fig. 9); and

specifying that the memory device output the timing reference signal associated with the read command based on the predetermined idle period transpiring (e.g., variations in programmable preamble time so that preamble time is selected based on current conditions following read operations, see para 0108, Fig. 23; where memory device waits unit DQS is stable before transferring data, para 0109, Fig. 24).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

Claim 12. Coteus in view of Best does not expressly disclose, but Kim discloses detecting that a predetermined time period has transpired in which an operational state of a memory device is idle (e.g., static preambles where static state prior to start of data transfer, see para 0109, Fig. 24); transmitting a command which specifies that the memory device output a timing reference signal having a predetermined burst length (e.g., static preamble time, para 0109, Fig. 24).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

Coteaus does not expressly disclose, but Best discloses receiving the timing reference signal, wherein the memory controller uses phase information provided by the timing reference signal output from the memory device to adjust a phase of an internal sampling clock used to sample data provided by the memory device (e.g., phase adjustment circuitry to enable desired phase offsets between internal clock signal and reference clock signal or between data signal sampling times in corresponding incoming data strobe signals, see para 0038, Fig. 1).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 13. Coteus in view of Best does not expressly disclose, but Kim discloses wherein the predetermined time period is detected directly prior to transmitting a write command to the memory device (e.g., preamble time where write operation are followed by read commands, see para 0108).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

Claim 26. Coteus in view of Best does not expressly disclose, but Kim discloses detecting that a predetermined time period has transpired in which an operational state of a memory device is idle (e.g., static preambles where static state prior to start of data transfer, see para 0109, Fig. 24); and transmitting a timing reference signal after detecting that the predetermined time period has transpired (e.g., preamble time when memory device waits until DQS is stable before transferring data, see para 0109, Fig. 24).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

Claim 34. Coteus discloses output the data; and output an error detection and correction signal after a first bit of the read data is output by the first transmitter circuit (e.g., error detection information to be transferred in addition to data, see para 0059).

Coteus in view of Best does not expressly disclose but Kim discloses a first transmitter circuit and a second transmitter circuit (e.g., Array controller block 1306 transmits data and parity check block 1308 transmits error, see Fig. 15).
It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

Claim 39. Coteus in view of Best does not expressly disclose but Kim discloses comprising a register that specifies whether the transmitter circuit provides one of the timing reference signal in a first mode and an error detection code in a second mode (e.g., error control coding circuitry for performing error control checking on received command, para 0004, 0089; programmable preamble control circuitry, para 0005).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of reducing power consumption by synchronizing a DLL in memory device on a periodic basis (see Kim, para 0066).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (cited above) in view of Best (cited above), and further in view of Kim (cited above) and Schaefer (US 6819599, issued Nov. 16, 2004)

Claim 10. Coteus in view of Best and Kim does not expressly disclose, but Schaefer discloses wherein the predetermined idle period is of a first duration (e.g., time length of preamble with default value, see col 7, line 30-33), the method further comprising: detecting that the memory device is to be accessed after an idle period transpires that includes a duration longer than the

first duration (e.g., if preamble longer than the default value, the format of bits can be used to program a preamble to a multiple of the default preamble, col 7, lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, and Kim with Schaefer, providing the benefit of reducing a preamble window by delaying the beginning of the data strobe preamble (see Schaefer, col 3, lines 15-19).

Coteus in view of Best does not expressly disclose, but Kim discloses
specifying that the memory device output a subsequent timing reference signal having a burst length that is longer than a burst length of the timing reference signal associated with the read command based on the predetermined idle period transpiring (e.g., programmable preamble with timing adjustments to periodic recalibration affecting the time at which DQS signal is sent (e.g., relative to data), para 0112, Fig. 27)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, with Kim, providing the benefit of ease of upgrade and reduced system environmental impact (such as space, power, and cooling) (see Kim, para 0003).

7. Claims 11, 19, 25, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (cited above) in view of Best (cited above), and further in view of Schaefer (cited above)

Claim 11. Coteus in view of Best does not expressly disclose, but Schaefer discloses wherein the information identifies a selected programmable register from a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal (e.g., controller programs a mode registers in each memory device 204_1 - 204_n with burst length, col 4, lines

60-65; including data representing time length for the DQS preamble of memory, col 7, lines 43-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, and Kim with Schaefer, providing the benefit of reducing a preamble window by delaying the beginning of the data strobe preamble (see Schaefer, col 3, lines 15-19).

Claim 19 is rejected for reasons similar to Claim 11 (see above).
Claim 25 is rejected for reasons similar to Claim 11 (see above).

Claim 33. Coteus in view of Best does not expressly disclose, but Schaefer discloses a plurality of programmable registers, disposed on the memory device, that store a corresponding plurality of burst length values that define a selected burst length for the timing reference signal wherein the information further selects a burst length value for the timing reference signal by addressing a corresponding register of the plurality of registers (e.g., loading one or more registers 304 includes loading registers with at least one bit indicating selecting DQS preamble greater than default DQS preamble, see col 9, lines 36-57, Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, and Park with Schaefer, providing the benefit of reducing a preamble window by delaying the beginning of the data strobe preamble (see Schaefer, col 3, lines 15-19).

8. Claims 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (cited above) in view of Best (cited above), and further in view of Park (cited above) and Schaefer (cited above)

Claim 32. Coteus in view of Best and Park does not expressly disclose, but Schaefer discloses a second register to store a value that is representative of a second burst length of the timing reference signal, wherein the information specifies at least one of the first and second burst lengths for the timing reference signal output by the transmitter, by selecting at least one of the first and second registers, wherein the transmitter circuit outputs the timing reference signal having a burst length as selected by at least the first and second register (e.g. one or more registers 304 to provide control information to delay element 308 to provide timing delay that reduces the DQS preamble of memory 300 to a shorter period than a default value for the DQS preamble, see col 5, lines 38-58, Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus in view of Best, and Park with Schaefer, providing the benefit of reducing a preamble window by delaying the beginning of the data strobe preamble (see Schaefer, col 3, lines 15-19).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GAUTAM SAIN whose telephone number is (571)270-3555. The examiner can normally be reached on Monday - Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GAUTAM SAIN
Examiner
Art Unit 2185

GS

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185

Notice of References Cited	Application/Control No. 13/105,798	Applicant(s)/Patent Under Reexamination SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,819,599	11-2004	Schaefer, Scott	365/189.07
*	B	US-2010/0220536	09-2010	Coteus et al.	365/193
*	C	US-2011/0055671	03-2011	Kim et al.	714/800
*	D	US-2010/0091537	04-2010	Best et al.	365/51
*	E	US-6,819,599	11-2004	Schaefer, Scott	365/189.07
*	F	US-2006/0083081	04-2006	Park et al.	365/191
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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	P					
	Q					
	R					
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet 1 of 1

Complete if Known	
Application Number	13/105,798
Filing Date	05/11/2011
First Inventor	SHAEFFER, Ian
Art Unit	2189
Examiner	
Atty Docket #	
Rambus #	RA764.P.US

US Patent Documents

Examiner Initials*	Cite No.	Document No.	Date (MM-DD-YYYY)	Patentee	Class	Subclass
/GS/	0023208	2004-0022088	02/05/2004	Schaefer, Scott	G11C	8/00
/GS/	0027357	2004-0052151	03/18/2004	Jacobs et al.	365	233
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/GS/	0027359	2006-0083081	04/20/2006	Park et al.	365	191
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/GS/	0023211	7606089	10/20/2009	Joo, Yong Suk	365	193
/GS/	0027354	8054928	11/08/2011	Macri et al.	375	356

Non-Patent Literature Documents

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T**
/GS/	0022821	PCT Search Report and the Written Opinion dated 11/30/2011 re Int'l. Application No. PCT/US2011/040690. 9 Pages	

Examiner Signature:	/Gautam Sain/ (05/31/2013)	Date Considered:	

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CONFIRMATION NO. 3982

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/105,798	05/11/2011	711	2185	2012043 / RA764.P.US

APPLICANTS

Ian Shaeffer, Los Gatos, CA;
Thomas J. Giovannini, San Jose, CA;

**** CONTINUING DATA ****************************

This appln claims benefit of 61/366,806 07/22/2010

**** FOREIGN APPLICATIONS ****************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/31/2011

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /GAUTAM SAIN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	7	45	5

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
see attached EAST search history	5/31/2013	gs

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/G.S./ Examiner.Art Unit 2185	

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Ex. 1050, p. 127

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13105798 13105798 - GAU: 2185
	Filing Date	2011-05-11
	First Named Inventor	Ian Shaeffer
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	R-RA0764.P.US

/GS/	1	"1Gb(32Mx32) GDDR5 SGRAM H5GQ1H24AFR", Hynix Semiconductor, Rev. 1.0, Nov. 2009	☐
/GS/	2	"GDDR5 SGRAM", JESD212, JEDEC Solid State Technology Association, December 2009	☐

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Examiner Signature	/Gautam Sain/ (05/31/2013)	Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798 13105798 - GAU: 2185
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	A. Richard Park	Date (YYYY-MM-DD)	2012-01-10
Name/Print	/A. Richard Park/	Registration Number	41,241

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Ex. 1050, p. 129

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Ex. 1050, p. 130

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/GS/	1	20080205187	A1	2008-08-28	Hong Beom PYEON	Abstract, claim 1 and figures 4-5
/GS/	2	20060203548	A1	2006-09-14	Byoung Sung YOU	Abstract, claims 1-2 and figure 4
/GS/	3	20050240838	A1	2005-10-27	Hitoshi IWAI	Abstract, claim1 and figure 1

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Ex. 1050, p. 131

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798 13105798 - GAU: 2185
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13105798 13105798 - GAU: 2185
Filing Date	2011-05-11
First Named Inventor	Ian Shaeffer
Art Unit	2189
Examiner Name	
Attorney Docket Number	R-RA0764.P.US

CERTIFICATION STATEMENT

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☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

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Signature	A. Richard Park	Date (YYYY-MM-DD)	2011-12-14
Name/Print	/A. Richard Park/	Registration Number	41,241

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Ex. 1050, p. 133

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Ex. 1050, p. 134

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		S39 and ((burst adj length) and same)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:41
		S39 and ((burst adj length) and same))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
		(error near4 signal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:29
		("error detection" near3 signal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:30
		((error near4 signal) edc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:27
S1	6	("20080205187" "20060203548" "20050240838").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 11:51
S2	22	("200400220088" "20040052151" "20060015683" "20060083081" "20070042758" "5566203" "6600681" "6819599" "7606089" "8054928").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 11:53

EAST Search History (Prior Art)

S3	13	(US-20080205187-$ or US-20060203548-$ or US-20050240838-$ or US-20040052151-$ or US-20060015683-$ or US-20060083081-$ or US-20070042758-$).did. or (US-5566203-$ or US-6600681-$ or US-6819599-$ or US-7606089-$ or US-8054928-$).did. or (US-20040022088-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/05/20 12:11
S4	0	S3 and "timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:11
S5	0	S3 and trs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:11
S6	2633	"timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:12
S7	96	S6 and (read adj command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:12
S8	84	S7 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:13
S9	31	S8 and (preamble (pre adj amble))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:18

EAST Search History (Prior Art)

S10	1	13/105798.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 14:51
S11	2633	"timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S12	96	S11 and (read adj command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S13	84	S12 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S14	63	S13 and sample	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S15	15	("20050082664" | "20050099834" | "20050139977" | "20050189639" | "20050285174" | "20060233012" | "20070005876" | "20070070669" | "20070158825" | "5838603" | "6236602" | "6469945" | "7579683").PN. OR ("8233303").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/20 15:17
S16	3	S11 and edc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:21

EAST Search History (Prior Art)

S17	15	("20050082664" | "20050099834" | "20050139977" | "20050189639" | "20050285174" | "20060233012" | "20070005876" | "20070070669" | "20070158825" | "5838603" | "6236602" | "6469945" | "7579683").PN. OR ("8233303").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/20 15:24
S18	42804	("error detection and correction" edc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S19	32151	("timing reference signal" trs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S20	137	S18 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S21	64	S20 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S22	16	(US-20080205187-$ or US-20060203548-$ or US-20050240838-$ or US-20040052151-$ or US-20060015683-$ or US-20060083081-$ or US-20070042758-$ or US-20100067314-$ or US-20100091537-$ or US-20120023363-$).did. or (US-5566203-$ or US-6600681-$ or US-6819599-$ or US-7606089-$ or US-8054928-$).did. or (US-20040022088-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/05/20 15:56
S23	2	S22 and (sampl$ near2 clock)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:56
S24	13	("2010/0091537").URPN.	USPAT	OR	OFF	2013/05/20 15:59

EAST Search History (Prior Art)

S25	79	"l11" and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 10:25
S26	72	S25 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 10:26
S27	37	("6477110" | "6493285").PN. OR ("6600681").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/28 10:29
S28	2	"20060007760"	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/28 10:35
S29	7	("2006/0083081").URPN.	USPAT	OR	OFF	2013/05/28 11:38
S30	0	"20100124131".pn.	USPAT	OR	OFF	2013/05/28 12:08
S31	2	"20100124131".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 12:08
S32	4768	dqs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:08
S33	477	S32 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:08
S34	437	S33 and read	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:09

EAST Search History (Prior Art)

S35	367	S34 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:09
S36	4772	dqs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S37	478	S36 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S38	438	S37 and read	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S39	367	S38 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S40	60	S39 and ((burst adj length) same register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:41

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	32	✓								
	33	✓								
	34	✓								
	35	✓								
	36	✓								

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								
	44	✓								
	45	✓								

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

APPLICANT RESPONSE TO NON-FINAL OFFICE ACTION/REQUEST FOR RECONSIDERATION

Please consider the materials below in response to the Office Action mailed June 6, 2013.

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AMENDMENT TO THE CLAIMS

Please amend the claims as set forth below. The listing set forth below replaces all prior listings of claims.

1. (Currently Amended) A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data; ~~data accessed from a memory core, the read command containing~~

with the read command, transmitting information which specifies a duration of a preamble ~~whether the memory device is to commence outputting of a timing reference signal~~ that is to be output prior to commencing outputting of the data; ~~and~~

receiving the preamble~~timing reference signal if the information specified that the memory device output the timing reference signal, wherein the memory controller samples~~ ; and

sampling the data output from the memory device ~~based~~in dependence on ~~information provided by~~ the ~~timing reference signal~~ preamble output from the memory device.

2. (Canceled)

3. (Currently Amended) The method of claim 1, wherein the memory controller ~~samples~~is to sample the data output from the memory device using a sampling clock, and ~~wherein,~~ wherein the method further ~~comprising~~comprises ~~adjusting the~~ sampling ~~clock~~ the data based on ~~phase information derived from~~ both the sampling clock and the preamble~~timing reference signal~~.

4. (Currently Amended) The method of claim 3, further comprising:

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after receiving the preamble~~timing reference signal~~, receiving an error detection and correction (EDC) signal from the memory device via a common signal line that is used to convey the preamble, wherein a first bit of the EDC signal is received after a first bit of the read data; and

using the EDC signal to ~~further~~ update ~~the~~ phase of ~~the internal receive~~sampling of the data ~~clock~~ after the receiving the preamble~~timing reference signal~~.

5. (Currently Amended) The method of claim 1, wherein the read command ~~further~~ includes information that specifies a ~~burst~~ length of the preamble~~timing reference signal~~.

6-10. (Canceled)

11. (Currently Amended) The method of claim 1, wherein the information identifies a length for a predetermined time parameter ~~period has transpired in which an operational state of a memory device is idle;~~ associated with the preamble.

12-13. (Canceled)

14. (Currently Amended) A memory controller, comprising:

~~a~~ transmitter ~~circuit~~circuitry to ~~provide~~transmit a read command ~~which specifies that~~to a memory device, the read command being transmitted ~~output data accessed from a memory core, the read command containing~~together with information which specifies which specifies a duration of a preamble that is to be output ~~whether the memory~~

~~device is to commence output of a timing reference signal~~ prior to commencing outputting of the data; and

~~a~~ receiver ~~circuit~~circuitry to receive the preamble ~~timing reference signal wherein~~from the ~~timing reference signal is used to adjust~~ memory ~~controller receive timing of~~device and to sample the data ~~output~~ from the memory device in dependence on the preamble.

15. (Currently Amended) The memory controller of claim 14, further comprising ~~a circuit, coupled to the receiver circuit,~~circuitry to generate a sampling clock ~~used to sample the data output from the memory device, the circuit to adjust the sampling clock based~~, the receiver circuitry operable to sample the data output from the memory device in dependence on the sampling clock and ~~on phase information derived from~~ the ~~timing reference signal.~~ preamble.

16-45. (Canceled)

46. (New) The method of claim 1, wherein the memory controller is operable to control multiple ranks of memory, and wherein the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble in connection with a rank switch in consecutive memory operations and in a manner to specify that the memory device is not to utilize the duration of the preamble if there is no rank switch in the consecutive memory operations.

47. (New) The method of claim 46, wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch.

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48. (New) The method of claim 46, wherein the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

49. (New) The method of claim 1, wherein the preamble comprises a toggling pattern, and wherein the method further comprises using the toggling pattern as a calibration preamble to facilitate sampling of read data from a specific rank.

50. (New) The method of claim 1, wherein transmitting further comprises transmitting the read command to the memory device together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

51. (New) The method of claim 1, wherein transmitting the read command with the information further comprises transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of the data.

52. (New) The method of claim 1, wherein the receiving the preamble includes receiving the preamble from a first set of signaling resources and wherein sampling the data includes sampling the data output by the memory device from a second set of signaling resources.

53. (New) The memory controller of claim 14, wherein:

the memory controller is operable to control multiple ranks of memory; and

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the memory controller is to cause the transmitter circuitry to transmit the information in a manner to specify that the memory device is to utilize the duration in connection with a rank switch in consecutive memory operations and in a manner to specify that the memory device is not to utilize the duration if there is no rank switch in the consecutive memory operations.

54. (New) The memory controller of claim 53, wherein the memory controller is to cause the transmitter circuitry transmit the information in a manner to cause the memory device to output a longer preamble in connection with the rank switch, relative to no rank switch.

55. (New) The memory controller of claim 53, wherein the receiver circuitry is to sample the data output from the memory in a manner dependent on rank-specific phase information derived by the memory controller from the preamble.

56. (New) The memory controller of claim 14, wherein the preamble comprises a toggling pattern, and wherein the memory controller is adapted to use the toggling pattern as a calibration sequence to facilitate sampling of read data from a specific rank.

57. (New) The memory controller of claim 14, wherein the memory controller is operable to cause the transmitter circuitry to transmit the read command together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

58. (New) The memory controller of claim 14, wherein the duration represents a specific length preamble, and wherein the transmitter circuitry is to transmit the information in manner that specifies

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that the memory device should output the specific length preamble prior to commencing outputting of the data.

59. (New) The memory controller of claim 14, wherein the information comprises a digital bit that indicates that the memory device should utilize the duration of the preamble in connection with the outputting of the data.

60. (New) The memory controller of claim 14, wherein the receiver circuitry comprises circuitry to receive the preamble from a first set of signaling resources, and circuitry to sample the data from a second set of signaling resources.

61. (New) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch.

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62. (New) The DRAM memory controller of claim 61, wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch.

63. (New) The DRAM memory controller of claim 61, wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank.

64. (New) The DRAM memory controller of claim 63, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles.

65. (New) The DRAM memory controller of claim 61, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

66. (New) The DRAM memory controller of claim 61, wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data.

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67. (New) The DRAM memory controller of claim 61, wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles.

68. (New) The DRAM memory controller of claim 61, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data.

69. (New) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command.

70. (New) The DRAM memory controller of claim 69, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory.

71. (New) The DRAM memory controller of claim 70, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

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REMARKS

There were previously 5 independent claims and 45 total claims pending; by this response, Applicants have amended the claims to cancel claims 2, 6-10, 12-13 and 16-45, while adding new claims 46-71. Following amendment, there are 33 total claims pending, 4 of which are independent claims. It is noted that following amendment all claims share limitations common to claims 1 and 14, that is, that a memory controller selectively instruct use of a specific preamble prior to outputting data for certain memory commands (i.e., read commands). No new matter has been added.

In the Office Action, the Examiner rejected all previously pending claims under 35 USC §103(a) as allegedly unpatentable over a base rejection of Coteus (USPB 20100220536) in view of Best (USPB 20100091537). This rejection is traversed, because contrary to the Examiner's statements in the Office Action, neither Coteus nor any other cited reference teaches a read command which specifies whether a memory device should output a preamble having a specified timing parameter prior to data. That is, many of the statements of the Office Action regarding what Coteus supposedly teaches are false. As no other cited reference supplies the missing teachings, there exist substantial differences between the claimed invention and the cited art, and reconsideration is therefore respectfully requested.

As the Examiner is aware, the present application specification discloses, among other things, a memory controller that selectively instructs memory to use a specific preamble in the event of a rank switch. The preamble from each memory device is used by the memory controller to receive data from each rank, in a manner that permits adjustment for intra rank skew that may have accumulated since the last time each specific rank was accessed.[1]

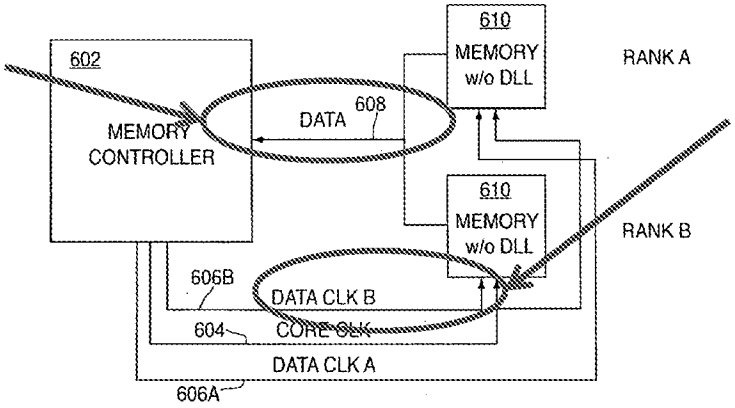
The outstanding rejection is incorrectly premised on the notion that Coteus shows (a) a read command that specifies use of the claimed preamble/timing reference signal, (b) where the memory device outputs the preamble/timing reference signal. Both of these statements are false and represent a misreading of Coteus.

Rather, Coteus provides a different solution to Applicants' claimed invention; as very clearly seen in Coteus' FIG. 5, Coteus teaches that intrarank skew should be addressed by provision by the

[1]As noted in the specification, the invention is not limited to use of multiple ranks, i.e., see the admonition of paragraph [0058] of Applicants' publication.

memory controller to each memory device of a dedicated IO clock. This is to say, Coteus calls for provision of a clock unique to each memory rank (e.g., for commands and write data), coupled with a variable delay circuit for each rank's return path, adjustable by the memory controller, to provide independent control when read data is output by each respective rank relative to its dedicated clock. FIG. 5 of Coteus is reproduced below:

Staggering of read data using variable delay permits control of return path



With Coteus, a dedicated clock travels from the memory controller to each rank...

Applicants have reviewed Coteus and have found no hint, suggestion, or anything else, for a read command that specifies preamble duration for a timing signal output from the memory device.

The Examiner's other references (including to Best) do not supply the missing teachings. It is noted in particular that Best relates to a memory device where the IO and storage functions are separated to multiple dice. Applicants have found no teachings in Best relating to the mitigation of rank switch bubbles.

Because Coteus' fails to support the Examiner's claims and otherwise suggests a solution to rank bubble problems that is inapposite Applicants' solution, the present invention cannot be considered obvious over Coteus (or the other cited art), and there exist substantial differences between the claimed invention and the cited art. The Office Action has therefore clearly not met its burden of demonstrating a *prima facie* case of unpatentability and reconsideration is respectfully urged.

Relative to the new claims set forth above, it is noted that all claims recite a memory controller that issues a read command together with information specifying the *selective* use of a preamble having a specific duration associated with it prior to outputting of read data. The newly added independent claims specify that this memory controller is a DRAM memory controller adapted for use with multiple

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ranks, and further, that the selective use of the specified preamble may be invoked in the event of a rank switch. The cited art does not suggest this solution, and it is respectfully submitted that all pending claims are therefore patentable.

If it would be helpful in the Examination of this case for the Examiner to discuss the cited art or the claims, the Examiner is respectfully requested to contact the undersigned using the contact information set forth below.

Respectfully Submitted,
Attorney for Applicants

/Marc P. Schuyler/
Marc P. Schuyler
Reg. No. 35675
(408) 655-6375

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Electronic Acknowledgement Receipt

EFS ID:	16791068
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	06-SEP-2013
Filing Date:	11-MAY-2011
Time Stamp:	20:19:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	RA764PUS-MPS-OA-Response-09-06-2013-MPS.pdf	138714 f8528b8c4eea15127ee7bb3672e5acfe60ff728a	no	13

Warnings:	
Information:	

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Total Files Size (in bytes):	138714

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/105,798	Filing Date 05/11/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **09/06/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 33	Minus	** 45	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DEBORAH PORTER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

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EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
12/02/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/105,798	Applicant(s) SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/6/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,3-5,11,14,15 and 46-71* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1, 3-5, 11, 14, 15 and 46-71* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 160

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Examiner assumes a typographical error in Claim 14 "which specifies which specifies."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-5, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (US 20100220536, filed Feb. 27, 2009) in view of Best (US 20100091537, published Apr. 15, 2010) and further in view of Schaefer (US 20040022088, published Feb 5, 2004)

Claims 1 and 14, Coteus (20100220536) discloses a method of operation in a memory controller (e.g., memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device, see para 0057), the method comprising:

transmitter circuitry to transmit a read command to a memory device (e.g., Fig. 4 shows three read commands 402, where first read command ("Read A") is directed to a memory device in memory rank A, para 0066)

receiver circuitry to receive the preamble from the memory device (e.g., data receiver 212, para 0064; receiving a clock signal at a receiving device, and data strobe signals in response

to read command, see para 0089, Fig. 22; adjusting data strobe preamble time for adjusting data transfer speed, 0059),

Coteus does not expressly disclose, but Best discloses wherein

to sample the data from the memory device in dependence on the preamble (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus in view of Best does not expressly disclose, but Schaefer discloses

the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data (e.g., preamble can be programmed by controller 202 ... delay element 308 is enabled to delay clock cycle at the beginning and time length of the preamble, para 0037, Fig. 2).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Schaefer, providing the benefit of memories capable of accommodating faster clocking frequencies, where bits are formatted specifically for enabling the data strobe preamble, and adjust data strobe preamble with a time length (see Schaefer, para 0013).

Claims 3 and 15. Coteus does not express disclose, but Best discloses

Controller is to sample data from memory using a sampling clock and sampling data based on both the sampling clock and preamble (e.g., internal clock signal is used to sample and

generate strobe signals output via data path in conjunction with read data, providing a timing reference for establishing a read-data sampling time, para 0038, Fig. 1)

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 4. Coteus discloses after receiving the preamble, receiving EDC signal from memory via common signal line that is used to convey the preamble, wherein a first bit of EDC signal is received after a first bit of the read data; using the EDC signal to update phase of sampling of the data after the receiving the preamble (e.g., permitting error detection information to be transferred in addition to the data, 0059).

Claims 5 and 11. Coteus in view of Best does not expressly disclose, but Schaefer discloses

a read command includes information that specifies length of preamble; wherein the information identifies a length for a predetermined time parameter associated with the parameter (e.g., preamble can be programmed by controller 202 ... delay element 308 is enabled to delay clock cycle at the beginning and time length of the preamble, para 0037, Fig. 2).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Schaefer, providing the benefit of memories capable of accommodating faster clocking frequencies, where bits are formatted specifically for enabling the data strobe preamble, and adjust data strobe preamble with a time length (see Schaefer, para 0013).

5. Claims 46, 47, 53, 54 and 61-71are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Schaefer, and further in view of Koshizuka (US 20100182855, published Jul. 22, 2010) and Jacob (US 20060248261, published Nov. 2 2006)

Claim 46, 53. Coteus discloses wherein the memory controller is operable to control multiple ranks of memory (e.g., Rank A, Rank B, Fig. 1),

Coteus, Best, and Schaefer do not expressly disclose, but Koshizuka discloses

transmitter circuitry is to transmit the information in a manner to specify that memory device is to utilize the duration of the preamble in connection with a rank switch in consecutive memory operations (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Coteus, Best, Schaefer and Koshizuka do not expressly disclose, but Jacob discloses in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch (e.g., rank-to-rank switching time allows spacing of ranks to allow one rank of DRAM devices to release control of data strobe synchronization signals and for a different rank of DRAM devices to gain control of them, para 0025, Fig. 2).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 47, 54. Coteus discloses wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch (e.g., delay time of passively controlled delay line is shorter than that of a conventional delay line, para 0058).

Claim 61 is rejected for reasons similar to Claims 1 and 14 (above) for similar limitations. Further, Coteus, Best, and Schaefer do not expressly disclose, but Koshizuka discloses

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Coteus, Best, Schaefer and Koshizuka do not expressly disclose, but Jacob discloses in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch (e.g., rank-to-rank switching time allows spacing of ranks to allow one rank of DRAM devices to release control of data strobe synchronization signals and for a different rank of DRAM devices to gain control of them, para 0025, Fig. 2).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 62. Coteus discloses wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch (e.g., for a read, preamble time is required prior to completing read transfer to allow data strobe to achieve a stable switching state, 0086, Fig. 19)

Claim 63. Coteus discloses wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank (e.g., controller includes phase lock loop (PLL) 216, 0064, Fig. 2)

Claim 64. Coteus, Best, and Schaefer do not expressly disclose, but Koshizuka discloses, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles (e.g., PLL is disposed for each DIMM between controller 2 and memory device 1 to realize synch of timing with controller for each DIMM, para 0047, Fig. 5).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 65. Coteus, Best, Schaefer and Koshizuka do not expressly disclose, but Jacob discloses, the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 66. Coteus, Best and Schaefer do not expressly disclose, but Koshizuka discloses

wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 67. Coteus discloses wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles (e.g., generates a separate data clock 606 for each rank. controller clocking to monitor drifts on data bus 608, and adjust timing of clocks 606 to each rank, such that data can be captured and contention does not occur on bus 608, para 0068 Fig. 6).

Claim 68. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claim 69 is rejected for reasons similar to Claims 1, 14 and 61 (above) for similar limitations. Further, Coteus, Best and Schaefer do not expressly disclose, but Koshizuka discloses

a digital bit of information which specifies according to its state that an addressed one of the ranks should be outputted of a duration of a preamble prior to outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to

read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8; disclosed flag is interpreted as disclosing claimed digital bit).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 70. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claim 71. Coteus, Best, Schaefer and Koshizuka do not expressly disclose, but Jacob discloses, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

6. Claims 48, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Schaefer, Koshizuka and Jacob, and further in view of Korger (US 6600681, issued Jul 2003)

Claim 48, 55. Coteus, Best, Schaefer, Koshizuka and Jacob do not expressly disclose but Korger discloses memory controller is to sample data output ... duration of preamble (e.g., the middle of the preamble phase is calculated after approximated beginning of the preamble phase, and delay setting is used to produce the sample value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase, col 8, lines 50-67, Fig. 6).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, Koshizuka, and Jacob with Korger, providing the benefit of calibrating a signal used for masking a strobe signal used for masking data strobe signal received from memory device with read data, and sampling using different time delays (col 2, lines 10-17).

7. Claims 49, 51, 56, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Schaefer, and further in view of Koshizuka

Claims 49 and 56. Coetus, Best and Schaefer do not expressly disclose but Koshizuka discloses

toggling pattern as a calibration preamble ....(e.g., read data is outputted with a signal toggle until read data output of a prescribed burst length is complete, 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 58. Coteus, Best, and Shaefer do not expressly disclose, but Koshizuka discloses

Duration represents length of preamble, and transmitter is to transmit information that device should output length preamble prior to data (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claims 51 and 59. Coteus, Best and Schaefer do not expressly disclose, but Koshizuka discloses

Transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

8. Claims 50, 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Schaefer, and further in view of Jacob

Claims 50, 57. Coteus, Best, and Schaefer do not expressly disclose, but Jacob discloses, transmitting the read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer, with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

9. Claims 52, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Schaefer, and further in view of Kim (US 20110055671, published Mar. 3, 2011)

Claim 52 and 60, Coteus, Best, and Schaefer do not expressly disclose, but Kim discloses wherein the receiving the preamble includes receiving the preamble on first resources and sampling data from second resources (e.g., Fig. 13 shows memory device sending data on one line and parity error on a separate line, where parity error includes EDC, 0089).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Schaefer with Kim, providing the benefit of an improved solution to maximize computer performance and density by improving memory device utilization and reduce space and power (see Kim, para 0003).

Response to Arguments

Applicant's arguments with respect to the amended and new claims have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection. See above rejections for details.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GAUTAM SAIN whose telephone number is (571)270-3555. The examiner can normally be reached on Monday - Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GAUTAM SAIN
Examiner
Art Unit 2185

GS

/YAIMA RIGOL/
Primary Examiner, Art Unit 2185

Notice of References Cited	Application/Control No. 13/105,798	Applicant(s)/Patent Under Reexamination SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2011/0055671	03-2011	Kim et al.	714/800
*	B	US-2004/0022088	02-2004	Schaefer, Scott	365/189.07
*	C	US-2006/0248261	11-2006	Jacob et al.	711/001
*	D	US-2010/0182855	07-2010	Koshizuka, Atsuo	365/193
*	E	US-6,600,681	07-2003	Korger et al.	365/193
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
see attached EAST search history	5/31/2013	gs
see attached EAST search history	11/27/2013	gs

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/G.S./ Examiner.Art Unit 2185	

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	-							
	7	✓	-							
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	9	✓	-							
	10	✓	-							
	11	✓	✓							
	12	✓	-							
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	14	✓	✓							
	15	✓	✓							
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	33	✓	-							
	34	✓	-							
	35	✓	-							
	36	✓	-							

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013							
	37	✓	-							
	38	✓	-							
	39	✓	-							
	40	✓	-							
	41	✓	-							
	42	✓	-							
	43	✓	-							
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	70		✓							
	71		✓							

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

APPLICANT AMENDMENT/RESPONSE

Please consider the materials below in response to the Final Office Action mailed December 2, 2013.

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AMENDMENT TO THE CLAIMS

Please amend the claims as set forth below. The listing set forth below replaces all prior listings of claims.

1. (Currently Amended) A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data;

with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;

receiving the preamble; and

sampling the data output from the memory device in dependence on the preamble output from the memory device;

wherein

the memory controller is to control multiple ranks of memory, and

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory device using a sampling clock, and wherein the method further comprises sampling the data based on both the sampling clock and the preamble.

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4. (Previously Presented) The method of claim 3, further comprising:

after receiving the preamble, receiving an error detection and correction (EDC) signal from the memory device via a common signal line that is used to convey the preamble, wherein a first bit of the EDC signal is received after a first bit of the read data; and

using the EDC signal to update phase of sampling of the data after the receiving the preamble.

5. (Previously Presented) The method of claim 1, wherein the read command includes information that specifies a length of the preamble.

6-10. (Canceled)

11. (Previously Presented) The method of claim 1, wherein the information identifies a length for a predetermined time parameter associated with the preamble.

12-13. (Canceled)

14. (Currently Amended) A memory controller, comprising:

transmitter circuitry to transmit a read command to a memory device, the read command being transmitted together with information which specifies ~~which specifies~~ a duration of a preamble that is to be output prior to commencing outputting of the data, wherein the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory device is to

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utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations; and

receiver circuitry to receive the preamble from the memory device and to sample the data from the memory device in dependence on the preamble.

15. (Previously Presented) The memory controller of claim 14, further comprising circuitry to generate a sampling clock, the receiver circuitry operable to sample the data output from the memory device in dependence on the sampling clock and the preamble.

16-46. (Canceled)

47. (Currently Amended) The method of ~~claim 46~~claim 1, wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch.

48. (Currently Amended) The method of ~~claim 46~~claim 1, wherein the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

49. (Previously Presented) The method of claim 1, wherein the preamble comprises a toggling pattern, and wherein the method further comprises using the toggling pattern as a calibration preamble to facilitate sampling of read data from a specific rank.

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50. (Previously Presented) The method of claim 1, wherein transmitting further comprises transmitting the read command to the memory device together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

51. (Previously Presented) The method of claim 1, wherein transmitting the read command with the information further comprises transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of the data.

52. (Previously Presented) The method of claim 1, wherein the receiving the preamble includes receiving the preamble from a first set of signaling resources and wherein sampling the data includes sampling the data output by the memory device from a second set of signaling resources.

53-54. (Canceled)

54. (Currently Amended) The memory controller of ~~claim 53~~claim 14, wherein the memory controller is to cause the transmitter circuitry transmit the information in a manner to cause the memory device to output a longer preamble in connection with the rank switch, relative to no rank switch.

55. (Currently Amended) The memory controller of claim 14~~claim 53~~, wherein the receiver circuitry is to sample the data output from the memory in a manner dependent on rank-specific phase information derived by the memory controller from the preamble.

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56. (Previously Presented) The memory controller of claim 14, wherein the preamble comprises a toggling pattern, and wherein the memory controller is adapted to use the toggling pattern as a calibration sequence to facilitate sampling of read data from a specific rank.

57. (Previously Presented) The memory controller of claim 14, wherein the memory controller is operable to cause the transmitter circuitry to transmit the read command together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

58. (Previously Presented) The memory controller of claim 14, wherein the duration represents a specific length preamble, and wherein the transmitter circuitry is to transmit the information in manner that specifies that the memory device should output the specific length preamble prior to commencing outputting of the data.

59. (Previously Presented) The memory controller of claim 14, wherein the information comprises a digital bit that indicates that the memory device should utilize the duration of the preamble in connection with the outputting of the data.

60. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry comprises circuitry to receive the preamble from a first set of signaling resources, and circuitry to sample the data from a second set of signaling resources.

61. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

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transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch.

62. (Previously Presented) The DRAM memory controller of claim 61, wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch.

63. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank.

64. (Previously Presented) The DRAM memory controller of claim 63, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles.

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65. (Previously Presented) The DRAM memory controller of claim 61, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

66. (Previously Presented) The DRAM memory controller of claim 61, wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data.

67. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles.

68. (Previously Presented) The DRAM memory controller of claim 61, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data.

69. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

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receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command.

70. (Previously Presented) The DRAM memory controller of claim 69, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory.

71. (Previously Presented) The DRAM memory controller of claim 70, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

72. (New) The method of claim 1, further comprising instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

73. (New) The memory controller of claim 14, wherein the memory controller is further to command the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

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REMARKS

In the Final Office Action mailed December 2, 2013, the Examiner rejected all previously pending claims under 35 USC §103(a) as allegedly unpatentable over a base rejection of Coteus (USPB 20100220536) in view of Best (USPB 20100091537) and Shaeffer (US 20040022088). The Examiner stated relative to Applicant's prior remarks that "the remarks have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection;" this is, however, false. That is, Coteus and Best were exactly the references used for the prior rejection, and all of Applicant's prior remarks apply. What the Examiner has done is to add a new reference (Shaeffer) to the prior rejection.

Applicant notes that claims 1 and 14 have been amended to emphasize that preamble duration is specified in connection with a rank switch. Claims 46 and 53-54 have been canceled, and new dependent claims 72 and 73 have been added.

Applicant respectfully requests reconsideration.

The gist of the Examiner's rejection is that according to the Examiner, Coteus shows transmitting a read command that adjusts data strobe preamble, Best discloses that strobe preamble is delayed relative to data, and Shaeffer discloses a programmable preamble. In this regard, several statements made by the Examiner in the Office Action are inaccurate, and the present invention cannot be considered unpatentable over this combination of references.

First, the Examiner has misinterpreted and/or misread Coteus. Contrary to the Examiner's statements, Coteus does not show or suggest adjustment of preamble time "for adjusting data transfer speed." In fact, Coteus does not show or suggest adjustment of any type of preamble or strobe at all insofar as Applicant can find; and paragraph [0059] of Coteus (cited by the Examiner) clearly does not indicate to the contrary. The Examiner is requested to note that Coteus defines his preamble as "the unusable dead time (referred to as the 'preamble' time) increases due to the reduction in data valid time (e.g., data valid 'window')." In other words, this is not a "preamble" as used by Applicant's claims, but rather, merely a statement that says that due to changes in technology development over the ages, as clock oscillation frequencies increase, the dead time needed for calibration increases. What Coteus proposes to address this issue is to transfer data at a slow rate (i.e., such that a stabilized, calibrated

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strobe is not needed to properly sample this data, thereby permitting at least some data to be transferred during the dead time when the strobe from the memory controller cannot be used to sample any data). Paragraph [0089] of Coteus, also referenced by the Examiner, says exactly the same thing. This is not a statement that a preamble duration should be varied in connection with a data read as erroneously asserted by the Examiner, nor anything even conceptually similar.

Coteus does not show or suggest a memory device that alters a strobe signal or preamble (as used in Applicant's claims or specification), nor does it as far as Applicant can find describe a memory device that transmits a strobe signal to a memory controller. That is, what Coteus relates to is providing respective memory with respective data clocks (and/or delays) such that read data from different memory devices can be levelized without requiring a DLL on each memory device. See, e.g., FIG. 6 of Coteus and paragraphs [0068]-[0069]. There is no teaching or suggestion in Coteus that one should selectively use a preamble of specified duration in connection with a rank switch as specified by Applicant's claims.

Best does not supply the teachings missing from Coteus.

As to Shaeffer, the newly-cited reference, this publication relates to a programmable DQS preamble where, by specific advance programming (e.g., using a mode register or data programmed from address or data lines), a memory device can configured at initialization to have a specific duration DQS (strobe) preamble. However, this publication also does not suggest the presently claimed invention; Shaeffer's teaching is that strobe preamble duration should be programmed memory device-by-memory device during an initialization sequence to negate differences in physical distance between sockets and in so doing, levelize read data at a memory controller. See, e.g., Shaeffer, paragraphs [0007], [0062], and [0054]. Shaeffer does not teach that data should be received in connection with a read command to command a memory device to use specific preamble duration in connection with a rank switch (i.e., whether a strobe preamble or any other type of preamble).

It is noted that several of the Examiner's statements regarding Shaeffer are false. For example, the Examiner asserts that "Shaeffer discloses the read command being transmitted together with information which specifies a duration of a preamble...." This is false; Shaeffer is quite clear that his programmable-duration preamble is defined during an initialization mode, i.e., see paragraphs [0054] and [0059] of Shaeffer. Shaeffer sets a preamble time, which is then uniformly used by all ensuing

commands, i.e., Shaeffer does not disclose any ability to select in connection with a command whether a specific preamble duration should be used, or for example, whether a different preamble should be used in the event of a rank switch.

It is noted in connection with the present invention that, because a read command typically specifies an address destination from which data is to be retrieved, it is known a priori whether any given read command in a series of commands represents a rank switch. Thus, in several embodiments of Applicant's invention (and as specified by several of the pending claims), it is the read command itself that specifies according to fields of the read command whether the specific duration preamble is to be used.

Coteus, Best and Shaeffer were used to reject each of the pending independent claims, but as seen above, none of these references show the limitations of the independent claims (or any other claims). These claims all recite limitations relating to the use of specific preamble duration in association with a rank switch. Therefore, there is clearly no *prima facie* case of unpatentability presented by the Office Action, and the outstanding rejection fails to establish a case of unpatentability as to any claim. It is noted that the other cited references, Koshizuka (USPB 20100182855), Jacob (USPB 20060248261), Korger (USPT 6600681) and Kim (USPB 20110055671) fail to show the limitations missing from Coteus/Best/Shaeffer. Therefore no pending claim can be considered unpatentable on the present record and reconsideration is respectfully requested.

Other errata are also noted for the Final Office Action.

1. Koshizuka:

The Examiner asserts on page 5 of the Office Action that Koshizuka discloses transmitter circuitry to transmit information in a manner to specify that the memory device is to use specific preamble duration in connection with a rank switch. This is false. Rather, Koshizuka is cumulative to Shaeffer. That is, Koshizuka proposes use of a programmable duration preamble effectuated by programming memory devices at power up or initialization. Koshizuka, paragraph [0018], referenced by the Examiner, does not support the Examiner's position, but instead simply states that a data strobe is output and accompanying data is output according to the length specified by the register, i.e., a strobe preamble is output, and the ensuing read data is output at a time corresponding to the length of the

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strobe preamble. What Koshizuka does add relative to Shaeffer is a discussion of a multiple rank context, discussed in paragraphs [0048]-[0052] of Koshizuka; here, Koshizuka states that all eight memory devices of each rank are programmed in common to have the same preamble length (paragraph [0048] to shift their relative phase of latching data, i.e., to once again levelize data receipt at the memory controller for differences in distance to each of the ranks) and that this programming is once again effectuated using a mode register (paragraph [0051]) at initialization or power up (paragraph [0052]). This is substantially cumulative to Shaeffer and is performed to levelize read data receipt at a memory controller such that memory does not have to utilize power-hungry DLL circuitry. Despite the Examiner's assertions to the contrary, Koshizuka does not discuss operation dependent on a rank switch.

At page 7 of the Office Action, in connection with discussing Applicant's claim 64, the Examiner states "Koshizuka discloses, wherein the DRAM memory controller is further adapted to store phase specific information to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to store phase information for each rank in dependence on the respective one of the preambles." This is false, or perhaps better stated, is badly garbled. Koshizuka indicates that his memory rank output timing should be "shifted" in phase (using controller-calibrated information) exactly so that the memory controller does not need to store rank-specific phase data for controller-based sampling of data. Perhaps otherwise stated, Koshizuka says that the memory devices should use phase shifts to levelize arrival of read data at the memory controller, but does not suggest that per-rank phase data should be used by the memory controller in the in sampling of read data.[1]

2. Jacob:

The Examiner asserts at page 6 of the Final Office Action that Jacob discloses a memory command transmitted in a manner to specify that an addressed rank is not to output (a specific duration preamble) if there is no rank switch. The Examiner cites paragraph [0025] and FIG. 2 of Jacob as supposedly supporting this assertion. Once again, the Examiner has misread the reference in question, and Jacob clearly does not support the Examiner's position.

[1]Claim 64 relates to certain of Applicant's embodiments where the preamble is sent on a non-timing signal path, e.g., on an error detection information signal line. For example, as represented by Applicant's FIG. 2 (EDC signal 209), phase information can be derived from toggling on this signal and is not directly linked to any timing signal at the memory controller; a memory controller can use rank-specific phase information derived from this EDC connection at certain times to update rank-specific phase used to sample read data.

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Jacob relates to an improved scheduling algorithm for scheduling multiple rank memory transactions. Jacob does not propose at all (insofar as Applicant can find) that memory device manner of operation (or memory device output signals) should be modified or varied dependent on a rank switch; rather, Jacob simply proposes that the output of memory controller commands to those ranks should be planned and interleaved in a manner promoting maximum bandwidth. That is, Jacob simply relates to command scheduling performed solely within the memory controller. There is no disclosure at all that Applicant can find that a specific duration preamble is or is not commanded from the memory device in connection with a rank switch, i.e., Jacob simply treats minimum time constraints as axiomatic and proposes scheduling around those constraints.

3. Korger:

At page 10 of the Final Office Action, the Examiner states that "Korger discloses memory controller is to sample data output ... duration of preamble (e.g., the middle of the preamble phase is calculated after the approximated beginning of the preamble phase, and delay setting is used to produce the same value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase, col. 8, lines 50-67, Fig. 6)." The Examiner asserts this is relevant to claims 48 and 55, which recite that "the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble." The Examiner is wrong.

What Applicant's claims 48 and 55 recite is that data is sampled using phase timing derived from the preamble, and further, that this sampling is rank specific. First, Korger has no disclosure relating to multiple ranks, and clearly discloses that his strobe signal (not any other "phase timing") is used to sample data. That is, what Korger relates to is identification of when data sampling should be enabled relative to a change of a strobe signal away from a high-Z state. Perhaps otherwise stated, Korger generates a mask signal which prevents use of his strobe signal until his strobe signal is determined to clearly change to an active state, where change to the active state is signaled by a strobe preamble. Responsive to a detected change in this state, it is Korger's goal to remove this mask signal (thereby permitting use of the strobe) with the removal of the mask signal timed to occur in the precise middle of a strobe preamble. What Korger proposes is that the strobe preamble should be calibrated, relative to Korger's system clock, so that Korger can perform this enablement at exactly the right time; after

enablement, the native (i.e., unaltered, undelayed), arriving edges of the strobe signal are then directly used for sampling data; this is completely independent of Korger's "phase" and calibration (i.e., which is performed merely to determine when to effectively turn "on" an enable signal). That is, the phase determination of Korger is simply used for the strobe mask signal (i.e., to effective define an enable signal), not in any way to determine timing for the sampling of data, and not in any manner that is rank specific. That is, it is submitted that the Examiner has here also not properly interpreted the reference in question.

Because the cited art does not suggest Applicant's claimed solution, it is respectfully submitted that all pending claims are therefore patentable.

If it would be helpful in the Examination of this case for the Examiner to discuss the cited art or the claims, the Examiner is respectfully requested to contact the undersigned using the contact information set forth below.

Respectfully Submitted,
Attorney for Applicants

/Marc P. Schuyler/
Marc P. Schuyler
Reg. No. 35675
(408) 655-6375

Samsung Electronics Co., Ltd.
Ex. 1050, p. 192

Electronic Acknowledgement Receipt

EFS ID:	17897767
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	13-JAN-2014
Filing Date:	11-MAY-2011
Time Stamp:	16:25:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response After Final Action	RA764PUS-MPS-OA-Response-2014-01-13-MPS.pdf	113961 d4d972c8268dc3e011996868f7bc12e5bdcd3db5	no	15

Warnings:	
Information:	

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Ex. 1050, p. 193

Total Files Size (in bytes):	113961

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/105,798	Filing Date 05/11/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **01/13/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 33	Minus	** 45	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA HARRISON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 02/04/2014

MARC P. SCHUYLER / Rambus
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EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
02/04/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 13/105,798	**Applicant(s)** SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	**Art Unit** 2185	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 January 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: .
    Claim(s) objected to: .
    Claim(s) rejected: .
    Claim(s) withdrawn from consideration: .

/SANJIV SHAH/ Supervisory Patent Examiner, Art Unit 2185	/GAUTAM SAIN/ Examiner, Art Unit 2185

Samsung Electronics Co., Ltd.
Ex. 1050, p. 197

Continuation of 3. NOTE: The amendments to Claims 1 and 14 change the scope of dependent claims 3-5, 11, 15, 47-52 and 54-60 which would require further search and/or consideration for claims 3-5, 11, 15, 47-52 and 54-60 because these claims were not examined with consideration of the proposed amendments to claims 1 and 14 relating to duration of the preamble in connection with rank switch in consecutive memory operations. New Claims 72 and 73 would require new search.

The amendments to Claims 1 and 14 appear to be similar to proposed cancelled claims 46 and 53, addressed below.

Continuation of 11. does NOT place the application in condition for allowance because: Applicant argues that Coteus, Schaeffer and Best do not disclose selective use of a preamble of specified duration in connection with a rank switch (pages 10-12 of Response), and that Koshizuka, Jacob, and Korger fails to make up for the deficiencies of of Coteus, Schaefer and Best (pages 12-15). The Office is not persuasuaded by Applicant's arguments.

For proposed amendments in Claims 1 and 14, Coetus discloses plurality of memory ranks controlled by controller (eg., Rank A, Rank B 104, and controller 102, Fig. 1), and utilizing the duration of the pramble prior to outputting data (eg., preamble time that varies and is required prior to completing read transfer to allow data strobe to achieve stable switching state (0086) .

Additionally, for Claims 1 and 14, Coteus discloses the limitations of in connection with a rank switch consecutive memory operations (eg., preamble time preceding a first burst operation and all information sent to memory device for a second burst operation when the second burst time is not preceded by a preamble time, sinc the strobe is in a stable switching state (0096, end). The Office interprets that the second burst time is consecutive after the first time with no preamble, and is in connection with a rank switch.

Applicant argues on (on page 10) that Coteus does not disclose preamble time. The Office disagrees. According to broadest reasonable interpretation of the claims, claimed preamble is reasonable interpreted as described by Coteus in para 0087, Fig. 20, item 1810 as a time period that varys based on factors such as frequency, loading, etc. The Office disagrees with Applicant's characterization that Coteus' preamble is "dead time." In Coteus, "dead time" is unused preamble time. Fig. 21 shows that in response to read command, that preamble bits are transferrred during preamble time (0088, Fig. 21), in order to reduce read latency (0092). A memory device sends a subset of information dyring preamble time preceding a first burst operation and all information sent to a memory device could be transferred ruding the burst time (0096, middle). Coteus discloses motivation to reduce dead time to transfer data at a slow rate (0059, middle).

Applicant argues (page 11, top), that Coteus does not disclose varying preamble duration. Coteus discloses that preamble time "will vary" based on factors such as switching frequency, etc… (para 0087, Fig. 20).

The Office submits Coteus, Schaeffer and Best are modified by Koshizuk and/or Jacob to disclose these limitations.

For Koshizuka, Applicant's argues that the references do not disclose that operation dependent on rank switch (from formerly cancelled claims 46 and 53), and that Koshizuka does not disclose Claim 64. The Office disagrees. Koshizuka discloses a read preamble that specifies length of the read preamble to be outputed prior to output of read data (0018, 0024), a PLL (or DLL) is disposed for each DIMM between controller and memory devices, 0047-0048, and the phase of an internal clock generated from the system clock is delayed and phase of data strobe signal is generated from the delayed clock, 0035. For the limitations related to rank switch, the Office Action relies on Jacob in combination with Koshizuka. It would have been obvious to one of orndiary skill in the art that the DLL storages phase information, as disclosed by Koshizuka would modify Coteus, Schaeffer and Best.

Applicant argues that Jacob does not disclose that a specific duration preamble is or is not commanded from the memory device in connectdion with a rank switch (page 14 of Response). Coteus discloses this limitations. Coteus discloses a strobe that is already in a stable switching state when data bursts are sent back-to-back and no preamble required (para 0096, end, Fig. 29). For limitations relating to "if there is no rank switch," Applicant's specification describes that no rank switch happens in relation to a write command resulting in an "idle pattern." Similarly, Coteus discloses write to a memory device and minimizing waiting time before writing (0084), and when a write command is received, the data strobe 1808 begins to switch, and after a time period, returns to a stable switch state (0085, middle).

Jacob is also relied upon to dislose the limitations relating to rank switch. Specifically, Jacob discloses consecutive commands to different ranks (para 0023-0024). Jacob discloses a on-rank-at-a-time and a rank-hopping with ideally pipelined DRAM commands. As compared to Applicant's specification that an "idle pattern" is provided during a bubble period between a turnaround of a read and write command (0037). Similarly, Jacob discloses a write-to-read turnaround times for DRAM scheduling, 0006, for example minimum time interval between end of write burst and start of read command, 0019. It would have been obvious that this interval discloses whether duration preamble in connection with rank switch, in combination with Schaefer's disclosure of reducing data strobe preamble for writing data into memory (see Abstract), with the Coteus' disclosure to reduce "dead time" where the strobe signals begin to switch (0059).

Applicant argues that Korger does not disclose Claims 48 and 55. The Office disagrees. Korger discloses to locate a stable beginning of the preamble and avoid uncertain regions, and calculate the middle of the preamble phase after the approximate beginning, and thus the delay setting is used to produce the DQS sample value corresponding to the delay setting for the middle fo the preamble phase (col 8, lines 40-67). The portions relating to rank are disclosed by Jacob. Further, Claims 48 and 55 would require further search and/or consideration since they depend from proposed amended Claims 1 and 14, respectively.

DO NOT ENTER: /GS/ (01/27/2014)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

APPLICANT AMENDMENT/RESPONSE

Please consider the materials below in response to the Final Office Action mailed December 2, 2013.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 199

DO NOT ENTER: /GS/ (01/27/2014)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

APPLICANT AMENDMENT/RESPONSE

Please consider the materials below in response to the Final Office Action mailed December 2, 2013.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 200

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13105798	Filing Date	2011-05-11	Docket Number (if applicable)	2012043 / RA764PUS	Art Unit	2185
First Named Inventor	Ian Shaeffer			Examiner Name	Guatam SAIN		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Applicant Response filed January 13, 2014

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☐ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Marc P. Schuyler/	Date (YYYY-MM-DD)	2014-02-10
Name	Marc P. Schuyler	Registration Number	35675

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13105798
Filing Date:	11-May-2011
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2012043 / RA764.P.US

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	18158894
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	10-FEB-2014
Filing Date:	11-MAY-2011
Time Stamp:	13:34:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1200
RAM confirmation Number	10850
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

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Ex. 1050, p. 206

1	Request for Continued Examination (RCE)	sb0030e_fill-RCE.pdf	697872 60fad9afced9b12ffdf93d6028bcd90f55b4512b	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30336 5934b984e3001222c86f657fcbfaef15620f0edd	no	2
Warnings:					
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			Total Files Size (in bytes):	728208	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/105,798	Filing Date 05/11/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **02/10/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 33	Minus	** 45	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DALE A. HALL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 04/08/2014

MARC P. SCHUYLER / Rambus
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EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
04/08/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/105,798	Applicant(s) SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/10/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,3-5,11,14,15,47,52 and 55-73* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,3-5,11,14,15,47,52 and 55-73* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *5/11/2011* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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Ex. 1050, p. 210

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/10/2014 has been entered.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 304. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-5, 11, 14, 15, 47, 49, 51, 54, 56, 58, 59, 61, 62, 64, 66, 68-70, 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (US 20100220536, filed Feb. 27, 2009) in view of Best (US 20100091537, published Apr. 15, 2010) and further in view of Koshizuka (US 20100182855, published Jul. 22, 2010) and Solomon (US 20060262586, published Nov 2006)

Claims 1 and 14, Coteus (20100220536) discloses a method of operation in a memory controller (e.g., memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device, see para 0057), the method comprising:

transmitter circuitry to transmit a read command to a memory device (e.g., Fig. 4 shows three read commands 402, where first read command ("Read A") is directed to a memory device in memory rank A, para 0066)

receiver circuitry to receive the preamble from the memory device (e.g., data receiver 212, para 0064; receiving a clock signal at a receiving device, and data strobe signals in response to read command, see para 0089, Fig. 22; adjusting data strobe preamble time for adjusting data transfer speed, 0059).

Coteus does not expressly disclose, but Best discloses wherein

to sample the data from the memory device in dependence on the preamble (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus in view of Best does not expressly disclose, but Koshizuka discloses

the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Coteus in view of Best and Koshizuka does not expressly disclose, but Solomon discloses

memory controller is to control multiple ranks (e.g., number of ranks 32, 0052, where memory controller 20 transmits data signals to the ranks 32a and 32b, para 0053);

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations (e.g., read commands accesses data from different memory devices... pre-amble time interval of the second read data burst.. Fig. 6B shows successive read accesses from different memory devices, para 0061).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claims 3 and 15. Coteus does not express disclose, but Best discloses

Controller is to sample data from memory using a sampling clock and sampling data based on both the sampling clock and preamble (e.g., internal clock signal is used to sample and generate strobe signals output via data path in conjunction with read data, providing a timing reference for establishing a read-data sampling time, para 0038, Fig. 1)

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 4. Coteus discloses after receiving the preamble, receiving EDC signal from memory via common signal line that is used to convey the preamble, wherein a first bit of EDC signal is received after a first bit of the read data; using the EDC signal to update phase of sampling of the data after the receiving the preamble (e.g., permitting error detection information to be transferred in addition to the data, 0059).

Claims 5 and 11. Coteus in view of Best does not expressly disclose, but Koshizuka discloses

a read command includes information that specifies length of preamble; wherein the information identifies a length for a predetermined time parameter associated with the parameter (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with

Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Claim 47, 54. Coteus discloses wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch (e.g., delay time of passively controlled delay line is shorter than that of a conventional delay line, para 0058).

Claims 49 and 56. Coetus and Best do not expressly disclose but Koshizuka discloses toggling pattern as a calibration preamble ....(e.g., read data is outputted with a signal toggle until read data output of a prescribed burst length is complete, 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claims 51 and 59. Coteus, and Best do not expressly disclose, but Koshizuka discloses Transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 58. Coteus, and Best do not expressly disclose, but Koshizuka discloses

Duration represents length of preamble, and transmitter is to transmit information that device should output length preamble prior to data (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 61 is rejected for reasons similar to Claims 1 and 14 (above) for similar limitations. Further, Coteus, and Best, do not expressly disclose, but Koshizuka discloses

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command (e.g., the pre-amble time of the second read command is skipped when there is a back-to-back adjacent read as two consecutive bursts of data from the same memory device, para 0060; disclosed burst from same memory device are interpreted as claimed no rank switch).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claim 62. Coteus discloses wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch (e.g., for a read, preamble time is required prior to completing read transfer to allow data strobe to achieve a stable switching state, 0086, Fig. 19)

Claim 63. Coteus discloses wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank (e.g., controller includes phase lock loop (PLL) 216, 0064, Fig. 2)

Claim 64. Coteus, and Best discloses, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank (e.g., sample command signals to generate strobe signals output via data path in conjunction with read data to establish read-data sampling within memory controller… including phase adjustment to enable desired phase offsets between sampling times and transitions in incoming data signals, para 0038).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles (e.g., controller sets preamble length beforehand and then determines time to start detection of clock to start transmission in consideration of phase delay outputted by controlled device, para 0020).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 66. Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 67. Coteus discloses wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles (e.g., generates a separate data clock 606 for each rank. controller clocking to monitor drifts on data bus 608, and adjust timing of clocks 606 to each rank, such that data can be captured and contention does not occur on bus 608, para 0068 Fig. 6).

Claim 68. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claim 69 is rejected for reasons similar to Claims 1, 14 and 61 (above) for similar limitations. Further, Coteus, and Best do not expressly disclose, but Koshizuka discloses

a digital bit of information which specifies according to its state that an addressed one of the ranks should be outputted of a duration of a preamble prior to outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a

prescribed burst length is complete, see para 0059, Fig. 8; disclosed flag is interpreted as disclosing claimed digital bit).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 70. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claims 72 and 73, Coteus in view of Best does not expressly disclose, but Koshizuka discloses

Instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one (e.g., determining a suitable read preamble length considering variation of start timing for data transmission. if length is too long... or if length is unnecessarily long, para 0040, Figs. 6 and 9; setting read preamble length from 1 clock 1 period to 5 periods, para 0060, Fig. 9).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

5. Claims 50, 57, 65, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Jacob (US 20060248261, published Nov. 2 2006)

Claim 65. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 71. Coteus, Best and Koshizuka do not expressly disclose, but Jacob discloses, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claims 50, 57. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, transmitting the read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and

Koshizuka, with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

6. Claims 48, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka, and further in view of Korger (US 6600681, issued Jul 2003)

Claim 48, 55. Coteus, Best, and Koshizuka do not expressly disclose but Korger discloses memory controller is to sample data output ... duration of preamble (e.g., the middle of the preamble phase is calculated after approximated beginning of the preamble phase, and delay setting is used to produce the sample value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase, col 8, lines 50-67, Fig. 6).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka, with Korger, providing the benefit of calibrating a signal used for masking a strobe signal used for masking data strobe signal received from memory device with read data, and sampling using different time delays (col 2, lines 10-17).

9. Claims 52, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best and Koshizuka, and further in view of Kim (US 20110055671, published Mar. 3, 2011)

Claim 52 and 60, Coteus, Best, and Koshizuka do not expressly disclose, but Kim discloses wherein the receiving the preamble includes receiving the preamble on first resources and sampling data from second resources (e.g., Fig. 13 shows memory device sending data on one line and parity error on a separate line, where parity error includes EDC, 0089).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka with Kim, providing the benefit of an improved solution to maximize computer

performance and density by improving memory device utilization and reduce space and power (see Kim, para 0003).

Response to Arguments

Applicant's arguments with respect to the amended and new claims have been considered but the arguments are not persuasive or moot in view of the present rejections including new references. See above rejections for details.

Applicant first argues, on page 10, that Coteus does not disclose adjusting the preamble time for adjusting data transfer speed, and on page 11, varying a preamble duration; however, these limitations are not expressly nor impliedly recited in the claims. Claim 1 recites information which specifies a duration of a preamble, which under broadest reasonably interpretation is interpreted as information regarding specified duration of a preamble. For which, Koshizuka discloses a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018.

Applicant argues that Coteus does not disclose using a preamble of a specified duration in connection with a rank switch. To address these amended limitations, Solomon discloses read commands accesses data from different memory devices... pre-amble time interval of the second read data burst.. Fig. 6B shows successive read accesses from different memory devices, para 0061 (see above rejection for details). Solomon's different memory devices are interpreted as disclosing claimed rank switch because of successive read accesses from different memory devices.

Arguments related to Shaeffer are moot as it is not relied upon in the present rejections.

Applicant argues that Koshizuka does not disclose rank switch. The present Office Action relies on Solomon to disclose the limitations related to rank switch (as stated above).

Applicant argues, for claim 64, that Koshizuka does not disclose that per-rank phase data should be used by memory controller in sampling read data. In the present Office Action, Best in view of Koshizuka (in combination with Coteus) is relied upon for Claim 64. Specifically, Best disclose sample command signals to generate strobe signals output via data path in conjunction with read data to establish read-data sampling within memory controller (para 0038), and Koshizuka discloses controller sets preamble length beforehand and then determines time to start detection of clock to start transmission in consideration of phase delay outputted by controlled device, para 0020.

Applicant argues, regarding Claim 61 that Jacobs does not disclose that memory device manner of operation should be modified or varied dependent on a rank switch. This argument related to Jacob is moot since the present rejection of Claim 61 does not rely on Jacob (see above rejection for details).

Applicant argues, for claims 48 and 55, that Korger does not disclose multiple ranks. These claims now rely on amend on Claims 1 and 14, respectively, where Solomon is relied upon to disclose the amendment related to multiple ranks (see above remarks and rejections).

Conclusion

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to GAUTAM SAIN whose telephone number is (571)270-3555. The examiner can normally be reached on Monday - Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GAUTAM SAIN
Examiner
Art Unit 2185

/GS/

/SANJIV SHAH/

Supervisory Patent Examiner, Art Unit 2185

Notice of References Cited	Application/Control No. 13/105,798	Applicant(s)/Patent Under Reexamination SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2010/0182855	07-2010	Koshizuka, Atsuo	365/193
*	B	US-2006/0262586	11-2006	Solomon et al.	365/063
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
see attached EAST search history	5/31/2013	gs
see attached EAST search history	11/27/2013	gs
see attached EAST search history (including limted CPC search)	3/28/2014	gs

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/G.S./ Examiner.Art Unit 2185	

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6	("20080205187" "20060203548" "20050240838").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 11:51
S2	22	("200400220088" "20040052151" "20060015683" "20060083081" "20070042758" "5566203" "6600681" "6819599" "7606089" "8054928").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 11:53
S3	13	(US-20080205187-$ or US-20060203548-$ or US-20050240838-$ or US-20040052151-$ or US-20060015683-$ or US-20060083081-$ or US-20070042758-$).did. or (US-5566203-$ or US-6600681-$ or US-6819599-$ or US-7606089-$ or US-8054928-$).did. or (US-20040022088-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/05/20 12:11
S4	0	S3 and "timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:11
S5	0	S3 and trs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:11
S6	2633	"timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:12
S7	96	S6 and (read adj command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:12

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S8	84	S7 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:13
S9	31	S8 and (preamble (pre adj amble))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 12:18
S10	1	13/105798.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 14:51
S11	2633	"timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S12	96	S11 and (read adj command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S13	84	S12 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S14	63	S13 and sample	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:10
S15	15	("20050082664" | "20050099834" | "20050139977" | "20050189639" | "20050285174" | "20060233012" | "20070005876" | "20070070669" | "20070158825" | "5838603" | "6236602" | "6469945" | "7579683").PN. OR ("8233303").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/20 15:17
S16	3	S11 and edc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2013/05/20 15:21

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			DERWENT; IBM_TDB			
S17	15	("20050082664" | "20050099834" | "20050139977" | "20050189639" | "20050285174" | "20060233012" | "20070005876" | "20070070669" | "20070158825" | "5838603" | "6236602" | "6469945" | "7579683").PN. OR ("8233303").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/20 15:24
S18	42804	("error detection and correction" edc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S19	32151	("timing reference signal" trs)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S20	137	S18 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S21	64	S20 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:25
S22	16	(US-20080205187-$ or US-20060203548-$ or US-20050240838-$ or US-20040052151-$ or US-20060015683-$ or US-20060083081-$ or US-20070042758-$ or US-20100067314-$ or US-20100091537-$ or US-20120023363-$).did. or (US-5566203-$ or US-6600681-$ or US-6819599-$ or US-7606089-$ or US-8054928-$).did. or (US-20040022088-$).did.	US-PGPUB; USPAT; DERWENT	OR	OFF	2013/05/20 15:56
S23	2	S22 and (sampl$ near2 clock)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/20 15:56
S24	13	("2010/0091537").URPN.	USPAT	OR	OFF	2013/05/20 15:59
S25	79	"l11" and preamble	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2013/05/28 10:25

			EPO; JPO; DERWENT; IBM_TDB			
S26	72	S25 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 10:26
S27	37	("6477110" | "6493285").PN. OR ("6600681").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/28 10:29
S28	2	"20060007760"	US-PGPUB; USPAT; USOCR	OR	OFF	2013/05/28 10:35
S29	7	("2006/0083081").URPN.	USPAT	OR	OFF	2013/05/28 11:38
S30	0	"20100124131".pn.	USPAT	OR	OFF	2013/05/28 12:08
S31	2	"20100124131".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 12:08
S32	4768	dqs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:08
S33	477	S32 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:08
S34	437	S33 and read	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:09
S35	367	S34 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/28 14:09
S36	4772	dqs	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2013/05/31 10:40

			DERWENT; IBM_TDB			
S37	478	S36 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S38	438	S37 and read	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S39	367	S38 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:40
S40	60	S39 and ((burst adj length) same register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/05/31 10:41
S41	2	"20040022088".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 16:14
S42	254	rank near2 switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 20:46
S43	5	S42 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 20:47
S44	186	S42 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 20:54
S45	47	S44 and timing	US-PGPUB; USPAT; USOCR;	OR	OFF	2013/11/26 20:55

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S46	0	("2010/0138598").URPN.	USPAT	OR	OFF	2013/11/26 21:00
S47	12	("2004/0022088").URPN.	USPAT	OR	OFF	2013/11/26 21:16
S48	67	rank adj switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:23
S49	39	S48 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:23
S50	2	"20060248261".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:39
S51	2556	rank and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:47
S52	933	S51 and switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:47
S53	108	S52 and (switch same preamble)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:48
S54	68	S53 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:49
S55	25991	rank and switch	US-PGPUB; USPAT; USOCR;	OR	OFF	2013/11/26 21:58

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S56	34	S55 and (switch and (timing adj reference adj signal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:59
S57	29	S56 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/11/26 21:59
S58	34	("2006/0248261").URPN.	USPAT	OR	OFF	2013/11/26 22:04
S60	1	13/105798.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/27 10:37
S61	0	"365".ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/27 15:08
S62	0	365/320.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/27 15:18
S63	0	365/320.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/27 15:18
S64	1958	365/193.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/27 15:18
S65	8	S64 and turnaround	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2014/01/27 15:18

			IBM_TDB			
S66	38	("2006/0248261").URPN.	USPAT	OR	OFF	2014/01/27 15:23
S67	1	13/105798.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:17
S68	276	rank near2 switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:54
S69	3026	"timing reference signal"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:55
S70	107286	("timing reference signal") (preamble (pre adj amble))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:55
S71	9	S68 and S70	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:55
S72	5	S71 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 14:56
S73	39	("2006/0248261").URPN.	USPAT	OR	OFF	2014/03/27 15:16
S74	0	S73 and flagh	USPAT	OR	OFF	2014/03/27 15:19
S75	0	S73 and flag	USPAT	OR	OFF	2014/03/27 15:19
S76	37934	(preamble (pre adj amble))	USPAT	OR	OFF	2014/03/27 15:20
S77	1	S73 and S76	USPAT	OR	OFF	2014/03/27 15:20
S78	811	("20010000822" | "20010003198" | "20010011322" | "20010019509" | "20010021106" | "20010021137" | "20010046129" | "20010046163" |	US-PGPUB; USPAT; USOCR	OR	OFF	2014/03/27 15:22

"20020002662" | "20020004897" |
"20020015340" | "20020019961" |
"20020034068" | "20020038405" |
"20020041507" | "20020051398" |
"20020060945" | "20020060948" |
"20020064073" | "20020064083" |
"20020089831" | "20020089970" |
"20020094671" | "20020121650" |
"20020121670" | "20020124195" |
"20020129204" | "20020145900" |
"20020165706" | "20020167092" |
"20020172024" | "20020174274" |
"20020184438" | "20030002262" |
"20030011993" | "20030016550" |
"20030021175" | "20030026155" |
"20030026159" | "20030035312" |
"20030039158" | "20030041295" |
"20030061458" | "20030061459" |
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"20030093614" | "20030101392" |
"20030105932" | "20030117875" |
"20030123389" | "20030126338" |
"20030127737" | "20030131160" |
"20030145163" | "20030158995" |
"20030164539" | "20030164543" |
"20030182513" | "20030183934" |
"20030189868" | "20030189870" |
"20030191888" | "20030191915" |
"20030200382" | "20030200474" |
"20030205802" | "20030206476" |
"20030217303" | "20030223290" |
"20030227798" | "20030229821" |
"20030230801" | "20030231540" |
"20030231542" | "20030234664" |
"20040016994" | "20040027902" |
"20040034732" | "20040034755" |
"20040037133" | "20040042503" |
"20040044808" | "20040047228" |
"20040057317" | "20040064647" |
"20040064767" | "20040083324" |
"20040088475" | "20040100837" |
"20040117723" | "20040123173" |
"20040125635").PN. OR ("20040133736"
| "20040139359" | "20040145963" |
"20040151038" | "20040174765" |
"20040177079" | "20040178824" |
"20040184324" | "20040186956" |
"20040188704" | "20040195682" |
"20040196732" | "20040205433" |
"20040208173" | "20040225858" |
"20040228166" | "20040228196" |
"20040228203" | "20040230932" |
"20040236877" | "20040250989" |
"20040256638" | "20040257847" |
"20040260957" | "20040264255" |
"20040268161" | "20050018495" |
"20050021874" | "20050024963" |
"20050027928" | "20050028038" |
"20050034004" | "20050036350" |
"20050041504" | "20050044303" |
"20050044305" | "20050047192" |
"20050071543" | "20050078532" |
"20050081085" | "20050086548" |
"20050099834" | "20050102590" |

"20050105318" | "20050108460" |
"20050127531" | "20050132158" |
"20050135176" | "20050138267" |
"20050138304" | "20050139977" |
"20050141199" | "20050149662" |
"20050152212" | "20050156934" |
"20050166026" | "20050193163" |
"20050193183" | "20050194676" |
"20050194991" | "20050195629" |
"20050201063" | "20050204111" |
"20050207255" | "20050210196" |
"20050223179" | "20050224948" |
"20050232049" | "20050235119" |
"20050235131" | "20050237838" |
"20050243635" | "20050249011" |
"20050259504" | "20050263312" |
"20050265506" | "20050269715" |
"20050278474" | "20050281096" |
"20050281123" | "20050283572" |
"20050285174" | "20050286334" |
"20050289292" | "20050289317" |
"20060002201" | "20060010339" |
"20060026484" | "20060038597" |
"20060039204" | "20060039205" |
"20060041711" | "20060041730").PN.
OR ("20060044909" | "20060044913" |
"20060049502" | "20060050574" |
"20060056244" | "20060062047" |
"20060067141" | "20060085616" |
"20060087900" | "20060090031" |
"20060090054" | "20060106951" |
"20060112214" | "20060112219" |
"20060117152" | "20060117160" |
"20060118933" | "20060120193" |
"20060123265" | "20060126369" |
"20060129712" | "20060129740" |
"20060129755" | "20060133173" |
"20060136791" | "20060149982" |
"20060174082" | "20060176744" |
"20060179262" | "20060179333" |
"20060179334" | "20060180926" |
"20060181953" | "20060195631" |
"20060198178" | "20060203590" |
"20060206738" | "20060233012" |
"20060236165" | "20060236201" |
"20060248261" | "20060248387" |
"20060262586" | "20060294295" |
"20070005998" | "20070050530" |
"20070058471" | "20070070669" |
"20070088995" | "20070091696" |
"20070106860" | "20070136537" |
"20070162700" | "20070188997" |
"20070192563" | "20070195613" |
"20070204075" | "20070216445" |
"20070247194" | "20070279084" |
"20070288683" | "20070288686" |
"20070288687" | "20080002447" |
"20080010435" | "20080025108" |
"20080025122" | "20080025136" |
"20080025137" | "20080027697" |
"20080027702" | "20080027703" |
"20080028135" | "20080028136" |
"20080028137" | "20080031030" |
"20080031072" | "20080037353" |

"20080056014" | "20080062773" |
"20080065820" | "20080082763" |
"20080086588" | "20080089034" |
"20080098277" | "20080103753" |
"20080104314" | "20080109206" |
"20080109595" | "20080109597" |
"20080109598" | "20080115006" |
"20080120443").PN. OR ("20080120458"
| "20080123459" | "20080126624" |
"20080126687" | "20080126688" |
"20080126689" | "20080126690" |
"20080126692" | "20080133825" |
"20080155136" | "20080159027" |
"20080170425" | "20080195894" |
"20080215832" | "20080239857" |
"20080239858" | "20080256282" |
"20090024789" | "20090024790" |
"20090109613" | "20090216939" |
"20090285031" | "20090290442" |
"20100005218" | "20100020585" |
"20100257304" | "20100271888" |
"20100281280" | "3800292" | "4069452"
| "4323965" | "4334307" | "4345319" |
"4392212" | "4525921" | "4566082" |
"4592019" | "4646128" | "4698748" |
"4706166" | "4710903" | "4764846" |
"4780843" | "4794597" | "4796232" |
"4807191" | "4841440" | "4862347" |
"4884237" | "4887240" | "4888687" |
"4899107" | "4912678" | "4922451" |
"4935734" | "4937791" | "4956694" |
"4982265" | "4983533" | "5025364" |
"5072424" | "5083266" | "5104820" |
"5193072" | "5212666" | "5220672" |
"5241266" | "5252807" | "5257233" |
"5278796" | "5282177" | "5332922" |
"5347428" | "5369749" | "5384745" |
"5388265" | "5390334" | "5408190" |
"5432729" | "5448511" | "5453434" |
"5467455" | "5483497" | "5498886" |
"5502333" | "5502667" | "5513135" |
"5513339" | "5519832" | "5526320" |
"5530836" | "5550781" | "5559990" |
"5561622" | "5563086" | "5566344" |
"5581498" | "5581779" | "5590071" |
"5598376" | "5604714" | "5606710" |
"5608262" | "5610864" | "5623686" |
"5627791" | "5640337" | "5640364" |
"5652724" | "5654204" | "5661677" |
"5661695" | "5668773" | "5675549" |
"5680342").PN. OR ("5682354" |
"5692121" | "5692202" | "5696732" |
"5702984" | "5703813" | "5706247" |
"5717654" | "5721859" | "5724288" |
"5729503" | "5729504" | "5742792" |
"5748914" | "5752045" | "5757703" |
"5761703" | "5781766" | "5787457" |
"5798961" | "5802010" | "5802395" |
"5802555" | "5812488" | "5818788" |
"5819065" | "5831833" | "5831931" |
"5831932" | "5834838" | "5835435" |
"5838165" | "5838177" | "5841580" |
"5843799" | "5843807" | "5845108" |
"5850368" | "5859792" | "5860106" |

"5870347" | "5870350" | "5872907" |
"5875142" | "5878279" | "5884088" |
"5901105" | "5903500" | "5905688" |
"5907512" | "5913072" | "5915105" |
"5915167" | "5917758" | "5923611" |
"5924111" | "5926435" | "5929650" |
"5943254" | "5946265" | "5949254" |
"5953215" | "5953263" | "5954804" |
"5956233" | "5963429" | "5963463" |
"5963464" | "5963504" | "5966724" |
"5966727" | "5969996" | "5973392" |
"5995424" | "5995443" | "6001671" |
"6002613" | "6002627" | "6014339" |
"6016282" | "6026050" | "6029250" |
"6032214" | "6032215" | "6034916" |
"6034918" | "6035365" | "6038195" |
"6038673" | "6044032" | "6047073" |
"6047344" | "6053948" | "6058451" |
"6065092" | "6069504" | "6070217" |
"6073223" | "6075730" | "6075744" |
"6078546" | "6079025" | "6084434" |
"6088290" | "6091251" | "6101152" |
"6101564" | "6101612" | "6108795" |
"6111812" | "6125072" | "6134638" |
"6154370" | "6166991" | "6181640" |
"6182184" | "6199151" | "6208168" |
"6216246" | "6222739" | "6226709" |
"6226730" | "6233192" | "6233650" |
"6240048").PN. OR ("6243282" |
"6252807" | "6260097" | "6260154" |
"6262938" | "6266285" | "6266292" |
"6274395" | "6279069" | "6295572" |
"6298426" | "6304511" | "6307769" |
"6314051" | "6317352" | "6317381" |
"6324120" | "6326810" | "6327664" |
"6330683" | "6336174" | "6338108" |
"6338113" | "6341347" | "6343042" |
"6353561" | "6356105" | "6356500" |
"6362656" | "6363031" | "6378020" |
"6381188" | "6381668" | "6389514" |
"6392304" | "6414868" | "6418034" |
"6421754" | "6424532" | "6426916" |
"6429029" | "6430103" | "6437600" |
"6438057" | "6442698" | "6445591" |
"6452826" | "6452863" | "6453400" |
"6453402" | "6453434" | "6455348" |
"6457095" | "6459651" | "6473831" |
"6476476" | "6480929" | "6487102" |
"6489669" | "6490161" | "6492726" |
"6493789" | "6496440" | "6496897" |
"6498766" | "6510097" | "6510503" |
"6512392" | "6521984" | "6526471" |
"6526473" | "6526484" | "6545895" |
"6546446" | "6553450" | "6560158" |
"6563337" | "6563759" | "6564281" |
"6564285" | "6574150" | "6584037" |
"6587912" | "6590822" | "6594770" |
"6597616" | "6597617" | "6614700" |
"6618267" | "6618791" | "6621760" |
"6630729" | "6631086" | "6639820" |
"6646939" | "6650588" | "6650594" |
"6657634" | "6657918" | "6657919" |
"6658016" | "6658530" | "6659512" |
"6664625" | "6665224" | "6665227" |

		"6668242" | "6674154" | "6683372" | "6684292" | "6690191" | "6697295" | "6701446" | "6705877" | "6708144" | "6710430" | "6711043" | "6713856" | "6714891" | "6724684" | "6730540" | "6731009" | "6731527" | "6742098" | "6744687").PN. OR ("6747887" | "6751113" | "6751696" | "6754129" | "6754132" | "6757751" | "6762948" | "6765812" | "6766469" | "6771526" | "6772359" | "6779097" | "6785767" | "6791877" | "6795899" | "6799241" | "6801989" | "6807598" | "6807655" | "6816991" | "6819602" | "6819617" | "6820163" | "6820169" | "6826104" | "6839290" | "6845027" | "6845055" | "6847582" | "6850449" | "6862202" | "6862249" | "6862653" | "6873534" | "6878570" | "6894933" | "6898683" | "6908314" | "6912778" | "6914786" | "6917219" | "6922371" | "6930900" | "6930903" | "6938119" | "6943450" | "6944748" | "6947341" | "6951982" | "6952794" | "6961281" | "6968416" | "6968419" | "6970968" | "6980021" | "6986118" | "6992501" | "6992950" | "7000062" | "7003618" | "7003639" | "7007095" | "7007175" | "7010642" | "7010736" | "7024518" | "7026708" | "7028215" | "7028234" | "7033861" | "7035150" | "7043599" | "7043611" | "7045396" | "7045901" | "7046538" | "7053470" | "7053478" | "7058776" | "7058863" | "7061784" | "7061823" | "7066741" | "7075175" | "7079396" | "7079441" | "7079446" | "7085152" | "7085941" | "7089438" | "7093101" | "7103730" | "7110322" | "7119428" | "7120727" | "7126399" | "7127567" | "7133960" | "7136978" | "7138823" | "7149145" | "7149824" | "7173863" | "7200021" | "7205789" | "7210059" | "7215561" | "7218566" | "7224595" | "7228264" | "7231562" | "7233541" | "7234081" | "7243185" | "7245541" | "7254036" | "7266639" | "7269042" | "7269708" | "7274583" | "7277333" | "7286436" | "7289386" | "7296754" | "7299330").PN. OR ("7302598" | "7307863" | "7317250" | "7337293" | "7363422" | "7366947" | "7379316" | "7386656" | "7392338" | "7408393" | "7409492" | "7414917" | "7428644" | "7437579" | "7441064" | "7457122" | "7464225" | "7472220" | "7474576" | "7480147" | "7480774" | "7496777" | "7515453" | "7532537" | "7539800" | "7573136" | "7580312" | "7581121" | "7581127" | "7590796" | "7599205" | "7606245" | "7609567" | "7613880" | "7619912" | "7724589" | "7730338" | "7761724" | "7934070" | "7990797" | "RE35733" | "RE36839").PN. OR ("8335894").URPN.				

S79	15	S78 and S70	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 15:23
S80	15	S79 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/27 15:23
S81	12257	(g06F12/00 g11c8/00 g06f13/28 g11c8/00).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/28 12:04
S82	67	S81 and preamble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/28 12:04
S83	41	S82 and @ad<"20100722"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/28 12:04
S84	69	S81 and (preamble (pre adj amble))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/03/28 12:05

4/4/2014 12:23:46 AM
C:\Users\gsain\Documents\EAST\Workspaces\13105798.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014						
	1	✓	✓	✓						
	2	✓	-	-						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	-	-						
	7	✓	-	-						
	8	✓	-	-						
	9	✓	-	-						
	10	✓	-	-						
	11	✓	✓	✓						
	12	✓	-	-						
	13	✓	-	-						
	14	✓	✓	✓						
	15	✓	✓	✓						
	16	✓	-	-						
	17	✓	-	-						
	18	✓	-	-						
	19	✓	-	-						
	20	✓	-	-						
	21	✓	-	-						
	22	✓	-	-						
	23	✓	-	-						
	24	✓	-	-						
	25	✓	-	-						
	26	✓	-	-						
	27	✓	-	-						
	28	✓	-	-						
	29	✓	-	-						
	30	✓	-	-						
	31	✓	-	-						
	32	✓	-	-						
	33	✓	-	-						
	34	✓	-	-						
	35	✓	-	-						
	36	✓	-	-						

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014						
	37	✓	-	-						
	38	✓	-	-						
	39	✓	-	-						
	40	✓	-	-						
	41	✓	-	-						
	42	✓	-	-						
	43	✓	-	-						
	44	✓	-	-						
	45	✓	-	-						
	46		✓	-						
	47		✓	✓						
	48		✓	✓						
	49		✓	✓						
	50		✓	✓						
	51		✓	✓						
	52		✓	✓						
	53		✓	-						
	54		✓	-						
	55		✓	✓						
	56		✓	✓						
	57		✓	✓						
	58		✓	✓						
	59		✓	✓						
	60		✓	✓						
	61		✓	✓						
	62		✓	✓						
	63		✓	✓						
	64		✓	✓						
	65		✓	✓						
	66		✓	✓						
	67		✓	✓						
	68		✓	✓						
	69		✓	✓						
	70		✓	✓						
	71		✓	✓						
	72			✓						

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014						
	73			✓						

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 04/10/2014

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EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
04/10/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/105,798	SHAEFFER ET AL.	
	Examiner	Art Unit	
	GAUTAM SAIN	2185	

All participants (applicant, applicant's representative, PTO personnel):

(1) *GAUTAM SAIN*. (3)_____.

(2) *Marc P. Schuyler, Rep. for Applicant*. (4)_____.

Date of Interview: *02 April 2014*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Coteus*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant briefly expalained the invention and claim limitations including transmitting a duration of a preamble with the read command, utilizing the duration of the preamble prior to commencing outputting the read data in connection with a rank switch.

Applicant argued that Coteus does not disclose the amended limitations related to adjustement of preamble time for adjusting data transfer speed, and does not disclose adjusting the duration of the preamble. Applicant argued that Coteus discloses providing respective memory with data clocks from different memory devices without requiring a DLL on each memory device (see Applicant's arguments in the filed resposne, page 11).

No agreement was reached regarding allowability .

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GAUTAM SAIN/ Examiner, Art Unit 2185	/SANJIV SHAH/ Supervisory Patent Examiner, Art Unit 2185

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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

APPLICANT AMENDMENT/RESPONSE

Please consider the materials below in response to the Non-Final Office Action mailed April 8, 2014.

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AMENDMENTS TO THE SPECIFICATION

Please amend the specification by replacing paragraph [0030] with the paragraph set forth below. Changes are shown in revision text as required by the rules.

"**[0030]** After the controller issues read command RD[A1], a rank switch occurs from rank 0 to idle rank 1. More specifically, immediately after issuing a precharge command PRE to close off the access to rank 0, two consecutive read commands RD[A2] and RD[A3] are issued to rank 1, wherein RD[A2] is the first memory access request on rank 1 after the idle period on rank 1. In response, rank 1 prepends a calibration preamble 304 to read data Q[A2]."

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AMENDMENT TO THE CLAIMS

There are no amendments to the claims, which are presented below solely for the Examiner's convenience.

1. (Previously Presented) A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data;

with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;

receiving the preamble; and

sampling the data output from the memory device in dependence on the preamble output from the memory device;

wherein

the memory controller is to control multiple ranks of memory, and

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory device using a sampling clock, and wherein the method further comprises sampling the data based on both the sampling clock and the preamble.

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4. (Previously Presented) The method of claim 3, further comprising:

after receiving the preamble, receiving an error detection and correction (EDC) signal from the memory device via a common signal line that is used to convey the preamble, wherein a first bit of the EDC signal is received after a first bit of the read data; and

using the EDC signal to update phase of sampling of the data after the receiving the preamble.

5. (Previously Presented) The method of claim 1, wherein the read command includes information that specifies a length of the preamble.

6-10. (Canceled)

11. (Previously Presented) The method of claim 1, wherein the information identifies a length for a predetermined time parameter associated with the preamble.

12-13. (Canceled)

14. (Previously Presented) A memory controller, comprising:

transmitter circuitry to transmit a read command to a memory device, the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data, wherein the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory device is to utilize the

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duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations; and

receiver circuitry to receive the preamble from the memory device and to sample the data from the memory device in dependence on the preamble.

15. (Previously Presented) The memory controller of claim 14, further comprising circuitry to generate a sampling clock, the receiver circuitry operable to sample the data output from the memory device in dependence on the sampling clock and the preamble.

16-46. (Canceled)

47. (Previously Presented) The method of claim 1, wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch.

48. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

49. (Previously Presented) The method of claim 1, wherein the preamble comprises a toggling pattern, and wherein the method further comprises using the toggling pattern as a calibration preamble to facilitate sampling of read data from a specific rank.

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50. (Previously Presented) The method of claim 1, wherein transmitting further comprises transmitting the read command to the memory device together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

51. (Previously Presented) The method of claim 1, wherein transmitting the read command with the information further comprises transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of the data.

52. (Previously Presented) The method of claim 1, wherein the receiving the preamble includes receiving the preamble from a first set of signaling resources and wherein sampling the data includes sampling the data output by the memory device from a second set of signaling resources.

53-54. (Canceled)

54. (Previously Presented) The memory controller of claim 14, wherein the memory controller is to cause the transmitter circuitry transmit the information in a manner to cause the memory device to output a longer preamble in connection with the rank switch, relative to no rank switch.

55. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry is to sample the data output from the memory in a manner dependent on rank-specific phase information derived by the memory controller from the preamble.

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56. (Previously Presented) The memory controller of claim 14, wherein the preamble comprises a toggling pattern, and wherein the memory controller is adapted to use the toggling pattern as a calibration sequence to facilitate sampling of read data from a specific rank.

57. (Previously Presented) The memory controller of claim 14, wherein the memory controller is operable to cause the transmitter circuitry to transmit the read command together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

58. (Previously Presented) The memory controller of claim 14, wherein the duration represents a specific length preamble, and wherein the transmitter circuitry is to transmit the information in manner that specifies that the memory device should output the specific length preamble prior to commencing outputting of the data.

59. (Previously Presented) The memory controller of claim 14, wherein the information comprises a digital bit that indicates that the memory device should utilize the duration of the preamble in connection with the outputting of the data.

60. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry comprises circuitry to receive the preamble from a first set of signaling resources, and circuitry to sample the data from a second set of signaling resources.

61. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

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transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch.

62. (Previously Presented) The DRAM memory controller of claim 61, wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch.

63. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank.

64. (Previously Presented) The DRAM memory controller of claim 63, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles.

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65. (Previously Presented) The DRAM memory controller of claim 61, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

66. (Previously Presented) The DRAM memory controller of claim 61, wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data.

67. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles.

68. (Previously Presented) The DRAM memory controller of claim 61, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data.

69. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

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receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command.

70. (Previously Presented) The DRAM memory controller of claim 69, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory.

71. (Previously Presented) The DRAM memory controller of claim 70, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

72. (Previously Presented) The method of claim 1, further comprising instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

73. (Previously Presented) The memory controller of claim 14, wherein the memory controller is further to command the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

REMARKS

In the Non-Final Office Action mailed April 8, 2013, the Examiner (1) objected to the drawings, for failure of the specification to refer to numeral 304 depicted in the drawings, and (2) rejected all pending claims under 35 USC §103(a) as allegedly unpatentable over a base rejection of Coteus (USPB 20100220536), Best (USPB 20100091537), Koshizuka (USPB 20100182855) and Solomon (USPB 200600262586).

As to the objection to the drawings, Applicant notes that paragraph [0030] of the Specification has been amended to refer to reference numeral 304. As a result, this objection is improper and should now be withdrawn.

As to the rejection over art, Applicant submits that this is in error and respectfully requests reconsideration. None of the Examiner's four primary references can be fairly read as suggesting anything akin to Applicant's invention. The art as a whole relied upon by the Examiner fails to show at least those limitations underlined below.

"1. A method of operation in a memory controller, the method comprising:
transmitting a read command which specifies that a memory device output data;
with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;
receiving the preamble; and
sampling the data output from the memory device in dependence on the preamble output from the memory device;
wherein
the memory controller is to control multiple ranks of memory, and
the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations."

The invention represented by claim 1 recites a memory controller method where the memory controller transmits, with a read command and in the event of a rank switch, information that specifies a duration of a preamble to be used by a memory device before outputting data. No reference fairly read show or suggests this solution or even addresses the same problem as Applicant.

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First, contrary to the Examiner's statements in the Office Action, Coteus as *nothing to do* with specifying a preamble duration and Coteus does not "adjust" a strobe preamble time. Rather, what Coteus refers to "the unusable dead time (referred to as the 'preamble' time)" of a data bus, which is a period during which valid data conventionally cannot be transmitted because timing is not yet stable. What Coteus says (see, e.g., paragraphs 59 and 89 of Coteus) is that during this time, data (i.e., parity bits) can be transmitted at half-rate and thus still received, because such data can be sampled without high accuracy provided by a valid strobe signal. Coteus specifically says as follows: "Exemplary embodiments utilize the dead time on the data bus, while the data strobe is stabilizing, to transfer data at a slow rate (e.g. a rate that permits data to be captured without the need of a data strobe or with the use of the strobe during a period in which the strobe has reduced timing accuracy." In other words, Coteus simply says that the *down time of the data bus* can be shortened by transmitting data at half-speed during the dead period (i.e., during a time interval conventionally thought unusable); Coteus as far as Applicant can tell does not specify a strobe preamble duration during this period, or anything analogous and does not specify a preamble duration in connection with a rank switch. There is for example no teaching or suggestion in Coteus that a memory controller should transmit, with a read command, information that causes a memory device to utilize a preamble of specified duration in connection with a rank switch, as specified by Applicant's claims.

Best does not supply the teachings missing from Coteus, and as far as Applicant can tell, is cited simply to show that a strobe is used to sample data bits at a destination.

Koshizuka proposes use of a programmable duration preamble effectuated by programming memory devices at power up or initialization. Koshizuka addresses a specific problem where, for some architectures, the system clock may be slow enough relative to timing delays of a memory device that a DQS preamble cannot be detected.[1] Koshizuka proposes a relatively straightforward solution, where a read preamble register is programmed in dependence on system clock frequency and internal delay time of the memory device.[2] Koshizuka further states at paragraphs [0048]-[0052] that all eight memory devices of each rank are programmed in common to have the same preamble length (paragraph [0048]

[1]See paragraphs 14-17of Koshizuka.

[2]See Koshizuka's abstract, i.e., "[a] memory controller gives consideration to system clock frequency and internal delay time of the semiconductor memory device, and by optimally setting the read preamble length, can perform data transmission at high speed and without missing head data even if read data output start timing of the semiconductor memory device varies." See also paragraph 41 of Koshizuka.

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to shift their relative phase of latching data, i.e., to levelize data receipt at the memory controller for differences in distance) and that this programming is once again effectuated using a mode register (paragraph [0051]) at initialization or power up (paragraph [0052]). Koshizuka does not discuss operation dependent on a rank switch and there is no teaching that would lead one skilled in the art toward a solution where a memory controller transmits, with a read command, information that specifies or causes a preamble duration in the event of a rank switch.

At page 4 (and elsewhere) in of the Office Action, the Examiner asserts for example that "Coteus in view of Best does not expressly disclose, but Koshizuka discloses the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing output of data." This is incorrect. What Koshizuka says is that there is a register that specifies a preamble duration, and that a preamble duration determination u calibrates the duration "at system start-up time or for each fixed time interval." See paragraph 53 of Koshizuka. Thus, Koshizuka does not teach that a preamble duration should be specified with a read command in any manner, much less in the event of a rank switch.

The new reference Solomon also does not provide the teachings missing from the other references. That is, Solomon for example at paragraph [0056] (cited by the Examiner) indicates that memory modules that uses multiple ranks of memory can electrically isolate respective ranks to decrease the electrical load on Solomon's server, and thereby permit that server to run faster with better signal integrity. As with the other references, Solomon is devoid of any teaching that a preamble duration should be specified in association with a rank switch.

The Examiner's obviousness position is that claims 1, 3-5, 11, 14-15, 47, 49, 51, 54, 56, 58, 59, 61-62, 64, 66, 68-70 and 72-73 would have been obvious in view of Coteus, Best, Koshizuka and Solomon. This position is clearly erroneous, i.e.,

- even considered together, all seven of the Examiner's cited reference FAIL to show the limitations underlined in claim 1, above; none of these references address the same problem as Applicant;

- there is no teaching anywhere in the cited art that a preamble should be varied, changed, specified, or anything else in connection with a rank switch;

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- Koshizuka expressly teaches that a read preamble should be set during startup (or regular intervals) and be made dependent on memory device delay times and system clock frequency. Koshizuka has very specific guidance on how a read preamble duration should be established, none of which suggests Applicant's solution of specifying duration with a read command and in the event of a rank switch.

- There is no teaching or suggestion in the art that would lead one to the present invention. It is noted that the Examiner at page 5 attempts to justify his combination with a statement that the motivation would have been "providing the benefit of improving performance and capacity of memory modules." This generalized statement falls well short of the requirement that a specific teaching or motivation to combine be demonstrated in the references in order to obtain the Applicant's invention. As stated by the Federal Circuit in *In Re Dembiczak*, Opinion 98-1498 (CAFC 1999), a teaching or motivation to combine references can come from the references themselves or from the art, but that showing must be clear and particular, and broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence of such a teaching. "In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed" (In Re Rouffet, 149 F.3d 1350, 47 U.S.P.Q.2d 1453, CAFC 1998). Such a showing has not been made here. For example, the Examiner's purported justification for combination that motivation would be to provide "the benefit of improving performance and capacity of memory modules" appears to be a hindsight attempt to justify rejection of Applicant's claims by any means possible, i.e., the point is that there is no reason in the references (or anywhere else) why one would look to the very references selected by the Examiner with an expectation that they would lead to Applicant's invention.

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All claims at issue depend on claims 1, 14, 61 or 69 which contain the referenced limitations or their equivalent. It should therefore be clear that no claim of record is unpatentable over Coteus/Best/Koshizuba/Solomon.

It is noted that the Examiner further introduces the additional references of Jacob (20060248261), Korger (USPT 6600681)and Kim (USPB 20110055671), in addition to the base references discussed above, in rejecting claims 48, 50, 52, 55, 57, 60 65 and 71. However, none of these references are cited as supplying the teachings missing from the base references.

Because the cited art does not suggest Applicant's claimed solution, it is respectfully submitted that all pending claims are therefore patentable. Reconsideration is therefore respectfully requested.

If it would be helpful in the Examination of this case for the Examiner to discuss the cited art or the claims, the Examiner is respectfully requested to contact the undersigned using the contact information set forth below.

Respectfully Submitted,
Attorney for Applicants

/Marc P. Schuyler/
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Electronic Acknowledgement Receipt

EFS ID:	19399006
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	24-JUN-2014
Filing Date:	11-MAY-2011
Time Stamp:	17:27:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	RA764PUS-MPS-OA-Response-2014-06-23.pdf	111169 8a180fb630272804c4c327b39f7ab8656d56094f	no	15

Warnings:	
Information:	

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Total Files Size (in bytes):	111169

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/105,798	Filing Date 05/11/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **06/24/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 33	Minus	** 45	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA MURPHY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

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EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
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10/01/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/105,798	Applicant(s) SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2185	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/24/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1,3-5,11,14,15,47,52 and 55-73* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,3-5,11,14,15,47,52 and 55-73* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *5/11/2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Samsung Electronics Co., Ltd.
Ex. 1050, p. 266

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. The objections to the drawings are withdrawn in view of the amendment to the specification.

Response to Arguments

3. Applicant's arguments filed 6/24/2014 have been fully considered but they are not persuasive.

Regarding Claim 1, Applicant argues that the cited references do not disclose a preamble duration in connection with a rank switch. The Office disagrees.

Koshizuka discloses detecting a read preamble with suitable timing to receive read data (0013). A read preamble register that specifies length of the read preamble outputted prior to output of read data (0018, Fig. 9), compared to claimed limitation of information which specifies a duration of a preamble that is output prior to commencing outputting data, according to the broadest reasonable interpretation. Fig. 9 disclose setting of read preamble length register where preamble length is selected (0060). The length of the read preamble signal is lengthened (0064). Lenghtening a premable is equivalent to varying the preamble.

Solomon disclose selectively switching between two ranks of memory devices 30 (0055). Data bursts with pre-amble time interval, and two consecutive read bursts from different memory devices than the first read command (interpreted as equivalent to claimed rank switch)(0061). Memory boundaries between ranks of memory module prior to issue read commands where a wait time is inserted to avoid collisions between back-to-back adjacent read commands which

cross memory device boundaries (0062). Solomon's different memory devices are interpreted as disclosing claimed rank switch because of successive read accesses from different memory devices.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a preamble duration in connection with a rank switch, based at least on the disclosure of Koshizuka and Solomon. One of ordinary skill in the art would have been motivated to modify Koshizuka's disclosure of lengthening read preamble length, with Solomon's disclosure of selectively switching between two ranks of memory devices with pre-amble time intervals in between ranks switching, thus avoiding collisions between two consecutive read bursts between different memory devices.

Next, Applicant argues that the cited references do not disclose that a preamble should be varied. However, varying the preamble is not in the claims. But in any case, this argument is addressed above.

Applicant's arguments for Claims 3-5, 11, 14-15, 47, 49, 51, 54, 56, 58, 59, 61-62, 64, 66, 68-70 and 72-73 are based on same rational as for Claim 1, thus are addressed accordingly herein (see above).

Applicant's arguments for Claims 47, 50, 52, 57, 60, 65, and 71 are based on same rational as for Claim 1, thus are addressed accordingly herein (see above).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-5, 11, 14, 15, 47, 49, 51, 54, 56, 58, 59, 61, 62, 64, 66, 68-70, 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (US 20100220536, filed Feb. 27, 2009) in view of Best (US 20100091537, published Apr. 15, 2010) and further in view of Koshizuka (US 20100182855, published Jul. 22, 2010) and Solomon (US 20060262586, published Nov 2006)

Claims 1 and 14, Coteus (20100220536) discloses a method of operation in a memory controller (e.g., memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device, see para 0057), the method comprising:

transmitter circuitry to transmit a read command to a memory device (e.g., Fig. 4 shows three read commands 402, where first read command ("Read A") is directed to a memory device in memory rank A, para 0066)

receiver circuitry to receive the preamble from the memory device (e.g., data receiver 212, para 0064; receiving a clock signal at a receiving device, and data strobe signals in response to read command, see para 0089, Fig. 22; adjusting data strobe preamble time for adjusting data transfer speed, 0059).

Coteus does not expressly disclose, but Best discloses wherein

to sample the data from the memory device in dependence on the preamble (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus in view of Best does not expressly disclose, but Koshizuka discloses

the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018; detecting a read preamble with suitable timing to receive read data (0013). A read preamble register that specifies length of the read preamble outputted prior to output of read data (0018, Fig. 9), compared to claimed limitation of information which specifies a duration of a preamble that is output prior to commencing outputting data, according to the broadest reasonable interpretation. Fig. 9 disclose setting of read preamble length register where preamble length is selected (0060). The length of the read preamble signal is lengthened (0064)).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Coteus in view of Best and Koshizuka does not expressly disclose, but Solomon discloses

memory controller is to control multiple ranks (e.g., number of ranks 32, 0052, where memory controller 20 transmits data signals to the ranks 32a and 32b, para 0053);

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations (e.g., read commands accesses data from different memory devices... pre-amble time interval of the second read data burst.. Fig. 6B shows successive read accesses from different memory devices, para 0061; selectively switching between two ranks of memory devices 30 (0055). Data bursts with pre-amble time interval, and two consecutive read bursts from different memory devices than the first read command (interpreted as equivalent to claimed rank switch)(0061). Memory boundaries between ranks of memory module prior to issue read commands where a wait time is inserted to avoid collisions between back-to-back adjacent read commands which cross memory device boundaries (0062).).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claims 3 and 15. Coteus does not express disclose, but Best discloses

Controller is to sample data from memory using a sampling clock and sampling data based on both the sampling clock and preamble (e.g., internal clock signal is used to sample and generate strobe signals output via data path in conjunction with read data, providing a timing reference for establishing a read-data sampling time, para 0038, Fig. 1)

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 4. Coteus discloses after receiving the preamble, receiving EDC signal from memory via common signal line that is used to convey the preamble, wherein a first bit of EDC signal is received after a first bit of the read data; using the EDC signal to update phase of

sampling of the data after the receiving the preamble (e.g., permitting error detection information to be transferred in addition to the data, 0059).

Claims 5 and 11. Coteus in view of Best does not expressly disclose, but Koshizuka discloses

a read command includes information that specifies length of preamble; wherein the information identifies a length for a predetermined time parameter associated with the parameter (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Claim 47, 54. Coteus discloses wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch (e.g., delay time of passively controlled delay line is shorter than that of a conventional delay line, para 0058).

Claims 49 and 56. Coetus and Best do not expressly disclose but Koshizuka discloses

toggling pattern as a calibration preamble ....(e.g., read data is outputted with a signal toggle until read data output of a prescribed burst length is complete, 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claims 51 and 59. Coteus, and Best do not expressly disclose, but Koshizuka discloses

Transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 58. Coteus, and Best do not expressly disclose, but Koshizuka discloses

Duration represents length of preamble, and transmitter is to transmit information that device should output length preamble prior to data (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 61 is rejected for reasons similar to Claims 1 and 14 (above) for similar limitations. Further, Coteus, and Best, do not expressly disclose, but Koshizuka discloses

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command (e.g., the pre-amble time of the second read command is skipped when there

is a back-to-back adjacent read as two consecutive bursts of data from the same memory device, para 0060; disclosed burst from same memory device are interpreted as claimed no rank switch).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claim 62. Coteus discloses wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch (e.g., for a read, preamble time is required prior to completing read transfer to allow data strobe to achieve a stable switching state, 0086, Fig. 19)

Claim 63. Coteus discloses wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank (e.g., controller includes phase lock loop (PLL) 216, 0064, Fig. 2)

Claim 64. Coteus, and Best discloses, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank (e.g., sample command signals to generate strobe signals output via data path in conjunction with read data to establish read-data sampling within memory controller… including phase adjustment to enable desired phase offsets between sampling times and transitions in incoming data signals, para 0038).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles (e.g., controller sets preamble length beforehand and then determines time to start detection of clock to start transmission in consideration of phase delay outputted by controlled device, para 0020).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 66. Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 67. Coteus discloses wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles (e.g., generates a separate data clock 606 for each rank. controller clocking to monitor drifts on data bus 608, and adjust timing of clocks 606 to each rank, such that data can be captured and contention does not occur on bus 608, para 0068 Fig. 6).

Claim 68. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less

than a data rate used for transmission of data memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claim 69 is rejected for reasons similar to Claims 1, 14 and 61 (above) for similar limitations. Further, Coteus, and Best do not expressly disclose, but Koshizuka discloses

a digital bit of information which specifies according to its state that an addressed one of the ranks should be outputted of a duration of a preamble prior to outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8; disclosed flag is interpreted as disclosing claimed digital bit).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 70. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claims 72 and 73, Coteus in view of Best does not expressly disclose, but Koshizuka discloses

Instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble wherein the preamble to be output beginning

at a predetermined time prior to commencing the outputting of the data is the selective one (e.g., determining a suitable read preamble length considering variation of start timing for data transmission. if length is too long... or if length is unnecessarily long, para 0040, Figs. 6 and 9; setting read preamble length from 1 clock 1 period to 5 periods, para 0060, Fig. 9).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

6. Claims 50, 57, 65, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Jacob (US 20060248261, published Nov. 2 2006)

Claim 65. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 71. Coteus, Best and Koshizuka do not expressly disclose, but Jacob discloses, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claims 50, 57. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, transmitting the read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka, with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

7. Claims 48, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Korger (US 6600681, issued Jul 2003)

Claim 48, 55. Coteus, Best, Koshizuka and Solomon do not expressly disclose but Korger discloses memory controller is to sample data output ... duration of preamble (e.g., the middle of the preamble phase is calculated after approximated beginning of the preamble phase, and delay setting is used to produce the sample value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase, col 8, lines 50-67, Fig. 6).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Koshizuka, and Solomon with Korger, providing the benefit of calibrating a signal used for masking a strobe signal used for masking data strobe signal received from memory device with read data, and sampling using different time delays (col 2, lines 10-17).

8. Claims 52, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Kim (US 20110055671, published Mar. 3, 2011)

Claim 52 and 60, Coteus, Best, Koshizuka and Solomon do not expressly disclose, but Kim discloses wherein the receiving the preamble includes receiving the preamble on first resources and sampling data from second resources (e.g., Fig. 13 shows memory device sending data on one line and parity error on a separate line, where parity error includes EDC, 0089).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Koshizuka and Solomon with Kim, providing the benefit of an improved solution to maximize computer performance and density by improving memory device utilization and reduce space and power (see Kim, para 0003).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GAUTAM SAIN whose telephone number is (571)270-3555. The examiner can normally be reached on Monday - Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GAUTAM SAIN
Examiner
Art Unit 2185

/GS/

/SANJIV SHAH/
Supervisory Patent Examiner, Art Unit 2185

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
see attached EAST search history	5/31/2013	gs
see attached EAST search history	11/27/2013	gs
see attached EAST search history (including limted CPC search)	3/28/2014	gs
see search EAST history from 3/28/2014	9/29/2014	gs

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/G.S./ Examiner.Art Unit 2185	

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014					
	1	✓	✓	✓	✓					
	2	✓	-	-	-					
	3	✓	✓	✓	✓					
	4	✓	✓	✓	✓					
	5	✓	✓	✓	✓					
	6	✓	-	-	-					
	7	✓	-	-	-					
	8	✓	-	-	-					
	9	✓	-	-	-					
	10	✓	-	-	-					
	11	✓	✓	✓	✓					
	12	✓	-	-	-					
	13	✓	-	-	-					
	14	✓	✓	✓	✓					
	15	✓	✓	✓	✓					
	16	✓	-	-	-					
	17	✓	-	-	-					
	18	✓	-	-	-					
	19	✓	-	-	-					
	20	✓	-	-	-					
	21	✓	-	-	-					
	22	✓	-	-	-					
	23	✓	-	-	-					
	24	✓	-	-	-					
	25	✓	-	-	-					
	26	✓	-	-	-					
	27	✓	-	-	-					
	28	✓	-	-	-					
	29	✓	-	-	-					
	30	✓	-	-	-					
	31	✓	-	-	-					
	32	✓	-	-	-					
	33	✓	-	-	-					
	34	✓	-	-	-					
	35	✓	-	-	-					
	36	✓	-	-	-					

Samsung Electronics Co., Ltd.
Ex. 1050, p. 282

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
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	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014					
	37	✓	-	-	-					
	38	✓	-	-	-					
	39	✓	-	-	-					
	40	✓	-	-	-					
	41	✓	-	-	-					
	42	✓	-	-	-					
	43	✓	-	-	-					
	44	✓	-	-	-					
	45	✓	-	-	-					
	46		✓	-	-					
	47		✓	✓	✓					
	48		✓	✓	✓					
	49		✓	✓	✓					
	50		✓	✓	✓					
	51		✓	✓	✓					
	52		✓	✓	✓					
	53		✓	-	-					
	54		✓	-	-					
	55		✓	✓	✓					
	56		✓	✓	✓					
	57		✓	✓	✓					
	58		✓	✓	✓					
	59		✓	✓	✓					
	60		✓	✓	✓					
	61		✓	✓	✓					
	62		✓	✓	✓					
	63		✓	✓	✓					
	64		✓	✓	✓					
	65		✓	✓	✓					
	66		✓	✓	✓					
	67		✓	✓	✓					
	68		✓	✓	✓					
	69		✓	✓	✓					
	70		✓	✓	✓					
	71		✓	✓	✓					
	72			✓	✓					

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Ex. 1050, p. 283

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014					
	73			✓	✓					

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APPLICANT'S PREAPPEAL CONFERENCE BRIEF

Applicant requests reversal of a final rejection of (all) pending claims 1, 3-5, 11, 14-15, 47, 52 and 55-73 as allegedly obvious over Coteus (USPB 20100220536), Best (USPB 20100091537), Koshizuka (USPB 20100182855), and Solomon (USPB 20060262586).

SUMMARY.

Applicant's invention relates to a memory controller that transmits information together with a memory read command where that information mandates that a preamble with specific duration is to be used in the event of a rank switch. The preamble is used for timing calibration and precedes the transmission of data. That is, as explained at ¶12 of Applicant's publication (USPB 20120023363), different ranks of memory can experience timing drift and, while current timing information is available for ranks in active use, a timing update must typically be performed before a new rank can be accessed. Applicant's invention permits a memory controller (e.g., that "knows" that a rank switch is being requested) to specify in connection with a transmitted command (e.g., via a flag) that a preamble certain be used on a selective basis (i.e., in the event of a rank switch).

Applicant's invention for purposes of preappeal is represented by pending claim 1, with underlined limitations being clearly not shown by the cited art:

> "1. A method of operation in a memory controller, the method comprising:
> transmitting a read command which specifies that a memory device output data;
> *with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;*
> receiving the preamble; and
> sampling the data output from the memory device in dependence on the preamble output from the memory device;
> *wherein*
> *the memory controller is to control multiple ranks of memory, and*
> *the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations*."

ERRORS IN THE REJECTION.

The Examiner relies upon Koshizuka as teaching programmable preamble time in connection with accessing a memory device, and Solomon as disclosing rank switches. The Examiner concludes based on this combination that the claimed invention would have been obvious. Applicant views the rejection as unreasonable.

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Koshizuka is directed to DDR3 standard SDRAM devices and a DLL OFF mode used for power savings (see Koshizuka, ¶13). According to Koshizuka, this mode is rarely used in practice because it is possible for a memory controller to miss a read preamble, and thus experience undesirable error, given certain drift conditions (¶¶ 15-17). To address this, Koshizuka teaches that a memory device should have a register to store a preamble length (see Koshizuka FIG. 9), and that a memory controller "beforehand" should specify a preamble duration, given consideration to frequency of the system clock, existing preamble timing, phase delay variation, and clock delay (¶ 20). Koshizuka does not deal with rank switch, but rather, contemplates that a memory controller will program the preamble register once during a calibration mode, and then never change that value during normal operation, all so as to enable accurate operation in the DLL OFF mode.

Contrary to the Examiner's allegations, Koshizuka does not teach transmission of information with a read command that specifies whether a certain preamble duration to be used with that command, and Koshizuka's advance register programming would not be effective to obtain the results of Applicant's invention; that is, with Koshizuka's system, one would need at least two commands, including a first one to program a register (i.e., in connection with a calibration), followed at some point thereafter by a read command – such a scheme is not what Applicant claims and is inconsistent with the solution to Applicant's problem, because in Applicant's system, a given rank may or may not involve a rank switch (i.e., the entire point is that if there is no rank switch, the preamble duration in question should not be used because it precedes data output and therefore would presumably affect the ability to efficiently pipeline memory commands to the same rank). The Examiner appears to miss this subtlety, and simply argues that "lengthening a preamble is equivalent to varying a preamble;" this assertion is incorrect, i.e., Koshizuka does not teach that a preamble duration should be "varied," but rather, that it should be calibrated and set once by a mode register programming command (e.g., at system initialization), so as to permit error-free use of the DLL OFF mode during normal system operation.

Solomon does not provide the referenced teachings. That is, Solomon at ¶¶55-61 discloses that a multiple rank memory system can electrically isolate respective ranks to decrease server electrical load, and thereby permit that server to run faster with better signal integrity. At ¶61, Solomon discusses back-to-back memory commands that involve a rank switch, and teaches that the memory controller should insert an additional clock cycle between commands representing a rank switch, to effectively provide more time when a second read command in a series is directed to a different

memory device. As should be apparent to the Examiner, this teaches a different solution than Applicant's claimed invention, i.e., it teaches that a memory controller should handle rank switches by delaying issuance of a second read command. One skilled in the art presented by this teaching would not be lead to Applicant's invention, but rather, would be counseled to do exactly what Solomon says (i.e., delay read command issuance).

As to the remaining two references, Coteus and Best, these references do not add anything to the rejection.

Coteus has *nothing to do* with specifying a preamble duration and Coteus does not "adjust" a strobe preamble time. Rather, Coteus deals with "the unusable dead time" (which he refers to as the 'preamble' time of a data bus, which is a period during which valid data conventionally cannot be transmitted because timing is not yet stable). What Coteus says (see, e.g., ¶¶ 59 and 89) is that during this time, data (i.e., parity bits) can be transmitted at half-rate and still be received notwithstanding lack of current timing information, because such data can be sampled without needing high accuracy provided by a valid strobe signal. Coteus specifically says as follows: "Exemplary embodiments utilize the dead time on the data bus, while the data strobe is stabilizing, to transfer data at a slow rate (e.g. a rate that permits data to be captured without the need of a data strobe or with the use of the strobe during a period in which the strobe has reduced timing accuracy." In other words, Coteus simply says that the *down time of the data bus* can be shortened by transmitting data at half-speed during the dead period (i.e., during a time interval conventionally thought unusable); Coteus as far as Applicant can tell does not specify a strobe preamble duration during this period, or anything analogous and does not specify that a preamble duration be used in connection with a rank switch. There is for example no teaching or suggestion in Coteus that a memory controller should transmit, with a read command, information that causes a memory device to utilize a specific preamble period in connection with a rank switch, as specified by Applicant's claims.

Best does not supply the teachings missing from Coteus, and as far as Applicant can tell, is cited simply to show that a strobe is used to sample data bits at a destination.

Considering the cited art as a whole, none of Applicant's claims can be considered obvious over that art. As noted above, Applicant's invention, represented for purposes of preappeal by claim 1, relates to a memory controller that transmits information together with a memory read command where that information specifies selects whether a preamble duration should be used, that is, the event

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of a rank switch. The cited art fairly read does not teach or suggest this. Rather, Koshizuka teaches that a register can be programmed to have a calibrated, preplanned preamble duration, but Koshizuka does not teach either that this value should be varied, nor that a preamble duration should be tied to a rank switch. Koshizuka does not disclose any structure by which a memory device might utilize contents of a register, fixing a preamble period, to determine whether or not a given read command should benefit from register contents or not. Solomon deals with rank switches, but proposes that a memory controller should insert extra time between issuance of memory read commands to new ranks. Coteus also deals with rank switches, but simply teaches that dead time when a strobe is unreliable can be recovered using half-rate data transmission (i.e., such that accurate sampling is not necessary because of much slower data speeds). Best simply discloses that a strobe can be used for data sampling.

None of these references, together or apart, suggest specifying preamble usage as part of, or with information transmitted together with, a read command. As noted earlier, access to a given rank of memory might or might not involve a rank switch – Applicant's invention permits a memory controller to selectively specify whether it wants memory to use a specific preamble or preamble parameter to be employed in conjunction with a specific command, and thus provides a capability not taught or suggested by any reference of record or any combination of references of record.

Applicant therefore submits that the cited art clearly fails to teach the underlined limitations seen above and thus clearly fails to establish a *prima facie* case of unpatentability.

Respectfully submitted,

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35675
Attorney for Applications

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Ex. 1050, p. 288

Doc Code: AP.PRE.REQ

PTO/AIA/33 (07-09)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
2012043 / RA764PUS

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Signature _____

Typed or printed name _____

Application Number	Filed
13/105798	05/11/2011

First Named Inventor: Ian Shaeffer

Art Unit	Examiner
2185	SAIN, Guatam

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 35675.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Marc P. Schuyler/
Signature

Marc P. Schuyler
Typed or printed name

408 6556375
Telephone number

16 January 2015
Date

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of one forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD

Docket Number (Optional): 2012043 / RA764PUS

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on _____.

Signature _____

Typed or printed name _____

In re Application of: Ian Shaeffer

Application Number	Filed
13/105798	05/11/2011

For: Protocol including a command-specified timing reference signal

Art Unit	Examiner
2185	SAIN, Gautam

Applicant hereby **appeals** to the Patent Trial and Appeal Board from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 800

☐ Applicant asserts small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by 50%, and the resulting fee is: $ _____

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Therefore, the fee shown above is reduced by 75%, and the resulting fee is: $ _____
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☐ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. _____.

☑ Payment made via EFS-Web.

☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/AIA/22 or equivalent) is enclosed.
For extensions of time in reexamination proceedings, see 37 CFR 1.550.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant

☑ attorney or agent of record
Registration number 35675

☐ attorney or agent acting under 37 CFR 1.34
Registration number _____

Signature /Marc P. Schuyler/

Typed or printed name Marc P. Schuyler

Telephone Number 408 655 6375

Date January 16, 2015

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 41.20(b)(1) and 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13105798
Filing Date:	11-May-2011
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2012043 / RA764.P.US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of Appeal	1401	1	800	800
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	21232346
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	16-JAN-2015
Filing Date:	11-MAY-2011
Time Stamp:	14:44:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1000
RAM confirmation Number	1045
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Pre-Brief Conference request	A001-PreappealConferenceBrief-RA764PUS-2015-01-16-FIN.pdf	67086 5aa1866d547b85ed537da0301d464ac1b62fe918	no	4
Warnings:					
Information:					
2	Pre-Brief Conference request	A002-aia0033-PREAppealConferenceRequest.pdf	46278 5a65eb67e20d4e4c4b87d904b43b400ec5303c11	no	1
Warnings:					
Information:					
3	Notice of Appeal Filed	aia0031-NoticeAppeal.pdf	265126 fd9eebb0fa9674b5e5e52c126bbd79aeabb0caee	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32252 26f8c58d6ed950d589a37790621b29d92f73f369	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	410742		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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<u>New International Application Filed with the USPTO as a Receiving Office</u>
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application No.	Applicant(s)
	13/105,798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2135

This is in response to the Pre-Appeal Brief Request for Review filed 16 January, 2015.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: *1,3-5,11,14-15,47,52,55-73*.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *GAUTAM SAIN*.	(3) *Sanjiv Shah*.
(2) *Kevin Ellis*.	(4)_____.

/GAUTAM SAIN/ Examiner, Art Unit 2135		/SANJIV SHAH/ Supervisory Patent Examiner, Art Unit 2135

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number:	13/105798
Confirmation Number:	3982
First Named Inventor:	Ian Shaeffer
Title:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
Filing Date:	May 11, 2011
Priority Claimed:	July 22, 2010
Publication No.:	USPB 20120023363
Attorney Docket:	2012043 / RA764PUS

APPLICANT'S APPEAL BRIEF

All references below to Applicant's specification are made as required by rule with reference to the paragraph numbering of the application as-filed, and not the publication, USPB 20120023363.

1. Real Party In Interest.

The real party in interest is Rambus Inc.

2. Related Appeals, Interferences And Trials.

None.

3. Summary Of Claimed Subject Matter.

As background, and discussed at ¶¶11-12 of Applicant's specification, inactive ranks of memory in some memory designs can still consume power when they are not being accessed, which is undesirable. To address this, certain circuit elements (such as a phase-locked loop or "PLL" or delay-locked look or "DLL") can be moved from the memory ranks to a memory controller, to reduce idle

memory rank power consumption. In some of these designs, the memory controller stores phase information for each memory rank timed relative to a memory controller internal clock, so as to be able to properly sample incoming data. Unfortunately, in these designs, while power is saved, when an inactive rank of memory is again accessed, it is first necessary to perform timing calibration so as to update the stored phase information for drift and noise which has shifted proper sampling points relative to previous accessed of the inactive rank; this interferes with memory bandwidth, because there is a delay following a rank switch (i.e., needed for this drift calibration) before a previously inactive rank can be again properly accessed.

The solution presented by Applicant's claims on appeal and discussed in part by ¶13 of the Specification is a memory controller that transmits an indication with a read command (e.g., the command includes a digital bit or special flag) that informs memory whether or not to insert a preamble period prior to outputting the read data. The memory controller can selectively use this flag in the event of a rank switch, to trigger sending by the memory device to the memory controller of a timing reference signal ("TRS") in advance of the read data, for example, on one or more data links, which the memory controller then uses to derive phase information and optimize a sampling point for ensuing data relative to the memory controller's internal clocks - see, e.g., ¶13 of the Specification.

Claims 1, 3-5, 11, 14-15, 47-52 and 54-73 are pending, with claims 1, 14, 61 and 69 being independent claims. As required by the rules, Applicant summarizes the independent claims with reference to paragraph numbers of Applicant's specification as filed.

Claim 1.

"1. A method of operation in a memory controller, the method comprising:
transmitting a read command which specifies that a memory device output data;
with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;
receiving the preamble; and
sampling the data output from the memory device in dependence on the preamble output from the memory device;
wherein
the memory controller is to control multiple ranks of memory, and
the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations."

Applicant's specification provides for a method of operation in a memory controller (see ¶13 of the specification) where the memory controller transmits to a memory device a read command specifying whether the memory device is to insert a preamble period prior to outputting data in response to the read command. As disclosed at ¶¶32-34, in some embodiments, a preamble request can take the form of a command field (i.e., one or more bits long) to specify whether a specific duration or period of the preamble is to be used before data. For example, the memory controller can use a one-bit command field to determine whether to send a long preamble or a short preamble, or whether to use a preamble at all (see, e.g., ¶32). As further described at ¶23, responsive to this read command and accompanying information, the memory controller receives a toggling signal for the preamble duration sent by a memory rank in advance of data; the memory controller uses this timing reference signal to perform fast phase updates to correct a substantial portion of the timing drift and jitter relative to previously stored phase information for the rank (see ¶21).[1] Based on the updated timing information derived from the use of the preamble, the memory controller then uses proper phase points relative to its internal sampling clock to properly sample ensuing read data from the particular rank of memory (¶13).

See also, e.g., FIG. 3 (preambles 302 and 304), and ¶¶16 and 32-39 generally; a preamble period can be used when there is a rank switch in connection with a data read, but can be omitted in between consecutive reads to the same rank (such as represented by consecutive read data Q:[A0] and Q:[A1], or consecutive read data Q:[A2] and Q:[A3]). The fact that the memory controller specifies this information together with any given command permits the memory controller to determine whether consecutive sets of read data are received with or without a timing gap. For example, as just referenced (relative to FIG. 3), the memory controller can specify with *each* read command whether read data is to be preceded by a preamble duration (e.g., preamble 302 or 304) (which, as just described, permits a memory controller to specify command-by-command whether or not it wants additional time to achieve fast timing update for a previously inactive rank). Since the memory controller "knows" whether consecutive reads involve a rank switch, it can omit the preamble interval when ensuing reads are to the same rank, as the memory controller already has current timing information; this permits reads to occur more frequently (i.e., without an idle period) because reads can occur back-to-back as seen in FIG. 3 (i.e., there is no break in between Q:[A0] and Q:[A1], or between Q:[A2] and Q:[A3]). Note that in some embodiments, as depicted in FIG. 3 and discussed by ¶23, the preamble and associated timing signal

[1]As disclosed at ¶24, for example, a fast edge tracking circuit 136 of the memory controller can use a significantly faster clock rate to lock to timing edges within the preamble duration, before actual read data requested by the command arrives at the memory controller. Stored phase information maintained by the memory controller is then updated, for example, as disclosed at ¶21 of Applicant's specification.

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(TRS) can be added to the head of a read data burst from a newly accessed memory rank (i.e., it is sent on a data link), and the memory controller selectively commands insertion of this signal and associated preamble duration when it needs to update correction for drift and jitter (e.g., when once again accessing a previously inactive rank, to update timing for drift and noise). See also ¶21. In other embodiments, the preamble signal can be placed on an EDC link (element 130 in FIG. 1A, as also discussed at ¶22).

Claim 14.

"14. A memory controller, comprising:

transmitter circuitry to transmit a read command to a memory device, the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data, wherein the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations; and

receiver circuitry to receive the preamble from the memory device and to sample the data from the memory device in dependence on the preamble.

The memory controller is seen as element 102 in FIGS. 1A & FIB. 1B and as element 510 in FIG. 5. The memory controller includes interface circuitry (such as depicted by numeral 518-1 of FIG. 5) where that interface circuitry includes a transmitter circuit and a receiver circuit (see ¶59). The memory controller uses such a transmitter circuit to transmit to a memory device a read command specifying whether the memory device is to use a preamble (e.g., with a timing reference signal ("TRS")) prior to outputting data in response to the read command; generally speaking, and as is well known, the memory controller has a transmit circuit (transmitter circuitry) for each link over which it is to transmit information, and a receiver circuit (receiver circuitry) for each link over which it is to receive information. As disclosed at ¶¶32-34, in some embodiments, a command sent by the memory controller can include a command field (one or more bits long) to specify whether a specific duration preamble is to be output and/or to vary the duration of the preamble, as needed. For example, the memory controller can use a one-bit command field to determine whether to send a long preamble or a short preamble, or whether to use specific duration of preamble at all prior to read data output (see, e.g., ¶32). As further described at ¶23, the memory controller responsive to this information (transmitted with a read command) is

provided the requested preamble by a memory rank (see, e.g., ranks 104 of FIGS. 1A-1B) in advance of data, and it receives timing information using a receiver circuit. The memory controller uses this requested preamble duration to perform fast phase updates to correct a substantial portion of the timing drift and jitter relative to previously stored phase information for the rank (see ¶21). The memory controller uses this information to adjust receive timing at the memory controller (¶14) relative to a memory controller internal clock, and uses this receive timing (i.e., stored phase information) to thereby properly sample ensuing read data from the particular rank of memory (¶13) using a receiver circuit of the memory controller.

See also, e.g., FIG. 3 (preamble periods 302 and 304), and ¶¶16 and 32-39 generally; a preamble can be used when there is a rank switch in connection with a data read, but can be omitted in between consecutive reads to the same rank (such as represented by Q:[A0] and Q:[A1], or between Q:[A2] and Q:[A3]). The fact that the memory controller specifies this information together with any given command permits the memory controller to determine whether consecutive sets of read data are received with or without a timing gap. For example as just referenced (relative to FIG. 3), the memory controller can specify with *each* read command whether read data is to be preceded by a preamble (e.g., 302 or 304) (which, as just described, permits a memory controller to specify command-by-command whether or not it wants additional time to achieve fast timing update for a previously inactive rank). Since the memory controller "knows" whether consecutive reads involve a rank switch, it can omit the preamble when consecutive reads are to the same rank, or when write data is being sent (e.g., as is discussed relative to FIG. 4A). Note that in some embodiments, as depicted in FIG. 3 and discussed by ¶23, a preamble and associated timing signal (TRS) can be added to the head of a read data burst from a newly accessed memory rank, such that precedes read data over a data link. In other embodiments (see ¶21), the preamble can be applied over an EDC link such as link 130 from FIG. 1A. The memory controller selectively commands insertion of a specific preamble duration when it needs to update correction for drift and jitter (e.g., when once again accessing a previously inactive rank, to update timing for drift and noise).

Claim 61.

> "61. A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch."

As disclosed at ¶45 of Applicant's specification, the memory devices can be dynamic random access memory (DRAM) devices, and the memory controller can be a controller that controls such DRAM devices; the DRAM devices are arranged in multiple ranks such as ranks 104 from FIG. 1. Each rank of memory includes at least one memory device (see elements 512 from FIG. 5). The memory controller includes interface circuitry (such as depicted by numeral 518-1 of FIG. 5) for communicating with the various ranks of memory where that interface circuitry includes a transmitter circuit and a receiver circuit (see ¶59). The memory controller uses such a transmitter circuit to transmit to an addressed one of the memory ranks a read command specifying whether the memory rank is to insert a preamble (e.g., and output a timing reference signal ("TRS")) prior to outputting data in response to the read command; generally speaking, and as is well known, the memory controller has a transmit circuit (transmitter circuitry) for each link over which it is to transmit information ,and a receiver circuit (receiver circuitry) for each link over which it is to receive information. As disclosed at ¶¶32-34, in some embodiments, a preamble request command sent by the memory controller can include a command field (one or more bits long) to specify whether a specific duration or period of preamble is to be output and/or to vary the duration of the preamble to allow the memory controller to specify the length of the preamble as needed. For example, the memory controller can use command fields to determine whether the preamble should be long or short (e.g., for a long or short timing reference signal), or whether to use specific preamble duration at all (see, e.g., ¶32). As further described at ¶23, the memory controller responsive to this information (transmitted with a read command) is provided with the requested preamble by a memory rank prior to data (see, e.g., ranks 104 of FIGS. 1A-1B) and uses a receiver circuit to process timing information provided using this preamble. The memory controller uses this information to perform fast phase updates to correct a substantial portion of the timing drift and jitter relative to previously stored phase information for the rank (see ¶21). The memory controller can

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update stored phase information at the memory controller (¶21), with this phase information being used relative to an internal sampling clock, so that the memory controller uses phase information respective to each rank to properly sample data from that rank using a receiver circuit of the memory controller.

See also, e.g., FIG. 3 (preambles 302 and 304), and ¶¶16 and 32-39 generally; a preamble can be used when there is a rank switch in connection with a data read, but can be omitted in between consecutive reads to the same rank (such as represented by Q:[A0] and Q:[A1], or between Q:[A2] and Q:[A3]). The fact that the memory controller specifies this information together with any given command permits the memory controller to determine whether consecutive sets of read data are received with or without a timing gap. For example as just referenced (relative to FIG. 3), the memory controller can specify with *each* read command whether read data is to be preceded by a preamble (e.g., preamble 302 or 304) or whether the preamble is to be omitted (e.g., as in between read data Q:[A0] and read data Q:[A1] from FIG. 3, or in between read data Q:[A2] and read data Q:[A3]). Thus, these reads are efficiently performed, since the read command is performed without any idle time on the data bus in between consecutive reads. Since the memory controller "knows" whether consecutive reads involve a rank switch, it can select, for each command, whether it wishes to request that a preamble be inserted in advance of data. Note that in some embodiments, as depicted in FIG. 3 and discussed by ¶23, the preamble and associated timing signal (TRS) can be added to the head of a read data burst from a newly accessed memory rank; the preamble and an associated TRS in other embodiments can also be put on an EDC link (such as link 130 from FIG. 1A). See also ¶21.

Claim 69.

"69. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command."

As disclosed at ¶45 of the Applicant's specification, the memory devices can be dynamic random access memory (DRAM) devices, and the memory controller can be a controller that controls such DRAM devices, arranged in multiple ranks such as ranks 104 from FIG. 1. Each rank of memory includes at least one memory device (see elements 512 from FIG. 5). The memory controller includes interface circuitry (such as depicted by numeral 518-1 of FIG. 5) for communicating with the various ranks of memory where that interface circuitry includes a transmitter circuit and a receiver circuit (see ¶59). The memory controller uses such a transmitter circuit to transmit to an addressed one of the memory ranks a read command specifying whether the memory rank is to insert a preamble (and, e.g., output a timing reference signal ("TRS")) prior to outputting data in response to the read command; generally speaking, and as is well known, the memory controller has a transmit circuit (transmitter circuitry) for each link over which it is to transmit information, and a receiver circuit (receiver circuitry) for each link over which it is to receive information. As disclosed at ¶¶32-34, in some embodiments, a preamble request command sent by the memory controller can include a command field (e.g., a single bit) to specify whether a specific duration or period of preamble is to be output and/or to vary the duration of the preamble to allow the memory controller to specify the length of the preamble as needed. For example, the memory controller can use a single bit to specify whether the memory rank is to insert a long preamble or a short preamble, or whether to use specific preamble duration at all (see, e.g., ¶32). As further described at ¶23, the memory controller responsive to this information (transmitted with a read command) is sent a timing reference signal during the requested preamble by a memory rank prior to the provision of data (see, e.g., ranks 104 of FIGS. 1A-1B) and the memory controller receives this signal with a receiver circuit. The memory controller uses this requested preamble signal to perform fast phase updates to correct a substantial portion of the timing drift and jitter relative to previously stored phase information for the rank (see ¶21). The memory controller uses this information to adjust rank-specific receive timing at the memory controller (¶14), and it updates the phase/timing information relative to an internal sampling clock, to thereby properly sample ensuing read data from the particular rank of memory (¶13) (i.e., using a receiver circuit of the memory controller). Sampling is thus performed in dependence on processing of the preamble as well as the memory controller's internal sampling clock.

See also, e.g., FIG. 3 (preambles 302 and 304), and ¶¶16 and 32-39 generally; a preamble can be used when there is a rank switch in connection with a data read, but can be omitted in between consecutive reads to the same rank (such as represented by Q:[A0] and Q:[A1], or between Q:[A2] and Q:[A3]). The fact that the memory controller specifies this information together with any given

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command permits the memory controller to determine whether consecutive sets of read data are received with or without a timing gap. For example as just referenced (relative to FIG. 3), the memory controller can specify with *each* read command whether read data is to be preceded by a preamble (e.g., preamble 302 or 304) or whether this preamble is to be omitted in favor of gapless reads of consecutive data. Since the memory controller "knows" whether consecutive reads involve a rank switch, it can select, for each command, whether it wishes to request a preamble. Note that in some embodiments, as depicted in FIG. 3 and discussed by ¶23, a timing reference signal (TRS) can be added to the head of data from a newly accessed memory rank, or an EDC signal (as indicated by ¶21).

4. Argument.

As required by 37 C.F.R. §41.37(iv), Applicant argues each rejection separately under a different heading. Claims 1, 3-5, 11, 14-15, 47-52 and 54-73 are pending.

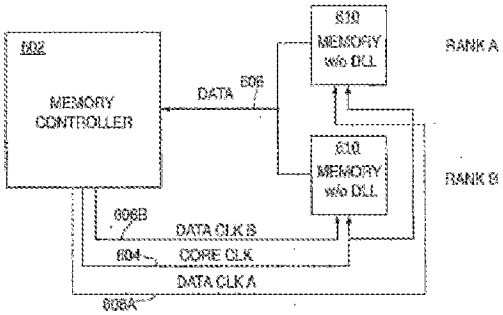
A. The rejection of claims 1, 3-5, 11, 14-15, 47, 49, 51, 54, 56, 58-59, 61-62, 64, 66, 68-70 and 72-73 over Coteus (USPB 20100220536), Best (USPB 20100091537) and Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586) is clear error.

Each reference cited by the Examiner shows a different solution to a different problem than was faced by Applicant, and is applied by the Examiner without regard to what the reference actually teaches. Applicant's position is that the references do not teach all of the limitations of the rejected claims, and the references, fairly considered, would teach one skilled in the art to do exactly what they say, without shedding any light on the problem faced by Applicant, or Applicant's claimed solution; simply stated, the presently claimed invention is clearly ***not*** rendered obvious by the Examiner's cited art.

As noted above in the summary section, the present invention relates to a memory controller that sends read commands to ranks of memory where each read command can be selectively accompanied by information that causes an addressed memory rank to apply a preamble duration before outputting data; that is, a previously inactive rank is commanded in this way (such that the preamble is selectively used during rank switches) and this information can be omitted during same-rank-reads, enabling more efficient use of the data links (i.e., without idle time). The preamble before

data is used by the memory controller to update stored phase information used to sample data relative to an internal clock of the memory controller.

The Examiner's first reference, Coteus, shows in one embodiment a memory system where a memory controller provides respective I/O clocks to each rank of memory (and where these clocks are separate from the memory device's core clocks and are used to transmit read data to the memory controller); See, i.e., the cover figure of Coteus, reproduced below.

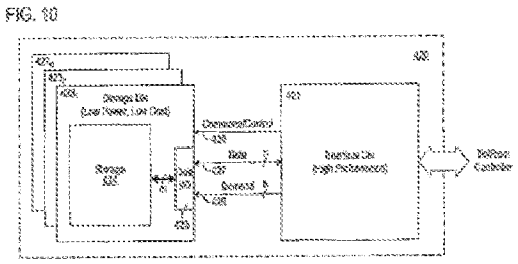


This is a different solution to a different problem than addressed by Applicant. That is, Coteus' structure (with clocks respective to each rank) permits a memory controller to levelize data receipt from different ranks by independently adjusting the data clock to each memory rank; in other words, because each rank is a slightly different "distance" from the memory controller, a time bubble would normally need to be inserted between reads from different ranks on a shared data bus in order to avoid the possibility of data collision. Coteus addresses this by providing the respective I/O clocks; by staggering these clocks in an amount related to the different in distance, Coteus can remove the need for a time bubble, because the read data from respective ranks are sent by the memory devices in a manner that is pre-aligned with one another on a data bus and at arrival at the memory controller (see FIG. above and, e.g., ¶58 of Coteus).

At ¶59, touted by the Examiner, what Coteus says is that a source-synchronous strobe timing signal also accompanies data; this strobe signal timing signal (DQS) is only turned on when data is being sent, and so it requires a preamble time before it becomes stable. Coteus notes that high speed data cannot be accurately sampled until this signal becomes stable and, so, to remedy the fact that a data bus is normally idle during this time, Coteus proposes that data should be transferred at a slow-speed during this "dead time," that is, in a manner that can be read without the DQS until the DQS becomes stable enough to sample read high speed data; this then permits better utilization of memory bandwidth.

Coteus teaches at best, away from the present invention, because it teaches in respective embodiments that (a) one should use a design where each rank transmits its own DQS to be used for sampling of data which that DQS accompanies (which renders it unnecessary for a memory controller to track rank specific phase and update this phase for sampling when inactive ranks are later accessed), and/or (b) one should use a design there each rank uses calibrated transmit timing, so that all data arrives irrespective of rank at the same phase (i.e., which renders it unnecessary for a memory controller to sample data using tracked phases for each rank). These are competing solutions to Applicant's proposed structure where a memory controller should track and update sampling phases for each respective rank of memory and use its own internal clock and selectively command a preamble as part of a read command when there is a rank switch. In the DQS embodiment of Coteus referenced by the Examiner, Coteus's DQS ALWAYS has a preamble (i.e., instability period) when each rank asserts it, and Coteus does not teach that this preamble should be changed, varied, or applied in any manner. Coteus certainly would not teach any one skilled in the art, i.e., per Applicant's claims, that a read command should be accompanied by information that tells a newly-accessed memory rank whether it is to selectively utilize a preamble of specific duration in advance of outputting read data.

The Examiner argues that Best shows sampling data from a memory device in dependence on a preamble. This is false and represents Examiner confusion. That is, Best (which is assigned in common to the Real Party In Interest for this application), relates to a high-performance memory integrated circuit package having an interface die and separate storage dice. This is seen in FIG. 10 of Best, reproduced below. The stated purpose for this is that conventional DRAM features inefficient high-speed logic circuitry that consumes too much power, so Best proposes efficiencies through the use of dedicated storage and I/O dice that feature different design processes (see i.e., ¶36 of Best).



As seen in the FIG. above, Best's interface die generates timing for operations in each storage die, and this interface die then provides a "demand signal" (see element 450 in FIG. 12 of Best) to all memory dies to time the transmission of read data from each memory die in Best's IC package to his interface die, for ensuing relay to a memory controller. At ¶64 of Best, touted by the Examiner, all Best says is

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that the interface die generates a timing signal which is provided to the transmitter of Best's storage dice so as to property coordinate transmission of read data to the interface die. Succinctly stated, this has nothing to do with a "preamble," or a preamble used for timing acquisition in the event of a rank switch, or anything else to do with the present claims, and is simply a timing signal to output data; this timing signal is generated or delayed by Best's interface circuit, so that read data arrives back at the interface circuit at a proper time. It is unclear to Applicant what teaching the Examiner thinks he is getting from Best or what the Examiner thinks Best would suggest to one faced with Applicant's problem, or what Best is supposedly contributing relative to the present claims. Best does not teach a memory controller that issues a read command to memory accompanies by information that causes a rank of memory to selectively insert a preamble before data in the event of a rank switch, nor does it shed any light on the problem which confronted Applicant. Furthermore, when the Examiner attempts to justify combination of Coteus and Best and states "it would've been obvious.... to modify ... Coteus with Best" for "providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power" (see page 5 of the Final Office Action), Applicant has no idea what the Examiner is even saying, i.e., it is unclear what or how Best would suggest anyone modify Coteus for any purpose.[2]

That is, Best relates to a high performance memory IC where "recognizing that compromises inherent in conventional DRAM fabrication processes yield relatively inefficient high-speed logic circuitry, reduced power may be achieved by relegating the high-speed circuitry that forms the control and signaling interface of a conventional memory die to a separate interface die that is fabricated using a process that yields power-efficient high speed circuitry" (see i.e., ¶36 of Best). Best would teach one that a memory IC should split the actual storage and interface onto separate dies ("period"); Best has little to no pertinence to the present application.

The Examiner's third reference Koshizuka relates to memory devices that output a strobe timing signal that is source synchronous with data; this signal from the memory device is used by the memory

[2]Applicant notes this generalized assertion falls well short of the type of teaching to combine references required by the CAFC. As stated in In Re As stated by the CAFC in *In Re Dembiczak*, Opinion 98-1498 (CAFC 1999), a teaching or motivation to combine references must be clear and particular and broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence of such a teaching: "In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination *in the manner claimed*" (In Re Rouffet, 149 F.3d 1350, 47 U.S.P.Q.2d 1453, CAFC 1998), emphasis added. Such a showing has not been made here, and the Examiner's purported motivation to combine is based on a general, conclusory statement having nothing to do with Applicant's problem.

controller to sample read data. As is known, such a timing signal typically has a preamble that signifies a transition from a low-Z state to a high-Z state (which signifies that the strobe is about to become active and that the memory controller should begin to look for transitions in the strobe signal). According to Koshizuka, ¶13, DDR3 SDRAMs have a DLL OFF mode that in practice is rarely used, because in DLL OFF mode, it is difficult for a memory controller to detect a DQS preamble with sufficient time to prepare receiver circuitry for sampling data. According to Koshizuka, the solution to this problem is to provide a DDR3 SDRAM memory controller with a DLL OFF mode DQS detection circuit, and to provide the memory devices with a read preamble register, programmable by the memory controller as part of general register configuration, to define in advance a length of the DQS preamble that will be used. See, e.g., ¶¶17-18, 20, 37 and 39 of Koshizuka. That is, Koshizuka clearly contemplates that in connection with a mode setting (i.e., DLL OFF), the DDR3 SDRAM controller will program the memory device register with a value that will then be used for the duration of the assigned mode - Koshizuka expressly indicates that this programming is done "beforehand" at system start up or at some fixed-time interval (see ¶52 if Koshizuka).

The Examiner states that Koshizuka teaches that a read command should be transmitted with information that specifies a duration of a preamble; *this is false, and as just stated, is contradicted by Koshisuka*. That is, Koshizuka states that his DQS preamble is programmed (i) in concert with DLL OFF mode in a DDR3 SDRAM, (ii) at system start up or otherwise in connection with a mode change, (iii) by programming a register of a memory device, i.e., by some type of programming command that writes configuration registers of the SDRAM (see ¶¶56-60 of Koshisuka). It is noted that Koshizuka teaches that a DQS preamble (i.e., the beginning of a high-Z state before signal toggling begins) should be programmed for use in a DLL OFF mode of a DDR3 memory device, i.e., Koshizuka has nothing to do with rank switches.[3]

Finally, the Examiner states that Coteus, Best and Koshizuka do not disclose multiple ranks, but that Solomon does.[4] Solomon relates to a multi-rank memory system that (as with Coteus), uses rank-specific, source-synchronous strobe signals that accompany read data (see, i.e., ¶64 of Solomon). As succinctly described at his ¶15, Solomon proposes that a memory system having multiple ranks of

[3]It is noted that Applicant's system relates to an environment where a memory controller normally uses a PLL or DLL (i.e., it is on) to provide a source clock, and tracks per-rank phase relative to this clock, but where, due to memory rank dormancy and voltage drift or power supply noise, the per-rank phase must be recalibrated or adjusted before data arrives to ensure data is sampled at the proper point.

[4]This position is not understood as Coteus clearly teaches multiple ranks but, of course, with a completely different solution than suggested by Applicant, i.e., where one should a source-synchronous strobe from each rank. Solomon adds nothing to Coteus.

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memory should selectively electrically couple and decouple each rank (e.g., when that rank is read) so as to reduce loading. Notably, Solomon does discuss ranks switches, and indicates that when there is a rank switch, it is necessary to insert a "bubble" in between read commands to avoid a data collision (i.e., because the ranks are not exactly at the same "distance" from the memory controller - this is the problem addressed by Coteus, i.e. Coteus' solution of using an I/O clock provided to interface circuitry of each rank, dedicated to that rank, see the discussion above). Solomon adds nothing at all to Coteus and is cumulative thereto.

That is, notwithstanding the Examiner's arguments, all Solomon contributes is that a bubble (inserted time intervals) should be inserted between consecutive read commands addressed to different ranks of memory (see, i.e., ¶62 of Solomon) and that a source-synchronous strobe from each rank should accompany data and be used by a memory controller to sample that data. This does nothing at all to address Applicant's problem or suggest Applicant's solution, i.e., one skilled in the art presented with Solomon would be counseled to do exactly as Solomon suggests, i.e., insert time bubbles (i.e., extra clock cycles worth of idle time) in between read commands to respective ranks and rely on a DQS at the memory controller from each rank for proper sampling; Solomon would not suggest to one skilled in the art that one ought to "dispense with everything Solomon says" in favor of a preambule duration that precedes the output of data and which is used only when there is a rank switch, pursuant to information electively included with the memory read command by the memory controller.

Summarizing, the Examiner's position is clear error, because no cited reference teaches that a memory controller should transmit, with a read command, elective information specifying that a preamble duration should precede the outputting of data, in connection with a rank switch. That is, with reference to claim 1, the cited art clearly fails to show at least the following limitations:

"1. A method of operation in a memory controller, the method comprising:
transmitting a read command which specifies that a memory device output data;
with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;
receiving the preamble; and
sampling the data output from the memory device in dependence on the preamble output from the memory device;
wherein
the memory controller is to control multiple ranks of memory, and
the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations."

None of the art suggests the underlined limitations. Considering what each cited reference would suggest to one skilled in the art:

1) Coteus states that a dedicated IO clock should be provided by a memory controller to each memory rank (i.e., to levelize receipt of read data by the memory controller), that each rank should provide a source-synchronous strobe signal for the memory controller to sample data, and that data can be transmitted at half-rate until the strobe signal from a given rank becomes stable. Coteus does not deal with the need to recalibrate timing for drift following reactivation of a rank, because in one embodiment, Coteus continuously provides I/O clocks to memory (i.e., decoupled from memory core clocks) and in another embodiment, Coteus relies on a source-synchronous DQS.

Best relates to a memory IC where storage and interface dies are separated to provide higher performance; Best does not shed any light on the claimed solution to Applicant's problem, and it is unclear to Applicant what the Examiner thinks he is getting from Best.

Koshizuka teaches that in connection with a DLL OFF mode, a DDR3 SDRAM should have a DQS preamble duration programmed in advance, for example, at system startup. Koshizuka does not deal with ranks of memory or have anything to do with recalibrating timing to adjust for voltage drive or power supply noise or timing phases tracked by a memory controller, but merely indicates that a memory controller may wish to lengthen a DQS preamble if its DLL is off pursuant to a DLL OFF mode, e.g., by programming a SDRAM control register at system startup.

Solomon is redundant to Coteus, and also indicates that a source synchronous DQS provided by each rank should be used to sample data.

There is nothing at all, by any stretch of imagination in the cited art, that suggest that a memory controller should electively accompany a read command (i.e., in the event of a rank switch) that indicates that a newly accessed rank should insert a specific duration of preamble before transmitting data. That is, notwithstanding the Examiner's cited art and arguments, Applicant's invention permits a memory controller to select whether or not a duration of preamble will be used with each command. There is nothing in the art that (1) relates to the problem of drift tracking upon rank switch, or that (2) provides the same capability as the present invention. Assuming Koshizuka teaches that a preamble duration may be programmed into a memory device by writing a mode register during some sort of configuration (e.g., startup) mode, this would require multiple commands, i.e., Koshizuka does not teach

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a structure or a solution where a read command effectively selects a preamble according to information transmitted with that command. Thus, no reference cited by the Examiner is even capable of obtaining the same results as the claimed solution. Such a teaching is not supplied anywhere in the cited art.

As is well-known, an obviousness determination requires a determination of what the cited references would each fairly suggest to one of ordinary skill in the art, a determination of the differences between the teachings of the art and the claims at issue, and a determination as to whether the claimed invention would have been an obvious solution to the problem which was faced by the Applicant in view of those differences. An Examiner is required to consider portions of the references which teach away from the claimed solution and cannot combine references where the purported combination would destroy the principle of operation of one of the references.

In this case, only two cited references deal with rank switches, Coteus and Solomon. Solomon teaches that reads from each rank should be accompanied by a source-synchronous strobe timing signal, so as to permit a memory controller to properly sample data from that rank. Solomon teaches that it may be necessary to insert time bubbles in between read commands so as to avoid data collisions (because the data transmission windows from different ranks might overlap). Coteus teaches exactly the same thing, except Coteus addresses the data collision issue via an embodiment that provides an I/O clock dedicated to each rank, where the memory controller skews phase of these clocks so as to levelize arrival of read data at the memory controller (i.e., to avoid the collision issue). One skilled in the art and presented with these references would be counseled to do exactly as these references suggest, i.e., *to use a source-synchronous DQS transmitted along with read data from each rank so as to provide the memory controller with exact sample timing along with the read data or, per Coteus' forwarded I/O clock embodiment, provide respective clocks to memory ranks so that arriving data has no rank-dependent phase difference*. One would not be counseled to, as the Examiner suggests, completely dispense with the DQS, and instead use phase tracking respective to each rank at the memory controller and a preamble duration which allows the memory controller to update its tracked phase information for a previously inactive rank. The present claims recite this structure by claiming a memory controller that, with a read command, issues information that tells an addressed memory rank to insert a specific preamble duration in advance of outputting data, and by adjusting sample timing in dependence on a preamble signal (e.g., and the memory controller's internal clocks). Solomon is cumulative to Coteus, Best adds nothing to the rejection, and Koshizuka teaches that a DQS preamble can have a programmable duration that is defined at startup so as to support a DLL OFF mode. There is no cited

reference which addresses Applicant's problem or provides the claimed solution, and the differences between the claimed invention and the cited art are not such that one skilled in the art would have "obviously" designed a system where a preamble is specified by a read command in the event of a rank switch. The claimed invention is clearly patentable notwithstanding any position of the Examiner to the contrary.

Thus, Applicant respectfully requests reversal of the Examiner on all rejected claims.

Applicant also expressly and separately argues the patentability of many of the dependent claims.

Relative to claims 3 and 15, these claims specify that Applicant's sampling of read data is performed dependent both on a sampling clock and at the preamble from an accessed rank. The Examiner's position is that Coteus, Best, Koshizuka and Solomon would make this obvious, because this would "provide the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power." Once again, it is not understood "what" teachings the Examiner is supposedly combining from each reference; Coteus and Solomon teach that a DQS signal is used to sample data. It would NOT be "obvious" to simply disregard this in and instead substitute a memory controller sampling clock, nor is it understood (by anyone) how doing this would "provide the benefit of scaling bandwidth and storage capacity for improving signaling rate" as offered by the Examiner. This rejection is traversed.

Similarly, Applicant's claim 4 adds that the claimed preamble is transmitted on a common signal line with an error detection and correction (EDC) signal from the memory device. The Examiner asserts that this is shown by ¶59 of Coteus, *which is false*. That is, as referenced above, what Coteus says is that during the time that his DQS signal is becoming stable, and during the time that his data links are therefore unusable for high-speed data, that data can be transmitted at slower speeds (e.g., half-speed) and can still be sampled without a stable strobe signal. According to Coteus ¶59 (see sixth line from end), this increases usable bandwidth on the data bus and potentially permits inclusion of error detection information along with the data within the time allotted for a data transfer. However, Coteus still does not show or use any type of 'preamble' as claimed by Applicant; that is to say, what the Examiner has done is to "latch onto" the "naked" use of the word "preamble" by Coteus, and then assert without analytical rigor that this somehow suggests Applicant's claimed limitation. In fact, what Coteus proposes is that this normally usually dead time can be filled with data transmitted at half rate (i.e., 'slower rates') which can be sampled notwithstanding that the strobe signal is not yet stable; Coteus is proposing transmitting data during this time, so this is not "a preamble that is to be output prior to

commencing outputting of data" as claimed by Applicant, i.e., Coteus does not teach the limitations of Applicant's claims. This additional difference also underscores patentability.

Claims 5 and 11 further specify that the read command to memory includes information that specifies a length of the preamble, e.g., whether the preamble duration is to last for 16 or 32 clock cycles as disclosed at ¶33 of Applicant's specification. The Examiner asserts that this is shown by Koshizuka, which is false. That is, Koshizuka shows expressly that that a duration of a DQS preamble is programmed as part of a general process of programming configuration registers of an SDRAM at startup, and in connection with a DLL off mode. Neither Koshizuka nor any other reference of record teaches a memory controller that issues a read command, that selectively indicates *with the command* whether a preamble duration is to be used by addressed memory prior to outputting data, and further (per claims 5 and 11), a value that varies the duration of the preamble, all in connection with a rank switch. This additional reason further underscores patentability.

Relative to claims 47 and 54, these claims specify that the information transmitted by the memory controller with the read command further causes the memory device to use a longer duration of the preamble in connection with a rank switch relative to no rank switch. The Examiner asserts this is shown by Coteus, ¶58 because "a delay time of a passively controlled delay line is shorter than that of a conventional delay line"). Applicant has no idea what the Examiner is arguing and believes that the Examiner's statement represents confusion as to what Coteus teaches. That is, Coteus is proposing (see Coteus FIG. 1 and ¶57) is that each memory rank is provided a respective clock for IO operations, and that a delay line is used to adjust phase of each respective clock. This is not a "preamble," and it does not cause a memory device to use a longer or shorter duration when there is a rank switch as opposed to no rank switch; rather, what Coteus is proposing is that (a) memory devices in rank A use clock phase 1 (generated by first delay line in memory controller) *always and irrespective of same rank or switched-rank access*, and that (b) memory devices in rank B use clock phase 2 (generated by second delay line in memory controller) *always and irrespective of same rank or switched-rank access*, and that because of minute differences in distance of each rank from the memory controller (i.e., that might otherwise cause read data boundaries to overlap), these delays cause read data boundaries to aligned with each other in flight back to the memory controller, such that no "bubble" needs to be inserted between memory commands. Coteus does not show transmitting "anything relating to a preamble" with a read command, and does not show using a read command to vary "anything" in terms of read output timing or procedure. That is, once again, the cited art does not show the limitations of the claims.

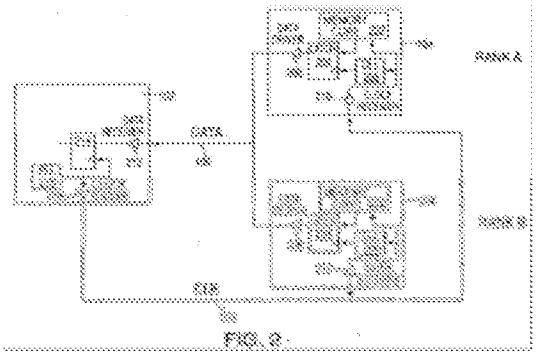
Applicant's claims 49 and 56 recite that the preamble comprises a toggling pattern, wherein the memory controller uses this toggling pattern as a calibration preamble. The Examiner asserts that Koshizuka discloses this, but here also the Examiner is wrong. That is, Koshzuka teaches that a memory device should output a DQS with a preamble (i.e., a high-Z state that precedes toggle) which is defined "beforehand" and is for use in conjunction with a DDR3 SDRAM "DLL OFF" mode. Koshizuka's toggling pattern is his strobe signal, and is used to sample data, i.e., not for calibration. The Examiner touts Koshizuka ¶59 as indicating to the contrary, but all Koshizuka indicates is that the DQS is a toggling pattern and is preceded by a preamble and followed by a postamble, as is conventional for a DQS. There is no disclosure that this toggling signal is used for "any" type of calibration.

Applicant's claims 51 and 59 effectively indicate that the information transmitted with the read command is a digital bit which specifies that the memory device should use a specific duration preamble prior to outputting data. The Examiner asserts this is shown by Koshizuka ¶59, because Koshizuka discloses that his memory device generates a DQS preamble using "a read data flag" which is internally generated by Koshizuka's memory device when memory device logic detects a read command. Applicant fails to see how this teaches that a *memory controller should transmit a bit to a memory device* indicating whether a preamble should be inserted to precede data output. That is, the Examiner has clearly confused internal operation of Koshizuka's DQS generation circuit with fields transmitted to a memory device by a memory controller as part of a read command. Koshizuka simply teaches that a DQS signal is output with read data, nothing more, and does not teach that a preamble should be selectively inserted for a rank switch (e.g., per claims 1 and/or 14) by the memory controller, where this is commanded by the memory controller using a single digital bit within the read command. Once again, Applicant submits that the Examiner's position clearly fails to show the limitations of the claims and clearly fails to establish a position of unpatentability.

Claim 61 is similar to claim 14, but is still more specific in that it says that the claimed DRAM memory controller formats and transmits the command in a manner that indicates that an addressed rank is to output a specific duration preamble prior to outputting data if there is a rank switch, and that the addressed rank is not to use the specific duration preamble prior to outputting data if there is no rank switch. Once again, the cited art is completely silent on any operation of this type, simply indicating (per Coteus and Solomon) that a source-synchronous DQS should be output by each given rank of memory any time the given rank of memory is the subject of a read command. Once again, there is no cited art that says that a preamble duration should be selectively used in dependence on

whether there is a rank switch. Applicant notes that claims 62-68 depend on claim 61, and are additionally allowable for this reason.

Claim 63 (and its dependency, claim 64) depend on claim 61 but add that the memory controller's receiver circuitry is to sample data from each rank in a manner dependent on rank-specific phase information which is derived from the preamble for the respective rank. Claim 64 further adds (to claim 63) that the memory controller stores this phase information specific to each rank, and updates this phase information in dependence on the preamble (which precedes data transmission) from the respective rank. The Examiner asserts this is shown by Coteus, because Coteus shows a memory controller with a phase locked loop (PLL), element 216 in Coteus FIG. 2. Once again, this does not show the limitations of Applicant's claims. In this embodiment of Coteus, Coteus uses a PLL to generate an internal clock, which he then uses to latch data from a memory controller receiver into the memory controller's internal logic; this PLL is used for all memory reads irrespective of phase, and Coteus in no way uses rank-specific phase information "derived from the preamble for the respective rank" to sample data. In Coteus (see FIG. 2, reproduced below), element 214 is a latch, and is used for timing domain



crossing in-between receiver 212 and the memory controller's internal logic. In fact, what Coteus proposes for the embodiment of his FIG. 2 is that the elements on the memory device (i.e. the memory core 202, data driver 206, latch 204, and DLL 206) receive the clock forwarded 108 from the memory controller and are adjusted so as to align output data with the edge of clock 108 (i.e., to levelize data across ranks, as stated earlier). Coteus therefore expressly teaches that for this embodiment, the memory controller does not sample data from each rank using rank-specific phase information, but rather teaches that one should adjust transmission from each rank so that data arrives at the memory controller WITHOUT any rank-specific phase deviation. Once again, it is submitted that the reference clearly fails to show the limitations of the rejected claims. Coteus does not show a memory controller adjusting phase for each rank dependent on a respective preamble (claims 63-64) or a memory controller that stores and updates stored phase information for each rank (claim 64) for sampling of

read data. The Examiner asserts that Best discloses phase information "specific to each rank," however, once again, this is clear error, i.e., Best simply discloses that an interface die can provide timing to a memory die, which then outputs data using the provided timing; the Examiner has not pointed to any teaching in Best that a memory controller (or interface tie or anything else) stores rank-specific phase information, which it uses for data *sampling* (or any other purpose). Again, the rejection is clear error and should be withdrawn.

Claim 66 specifies that the read command transmitted by the memory controller comprises a digital bit which specifies that the memory device should use the specific duration preamble prior to outputting data. Claim 69 is similar to claim 66, and is argued with claim 66, because it also includes this limitation (and has limitations similar to claim 61). The Examiner asserts this is shown by Koshizuka ¶59, because Koshizuka discloses that his memory device generates a DQS preamble using "a read data flag" which is internally generated by Koshizuka's memory device when memory device logic detects a read command. Applicant fails to see how this teaches that a *memory controller should transmit a bit to a memory device* indicating whether a preamble should be inserted to precede data output. That is, the Examiner has clearly confused internal operation of Koshizuka's DQS generation circuit with fields transmitted to a memory device by a memory controller as part of a read command. Koshizuka simply teaches that a DQS signal is output with read data, nothing more, and does not teach that a preamble should be selectively inserted for a rank switch (e.g., per claims 1 and/or 14) by the memory controller, where this is commanded by the memory controller using a single digital bit within the read command. Once again, Applicant submits that the Examiner's position clearly fails to show the limitations of the claims and clearly fails to establish a position of unpatentability. It is further noted that claims 70-71 depend on claim 69 and so are also patentable for the reasons advanced above.

B. The rejection of claims 50, 57, 65 and 71 over Coteus (USPB 20100220536), Best (USPB 20100091537), Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586), in further view of Jacob (USPB 20060248261) is clear error.

The Examiner's position is that Coteus/Best/Koshizuka and Solomon show the limitations of the independent claims (1, 14, 61 and 69) and that Jacob further shows (relative to claims 50, 57, 65 and 71) a memory controller that transmits information with a read command indicating that a bank should be automatically precharged following retrieval of read data responsive to the read command. This rejection is traversed for multiple reasons.

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First, the arguments stated above in connection with claims 1, 14, 61 and 69 are hereby incorporated by reference; that is, Coteus/Best/Koshizuka and Solomon do not teach the invention of the independent claims, and Jacob is not cited as supplying the missing teachings. In fact, Jacob teaches away from the invention because Jacob deals with a memory system having multiple ranks, and teaches that in order to avoid inefficiencies caused by a T_{RTRS} parameter (i.e., a rank switching time), it is necessarily to use a command rescheduling algorithm that decouples column access commands from row activation commands, and in so doing, avoid or minimize the bandwidth loss associated with rank switches (see, i.e., Jacob, ¶¶33-35). One skilled in the art presented with Jacob would be taught to do what Jacob literally suggests and use the described scheduling algorithm, not use special commands that call for preamble insertion in the event of rank switches (as claimed by Applicant). Because Jacob does not supply teachings missing from Coteus/Best/Koshizuka and Solomon, claims 1, 14, 61 and 69 and all of their dependencies are patentable notwithstanding Jacob.

Relative to claims 50, 57, 65 and 71, the Examiner's position is also clear error, because Jacob does not suggest the limitations added by these claims: at ¶19 of Jacob, touted by the Examiner, Jacob sets forth "Preliminary Information" (i.e., standard DDR3 SDRAM parameters) prior to proceeding to discussion of Jacob's invention; at table 1 within ¶19, Jacob merely introduces the concept of T_{RAS} (meaning the row access strobe time, i.e., the time it takes after a row activation until another row can be accessed) and indicates that after expiration of this time, a DRAM sense array could be precharged. This is true of all DRAM, i.e., Jacob does not indicate any precharge mechanism of any type, and he does not suggest the language of claims 50, 57, 65 and 71 *where the read command includes information that commands auto-precharge following retrieval of data by a memory device*. Because Jacob does not show the claimed limitations, and because the Examiner has not demonstrated any art that does, the rejection of these claims is in error for this additional reason, i.e., the Examiner has failed to establish a *prima facie* case. Perhaps otherwise stated, simply citing to art that mentions on a naked basis the "concept of precharge" falls well short of showing the limitations of the rejected claims in the cited art, including the limitation that a precharge be commanded by information transmitted with a read command. For these additional reasons, the rejection of these claims must be reversed.

C. <u>The rejection of claims 48 and 55 over Coteus (USPB 20100220536), Best (USPB 20100091537), Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586), in further view of Korger (USPT 6600681) is clear error.</u>

The Examiner's position is that Coteus/Best/Koshizuka and Solomon show the limitations of the independent claims (1 and 14) and that Korger shows (relative to claims 48 and 55) that a memory controller derives rank-specific phase information using the duration of the preamble (i.e., from an accessed rank). This rejection is also clear error for multiple reasons.

First, the arguments stated above in connection with claims 1, 14, 61 and 69 are hereby incorporated by reference; that is, Coteus/Best/Koshizuka and Solomon do not teach the invention of the independent claims, and Korger is not cited as supplying the missing teachings. In fact, Korger has nothing to do with multiple ranks at all, and simply teaches a method for detecting a strobe timing signal (DQS). What Korger teaches (and as is well known) is that a DQS signal transitions from a low-Z state (during which a DQS signal floats and is unreliable and must not be sampled) to a high-Z state (a preamble period before DQS oscillation begins), and that it is necessary to mask the DQS signal until the high-Z state is reliable, so that the DQS signal is not sampled and erroneously interpreted as having "live" timing edges before the proper time; Korger's improvement is in the generation of this mask signal and when it is applied and removed. Korger if anything teaches away from the present invention, because it deals with DQS receipt by a memory controller (i.e., a signal transmitted from memory rendering it unnecessary for the memory controller to recalibrate phase information for previously inactive memory in order to track drift). Beyond this, however, Korger does not teach that a read command should be accompanied by information which specifies that a preamble be used prior to outputting data, and it most certainly does not teach (per claims 48 and 55) that a memory controller should sample data using rank specific phase information derived from a preamble (output prior to data). That is, the only thing that Korger derives from his preamble is a mask signal, which is not used in any manner to sample data, but simply to mask receiver circuits *so that they do not sample data* until the mask signal is removed (i.e., until the high-Z state is reliable). Korger's receiver circuits then, as is conventional, use the DQS' oscillation edges to sample data, but these edges (and their phase and Korger's mask signal) have nothing whatsoever to do with the DQS preamble, and Korger does not teach deriving rank specific phase information from a preamble.

Korger does not teach the limitations missing from Coteus/Best/Koshizuka or Solomon, and so it cannot render obvious any claims of this application. With specific focus on dependent claims 48 and 55, Korger also fails to show the limitations of these claims, but rather, merely teaches a method (and circuit) for generating a DQS mask signal. It is respectfully submitted that, once again, the Examiner's position lacks analytical rigor, and that a rejection of these claims cannot be maintained.

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D. The rejection of claims 52 and 60 over Coteus (USPB 20100220536), Best (USPB 20100091537), Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586), in further view of Kim (USPB 20110055671) is clear error.

The Examiner's position is that Coteus/Best/Koshizuka and Solomon show the limitations of the independent claims (1 and 14) and that Kim further shows (relative to claims 52 and 60) that a memory controller receives the claimed preamble from a first set of signaling resources (e.g., an EDC link) and samples the data from a second set of signaling resources (e.g., a data link). This rejection is also clear error for multiple reasons.

First, the arguments stated above in connection with claims 1, 14, 61 and 69 are hereby incorporated by reference; that is, Coteus/Best/Koshizuka and Solomon do not teach the invention of the independent claims, and Kim is not cited as supplying the missing teachings. The Examiner points to FIG. 13 and ¶¶3 and 89 as supposedly relevant, but all that Kim indicates (see, e.g., FIG. 13 and ¶89) is that a command from a memory controller can be accompanied by a parity bit, which the memory device uses to detect errors in the command or the address. Note that this does not equate to a memory controller receiving an EDC signal *from* a memory device, which the Examiner apparently thinks it does. Kim *does not*, insofar as Applicant can find, teach that any type of EDC signal should be sent *to* a memory controller. Also, Kim does not teach that any type of preamble should be sent on an EDC link (in any direction). Finally, Kim does not indicate (i.e., per the limitations of the rejected claim) that a preamble duration should be selectively applied by a memory rank prior to outputting data (i.e., per the independent claims) where the preamble and data are applied on different signaling links (per the rejected dependent claims). In short, none of the cited art discloses the limitations of the rejected claims; Kim does not supply the teachings missing from the independent claims, and it wholly fails to show anything of pertinence relative to claims 52 and 60 (other than a memory controller could transmit a parity bit for command and address information *to a memory device*). Applicant fails to see the relevance of Kim.

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CONCLUSION.

As with all of the rejected claims, the cited art fails to show all of the limitations of any claim, and fails to conceptually or otherwise show even the "gist" of Applicant's claimed solution. No reference of record deals with a memory controller that updates phase information for respective ranks of memory where that phase information is used to sample data for the respective rank, and where a preamble is selectively used prior to outputting read data in the event of a rank switch, so that the controller can reacquire timing for an inactive memory rank (and phase update for drift and noise). Generally speaking, the cited art suggests that one ought to use a per-rank DQS signal, that is, a source-synchronous timing signal that travels "next to" data and thus propagates with edges that are precisely related to an idea sampling point, that the memory controller then directly uses for sampling. There is nothing at all in the cited art that suggests that a memory controller should accompany a read command with information that tells a memory device that it should insert a preamble, before outputting data, in the event of a rank switch. Applicant therefore submits that the rejection is untenable and cannot be maintained based on the current record. Applicant respectfully submits that all claims of record are clearly patentable over the cited art, and requests reversal of the Examiner on all issues.

Respectfully Submitted,
ATTORNEY FOR APPLICANTS

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35675

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5. Claims Appendix.

1. (Previously Presented) A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data;

with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;

receiving the preamble; and

sampling the data output from the memory device in dependence on the preamble output from the memory device;

wherein

the memory controller is to control multiple ranks of memory, and

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory device using a sampling clock, and wherein the method further comprises sampling the data based on both the sampling clock and the preamble.

4. (Previously Presented) The method of claim 3, further comprising:

after receiving the preamble, receiving an error detection and correction (EDC) signal from the memory device via a common signal line that is used to convey the preamble, wherein a first bit of the EDC signal is received after a first bit of the read data; and

using the EDC signal to update phase of sampling of the data after the receiving the preamble.

5. (Previously Presented) The method of claim 1, wherein the read command includes information that specifies a length of the preamble.

6-10. (Canceled)

11. (Previously Presented) The method of claim 1, wherein the information identifies a length for a predetermined time parameter associated with the preamble.

12-13. (Canceled)

14. (Previously Presented) A memory controller, comprising:

transmitter circuitry to transmit a read command to a memory device, the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data, wherein the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations; and

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receiver circuitry to receive the preamble from the memory device and to sample the data from the memory device in dependence on the preamble.

15. (Previously Presented) The memory controller of claim 14, further comprising circuitry to generate a sampling clock, the receiver circuitry operable to sample the data output from the memory device in dependence on the sampling clock and the preamble.

16-46. (Canceled)

47. (Previously Presented) The method of claim 1, wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch.

48. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

49. (Previously Presented) The method of claim 1, wherein the preamble comprises a toggling pattern, and wherein the method further comprises using the toggling pattern as a calibration preamble to facilitate sampling of read data from a specific rank.

50. (Previously Presented) The method of claim 1, wherein transmitting further comprises transmitting the read command to the memory device together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

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51. (Previously Presented) The method of claim 1, wherein transmitting the read command with the information further comprises transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of the data.

52. (Previously Presented) The method of claim 1, wherein the receiving the preamble includes receiving the preamble from a first set of signaling resources and wherein sampling the data includes sampling the data output by the memory device from a second set of signaling resources.

53-54. (Canceled)

54. (Previously Presented) The memory controller of claim 14, wherein the memory controller is to cause the transmitter circuitry transmit the information in a manner to cause the memory device to output a longer preamble in connection with the rank switch, relative to no rank switch.

55. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry is to sample the data output from the memory in a manner dependent on rank-specific phase information derived by the memory controller from the preamble.

56. (Previously Presented) The memory controller of claim 14, wherein the preamble comprises a toggling pattern, and wherein the memory controller is adapted to use the toggling pattern as a calibration sequence to facilitate sampling of read data from a specific rank.

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57. (Previously Presented) The memory controller of claim 14, wherein the memory controller is operable to cause the transmitter circuitry to transmit the read command together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

58. (Previously Presented) The memory controller of claim 14, wherein the duration represents a specific length preamble, and wherein the transmitter circuitry is to transmit the information in manner that specifies that the memory device should output the specific length preamble prior to commencing outputting of the data.

59. (Previously Presented) The memory controller of claim 14, wherein the information comprises a digital bit that indicates that the memory device should utilize the duration of the preamble in connection with the outputting of the data.

60. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry comprises circuitry to receive the preamble from a first set of signaling resources, and circuitry to sample the data from a second set of signaling resources.

61. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch.

62. (Previously Presented) The DRAM memory controller of claim 61, wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch.

63. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank.

64. (Previously Presented) The DRAM memory controller of claim 63, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles.

65. (Previously Presented) The DRAM memory controller of claim 61, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

66. (Previously Presented) The DRAM memory controller of claim 61, wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data.

67. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles.

68. (Previously Presented) The DRAM memory controller of claim 61, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data.

69. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command.

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70. (Previously Presented) The DRAM memory controller of claim 69, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory.

71. (Previously Presented) The DRAM memory controller of claim 70, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

72. (Previously Presented) The method of claim 1, further comprising instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

73. (Previously Presented) The memory controller of claim 14, wherein the memory controller is further to command the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Application Number: 13/105,798
Filing Date: May 11, 2011
Appellant(s): SHAEFFER ET AL.

Marc. P. Schuyler
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/24/2015 appealing from the Office action mailed 10/1/2014.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

1. (Previously Presented) A method of operation in a memory controller, the method comprising:

transmitting a read command which specifies that a memory device output data;
with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;
receiving the preamble; and
sampling the data output from the memory device in dependence on the preamble output from the memory device;
wherein
the memory controller is to control multiple ranks of memory, and
the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory device using a sampling clock, and wherein the method further comprises sampling the data based on both the sampling clock and the preamble.

4. (Previously Presented) The method of claim 3, further comprising:
after receiving the preamble, receiving an error detection and correction (EDC) signal from the memory device via a common signal line that is used to convey the preamble, wherein a first bit of the EDC signal is received after a first bit of the read data; and
using the EDC signal to update phase of sampling of the data after the receiving the preamble.

5. (Previously Presented) The method of claim 1, wherein the read command includes information that specifies a length of the preamble.

6-10. (Canceled)

11. (Previously Presented) The method of claim 1, wherein the information identifies a length for a predetermined time parameter associated with the preamble.

12-13. (Canceled)

14. (Previously Presented) A memory controller, comprising:
transmitter circuitry to transmit a read command to a memory device, the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data, wherein the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive

memory operations; and
receiver circuitry to receive the preamble from the memory device and to sample the data from the memory device in dependence on the preamble.

15. (Previously Presented) The memory controller of claim 14, further comprising circuitry to generate a sampling clock, the receiver circuitry operable to sample the data output from the memory device in dependence on the sampling clock and the preamble.

16-46. (Canceled)

47. (Previously Presented) The method of claim 1, wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch.

48. (Previously Presented) The method of claim 1, wherein the memory controller is to sample the data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

49. (Previously Presented) The method of claim 1, wherein the preamble comprises a toggling pattern, and wherein the method further comprises using the toggling pattern as a calibration preamble to facilitate sampling of read data from a specific rank.

50. (Previously Presented) The method of claim 1, wherein transmitting further comprises transmitting the read command to the memory device together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

51. (Previously Presented) The method of claim 1, wherein transmitting the read command with the information further comprises transmitting a digital bit to the memory device which specifies

that the memory device should utilize the specific duration prior to commencing outputting of the data.

52. (Previously Presented) The method of claim 1, wherein the receiving the preamble includes receiving the preamble from a first set of signaling resources and wherein sampling the data includes sampling the data output by the memory device from a second set of signaling resources.

53-54. (Canceled)

54. (Previously Presented) The memory controller of claim 14, wherein the memory controller is to cause the transmitter circuitry transmit the information in a manner to cause the memory device to output a longer preamble in connection with the rank switch, relative to no rank switch.

55. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry is to sample the data output from the memory in a manner dependent on rank-specific phase information derived by the memory controller from the preamble.

56. (Previously Presented) The memory controller of claim 14, wherein the preamble comprises a toggling pattern, and wherein the memory controller is adapted to use the toggling pattern as a calibration sequence to facilitate sampling of read data from a specific rank.

57. (Previously Presented) The memory controller of claim 14, wherein the memory controller is operable to cause the transmitter circuitry to transmit the read command together with information indicating that sense amplifiers of the memory device should be automatically precharged following retrieval of read data in response to the read command.

58. (Previously Presented) The memory controller of claim 14, wherein the duration represents a specific length preamble, and wherein the transmitter circuitry is to transmit the information in

manner that specifies that the memory device should output the specific length preamble prior to commencing outputting of the data.

59. (Previously Presented) The memory controller of claim 14, wherein the information comprises a digital bit that indicates that the memory device should utilize the duration of the preamble in connection with the outputting of the data.

60. (Previously Presented) The memory controller of claim 14, wherein the receiver circuitry comprises circuitry to receive the preamble from a first set of signaling resources, and circuitry to sample the data from a second set of signaling resources.

61. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:
transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and
receiver circuitry to receive the preamble of the specific duration from each of the ranks and to sample the data from each rank in dependence on a respective one of the preambles;
wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output of the preamble of the duration if there is no rank switch.

62. (Previously Presented) The DRAM memory controller of claim 61, wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch.

63. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank- specific phase information for each rank being derived by the memory controller from the preamble from the respective rank.

64. (Previously Presented) The DRAM memory controller of claim 63, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank, and wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles.

65. (Previously Presented) The DRAM memory controller of claim 61, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

66. (Previously Presented) The DRAM memory controller of claim 61, wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data.

67. (Previously Presented) The DRAM memory controller of claim 61, wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles.

68. (Previously Presented) The DRAM memory controller of claim 61, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data.

69. (Previously Presented) A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising

at least one DRAM memory device, the DRAM controller comprising:
transmitter circuitry to transmit each of the read commands together with a digital bit of information which specifies according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and
receiver circuitry to receive the preamble from each of the ranks and to sample data from the respective rank in dependence on the respective preamble;
wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command.

70. (Previously Presented) The DRAM memory controller of claim 69, wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory.

71. (Previously Presented) The DRAM memory controller of claim 70, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data.

72. (Previously Presented) The method of claim 1, further comprising instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

73. (Previously Presented) The memory controller of claim 14, wherein the memory controller is further to command the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble, wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-5, 11, 14, 15, 47, 49, 51, 54, 56, 58, 59, 61, 62, 64, 66, 68-70, 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (US 20100220536, filed Feb. 27, 2009) in view of Best (US 20100091537, published Apr. 15, 2010) and further in view of Koshizuka (US 20100182855, published Jul. 22, 2010) and Solomon (US 20060262586, published Nov 2006)

Claims 1 and 14, Coteus (20100220536) discloses a method of operation in a memory controller (e.g., memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device, see para 0057), the method comprising:

transmitter circuitry to transmit a read command to a memory device (e.g., Fig. 4 shows three read commands 402, where first read command ("Read A") is directed to a memory device in memory rank A, para 0066)

receiver circuitry to receive the preamble from the memory device (e.g., data receiver 212, para 0064; receiving a clock signal at a receiving device, and data strobe signals in response to read command, see para 0089, Fig. 22; adjusting data strobe preamble time for adjusting data transfer speed, 0059).

Coteus does not expressly disclose, but Best discloses wherein

to sample the data from the memory device in dependence on the preamble (e.g., in response to demand signal, sampling signals 444 are generated that that are time delayed relative to the demand signals 434 in the read data chunk. Sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, para 0064).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus in view of Best does not expressly disclose, but Koshizuka discloses

the read command being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018; detecting a read preamble with suitable timing to receive read data (0013). A read preamble register that specifies length of the read preamble outputted prior to output of read data (0018, Fig. 9), compared to claimed limitation of information which specifies a duration of a preamble that is output prior to commencing outputting data, according to the broadest reasonable interpretation. Fig. 9 discloses setting of read preamble length register where preamble length is selected (0060). The length of the read preamble signal is lengthened (0064)).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Coteus in view of Best and Koshizuka does not expressly disclose, but Solomon discloses

memory controller is to control multiple ranks (e.g., number of ranks 32, 0052, where memory controller 20 transmits data signals to the ranks 32a and 32b, para 0053);

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations (e.g., read commands accesses data from different memory devices... pre-amble time interval of the second read data burst.. Fig. 6B shows successive read accesses from different memory devices, para 0061; selectively switching between two ranks of memory devices 30 (0055). Data bursts with pre-amble time interval, and two consecutive read bursts from different memory devices than the first read command (interpreted as equivalent to claimed rank switch)(0061). Memory boundaries between ranks of memory module prior to issue read commands where a wait time is inserted to avoid collisions between back-to-back adjacent read commands which cross memory device boundaries (0062).).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claims 3 and 15. Coteus does not express disclose, but Best discloses

Controller is to sample data from memory using a sampling clock and sampling data based on both the sampling clock and preamble (e.g., internal clock signal is used to sample and generate strobe signals output via data path in conjunction with read data, providing a timing reference for establishing a read-data sampling time, para 0038, Fig. 1)

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Claim 4. Coteus discloses after receiving the preamble, receiving EDC signal from memory via common signal line that is used to convey the preamble, wherein a first bit of EDC

signal is received after a first bit of the read data; using the EDC signal to update phase of sampling of the data after the receiving the preamble (e.g., permitting error detection information to be transferred in addition to the data, 0059).

Claims 5 and 11. Coteus in view of Best does not expressly disclose, but Koshizuka discloses

a read command includes information that specifies length of preamble; wherein the information identifies a length for a predetermined time parameter associated with the parameter (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

Claim 47, 54. Coteus discloses wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch (e.g., delay time of passively controlled delay line is shorter than that of a conventional delay line, para 0058).

Claims 49 and 56. Coetus and Best do not expressly disclose but Koshizuka discloses

toggling pattern as a calibration preamble ....(e.g., read data is outputted with a signal toggle until read data output of a prescribed burst length is complete, 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claims 51 and 59. Coteus, and Best do not expressly disclose, but Koshizuka discloses

Transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 58. Coteus, and Best do not expressly disclose, but Koshizuka discloses

Duration represents length of preamble, and transmitter is to transmit information that device should output length preamble prior to data (e.g., outputting read data in in synch with data strobe signal including outputting a read preamble signal of the length specified by preamble register prior to timing of starting output of read data determined in advance, followed by outputting a data strobe signal to the data strobe terminal, from the timing of starting output of the read data, see para 0018, 0042).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

Claim 61 is rejected for reasons similar to Claims 1 and 14 (above) for similar limitations. Further, Coteus, and Best, do not expressly disclose, but Koshizuka discloses

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior

memory command (e.g., the pre-amble time of the second read command is skipped when there is a back-to-back adjacent read as two consecutive bursts of data from the same memory device, para 0060; disclosed burst from same memory device are interpreted as claimed no rank switch).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of improving performance and capacity of memory modules (see Solomon, para 0003).

Claim 62. Coteus discloses wherein the DRAM memory controller is to cause the transmitter circuitry to transmit the information in a manner to cause the addressed one of the ranks to output a preamble at an earlier time in connection with the rank switch, relative to no rank switch (e.g., for a read, preamble time is required prior to completing read transfer to allow data strobe to achieve a stable switching state, 0086, Fig. 19)

Claim 63. Coteus discloses wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank (e.g., controller includes phase lock loop (PLL) 216, 0064, Fig. 2)

Claim 64. Coteus, and Best discloses, wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank (e.g., sample command signals to generate strobe signals output via data path in conjunction with read data to establish read-data sampling within memory controller… including phase adjustment to enable desired phase offsets between sampling times and transitions in incoming data signals, para 0038).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power (see Best, para 0002, 0036).

Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles (e.g., controller sets preamble length beforehand and then determines time to start detection of clock to start transmission in consideration of phase delay outputted by controlled device, para 0020).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 66. Coteus, and Best do not expressly disclose, but Koshizuka discloses

wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 67. Coteus discloses wherein the receiver circuitry comprises circuitry to receive the respective data from signaling resources that are independent from signaling resources used to convey each of the preambles (e.g., generates a separate data clock 606 for each rank. controller clocking to monitor drifts on data bus 608, and adjust timing of clocks 606 to each rank, such that data can be captured and contention does not occur on bus 608, para 0068 Fig. 6).

Claim 68. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of data memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claim 69 is rejected for reasons similar to Claims 1, 14 and 61 (above) for similar limitations. Further, Coteus, and Best do not expressly disclose, but Koshizuka discloses

a digital bit of information which specifies according to its state that an addressed one of the ranks should be outputted of a duration of a preamble prior to outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8; disclosed flag is interpreted as disclosing claimed digital bit).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuks, para 0013).

Claim 70. Coteus discloses wherein the transmitter circuitry comprises circuitry to transmit commands and address information for each read command at a data rate that is less than a data rate used for transmission of the data from ranks of DRAM memory (e.g., running core clock at a slower frequency enables slower signaling rate for command and address signal, where command and address signals do not require same transfer rate as data because memory core speed is slower than I/O transfer speed, para 0071, Fig. 9).

Claims 72 and 73, Coteus in view of Best does not expressly disclose, but Koshizuka discloses

Instructing the memory device to employ a selective one of a relatively-longer duration preamble or a relatively-shorter duration preamble wherein the preamble to be output beginning at a predetermined time prior to commencing the outputting of the data is the selective one (e.g., determining a suitable read preamble length considering variation of start timing for data transmission. if length is too long... or if length is unnecessarily long, para 0040, Figs. 6 and 9; setting read preamble length from 1 clock 1 period to 5 periods, para 0060, Fig. 9).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices with detecting a read preamble signal with suitable timing (para 0010, 0013).

3. Claims 50, 57, 65, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Jacob (US 20060248261, published Nov. 2 2006)

Claim 65. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Schaefer, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claim 71. Coteus, Best and Koshizuka do not expressly disclose, but Jacob discloses, wherein the memory controller is operable to cause the transmitter circuitry to transmit each read command together with information indicating that a sense amplifier of the addressed one the

ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

Claims 50, 57. Coteus, Best, and Koshizuka do not expressly disclose, but Jacob discloses, transmitting the read command together with information indicating that a sense amplifier of the addressed one the ranks should be automatically precharged following retrieval of data (e.g., after tRAS, DRAM bank could be precharged, para 0019).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, and Koshizuka, with Jacob, providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

4. Claims 48, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Korger (US 6600681, issued Jul 2003)

Claim 48, 55. Coteus, Best, Koshizuka and Solomon do not expressly disclose but Korger discloses memory controller is to sample data output ... duration of preamble (e.g., the middle of the preamble phase is calculated after approximated beginning of the preamble phase, and delay setting is used to produce the sample value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase, col 8, lines 50-67, Fig. 6).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Koshizuka, and Solomon with Korger, providing the benefit of calibrating a signal used for

masking a strobe signal used for masking data strobe signal received from memory device with read data, and sampling using different time delays (col 2, lines 10-17).

5. Claims 52, 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus in view of Best, Koshizuka and Solomon, and further in view of Kim (US 20110055671, published Mar. 3, 2011)

Claim 52 and 60, Coteus, Best, Koshizuka and Solomon do not expressly disclose, but Kim discloses wherein the receiving the preamble includes receiving the preamble on first resources and sampling data from second resources (e.g., Fig. 13 shows memory device sending data on one line and parity error on a separate line, where parity error includes EDC, 0089).

It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, Best, Koshizuka and Solomon with Kim, providing the benefit of an improved solution to maximize computer performance and density by improving memory device utilization and reduce space and power (see Kim, para 0003).

(10) <u>Response to Argument</u>

A. The rejection of claims 1, 3-5, 11, 14-15, 47, 29, 51, 56, 58-59,61-62,64,66,68-70 and 72-72 over Coteus (USPB 20100220536), Best (USPB 20100091537) and Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586)

Generally, Applicant argues that the cited references do not disclose the limitations recited in Claim 1 (pages 9-14). The Office disagrees.

The primary reference Coteus is relied upon to disclose claimed transmitting a read command and receiving a preamble (e.g., Coteus discloses numerous read commands 402, where first read command ("Read A") is directed to a memory rank A, and another read command is directed toward rank B (0066, Fig. 4) and Fig. 5 shows a timing diagram showing contention when data is read from two different ranks to maintain a synchronization (0067)). During a read operation, a memory device in a selected rank (A or B0 transmits data via controller (0063), including a data receiver for receiving "read" data and clock to compensate as delays (0064). Fig. 4 shows a timing diagram describing read burst from two ranks (0066). A first read command is directed to memory rank A and a next read command is directed to memory rank B, thus having back-to-back data transfer from two ranks of memory with minimal overlapping of two ranks being read.

Second reference Best is relied upon to disclose claimed sampling data output from memory device (e.g., sampling signals supplied to data receiver to sample the incoming read data chunks and receive read data word output in response to memory read command, 0064). Best discloses delaying between receipt of memory read commands, and asserting a signal to enable demand sequencer to issue a sequence of demand signals. A sequence of sampling signals are time delayed between read chunks (0064). Best is relevant to Coteus because Best discloses using a preamble to indicate edges used for transmission operations within the storage die (0066). Best also relates to timing signals and memory access commands (0038, Fig. 1).

For the independent claims 1, 14, 61 and 69, the thrust of Applicant's arguments relate to Koshizuka and Solomon.

1) Applicant argues (on pages 14-17) that cited references do not disclose the limitation of, *with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data.*

The Office disagrees. Koshizuka is relied upon to render this limit as obvious, in combination with Coteus and Best. Specifically, Koshizuka discloses detecting a read preamble with suitable timing to receive read data (0013). A read preamble register that specifies length of the read preamble outputted prior to output of read data (0018, Fig. 9), compared to claimed limitation of information which specifies a duration of a preamble that is output prior to commencing outputting data, according to the broadest reasonable interpretation of claimed duration (disclosed length is equivalent to claimed duration because both indicate how long the preamble will be). Koshizuka discloses a waiting a time based on read preamble length, and reading date (sic) subsequent to the read preamble signal (0019). The device includes a preamble length that determines length of a preamble signal to be outputted prior to starting transmission of data (0020), this provides the benefit of reading read data transmitted easily without occurrence of missing data (0022).

Further, Koshizuka discloses memory device with a read command, waiting a predetermined time based on the read preamble length, and detecting the read preamble signal and read date subsequent to the read preamble signal (0019). The controlled device includes a preamble length register that determines length of a preamble signal to be outputted to the transmission clock line prior to the controlled device starting transmission of data to the controller. The controller sets the preamble length register of the controlled device beforehand (0020). Fig. 9 discloses setting of read preamble length register where preamble length is selected (0060). The length of the read preamble signal is lengthened (0064).

Analogous to Coteus and Best, Koshizuka relates to a need in the art addressing the difficulty of detecting a read preamble signal with suitable timing to receive head data of read data (0013). Fig. 3 shows a timing diagram in which output of read data is started (0014). In order to correctly read the read data, a detection operation of read preamble is entered (0016).

2) Applicant argues (on pages 14-17) that the cited references do not disclose the limitation of *controlling multiple ranks, and transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations*.

First, Applicant admits that Solomon discloses rank switching and read commands (page 16, Brief).

Solomon is relied upon to render these limitations as obvious, in combination with Coteus, Best and Koshizuka. Solomon discloses controlling multiple ranks (e.g., number of ranks 32, para 0052, controller 20).

Solomon further disclose selectively switching between two ranks of memory devices 30 (0055) for successive read command (Fig 6B). Data bursts with pre-amble time interval, and two consecutive read bursts from different memory devices than the first read command (interpreted as equivalent to claimed rank switch)(0061). Memory boundaries between ranks of memory module prior to issue read commands where a wait time is inserted to avoid collisions between back-to-back adjacent read commands which cross memory device boundaries 0062). Solomon's different memory devices are interpreted as disclosing claimed rank switch because of successive read accesses from different memory devices.

This disclosures renders obvious to have a preamble duration in connection with a rank switch, based at least on the disclosure of Koshizuka and Solomon, in combination with Coteus' disclosure of a memory device operation in memory controller where data can be read from ranks of memory with data transfer timing controlled by the receiving device (0057) . One of ordinary skill in the art would have been motivated to modify Coteus with Koshizuka's disclosure of lengthening read preamble length, and with Solomon's disclosure of selectively switching between two ranks of memory devices with pre-amble time intervals in between ranks switching, thus avoiding collisions between two consecutive read bursts between different memory devices.

Applicants invention relates to protocol for high speed signaling between a memory device and a memory controller. Similarly, the cited references are direct to the same benefit,

therefore, motivated to combine. Koshizuka discloses controller for optimally setting the read preamble length, that can perform data transmission at high speed even if read data output timing varies. Solomon discloses utilizing multiple ranks of memory to run faster with improved signal integrity (0056). The combination of these references renders claims 1, 14, 61 and 69 as obvious.

For claims 3 and 15, Applicant argues that the cited references do not disclose sampling the data based on both the sampling clock and preamble. The Office disagrees.

Best discloses claimed sampling in dependent on preamble (sampling signal on incoming read in response to read command, 0064) and further and sampling clock (e.g., internal clock signal used to sample, 0038, Fig. 1). A sequence of sampling signals are time delayed between read chunks (0064). Best is relevant to Coteus because Best discloses using a preamble to indicate edges used for transmission operations within the storage die (0066). Best also relates to timing signals and memory access commands (0038, Fig. 1).

For claim 4, Applicant argues that the cited reference does not disclose using an error detection and correction (EDC) signal to update phase of sampling of the data after receiving the preamble. The Office disagrees.

Coteus discloses this limitation (e.g., permitting error detection information to be transferred in addition to the data, 0059; preamble time is varied based on factors, including slowing down transfer rate, 0087, Fig. 20; first data byte is transferred during preamble time, which reduces read latency because data can be sent prior to preamble completion, 0092).

For claims 5 and 11, Applicant argues that the cited references do not disclose a read command includes information that specifies length of preamble; wherein the information identifies a length for a predetermined time parameter associated with the parameter. The Office disagrees.

Koshizuka renders these limitations as obvious (e.g., a read preamble register that specifies a length of a read preamble to be output prior to output of the read data … read

preamble signal of the length specified by the read preamble register prior to output of the read data, para 0018).

For claims 47 and 54, Applicant argues that the cited references do not disclose wherein the information is transmitted in a manner to cause the memory device to utilize a longer duration in connection with the rank switch, relative to no rank switch. The Office disagrees.

Coteus discloses that delay time of passively controlled delay line is shorter than that of a conventional delay line (para 0058). The memory controller 602 includes DLL, PLL or other such clocking circuitry to monitor drift (e.g. variations in the time in which data is received from memory rank A and memory rank B on data bus 608) and to adjust the timing of the data clocks 606 to each memory device rank such that data can be accurately captured by the memory controller and data contention does not occur on data bus 608, para 0068).

For Claims 49 and 56, Applicant argues that the cited references not disclose toggling pattern as a calibration preamble. The Office disagrees.

Koshizuk discloses read data is outputted with a signal toggle until read data output of a prescribed burst length is complete (0059, Fig. 8). It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in memory controller as disclosed by Coteus, and Best, with Koshizuka, providing the benefit of reduction in power consumption in semiconductor memory devices to detect a read preamble signal with suitable timing to receive head data of read data without error (see Koshizuka, para 0013).

For Claims 51 and 59, Applicant argues that the cited references not disclose transmitting a digital bit to the memory device which specifies that the memory device should utilize the specific duration prior to commencing outputting of data. The Office disagrees.

Koshizuka discloses that upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8.

For claim 61, in addition to claim 14, Applicant argues that the cited references do not disclose DRAM controller that formats and transmits the command….and that duration is selectively used. The Office disagrees.

First, claim 61 does not recite formatting and does not recite preamble duration that should be selectively used (claim 61 recites "specific" duration which is not same as argues "selective"). In any case, Koshizuka is relied upon to disclose that the pre-amble time of the second read command is skipped when there is a back-to-back adjacent read as two consecutive bursts of data from the same memory device, para 0060; disclosed burst from same memory device are interpreted as claimed no rank switch. Claims 62-68 are argued based on dependency from claim 61, thus are treated accordingly, herein.

For Claim 63, Applicant argues that the cited references not disclose wherein the receiver circuitry is to sample the data from each rank in a manner dependent on rank-specific phase information, the rank-specific phase information for each rank being derived by the memory controller from the preamble from the respective rank. Coteus discloses a controller that includes phase lock loop (PLL) 216 to monitor drifts (variations in time in which data is received from rank A and rank B, and to adjust timing of data clocks to each rank (0064, Fig. 2). To minimize data contention between data read from each rank, the controller adjusts the amount of delay (0069).

For Claim 64, Applicant argues that the cited references not disclose wherein the DRAM memory controller is further adapted to store phase information specific to each rank for sampling of read data from the respective rank. Best discloses sample command signals to generate strobe signals output via data path in conjunction with read data to establish read-data sampling within memory controller… including phase adjustment to enable desired phase offsets between sampling times and transitions in incoming data signals (para 0038).

Applicant argues that the cited references not disclose wherein the memory controller is adapted to update the stored phase information for each rank in dependence on the respective one of the preambles. Koshizuka discloses controller sets preamble length beforehand and then determines time to start detection of clock to start transmission in consideration of phase delay outputted by controlled device (para 0020).

For Claim 66, Applicant argues that the cited references not disclose wherein the information for each read command comprises a digital bit that indicates that the respective rank memory should output the preamble of the duration prior to commencing outputting of data. Koshizuka discloses upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete (see para 0059, Fig. 8).

Applicant argues for Claim 69 as similar to 66 and 61, and additionally argues that Koshizuka fails to disclose memory controller that should transmit a bit to a memory device. The Office disagrees. Koshizuka discloses a digital bit of information which specifies according to its state that an addressed one of the ranks should be outputted of a duration of a preamble prior to outputting of data (e.g., upon detecting of a read flag, counting internal clock until read preamble signal output timing prior to read data output start timing decided in advance is reached .. until read data output of a prescribed burst length is complete, see para 0059, Fig. 8; disclosed flag is interpreted as disclosing claimed digital bit).

Claims 70-71 are argued based on dependency on claim 69 (page 21).

B. The rejection of claims 50, 57, 65 and 71 over Coteus (USPB 20100220536), Best (USPB 20100091537) and Koshizuka (USPB 20100182855), Solomon (USPB 20060262586) and further in view of Jacob (USPB 20060248261)

First, for claims 50, 57, 65 and 71, Applicant's arguments are based on incorporation of arguments from claims 1, 14, 61 and 69 (addressed above). Specifically, Applicant argues that Jacob does not disclose preamble insertion in event of rank switch. These limitations are addressed in the arguments above relating to Coteus, Best and Koshizuka.

Further, for claims 50, 57, 65 and 71, Applicant argues that the cited references, specifically Jacob, don't show that ranks should be automatically charged following retrieval of data. Applicant argues that Jacob does not disclose precharge mechanism of any type. The Office disagrees.

Jacob renders this limitations as obvious (e.g., after tRAS, DRAM bank could be precharged, para 0019), providing the benefit of a high performance memory to obtain optimal bandwidth with low request access latencies (see Jacob, para 0005, 0007).

C. The rejection of claims 48 and 55 over Coteus (USPB 20100220536), Best (USPB 20100091537) and Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586) and further in view of Korger (USPT 6600681)

First, for claims 48 and 55, Applicant's arguments are based on incorporation of arguments from claims 1, 14, 61 and 69 (addressed above).

Further, for Claim 48, 55, Applicant argues that the cited references not disclose memory controller is to sample data output from the memory in a manner dependent on rank-specific phase information derived using the duration of the preamble.

Korger discloses, the middle of the preamble phase is calculated after approximated beginning of the preamble phase, and delay setting is used to produce the sample value corresponding to the delay setting that is programmed into delay line in the middle of the preamble phase (col 8, lines 50-67, Fig. 6), providing the benefit of calibrating a signal used for masking a strobe signal used for masking data strobe signal received from memory device with read data, and sampling using different time delays (col 2, lines 10-17).

D. The rejection of claims 52 and 60 over Coteus (USPB 20100220536), Best (USPB 20100091537) and Koshizuka (USPB 20100182855) and Solomon (USPB 20060262586), and further in view of Kim (USPB 20110055671)

First, for claims 52 and 60, Applicant's arguments are based on incorporation of arguments from claims 1, 14, 61 and 69 (addressed above).

Claim 52 and 60, Applicant argues that the cited references not disclose wherein the receiving the preamble includes receiving the preamble on first resources and sampling data from second resources. This is interpreted as receiving signal resources from different sources. Accordingly, Kim suggests this limitation. Specifically, Kim discloses in Fig. 13 that memory device is sending data on one line and parity error on a separate line, where parity error includes EDC (0089), providing the benefit of an improved solution to maximize computer performance and density by improving memory device utilization and reduce space and power (see Kim, para 0003).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Requirement to pay appeal forwarding fee. In order to avoid dismissal of the instant appeal in any application or ex parte reexamination proceeding, 37 CFR 41.45 requires payment of an appeal forwarding fee within the time permitted by 37 CFR 41.45(a), unless appellant had timely paid the fee for filing a brief required by 37 CFR 41.20(b) in effect on March 18, 2013.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent App. Serial No.:	*13/105798*	Filing Date:	*05/11/2011*
Confirmation:	*3982*	Publication No.:	*20120023363*
First Named Inventor:	*Ian Shaeffer*	GAU:	*2185*
Title:	*Protocol Including a Command-Specified Timing Reference Signal*	Examiner:	*SAIN, Guatam*

REQUEST TO FORWARWARD APPEAL TO BOARD OF PATENT APPEALS

Applicant herewith submits the appeals forwarding fee and requests forwarding of the appeal to the Board of Patent Appeals.

Applicant is not submitting a reply brief, as there are no new grounds of rejection stated by the Examiner's Answer, and Applicant's Appeals Brief adequately addresses the Examiner's arguments.

As stated more fully in the Appeals Brief, the cited art, alone or in combination does not suggest structure capable of addressing the problem faced by Applicant or the solution claimed by Applicant, to wit, transmitting information which specifies a duration of a preamble which is to be output prior to commencing outputting of data *together with* a read command. Koshizuka's register "configuration" process performed at initialization up would not be usable to eliminate time bubbles in between rank switches as it would require entry into a configuration mode and entail register reprogramming in between rank-switch read commands (i.e., the intent is that these follow each other as closely as possible, not that they be separated by register programming commands or other operations). There is nothing in the cited art which speaks to a rank switch solution where a read command is transmitted with information that specifies a duration of a preamble which is to be output prior to commencing outputting of data, as claimed.

Respectfully Submitted,
Attorney for Applicants

/Marc P. Schuyler/
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Samsung Electronics Co., Ltd.
Ex. 1050, p. 365

Electronic Patent Application Fee Transmittal

Application Number:	13105798
Filing Date:	11-May-2011
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2012043 / RA764.P.US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Appeal Forwarding Fee	1413	1	2000	2000
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2000**

Electronic Acknowledgement Receipt

EFS ID:	23907203
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	27-OCT-2015
Filing Date:	11-MAY-2011
Time Stamp:	17:07:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2000
RAM confirmation Number	3902
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reply Brief Filed	0000-RA764PUS-MPS-AppealForward-2015-10-27-MPS.pdf	48713 e59a333c33754d91aed58c8ce0e21f2a1f727a11	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30420 7d214ebf9801d15fcaf9c607561306b3cd543255	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	79133		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 11/03/2015

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EXAMINER
SAIN, GAUTAM

ART UNIT	PAPER NUMBER
2135	

MAIL DATE	DELIVERY MODE
11/03/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

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MARC P. SCHUYLER / RAMBUS
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SARATOGA, CA 95070

Appeal No: 2016-000846
Application: 13/105,798
Appellant: Ian Shaeffer et al.

Patent Trial and Appeal Board Docketing Notice

Application 13/105,798 was received from the Technology Center at the Board on November 02, 2015 and has been assigned Appeal No: 2016-000846.

In all future communications regarding this appeal, please include both the application number and the appeal number.

The mailing address for the Board is:

PATENT TRIAL and APPEAL BOARD
UNITED STATES PATENT AND TRADEMARK OFFICE
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Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number listed above.

By order of the Patent Trial and Appeal Board.

AL

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

78408 7590 01/18/2017

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MAIL DATE	DELIVERY MODE
01/18/2017	PAPER

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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte IAN SHAEFFER and THOMAS J. GIOVANNINI

Appeal 2016-000846
Application 13/105,798[1]
Technology Center 2100

Before ERIC S. FRAHM, JAMES W. DEJMEK, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

DEJMEK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 1, 3–5, 11, 14, 15, 47–52, and 54–73. Claims 2, 6–10, 12, 13, 16–46, and 53 have been canceled. Br. 26–29. We have jurisdiction over the remaining pending claims under 35 U.S.C. § 6(b).

We reverse.

---

[1] Appellants identify Rambus Inc. as the real party in interest. Br. 1.

STATEMENT OF THE CASE

Introduction

Appellants' claimed invention is directed to "high speed signaling between a memory device and a memory controller." Spec. ¶ 2. According to the Specification, idle power may be an issue in computer systems containing numerous ranks of memory. Spec. ¶ 11. This is because at any given time only one memory rank may be accessed while the other memory ranks are idle. Spec. ¶ 11. The Specification states "power can be saved by moving timing control components, such as phase-locked loop (PLL) or delay-locked loop (DLL), from the ranks to the memory controller (which typically controls multiple ranks)." Spec. ¶ 11. Further, according to the Specification, using common timing reference/data resources for multiple memory ranks may result in supply voltage and temperature drift, causing a delay of the circuitry in individual ranks. Spec. ¶ 12. In a disclosed embodiment, a timing reference signal (TRS) is used as a calibration preamble, which is provided by the memory device on demand from the memory controller prior to outputting data. Spec. ¶¶ 13–15.

Claim 1 is illustrative of the subject matter on appeal and is reproduced below with the disputed limitations emphasized in *italics*:

> 1. A method of operation in a memory controller, the method comprising:
>
> transmitting a read command which specifies that a memory device output data;
>
> *with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data*;
>
> receiving the preamble; and

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sampling the data output from the memory device in dependence on the preamble output from the memory device;

wherein

the memory controller is to control multiple ranks of memory, and

the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations.

The Examiner's Rejections

1. Claims 1, 3–5, 11, 14, 15, 47, 49, 51, 54, 56, 58, 59, 61–64, 66–70, 72, and 73 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus et al. (US 2010/0220536 A1; Sept. 2, 2010) ("Coteus"); Best et al. (US 2010/0091537 A1; Apr. 15, 2010) ("Best"); Koshizuka (US 2010/0182855 A1; July 22, 2010); and Solomon et al. (US 2006/0262586 A1; Nov. 23, 2006) ("Solomon"). Final Act. 4–12.

2. Claims 50, 57, 65, and 71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus, Best, Koshizuka, Solomon, and Jacob et al. (US 2006/0248261 A1; Nov. 2, 2006) ("Jacob"). Final Act. 12–13.

3. Claims 48 and 55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus, Best, Koshizuka, Solomon, and Korger et al. (US 6,600,681 B1; July 29, 2003) ("Korger"). Final Act. 13.

4. Claims 52 and 60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus, Best, Koshizuka, Solomon, and Kim et al. (US 2011/0055671 A1; Mar. 3, 2011) ("Kim"). Final Act. 14.

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Issue on Appeal[2]

Did the Examiner err in relying on the proposed combination of, *inter alia*, Coteus and Best in rejecting the claims on appeal?

ANALYSIS[3]

Appellants dispute the Examiner's reasoning that an ordinarily-skilled artisan would have been motivated to modify the teachings of Coteus with those of Best to "provid[e] the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power." Br. 12 (citing Final Act. 5). For the reasons discussed *infra*, we consider Appellants' argument persuasive of Examiner error.

Coteus is generally directed to reducing the power at a memory device by removing all or a portion of the delay-locked loop (DLL) circuitry. Coteus ¶ 57. Data clocking circuitry is moved to the memory controller or data receiving device. Coteus ¶ 57. Additionally, Coteus discloses embodiments designed to reduce the amount of "dead time" before data can be transferred from a memory device. Coteus ¶ 59. Coteus describes the "dead time," which Coteus also refers to as a "preamble" time, as the period of time "where the data strobe signal(s) (which are used by the receiving device to capture the data being received) begin to switch but data cannot be transferred to a recipient until the data strobe signal(s) achieve a stable

[2] We only address this issue, which is dispositive. We do not address additional issues raised by Appellants' arguments.

[3] Throughout this Decision we have considered the Appeal Brief, filed April 24, 2015 ("Br."); the Examiner's Answer, mailed on October 7, 2015 ("Ans."); and the Final Office Action ("Final Act."), mailed on October 1, 2014, from which this Appeal is taken.

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switching condition." Coteus ¶ 59. Coteus discloses instead of waiting to begin the transfer of data until after the "dead time" (i.e., the "preamble"), data transfer occurs during the "dead time," albeit at a slower rate. Coteus ¶ 59.

Best is generally directed to a "memory device having storage and control functions split between separate integrated circuit dice within a multi-die integrated circuit package." Best ¶ 36. According to Best, in order to achieve a reduction in power consumption along with high production yields, high-speed circuitry that forms the control and signaling interface of individual memory devices is moved to a separate interface die. Best ¶ 37. Best discloses an embodiment wherein timing circuitry such as a phase-locked loop (PLL) or delay-locked loop (DLL) is used to generate an internal clock signal from a received reference clock. Best ¶ 38. "[T]he internal clock signal is used to sample command signals conveyed via the command path **108**, and to generate strobe signals that are output via data path **110** in conjunction with read data, thereby providing a source-synchronous timing reference for establishing a read-data sampling time within the external memory controller." Best ¶ 38.

The Examiner finds, *inter alia*, Coteus teaches transmitter circuitry to transmit a read command and receiver circuitry to receive the preamble from a memory device, as recited in claim 1 (and similarly recited in independent claims 14, 61, and 69). Final Act. 4 (citing Coteus ¶¶ 57, 59, 64, and 66). The Examiner also finds Best teaches sampling data from the memory device in dependence on the preamble. Final Act. 5 (citing Best ¶ 64). The Examiner states: "It would've been obvious to one of ordinary skill in the art at the time of the invention to modify the memory device operation in

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memory controller as disclosed by Coteus, with Best, providing the benefit of scaling bandwidth and storage capacity for improving signaling rate and saving power." Final Act. 5 (citing Best ¶¶ 2, 36). The Examiner further explains "Best is *relevant to* Coteus because Best discloses using a preamble to indicate edges used for transmission operations within the storage die." Ans. 21 (citing Best ¶ 66) (emphasis added).

The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. The key to supporting any prima facie conclusion of obviousness under 35 U.S.C. § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007), noted that the analysis supporting a rejection under 35 U.S.C. § 103 should be made explicit. Our reviewing court has stated that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006), *cited with approval in KSR*, 550 U.S. at 418.

Here, we find the Examiner has not provided some articulated reasoning with rational underpinning to support the proposed combination of Coteus and Best. Best only mentions the use of a preamble (optionally) once:

> The demand signal may also be parked at midpoint or other level between the logic low and high levels and, if desired or necessary, a preamble and/or postamble protocol established to indicate transmit-enable edges (i.e., edges that are used to enable latching and/or transmission operations within the storage die).

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Best ¶ 66. As discussed, the "preamble" (i.e., "dead time") of Coteus is used to transmit the read data at a slower rate until the data strobe signal(s) achieve a stable switching condition. The Examiner has not sufficiently explained *what* teachings of Coteus are being modified by which specific teachings of Best, or *how* a person of ordinary skill in the art would make such (unspecified) modifications.

For the reasons discussed *supra*, and on the record before us, we do not sustain the Examiner's rejection of claim 1. For similar reasons, we also do not sustain the Examiner's rejection of independent claims 14, 61, and 69, which recite similar limitations. Additionally, we do not sustain the Examiner's rejections of claims 3–5, 11, 15, 47–52, 54–60, 62–68, and 70–73, which depend therefrom.

DECISION

We reverse the Examiner's decision to reject claims 1, 3–5, 11, 14, 15, 47–52, and 54–73.

REVERSED

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NOTICE OF ALLOWANCE AND FEE(S) DUE

78408 7590 02/24/2017

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER
SAIN, GAUTAM

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 02/24/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

TITLE OF INVENTION: PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/24/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/11/2011	Ian Shaeffer	2012043 / RA764.P.US	3982

TITLE OF INVENTION: PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/24/2017

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SAIN, GAUTAM	2135	711-167000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
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- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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78408 7590 02/24/2017

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P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER	
SAIN, GAUTAM	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 02/24/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/105,798	Applicant(s) SHAEFFER ET AL.	
	Examiner GAUTAM SAIN	Art Unit 2135	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/24/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,3-5,11,14,15,47-52 and 54-73*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20170209* .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/TUAN THAI/
Primary Examiner, Art Unit 2135

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DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Claims 1,3-5,11,14,15,47-52,54-73 are allowed.

3. Appeal Decision on Appeal was mailed on 1/18/2017.

4. Note: In the listing of claims, Claim 54 is pending as Previously Presented. Applicant's confirmed typographical error indicating claims "53-54. (Canceled)" Claim 53 is canceled, not claim 54.

5. The following is a statement of reasons for the indication of allowable subject matter: In Claim 1, the prior art does not teach

A method of operation in a memory controller, the method comprising: with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;

wherein the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations, in combination with the other limitations in the claim..

Claims 3, 4, 5, 11, 47-52 are allowable based on dependency from claim 1.

Claim 14, the prior art does not teach a memory controller, comprising:

The read commend being transmitted together with information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data, where in the memory controller is to control multiple ranks of memory and is to transmit the read command to the memory device in a manner to specify that the memory is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations, in combination with the other limitations in the claim.

Claims 15, 54-60 and 73 are allowable based on dependency from claim 14.

In claim 61, the prior art does not teach

A dynamic random access memory DRAM controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each read command together with information which specifies a duration of a preamble that the respective rank is to output prior to commencing the outputting of data; and

wherein the transmitter circuitry is to transmit the information for each read command in a manner to specify that an addressed one of the ranks is to output the preamble of the duration prior to outputting of the respective data in connection with a rank switch relative to a prior memory command, and in a manner to specify that the addressed one of the ranks is not to output

of the preamble of the duration if there is no rank switch, in combination with the other limitations in the claim.

Claims 62-68 are allowable based on dependency from claim 61.

In claim 69, the prior art does not teach

A dynamic random access memory (DRAM) controller to transmit read commands to respective ranks of DRAM memory, each rank of DRAM memory comprising at least one DRAM memory device, the DRAM controller comprising:

transmitter circuitry to transmit each of the read commands according to its state that an addressed one of the ranks of DRAM memory should output of a duration of a preamble prior to outputting of data; and

wherein the transmitter circuitry is to transmit the digital bit for each read command in a manner that specifies use of the duration of the preamble in event of a rank switch relative to a previous memory command, , in combination with the other limitations in the claim.

Claims 70-72 are allowable based on dependency from claim 69.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GAUTAM SAIN whose telephone number is (571)270-3555. The examiner can normally be reached on Monday - Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GAUTAM SAIN
Examiner
Art Unit 2135

/GS/

/TUAN THAI/
Primary Examiner, Art Unit 2135

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	13/105,798	SHAEFFER ET AL.	
	Examiner	Art Unit	
	GAUTAM SAIN	2135	

All participants (applicant, applicant's representative, PTO personnel):

(1) *GAUTAM SAIN*. (3)_____.

(2) *Marc P. Schuyler, Rep for Applicant*. (4)_____.

Date of Interview: *09 February 2017*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *53 and 54*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant confirmed that claim 54 is pending and not cancelled (the listing of claims filed on 6/24/14 erroneously show claim 54 as cancelled and Previously Presented). Claim 53 was cancelled (not claim 54 - typographical error) .

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/TUAN THAI/ Primary Examiner, Art Unit 2135	

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2135

CPC						
Symbol					**Type**	**Version**
G06F		13	/	1689	F	2013-01-01
G06F		12	/	00	I	2013-01-01
G11C		7	/	10	I	2013-01-01
G11C		7	/	1066	I	2013-01-01
G11C		7	/	1093	I	2013-01-01
G11C		7	/	222	I	2013-01-01
G11C		2207	/	2254	A	2013-01-01
			/			
			/			
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			/			
			/			

CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

/GAUTAM SAIN/ Examiner.Art Unit 2135 (Assistant Examiner)	02/09/2017 (Date)	**Total Claims Allowed:** 33	
/TUAN THAI/ Primary Examiner.Art Unit 2135 (Primary Examiner)	02/21/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2135

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
711	167	G 0 6 F 13 / 16 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
365	193	51	189.07		

/GAUTAM SAIN/ Examiner.Art Unit 2135	02/09/2017	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	33	
/TUAN THAI/ Primary Examiner.Art Unit 2135	02/21/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2135

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17		33	8	49	26	65						
	2		18		34	9	50	27	66						
2	3		19		35	10	51	28	67						
3	4		20		36	11	52	29	68						
4	5		21		37		53	30	69						
	6		22		38	14	54	31	70						
	7		23		39	15	55	32	71						
	8		24		40	16	56	33	72						
	9		25		41	17	57	21	73						
	10		26		42	18	58								
5	11		27		43	19	59								
	12		28		44	20	60								
	13		29		45	22	61								
12	14		30		46	23	62								
13	15		31	6	47	24	63								
	16		32	7	48	25	64								

/GAUTAM SAIN/ Examiner.Art Unit 2135 (Assistant Examiner)	02/09/2017 (Date)	**Total Claims Allowed:** 33	
/TUAN THAI/ Primary Examiner.Art Unit 2135 (Primary Examiner)	02/21/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2185

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 12/00 (limited)	3/28/2014	gs

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	193	3/28/2014	gs

SEARCH NOTES		
Search Notes	Date	Examiner
see attached EAST search history	5/31/2013	gs
see attached EAST search history	11/27/2013	gs
see attached EAST search history (including limted CPC search)	3/28/2014	gs
see search EAST history from 3/28/2014	9/29/2014	gs
see attached EAST search history (with intereference search)	2/9/2017	gs

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711/G06F	167 / 12/00	2/9/2017	gs

/G.S./ Examiner.Art Unit 2185	

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EAST Search History (Prior Art)

		<This search history is empty>			

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	"sampling the data output from the memory"	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:04
L1	0	"receiving the preamble"	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:04
L7	0	l6 and "receiving the preamble"	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:05
L6	1847	g06f12/00.cpc.	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:05
L5	0	l3 and "receiving the preamble"	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:05
L4	88	l3 and preamble	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:05
L3	3131	711/167.ccls.	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:05
L8	1	13/"Term Removed"	US-PGPUB; USPAT	OR	OFF	2017/02/09 16:28

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014	02/09/2017				
1	1	✓	✓	✓	✓	=				
	2	✓	-	-	-	-				
2	3	✓	✓	✓	✓	=				
3	4	✓	✓	✓	✓	=				
4	5	✓	✓	✓	✓	=				
	6	✓	-	-	-	-				
	7	✓	-	-	-	-				
	8	✓	-	-	-	-				
	9	✓	-	-	-	-				
	10	✓	-	-	-	-				
5	11	✓	✓	✓	✓	=				
	12	✓	-	-	-	-				
	13	✓	-	-	-	-				
12	14	✓	✓	✓	✓	=				
13	15	✓	✓	✓	✓	=				
	16	✓	-	-	-	-				
	17	✓	-	-	-	-				
	18	✓	-	-	-	-				
	19	✓	-	-	-	-				
	20	✓	-	-	-	-				
	21	✓	-	-	-	-				
	22	✓	-	-	-	-				
	23	✓	-	-	-	-				
	24	✓	-	-	-	-				
	25	✓	-	-	-	-				
	26	✓	-	-	-	-				
	27	✓	-	-	-	-				
	28	✓	-	-	-	-				
	29	✓	-	-	-	-				
	30	✓	-	-	-	-				
	31	✓	-	-	-	-				
	32	✓	-	-	-	-				
	33	✓	-	-	-	-				
	34	✓	-	-	-	-				
	35	✓	-	-	-	-				
	36	✓	-	-	-	-				

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	**Art Unit**
	GAUTAM SAIN	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014	02/09/2017				
	37	✓	-	-	-	-				
	38	✓	-	-	-	-				
	39	✓	-	-	-	-				
	40	✓	-	-	-	-				
	41	✓	-	-	-	-				
	42	✓	-	-	-	-				
	43	✓	-	-	-	-				
	44	✓	-	-	-	-				
	45	✓	-	-	-	-				
	46		✓	-	-	-				
6	47		✓	✓	✓	=				
7	48		✓	✓	✓	=				
8	49		✓	✓	✓	=				
9	50		✓	✓	✓	=				
10	51		✓	✓	✓	=				
11	52		✓	✓	✓	=				
	53		✓	-	-	-				
14	54		✓	-	-	=				
15	55		✓	✓	✓	=				
16	56		✓	✓	✓	=				
17	57		✓	✓	✓	=				
18	58		✓	✓	✓	=				
19	59		✓	✓	✓	=				
20	60		✓	✓	✓	=				
22	61		✓	✓	✓	=				
23	62		✓	✓	✓	=				
24	63		✓	✓	✓	=				
25	64		✓	✓	✓	=				
26	65		✓	✓	✓	=				
27	66		✓	✓	✓	=				
28	67		✓	✓	✓	=				
29	68		✓	✓	✓	=				
30	69		✓	✓	✓	=				
31	70		✓	✓	✓	=				
32	71		✓	✓	✓	=				
33	72			✓	✓	=				

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13105798	SHAEFFER ET AL.
	Examiner	Art Unit
	GAUTAM SAIN	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2013	11/27/2013	03/28/2014	09/29/2014	02/09/2017				
21	73			✓	✓	=				

Samsung Electronics Co., Ltd.
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105798	05/11/2011	Ian Shaeffer	2012043 / RA764PUS	3982

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	960	0	0	960	05/15/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Rambus Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Sunnyvale, California (USA)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ■ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☑ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Marc P. Schuyler/ Date 04/26/2017

Typed or printed name Marc P. Schuyler Registration No. 35675

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Samsung Electronics Co., Ltd.
Ex. 1050, p. 398

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13105798
Filing Date:	11-May-2011
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2012043 / RA764.P.US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt

EFS ID:	29037638
Application Number:	13105798
International Application Number:	
Confirmation Number:	3982
Title of Invention:	PROTOCOL INCLUDING A COMMAND-SPECIFIED TIMING REFERENCE SIGNAL
First Named Inventor/Applicant Name:	Ian Shaeffer
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2012043 / RA764.P.US
Receipt Date:	26-APR-2017
Filing Date:	11-MAY-2011
Time Stamp:	16:16:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	042717INTEFSW16173900
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	0000-ptol85b.pdf	72437 7c90b02d1e1acf2796b455e88aadb331d37dec3f	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30484 d94ea0fdd8472a5e1905bd8d34c9c06e17775a51	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	102921		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/105,798	05/30/2017	9665507	2012043 / RA764.P.US	3982

78408 7590 05/10/2017

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 764 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Ian Shaeffer, Los Gatos, CA;
Thomas J. Giovannini, San Jose, CA;

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