UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

_____

IPR2022-01427

Patent 9,318,160

_____

IPR2022-01428

Patent 8,787,060

_____

September 27, 2023

Remote deposition of MICHAEL BROGIOLI, Ph.D. was taken pursuant to notice, beginning at 9:01 a.m. on the above date before Gail Verbano, Registered Diplomate Reporter, Certified Realtime Reporter, Certified Shorthand Reporter, and Notary Public, there being present via videoconferencing:

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I N D E X

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By Attorney Chandler 9

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REPORTER'S NOTE:

QUOTATION MARKS ARE USED FOR CLARITY AND DO NOT NECESSARILY REFLECT A DIRECT QUOTE.

THE VIDEOGRAPHER: Good morning, Counselors. We are now on the record, and the time is 9:01 a.m. on September 27th, 2023.

This begins the video deposition of Dr. Michael Brogioli, taken in the matter of Samsung Electronics Co. Ltd, v. Netlist, Inc., held before the United States Patent and Trademark Office before the Patent Trial and Appeal Board, Case Numbers IPR2022-01427; IPR2022-01428.

My name is Chris Jordan, and I'm your remote videographer today. The court reporter is Gail Verbano.

Will counsel please state your name and whom you represent for the record, please.

ATTORNEY CHANDLER: Good morning. This is Ted Chandler from Baker Botts on behalf of petitioner, Samsung Electronics Co., Limited; and with me is my colleague, Ferenc Pazmandi.

ATTORNEY ZHONG: This is Annita Zhong from Irell & Manella on behalf of Patent Owner, Netlist, Inc.

THE VIDEOGRAPHER: Thank you, Counsel. Will the reporter please swear in the witness.

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WHEREUPON,

MICHAEL BROGIOLI, Ph.D.,

being first duly sworn or affirmed to testify to the truth, the whole truth, and nothing but the truth, was examined and testified as follows:

ATTORNEY CHANDLER: For the court reporter, I still don't see the realtime.

THE COURT REPORTER: I thought you were connected earlier.

ATTORNEY CHANDLER: I'm connected, but I don't see any words that anyone is saying.

ATTORNEY ZHONG: I don't think I see any typings either. The last I see is a term for generic "yada."

ATTORNEY PAZMANDI: Same here.

THE COURT REPORTER: Let me see. Can we go off the record, please?

ATTORNEY ZHONG: Sure.

ATTORNEY CHANDLER: Sure.

THE VIDEOGRAPHER: Off the record. The time is 9:04.

(Recess taken from 9:04 a.m. to 9:11 a.m.)

THE VIDEOGRAPHER: Back on the record. The time is 9:11.

EXAMINATION

BY ATTORNEY CHANDLER:

Q. Good morning. Please state your name for the record.

A. Michael Charles Brogioli.

Q. What do you do for a living, Dr. Brogioli?

A. I work as an engineering consultant and an adjunct professional in electrical and computer engineering.

(Interruption by the court reporter to clarify the record.)

Q. Dr. Brogioli, were you retained by Netlist to provide opinions in this case related to Netlist's '160 and '060 patents?

A. In this IPR matter, that's correct.

(Exhibit Number 1001 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. And the '160 patent has been premarked as Exhibit 1001 and IPR 2022-01427. And it's U.S. Patent Number 9,318,160; correct?

A. That's marked as Exhibit 1001, I think is what you said. I think that's correct.

Q. And the '060 patent is marked as

Exhibit 1001 and IPR2022-1428 and is U.S. Patent Number 8,788,060; correct?

A. That's correct, yes.

Q. And the two patents, the '160 and the '060 patent, they're related to each other and they have the same figures and the same written description; correct?

A. That's my recollection, yes.

Q. Given that this is a remote deposition, meaning that we're not in the same physical room together, there are a few questions I need to ask you, starting with where are you physically located right now during this deposition?

A. I'm in Austin, Texas, in a separate home office that I have.

Q. Is there anyone else in the room with you right now?

A. No, there is not.

Q. And given that I cannot see the room that you're in, will you please let us know if someone enters the room you're in at any time before the deposition ends?

A. Absolutely.

Q. Dr. Brogioli, did you bring anything with you to your deposition today?

A. No physical materials. I did bring a few unmarked or clean, if you will, PDFs of probably a subset of the exhibits you already sent. My declaration and the patents, for example.

Q. And is there anything in front of you on your computer besides the video feed and the exhibits for this case?

A. No.

Q. Given that I cannot see whether you have anything in front of you, will you please let us know if you or anyone else puts anything in front of you at any time before the deposition ends?

A. Yes, I will.

Q. I will take breaks throughout the deposition, but I want to remind you that, under the PTAB procedures, that during those breaks, you should not consult with your counsel about the substance of your testimony.

Do you understand that?

A. Understood, yes.

Q. And during the deposition, I would ask that you do not look things up on the internet or do other things on your computer or your phone

that we cannot see on camera.

Understood?

A. Understood.

Q. And you also understand that you, during the deposition, should not be emailing or texting other people?

A. Understood.

Q. And approximately how many times have you been deposed before?

A. I think it's on the range of maybe 45, maybe a little bit more than that.

Q. Do you have any questions for me about the procedure for today's deposition?

A. I don't think so, no.

Q. What did Netlist ask you to do in this matter?

A. It was generally to review the '060 and '160 patents and address certain opinions that Samsung's expert, Dr. Wolfe, had offered in his -- in his declarations and his depositions.

Q. Did anyone help you with your work in these two IPRs?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I'm saying no, not with the technical work. There may have been minor

things, as usual, assembling the report in terms of footnotes and formatting or things like that, but the technical work and opinions was all mine.

BY ATTORNEY CHANDLER:

Q. What did you do to prepare for today's deposition?

A. I began with reviewing the patent specification and claims of the patents, looking at my declaration. I had a few, I think two perhaps, meetings with counsel over the last four or five days, I think, including the weekend in there.

And then looked at other technical -- some of the prior art references, perhaps some of Dr. Wolfe's opinions that I address in my declaration, generally things of that type.

Q. Approximately how many hours did you prepare for the deposition over the last week?

A. I would say -- I'll answer that in two parts. One, it will be detailed in my invoices. I would ballpark maybe 40 or 50 or more hours. And the reason I say "ballpark" is there's other things that I'm working on right now that -- that are kind of filling the day. So it hasn't just been this preparation. But I would say 40 or 50

hours, if not more.

Q. And I think you said that in preparation for today's deposition, you had two meetings with counsel; is that correct?

A. That's what I recall, yes.

Q. And who attended those meetings?

A. Annita, who, I believe, is here on the Zoom link; and I think another gentleman. I believe his name might have been Jonathan, but I'd have to go back and check for you.

Q. But both of them were from the Irell law firm?

A. That's correct.

Q. Anyone else join the meetings that you had to prepare for today's deposition?

A. Not that I recall, no.

Q. As part of your work for Netlist on these IPRs, did you personally talk to anyone else, such as the inventors or anyone else with experience in the field?

A. No, I didn't.

(Whereupon, Exhibit Number 1053 in both IPRS was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. I marked a new exhibit in both IPRs, Exhibit 1053, which I've put into the chat. It's a redline comparison -- a redline comparison of Exhibit 2023 in the two different IPRs.

Do you have Exhibit 1053 in front of you?

A. I do. I downloaded it a moment ago.

Q. So to be precise, I'll represent to you that Exhibit 1053 is a computer-generated redline comparing your declaration and IPR2022-1427, marked as Exhibit 2023, against your declaration, IPR2022-1428, marked as Exhibit 2023.

Do you understand?

A. I do.

Q. Am I correct that your declaration marked as Exhibit 2023 in IPR2022-1427 is substantively identical to your declaration marked as Exhibit 2023 in IPR2022-1428?

A. That should be the case. As I recall, as we can see on the first page here, the cover page was changed; but if I remember right, the opinions between the two are the same. The content was largely the same.

Q. So as shown in the redline marked as

Exhibit 1053, the only difference between your declaration in the two IPRs is the cover page and the header that provides the case number and the patent number for the IPR; correct?

A. That's my recollection. And that also, as I'm flipping through the redline, Exhibit 1053 you gave me, looks to be the case as well in the redline.

Q. All right. Given that your declaration marked as Exhibit 2023 is substantively the same in both IPRs, I will just refer to your declaration as Exhibit 2023, with the understanding that the questions and answers about your declaration will apply equally to both IPRs; is that fair?

A. That sounds fair.

Q. In Exhibit 2023, can you turn to page 199.

A. Okay.

Q. Page 199 of Exhibit 2023 is your -- part of your CV; correct?

A. That's correct.

Q. Does the CV at the end of your expert declaration marked as Exhibit 2023 list all of your prior expert engagements in which you were

either deposed or testified at trial?

A. That is the intention of this section. There may be -- so I note that the generated date on the bottom is July 20th of 2023. The -- this section of the CV and perhaps others, to a minor degree as well, might be slightly out of date. But I don't think -- I think at the time that this was attached to my declaration, at least in terms of deposition testimony and trials, it would have been up to date.

Q. Before this pair of IPRs, when did you first do any work for Netlist?

A. A few years ago. It should be in my CV here. Perhaps -- let me just find it for you.

It looks like starting in 2016 to, if I recall right, the spring of 2017-ish.

Q. In what matter are you looking at?

A. Sorry. That's on page 205 of Exhibit 2023; and that was a Netlist matter at the International Trade Commission.

Q. That's Investigation Number 337-TA-1023? That's what you're referring to?

A. That's correct.

Q. Besides the Netlist litigation against SK Hynix and the Netlist litigation in this

matter, are there other cases or other work that you've done for Netlist?

A. There are. There was a trial here in Texas, which was earlier this year, relating to, at least in part, the patents we're talking about today that I did work on as well as, if I recall correctly, one or two other IPRs for other patents.

Q. Before you were first engaged by Netlist around 2016 or 2017, did you know the named inventor on the '160 and '060 patents identified as Hyun Lee?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't believe I knew him personally, no.

BY ATTORNEY CHANDLER:

Q. And have you ever met the named inventor, Hyun Lee, on the '160 and '060 patents?

A. I'm not sure. To the extent I had met him, perhaps he may have been present at the trial back in, I think, 2017. But I don't recall -- I don't recall specifically if someone had introduced us or not.

Q. When was the first time you had heard of the named inventor on the '160 and '060

patents, Hyun Lee?

A. I don't recall.

Q. Do you believe that you had heard of the named inventor, Hyun Lee, before you started working for Netlist in 2016 or 2017?

A. I don't remember.

Q. Do you own any Netlist stock or stock options?

A. I do not.

Q. How much are you charging Netlist per hour for your time spent on these two IPRs?

A. As I recall, it's $700 per hour.

Q. Approximately how many hours have you spent working as an expert for Netlist on the '160 and '060 patents?

A. If you're asking in regard to this IPR as well the other what I'll refer to as the district litigation, again, those numbers will be in my invoices. At this point it would be in the hundreds of hours between expert reports, depositions, trial preparation, IPR, things of that nature.

Q. And so if I'm doing the math correctly, would it be fair to say that Netlist has paid you over $200,000 to work on matters related to the

'060 and '160 patents?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I go back to the invoices, but that number might -- that number might seem reasonable, given the work over the past year and a half or however long it's been.

(Exhibit Number 1044 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. I was going to ask you to pull up an exhibit, but maybe it's just easier if I -- for the court reporter if I can put it in the chat. So let me go ahead and do that. It will be Exhibit 1044, which is -- let me know when you've got Exhibit 1044 in front of you.

Exhibit 1044 is Netlist's First Amended Complaint against Samsung in the Eastern District of Texas in Civil Action Number 2:21-CV-463-JRG; correct?

A. That sounds right to me.

Q. As shown in paragraph 3 of Exhibit 1044, Netlist asserted the '060 and '160 patents against Samsung in the Eastern District of Texas; correct?

A. That looks correct, yes.

Q. And you provided expert testimony for Netlist against Samsung in the Eastern District of Texas as part of the case related to Exhibit 1044; correct?

A. That's correct.

Q. Please turn to page 21 of Exhibit 1044. Let me know when you're there.

A. Okay.

Q. In the Eastern District of Texas, you provided expert testimony for Netlist that Samsung's accused HBM products infringed the '060 and '160 patents; correct -- is that correct?

A. That certain of these HBM products infringed, as I recall, some of the claims of the patents. I don't think I addressed all of the claims.

Q. And the accused HBM products that you opined infringe included Samsung's HBM2, HBM2E and newer products; is that fair?

A. That's right. I think I testified on products up to the HBM -- up through the HBM3.

Q. And the jury in the Eastern District of Texas agreed with you that Samsung's accused HBM products infringed the '060 and '160 patents; correct?

Samsung Electronics Co., Ltd.
Ex. 1052, p. 21

A. That's my understanding, yes.
Q. Could you turn back to your declaration marked as Exhibit 2023. Let me know when you have it in front of you.
A. Okay.
Q. When did you start your work for Netlist on these two IPRs?
A. So, again, I -- I would want to go back to the invoices. And they should show it, probably down to the day. If we're in September now, my somewhat vague recollection would be probably early this year, maybe in the spring.
Q. So early 2023?
A. Going from my -- from my recollection. And the reason I -- I'm just a little hazy on my recollection is, with the trial for the '060 patent that we're just talking about, from my memory, there's a lot of technical overlap there. So I don't recall if I was specifically working on IPR or the trial material in April, for example.
But I think probably early part of this year sounds generally right.
Q. Are your expert declarations for the '160 and '060 patents marked as Exhibit 2023 complete, meaning they provide a complete

statement of all the opinions you intend to express in each IPR along with the basis and the reasons for those opinions?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say as of today, yes. As we go through them today, there are probably some minor typo-type things or maybe clarification. But in terms of the opinions, I don't have additional opinions sitting here right now.

BY ATTORNEY CHANDLER:

Q. Are your expert declarations for the '160 and '060 patents marked as Exhibit 2023 accurate, meaning they do not have any mistakes as far as you are aware right now?

A. I would say there are probably one or two minor corrections in them that we'll find a word that is misspelled or perhaps -- things of that nature, as I recall.

Q. Is there anything right now that comes to mind that you would like to point out that should be corrected?

A. Off the top of my head, I don't recall, no.

Q. And to be clear, do you have any

present plans to correct or supplement your expert declarations for the '160 and '060 patents marked as Exhibit 2023?

A. Not as of today, I don't.

Q. Have you carefully read Netlist's '160 and '060 patents marked as Exhibit!1001 in each IPR?

A. Yes, I have.

Q. Do you believe that you understand Netlist's '160 and '060 patents?

A. Yes.

Q. Do you believe you understand the figures of Netlist's '160 and '060 patents?

A. Yes.

Q. Do you believe you understand the claims at the end of the '160 and '060 patents?

A. Yes, I do.

(Exhibit Number 1011 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please pull up Exhibit 1011, which is the same in both IPRs. Let me know when you're there.

A. Okay.

Q. Have you carefully read the Rajan '137

prior art reference marked as Exhibit 1011 in both IPRs?

A. I would say certainly certain sections of it. I don't think I offer opinions on the entire thing, but I've certainly read the reference.

Q. And do you believe you understand the Rajan '137 prior art reference marked as Exhibit 1011 in both IPRs?

A. To the extent I offer opinions about it in my declaration, yes.

(Exhibit Number 1014 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please pull up Exhibit 1014, which is the same in both IPRs, and let me know when you have it in front of you.

A. Okay.

Q. Have you carefully read the Kim prior art reference marked as Exhibit 1014 in both IPRs?

A. Yes, I have.

Q. Do you believe you understand the Kim prior art reference marked as Exhibit 1014 in both IPRs?

A. I do -- again, similar answer: I do to the extent I'm offering opinions about certain portions of it.

(Exhibit Number 1015 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please pull up Exhibit 1015, which is the same in both IPRs, and let me know when you're there.

A. Okay.

Q. Have you carefully read the Rajan prior art reference marked as Exhibit 1015 in both IPRs?

A. I've -- I would say, yes, I've reviewed this reference in this IPR, and I've carefully reviewed it to the extent I'm offering opinions about certain sections of it.

Q. Do you believe you understand the Rajan prior art reference marked as Exhibit 1015 in both IPRs?

A. I do, yes.

(Exhibit Number 1016 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1016, which is

the same in both IPRs, and let me know when you're there.

A. Okay.

Q. Have you carefully read the Riho prior art reference marked as Exhibit 1016 in both IPRs?

A. I've reviewed this reference, yes.

Q. Do you believe you understand the Riho prior art reference marked as Exhibit 1016 in both IPRs?

A. I would say yes. Regarding the portions of it that I offer opinions on, yes.

(Exhibit Number 1017 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1017, which is the same in both IPRs, and let me know when you're there.

A. Okay.

Q. Have you carefully read the Wyman reference marked as Exhibit 1017 in both IPRs?

A. I would say, yes, I've reviewed this reference.

Q. And do you believe you understand the Wyman reference marked as Exhibits 1017 in both

IPRs?

A. I would say I do in the context of the opinions I'm offering in my declarations, yes.

(Exhibit Number 1018 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1018, which is the same in both IPRs, and let me know when you're there.

A. Okay.

Q. Have you carefully read the Riho 2 reference marked as Exhibit 1018 in both IPRs?

A. Yes, I have reviewed the reference.

Q. Do you believe you understand the Riho 2 reference marked as Exhibit 1018 in both IPRs?

A. I do in the context of the opinions that I'm offering in my declaration.

(Exhibit Number 1019 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1019, which is the same in both IPRs, and let me know when you're there.

A. Okay.

Q. Have you carefully read the JEDEC, the JESD79-3C DDR3 SDRAM standard, dated November 2008, marked as Exhibit 1019 in both IPRs?

A. As I recall certain portions of it, yes.

Q. And do you believe you understand the DDR3 standard, dated November 2018, marked as Exhibit 1019 in both IPRs?

A. With the context of the sections of this standard that I discuss in my declarations, yes.

Q. Could you pull back up your expert declaration marked as Exhibit 2023. Let me know when you're there.

A. Okay.

Q. I'd like to ask you some questions about the hypothetical person of ordinary skill in the art, starting with the relevant time frame for such a person. So understood what we're about to talk about?

A. Okay.

Q. To start, please look at paragraph 29 in your expert declaration marked as Exhibit 2023. And let me know when you're there.

A. Okay.

Q. Samsung's expert, Dr. Wolfe, expressed

the opinion that the effective filing date for the '160 and '060 patents was no earlier than November 3rd, 2011.

My question for you is whether you expressed any opinion disagreeing with Dr. Wolfe on this point. I did not see any opinion in your expert declaration disagreeing with Dr. Wolfe on this point; but if you do disagree with him on this point, could you let me know where that is.

A. I don't recall offering an opinion that I necessarily disagreed with his November 3rd, 2011, date.

Q. So your expert declaration, marked as Exhibit 2023, does not express the opinion that the '160 and '060 patents are entitled to an earlier effective filing date of November 3rd, 2010; is that fair?

A. I would say I haven't offered an opinion on that one way or the other. I don't recall it being something I was asked to address in my declaration.

Q. Would it be fair to say that you assumed a date of invention no earlier than November 3rd, 2011, consistent with Dr. Wolfe's assumption?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I think that generally sounds right. If I -- if I were proactively disagreeing with the date, I would have -- I would have added a section on that.

BY ATTORNEY CHANDLER:

Q. Unless stated otherwise today, can you please answer my questions from the perspective of a person of ordinary skill in the art as of November 3, 2011?

A. Yes.

Q. And can you also please answer my questions today in a way that would be consistent with the ordinary and accustomed meaning of words to a person of ordinary skill in the art as of November 3rd, 2011?

A. Okay.

Q. Please turn to paragraph 5 of your expert declaration marked as Exhibit 2023, and let me know when you're there.

A. Okay.

Q. Starting with paragraph 5 of your expert declaration marked as Exhibit 2023, you describe your qualifications and experience relevant to these two IPRs; correct?

A. That's correct.

Q. In paragraph 7, at the bottom of page 6 of Exhibit 2023, you state that, from 1999 to 2003, you worked with "dynamic power management and performance of configurable memory systems, including SRAM-based caches"; correct?

A. Correct.

Q. Could you explain that in a little more detail?

A. Sure. I was looking at the high-speed portion of very close memory in CPU systems at the time and applications that used large amounts of data beyond what would fit into that memory you had and came up with a system as to how you could turn on or -- conceptually turn on or turn off portions of the memory system to save power in what was -- trying to be real time, effectively, to reduce power consumption of the memory system while -- if possible, not negatively impacting performance.

And so it was a mix of hardware design of the memory portion and some CPU stuff, if you will, and modeling and other things around programming languages to give the hardware hints, if you can do it in an automated way and a bunch

of math that wraps around that.

Q. And did you say the goal of that work was to reduce the power consumption?

A. As I recall, that was at least one of the goals or one of the main goals of it.

Q. And what was the motivation for wanting to reduce power consumption of the memory system?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That -- at that time, the idea was that we had a bunch of memory or cache memory on our CPUs or attached to our CPUs, and it was consuming all our power; and if you could use it more intelligently for certain kinds of applications that you could kind of predict the future on, if you will, in terms of what they were going to need from memory or memory access patterns or requirements in the future, you could have this adaptive hardware that kind of ran along in parallel or did things in advance to kind of expand or deflate the size of the memory to maintain performance that was acceptable while saving power, things like that.

BY ATTORNEY CHANDLER:

Q. What is a configurable memory system that you referred to in paragraph 7 of

Exhibit 2023?

A. As I recall in this context, it was -- configurable meant that something could write or -- something could access the hardware on the system or on the chip to power down or -- put in a lower power state parts of the memory and take the bits and bytes that were sitting in there and store them somewhere else so they weren't lost forever. And so as the machine was running along, the cache memory system could be dynamically configured to look different ways at different points of time.

Q. So where would the memory be stored when there was no power? How did that work?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: If I remember 20-some-odd years ago, I think the data stored in -- in a kind of simpler example, if there was data stored in L2 cache or L1 cache and you were going to power down some part of it, in that case, the data was sent to maybe DRAM or somewhere else in the system. There was a bunch of kind of peculiar things that I and we were experimenting with at the time, but ...

///

BY ATTORNEY CHANDLER:

Q. What is SRAM?

A. It's a type of memory that's used to store bits and bytes that's used at certain -- certain design considerations in a computer system.

Q. What does the S in SRAM stand for?

A. Static.

Q. Were SRAM memory devices commercially available in 2003 when you were doing this work?

A. Yes. SRAM was used in a number of different contexts at the time.

Q. And so as part of your work, were you transferring data between SRAM and DRAM and back?

A. I think so. It's been a while since I've read it, but I think that was part of what was going on in that system.

Q. How does the interface for an SRAM memory device compare to the interface for a DRAM memory device? Are they identical?

A. I would say we probably need to get more specific there, and I talk about some of this in my declaration. But there are some differences between SRAMs and DRAMs, for example, the way that they're designed and the commands that they

receive and the signaling that they use to communicate to the outside world.

Q. But in 2003, you and others knew how to interface between both an SRAM memory device and a DRAM memory device as part of the --

ATTORNEY ZHONG: Objection; form.

THE WITNESS: No, that's not what I'm saying. So we're talking about SRAM -- your prior question was about SRAM in a prebuilt computer system I, you know, purchased from Intel or IBM or something like that where the SRAM cache can be flushed out to DRAM using a prebuild system that you've bought, for example.

BY ATTORNEY CHANDLER:

Q. I'm a little confused by your last answer.

Are you saying that there did exist prebuild systems in 2003 that could transfer data from an SRAM cache to a DRAM memory device?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say you could purchase, for example, a -- a computer from Intel, as an example, and that computer would know that if I'm -- if there's data stored in SRAM, cell-based data cache, for example, at certain

points in time I may need to -- or the system may need to, quote, what we call flush the contents of that cache out to the DRAM, and that's part of the silicone that you purchased. Or if there's a miss in the cache, which was SRAM cell-based, data would be loaded from DRAM and stored in that cache for faster access subsequently in time.

I'm not talking about buying separate chips here. We're talking about computer chips purchased from vendors with different types of memory in them or attached to them.

BY ATTORNEY CHANDLER:

Q. So by 2003, there were commercially available products that combined SRAM and memory devices and DRAM memory devices; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say that there were products you could buy -- for example, a commercial PC or server -- that were comprised of different components; and those components, for example, may have had DRAM chips on -- or DRAM memory devices on various PCBs in the system. And then oftentimes you would have separate SRAM cell-based cache storage up very close to the CPU or on that same chip.

BY ATTORNEY CHANDLER:

Q. How are the configurable memory systems, including SRAM-based caches that you worked on from 1999 to 2003, relevant to your qualifications for providing expert testimony in this case?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say as part of my overall experience, that work related to how various SRAM memory operated, at what speeds, at what I/O, access patterns, and things like that. And as I recall, also involved how that -- in the context of those studies related to how DRAM-type technology at the time or prior in time worked and how the team kind of used the two constructively in these systems for better power management and performance maintenance.

BY ATTORNEY CHANDLER:

Q. Are SRAM memory devices relevant to understanding the stacked DRAM memory devices described in the '060 and '160 patents?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say in general, it probably depends on the context of a given question or -- or something of that nature.

BY ATTORNEY CHANDLER:

Q. If you look at the end of paragraph 7 of Exhibit 2023, you state that from 2004 to 2009, you developed a computer architecture design and modeling tool set called Spinach DSP-FPGA; correct?

A. That's correct -- I think you're referring to the fifth line down on the next page. That's correct.

Q. What was Spinach, and how was your work on Spinach relevant to your qualifications providing expert testimony in this case?

A. So Spinach was a -- not a simulator for systems that include types of CPUs and different types of memory technology, but a simulator design tool.

So you could go say, I want, for example, an eight-processor system with four processors of flavor A and four of flavor B and a bunch of memory here and memory there. And this memory is partitioned this way, and maybe this one is super fast. And a whole bunch of different interconnects between the memories, and maybe there's accelerators in there and other things and a lot of components that are similar to or

identical to components that are used in memory like decoding and things like that or the various building blocks. And it would go out and build this giant simulator for you, and then you could do all of these studies on how your new whizbang computer you designed was either fantastically fast or a terrible design and you went back to the drawing board.

And at the end of the day, that whole simulator design tool comes with a bucket of all these different bits and components you can use from full CPUs to 16-bit adders and switches and things. And you can kind of connect them together like tinker toys, if you will, and go build your thing.

So there's a lot of components in there that either relate to memory devices or explicitly modeled performance and other aspects of memory technology.

Q. Could you turn to page 198 of your expert declaration marked as Exhibit 2023 and let me know when you're there.

A. Okay.

Q. In the middle of page 198 of Exhibit 2023, you summarize your work on Spinach

between the years 2004 and 2009; correct?

A. That's correct -- well, yes, and then there's another section going back to 2002 for a different flavor of it. But that's right.

Q. In the middle of that summary, you state, Based -- well, there are two paragraphs there. So you see the -- the paragraph about -- the top paragraph about Spinach under 2004 to 2009?

A. Yes.

Q. You state, in the middle of that paragraph, that between 2004 and 2009, as part of your work on Spinach, you, quote:

"Designed and developed support for SRAM and DRAM style memories, heterogeneous memory systems, heterogeneous clock domains, as well as runtime configurable [sic] Xilinx Virtex II based FPGA computing elements, cache and memory controllers, bus arbiters, and on-chip Internet connect [sic] fabric," end quote.

Did I read that accurately?

A. Yes.

Q. What are heterogeneous memory systems?

A. In this context, I believe -- we're going back about 20 years here. But as I recall, it was the ability to have a system that had everything from things like SRAM cache or perhaps SRAM or other type of memory -- scratchpad memory -- but then you could have perhaps other memory, like DRAM elsewhere in the system or -- or maybe attached to things like hardware accelerators or FPGAs. I think it was generally that -- what fell into that idea.

Q. So if I understand correctly, by 2009, were there heterogeneous memory systems that included both SRAM and DRAM memory devices?

A. In this context, it was giving you a tool set to go explore that kind of thing where you might have a little patch of SRAM attached to your CPU that's a kilobyte or something. But then you might have a different type of memory somewhere else in the system, not -- you know, not directly connected to it or things like that. You have to copy information around perhaps, things like that -- which was available, you know, in -- as I even recall, in the -- some of the machines that were modeled in the 2002 line entry here, where you might have a little bit of SRAM sitting

somewhere and other bigger memory elsewhere in the system.

Q. To what extent was your work on Spinach, between 2002 and 2009 relevant to stacked DRAM memory devices?

A. So I don't -- I don't know that I've contemplated the universe of ways that it's relevant.

But in stacked memory devices, just speaking in a general sense, you might have a control chip that does handling of certain signals and decoding of address bits and things like that, and control commands; and then in things like the memory, you would have various storage elements -- storage -- places where the bits get stored. And so -- then a lot of different touch points in this Spinach tool, there are, I would say, building blocks that you can use to explore that type of thing, like decoding address bits coming in to figure out, for example, if you want to put -- if the data is stored in cache locally or if you need to go elsewhere to find it. So it gives you some building blocks that you can use to explore things like that.

Q. Did Spinach, in the 2004 to 2009 time

frame, permit a person to simulate the control chip that might be used in a stacked DRAM memory device?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't know. I don't recall, from my understanding, people explicitly doing something like that, but other people, you know, took the tool and used it in whatever ways they used it.

All I'm saying is there are -- there are building blocks within the Spinach tool at that time frame that you could use to perform logic and things that might be common to what's done in a control chip or a control die, or other types of memory.

BY ATTORNEY CHANDLER:

Q. Was Spinach in the 2004 to 2009 time frame capable of simulating and debugging the timing issues related to memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It was capable -- it was capable of modeling, measuring, simulating, debugging, if you will, as well, certain aspects of timing in systems -- you could use it to look at things. It didn't give you an answer to

problems. It would just "tell you if it wasn't working" kind of thing. And some of that related to, you know, certain examples of different types of memory, depending on what context you, the user, came up with and wanted to investigate.

BY ATTORNEY CHANDLER:

Q. Did Spinach simulate translating between one memory protocol and another memory protocol? Was that within its capabilities?

A. I don't -- I don't think so, but I don't remember. Perhaps someone else took it and modified it elsewhere, but I don't recall that being a thing that was given to you out of the box.

Q. Could you go back to paragraph 7 of Exhibit 2023. Let me know when you're there.

A. Okay.

Q. Toward the end of paragraph 7 on page 7 of Exhibit 2023, you state that from 2004 to 2009 you developed a "retargetable compiler infrastructure and hardware design exploration toolkit."

Is that correct?

A. I must have missed where you're reading from. It sounds right, but I can't find the

sentence. Where are you?

Q. It's like the fifth from -- sentence from the end of paragraph 7.

A. Oh, yes, I see that.

Q. Could you explain what that work was about in a little bit more detail about the toolkit and what it was used for.

A. So it could be used for a number of things. One of which I designed it for was to take an application and feed it into this tool. And rather than it generate the bits and bytes that might run on your laptop for Zoom, for example, like we're using today, it would look at Zoom and say, okay, if I have the freedom to design the CPU and the nearby memory system -- I'll put quotes around this -- anyway I want within sort of -- within reason of what's possible in terms of computer architecture, it would go off and think about that problem and come back and say, okay, rather than run this application on a X80 -- well, this is just an example -- an X86 CPU at one gigahertz with blah, blah, blah, it would say, perhaps you make the CPU look like these 16 different clusters, and they can each do some kind of logic; and then they each have their own very

local, fast memory associated with them and what that memory size needs to be to make everything run right. And it gave you a bunch of trade-offs in terms of clock speed or how parallel the machine needed to look. And it would also take into consideration when these blocks of, if I remember right, really fast local memory were kind of associated with each tiny, little CPU, how fast could the memory go? And what could you actually achieve in terms of input and output and signaling to the actual compute elements? And did the little CPU need more memory cells than were going to be possible to get I/O at that speed? And if so, maybe we need the tool we need to keep thinking and explore this kind of design space and come back to you with a bunch of different trade-offs for all these variables.

Q. Was that toolkit that you worked on from 2004 to 2009 related to stacked DRAM memory devices?

A. I would say that -- I haven't thought about how it may or may not be related to stacked DRAM memory devices. At the time I don't recall using it to investigate those types of systems explicitly.

Q. And in paragraph 8 of Exhibit 2023, you mentioned that you worked for a company named Vicarious Visions in the late 1990s; correct?

A. That's right.

Q. And then if you turn to page 192 of Exhibit 2023, you provide a little more detail about that work; right? In the year 1999.

A. That's right, yes.

Q. On page 192 of Exhibit 2023 you state your work for Vicarious Visions in 1999 included coding "innovative, highly optimized assembly routines for real-time speech and full-motion video on the console's limited Zilog Z80 processor resources."

Correct?

A. That's correct.

Q. Did that work that you did for Vicarious Visions relate to stacked DRAM memory devices?

A. I would say that it related to memory devices more generally, that -- that bucket of work at that company in two ways.

One is the with regard to the sentence you just read of having a memory system in these little consumer electronics devices, it wasn't

designed to be particularly aggressive in any way, really.

It was designed to be inexpensive; and figuring out how to make things stored in the memories and how they were being brought in and out of the memories, both to the CPU and elsewhere, go just about as fast as -- as electronically possible.

And then in addition to that work, I designed hardware interfaces where, if you are -- if you're a game developer in a PC in 1999 and you're developing on this little handheld console, it was a way to interface your little hardware console to the PC and have all of these memory buffers to swizzle things back and forth effectively for development and optimization and things. And so I built like printed circuit boards that interfaced to either side with local memory on them and things like that.

Q. The Zilog Z80 that you were working on at Vicarious Visions in 1999 had a data bus for communicating with the memory devices that was only 8 bits wide; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: As I recall, that CPU

or -- there was a variant of that CPU in the device, and I -- I generally recall it being 8 bits. And then I think there were other components in the system, like a direct memory access engine that might have been a different bit width. I don't remember anymore. But there was also moving things around the memory system.

BY ATTORNEY CHANDLER:

Q. And what kind of memory were you working with for the Zilog Z80? Was it DRAM or SRAM or something else?

ATTORNEY ZHONG: Objection; form, relevance.

THE WITNESS: In terms of the console, the hardware console itself, portions of it were SRAM. I don't recall what the other portions of it were. And I'm not sure recall -- I don't recall the actual PCB hardware design that I was doing with a huge amount of familiarity, other than there was custom logic and memory and things on it.

BY ATTORNEY CHANDLER:

Q. Could you turn back to paragraph 9 of Exhibit 2023. Let me know when you're there, on page 8.

A. Okay.

Q. If you look at paragraphs 9, 10 and 11 of Exhibit 2023, you discuss work at various places between 2006 and 2011. And my question for you is whether any of that work related to stacked DRAM memory devices.

A. I would say -- I lost my place.

I would say at times in paragraph 10, in my teachings at Rice, without specificity, there were modules that my class was going to around certain types of high-performance computing and things like general-purpose GPUs for nongraphics applications.

And I recall there being content in there around memory and memory designs that were going to be able to, you know, feed these things in the future. I don't recall all of the specificity there. But that -- that may have related to stacked -- some flavor of a stacked memory device.

The other work I don't recall from memory.

Q. In paragraph 12 of Exhibit 2023, you mention that you worked at Texas Instruments and Intel; correct?

A. That's right.

Q. And then if you turn to page 192 of Exhibit 2023, you state that your work at Texas Instruments was in 2005 and your work at Intel was in 2000; correct?

A. That's more or less correct when I was in-house at those companies, but my work overlapped with subsequent years as I recall.

Q. Did your work at Texas Instruments in 2005 or your work at Intel in 2000 relate to stacked DRAM memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't recall my work in those two roles explicitly targeting a form of a stacked DRAM memory device one way or the other. Certainly there were various types of memory technology in the technologies I was working on.

In the case of the Texas Instruments work, there were a number of different types of memory in these machines at different places, but I don't -- to answer the initial question, I don't recall focusing on what you're referring to as a stacked DRAM memory device explicitly.

BY ATTORNEY CHANDLER:

Q. When you were working at Texas

Instruments in 2005, it says you were working on on-chip and off-chip memory controllers; is that right?

A. That's correct, yes.

Q. And what type of memory devices did those on-chip and off-chip memory controllers interface with when you were working at Texas Instruments in 2005?

A. I don't recall the specifics of that system architecture. But I generally recall it having DRAM on the boards for the various components, like DSPs and other processors. And then the on-chip may have been for an on-chip SRAM or something like that in a scratchpad technology. But I'm a little hazy on that system architecture at this point.

Q. But you think you may have been working on an on-chip controller that interfaced with both SRAM and DRAM back in 2005; is that correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: No. As I recall, there was an on-chip controller that talked to certain things, and I don't think there was on-chip DRAM.

And then just from my general recollection in these types of devices, you would

have another controller that was out talking to some kind of really big, faraway DRAM. And I -- as I generally recall, those two kind of separate paths or portions of the system were in the focus of at least some things I was working on at that time.

ATTORNEY ZHONG: Counsel, we've been going for a little bit over an hour, and it's also 12:22 for Dr. Brogioli. I don't know whether he wants to take his lunch break right now or not, but I think we should take a break.

ATTORNEY CHANDLER: Why don't we just finish going through your experience, only a few more paragraphs.

ATTORNEY ZHONG: Okay.

BY ATTORNEY CHANDLER:

Q. Could you turn to paragraph 14 of Exhibit 2023. Let me know when you're there.

A. Okay.

Q. You state that you have publications related to "memory system design, optimization for memory systems and interconnect technology."

Correct?

A. That's correct.

Q. Are any of these publications

specifically related to stacked DRAM memory devices?

A. I don't recall specifically. As I remember, a number of them talked about different memory technologies and, in some cases, optimizing related to different memory technologies. I don't recall if some of those references also make reference to stacked DRAM or not -- stacked DRAM specifically or not.

Q. In paragraph 15 of Exhibit 2023, you state that you have various patents and patent applications; correct?

A. That's right.

Q. Are any of your patents or patent applications specifically related to stacked DRAM memory devices?

A. They, as I recall, don't specifically focus their claims on that, no. They may mention it in the specification.

Q. Before 2011, as we've been discussing these past few minutes, you worked with various SRAM and DRAM technologies, but not specifically stacked DRAM memory devices; is that fair?

A. In that time frame, I was not designing a complete or stacked DRAM device itself as a

whole.

Q. By 2011, do you believe a person of ordinary skill in the art would have been familiar with stacked DRAM memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say familiar with the concept in various contexts, depending on, you know, if they had seen an IEEE white paper that was published relating to some -- something called stacked DRAM. They would be aware of it.

BY ATTORNEY CHANDLER:

Q. By 2011, do you believe a person of ordinary skill in the art knew about ways to control and operate stacked DRAM memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Depending on -- we'd have to ask a more specific question. But if they were given an instruction manual for a product, I would think that they would understand an instruction manual, for example.

BY ATTORNEY CHANDLER:

Q. By 2011, were stacked DRAM memory devices known in the art?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: There were different --

different references, publications, and things out there that were using the term "stacked" and the term "DRAM" perhaps, and they were using them in a lot of different ways. So those words were out there in the literature. But there were a lot of different variability in terms of how these different systems were designed or not designed and operated and things like that.

BY ATTORNEY CHANDLER:

Q. And the '160 and '060 patents disclose stacked DRAM memory devices in the patents; right?

ATTORNEY ZHONG: Objection; form.

Counsel, you said you would finish the line of question on his background, and I asked for a break about four minutes ago. How much longer are you going to go?

BY ATTORNEY CHANDLER::

Q. Can you answer the question, Dr. Brogioli?

A. I would say the '060 patent, for example, talks about memory devices and the ability to have multiple of what the patent refers to as array dies vertically above other components in the system. That's a concept -- one of the

concepts in the patent.

ATTORNEY ZHONG: Counsel, can we take a break? This is the second request.

ATTORNEY CHANDLER: Just one moment.

BY ATTORNEY CHANDLER::

Q. Would you, Dr. Brogioli, consider that to be stacked?

A. I would say in the general sense that your -- I think the term "stacked" may be fitting here in the sense of putting multiple things vertically arranged. There's a lot -- certainly a lot more than what these patents are getting at, but that's one concept within them.

ATTORNEY CHANDLER: All right. Why don't we take a break.

THE VIDEOGRAPHER: Off the record. The time is 10:27.

(Recess taken from 10:27 a.m. to 10:42 a.m.)

THE VIDEOGRAPHER: Back on the record. The time is 10:42 a.m.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have any corrections or clarifications to any of your testimony earlier today?

A. Not that I recall, no.
Q. Please turn to paragraph 29 of your expert declaration, marked as Exhibit 2023 and let me know when you're there.
A. Okay.
Q. In paragraph 29 of your expert declaration marked as Exhibit 2023, you state that you have been "asked to apply Samsung's definition of education and work experience."
Correct?
A. Yes.
Q. And I want you to take a look at the petition where Samsung provided that information -- I'll put it in the chat again for everyone to see, or feel free to pull up your own copy if you have one handy.
(Exhibit Number was previously marked for identification.)
BY ATTORNEY CHANDLER:
Q. We can start with the petition for the '160 patent. Let me know when you have that on the screen.
A. Okay.
Q. Page 5 of the -- both petitions, actually, provided Samsung's definition of a

person of ordinary skill in the art; correct?

A. That's correct.

Q. So does -- does page 5 of the petitions in the two IPRs show the definition of a person of ordinary skill in the art that you applied?

A. Reviewing it.

(Witness reviews document.)

A. Okay. Yes, that looks right.

Q. For purposes of these proceedings, do you agree that a person of ordinary skill in the art would have been familiar with the JEDEC industry standards, been knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with the memory controller and other parts of a computer system?

A. Yes, that's right.

Q. For purposes of these proceedings, do you agree that a person of ordinary skill in the art would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed, three-dimensional stacking and circuitry used to access and control

computer memories?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That looks right in the context of this sentence, yes.

BY ATTORNEY CHANDLER:

Q. And that's what you applied as the definition of a person of ordinary skill in the art; correct?

A. In the context of this overall definition, yes.

Q. Could you turn to the '160 patent, marked as Exhibit 1001. Let me know when you've got it.

A. Okay.

Q. And you might as well also pull up the '060 patent, just to have them handy.

A. Okay.

Q. In the '060 patent, turn to the top of Column 22. And I'll ask you about both patents, but I'll just give you column and line numbers for the '060 patent.

A. Okay.

All right.

Q. The top of Column 22, the '060 patent, and there's also a similar disclosure in the '160

patent, refers to "array dies may include DDR, DRAM, SDRAM, flash memory, or SRAM, to name a few."

Correct?

A. I see that portion of the sentence. It looks like it's referring to Figure 8.

So it's saying that as with the array dies 210 and 310, the array dies 824 may include any type of random access memory die -- for example, array dies include DDR, DRAM, SDRAM, flash memory, or SRAM, to name a few.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with SRAM memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: As a memory device itself, yes.

BY ATTORNEY CHANDLER:

Q. In your opinion, would a person of ordinary skill in the art have been familiar with flash memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say as a memory device or a product you could purchase, yes.

///

BY ATTORNEY CHANDLER:

Q. A person of ordinary skill in the art would have been familiar with a type of flash memory referred to as NAND, flash memory; correct? N-A-N-D?

A. I would say, yes, NAND memory was a type of memory product available at the time or known at the time.

Q. In your opinion, did a person of ordinary skill in the art know how to implement the invention of the '060 and '160 patents using array dies with SRAM memory as referenced, for example, at the top of Column 22 of the '060 patent?

A. Going back to the description in Figure 8.

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So it looks like Figure 8 is talking about an embodiment that supports the JEDEC 3DS operation, makes reference to RDIMM architectures.

And then at the top, 20 is saying a number of different components that can go into this topology. So it looks like, to the extent that block 824 in Figure 8 is talking about

flavors of these different memory technologies, a person of skill would understand what Figure 8 is talking about.

BY ATTORNEY CHANDLER:

Q. The top of Column 22 refers to array dies 210 and 310 as well; correct? And the same in the '160 patent.

A. That's correct. It says, "As with the array dies 210 and 310."

Q. So, in your opinion, would a person of ordinary skill in the art be able to practice the inventions of the '060 and '160 patent using array dies 210 and 310 where those array dies are SRAM memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That sounds like something outside the scope of what I've addressed in my declaration. But it looks like what the patent is saying -- I guess what the patent is saying in the top of 22 is, similar to array dies 210 and 310, if these array days 824 in Figure 8 can include a type of random access memory die, and it gives a couple of examples.

BY ATTORNEY CHANDLER:

Q. What about array dies 210 and 310? In

your opinion, can those be SRAM memory devices?

A. I haven't performed that analysis. The way I'm interpreting this passage at the bottom of Column 21 and top of 22 is it's just saying, similar to 210 and 310, these array dies 824, it can include a type of -- of random access memory die. So it's -- it's a characteristic of the access pattern.

Q. In your opinion, can array dies 210 and 310 in the '060 and '160 patents be flash memory, as suggested, for example, at the top of Column 22 of the '060 patent?

A. It looks like what Column 22 is saying at the top about Figure 8 is that the array dies can include, the third line down, flash memory as a form of random access memory.

Q. What about array dies 210 and 310, which are not in Figure 8 but are in Figures 2 and 3?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Well, it looks like this sentence at least is saying, as with the array dies 210 and 310, that the array dies may include any type of RAM, R-A-M, and it gives a couple of examples. It seems like that qualifier in this

sentence is intended to apply to the array dies 210 and 310 as well.

BY ATTORNEY CHANDLER:

Q. I'm a little unclear what you're trying to convey.

In your opinion, can the array dies 210 and 310, shown in Figures 2 and 3 of the '060 and '160 patents, be SRAM memory devices or not?

ATTORNEY ZHONG: Objection; form, outside the scope.

THE WITNESS: So, again, I haven't, in my declaration, performed an analysis of all of the types of -- or if there are other types of memory technology that can be used for 210 and 310.

However, what the specification is saying is that, at the top of Column 22, you can include any type of random access memory die, and that qualifier is applying to 210 and 310 as well. So it looks like it's talking about random access memory die here and different flavors of them that apply to array dies 210 and 310 as well.

BY ATTORNEY CHANDLER:

Q. And do you believe an SRAM is a flavor of a random access memory die?

A. If you're asking -- I would say that this sentence is talking about -- or this passage, memory technology, in this case a form of static random access memory storage. I haven't looked at whether or not a given SRAM itself, either physical device or publication on it, would be an array die in this context one way or the other.

Q. So to be clear, do you have an opinion on whether or not the array dies 210 and 310, shown in Figures 2 and 3 of the '060 and '160 patents can be SRAM?

A. I would say what this sentence is saying is that the array dies here, 210 and 310, can include various types of random access memory die. And some of the example of array dies it talks about -- I think your question was initially around SRAMs, as it mentioned SRAMs array dies.

Q. And do you believe a person of ordinary skill in the art could successfully practice the '060 and '160 patents where the array dies 210 and 310, as shown in Figures 2 and 3, are SRAM? Or do you think that would be beyond the skill of a person of ordinary skill in the art?

ATTORNEY ZHONG: Objection; form, outside the scope.

THE WITNESS: So to the extent these two sentences are saying that the array dies 210 and 310, can include a type of random access memory die that is an SRAM die, I haven't been asked to perform that analysis one way or the other as -- in this declaration as to whether a person of skill in the art could perform that or not.

BY ATTORNEY CHANDLER:

Q. Do you have any opinion on that question right now?

A. I don't have an opinion one way or the other coming into today's deposition. I haven't really studied the patent to that length today.

Q. In your opinion, can array dies 210 and 310, shown in Figures 2 and 3 of the '060 and '160 patents, be flash memory?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So, again, I would say, just as this language at the bottom of Column 21 and top of 22 states, that the array dies 210 and 310 can be various types of random access memory dies, and examples of array dies that are given are flash memory array dies.

Q. Do you believe a person of ordinary skill in the art would have a reasonable

expectation of success if they implemented array dies 210 and 310 shown in Figures 2 and 3 of the '060 and '160 patents using flash memory, or do you think that would be beyond the skill of a person of ordinary skill in the art?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: Yeah, I would say coming into today, I don't recall a discussion of a reference that may have been something that met the limitation of a flash memory array die; and I haven't formed an opinion one way or the other if this person of skill could implement what's described in the patents with something being a flash memory array die.

I haven't been asked to look at that yet, or today.

BY ATTORNEY CHANDLER:

Q. But to be clear, the '060 and '160 patents, if I understand your testimony a moment ago, indicate that array dies 210 and 310 can be flash memory; correct?

A. That the array dies 210 and 310 can include different types of random access memory die, and an example of one of those random access memory die is flash -- is a flash memory type

random access memory die.
Q. Could you turn to Column 5 of the '060 patent and go to line 39, please.
A. Okay.
Q. The '060 and '160 patents disclose an embodiment with three array dies; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: I'm not sure I'm quite following you. You pointed me to Column 5 at 39?
BY ATTORNEY CHANDLER:
Q. Correct.
A. Oh, I was one line off:
"As further examples, the memory package 200, which is Figure 2, may include three or sixteen array dies."
Q. So do you agree the '060 and '160 patents disclose the element embodiment of the invention with three array dies?
ATTORNEY ZHONG: Objection; form, outside the scope.
THE WITNESS: So it looks like it's saying -- I'm going back up to about line 34.
"While the memory package 200 is illustrated, including four dies, the memory package is not limited as such

and can include any number. Figure 3, the memory package may include eight array dies. As another example, memory package 200 may include three or sixteen array dies."

So it looks like at least in terms of the embodiment pointed to in Figure 2, it's mentioning three array dies as one example here.

BY ATTORNEY CHANDLER:

Q. In your opinion, would a person of ordinary skill in the art know how to take an address space and divide it by three?

ATTORNEY ZHONG: Objection; form. If you're asking in sort of a numerical pencil-and-paper exercise, then I would think so. But in terms of building a memory device or memory module that -- you know, using a -- base 2 addressing and trying to break things up into threes, that tends to be complicated.

BY ATTORNEY CHANDLER:

Q. In your opinion, would a person of ordinary skill in the art have a reasonable expectation of success in practicing the claimed inventions of the '060 and '160 patents when there are three array dies, as suggested in this

example of Column 5, line 39, of the '060 patent?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So I see here that it -- the patent's mentioning the embodiment in Figure 2, three array dies is an option.

I haven't performed an analysis of -- of whether -- one way or the other the level of difficulty a person of skill would have in trying to accomplish that.

BY ATTORNEY CHANDLER:

Q. But as far as actually taking an address space and dividing it into three, that's a calculation that a person of ordinary skill in the art could successfully complete in the context of a stacked memory device; is that fair?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say that if I -- if I said to a person of skill in the art, "Here is a 900-byte address space for a piece of memory," they would understand, as an academic exercise, while one piece is the zero to 299 and the next piece is 300 to 599 and maybe the next third piece is 600 to 899. But that's more of a -- sort of a pencil-and-paper-type exercise.

///

BY ATTORNEY CHANDLER:

Q. Does the '060 and '160 patents provide any teachings on how to implement the claimed inventions in the situation where there are three array dies?

A. I see that the -- at least three array dies are mentioned here in Column 5. And it looks like there's some mention of it in the background. I haven't performed an analysis -- I'm just skipping back through the specification.

I haven't performed an analysis as to the universe of teachings the '060 -- the patents, I should say, teach one way or the other around a specific three-array-die embodiment.

(Whereupon, Exhibit Number 1054 in both IPRs was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. All right. I want to introduce a new exhibit, which I'll put in the chat. It's the same exhibit for both IPRs, so I'll put it in twice. One is stamped with the '060 IPR. The other is stamped with the '160 IPR. But it's, otherwise, the same document. And let me know

when you have Exhibit 1054 in front of you.

A. I dragged it to the wrong place.

ATTORNEY ZHONG: Objection. I'm going to object to the exhibit as lacking authentication and complete hearsay.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have Exhibit 1054 in front of you?

A. I do, yes.

Q. Exhibit 1054 is Netlist's technology tutorial in the case where you were the expert witness for Netlist in the area of JEDEC standard essential DRAM memory technology related to DIM, RDIMM and LRDIMM, as stated on pages 205 to 206 of your expert declaration marked as Exhibit 2023; correct?

A. I would say, as I recall, this presentation was a -- excuse me -- a technology tutorial that was printed -- as I recall, presented at that hearing related to the 1023 matter that I -- I believe I testified on one or perhaps maybe two of the Netlist patents.

Q. You've seen Exhibit 1054 before; correct?

A. I certainly don't recall all of the

content from memory, but I think I may have seen this presented at that hearing some time ago and perhaps in another Netlist-related deposition.

Q. Please turn to page 2 of Exhibit 1054 and let me know when you're there.

A. Okay.

Q. Does page 2 of Exhibit 1054 show a picture of a DIMM, D-I-M-M, which is to say a dual in-line memory module?

A. It looks like the green arrow labeled "Memory Module" is pointing to -- perhaps what this slide is intending to indicate is a dual in-line memory module.

Q. Please turn to page 3 of Exhibit 1054 and let me know when you're there.

A. Okay.

Q. Does page 3 of Exhibit 1054 also show a DIMM memory module at the bottom of the page?

A. Possibly. I don't -- the description on the prior page characterizes or notes the fact that there are dual in-line memory modules as there's connections on each side of the module, but I note that the -- it looks like a Samsung device. We're really only seeing one side of it visually.

Q. Do you agree that SDRAM memory devices emerged in the 1990s and have been standardized by JEDEC?

A. Yes, that sounds right.

Q. Do you agree that SDRAM has evolved in several generations, including DDR, DDR2, DDR3, and more recently, DDR4?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That there are JEDEC -- JEDEC iterations of these different DDR technologies. At the time of this presentation, I think the most recent was DDR4, as it says.

BY ATTORNEY CHANDLER:

Q. DDR, DDR2, DDR3, and DDR4 are JEDEC standards that a person of ordinary skill in the art knew about; correct?

A. That there are, as I recall, JEDEC-related standards for each these technologies, that at the time of this -- the time this presentation was created, existed.

I guess I don't know whether or not a person of skill -- if sort of a person off the street had access to them or not. But those JEDEC documents existed.

Q. And the '060 and '160 patents, they

specifically refer to DDR3 and DDR4; correct?

A. Looks like there's mention of DDR3 and 4 in certain descriptions.

Q. In the '060 and '160 patents?

A. That's -- that's right. I'm at least seeing it -- roughly the top of Column 5, there's some mention of it.

Q. Could you pull up Exhibit 1019, which is the JEDEC DDR3 standard that I believe I shared in the chat earlier with you. And just let me know when you have it up on the screen.

A. You did share it. I have it up.

Q. You do not dispute that a person of ordinary skill in the art would have known about the JEDEC DDR3 standard marked as Exhibit 1019, dated November 2008; correct?

A. That a person of skill in the art would be aware that these JEDEC standards were published -- this one looks like April of '08 -- sorry -- November of '08.

(Exhibit Number 1021 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you pull up Exhibit 1021, which I just put in the chat. Let me know when you have

it.

A. Okay.

Q. And you do not dispute that a person of ordinary skill in the art would have known about the JEDEC standard MO-207 marked as Exhibit 1021 and dated December 2010; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I'm just taking a second to flip through this.

(Witness reviews document.)

So I see that the -- I'm just on page 1 of the exhibit. It says it's a JEDEC solid state product outline. I don't remember -- I don't recall that I've specifically seen this or not. But it looks like a JEDEC document that it says, in the bottom, quote, "has been prepared and published by the JEDEC JC-11 committee."

BY ATTORNEY CHANDLER:

Q. If you turn back to the DDR3 JEDEC standard marked as Exhibit 1019 and if you go to page 3, you'll see that the DDR3 standard refers to this MO-207 standard marked as Exhibit 1021; correct?

A. That looks correct. It's using the -- a ball-out that's using the MO-207 that is

exhibit -- it sounds like is Exhibit 1021.

Q. Could you pull up Exhibit 1035, which should be coming in the chat. Let me know when you have it.

(Exhibit Number 1035 was previously marked for identification.)

THE WITNESS: Okay.

BY ATTORNEY CHANDLER:

Q. You do not dispute that a person of ordinary skill in the art would have known about the JEDEC standard for GDDR4 SGRAM marked as Exhibit 1035; correct? Which is dated November 2005, as shown on the second page.

A. That sounds correct. This, at least looking at it at a high level, looks like another JEDEC standard published in the 2005 time frame.

(Exhibit Number 2017 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. I'm going to put in the chat Exhibit 2017 that you cited, and just let me know when you have it open.

A. Okay.

Q. You do not dispute that a person of ordinary skill in the art would have known about

the JEDEC standard number 21C for DDR SDRAM registered DIMMs dated January of 2002, marked as Exhibit 2017; correct?

A. That looks correct. It's the 21C, it says, on the next few pages, published -- or at least January of 2002.

ATTORNEY CHANDLER: I'm going to mark a new exhibit in both IPRs as Exhibit 1055. I put it in the chat. They're the same exhibit in both IPRs so you can choose either one to open. And just let me know when you have Exhibit 1055 in front of you.

(Whereupon, Exhibit Number 1055 in both IPRs was marked for identification and is attached hereto.)

ATTORNEY ZHONG: Okay.

BY ATTORNEY CHANDLER:

Q. Exhibit 1055 is the JEDEC standard JESD79 for DDR SDRAM, dated June 2000; correct?

A. That's correct, yes.

Q. And DDR SDRAM is the type of memory devices discussed in Exhibit 2017 that we looked at just a second ago; correct?

A. It looks like the -- there's a variant

of DDR also discussed in Exhibit 2017 as well.

Q. You do not dispute that a person of ordinary skill in the art would have known about the JEDEC standard JESD79 for DDR SDRAM memory dated June 2000, marked as Exhibit 1055; correct?

A. No. That sounds right.

Q. The '060 and '160 patents refer to a proposed JEDEC standard for three-dimensional stacking, sometimes referred to as 3DS; correct?

A. That's right. I think in a few different places it mentions a 3DS architecture, or three-dimensional -- 3DS structure.

Q. And it would be fair to say that a person of ordinary skill in the art would have been familiar with the proposed JEDEC standard for three-dimensional stacking known as 3DS at the time of the '060 and '160 patents?

A. So it looks like in Column 18 of the '060, at line 15, it mentions a proposed three-dimensional stacking or 3DS standard for dual inline memory modules that's being considered by JEDEC.

I don't recall -- I don't recall that proposal necessarily being produced or if I saw it or not. But I see that it mentions it.

Q. It wasn't a secret; correct?
A. I would say -- I don't recall that I've seen it; but the patent specification makes mention of it, sure, in Column 18.
Q. Could you turn back to Exhibit 1019, the JEDEC JESD79-3 standard for DDR3 memory devices, and let me know when you have that back in front of you.
A. Okay.
Q. Page 13 of Exhibit 1019 refers to the chip select signal; correct?
A. That's correct.
Q. What does the chip select signal do?
A. It says, in the third row down, "Chip Select" -- the function is:
"All commands are masked, when chip select is registered high. Chip select provides for external rank selection on systems with multiple ranks. Chip select is considered part of the command code."
Q. Turn to page 33 of Exhibit 1019, the DDR3 standard, and let me know when you're there.
A. Okay.
Q. Page 33 of Exhibit 1019 shows a command

truth table for DDR3 memory devices; correct?

A. That's right.

Q. And as you mentioned a moment ago, one of the command signals for DDR3 memory devices is the chip select signal, which is the column with the heading "CS#"; correct?

A. That's right. It's one of the signals in this table or one of the fields in this table.

Q. The chip select signal is one of the signals used for a read or write command; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: If you look at the rows in bit Table 6, the write and read commands roughly start the 8th row down and go down for about the next 10 or 12; and we see that for -- excuse me -- each of these command and codings or commands that are coded in this table, the value of chip select is set to low.

Q. If the value of chip select were set to high, you could not perform a read or write command; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: If you are adhering to the command and coding mandated by this table and

trying to perform the writes and reads described from Row 8 through, I guess, six up from the bottom, what the table is telling you is that some command with the chip select set to high is not going to map to these commands, these reads and writes. So it doesn't look like you're going to get that specific command in that case.

BY ATTORNEY CHANDLER:

Q. Could you turn back to Exhibit 1054, which was the technology tutorial, and go to page 5, and let me know when you're there.

A. Okay.

Q. Do you agree with the statement on page 5 of Exhibit 1054 that a rank is a set of DRAMs that are written to or read from together?

A. In the context of what this slide is showing, that sounds right, that it's got a rank 1 illustrated or a rank 0 illustrated.

Q. And rank 1 is the green rectangle, and rank 0 is the red rectangle?

A. In this slide, yes.

Q. DQ refers to the data lines; is that correct?

A. That looks like what this slide is saying, yes. So there's eight -- excuse me --

eight DQ bits, and there's eight of them -- eight of those lines or eight sets shown in this slide.

Q. In a standard DIMM, the DQ data lines are bidirectional; correct?

A. In terms of the ability to send data or get data from a memory module, you could send -- yeah, you can write and receive data on the DQs.

Q. On the same DQs. So, in other words, it's not like there's dedicated DQs for write commands and then some other separate DQs for read commands; it's the same DQ data lines that are used for both read and write commands, meaning those DQ data lines are bidirectional; correct?

A. I think that sounds right, as I recall. I don't think this slide is getting into that, but ...

Q. In a standard DIMM with two ranks of memory devices, such as the example shown here on page 5 of Exhibit 1054, each DQ data line connects to both ranks of memory devices; correct?

A. I would say what this slide is intending to show is the concept that -- similar to your just previous question, the memory controller has

the connection of these eight sets of eight DQ lines, and you can see the downward-facing arrow with the memory controller and the upward-facing one in the green block -- the green rank 1 rectangle, that there's the ability to communicate data to and from the various DRAM memory devices on these modules.

Q. For example, if we look at the leftmost DQ data lines that go to DRAM-1, those DQ data lines will connect to both the DRAM-1 in rank 0 as well the DRAM-1 in rank 1; correct?

ATTORNEY ZHONG: Objection; form, relevance, scope.

THE WITNESS: So it looks like what this slide is showing is that there's -- it's intended to convey that for this memory -- this DIMM module that's illustrated here, there's the ability to send the DQ signals to the DRAM-1 in rank 0 or the DRAM-1 in rank 1. It's a high-level tutorial illustration. It's not showing the actual layout.

BY ATTORNEY CHANDLER:

Q. But to be clear, if each rank of memory devices is 64 bits wide, as shown in this example on page 5 of Exhibit 1054, there will only be 64 DQ data lines, not 128 DQ data lines, even though

there's two ranks of memory devices; correct?

A. I would say --

ATTORNEY ZHONG: Objection; form.

THE WITNESS: -- in this -- in this example, it's showing that there's 64 total DQ lines into and out of -- flowing to the memory controller; and the ability to, for example, read or write that 64 bits of data into either of the rank 0 or rank 1. In terms of how this is implemented in a -- in a given DIMM or something like that or what signals on the PCB are called, that's beyond the scope of this tutorial material.

BY ATTORNEY CHANDLER:

Q. In a standard DIMM using DDR memory devices, when each DQ data line connects to memory devices in two different ranks, similar to what's shown here on Page 5 of Exhibit 1054, how is it possible to read data from just one rank at a time or to write data to just one rank at a time?

A. I don't -- if you're asking in the context of Slide 5, I don't know that it gets into that level of detail.

Q. I'm asking in the context of a standard DIMM using DDR memory devices.

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say just as a general concept, the memory controller is sending various signaling; and then if the memory module itself is trying to support different numbers of rank, it may do things with the signaling coming in different ways to address the multiple ranks.

This doesn't sound like something I'm talking about were opinions in my declaration today, and I don't see that that's something discussed in this tutorial slide either.

BY ATTORNEY CHANDLER:

Q. The DDR standard that we just looked at, I believe you said the chip select signal is used for rank selection; is that correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I believe there was mention of rank in the description of the chip select signal in this reference that we were looking at a moment ago. I think Exhibit 1019.

BY ATTORNEY CHANDLER:

Q. The chip select signal can be used to select the rank of memory devices being targeted for a read or write command; correct?

A. As I recall that definition -- perhaps

you can point me back to the page -- talked about in the command table -- here it is. Maybe not -- in the command table how the chip select signal is described, and it described it as being related to ranks.

Q. And specifically selecting the rank of memory devices; correct?

A. So I'm back to Table 1 on page 28, and it says -- the various chip select signals are shown here. There's, I think, four of them in this example. And commands are masked when chip select is registered high. It provides for external rank selection on systems with multiple ranks. Chip select is considered part of the command code.

Q. You believe a person of ordinary skill in the art knew that the chip select signals can be used to select the rank of memory devices targeted for a read or write command?

A. I think they would understand this Exhibit 1019 and the description in this table that says, "Chip select provides for external rank selection on systems with multiple ranks," you know, taken in the context of the document.

Q. Can you turn back to Exhibit 2017, the

JEDEC 21-C standard, and go to page 13.

A. 2017. And you said page 13?

Q. Yes.

A. Okay.

Q. Page 13 of the JEDEC 21-C standard marked as Exhibit 2017, shows the wiring for a 64-bit-wide DIMM with two ranks of memory devices; correct?

A. It says in the -- the heading right under the blue bar -- it's a block diagram, 64-wide DIMM. And it says it's "populated as two physical banks of by-8 DDR SDRAMs.

Q. And at the time of Exhibit 2017, the term "physical bank," shown in the upper right, was used instead of the term "rank"; but the two terms are referring to the same thing; correct? The physical bank is a rank?

A. I would say that this -- there's been some back-and-forth between, I think, various experts on this -- that at certain points in time, the words "bank" and "rank" in -- in the world of JEDEC were used sometimes interchangeably, perhaps sometimes not.

They're also used in different ways in different references. I see here that the

reference, at least for this page, is using the term "bank."

Q. It would be fair to characterize page 13 of the JEDEC 21-C standard marked as Exhibit 2017 as showing a 64-bit-wide DIMM with two ranks of memory devices; correct?

A. It could be. I don't recall discussing this in my declaration, but I note that for this figure, there an RS1 signal in the upper left and an RS0. It looks like the RS1 is going to D8 through D15 on its chip select line; whereas, the RS0 signal is going to D0 do D7 on its chip select line. So those -- those incoming signals may be selecting one set of memory devices, D0 to D8, versus a second set of memory devices, D8 to D15.

Q. On page 13 of Exhibit 2017, would it be fair to call all memory devices D0 through D7 which receive the chip select signal RS0 as part of rank 0; and to call the memory devices D8 through D15, which receive the chip select signal RS1, as part of rank 1?

A. I would say possibly. I haven't studied this figure coming into today, but it looks like the -- going back to page 13, I lost my place.

The RS0 and RS1 are using -- being used

to go to chip selects for these SDRAMs in set D0 and D7 or D8 to D15; and then it notes in footnote -- or note 5 that the RS0 is for one side of the DIMM and RS1 is the other. So that's possibly what's going on here.

Q. And so the memory devices D0 through D7, they will all respond together to the same read or write command; correct?

A. It looks like in this figure, if you're sending the RS0 to D0 to D7 in a command, they are going to listen to that command and -- and handle their input bits accordingly that are shown here -- the D0 to -- sorry -- DQ0 to DQ7 for D0 or DQ8 to DQ15 or D1.

Q. So the memory devices D0 through D7 will operate together in response to a read or write command; or in the alternative, memory devices D8 through D15 will operate together in response to a read or write command; is that fair? As shown here on page 13 of Exhibit 2017?

A. I think that may be what the figure is showing, that there's -- the D0 to D7 is on one physical side of the DIMM; D8 to D15 is on the other. Depending on the RS 0 or RS 1 lines coming in and how they're set, that these -- the set of

these memory devices, if you will, the D0 to D15 -- whichever set is selected is going to respond to a command here.

Q. Each DQ data line shown on page 13 of Exhibit 2017 is shared by two memory devices; correct? So, for example, DQ0 is -- connects to both memory device D0 as well memory device D8?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That at least in terms of the -- the block diagram level of this illustration -- and I know that it's showing a block diagram -- it's showing that that DQ0 signal, for example, is able to connect to the I/O 0 D0 as well the I/O 0 D8.

BY ATTORNEY CHANDLER:

Q. So a data signal sent on any given DQ data line will go to two different memory devices; correct? As shown on page 13 of Exhibit 2017.

A. I don't see that the block diagram on this slide is showing necessarily a physical or electrical wiring diagram; but it's illustrating that this DQ0 signal, or line, coming into the module has to ultimately connect to D0 and D8 in its first I/O 0 input, or input/output.

Q. And that's true for all 64 DQ data lines; they're all shared by two memory devices, as shown on page 13 of the Exhibit 2017; correct?

A. I would say they're all illustrated the same way in this block diagram.

Q. The chip select signal prevents collisions when there are multiple memory devices sharing a data line that is shown on page 13 in Exhibit 2017; correct?

ATTORNEY ZHONG: Objection; form. I don't see the figure here talks about that one way or the other.

BY ATTORNEY CHANDLER:

Q. That's what's taught by the JEDEC standard; correct, the rank selection by the chip select signal?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say that the JEDEC specification we're looking at talks about the chip select signal and how it -- how it relates to signaling for ranks. If there's a section of the JEDEC you'd like me to look at, I'm happy to, but I don't see that anything we've looked at up until now gets into that part of the potential behavior of a memory module.

BY ATTORNEY CHANDLER:

Q. In forming your opinions, you did not consider whether the chip select signal can be used to prevent collisions when there are multiple memory devices sharing a data line; correct?

A. In my declaration, there's discussion of various chip select signals in various embodiments of various other prior art references. I don't recall in my declarations for today discussing -- I believe I mentioned this JEDEC -- perhaps this JEDEC reference in my declaration, but discussing the universe of language of chip select and how it's described in this reference.

Q. In forming your opinions, did you consider whether a person of ordinary skill in the art knew how to use the chip select signal to prevent collisions when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form. Vague.

THE WITNESS: I would say I took into consideration the way in which chip select signal would be described in various parts of the JEDEC standard and in addition to how chip select may be

used in various of the prior art references that I discuss in my declaration.

BY ATTORNEY CHANDLER:

Q. Did a person of ordinary skill in the art know how to use chip select signals to prevent collisions when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: I would say the person of skill in the art would know how to use chip select -- for example, how it would be described in JEDEC; or in other examples, how it might be described or used in its -- in a specific way in a given reference.

BY ATTORNEY CHANDLER:

Q. So what's the answer to my question about whether the person of ordinary skill in the art knew how to use chip select signals to prevent collisions when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: So my answer: You'd have to be more specific in your question.

The -- the chip select signal is discussed in my declaration in various places,

specifically with certain references or certain arguments Samsung's expert made during his deposition, as I recall.

It's also discussed in certain ways in the various JEDEC references.

BY ATTORNEY CHANDLER:

Q. But can you tell me now what your opinion is about whether or not a person of ordinary skill in the art would know how to use the chip select signal to prevent collisions when there are multiple memory devices sharing a data line? Or do you not have an opinion on that question?

ATTORNEY ZHONG: Objection; form, misstates the prior testimony, and vague.

THE WITNESS: I would say you have to ask a more specific question or a more specific reference, for example.

BY ATTORNEY CHANDLER:

Q. Can you give me any opinion in any situation whether or not a person of ordinary skill in the art would know how to use the chip select signal to prevent collisions when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would have to ask for a more specific example, or we can talk about in my declaration various places I mention chip select. But the -- that is potentially a signal in a much broader complex system with a number of other things going around. So I'd have to get much more specific for your example.

BY ATTORNEY CHANDLER:

Q. Well, I'm not the one trying to provide the example. I'm trying to get your opinion. I'll just ask you one more time, and it's okay if you can't give a better answer. But I just want to make sure we're giving you every opportunity to express yourself.

The question is: Do you have an opinion on whether or not a person of ordinary skill in the art would know how to use the chip select signal to prevent a collision when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: Again, I would say I'd have to answer you in the context of a give -- or we can give an example. Chip select, even in the JEDEC standard you referenced me to, is just one -- well, the chip select signal may be

comprised of multiple signals, but that's one of hundreds and hundreds of other signals here.

So I'd have to -- either we could discuss the examples that I discuss in my declaration or a specific use in the JEDEC reference. But, in general, that's too vague of a question for me to answer.

BY ATTORNEY CHANDLER:

Q. So taking the specific example of page 13 of the JEDEC reference marked as Exhibit 2017, do you believe a person of ordinary skill in the art could use the chip select signal to prevent a collision when there are multiple memory devices sharing a data line, as shown here?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say a person of skill in the art would understand how to use the chip select signal as it's described in this reference. For example, at least in part, how it's talked about in the command and codings of Table 1 or the definition of chip select signal elsewhere.

BY ATTORNEY CHANDLER:

Q. And would that use of the chip select signal that you were referring to prevent a

collision when there are multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: The question is a little too vague. I don't -- again, you'd have to get more specific. This person of skill would understand what chip select does, for example, in the context of this reference.

BY ATTORNEY CHANDLER:

Q. I'll give you one last chance. Page 13 of the JEDEC 21-C standard marked as Exhibit 2017 shows multiple memory devices sharing a data line.

My question is whether a person of ordinary skill would know how to use the chip select signal to prevent collisions when there are multiple memory devices sharing a data line.

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say, again, they would know how to use the chip select signals described in this reference for their intended use in the document as to how they're described.

If you're asking about a use case outside of this reference or something else, I'm happy to talk about a specific example.

BY ATTORNEY CHANDLER:

Q. How about during a read command?

A. As I recall, the reference talks about how, in at least the table we discussed earlier, a chip select signal is to be set for various flavors of read commands.

Q. Would a person of ordinary skill in the art know how to use the chip select signal to prevent collisions when performing a read command on a memory module with multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say for a memory module, for example, as those described in this 21-C standard, they would understand how the chip select signal is described in the reference.

BY ATTORNEY CHANDLER:

Q. That doesn't answer my question, though, because my question concerns collisions.

Can you answer my question?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: The question is too vague as to generally contemplate what you're referring to as "collisions."

///

BY ATTORNEY CHANDLER:

Q. What's a collision?

A. I'm not -- it was your question. Perhaps you can clarify what you're referring to. I believe I talk about certain types of collisions in my declaration --

Q. Would a person of ordinary skill in the art know how --

A. Sorry. I was going to -- go ahead.

Q. Would a person of ordinary skill in the art know about collisions between multiple memory devices sharing a data line? For example, if they both tried to output read data at the same time?

A. I would say that sounds like you're asking something similar to what I talk about in my declaration, that a person of skill would understand -- it would be problematic to write -- sorry.

If multiple memory devices, for example, are outputting read data onto the same wire at the same time, that's going to cause problems.

Q. That would be an example of a collision?

A. In the context that multiple memory

devices are outputting their respective read data onto the same wire at the same time, that can be viewed as -- that's a form of collision.

Q. And another example of a collision is if the memory controller is sending write data at the same time that the memory devices on the other end of the data lines are outputting read data; correct?

A. As a general example, that's another flavor of collision, yes.

Q. When I was using the word "collision," that's what I had in mind. Did you have something else in mind?

A. Not specifically one way or the other, no. I think those are two examples that I discuss -- possibly the only two examples I discuss in my declaration.

Q. Would a person of ordinary skill in the art know how to use the chip select signal to prevent collisions when performing a write operation to a memory module with multiple memory devices sharing a data line?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: Well, in real systems or the prior art references I discuss in my

declaration, there's more going on than just a chip select signal. But just as the JEDEC reference says, this person would understand, at least in the context of a memory module similar to that described by JEDEC in 21-C, how the chip select signal works here.

BY ATTORNEY CHANDLER:

Q. And does the chip select signal prevent collisions when there are memory devices sharing a data line?

A. I would answer a little differently that there are a number of things going on in memory systems that are coordinating the various timing of things going across wires, for example.

Q. And those --

A. Just as we see in the prior art references in terms of trying to deal with various aspects of timing.

Q. A person of ordinary skill in the art knew how to prevent collisions when there are multiple memory devices sharing a data line in the memory module; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It would depend on your example.

BY ATTORNEY CHANDLER:

Q. Well, they knew how to do it, for example, on page 13 of the JEDEC 21-C standard marked as Exhibit 2017; right?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: This page, as I'm viewing it, doesn't mention anything using your word "collision." It's describing at a block diagram level how a subset of signals should be, I guess, logically connected together on this page.

BY ATTORNEY CHANDLER:

Q. Can you answer my question whether a person of ordinary skill in the art would be able to prevent collisions in a memory module such as the one described on page 13 of the exhibit -- JEDEC 21-C standard marked as Exhibit 2017?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Perhaps there's a section of this standard talking about collisions you want to point me to. But just as I said before, if you're asking about a chip select signal, this person of skill in the art would know how to use it as it's described in the JEDEC reference.

BY ATTORNEY CHANDLER:

Q. To avoid collisions?

ATTORNEY ZHONG: Objection; form. Asked and answered multiple times.

THE WITNESS: I would say to the -- to however it's described in the reference. I don't see where you've pointed me in this JEDEC specification that it talks about collisions one way or the other.

BY ATTORNEY CHANDLER:

Q. I'm asking you. I'm not asking myself to point to something. I'm asking you for your opinion.

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say, again, they -- they would know how to use the chip select signal, if we're focusing just on this JEDEC reference, in the manner in which the JEDEC reference describes it.

BY ATTORNEY CHANDLER:

Q. Would a person of ordinary skill in the art have a motivation to avoid data collisions?

A. If we're talking about the general concept of four memory devices all trying to send or read data to some kind of receiver and they're all sending it at the same instance in time, and the -- just like I talk about in my declaration,

the line can either be in a logic low or a logic high state. I think as a general example, they might understand that that's problematic, or they would understand that that's problematic.

Q. And they'd be motivated to avoid such data collisions; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: In that sort of hypothetical tutorial example, if they understood that there was one wire and only one sender can use it at a time, then I probably don't want to have four senders using it at a time.

BY ATTORNEY CHANDLER:

Q. If a person of ordinary skill in the art did not use the correct timing provided in the JEDEC standards for DDR3 memory devices, they could get collisions on the bidirectional data lines used with those memory devices; correct?

A. I guess I would say that there are certain timing requirements mandated -- generally mandated by JEDEC. And so if I'm trying to build a JEDEC-compliant device -- for example, something that would be compliant with what's described in Exhibit 2017 -- I would want to at least obey those timing requirements that are mandatory by

the standard.

Q. And if you don't obey those timing requirements, one result is there could be data collisions; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say one result is your -- your system wouldn't be compliant with JEDEC as to whether or not that would result in some form of collision. I haven't performed that kind of analysis for a specific example.

BY ATTORNEY CHANDLER: Why don't we go off the record for lunch.

THE VIDEOGRAPHER: Off the record. The time is 12:05.

(Luncheon recess taken from 12:05 p.m. to 12:51 p.m.)

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P R O C E E D I N G S

- - -

CONTINUED EXAMINATION

THE VIDEOGRAPHER: Back on the record. The time is 12:51.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have any clarifications or corrections you would like to make to any of your testimony so far?

A. Not that I recall, no.

Q. Could you turn back to Exhibit 1019, the JEDEC standard for DDR3, and let me know when you have it in front of you, and go to page 23.

A. Okay.

Q. Toward the bottom right of page 23 of Exhibit 1019, the JEDEC standard for DDR3, there is a figure with a column for CAS latency; correct?

A. Yes, I see that.

Q. What is CAS latency?

A. I believe it refers to the column address strobe latency. And it's an aspect of

timing related to -- in certain types of memory devices. And it looks like this section talks about some of the mode registers for DDR3 that relate to that and some other fields.

Q. Under the JEDEC standard for DDR3 memory devices, CAS latency could be set to 5, 6, 7, 8, or 9 clock cycles, as shown on page 23 of Exhibit 1019; is that correct?

A. That looks like at least some of the values that the -- excuse me -- that the CAS latency could be set to. I think you mentioned 5 through 9.

Q. Or 10 clock cycles; right? That's also specified in the standard?

A. I see that, yes. Those are the -- that's the CAS latency. You set the bits accordingly to get a different value.

Q. So the JEDEC standard permits a range of different CAS latency. It doesn't mandate which of those CAS latencies you have to use; instead, the JEDEC standard permits you to choose one of the possible CAS latencies between, for example, five clock cycles up through 10 clock cycles? Is that fair?

A. It looks like it's reporting the writing

of this mode register to handle the different modes of operation for the DDR3 SDRAMs themselves. And so you can set the field accordingly as to which value you're using in your system.

Q. At the bottom of the next page, which is page 24 of Exhibit 1019, the JEDEC standard for DDR3, it says that, in the third or fourth line from the bottom, that read latency is defined as additive latency plus CAS latency; correct?

And it uses the abbreviations RL for read latency, AL for additive latency, and CL for CAS latency, resulting in a little equation, RL equals AL plus CL; correct?

A. That looks to me what it's saying in this CAS latency subsection.

Q. So the JEDEC standard for DDR3 memory devices permits a range of different read latencies that you can choose from rather than mandating only one possible read latency value; is that correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Looks like it's saying the read latency here, the overall read latency is comprised of two things, one being the CAS

latency, CL; and then you'd say, if you want additional information here, you can refer to the standard speed bin section on page 157.

BY ATTORNEY CHANDLER:

Q. But the read latency will be equal to or greater than the CAS latency. And as shown on page 23, the CAS latency can be set to the value that you get to choose between 5 clock cycles and at least 10 clock cycles; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like CAS latency is a parameter that you can control by this mode register based on, it sounds like, operating frequency and speed of your devices. And then as we go back to the bottom of 24, it refers us back to more of the standard speed bins, section for additional information.

And if I go there, it looks like it's showing a bunch of speed bin and table modes, so relating to how fast your device is operating or successfully operating, et cetera.

BY ATTORNEY CHANDLER:

Q. Could you turn to page 62 of Exhibit 1019, the DDR3 standard. Let me know when you're there.

A. Okay.

Q. The JEDEC standard for DDR3 memory devices provides examples of timing diagrams for various operations, such as a read command followed by another read command, as shown, for example, on page 62 of Exhibit 1019; is that correct?

THE DOCUMENT TECH: It looks like here it's showing various timing scenarios for a read command followed by a read command, and it seems to be showing for different burst lengths.

BY ATTORNEY CHANDLER:

Q. And -- and in the examples on page 62, Exhibit 1019, note 1 for the top example, Figure 33, states that the burst length, BL, is 8 pieces of data; the read latency, RL, is 5 clock cycles; the CAS latency, CL, is 5 clock cycles; and the additive latency, AL, is zero clock cycles; correct?

A. That looks like what it's saying.

Q. And then Figure 33 on page 62, Exhibit 1019, shows the timing diagram using those latencies and that burst length for an example of a read command followed by another read command; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like here it's showing read followed by read commands with the same CL is 5; AL is zero. I note that it's denoting BC4 now rather than BL8. It has a similar -- not quite identical, but similar diagram to what we saw in the above Figure 33.

BY ATTORNEY CHANDLER:

Q. Okay. To be clear, I was talking -- my question was about Figure 33 above. I think you were answering about Figure 34 below.

A. That's right. Maybe you can ask me again. Sorry.

Q. Figure 33 on page 62 of Exhibit 1019 shows the timing diagram using the latencies and burst length listed in note 1 for an example a read command followed by another read command; correct?

A. Yes. It's showing a read command, for example, at time T-zero, and another read command later in time, after some NoOps in time, T4.

Q. Now, if you go to the next page of Exhibit 1019, which is page 63, that shows an example of a timing diagram for a read command followed by a write command; correct?

A. A read command and then a number of NoOps -- sorry, read command at time -- or clock T-zero, and then a number of NoOps, I think five of them, and then a write command at T6.

Q. And the timing diagram in Figure 35 on page 63 of Exhibit 1019 uses in that example the latencies and the burst length that's indicated in note 1; correct? So, for example, a CAS latency of five clock cycles.

A. That looks like right, yes.

Q. And then if you go to page 73 of Exhibit 1019, the DDR3 standard gives an example of a timing diagram for a write command followed by another write command using the latencies and burst lengths indicated in note 1 of Figure 51 and also Figure 52; correct?

A. Looks like Figure 51 is a write -- a scenario where there's a write at clock T-zero and then a number of three NoOps, followed by a write command at T4. And the parameters settings are shown in here in footnote -- or in note 1; and then it looks like Figure 52 is the same WL, CL, and AL numbers. It looks like the BC is set to 4. And this is also a write -- followed by a write scenario of a write at clock T-zero; and then

three NoOps and a write at clock T4.

Q. In Exhibit 1019 on page 74 the JEDEC DDR3 standard provides examples of timing diagrams for a write command followed by a read command; using the burst length and latencies specified in note 1 of Figure 53 and note 1 of Figure 54; correct?

A. It looks like a write-to-read scenario where the write happens at time T-zero; and then there's NoOps for, I guess, 12 cycles or 12 time clots until a read in time 13. And the parameters used here are denoted in the four notes below the table.

Q. So on page -- I'm sorry.

On page 74 of Exhibit 1019, for the timing diagrams in Figure 53 and 54 where there's a write followed by a read command -- in both of those examples, the read latency is 5 clock cycles -- that's abbreviated RL; the CAS latency, CL, is also 5 clock cycles; the additive latency, AL, is zero clock cycles; and the write latency, WL, is 5 clock cycles; correct?

A. That seems to be what note 1 is saying, yes.

Q. And a person of ordinary skill in the

art would understand these timing diagrams in the DDR3 standard marked as Exhibit 1019 that we've been discussing on page 74, 73, 63, 62; is that fair?

ATTORNEY ZHONG: Objection to form.

THE WITNESS: I think that's right. In the context of this document, they would understand these timing -- this scenario that these timing diagrams are describing.

BY ATTORNEY CHANDLER:

Q. And we discussed earlier, a person of ordinary skill in the art would understand that it's important to follow the timing specifications in the JEDEC standard because the data lines for the DDR3 memory devices are bidirectional, meaning the same data lines used for a write command, that can be used for a read command. And if the timing isn't correct, there's a risk of a data collision; correct?

ATTORNEY ZHONG: Objection; form, vague.

THE WITNESS: I would say if a person of skill in the art is attempting to build a JEDEC-compliant device, they would look to the relevant JEDEC specification for timing that they -- they need to follow for that device. An

example of that might be a reference such as this.
BY ATTORNEY CHANDLER:
Q. To be more precise, for DDR3 memory devices, the JEDEC standard for the timing of read and write commands to the DDR3 memory device is Exhibit 1019; correct?
A. It looks like it is getting us various examples of write and read scenarios in how those memory devices behave for the timing parameters that are denoted in the notes we were discussing.
Q. If you go to the '060 patent marked as Exhibit 1001, go to Column 22, line 34.
A. Okay.
Q. Both the '060 patent and the '160 patent refer to something called rank multiplication; correct?
A. It looks like that's something that is mentioned here in Column 22.
Q. What is rank multiplication? How would you explain it to a layperson?
A. So I would say, in general, it can be the idea of -- one example being a memory module having more ranks of memory on it than perhaps the host system is aware of.
Q. Was a person of ordinary skill in the

art familiar with rank multiplication?

ATTORNEY ZHONG: Objection; form. At what time point are you asking?

BY ATTORNEY CHANDLER:

Q. At the time of the '060 and '160 patents, which -- and to be more precise, as we discussed at the beginning of the deposition, November 3rd, 2011.

A. Okay. I would say that they would be familiar with the concept at that point in time.

Q. Was rank multiplication known in the prior art?

A. I would say there were prior art examples that have different -- different examples of rank multiplication. In, you know, things like DIMMs for -- things like that.

Q. I'd like to introduce a new exhibit, which will be Exhibit 1058 in both IPRs. I just put it in the chat. And, again, it's the same exhibit, just different stamp, one for the '060 IPR and the other for the '160 IPR.

(Whereupon, Exhibit Number 1058 in both IPRs was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. Could you let me know when you have Exhibit 1058 open.

ATTORNEY ZHONG: I'm going to object to this new exhibit on the relevance ground at least.

THE WITNESS: Okay.

BY ATTORNEY CHANDLER:

Q. Exhibit 1058 is U.S. Patent Number 7,619,912, issued to Netlist; correct?

A. That's correct.

Q. You are familiar with the '912 patent; correct?

A. Yes, but I haven't looked at it recently -- super recently.

Q. The cover of the '912 patent marked as Exhibit 1058, shows that it's a continuation of an application filed on July 1st, 2005, that is now U.S. Patent Number 7,289,386; correct?

A. Correct.

Q. And if you look back at the passage in the '060 patent that we were talking about just a second ago, in the middle of Column 22, the '060 and '160 patents identify U.S. Patent Number 7,289,386 as disclosing rank multiplication; correct?

A. Going back to the '060 in the column 22 we are just at, it mentions embodiments of rank multiplication are described in greater detail in the '386 patent you just mentioned and '537, which are incorporated in their entirety by reference.

Q. And the '537 patent you're referring to is U.S. Patent Number 7,532,537; correct?

A. Correct.

Q. So for clarity, the '060 and '160 patents identified both the '386 patent and the '537 patent as embodiments of rank multiplication that are incorporated in their entirety by reference into the '060 and '160 patents; is that fair?

A. That sounds right, or embodiments of rank multiplication are described in greater detail in those patents.

Q. And as we just saw in the '912 patent marked as Exhibit 1058, the '386 patent was filed in 2005. So making it several years earlier than the '060 and '160 patent; correct?

A. That's -- that's correct, yes.

Q. Now, the '912 patent, marked as Exhibit 1058, also discloses rank multiplication, just like the '386 patent; right?

A. As I recall, that's correct; uses the term "multiplication" and so forth.

Q. And the '912 patent marked as Exhibit 1058 issued on November 17th, 2009, before the '060 and '160 patents were filed; correct?

A. Your question one more time?

Q. The '912 patent, marked as Exhibit 1058, issued on November 17th, 2009, which was before the '060 and '160 patents were filed; correct?

A. Gotcha.

That is -- that looks correct, yes.

Q. Figure 1A of the '912 patent, marked as Exhibit 1058, illustrates an example of a memory module with rank multiplication; is that fair?

A. It looks like 1A, at least the description of the drawing, is a module with four ranks of memory devices. And it says in Column 7, roughly line 36:

"Figure 1A, the memory module 10 has four ranks of memory devices and the computer system is configured for two ranks of memory devices per memory module."

Seems to be conceptually what that's describing.

Q. So, conceptually, Figure 1A of the '912 patent marked as Exhibit 1058 is describing rank multiplication? Is that what you're trying to say?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like it's describing, at least this figure, as having a module that's got four ranks of memory devices on it. And it's being inserted or it's in a computer system that's configured for two ranks of memory devices. So I don't see that it -- that's what it's describing. It seems to be like the module is containing more ranks than the system is aware of.

(Whereupon, 1059 Exhibit Number 1059 in both IPRs was marked for identification and is attached hereto.)

ATTORNEY CHANDLER: I'm going to introduce a new exhibit, 1059. Again, the same exhibit in both IPRs, the only difference being the stamp at the bottom. I've put it in the chat, and if you can let me know if you have it open on

the screen.

THE WITNESS: Okay.

BY ATTORNEY CHANDLER:

Q. And if you go to page 187 of Exhibit 1059, that's your signature on August 10th, 2023; correct?

A. That's correct.

Q. Then if you go to page 17 of Exhibit 1059, it's your testimony that Figure 1A from the '912 patent illustrates an example of a memory module with rank multiplication capability; is that fair?

A. That looks correct in this paragraph, yes.

Q. And a person of ordinary skill in the art, by the time of the '060 and '160 patents would have known about Figure 1A of the '912 patent and the '386 patent; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say that I think they would be aware of the -- for example, the '912 patent as a prior art reference.

BY ATTORNEY CHANDLER:

Q. And also the '386 patent, which was previously marked as Exhibit 1028? I can put it

in the chat if you like.

(Exhibit Number 1028 was previously marked for identification.)

ATTORNEY ZHONG: Is there a question pending?

BY ATTORNEY CHANDLER:

Q. A person of ordinary skill in the art by the time of the '160 and '060 patents would have known by Figure 1A of the '912 patent, marked as Exhibit 1058; and also Figure 1A of the '386 patent, marked as Exhibit 1028; correct?

A. It seems they would also be aware of the '386 patent, which is a filing date of July 1st, 2005.

(Exhibit Number 1031 was previously marked for identification.)

BY ATTORNEY CHANDLER::

Q. And a person of ordinary skill in the art at the time of '060 and '160 patents would also have known about rank multiplication as described in the '537 patent marked as Exhibit 1031; correct?

A. I'm just double-checking. Maybe I didn't download -- oh, here it is, 1031.

So it looks like the '537 patent has a

filing date of January 19th, 2006. So it seems like a person of skill in the art would be aware of these -- this reference as well.

BY ATTORNEY CHANDLER:

Q. Could you turn to the '160 patent marked as Exhibit 1001. Let me know when you have that one in front of you.

A. Okay.

Q. And then I want you to look at both, Claim 1 of the '160 patent as well as Claim 1 of the '060 patent. It doesn't matter to me where you get the claim language. If you want to get it from the patents directly, that's fine. If it's in your declaration or if you want to look at the petition, that's fine. I'm going to have some questions about the claim language. Just let me know when you're ready.

A. Okay. I've got the patents up.

Q. All right. And I'm first going to start sort of generally.

Claim 1 of the '160 patent recites a memory package comprising various limitations, including data terminals and control terminals; and then there are some limitations regarding stacked array dies; and then there's limitations

regarding die interconnects; and then there's limitations regarding a control die.

Is that fair?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: You're asking about Claim 1 of the '160; is that correct?

BY ATTORNEY CHANDLER:

Q. Yes.

A. So maybe we can take it from the top. It talks about data terminals and control terminals and makes mention of array die, and those components are -- are array dies are present in this Claim 1.

Q. The second limitation of Claim 1 of the '160 patent requires, quote:

"Stacked array dies including a first group of array dies and a second group of at least one array die," end quote.

Correct?

A. That's correct.

Q. And then in the '060 patent, Claim 1, there's a similar limitation requiring, quote:

"A plurality of stacked array dies, including a first group of array dies

and a second group of at least one array die," end quote.

Correct?

A. Yes. That's -- that's part of that limitation.

Q. Neither Claim 1 of the '160 patent nor Claim 1 of the '060 patent requires a rank; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't see that the word "rank" itself is explicitly used in either of the independent Claim 1 of the '060 or '160.

BY ATTORNEY CHANDLER:

Q. Neither Claim 1 of the '160 patent nor Claim 1 of the '060 patent requires a chip select signal; correct?

A. I don't see that the phrase, quote, "chip select" itself is used verbatim in these claim elements or in these independent claims.

Q. Neither Claim 1 of the '160 patent nor Claim 1 of the '060 patent includes any requirements on how any chip select signals are connected to the array dies or to the groups of array dies; correct?

A. I would say that neither -- similar

answer to before: Neither of these independent claims make an explicit mention of the phrase "chip select" in their language.

Q. And you haven't offered any opinions that either Claim 1 of the '160 patent or Claim 1 of the '060 patent should be construed to require a chip select signal or a rank; correct? That's not a claim construction opinion that you've offered?

A. I don't recall that being an opinion I offered in my declaration or declarations for this IPR.

Q. In Claim 1 of the '160 patent and Claim 1 of the '060 patent, the claimed group of array dies could be different from a rank of memory devices; correct?

A. So in the context of the '060 in the second claim element, it talks about a first group of array dies and a second group of at least one array die, each day -- I'm sorry -- each array die having data ports. I don't see that it's mentioning the word "rank" in this claim element or overall explicitly in Claim 1 as a whole one way or the other.

Q. And is your answer the same for the

'160 patent?

A. In that the '160 patent, Claim 1, also mentions groups of array dies, but doesn't use the language of rank within it -- within the language of the claim, the word "rank" specifically.

Q. Did you -- go to your expert declaration, marked as Exhibit 2023, and turn to page 46, and let me know when you're there.

A. Okay.

Q. In paragraph 84 of Exhibit 2023, you expressed the opinion that the claimed first group of array dies requires two or more array dies; correct?

A. That's right, that the claim recites the first group of array dies with die being --

(Interruption by the court reporter to clarify the record.)

THE WITNESS: With -- with -- so the claim states the first group of array dies with "dies" being in plural.

BY ATTORNEY CHANDLER:

Q. You have not offered any opinion about the validity of the '160 patent or the '060 patent if the claimed first group of array dies is satisfied by a single array die; correct?

A. I don't recall offering opinions on that one way or the other in this declaration or addressing that specifically.

(Exhibit Number 2007 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you turn to Exhibit 2007, which I'll also put in the chat for the convenience of everyone. And let me know when you have it on your screen.

A. Okay.

Q. Exhibit 2007 is a conference paper published in 2018, as shown at the bottom of the page; correct?

A. That is correct.

Q. In the second full paragraph of Exhibit 2007, in the middle of that paragraph, there's a reference to Figure 12.3.1; correct?

A. Just taking a second to revisit the paragraph.

Okay. I do see in the second paragraph -- I think you asked about Figure 12.3.1.

Q. And specifically in the second full paragraph of Exhibit 2007, there's a sentence

that reads:

"Figure 12.3.1 shows a conventional multi-drop TSV structure and the proposed spiral P2P TSV structure."

Did I read that accurately?

A. Yes.

Q. And the second paragraph of Exhibit 2007 refers to capacitive load; correct?

A. Yes, it mentions that.

Q. What is capacitive load?

A. It is -- in this context, it's talking about a load that -- or a load relating to capacitive in the system that can cause adverse effects -- for example, how tall you can build the stack of devices or how fast you can run it or the amount of power that's required, thermal issues, things like that.

Q. How would you explain to a layperson what the concept of capacitive load is and sort of what its relevance is to memory devices in general?

A. I would say as a -- as a general example, you might think of it trying to lift a weight or something like that. And you want to lift it up and down quite quickly. And if there's

a lot of -- if the capacitive load is increasing, you can't lift it up and down as quickly. So if you're trying to, for example, send signals down a wire, as the load's increasing on the wire, you might have to do things more slowly. But if you can reduce the load, you can send information more quickly, which in a lot of cases is better; things can run faster.

Q. So would a person of ordinary skill in the art have known about a capacitive load and the potential problems created by too much capacitive load?

A. Depending on the context, perhaps, yes.

Q. Would a person of ordinary skill in the art have known about capacitive load and the potential problems created by too much capacitive load in the context of memory devices?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say it would depend on -- probably on the context. I think as a concept, capacitive load -- as a general concept, a person of skill would understand what it is. In terms of how it may impact a specific aspect of designing a memory system, we'd have to get more specific.

BY ATTORNEY CHANDLER:

Q. Does capacitive load create a potential impact on the bandwidth of data transmissions, as indicated in the second paragraph of Exhibit 2007?

A. It looks like that's what this second sentence may be getting at, that because of drawbacks with the multi-drop implementation, there are obstacles that came up in getting, presumably, a new, higher bandwidth from the device.

Q. And does capacitive load create a potential impact on power consumption?

A. In -- in the context of the type of system that this reference might be talking about, it can.

Q. Would a person of ordinary skill in the art have known about the potential impacts of capacitive load on bandwidth of data transmissions and power consumption in the context of memory modules?

A. I would say a person of skill in the art would know that -- excuse me -- the notion of capacitive load can be applicable in designing certain types of memory modules, depending on what

you're trying to accomplish.

Q. And a lower capacitive load could help accomplish the goal of higher bandwidth of data transmission and lower power consumption; is that fair?

A. A person of skill trying to design a system may want to try and achieve all of those nice things you just said with a lower capacitive load. I'm not sure that lowering capacitive load, in and of itself just as a concept, is going to get you there. It's a concept, but it's -- it -- it impacts different things in different ways with the different systems.

Q. Let's be clear: If the capacitive load is higher, a person of ordinary skill in the art would know that that could slow down the bandwidth of the data transmission and increase the power consumption; correct?

A. Not necessarily. I think it would probably -- it would probably relate to the specific context that we're talking about.

Q. In the context of memory modules, if the capacitive load is higher, a person of ordinary skill in the art would know that could slow down the bandwidth of data transmissions and

increase the power consumption; correct?

A. It would depend on the system -- a specific system we're talking about or what was trying to be achieved or designed.

Q. In your opinion, did a person of ordinary skill in the art of memory modules care about the capacitive load or not?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It would depend on the type of memory module or the type of system they were trying to design or the environment it was going into.

BY ATTORNEY CHANDLER:

Q. So, in your opinion, in some types of memory modules, a person of ordinary skill in the art may be less sensitive to the amount of capacitive load than in other types of memory modules; is that fair?

A. That doesn't sound unreasonable, but they may not -- depending on what they're trying to design for in this module context, they, you know, would have to get much more specific as to whether they were particularly concerned one way or the other.

Q. Could you turn to page 2 of

Exhibit 2007 and look on the upper left in Figure 12.3.1 at the spiral PTP -- or, rather, P2P TSV structure proposed by this conference paper in 2018 and let me know if you see it.

A. I see it, yes.

Q. In the proposed spiral structure of Figure 12.3.1 of Exhibit 2007, what are the little purple tubes that are vertical?

(Witness reviews document.)

ATTORNEY ZHONG: Did you say "little purple tubes" or "little purpose tubes"?

ATTORNEY CHANDLER: Purple. Color purple.

THE WITNESS: It looks like it's showing at least part of what's the -- the interconnect either in the multi-drop -- the multi-drop scenario or the spiral P2P scenario.

BY ATTORNEY CHANDLER:

Q. In the proposed spiral structure in Figure 12.3.1 of Exhibit 2007, what are the purple lines that connect the purple tubes?

ATTORNEY ZHONG: Objection form.

THE WITNESS: I'm just rereading the reference to see how it describes them.

(Witness reviews document.)

THE WITNESS: I don't see that it's putting a label on what the purple lines are in the spiral P2P. As I recall, it's showing a pathway within the spiral layout or topology.

BY ATTORNEY CHANDLER:

Q. A pathway for what?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like -- in contrast to the conventional multi-drop on the left that goes up vertically connecting to each -- in each -- in each layer here, it's showing the pathway that goes around in a spiral configuration in the figure on the right.

BY ATTORNEY CHANDLER:

Q. In the proposed spiral structure in Figure 12.3.1 of Exhibit 2007, is the pathway that you're referring to in the chip itself?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't know that the figure we're talking about is -- is visualizing things in that level of detail. It's showing for this 8-high stack visualization how things are moving around as things go up, vertically up the stack. It's a very high-level figure.

///

BY ATTORNEY CHANDLER:

Q. In the proposed spiral structure in Figure 12.3.1 of Exhibit 2007, is the pathway that you're referring to external to the chip?

ATTORNEY ZHONG: Objection to form.

THE WITNESS: Yeah, I guess in this reference, I haven't -- or in the context of this visualization denoted what portions of that pathway may or may not be inside some definition of what the chip itself is.

I mean, there's -- as we can see, connections here to the drivers in a spiral proposal as to how this would be -- how this particular configuration is manufactured at every level of detail, you know, there's some visualization in 12.3.2, but I don't see that this short reference goes into all of that detail.

BY ATTORNEY CHANDLER:

Q. In the proposed spiral structure in Figure 12.3.1 of Exhibit 2007, there is a driver receiver named channel CH0 in the base die?

A. I see that.

Q. And that is -- do you see that?

A. I do.

Q. And that driver receiver named channel

CH0 in the base die has a path connected to the driver receiver that's shown; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like there's a driver here that's connected to the vertical pathway up in the multi-drop, and there are respective drivers here that are also in purple that have a connection.

BY ATTORNEY CHANDLER:

Q. In the proposed spiral structure on the right in Figure 12.3.1 of Exhibit 2007, if you focus on the highlighted path of channel CH0, two of the dies in the stack have a driver receiver coupled to the highlighted path; correct? One near the bottom of the stack and the other towards the middle of the stack?

A. It shows that the driver for the lower CH0 and then the one for CH0 halfway up the stack had drivers that are -- that are highlighted in purple here.

Q. And are they illustrated as being coupled to the path highlighted in purple coming from channel CH0?

A. They look like those dies have drivers which are connected or electrically communicating

here with -- for the -- for those dies with this channel.

Q. In the proposed spiral structure on the right of Figure 12.3.1 of Exhibit 2007, the highlighted path of channel CH0 goes all the way up to the top die in the stack; correct?

A. That's -- looks correct, yes.

Q. But only two of the dies that have drivers and receivers are coupled to the highlighted path and are in electrical communication with the base die; correct?

A. I would say what it is visualizing at a high level is those dies -- or, sorry. The purple highlighted drivers for CH0 have drivers that are connected to, for example, by a pad, to the interconnect here and can electrically communicate with those dies.

Q. And the other dies in the proposed spiral structure in Figure 12.3.1 of Exhibit 2007 are not illustrated as being in electrical communication with the purple highlighted path of channel 0; correct?

A. I believe, again, it's a very high-level figure -- it's intending to show that those dies with the white driver, that that -- there is no

communication happening for those dies with that purple highlighted path.

I know you're probably not at a breaking point, but I could use the restroom when you get to one.

Q. In the proposed spiral structure in Figure 12.3.1 of Exhibit 2007, are the purple tubes part of a TSV?

A. As I recall, they are intended to be part of the spiral P2P TSV structure that's talked about in the first or second paragraphs of the reference as a concept. I don't see that the reference breaks down each of the individual constituent pieces here and labels them. As a concept, I think that's what it's illustrating.

Q. So as a concept, the proposed spiral structure in Figure 12.3.1 of Exhibit 2007 would have TSVs, as indicated by the purple tubes? Is that generally fair?

A. That the spiral is the -- the path that is present in this stack in contrast to the -- the older multi-drop TSV structure, just connecting to every -- to every -- every layer in the stack.

Q. But in both the conventional multi-drop and the proposed spiral P2P, or P2P in

Figure 12.3.1 of Exhibit 2007, they both have TSVs as indicated by the purple tubes; correct?

A. That -- the purple tubes are components in both of these -- in both of these topologies or layouts.

Q. Components of the TSV?

A. Going on the high-level visualization here, I think that sounds right.

ATTORNEY CHANDLER: Okay. Why don't we take a five-minute break.

THE VIDEOGRAPHER: Off the record. The time is 1:57.

(Recess taken from 1:57 p.m. to 2:06 p.m.)

THE VIDEOGRAPHER: Back on the record. The time is 2:06.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, are there any corrections you would like to make to any of your testimony earlier today?

A. I think just one minor thing. I think you were asking about the TSVs earlier and the chips. I was just getting at the figure on the left is a high-level figure. But as we can see, I think, even probably in 12.3.2, these are going

through the various layers here, that we can see at least the columns moving through. That was it. I think we went back and forth on that a bit earlier.

Q. And you're referring to Exhibit 2007, page 2, and the proposed spiral P2P in Figure 12.3.1?

A. That's right. The figure, roughly what we're talking about, 12.3.1.

Q. Could you turn to the Exhibit 1016, which I believe you have previously -- it's the Riho reference. I think I gave it to you at the beginning of the day.

A. I think that's right.

Q. Do you have it in front of you?

A. I just lost track of the number. Which exhibit again?

Q. 1016.

A. Okay. I do.

Q. Take a look briefly at Figure 4 of the Riho reference marked as Exhibit 1016, and then go to paragraph 64 of the Riho reference. And let me know when you're there.

A. Okay.

Q. The second sentence of paragraph 64 of

the Riho reference marked as Exhibit 1016 discloses that DQ TSV 08 is shared by SDRAMs D0 and D8; correct?

A. I see that portion of the sentence, yes.

Q. And Riho also discloses that the circuits on the surfaces of SDRAMs D0 and D8 are in a conductive state with DQ TSV 08; correct?

A. I see that, yes.

Q. Do you agree that Riho is teaching that DQ TSV 08 is in the electrical communication with the circuits of both of SDRAM D0 and SDRAM D8?

A. That those SDRAMs 0 and 8 would -- excuse me -- would be in electrical communication.

Q. With DQ TSV 08; correct?

A. That's correct, yes.

Q. Paragraph 64 of Riho marked as Exhibit 1016, also discloses that the SDRAMs other than D0 and D8 are in a nonconductive state with respect to DQ TSV 08; correct?

A. I see that it says that, yes.

Q. Do you do agree that Riho teaches that DQ TSV 08 is not in electrical communication with circuits on SDRAMs other than SDRAM D0 and D8?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I'm just flipping back to

my declaration for you.

(Witness reviews document.)

THE WITNESS: So it -- going back to Riho, and as I talk about roughly page 153 onward or so in my declaration, that in Riho, there isn't a second group of the -- at least one array die that's not in electrical communication, based on Riho's use of the switches and drivers in its design.

BY ATTORNEY CHANDLER:

Q. So if I understand correctly, in your opinion, DQ TSV 08 is in a nonconductive state with SDRAMs other than D0 and D8 but is still in electrical communication with all of the SDRAMs, including those other than D0 and D8. Is that correct?

A. That -- yes, I'll put us back to roughly 251 in my declaration, that there is electrical communication in Riho between the TSV and, as I say, the TSV and the transistors on the array die, or on the -- you know, the DRAM in Riho.

Q. Paragraph 64 of Riho, marked as Exhibit 1016 also teaches that, quote:

"The data signal DQ TSV 19 and circuits formed at the front service --

surfaces of the SDRAMs D1 and D9 are in a conductive state (i.e. on state) while the data signal DQ TSV 19 is not electrically connected to the SDRAMs other than the SDRAMs D1 and D9," end quote.

Did I read that accurately?

A. Yes, you did, from paragraph 65.

Q. Correct.

A. That sounded correct.

THE COURT REPORTER: I'm sorry?

THE WITNESS: I was saying that sounded correct.

BY ATTORNEY CHANDLER:

Q. Do you agree that Riho teaches that DQ TSV 19 is in electrical communication with the circumstances of both SDRAM D1 and SDRAM D9?

A. That they're -- for DQ TSV 19, there is electrical communication with D1 and D9?

Q. Do you agree that Riho teaches that DQ TSV 19 is not in electrical communication with circuits on SDRAMs other than SDRAM D1 and SDRAM D9?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Can you ask me again about

the specific TSVs and dies you're referring to?
BY ATTORNEY CHANDLER:
Q. Do you agree that Riho teaches that DQ TSV 19 is not in electrical communication with circuits on SDRAMs other than SDRAM D1 and SDRAM D9?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: It is my opinion that the TSV 19 is in electrical communication with DRAMs other than -- if you were asking about D1 and D9. It is also in electrical communication with other --
BY ATTORNEY CHANDLER:
Q. So to be clear, in your opinion, DQ TSV 19 is not electrically connected to SDRAMs other than D1 and D9, but is still in electrical communication with the SDRAMs other than D1 and D9; is that fair?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: That -- what I'm saying in my declaration, for example, even in the paragraph 267 region, is that the TSV, for example, TSV -- DQ TSV 19, in Riho, is in electrical communication with additional DRAMs other than the DRAM D1 and D9. It would be in electrical communication with

all of the -- all the DRAMs in this case.
BY ATTORNEY CHANDLER:
Q. Even though many of those DRAMs are not electrically connected to DQ TSV 19, in your opinion, they are still all in electrical communication with DQ TSV 19; is that fair?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: Perhaps you can clarify. I don't recall using the phrase, quote, "electrically connected" in context to this discussion.
BY ATTORNEY CHANDLER:
Q. I'll use a phrase that Riho uses in paragraph 65 that we read a moment ago.
A. Perhaps I lost my place in 65.
Okay. So Riho -- thank you.
Riho says -- the phrase "not electrically connected to SDRAMs" in his language. But in my assessment, in a -- well, Dr. Wolfe's opinion and his discussion around how the switching in Riho works, that, in fact, all of those SDRAMs are in electrical communication.
Q. So to be clear, in your opinion of Riho, even though DQ TSV 19 is not electrically connected to all of the SDRAMs, in your opinion,

all of the SDRAMs are still in electrical communication with DQ TSV 19; is that fair?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That despite Riho using his language of in paragraph 65, TSV 19 is not electrically connected to the SDRAMs other than the SDRAMs D1 and 9. It is my opinion that they are still, per the language of the '060 patent -- there is still electrical communication.

BY ATTORNEY CHANDLER:

Q. Could you turn to page 136 of your expert declaration marked as Exhibit 2023, and let me know when you're there.

A. Okay.

Q. On page 136 of your declaration marked as Exhibit 2023, you show Figure 5 from Riho marked as Exhibit 1016; correct?

A. That is correct.

Q. In Figure 5 of Riho, marked as Exhibit 1016, there is a TSV715 illustrated on the left side of the figure; correct?

A. Yes.

Q. The TSV715 in Figure 5 of Riho is connected to a switch circuit CS15, which includes two switches called sa and sb; correct?

A. That's -- that's correct.
Q. And Figure 5 of Riho marked as Exhibit 1016, switch sa is on for SDRAM D15, and switch sb is on for SDRAM D7; and all of the other switches shown in that figure are off; correct?
A. I'm just going back to that description in Riho.
(Witness reviews document.)
A. So it looks like that's -- what Riho is describing, at least in part in 72 of Riho, that in Figure 5, the switch sa "is put in an on (conductive) state," and then talks later about, in 73, other switches being "in an off state." So that sounds right.
Q. So, for example, if you look, in Figure 5 of Riho, in SDRAM D14, both switches sa and sb are off for SDRAM D14; correct?
A. It looks like for that SDRAM, Riho switch A and switch B are off in the figure.
(Interruption by the court reporter to clarify the record.)
BY ATTORNEY CHANDLER:
Q. Figure 5 of Riho, marked as Exhibit 1016, shows that, to the right of those

off switches is a circuit labeled L1C2R2; correct?

A. That there is a block in Figure 5's block diagram denoting that.

Q. Figure 5 of Riho shows that to the right of the off switches is a block labeled L1C2R2 circuit; correct?

A. That that's the -- yeah, that's the text in that visualization on the right-hand portion of Figure 5.

Q. Figure 5 of Riho marked as Exhibit 1016 shows that to the right of the off switches is a MOS driver circuit used for read operations; correct?

A. In Figure 5, that's denoted, yes.

Q. And would you pronounce that "moss" driver?

A. Yes, that's fine.

Q. In Figure 5 of Riho, marked as Exhibit 1016, the L1C2R2 circuit to the right of the off switches labeled CS14 is not electrically connected to the TSV715 to the left of the off switches; correct?

A. So the L1C2R2 block here in Riho is a model -- basically what Riho is saying is sort of

a way of modeling the driver circuit here in -- at least in Riho's Figure 5.

Q. And that circuit is on the right of the off switches labeled CS14. It's not electrically connected to the TSV715 to the left of the off switches; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So I would say a couple of things.

One, the L1C2R2 is, as I discuss in the -- in my declaration at 153, is a way that -- page 153 of my declaration is a way that the -- or is how the MOS driver is modeled; and that in Riho, those -- all of these SDRAMs are in electrical communication with the TSV that's on the left-hand side of Figure 5.

BY ATTORNEY CHANDLER:

Q. My question is a little different. So I'm not asking about the SDRAMs in general. Now I'm asking specifically about the L1C2R2 circuit, which I understand is a model of the MOS driver.

So do you understand what I'm focused on specifically now?

A. I understand.

Q. In Figure 5 of Riho, marked as

Exhibit 1016, the L1C2R2 circuit, to the right of the off switches labeled CS14, is not electrically connected to the TSV715 to the left of the off switches; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I think that's what Riho would be saying in the, quote, electrically connected language, at least of Riho's paragraph 65.

BY ATTORNEY CHANDLER:

Q. In Figure 5 of Riho, marked as Exhibit 1016, the L1C2R2 circuit to the right of the off switches labeled CS14, is not in electrical communication with the TSV715 to the left of the off switches; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Are you asking, in my declaration and in my opinion, each one of those DRAM or SDRAMs of Riho is itself in electrical communication with that TSV. The L1C2R2 circuit is a model for -- or a representation of the MOS driver that's part of that SDRAM.

BY ATTORNEY CHANDLER:

Q. Again, I'm trying to be specific to the L1C2R2 circuit, which I understand is a model of

the MOS driver. So I'm not talking about the SDRAM in general. I'm talking about the specific L1C2R2 circuit, which I understand is a model of the MOS driver.

So do you have that in mind? And then I'll ask the question again when you're ready.

A. Sure. Go ahead.

Q. In Figure 5 of Riho marked as Exhibit 1016, the L1C2R2 circuit to the right of the off switches labeled CS14, is not in electrical communication with the TSV715 to the left of the off switches; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would answer that, that in the opinions I've offered in my declaration talk about Riho's switches and the electrical communication regarding the TSV and the SDRAM and the switches.

Perhaps you can point me somewhere in my declaration, but I don't -- if you're asking did I parse out as a given subcomponent of this MOS driver model within the array or the SDRAM of Riho itself in electrical communication, I don't recall parsing things down to sort of the subcomponent level of granularity. But if -- maybe I'm

forgetting a portion of my declaration.
BY ATTORNEY CHANDLER:
Q. I don't think so. And that's why I'm trying to ask you right now.
ATTORNEY ZHONG: It's beyond the scope.
BY ATTORNEY CHANDLER:
Q. So are you still thinking, or should I ask the next question?
A. You can go ahead and ask the next question.
Q. In Figure 5 of Riho, marked as Exhibit 1016, the MOS driver circuit to the right of the off switches labeled CS14 is not in electrical communication with TSV715 to the left of the off switches; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: That I have offered the analysis and opinion in my declaration that the SDRAMs of Riho, Figure 5, themselves in an analysis of the, for example, CS15 switch, are in electrical communication with the TSV on the left-hand side of Riho. I have not offered an opinion one way or the other on the L1C2R2 MOS driver model or components therein. If certain pieces of that -- I'm analyzing this in the lens

of the claims of the '060 and the language of the array die in the '060 and the switch within Riho.
BY ATTORNEY CHANDLER:
Q. So you've not offered an opinion one way or another whether in Figure 5 of Riho marked as Exhibit 1016, whether or not the L1C2R2 circuit to the right of the off switches labeled CS14 is in electrical communication with TSV715 to the left of the off switches; correct? You don't have an opinion to express on that question?
ATTORNEY ZHONG: Objection; form, misstated testimony.
THE WITNESS: Well, if I recall, Dr. Wolfe also pointed out that the L1C2R2 block is just a model of this driver. And I'm performing my analysis at the level of the array -- or the SDRAMs in -- in Riho and the switches within Riho, within those SDRAMs, as being in electrical communication.
I haven't performed a subanalysis of what I understand to be a non-specific circuit model of a MOS driver.
BY ATTORNEY CHANDLER:
Q. You have not offered an opinion about

whether the MOS driver circuit to the right of the off switches labeled CS14 in Figure 5 of Riho marked as Exhibit 1016 is in electrical communication with the TSV715 to the left side of the off switches; correct? You don't have an opinion to express on that question?

ATTORNEY ZHONG: Objection; form, misstated testimony, asked and answered multiple times.

THE WITNESS: I have -- I think there may be a couple of layers to this answer. But the -- my analysis is in regard to the TSV, the switch within Riho, and the SDRAM within Riho in relation to the '060 claim language; and the data port -- I have not gone into the MOS driver model, L1C2R2, that I think Dr. Wolfe and I -- or Dr. Wolfe at least also states is just a model -- and as to whether the components or subsets of representative components in that model are in electrical communication one way or the other.

BY ATTORNEY CHANDLER:

Q. Could you go to Riho Exhibit 1016 and turn to Figure 10. Let me know when you have that in front of you.

A. Okay.

Q. The bottom of Figure 10 of Riho marked as Exhibit 1016 shows a single labeled "RLON" towards the bottom left; correct?

A. I see that, yes.

Q. And then take a look at paragraph 123 of Riho marked as Exhibit 1016, and let me know when you're there.

A. Okay.

Q. Paragraph 123 of Riho, marked as Exhibit 1016, teaches that "the RL output control circuit 95 outputs, as a RLWLON signal, a RLON signal," correct?

A. That looks correct, second or third line -- or second and third line down in that paragraph.

Q. And then paragraph 123 of Riho, marked as Exhibit 1016, goes on to teach, at the top of the next column:

> "The SDRAM ship is connected to the data signal DQ penetrating through electrode (TSV) for a period in which the RLON signal has a logic '1' level. On the other hand, the SDRAM chip is disconnected from this penetrating through electrode (TSV) for a period in

which the RLON signal has a logic '0' level. Accordingly, the load capacitive from this SDRAM chip is in an off state."

Did I read that accurately?

A. I think so, yes.

Q. If you look at the bottom of Figure 10 of Riho, it teaches, that "load capacitance from DQ in chip is off with RLON equal to 'L.' "

Did I read that accurately?

A. Yes. And then continues on "for other than data input/output period."

Q. So the bottom of Figure 10 of Riho is consistent with the portions of paragraph 123 of Riho that we just looked at; correct?

(Witness reviews document.)

A. I would say paragraph 123 of Riho states what it states. I don't recall performing an analysis of this paragraph as to whether it was inconsistent with Figure 10, but the paragraph states what it states.

Q. Both Figure 10 of Riho and paragraph 123 of Riho, marked as Exhibit 1016, states that when the SDRAM chip is disconnected from the TSV, the load capacitance from the SDRAM chip is off;

correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I see that Riho says what it says, top of page 10.

"The SDRAM chip is disconnected from this penetrating through electrode (TSV) for a period in which the RLON signal has a logic '0' level. Accordingly, the load capacitance from this SDRAM chip is in an off state."

BY ATTORNEY CHANDLER:

Q. And that's consistent with the bottom of Figure 10, where Riho states: Load capacitive from DQ in chip is off with RLON equal to 'L,'" L being an abbreviation for low or 0; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like the paragraph 123, as it's written, is at least partially in the context of Figure 9 -- 9A and B, based on 121. Figure 10 may be visualizing certain aspects of the signals in there.

BY ATTORNEY CHANDLER:

Q. Figure 10 is consistent with the discussion in paragraph 123 of Riho, correct, with respect to --

ATTORNEY ZHONG: Objection; form.
BY ATTORNEY CHANDLER:
Q. -- with respect to the RLON signal and the text at the bottom of Figure 10 with respect to the RLON signal?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: I would say I don't recall -- well, I don't recall addressing this figure in my declaration. But sitting here right now, I don't see any internal inconsistencies within Riho itself around the Figure 10 and what's perhaps being described in paragraph 123 of Riho.
BY ATTORNEY CHANDLER:
Q. Could you turn to Figure 8A of Riho marked as Exhibit 1016. Let me know when you're there.
A. Okay.
Q. At the top of Figure 8A of Riho, marked as Exhibit 1016, there is a, quote, output load disconnect control, end quote.
Is that right?
A. I see that, yes.
Q. Figure 8A of Riho points to RLWLON as the, quote, output load disconnect control, end quote; is that fair?

A. Let me check for you.

(Witness reviews document.)

A. Okay. In 110 it looks like it's describing that SDRAM's D15 and D7 respectively have the WL -- sorry -- RLWLON signal.

Q. And Figure 8A of Riho draws an arrow to RLWLON to indicate that that is the, quote, output load disconnect control, end quote? Is that a fair description of the Figure 8A?

A. I see that text within 8A, at least within the figure.

Q. And you see the arrow as well pointing to RLWLON?

A. It looks like that's what it's visualizing, yes.

Q. And Figure 8A of Riho shows that the RLWLON is connected to both switches sa and sb; correct?

A. It looks like within Figure 8A, the RLWLON arrow is going to sa and sb.

Q. And paragraph 123 of Riho states that the RLWLON can be an RLON signal, as we previously discussed; correct?

A. If I'm following, it says in 123:

"The RL output control circuit 95

outputs, as an RLWLON signal, a RLON signal."

Q. And paragraph 123 of Riho goes on to teach, at the top of the column, that the RLON signal controls whether or not the SDRAM chip is connected to the TSV; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It says at the top of the column:

"On the other hand, the SDRAM chip is disconnected from this penetrating through electrode (TSV) for a period in which the RLON signal has a logic '0' level. Accordingly, the load capacitive from this SDRAM chip is in an off state."

BY ATTORNEY CHANDLER:

Q. Both Figure 8A of Riho and paragraph 123 of Riho, marked as Exhibit 1016, teach that when the SDRAM chip is disconnected from the TSV, the load from the SDRAM chip is disconnected; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: No. It says at the top of the column or page:

"The SDRAM chip is disconnected from this penetrating electrode" -- sorry -- "disconnected from this penetrating through electrode (TSV) for a period in which the RLON signal has a logic '0' level. Accordingly, the load capacitive from this SDRAM chip is in an off state."

BY ATTORNEY CHANDLER:

Q. And the top of Figure 8A refers to that as the "output load disconnect control"; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like, within the confines of Figure 8A, there is a W -- sorry -- RLWLON generating circuit within RLWLON signal or output arrow; and there's an arrow pointing to that, saying "output load disconnect control."

I don't see the phrase "Output load disconnect control" in this paragraph 123 that we've been talking about.

BY ATTORNEY CHANDLER:

Q. That phrase is in Figure 8A, though; correct?

A. It is itself in -- in Figure 8A; that's right.

Q. Could you turn to page 166 of your expert declaration marked as Exhibit 2023, and let me know when you are there.

A. Okay.

Q. At the top of page 166 in Exhibit 2023, you created two figures, one labeled "without transmission gate" on the left side and the other labeled "with transmission gate" on the right side; correct?

A. That's correct.

Q. Am I correct that the two figures on the top of page 166 of Exhibit 2023 are intended to be the same except for the addition of the transmission gate on the figure on the right?

A. That sounds right. The difference I point out is primarily pointing to that transmission gate.

(Interruption by the court reporter to clarify the record.)

Q. On the figure on the right side of page 166 of Exhibit 2023, the transmission gate is the circuitry connected to the label GATE_CRTL; is that correct?

A. That's right. The GATE_CRTL is going to the -- to the transmission gate.

Q. If you turn back a few pages to paragraph 258 of your declaration marked as Exhibit 2023, you refer to what you call, quote, huge transistors at the end of that paragraph; correct?

A. That is correct, yes.

Q. And then if we go back to page 166 of Exhibit 2023, in the circuit that you've drawn on the left side, which transistors, in your opinion, are the, quote, huge transistors?

A. That these would be the transistors here driving signals to the TSV. So they would be the DP and DN within the figure.

Well, I'm sorry. As I talked about the -- there would be the transistors doing the driving. And, also, as I mentioned in 266, the double-sized transistors here pertain to those at the gate as well.

Q. I'm a little confused. So on the figure on the left-hand side of page 166 of Exhibit 2023, which are the transistors that, in your opinion, are the, quote, huge transistors?

A. In the figure on the left, it's going to be, as I discussed earlier, those driving the outward signal towards the TSV. So it would be

the DP, DN on the left-hand side.

Q. If you could turn back to Figure 5 of Riho marked as Exhibit 1016, and let me know when you're there.

A. Okay.

Q. In your opinion, where would the, quote, huge transistors be located in Figure 5 of Riho?

A. I don't know that I've assigned in my example where in the Riho Figure 5 the high-level model they may or must sit. But they would be used in driving the signal, just as I say in my declaration, out to -- driving out to the TSV on the left.

Q. In your opinion, would the, quote, huge transistors in Figure 5 of Riho be to the right of the switches labeled sa and sb?

ATTORNEY ZHONG: Objection.

THE WITNESS: That sounds like a sort of design -- or implementation-specific question. I mean, in -- in Riho's Figure 5, the chip internal circuit there, it's showing everything from switches to inductors to read-only memory components.

///

BY ATTORNEY CHANDLER:

Q. If I understand your reasoning from page 166, you're saying that the output drivers are what are the large transistors -- or the huge transistors, rather; is that correct?

A. That the -- going back to paragraph 258, that output stage is going to use the, quote, huge transistors.

Q. In Figure 5 of Riho, do the MOS drivers for read commands have an output stage that, in your opinion, would have, quote, huge transistors?

A. What I'm discussing about Riho in this section is this -- really responding to Dr. Wolfe's opinion on Riho's -- I think Riho and Dr. Wolfe's use of the transition gate characterization of the switches and how that impacts things.

I don't know that I've performed an analysis to where -- if you're asking where the output transistors need to or can't sit within the design, I haven't sort of performed that analysis. A lot of this figure is really just a high-level model of things.

Q. To be clear, are you able to explain to

me, in Figure 5 of Riho, where the, quote, huge transistors would be located.

A. I think, conceptually, they would be part of the SDRAM in Riho as part of the functionality driving the signal to the TSV on the left. In Riho's Figure 5 sort of functional illustration, I haven't assigned them to a -- you know, a specific block or not block; but they're -- they're part of the -- what's driving signals here.

Q. Are they part of the MOS driver, or memory read shown on the right side, Figure 5 of Riho?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say again that MOS driver block, the L1C2R2, is a model.

The transistors themselves used for the driving of the signal would be part of this overall portion of Riho as to drive a signal to the TSV -- in Figure 5, the TSV715.

ATTORNEY CHANDLER: Why don't we take a short break.

THE VIDEOGRAPHER: Off the record. The time is 3:05.

(Recess taken from 3:05 p.m. to

3:18 p.m.)

THE VIDEOGRAPHER: Back on the record. The time is 3:18.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have any corrections or clarifications you would like to make to your testimony so far?

A. Not that I recall, no.

Q. Could you please turn to Exhibit 1015, which is Exhibit I gave to you at the beginning of the morning, U.S. Patent Number 8,041,881, the Rajan, R-A-J-A-N.

A. Okay.

Q. And could you turn to Column 2 of Rajan.

Rajan, marked as Exhibit 1015, teaches at Column 2, lines 22 through 25, that:

"Digital memories come in several types, such as DRAM, SRAM, flash memory, EE-PROM, and so forth."

Correct?

A. Let me pause for a second. You said Exhibit 1015?

Q. Yes.

A. And Column 2.

Q. Yes, lines 22 through 25.

ATTORNEY ZHONG: Objection; form.

BY ATTORNEY CHANDLER:

Q. I apologize. Column -- sorry. Column 1, lines 22 through 25.

So be clear, Rajan teaches at Column 1, lines 22 to 25, that:

"Digital memories come in several types, such as DRAM, SRAM, flash memory, EE-PROM, and forth."

Correct?

A. It looks like it's saying there are different types of these memories, such as the dynamic random access memory, static random access memory, flash memory, et cetera, in the background of the -- it's like in the background of the art.

BY ATTORNEY CHANDLER:

Q. Could you turn to Figure 4 of Rajan, marked as Exhibit 1015. Let me know when you're there.

A. Okay.

Q. Figure 4 of Rajan shows a buffered stack of memory circuits; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So Figure 4 in Column 2 is

described as, quote:

"Shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses."

BY ATTORNEY CHANDLER:

Q. The stack in Figure 4 of Rajan includes a buffered chip 413 and four memory chips labeled 417A through 417D; correct?

A. So Figure 4 is described as the buffered chip 413 interfaced to a host system, and it's coupled to DRAM chips 417A through D.

Q. And you're reading from Column 5 between lines 36 and 43, is that correct, of Rajan marked as Exhibit 1015?

A. That's correct.

Q. Figure 4 of Rajan marked as Exhibit 1015 shows data bus 415A is in electrical communication with memory chips 417A and 417B and is not in electrical communication with memory chips 417C and 417D; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: So the way Rajan describes it is -- I'm in line 40 of Column 5. There's a plurality of shared data busses, 415A and B; and each of the busses has two or more DRAM chips

coupled to it.
BY ATTORNEY CHANDLER:
Q. And then the Figure 4 itself illustrates data busses 415A and 415B, and Figure 4 illustrates the data bus 415A is in electrical communication with memory chips 417A and 417B and is not in electrical communication with memory chips 417C and 417D; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: No. That's -- Rajan doesn't use that language. It's just showing -- Rajan is just showing here that you've got this buffer chip that talks to a host system. And you've got a data bus 415A and 415B. And those -- in this figure, those data busses are connected to these different DRAM chips.
BY ATTORNEY CHANDLER:
Q. In fairness, Figure 4 of Rajan draws the data busses 415A and 415B; correct?
A. In this figure, yes, they're shown in a specific way.
Q. And neither Figure 4 of Rajan nor any of the text in Rajan shows data bus 415A having any connection to memory chips 417C and 417D; correct?

A. I would phrase it that Figure 4 is showing data bus 415A goes to one place, and data bus 415B goes to another place.

Q. And those two places, they're distinct from each other. They don't overlap; right?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: The 415A is connected to Rajan's DRAM chips, the 2 DRAM chips, 415A and 415B.

BY ATTORNEY CHANDLER:

Q. And 417B?

A. That's correct. Thank you.

And data bus 415B is connecting to Rajan's DRAM chip 417C and 417D.

Q. And not vice versa; right? So data bus 415A is not shown as being connected to 417C or 417D; and data bus 415B is not shown as being connected to either 417A or 417B; correct?

A. That's not visualized here in Figure 4. It's just two busses that go two different places.

Q. When you say "that's not visualized," you're agreeing with what I am saying, right, as opposed to trying to disagree with what I'm saying?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say the figure stands on its own, that there's two busses, 415A and 415B; and one goes to two of Rajan's DRAM chips and one goes to -- in this figure, another two Rajan's DRAM chips.

BY ATTORNEY CHANDLER:

Q. And a person of ordinary skill in the art would be able to understand Figure 4 of Rajan, marked as Exhibit 1015; correct?

A. In -- taking in the context of Rajan as a reference, yes.

Q. And a person of ordinary skill in the art, looking at Figure 4 of Rajan, marked as Exhibit 1015, would understand that data bus 415A is not connected to memory chips 417C and 417D; correct?

A. That in Figure 4, the bus 415A doesn't have a path to 417C and 417B.

Q. And it doesn't have any way of electrically communicating from data bus 415A to 417C or to 417D; correct, as shown Figure 4?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't think Rajan uses the phrase "electrically communicating." That's a phrase from the '060 patent itself.

BY ATTORNEY CHANDLER:

Q. I understand. I'm trying to get at what a person of ordinary skill in the art would understand from the teachings of Rajan. Do you understand what I'm asking is not necessarily whether Rajan uses the phrase "electrical communication." It's whether a person of ordinary skill in the art would see any electrical communication disclosed by Figure 4 of Rajan between data bus 415A and the memory chips 417C and 417D.

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say a person of skill reading Rajan and the description of Figure 4 would interpret it as there's wires going from -- the data bus 415A that connect to 417A and 417B; and there's wires that go from 417 -- from the data of -- or there's wires compromising data bus 4 -- 415B going to 417C and then to 417D.

BY ATTORNEY CHANDLER:

Q. And in Figure 4 of Rajan, there's no teaching of wires going from data bus 415A to either 417C or to 417D; correct?

A. I -- I don't recall that Rajan describes Figure 4 that way, no.

Q. Are you trying to disagree with me?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: What I'm saying is I don't -- the -- I don't recall Rajan saying something in its description of Figure 4 that there are wires not visualized for bus 415A going somewhere else.
BY ATTORNEY CHANDLER:
Q. Figure 4 of Rajan marked as Exhibit 1015 shows that the data bus 415B is not connected to 417A or to 417B; correct?
A. That -- that sounds right. Data bus 415B is connected to Rajan's DRAM chips, just 417D and 417C.
Q. Could you turn to Column 15 of Rajan, and let me know when you're there.
A. Okay.
Q. Column 15 of Rajan, marked as Exhibit 1015, at lines 2 through 9, teach that:
"The physical memory circuits employed in practicing this invention may be any type of memory whatsoever."
Correct?
A. I see that.
Q. For example, Rajan teaches that his

invention can be employed using DDR3 DRAM memory devices; correct?

A. That it mentions as a type of memory, DDR3 DRAM is one that's listed.

Q. Rajan also teaches that his invention can be employed using SGRAM memory devices; correct?

A. That is -- well, SGRAM is a type of memory that it contemplates.

Q. Rajan also teaches that his invention can be employed using NAND flash memory devices; correct?

A. I see NAND flash listed in this section as well.

Q. Rajan teaches that his invention can be employed using PSRAM memory devices; correct?

A. I see that listed as well.

Q. And as we saw back in Column 1 of Rajan, Rajan also teaches that a type of memory device that was known was SRAM; correct?

A. In Column 1, Rajan mentions that digital memories come in different types. One flavor is SRAM, static random access memory.

Q. In Column 15, lines 10 through 12, of Rajan, marked as Exhibit 1015, Rajan teaches that

the stacked memory devices "may be coupled to any type of memory module, including DIMM, R-DIMM, SO-DIMM, FB-DIMM, unbuffered DIMM," et cetera; correct?

A. I see that statement, yes.

Q. In Figure 4 of Rajan marked as Exhibit 1015, the buffer chip at the bottom of that figure receives address, control, clock, and data signals from the host system; is that fair?

A. That those signals or signals of that kind are coming from the host 404.

Q. That's shown in Figure 4 of Rajan?

A. The host system 404 is shown at least in Figure 4, yes.

Q. Is showing signals going from the host system 404 labeled address, control, clock, and data to the buffer chip 413 in Figure 4 of Rajan; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like it's talking -- I'm going back to Column 5. It says:

"Figure 4 illustrates another embodiment of a system 411, in which buffer chip 413 is interfaced to a host system 404 and is coupled to the DRAM

chips 417A through D."

BY ATTORNEY CHANDLER:

Q. And in Figure 4, the host system 404 is sending address, control, clock and data signals to the buffer chip? Is that a fair interpretation of Figure 4?

A. That those types -- those are types of signals that are coming in this case from the host system the way the data signals -- the data arrow is bidirectional because data would go back to the host in some cases.

Q. In Figure 4 of Rajan, marked as Exhibit 1015, the buffer chip uses as shown by 419 on the left, a shared address, control and clock bus to control the memory chips; correct?

A. That's the way -- one moment. I think I'm sneezing.

That's the way it's described in Column 5, that the -- excuse me -- there is a shared address, control and clock bus 419 in this figure.

Q. And that shared address, control and clock bus 419 connects to all of the memory devices 417A through 417D; correct?

A. In Figure 4, that shared bus is going to

each of the DRAM chips of Rajan's Figure 4.

Q. In Figure 4 of Rajan, marked as Exhibit 1015, the shared address, control and clock bus 419 is separated by the buffer chip 413 from the address, control and clock signals coming from the host system 404; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't recall that Rajan uses the word "separated." But as Figure 4 shows, there are address, control, clock and data signals from a host. And then there are address, control and clock sent specifically over the shared bus 419.

BY ATTORNEY CHANDLER:

Q. Coming from the buffer chip 413?

A. The --

ATTORNEY ZHONG: Objection; form.

THE WITNESS: The address, control and clock of shared bus 419 look to be coming -- that arrow in Figure 4 is denoting them coming out of the buffer chip.

BY ATTORNEY CHANDLER:

Q. In Figure 4 of Rajan, marked as Exhibit 1015, the buffer chip 413 uses two data busses, 415A and 415B, to communicate data with

the memory chips 417A through 417D; is that correct?

THE COURT REPORTER: Did you say B as in "boy" or D as in "dog"?

ATTORNEY CHANDLER: D as in "dog."

THE COURT REPORTER: Thank you.

THE WITNESS: Can you ask me again? I lost track of your numbering there.

BY ATTORNEY CHANDLER:

Q. In Figure 4 Rajan, marked as Exhibit 1015, buffer chip 413 uses two data busses, 415A and 415B [sic] to communicate data with the memory chips; correct?

A. That -- that sounds right. The -- the -- what Rajan calls the shared data busses, 415A and B, are, as Rajan says, coupled to the DRAM chips that you see denoted by the arrows.

Q. And in Figure 4 of Rajan, marked as Exhibit 1015, the buffer chip 413 is between the data signals to and from the host system and the data busses 415A and 415B; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: In the way Figure 4 is illustrated, I suppose at this level of abstraction that's fair. There's a block 413

called buffer chip that sits in between these signals from the host going up, and then there's shared busses visually above the buffer chip going to the various DRAM chips in Rajan.

BY ATTORNEY CHANDLER:

Q. Rajan, marked as Exhibit 1015, never uses the words "wire bond" or "wire bonding"; correct?

A. So if I recall, just in a quick search, this Rajan reference itself doesn't seem to use the exclusive phrase "wire bond."

Q. And Rajan, marked as Exhibit 1015, never states that the connections between the buffer chip and the memory chips are limited to wire bonding; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't -- since Rajan doesn't use the explicit phrase "wire bond," I don't recall one way or the other what it says in regard to that. I don't recall addressing this issue in my declaration for this IPR.

At the time that was -- at the time of Rajan, the way certain things were done.

BY ATTORNEY CHANDLER:

Q. Can you look at Exhibit 1011, which is

the other Rajan reference referred to as Rajan '137.

A. Okay.

Q. And look at paragraph 50 of Rajan '137. Do you have that in front of you?

A. I do, just now.

Q. Paragraph 50 of Rajan 137, marked as Exhibit 1011, teaches that the electrical connections between the buffer chip and the stack of memory chips may be configured in any desired manner; correct?

A. No. It says the electrical connections between the buffered chip and the stack of DRAM circuits may be configured in any desired manner.

Q. Are DRAM circuits memory chips?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: You'd have to be more specific. It looks like this reference talks about DRAM circuits. I believe the other Exhibit 1015 Rajan reference mentions DRAM circuits as well.

BY ATTORNEY CHANDLER:

Q. And are DRAM circumstances an example of a memory chip?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I'd have to look in a specific context.

BY ATTORNEY CHANDLER:

Q. In the context of Rajan '137, are DRAM circuits an example of memory chips?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say the Rajan reference talks about DRAM circuits, even this paragraph and data signals being wired in certain ways. I haven't performed an analysis in this -- in this IPR as to whether in given references, Rajan's DRAM circuit is a memory -- I think your question was a memory chip in another reference or something like that.

BY ATTORNEY CHANDLER:

Q. The acronym TSV stands for through-silicon via; is that correct?

A. That's correct.

Q. By 2011, TSVs were a known way to provide electrical connection between stacked chips; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That by 2011, there were papers out there talking about the use of TSVs, different ways to possibly use them for different

kinds of electronic devices, I would say.
BY ATTORNEY CHANDLER:
Q. In paragraph 50 of Rajan '137, marked as Exhibit 1011, and it states that:
"The electrical connections between the buffer chip 202 and the stack of DRAM circuits 206A through D may be configured in any desired manner."
ATTORNEY ZHONG: Objection; form. Misreading the text.
BY ATTORNEY CHANDLER:
Q. Did I read that accurately?
A. Sorry. I didn't hear a question.
I'm not sure that you did. It says:
"The electrical connections between the buffer chip 202 and the stack of DRAM circuits 206A through D may be configured in any desired manner."
Q. By 2011, would a person of ordinary skill in the art reading paragraph 50 of Rajan '137, marked as Exhibit 1011, been able to configure the electrical connections between the buffer chip 202 and the stack of DRAM circuits 206A through D with a TSV, if that was their desire?

ATTORNEY ZHONG: Objection; form. Did you say electrical communication or electrical connection?

ATTORNEY CHANDLER: Electrical connection.

ATTORNEY ZHONG: Okay. Because the transcription says "electrical communication."

THE WITNESS: I don't recall Rajan talking about the use of TSVs in its description. And the -- so I haven't performed that analysis in this -- in this IPR. Rajan is typically talking about -- or he's talking about these DRAM circuits that use a wired solution, an external wired solution.

BY ATTORNEY CHANDLER:

Q. But Rajan '137 in paragraph 50 does not exclude the use of TSVs; is that fair?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say this paragraph is talking about DRAM circuits. I don't see that it's talking about TSVs.

BY ATTORNEY CHANDLER:

Q. So there's nothing in this paragraph or anywhere is Rajan '137 that excludes the use of TSVs; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Well, I would say to the extent DRAM circuits don't use a TSV solution, one wouldn't consider TSVs with that type of implementation.

BY ATTORNEY CHANDLER:

Q. And Rajan '137 never says don't use TSVs; right?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't recall Exhibit 1011 mentioning TSV at all.

BY ATTORNEY CHANDLER:

Q. If you turn back to Exhibit 1015, the other Rajan reference, and go to Figure 7.

A. Okay.

Q. Figure 7 of Rajan, marked as Exhibit 1015, teaches storing information associated with a first operation, and then using that stored information as part of a second operation; correct?

A. That seems like a way -- if I recall what you said, at the top of Column 6 in 3 of Rajan -- I'm sorry, Exhibit 1015, Figure 7 illustrates one embodiment of a method 700 for storing at least a portion of the information

received in association with a first operation for use in performing a second operation.

Q. Could you turn to Figure 9 of Rajan. Let me know when you're there.

A. Okay.

Q. Figure 9 of Rajan marked as Exhibit 1015, is described in Column 9 at lines 22 to 31, among other places; correct?

A. That looks like it's describing parts of Figure 9; that's correct.

Q. And Figure 9 of Rajan, marked as Exhibit 1015, the physical DRAM chips have a CAS latency of four clock cycles, but the buffer chip emulates DRAM having a CAS latency of six clock cycles; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Let me just read this section.

So I'm at line 26 of Column 9.

"The DRAM chips have a native CAS latency of 4 four clocks, and the total latency through the buffer chip is two clocks. The buffer chip" -- I'm skipping the parens.

"The buffer chips emulates a DRAM

having a six clock CAS latency."
BY ATTORNEY CHANDLER:
Q. Okay. So it's consistent with the question I asked?
A. It looks like the buffer chip is emulating the DRAM with a six clock CAS latency.
Q. Even though the physical DRAM has a CAS latency of four clock cycles; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: That the DRAM chips in this -- as described in this paragraph have a native CAS latency of four clocks.
BY ATTORNEY CHANDLER:
Q. So in this example of Rajan, marked as Exhibit 1015, the buffer chip is interfacing with the system memory controller on the basis of a CAS latency of six clock cycles, and then the buffer chip is interfacing with the DRAM chips on the basis of CAS latency of four clock cycles; is that fair?
A. I would phrase it that the DRAM chips of this paragraph have the native latency of four clock cycles, and the buffer chip is performing emulation of a DRAM -- emulation and presentation to the host of a DRAM having six clock cycles.

Q. So from the perspective of the system memory controller and the host computer, in this Figure 9 example of Rajan marked as Exhibit 1015, the CAS latency appears to be six clock cycles as a result of the emulation by the buffer chip; is that fair?

A. That -- that sounds right, that that's the host -- the host view of the CAS latency.

Q. Could you turn to Figure 11 of Rajan, marked as Exhibit 1015, and let me know when you're there.

A. I'm there.

Q. Figure 11 of Rajan, marked as Exhibit 1015, is described, for example, at Column 10, lines 11 through 27; correct?

A. That looks right, yep.

Q. Figure 11 of Rajan, marked as Exhibit 1015, teaches that the system memory controller expects a right CAS latency of five clock cycles as stated in Column 10 around lines 23 through 24, and is also shown in Figure 11; correct?

A. That it's -- it's generally saying the memory controller expects that right CAS latency of five clocks.

Q. But in the example of Figure 11 of Rajan, the -- the actual CAS latency of the DRAM chips is three clock cycles, as stated at Column 10, line 21, and as shown in Figure 11; correct?

A. That looks right. It says:

"The DRAM chips receive the write operation at T3 and have a write CAS latency of three clocks."

Which looks like what the figure is showing.

Q. So to make the timing work properly, the buffer chip in this example of Figure 11 of Rajan adds an extra two clock cycles of delay to the write operation as stated at Column 10, line 18, so that the data arrives at the time expected by the DRAM chips, which in this example is a time t6; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It says:

"Because those chips receive the write operation at T3 and they have a right CAS latency of three clocks, they are expecting to receive the write data at t3 plus 3," which is t6.

BY ATTORNEY CHANDLER:

Q. And Column 10, lines 26 through 27, of Exhibit 1015 explain that in this Figure 11 example of Rajan, that the timing problem for this write operation is solved by Rajan's buffer chip adding those two extra clock cycles; correct?

ATTORNEY ZHONG: That in line 25 it says:

"After a one clock delay through the buffer, the write data arrives at those DRAM chips at t5 plus 1, or t6."

And that's the particular timing issue that's being addressed in this -- this Figure 11.

BY ATTORNEY CHANDLER:

Q. And just to be clear, though, the buffer has a one clock cycle delay; but then it also adds another two clock cycles of delay for the write operation as stated as Column 10, line 18, in this example of Figure 11; correct?

A. That sounds right. The end of this paragraph talks about a one cycle delay through the buffer; and at line 18, that the buffer chip adds an extra two clocks of delay to the write operation.

Q. Could you turn to Figure 12 of Rajan, and let me know when you're there.

A. Okay.

Q. Figure 12 of Rajan, marked as Exhibit 1015, is described, for example, at Column 10, lines 34 through 60; correct?

A. That looks right. At least that section refers to Figure 12.

Q. Figure 12 of Rajan is a --

ATTORNEY ZHONG: I'm going to object to this line of questioning as being outside the scope of direct.

But you can ask the question. Go ahead.

BY ATTORNEY CHANDLER:

Q. Figure 12 of Rajan, marked as Exhibit 1015:

"Is a timing diagram illustrating the operation of an advanced memory buffer, abbreviated AMB, in an FB-DIMM, which may be designed to send write data earlier to the buffered stacks instead of delaying the write address and operation, as was done in Figure 11."

Correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like the Figure 12 is talking about an illustration pertaining to an FB-DIMM and the AMB of the FB-DIMM.

BY ATTORNEY CHANDLER:

Q. And that AMB, according to Column 10, starting at line 34, of Rajan marked as Exhibit 1015, may be designed to send the write data earlier to the buffered stacks instead of delaying the write address and operation, as was done in Figure 11; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I see that --

ATTORNEY ZHONG: Outside the scope of direct.

THE WITNESS: I see that language in the first sentence of the paragraph.

BY ATTORNEY CHANDLER:

Q. Column 10, lines 44 through 47, of Exhibit 1015 explain that another solution is for the memory controller itself in the host to send the write data early to compensate for the delay caused by Rajan's buffer chip; correct?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: It talks about another

embodiment, and here the memory controller can send write data early. And it's -- it says, as you read, to compensate for J clocks of cumulative inherent delay caused by the buffer chip.

BY ATTORNEY CHANDLER:

Q. Either way, the result taught by Rajan in Column 10, lines 57 through 58, of Exhibit 1015 is that the write data arrives exactly when the DRAM expects it; correct?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: It says, starting at 55: "After the inherent delay 1203 through the buffer chip, the write data arrive at the DRAM at t4, exactly when the DRAM expects it -- specifically."

BY ATTORNEY CHANDLER:

Q. And the reason that the write data arrives exactly when the DRAM expects it in the example of Figure 12 of Rajan is because the AMB buffer can be designed to send the write data earlier; or, in the alternative, as described in Column 10 at lines 44 through 47, the memory controller can send the write data earlier; correct?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: That generally what this section is talking about is making sure a piece of data shows up at Rajan's DRAM at the exact point in time it's supposed to. And one way to do that is the -- is based with the buffer chip adjustment, and one is with the -- I'm sorry -- AMB adjustment and so forth.

BY ATTORNEY CHANDLER:

Q. And the other way is with the memory controller making the adjustment; correct?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: Similarly, for this example of write data arriving at a DRAM in Rajan, you can adjust -- make an adjustment in the memory controller for this small example in Figure 12.

BY ATTORNEY CHANDLER:

Q. If you turn to Figure 13 of Rajan, and let me know when you're there.

A. Okay.

Q. Figure 13 of Rajan, marked as Exhibit 1015, is described, for example, at Column 10, line 61, through Column 11, line 11; is that correct?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: It looks like that section

of Exhibit 1015 focuses on this figure.
BY ATTORNEY CHANDLER:
Q. Figure 13 of Rajan, marked as Exhibit 1015, illustrates bus conflicts that can be caused by delayed write operations resulting in collisions; correct?
ATTORNEY ZHONG: Objection; form, scope.
THE WITNESS: If looks like Figure 13 is described as illustrating bus conflicts which can be caused by what it called delay write operations.
BY ATTORNEY CHANDLER:
Q. And if you keep reading that paragraph, the result of those bus conflicts can include collisions; correct?
ATTORNEY ZHONG: Objection; form, scope.
THE WITNESS: It says, at the very bottom of Column 10, second-from-the-last line:
"Because the memory controller is unaware of this delay, it may schedule subsequent operations such as activate or precharge operations. And those may collide with delayed writes on the address bus to Rajan's DRAM chips."
///

BY ATTORNEY CHANDLER:

Q. And would it be fair to say that, in general, collisions are bad, something that you would try to avoid?

A. In this context, it looks like there's collisions happening from multiple types of commands. It looks a write and an activate or a write and precharge, and you don't want to do that. That's something to avoid, I would say.

Q. Figure 14 of Rajan teaches how to avoid such a collision, as explained, for example, starting at Column 11, line 12, of Exhibit 1015; is that fair?

ATTORNEY ZHONG: Objection; form, scope.

THE WITNESS: It looks like Figure 14 says it's a timing diagram illustrating methods of avoiding such collisions. These look like command collisions of things like activate commands, read and write commands.

BY ATTORNEY CHANDLER:

Q. For example, Rajan teaches at Column 11, lines 23 through 25, of the Exhibit 1015 that:

"The buffer chip can delay the activate and precharge operations to

avoid collisions in a manner that's transparent to the host system."

Correct?

A. That in this certain example, starting in the description on line 20, if the DRAM chips are what it says, 4 clock cycles each, then the buffer chip tells the hosts that there are six clock cycles, and then delays -- the buffer chip delays various activate and precharge commands or operations to, it looks like, avoid collisions on the command side.

Q. Could you go to your expert declaration and turn to page 97, and let me know when you're there.

A. Okay.

Q. At the bottom of page 97 of your expert declaration marked as Exhibit 2023, in the last sentence, you express the opinion that, quote:

"The presence of significant load to a TSV attributable to a disabled buffer that is described as not electrically coupled to the TSV confirms that the buffer is still in electrical communication with the TSV," end quote.

Did I read that accurately?

A. Yes.
Q. And is that your opinion?
A. In the context of this paragraph, yes.
Q. Your opinion is that a disabled buffer that is not electrically connected to a TSV is still in electrical communication with the TSV; is that correct?
A. That the -- the load to a TSV from a disabled buffer that's, as you read a moment ago, described as not electrically coupled to the TSV, confirms that the buffer is still in electrical communication.
Q. And you relied upon that understanding in forming your validity opinions; correct?
A. In -- in this -- in this IPR, yes.
(Exhibit Number 1024 was previously marked for identification.)
BY ATTORNEY CHANDLER:
Q. Please pull up Exhibit 1024 to Ruckerbauer -- also, I'll put it in the chat because I don't recall if I gave it to you previously. And let me know when you got it.
A. Okay.
Q. Go to Column 9, please.
A. All right.

Q. In Ruckerbauer, marked as Exhibit 1024 at Column 9, lines 51 through 52, the reference identifies the first external data path 112A as a TSV, and also identifies the second external data path 112B as a TSV; correct?

A. That is what it says in the section, yes.

Q. And Figure 5A of Ruckerbauer also shows those two TSVs on the left side of the figure, again, as 112A and 112B; correct?

A. That's correct in Figure 5A.

Q. The bottom of Column 9 through the top of Column 10 of the Ruckerbauer reference marked as Exhibit 1024 describes two bidirectional buffers, 10A and 10B, where only one of the bidirectional buffers, 10A or 10B, electrically couples the memory array data terminal to the TSV; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It says at 66 -- well, let me back up for you.

At 63:

"It may be noted that the first bidirectional buffer is physically connected to the first external data

path 112a as well the second bidirectional buffer 10b, physically connected to the second external data path 12b [sic]. However, only one of the bidirectional buffers 10a or 10b electrically couples to the memory array data terminal to the associated external data path."

BY ATTORNEY CHANDLER:

Q. I think you slightly misquoted it. You said it "couples to the memory array data terminal," but the text couple says "couples the memory array data terminal to the associated data path"; correct?

A. That's right. It does say that.

Q. So at the bottom of Column 9 to the top of Column 10 of Ruckerbauer, marked as Exhibit 1024, the teaching is that only one of the bidirectional buffers, 10A or 10b, electrically couples the memory array data terminal to TSV 112a or 112b; correct?

A. To the associated external data path, which in this context is the 112a and 112b.

Q. Which are TSVs, correct, as we discussed up on line 51?

A. That's right. They're labeled as -- the first external data path TSV and a second external data path TSV.

Q. So in this example, one of the bidirectional buffers is electrically coupled to the TSV while the other bidirectional buffer is not electrically coupled to the TSV, according to Ruckerbauer, marked as Exhibit 1024; correct?

A. That it -- Ruckerbauer is describing only one of these bidirectional buffers, 10a or b, are electrically coupled -- or electrically couples the memory array data terminal to that external TSV. And it does it using a signal for the -- to the buffers.

Q. In your opinion, when the bidirectional buffer is not electrically coupled to the TSV in the Ruckerbauer reference marked as Exhibit 1024, is that bidirectional buffer in electrical communication with the TSV?

A. That's correct, yes.

Q. So even if the supply voltage to the bidirectional buffer is turned off, in your opinion, that bidirectional buffer is still in electrical communication with the TSV; correct?

A. That -- that's right. In Column 10 at

the very top, it's saying -- Ruckerbauer is saying:

"This may be achieved by providing an enable signal to the bidirectional buffer to be used or by any other appropriate measure, for example, by switching only the buffers to be used to the supply voltage or the like."

But, in this case, we would still have the electrical communication --

Q. And that's because --

A. -- that the patent is talking about.

Q. That's because, in your opinion, a disabled buffer has a significant load; and, therefore, you believe that means it's in electrical communication with the TSV? Is that fair?

A. Well, I would say that there is a load present and that there's still a connection to the bidirectional buffer driver here, as we see it in Ruckerbauer.

Q. So just to be clear, when you formed your opinions, assuming -- to be clear, you formed your opinions assuming that there could be electrical communication even if there's no

electrical connection and even if no information can be exchanged between the buffer and the TSV; correct?

ATTORNEY ZHONG: Objection; form, misstates the reference, misstated testimony.

THE WITNESS: In the context of Ruckerbauer, Ruckerbauer talks -- uses the phrase "electrical coupling" and -- or "electrically coupled."

And what I'm saying is, even in the case where Ruckerbauer uses the phrase, there is no -- one of the buffers is electrically couples to the -- couples the memory array data terminal, and the other one is not in the on state. There is still electrical communication in both cases.

BY ATTORNEY CHANDLER:

Q. But I'm trying to just make clear the distinctions your drawing between electrical communication, electrical coupling. You're not treating the two as coextensive; correct?

A. I would say the phrase -- the electrically coupled phrase, as I recall, comes from Ruckerbauer specifically. But as I talked about, for instance, in paragraph 156, in the context of the '060 patent, not being electrically

coupled in this case to a buffer doesn't mean that there's not electrical communication with the buffer or that -- the die that the buffer is associated with.

Q. So, in your opinion, it's possible for a buffer to not be electrically coupled to the TSV, not to be electrically connected to the TSV, but to still be in electrical communication with the TSV; is that fair?

A. I would say that there -- it is still -- in the context of Ruckerbauer, for example, it is still possible -- there's still electrical communication even in the case where the buffer is not electrically coupled.

Q. And even if the case where the buffer is not electrically connected to the TSV; correct?

ATTORNEY ZHONG: Objection; form. Misstates the reference.

THE WITNESS: Yeah. Perhaps there's a section in my declaration where I talk about the phrase "electrically connected" in the context of Ruckerbauer.

BY ATTORNEY CHANDLER:

Q. I'm trying to ask you -- so -- do you

have the -- do you have an opinion on whether a bidirectional buffer in Rucker -- Ruckerbauer that is not electrically connected to the TSV, whether such an electrical -- let me see if I can phrase it a little bit more precisely.

Do you have an opinion about whether a bidirectional buffer in Ruckerbauer that is not electrically connected to the TSV can still be in electrical communication with the TSV?

ATTORNEY ZHONG: Objection; form, misstated reference.

THE WITNESS: I'm just skimming through the section of my declaration for you.

(Witness reviews document.)

THE WITNESS: Yeah, it looks like my discussion of Ruckerbauer is, unless I'm missing a section in my declaration, is talking about Ruckerbauer's characterization of things using the phrase "electrical coupled" -- "electrically coupled." And what I'm saying is, even in the case that one of Ruckerbauer's bidirectional drivers is not electrically coupled, it is still in electrical communication.

BY ATTORNEY CHANDLER:

Q. In your opinion?

A. That's correct.
Q. Do you see a difference between "electrically coupling" and "electrically connected"?
A. I -- I don't recall performing that analysis of -- in the context of Ruckerbauer or Ruckerbauer's use of "electrically coupled."
Q. "Electrically coupled" is a pretty common phrase to a person of ordinary skill in the art.
So more generally speaking, do you consider there to be a difference between electrically coupling and electrically connected?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: I would say it would depend on context or the references that someone might be looking at.
ATTORNEY CHANDLER: All right. Let's take a short break.
THE WITNESS: I was just going to ask, actually.
THE VIDEOGRAPHER: Off the record. The time is 4:25.
(Recess taken from 4:25 p.m. to 4:33 p.m.)

THE VIDEOGRAPHER: Back on the record. Time is 4:33 p.m.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have any corrections or clarifications you would like to make to your earlier testimony?

A. Not that I can think of right now, no.

Q. All right. Could you please look at Exhibit 1026, which I will put in the chat. Let me know when you have it open.

(Exhibit Number 1026 was previously marked for identification.)

THE WITNESS: Okay.

BY ATTORNEY CHANDLER:

Q. Exhibit 1026 is the Ellsberry reference; correct?

A. That is correct.

Q. Paragraph 12 of Ellsberry, marked as Exhibit 1026, in the middle of the paragraph teaches that the load on the bus is not increased because the memory bank switches present a single load to the bus, not the load of the individual memory devices coupled thereto; correct?

A. It's talking about the -- paragraph 12 says:

"The load on the bus is not increased because the memory bank switches present a single load to the bus."

And as I recall, that's referring to the load seen by the host system or the host system memory controller.

Q. So Ellsberry teaches --

A. I haven't looked at this reference in a little while, but -- at least in its entirety.

But go ahead.

Q. Ellsberry teaches in paragraph 12 that, from the perspective of the host computer, the load on the bus is not increased because the memory bank switches present a single load to the bus, not the load of the individual memory devices coupled to the memory bank switches; correct?

A. It looks like you read the sixth -- sixth line down, that looks like what it said; correct.

Q. And paragraphs 27 and 31 of Ellsberry at the end of those paragraphs also teach that Ellsberry reduces the load on the data bus; correct?

A. That at the end of 27, it is describing the capacitive load on the bus for the host is not increased because of the memory module presenting a signal load to the bus; and then the bottom of 28, I think you asked about --

Q. 31.

A. 31. It mentions reducing capacitive loading on the data bus 110 again -- again, at the DIMM interface that's relative to the host computer.

Q. Paragraph 45 of Ellsberry teaches that Figure 4 illustrates a block diagram of a data processing system 400, which may be implemented as part of the memory bank switch 206, which is shown in Figure 2; correct?

A. "That the data processing system may be implemented as part of a memory bank switch 206."

Q. So paragraph 45 of Ellsberry teaches that:

"Figure 4 illustrates the block diagram of a data processing system 400, which may be implemented as part of the memory bank switch 206," which is shown in Figure 2; correct?

A. That the block diagram of the processing

system 400 is for capacity expanding memory device and that this data processing system 400 can be implemented as part of the memory bank switch 206.

Q. That's what paragraph 45 of Ellsberry teaches?

A. In part, yes.

Q. Figure 4 of Ellsberry shows two bidirectional signal drivers labeled 402 and 404; correct?

A. That's correct. They're called bidirectional signal drivers in paragraph 45.

Q. And Figure 4 of Ellsberry, bidirectional signal driver 402 is coupled to data bus 234; and bidirectional signal driver 404 is coupled to data bus 236; correct?

A. That -- the signal driver 402 drives signals over the data bus 234; and then, similarly, the signal driver 404 is communicating over -- or signal 404 is transmitting and receiving over bus 236.

Q. So Figure 4 shows 402 coupled to 234 and 404 coupled to 236; correct?

A. That those -- those drivers are sending data over those busses. I don't see that this paragraph we've been discussing uses the word

"coupled."

Q. I'm just using "coupled" in the ordinary sense of the word. Is there anything that gives you pause about whether there's a coupling between 402 and 234 or between 404 and 236?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I haven't -- I don't think I've traditionally used that language in describing this part of Ellsberry. But I would say those bidirectional signal drivers, 402 and 404, they're transmitting and receiving the data over those two separate busses.

BY ATTORNEY CHANDLER:

Q. And "coupled" is the word that Ellsberry uses repeatedly; right? I mean, you can search for "coupled," and it shows up about 50 times in the --

ATTORNEY ZHONG: Objection; form. Is there a question pending?

ATTORNEY CHANDLER: Well, if you let me finish, there would be, yes.

ATTORNEY ZHONG: Okay.

BY ATTORNEY CHANDLER:

Q. "Coupled" is the word that is used

repeatedly by Ellsberry. If you search for the word "coupled" in Exhibit 1026, it comes up over 50 times; correct?

ATTORNEY ZHONG: Objection; form, argumentative.

THE WITNESS: The word or the phrase "coupled" is used in a number of different contexts in Ellsberry; that's correct.

BY ATTORNEY CHANDLER:

Q. Would it be fair to say that in Figure 4 of Ellsberry, bidirectional signal driver 402 is coupled to the data bus 234, and bidirectional signal driver 404 is coupled to the data bus 236; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: The paragraph we were just discussing describing those bidirectional drivers and busses, I don't see that it uses that word "coupled"; whereas, Ellsberry explicitly uses that language elsewhere.

BY ATTORNEY CHANDLER:

Q. In Figure 2 of Ellsberry, memory bank 0 and memory bank 2 are coupled to data bus 234 but are not coupled to data bus 236; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I was looking at the left-hand side.

So bank 0 and bank 2 in Figure 2 are communicating over the bus 234 shown here that connects to switch ASIC 206.

(Interruption by the court reporter to clarify the record.)

BY ATTORNEY CHANDLER:

Q. Figure 2 of Ellsberry shows that memory bank 0 and memory bank 2 are not coupled or communicating with data bus 236; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like for bus 236 in Figure 2, that the block labeled the bank 0 and bank 2 are not communicating over that data bus.

BY ATTORNEY CHANDLER:

Q. Figure 2 of Ellsberry shows that memory bank 1 and memory bank 3 are coupled to data bus 236 but are not coupled to data bus 234; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say that the data bus 236 is used to communicate with the bank 1 and bank 3.

BY ATTORNEY CHANDLER:

Q. And not with bank 0 and bank 2;

correct?

A. That looks right. Bank 0 and bank 2 do not use the data bus 236.

Q. Figure 2 of Ellsberry shows that memory bank 0 and memory bank 2 do not communicate using data bus 236; correct?

ATTORNEY ZHONG: Objection; form.

ATTORNEY CHANDLER: Is that correct?

THE WITNESS: Sorry. Your question one more time?

BY ATTORNEY CHANDLER:

Q. Figure 2 of Ellsberry shows that memory bank 0 and memory bank 2 do not communicate using data bus 236; correct?

A. It looks like those banks -- I don't see that that figure is illustrating block 214, bank 0, and block 218, bank 2, are communicating over the bus 236.

Q. Bidirectional signal driver 402 only sees the load of memory bank 0 and memory bank 2 that communicate using data bus 234; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't recall discussing what -- to your question, what load a driver -- a bidirectional driver 402 might see within

Ellsberry. I don't recall discussing that in this declaration.

BY ATTORNEY CHANDLER:

Q. Do you understand Ellsberry? Can you answer my question?

A. I do understand Ellsberry, although I'm not -- I don't talk about it extensively in my declaration. That sounds like something I've not looked at in the context of this proceeding.

Q. It's very simple, though. In Figure 4 and Figure 2 of Ellsberry, you see there's data bus 234, which, as shown in Figure 4, connects to bidirectional 402; and as shown in Figure 2, connects to memory banks zero and 2; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That there is a bidirectional driver 402 and a data bus 234; and then there is a bank -- in this case, a bank 0 and a bank 2.

BY ATTORNEY CHANDLER:

Q. Connected to data bus 234; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Banks 0 -- sorry. Bank 0 and bank 2 communicate over bus 234.

///

BY ATTORNEY CHANDLER:

Q. And so on bus 234, it's only bank 0 and bank 2 that present a load and not bank 1 or bank 3; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say only bank 0 and bank 2 communicate over that data bus 234; whereas, bank 1 and bank 3 communicate over the data bus 236.

BY ATTORNEY CHANDLER:

Q. Only bank 0 and bank 2 present an electrical load on data bus 234 to the switch ASIC. Banks 1 and 3 do not present electrical load over bus 234 to the switch ASIC; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I don't recall Ellsberry talking about that one way or the other or me offering or addressing -- offering an opinion on that in this declaration.

BY ATTORNEY CHANDLER:

Q. Are you able to answer my question now about what Ellsberry teaches?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: To the extent Ellsberry addresses that, I haven't looked at that issue or

addressed that in my declaration for today.
BY ATTORNEY CHANDLER:
Q. Let me just ask one more time just to give you a chance.
Memory bank 0 and memory bank 2 present a capacitive load on data bus 234; whereas, memory bank 1 and memory bank 3 do not present a capacitive load on data bus 234; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: I don't recall Ellsberry discussing that question that you're asking about the bidirectional driver inside the switch ASIC and -- and that type of loading question. Ellsberry is focused on expanding the storage capacity in terms of bits of storage, information storage of the -- of the device.
BY ATTORNEY CHANDLER:
Q. So you can't tell, looking at Ellsberry, whether there's a capacitive load presented on data bus 234 by memory banks 1 or 3? Is that your testimony?
ATTORNEY ZHONG: Objection; form, misstated prior testimony.
THE WITNESS: I would say that's not an issue I've addressed. Also, Figure 2 that we're

looking at right now is a very, very high-level block diagram with arrows and squares.

BY ATTORNEY CHANDLER:

Q. Making pretty clear what's connected to what; right?

ATTORNEY ZHONG: Objection; form. Argumentative.

THE WITNESS: I would say it points out different shared data busses -- well, what it refers to as shared data busses in arrows of one direction or another within the figure.

BY ATTORNEY CHANDLER:

Q. In Figure 2, memory bank 1 and memory bank 3 present a capacitive load on data bus 236; but memory bank 0 and memory bank 2 do not present a capacitive load on databank 236; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say bank 3 and bank 1 in Figure 2 are communicating over bus 236. Similarly, bank 2 and bank 0 are communicating over bus 234. I don't recall Ellsberry getting into -- and feel free to point me in the reference if it is -- but I don't recall addressing this in this IPR or Ellsberry going into that level of

detail, certainly not visually denoted in this figure.

BY ATTORNEY CHANDLER:

Q. I just want to give you the opportunity to answer the question. So I haven't heard you answer the question. I just want to, you know, make sure I've give you the opportunity so you can present it. This is your chance to present your testimony. And so here's the question:

In Figure 2 of Ellsberry, memory banks 1 and 3 present a capacitive load on data bus 236, but memory banks 0 and 2 do not present a capacitive load on data bus 236; correct? Or you're unable to answer that question?

A. I would say that's -- that's not something I recall Ellsberry discussing. Perhaps it is, but it's not something that I've discussed -- that I offer an opinion on one way or the other in my declaration.

Q. Memory bank 0 has a capacitive load; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I --

(Witness reviews document.)

THE WITNESS: So in the context of load,

when I look at a quick search through Ellsberry, it's talking about the load presented to the host as one aspect of Ellsberry.

BY ATTORNEY CHANDLER:

Q. You know that memory devices have a capacitive load, though; correct? On the data lines?

A. In a general sense, they can.

Q. Not only can, but do; right?

ATTORNEY ZHONG: Objection; form, argumentative.

THE WITNESS: I would say, generally, when you're connecting things to a shared line and putting additional attached devices that can communicate over it, in certain contexts, you may be concerned about load there.

BY ATTORNEY CHANDLER:

Q. And Ellsberry discloses that the memory banks can be compatible with the JEDEC standard, right, in his invention, for example, at the end of paragraph 50?

A. That the memory module is presenting a single electrical load to the system and is compatible with existing standards such as JEDEC.

Q. Which are incorporated by reference?

A. That's what it says in paragraph 50, yes.

Q. And at the end of paragraph 47, it teaches the -- the bank switch may support DDR1 and DDR2 memory devices; correct?

A. Did you say paragraph 47?

Q. End of paragraph 46.

A. I see that it mentions DDR1 and DDR2 specifications.

Q. And the end of paragraph 27 of Ellsberry teaches that individual memory devices have a load; right?

A. It's saying that the capacitive load on the bus 110 is increased because the memory module itself presents a single load on -- to the bus, not the load of the individual memory devices. It sounds like coupled to -- coupled to the memory module.

Q. So do you agree that memory bank 0 in Figure 2 of Ellsberry has a capacitive load?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It sounds like this sentence is referring to memory devices on a module and that those memory devices may have a resistive and/or capacitive load and that in

Ellsberry, that load of the memory device -- at least what it's saying here, the load of the memory device is not what's being presented to the -- to the host.

BY ATTORNEY CHANDLER:

Q. In Figure 2 of Ellsberry, memory banks 0 and 2 present a capacitive load on data bus 234; correct?

A. I would say that there is a shared data bus 234 and a bank 0 and a bank 2 that are communicating over it. I don't see that Figure 2 gets -- the description we're looking at gets into more than that, although in paragraph 27, the reference is mentioning that individual memory devices coupled to a module may have a load, a capacitive load.

Q. A person of ordinary skill in the art reading Figure 2 of Ellsberry would understand that memory banks 0 and 2 present a capacitive load on data bus 234; correct?

A. I don't see that it's -- I don't see that Ellsberry is explicitly saying that here. But it's saying that there are -- the bank 0 and bank 2 memory devices -- and there's a resistive or capacitive load associated with them, and it's

talking about the switch communicating over the shared data busses. If you're saying that there's a nonzero load -- capacitive load associated with bank 0 and it's connected to a bus, it may present a capacitive load on that bus, or may not. It would depend on specific configuration.

BY ATTORNEY CHANDLER:

Q. In the embodiment of Figure 2 of Ellsberry where the memory banks are DDR memory devices, they would present a capacitive load from 214 and 218 to data bus 234; correct?

A. If I have those memory devices and they have some nonzero capacitive load associated with them, and rather than connecting them directly to a host or a host bus, I stick them on another bus 234, they may present a capacitive load on that bus.

Q. But not on data bus 236 in Figure 2 of Ellsberry; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Again, Figure 2 is a very high-level diagram. But I would say if I have a separate shared data bus in some example that is in no way -- goes in the other physical direction over the PCB and never even interacts with bank 0

or bank 2, depending on context, I don't know that someone would say that those banks 0 and 2 are presenting the capacitive load on a separate bus.

BY ATTORNEY CHANDLER:

Q. It's a pretty simple question I'm trying to ask, Dr. Brogioli, but you seem to be having a difficult time answering it. And I'm a little sort of confused why.

Why do you view it as a difficult question to give a straight answer to?

ATTORNEY ZHONG: Objection; form, argumentative.

THE WITNESS: Well, I would say --

ATTORNEY ZHONG: It's an incomplete hypothetical.

THE WITNESS: These aren't subjects that I've addressed in my declaration, and you're asking questions about a very high-level block diagram in Ellsberry.

BY ATTORNEY CHANDLER:

Q. I'm also asking questions that are easy and well known to a person of ordinary skill in the art, such as a memory device presents a capacitive load.

ATTORNEY ZHONG: Objection; form.

Incomplete hypothetical, form.

THE WITNESS: I -- okay. There's language in Ellsberry talking about not -- quote, not the load of the individual memory devices coupled [inaudible].

(Interruption by the court reporter to clarify the record.)

THE WITNESS: Quote, not the load of the individual memory devices coupled thereto.

BY ATTORNEY CHANDLER:

Q. A person of ordinary skill in the art knows that the memory devices present a capacitive load, fair?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: If you're asking in the context of Ellsberry, it sounds like that is what the language at the end of paragraph 27 is getting at.

BY ATTORNEY CHANDLER:

Q. And a person of ordinary skill in the art, looking at Figure 2 of Ellsberry can see that the memory devices at banks 0 and 2 present their capacitive load to data bus 234 but not to data bus 236; correct?

ATTORNEY ZHONG: Objection; form,

incomplete hypothetical.

THE WITNESS: I don't see that Figure 2 discusses that one way or the other. It's just a high-level block diagram, in this case showing, at least in part, the shared data bus.

BY ATTORNEY CHANDLER:

Q. Figure 11 of Ellsberry also shows memory devices which are on the upper right side of that figure next to the brackets 1108 and 1110; correct?

A. Looks like it is showing a figure with multiple memory devices.

Q. And did the memory devices in Figure 11 have a capacitive load?

A. I'm looking in paragraph figure -- I'm sorry -- paragraph 54, talking about memory banks 1108 and 1110. It's just saying that each memory bank having four memory devices, 1112.

Q. Would a person of ordinary skill in the art, looking at Figure 11 of Ellsberry, understand that the memory devices, 1112, have a capacitive load? Or do you not know?

ATTORNEY ZHONG: Objection; form, incomplete hypothetical.

THE WITNESS: I don't see that this

description of the Figure 11 configuration is talking about load here one way or the other.

BY ATTORNEY CHANDLER:

Q. That's a little different from my question. I was asking what a person of ordinary skill in the art would understand, not what the two sentences that you're pointing to say.

ATTORNEY ZHONG: Objection; form, argumentative.

BY ATTORNEY CHANDLER:

Q. Can you try to answer my question.

A. I will give it the same answer: I don't see that Ellsberry, beyond our earlier discussion, is saying anything here regarding the configuration in Figure 11 and -- and the memory devices having load.

Q. In Figure 11, the memory devices that are by the bracket 1108, those connect to the data bus DQA; correct?

A. That looks correct, yes.

Q. The memory devices connected to the data bus DQA present a capacitive load on the data bus DQA; correct? That's what a person of ordinary skill in the art would understand looking at Figure 11 of Ellsberry?

A. I don't see that Ellsberry is saying that in regard to Figure 11. If there's a -- again, this is a high-level set of kind of rectangles illustrating the various controlling data signals.

Q. To be fair, this is illustrating DDR memory devices, right, what it says right there in Figure 11?

A. I note that Ellsberry mentions DDR memory devices. I don't see, at least where I'm looking, it's saying DDR memory devices for Figure 11. Perhaps that's elsewhere in Ellsberry.

Q. In 1112, each box says "DDR"; right? The bottom right corner of every single box.

A. In Figure 11? Oh, oh, oh. You're looking at the memory devices.

I see that it says the acronym DDR in each of the -- the blocks 1112.

(Interruption by the court reporter to clarify the record.)

BY ATTORNEY CHANDLER:

Q. DDR is a JEDEC standard for memory devices; correct?

A. There is a JEDEC standard for different types of DDR; that's correct.

Q. And the JEDEC standard specifies that there will be a capacitive load presented by the memory device; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Offhand, I don't recall specific language in the JEDEC standard from memory around that one way or the other.

BY ATTORNEY CHANDLER:

Q. But in forming your opinions in this case, you did not take into account whether or not memory devices presented a capacitive load; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: That's not correct. In the context of Ellsberry, I'm simply addressing certain points that Dr. Wolfe raised; and I don't recall this subject coming up as something that I was addressing.

BY ATTORNEY CHANDLER:

Q. You address DDR memory devices, not just in the context of Ellsberry, but in the context of the '060 patent, the '160 patent, Rajan, Riho, other references as well; correct?

ATTORNEY ZHONG: Objection; form, argumentative.

THE WITNESS: Some of those references mention DDR in various contexts; that's correct.
BY ATTORNEY CHANDLER:
Q. And it sounds like you have not taken into account whether or not memory devices present a capacitive load on the data bus; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: What I'm --
ATTORNEY ZHONG: Misstates the testimony.
THE WITNESS: What I'm saying is, I don't recall addressing an individual device in memory load in the context of Ellsberry or any points from Dr. Wolfe discussing this either that I address in my declaration. Ellsberry makes a passing reference in one or two places to JEDEC.
BY ATTORNEY CHANDLER:
Q. But a person of ordinary skill in the art would understand that memory devices present a capacitive load. Regardless of whether you characterize Ellsberry's discussion as passing or not, a person of ordinary skill in the art knows that memory devices present a capacitive load, especially DDR memory devices that comply with

the JEDEC standards; right?

A. If I -- if I hand a person of skill in the art a reference that says, "Here's a memory device and it's JEDEC-compliant, and it presents a load," then I think that they would understand what the reference told them.

ATTORNEY ZHONG: Counsel, how much longer do you have? It's 7:13 for Dr. Brogioli. Seems you guys don't want to start until 11 o'clock his time.

ATTORNEY CHANDLER: Yeah, if we can -- if we can go for just a little bit more, and then we can resume in the morning.

ATTORNEY ZHONG: How much longer do you have?

ATTORNEY CHANDLER: In fairness, it depends on how forthcoming the witness is. Why don't we go off the record and see how long we've been on -- on the record today. And then I'll try to certainly finish within seven hours for the day.

ATTORNEY ZHONG: Okay.

THE VIDEOGRAPHER: Yeah, we can go off, or I can just tell you. We've been going for 6 hours and 35 minutes, Counsel.

ATTORNEY CHANDLER: Okay. Well, so why don't we take a short break. I'll go no more than 25 minutes, and then we'll pick up again tomorrow at 9:00 Pacific.

THE VIDEOGRAPHER: Off the record. The time is 5:14.

(Recess taken from 5:14 p.m. to 5:22 p.m.)

THE VIDEOGRAPHER: Back on the record. The time is 5:22.

BY ATTORNEY CHANDLER:

Q. Dr. Brogioli, do you have any corrections or clarifications you'd like to make to your testimony earlier today?

A. No, I don't believe so.

(Exhibit Number 2043 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you please look at Exhibit 2043, which I have put in the chat for you. Let me know when you have it open.

A. Okay.

Q. Exhibit 2043 is a data sheet for NAND flash memory; correct?

A. This looks correct, yes.

Q. Please go to page 7 of Exhibit 2043. Let me know when you're there.

A. Okay.

Q. The second paragraph of page 7 of Exhibit 2043 teaches that there are five command pins labeled CLE, ALE, CE#, RE#, and WE# for NAND flash memory devices; correct?

A. Yes, that those are signals used for the command -- or the command bus protocol.

Q. And then if you turn to page 9 of the NAND flash memory data sheet marked as Exhibit 2043, it teaches that the pin labeled CE# is for the chip enable signal; correct?

A. That's correct.

Q. And then if you go to page 16 of Exhibit 2043, under the heading "Control Signals," the data sheet for NAND flash memory teaches that CE# is used to enable the NAND flash memory device, meaning that when CE# is low and the device is not in the busy state, the flash memory device will accept command data and address information; correct?

THE WITNESS: I see that sentence on page 16, yes.

///

BY ATTORNEY CHANDLER:

Q. And when the CE# signal is high, in that case the NAND flash memory device is not performing a read or write operation; instead, it enters a standby mode; correct?

A. When the device is not performing an operation, then CE is driven high and the device goes into a standby mode.

Q. And then turn to page 20 of Exhibit 2043. Let me know when you're there.

A. Okay.

Q. Page 20 of the NAND flash memory data sheet marked as Exhibit 2043 teaches, in the last row of Table 6, that when the CE# signal is high, the NAND flash memory device is in standby mode; correct?

A. That the mode is called standby, the various -- some various voltages are listed. And it denotes that CE is high in that state, or that mode.

Q. In contrast, as shown at the top of Table 6 of page 20 of Exhibit 2043, when CE# is low, the NAND flash memory device can perform read or write commands; correct?

A. That one of the things the device can do

when CE is low is a read mode command input, a write mode command input, as well as some other functionality -- data input, et cetera.

(Exhibit Number 2044 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. I put in the chat Exhibit 2044. Let me know when you have that up on your screen.

A. Okay.

Q. Exhibit 2044 is the data sheet for a SRAM memory chip; correct?

A. That seems to be the type of document this is for a certain type of SRAM -- SRAM -- SRAM chip, it looks like.

Q. Go to page 5 of Exhibit 2044. Let me know when you're there.

A. Okay.

Q. As shown on page 5 of Exhibit 2044, one of signals used by an SRAM memory device is labeled E overbar, and it is a chip enable signal; correct?

A. That is what the signal is called on this -- on this page, yes.

Q. And then on page 15 of Exhibit 2044, it teaches that in this data sheet the symbol VIL,

means input low voltage; and the symbol VIH means input high voltage; correct?

A. That looks correct.

Q. And then if you go back to page 7 of Exhibit 2044, Table 2 on page 7 of this SRAM data sheet marked as Exhibit 2044, shows in the top row that when the chip enable signal is high, the SRAM memory device is in a deselect mode; correct?

A. That for -- one moment, please. When the chip enable input symbol E bar is in the VIH or V high state, it is denoting the load in the leftmost column as deselect, and it looks like there's other ways that a mode deselect can be -- there's other ways -- it looks a mode deselect is represented.

Q. And did you say chip enable input symbol "E overbar," not "ER" but "E overbar"; is that correct?

A. That's what I meant to say, yes, with the bar on the top.

Q. And Table 2 on page 7 of Exhibit 2044 shows that when the chip enable symbol is low, the SRAM memory device can perform a read or write; correct?

A. That for at least Rows 2, 3 and 4 when the value of E bar is VIL, the chip is no longer in a standby mode and now it's in an active mode -- or active power state, denoted by the rightmost column, and that it is in a mode to either perform a read or a write.

Q. Okay. Let me give you another exhibit in the chat.

(Exhibit Number 2053 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. I've given you Exhibit 2053. Let me know when you have that open.

A. Okay.

Q. Exhibit 2053 indicates on the cover page in the bottom left that these are slides from the electrical computer engineering department of the University of New Mexico dated on the bottom right December 3rd, 2018, that you, I think, downloaded from the internet; correct?

A. That's my recollection.

Q. And as shown on the upper right of Exhibit 2053, these slides are from a course ECE 443; correct?

A. That looks right, yes.
Q. And a 400-level class like ECE 443 would typically be taught in the fourth year of college; is that fair?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: It's generally a more advanced class, so perhaps a senior-level -- if you're a fourth-year, senior, that ballpark kind of thing. Others might take it, but that's reasonable.
BY ATTORNEY CHANDLER:
Q. So senior in college, to be clear; correct?
A. That's what I was referring to, yes.
Q. Exhibit 2053 at the top of page 1 teaches that SRAM can be asynchronous; correct?
A. That's correct.
Q. And then in the third paragraph of page 1 of Exhibit 2053, the slides teach that memory controllers are usually synchronous; correct?
ATTORNEY ZHONG: Objection; form.
THE WITNESS: It looks like what, at least in part, the slides talk about the design of a memory controller for SRAM and trying to put an

extraction layer between the system and the asynchronous SRAM.

BY ATTORNEY CHANDLER:

Q. And the system is typically synchronous; whereas, in this example, the SRAM is asynchronous; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like, at least on Slide 1, that seems to be what it's referencing.

BY ATTORNEY CHANDLER:

Q. As shown at the bottom of page 1 of Exhibit 2053, the purpose of these slides is to teach students how to design a memory controller that can control asynchronous SRAM while making the SRAM look synchronous to the rest of the system, as explained in the middle of the slide; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Just skimming through the slides. So in part, I'm on Slide 8. And it talks about at the first sentence, "The memory controller provides a 'synchronous' wrap around the SRAM."

So it looks like at least one of the things the memory controller is trying to do is

provide a synchronous view of the underlying asynchronous SRAM.

BY ATTORNEY CHANDLER:

Q. And in 2008, undergraduates were expected to be able to design memory controllers that could control an SRAM; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: It looks like the exercise described in these slides is for students of this class to design aspects of what the slides refer to as a memory controller that presents some kind of synchronous view of SRAM to the outside world.

BY ATTORNEY CHANDLER:

Q. And as shown on page 5 of Exhibit 2053, that would involve getting the timing correct for read and write operations; correct?

A. It looks like Slide 5 is showing the viewer what the timing parameters are here to be followed.

Q. It would be fair to say that the slides marked as Exhibit 2053 would have been within the level of ordinary skill in the art in this IPR; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: I would say aspects of it

at least. To the extent the material was provided to and to be understood by, for example, this college senior taking this course, I would think it would generally be the case that they were supposed to understand -- or the intention would be for them to understand the material on these slides.

BY ATTORNEY CHANDLER:

Q. And Exhibit 2053, to be clear, this is a presentation that you found, you downloaded, and you introduced in this IPR; correct?

A. That's correct; and I note that much of the presentation is a lot of spoon feeding and giving hardware description language for all kinds of implementations that obey what looks like some of the variable timing constraints that are also handed -- given to the student as well for this small example.

Q. You relied on Exhibit 2053 in forming your opinions; correct?

A. This is an exhibit that I recall citing in my declaration; that's right.

Q. Okay. Why don't -- I'm prepared to go off the record and to come back tomorrow. But just before I do, last question: Do you have any

corrections or clarifications you would like to make? And as a reminder, unfortunately, during the break, you're not permitted to speak with your counsel about the substance of your testimony.

A. Understood. I don't have any corrections right now.

ATTORNEY CHANDLER: Why don't we resume tomorrow 9:00 a.m. Pacific.

ATTORNEY ZHONG: I have something tomorrow, so my colleague is going to be defending Dr. Brogioli tomorrow.

ATTORNEY CHANDLER: That's fine.

ATTORNEY ZHONG: Okay.

THE VIDEOGRAPHER: Off the record. The time is 5:42 p.m.

THE COURT REPORTER: Do you want rough drafts tonight?

ATTORNEY ZHONG: Yes, please.

ATTORNEY CHANDLER: Yes. And, actually, before we all disappear, Court Reporter, do you have any questions for us? Make the rough draft a little less rough.

(Whereupon, at 5:42 p.m., the proceedings adjourned.)

CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram, Registered Diplomate Reporter, Certified Realtime Reporter, California Certified Shorthand Reporter No, 8635, and Notary Public, the officer before whom the foregoing proceedings were taken, do hereby certify that the foregoing transcript is a true and correct record of the proceedings; that said proceedings were taken by me stenographically and thereafter reduced to typewriting under my supervision; and that I am neither counsel for, related to, nor employed by any of the parties to this case and have no interest, financial or otherwise, in its outcome.

Gail Inghram

GAIL INGHRAM, BA, RDR, CRR, CA-CSR 8635

MICHAEL BROGIOLI, PH.D.

RE: SAMSUNG ELECTRONICS CO., LTD. v. NETLIST, INC.
September 27, 2023, MICHAEL BROGIOLI, PH.D.
The above-referenced transcript has been completed by Esquire Deposition Solutions and review of the transcript is being handled as follows:

___ Per CA State Code (CCP 2025.520 (a)-(e)) - Contact Esquire Deposition Solutions to schedule a time to review the original transcript at a Esquire Deposition Solutions office.

__ Per CA State Code (CCP 2025.520 (a)-(e)) - Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Code of Civil Procedure.

___Waiving the CA Code of Civil Procedure per Stipulation of Counsel - Original transcript to be released for signature as determined at the deposition.

___Signature Waived - Reading and Signature was waived at the time of the deposition.

___Federal Read and Sign Requested (FRCP 30(e)(1)(B) -

Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Federal Rules.

XXX ___Federal Read and Sign Not Requested - Reading and Signature was not requested before the completion of the deposition.

E R R A T A

I wish to make the following changes, for the following reasons:

Page Line

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REASON: _____

I, MICHAEL BROGIOLI, PH.D., do hereby certify:

That I have read the foregoing deposition;

That I have made such changes in form and/or substance to the within deposition as might be necessary to render the same true and correct;

That having made such changes thereon, I hereby subscribe my name to the deposition.

I declare, under penalty of perjury, that the foregoing is true and correct.

Executed this _____ day of _____, 2023, at _____, _____.

(City) (State)

_____

MICHAEL BROGIOLI, PH.D.

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

_____

IPR2022-001427 and IPR2022-01428

U.S. Patent No. 8,787,060

U.S. Patent No. 9,318,160

ZOOM DEPOSITION OF DR. MICHAEL C. BROGIOLI

(Reported Remotely via video & Web videoconference)

Austin, Texas, (Deponent's location)

Thursday, September 28, 2023

Volume 2

STENOGRAPHICALLY REPORTED BY:
REBECCA L. ROMANO, RPR, CSR, CCR
California CSR No. 12546
Nevada CCR No. 827
Oregon CSR No. 20-0466
Washington CCR No. 3491

JOB NO. J10233368

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-001427 and IPR2022-01428

U.S. Patent No. 8,787,060

U.S. Patent No. 9,318,160

ZOOM DEPOSITION OF DR. MICHAEL C. BROGIOLI, taken on behalf of the Petitioner, with the deponent located in Austin, Texas, commencing at 11:01 a.m., Thursday, September 28, 2023, remotely reported via video & Web videoconference before REBECCA L. ROMANO, a Registered Professional Reporter, Certified Shorthand Reporter, Certified Court Reporter.

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Todd Bullock, Videographer

/////

I N D E X

DEPONENT		EXAMINATION
DR. MICHAEL C. BROGIOLI VOLUME 2		PAGE
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	BY MR. LINDSEY	340
	BY MR. CHANDER	350

EXHIBITS

NUMBER		PAGE
Exhibit 1057	US Patent No. 7,288,436, ('060);	287
Exhibit 1057	US Patent No. 7,288,436 ('160);	287
Exhibit 1060	Pub. No. US 2010/0110748 A1 ('060);	267
Exhibit 1060	Pub. No. US 2010/0110748 A1 ('160);	267

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Austin, Texas; Thursday, September 28, 2023
11:01 a.m.
---o0o---

THE VIDEOGRAPHER: We are now on the record. The time is 11:01 a.m. Central. The date is September 28th, 2023. 11:01:17

This begins videoconference deposition of Dr. Michael C. Brogioli, Volume 2, taken in the matter of Samsung Electronics Co., Ltd. versus Netlist, Inc., being heard before the United States Patent and Trademark Office, before the Patent Trial and Appeal Board, IPR 2022-01427 and IPR 2022-01428. 11:01:31

My name is Todd Bullock. I am the remote videographer. Our court reporter is Rebecca Romano. We represent Esquire Deposition Solutions. 11:01:53

Will everyone present please identify themselves and state who you represent, after which the court reporter will swear in the doctor. 11:02:04

MR. CHANDLER: Good morning. This is Ted Chandler from the law firm of Baker Botts on behalf of the Petitioner, Samsung Electronics Co., Limited, and with me is my 11:02:15

colleague Ferenc Pazamandi. 11:02:17

MR. LINDSAY: And this is Jonathan Lindsay with Irell & Manella, representing Patent Owner, Netlist, Inc., here to defend Dr. Brogioli today. 11:02:28

THE COURT REPORTER: Okay. Doctor, if you could raise your right hand for me, please.

THE DEPONENT: (Complies.)

THE COURT REPORTER: You do solemnly state, under penalty of perjury, that the testimony you are about to give in this deposition shall be the truth, the whole truth and nothing but the truth? 11:02:30

THE DEPONENT: I do. 11:02:30

11:02:30

11:02:31

/////

DR. MICHAEL C. BROGIOLI, 11:02:53

having been administered an oath, was examined and testified as follows:

EXAMINATION 11:02:53

BY MR. CHANDLER:

Q. Good morning, Dr. Brogioli.

Do you have any corrections or clarifications to the testimony you gave yesterday?

A. Not that I have right now, no. 11:03:01

Q. Could you please turn to the '160 patent marked as Exhibit 1001, which should be in the chat.

A. Okay.

Q. And go to column 5. Let me know when you're there. 11:03:21

A. Okay.

Q. Both the '160 patent and the '060 patent differentiate between DRAM packages, SDRAM packages, and flash memory packages as shown, for example, around line 5 of column 5 of the '160 patent, correct? 11:03:44

A. Let me take a look.

So looks like this section is describing the Figure 2 of the '160, and it's saying that the 11:04:32

package itself can include -- sorry, the package can include any type of memory package and, for example, packages of DRAM package, SDRAM package, flash memory package, et cetera. 11:04:39

Q. So do you agree that both the '160 and the '060 patent differentiate between DRAM packages, SDRAM packages, and flash memory packages? 11:04:55

A. I would say both specifications list those types of packages as what it sounds like this section is saying, at least in reference to hybrid memory cube or different types of packages. 11:05:15

Q. This section is in reference to Figure 2, which is the preferred embodiment of the claimed inventions, correct? 11:05:47

A. Yeah, Figure 2 is, I believe, the preferred -- or one of the example embodiments of a memory package in the present -- or, as it says, in the present disclosure.

Q. So for both the '160 patent and the '060 patent, according to the specification, the preferred embodiment of the invention can be implemented using a DRAM package, an SDRAM package, a flash memory package, or potentially other types of packages; is that fair? 11:06:16 11:06:37

A. That sounds as what this section is describing, yes. 11:06:42

Q. And this section differentiates between a DRAM package, an SDRAM package, and a flash memory package, correct? 11:06:57

A. In the sense that it's listing the -- those three examples as different types of packages.

Q. Could you turn to column 21 of the '160 patent and go down to line 54, please. Let me know when you're there. 11:07:14

A. Okay.

Q. Both the '160 patent and '060 patent teach that the array dies in the preferred embodiment of the invention may include DRAM, SDRAM, flash memory, or SRAM, to name a few, correct? 11:07:41

A. This section is referring back to Figure 88 and states that similar -- or it says, "As with the array dies 210 and 310," from Figures 2 and 3. The array dies can include -- for example, the array dies can include -- may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. 11:08:20

Q. And, to be clear, array dies 210 and 310 11:08:51

are the array dies in the preferred embodiment of the claimed inventions of the '060 and '160 patents, correct? 11:08:54

A. That sounds right, that those array dies, 210 and 310, are from the embodiment shown in figures 2 and 3. 11:09:11

Q. Please look at claim 10 of the '160 patent and let me know when you are there.

A. Okay.

Q. And it doesn't matter to me what copy of the claim language you are looking at. I am looking at the patent itself. 11:09:39

Is that what you are looking at, or are you looking at something else?

A. I am looking at the patent as well. 11:09:53

Q. So on the bottom of page 23 of Exhibit 1001 in claim 10, do you see that one of the limitations of claim 10 in the '160 patent is a DRAM package where each DRAM package comprises various elements, including stacked array dies, which show up on the top of page 24? 11:10:16

A. I see that section, yes.

Q. So claim 10 of the '160 patent requires, among other things, a DRAM package compromising stacked array dies, correct? 11:10:38

A. In compromising with the stacked arrays dies, at the top of column 25. 11:10:44

Q. According to the '160 and '060 patents, is it possible to have a DRAM package where the stacked array dies inside that package are SRAM chips? 11:11:01

A. I would say I haven't performed that analysis in my declaration.

Q. So it would be fair to say you have no testimony to offer today disagreeing with the statement that, according to the parts of the specification of the '060 and '160 patent that we just went over, they suggest that DRAM package can have stacked array dies that are SRAM chips, fair? 11:11:38

MR. LINDSAY: Objection. Outside the scope. Form. 11:12:05

THE DEPONENT: As I recall, the earlier language, when we were discussing column 21, states -- and I am roughly at line 53 -- the array dies may include any type of random access memory and then states, for example, DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. So I see the reference mentions that. I haven't performed an analysis in my declaration -- or in this matter, for example, around a specific device that may be 11:12:22 11:12:51

SRAM-based. 11:12:54

Q. (By Mr. Chandler) According to the '160 and '060 patents, it's also possible to have a DRAM package where the stacked array dies inside that package are flash memory chips, correct? 11:13:14

MR. LINDSAY: Objection. Outside the scope.

THE DEPONENT: I would say, referring us back to column 21, again, around line 53, it mentions that, for this embodiment, the array dies 11:13:31 can include -- well, it mentions they may include various types of random access memory and then, in the sentence starting at 54, mentions the array dies may include flash memory, in that context, as a type of random access memory. 11:13:53

Q. (By Mr. Chandler) Could you please go to your expert declaration marked as Exhibit 2023, which, as we discussed yesterday, is substantively the same in both IPRs, so it doesn't matter which copy of Exhibit 2023 you open up. So just open up 11:14:12 one of them and go to paragraph 180 to start and let me know when you are there.

A. Okay.

Q. At the bottom of page 112 of your expert declaration marked as 2023, in paragraph 180, you 11:14:46

site to U.S. Patent No. 8,301,833 marked as Exhibit 2042, correct? 11:14:51

A. That's correct.

Q. You describe the '833 patent, marked as Exhibit 2042, as an NVDIMM patent, non-volatile memory DIMM; is that correct? 11:15:06

A. That's correct.

Q. You indicate that the '833 patent, marked as Exhibit 2042, has a processor for controlling the exchange of information between the DRAM and the NAND flash memory, correct? 11:15:32

A. That it could -- that there's a single -- that could be a processor controlling that exchange of information, yes.

Q. So in the '833 patent marked as Exhibit 2042, there can be a processor that interfaces with both the DRAM memory devices and with the NAND flash memory devices; is that correct? 11:15:59

A. As I recall, it would be a processor core- -- controlling the movement of information from one to the other. 11:16:15

Q. Just to make sure the transcript is correct, did you say "processor core," C-O-R-E?

A. No, I said my recollection is there is a 11:16:39

processor there controlling the movement of data or information between the -- the two. 11:16:44

Q. So to make sure the question and the answer are -- are captured accurately, in the '833 patent marked as Exhibit 2042, you believe there is a processor there that can control the movement of data between both the DRAM memory device and the NAND flash memory device; is that correct? 11:17:09

MR. LINDSAY: Objection. Form. 11:17:33

THE DEPONENT: So I -- I don't have the '833 in front of me, but it looks like what I am saying -- and I am going on recollection -- is in the case of the Netlist NVDIMM patents, there may have been a processor of some form included that controls the -- the movement of information between a DRAM element over to a -- a NAND element in the device. 11:17:56

Q. (By Mr. Chandler) So I put in the chat Exhibit 2042, which is the '833 patent. 11:18:17

A. Okay.

Q. And I don't need to ask you a question about it, but I just wanted you to have it because your answer seems to suggest there was something you were trying to remember from it. 11:18:37

So if -- if it helps you to look at that, you are welcome to. If you don't have anything addition to -- anything additional to provide in your answer, that's fine as well. Just let me know either way. 11:18:41 11:18:56

A. I don't think I do. I was just characterizing in the -- in this paragraph the exchange of information between DRAM and NAND and characterizing that in the context of the '833 and Riho. 11:19:20

MR. CHANDLER: Okay. I do want to introduce a new exhibit. It will be Exhibit 1060.

(Exhibit 1060 was marked for identification by the Court Reporter and is attached hereto.) 11:19:28

MR. CHANDLER: Same exhibit in both IPRs. I will give you two copies, though, one stamped with the IPR number and the other stamped with the other IPR number.

So putting them in the chat. Let me know when you've got one of those open. 11:19:46

MR. LINDSAY: Hold on a second, Ted, let me give you a -- give me a chance to object if there is one.

Okay. You go can ahead. Thank you. 11:20:27

Q. (By Mr. Chandler) All right. 11:20:30
Dr. Brogioli, do you have Exhibit 1060 open?
A. I do.
Q. Exhibit 1060 is U.S. Patent Application Publication No. 2010/0110748 to the inventor Best 11:20:38
published on May 6th, 2010, correct?
A. Yes, that's correct.
Q. Figure 1A of the Best reference marked as Exhibit 1060 illustrates the memory device that includes both DRAM memory 103 and flash memory 101 11:21:15
with a shared interface 105 for both types of memory, correct?
MR. LINDSAY: Objection. Outside the scope.
THE DEPONENT: Give me a moment. I don't 11:21:33
believe I have seen this reference before. Let me take a second to look at it.
Okay. So I -- I'll just add before I answer: I don't think I've seen this before. I certainly haven't analyzed it before today. 11:22:03
It looks like -- at least the reference in paragraph 4 describes Figure 1A as, quote, "Illustrates an embodiment of a hybrid, composite memory device having a non-volatile storage IC, volatile storage IC and shared-interface IC." 11:22:21

Q. (By Mr. Chandler) In the title of Exhibit 1060 is "hybrid volatile and non-volatile memory device," correct? 11:22:27

A. That's correct.

Q. And you had mentioned earlier in the '060 and '160 patent that they reference hybrid memory, correct? 11:22:43

A. I -- maybe you can refresh me where I may have said that.

Q. Well, it was in response to a question that I had asked you. 11:23:19

A. I would say that the specifications refer back to at least the hybrid memory cube and some language around that we were discussing previously. I don't recall having much more of a discussion than that. 11:23:41

Q. By the time of the '060 and '160 patents, it was known in the art that a memory device could include both volatile and non-volatile memory together, correct? 11:24:05

A. I would say that it was known that there were memory modules or products designs that incorporated forms of volatile and non-volatile memory.

Q. And it was also known by the time of '060 11:24:28

and '160 patents how to convert signals from the DRAM format to the flash memory format and vice versa, correct? 11:24:30

MR. LINDSAY: Objection. Form. Outside the scope of direct. 11:24:43

THE DEPONENT: I don't recall performing in -- an analysis of that or references that talk about that. I would say that it was known that you could have a microprocessor in a system that read from some sort of volatile memory in one part of the systems and perhaps wrote it to a non-volatile memory somewhere else in the system, but I haven't really gotten to analyze anything beyond that. 11:25:04

Q. (By Mr. Chandler) Could you turn back to Exhibit 1060 and go to paragraph 15 and let me know when you are there. 11:25:17

A. Okay.

Q. Paragraph 15 of the Best reference marked as Exhibit 1060 describes, in the second sentence of that paragraph, an embodiment having a, quote, "DRAM external interface" correct? 11:25:38

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: I see that language, quote, "having a DRAM internal interface." 11:25:54

Q. (By Mr. Chandler) And that paragraph goes on to describe the embodiment by saying, quote, "control and data signals may be forwarded without change to a DRAM die," end quote; whereas, control and data signals, quote, "may be converted from DRAM format to flash memory format before being forwarded to the flash memory device," end quote. 11:26:00 11:26:23

Did I read that accurately?

MR. LINDSAY: Objection. Outside the scope of direct. 11:26:40

THE DEPONENT: Let me take a second to read the paragraph.

Okay. I see the two partial quotes from the second sentence that you read, but, again, I haven't -- I haven't analyzed this reference, but I see those words in this paragraph. 11:27:49

Q. (By Mr. Chandler) Paragraph 15 of the Best reference marked as Exhibit 1060 goes on to state, quote, "In general, any external protocol may be used to access the hybrid memory device, and any internal protocol or set of protocols may be used to control the volatile and non-volatile storage dice," end quote. 11:28:12

Did I read that correctly? 11:28:32

MR. LINDSAY: Objection. Outside the scope of direct. 11:28:33

THE DEPONENT: You did.

Q. (By Mr. Chandler) Do you agree that by May 6th, 2010, the publication date of the Best reference marked as Exhibit 1060, it was known how to convert signals from DRAM format to flash RAM -- flash memory format and vice versa? 11:28:40

MR. LINDSAY: Objection. Outside the scope of direct. Form. 11:29:00

THE DEPONENT: It looks like this sentence is talking about various sets of protocols that the reference contemplates in some sort of translation that the reference contemplates. I haven't really referenced what -- sorry, I haven't analyzed this reference before or what that actually entails or doesn't entail in this reference. 11:29:26

Q. (By Mr. Chandler) All right. Could you go to the '060 patent marked as Exhibit 1001 and let me know when you have that in front of you. 11:29:51

A. Okay.

Q. And go to column 5, line 52. Let me know when you are there.

A. Okay. 11:30:27

Q. Both the '060 patent and the '160 patent teach that "Examples of die interconnects include, but are not limited to, through-silicon vias," abbreviated "TSV," "conducting rods, wire bonds, and pins," correct? 11:30:32 11:30:49

A. Correct. And then it points to two other patents.

Q. Please turn to claim 5 of the '060 patent. Let me know when you are there.

A. Okay. 11:31:15

Q. Claim 5 of the '060 depends from claim 1, correct?

A. That's right.

Q. Claim 5 of the '060 patent requires the die interconnect to comprise a through-silicon via, abbreviated "TSV," correct? 11:31:30

MR. LINDSAY: Objection. Form.

THE DEPONENT: Your question one more time? I was focusing on the language and time, but I -- maybe I should hear your question again. 11:31:54

Q. (By Mr. Chandler) Claim 5 of the '060 patent requires the first die interconnect to comprise a through-silicon via, abbreviated "TSV," correct?

MR. LINDSAY: Objection. Form. 11:32:16

THE DEPONENT: So looking at claim 5, I see the language is talking about the control die and control circuit and states on the first data conduits and second data conduits. 11:32:36

Q. (By Mr. Chandler) You're looking at the '060 patent? 11:32:53

A. I'm sorry, I was looking at the '160.

(Court Reporter initiates discussion off the stenographic record.)

Q. (By Mr. Chandler) So take a look at -- you know, read claim 5 of the '060 and let me know when you are ready. 11:33:12

A. Go ahead. Thank you.

Q. In claim 5 of the '060 patent, the claim language requires the die interconnects to comprise a through-silicon via, abbreviated "TSV," correct? 11:33:35

MR. LINDSAY: Objection. Form.

THE DEPONENT: That comprises -- or a die interconnect that comprises a first through-silicon via. 11:33:52

Q. (By Mr. Chandler) And "through-silicon via" is commonly referred to as a "TSV" --

A. That's right.

Q. -- including in the patent?

A. That's right. 11:34:11

Q. Including in the patent? 11:34:12
A. Correct, yes.
Q. Independent claim 1 of the '060 patent does not require the die interconnects to comprise a through-silicon via, abbreviated "TSV," correct? 11:34:25
A. I, at least, don't see the explicit language "through-silicon via" present in the explicit words of claim 1.
Q. Do you believe that claim 1 of the '060 patent inherently requires the die interconnects to comprise a through-silicon via, abbreviated "TSV"? 11:35:22
MR. LINDSAY: Objection. Outside the scope.
THE DEPONENT: I -- I haven't performed that analysis in this IPR. 11:35:39
Q. (By Mr. Chandler) Okay. Let's go back to Exhibit 1058. I will put it back in the chat. It was marked yesterday. And let me know when you have Exhibit 1058 open. 11:36:27
A. I do.
MR. LINDSAY: If there was an objection made yesterday when this was first introduced, I would like to reiterate that same objection.
And just give me a second to open it 11:36:44

myself. 11:36:47

Okay. Thank you.

Q. (By Mr. Chandler) Exhibit 1058 is the '912 patent that you are familiar with, correct?

A. That's correct. 11:37:03

Q. And the '912 patent issued in 2009, before the '060 and '160 patents were filed, correct?

A. That's my recollection, yes.

Q. Please go to column 23 of the '912 patent marked as Exhibit 1058 and look starting at line 64 and let me know when you are there. 11:37:20

A. Okay.

Q. The '912 patent, marked as Exhibit 1058, refers to collisions, correct? 11:37:52

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: I see the word "collisions" is used in this paragraph.

Q. (By Mr. Chandler) And in your direct testimony, marked as Exhibit 2023, you talk about collisions over 50 times, correct? 11:38:11

A. We certainly discuss the -- or different variants of them yesterday.

Q. And how would you summarize what 11:38:36

collisions are in the context of a memory device? 11:38:39

A. I -- I haven't performed an analysis of the exhaustive set of things that folks might consider a collision.

But if I recall yesterday in the various references we were discussing, there were issues, as I recall, referred to as collisions, for example, when read or write data was trying to reside on a -- on a given pathway at the same moment in time or -- in -- in sort of the data 11:38:58 11:39:25
sense, and then I think there were other examples in that context yesterday that may have been from JEDEC talking about when commands such as -- it might have been refreshed, or something like that, overlapping with, for example, a write command in time, were a few examples. 11:39:48

Q. And would it be fair to say, when there's a collision, whether it's the data signals colliding or the command signals colliding, that's a bad outcome, something to be avoided in the context of a memory device? 11:40:09

MR. LINDSAY: Objection. Form.

THE DEPONENT: It -- it probably depends on the context and how a system is designed. But in -- in certain context yesterday, if there's a -- 11:40:30

you know, a shared wire, you don't want to have multiple devices trying to transmit on it at the same point in time, similarly to how I think Dr. Stone and Dr. Wolfe also testified to. 11:40:33

Q. (By Mr. Chandler) Would it be fair to say that a person of ordinary skill in the art was aware of the problem posed by collisions and also knew of various techniques to avoid collisions when memory devices in two different ranks share a data line? 11:40:51 11:41:15

MR. LINDSAY: Objection. Form.

THE DEPONENT: I -- I wouldn't agree with that statement.

Q. (By Mr. Chandler) Are you sure about that? 11:41:24

A. There's a lot in there. If you want to break it up into a couple questions, maybe we can address those.

Q. Would it be a fair to say a person of ordinary skill in the art was aware of the problems posed by collisions? 11:41:34

A. In the context I was discussing earlier, similar to Dr. Wolfe and Dr. Stone's testimony, that, for example, multiple devices trying to write data to a shared line at the same time -- a person 11:41:57

of skill in the art would understand that there's -- in this context, there's a problem there. That's problematic. 11:42:02

Q. Do you agree a person of ordinary skill in the art knew about various techniques to avoid collisions when memory devices in two different ranks share a data line? 11:42:12

A. I would say, in the general sense, there were probably examples yesterday. It might have been from JEDEC, or something of that nature, showing some solutions to that problem that may have been acceptable in that context. But I -- I don't -- I wouldn't say that they were aware of sort of a generally accepted solution for -- for all problems in this -- in this space. 11:42:40 11:42:57

Q. What technique does the '912 patent marked as Exhibit 1058 state, here at column 23, line 60 through 67, for avoiding collisions when memory devices in two different ranks share a data line? 11:43:22

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: It looks like, in this paragraph, the '912 is talking about memory boundaries between ranks in a memory module and 11:43:40

that in the case of what it refers to as a back-to-back adjacent read command, it, at least from the language of this paragraph, says the memory controllers can insert wait-time intervals or clock cycles to avoid collisions or interference in that scenario. 11:43:50 11:44:07

Q. (By Mr. Chandler) Would it be a fair to say a person of ordinary skill in the art knew that memory controllers could insert wait-time intervals or clock cycles to avoid collisions? 11:44:26

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: I would answer that that there may have been, I think, references, even yesterday, that mention this really naive solution that may be entirely unacceptable to just insert -- insert cycles of idle time or idle activity to just sort of dumbly wait and sit there. But that isn't -- isn't generally -- in a general sense, isn't desirable in high-performance memory systems for a number of reasons, either performance or just standards compliance perhaps. But I think there were references that mentioned that somewhat naive solution. 11:44:40 11:45:08

Q. (By Mr. Chandler) In the '060 and '160 11:45:34

patents, are there any limitations of the claims that require high performance? 11:45:36

A. I would say the inventions, overall in the '060 and '160, are striving for very high storage capacity in terms of bits -- bytes of storage and high-performance and high-bandwidth memory performance. 11:45:57

If you are asking does the phrase, quote, "high performance" explicitly present itself in the claims, I don't recall that it does. 11:46:17

Q. Do you regard Netlist '912 patent marked as Exhibit 1058 as claiming a high-performance memory module?

MR. LINDSAY: Objection. Outside the scope of direct. 11:46:33

THE DEPONENT: I don't know that I have analyzed that aspect of it, of the '912, and high performance has to probably be characterized in terms of the -- whatever the performance is that you are trying to make high versus low, if that -- if that makes sense, if it's speed or bandwidth or storage capacity or things like that. 11:47:00

Q. (By Mr. Chandler) Would it be fair to say that if there's data collisions, that could ruin the performance of any memory module? 11:47:24

MR. LINDSAY: Objection. Form. 11:47:36

THE DEPONENT: I wasn't sure I heard the whole question. Maybe you can repeat it.

Q. (By Mr. Chandler) Would it be fair to say that if there's data collisions, that could ruin the performance of any memory module? 11:47:48

MR. LINDSAY: Objection. Form.

THE DEPONENT: I'm -- sorry, I'm not really hearing your question. Are you asking, would it be fair to say if there's data collisions that could ruin the performance of any memory module? 11:48:04

Q. (By Mr. Chandler) Would it be fair to say that if there are data collisions, comma, that could ruin the performance of any memory module? 11:48:24

MR. LINDSAY: Objection. Form.

THE DEPONENT: Okay. Thank you.

I would say perhaps it would -- you would need to be more specific in terms of how the modules work, but you wouldn't want to have data collisions that corrupt -- in the -- in the data collision sense, corrupt data or destroy data. It seems like you, in that context, would end up with a -- you know, a incorrectly functioning device. 11:48:44

Q. (By Mr. Chandler) Turning back to the 11:49:12

'912 patent marked as Exhibit 1058 at column 23, line 60 through 67, which refer to one technique for avoiding collisions, which was the memory controller can insert wait-time intervals or clock cycles to avoid the collisions, correct? 11:49:13 11:49:38

MR. LINDSAY: Objection --

THE DEPONENT: That --

MR. LINDSAY: -- form.

THE DEPONENT: That seems to be what the second sentence of this paragraph is at least, in part, getting at. 11:49:48

Q. (By Mr. Chandler) Were there other techniques that were known to a person of ordinary skill in the art for avoiding collisions when memory devices in two different ranks share a data line? 11:49:59

A. I would say this inserting -- I am going to point us back to the '912, line 60 to 67, that the reference seems to be inserting clock cycles for this specific -- the memory controller inserting clock cycles for this specific scenario. 11:50:24

In terms of a general sense of data collisions, there are a lot of complexities into how to handle that the -- I would say are -- are beyond the scope of a person of skill. If just a 11:50:55

naive solution of inserting delays until the collision scenario passes in time. Even Kim doesn't contemplate that as accessible -- acceptable. 11:50:59

And so, in a general sense, one would need to account for a memory-controller-based solution and on-module-based solution, the timing of the on-module components, the complexity of the signaling, the speed at which things are operating, the protocol that may be obeyed, the standard that may have to be obeyed. There's -- there's a lot of variables to that. 11:51:15 11:51:32

Q. Is it fair to say that if the timing of the data signals or the timing of the control signals is off by even just one or two clock cycles, that the result can be a collision that causes problems? 11:52:01

MR. LINDSAY: Objection. Form.

THE DEPONENT: I am not sure if you are asking about a specific reference or design, but in a general sense, in the universe of memory devices signaling protocols for memory modules, generally speaking, you're very mindful of signal timing to make sure things work, I will use the word, appropriately in -- in the general sense. 11:52:26 11:52:57

Q. (By Mr. Chandler) And so, generally, for example, DDR memory devices are referred to as synchronous DRAM memory devices, meaning that they operate in accordance with what I will refer to, in general terms, a clock signal, correct? They don't just operate when they feel like it. They operate in accordance, in theory, with a sort of clock signal, correct? 11:53:00 11:53:16

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would say, generally, yes. Synchronous DRAM devices operate, at least in part, with this clock signal. 11:53:32

Q. (By Mr. Chandler) And so for synchronous memory devices, such as DDR memory devices, if the signal for the data or the signal for the controls is off by even just one or two clock cycles from where they are expected to be, that can result in collisions, correct? 11:53:53

MR. LINDSAY: Objection. Form. Asked and answered. 11:54:11

THE DEPONENT: I would have to answer you in a general sense, but these synchronous digital devices are operating in conjunction with a clock that's providing a notion of time.

If -- so your question -- generally, if I 11:54:33

say the device needs to operate within X number of clock cycles in a standard, let's say, and it's taking X plus Y cycles and the plus Y is outside of the specification of the standard or the specification of a given device, then that can be problematic. 11:54:40 11:54:57

Q. (By Mr. Chandler) Would it be fair to say that in high-performance synchronous memory devices, such as DDR memory devices, there may often be situations where -- if the signals are even one or two clock cycles outside of the acceptable range provided by the standard, that you could get a collision for either of the data signal or the control signals? In other words, the timing margins are that precise? 11:55:23 11:55:48

MR. LINDSAY: Objection. Form.

THE DEPONENT: I haven't looked at a specific example of that, for example, in -- in a DDR specification, but it -- that sounds like a scenario that could be possible. 11:56:06

Q. (By Mr. Chandler) So what other techniques did a person of ordinary skill in the art know of at the time to avoid collisions when memory devices in two different ranks share a data line? 11:56:26

MR. LINDSAY: Objection. Asked and answered. Form. 11:56:28

THE DEPONENT: I -- I haven't gone and done an analysis of that. The points that I have largely discussed in my declaration are, with respect to Samsung and Dr. Wolfe's, the references and -- and combinations and -- and arguments made there. 11:56:37

MR. CHANDLER: I would like to introduce a new exhibit, which will be 1057. I think I skipped over it yesterday. I am not quite sure, but I will put it in the chat. 11:57:00

(Exhibit 1057 was marked for identification by the Court Reporter and is attached hereto.) 11:57:12

MR. CHANDLER: And, again, it's the same exhibit in both IPRs, the only difference being the stamp with the IPR number.

Let me know when you have Exhibit 1057 in front of you. 11:57:26

And, Jonathan, let me know when you are ready to proceed.

MR. LINDSAY: Thanks. I'm -- I'm good.

THE DEPONENT: I have it up as well.

Q. (By Mr. Chandler) Exhibit 1057 is 11:57:36

U.S. Patent No. 7,286,436, filed on March 7th, 2005, correct? 11:57:37

A. That's correct, yes.

Q. And if you turn back to the '912 patent marked as Exhibit 1058, it states on the cover page, under the heading "Related U.S. Application Data," that the '912 patent is a continuation, in part, of the '436 patent marked as Exhibit 1057, correct? 11:57:55

A. I see that, yes. 11:58:22

Q. I want to turn back to Exhibit 1059, which we talked about briefly yesterday, but I will put it back in the chat again, so let me know when you have Exhibit 1059 back in front of you.

A. I do. 11:58:49

Q. And please go to page 187 of Exhibit 1059.

MR. LINDSAY: Ted, was this introduced yesterday?

MR. CHANDLER: Yes. 11:59:00

MR. LINDSAY: Okay. For the record, whatever objection was made yesterday, same objection today.

THE DEPONENT: Okay. I am on page 1087 -- I'm sorry, 187. 11:59:15

Q. (By Mr. Chandler) Page 187 of Exhibit 1059 shows your signature on August 10th, 2023, correct? 11:59:21

A. Correct.

Q. Please turn to page 81 of Exhibit 1059 and let me know when you are there. 11:59:34

A. Okay.

Q. In paragraph 29 -- I apologize.

Are you on page 81?

A. I am. 12:00:24

Q. In paragraph 91, in the second sentence, you express the opinion that "a person of ordinary skill in the art could readily configure the memory controller in a memory system featuring the '436 module to use appropriate timing sequences to avoid 12:00:44 such collisions by inserting a delay between successive read commands, without the need to know the physical boundaries of the memory devices. The... designer could also use a serial presence detect (SPD) device to inform the memory controller 12:01:05 of the physical boundaries of each memory device."

Did I read that accurately?

A. Yes, you did.

Q. And have you changed your opinions since you wrote that on August 10th, 2023? 12:01:22

A. Those statements, in the context of this -- the '912 declaration? No, my opinions stay the same. 12:01:29

Q. Could you pull up Exhibit 1014 and let me know when you have it. 12:01:46

A. Okay.

Q. Exhibit 1014 is the Kim reference, correct?

A. That's right.

Q. Please turn to Figure 1 of Kim. 12:02:39

A. Okay.

MR. CHANDLER: And you know what? This might be a good time for a break. It's been about an hour and -- why don't we take a short break right now. 12:02:58

THE DEPONENT: Okay.

MR. LINDSAY: Okay.

MR. CHANDLER: Thanks.

THE VIDEOGRAPHER: We are off the record at 12:03 p.m. 12:03:05

(Recess taken.)

THE VIDEOGRAPHER: We are back on the record at 12:12 p.m.

Q. (By Mr. Chandler) Dr. Brogioli, do you have any corrections or clarifications to your 12:12:58

testimony that you would like to make? 12:13:00

A. No, I do not.

Q. Dr. Brogioli, the '912 patent, Exhibit 1058, when it was discussing collisions and the potential solutions to collisions, that was in 12:13:15 the context of rank multiplication, correct?

MR. LINDSAY: Objection. Outside the scope of direct.

MR. CHANDLER: And if I said "'921," I meant the '912 patent. 12:13:43

THE DEPONENT: Understood.

We were discussing specifically the language of column 23, roughly line 60 to 67, and as I generally recall, that paragraph is -- is taken in -- in context of the specification which 12:14:00 contemplates, at least within the '912's focal point, a form of rank multiplication.

Q. (By Mr. Chandler) And could you look at Exhibit 1059 and page 81 and let me know when you are there. 12:14:38

A. Okay.

Q. Shown in the first sentence, it's your opinion that, quote, "Even if it was necessary for a memory system designer to find a solution to the" back-to-back adjacent read commands, abbreviated 12:15:09

"BBARX," "issue, based on the '436 patent disclosure and knowledge of the art, such a designer could overcome the supposed challenge of executing" back-to-back adjacent read commands," abbreviated "BBARX," "on a rank-multiplied module without undue experimentation," end quote. 12:15:12 12:15:26

Did I accurately read your opinion?

A. You did.

Q. And have you changed your opinion since August 10th, 2023? 12:15:53

A. In this '912 declaration? No, I have not.

Q. Could you turn back to Exhibit 1014 and look at Figure 1 and let me know when you are there. 12:16:05

A. Okay.

Q. Figure 1 of the Kim reference marked as Exhibit 1014 shows a typical memory apparatus as of around 2009 when Kim was filed, correct?

A. That's -- that sounds right. Kim describes it as the typical semiconductor memory apparatus. 12:16:33

Q. And the memory apparatus in Figure 1 of Kim includes two memory chips, correct?

A. It -- it has right-side-facing lines that 12:16:58

are going to where what Kim refers to as a Rank0 in the top right and right-hand lines for a Rank1 on the lower part. 12:17:08

Q. And each of those would be a -- a memory chip; is that fair? 12:17:24

A. It would be some -- whatever -- some form of memory that -- that Kim discusses.

Q. Turn to paragraph 6 of Kim and let me know when you are there.

A. Okay. 12:17:40

Q. The middle of paragraph 6 of Kim, marked as Exhibit 1014, teaches that, quote, "The first chip is typically referred to as a first rank Rank0 and the second chip is referred to as a second rank Rank1," end quote. 12:18:20

Did I read that accurately?

A. You did.

Q. And paragraph 6 of Kim goes on to explain that each rank has a corresponding chip selection signal that selects the corresponding rank to perform the data input/output operations, correct? 12:18:39

A. To perform data input/output operations through the first rank Rank0 or the second rank Rank1.

Q. So according to paragraph 6 of Kim, each 12:19:05

rank has a corresponding chip selection signal that selects the corresponding rank to perform its data input or output operations, correct? 12:19:09

MR. LINDSAY: Objection. Form.

THE DEPONENT: That -- so as I recall, Kim uses language around the memory devices and rank and possibly bank in a number of different context. But there is disclosure in Kim, in the subsequent embodiments, about the use of a chip select signal. 12:19:31 12:20:02

Q. (By Mr. Chandler) But there's also disclosure here in paragraph 6 in the embodiment of Figure 1 of the use of a chip selection signal, correct?

A. It looks like it's talking about the use of a chip select to -- chip selection command signal as part of performing I/O operations on a first rank or a second rank. 12:20:24

Q. And could you turn back to Figure 1 and let me know when you are there -- in Kim. 12:20:45

A. Okay.

Q. Figure 1 of Kim, marked as Exhibit 1014, shows that Rank0 has a data pad DQ0 and Rank1 has a data pad DQ1, correct?

A. That's -- correct. There's a DQ0 and a 12:21:16

DQ1 on the leftmost side of the figure. 12:21:19

Q. Figure 1 of Kim shows that those two data pads, DQ0 and DQ1, are connected to each other, as shown on the left side of the figure, correct?

A. That's correct. 12:21:41

Q. So Kim teaches that the data lines for two separate ranks can be connected to each other, correct?

A. I would say what Kim is showing in this figure as -- the DQ0 and DQ1 in this figure are 12:22:06 shown being tied to the same line on the left-hand side of the figure, and then Kim goes into describing a number of issues that occur with this implementation.

Q. Kim describes this implementation as 12:22:32 prior art, as shown at the top of Figure 1, correct?

A. Figure 1 is prior art, correct.

Q. And it was not unusual by the time of Kim for multiple memory devices to share the same data 12:22:47 line where those devices were in different ranks, correct?

MR. LINDSAY: Objection. Form.

THE DEPONENT: I think what Kim is intending to convey with this image is that there 12:23:04

are multiple ranks here with intervening components, as shown in the figure. And at the time of Kim, this was the prior-art solution or a form of common solution at the time. 12:23:07

Q. (By Mr. Chandler) Besides Kim, there were other commonly used memory modules that were known to persons of ordinary skill at the art at the time that had multiple chips in multiple ranks sharing the same data lines, correct? 12:23:45

MR. LINDSAY: Objection. Form. 12:24:04

THE DEPONENT: I don't recall doing an analysis of that. I'm largely addressing a handful of prior-art references that -- that Dr. Wolfe presented.

Q. (By Mr. Chandler) So you do not consider, for example, that the JEDEC standards and common JEDEC-compliant memory modules, such as RDIMMs and UDIMMs, commonly had multiple memory devices in different ranks sharing the same data lines, correct? That's not something you considered in performing your analysis? 12:24:23 12:24:50

MR. LINDSAY: Objection. Form.

THE DEPONENT: There's a -- there's a lot that's sort of missing in your question, but there may have been even documents that we discussed 12:25:02

yesterday that, at a high level, look similar to what you are describing. But there's a lot of nuance and variability into how a set of prior-art references may contemplate that, so I haven't performed an analysis of the number of references or things like that. 12:25:07 12:25:23

Q. (By Mr. Chandler) Do you agree that JEDEC-compliant memory modules at the time commonly had multiple memory devices in different ranks sharing the same data lines? 12:25:38

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: I would say that there were JEDEC references contemplating multiple ranks of memory devices and very lengthy and detailed signal information, either just for a given memory device or how they are laid out in an implementation, so that sounds sort of within the universe of things we are talking about, but I -- I don't recall any of those references with specificity beyond that. 12:25:50 12:26:10

Q. (By Mr. Chandler) And, to be clear, those references had multiple memory devices in different ranks sharing the same data lines, correct? 12:26:24

MR. LINDSAY: Objection. Outside the scope of direct. Form. 12:26:26

THE DEPONENT: I would say those references talk about multiple memory devices and multiple ranks. As to what various lines are named or how they are connected and implemented, I'd have to go back and look at a specific reference for you. 12:26:35

Q. (By Mr. Chandler) Is it your opinion that it was beyond the level of skill for a person of ordinary skill in the art to implement two memory devices in two different ranks sharing the same data line? 12:26:48

A. You are asking a very sort of broad and generic question. I think a person of skill in the art would understand this concept. As to how a specific implementation works or what the requirements were is much more specific question. But they would understand this concept of multiple ranks in trying to send data over a, in your question, singular data line or the desire to do that. There's a lot more detail behind that. 12:27:09 12:27:24

Q. And I'm not just asking if a person of ordinary skill in the art would understand the concept. 12:27:46

I'm asking: Is it your opinion that it would be beyond the level of a person of ordinary skill to implement the concept of two memory devices in different two ranks sharing the same data line? 12:27:47 12:28:03

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would need more context on your -- on your question.

Q. (By Mr. Chandler) Would it be fair to say a person of ordinary skill in the art knew that sharing data lines was possible between memory devices and different ranks because each memory device has a separate chip select signal so collisions on the shared data line can be avoided? 12:28:18

MR. LINDSAY: Objection. Form. 12:28:40

THE DEPONENT: I would say that a person of skill in the art would be aware of the notion of trying to share multiple devices on a singular line. In terms of how to go about implementing that is a much more specific question and even -- even the references that Dr. Wolfe -- or that I'm responding to that Dr. Wolfe raised are much more complicated than just a single chip select one. 12:28:59

Q. (By Mr. Chandler) A person of ordinary skill in the art would have been familiar with chip 12:29:18

select signals for memory devices, correct? 12:29:21

A. Yeah, I think that's fair. Even yesterday we talked about some of the JEDEC references that go and talk about the chip select signal and how it's described in -- in some ways 12:29:36 that it's used.

Q. Could we turn to one of those JEDEC references marked as Exhibit 1019. I think I put it back in the chat this morning. If not, let me know and I can put it -- put it back. I think I 12:29:48 see it in the chat. So everyone should have access to it, including the court reporter, and just let me know when you've got it up on the screen.

A. I do.

Q. All right. So Exhibit 1019, to refresh 12:30:06 your recollection, is the JESD79-3C standard, dated November 2008, for DDR3 SDRAM memory devices, correct?

A. That's correct.

Q. And at the time of the '060 and '160 12:30:25 patents, a person of ordinary skill in the art would have known about the DDR3 standard marked as Exhibit 1019, correct?

A. Sounds right, yes.

Q. Please turn to page 12 of the DDR3 12:30:43

standard marked as Exhibit 1019 and let me know when you are there. 12:30:46

A. Okay.

Q. And I want focus, for now, on the Figure 2 in the middle of that page. 12:31:02

You got it?

A. Got it.

Q. Figure 2 on page 12 of the JEDEC DDR3 standard marked as Exhibit 1019 illustrates a memory package, including four stacked DDR3 memory chips, correct? 12:31:16

A. Looks like this is talking about a DDR3 SDRAM package and various aspects of it, and it shows -- it looks like it's intending to show the qual-stacked or quad-die DDR3 SDRAM with various -- it looks like various -- some of the signals that go to these various devices. 12:31:45

Q. So there would be four chips or four dies, correct?

A. It looks like the language of Figure 2 is "Qual-stacked/Quad-die DDR3 SDRAM," and it shows the -- the various signaling you would expect for a -- a device. 12:32:13

Q. And "quad" means four, correct?

A. That's correct, yes. 12:32:34

Q. In Figure 2 of page 12 of the DDR3 standard marked as Exhibit 1019, each chip in the stack has its own chip select signal labeled at the bottom as "CS0," "CS1," "CS2," and "CS3" respectively, correct? 12:32:39 12:33:02

A. I see those four -- those four chip select signals, yes.

Q. And each chip in the stack has its own circuitry to output data or to receive data on eight lines labeled at the top as "DQ0-7," correct? 12:33:27

MR. LINDSAY: Objection. Form.

THE DEPONENT: It looks like each of these DDR3 SDRAM devices has the DQ0-7 input/output on it for -- for transmitting data.

Q. (By Mr. Chandler) And those input/output data lines, DQ0 through 7 for each chip, are connected to a common set of data lines that are also labeled "DQ0-7" at the top left of Figure 2, correct? 12:33:58

A. That's how this figure is illustrated; that's correct. 12:34:24

Q. And a person of ordinary skill in the art would understand that this arrangement of stacked memory devices shown on page 2 of the DDR3 standard marked as Exhibit 1019 would be expected to work 12:34:50

without causing collisions on the common set of data lines labeled "DQ0-7" -- and if I said "page 2," I meant page 12 of Exhibit 1019 -- is that correct? 12:34:58

MR. LINDSAY: Objection. Form. 12:35:14

THE DEPONENT: I would say the intent of this Figure 2 on page 12, I would say, would be -- my understanding of the section would be it's informing the reader of how the devices operate when taken in context of this section and signaling and so forth. 12:35:33

Q. (By Mr. Chandler) And a person of ordinary skill in the art, reviewing the stacked memory devices shown on page 12 of the DDR3 standard marked as Exhibit 1019, would expect those stacked memory devices to operate correctly, without collisions, on the set of data lines labeled "DQ0-7," correct? 12:35:54

MR. LINDSAY: Objection. Form.

THE DEPONENT: I think they would understand this figure to be describing one way of implementing this D- -- DDR3 implementation within the confines of JEDEC and, taken as a whole, to provide an operating -- or a correctly operating device -- a functioning operational device per 12:36:15 12:36:41

JEDEC's definition. 12:36:46

Q. (By Mr. Chandler) As a general matter, would you agree that the DDR3 standard, in the time frame of the '060 and '160 patents, was the leading standard for DRAM memory devices commonly used in 12:37:07 the industry for lots and lots of memory devices sold throughout the world?

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would say, at that time frame, that DDR3 devices were used in many, many, 12:37:23 many -- or JEDEC-compliant DDR devices were used in many, many systems and products.

Q. (By Mr. Chandler) Around the entire world, correct?

A. That -- that sounds fair to me, yeah. 12:37:39

Q. All right. Let's look at Exhibit 1022, which I will put in the chat. I think it's a little bit bigger than some of the other exhibits, so it may take a little while to come through, but let me know when you've got it. 12:38:01

A. Okay.

Q. Exhibit 1022 is the textbook by Professor Jacob, correct?

A. That looks correct, yes.

Q. It's titled "Memory Systems: Cache, 12:38:31

DRAM, Disk," correct? 12:38:33

A. That's right.

Q. And you've seen this textbook before, and I believe you cited it yourself, correct?

A. That's correct, maybe in this IPR and, I think, in other matters, at least. 12:38:44

Q. Please turn to page 446 of Exhibit 1022 and let me know when you are there.

A. Okay.

Q. At the bottom of page 446 of the Jacob textbook marked as Exhibit 1022 is Figure 11.23 which shows the timing requirements for a read command following a write command to the same rank of DRAM devices, correct? 12:39:23

A. I see that that's what the title of Figure 11.23 is in this figure. 12:39:52

Q. It was known at the time to a person of ordinary skill in the art how to avoid bus conflicts when a read command follows a write command, right? 12:40:11

A. I'm just reading the column on this page that describes the figure.

It looks like this figure is showing a scenario of a read -- column-read command followed by a column-write command, and, generally, it's 12:41:23

just illustrating the concept that because these two things, the read after the write are going to the same column, you've got to wait till -- it sounds like it's just saying you've got to wait till the write's finished to do this read in this specific scenario that Jacobs is discussing here. 12:41:27 12:41:42

Q. Professor Jacob explains, on the right side of page 446 of Exhibit 1023, that due to the shared I/O circuit inside the memory device, a certain amount of time has to pass between the write command and the read command, correct? 12:42:12

MR. LINDSAY: Objection. Form.

THE DEPONENT: I'm trying to site to your -- I'm about ten lines from the bottom, and it's that sentence the starts: "Since the I/O gating resource is shared..." That is -- what it's saying is, because it's shared between the banks within a rank of DRAM devices, you need to -- the read command that follows the write command must wait until the write command has been completed because of that shared resource. 12:42:43 12:43:06

Q. (By Mr. Chandler) On --

A. The shared I/O gating -- I was just going to say, the shared I/O gating resource.

Q. On the next page, which is page 447 of 12:43:19

Exhibit 1023, the textbook by Professor Jacob goes on to explain that one solution to the, quote, "write-to-read turnaround time," end quote, was to use write buffers, correct? 12:43:23

A. It says -- I'm starting at the first full paragraph -- "In order to alleviate the write-to-read turnaround time illustrated in Figure 11.23, some high-performance DRAM devices such as Rambus Direct RDRAM have been designed with write buffers so that as soon as data has been written into the write buffers, the I/O gating resource can be used by another command such as a column-read command." 12:43:49 12:44:07

Q. So with the use of write buffers, the I/O circuit in the memory device can be used for a read command as soon as data has been written into the write buffers, correct? 12:44:27

A. So, one, this paragraph is mentioning Rambus, which is something we really haven't talked about today, and it's talking about a design with a write buffer and the notion that, well, as soon as data gets written into the -- the write buffer, then that I/O resource can be used for another command, such as a column-read command. So it seems to be indicating a write buffer to handle 12:44:50 12:45:13

aspects of a I/O -- a shared I/O gating resource in this context. 12:45:20

Q. The Jacob textbook was published around 2008 that is shown on page romanette 6, correct?

A. That is correct, yes. 12:46:03

Q. That was several years before the '060 and '160 patents were filed, right?

A. Correct.

Q. So several years before the '060 and '160 patents were filed, Professor Jacob is teaching one way to avoid conflicts between read command and an earlier write command, such as using a write buffer, correct? 12:46:25

MR. LINDSAY: Objection. Form.

THE DEPONENT: In that specific context within Jacob that we just discussed. 12:46:42

Q. (By Mr. Chandler) And the specific context is high-performance DRAM devices, correct?

A. It mentions high-performance DRAM, correct. 12:46:58

Q. If you look at the bottom of page 447 of Exhibit 2020 -- 20- -- 1022, do you see Figure 11.25?

A. Yes.

Q. Figure 11.25, at the bottom of page 447 12:47:14

of Professor Jacob's textbook marked as Exhibit 1022, concerns timing for a read command following a write command to a different rank, correct? 12:47:20

A. The title says "Read following write to different ranks of DRAM devices." 12:47:39

Q. It was known at the time of Professor Jacob's textbook, by 2008, how to avoid bus conflicts when there's a read command following a write command to a different rank of memory devices, correct? 12:48:05

MR. LINDSAY: Objection. Form.

THE DEPONENT: It looks like Figure 11.25 is described as, quote, "shows a slightly different case for a column-read command that follows a column-write command," and goes on to explain in detail. 12:48:20

So this looks like another specific scenario that Dr. Jacob's references is considering here, 11.25, of some kind. 12:48:40

Q. (By Mr. Chandler) Could you turn to the Kim reference marked as Exhibit 1014 and look at Figure 5 and let me know when you are there.

A. Okay -- oh. Okay.

Q. Figure 5 of the Kim reference marked as 12:49:03

Exhibit 1014 illustrates TSVs that are an electrical communication with some, but not all, of the array dies, correct? 12:49:05

A. It's described as schematically illustrating the configuration of a semiconductor memory apparatus in accordance with one embodiment of the invention, and it shows a TSV1 connecting to a C1 and TSV2 connecting to a C2. 12:49:29

Q. In Figure 5 of Kim, marked as Exhibit 1014, TSV1 on the left is not an electrical communication with the array die at the top of the stack, correct? 12:49:53

A. I -- as I recall, Kim just mentions that the TSV is directly connected to C1. I don't recall there being any discussion of a form of connection to C2. 12:50:14

Q. And in Figure 5 of Kim, marked as Exhibit 1014, TSV2 on the right is not an electrical communication with the array die in the middle labeled "C1," correct? 12:50:33

A. I would say that there's just a pathway illustrated in this figure of it connecting to C2; that there's only array -- or one of these Kim memory -- memory C2 or C1 connected to each of the TSVs. 12:50:58

Q. Please turn to paragraph 47 of Kim. Let me know when you are there. 12:50:59

A. Okay.

Q. Paragraph 47 of Kim, marked as Exhibit 1014, states that Figure 5 includes a main chip C0 and slave chips C1 and C2 and that those chips are stacked as shown in Figure 5, correct. 12:51:20

MR. LINDSAY: Objection. Form.

THE DEPONENT: It says that the -- it's a semiconductor memory apparatus, referring to apparatus 3, and it has a main chip C0 and this plurality of slave chips C1 and 2, and the chips C0, C1, and C2 are connected by TSVs. 12:51:51

Q. (By Mr. Chandler) As shown in Figure 5, those chips are stacked vertically, correct? 12:52:09

A. That is the way they are visualized in Figure 5.

Q. As shown in Figure 5 of Kim, marked as Exhibit 1014, each slave chip has its own input/output driving section numbered, for example, 100 and 200, correct? 12:52:33

A. In paragraph 28, the sections 100 and 200 are referred to as first and second input/output driving sections.

Q. In Figure 5 of Kim, marked Exhibit 1014, 12:53:23

ESV1 implements the data lines for GIO_Rank0, and TSV2 implements the data lines for GIO_Rank1, correct? 12:53:26

A. That sounds generally right. The TSV1 is for GIO_Rank0, and TSV2 is for GIO_Rank1. 12:53:55

Q. In Figure 5 of Kim, marked as Exhibit 1014, slave chip C1 is in a first rank called "Rank0," and the other slave chip C2 is in a second rank called "Rank1," correct?

A. That sounds right. I'm going back to paragraph 26, talking about the second data input/output line GIO_Rank1 in a memory bank of a second rank Rank1, et cetera. 12:55:03

Q. Please turn to paragraph 48 of Kim and let me know when you are there. 12:55:25

A. Okay.

Q. In the third sentence of paragraph 48 of Kim, marked as Exhibit 1014, it's disclosed that, quote, "In the 3D semiconductor apparatus in which the plurality of chips are stacked, the plurality of chips may operate individually," end quote. 12:55:58

Did I read that accurately?

A. Yes.

Q. And Kim goes on to state that the "first and second slave chip C1 and C2 may be divided as 12:56:26

first and second ranks Rank0 and Rank1 and be separately operated by chip selection signals CS0 and CS1," correct? 12:56:31

A. That's what the sentence states, yes.

Q. So it would be fair to say that Kim, marked as Exhibit 1014, discloses a stack of memory chips where each chip corresponds to a rank, and each rank can be selected by a chip selection signal, correct? 12:56:52

A. I would say this paragraph of Kim states that in its 3D semiconductor apparatus, there's -- a plurality of chips that are stacked, per the words it uses, and then states that the first and second slave chips C1 and C2 may be divided as first and second ranks and be separately operated by chip selection signals CS0 and CS1, and then goes to show its various figures that discusses this in further detail. 12:57:18 12:57:40

Q. Could you turn to your expert declaration marked as Exhibit 2023 and let me know when you are there. 12:58:06

A. Okay.

Q. Turn to page 51. Let me know when you are there.

A. Okay. 12:58:35

Q. In paragraph 92 of your declaration marked as Exhibit 2023, you have drawn four memory devices that are simultaneously outputting data to the same data lines resulting in a collision, correct? 12:58:48 12:59:05

A. That's correct, yes.

Q. In your opinion, would a person of ordinary skill in the art know that if four memory devices are simultaneously outputting data to the same data lines, that, as a result, there could be a collision? 12:59:20

A. In this high-level example, yes.

Q. Do you believe a person of ordinary skill in the art would be motivated to avoid such a collision? 12:59:39

A. If the collision we are talking about were causing the types of problems I list, you know, damage to circuits or electrical or signal problems, I think they would, yes.

Q. The figure shown in paragraph 92 of your expert declaration marked as Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, correct? 12:59:56

A. That's correct.

Q. In your opinion, a person of ordinary 01:00:16

skill in the art would not have shared a TSV for data signals connected to multiple chips in the same rank, correct? 01:00:17

A. I discuss as to why a person of skill would not do that in the context of Kim, given the solution that Kim -- or in Dr. Wolfe's proposed modifications to Kim, given the -- what Kim discloses to begin with, that it wouldn't work. 01:00:42

Q. And the reason that you state it wouldn't work is because of collisions, correct? 01:01:06

A. As I recall, that's part of the reason I discuss, in light of at least one of Dr. Wolfe's modifications to Kim.

Q. In your opinion, it was known at the time that sharing a TSV for data signals among multiple chips in the same rank could lead to data collisions, correct? 01:01:33

A. That's correct, in the context I discuss in my declaration.

Q. It was also known to a person of ordinary skill in the art that multiple chips in different ranks could share the same data line without causing collisions, correct? 01:02:00

A. In certain contents, correct.

Q. Please turn to page 64. 01:02:32

Do you have page 64 in front of you? 01:02:51

A. Yes.

Q. At the top of page 64 of Exhibit 2023, you created a modified version of Figure 2 of the Kim reference marked as Exhibit 1014, correct? 01:03:16

A. Yes, that's correct.

Q. And, to be clear, the figure at the top of page 64 of Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, correct?

A. That's correct, yes. 01:03:47

Q. In your modified version of Figure 2 of Kim shown on page 64 of your declaration marked as Exhibit 2023, you have added four chips labeled "chip A," "chip B," "chip C," and "chip D," correct? 01:04:06

A. Correct.

Q. And the way that you have modified Figure 2 of Kim at the top of page 64 of your declaration marked as Exhibit 2023 is inconsistent with the disclosure of Kim because you have chip C in Rank0 connecting to GIO_Rank1, correct? 01:04:27

A. I would say that this figure is intended to visualize one of the modifications to Kim that Dr. Wolfe presented in his deposition.

Q. Well, to be clear, just so there's no 01:05:02

misunderstanding, Dr. Wolfe did not present the figure shown at the top of page 64 of your declaration marked as Exhibit 2023, but, rather, that figure is your characterization of what Dr. Wolfe was talking about, correct? 01:05:05 01:05:18

A. I would say it's my visualization of what I'm understanding him to say in his deposition.

Q. Kim, marked as Exhibit 1014, does not teach having a chip in Rank0 connected to GIO_Rank1 and does not teach having a chip in Rank1 connected to GIO_Rank0 as you have shown at the top of page 64 of your declaration marked as Exhibit 2023, correct? 01:05:44

A. I don't believe Kim explicitly teaches that, no. 01:06:05

Q. In your opinion, if Kim were modified such that a chip in Rank0 were connected to GIO_Rank1 and a chip in Rank1 were connected to GIO_Rank0, the result of that could be collisions, correct? 01:06:47

A. As I discuss in my declaration, there are a few different adverse-effect scenarios that occur. I think collisions was one. Perhaps loss of data was another one, depending on how things are operating. 01:07:04

Q. And, in general, a person of ordinary skill in the art would be motivated to avoid collisions and loss of data; is that fair? 01:07:08

A. As we have talked about earlier today and yesterday, in a general sense, I think that's -- that's fair. 01:07:20

Q. Could you please turn to page 68 of your declaration and let me know when you are there.

A. Okay.

Q. In the middle of page 68 of your declaration marked as Exhibit 2023, you have created another modified version of Figure 2 of Kim marked as Exhibit 1014, correct? 01:07:50

A. That is correct. The intent was for me to visualize another modification to Kim that Dr. Wolfe expressed in his deposition, as I recall. 01:08:13

Q. And, to be clear, the figure in the middle of page 68 in your declaration marked as Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, correct? 01:08:35

A. That's correct.

Q. And you did not show this figure to Dr. Wolfe and ask him if it's an accurate representation of his opinions, correct?

A. I -- I, personally, haven't communicated 01:09:01

with him on this matter. 01:09:03

Q. And as far as you know -- as far as you know, nobody showed the figures that you created in your declaration marked as Exhibit 2023 to Dr. Wolfe to ask him if those figures accurately 01:09:14 represented his opinions, correct?

A. I am -- I am not aware one way or the other, sure.

Q. Could you turn to page 70 of your declaration and let me know when you are there. 01:09:41

At the top of page 70 of your expert declaration marked as Exhibit 2023, you have made a four-rank modification of Figure 2 of Kim marked as Exhibit 1014, correct?

A. I created this figure, again, as I 01:10:17 recall, to visualize what I understood as another modification to Kim that Dr. Wolfe proposed in his deposition.

Q. But, to be clear, the figure at the top of page 70 of your declaration marked as 01:10:37 Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, and was never shown to Dr. Wolfe for him to confirm whether or not it actually accurately represents his opinions, correct?

A. I would say that I -- this -- this figure 01:11:02

was created by me; you're right. And to the second part of your question, similar to before, I don't know one way or the other if this was presented to Dr. Wolfe at some point in time. 01:11:05

Q. In your four-rank version of Figure 2 of Kim shown at the top of page 70 of your expert declaration marked as Exhibit 2023, you assume that Kim's circuits would operate the same way as in Kim's original Figure 2, correct? 01:11:18

A. That is correct, as I recall figure -- the -- the earlier figures of Kim. 01:11:46

Q. For example, in your modification shown at the top of page 70 of Exhibit 2023, even though you modify Figure 2 of Kim to have four ranks of memory devices, you only show two chip select signals, CS0 and CS1, received by the shared data I/O circuit 1000, and you don't show anywhere in this figure that there would be four chips of select signals, correct? 01:12:10

MR. LINDSAY: Objection. Form. 01:12:36

THE DEPONENT: I don't -- as I recall, Dr. Wolfe didn't articulate anything about additional chip select signals that would relate to what this figure is visualizing.

Q. (By Mr. Lindsay) And you have not shown 01:12:56

or addressed whether or not there would be four chip select signals in your four-rank modified version of Figure 2 of Kim shown at the top of page 70 of your declaration marked as Exhibit 2023, correct? 01:12:59 01:13:15

A. Dr. Wolfe didn't offer that in his modification to Kim. I am simply addressing what he proposed.

Q. Well, to be clear, you are addressing what you are characterizing he proposed. 01:13:27

You never asked him -- and I don't believe Netlist ever asked him -- whether there would be four chip select signals if there are four ranks, correct?

MR. LINDSAY: Objection. Form. 01:13:44

THE DEPONENT: I'm going -- my -- my visualization here is what Dr. Wolfe, my understanding, has testified to under oath. I don't recall the exact line of question and answers. If I've mischaracterized it, I would be happy to bring up his deposition transcript, perhaps -- if you think he mentioned additional chip select. I don't recall that. 01:13:57

Q. (By Mr. Chandler) Do you recall anyone asking him how many chip select signals would be 01:14:09

used for a four-rank memory module? 01:14:12

A. I -- I don't recall all of his, if I remember, two days of deposition testimony. I would think, though, if he had offered that information, I would have certainly -- my intention 01:14:27 would be to -- have included it in this visualization.

Q. In paragraph 122 -- why don't you just briefly review paragraph 122 of your declaration and let me know when you're -- you're ready. 01:15:04

A. Okay.

Okay.

Q. Your conclusion, with respect to the four-rank modification of Figure 2 of Kim shown at the top of page 70 of your expert declaration 01:15:34 marked as Exhibit 2023, is that that modification would work the same way as described with reference to Figure 1 of Kim thus resulting in, quote, "unavoidable data collisions," correct?

A. That the unavoidable data collision that 01:16:01 Kim talks about would be present -- would be, again, present in this solution in -- in the figure at the top of page 70.

Q. At the end of paragraph 122 of your expert declaration marked as Exhibit 2023, you 01:16:21

created another figure, correct? 01:16:26

A. That's -- that's correct.

Q. On the left side of the figure shown in the top of page 71 of your expert declaration marked as Exhibit 2023 is Figure 1 of Kim 01:16:41 describing the prior art at the time, and then, on the right, you added an equal sign, and then, to the right of that, you added what you characterize Dr. Wolfe was proposing, correct?

A. That is a visualization of what he was 01:17:15 proposing in relation to this modification that he discussed.

Q. And it's your characterization of what he was proposing. You and Netlist never showed the figure on page 71 of Exhibit 2023 to Dr. Wolfe, 01:17:35 correct?

A. I am unaware if it was shown to him or not. It was my intent to visualize -- to create a visualization for exactly what he was saying in his deposition. 01:17:57

Q. So, to be clear, the figure shown towards the top of page 71 of your expert declaration marked as Exhibit 2023 is something that you created, not something that Dr. Wolfe or Samsung created, correct? 01:18:21

A. The figure itself, yes, that's correct. 01:18:24

Q. And the figures that you created in your expert declaration marked as Exhibit 2023, you created them after Dr. Wolfe's deposition, meaning the -- neither you nor Netlist could have shown them to Dr. Wolfe during his deposition, right? 01:18:38

MR. LINDSAY: Objection. Form.

THE DEPONENT: The figures we have been discussing for the last half hour or so, yes, I created those after what I understand was Dr. Wolfe's deposition -- or his sort of one and only deposition, after reviewing that transcript. I really don't know if they may have present -- may have been presented to him. I'm guessing he read my report, but they -- they would have been generated by me after that either one and only or first deposition I reviewed. 01:18:57 01:19:16

Q. (By Mr. Chandler) Please turn to page 76 of your declaration and let me know when you are there. 01:19:39

A. Okay.

Q. At the top of page 76 of your expert declaration marked as Exhibit 2023, you have created another modification to Kim's figures, correct? 01:20:04

A. That is correct. 01:20:09

Q. And, to be clear, the modified version of Kim at the top of page 76 of your expert declaration marked as Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, correct? 01:20:22

A. The figures themselves, yes.

Q. And you are not aware of anyone ever showing those modified figures or variations of those modified figures to Dr. Wolfe during his deposition so that he could comment on whether or not they accurately represent his opinions, correct? 01:20:47

A. I am not aware of the figures being shown to Dr. Wolfe one way or the other.

Q. In forming your opinions in your expert declaration marked as Exhibit 2023, you relied on your modified figures of Kim which are not part of Dr. Wolfe's declarations and not part of Samsung's petitions, correct? 01:21:09

MR. LINDSAY: Objection. Form. 01:21:31

THE DEPONENT: I relied on Dr. Wolfe's, I would say, declaration and deposition testimony, parts of which I visualized in these figures.

Q. (By Mr. Chandler) And, again, to be clear, these modified figures in your expert 01:21:51

declaration marked as Exhibit 2023 are -- are your characterizations of Dr. Wolfe's opinions and are not actually figures that either Dr. Wolfe or Samsung has ever presented, correct? 01:21:54

MR. LINDSAY: Objection. Asked and answered. Form. 01:22:11

THE DEPONENT: They're -- they are figures representing my understanding of what Dr. Wolfe was articulating in his report -- or dep- -- or declaration and, I think, more specifically his deposition. I don't -- they were not created by Samsung or Dr. Wolfe. I don't know if they have been presented to Samsung or Dr. Wolfe one way or the other. 01:22:22

MR. CHANDLER: Why don't we take a break, but before you run away after the videographer gets us off the record, we should chat about how long the break should be. 01:22:53

THE DEPONENT: Okay.

THE VIDEOGRAPHER: We are off the record at 1:23 p.m. 01:23:02

(Recess taken.)

THE VIDEOGRAPHER: We are back on the record at 2:15 p.m.

Q. (By Mr. Chandler) Dr. Brogioli, do you 02:15:21

have any corrections or clarifications you would like to make to your earlier testimony? 02:15:22

A. Not at this time, no.

Q. Could you pull up Exhibit 1017, which is the Wyman reference, and I put it in the chat at the beginning of the day. 02:15:47

A. Okay.

Q. And please turn to Figure 5. Let me know when you are there.

A. Okay. 02:16:21

Q. In Figure 5 of the Wyman reference marked as Exhibit 1017, the signal will come from the left side of the figure and can be output at any of the tap-off locations, T0, T1, T2 or T3, as well as 508 on the right, correct? 02:16:49

A. That's right, the -- the five tap-off locations that Wyman refers to.

Q. In Figure 5 of Wyman marked as Exhibit 1017, if only the driver 502-1 is enabled, the input signal is driven only by driver 502-1 to tap T1, correct? 02:17:26

A. I am just rereading the section of Wyman.

So it looks like if only the 502-1 driver is off, you would be using the T1, or 506-2 tap, to get that output value. 02:18:20

Q. And the transcript, I think, didn't accurately get your testimony. I think you said if only 502-1 is "on," not "off" but "on," correct? 02:18:26

A. That -- that's correct, yes.

Q. So for clarity, could you give your answer again. 02:18:47

A. I was saying that if -- if only the 502-1 driver is on, one would use the -- you could use 506-2 tap to get a -- a value output.

Q. So in the situation where only driver 502-1 is enabled, the signal is driven only by driver 502-1 to tap T1, which is also labeled "506-2"; is that correct? 02:19:15

A. That appears to be at least what Figure 5 is illustrating. 02:19:41

Q. And if Figure 5 of Wyman marked as Exhibit 1017, if only drivers 502-1 and 502-2 are enabled, the input signal is driven by both driver 502-1 to tap T1 marked as "506-2," and driver 502-2 will drive to tap T2 marked as "506-3," correct? 02:20:10

A. I think that sounds right, in -- Wyman talked about different configurations or -- different configurations of the different drivers to divide up the driver level.

Q. So in Figure 5 of Wyman marked as 02:20:47

Exhibit 1017, tap T2 labeled "506-3" can be selected as the output driven both drivers 502-1 and 502-2, correct? 02:20:49

A. That's my -- that is my recollection; that's right. You could pull the T2 or 506-3 tap which would be including a signal coming from ENB1 and ENB0. 02:21:21

Q. For clarity, I think you just misspoke. The -- the ENB is referring to the --

A. You're right. 02:22:07

Q. -- a name --

A. You're right. I -- I -- let me reanswer.

If -- if you're -- the output at tap T2, or 506-3, would be a signal compromising the -- the driver triangles we see in 502-2 and 502-1. 02:22:21

Q. And just to do one more example from Figure 5 of Wyman marked as Exhibit 1017, if only drivers 502-1, 502-2 and 502-3 are enabled, then the same input signal is driven by driver 502-1 to tap T1, driver 502-2 to tap T2, and driver 502-3 to tap T3, correct? 02:22:47

A. There are -- I would say that those drivers are used to generate a signal available on those various taps, as I recall.

Q. Thus, in that example of Figure 5 of 02:23:16

Wyman marked as Exhibit 1017, tap T3 can be selected as the output driven by drivers 502-1, 506-2, and 502-3, correct? 02:23:19

A. The driver -- those driver components within Figure 5, yes. 02:23:36

Q. In Figure 5 of Wyman marked as Exhibit 1017, in the example where the output is tapped off at T2, the driver size is larger than when the output is tapped off at T1, correct?

A. No. The driver size of Wyman is the fixed driver that Wyman talks about. It's -- Figure 5 just gives you various output level selections that you can select from its Figure 5 circuit. 02:24:16

Q. Take a look at Figures 3 and 4 of Wyman and let me know when you are there. 02:24:35

A. Okay.

Q. The driver size in Figure 4 of Wyman, in your opinion, is larger than the driver size in Figure 3 of Wyman, correct? 02:24:54

A. It looks like, at least the way these two figures are visualized, Figure 4 has more stages to it than Figure 3 --

Q. And would you consider --

A. -- so -- 02:25:14

Q. Oh, sorry, go ahead. 02:25:16
A. I would say the -- the universe of functionality, there are more components in Figure 3 than in Figure 4.
Q. Is the driver size in Figure 4 of Wyman larger than the driver size in Figure 3 of Wyman marked as Exhibit 1017? 02:25:29
A. I -- I don't think I performed -- well, if your question is in terms of physical size, I don't know that I have performed an analysis comparing Figure 3 of Wyman to Figure 4 of Wyman. They both represent a driver in Wyman. 02:25:46
Q. I was asking about driver size.
A. Right. I don't -- I don't recall an analysis of whether -- what constitutes Wyman's Figure 3 driver must be, for example, physically larger or smaller than the Figure 4 driver of Wyman. 02:26:13
Q. What is "driver size"?
A. It could be the physical size of a driver. It could be -- if you are looking at the power output, things of that nature. 02:26:33
Q. And in the context of the '060 and '160 patents, what is "driver size"?
A. As I recall, it's talking about using a 02:26:55

small -- in cases of using a smaller driver for instances where you may not need as much power, things like that, you can use something physically smaller. 02:26:59

Q. In general, is there -- or can there be a correlation between the physical size of the driver and the amount of power associated with the driver? 02:27:21

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would say, in a general sense, perhaps, if someone is looking at transistor sizes to drive a signal, and things like that. 02:27:40

Q. (By Mr. Chandler) The only reason I ask is because when I asked you about driver size in context of the '060 and '160 patents, you seem to be referring to both physical size and the amount of power, so it was unclear to me if you were suggesting that driver size is one or the other or both or if they are correlated, and, therefore, it doesn't make a difference. 02:28:00

MR. LINDSAY: Objection. Form. 02:28:20

THE DEPONENT: I would say that they are generally related.

Q. (By Mr. Chandler) Could you look at Figure 7 of Wyman. Let me know when you are there.

A. Okay. 02:28:58

Q. And you may want to look at the description of Figure 7 and 8 briefly and just let me know when you are ready. 02:29:19

A. Sure. Give me one moment.

Q. And you don't have to go all through Figure 8A and all that. Just -- just look at Figure 7 and 8. And, if you want, you can look at the corresponding description and just let me know when you are ready. 02:29:31

A. Okay. One minute. 02:29:42

Okay. Go ahead.

Q. Figure 8 of Wyman marked as Exhibit 1017 shows different cross-sections of Figure 7, correct?

A. It says it's the cross-sections of the chips in Figure 7. 02:30:29

Q. And how would you explain to a layperson what Wyman is teaching with Figures 7 and 8?

A. So it's saying that Figure 7 is a simplified form of a stack and that it's talking about drive in relation to capacitance, resistance, and so forth. 02:31:07

And then Figure 8 shows cross-sections of Figure 7.

And then it mentions Figure 8A in a 02:31:54

scenario of -- the connection would require minimal drive and refers -- talking about how the driver in Figure 5 is used in this scenario. 02:31:58

Q. In Figure 8, would it be fair to call 802, 804, 806, 808 TSVs? 02:32:39

A. I -- that may be what it's referring to. In column 6, it's referring to this through-chip via connection.

Q. And is a TSV a type of through-chip via connection? 02:33:07

A. Oh, we have talked about the through-silicon via yesterday and today. We may be talking about the same thing.

Q. Could you go to your expert declaration and go to paragraph 94 and let me know when you are there. 02:33:35

A. Okay.

Q. In paragraph 94 of your expert declaration marked as Exhibit 2023, you cite to page 413 of the Jacob textbook marked as Exhibit 1022 as shown at the bottom of that paragraph, correct? 02:34:16

A. That looks right, yes.

Q. And you state that "normally, in a JEDEC-compliant DIMM, when a read or write command 02:34:35

is sent, devices in the rank selected by the chip select signal would output or receive data bits simultaneously in parallel with each bit accessed in an access cycle carried on a separate data line to a separate data terminal, as illustrated below and as would" be "understood by a person of ordinary skill in the art," correct? 02:34:39 02:34:54

A. That's -- that's right.

Q. And then can we look at the page that you cited from the Jacob's textbook and let me know what you are there. 02:35:12

A. 413. Okay.

Q. And you believe the description by Professor Jacob of ranks in section 10.2.2 of his textbook marked as Exhibit 1022 is consistent with the understanding of a person of ordinary skill in the art? 02:35:52

A. That he seems to be addressing, on this page, some of the ambiguity between rank and bank but then explains that the word "rank" being used for a set of DRAM devices that are performing a read or write together. So, at a high level, this seems accurate. 02:36:31

Q. So, at a high level, Professor Jacob's descriptions of rank in section 10.2.2 of his 02:36:58

textbook marked as Exhibit 1022, you would say, is -- accurately represents the understanding of a person of ordinary skill in the art? 02:37:02

A. It seems to be at the time that this was written in terms of addressing some of the ambiguity between bank and rank in illustrating in his reference, at least in this section at this time, what a rank is as shown in the figure. 02:37:20

Q. And with respect to what you described as the ambiguity between bank and rank, there was a time when the phrase "physical bank" was used, and now, according to Professor Jacob, the more preferred term for the same concept is "rank," correct? 02:37:46

A. That's more or less what was going on. I think other -- other experts for Samsung have, and myself have, generally been in agreement in -- in that -- have been in agreement on that -- that point. 02:38:11

Q. Netlist did not invent SDRAM memory devices, correct? 02:38:54

A. I would say in the -- at least in the context of my engagement, I don't recall them stating on paper or publications that they invented the SDRAM memory device. 02:39:17

Q. In other words, SDRAM memory devices were known before the '160 and '060 patents, right? 02:39:21

A. Yes, that's right.

Q. And Netlist did not invent DDR memory devices, including DDR1 or DDR2 or DDR3, correct? 02:39:36

A. I don't recall seeing in my -- in the materials I reviewed or the -- the patents that I have worked on Netlist claiming to have invented that.

Q. DDR memory devices, such as DDR1, DDR2, and DDR3, were known before the '160 and '060 patents, correct? 02:39:55

A. That's correct.

Q. Netlist did not invent non-volatile memory, correct? 02:40:10

A. Not that I have seen in my -- my role. I don't recall the materials I have reviewed claiming that.

Q. Non-volatile memory was known before the '160 and the '060 patents, correct? 02:40:25

A. That's correct.

Q. Netlist did not invent SRAM memory, correct?

A. I don't recall them claiming to have done that. I haven't seen evidence of that either. 02:40:40

Q. SRAM memory devices were known before the '160 and the '060 patents, correct? 02:40:48

A. That's correct.

Q. Netlist did not invest memory packages such as DRAM packages, correct? 02:41:01

A. I don't recall Netlist claiming to have invented that or I don't recall, myself, seeing information of -- of -- of that type either.

Q. Memory packages, such as DRAM packages, were known before the '160 and the '060 patents, correct? 02:41:22

A. That's correct.

Q. Netlist did not invent through-silicon via, abbreviated "TSVs," correct?

A. I think that's correct. There were references discussing forms or uses of -- of TSVs in the path. 02:41:42

Q. TSVs were known before the '160 and the '060 patents, correct?

A. That's correct. 02:42:05

Q. Netlist did not invent array dies, correct?

A. I -- I don't know if I have formed an opinion on that one way or the other if we are talking about the array dies as contemplated in 02:42:27

the -- in these patents. 02:42:30

Q. As we discussed earlier, the '060 and '160 patents, each of the array dies can be SDRAM or non-volatile memory or SRAM memory, all of which existed before the '160 and the '060 patents, 02:42:44 correct?

A. Those types of memory technology, for example, SRAM or DRAM itself, were known prior to these patents; that's correct.

Q. Do you have any corrections or 02:43:05 clarifications you would like to make to any of your testimony earlier today or yesterday?

A. Not that I have right now, no.

MR. CHANDLER: All right. I will pass the witness. 02:43:20

MR. LINDSAY: Okay. I will need some time to go through notes from yesterday and today. Can we take maybe half hour?

MR. CHANDLER: Sure.

THE VIDEOGRAPHER: Off the record, 02:43:43 Counsel?

MR. CHANDLER: Yes.

THE VIDEOGRAPHER: We are off the record at 2:43 p.m.

(Recess taken.) 02:48:31

THE VIDEOGRAPHER: We are back on the record at 3:16 p.m. 03:16:46

EXAMINATION

BY MR. LINDSAY:

Q. Dr. Brogioli, do you recall yesterday discussing with counsel the Riho reference, Exhibit 1016, and whether there were electrical communication between TSV715 or TSV08 with certain SDRAM dies? 03:16:53

A. I generally recall a discussion around that. Pulling up Riho now. 03:17:22

Okay. I have it up.

Q. Okay. If you could take a look at paragraph 112 discussing Figure 8A?

A. Okay. 03:18:00

Q. Can you -- sorry.

A. Go ahead.

Q. Can you read the last sentence of that paragraph 112, please.

MR. CHANDLER: Objection. Leading. 03:18:11

THE DEPONENT: And you are -- you are asking paragraph 112 of Riho, correct?

MR. LINDSAY: Yes. Correct.

THE DEPONENT: The last sentence states: "Therefore, the SDRAM D15 is in a state completely 03:18:20

disconnected from the data signal DQ TSV715." 03:18:25

Q. (By Mr. Lindsay) Okay. And the '060 and '160 patents mention both electrical connection and electrical communication?

A. That's correct. 03:18:47

Q. So applying the same meaning of the '060 patent for the term "electrical connection," is there electrical connection between DQ TSV715 and at least a portion of the SDRAM D15?

A. Yes, there is. 03:19:20

Q. And which -- so which portion of SDRAM D15 is DQ TSV715 electronically connected to if you looked at Figure 8A of Riho?

A. It would be the CSI5 with a block here showing -- encompassing the SA and SB switch. 03:19:51

Q. Okay. And if we look at Figure 5 of Riho next, again, applying the same meaning of electrical connection as in the '060 and '160 patents, is TSV715 electronically connected to any portion of the SDRAM D14? 03:20:34

A. Yes, it is. It would be the same scenario where it is -- it is connected to that same SDRAM -- electronically connected.

Q. And what -- what portion would be electronically connected? If you want to refer 03:21:05

Figure 8A, that's fine, or Figure 5. 03:21:09

A. It would be at least that same portion of the -- I think the CS15 block shown here with the SA and SB components as part of it.

Q. Okay. If we could take a look at your -- 03:21:28
your declaration for a moment, Exhibit 1023 [sic], paragraph 251 -- I will get there as well -- which is on page 156, and it continues with a figure onto page 157.

A. Okay. 03:21:56

Q. Does this paragraph and the accompanying figure explain one reason why you concluded that there is an electrical connection between Riho's TSVs and each of the SDRAM dies when switches SA and SB are turned off? 03:22:24

A. It is. This -- this section is, in fact, talking about just that; that even when this transmission gate is off or if the switch were off, there's still signals between that TSV we have been talking about and the input stages and that -- and, 03:22:44
thus, there's the -- there's electrical connections and electrical communication.

Q. Okay. If I could direct your attention to the Ruckerbauer reference Exhibit 1024 and, in particular, Figure 5A and -- 03:23:12

A. One second. 03:23:19
Q. -- there's some disclosure around that if you want to take a look at paragraph 9 -- I'm sorry, column 9, line 66, and that continues to column 10, line 8 or so. 03:23:37
A. Okay.
MR. CHANDLER: Just one moment. I need to pull that back up, if you give me one second.
Got it, so the end of column 9, top of column 10? 03:24:18
MR. LINDSAY: Yes.
MR. CHANDLER: Okay.
Q. (By Mr. Lindsay) According to Ruckerbauer, what do the solid lines between the bidirectional buffer and the TSV mean? 03:24:36
A. That in the case of the solid line -- I'm trying to find the exact language Ruckerbauer uses.
The -- as I recall, the solid line, as we see here in 5A, is the ability to have that switch enabled to effectively send data back and forth, if you will. 03:25:11
Q. Okay. And then with respect to the dash lines, what's the significance of Ruckerbauer's use of the dash lines?
A. That there's still -- as this 03:25:30

paragraph -- bottom of -- I think we are in column 10 -- 9, top of column 10, that there's still a connection there, but they're -- it's turned off, so you are not able to send data bits, for example, back and forth, or the enable signal is -- is saying it's off. 03:25:32 03:25:45

Q. So there would be -- is it accurate to say there would be a physical connection between the buffer and the TSV but that the physical connection is not used for electrical coupling? 03:26:07

MR. CHANDLER: Objection. Leading.

THE DEPONENT: I would say, yes, that's roughly what -- that's what Ruckerbauer gets at at the top of column 10 where, I guess, at line 6 is saying, "To illustrate the implemented coupling, solid lines are used in the figures, whereas dashed lines indicate existing physical connections, which are not used for an electrical coupling." 03:26:22

Q. (By Mr. Lindsay) So using the same meaning of electrical connection as in the '060 and '160 patent where a buffer is illustrated as physically connected to a TSV but not used for electrical coupling, is there an electrical connection between the TSV and the buffer? 03:26:38

MR. CHANDLER: Objection. Leading. 03:27:02

THE DEPONENT: Yes, there is in Ruckerbauer. 03:27:03

Q. (By Mr. Lindsay) And -- and so why -- why would there be an electrical connection still between the buffer and the TSV? 03:27:19

A. Well, because, as we discussed earlier, there's still this physical pathway and connection between the TSV and buffer, and so there's still an electrical connection there regardless of the enable signal. 03:27:33

Q. Okay. Would there be an electrical connection to at least the input stage of that bidirectional buffer?

A. Yes, there would; that's right.

Q. And so would -- the TSV is still going to experience the -- the load that's presented by the buffer? 03:27:51

MR. LINDSAY: Objection. Leading.

THE DEPONENT: Yes, that's -- that's correct, and that's -- I think it was paragraph 251, perhaps, of my declaration that talks about that same -- that same concept. 03:28:06

MR. LINDSAY: Okay. If we can take a look at Ellsberry next and --

MR. CHANDLER: What exhibit? 03:28:47

MR. LINDSAY: 1026, Figure -- Figure 2. 03:28:49

THE DEPONENT: Okay.

Q. (By Mr. Lindsay) So looking at Figure 2, you see a -- connected to switch ASIC 208, there's a bank 3 and bank 1? 03:29:19

A. Yes.

Q. Do bank 3 and bank 1 present a capacitive load to bus 234 that's shown above switch ASIC 206?

A. No.

Q. Okay. I think that's all I have on Ellsberry, if you next open up Exhibit 1015 for me, Rajan. 03:29:52

A. Okay.

Q. Do you recall discussing with counsel yesterday certain timing diagrams in -- in Rajan? 03:30:22

A. I do, yes.

Q. Do you recall questions yesterday regarding latency, other than the actual latency of a device may be presented to the memory controller?

A. Yes, I do. 03:30:46

Q. Would -- would such an approach resolve the unavoidable data collisions in the Kim reference where it's doing cross rank, read-after-write operation?

MR. CHANDLER: Objection. Leading. 03:31:05

THE DEPONENT: No, and just providing a value to the memory controller doesn't solve the -- the scenario that Kim contemplates of the read-after-these-write operations. 03:31:07

Q. (By Mr. Lindsay) Do you also recall discussing with counsel yesterday Exhibit 1019, which is the DDR3 SDRAM JEDEC specification, in particular, a -- certain timing diagrams in Exhibit 1019? 03:31:35

A. I do, yes. 03:31:58

Q. Does the device in Kim -- in the Kim reference follow the timing diagrams of Exhibit 1019?

A. No. That -- my -- that's not my understanding. Kim has its own timing illustrations. 03:32:13

Q. Separate topic.

Do you recall discussions with counsel yesterday regarding whether a POSITA would have been able to carry out the mention of the '060 and '160 patents where the array die is an SRAM or NAND? 03:32:31

A. I -- I remember that line of questioning, yes.

Q. Would a POSITA interpret the '060 or 03:32:49

'160 patent, or any of the prior-art references even, as suggesting using NAND or SRAM as the array die and implementing a DRAM interface on the logic -- logic die? 03:32:54

MR. CHANDLER: Objection. Vague. And also objection. Leading. 03:33:13

THE DEPONENT: I would say no, and that's -- I have a -- a fairly lengthy discussion in my declaration as to -- to various challenges and aspects with -- with that -- or related to that. 03:33:25

Q. (By Mr. Lindsay) And I will just switch gears, and, next, if you could take a look at and pull up Exhibit 1022. This is the Jacob publication. 03:33:52

A. Okay. One second.

Okay.

Q. Okay. And, in particular, if you could turn to page 413 of the -- of the text.

A. Okay. 03:34:16

Q. Do you recall discussing this paragraph -- the section 10.2.2 earlier today with Mr. Chandler?

A. Yes.

Q. And in this paragraph, Jacob describes a 03:34:37

couple different things. In paragraph -- I'm sorry, in sentence 2, Jacob says that a rank of memory is a bank of one or more DRAM devices that operate in lockstep in response to a given command. 03:34:45

Did I read that right? 03:35:06

A. Yes, I believe so.

Q. And then a couple of sentences down, Jacob then says that the word "rank" is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory device -- in a memory system; is that right? 03:35:25

A. That's right, yes.

MR. CHANDLER: Objection.

Q. (By Mr. Lindsay) So earlier today when you were providing answers about this paragraph and whether you agreed with it or not, were you agreeing with the last part that I just read, where rank is being used to denote a set of DRAM devices? 03:35:41

A. Yes, and that's what I have used in various part of my declarations, the later -- I think the last sentence of that paragraph. 03:36:06

Q. So just to be clear, you were not agreeing with any sort of reading of the second sentence that might be construed to include one DRAM device in a rank? 03:36:27

MR. CHANDLER: Objection. Leading. 03:36:31
THE DEPONENT: That's right, yes.
MR. LINDSAY: Okay. Nothing further from me.
MR. CHANDLER: Let's go off the record. 03:36:41
I want to check my notes.
THE VIDEOGRAPHER: We are off the record at 3:36 p.m.
(Recess taken.)
THE VIDEOGRAPHER: We are back on the 04:01:54
record at 4:01 p.m.

FURTHER EXAMINATION

BY MR. CHANDLER:

Q. Dr. Brogioli, I would like to follow up on some of the questions that counsel for Netlist 04:02:06
asked you, starting with the Ellsberry reference marked as Exhibit 1026, Figure 2.
Could you pull that up?
A. Okay.
Q. Yesterday, we had a pretty lengthy 04:02:26
discussion about Ellsberry and capacitive load presented by banks of memory devices; is that fair?
A. I recall portions of that anyway.
Q. And I asked if you had any clarifications to your testimony, and you told me yesterday that 04:02:47

you didn't, correct? 04:02:48

A. That's right.

Q. But then this afternoon, counsel for Netlist asked you similar questions about Figure 2, and you gave testimony that was different from the 04:02:59 testimony that you gave to me, correct, yesterday?

MR. LINDSAY: Objection. Misstates prior testimony. Form.

THE DEPONENT: I don't think so, no.

Q. (By Mr. Chandler) So you think the 04:03:20 testimony that you gave counsel for Netlist today was consistent with what you were telling me yesterday?

A. If I recall the various questions that you were asking, I think it was yesterday, and the 04:03:36 one -- I think it was one question I was asked today, I don't think there was any inconsistency there.

Q. In Figure 2 of Ellsberry, memory banks 1 and 2 present a capacitive load on the data bus 236 04:03:57 but not onto data bus 234, correct?

A. I am saying that -- banks [sic] 3 and bank 1 not being connected to 234 wouldn't present anything, and then you and I went back and forth yesterday, as I recall, about a bank 3 and a bank 1 04:04:27

connected to bus 236 and what Ellsberry did or did not disclose or what might be true, in a general sense, that a POSITA might consider. 04:04:31

Q. So you agree that, in Figure 2 of Ellsberry, memory banks 1 and 3 are not presenting a capacitive load onto the data bus 234? 04:04:52

A. I would say that Figure 2, to me, is -- seems to be illustrating that they are not connected to 234 in any way.

Q. In Figure 2 of Ellsberry, memory banks 1 and 3 are not an electrical communication with data bus 234, correct? 04:05:15

A. I don't think I have addressed that in my declaration, but it doesn't look to me like they are physically connected to it whatsoever. 04:05:32

Q. And they not electronically connected either, right?

A. I don't think Ellsberry intends for Figure 2 to show something like that.

Q. And there's no indication of any electrical communication between memory banks 1 and 3 and data bus 234 in Figure 2 of Ellsberry, correct? 04:05:53

A. I don't recall Ellsberry trying to convey that. For example, in Figure 2, memory bank 1 is 04:06:11

actually communicating over bus 234. 04:06:15

Q. In your opinion -- and I should back up. I am going to ask a question that's not necessarily specific to -- to Figure 2 of Ellsberry, so I don't want you to get too hung up on Figure 2 of 04:06:43
Ellsberry for the -- the next question, understood?

A. Okay.

Q. In your opinion, if an electrical load is presented, does that mean that there is electrical communication? 04:07:03

MR. LINDSAY: Objection. Form.

THE DEPONENT: I haven't -- I haven't formed an opinion on all scenarios that may encompass the question you are talking about.

Q. (By Mr. Chandler) Well, then, can you 04:07:25
explain to me what you understand "electrical communication" to mean?

A. Well, examples of it are just as I've talked about today and in my declaration.

Q. I'm not asking for examples. I am trying 04:07:37
to get your definition of "electrical communication" consistent with the '060 and '160 patents.

MR. LINDSAY: Objection. Form.

THE DEPONENT: I mean, I would go right 04:07:48

back to the '060 patent for you, and we can look at the language discussing electrical communication. 04:07:50

Q. (By Mr. Chandler) Unfortunately, Dr. Brogioli, despite the language in the patent, which we have all read, there still seems to be some disagreement between you and Dr. Wolfe as to what electrical communication requires. 04:08:00

So I am interested in your opinions and your definition that you applied in your declaration in forming your opinions as to what is "electrical communication"? 04:08:14

MR. LINDSAY: Objection. Form.

THE DEPONENT: I don't recall offering construction of what "electrical communication" means in this proceeding. I have certainly talked about it at length in my declaration of various aspects of, for example, certain transmissions dates and things that Dr. Wolfe has pointed to and aspects of them that show electrical communication. 04:08:32

Q. (By Mr. Chandler) In our conversation yesterday, you often suggested to me that if there's an electrical load, that means there's electrical communication, and so I am trying to get clarity on whether that is, in your mind, how you know if something is an electrical communication or 04:09:00 04:09:24

not, is whether you look at the load? 04:09:27

MR. LINDSAY: Objection. Form.

THE DEPONENT: You seem to be asking a very broad question that I -- isn't something I have addressed in my declaration. 04:09:41

Again, I'm -- I'm am addressing a number of points that Dr. Wolfe raised in my declaration. My intent is not to provide a universal definition for, potentially, references I -- how they may relate to references I haven't even seen. 04:09:59

Q. (By Mr. Chandler) I am talking about the '060, '160 patent and the claims that use the phrase "electrical communication," and so we -- we need a construction and understanding of what those claims mean. 04:10:11

And the meaning of those claims should be the same regardless of what prior-art reference we are talking about; is that fair?

A. The meaning of the claims, that's right.

Q. So what is the meaning of "electrical communication" in the claims of the '060 and '160 patents? Can you tell us? 04:10:26

MR. LINDSAY: Objection. Form.

THE DEPONENT: So there's various places in the patent that talks about electrical 04:11:03

communication, for example in the summary, and where there's an electrical communication with at least one data port of an array die or a first array die. It talks about other instances of data ports and electrical communication with the data ports, all of which are consistent with the claims and consisting with the number of examples that I discussed which Dr. Wolfe raised in his prior-art references. 04:11:05 04:11:16

Q. (By Mr. Chandler) In the answer you just gave me right now, I didn't hear you use the word "load," correct? 04:11:43

A. I did not use the word "load" in my answer.

Q. So would it be fair to say that the construction of electrical communication does not depend on load? 04:11:55

MR. LINDSAY: Objection. Form.

THE DEPONENT: I don't have an opinion on that one way or the other right now. I wasn't asked to analyze that. 04:12:06

Q. (By Mr. Chandler) And in the answer you just gave me, I didn't hear you say the word "connection" or "electrical connection."

In your opinion, does the construction 04:12:30

for electrical communication depend at all on whether or not there's an electrical connection? 04:12:38

A. Again, I haven't been asked to perform that analysis or offer a construction on, quote, "electrical communication" by itself or how it may relate to electrical connection. 04:12:54

Q. Could you turn to your expert declaration, paragraph 251?

A. Okay.

Q. It's actually on the next page where you've got that figure. 04:13:22

A. Okay.

Q. So at the top of page 157 of your expert declaration marked as Exhibit 2023 is a figure that you created, correct? 04:13:44

A. That's correct.

Q. And the figure at the top of page 157 of Exhibit 2023 is a figure that you are using to explain why, in your opinion, there's electrical communication in the Riho reference; is that fair? 04:14:12

A. That's -- that's right. It's being used -- I am using that figure in support of what I am saying in 251 -- paragraph 251.

Q. The figure you created at the top of page 157 your declaration marked as Exhibit 2023 is 04:14:45

a lit bit misleading with respect to that arrow under the label "signal," to me at least, because it suggests that the signal from the TSV will go to the right side of the transmission gate and touch the black dot on the other side of the transmission gate even when the transmission gate is off, and that's not what actually happens, though, right? 04:14:55 04:15:19

A. I would say there would be signals at least to the input stage of the transmission gate.

Q. And so the transmission gate shown at the top of page 157 of your declaration marked as Exhibit 2023 -- when it's off, any signal coming from the TSV will not make it to the black dot on the right side of the transmission gate, correct? 04:15:50

A. I think, at a high level, the -- if we are -- if there's a logical 1, for example, coming up the TSV and the gate is off, the logical 1 value wouldn't be making it out the other side or at that adjoining point on the other side of the transmission gate. 04:16:27 04:16:48

Q. Because, in fairness, when I look at the orange arrow under the label "signal," as a layperson when I look at that arrow, the first reaction someone like me has looking at that arrow is it's trying to suggest that the signal from the 04:17:08

TSV will go all the way to the other transmission gate, touch the black dot, and potentially bounce back into the TSV. 04:17:12

And so, for clarity, that's not what happens when the transmission gate is off, correct? 04:17:26

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would say that when the transition gate is off -- if I'm sending a -- the -- a signal that's intended to be a logical 0 or 1 of the TSV is that -- I don't believe that logical 1 value is going to be reaching the outward bound side of the transmission gate if the gate is turned off. 04:17:41

Q. (By Mr. Chandler) In the figure at the top of page 157 of your expert declaration marked as Exhibit 2023, when the transmission gate is off, the L1C2R2 circuit to the right of the transmission gate is not an electrical communication with the TSV to the left of the transmission gate, correct? 04:18:02

A. So going back to Riho, the L1C2R2 is a model of the driver, and I'm describing, in paragraph 251, that when the gate is off, there is still the signals going from the TSV to the input stage in that gate, and, thus, there's electrical communication with transistors on the die. I don't 04:18:30 04:18:56

recall performing an analysis of -- well, that being electrical communication with the die, I think as we were -- you were, perhaps, asking yesterday, I haven't performed an analysis of subcomponents -- other subcomponents that may be in the die or models of component. 04:19:01 04:19:15

Q. To be clear, I was asking about the figure you created, and the figure you created is based on a textbook. It's not based on Riho. You took a textbook image of the transmission gate, and you drew a box of the TSV on the left side and you drew a box for a L1C2R2 driver circuit on the right side, correct? 04:19:30

A. In the context of explaining portions of Riho in response to what Dr. Wolfe was saying about Riho. 04:19:46

Q. Okay. Well, let me ask you in the context of transmission gates.

If you have a transmission gate like the one that you've shown at the top of page 157 of Exhibit 2023 and you've got a TSV on the left side of that transmission gate and you have another circuit, which we can call the L1C2R2 driver circuit on the right side of the transmission gate, when the transmission gate is off, there is no 04:19:59 04:20:13

electrical communication between the L1C2R2 driver circuit on the right side of the transmission gate with the TSV on the left side of the transmission gate, correct? 04:20:17

MR. LINDSAY: Objection. Form. Asked and answered. 04:20:30

THE DEPONENT: I would say, when the TSV is -- I'll stick with my logic -- logical 1 example -- that there are signals between the TSV and that input stage of the transmission gate, and, thus, there's electrical communication between that TSV and the array die as there's -- the tran- -- the transistors we're talking about are part of the array die. I haven't performed an analysis of other components or models of things that may reside on the array die beyond what I just said. 04:20:43 04:21:00

Q. (By Mr. Chandler) In fairness, Dr. Brogioli, my question to you did not include an array die, and your figure at the top of page 157 of Exhibit 2023 does not include an array die, so it's not exactly responsive to my question to start talking about array dies. 04:21:16

Can you answer my question without talking about array dies?

MR. LINDSAY: Objection. Form. 04:21:29

THE DEPONENT: Okay. My answer is -- is the same. Again, there is electrical communication between the TSV and the transistors of the transmission gate in this illustration. 04:21:33

Q. (By Mr. Chandler) But there's no electrical communication between the TSV to the left of the transmission gate and the L1C2R2 driver circuit to the right of the transmission gate, correct? 04:21:58

MR. LINDSAY: Objection. Asked and answered. Form. 04:22:13

THE DEPONENT: I have -- sorry.

I -- I haven't performed that analysis. It wasn't something that I was considering one way or the other in providing this high-level example -- or this high-level illustration to complement the two or three sentences in this paragraph. 04:22:21

Q. (By Mr. Chandler) Could you turn to Riho, which is Exhibit, I guess, 1016, and we can start with Figure 5. 04:23:42

A. Okay.

Q. So I just want to make sure that we are clear about your testimony on Riho, marked as Exhibit 1016. 04:24:14

Your testimony is that taking, for example, SDRAM D14, that ESV715, you say, is connected and in communication with the left side of the transmission gate of SA and SB, but you do not have any opinions to offer about whether there's electrical communication with the right side of the transmission gates for SA and SB, correct? 04:24:17 04:24:49

MR. LINDSAY: Objection. Form.

THE DEPONENT: That there is elec- -- in the case of SDRAM D14 in Riho's Figure 5, that there is electrical communication and -- and as we discussed a moment ago earlier today, electrical connection to the block CS14 that has the SA and SB in it, and I have discussed that in the context of Dr. Wolfe discussing the transmission gate that we just talked about a moment ago. 04:25:12 04:25:35

In terms of the L1C2R2 model or other things to what would be potentially to the right side of CS14, I haven't offered opinions on it. 04:25:53

Q. (By Mr. Chandler) So would your answer be the same for Figure 8A with respect to the transmission gates for SA and SB for SDRAM D15?

A. That -- in this figure as well, there would be similar electrical connection and 04:26:29

electrical communication with the components within CS15. 04:26:31

Q. And, specifically, you are pointing to the left side of the transmission gate for SA and SB, but you are not offering any testimony or opinions that there would be electrical communication with anything on the right side of the transmission gate SA and SB for SDRAM D15 and Figure 8A of Riho, correct? 04:26:49

A. I would say, in the context of this visualization, I haven't offered an opinion on that. As I recall, what's visualized in Riho Figure 8A to the right of CS15 is Riho's model of some kind of driver. 04:27:09

Q. You were asked about the Kim reference, so I would like to follow up with you about Kim. 04:27:38

Do you have Kim in mind?

A. Yes. Let me pull it up quickly.

Okay.

MR. LINDSAY: What exhibit number? 04:27:57

MR. CHANDLER: 1014.

Q. (By Mr. Chandler) And the question you were asked by Netlist, if I recall, was to the effect of whether the JEDEC DDR3 standard is relevant to Kim. 04:28:19

Do you recall that question? 04:28:22

A. I recall a question about if I remember the timing diagrams in JEDEC and, if I remember right, various of the timing diagrams in Kim.

Q. In forming your validity opinions, did you consider the timing diagrams in the JEDEC DDR3 standard, marked as Exhibit 1019, relevant to understanding the obviousness combinations involving the Kim reference marked as Exhibit 1014? 04:28:50

A. Yes, in the sense that this person of skill would be aware of those timing diagrams in the JEDEC standard. 04:29:21

Q. And so a person of ordinary skill in the art combining Kim with another reference wouldn't limit themselves to only the timing diagram and Kim, correct? They would also take into account other teachings in the art, as well as their common sense, which would include, but not be limited to, the timing diagrams in the JEDEC DDR3 standard marked as Exhibit 1019; is that fair? 04:29:44 04:30:09

MR. LINDSAY: Objection. Form.

THE DEPONENT: I think that they would be aware of those figures within the JEDEC reference. In terms of the subject matter and relevance of those to specific aspects of Kim, they would have 04:30:24

to take that into consideration as to what part of Kim that they were considering. 04:30:28

Q. (By Mr. Chandler) Could you turn to the '060 patent. I am going to ask you about both, but, you know, pick your favorite one. 04:31:06

A. Okay. Go ahead.

Q. You were asked some questions about implementing the '060 patent with the SRAM or a flash memory, and so I just want to follow up on that a little bit. 04:31:32

Do you recall the question and the answer you had with counsel from Netlist along those lines?

A. I believe so, yes.

Q. And what was the point you were trying to make for counsel to Netlist? 04:31:44

A. As I recall, the question was around: Was the patent, the '060, for example, talking about using NAND flash, if I am remembering right, as the array die to -- to support a type of interface that was, for example, a DDR-type interface, or DDR DRAM, for example. 04:32:08

Q. So the '060 and '160 packets -- patents, as we discussed, I believe, yesterday, each, that the preferred embodiment can use a package that's a 04:32:42

DRAM package, an SDRAM package, or a flash memory package, to name a few, correct? 04:32:48

A. That's -- it sounds like what the patent is talking about, for example, at the top of column 22. 04:33:06

Q. And it may have been this morning that we talked about it instead of yesterday.

The patent also talks about preferred embodiments where the array die could be a DRAM, could be an SDRAM, could be an SRAM, could be a flash memory, correct? 04:33:21

A. That's right.

Q. So according to the '060 and '160 patents, is it possible to have a DRAM package where the array die inside of that package is an SRAM chip? 04:33:46

A. That's not something I have analyzed in the scope of -- of my declaration, but I have just a number of issues as to challenges that would -- a person of skill would encounter trying to use, for example, flash-type memory in various regard -- in various aspects. 04:34:14

Q. Well, that's what I am getting at, because the patent seems pretty clear that the array die could be an SRAM or the package could be 04:34:36

a DRAM package, and, yet, in response to your question from counsel for Netlist, you seem to suggest that a person of ordinary skill in the art would not have a reasonable expectation of success if they tried to implement such an embodiment of the invention of the '060 and '160 patent. 04:34:41 04:34:55

And so I want to try to get your best testimony on this question of whether a person of ordinary skill in the art, reading the '060 and '160 patent, would have a reasonable expectation of success of practicing the invention with an array die that's an SRAM and a memory package that's a DRAM package as -- 04:35:14

MR. LINDSAY: Objection. Form.

MS. ZHONG: And this is Annita. Objection. Completely misleading questions regarding the claim scope. 04:35:46

Q. (By Mr. Chandler) Go ahead and answer, Dr. Brogioli.

A. So as I talk about in my declaration, if -- if the question is someone implementing a NAND -- I'm sorry, a DR -- DRAM package, for example, in implementing that with NAND flash memory, there are a number of problems that come up in trying to do that, which is what is addressed in 04:36:01 04:36:18

portions of my declaration. 04:36:22

Q. (By Mr. Chandler) But are those problems beyond the level of skill for a person of ordinary skill in the art?

A. In terms of heterogeneously trying to mix 04:36:37
these technologies, that's -- if I am understanding your question correctly, what I am getting at in my declaration -- declaration; that it is beyond the skill of -- of this person of skill in the art.

Q. So -- so when the '060 and '160 patent 04:36:54
teaches that the memory package can be a DRAM package or the array die can be a SRAM die or a flash memory die, you believe that teaching in the '060 and '160 patent is beyond the level of a person of ordinary skill in the art? 04:37:21

MR. LINDSAY: Objection. Form. Misleading and vague.

THE DEPONENT: What I am getting at in my declaration is that if -- if -- if a person of skill in the art is asked to implement, for 04:37:35
example, a DDR2 or 3 host interface using a NAND-flash-type internal memory, that's beyond the skill of a person -- of this person of skill in the art.

Q. (By Mr. Chandler) In your opinion. 04:37:56

A. In my opinion. 04:37:59

Q. And you used that opinion and that belief in forming your conclusions that the claims of the '060 and '160 patents are nonobvious, right?

A. I would say I used that belief in coming 04:38:18
to the -- to the conclusions and opinions expressed in my declaration.

Q. And you did not express validity opinions for the '060 and '160 patent based on the belief 04:38:41
that a person of ordinary skill in the art would be able to implement an array die that's either SRAM or flash in a DRAM package, correct? It's not something you --

MR. LINDSAY: Objection. Form.

Q. (By Mr. Chandler) -- based your opinions 04:39:04
on under that scenario?

A. I would say I addressed certain aspects of that in my declaration in response to various combinations that -- or various combinations of references that Dr. Wolfe had proposed. 04:39:20

Q. Well, I am a little confused by your last answer.

So are there situations where you think a person of ordinary skill in the art can implement an array die with SRAM or flash memory in a DRAM 04:39:37

package? 04:39:45

MR. LINDSAY: Objection. Form. Outside the scope of direct.

THE DEPONENT: I address a number of issues that a person of skill would face in an 04:39:52
example like that in my declaration. I don't recall performing an analysis -- I have a lengthy list of problems that this person of skill in the art would face in that context. My opinions stop there. I haven't performed a hypothetical anal- -- 04:40:13
analysis of a hypothetical of the scenario where someone may succeed. I certainly didn't see anything that indicated that in the references that Dr. Wolfe had offered or the combinations he offered. 04:40:31

Q. (By Mr. Chandler) Can you give me any examples of an embodiment of the invention of the '060 and '160 patent that has a DRAM package, but the array die does not include the DRAM circuits?

A. I am not quite sure I understand your 04:41:32
question.

Q. And what part of it?

A. Well, in the prosecution history and as has come in the past, the array dies, as I recall, are construed as something different from a DRAM 04:41:58

circuit. 04:42:03

Q. That's fine. I am not trying to get a claim construction. I am trying to understand your opinions about SRAM and flash memory and -- and the difficulties of implementing the -- the claimed 04:42:15 invention, so -- so let me ask the question. I won't use the phrase "DRAM circuit." I will just use the phrase "DRAM."

All right. So will you keep that in mind as I ask the question again? 04:42:52

A. Okay.

Q. Can you give me any examples of embodiment of the invention of the '060 and '160 patent that has a DRAM package, but the array die does not include DRAM? 04:43:08

A. If I am understanding your question right, I haven't performed -- I have listed a number of challenges that one would face trying to implement a DRAM-type interface using a different memory technology, such as flash memory, due to 04:43:34 various technical challenges, limitations, and so forth; that, as I recall, is the extent of opinions I have offered.

If you are asking me to, on the fly, look at a system that would implement the patent's DRAM 04:43:56

package or interface with -- they would succeed with a NAND flash memory internally, I haven't done that analysis. 04:44:01

Q. And, to be clear, you're -- you haven't done that analysis either way, so you're unable to tell me whether it can be done, but you are also unable to tell me that it cannot be done, correct? 04:44:21

A. Well, in my declaration, I have offered a number of statements and opinions as to the difficulty of why this person of skill wouldn't succeed or why it wouldn't make sense. 04:44:37

Q. But I am focused on the '060 and '160 patent. I think your declaration was more focused on your characterization of certain prior art that Dr. Wolfe was relying upon. And I am trying to understand what the '060 and '160 patent is talking about and your opinions about what it's talking about. 04:44:53

A. I see.

I don't recall performing that analysis in my declaration as to -- again, whether, to your question, a DRAM package or interface can be built using some other heterogeneous memory technology in the context of the '060. I don't recall offering opinions on that one way or the other. 04:45:09 04:45:31

Q. So, to be clear, you are unable to tell me now of an example of an embodiment of the '060 or '160 claims that has a DRAM package with an array die that does not include DRAM, correct? 04:45:37

MR. LINDSAY: Objection. Asked and answered and, as we have established, outside the scope of direct. 04:46:01

THE DEPONENT: I haven't -- I would say I have not performed an analysis of a DRAM package within the scope -- in the confines of the patent implemented with some other, I will call, heterogenous memory technology like a flash memory technology. 04:46:14

Q. (By Mr. Chandler) Or any other type of array die that is not DRAM, correct? 04:46:36

MR. LINDSAY: Same objection: Asked and answered. Outside the scope of direct.

THE DEPONENT: So, similarly, I haven't performed that analysis one way or the other with a -- an SRAM-type memory technology instead of a flash-memory-type technology in my previous answer. 04:46:49

Q. (By Mr. Chandler) Or any other type of array die that does not include DRAM, correct?

MR. LINDSAY: Objection. Asked and answered. Outside the scope of direct. 04:47:05

THE DEPONENT: Again, I -- I don't recall being asked to or performing that analysis. 04:47:09

Q. (By Mr. Chandler) Could you pull up the Jacob textbook that counsel for Netlist asked you some questions about. It's Exhibit 1022, page 413. 04:47:23

A. All right. One moment.

Okay.

Q. In forming your validity opinions for the '060 and '160 patents, did you understand the term "rank" as requiring more than one memory device in the rank? 04:47:57

A. That I was using -- I see the section from Jacob, and going on the statement that is "T lessen the confusion associated with overloading the nomenclature, the word rank is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system." 04:48:19

Q. Well, just -- just to be clear -- and I am not trying to push you in one direction or the other. I am trying to make it clear as to the understanding that you are using. 04:48:34

And the reason I ask is because when I read page 413 of Exhibit 1022, I see the second sentence where he says, essentially, a rank is a 04:48:51

bank of one more DRAM devices. And so I would read that as rank can have one device. 04:48:55

But now I hear you pointing to a later sentence where you seem to be saying that rank must have two or more memory devices, and so I am just trying to get clarity as to what understanding of the term "rank" you were using in forming your opinions for the '060 and '160 patents? 04:49:14

MR. LINDSAY: Objection. Form.

THE DEPONENT: I would say generally using this language from Jacob that's talking about the rank used to denote a set of DRAM devices that operate in lockstep. 04:49:37

Q. (By Mr. Chandler) And does that encompass a rank with just one memory device, in your opinion, or, in your opinion, does rank require multiple memory devices? 04:49:56

MR. LINDSAY: Objection. Form.

THE DEPONENT: That -- as we have been talking about, the -- in -- in a number of the other references, that we see that the rank is denoting a set of DRAM devices that are operating in lockstep. 04:50:24

Q. (By Mr. Chandler) That doesn't seem to answer my question. 04:50:41

My question is pretty simple and numerical. It's whether a rank can be just one device or whether a rank requires at least two devices? 04:50:41

MR. LINDSAY: Objection. Form. Asked and answered. 04:51:02

Q. (By Mr. Chandler) What --

A. The --

Q. What's your interpretation that you applied forming your validity opinions for the '060 and '160 patents? 04:51:11

A. It's in line as -- as I just said where we have a rank denoting a set of DRAM devices, and that's also in line with the definition of "rank" as it comes from JEDEC itself. 04:51:27

Q. Still not sure you've answered the question. Still not sure your testimony is clear.

Does a rank encompass a single memory device, or are you unable to provide an opinion on that for these IPRs? 04:52:18

MR. LINDSAY: Objection. Asked and answered. The question has been answered. And objection to form. Compound questions.

THE DEPONENT: So just as this -- the Jacob reference you are pointing me to, I am using 04:52:33

the understanding that "rank" is used to denote this set of DRAM devices here that he's saying operate in lockstep, which is the same definition -- or, as I recall, in JEDEC itself defining "rank" -- that is denoting multiple of these DRAM devices, and that's the understanding that I have been using. 04:52:35 04:52:48

Q. (By Mr. Chandler) So in forming your opinions for the '060 and '160 patents, you interpreted "rank" as requiring multiple devices, correct? 04:53:03

A. In the context that "rank" is used in its JEDEC definition and similar to the language we've just been talking about.

Q. It is unclear to me whether the answer to my question that I just asked you was "yes" or "no." 04:53:26

Can you try to answer it more clearly?

A. That, as I just said, JEDEC is talking about the definition of "rank" being multiple of these, in this case, DRAM devices. Here is also in Jacob that you pointed me to a definition of "rank" for multiple where he said DRAM devices, and that's the definition I have been using, not a definition that a rank is one DRAM device. 04:53:38 04:53:57

Q. Dr. Brogioli, do you have any clarifications that you would like to make to any of the testimony that you have given to me either this afternoon or earlier today or yesterday? 04:54:15

A. Not going from memory, I don't. 04:54:31

MR. CHANDLER: All right. That will conclude the deposition. See you next week.

THE VIDEOGRAPHER: Before we go off the record, we ask for any transcript or video orders.

MR. CHANDLER: Yes. So for us we would like the transcript by the end of the day on Monday, October 2nd, and for the video, there's no rush, so we will purchase it, but only in the sort of ordinary course. 04:55:00

THE VIDEOGRAPHER: Okay. 04:55:18

MR. LINDSAY: And we'll just take a rough.

THE VIDEOGRAPHER: All right.

MR. CHANDLER: And we'll take a rough for today as well. 04:55:30

THE VIDEOGRAPHER: All right. Thank you.

This concludes today's video conference deposition. Going off the record, September 28th, 2023 at 4:55 p.m. Central.

(TIME NOTED: 4:55 P.M.) 04:55:41

I, Rebecca L. Romano, a Certified Shorthand Reporter of the State of California, do hereby certify:

That the foregoing proceedings were taken before me at the time and place herein set forth; that any witnesses in the foregoing proceedings, prior to testifying, were administered an oath; that a record of the proceedings was made by me using machine shorthand which was thereafter transcribed under my direction; that the foregoing transcript is true record of the testimony given.

Further, that if the foregoing pertains to the original transcript of a deposition in a Federal Case, before completion of the proceedings, review of the transcript [ ] was [X] was not requested.

I further certify I am neither financially interested in the action nor a relative or employee of any attorney or any party to this action.

IN WITNESS WHEREOF, I have this date subscribed my name.

Dated: October 2, 2023

Rebecca L. Romano, RPR,
CSR. No 12546

I, DR. MICHAEL C. BROGIOLI, do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made any corrections as appear notes; that my testimony as contained herein, as corrected, is true and correct.

Executed this _____ day of _____, 2023, at _____, _____.

_____
DR. MICHAEL C. BROGIOLI

DEPOSITION ERRATA SHEET

Case Name: Samsung Electronics, Co., Ltd. vs. Netlist, Inc.
Name of Deponent: Dr. Michael C. Brogioli
Date of Deposition: September 28, 2023
Job No.: J10233368
Reason Codes: 1. To clarify the record.
2. To conform to the facts.
3. To correct transcript errors.

Page _____ Line _____ Reason _____

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_____ Subject to the above changes, I certify that the transcript is true and correct

_____ No changes have been made. I certify that the transcript is true and correct.

_____

DR. MICHAEL C. BROGIOLI