UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[†]

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2022-01428
Patent 8,787,060 B2

EXHIBIT 1067:

Petitioner's Demonstratives for Oral Argument on January 11, 2024

[†] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00882 and have been joined as petitioners to this proceeding.

Petitioner Samsung Electronics Co., Ltd.'s Oral Argument for PTAB Hearing

Samsung Electronics Co., Ltd. v. Netlist, Inc.,

IPR2022-01427 and IPR2022-01428 (U.S. Patent Nos. 9,318,160 and 8,787,060)

January 11, 2024

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DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

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04 Petitioner’s Motion to Exclude

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OVERVIEW 01

OVERVIEW OF ’060 AND ’160 PATENTS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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’060 AND ’160 PATENTS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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’060 Patent

(12) **United States Patent**
Lee

(10) **Patent No.: US 8,787,060 B2**
(45) **Date of Patent: Jul. 22, 2014**

(54) **METHOD AND APPARATUS FOR OPTIMIZING DRIVER LOAD IN A MEMORY PACKAGE**

(75) Inventor: **Hyun Lee**, Ladera Ranch, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(22) Filed: **Nov. 3, 2011**

(65) **Prior Publication Data**

US 2012/0106228 A1 May 3, 2012

Related U.S. Application Data

(60) Provisional application No. 61/409,893, filed on Nov. 3, 2010.

No support in Provisional for ’060 claims

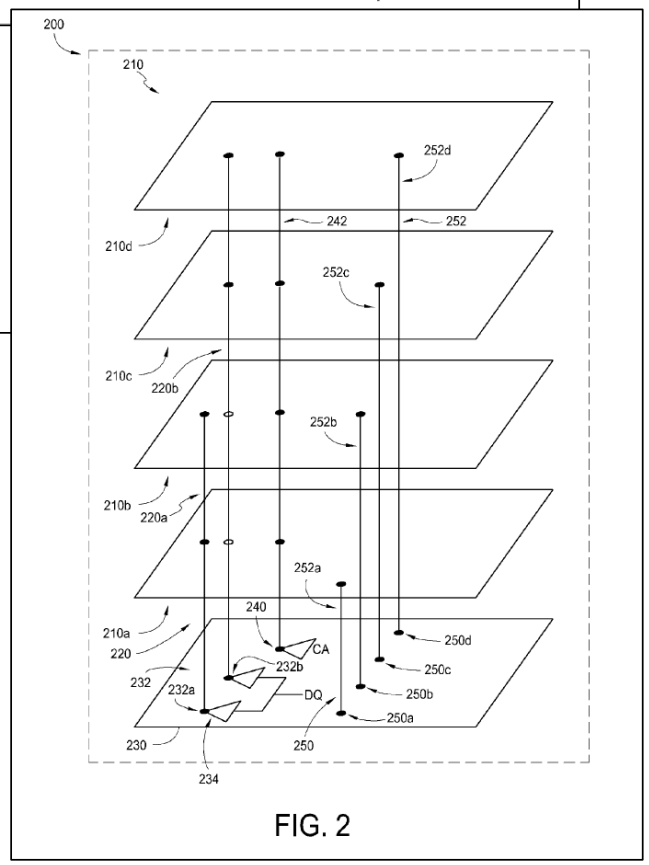


FIG. 2

’160 Patent (continuation of ’060 Patent)

(12) **United States Patent**
Lee

(10) **Patent No.: US 9,318,160 B2**
(45) **Date of Patent: *Apr. 19, 2016**

(54) **MEMORY PACKAGE WITH OPTIMIZED DRIVER LOAD AND METHOD OF OPERATION**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventor: **Hyun Lee**, Ladera Ranch, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(22) Filed: **Jul. 21, 2014**

(65) **Prior Publication Data**

US 2015/0070959 A1 Mar. 12, 2015

Related U.S. Application Data

(63) Continuation of application No. 13/288,850, filed on Nov. 3, 2011, now Pat. No. 8,787,060.

(60) Provisional application No. 61/409,893, filed on Nov. 3, 2010.

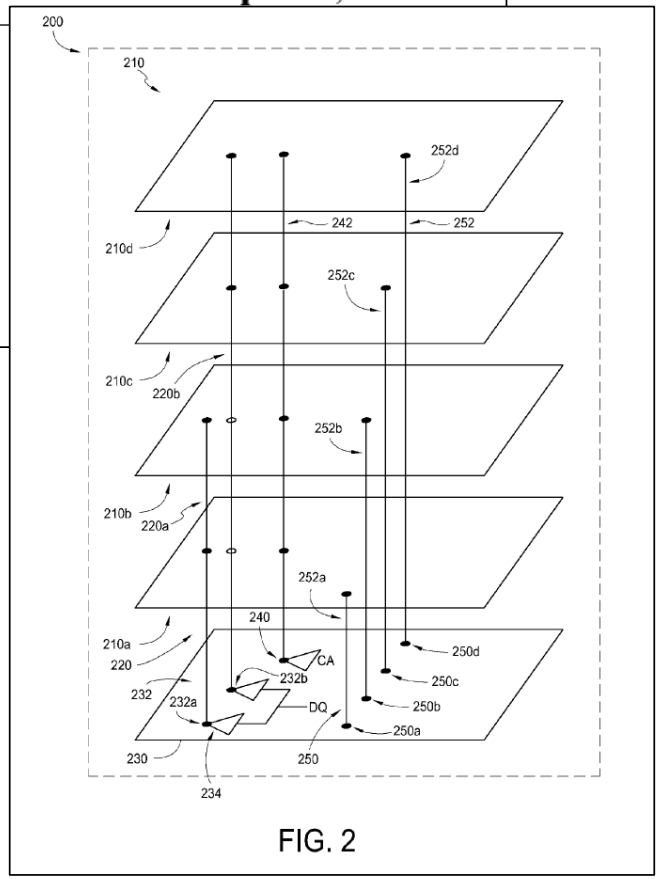


FIG. 2

No support in Provisional for ’160 claims

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'060/'160 Patent: Optimizing Load on "Die Interconnects"

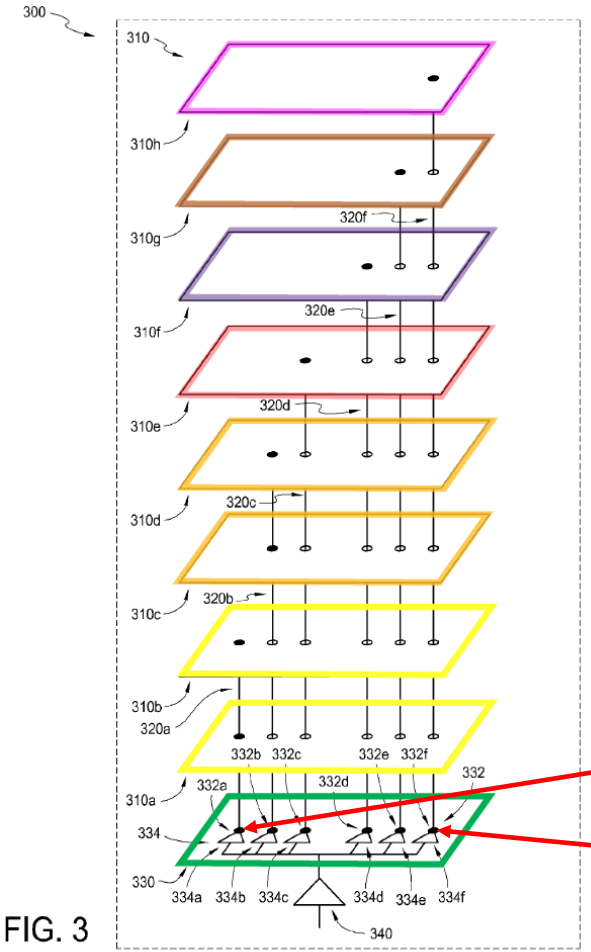


FIG. 3

In some cases, the load contribution of each segment of the die interconnect **320** may be measured as a fraction of the load contribution from an array die **310**. For example, the load of one segment of the die interconnect **320***a* may be equivalent to one quarter of the load of an array die **310**. Thus, for example, the load of the conduit **332***a* may be 2.5L assuming a load contribution of L per array die **310** (two in this case) in electrical communication with the die interconnect **320***a* and a load contribution of 0.25L per segment (two in this case) of the die interconnect **320***a*. As a second example, the load of the conduit **332***f* may be 3L assuming the same load values as the previous example and a load contribution from one array die **310***h* and eight die interconnect **320***f* segments. Table 1 specifies the capacitive load values for each conduit **332**

1L load / die | **0.25L load / segment of die interconnect**

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5 L	0.5
332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

'060: EX1001 at Fig. 3, 12:51-:66 & Table 1; Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
'160: EX1001 at Fig. 3, 12:46-:61 & Table 1; Paper 1 (Pet.) at 11-16; EX1003 at ¶¶ 61-65

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’060/’160 Claims: Groups of Stacked “Array Dies”

’060 Patent, Claim 1:

1. A memory package, comprising:
a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

’160 Patent, Claim 1:

1. A memory package, comprising:
data terminals and control terminals;
stacked array dies including a first group of array dies and a second group of at least one array die;

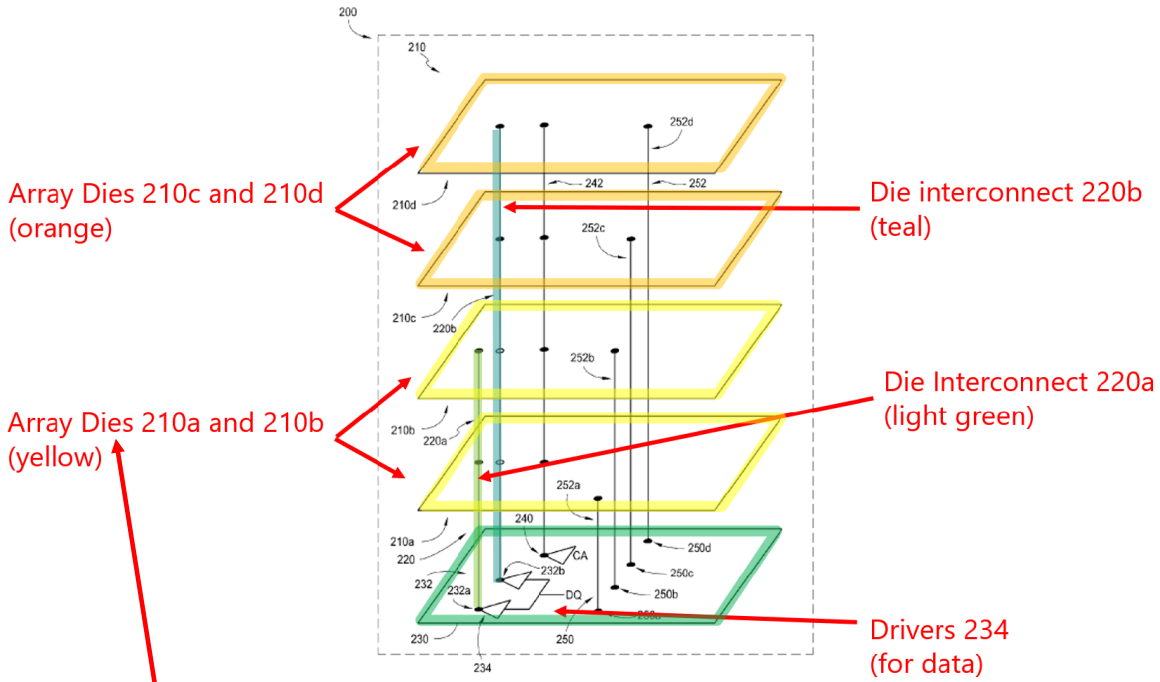


FIG. 2

receive data signals from the control die **822**. As with the array dies **210** and **310**, the array dies **824** may include any type of Random Access Memory (RAM) die. For example, the array dies **824** may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory

’060: EX1001 at 21:67-22:4
’160: EX1001 at 21:52-:56

’060: Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
’160: Paper 1 (Pet.) at 11-16; EX1003 at ¶¶ 61-65

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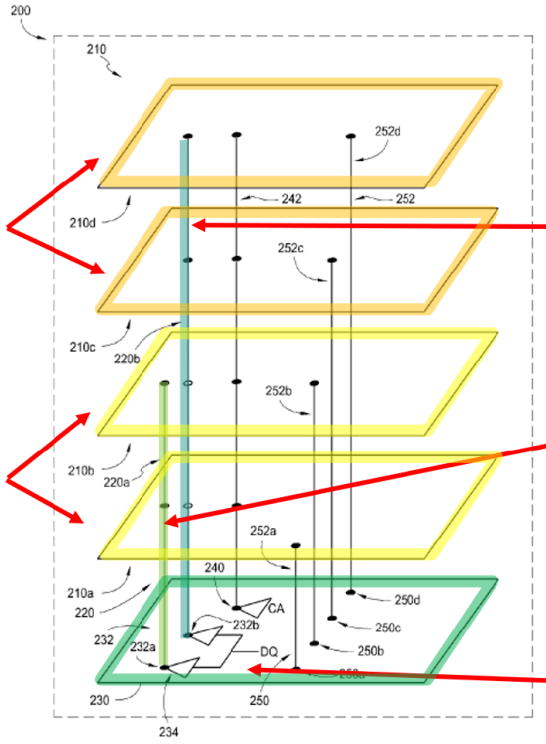
’060/’160 Claims: Separate “Die Interconnects” for Each Group

’060 Patent, Claim 1:

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

’160 Patent, Claim 1:

first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and



Array Dies 210c and 210d (orange)

Array Dies 210a and 210b (yellow)

Die interconnect 220b (teal)

Die Interconnect 220a (light green)

Drivers 234 (for data)

FIG. 2

to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g.,

’060: EX1001 at 5:51-:53
’160: EX1001 at 5:43-:56

’060: Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
’160: Paper 1 (Pet.) at 11-16; EX1003 at ¶¶ 61-65

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’060/’160 Claims: “Control Die” with “Data Conduits” to “Die Interconnects”

’060 Patent, Claim 1:

a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

’160 Patent, Claim 1:

a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first

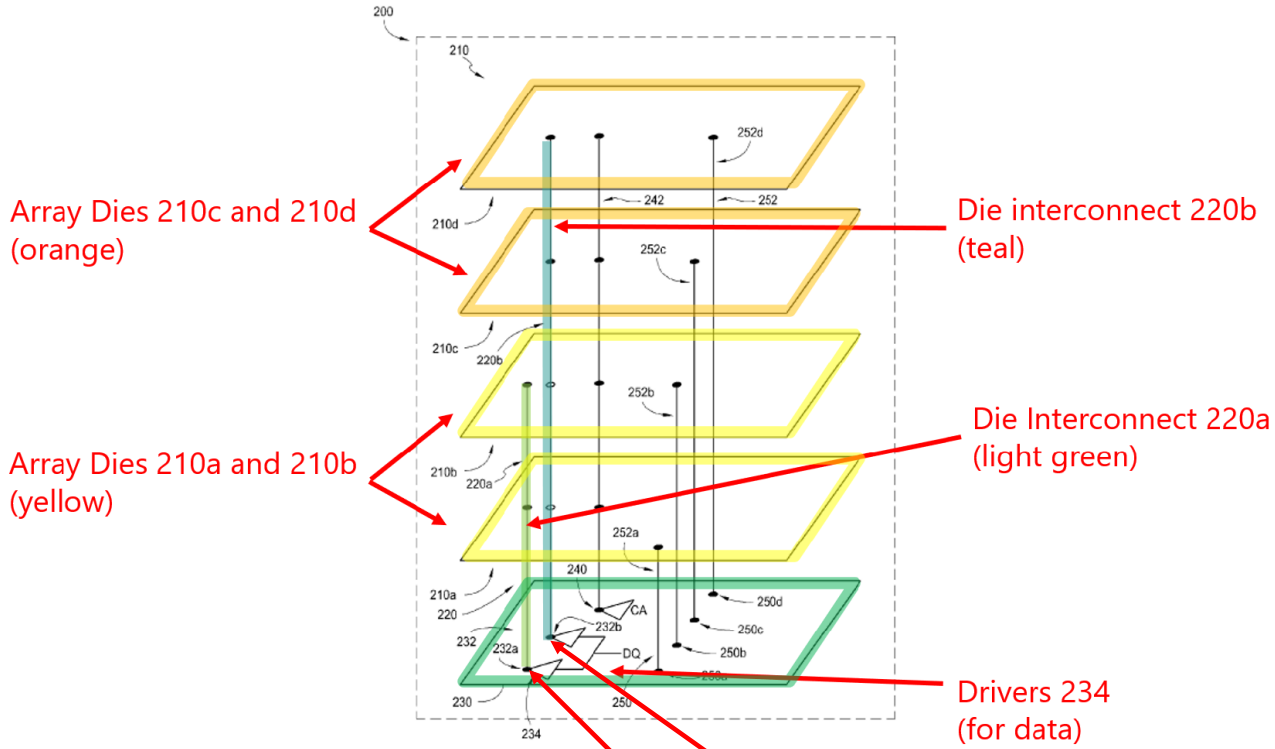


FIG. 2

The control die **230** may include a number of data conduits **232**, which includes data conduits **232***a* and **232***b*. Each of these data conduits **232** may be configured to transmit a data signal to a single die interconnect **220**. For example, the data

’060: EX1001 at 6:48-:51
’160: EX1001 at 6:51-:54

’060: Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
’160: Paper 1 (Pet.) at 11-16; EX1003 at ¶¶61-65

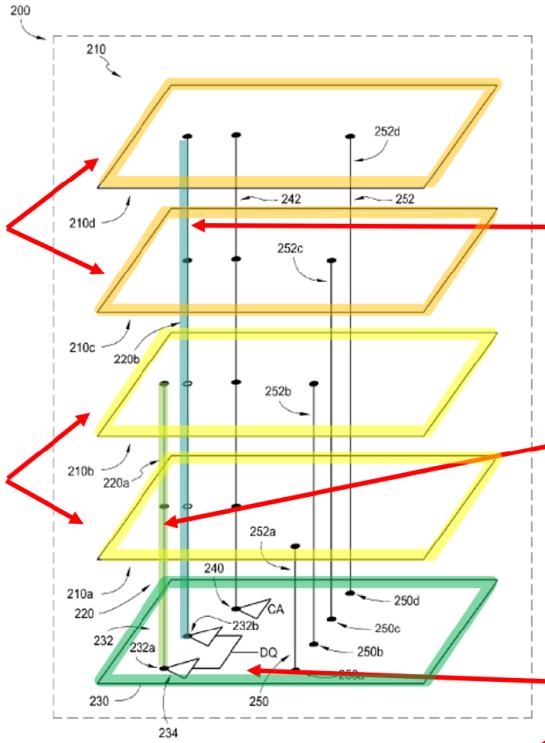
'060/'160 Claims: "Data Conduits" include Respective *Drivers*

'060 Patent, Claim 15:

15. The memory package of claim **11**, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

'160 Patent, Claim 1:

the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.



Array Dies 210c and 210d (orange)

Array Dies 210a and 210b (yellow)

Die interconnect 220b (teal)

Die Interconnect 220a (light green)

Drivers 234 (for data)

FIG. 2

interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more

'060: EX1001 at 17:43-:45
'160: EX1001 at 17:32-:35

'060: Paper 1 (Pet.) at 11-14; EX1003 ¶¶ 61-65
'160: Paper 1 (Pet.) at 11-16; EX1003 ¶¶ 61-65

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’060/’160 Patent: Optimizing Load on “Die Interconnects”

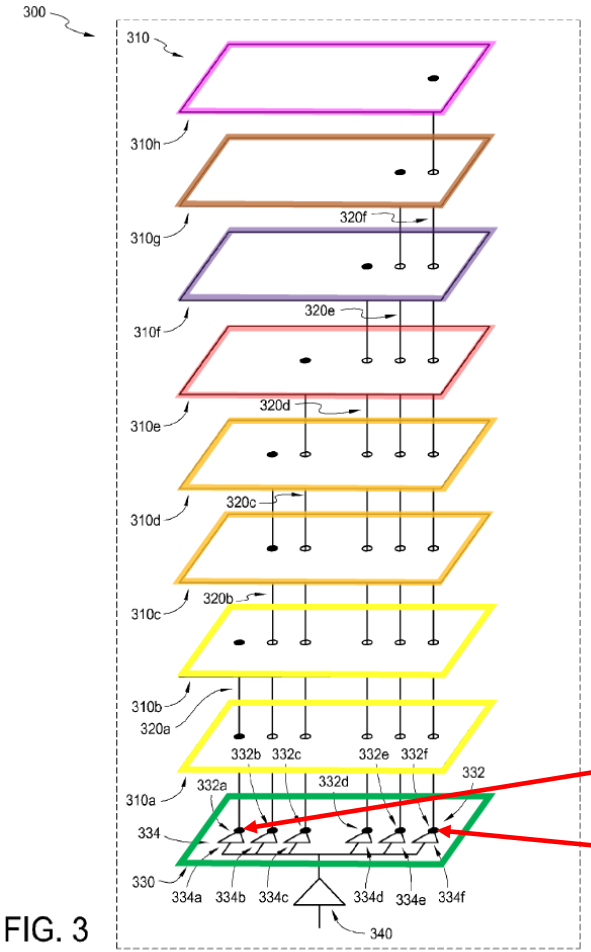


FIG. 3

In some cases, the load contribution of each segment of the die interconnect **320** may be measured as a fraction of the load contribution from an array die **310**. For example, the load of one segment of the die interconnect **320***a* may be equivalent to one quarter of the load of an array die **310**. Thus, for example, the load of the conduit **332***a* may be 2.5L assuming a load contribution of L per array die **310** (two in this case) in electrical communication with the die interconnect **320***a* and a load contribution of 0.25L per segment (two in this case) of the die interconnect **320***a*. As a second example, the load of the conduit **332***f* may be 3L assuming the same load values as the previous example and a load contribution from one array die **310***h* and eight die interconnect **320***f* segments. Table 1 specifies the capacitive load values for each conduit **332**

1L load / die | **0.25L load / segment of die interconnect**

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
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332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

’060: EX1001 at Fig. 3, 12:51-:66 & Table 1; Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
’160: EX1001 at Fig. 3, 12:46-:61 & Table 1; Paper 1 (Pet.) at 11-16; EX1003 at ¶¶ 61-65

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INSTITUTED GROUNDS & PRIOR ART

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Instituted Grounds

'060 Grounds & Claims	'160 Grounds & Claims	Prior Art
Ground 1: Claims 1-6, 8-14, 16-19, 29-34		**Kim** + **Rajan**
Ground 2: Claims 1-14, 16-19, 29-34		**Kim** + **Rajan** + Riho
Ground 3: Claims 1-6, 8-34	Ground 1: Claims 1-20	**Kim** + **Rajan** + Wyman
Ground 4: Claims 1-14, 16-19, 29-34		**Riho** + **Rajan**
Ground 5: Claims 1-34	Ground 2: Claims 1-20	**Riho** + **Rajan** + Riho2

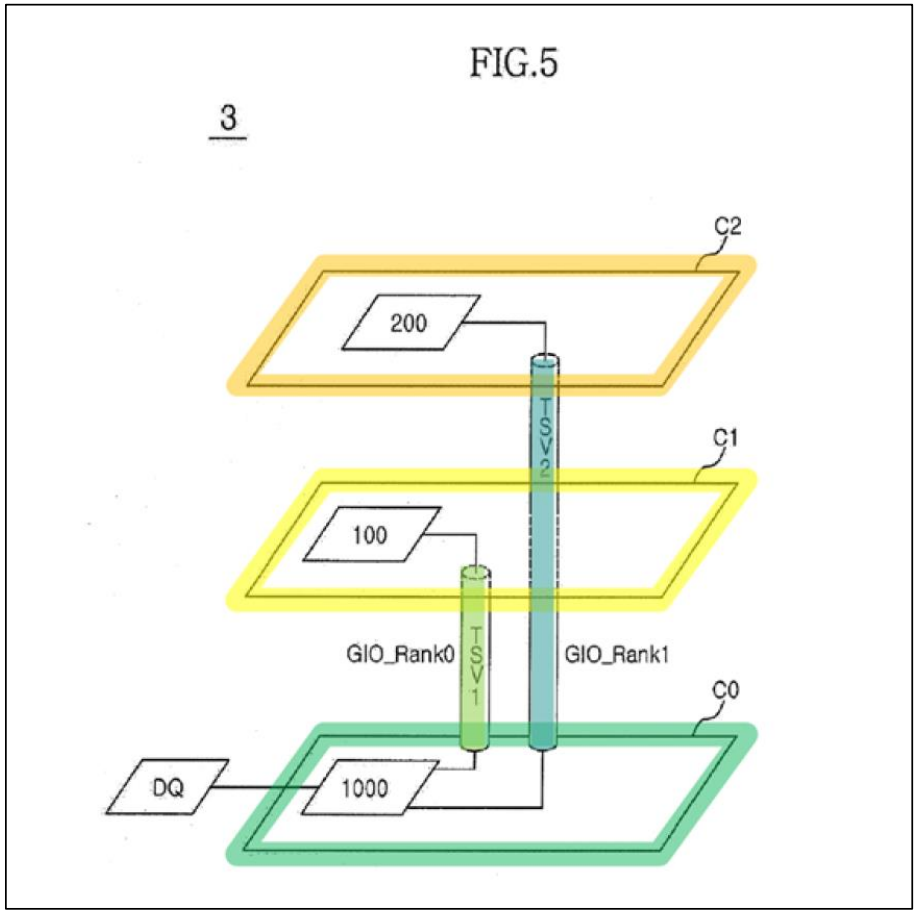
'060: Paper 1 (Pet.) at 3; Paper 13 (ID) at 5, 28
'160: Paper 1 (Pet.) at 3; Paper 13 (ID) at 5, 28

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Prior Art: Kim [EX1014]

[0048] FIG. **5** shows an exemplary embodiment in which one main chip C0 and two slave chips C1 and C2 are stacked. Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used. In the 3D semiconductor apparatus in which the

EX1014 (Kim) at [0048] & Fig.5



'060: Paper 1 (Pet.) at 15-16
'160: Paper 1 (Pet.) at 17-18

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Ex. 1067, p. 15

Prior Art: Rajan [EX1015]

The physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc.

EX1015 (Rajan) at 15:3-:9

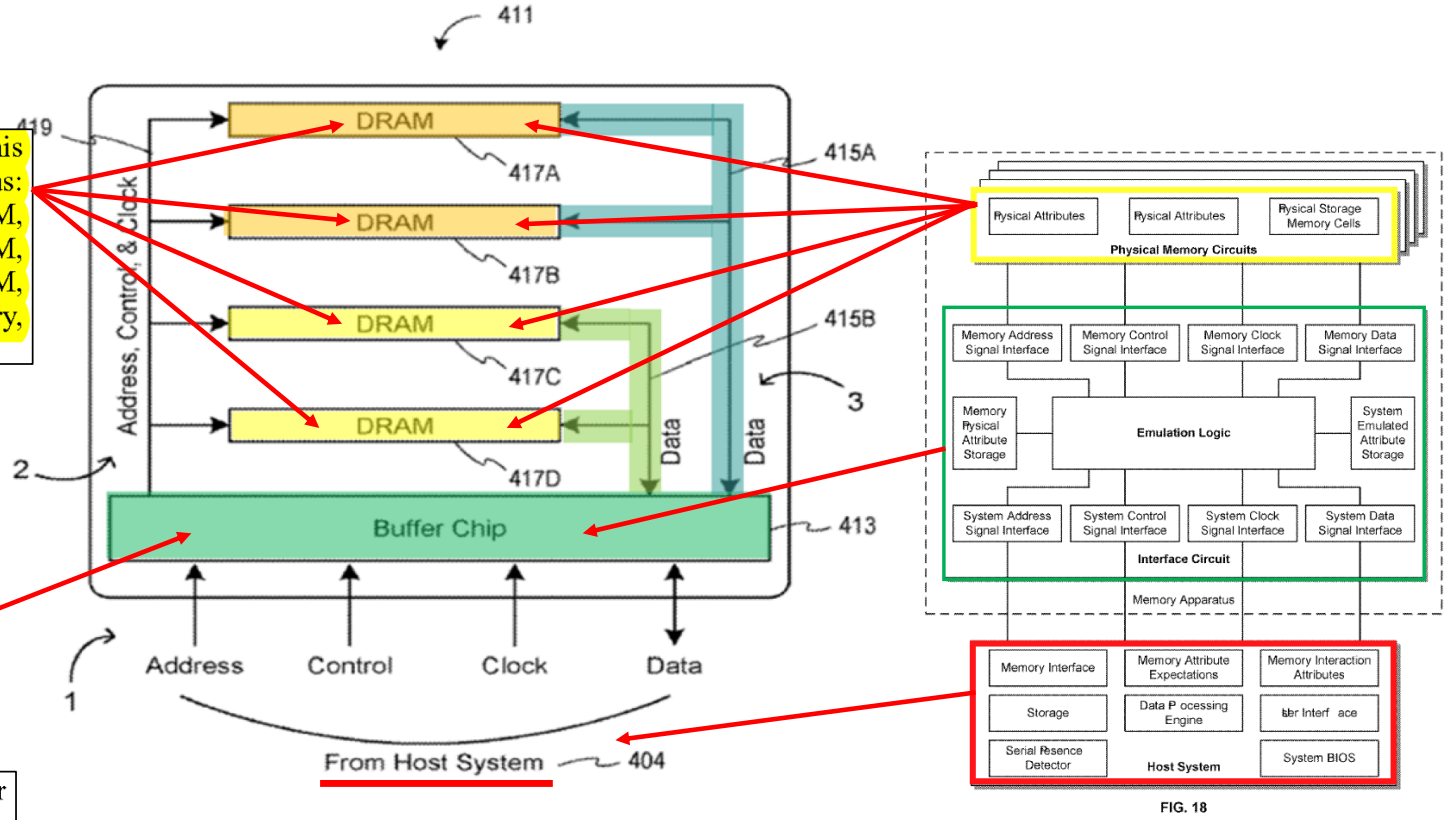


FIG. 4

FIG. 18

The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

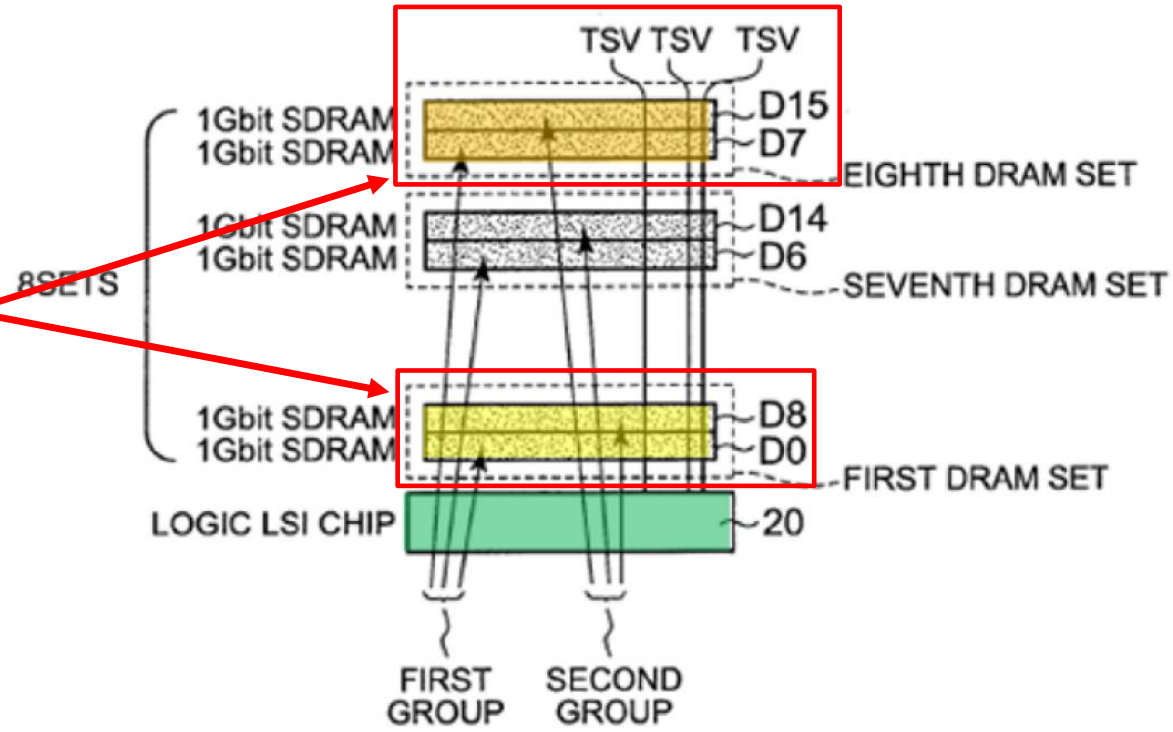
EX1015 (Rajan) at 4:20-:24; *see also id.* at 4:48-:50, 14:6-:11, 14:39-:62 & Fig. 18

Prior Art: Riho [EX1016]

[0103] Further, by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups.

EX1016 (Riho) at [0103]

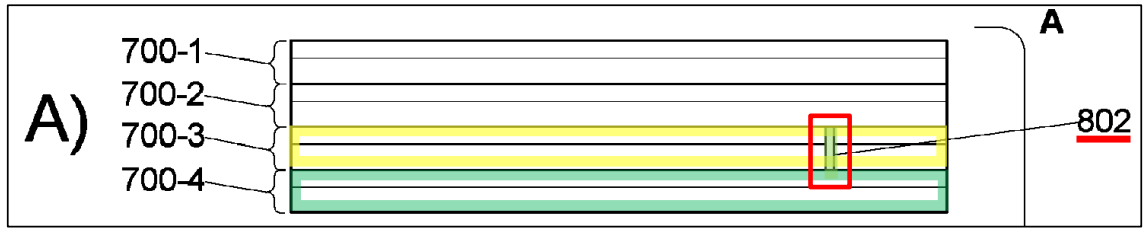
FIG. 1



'060: Paper 1 (Pet.) at 18-19
'160: Paper 1 (Pet.) at 20-21

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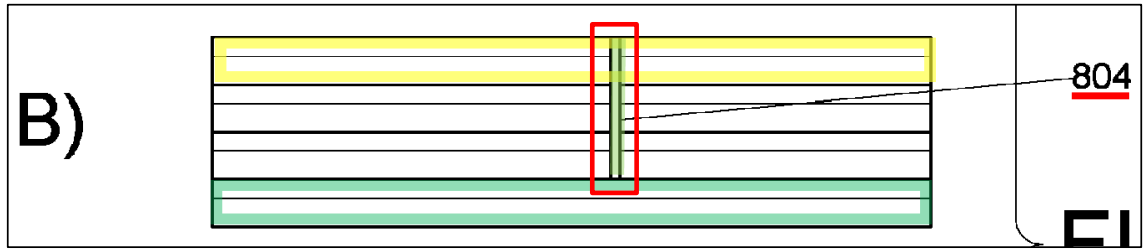
Prior Art: Wyman [EX1017]



EX1017 (Wyman) at Fig. 8A

FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3). Presuming that this connection would require minimal drive, if a driver portion 500 of FIG. 5 was

EX1017 (Wyman) at 6:15-:18

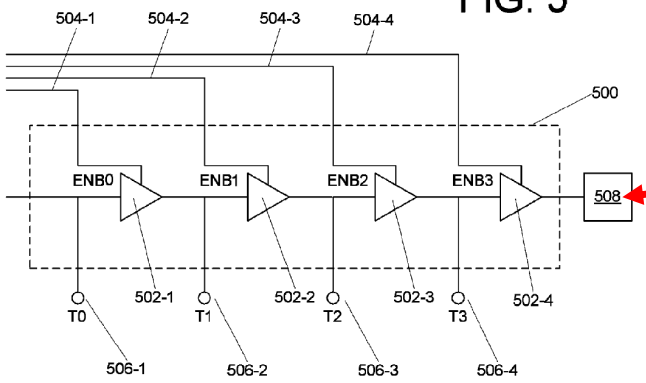


EX1017 (Wyman) at Fig. 8B

FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. In other words, the

EX1017 (Wyman) at 6:21-:26

FIG. 5



(506-3) would be inadequate, but the total drive from the pad (508) would be overkill. In this case, the designer could tap

EX1017 (Wyman) at 6:48-:49

GROUNDS 1-3 (’060) AND GROUND 1 (’160)

02

GROUND 1 (’060): KIM+RAJAN

GROUND 2 (’060): KIM+RAJAN+RIHO

GROUND 3 (’060), GROUND 1 (’160): KIM+RAJAN+WYMAN

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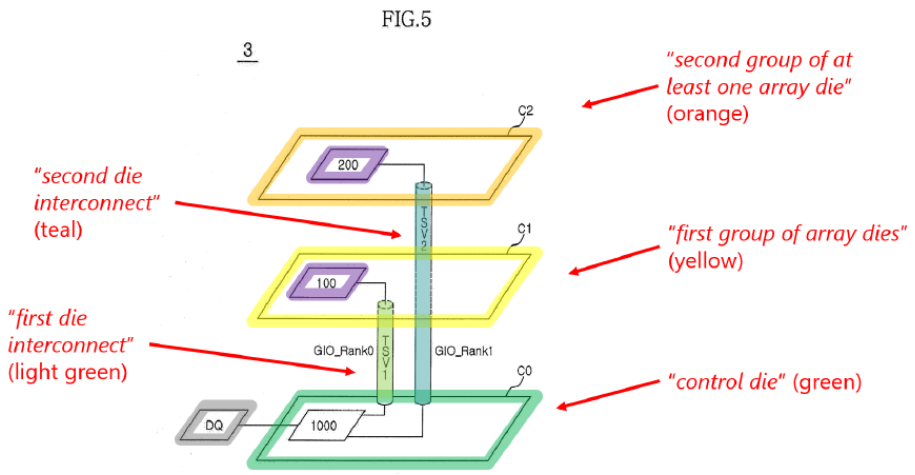
SUMMARY OF COMBINATIONS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Ground 1 ('060): Kim + Rajan

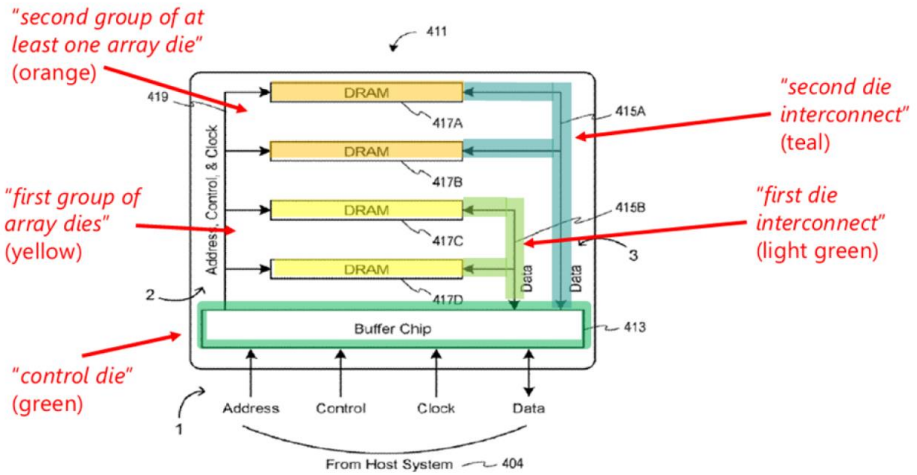
Kim: Separate TSVs to stacked memory chips



[0048] FIG. **5** shows an exemplary embodiment in which one main chip C0 and two slave chips C1 and C2 are stacked. Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used. In the 3D semiconductor apparatus in which the

EX1014 (Kim) at [0048] & Fig. 5

Rajan: (1) additional stacked memory chips for rank multiplication and (2) JEDEC interface

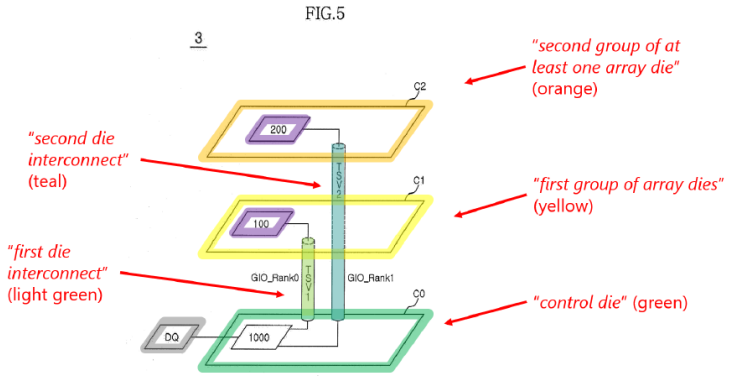


If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

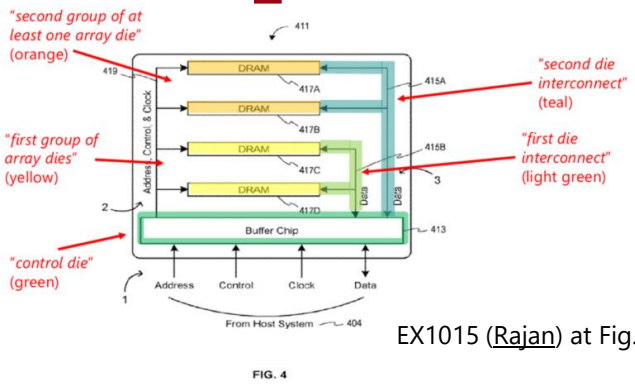
EX1015 (Rajan) 6:30-:38 & Fig. 4

Ground 2 ('060): Ground 1 + Riho

Kim's stack with Rajan's JEDEC interface and additional ranks of memory chips

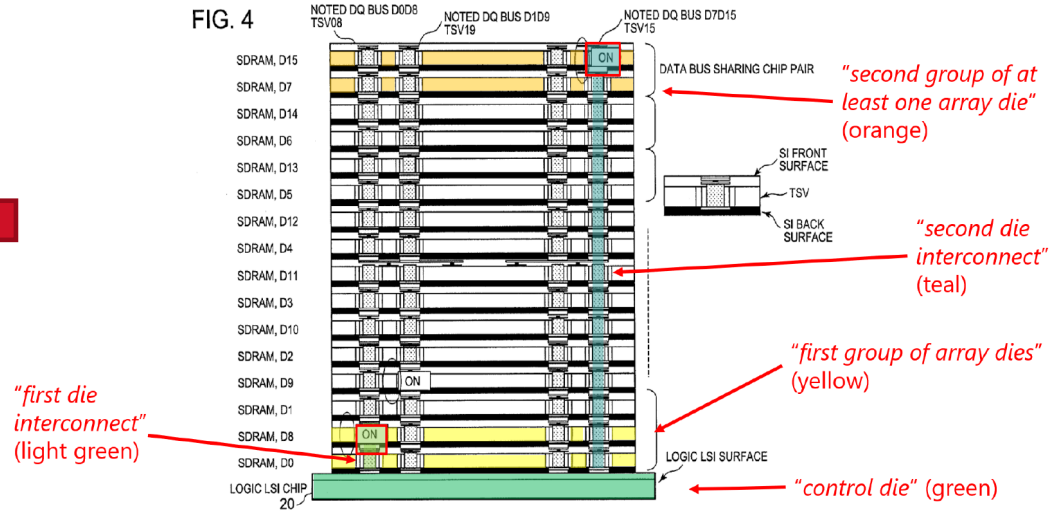


EX1014 (Kim) at Fig. 5



EX1015 (Rajan) at Fig. 4

Riho: grouping two memory chips per TSV reduces load, and equi-length TSVs minimize skew



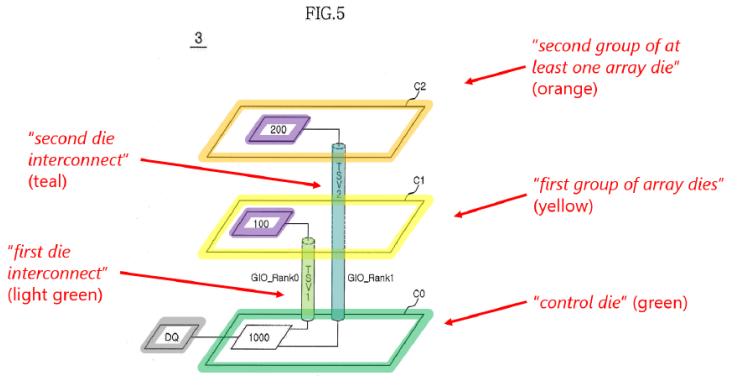
EX1016 (Riho) at Fig. 4

'060: Paper 1 (Pet.) at 81-83; Paper 24 (Reply) at 16-17; EX1003, ¶¶ 169-173, 339-341

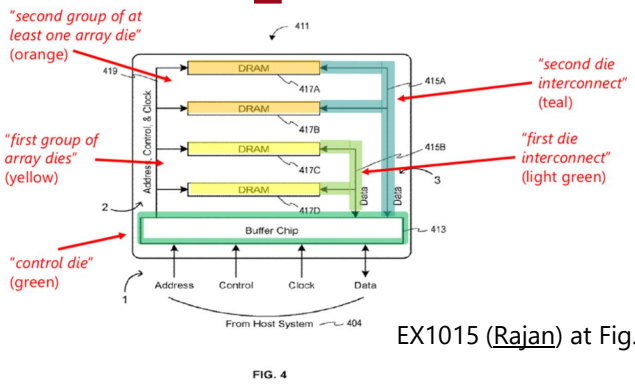
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Ground 3 ('060) / Ground 1 ('160): Ground 1 ('060) + Wyman

Kim's stack with Rajan's JEDEC interface and additional ranks of memory chips



EX1014 (Kim) at Fig. 5



EX1015 (Rajan) at Fig. 4

Wyman: additional drive for longer die interconnects

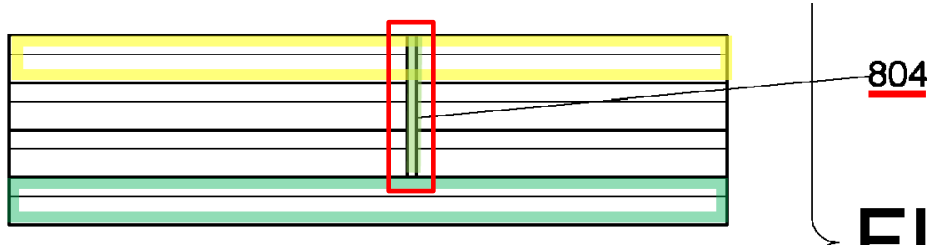


FIG. **8B** illustrates, in simplified form, a longer through-chip via connection (**804**) extending directly between the mother chip (**700-4**) and daughter **3** (**700-1**) in a straight line. The increased resistance, capacitance and impedance of such a connection (**804**) might require additional drive than that referred to in connection with FIG. **8A**. In other words, the

EX1017 (Wyman) at 6:21-:26 & Fig. 8B

'060: Paper 1 (Pet.) at 83-91; Paper 24 (Reply) at 16-17
'160: Paper 1 (Pet.) at 23-80; Paper 24 (Reply) at 2-19

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REASONABLE EXPECTATION OF SUCCESS: COLLISIONS ON SHARED DATA LINES WERE AVOIDABLE

"GROUP OF ARRAY DIES" CLAIM CONSTRUCTION

GROUND 1 ('160)

GROUNDS 1-3 ('060)

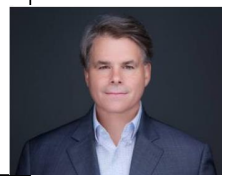
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

Undisputed: collisions on shared data lines would be avoided

Q. It was also known to a person of ordinary skill in the art that multiple chips in different ranks could share the same data line without causing collisions, correct?

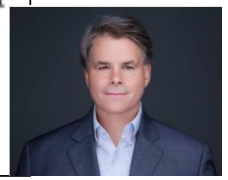
A. In certain contents, correct.



EX1052 (Brogioli) at 315:20-:24

Q. And, in general, a person of ordinary skill in the art would be motivated to avoid collisions and loss of data; is that fair?

A. As we have talked about earlier today and yesterday, in a general sense, I think that's -- that's fair.

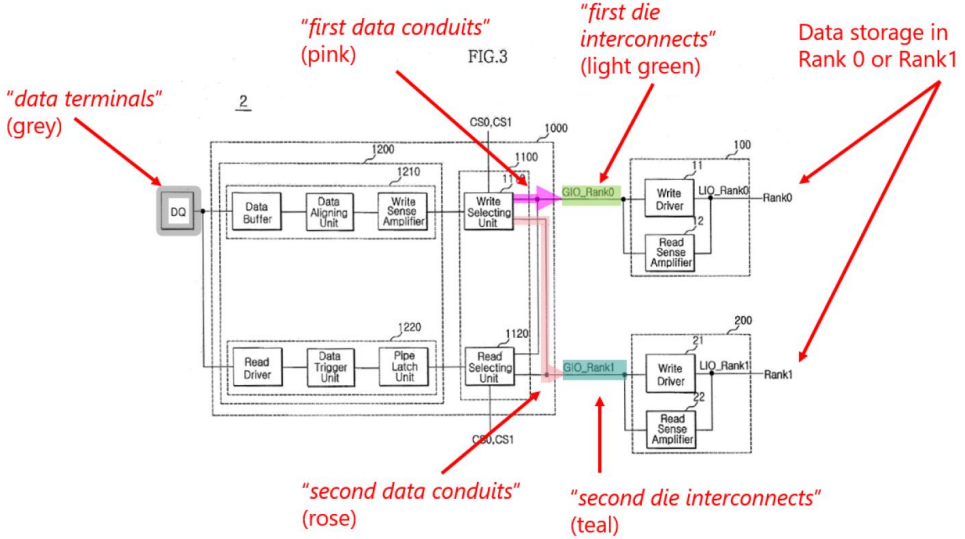


EX1052 (Brogioli) at 318:1-:6

'060: Paper 24 (Reply) at 4
'160: Paper 24 (Reply) at 4

Kim + Rajan does not result in data collisions

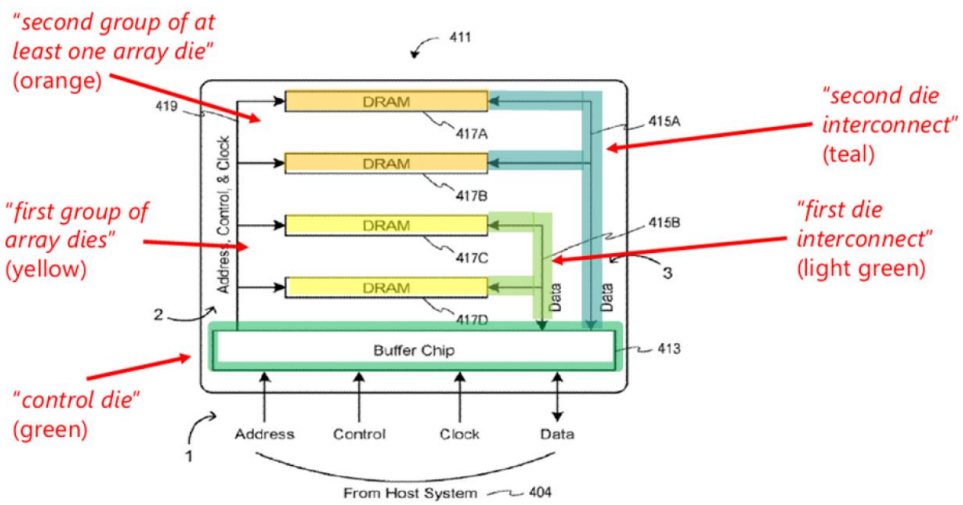
Kim



[0044] Conversely, in the semiconductor memory apparatus **2** in accordance with one embodiment of the present invention, since the first and second ranks Rank**0** and Rank**1** share the data input/output unit **1200** and have the rank selecting unit **1100** which responds to the chip selection signals CS**0** and CS**1**, a data collision as described above does not occur. First, when the write operation of the first rank Rank**0**

EX1014 (Kim) at [044] & Fig. 3

Rajan



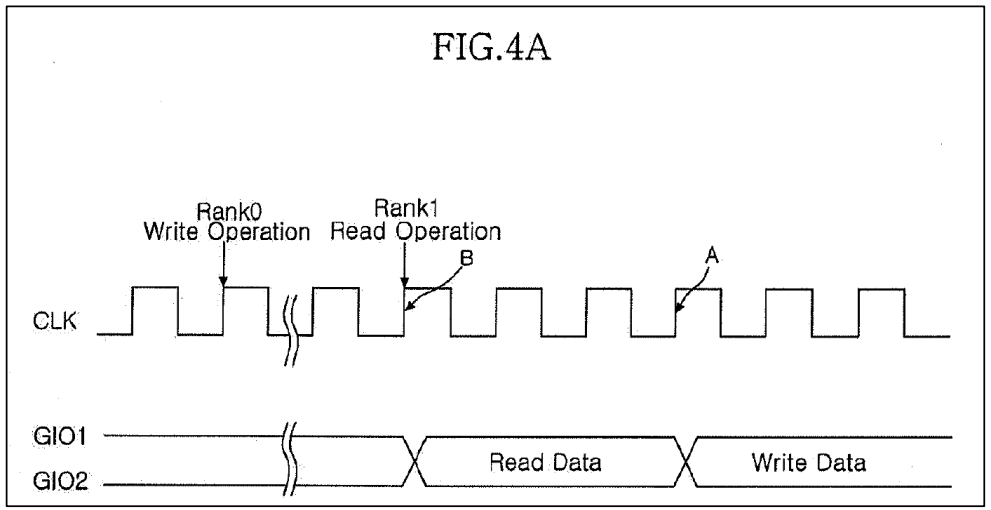
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

Netlist's theory: any combination with Kim results in "unavoidable" data collisions

[0042] FIG. **4**A shows a problem that is caused in a typical semiconductor memory apparatus because the first and second ranks Rank**0** and Rank**1** cannot share a data input/output circuit. Even when a read operation and a write operation for either of the first and second ranks Rank**0** and Rank**1** are successively performed, a data collision does not occur. That is, since the read operation and the write operation for one rank are performed with a predetermined time interval set therebetween, even when the read operation and the write operation are alternately performed, a data collision does not occur. However, in the case where the write operation of the first rank Rank**0** is performed and then the read operation of the second rank Rank**1** is performed, a data collision is unavoidable. Assuming that the first and second ranks Rank**0** and Rank**1** share a data input/output circuit, first and second data input/output lines operate in the same manner. Since it takes a time for data inputted through the data pad DQ to pass through the data input/output section, when the write operation of the first rank Rank**0** is performed, a time A at which the data is actually loaded on the data input/output line is after a certain time interval is lapsed. That is to say, the write data is loaded on the data input/output line GIO**1** or GIO**2** at the time A.

EX1014 (Kim) at [0042]



EX1014 (Kim) at Fig. 4A

'060: Paper 20 (POR) at 7-8; Paper 24 (Reply) at 2-13
'160: Paper 20 (POR) at 7-8; Paper 24 (Reply) at 2-14

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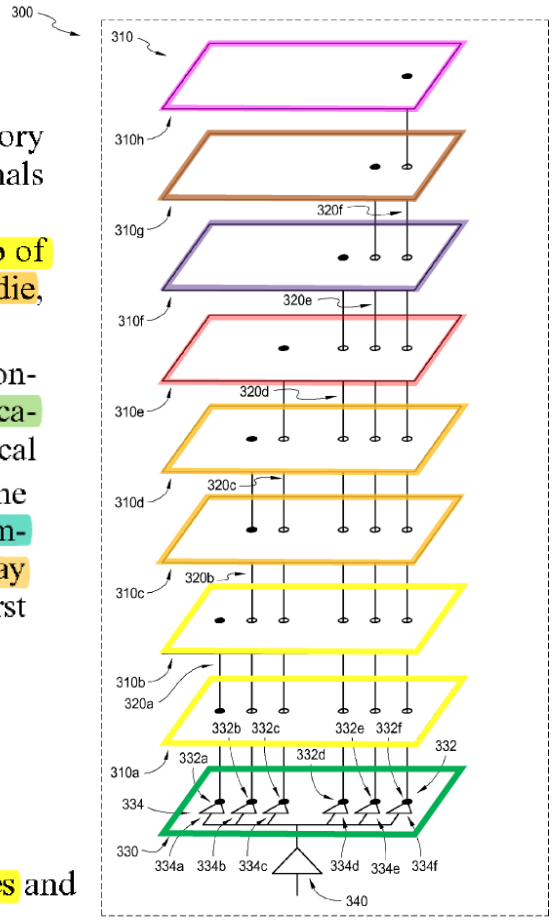
Netlist's collision theory assumes the claims require a "*group of at least two array dies,*" but the actual claim language ("*first group of array dies*") can include just one die

'060 Patent, Claim 1:

1. A memory package, comprising:
a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

'160 Patent, Claim 1:

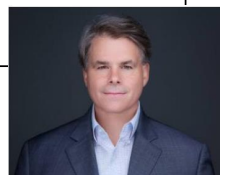
1. A memory package, comprising:
data terminals and control terminals;
stacked array dies including a first group of array dies and a second group of at least one array die;



Q. You have not offered any opinion about the validity of the '160 patent or the '060 patent if the claimed first group of array dies is satisfied by a **single** array die; correct?

A. I don't recall offering opinions on that one way or the other in this declaration or addressing that specifically.

EX1052 (Brogioli) at 130:22-131:3



'060: EX1001 at Fig. 3, 13:6-:18
'160: EX1001 at Fig. 3, 13:1-:10

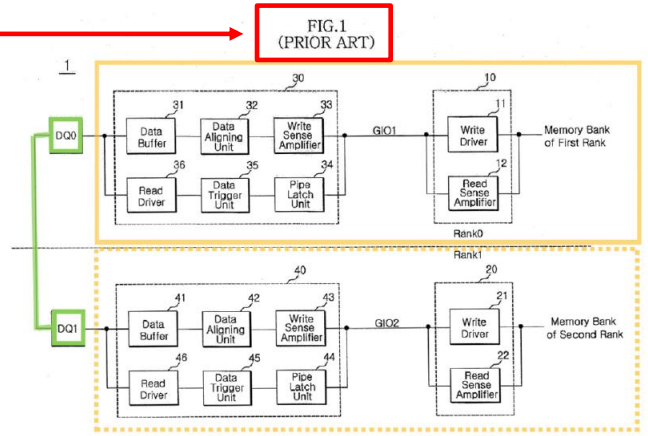
'060: Pet. at 34-40; Paper 24 (Reply) at 7-8; Paper 28 (Sur-Reply) at 10-11
'160: Pet. at 39-43; Paper 24 (Reply) at 8-9; Paper 28 (Sur-Reply) at 11-12

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"Unavoidable" data collision in Kim refers to prior-art input/output circuit being shared unbeknownst to the controller (thus without proper timing)

[0042] FIG. **4**A shows a problem that is caused in a typical semiconductor memory apparatus because the first and second ranks Rank**0** and Rank**1** cannot share a data input/output circuit. Even when a read operation and a write operation for either of the first and second ranks Rank**0** and Rank**1** are successively performed, a data collision does not occur. That is, since the read operation and the write operation for one rank are performed with a predetermined time interval set therebetween, even when the read operation and the write operation are alternately performed, a data collision does not occur. However, in the case where the write operation of the first rank Rank**0** is performed and then the read operation of the second rank Rank**1** is performed, a data collision is unavoidable. Assuming that the first and second ranks Rank**0** and Rank**1** share a data input/output circuit, first and second data input/output lines operate in the same manner. Since it takes a time for data inputted through the data pad DQ to pass through the data input/output section, when the write operation of the first rank Rank**0** is performed, a time A at which the data is actually loaded on the data input/output line is after a certain time interval is lapsed. That is to say, the write data is loaded on the data input/output line GIO**1** or GIO**2** at the time A.

EX1014 (Kim) at [0042]



EX1014 (Kim) at Fig. 1

Q. Okay. And in those systems, is data collision avoidable as described in 42?
A. Data collision is always avoidable. The question is what constraints the system designer wants to place on time. If one carefully reads 42, paragraph 42 and 43 of Kim, they're not saying that that problem is unavoidable, but merely that they think that they have an improvement.
Q. Okay. So I don't understand. Why would there be a data collision problem when you do a read operation after a write operation across the rank?
....
THE WITNESS: Because in this one very narrow circumstance that is being discussed, these are burst operations and burst operations require multiple data transfers. And in this one particular example, the command to data delays have not been properly selected for optimal performance on a two-rank system. But there are many, many known solutions to that problem.



EX2025 (Wolfe) at 69:24-70:18

Netlist's collision theory is based on bodily incorporating Kim's prior-art input/output circuit, ignoring Rajan and a POSITA's knowledge

"The test for obviousness is not whether the feature of a secondary reference may be bodily incorporated into the structure of the primary reference, but rather whether a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention."

Elbrus Int'l Ltd. v. Samsung Elecs. Co.,
783 F. App'x 694, 698-99 (Fed. Cir. 2018)

"It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements."

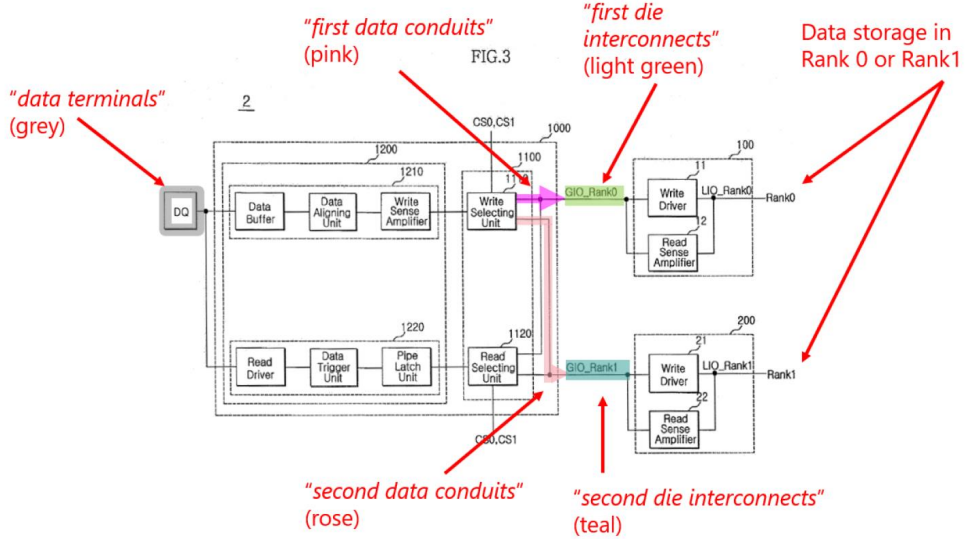
In re Mouttet,
686 F.3d 1322, 1332 (Fed. Cir. 2012)

'060: Paper 24 (Reply) at 3, 12-13; Paper 20 (POR) 38-44
'160: Paper 24 (Reply) at 3, 13-14; Paper 20 (POR) 38-44

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The proposed combination does not use Kim's prior art (Figure 1), and Netlist's collision theory ignores the teachings of Rajan

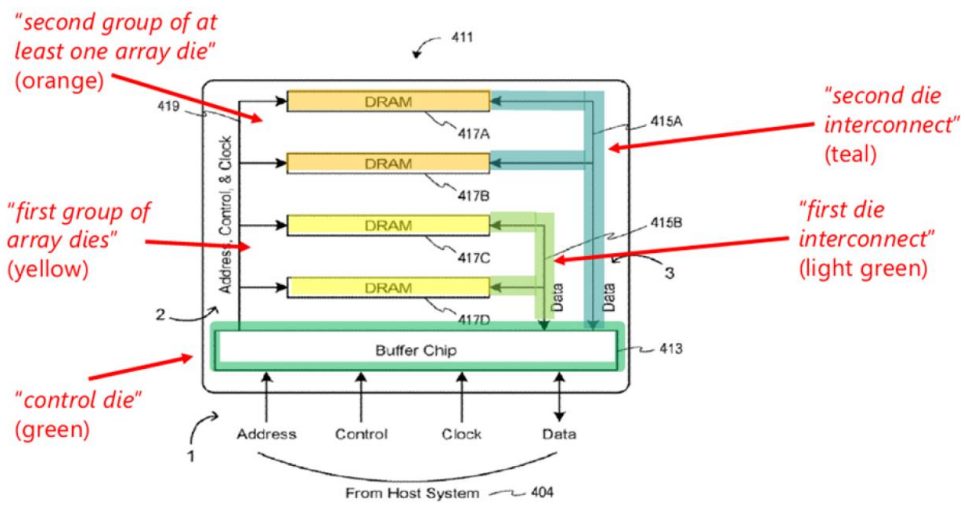
Kim



[0044] Conversely, in the semiconductor memory apparatus **2** in accordance with one embodiment of the present invention, since the first and second ranks Rank**0** and Rank**1** share the data input/output unit **1200** and have the rank selecting unit **1100** which responds to the chip selection signals CS**0** and CS**1**, a data collision as described above does not occur. First, when the write operation of the first rank Rank**0**

EX1014 (Kim) at [044] & Fig. 3

Rajan



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

Kim teaches avoiding collisions by selectively performing operations with a "predetermined time interval set therebetween"

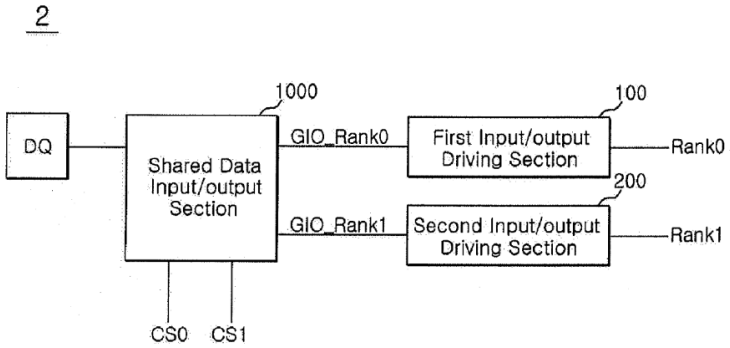
[0031] Accordingly, even though the first and second ranks Rank**0** and Rank**1** may comprise one data input/output circuit, the semiconductor memory apparatus **2** may allow a read operation and a write operation to be selectively performed for one of the first and second ranks Rank**0** and Rank**1** in response to the chip selection signals CS**0** and CS**1**, whereby it is possible to prevent a data collision from occurring.

EX1014 (Kim) at [0031]

circuit. Even when a read operation and a write operation for either of the first and second ranks Rank**0** and Rank**1** are successively performed, a data collision does not occur. That is, since the read operation and the write operation for one rank are performed with a predetermined time interval set therebetween, even when the read operation and the write operation are alternately performed, a data collision does not occur. However, in the case where the write operation of the

EX1014 (Kim) at [0042]

FIG.2

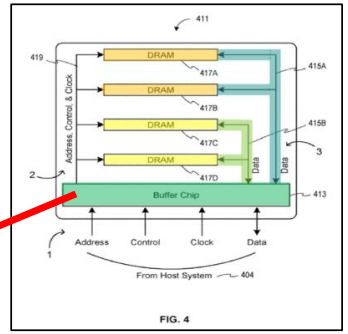


EX1014 (Kim) Fig. 2

'060: Paper 1 (Pet.) at 29-30, 40, 49; Paper 24 (Reply) at 3
'160: Paper 1 (Pet.) at 31-32, 43, 67; Paper 24 (Reply) at 3

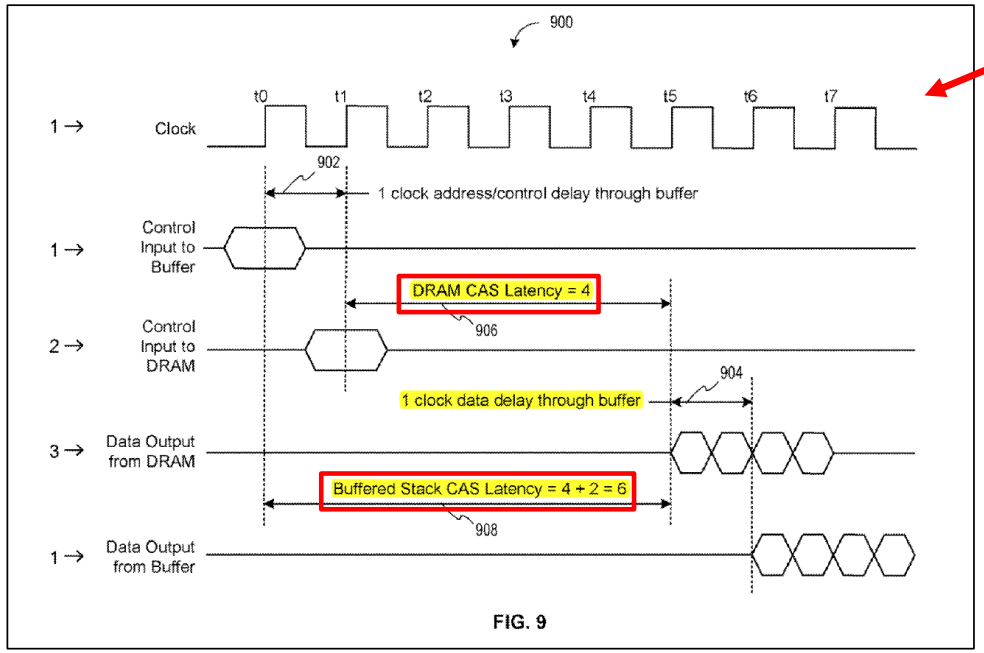
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Rajan also teaches adding delays (e.g., in the buffer) to avoid collisions



EX1015 (Rajan) at Fig. 4





EX1015 (Rajan) at Fig. 9

Q. So from the perspective of the system memory controller and the host computer, in this Figure 9 example of Rajan marked as Exhibit 1015, the CAS latency appears to be six clock cycles as a result of the emulation by the buffer chip; is that fair?

A. That -- that sounds right, that that's the host -- the host view of the CAS latency.

EX1052 (Brogioli) at 192:1-:8

Rajan also teaches adding delays (e.g., in the buffer) to avoid collisions

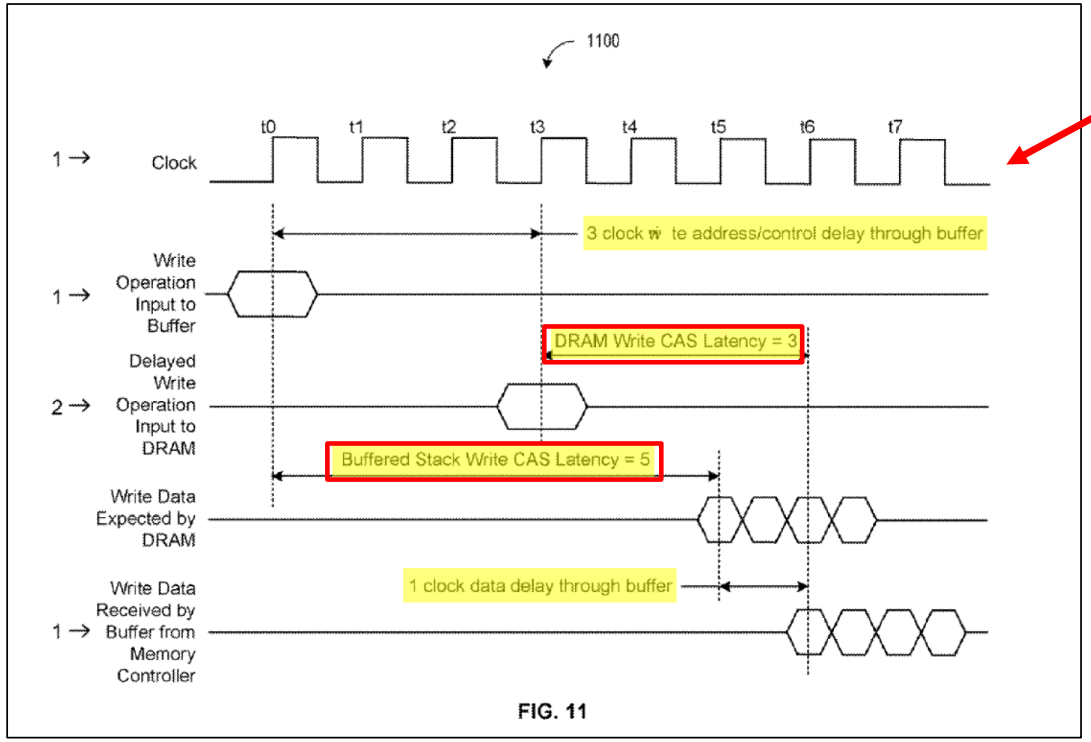


FIG. 11

EX1015 (Rajan) at Fig. 11

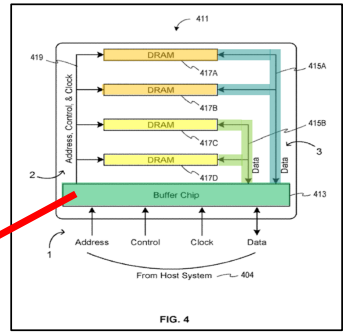


FIG. 4

EX1015 (Rajan) at Fig. 4



Q. And just to be clear, though, the buffer has a one clock cycle delay; but then it also adds another two clock cycles of delay for the write operation as stated as Column 10, line 18, in this example of Figure 11; correct?

A. That sounds right. The end of this

EX1052 (Brogioli) at 194:16-:25

'060: Paper 1 (Pet.) at 79-80; Paper 24 (Reply) at 6-7
'160: Paper 1 (Pet.) at 78-80 ; Paper 24 (Reply) at 6-7

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Alternatively, the controller on the host can add delays to avoid collisions



THE WITNESS: That generally what this section is talking about is making sure a piece of data shows up at Rajan's DRAM at the exact point in time it's supposed to. And one way to do that is the -- is based with the buffer chip adjustment, and one is with the -- I'm sorry -- AMB adjustment and so forth.

BY ATTORNEY CHANDLER:

Q. And the other way is with the memory controller making the adjustment; correct?

THE WITNESS: Similarly, for this example of write data arriving at a DRAM in Rajan, you can adjust -- make an adjustment in the memory controller for this small example in Figure 12.

EX1052 (Brogioli) at 198:1-:15

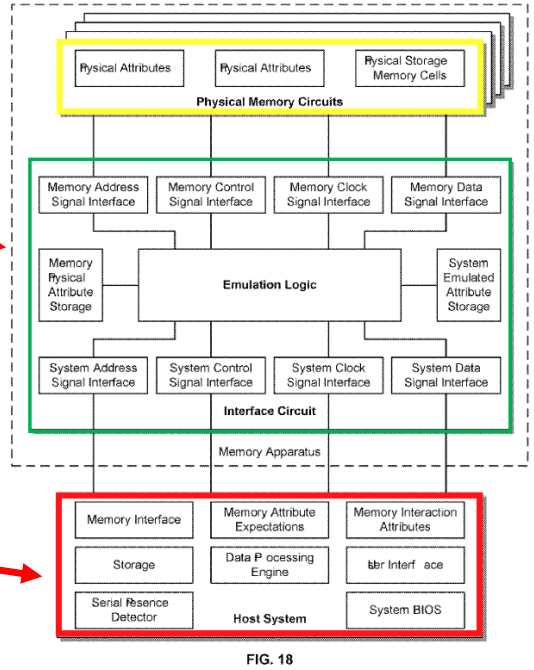
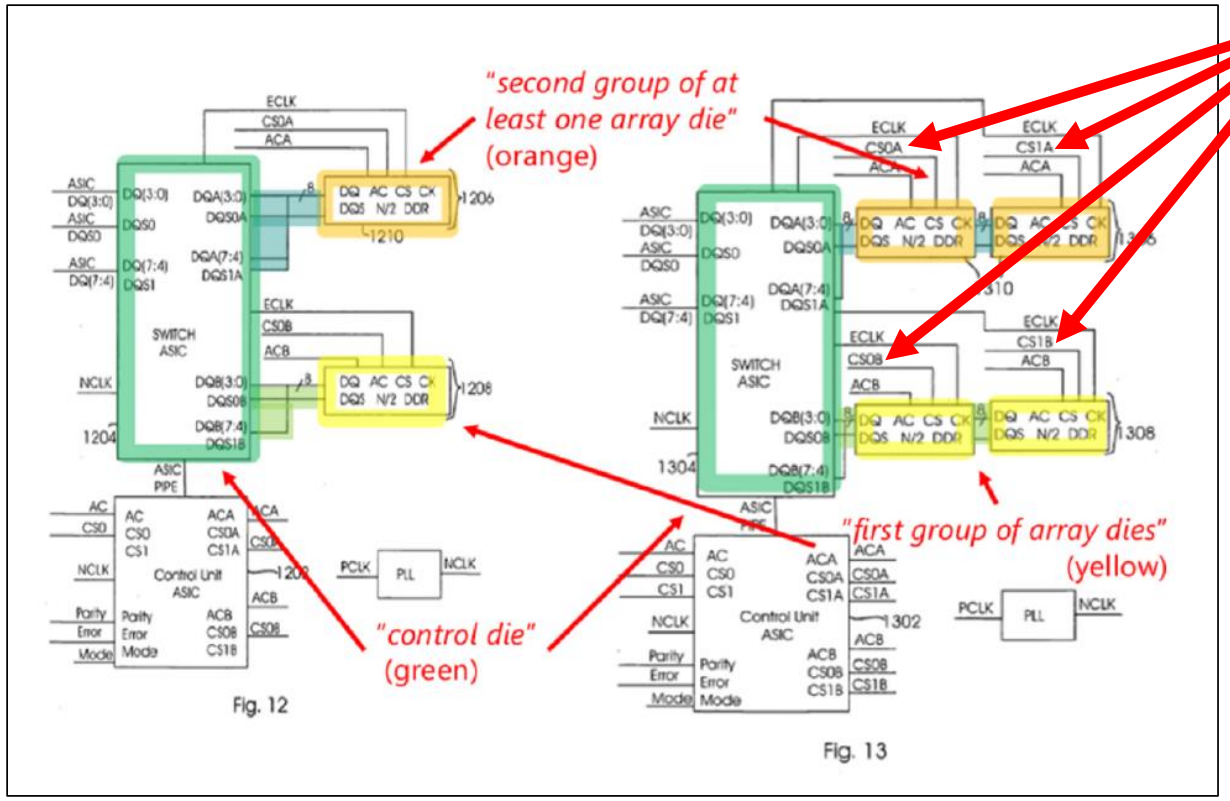


FIG. 18

EX1015 (Rajan) at Fig. 18

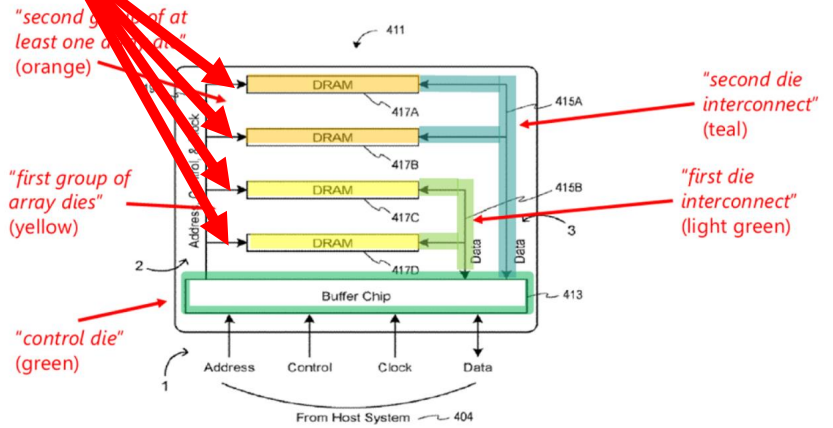
'060: Paper 1 (Pet.) at 80; Paper 24 (Reply) at 6-7
'160: Paper 1 (Pet.) at 79-80 ; Paper 24 (Reply) at 6-7

Rajan's separate chip selects and shared data buses (on the right) were well known for rank multiplication (without data collisions) as shown by Ellsberry (on the left)



EX1026 (Ellsberry) at Figs. 12-13

Four separate chip selects (CS0A, CS1A, CS0B, CS1B), one for each rank (four ranks total)



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

'060: Paper 1 (Pet.) at 27, 29-30; Paper 24 (Reply) at 8-9
'160: Paper 1 (Pet.) at 29, 21-32; Paper 24 (Reply) at 9-10

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Undisputed: JEDEC standards taught how to avoid collisions on shared data lines (green) using properly timed chip-select signals (red) for commands



Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

EX1019 at 12

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

EX1019 at 33

Q. (By Mr. Chandler) And a person of ordinary skill in the art, reviewing the stacked memory devices shown on page 12 of the DDR3 standard marked as Exhibit 1019, would expect those stacked memory devices to operate correctly, without collisions, on the set of data lines labeled "DQ0-7," correct?

THE DEPONENT: I think they would understand this figure to be describing one way of implementing this D- -- DDR3 implementation within the confines of JEDEC and, taken as a whole, to provide an operating -- or a correctly operating device -- a functioning operational device per JEDEC's definition.



EX1052 (Brogioli) at 303:12-304:1

'060: Paper 1 (Pet.) at 46; Paper 24 (Reply) at 4-5
'160: Paper 1 (Pet.) at 37-38; Paper 24 (Reply) at 4-5

JEDEC standard taught using programmable timing parameters (e.g., CAS latency, CL, of 5 to 10 clock cycles) to avoid collisions

Q. Under the JEDEC standard for DDR3 memory devices, CAS latency could be set to 5, 6, 7, 8, or 9 clock cycles, as shown on page 23 of Exhibit 1019; is that correct?

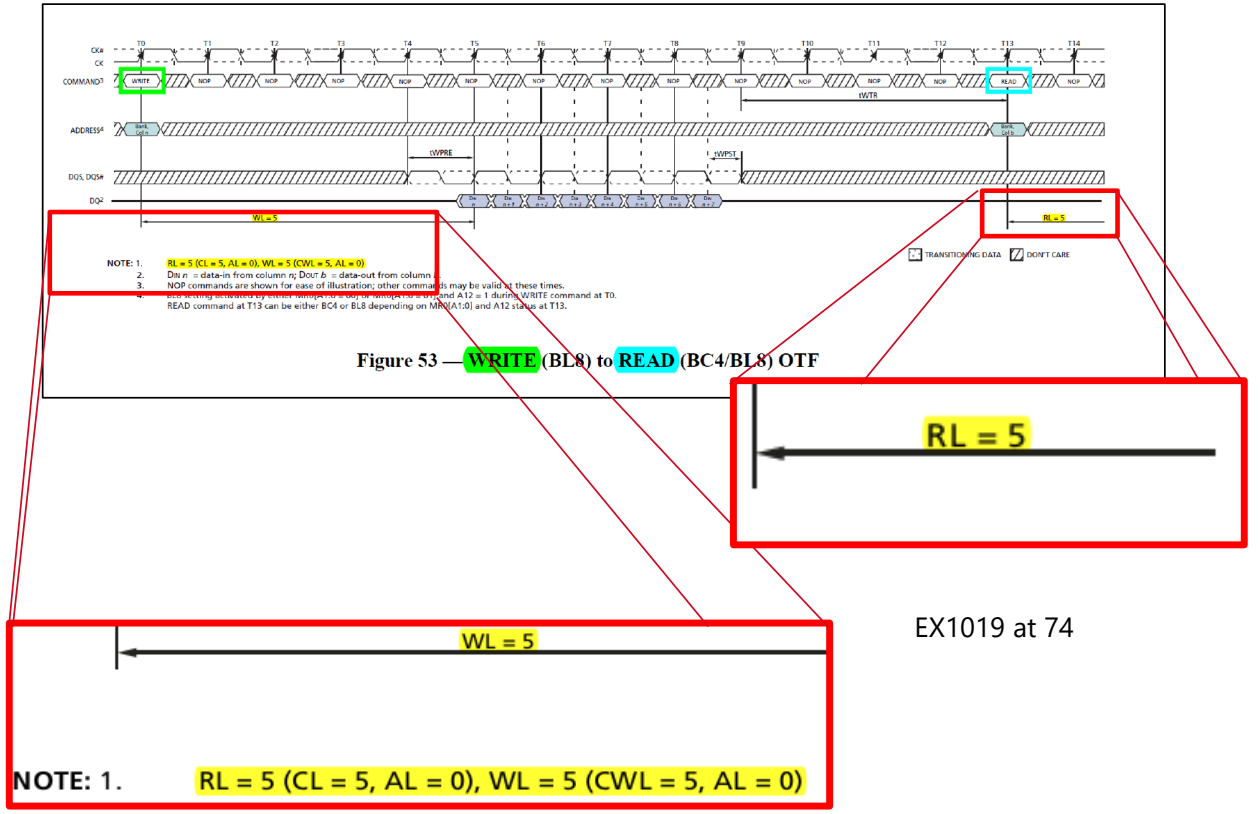
A. That looks like at least some of the values that the -- excuse me -- that the CAS latency could be set to. I think you mentioned 5 through 9.

Q. Or 10 clock cycles; right? That's also specified in the standard?

A. I see that, yes. Those are the -- that's the CAS latency. You set the bits accordingly to get a different value.

EX1052 (Brogioli) at 110:5-:17;
see also id. at 116:2-117:9



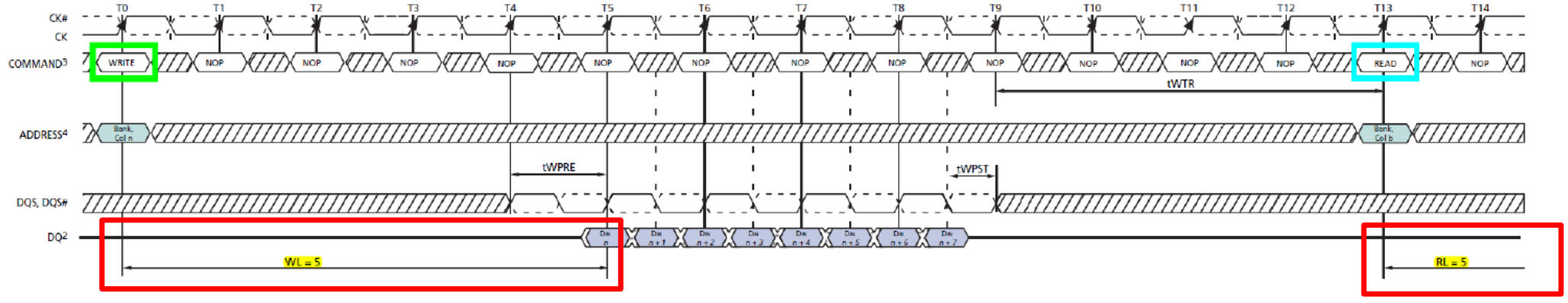


EX1019 at 74

'060: Paper 24 (Reply) at 4-5
'160: Paper 24 (Reply) at 4-5

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JEDEC standard teaches that READ latency (RL) can be increased independently of WRITE latency (WL), so no collision



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0. READ command at T13 can be either BC4 or BL8 depending on MR0[A1:0] and A12 status at T13.

Figure 53 — WRITE (BL8) to READ (BC4/BL8) OTF

EX1019 at 74;
EX1052 (Brogioli) at 116:2-117:9

problem with shared TSVs. For instance, if the read and write latencies were increased by the same amount, read and write data would still appear at the same relative timing and collisions would still occur, as illustrated below.

'060: Paper 28 (Sur-Reply) at 6-8:
'160: Paper 28 (Sur-Reply) at 6-8:

'060: Paper 24 (Reply) at 4-5
'160: Paper 24 (Reply) at 4-5

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Kim + Rajan can emulate timing from the JEDEC standard, even if the memory chips are not DRAM

The physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc.

EX1015 (Rajan) at 15:3-:9

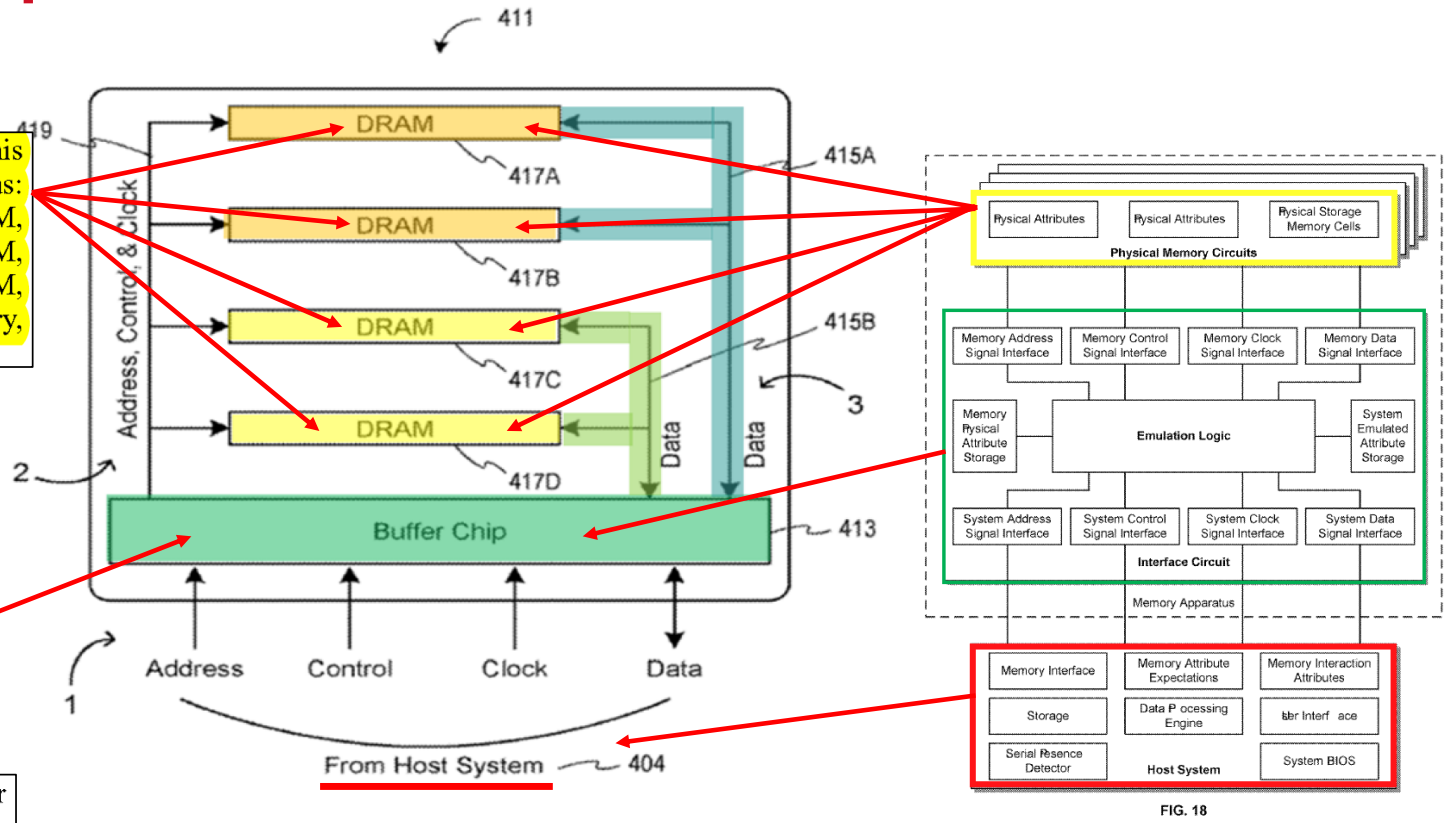


FIG. 4

FIG. 18

The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

EX1015 (Rajan) at 4:20-:24; *see also id.* at 4:48-:50, 14:6-:11, 14:39-:62 & Fig. 18

The admitted prior art in the '060 and '160 Patents teaches how to avoid data collisions (e.g., by adding "one-clock cycle" to CAS latency)

In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Pat. Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912,

'060: EX1001 at 4:7-:11 *see also id.* at 19:44-:47, 22:34-:40
'160: EX1001 at 4:11-:15; *see also id.* at 19:29-:32, 22:21-:25

In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

EX1031 (537 patent) at 21:28-:53 (published Nov. 23, 2006)

'060: Paper 24 (Reply) at 5-6
'160: Paper 24 (Reply) at 5-6

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Ex. 1067, p. 41

The admitted prior art in the '060 and '160 Patents teaches how to avoid data collisions (e.g., by "inserting a delay")

In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Pat. Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912,

'060: EX1001 at 4:7-:11 *see also id.* at 19:44-:47, 22:34-:40
'160: EX1001 at 4:11-:15; *see also id.* at 19:29-:32, 22:21-:25



Q. In paragraph 91, in the second sentence, you express the opinion that "a person of ordinary skill in the art could readily configure the memory controller in a memory system featuring the '436 module to use appropriate timing sequences to avoid such collisions by inserting a delay between successive read commands, without the need to know the physical boundaries of the memory devices. The... designer could also use a serial presence detect (SPD) device to inform the memory controller of the physical boundaries of each memory device."

Did I read that accurately?

A. Yes, you did.

Q. And have you changed your opinions since you wrote that on August 10th, 2023?

A. Those statements, in the context of this -- the '912 declaration? No, my opinions stay the same.

EX1052 (Brogioli) at 289:11-290:3

'060: Paper 24 (Reply) at 5-6
'160: Paper 24 (Reply) at 5-6

Samsung Electronics Co., Ltd.
Ex. 1067, p. 42

The admitted prior art in the '060 and '160 Patents teaches how to avoid data collisions (e.g., by inserting "wait-time intervals or clock cycles")

In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Pat. Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912,

'060: EX1001 at 4:7-:11 *see also id.* at 19:44-:47, 22:34-:40
'160: EX1001 at 4:11-:15; *see also id.* at 19:29-:32, 22:21-:25



EX1052 (Brogioli) at 279:16-280:6;
see also EX1058 (912 patent) at 23:60-:67

Q. What technique does the '912 patent marked as Exhibit 1058 state, here at column 23, line 60 through 67, for avoiding collisions when memory devices in two different ranks share a data line?

MR. LINDSAY: Objection. Outside the scope of direct.

THE DEPONENT: It looks like, in this paragraph, the '912 is talking about memory boundaries between ranks in a memory module and that in the case of what it refers to as a back-to-back adjacent read command, it, at least from the language of this paragraph, says the memory controllers can insert wait-time intervals or clock cycles to avoid collisions or interference in that scenario.

'060: Paper 24 (Reply) at 5-6
'160: Paper 24 (Reply) at 5-6

Samsung Electronics Co., Ltd.
Ex. 1067, p. 43

Jacob textbook also taught adding delays or write buffers to avoid collisions

proper columns of the selected bank. Since the I/O gating resource is shared between all banks within a rank of DRAM devices, the sharing of the I/O gating device means that a read command that follows a write command to the same rank of DRAM devices must wait until the write command has been completed before the read command can make use of the shared I/O gating resources regardless of the target or destination bank IDs of the respective column access commands. Figure 11.23 shows that the minimum scheduling distance between a write command and a subsequent read command to the same rank of memory is $t_{CWD} + t_{BURST} + t_{WTR}$.

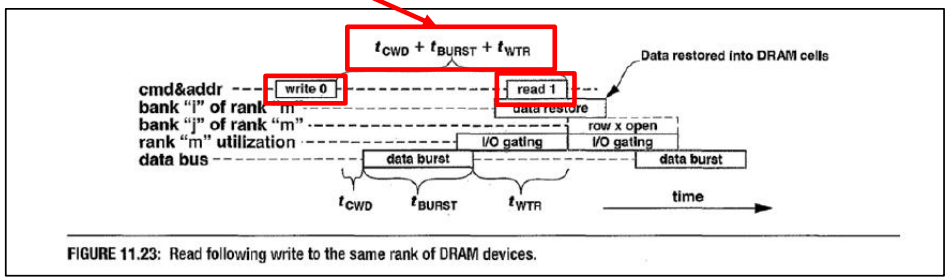


FIGURE 11.23: Read following write to the same rank of DRAM devices.

Memory Systems

Cache, DRAM, Disk

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In order to alleviate the write-to-read turnaround time illustrated in Figure 11.23, some high-performance DRAM devices such as Rambus Direct RDRAM have been designed with write buffers so that as soon as data has been written into the write buffers, the I/O gating resource can be used by another command such as a column-read command.

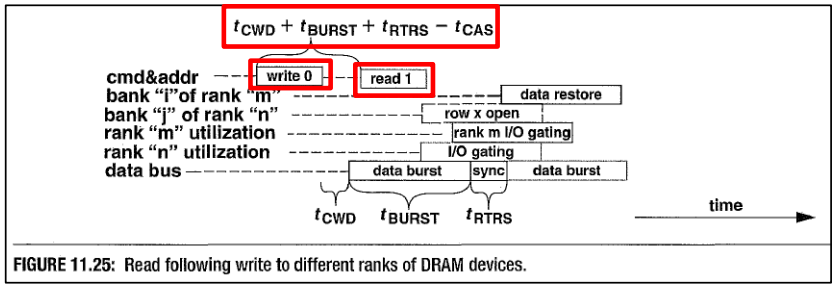
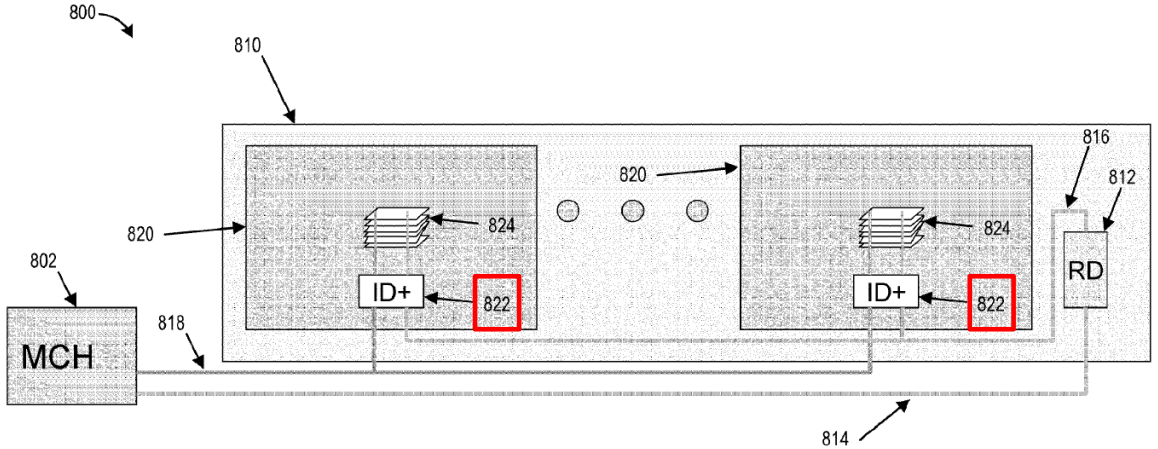


FIGURE 11.25: Read following write to different ranks of DRAM devices.

EX1022 (Jacob) at 446-447

The ‘060 and ‘160 Patents do not teach any solutions to data collisions beyond what was known in the admitted prior art



Controlling the command/address time slots and the data bus time slots enables the control dies **822** to reduce or prevent signal collisions caused by multiple memory packages **820** sharing the data path control lines **816** and the data bus **818**. In some implementations, the data path control circuit may be separate from the control die **822**.

‘060: EX1001 at Fig. 8, 21:51-:56
‘160: EX1001 at Fig. 8, 21:36-:41

“[T]he [challenged] patent itself does not disclose the level of detail that [Patent Owner] would have us require of the prior art.”

Lockwood v. Am. Airlines, Inc.,
107 F.3d 1565, 1570 (Fed. Cir. 1997)
(affirming summary judgment of invalidity)

‘060: Paper 24 (Reply) at 5-6 , 12
‘160: Paper 24 (Reply) at 5-6, 13

Samsung Electronics Co., Ltd.
Ex. 1067, p. 45

Netlist's collision theories are based on "strawman" arguments, not the actual combination proposed in the Petition by Dr. Wolfe

Q. And as far as you know -- as far as you know, nobody showed the figures that you created in your declaration marked as Exhibit 2023 to Dr. Wolfe to ask him if those figures accurately represented his opinions, correct?

A. I am -- I am not aware one way or the other, sure.



EX1052 (Brogioli) at 319:2-:8

Q. And you are not aware of anyone ever showing those modified figures or variations of those modified figures to Dr. Wolfe during his deposition so that he could comment on whether or not they accurately represent his opinions, correct?

A. I am not aware of the figures being shown to Dr. Wolfe one way or the other.



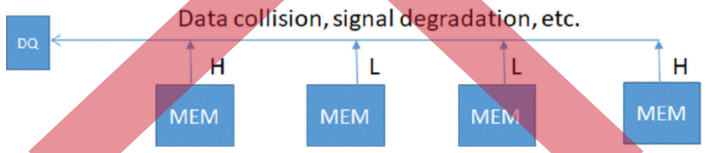
EX1052 (Brogioli) at 325:7-:14

'060: Paper 24 (Reply) at 10; Paper 20 (POR) at 23-27
'160: Paper 24 (Reply) at 11; Paper 20 (POR) at 23-27

Samsung Electronics Co., Ltd.
Ex. 1067, p. 46

Petition did NOT propose multiple chips in same rank sharing same TSV for data (Netlist's Strawman #1)

92. A person of ordinary skill in the art would not have modified Kim in such a way that chips from the same rank share a TSV because such a modification would result in data collisions, for example, when chips of the same rank output bits of different value to the same TSV (which is just a type of conductive wire) concurrently. *See* illustration below. This would cause electrical problems, signal degradation and even damages to circuits.



EX2023 at ¶ 92

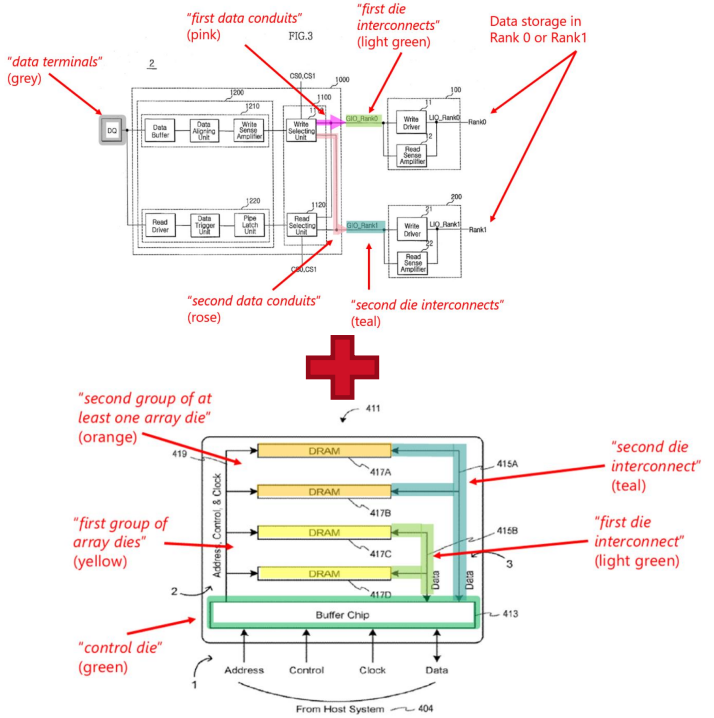
Q. In your opinion, would a person of ordinary skill in the art know that if four memory devices are simultaneously outputting data to the same data lines, that, as a result, there could be a collision?

A. In this high-level example, yes.



EX1052 (Brogioli) at 314:8-:11

Kim + Rajan



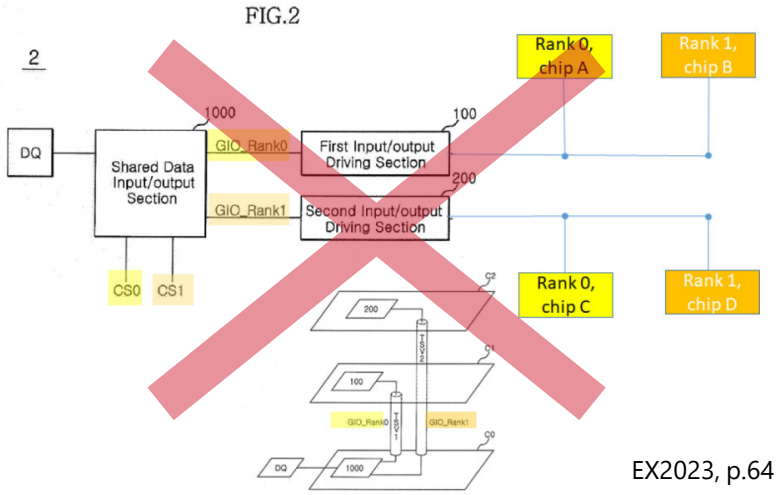
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

'060: Paper 24 (Reply) at 10; Paper 20 (POR) at 23-27
'160: Paper 24 (Reply) at 11; Paper 20 (POR) at 23-27

Samsung Electronics Co., Ltd.
Ex. 1067, p. 47

Petition did NOT propose cross-connecting TSVs and ranks (Netlist's Strawman #2)



EX2023, p.64

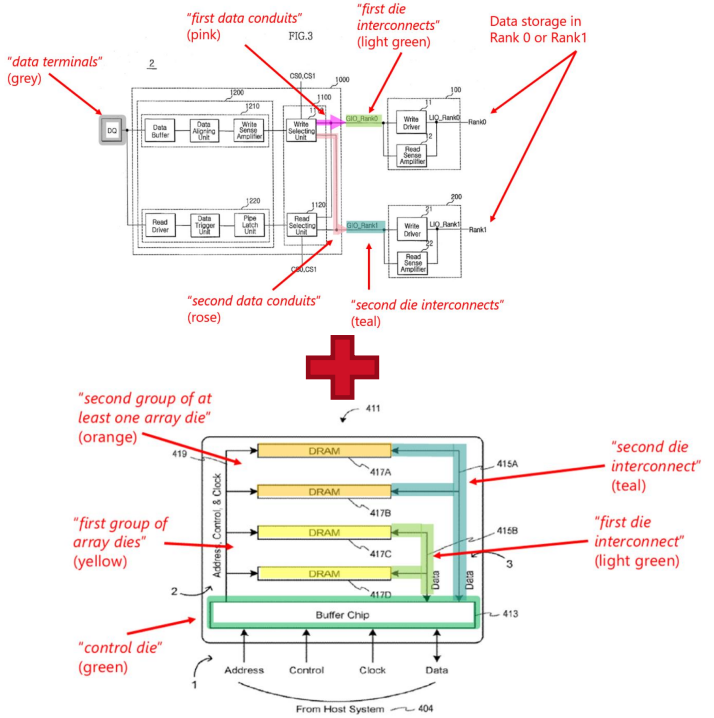
Q. Kim, marked as Exhibit 1014, does not teach having a chip in Rank0 connected to GIO_Rank1 and does not teach having a chip in Rank1 connected to GIO_Rank0 as you have shown at the top of page 64 of your declaration marked as Exhibit 2023, correct?

A. I don't believe Kim explicitly teaches that, no.



EX1052 (Brogioli) at 317:8-:15

Kim + Rajan



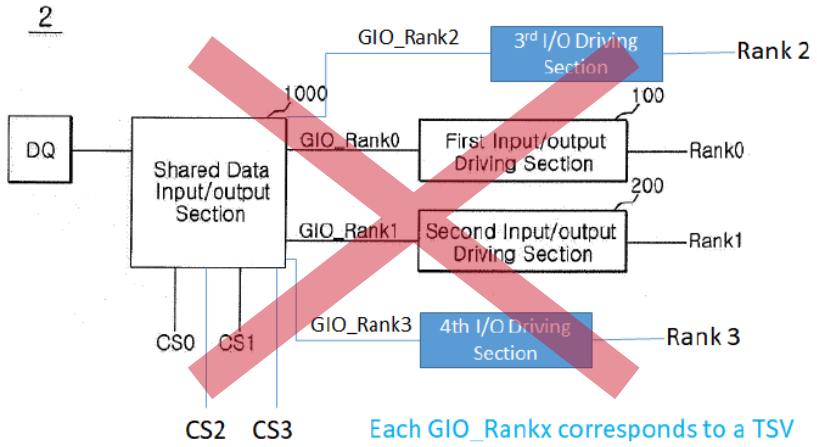
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 28-31
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 28-31

Samsung Electronics Co., Ltd.
Ex. 1067, p. 48

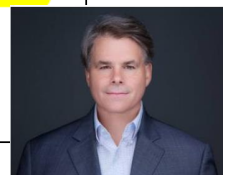
Petition does NOT depend on separate TSVs for each rank (Netlist's Strawman #3, requiring "*group of at least two array dies*")



EX2023, p.68

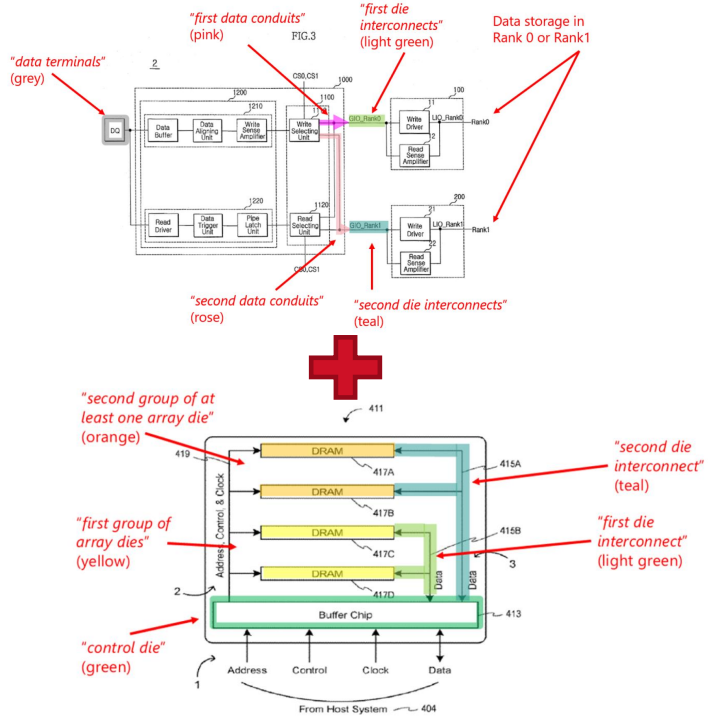
Q. And, to be clear, the figure in the middle of page 68 in your declaration marked as Exhibit 2023 was created by you, not by Dr. Wolfe or by Samsung, correct?

A. That's correct.



EX1052 (Brogioli) at 318:17-:21

Kim + Rajan



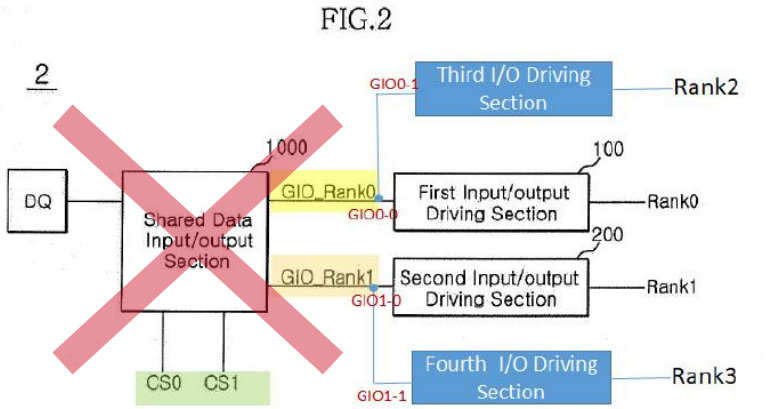
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

'060: Paper 24 (Reply) at 11; Paper 01 (Pet.) at 28; Paper 20 (POR) at 30-31
'160: Paper 24 (Reply) at 12; Paper 01 (Pet.) at 30; Paper 20 (POR) at 31-32

Samsung Electronics Co., Ltd.
Ex. 1067, p. 49

Petition did NOT propose a combination with Kim's circuit operating *the same way* as in Kim's original 2-rank figure (Netlist's Strawman #4)



EX2023, p.70

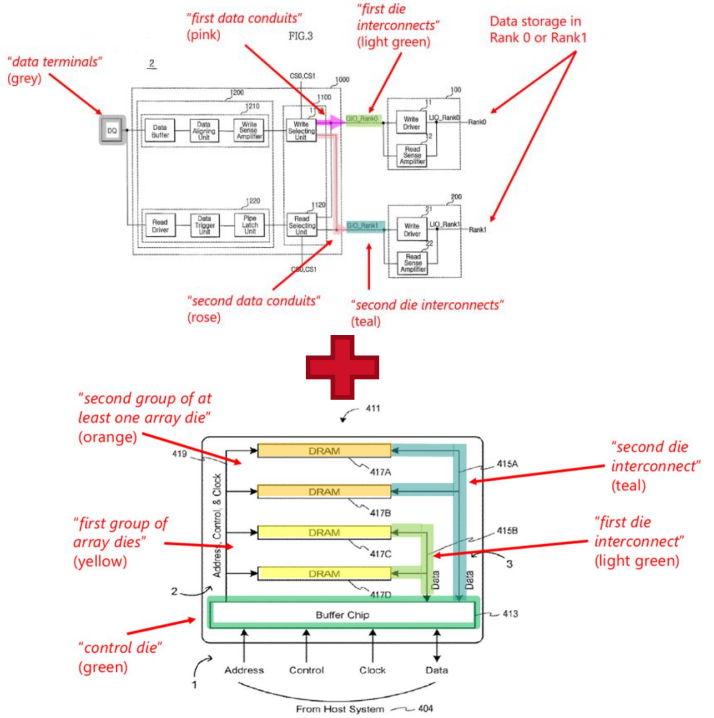
Q. In your four-rank version of Figure 2 of Kim shown at the top of page 70 of your expert declaration marked as Exhibit 2023, you assume that Kim's circuits would operate the same way as in Kim's original Figure 2, correct?

A. That is correct, as I recall figure -- the -- the earlier figures of Kim.



EX1052 (Brogioli) at 320:5-:11

Kim + Rajan



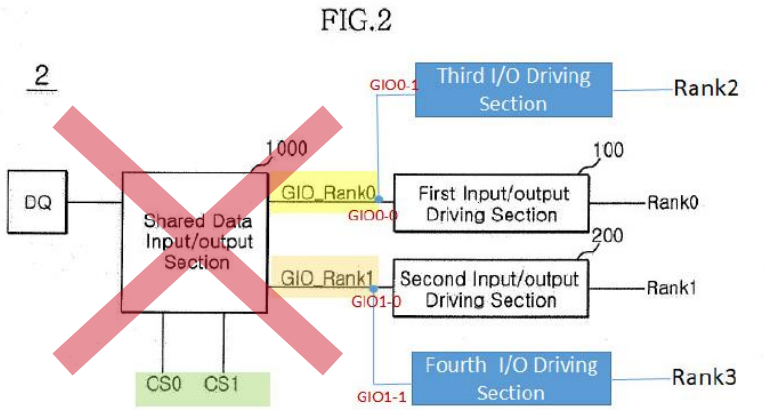
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

EX2025 (Wolfe) at 46:3-:12, 55:18-57:9, 79:13-80:11, 86:12-:17, 201:3-202:5, 204:2-205:8
'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 32-38

Samsung Electronics Co., Ltd.
Ex. 1067, p. 50

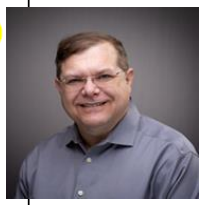
Petition did NOT propose a combination with Kim's circuit operating *the same way* as in Kim's original 2-rank figure (Netlist's Strawman #4)



EX2023, p.70

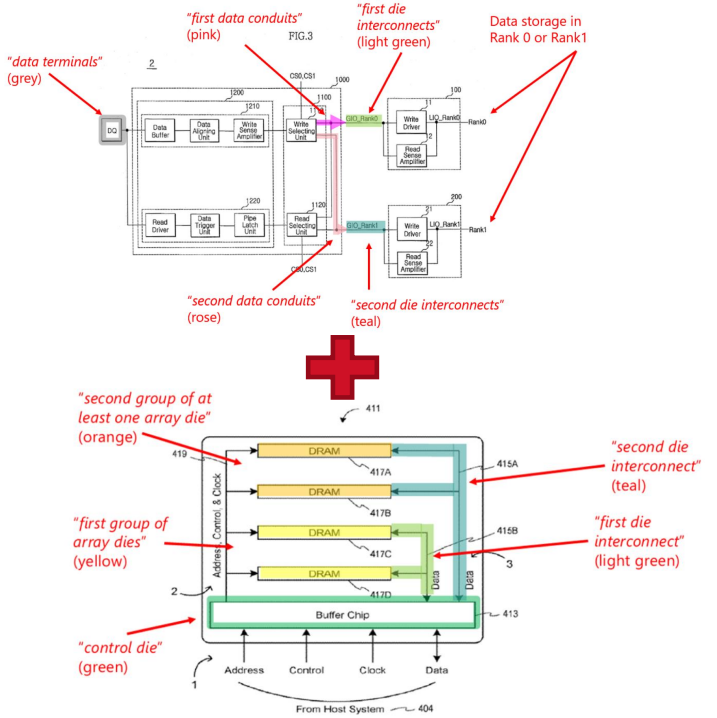
Q. So like the Rank0 is also going to be added to the GIO_Rank0 line, basically just a duplicate --

A. One option would be to add -- to connect Rank2 to the GIO_Rank0 line and to connect Rank3 to the GIO_Rank1 line, and create the appropriate control signals so that only one rank would drive each of those I/O lines at a time or only one rank would respond to write operations on them. There are lots of different ways to make rank multiplication work.



EX2025 (Wolfe) at 46:3-:12

Kim + Rajan



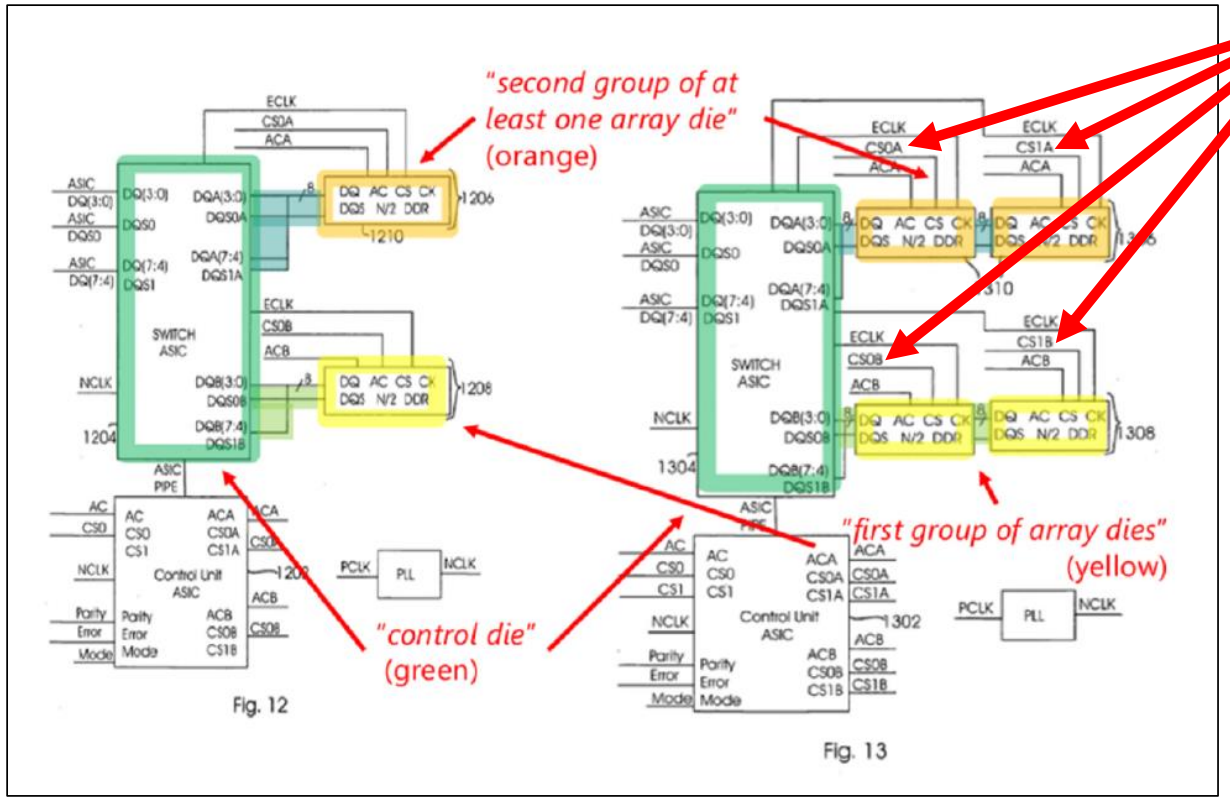
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

EX2025 (Wolfe) at 46:3-:12, 55:18-57:9, 79:13-80:11, 86:12-:17, 201:3-202:5, 204:2-205:8
'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 32-38

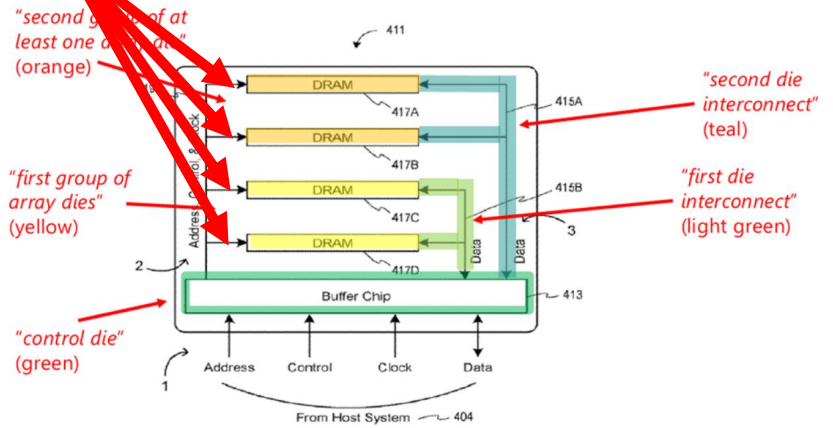
Samsung Electronics Co., Ltd.
Ex. 1067, p. 51

Rajan's separate chip selects and shared data buses (on the right) were well known for rank multiplication (without data collisions) as shown by Ellsberry (on the left)



EX1026 (Ellsberry) at Figs. 12-13

Four separate chip selects (CS0A, CS1A, CS0B, CS1B), one for each rank (four ranks total)



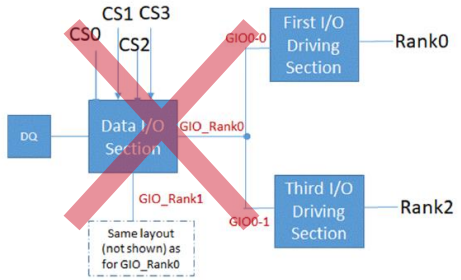
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

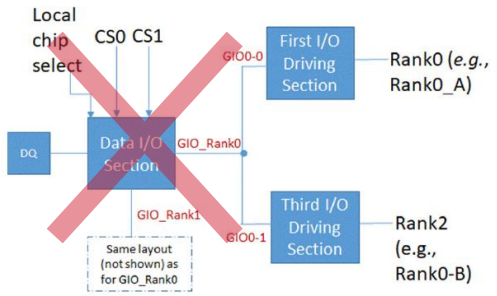
'060: Paper 1 (Pet.) at 27, 29-30; Paper 24 (Reply) at 8-9
'160: Paper 1 (Pet.) at 29, 21-32; Paper 24 (Reply) at 9-10

Samsung Electronics Co., Ltd.
Ex. 1067, p. 52

Netlist's sur-reply raises new arguments like Strawman #4



GIO_rank0 with CS0 and CS2
GIO_rank1 with CS1 and CS3

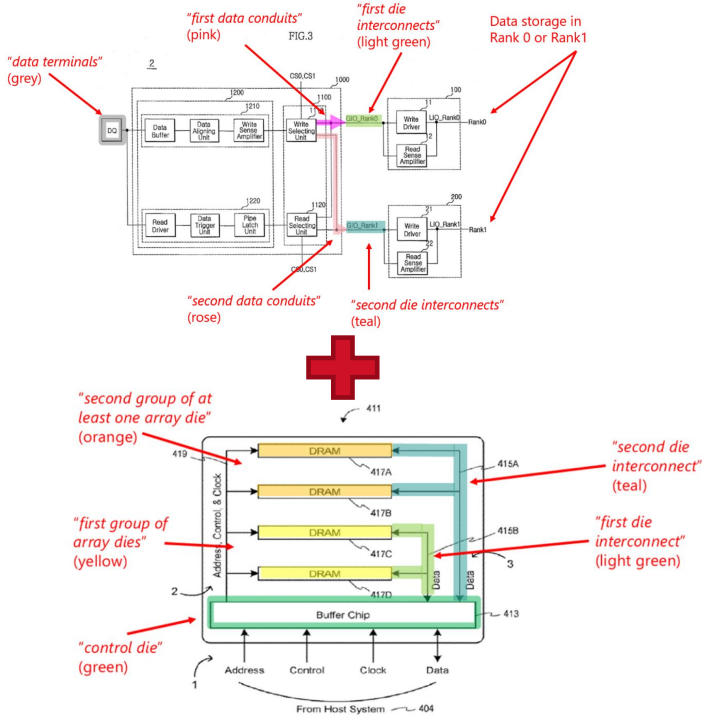


GIO_rank0 with CS0, local chip-select selects between GIO0-1 and GIO0-0
GIO_rank1 with CS1, local chip-select selects between GIO1-1 and GIO1-0

(rank multiplication)

'060: Paper 28 (Sur-reply) at 12
'160: Paper 28 (Sur-reply) at 13

Kim + Rajan



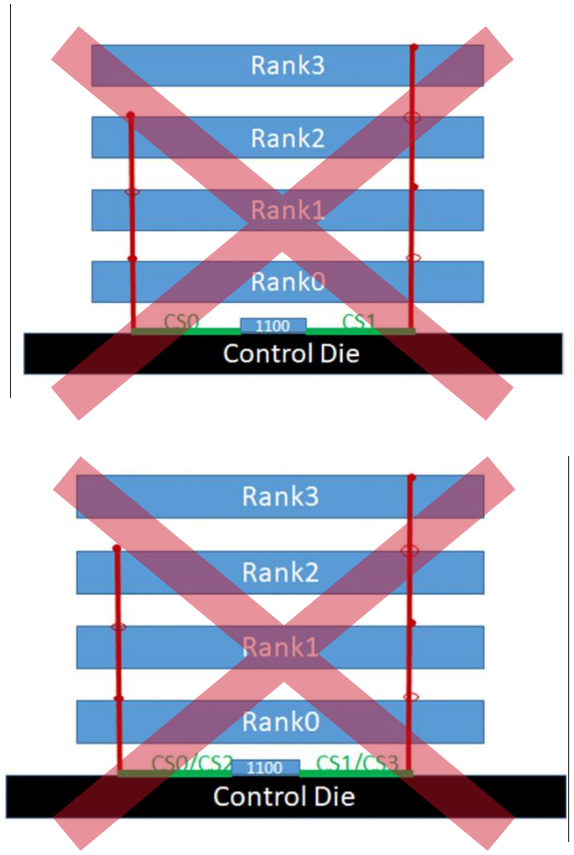
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

EX2025 (Wolfe) at 46:3-:12, 55:18-57:9, 79:13-80:11, 86:12-:17, 201:3-202:5, 204:2-205:8
'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 32-38

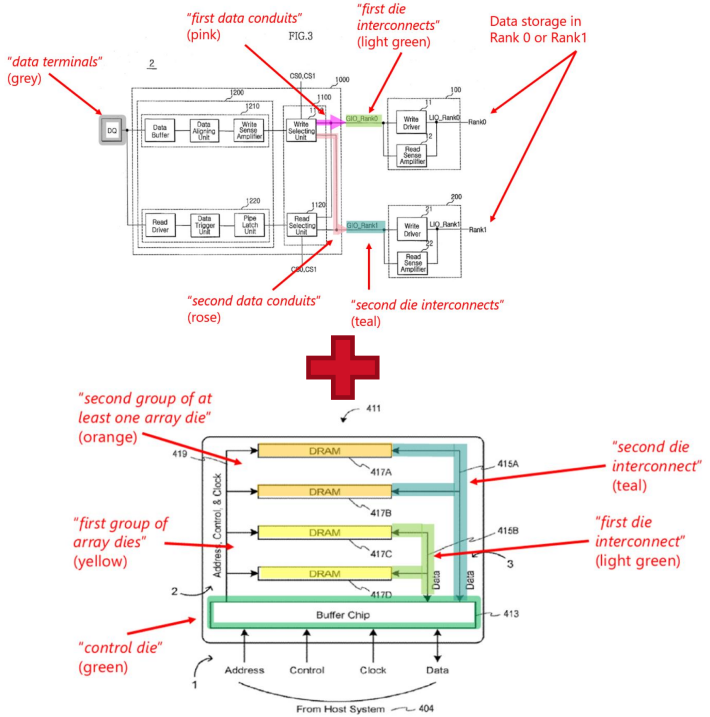
Samsung Electronics Co., Ltd.
Ex. 1067, p. 53

Netlist's sur-reply raises new arguments like Strawman #4



'060: Paper 28 (Sur-reply) at 13
'160: Paper 28 (Sur-reply) at 14

Kim + Rajan



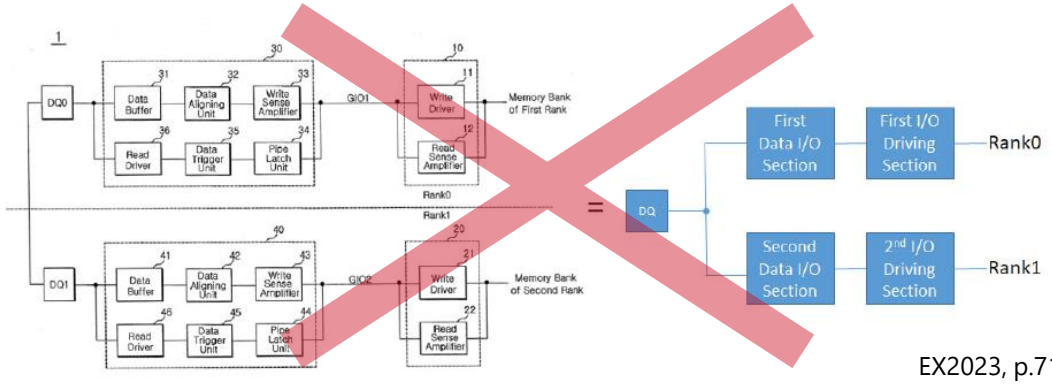
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

EX2025 (Wolfe) at 46:3-:12, 55:18-57:9, 79:13-80:11, 86:12-:17, 201:3-202:5, 204:2-205:8
'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 32-38

Samsung Electronics Co., Ltd.
Ex. 1067, p. 54

Petition did NOT equate Kim's prior-art Fig. 1 with the proposed combination (Netlist's Strawman #5)



EX2023, p.71

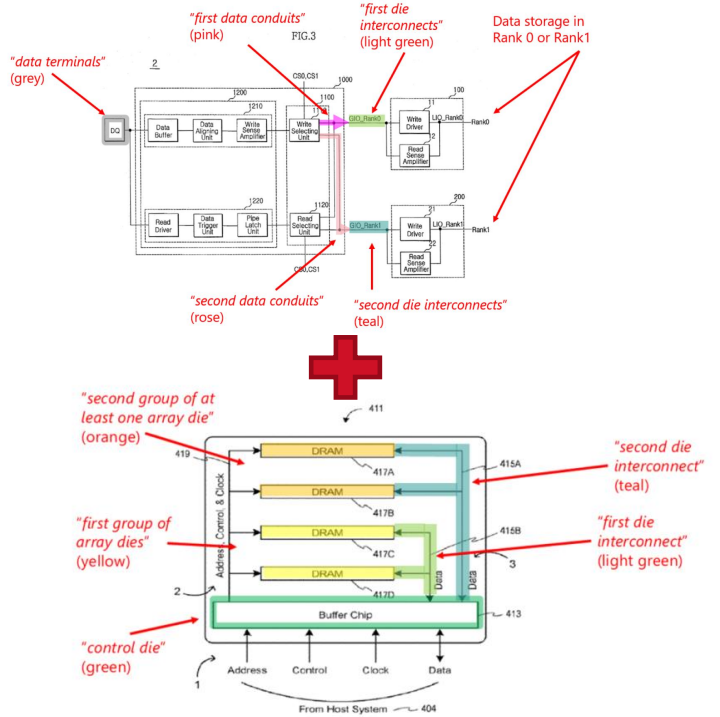
Q. So, to be clear, the figure shown towards the top of page 71 of your expert declaration marked as Exhibit 2023 is something that you created, not something that Dr. Wolfe or Samsung created, correct?

A. The figure itself, yes, that's correct.



EX1052 (Brogioli) at 323:21-324:1

Kim + Rajan



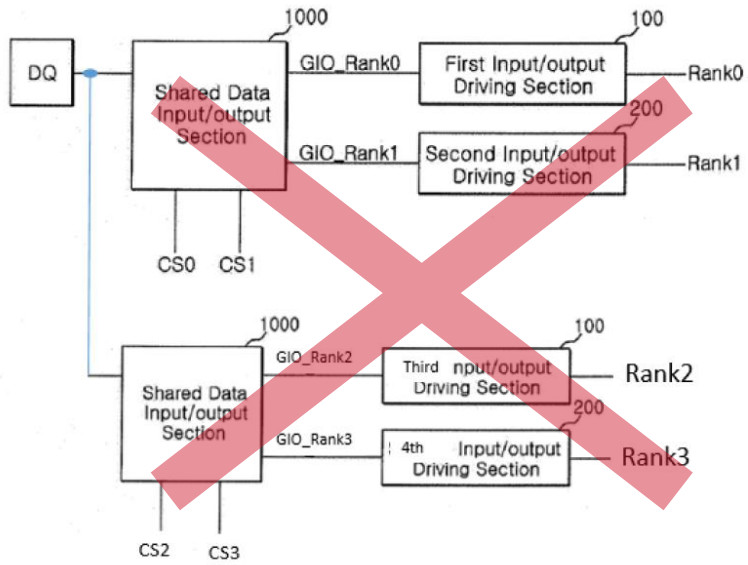
the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

'060: Paper 24 (Reply) at 11-12; Paper 1 (Pet.) at 23-34; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12-13; Paper 1 (Pet.) at 25-36; Paper 20 (POR) at 32-38

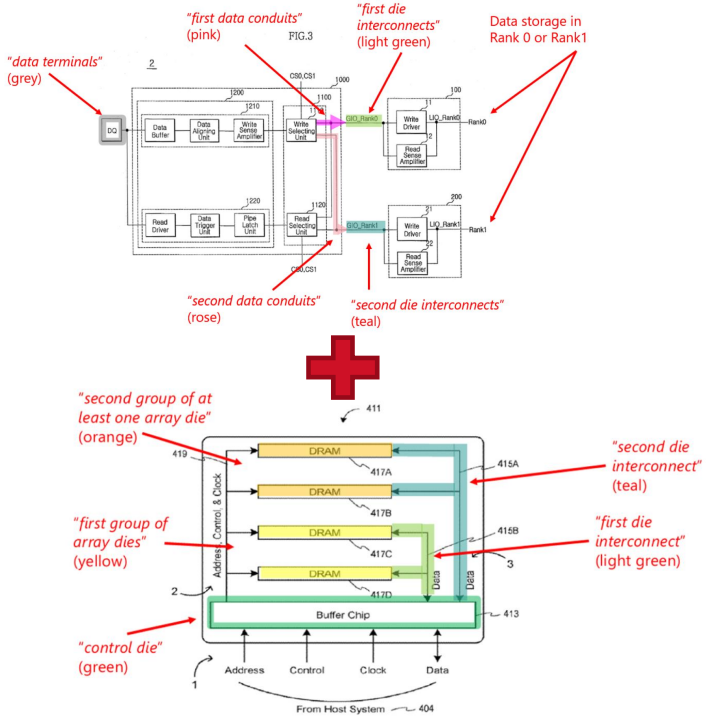
Samsung Electronics Co., Ltd.
Ex. 1067, p. 55

Netlist's sur-reply raises yet another strawman (Strawman #6)



'060: Paper 28 (Sur-reply) at 16
'160: Paper 28 (Sur-reply) at 17

Kim + Rajan



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

EX2025 (Wolfe) at 46:3-:12, 55:18-57:9, 79:13-80:11, 86:12-:17, 201:3-202:5, 204:2-205:8
'060: Paper 24 (Reply) at 11; Paper 20 (POR) at 32-38
'160: Paper 24 (Reply) at 12; Paper 20 (POR) at 32-38

"DRIVER SIZE" CLAIM CONSTRUCTION

USING DRIVERS OF DIFFERENT "SIZES" FOR TSV1 AND TSV2 WAS OBVIOUS

GROUND 1 ('160), [1.E.4]-[1.E.5]

GROUND 3 ('060), [15.A]-[15.B]

(KIM + RAJAN + WYMAN)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

’060/’160 Claims: “driver size”

’060 Patent, Claim 15:

15. The memory package of claim **11**, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

’160 Patent, Claim 1:

the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.

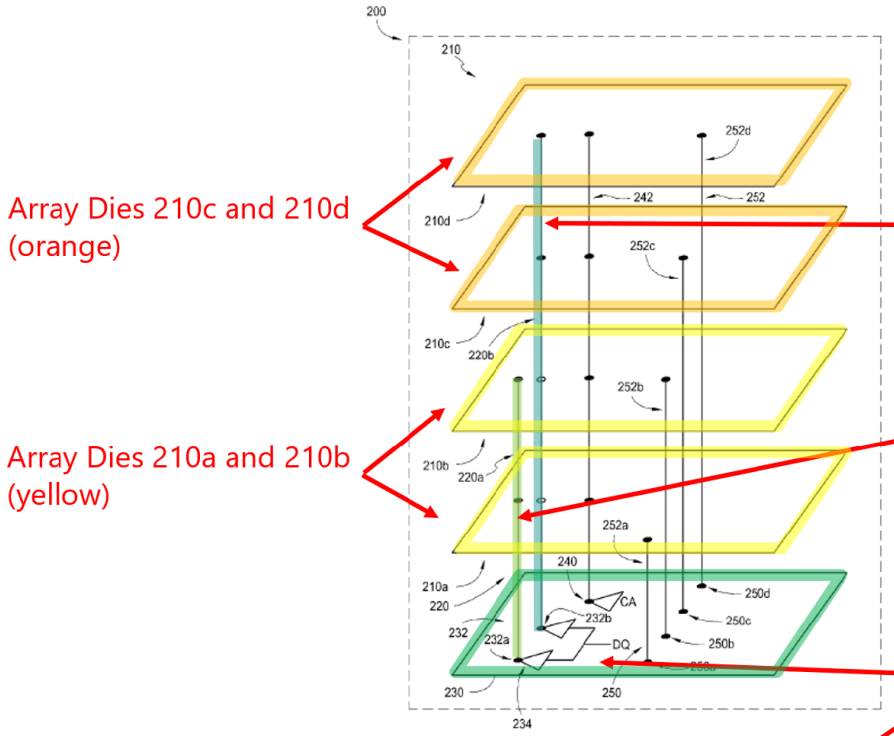


FIG. 2

interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more

’060: EX1001 at 17:43-:45
’160: EX1001 at 17:32-:35

’060: Paper 1 (Pet.) at 11-14; EX1003 ¶¶ 61-65
’160: Paper 1 (Pet.) at 11-16; EX1003 ¶¶ 61-65

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Ex. 1067, p. 58

District Court's construction of "driver size" recognizes the correlation identified in the Petition between "driver strength" and "transistor size and/or number of transistors"

Collectively, the parties point to the following excerpts from the patents:

- "The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver." '160 Patent at 17:31–33.

PTAB and another before a district court. Regardless, even in the Petition, Micron distinguishes between driver size and driver strength. *See* Petition, Dkt. No. 97-12 at 48–49 (citing to EX1030 as "disclosing different-sized transistors to achieve different driver strengths"). Because the weight of the evidence supports Micron's position, the Court construes "driver size" as "driver physical size."

EX1066 at 12-13 (quoting '160 Pet. at 52 (citing EX1030, p.135 ("Buffers can be created with different amounts of *drive capability*, depending on the sizes of the transistors....")))

'060: Paper 32 (Mandatory Notices) at 3; Paper 24 (Reply) at 19-20
'160: Paper 32 (Mandatory Notices) at 3; Paper 24 (Reply) at 16

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Ex. 1067, p. 59

Number of transistors in Wyman (on the right) corresponds to "driver size" in the '060/'160 Patents

The process **500** further comprises selecting a driver size for a first driver at block **508** and selecting a driver size for a second driver at block **510**. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package.

'060: EX1001 at 17:36-:48
'160: EX1001 at 17:24-:36

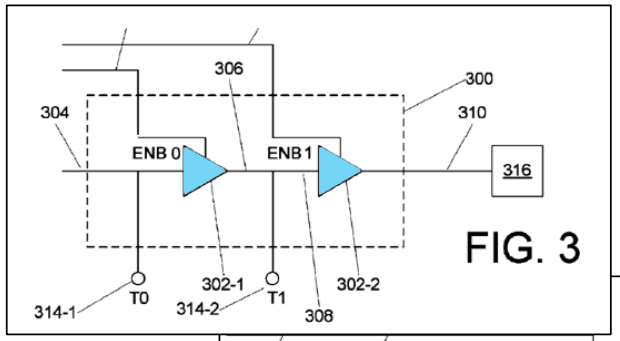


FIG. 3

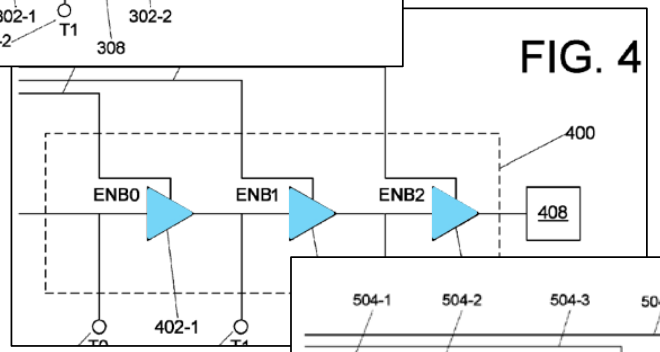


FIG. 4

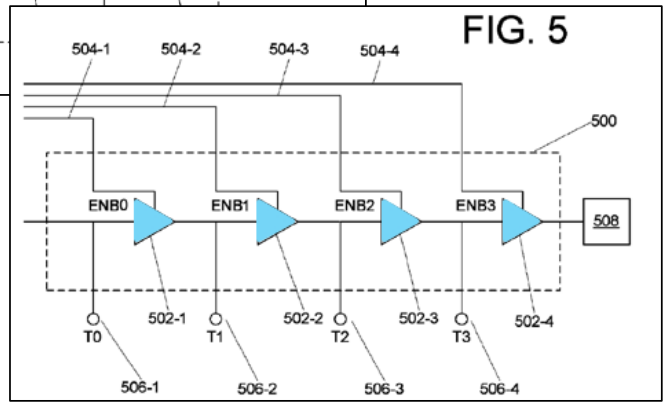


FIG. 5

EX1017 (Wyman) at Figs. 3-5

'060: Paper 24 (Reply) at 18-20
'160: Paper 24 (Reply) at 14-16

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Ex. 1067, p. 60

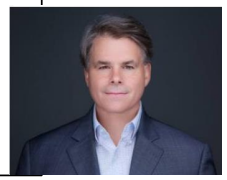
Number of transistors in Wyman (on the right) corresponds to "driver size" in the '060/'160 Patents

Q. So in the situation where only driver 502-1 is enabled, the signal is driven only by driver 502-1 to tap T1, which is also labeled "506-2"; is that correct?

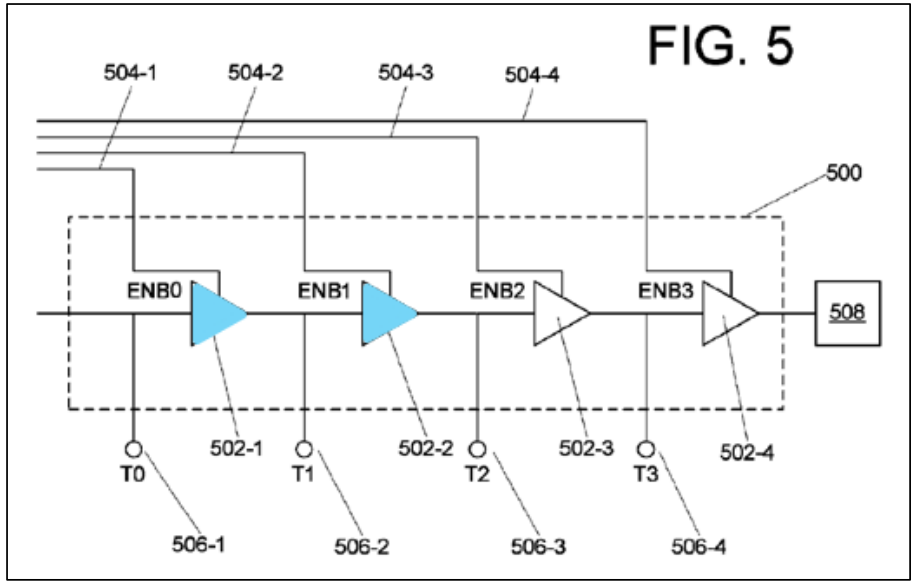
A. That appears to be at least what Figure 5 is illustrating.

Q. And if Figure 5 of Wyman marked as Exhibit 1017, if only drivers 502-1 and 502-2 are enabled, the input signal is driven by both driver 502-1 to tap T1 marked as "506-2," and driver 502-2 will drive to tap T2 marked as "506-3," correct?

A. I think that sounds right, in -- Wyman talked about different configurations or -- different configurations of the different drivers to divide up the driver level.



EX1052 (Brogioli) at 328:10-:24



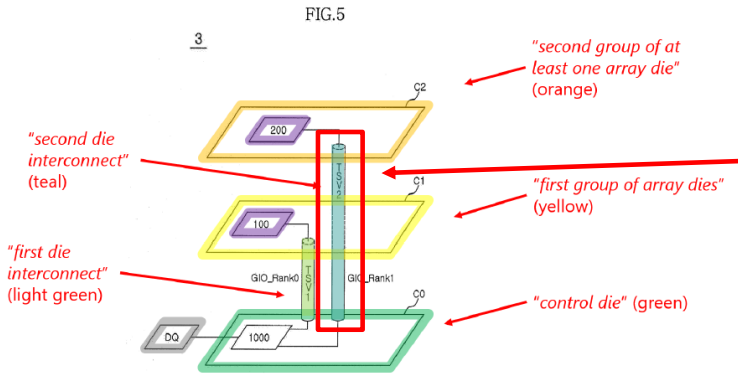
EX1017 (Wyman) at Fig. 5

'060: Paper 24 (Reply) at 18-20
'160: Paper 24 (Reply) at 14-16

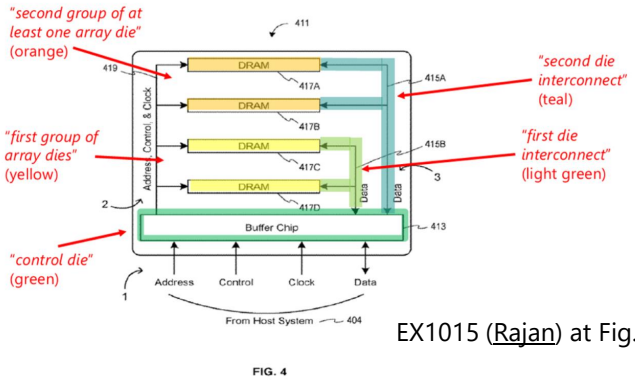
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Ex. 1067, p. 61

Using Wyman's drivers of different sizes for Kim's TSVs of different lengths was obvious

Kim + Rajan



EX1014 (Kim) at Fig. 5



EX1015 (Rajan) at Fig. 4

Wyman: additional drive for longer die interconnects

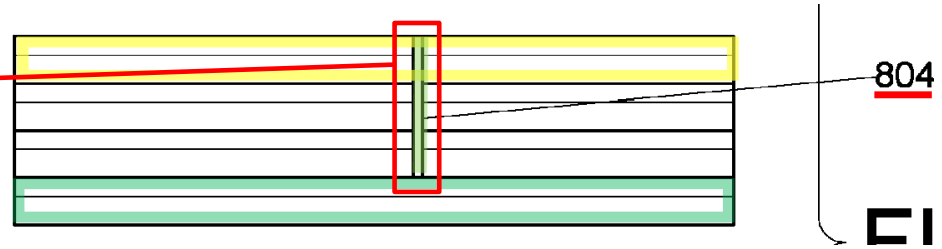


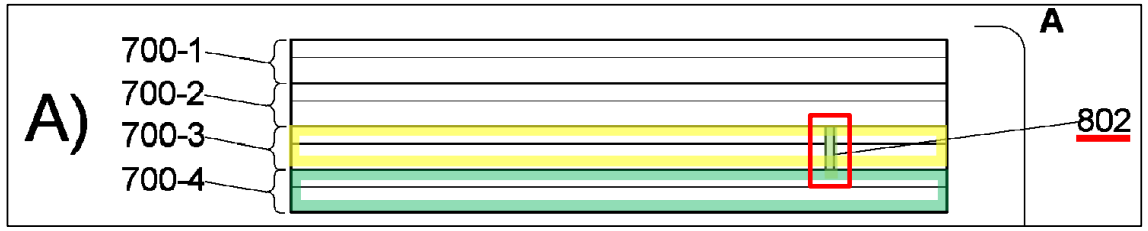
FIG. **8B** illustrates, in simplified form, a longer through-chip via connection (**804**) extending directly between the mother chip (**700-4**) and daughter **3** (**700-1**) in a straight line. The increased resistance, capacitance and impedance of such a connection (**804**) might require additional drive than that referred to in connection with FIG. **8A**. In other words, the

EX1017 (Wyman) at 6:21-:26 & Fig. 8B

'060: Paper 24 (Reply) at 18-20
'160: Paper 24 (Reply) at 14-16

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Ex. 1067, p. 62

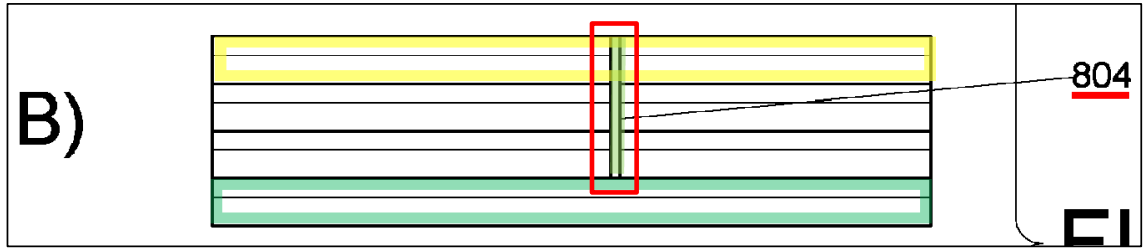
Wyman, like the ’060/’160 Patents, teaches that the difference in load for TSVs of different lengths is NOT negligible



EX1017 (Wyman) at Fig. 8A

FIG. **8**A illustrates, in simplified form, a through-chip via connection (**802**) extending between the mother chip (**700-4**) and daughter **1** (**700-3**). Presuming that this connection would require minimal drive, if a driver portion **500** of FIG. **5** was

EX1017 (Wyman) at 6:15-:18



EX1017 (Wyman) at Fig. 8B

FIG. **8**B illustrates, in simplified form, a longer through-chip via connection (**804**) extending directly between the mother chip (**700-4**) and daughter **3** (**700-1**) in a straight line. The increased resistance, capacitance and impedance of such a connection (**804**) might require additional drive than that referred to in connection with FIG. **8**A. In other words, the

EX1017 (Wyman) at 6:21-:26

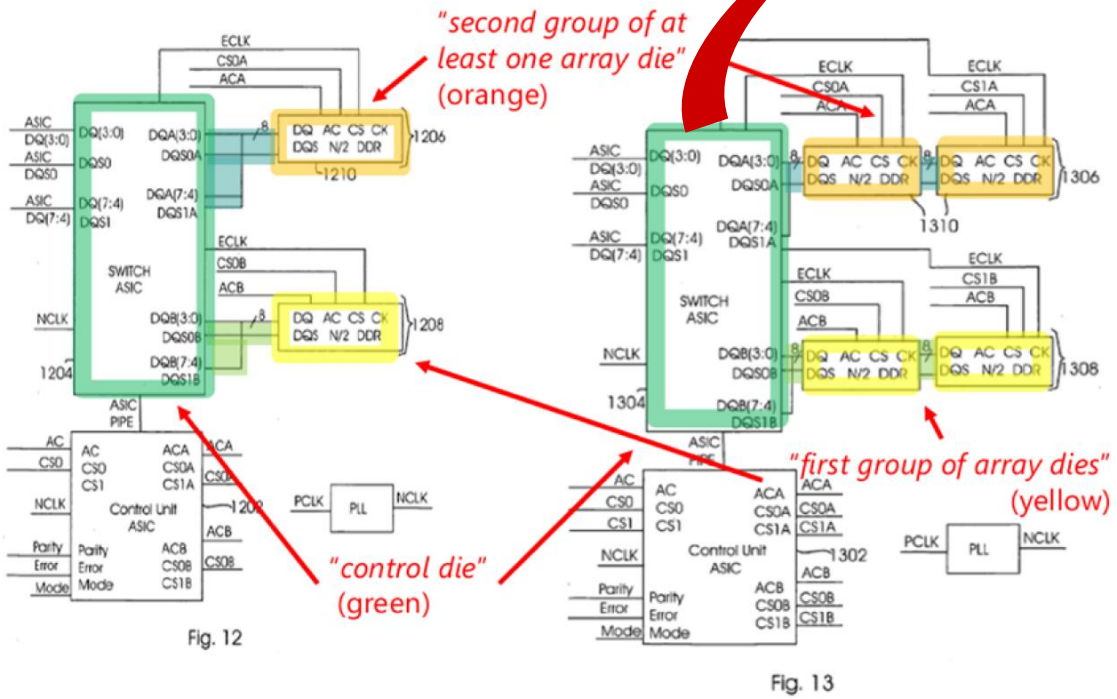
’060: EX1001 at 4:42-:45
’160: EX1001 at 4:45-:48

considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become

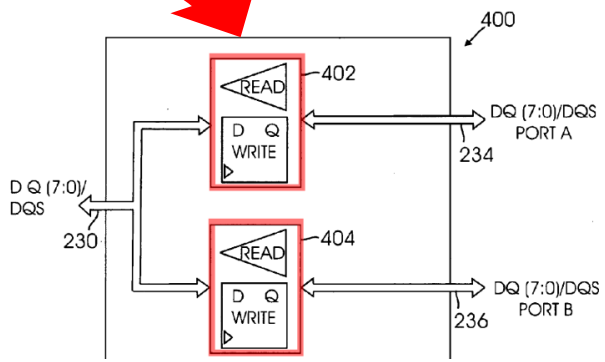
’060: Paper 24 (Reply) at 18-20; Paper 1 (Pet.) at 20-21
’160: Paper 24 (Reply) at 14-16; Paper 1 (Pet.) at 22-23

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Ex. 1067, p. 63

It was obvious to use a separate driver for each TSV (e.g., for rank multiplication)



EX1026 (Ellsberry) at Figs. 12-13

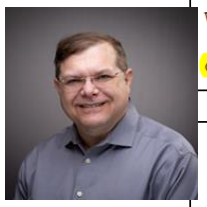


EX1026 (Ellsberry) at Fig. 4

"[I]t's not necessary to show that a combination is the *best* option, only that it be a ***suitable*** option."

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023)

It was obvious to use a separate driver for each TSV

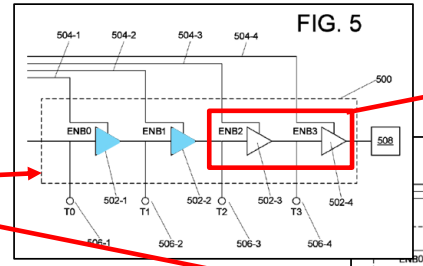


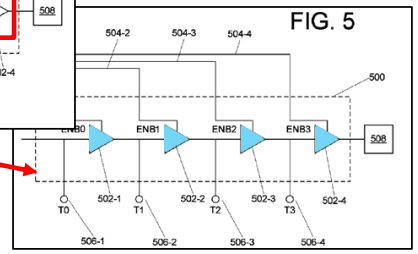
A. Again, understanding that there are many variations disclosed of circuit 500, the particular examples indicate that you can use the taps independently, or you can provide a separate copy of circuit 500 for each thing that needs to be driven after you analyze the current requirements.

And there are a number of examples given where you can use just a portion of the total current and you can disable other portions of 500,

THE WITNESS: That is correct for a particular wire. But there is a clear teaching that you can make a determination for one wire that you might require two taps, like Figure 3, and for another wire, you might require a three-buffer system like Figure 4, and for another wire, you might require a system like Figure 5, and even within each of those, you can make them in different sizes.

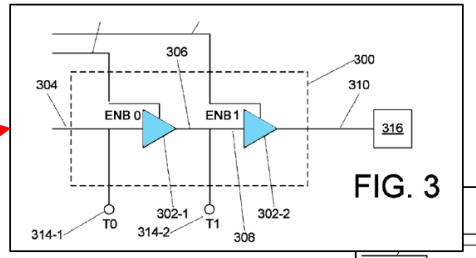
EX2025 (Wolfe) at 129:2-:10, 131:11-:19

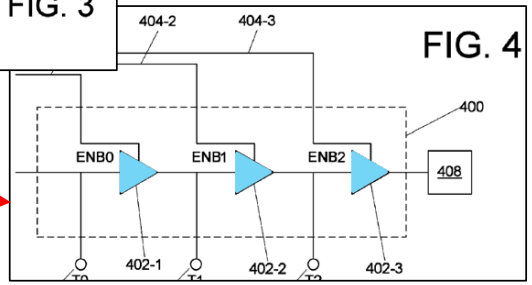




At this point it is also useful to mention that the "taps" need not be specifically supplied as part of a design. For example, the above approach could be used with a conventional drive circuit made up of multiple stages by using a via approach, such as described in the above incorporated U.S. patent applications, to form a low parasitic, electrically conductive connection to an intermediate point between stages where the current drive is adequate, as needed, and to disable any remaining downstream stage(s) by using a via to break one or more connections and leaving the via unfilled or filling the via with an insulator.

EX1017 (Wyman) at Figs. 3-5, 5:34-:44





'060: Paper 24 (Reply) at 18-20
'160: Paper 24 (Reply) at 14-16

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Ex. 1067, p. 65

"ARRAY DIES" CLAIM CONSTRUCTION

NON-DRAM "ARRAY DIES" WERE OBVIOUS

GROUND 1 ('160)
GROUNDS 1-3 ('060)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

The Institution Decision correctly found that the construction of "*array dies*" has no impact on these IPRs

Thus, Patent Owner appears to argue that the district court's construction is that the claimed array dies are different from Rajan137's DRAM circuits 206A–D, not all DRAM circuits.

For the reasons explained below in section II.E.3.a, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction and also under that construction as interpreted by Patent Owner. Because the constructions advocated by Patent Owner do not impact the decision whether to institute, we need not resolve this claim construction issue at this time. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

'060: Paper 13 (ID) at 11;
see also '160: Paper 13 (ID) at 11

a) Element 1.c ("array dies")

As to element 1.c regarding the recited "array dies," Patent Owner argues that Petitioner has not shown that Kim's or Rajan's memory dies are different from Rajan137's DRAM circuits, which Patent Owner asserts are excluded from the scope of the claim. Prelim. Resp. 20–22, 25–30. On this record, we disagree. As Petitioner correctly points out, Kim does not even mention DRAM and thus is not limited to DRAM. *See* Reply 3. Furthermore, as Petitioner points out (Reply 2–3), Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Ex. 1015, 15:3–9. Patent Owner argues that Rajan137

'060: Paper 13 (ID) at 23;
see also '160: Paper 13 (ID) at 24

'060: Paper 24 (Reply) at 1, 13-15
'160: Paper 24 (Reply) at 1, 16-18

Samsung Electronics Co., Ltd.
Ex. 1067, p. 67

"array dies": No construction necessary because the claims are obvious under either interpretation

Specification

receive data signals from the control die **822**. As with the array dies **210** and **310**, the array dies **824** may include any type of Random Access Memory (RAM) die. For example, the array dies **824** may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory

'060: EX1001 at 21:67-22:4
'160: EX1001 at 21:52-:56

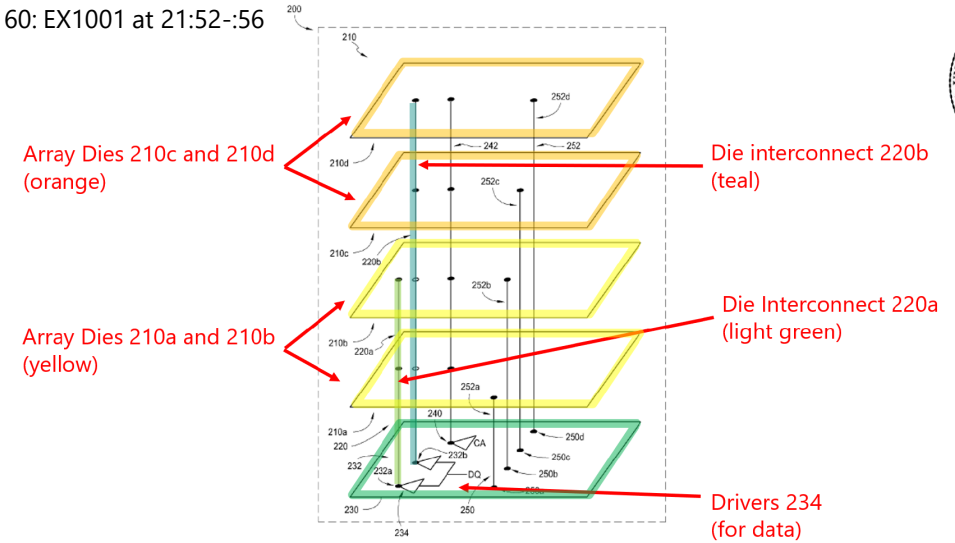


FIG. 2

Prosecution History

First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting

EX1002, 465

District Court's Claim Construction

Netlist *structurally* distinguished "stacked DRAM circuits" from "stacked array dies" to obtain the patent. Based on that distinction, the Court construes "array die" as "array die that is different from a DRAM circuit."

EX2004 at 32

'060: Paper 1 (Pet.) at 15; EX1003, ¶73; Paper 20 (POR) at 16
'160: Paper 1 (Pet.) at 17; EX1003, ¶73; Paper 20 (POR) at 16

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Ex. 1067, p. 68

District Court's final judgment (based on jury verdict): "DRAM dies" are "*array dies*" (but post-trial motion to overturn the verdict [ECF 566] is pending before Judge Gilstrap)

Final Judgment:

Q. And the jury in the Eastern District of Texas agreed with you that Samsung's accused HBM products infringed the '060 and '160 patents; correct?

A. That's my understanding, yes.



EX1052 (Brogioli) at 21:17-22:1

119. The Accused HBM Products also each include a plurality of array dies arranged in a stack (*e.g.*, 8 stacked DRAM dies). The plurality of array dies can be divided into at least two

EX1044 at ¶ 119

'060: Paper 1 (Pet.) at 21 Paper 24 (Reply) at 13
'160: Paper 1 (Pet.) at 23; Paper 24 (Reply) at 16-17

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Ex. 1067, p. 69

"*array die*": No construction needed because the claims are obvious under either interpretation

VI. CLAIM CONSTRUCTION

In related litigation, Patent Owner has interpreted some claim terms broadly for purposes of infringement, *see* EX1044, pp.63-68; EX1046, pp.63-69, even though a narrower interpretation may be more reasonable, but Petitioner contends that no express constructions are needed for this proceeding because the claims are obvious under either interpretation. EX1003, ¶112-113.

'060: Paper 1 (Pet.) at 21
'160: Paper 1 (Pet.) at 23

1. "*array die*" (POR 16-18)

The Board correctly concluded there is no need to construe "*array die*" because the claims are obvious under either interpretation. ID 9-11, 16-17. As discussed below (pp.13-15, 33), that is still the correct approach.

'060: Paper 24 (Reply) at 1
'160: Paper 24 (Reply) at 1

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Ex. 1067, p. 70

Kim's "slave chips" are not limited to DRAM dies

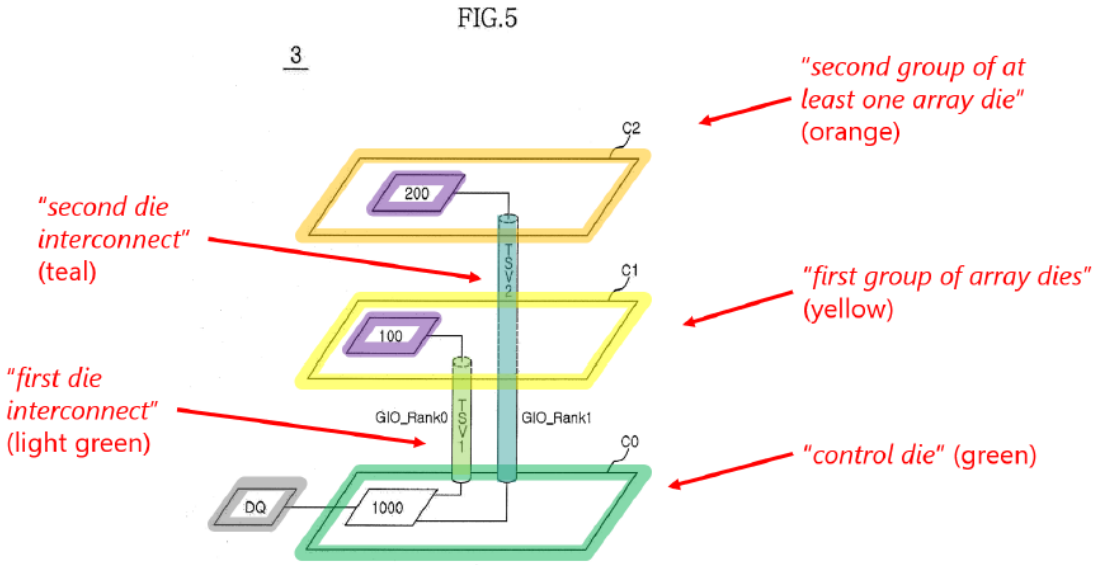


rec[illegible] disagree. As Petitioner correctly points out, Kim does not even mention DRAM and thus is not limited to DRAM. *See* Reply 3.

'060: Paper 13 (ID) at 23;
see also '160: Paper 13 (ID) at 24

[0048] FIG. **5** shows an exemplary embodiment in which one main chip C0 and two slave chips C1 and C2 are stacked. Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used. In the 3D semiconductor apparatus in which the

EX1014 (Kim) at [0048]



EX1014 (Kim) at Fig. 5

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Ex. 1067, p. 71

Rajan is not limited to DRAM dies

Furthermore, as Petitioner points out (Reply 2–3), Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Ex. 1015, 15:3–9. Patent Owner argues that Rajan137

'060: Paper 13 (ID) at 23;
see also '160: Paper 13 (ID) at 24

The physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc.

EX1015 (Rajan) at 15:3-:9; *see also* EX1052 (Brogioli) at 178:25-179:17

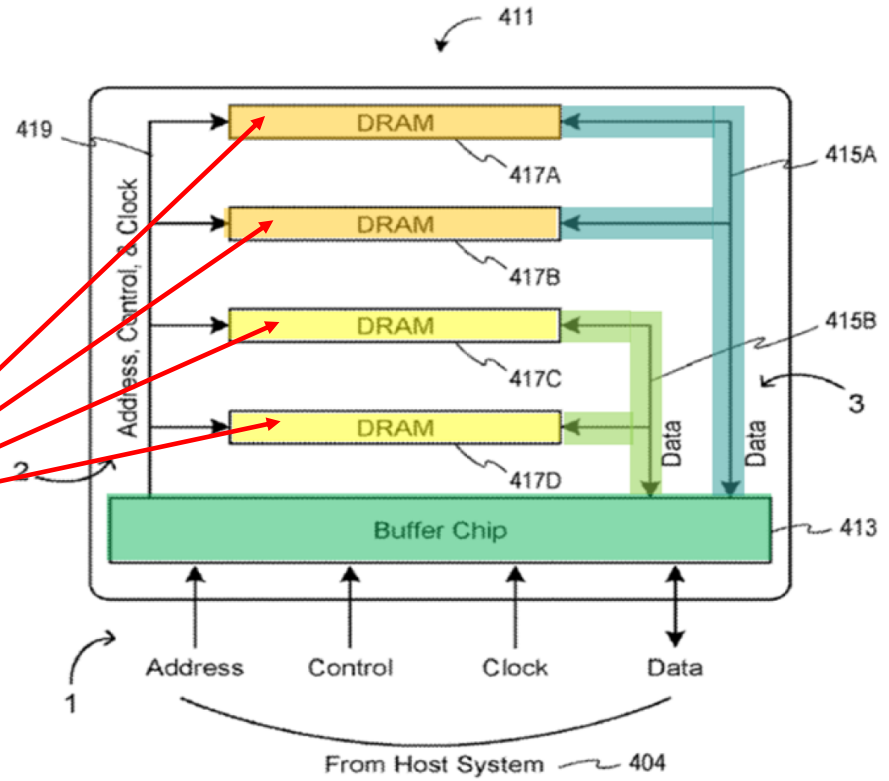


FIG. 4

Rajan discloses a JEDEC (DRAM) interface, even for non-DRAM dies

II.[illegible] similar argument as to Riho, Petitioner's contention is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 93 (emphasis added); *see also* Pet. 94 (asserting that "emulating a standard JEDEC interface was well-known"). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

'060: Paper 13 (ID) at 24;
see also '160: Paper 13 (ID) at 25

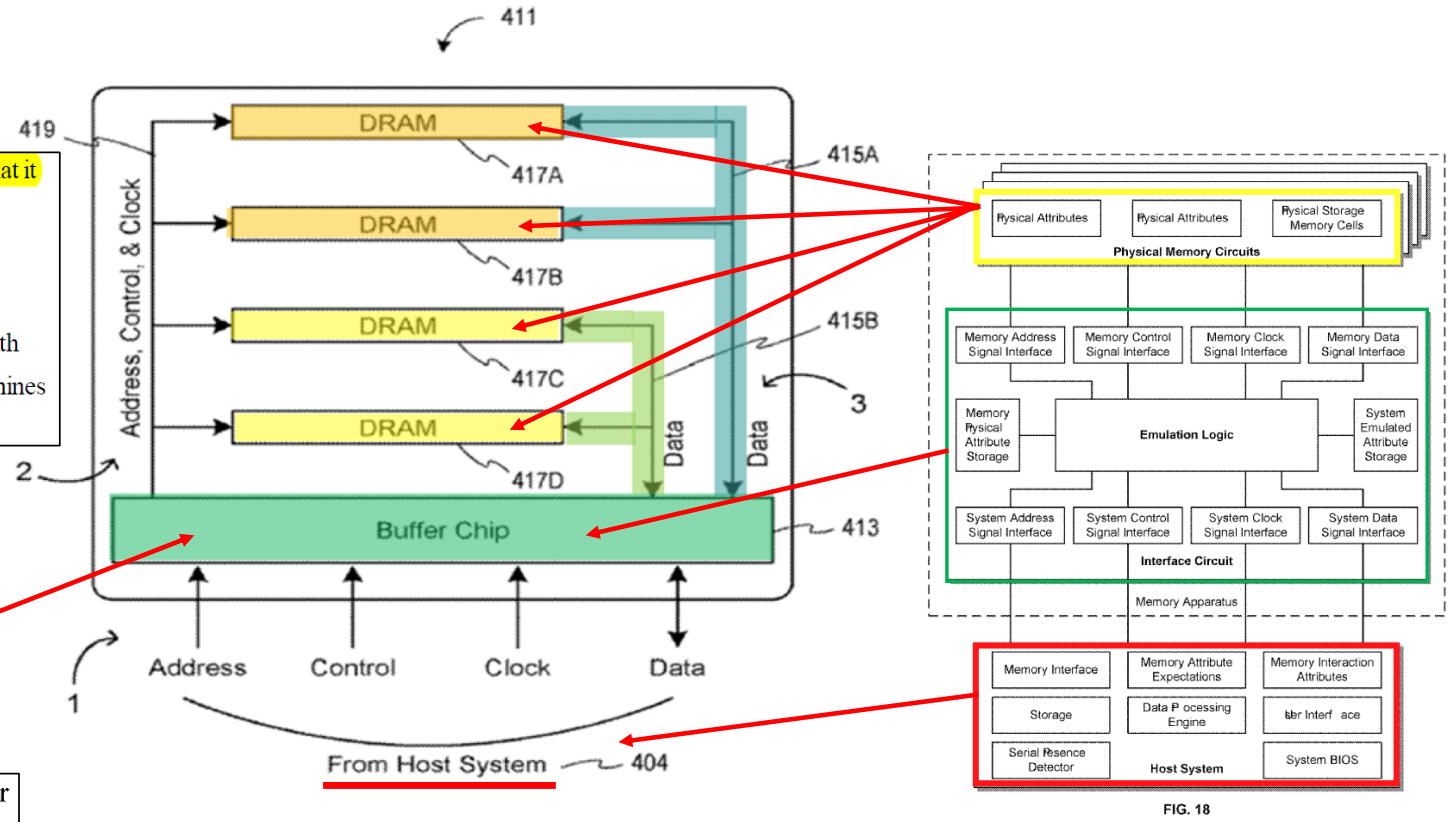


FIG. 4

FIG. 18

The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

EX1015 (Rajan) at 4:20-:24; *see also id.* at 4:48-:50, 14:6-:11, 14:39-:62 & Fig. 18

'060: Paper 24 (Reply) at 13-15
'160: Paper 24 (Reply) at 16-18

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Ex. 1067, p. 73

Using non-DRAM dies (e.g., Flash or SRAM) with a DRAM interface was known

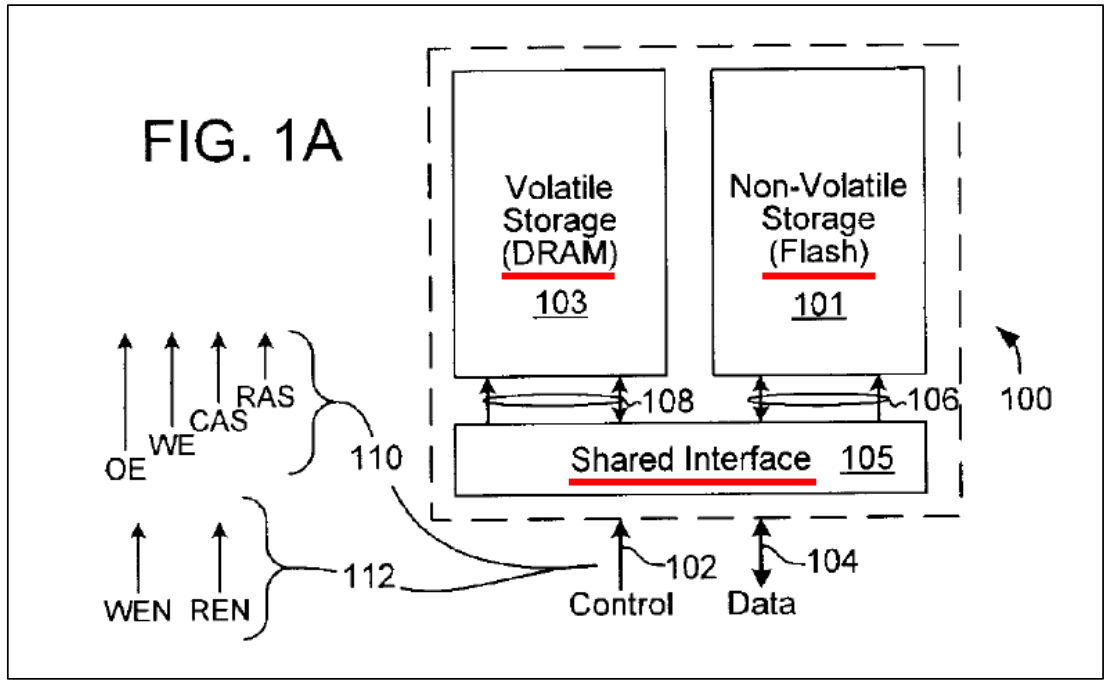
[0015] Internally, the shared interface **105** includes circuitry to forward control and data signals to the appropriate memory die, converting signals from the external data access protocol to an internal data access protocol as necessary. For example, in an embodiment having a DRAM external interface, control and data signals may be forwarded without change to a DRAM die (or with data serialization or deserialization to compensate for differences in path width between the internal and external data and/or control paths), but may be converted from DRAM format to Flash memory format before being forwarded to the Flash memory device. In general, any external protocol may be used to access the hybrid memory device, and any internal protocol or set of protocols may be used to control the volatile and non-volatile storage dice. Further, while only two storage dice are shown, multiple non-volatile storage dice and/or multiple volatile storage dice may be provided and selected by the shared interface circuitry based on incoming address and/or control signals. In such instances, the multiple volatile storage dice may be identical, or may be different in various regards, including storage capacity, storage technology (e.g., one or more SRAM dice may be packaged with one or more DRAM device), and/or the multiple non-volatile storage dice may be identical or mixed as where a Flash memory device is packaged with one or more ROM devices to form a system in package.

(19) **United States**
(12) **Patent Application Publication**
Best
(10) **Pub. No.: US 2010/0110748 A1**
(43) **Pub. Date: May 6, 2010**

(54) **HYBRID VOLATILE AND NON-VOLATILE MEMORY DEVICE**

Related U.S. Application Data

(60) Provisional application No. 60/912,321, filed on Apr. 17, 2007.



EX1060 (Best) at [0015] & Fig.1a; *see also* EX1052 (Brogioli) at 268:4-272:18; EX1061, 22-25 (Final Written Decision against Netlist applying Best)

'060: Paper 24 (Reply) at 13-15
'160: Paper 24 (Reply) at 16-18

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Ex. 1067, p. 74

Using non-DRAM dies (e.g., SRAM) with a different interface was known

Q. As shown at the bottom of page 1 of Exhibit 2053, the purpose of these slides is to teach students how to design a memory controller that can control asynchronous SRAM while making the SRAM look synchronous to the rest of the system, as explained in the middle of the slide; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Just skimming through the slides. So in part, I'm on Slide 8. And it talks about at the first sentence, "The memory controller provides a 'synchronous' wrap around the SRAM."

So it looks like at least one of the things the memory controller is trying to do is provide a synchronous view of the underlying asynchronous SRAM.

EX1052 (Brogioli) at 243:11-244:2



Hardware Design with VHDL Design Example: SRAM ECE 443

External SRAM

A common type of system RAM is asynchronous static RAM (SRAM).

Access is more complicated than internal memory -- here data, address and control signals must be asserted in a specific order and held for a specific time.

A *memory controller* is usually used to shield the synchronous system from SRAM. It is responsible for generating the properly timed signals and making the SRAM look 'synchronous'.

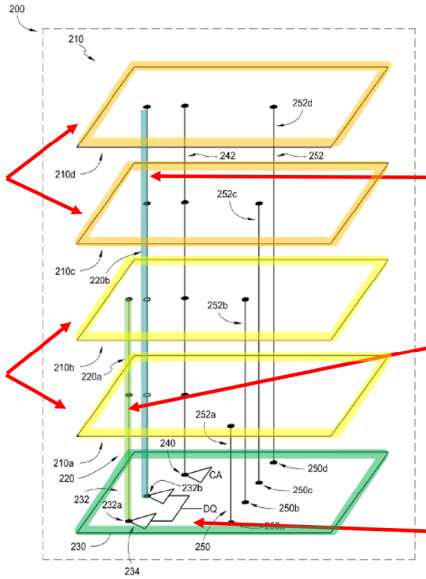
EX2053 (SRAM) at 1

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Ex. 1067, p. 75

'060/'160 Patents admit DRAM package can have non-DRAM "*array dies*"

The memory package **200** can include any type of memory package. For example, the memory package **200** may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few. A memory module (not shown) may include one

'060: EX1001 at 5:1-:5
'160: EX1001 at 5:4-:8



Array Dies 210c and 210d (orange)

Array Dies 210a and 210b (yellow)

Die interconnect 220b (teal)

Die Interconnect 220a (light green)

Drivers 234 (for data)

FIG. 2

receive data signals from the control die **822**. As with the array dies **210** and **310**, the array dies **824** may include any type of Random Access Memory (RAM) die. For example, the array dies **824** may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory

'060: EX1001 at 21:67-22:4
'160: EX1001 at 21:52-:56

Q. As we discussed earlier, the '060 and '160 patents, each of the ***array dies*** can be SDRAM or ***non-volatile memory*** or ***SRAM*** memory, all of which existed before the '160 and the '060 patents, correct?

A. Those types of memory technology, for example, SRAM or DRAM itself, were known prior to these patents; that's correct.

....

Q. So claim 10 of the '160 patent requires, among other things, a ***DRAM package*** compr[i]sing stacked ***array dies***, correct?

A. In compr[i]sing with the stacked ***arrays dies***, at the top of column 25.



EX1052 (Brogioli) at 339:2-:9, 262:23-263:2

'060: Paper 24 (Reply) at 1, 13-15
'160: Paper 24 (Reply) at 1, 16-18

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Ex. 1067, p. 76

"CHIP SELECT SIGNALS" CLAIM CONSTRUCTION

"CHIP SELECT SIGNALS" AND CONDUITS WERE OBVIOUS

GROUND 1 ('160), CLAIMS 15-16
GROUNDS 1-3 ('060), CLAIM 6

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

District Court: "*chip select signal*" for a given memory package has plain and ordinary meaning (which was well-known)

EX2004 at 35

"chip select signal" ('060 Patent, Claims 11–14, 16–19, 20–21, 23–28)	Plain and ordinary meaning.
"chip select conduit" ('060 Patent, Claims 6, 11–14, 16–19)	Plain and ordinary meaning.

JEDEC Standard No. 79-3C
Page 13
EX1019 at 13

Symbol	Type	Function
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.

Memory Systems

Cache, DRAM, Disk

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EX1022 at 319-20

This last bus, the chip-select bus, is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request. A value is asserted on the chip-select bus at the time of a request (e.g., read or write). The chip-select bus contains a separate wire for every rank of DRAM in the system. The chip-select signal passes over a wire unique to each small set of DRAMs and enables or disables the DRAMs in that rank so that they, respectively, either handle the request currently on the bus or ignore the request currently on the bus. Thus, only the DRAMs to which the request is directed handle the request. Even though all DRAMs in the system are connected to the same address and control busses and could, in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening.

'060: Paper 1 (Pet.) at 60-61; Paper 24 (Reply) at 1-2, 15
'160: Paper 1 (Pet.) at 74-75; Paper 24 (Reply) at 1-2, 18-19

JEDEC teaches separate "*chip select signal*" (red) to each stacked die (orange) sharing the data bus (green), thus avoiding collisions

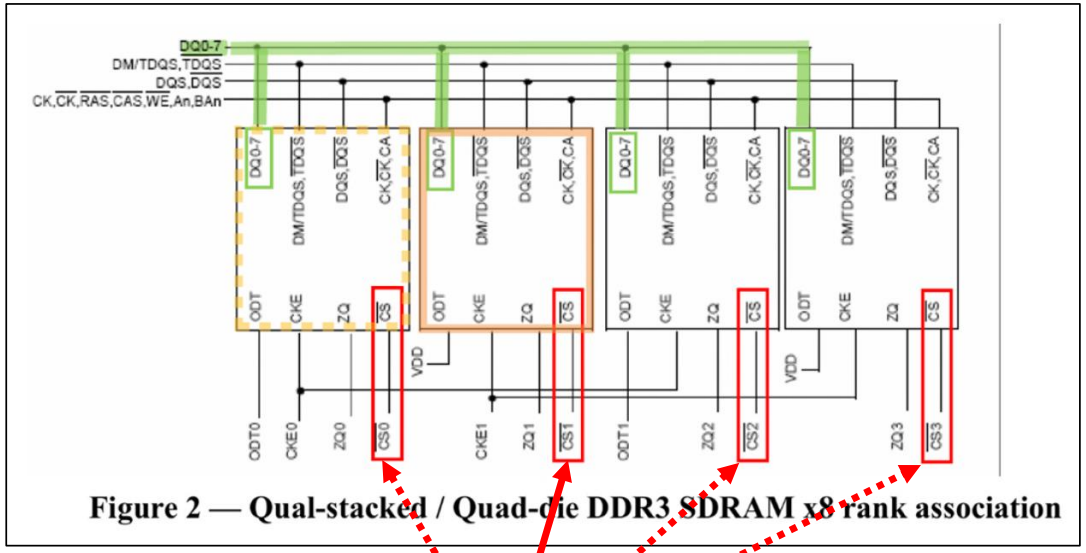


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

EX1019 at 12

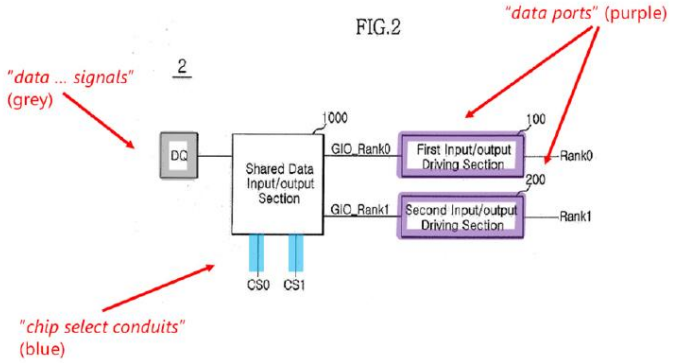
Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

EX1019 at 33

Both Kim and Rajan teach using "*chip select signals*"

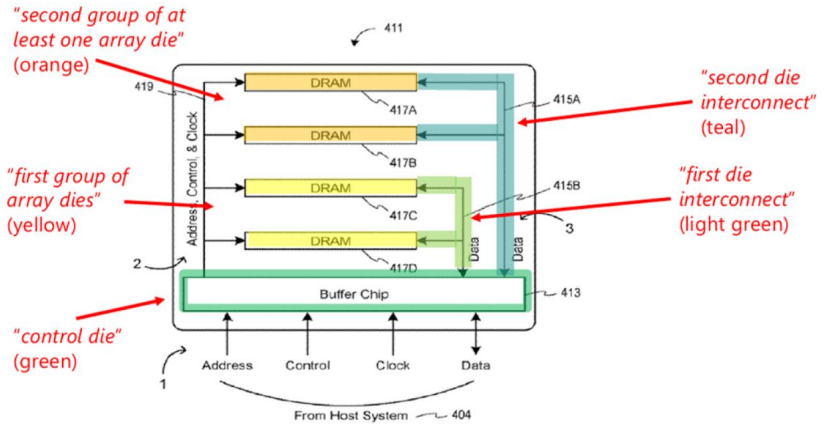
Kim



[0032] The chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus **2** and buffered. In general, if command signals are applied from an

EX1014 (Kim) at [0032] & Fig.2

Rajan



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

EX1015 (Rajan) at 4:20-:24, 6:34-:38 & Fig.4

Rajan teaches rank multiplication with a separate "*chip select signal*" for each die in the stack

Rajan

the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

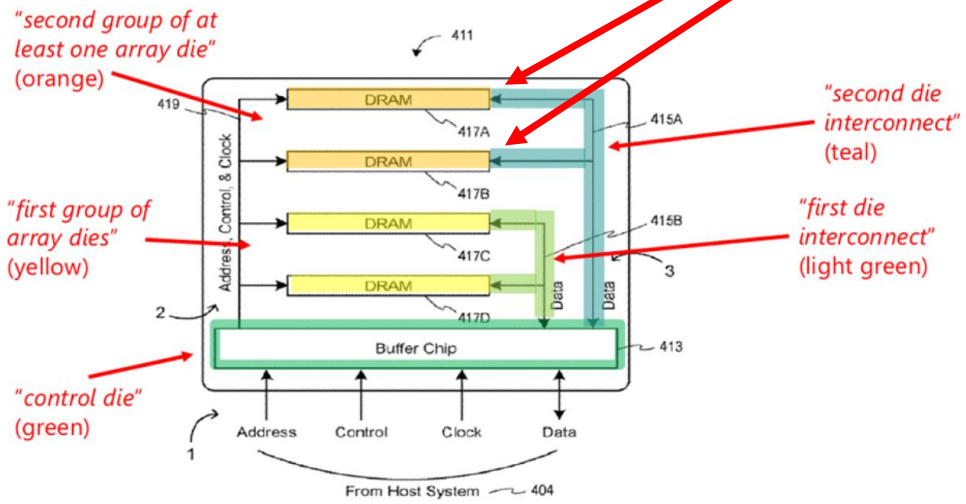


FIG. 4

EX1015 (Rajan) at 4:20-:24, 6:34-:38 & Fig.4

Q. So if 417A and 417B belonged to the same rank and they're connected to the same data wire, there potentially can be collision issues and current issues if they output data at the same time; is that right?

A. That is a big if. You would never let them output data at the same time if you made them in the same rank. You would -- you would put them in different places of the address space so only one or the other was operable.

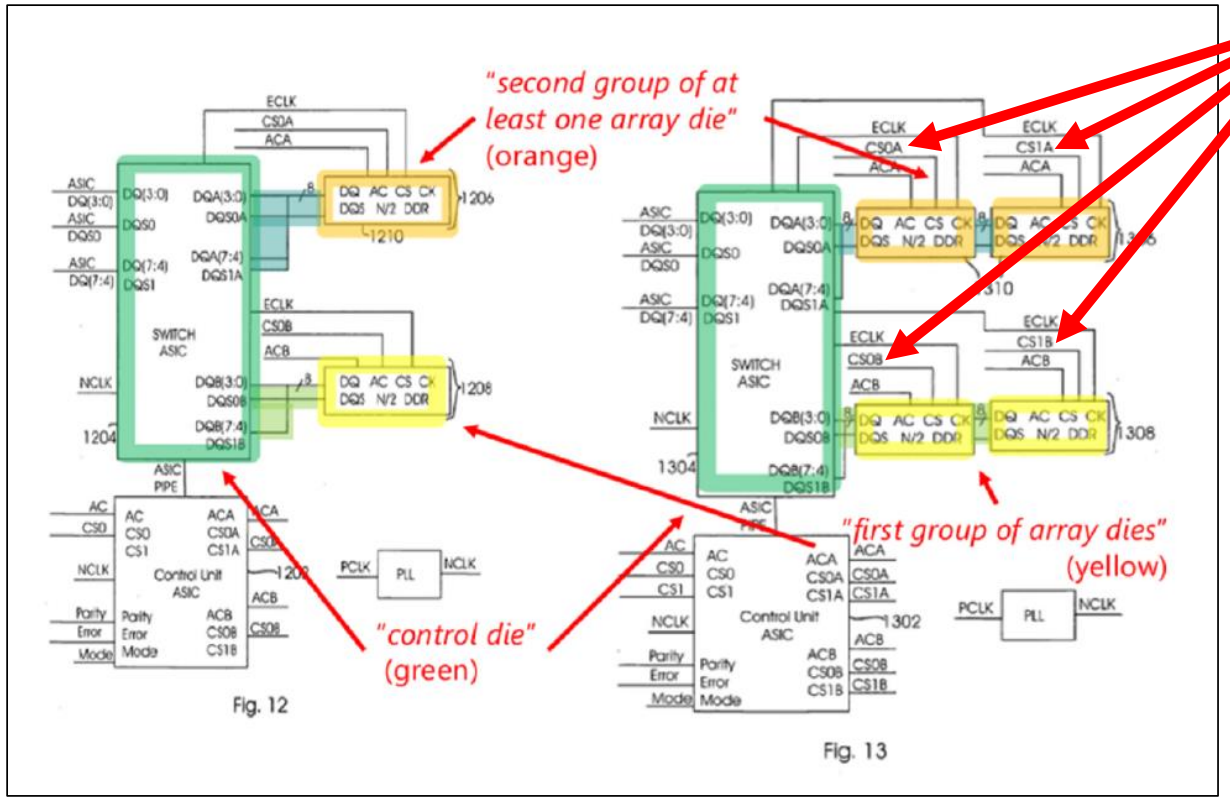
Q. But if they are in the same rank, then they would be responding to the chip selection or read commands and output data simultaneously, wouldn't they? Isn't that what a rank of memory does?

A. I guess that's right. So you wouldn't put them in the same rank, then, unless you had some local modification to be able to do -- yeah. So you wouldn't put them in the same rank. Again, that is not what I relied on.



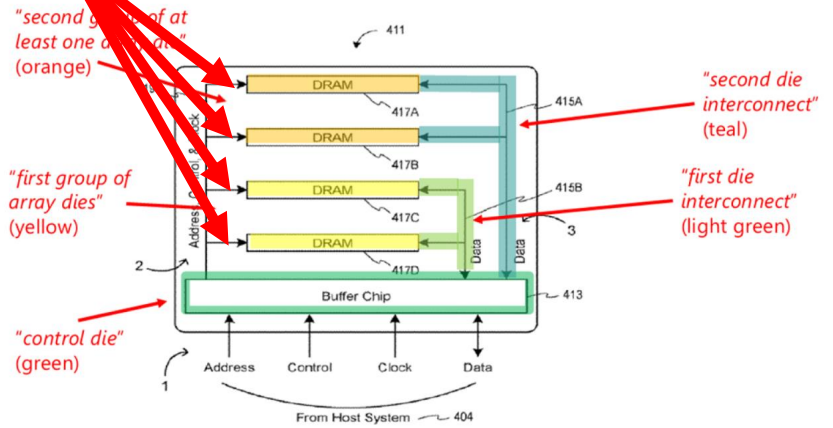
EX2025 (Wolfe) at 91:4-:22

Rajan's separate chip selects and shared data buses (on the right) were well known for rank multiplication (without data collisions) as shown by Ellsberry (on the left)



EX1026 (Ellsberry) at Figs. 12-13

Four separate chip selects (CS0A, CS1A, CS0B, CS1B), one for each rank (four ranks total)



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

'060: Paper 1 (Pet.) at 27, 29-30; Paper 24 (Reply) at 8-9
'160: Paper 1 (Pet.) at 29, 21-32; Paper 24 (Reply) at 9-10

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Ex. 1067, p. 82

The Institution Decision correctly found that the Petitions demonstrated invalidity under the District Court's construction of "*chip select signals*"

2. "Chip Select Signals," "Chip Select Conduits"

Claims 6, 11–14, 16–19, and 29–34 recite "chip select signals" or "chip select conduits." Patent Owner argues that the district court construed the term "chip select signals" and associated "chip select conduits" to "exclude[] situations in which a chip select signal could enable multiple array dies at once" and contends that we should adopt this construction. Prelim. Resp. 23–24 (citing Ex. 2004, 33–34). For the reasons explained below in section II.E.6, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction, and, therefore, we need not further address this claim construction at this time.

'060: Paper 13 (ID) at 11-12, 26

On this record, we disagree with Patent Owner's argument because Petitioner relies on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 61 (citing Ex. 1003 ¶¶ 329–330). Thus, we disagree with

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Ex. 1067, p. 83

The Institution Decision correctly found that the Petitions demonstrated invalidity under the District Court's construction of "*chip select signals*"

record, we agree with this interpretation as applied to the "second chip select signals" term of claims 15 and 16 of the '160 patent because these claims recite "the second chip select signals having a number of chip select signals greater than the first chip select signals and *equal to a number of array dies in the plurality of array dies*" (emphasis added). Claims 15 and 16 recite that there are fewer "first chip selection signals" than "second chip selection signals," and, therefore, each of the "first chip selection signals" appears to apply to multiple array dies, which makes sense in the context of the "rank multiplication" of claims 15 and 16.

'160: Paper 13 (ID) at 11-12, 27

obviousness. Petitioner, however, also relies on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 73 (citing Ex. 1003 ¶¶ 443–450). Thus, we disagree with Patent Owner's contention that Petitioner has not shown "where in the Petition it argues that each die in the modified Kim (where a TSV is connected to more than one die) belongs to a separate rank or *receives a separate chip select signal*." *See* Sur-reply 5 (emphasis added).

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Ex. 1067, p. 84

Non-DRAM devices also used "*chip select signals*"

Q. And do you use chip select signals with SRAMs?

A. Normally, yes.

Q. What about with NAND memory devices?

A. Often, yes.



EX2025 (Wolfe) at 72:6-:10

M48Z512A
M48Z512AY, M48Z512AV

4 Mbit (512 Kbit x 8) ZEROPOWER® SRAM

Table 1. Signal names

A0-A18	Address inputs
DQ0-DQ7	Data inputs/outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
V_{CC}	Supply voltage
V_{SS}	Ground

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V or 3.0 to 3.6 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

EX2044 (STMicroelectronics) at 1, 5, 7

2, 4, 8Gb: x8/x16 Multiplexed NAND Flash Memory
Bus Operation

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, data, and address information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH

EX2043 (Micron) at 16

'060: Paper 24 (Reply) at 15
'160: Paper 24 (Reply) at 18-19

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Kim + Rajan's interface can use signals from the JEDEC standard, even if the memory chips are not DRAM

The physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc.

EX1015 (Rajan) at 15:3-:9

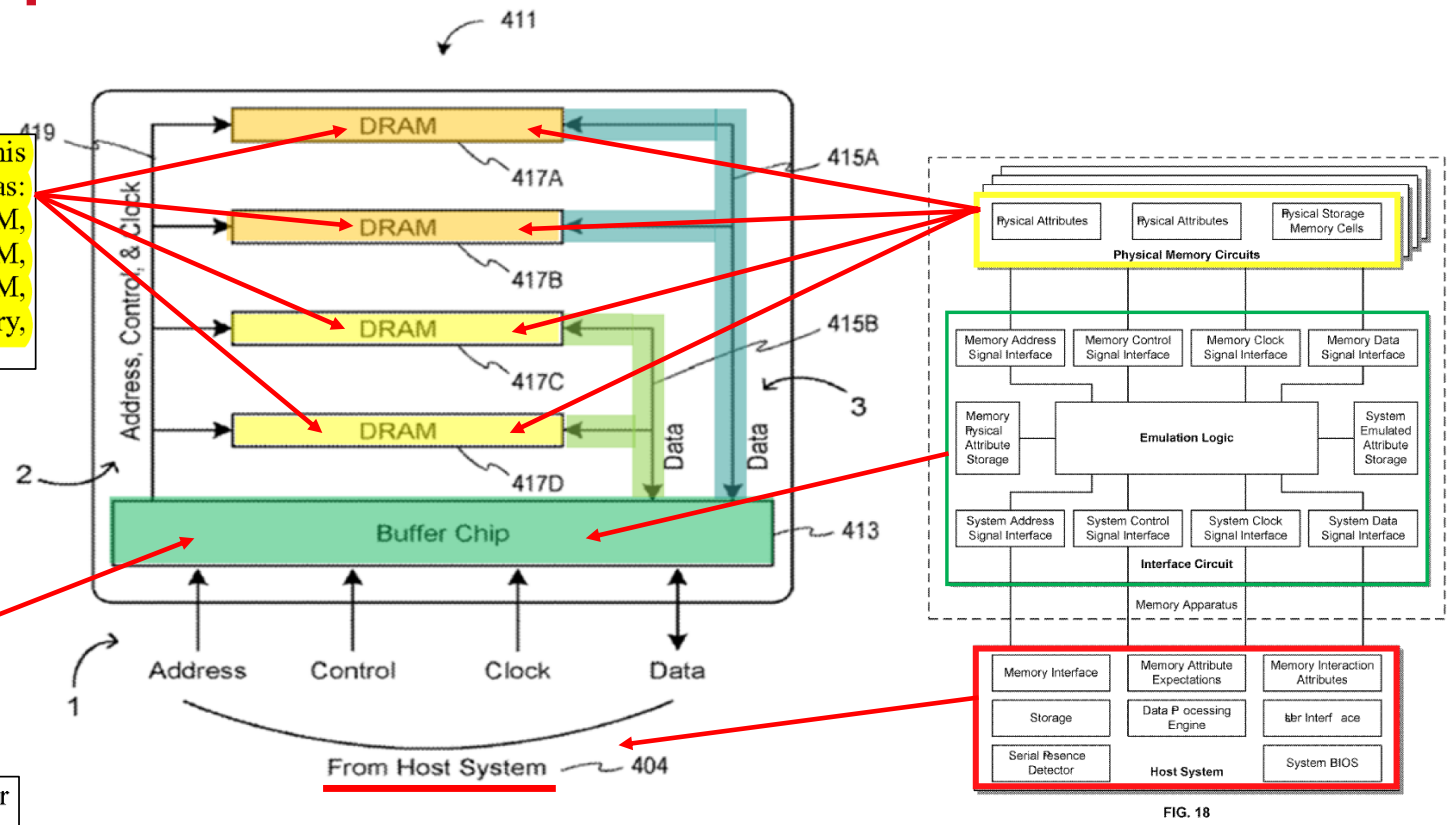


FIG. 4

FIG. 18

The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

EX1015 (Rajan) at 4:20-:24; *see also id.* at 4:48-:50, 14:6-:11, 14:39-:62 & Fig. 18

CLAIM 7 OF ‘060 PATENT

GROUND 2 (’060)

(KIM + RAJAN + RIHO)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

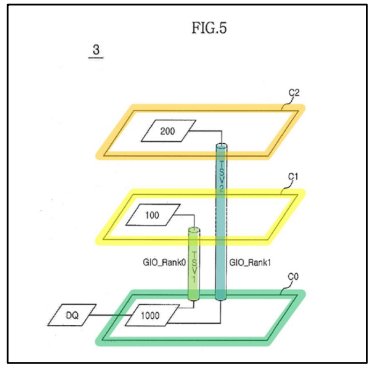
BAKER BOTTS

’060 Claim 7

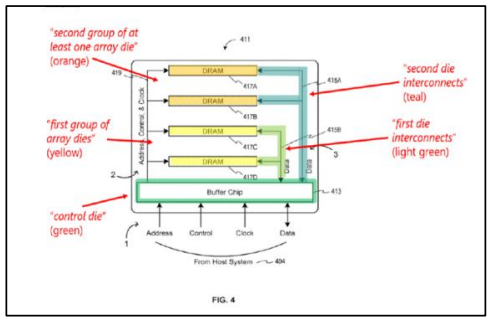
7. The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.

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Ex. 1067, p. 88

Ground 2 ('060): Kim and Rajan + Riho — minimizes skew and load

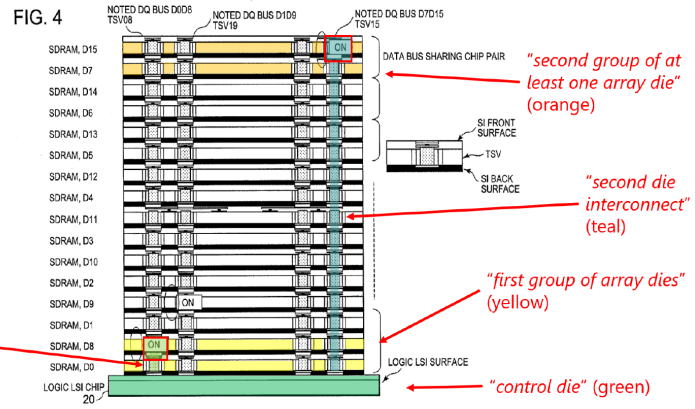


EX1014 (Kim) at Fig. 5



EX1015 (Rajan) at Fig. 4

Riho



EX1016 (Riho) at Fig. 4

[0050] In the illustrated structure, since the data signal DQ and data strobe signal DQS/B TSVs for all the DRAM sets corresponding to the respective I/O groups can be made substantially equal in length to each other, the skew between data signals DQ and data strobe signals DQS/B can be minimized. This structure (equi-length interconnections) is very important in the stacked structure in which the plurality of DRAM sets are stacked in sequence with respect to the controller chip. This is because, in this embodiment, each I/O group is

EX1016 (Riho) at [0050]

[0103] Further, by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups.

EX1016 (Riho) at [0103]

Netlist admits that Riho teaches two dies in two ranks sharing "equi-length" TSVs, thus reducing skew without the need for more TSVs that "were difficult and expensive"

TSVs, in Riho, pairs of dies from two different ranks are connected to the same TSV. *See* Kim, Fig. 5, [0042]-[0045], discussion in Section VII.A; Riho, Fig. 4

'060: Paper 20 (POR) at 52

Riho discloses instead that the skew between DQ and DQS/B are reduced by making the corresponding TSVs "substantially equal in length to each other."

EX2023 (Brogioli) at ¶ 203



designed to receive or decode such signals. TSVs that penetrate through multiple dies were difficult and expensive to form at the time of the invention. For instance,

EX2023 (Brogioli) at ¶ 195

A larger load on one TSV vs. another TSV would skew the signals

of those data signal TSVs] *so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit* [which a Skilled Artisan understood reduces skew between the data signals]." *Supra* at ¶¶135-137.

For example, a Skilled Artisan would have understood that the larger the capacitive load, the larger the delay in the transition of the driven signal. Ex. 1030 (Brown) at p.134. Accordingly, a difference in load may result in different signal timing, resulting in a skew between different signals. For example, DQ and DQS signals should be synchronized, but a skew between them may result in an erroneous read of the data value. Ex. 1019 (JESD79-3C) at 13 ("The data strobes DQS, DQSL,

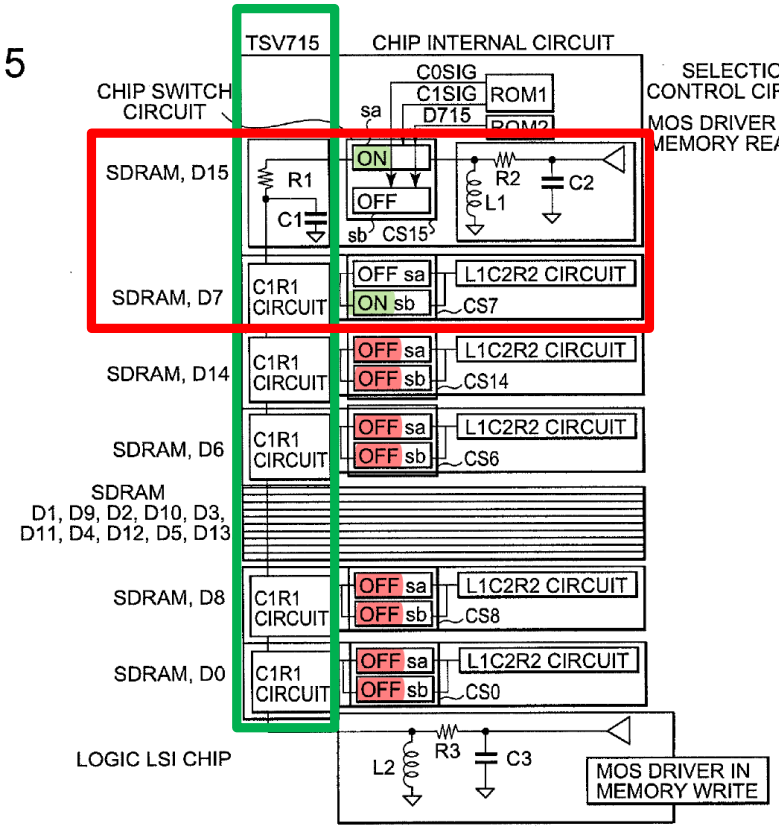


'060: EX1003 (Wolfe) at ¶341

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Ex. 1067, p. 91

Riho teaches to have "equi-length" TSVs and the same number of chips (e.g., two) on each TSV "*in consideration of a load of the …die interconnect*" (e.g., to reduce skew)

FIG. 5



EX1016 (Riho) at Fig. 5



Q. Okay. Do you have to overcome the loads that's imposed by the segments, basically the unused segments of the TSVs --

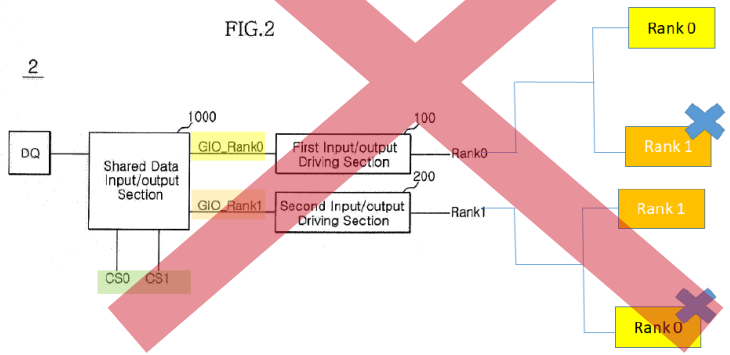
A. Yes.

A. Yes. As we discussed yesterday, you need to look at the entirety of the resistance capacitance, inductance network in order to understand the load on the driver that is driving that TSV and that's what's illustrated in Figure 5.

EX2025 (Wolfe) at 197:21-198:5

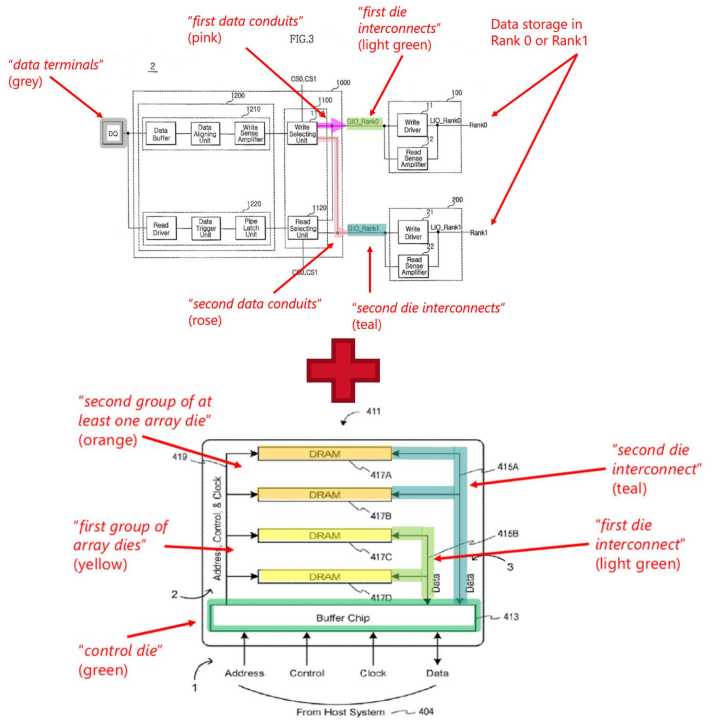
Netlist's new sur-reply argument relies on Strawman #2 (cross-connecting TSVs and ranks), contrary to teaching of Kim + Rajan

Riho's die grouping to Kim. Reply 16. Riho's die grouping would be the same as the second scenario discussed in the POR, and Samsung does not dispute its inoperability.[7] POR 28-30; Reply 11.



'060: Paper 28 (Sur-reply) at 21

Kim + Rajan



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38

'060: Paper 1 (Pet.) at 81-82; Paper 24 (Reply) at 11, 16-18

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GROUNDS 4-5 (’060) AND GROUND 2 (’160)

03

GROUND 4 (’060): RIHO+RAJAN

GROUND 5 (’060), GROUND 2 (’160): RIHO+RAJAN+RIHO2

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

Prior Art: Riho2 [EX1018] (same inventor as Riho [EX1016])

[0003] This invention relates to a semiconductor device having a DRAM or the like, and particularly to a semiconductor device formed by stacking a plurality of chip dies.

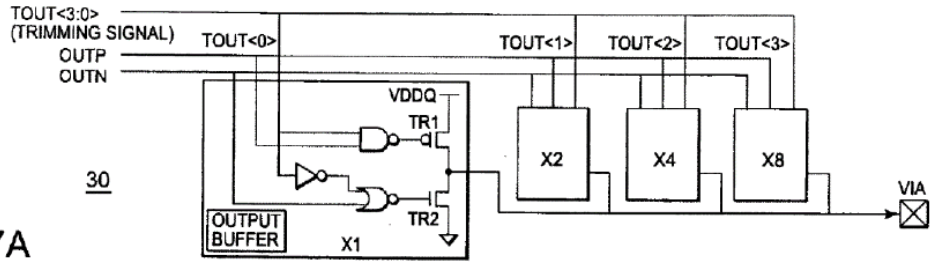


FIG. 7A

[0097] FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit **30**, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In

EX1018 (Riho2) at [0003], [0097] & Fig.7A

'060: Paper 1 (Pet.) at 20-21, 138-40
'160: Paper 1 (Pet.) at 22-23, 81-86

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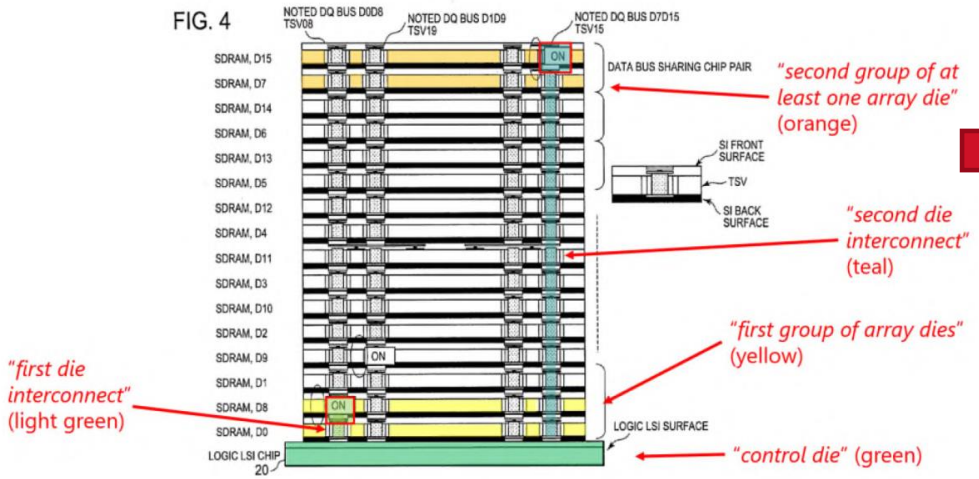
SUMMARY OF COMBINATIONS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

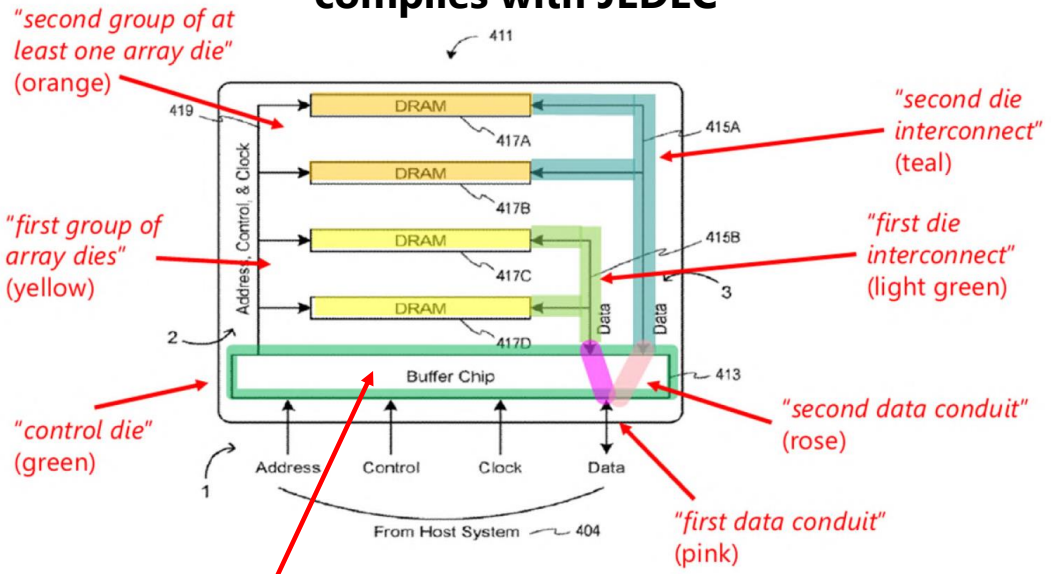
Riho + Rajan

Riho: control die with TSVs to groups of stacked array dies



EX1016 (Riho) at Fig. 4

Rajan: interface that complies with JEDEC

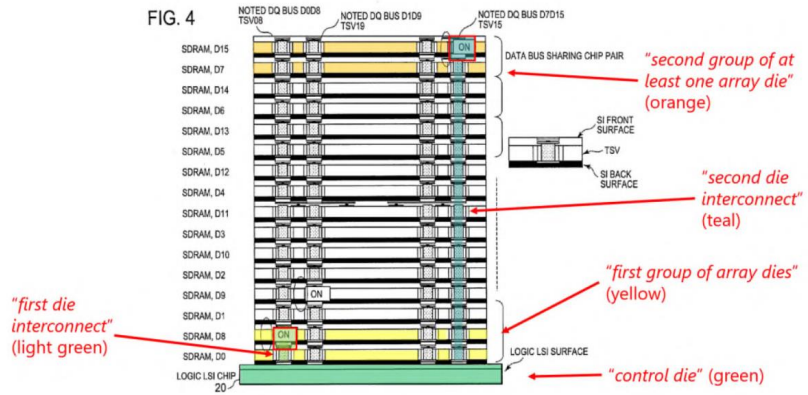


The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities.

EX1015 (Rajan) at 4:20-:24; *see also id.* at 4:48-:50, 14:6-:11, 14:39-:62 & Fig. 18

Riho and Rajan + Riho2 — optimizes drivers given TSV's variations in capacitance/resistance

Riho's TSVs have varying impedance (capacitance, resistance) due to *manufacturing* and *position*

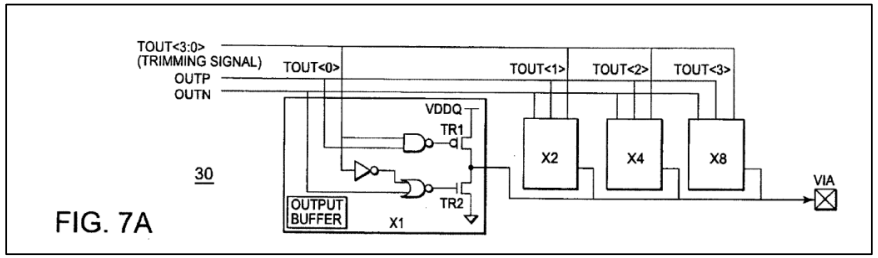


[0055] It is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in manufacturing processes (TSV forming process, bump forming process, and TSV-bump connection process). That is, TSVs formed in different manufac-

[0061] As is clear from FIG. **3**, the SDRAM chip located closer to the logic LSI chip **20** has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip **20** has a larger penetrating through resistance. Further, these penetrating through resistances

EX1016 (Riho) at [0055], [0061] & Fig.4

Riho2: optimizes drivers according to timing variations caused by capacitance/resistance



[0097] FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit **30**, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In

EX1018 (Riho2) at [0097] & Fig.7A

"ELECTRICAL COMMUNICATION" CLAIM CONSTRUCTION

"NOT IN ELECTRICAL COMMUNICATION WITH [SOME OF] THE … ARRAY DIES"

GROUND 2 ('160), [1.D.1]-[1.D.2]

GROUNDS 4-5 ('060), [1.D.1]-[1.D.2]

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

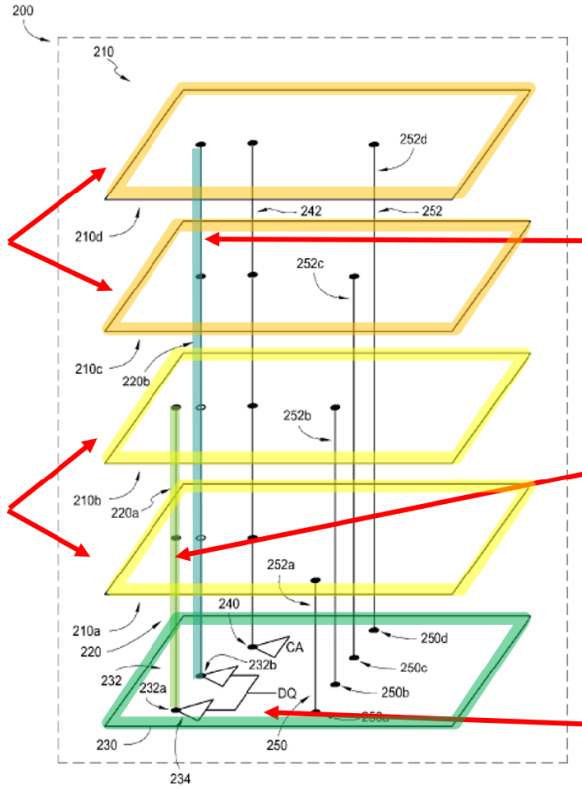
’060/’160 Claims: *“<u>not</u> in electrical communication”*

’060 Patent, Claim 1:

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

’160 Patent, Claim 1:

first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and



Array Dies 210c and 210d (orange)

Array Dies 210a and 210b (yellow)

Die interconnect 220b (teal)

Die Interconnect 220a (light green)

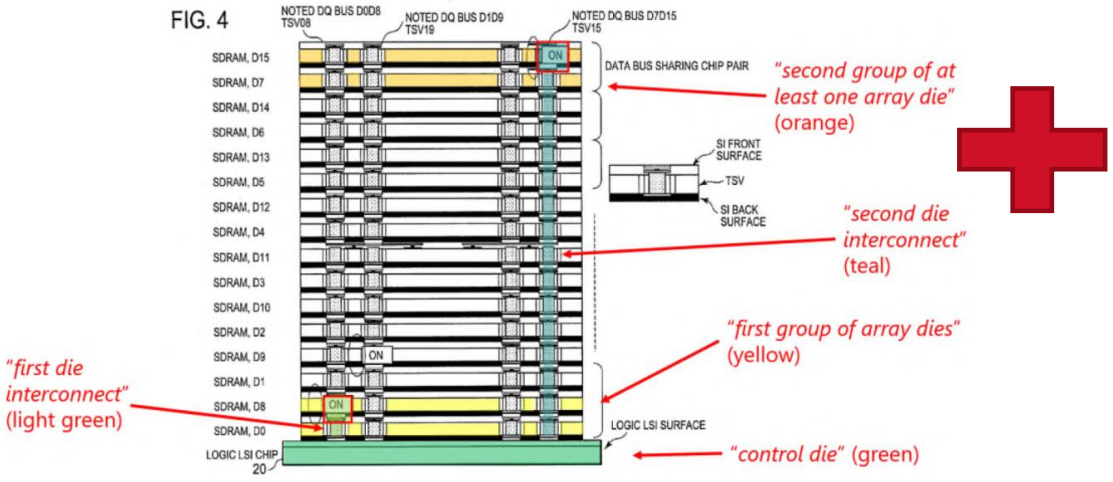
Drivers 234 (for data)

FIG. 2

Samsung Electronics Co., Ltd.
Ex. 1067, p. 100

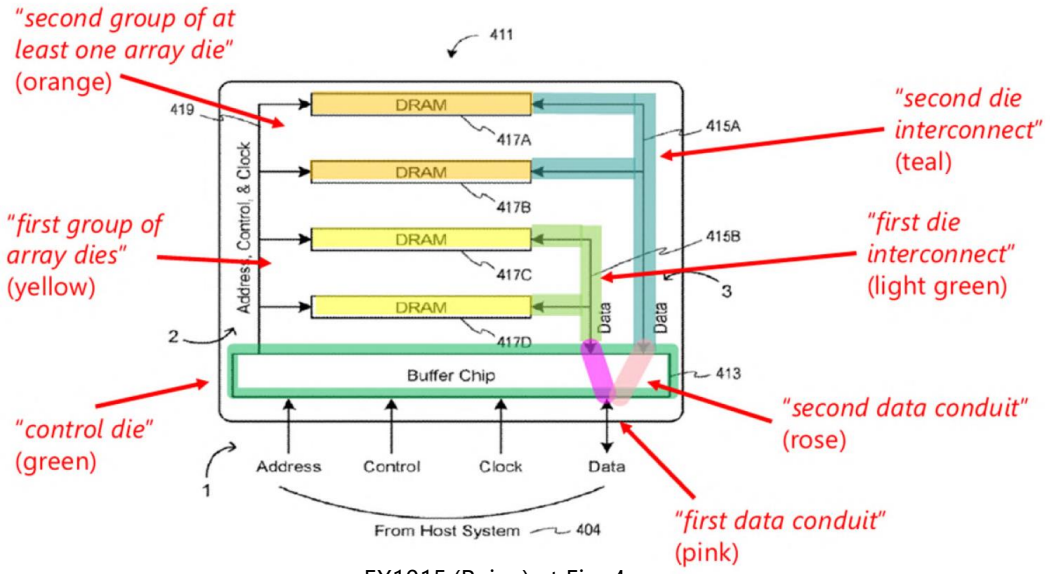
Riho + Rajan: each die interconnect is "*not* in electrical communication with [*some* of] the … array dies"

Riho



EX1016 (Riho) at Fig. 4

Rajan



EX1015 (Rajan) at Fig. 4

The Institution Decision correctly found that Riho + Rajan renders obvious *"not in electrical communication with [some of] the … array dies"*

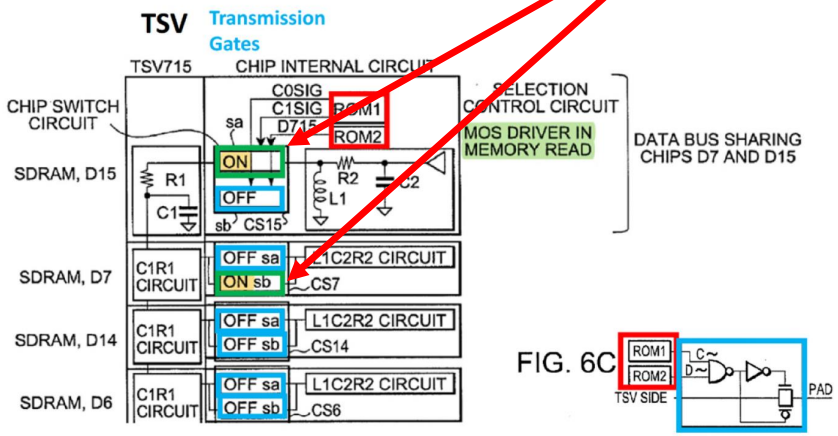
On the present record, we find Petitioner's contentions sufficiently persuasive. Riho describes the TSV configuration as follows: "[T]he data signal DQ TSV19 and circuits formed at the front surfaces of the SDRAMs D1 and D9 are in a conductive state (i.e. on state) while the data signal DQ TSV19 is *not electrically connected to the SDRAMs other than the SDRAMs D1 and D9*." Ex. 1016 ¶ 65 (emphasis added); *see* Pet. 100–01 (citing this disclosure). Thus, Riho expressly discloses that there is no electrical connection to SDRAMs other than the pair with which the TSV is in a "conductive state." On this record, we disagree with Patent Owner's argument that Riho's use of a switch to accomplish this is no different from the prior art configuration in Figure 1A of the '060 patent. *See* Prelim. Resp. 39. In describing the state of the prior art, the '060 patent explains that "a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects *and the corresponding circuitry of the array dies*," which requires a driver "large enough to overcome the load on the driver." Ex. 1001, 2:8–13 (emphasis added). Riho does not present the same issue because the TSVs are "not electrically connected to" all of the SDRAMs, as explained in paragraph 65 of Riho, thus obviating the need for drivers large enough to drive signals to all of the circuitry on all chips.

'060: Paper 13 (ID) at 18;
see also '160: Paper 13 (ID) at 19-20

[0065] Likewise, the data signal DQ TSV**19** and circuits formed at the front surfaces of the SDRAMs D**1** and D**9** are in a conductive state (i.e. on state) while the data signal DQ TSV**19** is not electrically connected to the SDRAMs other than the SDRAMs D**1** and D**9**. Further, the data signal DQ TSV**715** and circuits formed at the front surfaces of the SDRAMs D**7** and D**15** are in a conductive state (i.e. on state).

EX1016 (Riho) at [0065]

FIG. 5



EX1016 (Riho) at Figs. 5, 6C

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Ex. 1067, p. 102

Netlist's expert had no opinion on the construction of "*electrical communication*"



Q. So would it be fair to say that the construction of electrical communication does not depend on load?

MR. LINDSAY: Objection. Form.

THE DEPONENT: I don't have an opinion on that one way or the other right now. I wasn't asked to analyze that.

Q. (By Mr. Chandler) And in the answer you just gave me, I didn't hear you say the word "connection" or "electrical connection."

In your opinion, does the construction for electrical communication depend at all on whether or not there's an electrical connection?

A. Again, I haven't been asked to perform that analysis or offer a construction on, quote, "electrical communication" by itself or how it may relate to electrical connection.

EX1052 (Brogioli) at 356:15-:21, 356:25-357:6

'060: Paper 24 (Reply) at 20-23
'160: Paper 24 (Reply) at 19-22

Samsung Electronics Co., Ltd.
Ex. 1067, p. 103

District Court: "*electrical communication*" has plain and ordinary meaning, and requires more than the "mere presence of 'data ports'"

this is simply an infringement argument by Netlist rather than a dispute about scope. That said, if Netlist's position is the mere presence of "data ports" is enough to meet the "electrical communication" requirement for the purpose of determining infringement or invalidity, the Court agrees with Micron that is improper.

Based on the foregoing, the Court agrees with Netlist that "electrical communication" is different from "electrical connection." The Court also agrees with Micron that the existence of data ports, without more, does not satisfy the "electrical communication" requirement in the claims. With this guidance, however, the Court will give this term a "plain and ordinary meaning" construction.

EX1066 at 8-11

'060: Paper 32 (Mandatory Notices) at 2-3
'160: Paper 32 (Mandatory Notices) at 2-3

Samsung Electronics Co., Ltd.
Ex. 1067, p. 104

'060/'160 Patents: "*electrical communication*" requires an electrical connection

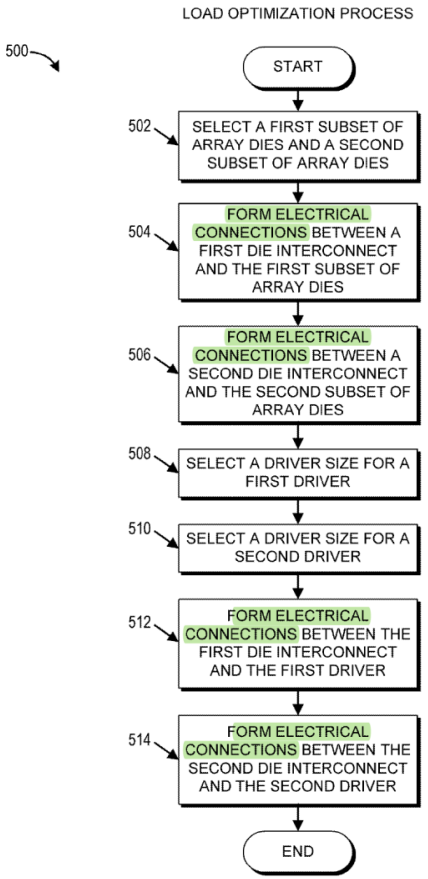


FIG. 5

The process **500** further comprises forming electrical connections between the first die interconnect and the first subset of array dies in an operational block **504**. The process **500** further comprises forming electrical connections between the second die interconnect and the second subset of array dies in an operational block **506**. Forming the electrical connections places the die interconnects in electrical communication with the respective subsets of array dies. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and at least one port from each array die of the respective subsets of array dies.

514. Forming the electrical connections places the die interconnects in electrical communication with the respective drivers. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and a data conduit that includes the respective driver.

'060: EX1001 at 17:25-:35, 17:65-18:3 & Fig. 5
'160: EX1001 at 17:13-:25, 17:55-:60 & Fig. 5

'060: Paper 24 (Reply) at 20-23
'160: Paper 24 (Reply) at 19-22

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Ex. 1067, p. 105

'060/'160 Patents: "data ports" without electrical connection (e.g., due to "insulator" or "stubs") are not "*in electrical communication*"

In addition, the die interconnects **220** may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect **220***b* may pass through array dies **210***a* and **210***b* using TSVs that do not enable electrical communication between the die interconnect **220***b* and data ports of the array dies **210***a* and **210***b* (illustrated by the unfilled circles). In this way, the array dies **210***a*, **210***b* are not responsive to the data signal beings transmitted by the die interconnect **220***b*. However, the die interconnect **220***b* may be connected with at least one data port of each of the array dies **210***c* and **210***d* using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.

'060: EX1001 at 8:35-:62
'160: EX1001 at 8:38-:65

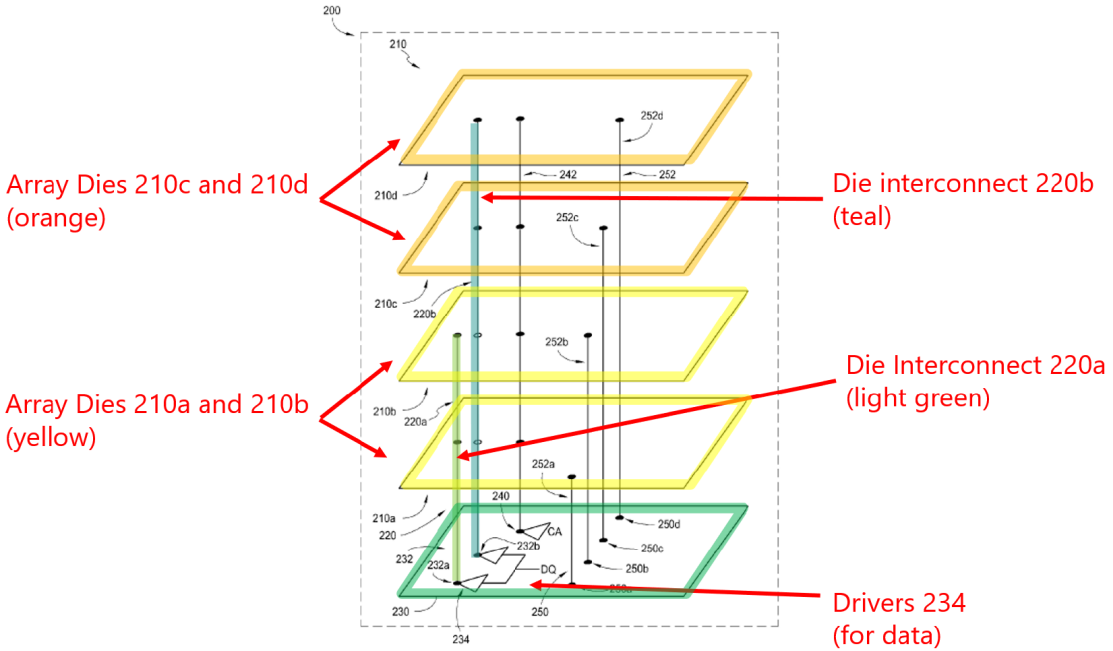


FIG. 2

'060: Paper 24 (Reply) at 20-23
'160: Paper 24 (Reply) at 19-22

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Ex. 1067, p. 106

Netlist agrees that "*electrical communication*" requires more than just an electrical connection to a "portion" or "pad" of an array die

> electrical connection between the TSV and the stubs. *Id.*, 8:60-62. Hence, it is incorrect that any electrical connection between a die interconnect and a portion of an array die would lead to electrical communication.

> Brogioli also explained that a die interconnect was not in communication with an array die if the TSV was connected to only dummy pads on the die, because there was nothing on the other side of the pad in the particular array die for the die interconnect to communicate with. *Id.*

'060: Paper 20 (POR) at 60-62
'160: Paper 20 (POR) at 57-59

'060: Paper 24 (Reply) at 20-23
'160: Paper 24 (Reply) at 19-22

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Ex. 1067, p. 107

Dictionary definition: "*electrical communication*" is electrical connection that exchanges information

"electrical":

1 *or* **elec·tri·cal** Listen to the pronunciation of electrical \-tri-kəl\ **:** of, relating to, or operated by **electricity** <an *electric* current> <an *electric* heater>

EX1063 (Merriam-Webster)

"communication":

1 : an act or instance of transmitting
2 a : information **communicated** **b :** a verbal or written message
3 a : a process by which information is exchanged between individuals through a common system of symbols, signs, or behavior <the function of pheromones in insect communication>; *also* **:** exchange of information **b :** personal rapport <a lack of communication between old and young persons>

EX1064 (Merriam-Webster)

'060: Paper 24 (Reply) at 20-23
'160: Paper 24 (Reply) at 19-22

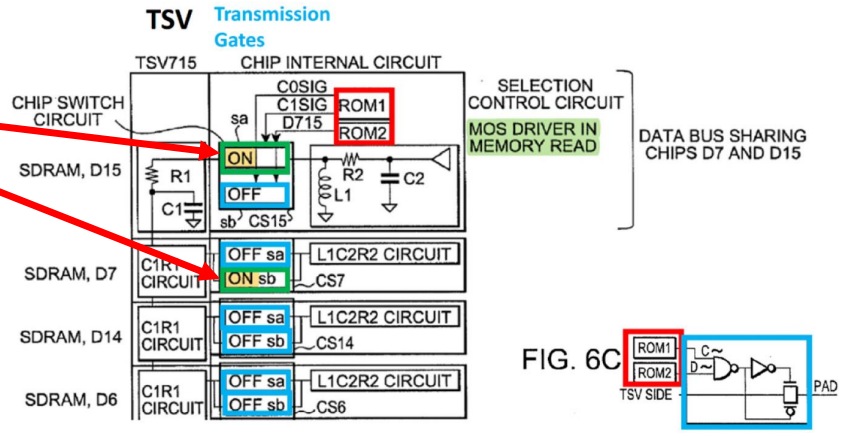
Samsung Electronics Co., Ltd.
Ex. 1067, p. 108

In Riho, there is NO electrical connection, thus NO "*electrical communication*" through switches (transmission gates) that are permanently OFF

[0065] Likewise, the data signal DQ TSV**19** and circuits formed at the front surfaces of the SDRAMs D**1** and D**9** are in a conductive state (i.e. on state) while the data signal DQ TSV**19** is not electrically connected to the SDRAMs other than the SDRAMs D**1** and D**9**. Further, the data signal DQ TSV**715** and circuits formed at the front surfaces of the SDRAMs D**7** and D**15** are in a conductive state (i.e. on state).

EX1016 (Riho) at [0065]

FIG. 5



EX1016 (Riho) at Figs. 5, 6C

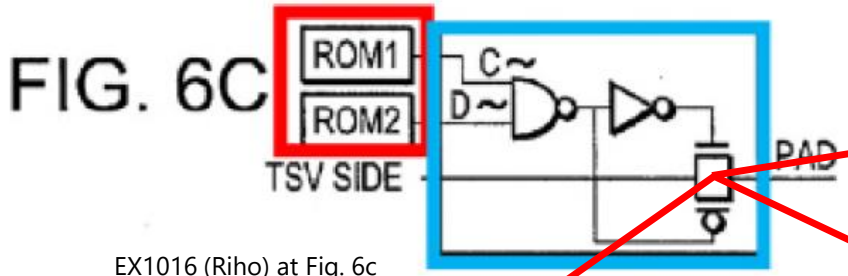
FIG. 6C

A. -- in a certain embodiment, TSV 715 is electrically connected to the D15 die and it's electrically connected to the D17 die -- I'm sorry, the D7 die, but it is disconnected from the remaining SDRAM die.

EX2025 (Wolfe) at 9:10-:14



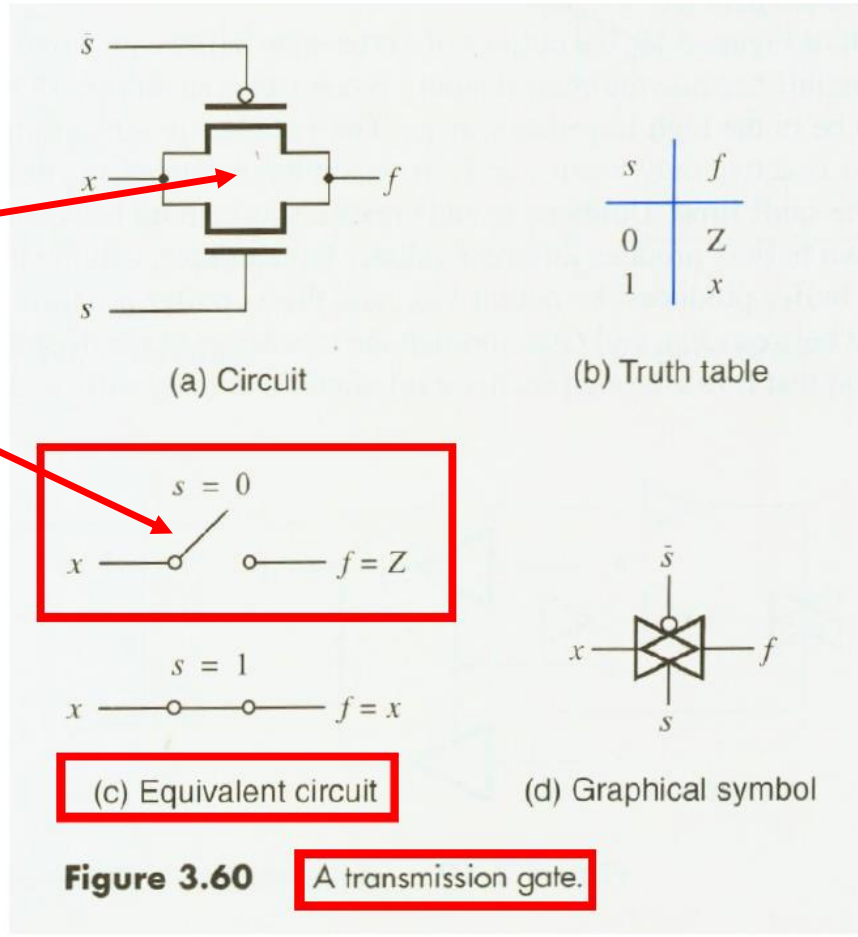
Riho's OFF switch is a transmission gate that (in the words of the '060/'160 Patents) creates "an insulator…to prevent electrical communication …[with] the array die circuitry"



EX1016 (Riho) at Fig. 6c

circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies

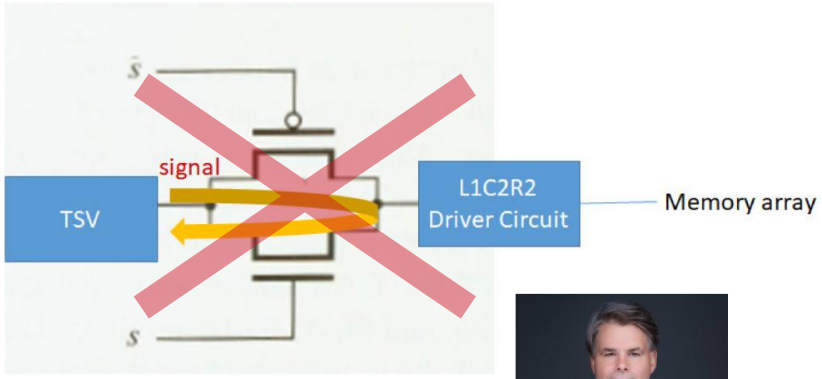
'060: EX1001 at 8:47-:53
'160: EX1001 at 8:50-:56



EX1030 (Brown) at 138

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Ex. 1067, p. 110

Netlist's expert admitted his figure was wrong, because information from the TSV (on the left) "wouldn't be making out to the other side … of the transmission gate"



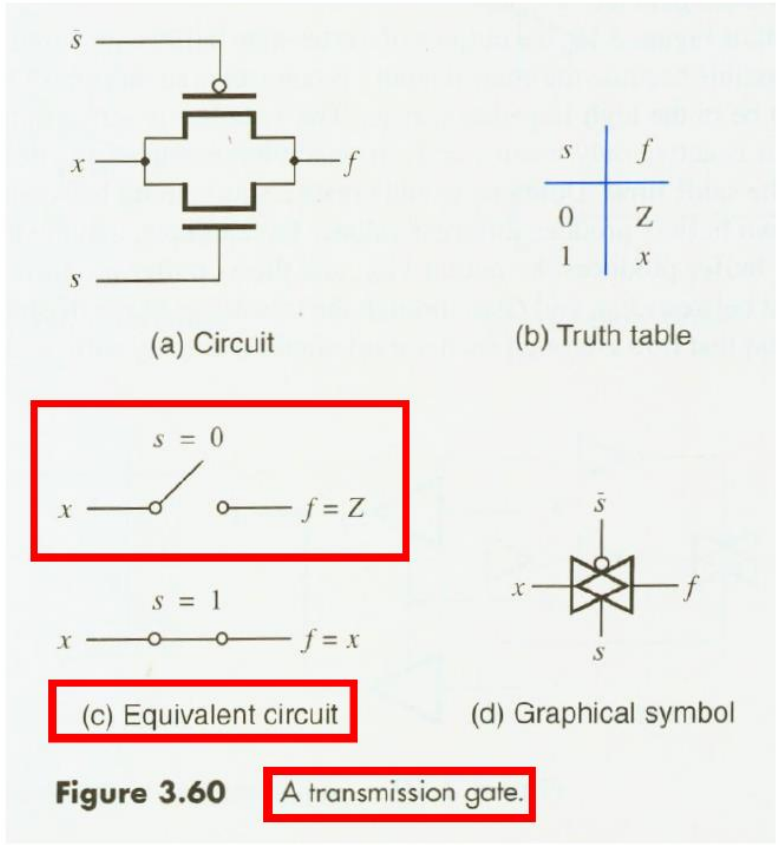
EX2023 (Brogioli) at p.157



Q. And so the transmission gate shown at the top of page 157 of your declaration marked as Exhibit 2023 -- when it's off, any signal coming from the TSV will not make it to the black dot on the right side of the transmission gate, correct?

A. I think, at a high level, the -- if we are -- if there's a logical 1, for example, coming up the TSV and the gate is off, the logical 1 value wouldn't be making it out the other side or at that adjoining point on the other side of the transmission gate.

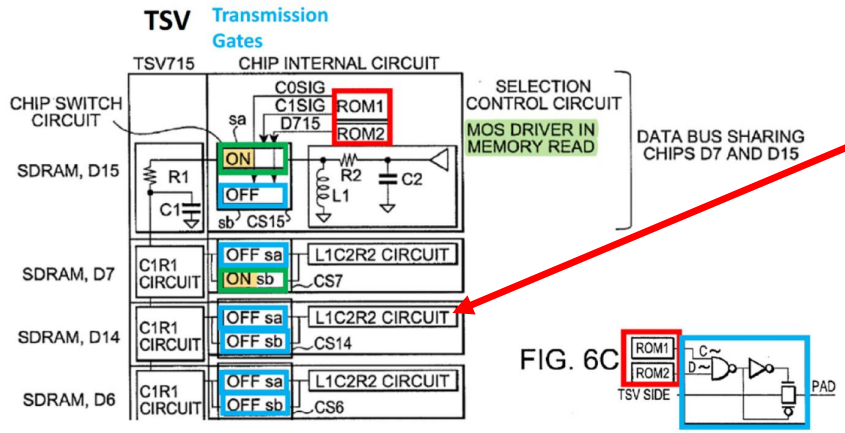
EX1052 (Brogioli) at 358:10-:20



EX1030 (Brown) at 138

Netlist's expert admitted that Riho's OFF switch means the TSV on the left is not "electrically connected" to the L1C2R2 driver circuit on the right

FIG. 5



EX1016 (Riho) at Figs. 5, 6C

FIG. 6C

Q. In Figure 5 of Riho, marked as Exhibit 1016, the L1C2R2 circuit, to the right of the off switches labeled CS14, is not electrically connected to the TSV715 to the left of the off switches; correct?

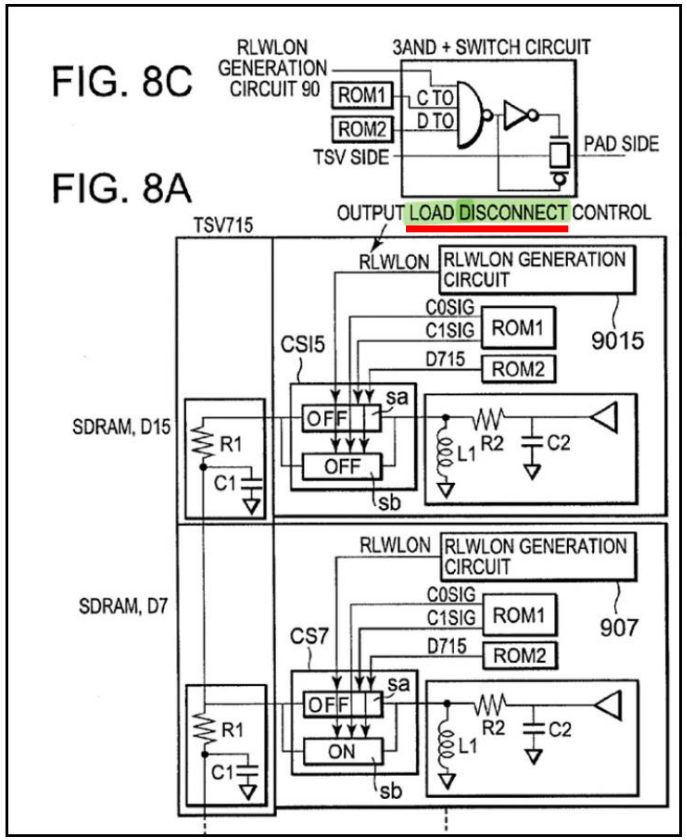
ATTORNEY ZHONG: Objection; form.

THE WITNESS: I think that's what Riho would be saying in the, quote, electrically connected language, at least of Riho's paragraph 65.

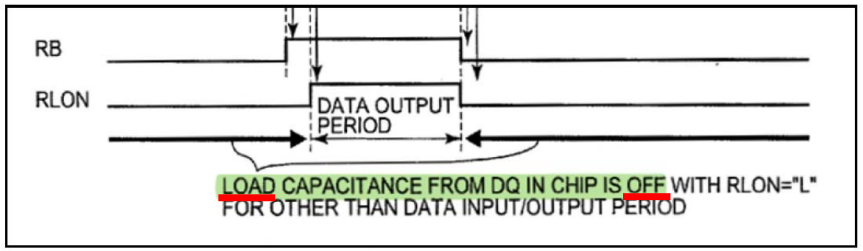
EX1052 (Brogioli) at153:25-154:9



Riho's "OFF" switch also disconnects the load of the SDRAMs



EX1016 (Riho) at Fig. 8a, Fig. 8c



EX1016 (Riho) at Fig. 10

described. The semiconductor device shown in FIG. **8**A has a structure in which only either one of each of SDRAM pairs forming sets (DRAM sets) and sharing data signal DQ TSVs, respectively, is connected to the corresponding shared data signal DQ TSV while the other SDRAM is completely disconnected from the corresponding shared data signal DQ TSV, thereby not only compensating for phase variations of data signals DQ, but also reducing by half the load capacitance of data buses formed by the data signal DQ penetrating through electrodes TSV. This will be explained in more detail.

EX1016 (Riho) at [0110]

"1" level. On the other hand, the SDRAM chip is disconnected from this penetrating through electrode (TSV) for a period in which the RLON signal has a logic "0" level. Accordingly, the load capacitance from this SDRAM chip is in an off state.

EX1016 (Riho) at [0123]

When Riho's switch is OFF, any remaining load is "negligible"



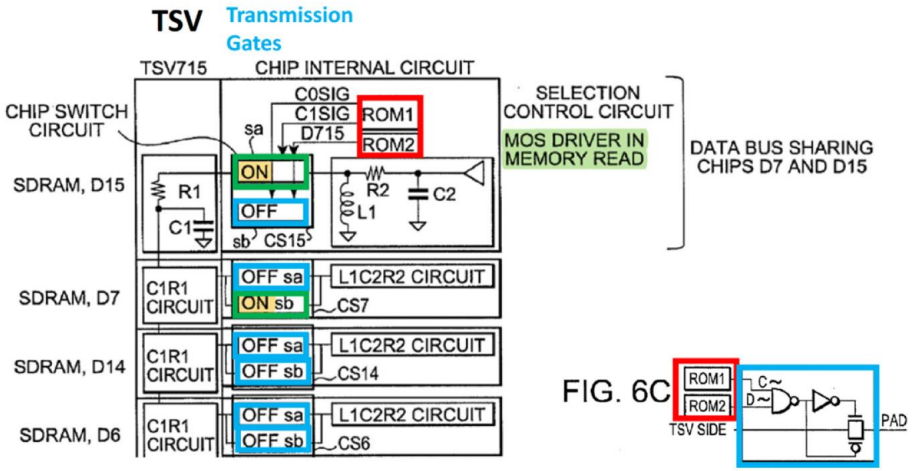
A. -- and, therefore, the question of interest essentially is does the driver on another die present a load to another driver that's trying to drive through the TSV, and the answer here would be that when the switch is on, connected to a particular driver, it does add to the load; and when the switch is off, connected to a particular driver, it does not add to the load.

THE WITNESS: As I mentioned, everything in the universe provides a capacitive load on everything else.

When we do the analysis and the teaching from Riho is that the capacitive load of the turned-off transmission gates is negligible. It can be ignored. And that if -- their purpose is to isolate the capacitive load from the driver circuits, which is much more substantial.

EX2025 (Wolfe) at 17:20-18:2 , 49:6-49:14

FIG. 5



EX1016 (Riho) at Figs. 5, 6C

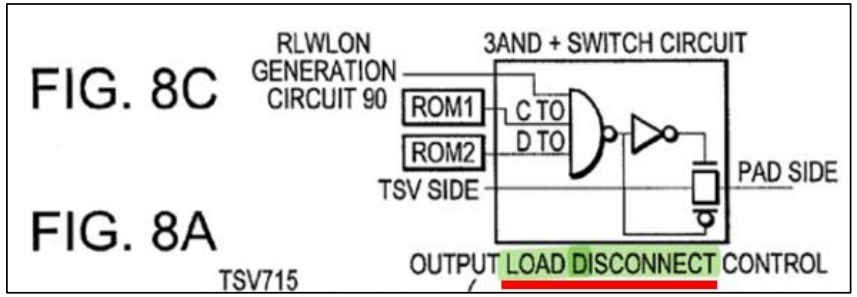
Netlist's expert's opinion that Riho's transmission gate "will materially increase the load" is contrary to Riho's express disclosure

267. Therefore, a person of ordinary skill would recognize that adding a transmission gate in a practical system that maintains constant drive strength will materially increase the load presented to the TSV driver in the control die, not decrease it. Accordingly, in Riho, each TSV is electrical communication with all dies.

EX2023 (Brogioli) at ¶ 267



vs.



described. The semiconductor device shown in FIG. **8**A has a structure in which only either one of each of SDRAM pairs forming sets (DRAM sets) and sharing data signal DQ TSVs, respectively, is connected to the corresponding shared data signal DQ TSV while the other SDRAM is completely disconnected from the corresponding shared data signal DQ TSV, thereby not only compensating for phase variations of data signals DQ, but also reducing by half the load capacitance of data buses formed by the data signal DQ penetrating through electrodes TSV. This will be explained in more detail.

"1" level. On the other hand, the SDRAM chip is disconnected from this penetrating through electrode (TSV) for a period in which the RLON signal has a logic "0" level. Accordingly, the load capacitance from this SDRAM chip is in an off state.

EX1016 (Riho) at [0110], [0123] & Figs. 8A, 8C

'060: Paper 24 (Reply) at 23-30
'160: Paper 24 (Reply) at 22-29

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Ex. 1067, p. 115

Netlist's expert's opinion must be disregarded

"[W]e must disregard the testimony of an expert that is plainly inconsistent with the record"

Homeland Housewares, LLC v. Whirlpool Corp.,
865 F.3d 1372, 1378 (Fed. Cir. 2017)

"Courts and tribunals properly discount expert testimony that is at odds with a patent's disclosure, as we did here."

CareFusion Corp. v. Baxter Int'l Inc.,
IPR2016-01463, Paper 40, at 4 (PTAB June 13, 2018)

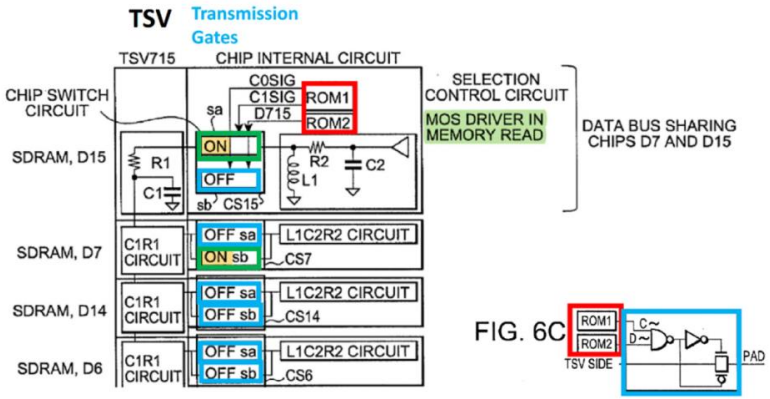
Netlist's expert's opinion on "*electrical communication*" is contrary to the District Court's claim construction



248. Hence, because each TSV in Riho's structure has an electrical connection to a switch circuit (data port) that connects to a driving circuit and memory arrays in every die, each TSV would be regarded as in electrical communication with each and every die in the stack. EX1016, [0086] ("An output

EX2023 (Brogioli) at ¶ 248

FIG. 5



EX1016 (Riho) at Figs. 5, 6C

vs.



this is simply an infringement argument by Netlist rather than a dispute about scope. That said, if Netlist's position is the mere presence of "data ports" is enough to meet the "electrical communication" requirement for the purpose of determining infringement or invalidity, the Court agrees with Micron that is improper.

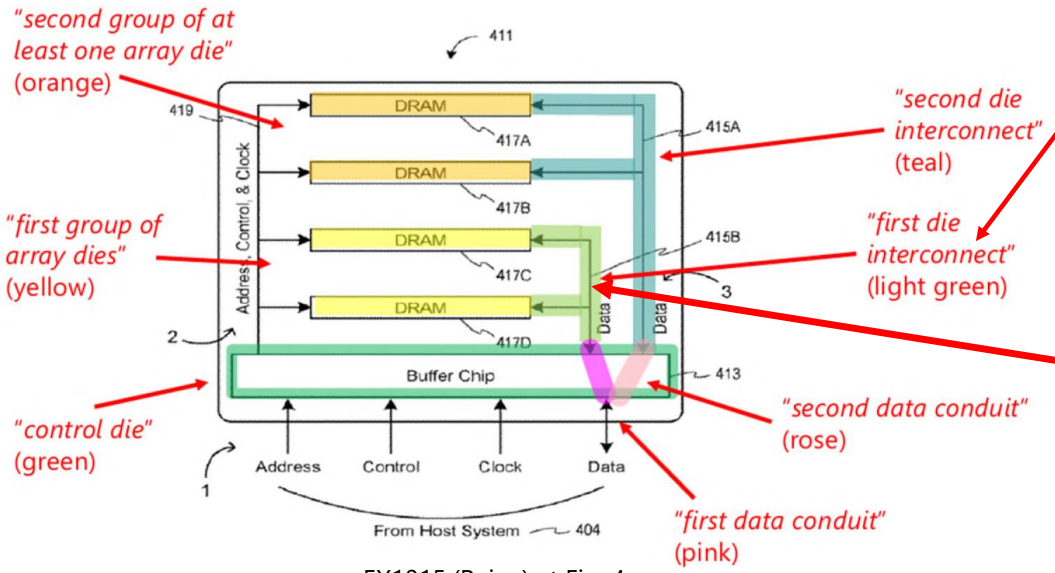
Based on the foregoing, the Court agrees with Netlist that "electrical communication" is different from "electrical connection." The Court also agrees with Micron that the existence of data ports, without more, does not satisfy the "electrical communication" requirement in the claims. With this guidance, however, the Court will give this term a "plain and ordinary meaning" construction.

EX1066 at 8-11

'060: Paper 32 (Mandatory Notices) at 2-3; Paper 20 (POR) at 66; Paper 24 (Reply) at 22-30
'160: Paper 32 (Mandatory Notices) at 2-3; Paper 20 (POR) at 63; Paper 24 (Reply) at 23-32

Samsung Electronics Co., Ltd.
Ex. 1067, p. 117

Rajan also discloses "*die interconnects*" that are "*not in electrical communication with [some of] the … array dies*"



EX1015 (Rajan) at Fig. 4

to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g.,

'060: EX1001 at 5:51-:53
'160: EX1001 at 5:43-:56

Q. Figure 4 of Rajan marked as Exhibit 1015 shows that the data bus 415B is not connected to 417A or to 417B; correct?

A. That -- that sounds right. Data bus 415B is connected to Rajan's DRAM chips, just 417D and 417C.

EX1052 (Brogioli) at 178:9-:14



'060: Paper 24 (Reply) at 31-32; Paper 1 (Pet.) at 100-102
'160: Paper 24 (Reply) at 30-31; Paper 1 (Pet.) at 81-84

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Ex. 1067, p. 118

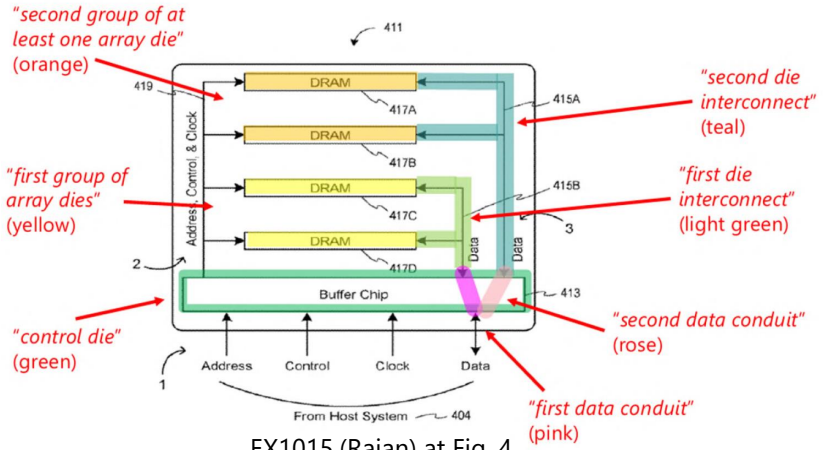
POSITA understood that reducing the load, by not connecting to every die in the stack, increases the speed

Q. How would you explain to a layperson what the concept of capacitive load is and sort of what its relevance is to memory devices in general?

A. I would say as a -- as a general example, you might think of it trying to lift a weight or something like that. And you want to lift it up and down quite quickly. And if there's a lot of -- if the capacitive load is increasing, you can't lift it up and down as quickly. So if you're trying to, for example, send signals down a wire, as the load's increasing on the wire, you might have to do things more slowly. But if you can reduce the load, you can send information more quickly, which in a lot of cases is better; things can run faster.

EX1052 (Brogioli) at 132:18-133:8





EX1015 (Rajan) at Fig. 4

[0013] Further, when the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used.

EX1016 (Riho) at [0013]

'060: Paper 24 (Reply) at 31-32; Paper 1 (Pet.) at 100-102
'160: Paper 24 (Reply) at 30-31; Paper 1 (Pet.) at 81-84

Samsung Electronics Co., Ltd.
Ex. 1067, p. 119

"[FIRST]/[SECOND] DATA CONDUITS"

GROUND 2 ('160), [1.E.2]-[1.E.3]

GROUNDS 4-5 ('060), [1.E.2]-[1.E.3]

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

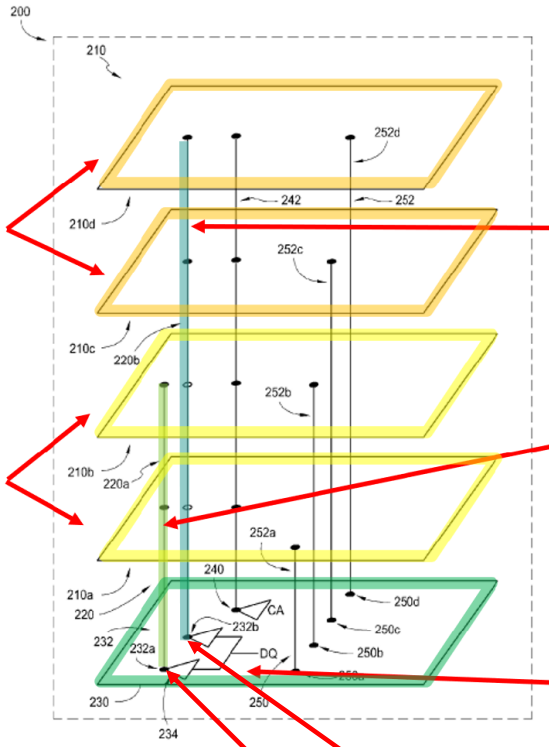
'060/'160 Claims: "*[first]/[second] data conduits*" to the same data terminals

'060 Patent, Claim 1:

a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

'160 Patent, Claim 1:

a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first



Array Dies 210c and 210d (orange)

Array Dies 210a and 210b (yellow)

Die interconnect 220b (teal)

Die Interconnect 220a (light green)

Drivers 234 (for data)

FIG. 2

The control die **230** may include a number of data conduits **232**, which includes data conduits **232***a* and **232***b*. Each of these data conduits **232** may be configured to transmit a data signal to a single die interconnect **220**. For example, the data

'060: EX1001 at 6:48-:51
'160: EX1001 at 6:51-:54

'060: Paper 1 (Pet.) at 11-14; EX1003 at ¶¶ 61-65
'160: Paper 1 (Pet.) at 11-16; EX1003 at ¶¶61-65

Samsung Electronics Co., Ltd.
Ex. 1067, p. 121

Riho + Rajan teaches a "fork-in-the-road" layout (e.g., for rank multiplication, like Ellsberry) with an interface that complies with JEDEC's bit-width

763. The claim also requires that the "*second data conduit*" is coupled to the same "*first terminal*" as the "*first data conduit.*" Such an arrangement of external data terminals in the control chip of Riho would have been obvious to a Skilled Artisan in view Rajan. *See, e.g., supra* ¶¶138-140 (rank multiplication), 683-692 (obviousness of combining Rajan and Riho, including emulating different number of ranks). For example, a Skilled Artisan would have been motivated to implement a 32-bit wide or narrower JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard

'060: EX1003 (Wolfe) at ¶ 763
'160: EX1003 (Wolfe) at ¶ 582

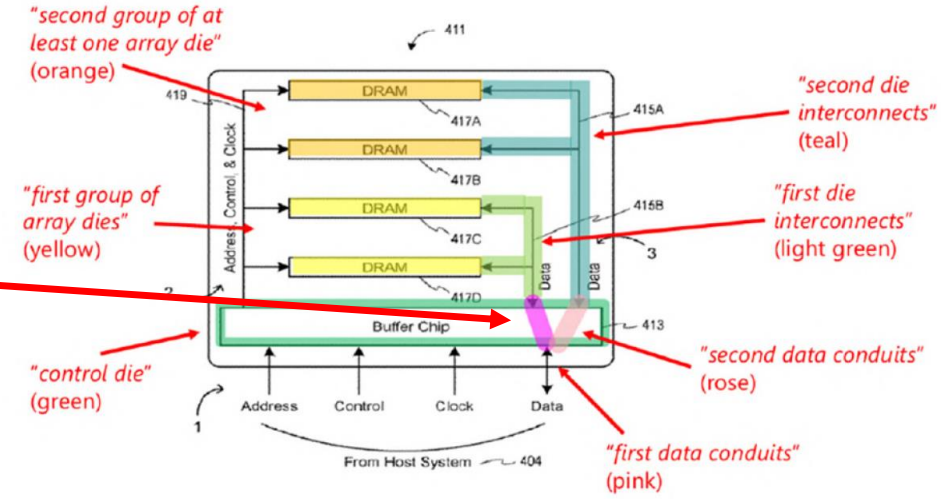


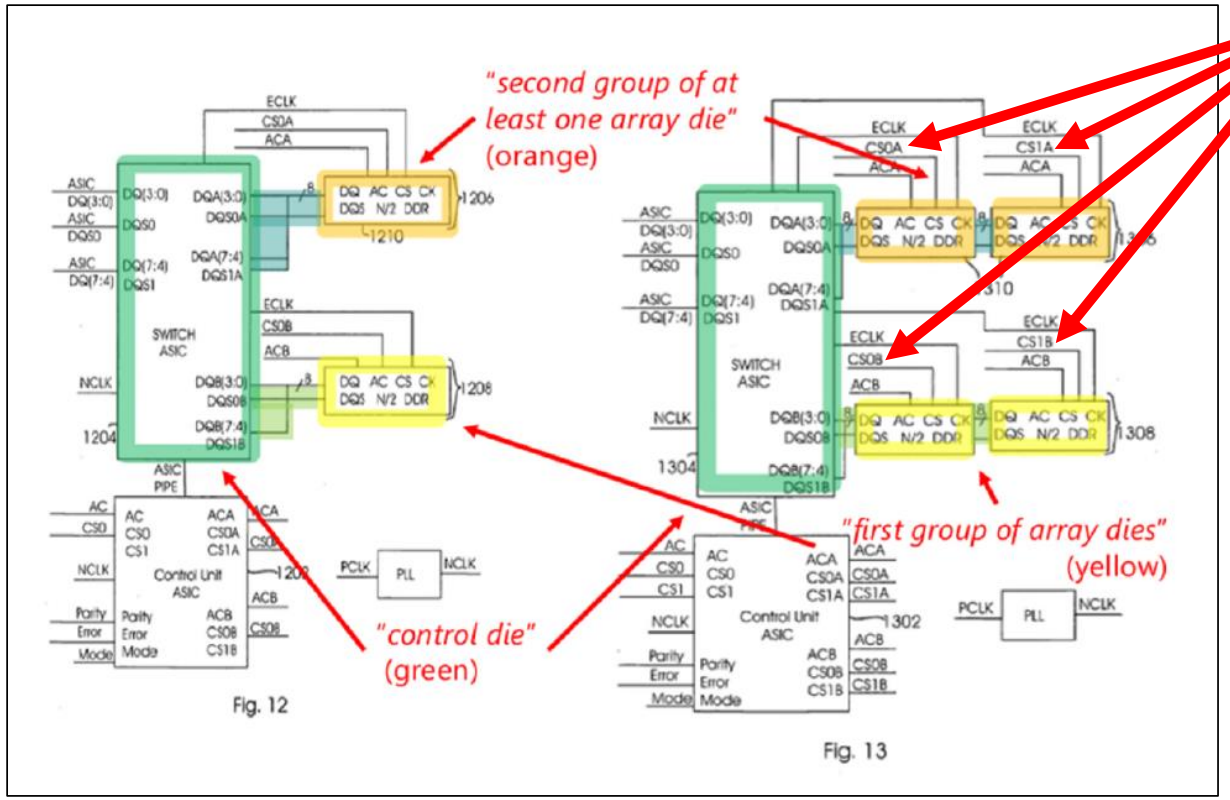
FIG. 4

EX1015 (Rajan) at Fig. 4

'060: Paper 24 (Reply) at 32-33; Paper 1 (Pet.) 103-106 (citing 8-11, 29-30)
'160: Paper 24 (Reply) at 31-32; Paper 1 (Pet.) 96-97 (citing 8-11, 31-32)

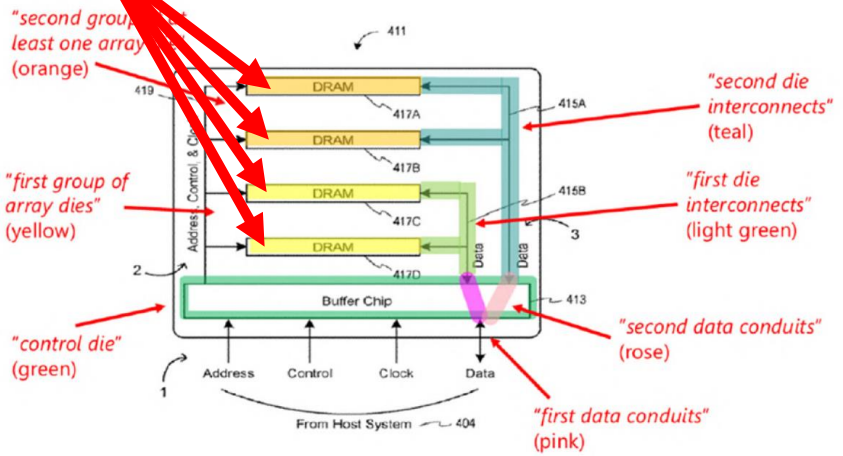
Samsung Electronics Co., Ltd.
Ex. 1067, p. 122

Rajan's "fork-in-the road" layout (on the right) was well known for rank multiplication as shown by Ellsberry (on the left)



EX1026 (Ellsberry) at Figs. 12-13

Four separate chip selects (CS0A, CS1A, CS0B, CS1B), one for each rank (four ranks total)



the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:34-:38 & Fig. 4

Rajan teaches rank multiplication with a separate "*chip select signal*" for each die in the stack

Rajan

the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

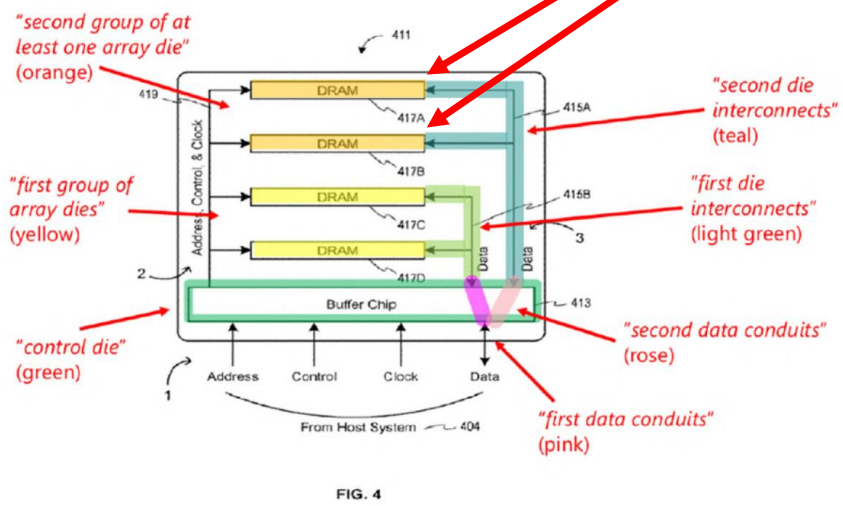


FIG. 4

EX1015 (Rajan) at 4:20-:24, 6:34-:38 & Fig.4

Q. So if 417A and 417B belonged to the same rank and they're connected to the same data wire, there potentially can be collision issues and current issues if they output data at the same time; is that right?

A. That is a big if. You would never let them output data at the same time if you made them in the same rank. You would -- you would put them in different places of the address space so only one or the other was operable.

Q. But if they are in the same rank, then they would be responding to the chip selection or read commands and output data simultaneously, wouldn't they? Isn't that what a rank of memory does?

A. I guess that's right. So you wouldn't put them in the same rank, then, unless you had some local modification to be able to do -- yeah. So you wouldn't put them in the same rank. Again, that is not what I relied on.



EX2025 (Wolfe) at 91:4-:22

Netlist's sur-reply raises new "strawman" argument that dies 417A/C and 417B/D in Rajan receive the same chip-select signal (when Rajan teaches separate chip-select signals)

Netlist's Sur-Reply

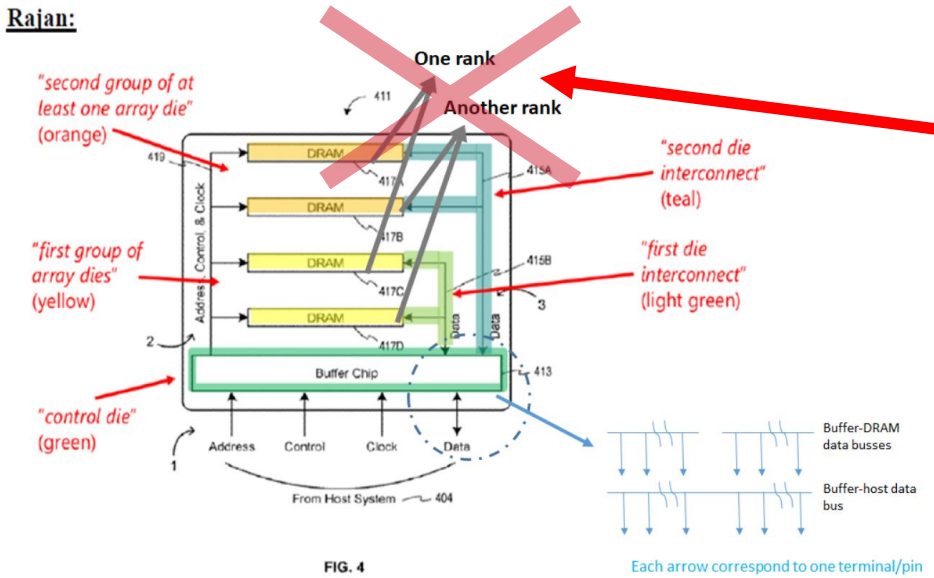
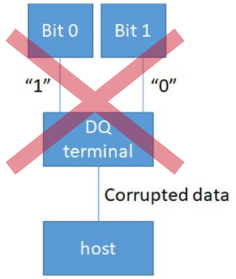


FIG. 4



'060: Paper 28 (Sur-reply) at 25-26
'160: Paper 28 (Sur-reply) at 24-25

Rajan (and JEDEC standard)

the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 4:20-:24, 6:34-:38 & Fig.4

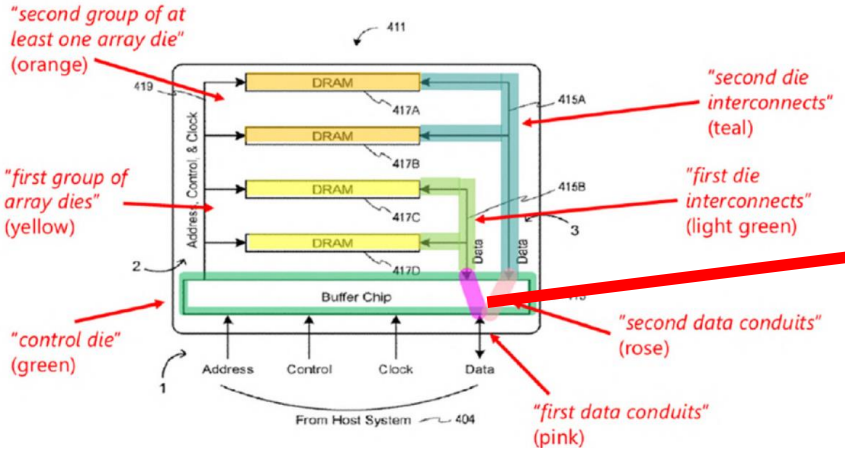
Symbol	Type	Function
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.

EX1019 at 13

'060: Paper 24 (Reply) at 32-33; Paper 1 (Pet.) 103-106 (citing 8-11, 29-30)
'160: Paper 24 (Reply) at 31-32; Paper 1 (Pet.) 96-97 (citing 8-11, 31-32)

Netlist's sur-reply raises another "strawman" argument that ignores Rajan's rank multiplication with fork-in-the-road data path

Rajan

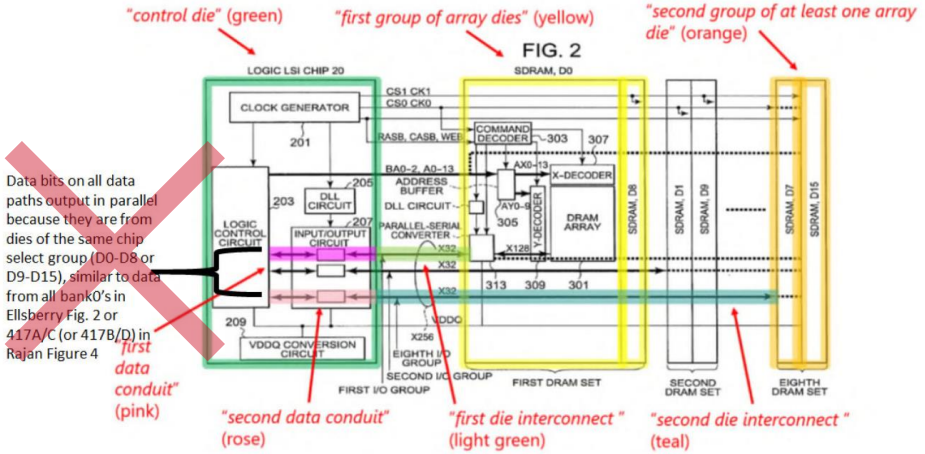


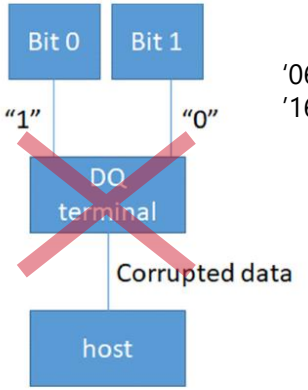
763. The claim also requires that the "*second data conduit*" is coupled to the same "*first terminal*" as the "*first data conduit*." Such an arrangement of external data terminals in the control chip of Riho would have been obvious to a Skilled Artisan in view Rajan. *See, e.g., supra* ¶¶138-140 (rank multiplication), 683-692 (obviousness of combining Rajan and Riho, including emulating different number of ranks). For example, a Skilled Artisan would have been motivated to implement a 32-bit wide or narrower JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard



'060: EX1003 (Wolfe) at ¶ 763
'160: EX1003 (Wolfe) at ¶ 582

Netlist's Sur-Reply





'060: Paper 28 (Sur-reply) at 26-27
'160: Paper 28 (Sur-reply) at 25-26

'060: Paper 24 (Reply) at 32-33; Paper 1 (Pet.) 103-106 (citing 8-11, 29-30)
'160: Paper 24 (Reply) at 31-32; Paper 1 (Pet.) 96-97 (citing 8-11, 31-32)

Samsung Electronics Co., Ltd.
Ex. 1067, p. 126

"ARRAY DIES" CLAIM CONSTRUCTION

NON-DRAM "ARRAY DIES" WERE OBVIOUS

GROUND 2 ('160)
GROUNDS 4-5 ('060)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

The Institution Decision correctly found that the construction of "*array dies*" has no impact on these IPRs

Thus, Patent Owner appears to argue that the district court's construction is that the claimed array dies are different from Rajan137's DRAM circuits 206A–D, not all DRAM circuits.

For the reasons explained below in section II.E.3.a, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction and also under that construction as interpreted by Patent Owner. Because the constructions advocated by Patent Owner do not impact the decision whether to institute, we need not resolve this claim construction issue at this time. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

'060: Paper 13 (ID) at 11;
see also '160: Paper 13 (ID) at 11

a) Element 1.c ("array dies")

. . . .

Furthermore, to the extent the claim excludes any DRAM chips at all, Riho explains that its disclosures are not limited to SDRAM. Ex. 1016 ¶ 135; *see* Reply 4. Patent Owner counters that Petitioner "relies on DRAM-based 'JEDEC standards' and textbooks . . . and compliance thereof to argue that the limitations are met." Sur-reply 3. Petitioner's contention, however, is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 93 (emphasis added); *see also* Pet. 94 ("Such a combination would have been well within a [person of ordinary skill in the art]'s level of skill since *emulating* a standard JEDEC interface was well-known, as demonstrated by Rajan . . . and the 060 Patent's admitted prior art . . . ." (emphasis added)). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

'060: Paper 13 (ID) at 16-17;
see also '160: Paper 13 (ID) at 17-18

'060: Paper 24 (Reply) at 1, 33-34
'160: Paper 24 (Reply) at 1, 33

Riho, like Rajan, discloses using non-DRAM "*array dies*"

Riho

[0135] It is apparent that the basic technical idea of this invention is not limited to the above-mentioned embodiments but may be modified and changed without departing from the scope and spirit of this invention. For example, although only the SDRAM chips are described in the embodiments, this invention is not limited thereto. This invention is applicable regardless of the function of chips and thus is applicable to any structure in which signal lines commonly provided in a plurality of chips continuously pass through from the uppermost chip to the lowermost chip. Further, the controlled chips (slave chips) are not limited to the SDRAMs and may be, for example, SRAMs or nonvolatile memories. Further, the circuit types are not limited to those disclosed in the embodiments. Although the control chip is disposed at the lowermost position in the embodiments, it may alternatively be disposed at the uppermost position.

EX1016 (Riho) at [0135]

Rajan

The physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc.

The physical memory circuits may be coupled to any type of memory module, such as: DIMM, R-DIMM, SO-DIMM, FB-DIMM, unbuffered DIMM, etc.

EX1015 (Rajan) at 15:3-:9

Using non-DRAM dies (e.g., Flash or SRAM) with a DRAM interface was known

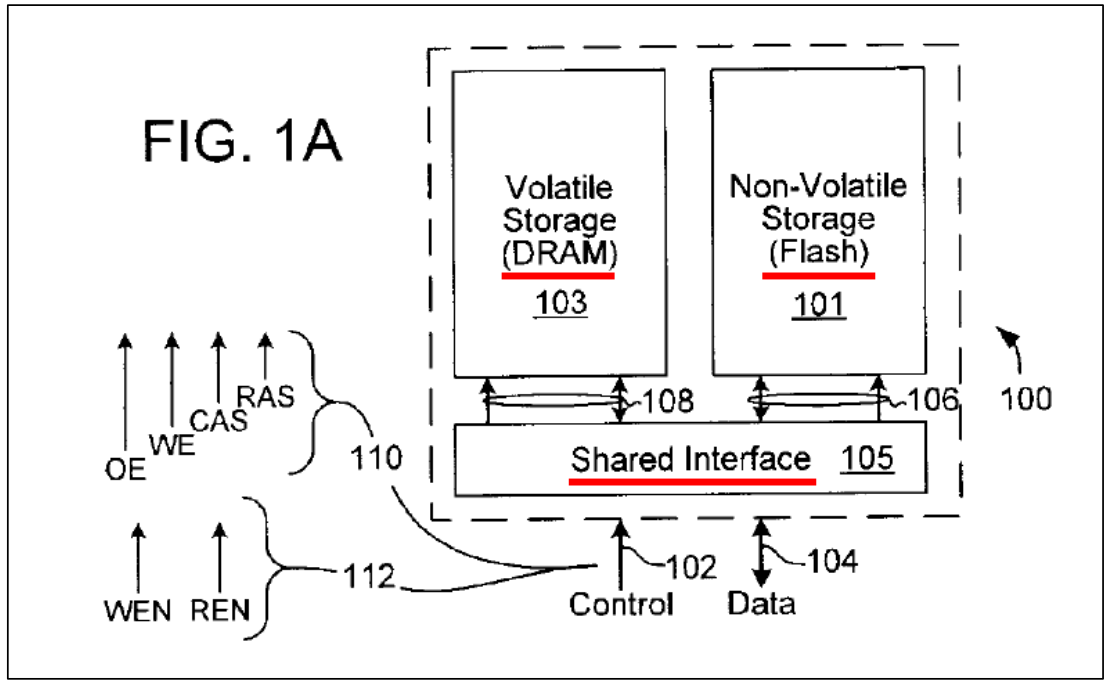
[0015] Internally, the shared interface **105** includes circuitry to forward control and data signals to the appropriate memory die, converting signals from the external data access protocol to an internal data access protocol as necessary. For example, in an embodiment having a DRAM external interface, control and data signals may be forwarded without change to a DRAM die (or with data serialization or deserialization to compensate for differences in path width between the internal and external data and/or control paths), but may be converted from DRAM format to Flash memory format before being forwarded to the Flash memory device. In general, any external protocol may be used to access the hybrid memory device, and any internal protocol or set of protocols may be used to control the volatile and non-volatile storage dice. Further, while only two storage dice are shown, multiple non-volatile storage dice and/or multiple volatile storage dice may be provided and selected by the shared interface circuitry based on incoming address and/or control signals. In such instances, the multiple volatile storage dice may be identical, or may be different in various regards, including storage capacity, storage technology (e.g., one or more SRAM dice may be packaged with one or more DRAM device), and/or the multiple non-volatile storage dice may be identical or mixed as where a Flash memory device is packaged with one or more ROM devices to form a system in package.

(19) **United States**
(12) **Patent Application Publication**
Best
(10) **Pub. No.: US 2010/0110748 A1**
(43) **Pub. Date: May 6, 2010**

(54) **HYBRID VOLATILE AND NON-VOLATILE MEMORY DEVICE**

Related U.S. Application Data

(60) Provisional application No. 60/912,321, filed on Apr. 17, 2007.



EX1060 (Best) at [0015] & Fig.1a; *see also* EX1052 (Brogioli) at 268:4-272:18; EX1061, 22-25 (Final Written Decision against Netlist applying Best)

'060: Paper 24 (Reply) at 13-15
'160: Paper 24 (Reply) at 16-18

Samsung Electronics Co., Ltd.
Ex. 1067, p. 130

Using non-DRAM dies (e.g., SRAM) with a different interface was known

Q. As shown at the bottom of page 1 of Exhibit 2053, the purpose of these slides is to teach students how to design a memory controller that can control asynchronous SRAM while making the SRAM look synchronous to the rest of the system, as explained in the middle of the slide; correct?

ATTORNEY ZHONG: Objection; form.

THE WITNESS: Just skimming through the slides. So in part, I'm on Slide 8. And it talks about at the first sentence, "The memory controller provides a 'synchronous' wrap around the SRAM."

So it looks like at least one of the things the memory controller is trying to do is provide a synchronous view of the underlying asynchronous SRAM.

EX1052 (Brogioli) at 243:11-244:2



Hardware Design with VHDL Design Example: SRAM ECE 443

External SRAM

A common type of system RAM is asynchronous static RAM (SRAM).

Access is more complicated than internal memory -- here data, address and control signals must be asserted in a specific order and held for a specific time.

A *memory controller* is usually used to shield the synchronous system from SRAM. It is responsible for generating the properly timed signals and making the SRAM look 'synchronous'.

EX2053 (SRAM) at 1

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Ex. 1067, p. 131

'060/'160 Patents admit DRAM package can have non-DRAM "*array dies*"

The memory package **200** can include any type of memory package. For example, the memory package **200** may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few. A memory module (not shown) may include one

'060: EX1001 at 5:1-:5
'160: EX1001 at 5:4-:8

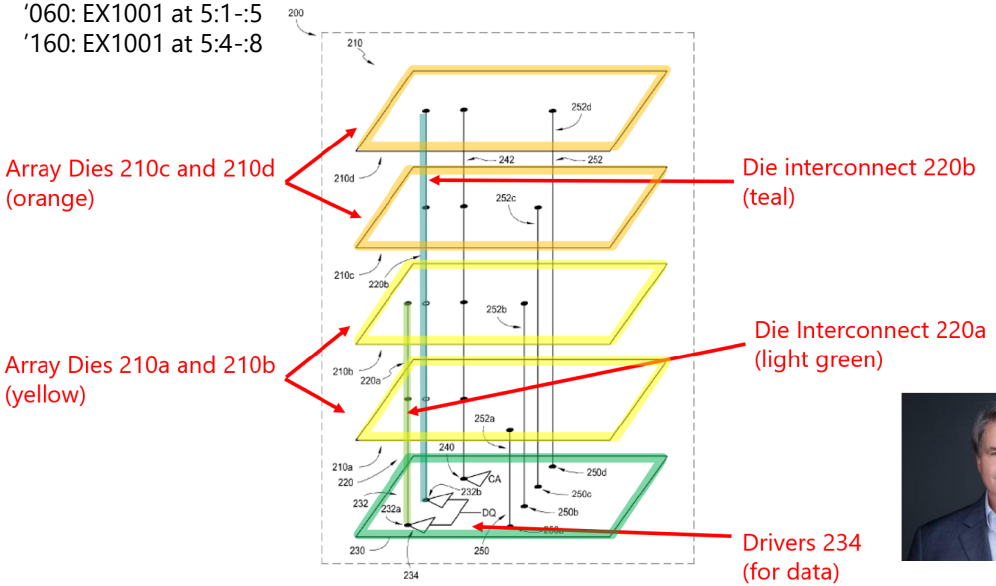


FIG. 2

receive data signals from the control die **822**. As with the array dies **210** and **310**, the array dies **824** may include any type of Random Access Memory (RAM) die. For example, the array dies **824** may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory

'060: EX1001 at 21:67-22:4
'160: EX1001 at 21:52-:56

Q. As we discussed earlier, the '060 and '160 patents, each of the ***array dies*** can be SDRAM or ***non-volatile memory*** or ***SRAM*** memory, all of which existed before the '160 and the '060 patents, correct?

A. Those types of memory technology, for example, SRAM or DRAM itself, were known prior to these patents; that's correct.

....

Q. So claim 10 of the '160 patent requires, among other things, a ***DRAM package*** compr[i]sing stacked ***array dies***, correct?

A. In compr[i]sing with the stacked ***arrays dies***, at the top of column 25.



EX1052 (Brogioli) at 339:2-:9, 262:23-263:2

'060: Paper 24 (Reply) at 1, 13-15
'160: Paper 24 (Reply) at 1, 16-18

Samsung Electronics Co., Ltd.
Ex. 1067, p. 132

"CHIP SELECT SIGNALS" CLAIM CONSTRUCTION

"CHIP SELECT SIGNALS" AND CONDUITS WERE OBVIOUS

GROUND 2 ('160), CLAIMS 15-16
GROUNDS 4-5 ('060), CLAIM 6

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

District Court: "*chip select signal*" for a given memory package has plain and ordinary meaning (which was well-known)

"chip select signal" ('060 Patent, Claims 11–14, 16–19, 20–21, 23–28)	Plain and ordinary meaning.
"chip select conduit" ('060 Patent, Claims 6, 11–14, 16–19)	Plain and ordinary meaning.

EX2004 at 35

JEDEC Standard No. 79-3C
Page 13
EX1019 at 13

Symbol	Type	Function
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.

Memory Systems

Cache, DRAM, Disk

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EX1022 at 319-20

This last bus, the chip-select bus, is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request. A value is asserted on the chip-select bus at the time of a request (e.g., read or write). The chip-select bus contains a separate wire for every rank of DRAM in the system. The chip-select signal passes over a wire unique to each small set of DRAMs and enables or disables the DRAMs in that rank so that they, respectively, either handle the request currently on the bus or ignore the request currently on the bus. Thus, only the DRAMs to which the request is directed handle the request. Even though all DRAMs in the system are connected to the same address and control busses and could, in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening.

'060: Paper 1 (Pet.) at 60-61; Paper 24 (Reply) at 1-2, 15
'160: Paper 1 (Pet.) at 74-75; Paper 24 (Reply) at 1-2, 18-19

JEDEC teaches separate "*chip select signal*" (red) to each stacked die (orange) sharing the data bus (green), thus avoiding collisions

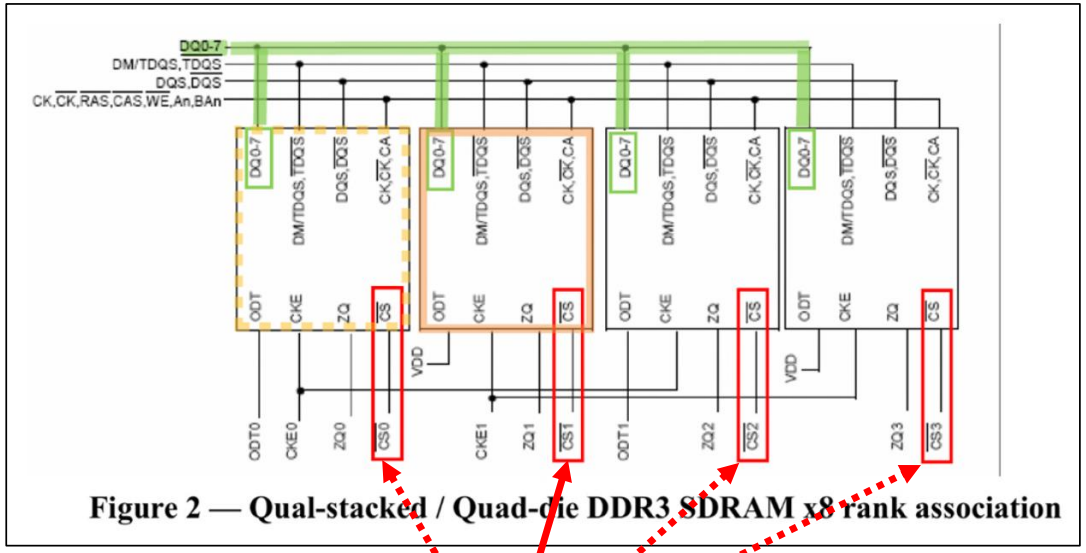


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

EX1019 at 12

Table 6 — Command Truth Table

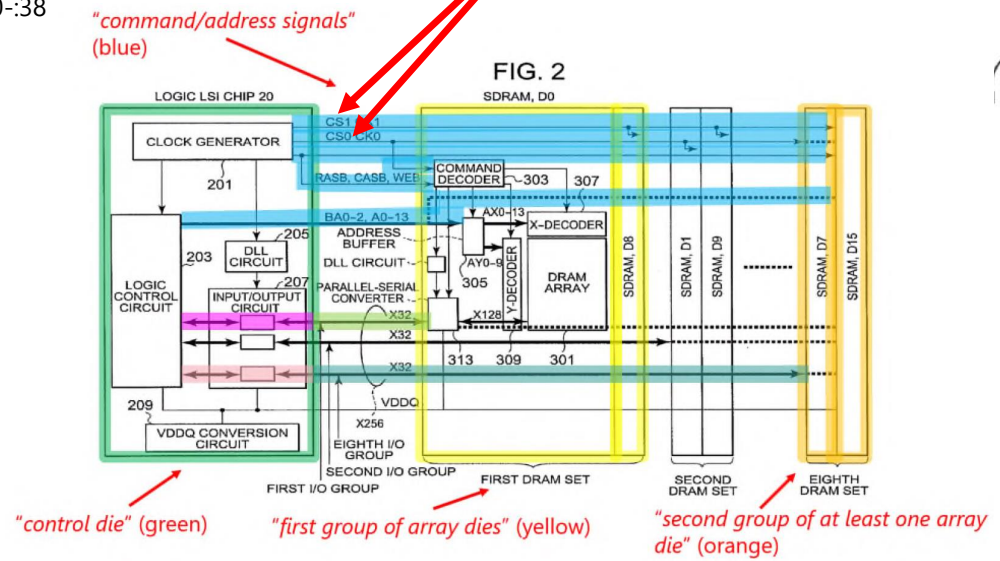
Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

EX1019 at 33

The combination of Riho and Rajan uses "separate chip select signals … to each of the DRAM chips," e.g., for rank multiplication

If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

EX1015 (Rajan) at 6:30-:38



EX1016 (Riho) at Fig. 2

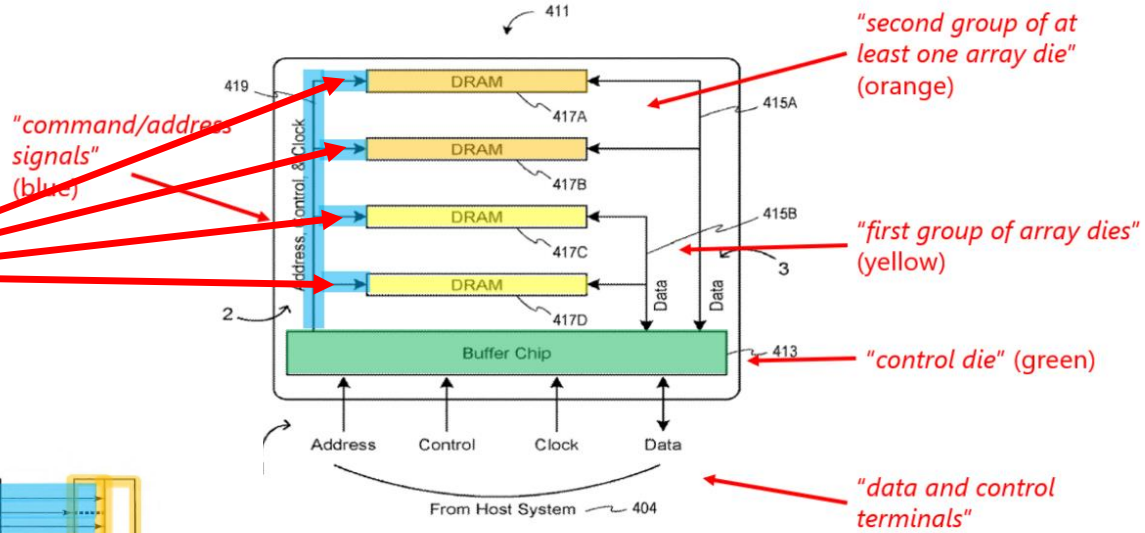


FIG. 4

EX1015 (Rajan) at Fig. 4

'060: Paper 1 (Pet.) at Pet. 91-94, 116-19; Paper 24 (Reply) at 34
'160: Paper 1 (Pet.) at Pet. 81-84, 119-23; Paper 24 (Reply) at 34

Samsung Electronics Co., Ltd.
Ex. 1067, p. 136

The Institution Decision correctly found that the Petitions demonstrated invalidity under the District Court's construction of "*chip select signals*"

2. "Chip Select Signals," "Chip Select Conduits"

Claims 6, 11–14, 16–19, and 29–34 recite "chip select signals" or "chip select conduits." Patent Owner argues that the district court construed the term "chip select signals" and associated "chip select conduits" to "exclude[] situations in which a chip select signal could enable multiple array dies at once" and contends that we should adopt this construction. Prelim. Resp. 23–24 (citing Ex. 2004, 33–34). For the reasons explained below in section II.E.6, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction, and, therefore, we need not further address this claim construction at this time.

'060: Paper 13 (ID) at 11-12, 20-21

Patent Owner argues that Riho has only two chip select signals, CS0CK0 and CS1CK1, each of which selects multiple dies, and, therefore, that Petitioner's contentions fail to meet the district court's constructions for "chip select signal" and "chip select conduit." Prelim. Resp. 47–48 (citing Ex. 1016 ¶ 37, Fig. 2). This argument, however, does not address Petitioner's contentions that Riho discloses additional signals sent to select particular dies, such as bank address signals BA0–2, and that it would have been obvious to "transmit[] separate chip-select signals through 'die interconnects' to select an 'array die.'" Pet. 116–18 (emphasis omitted). On this record, we are sufficiently persuaded that using separate chip select signals for each die was a known option for a person of ordinary skill in the art. *See* Ex. 1003 ¶ 830 (Dr. Wolfe's testimony that transmitting separate chip select signals was well known); *see also* Ex. 1015, 6:34–38 (Rajan's disclosure that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack"), *cited in* Pet. 61.

Samsung Electronics Co., Ltd.
Ex. 1067, p. 137

The Institution Decision correctly found that the Petitions demonstrated invalidity under the District Court's construction of "*chip select signals*"

record, we agree with this interpretation as applied to the "second chip select signals" term of claims 15 and 16 of the '160 patent because these claims recite "the second chip select signals having a number of chip select signals greater than the first chip select signals and *equal to a number of array dies in the plurality of array dies*" (emphasis added). Claims 15 and 16 recite that there are fewer "first chip selection signals" than "second chip selection signals," and, therefore, each of the "first chip selection signals" appears to apply to multiple array dies, which makes sense in the context of the "rank multiplication" of claims 15 and 16.

'160: Paper 13 (ID) at 11-12, 21-22

Petitioner argues that it would have been obvious to have the number of chip select signals equal the number of array dies based on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 120 (citing Ex. 1003 ¶¶ 784–791); *see also* Pet. 121 (asserting that "the JEDEC standard required separate chip-select signals for each stacked memory chip").

Patent Owner argues that Riho has only two chip select signals, CS0CK0 and CS1CK1, each of which selects multiple dies. Prelim. Resp. 48–49 (citing Ex. 1016 ¶ 37, Fig. 2). This argument, however, does not address Petitioner's contentions based on Rajan's disclosure of using separate chip select signals for each DRAM chip. Ex. 1015, 6:34–38.

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that the subject matter of claims 15 and 16 reciting "a number of chip select signals . . . equal to a number of array dies in the plurality of array dies" would have been obvious to a person of ordinary skill in the art based on the combination of Riho, Rajan, and Riho2.

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Ex. 1067, p. 138

"SECOND DRIVER SIZE BEING DIFFERENT FROM THE FIRST DRIVER SIZE"

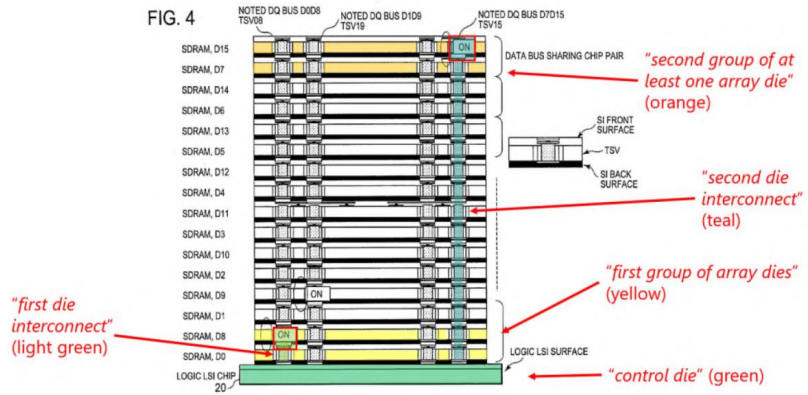
GROUND 2 ('160), [1.E.5]

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

Riho and Rajan + Riho2 — optimizes drivers given TSV's variations in capacitance/resistance

Riho's TSVs have varying impedance (capacitance, resistance) due to *manufacturing* and *position*

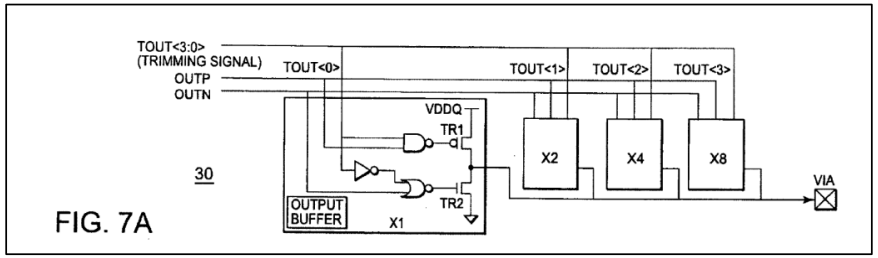


[0055] It is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in manufacturing processes (TSV forming process, bump forming process, and TSV-bump connection process). That is, TSVs formed in different manufac-

[0061] As is clear from FIG. **3**, the SDRAM chip located closer to the logic LSI chip **20** has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip **20** has a larger penetrating through resistance. Further, these penetrating through resistances

EX1016 (Riho) at [0055], [0061] & Fig.4

Riho2: optimizes drivers according to timing variations caused by capacitance/resistance



[0097] FIG. **7A** shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit **30**, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In

EX1018 (Riho2) at [0097] & Fig.7A

Riho2 teaches optimizing driver size due to any variation in capacitance/resistance, including from "number of stacked chip dies" or "number of groups"

[0096] The first to fourth memory modules have 2-Gbit, 4-Gbit, 8-Gbit, and 16-Gbit memory capacities, respectively. When the memory modules have mutually different numbers of stacked chip dies as in the first to fourth memory modules, it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another. In the fourth embodiment, a configuration is provided to optimize the output drive capacity of output buffers according to the number of stacked chip dies, and preferably according to the number of stacked chip dies and the number of groups, and a third ROM is further provided to control the drive capacity. This third ROM may be provided either in the inside of the semiconductor device (e.g. in the IO chip) forming a memory module, or in the outside of the semiconductor device.

EX1018 (Riho2) at [0096]

[0097] FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In

EX1018 (Riho2) at [0097]

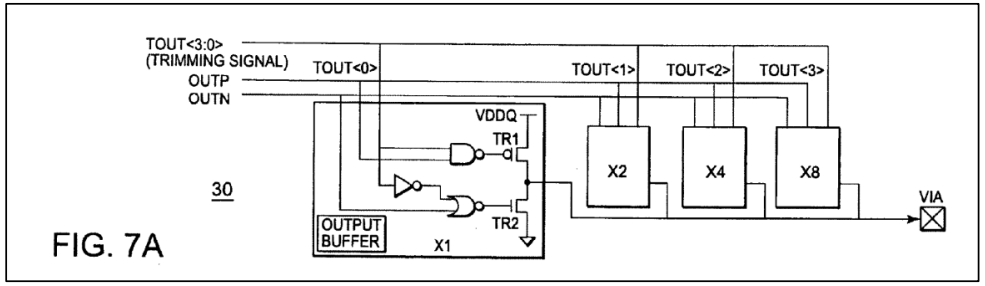


FIG. 7A

EX1018 (Riho2) at Fig. 7a

Optimizing drivers according to differences in die location was also well known (e.g., EX1039 (Ma))

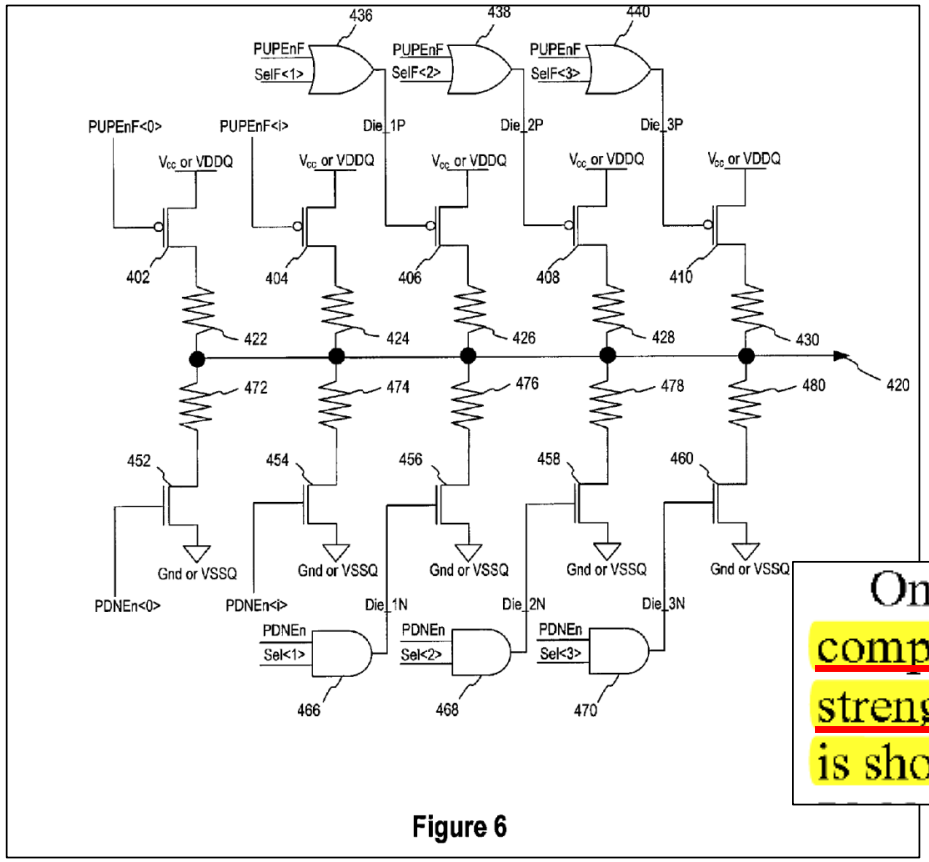


Figure 6

EX1039 (Ma) at Fig. 6

(57) **ABSTRACT**

Embodiments are described that compensate for a difference in a characteristic (e.g., of performance or operation) of a semiconductor device that is a function of the location of a die in a device. In one embodiment, a clock circuit may generate a clock signal having a timing that varies with the location of a die so that signals are coupled from the die to a substrate at the same time despite differences in the signal propagation time between the substrate and the various die. In other embodiments, for example, differences in the termination impedance or driver drive-strength resulting from differences in the location of a die in a stack may be compensated for. Other embodiments are also disclosed.

EX1039 (Ma) at Abstract

One embodiment of a compensation circuit **400** that may compensate for both termination impedance and drive strength variations resulting from differences in die location is shown in FIG. **6**. The circuit **400** may include a plurality of

EX1039 (Ma) at 7:46-:49

’160 DEPENDENT CLAIMS

GROUND 2 (’160)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

’160 Claims 2-3, 6-9

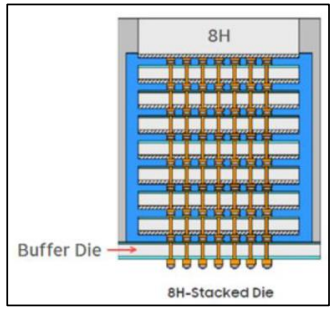
2. The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size.

3. The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

6. A memory package, comprising:
data terminals and control terminals;
stacked array dies including a first group of array dies and a second group of at least one array die;
first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
wherein the second die interconnects are longer than the first die interconnects, and wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

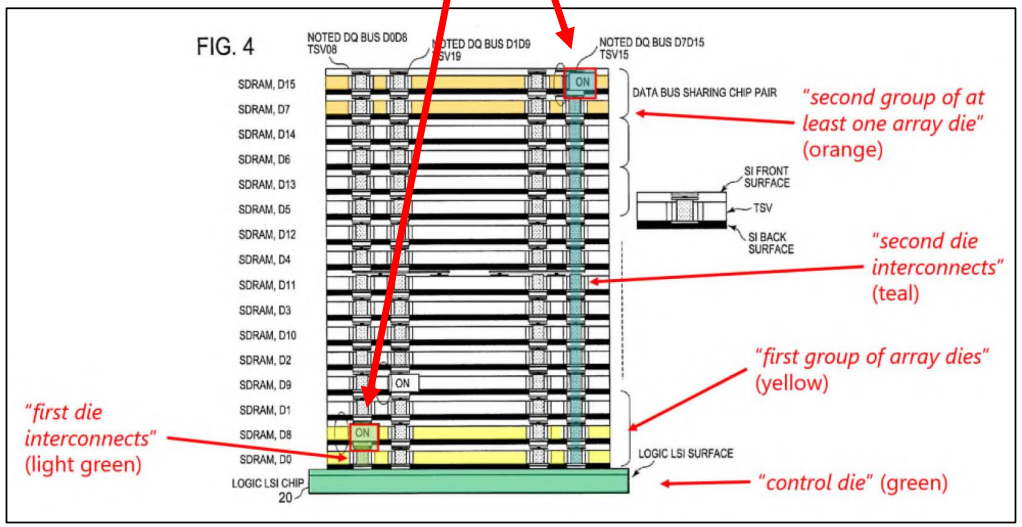
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Ex. 1067, p. 144

Netlist has interpreted claims 2-3 to merely require "different *distances* data signals have to travel to reach the respective dies in the stack," similar to Riho



group of at least one array die. The second driver size is different from the first driver size, for example, to account for the different distances data signals have to travel to reach the respective array dies in the stack.

EX1044 (Netlist's Complaint) at 65, 68



EX1016 (Riho) at Fig. 4

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Ex. 1067, p. 145

Riho + Rajan teaches TSVs of different lengths (e.g., to reduce load)

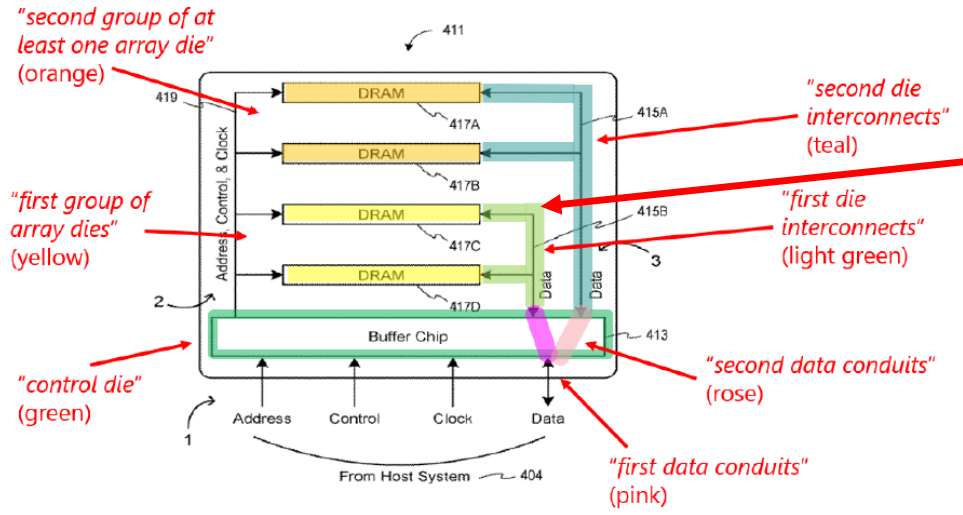


FIG. 4

EX1015 (Rajan) at Fig. 4

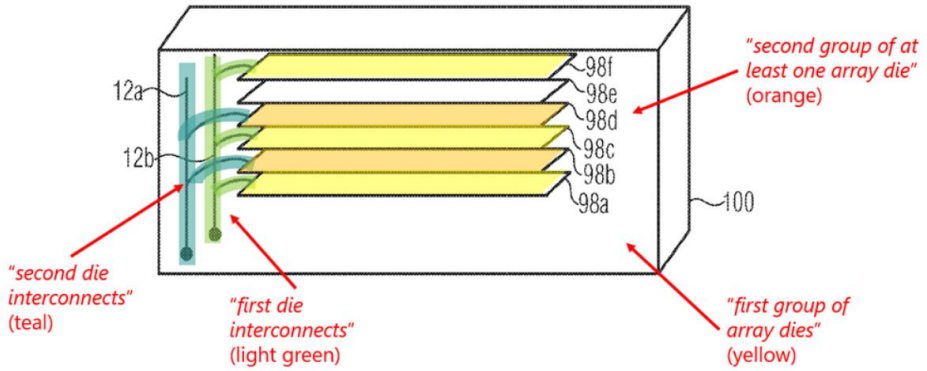
613. As illustrated in Fig. 4 of Rajan, the second die interconnects (teal) are longer than the first die interconnects (light green). A Skilled Artisan would have understood that, by using shorter die interconnects for the first group of memory devices as taught by Rajan, the load on those die interconnects is advantageously reduced. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled

'160: EX1003 (Wolfe) at ¶ 613



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Ex. 1067, p. 146

Ruckerbauer (EX1024) teaches "asymmetrical" stack of dies with "*electrical communication*" with some, but not all, dies



That is, within the memory stack **100**, a first sub set of memory dies is coupled to the first transfer data path **12***a* and a second sub set is coupled to the second transfer data path **12***b*. These different sub sets could, for example, be associated to different ranks within the stack **100**. The configura-

EX1024 (Ruckerbauer) at 9:14-:18 & Fig. 5

THE WITNESS: Again, we'd have to look at specific situations. But in both of -- both in the Riho reference and in the Ruckerbauer reference, they are both very explicit that the point of the configuration is to eliminate the electrical communication with some of the die while supporting the electrical communication with other die.

EX2025 (Wolfe) at 112:5-:18



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Ex. 1067, p. 147

CLAIM 7 OF ’060 PATENT

GROUND 4-5 (’060)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

For claim 7 in Ground 4, Netlist just refers back to Ground 2

POR:

> **E. Claim 7**
>
> Petitioner's analysis for claim 7 for Ground 4 largely tracks that for Ground 2. *Compare* Pet. 83 *with* Pet. 119-120. For the same reasons as stated for Ground 2, Claim 7 is not obvious in Ground 4. Brogioli, ¶¶287, 205-208.

'060: Paper 20 (POR) at 82

Reply:

> **5. Grounds 4-5 render obvious claim 7 (POR 82)**
>
> For claim 7 in Ground 4, Netlist refers back to its arguments for Ground 2, POR 82, which are incorrect as explained above (pp.16-18).

'060: Paper 24 (Reply) at 34

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Ex. 1067, p. 149

GROUND 5 (‘060 PATENT)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

For Ground 5, Netlist repeats its erroneous argument about Riho's TSVs being "in electrical communication with every die in the stack"

POR:

> **F. Ground 5**
>
> As explained above, in Riho, each TSV is in electrical communication with every die in the stack. As such, the drivers used to drive signals along the TSVs need to have at least the size of, and not less than the size of a driver "sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation." *Contra* Pet. 141-42;

'060: Paper 20 (POR) at 83

Reply:

> **6. Ground 5 (POR 83)**
>
> For Ground 5, Netlist repeats its argument that in Riho "each TSV is in electrical communication with every die in the stack," POR 83, which is incorrect as explained above (pp.20-32).

'060: Paper 24 (Reply) at 34

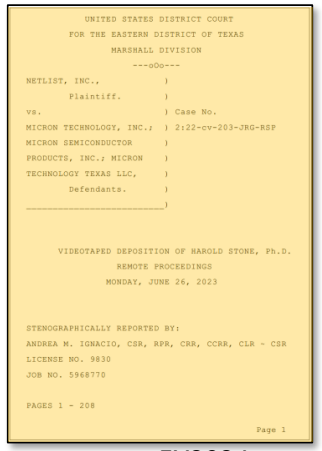
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Ex. 1067, p. 151

MOTION TO EXCLUDE 04

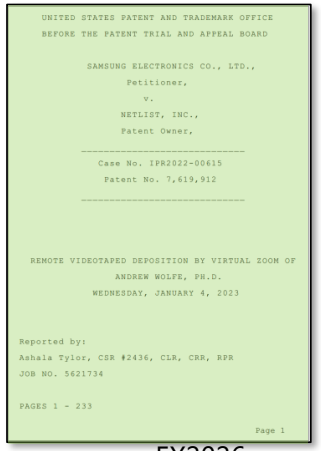
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

BAKER BOTTS

EX2024, 2026–2029, and 2031 are improper hearsay


UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
---oOo---
NETLIST, INC., Plaintiff. vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.) Case No. 2:22-cv-203-JRG-RSP
VIDEOTAPED DEPOSITION OF HAROLD STONE, Ph.D.
REMOTE PROCEEDINGS
MONDAY, JUNE 26, 2023
STENOGRAPHICALLY REPORTED BY:
ANDREA M. IGNACIO, CSR, RPR, CRR, CCRR, CLR - CSR
LICENSE NO. 9830
JOB NO. 5968770
PAGES 1 - 208
Page 1

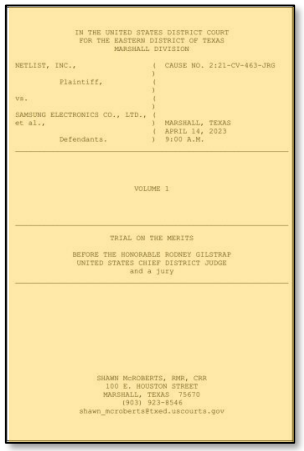
EX2024


UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD
SAMSUNG ELECTRONICS CO., LTD., Petitioner, v. NETLIST, INC., Patent Owner,
Case No. IPR2022-00615
Patent No. 7,619,912
REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF ANDREW WOLFE, PH.D.
WEDNESDAY, JANUARY 4, 2023
Reported by:
Ashala Tylor, CSR #2436, CLR, CRR, RPR
JOB NO. 5621734
PAGES 1 - 233
Page 1

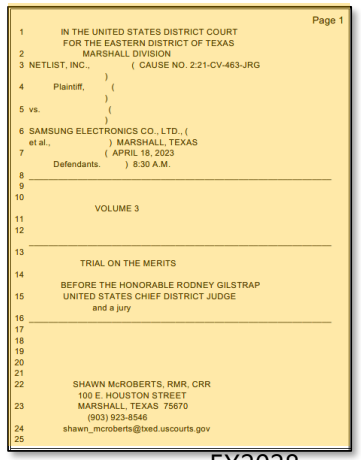
EX2026

Statements offered for the truth of the matter asserted made outside this proceeding:

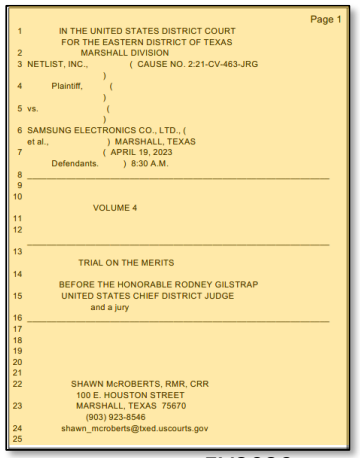
- District court proceeding
- A different IPR proceeding


IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants. (CAUSE NO. 2:21-CV-463-JRG) MARSHALL, TEXAS (APRIL 14, 2023) 9:00 A.M.
VOLUME 1
TRIAL ON THE MERITS
BEFORE THE HONORABLE RODNEY GILSTRAP
UNITED STATES CHIEF DISTRICT JUDGE
and a jury
SHAWN McROBERTS, RMR, CRR
100 E. HOUSTON STREET
MARSHALL, TEXAS 75670
(903) 923-8546
shawn_mcroberts@txed.uscourts.gov

EX2027


Page 1
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VOLUME 3
TRIAL ON THE MERITS
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UNITED STATES CHIEF DISTRICT JUDGE
and a jury
SHAWN McROBERTS, RMR, CRR
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EX2028


Page 1
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VOLUME 4
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UNITED STATES CHIEF DISTRICT JUDGE
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SHAWN McROBERTS, RMR, CRR
100 E. HOUSTON STREET
MARSHALL, TEXAS 75670
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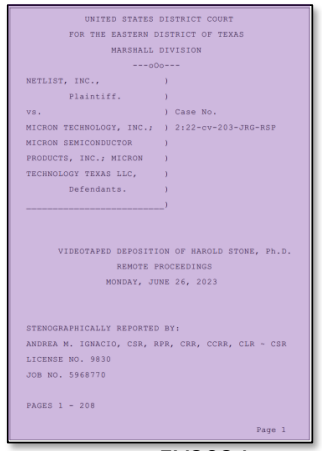
EX2029


NETLIST, INC., Plaintiff
vs.
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants
Scott Milton
April 14, 2023
NETLIST
PDX2.1

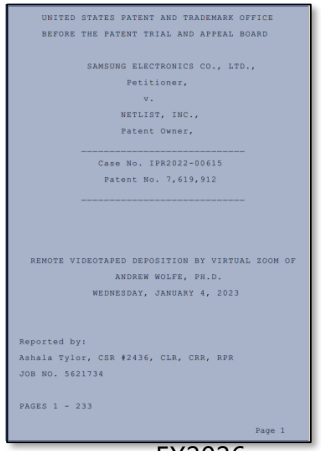
EX2031

Paper 34 (Motion to Exclude)
Paper 36 (Reply to Motion to Exclude)

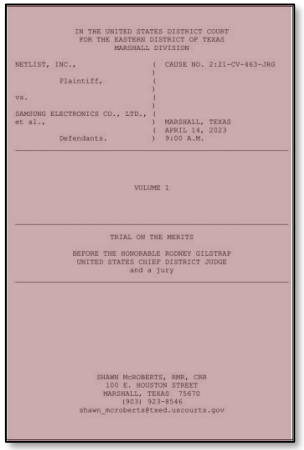
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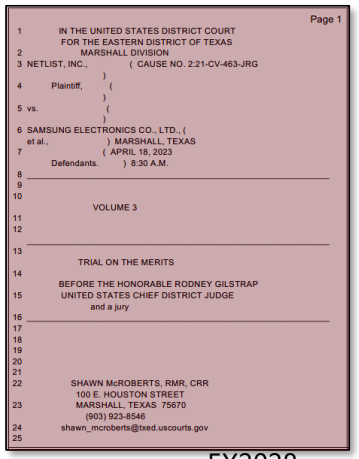
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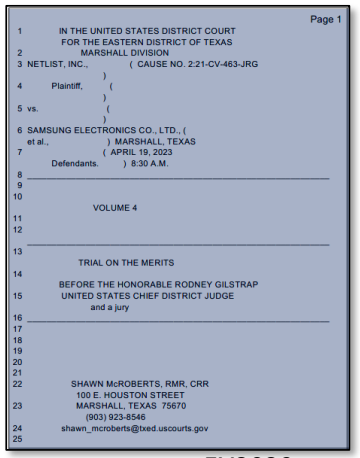
EX2026


IN THE UNITED STATES DISTRICT COURT
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EX2027


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EX2028


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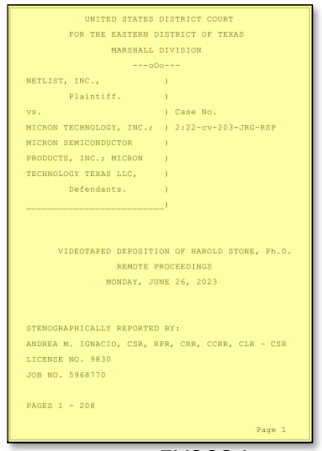
EX2029


NETLIST, INC., Plaintiff
vs.
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants
Scott Milton
April 14, 2023
NETLIST
PDX2.1

EX2031

- **Not subject to FRE 801(d) exemptions:**
  - Micron expert witness (Stone)
  - Netlist witnesses (Milton and Hyun Lee)
  - Netlist demonstratives
  - Samsung *expert* witnesses in other cases (Wolfe and Robins)
    - *Not subject to 801(d)(2) — not "made by [Petitioner's] agent or employee on a matter within the scope of that relationship and while it existed." See, e.g., HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489–90 (5th Cir. 2021)

EX2024, 2026–2029, and 2031 are improper hearsay



UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION
---oOo---

NETLIST, INC., Plaintiff. vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.) Case No. 2:22-cv-203-JRG-RSP

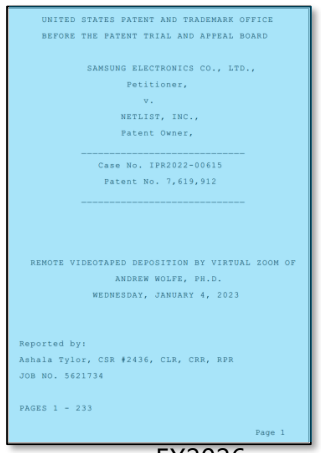
VIDEOTAPED DEPOSITION OF HAROLD STONE, Ph.D.
REMOTE PROCEEDINGS
MONDAY, JUNE 26, 2023

STENOGRAPHICALLY REPORTED BY:
ANDREA M. IGNACIO, CSR, RPR, CRR, CCRR, CLR - CSR
LICENSE NO. 9830
JOB NO. 5968770

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EX2024



UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,
v.
NETLIST, INC.,
Patent Owner,

Case No. IPR2022-00615
Patent No. 7,619,912

REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF
ANDREW WOLFE, PH.D.
WEDNESDAY, JANUARY 4, 2023

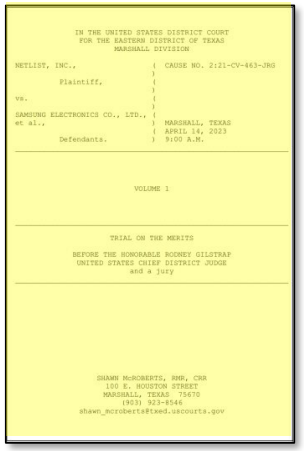
Reported by:
Ashala Tyler, CSR #2436, CLR, CRR, RPR
JOB NO. 5621734

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Page 1

EX2026

- **No exception applies:**
  - FRE 804 unavailable because:
    - Netlist made no attempt to bring witness
    - Witness testified in this proceeding
  - FRE 807 also unavailable because (i) insufficient guarantees of trustworthiness, (ii) not more probative than other available evidence, (iii) absence of any interest of justice



IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants. (CAUSE NO. 2:21-CV-463-JRG) MARSHALL, TEXAS (APRIL 14, 2023) 9:00 A.M.

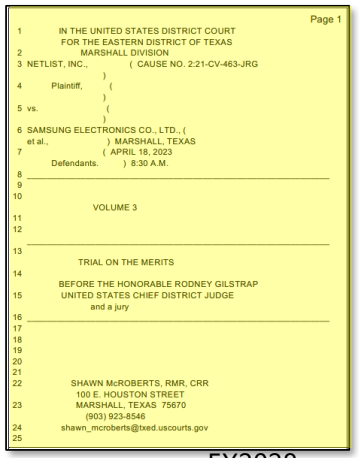
VOLUME 1

TRIAL ON THE MERITS

BEFORE THE HONORABLE RODNEY GILSTRAP
UNITED STATES CHIEF DISTRICT JUDGE
and a jury

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EX2027



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IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants. (CAUSE NO. 2:21-CV-463-JRG) MARSHALL, TEXAS (APRIL 18, 2023) 8:30 A.M.

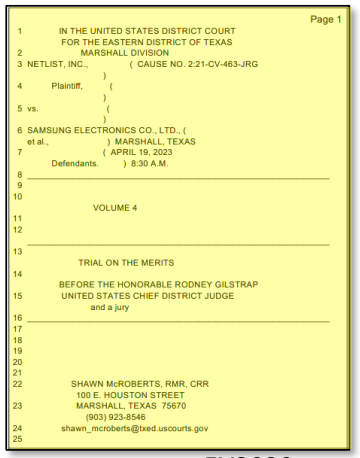
VOLUME 3

TRIAL ON THE MERITS

BEFORE THE HONORABLE RODNEY GILSTRAP
UNITED STATES CHIEF DISTRICT JUDGE
and a jury

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EX2028



Page 1

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants. (CAUSE NO. 2:21-CV-463-JRG) MARSHALL, TEXAS (APRIL 19, 2023) 8:30 A.M.

VOLUME 4

TRIAL ON THE MERITS

BEFORE THE HONORABLE RODNEY GILSTRAP
UNITED STATES CHIEF DISTRICT JUDGE
and a jury

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EX2029



NETLIST, INC.,
Plaintiff

vs.

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.,
Defendants

Scott Milton

April 14, 2023

NETLIST

PDX2.1

EX2031

EX2024 and 2026–2031 are irrelevant and lack probative value

- **Evidence already of record in this proceeding is more relevant and more reliable**
  - Expert declarations (EX1003 (Wolfe Decl.), EX2023 (Brogioli Decl.)
  - Expert testimony (EX2025 (Wolfe Depo.), EX1052 (Brogioli Depo.)
- **These exhibits are from different proceedings that did not address the same patentability grounds**

Reply to Netlist's opposition brief

1. **Testimony by experts (*e.g.*, Drs. Stone, Wolfe, Robins) regarding the meaning of terms of art is proffered for the truth of the matter asserted.**
2. **Samsung is not Micron, rendering Netlist's FRE 801(d)(2)(B)–(D) arguments inapplicable.**
3. **The Fifth Circuit has explicitly rejected Netlist's arguments about expert testimony.**

In *Fox v. Taylor Diving & Salvage Co.*, 694 F.2d 1349, 1355-56 (5th Cir. 1983), the Fifth Circuit found that, where a party allowed its expert to testify without objection in a prior trial, the trial testimony became binding on the party. Here, Petitioner at most objected to the form of the questions, and in many cases, did not object at all. Thus, the testimony should be treated as party statements.

Paper 35 (Netlist Opp'n to Motion to Exclude) at 2.

"Those cases where we have allowed expert testimony to serve as a party admission have been limited to circumstances where the expert was an agent of the opposing party or where the expert's statements or reports were **prepared for the very case in which admission was sought.**"

HTC Corp. v. Telefonaktiebolaget LM Ericsson, 12 F.4th 476, 489–90 (5th Cir. 2021) (emphasis added) (distinguishing *Fox v. Taylor Diving & Salvage Co.*, 694 F.2d 1349, 1355 (5th Cir. 1983)).

4. **37 C.F.R. § 42.51(b)(1)(iii) is a discovery rule, not an admissibility rule.**

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DEMONSTRATIVE EXHIBIT – NOT EVIDENCE