**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

| | | |
|---|---|---|
| NETLIST, INC., | § | |
| | § | |
| *Plaintiff*, | § | |
| | § | |
| v. | § | |
| | § | CIVIL ACTION NO. 2:21-CV-00463-JRG |
| SAMSUNG ELECTRONICS CO., LTD., | § | |
| SAMSUNG ELECTRONICS AMERICA, | § | |
| INC., and SAMSUNG SEMICONDUCTOR, | § | |
| INC., | § | |
| | § | |
| *Defendants*. | § | |

**CLAIM CONSTRUCTION ORDER**

Netlist asserts claims from six patents relating to computer memory against Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (together, "Samsung"). U.S. Patent 10,949,339, entitled "Memory Module with Controlled Byte-Wise Buffers," relates to improving the performance and memory capacity of memory subsystems. '339 Patent at 1:18–23. U.S. Patent 10,860,506, entitled "Memory Module With Timing-Controlled Data Buffering," generally concerns "multi-rank memory modules and methods of operation." '506 Patent at 1:37–39. U.S. Patents 11,016,918 and 11,232,054, which are related and share a common specification, concern computer memory devices that use different types of memory. '918 Patent at 1:66–2:2; *see also* '054 Patent at 1:66–2:2. Finally, U.S. Patents 8,787,060 and 9,318,160, which are related and share a common specification, concern "systems and methods for reducing the load of drivers of memory packages included on memory modules." '060 Patent at 1:19–21; *see also* '160 Patent at 1:21–23.

The parties dispute the proper constructions of fourteen terms from the patents. Having considered the parties' briefing, along with arguments of counsel during the November 4, 2022 *Markman* Hearing, the Court resolves the disputes as follows.

## I. LEGAL STANDARDS

### A. Generally

"'[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure-Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g.*, *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, "is not an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, "[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims . . . ." *Id.* A court need not "repeat or restate every claim term in order to comply with the ruling that claim construction is for the court." *Id.*

When construing claims, "[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as

of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."). But for claim terms with less-apparent meanings, courts consider "'those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean[,] [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.'" *Phillips*, 415 F.3d at 1314 (quoting *Innova*, 381 F.3d at 1116).

## II. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the

technology, and the education of workers active in the field. *Id.* Importantly, "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Here, neither party proffers a level of ordinary skill in the art in its briefing. Elsewhere, however, Samsung asserted:

> [a] POSITA in the field of the 054 Patent in 2008 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. . . . Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

Pet. for *Inter Partes* Review of U.S. Patent No. 11,232,054, Dkt. No. 82-1 at 7–8. *See also* Pet. for *Inter Partes* Review of U.S. Patent No. 11,016,918, Dkt. No. 87-2 at 8–9; Pet. for *Inter Partes* Review of U.S. Patent No. 9,318,160, Dkt. No. 87-3 at 5 (similar); Pet. for *Inter Partes* Review of U.S. Patent No. 10,949,339, Dkt. No. 87-3 at 5 (similar).

## III. U.S. PATENT 10,949,339

### A. Background

According to the '339 Patent, designing memory subsystems requires balancing memory density, power dissipation, speed, and cost. '339 Patent at 2:5–7. Adjusting one of these may

negatively affect the others. *Id.* at 2:7–12. For example, the ’339 Patent notes two ways of increasing memory space: (1) an address decoding scheme, and (2) combining chip-select and address signals “to increase the number of physically addressable memory spaces . . . .” *Id.* at 5: 15–25. But because both ways add memory chips, the system outputs have a heavier load. That, in turn, slows the system and increases the necessary power. *Id.* at 4:27–33. Moreover, it results in uneven propagation delay, which can negatively affect internal timing of accessing memory. *Id.* at 4:38–44. As examples, FIGS. 1–2 show prior-art systems in which differences in trace lengths or complexity of the memory controllers affect system speed.

As shown in FIG. 3A (below), the ’339 Patent teaches arranging the memory devices 412 in multiple ranks A, B, C, D, and a module controller 430 configured to receive and register input control signals from a memory controller 420. The address and control signals select one of the multiple ranks to perform a read or write operation. In response, the module controller 430 outputs a set of control signals that drive data signals between the memory controller 420 and the selected rank. *See generally id.* fig.3A.

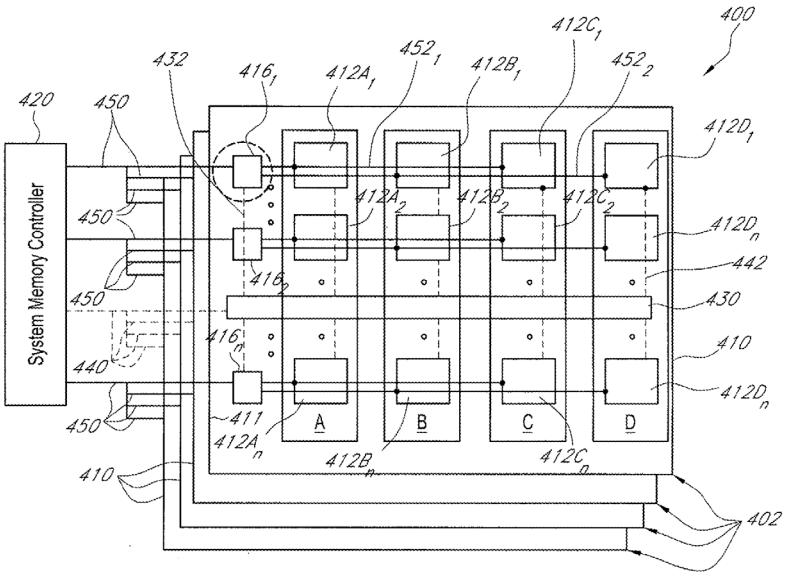


FIG. 3A

Based on signals received from the control circuit 430, the data transmission circuits 416 selectively enable or disable access to the memory devices 412. For example, whereas a set of control signals from the memory controller 420 may address two memory devices (e.g., $412A_1$ and $412B_1$), only one of those devices might be enabled depending on the state of the associated data transmission circuit $416_1$. In FIG. 3A, the data transmission circuit $416_1$ enables or disables memory devices $412A_1$ and $412C_1$ together and memory devices $412B_1$ and $412D_1$ together.

For claim construction, the relevant limitations are the module controller 430 and the data transmission circuits 416, which the claims refer to as "byte-wise buffers". Regarding those limitations, Claim 1 recites a memory module comprising:

> a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and
>
> a plurality of byte-wise buffers . . . configured to receive the module control signals, wherein each respective byte-wise buffer . . . has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side in accordance with a latency parameter . . . ; [and]
>
> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is

> enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period.

*Id.* at 19:40–61.

### B. The Disputed Terms From the '339 Patent

#### 1. the "drive" claim terms ('339 Patent, Claims 1, 11, 19, 27)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| plain and ordinary meaning | "each respective byte-wise buffer further includes logic configurable to, in response to the module control signals, ***activate*** the byte-wise data path connected to a first DDR DRAM device (in a first N-bit-wide rank), and ***disable*** the byte-wise data path connected to a second DDR DRAM device (in a second N-bit-wide rank), to cause a respective byte-wise section of the N-bit wide write data associated with the memory operation to be ***sent*** from the first side to the first DDR DRAM device ***along the activated*** byte-wise data path and ***not sent*** to the second DDR DRAM device ***along the disabled*** byte-wise data path during the first time period in accordance with a latency parameter" |

Claim 1 recites a module controller and a plurality of byte-wise buffers, each of which has a first side connected to data lines and a second side connected to physical memory. '339 Patent at 19:40–52; *see also id.* at 21:66–22:5 (Claim 11); *id.* at 24:18–29 (Claim 19); *id.* at 26:17–26 (Claim 27). The claims also require logic configurable to enable a data path to "actively drive" write data from one side of the buffer to the other side. *See, e.g.*, *id.* at 19:53–67 (reciting logic configurable to drive write data from the first side to the second side).

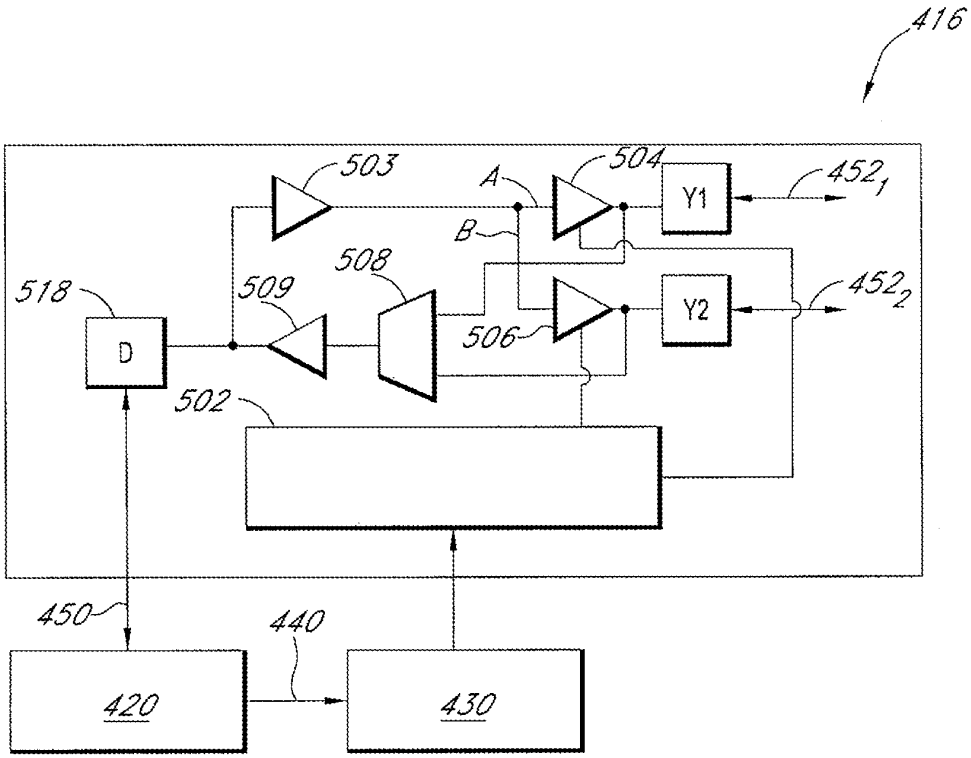


FIG. 5

This claim language is best understood with respect to FIG. 5 (above). As the patent explains:

> For a write operation . . . the control circuit 430, in one embodiment, provides enable control signals to the control logic circuitry 502 of each data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data. Accordingly, when the control logic circuitry 502 receives, for example, an "enable A" signal, a first tristate buffer 504 in path A is enabled and actively drives the data value on its output, while a second tristate buffer 506 in path B is disabled with its output in a high impedance condition. In this state, the data transmission circuit 416 allows the data to be directed along path A to a first terminal Y1, which is connected to and communicates only with the first group of the memory devices 412, e.g., those in ranks A and C. Similarly, if an "enable B" signal is received, the first tristate 504 opens path A and the second tristate 506 closes path B, thus directing the data to a second terminal Y2, which is connected to and communicates only with the second group of the memory devices 412, e.g., those in ranks B and D.

*Id.* at 16:7–25. To simplify, depending on to where the data will be written, the control logic circuitry 502 selects either Path A or Path B and disables the other path by commanding the associated tristate buffer into a high-impedance state.

The parties' dispute centers on what it means to "drive" data from one side of the buffer to the other. More specifically, it concerns whether, when one path is enabled, the other paths *must* be disabled. Samsung contends the claims require only one path be enabled at a time, for two reasons. First, this is how FIG. 5 works. Dkt. No. 82 at 21–22. Second, during prosecution, the applicants argued the "fork"—i.e., one path or the other, but not both—distinguished their invention from the prior art. *Id.* at 22–23. Netlist argues the inventors never disclaimed the plain meaning of the claim language to limit the scope of the claims as suggested by Samsung.

The Court agrees with Samsung based on both the prosecution history and the specification. During prosecution, the applicants wrote:

> This claimed limitation . . . is about controlling the data paths between the memory devices and the bus interface so that the data paths are open for a time period to allow data to be driven between the memory devices and the memory controller. *This allows the data paths to be kept closed to isolate the memory devices from the bus interface when the memory module is not communicating data with the memory controller.*

Resp. to Office Action (Mar. 25, 2020), Dkt. No. 82-6 at 16 (emphasis added). In other words, the claimed invention, unlike the cited prior art, is about selectively opening otherwise closed data paths. *See also, e.g.*, Resp. to Final Office Action (June 23, 2020), Dkt. No. 82-7 at 15–16 (arguing the prior art teaches "write data is sent *to both ports A and B* of the switch 206/208"; thus, the prior art's statement "that the control unit 204 'causes Port B to be activated and Port A to be disabled' cannot possibly mean activating a data path through Port B and disabling a data path through Port A" (emphasis in original)); Amendment & Req. for Continued Examination, Dkt. No. 82-8 at 21

(explaining "[t]he data paths can thus be kept disabled to isolate the memory devices from the bus interface, or vice versa, when the memory module is not communicating data with the memory controller"); *id.* at 18 (arguing the prior art "reject[s] the idea of using switches to select a data line" and "teaches away from switching data paths"). Although the applications remarks are phrased in terms of "capability" and what the invention "allows," a skilled artisan would nonetheless understand those statements as characterizing the applicants' invention.

This is consistent with the specification. When describing the technological problem to be solved, the patent emphasizes reducing the load at the outputs of the memory devices. '339 Patent at 4:27–31. In addition, the sole embodiment describing path selection during a write operation disables one path within the buffers when the other path is enabled. *Id.* at 16:1–18 ("the control logic circuitry 502 selects either path A or path B to direct the data"); *id.* at 17:30–44 (the data transmission circuits "enabl[e] the proper data paths between the system memory controller 420 and the targeted or selected memory devices," so "the memory controller 420 . . . sees four load-reducing switching circuit loads, instead of sixteen memory device loads"); *id.* at 14:59–15:4 ("the data transmission circuits . . . electrically couple only the enabled memory devices to the memory controller and . . . electrically isolate the other memory devices 412 from the memory controller").

Based on this intrinsic record, the Court adopts the so-called fork-in-the-road approach. A skilled artisan would understand "driving" data from one side of the buffer to the other means, when there are multiple paths in a buffer through which that data can be driven, enabling only one of the data paths while the other possible paths are disabled. Thus, "to drive" as used in these claims means "enabling only one of the data paths while the other possible paths are disabled."

### 2. "module controller" claim terms ('339 Patent, Claims 1, 11, 19, 27)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| No construction is necessary (i.e., plain and ordinary meaning). | "a control circuit configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation . . . and corresponding to a number of ranks of memory devices lower than the physical number of ranks of memory devices on the module, and in response to receiving the input address and control signals, to output registered address and control signals corresponding to the number of physical ranks of memory devices on the module . . ." |

The second limitation of Claim 1 recites:

> a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals[.]

'339 Patent at 19:24–39. The dispute concerns the "multiple N-bit-wide ranks," which Samsung contends must be lower than the number of physical memory devices (i.e., chips) on the memory module. Dkt. No. 82 at 27–28. Netlist refers to this concept as "rank multiplication" as described by U.S. Patents 7,289,386 and 7,532,537, which the '339 Patent incorporates by reference. *Id.* at 10:50–52.

Samsung's reasoning stems from the '339 Patent's incorporation by reference of the '386 and '537 Patents. As the argument goes, the '339 Patent discloses specific module-controller circuits only by referencing those patents. Those patents, in turn, only disclose mobile control circuits

in which the number of memory devices (e.g., virtual memory devices) is smaller than the physical number of ranks of memory devices. Accordingly, says Samsung, the independent claims of the '339 Patent must be so limited. Dkt. No. 82 at 27–28. Further supporting that conclusion, says Samsung, Netlist's position would exclude the sole embodiment disclosed by the '339 Patent. *Id.* at 28–29.

Samsung cites *Techtronic Indus. Co. v. ITC*, 944 F.3d 901 (Fed. Cir. 2019), and *Cortland Line Co. v. Orvis Co.*, 203 F.3d 1351 (Fed. Cir. 2000), but neither case is helpful to its position. *Cortland* concerns a means-plus-function term, which invokes different claim-construction principles. *See Cortland*, 203 F.3d at 1355–59. And *Techtronic* is distinguishable, concluding "the patentee disavowed claim scope in each of the patent's sections" and consistently represented the invention a certain way. *Techtronic*, 944 F.3d at 908. Samsung makes no such showing here.

Regarding Samsung's suggestion its construction must be adopted to avoid excluding the sole embodiment of the patent, that is incorrect. Netlist's position is broader than Samsung's and therefore would include embodiments in which the number of N-bit-wide ranks is lower than the number of physical memory devices on the memory module.

The Court rejects Samsung's position, but otherwise gives the term its plain and ordinary meaning.

### 3. "time period in accordance with a latency parameter" ('339 Patent, Claims 1, 11, 34, 35)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| "a time period wherein both the start of the time period and duration of the time period depends on at least a latency parameter" | Plain and ordinary meaning. |

The relevant claim limitation reads:

> each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, *wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter* to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period[.]

'339 Patent at 19:53–62 (emphasis added); *see also id.* at 21:66–2:5 ("each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive [write data] from the first side to the second side during the first time period"); *id.* at 28:22–27 (reciting, in Claims 34–35, that the first and second tristate buffers, respectively, "are enabled for a first time period in accordance with a latency parameter"). The parties dispute whether the recited "latency parameter" relates to just a start time (Samsung's position), or both a start time and a duration (Netlist's position). *See* Dkt. No. 76 at 12; Dkt. No. 82 at 29 ("There is no support for Netlist's argument that the 'latency' determines the duration of the data transfer . . . .").

"Latency parameter" appears only once in the specification. *See id.* at 3:26–28 (noting, in the Summary, that "[i]n certain embodiments, the control circuit controls the byte-wise buffers in accordance with a CAS latency parameter"). But the specification provides more detail on latency:

> Column Address Strobe (CAS) latency is a *delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row*. . . . During the latency, address and control signals pass from the memory controller 420 to the control circuit 430 which produces controls sent to the control logic circuitry 502 (e.g., via lines 432) which then controls operation of the components of the data transmission circuits 416.
>
> For a write operation, during the CAS latency, the control circuit 430, in one embodiment, provides enable control signals to the control logic circuitry 502 of each

> data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data.

*Id.* at 15:61–16:11 (emphasis added).

From this, a skilled artisan would understand the "first time period" recited in the claims is *not* the latency. Rather, the "first time period" is the period during which the data path is enabled. Latency, on the other hand, is the time between (1) the moment the memory controller informs the memory modules to access the memory and (2) the moment the data is on the output pins. While there is a relationship between latency and the "first time period," the claims do not limit when the "first time period" ends. Accordingly, the Court construes "time period in accordance with a latency parameter" as "a time period wherein the start of the time period depends on at least a latency parameter."

## IV. U.S. PATENT 10,860,506

### A. Background

The patent teaches a memory module having memory devices, a module control circuit, and buffer circuits between respective sets of data signal lines in a data bus and respective sets of the memory devices. Each buffer circuit is positioned between a set of data lines and a set of memory devices. The buffer circuit buffers data signals in response to module control and clock signals. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals. '506 Patent at [57].

Only Claim 14 is at issue, which recites a method comprising the steps of:

> receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

'506 Patent at 21:54–22:15. The parties' dispute concerns the last claim limitation.

### B. "before receiving the input C/A signals corresponding to the memory read operation" ('506 Patent, Claim 14)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| The step of "determining the first predetermined amount based on at least signals received by the first data buffer" occurs before the earlier recited step of "receiving, at the module device, input C/A signals corresponding to a memory read operation via the C/A signal lines." | "during one or more previous memory operations" |

Relying mainly on prosecution history, Samsung's construction comes from the allegedly interchangeable use of part of the disputed term with Samsung's construction during prosecution. Dkt. No. 82 at 19. More specifically, Samsung's argument hinges on Netlist's post-allowance amendment of nine claims to replace "before the memory read operation" with "during one or more previous memory operations." *Id.* When making those amendments, Netlist represented to the Office that "[n]o new matter was added." Dkt. No. 82 at 19. Thus, says Samsung, the disputed term has the same scope of "before the memory read operation," and the alleged interchangeability of the two phrases with respect to the amended claims also extends to the disputed phrase in Claim 14. *Id.* at 19–20.

The Court disagrees for two reasons. First, "interchangeability" of terms is not a basis for construing claims. Second, even if it was, Samsung's reasoning is backwards. If anything, Netlist's position during prosecution was that the new phrase meant the same thing as the old phrase—because "no new matter was added"—not the other way around.

Samsung also relies on the specification, arguing certain excerpts show the disputed phrase occurs "during one or more previous memory operations." *Id.* (citing '506 Patent at 4:9–19, 18:29–40, 18:49–64). But even if true, that is not inconsistent with the plain and ordinary meaning of the claim language.

The disputed phrase is clear. The step of "determining the first predetermined amount based on at least signals received by the first data buffer" occurs before the earlier recited step of "receiving, at the module device, input C/A signals corresponding to a memory read operation via the C/A signal lines."

## V. U.S. PATENTS 11,016,918 AND 11,232,054

### A. Background

These patents concern power management on memory modules. The claimed modules include buck converters—a type of DC-to-DC power converter—that provide power to memory devices. For example, Claim 1 of the '918 Patent recites:

> 1. A memory module comprising:
>
> a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
>
> a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
>
> a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
>
> a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
>
> a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
>
> a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
>
> at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein

> a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

'918 Patent at 38:18–52. Claim 1 of the '054 Patent is similar. *See* '054 Patent at 39:66–40:4 (reciting, in Claim 16, "a voltage conversion circuit [comprising three buck converters] and configured to provide a plurality of voltages"). Generally, the parties dispute whether the voltages output by the buck converters can be the same amplitude and still fall within the scope of the claims. In addition, they dispute whether the preamble is limiting and whether the recited "second plurality of address and control signals" recited in the last limitation must be "distinct" from the earlier recited "first plurality of address and control signals."

### B. The Disputed Terms From the '918 and '054 Patents

#### 1. "dual buck converter" ('918 Patent, Claims 2, 17, 28); "dual-buck converter" ('054 Patent, Claim 15)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a buck converter with two regulated voltage outputs whose amplitude may be the same or different") | "buck converter with two outputs outputting two distinct regulated voltages" |

Claim 1 of the '918 Patent recites first, second, and third buck converters, each of which provides a regulated voltage having a voltage amplitude. '918 Patent at 38:25–30. Claim 2 further limits Claim 1 so the first and third buck converters are "configured to operate as a dual buck converter." *Id.* at 38:53–55. Other claims impose similar limitations. *See id.* at 40:13–15 (requiring, in Claim 17, "the second and third buck converters . . . configured to operate as a dual buck converter"); *id.* at 42:13–15 (reciting a similar limitation in Claim 28); '054 Patent at 39:59–61

(requiring, in Claim 15, "two of the at least three buck converters . . . configured to operate as a dual-buck converter").

The parties agree a dual buck converter has two regulated outputs, but dispute whether the claims require the voltage levels at those outputs be different. Other than the claims, the patents reference "dual buck converter" once. *See* '918 Patent at 29:27–31 ("[I]n one embodiment, . . . sub-block 1124 comprises a dual buck converter . . . as schematically illustrated by FIG. 16."). Neither party submits extrinsic evidence about the term's meaning. Nonetheless, Samsung contends "dual buck converter" is a coined term the patents define by implication "as an element that provides different voltage values." Dkt. No. 82 at 3–4 (suggesting the specification does not disclose an embodiment where the two output voltages of the dual buck converter are identical).

Samsung relies on three cases for support of its implicit-definition argument, Dkt. No. 82 at 3–4, but each is distinguishable. In *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258 (Fed. Cir. 2001), the court relied on the use of the term in the Summary of the Invention and the extensive use of the term throughout the written description to find implicit definition. *See Bell Atl.*, 262 F.3d at 1271 ("[I]n addition to the Summary of the Invention, the Detailed Description of the Preferred Embodiments continues to use the terms 'mode' and 'rate' to refer to two separate and distinct concepts.").[1] Here, however, there is only one use of "dual buck converter" in the specification, and the "Background" and "Overview" sections do not address buck converters or whether the inventions require the provision of different voltage amplitudes at their outputs.

[1] In *Bell Atlantic*, the appellant argued changing the data rate of the claimed invention would create additional "modes," and the court should not limit the construction of "mode" to only "the three broad categories described in the specification." *See generally Bell Atl.*, 262 F.3d at 1269–70.

The two other cases on which Samsung relies—*ICU Med. Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368 (Fed. Cir. 2009), and *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313 (Fed. Cir. 2005))—support the uncontroversial position that a court can consider the function of the invention when construing claims. In *ICU Medical*, for example, the parties disputed whether the recited "spike" required a pointed tip. *ICU Med.*, 558 F.3d at 1373. The appellate court noted "the specification 'repeatedly and uniformly describes the spike as a pointed instrument *for the purpose of piercing a seal inside the valve.*'" *Id.* at 1375 (quoting the trial court and citing 4 excerpts from the patent) (emphasis added). When ICU argued the court "should not import the functional limitation of piercing where that function is not recited in the claim, the court explained "it is 'entirely proper to consider the functions of an invention in seeking to determine the meaning of particular claim language.'" *Id.* (quoting *Medrad*, 401 F.3d at 1319). Based on that, the court rejected ICU's contention the term in question could be "spikeless." *Id.* at 1376.

Here, however, the specification does not explain the function of the recited "dual buck converter." Instead, it provides one example of use, from which Samsung *presumes* its function. In other words, Samsung concludes a skilled artisan would infer, from a single disclosed embodiment, the function of the "dual buck converter" is to provide different output voltage amplitudes, despite that the background sections do not explain why that would be critical to the claimed inventions. Accordingly, the Court rejects the argument that the voltage amplitudes cannot be the same.

Any "'implied' redefinition must be so clear that it equates to an explicit one." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1368 (Fed. Cir. 2012). "In other words, a person of ordinary skill in the art would have to read the specification and conclude that the

applicant . . . has acted as its own lexicographer." *Id.* Samsung makes no such showing here. Accordingly, the Court construes this term as "a buck converter with two regulated voltage outputs."

**2. "pre-regulated input voltage" ('918 Patent, Claims 16, 30)**

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, modulated input voltage) / (that is, voltage that is provided to the earlier mentioned converters or converter circuit). | "regulated voltage generated on the memory module from an input voltage" |

Claim 16 of the '918 Patent requires a memory module comprising:

> a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> first, second, and third buck converters configured to receive *a pre-regulated input voltage* and to produce first, second and third regulated voltages; . . . and
>
> a voltage monitor circuit configured to monitor *an input voltage* received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

'918 Patent at 39:54–40:12 (emphasis added); *see also id.* at 42:21–26 (reciting, in Claim 30, "first second, and third buck converters . . . configured to receive a pre-regulated input voltage"). Samsung contends the claims require the "pre-regulated voltage" to be regulated by the memory module rather than the host system to which it connects. *See* Dkt. No. 82 at 4 (characterizing the dispute as "specifically where the 'pre-regulation' occurs").

Samsung makes two arguments for its position. First, it relies on language from Claim 16 that requires "a voltage monitor circuit configured to monitor an input voltage" at the edge connections. Dkt. No. 82 at 5. According to Samsung, something must convert that input voltage into the "pre-regulated input voltages" received by the buck converters. Second, Samsung points to the specification's description of the disclosed memory module's first and second power elements 1130, 1140 as the sources of the pre-regulated fourth and fifth voltages 1110, 1112. *Id.* at 5–6.

Neither argument is persuasive. Notably, the disputed term is a small part of the "buck converter" limitations and gives context to what the buck converters do—that is, receive an input voltage and produce an output voltage. And although the claims characterize the input voltage into the buck converters as "pre-regulated" and the output voltages as "regulated," they impose no further limitations on the buck converters or, for that matter, the memory module. Although the written description discloses such structure (e.g., first and second power elements 1130, 1140), the claims do not require it. Instead, they only require what the buck converters receive, not what the other elements of the memory module provides. Accordingly, the Court rejects Samsung's proposed construction. The term will otherwise be given its plain and ordinary meaning.

### 3. "first" / "second" / "third" / "fourth regulated voltages" / "first"; "second" / "third" / "fourth" "voltage amplitude" ('918 Patent, Claim 1 and most other claims)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| "Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, first, second, third and fourth voltages that are adjusted, within tolerance, to a particular voltage level).<br><br>"Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, first/second/third/fourth amplitude of voltage which need not all be different)." | "first regulated voltage that is distinct from the second, third, and fourth regulated voltages" / "second regulated voltage that is distinct from the first, third, and fourth regulated voltages" / "third regulated voltage that is distinct from the first, second, and fourth regulated voltages" / "fourth regulated voltage that is distinct from the first, second, and third regulated voltages" first voltage amplitude that is distinct from the second, third, and fourth voltage amplitudes" / "second voltage amplitude that is distinct from the first, third, and fourth voltage amplitudes" / "third voltage amplitude that is distinct from the first, second, and fourth voltage amplitude" / "fourth voltage amplitude that is distinct from the first, second, and third voltage amplitude" |

Claim 1 of the '918 recites:

> a first buck converter configured to provide a *first regulated voltage* having a *first voltage amplitude*;
>
> a second buck converter configured to provide a *second regulated voltage* having a *second voltage amplitude*;
>
> a third buck converter configured to provide a *third regulated voltage* having a *third voltage amplitude*;
>
> a converter circuit configured to provide a *fourth regulated voltage* having a *fourth voltage amplitude*[.]

'918 Patent at 38:25–33. Relying on what it calls "this Court's lengthy precedent," Samsung contends each of these voltage amplitudes must have different values. Dkt. No. 82 at 7–10. Samsung

stresses Claims 3–4 recite different values for each of the first, second, third, and fourth voltage amplitudes. *Id.* at 8.

The Court rejects this position. To start, "claim construction issues presented in patent cases are highly fact and case-specific because they rely on the intrinsic evidence: the claim language, the written description, and the prosecution history." *Emerson Elec. Co. v. SIPCO, LLC*, 826 F. App'x 904, 914 (Fed. Cir. 2020) (citing *Phillips*, 415 F.3d at 1312–1317). Here, none of the cases on which Samsung relies relate to specific outputs of power converters and voltage levels, so those cases are not helpful on this record. Moreover, Samsung provides no technical reason why the voltage amplitudes could not be the same, nor any citation from the background sections suggesting different voltage levels advance the purposes of the invention. Accordingly, a skilled artisan would not read this claim language in such a limiting way.

The context of the claim language shows "first," "second," "third," and "fourth" are simply labels of convenience. The "first regulated voltage" is the voltage at the output of the "first buck converter," and the "first voltage amplitude" is simply the amplitude at that output. Similarly, the "second regulated voltage" is the voltage at the output of the second buck converter, and the "second voltage amplitude" is simply the amplitude at that output, and so on. The regulated voltages are distinct in the sense they are voltages at different physical outputs, but there is no reason to exclude embodiments in which one or more of the first through fourth voltage amplitudes are the same value. As such, the Court rejects Samsung's construction, but will otherwise give this term its plain and ordinary meaning.

#### 4. "at least three regulated voltages" ('054 Patent, Claims 1–15); "plurality of regulated voltages" ('054 Patent, Claims 16, 24)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| **"at least three regulated voltages"** | |
| "Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, three or more regulated voltages)." | "at least three distinct regulated voltages" |
| **"plurality of regulated voltages"** | |
| "Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, multiple regulated voltages)." | "plurality of regulated voltages" |

The parties agree construction of these terms should track the disputed terms discussed in Part V.B.3. *supra*. Dkt. No. 76 at 18 (briefing the terms together); Dkt. No. 82 at 10 (advancing its construction "[f]or the same reasons provided immediately above"). Thus, for the reasons discussed *supra*, the Court rejects Samsung's proposed constructions, but will otherwise give these terms their plain and ordinary meanings.

#### 5. "a second plurality of address and control signals" ('918 Patent, Claims 1–3, 5–7, 9–13, 15, 21)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a second set of address and control signals). | "a second plurality of address and control signals that are distinct from a first plurality of address and control signals" |

The last limitation of Claim 1 requires:

> at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output *a second plurality of address and control signals* to the plurality of SDRAM devices . . . .

'918 Patent at 38:46–47; *see also id.* at 40:35–36 (reciting similar language in Claim 21).

The dispute about this term is somewhat nebulous. Netlist suggests Samsung's construction might not be wrong, but is simply unnecessary. Dkt. No. 76 at 22–23 (contending "[t]he claim itself provides all that is needed"). Samsung argues construction is needed because of Netlist's assertion the claim doesn't preclude the input and output signals being wholly or partially the same. Dkt. No. 82 at 12.

To the extent Samsung asserts that the amplitude or shape of the first and second pluralities of address and control signals cannot be the same, the Court rejects that notion for the same reasons set forth in Part V.B.3. *supra*. But the claim language is clear the first set of address and control signals pass between the edge connections and the "at least one circuit," whereas the second set of address and control signals pass between the circuit and the SDRAM devices. Thus, the signal *paths* are distinct, but the amplitude and shape of the signals can be the same. Subject to that requirement, this term will be given its plain and ordinary meaning.

**6. "A memory module" ('918 Patent, all claims; '054 Patent, all claims)**

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| Preamble is limiting | Preamble is non-limiting |

Netlist argues the preambles of these patents' claims are limiting because they provide antecedent basis for "memory module" when later recited, such as in Claim 1 of the '918 Patent. Dkt. No. 76 at 24. *See* '918 Patent at 38:21–24 (reciting "a plurality of edge connections configured to

couple power, data, address and control *signals between the memory module and* the host system"); '054 Patent at 38:19–24 (reciting similar language in Claim 1). "Memory module" also appears in the body of Claims 4, 6, 11, 16, and 25 of the '054 Patent.

"Whether to treat a preamble as a limitation is a determination 'resolved only on review of the entire[] . . . patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim." *Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808–09 (Fed. Cir. 2002) (quoting *Corning Glass Works v. Sumitomo Electric U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989)); *see also Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1572-73, (Fed. Cir. 1996) ("Whether a preamble stating the purpose and context of the invention constitutes a limitation of the claimed process is determined on the facts of each case in light of the overall form of the claim, and the invention as described in the specification and illuminated in the prosecution history.").

"In general, a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Id.* (quoting *Pitney Bowes*, 182 F.3d at 1305). "Conversely, a preamble is not limiting 'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Id.* (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)). Similarly, "a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention." *Id.* (citing *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1434 (Fed. Cir. 2000) (holding "control apparatus" in the apparatus did not limit claim scope where it merely gives a name to the structurally complete invention)).

Having reviewed the entire patent "to gain an understanding of what the inventors actually invented and intended to encompass by the claim[s]," *Catalina Mktg. Int'l*, 289 F.3d at 808–09, the Court finds the preamble limiting. While the claims recite many of the structural requirements of a "memory module," the claims arguably read on other modular computer devices, such as a video card or network controller, despite no evidence the inventors intended to encompass such devices by the claims. To the contrary, as the Overview section explains, the invention "is couplable *to a memory controller* of a host system," '918 Patent at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller. *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

## VI. U.S. PATENTS 8,787,060 AND 9,318,160

### A. Background

These patents are directed to "systems and methods for reducing the load of drivers of memory packages included on memory modules." '060 Patent at 1:19–21. They describe prior-art memory devices in which one driver drives signals along a die interconnect connected to all array dies[2] of the device. *See id.* at 1:30–2:15. If the control die includes multiple drivers, each of those

[2] Generally, an array die is an array of memory circuits in a single piece of silicon. Dkt. No. 76-28 at 301 (defining "die" as "[a] single piece of silicon that contains one or more circuits and is or will be packaged as a unit").

drivers is connected to all array dies of the device. *See id.* at FIG. 1B (showing drivers 184, 186 each connected to all four array dies 160).

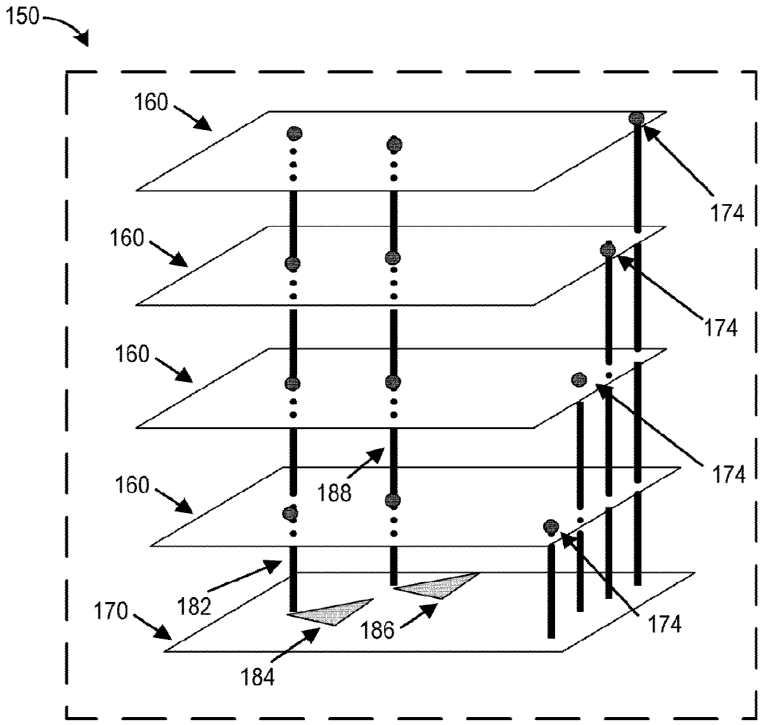


FIG. 1B

These patents address that problem by connecting a driver to less than all the array dies in a package. For example, in FIG. 2 (below), one driver is connected to a data conduit 232a that interconnects only with array dies 210a, 210b. A different driver is connected to data conduit 232b, which connects only with array dies 210c, 210d.

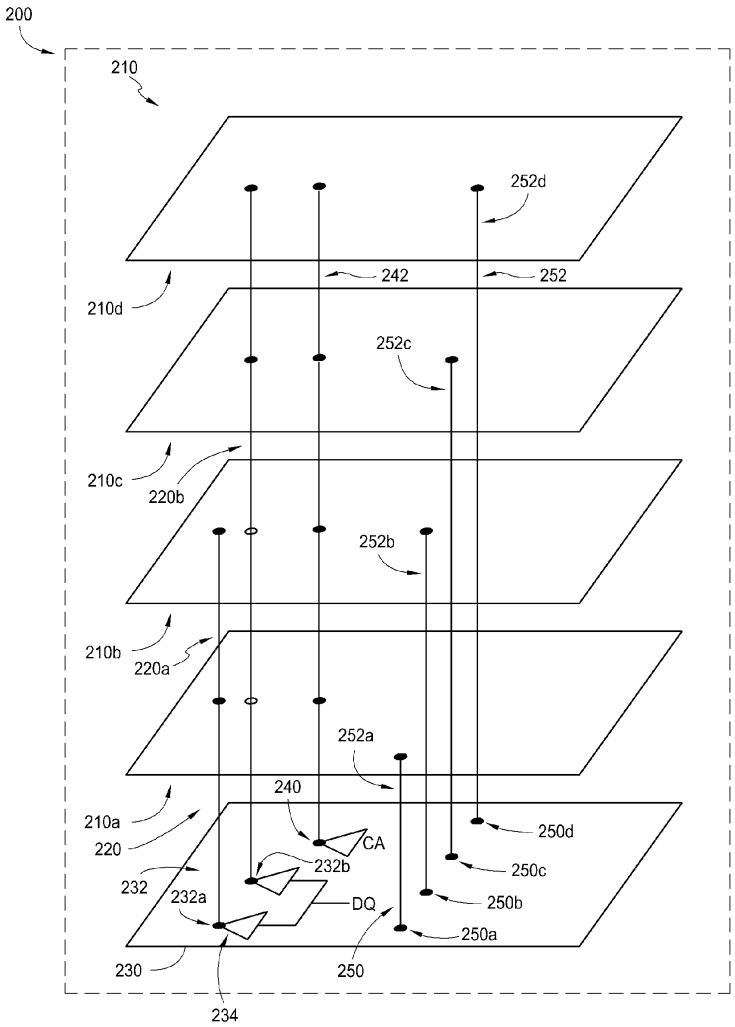


FIG. 2

As recited in Claim 1 of the ’060 Patent, FIG. 2 is a “[a] memory package, comprising:”

> a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
>
> a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
>
> at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die

> interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
>
> a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

'060 Patent at 23:58–24:15; *see also* '160 Patent at 23:47–24:3 (similar). The parties dispute the scope of "array die," "chip select signal," and "chip select conduit."

### B. Disputed Terms From the '060 and '160 Patents

#### 1. "array die" ('060 Patent, all claims; '160 Patent, all claims)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| "a die including memory cells" | "array die that is different from a DRAM circuit" |

Samsung contends Netlist disclaimed array dies that are "DRAM circuits" during prosecution. Dkt. No. 82 at 13–16. The alleged disclaimer centers on the Office's rejection of Claim 1 and Claim 29 of the '060 Patent based on U.S. Published Application 2008/0025137 (Rajan). *Id.* at 14 (citing Office Action (Oct. 11, 2013), Dkt. No. 82-2). At the time, Claim 1 recited "a plurality of stacked array dies" and Claim 29 recited "a plurality of array dies arranged in a stack." *See* Office Action (Oct. 11, 2013), Dkt. No. 82-2 at 4 (restating the "plurality of stacked array dies" limitation as found in the then-pending claims), *id.* at 8 (restating the "plurality of array dies arranged in a stack" limitation). Netlist made the same arguments with respect to each claim: "Rajan does not disclose 'a plurality of stacked array dies.' Rajan merely stacks DRAM circuits 206A–D, which

are different from array dies." Amendment (Jan. 13, 2014), Dkt. No. 82-3 at 10. But Netlist did not explain the structural difference between array dies and DRAM circuits, or even how they might be stacked differently.

Netlist counters with two arguments, neither of which is persuasive. First, says Netlist, it made the prosecution statements "to explain why [the prior art's] buffer circuit had a different structure, function and operation than the claimed 'control die,'" Dkt. No. 76 at 28, but the reason for the structural distinction is irrelevant.

Second, Netlist alleges that, because Claim 29 recites a plurality of DRAM packages that comprises a plurality of array dies, Samsung's position is nonsensical. Dkt. No. 76 at 28 ("It therefore cannot be the case that array dies in a DRAM package would exclude DRAM circuits."). Netlist contends that "by maintaining claim 29 and stating that the arguments for claim 1 also applied to claim 29, the applicant made clear that he did not intend to exclude 'DRAM circuits' from the scope of the 'array dies.'" *Id.* Yet the applicant's intent is irrelevant except to the extent it is clearly and unambiguously expressed, as Netlist did be explaining "DRAM circuits . . . are different from array dies." Amendment (Jan. 13, 2014), Dkt. No. 82-3 at 10. To the extent the applicants' disclaimer might create later difficulty in proving infringement, that is not a basis to avoid applying clear and unambiguous disavowal.

Netlist *structurally* distinguished "stacked DRAM circuits" from "stacked array dies" to obtain the patent. Based on that distinction, the Court construes "array die" as "array die that is different from a DRAM circuit."

### 2. "chip select signal" ('060 Patent, Claims 11–14, 16–19, 20–21, 23–28); "chip select conduit" ('060 Patent, Claims 6, 11–14, 16–19)

| Plaintiff's Construction | Defendants' Construction |
|---|---|
| "signal for enabling or selecting one or more array dies for data transfer" | Plain and ordinary meaning |
| "conduits for transmitting" "chip select signals," as construed above | Plain and ordinary meaning |

Claim 11 recites "a control die comprising . . . chip select conduits for providing chip select signals to respective array dies." '060 Patent at 25:16–21 (emphasis added). Samsung suggests the plain and ordinary meaning of this term excludes situations in which a chip select signal could enable multiple array dies at once. Dkt. No. 82 at 16. Netlist, however, argues one chip select signal could be used for more than one array die.

The claim language supports Samsung's position. Each of the independent claims ties the recited "chip select signals" and "chip select conduits" to "corresponding" or "respective" array dies. *See* '060 Patent at 24:31–36 (reciting, in Claim 6, third-die interconnects coupled between *respective* chip-select conduits and *respective* ones of the plurality of stacked array dies" (emphasis added); *id.* at 25:20–21 (reciting, in Claim 11, "chip select conduits for providing chip select signals to *respective* array dies" (emphasis added); *id.* at 26:8–9 (reciting, in Claim 20, "providing chip select signals to *respective* array dies through the control die" (emphasis added)).

The specification also supports this conclusion. *See* '060 Patent at 1:49–56 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive *corresponding* chip select signals to enable or select the array dies for data transfer." (emphasis added)); *id.* at 10:57–60 ("Each of the chip select conduits 250 may be configured to provide a chip select signal to a *corresponding* array die 210 via a corresponding die

interconnect 252." (emphasis added)); *id.* at 15:54–57 ("In some implementations, the drivers 404a and 404b may drive a signal to the array die *corresponding* to the chip select signal, and not to array dies that do not correspond to a chip select signal." (emphasis added)). Accordingly, the Court rejects Netlist's construction and will give this term its plain and ordinary meaning.

## VII. CONCLUSION

| Term | The Court's Construction |
|---|---|
| the "drive" claim terms<br>('339 Patent, Claims 1, 11, 19, 27) | to "drive" means "enabling only one of the data paths while the other possible paths are disabled" |
| "module controller"<br>('339 Patent, Claims 1, 11, 19, 27) | Plain and ordinary meaning. |
| "in accordance with a latency parameter"<br>('339 Patent, Claims 1, 11, 34, 35) | "a time period wherein the start of the time period depends on at least a latency parameter" |
| "before receiving the input C/A signals corresponding to the memory read operation"<br>('506 Patent, Claim 14) | The step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier recited step of "receiving . . . input C/A signals" |
| "dual buck converter"<br>('918 Patent, Claims 2, 17, 28)<br>"dual-buck converter"<br>('054 Patent, Claim 15) | "a buck converter with two regulated voltage outputs" |
| "pre-regulated input voltage"<br>('918 Patent, Claims 16, 30) | Plain and ordinary meaning |
| "first" / "second" / "third" / "fourth" "regulated voltages" / first"; "second" / "third" / "fourth" "voltage amplitude"<br>('918 Patent, Claim 1 and most other claims) | Plain and ordinary meaning. |
| "at least three regulated voltages"<br>('054 Patents, Claims 1–15) | Plain and ordinary meaning. |

| | |
|---|---|
| "plurality of regulated voltages"<br>('054 Patents, Claims 16, 24) | Plain and ordinary meaning. |
| "a second plurality of address and control signals"<br>('918 Patent, Claims 1, 21) | Plain and ordinary meaning. |
| "a memory module"<br>('918 Patent, all claims; '054 Patent, all claims) | Limiting. |
| "array die"<br>('060 Patent, all claims; '160 Patent, all claims) | "array die that is different from a DRAM circuit" |
| "chip select signal"<br>('060 Patent, Claims 11–14, 16–19, 20–21, 23–28) | Plain and ordinary meaning. |
| "chip select conduit"<br>('060 Patent, Claims 6, 11–14, 16–19) | Plain and ordinary meaning. |

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Neither party may take a position before the jury that contradicts the Court's reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

**SIGNED this 14th day of December, 2022.**

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE