



JEDEC
Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
TEL: (703) 907-7560
FAX: (703) 907-7583
<http://www.jedec.org>



COMMITTEE LETTER BALLOT

COMMITTEE: JC-42.3b

Committee Item Number: 1655.10

Subject: Proposed 3D Stacked DDR3 SDRAM Addressing

Background: At June '10 JEDEC meeting, motion by Intel and seconded by IBM to authorize the TG to issue one or more ballots on the items for DDR3 3D stacked addressing.

The motion passed by acclamation.

This proposal has been approved by the DDR3 SDRAM TG for 5-day review on Aug 11th 2010. The e-mail voting period ended Aug 16th 2010. Vote count was 6-yes, 0-no, 3-abstain.

Appendix A is for reference only and not part of this ballot.

Keywords: DDR3, 3D Stacked SDRAM, Addressing

PROPOSED

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1 3DS SDRAM Package Addressing

1.1 Logical Rank Addressing

3DS devices are sub-divided into two, four or eight logical ranks.

For 3DS devices with 2 and 4 logical ranks, the logical ranks are selected by dedicated CS# inputs. For 3DS devices with eight logical ranks, an additional select input CID (Chip ID) is used together with the four CS# inputs to decode eight internal select signals. Figure 3 and table 4 define the behavior of the CID input.

The functional behavior of logical rank(s) should not deviate from DDR3 JEDEC standard SDRAMs, except when noted in this document. Each logical rank may be implemented as a single die but the DDR3 3DS specification doesn't require this to be the case. For example a 3DS device with four logical ranks may be implemented as eight dies, i.e. two 4Gb dies with 1KB page size may be combined into an 8Gb logical rank with 2KB page size. Such an implementation has the advantage of not requiring a CID pin, making it more compatible with existing hosts and module support chips than regular 8H 3DS devices with eight 4Gb logical ranks (with 1KB page size).

1.2 3D Stack Organizations

Table 1, "Supported 3D Stack Organizations," indicates valid configurations supported by the 3DS specification.

Table 1 — Supported 3D Stack Organizations

Logical Ranks	CS#	CKE	ODT
2	2	1	1
4	4	1	1
8	4	1	1

The following figures show one architectural diagram per row of Table 1. For the names of the these figures the standard *3DS configuration notation* LR-CS-CKE-ODT is used where LR indicates the number of logical ranks, CS indicates the number of chip select inputs, CKE indicates the number of CKE inputs and ODT indicates the number of ODT inputs. Since there is only one valid configuration for each number of logical ranks, this document will typically use the abbreviations 2H, 4H and 8H to describe 3DS devices with two, four or eight logical ranks. Table 1 shows all valid CKE and ODT configurations.

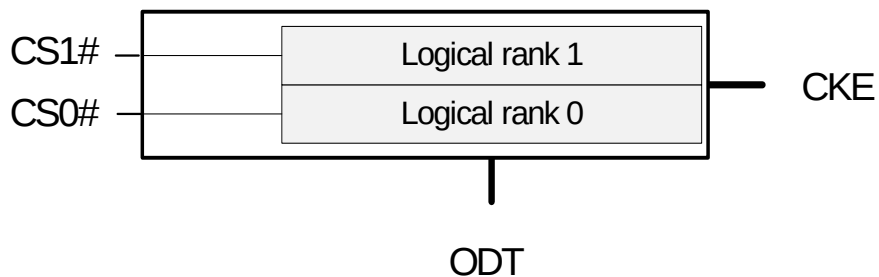


Figure 1 — 2-2-1-1 Device (2H)

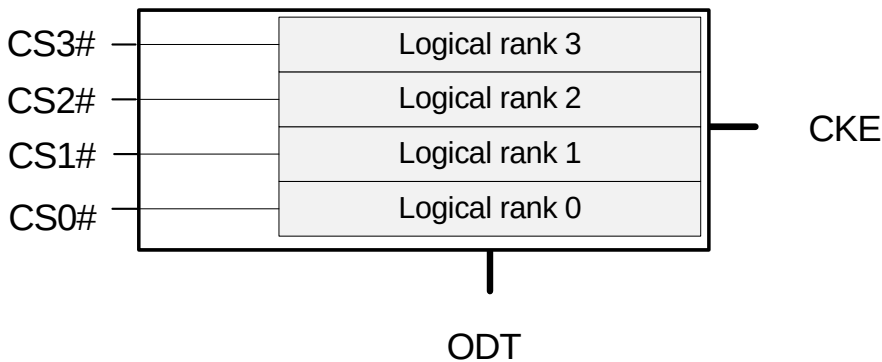


Figure 2 — 4-4-1-1 Device (4H)

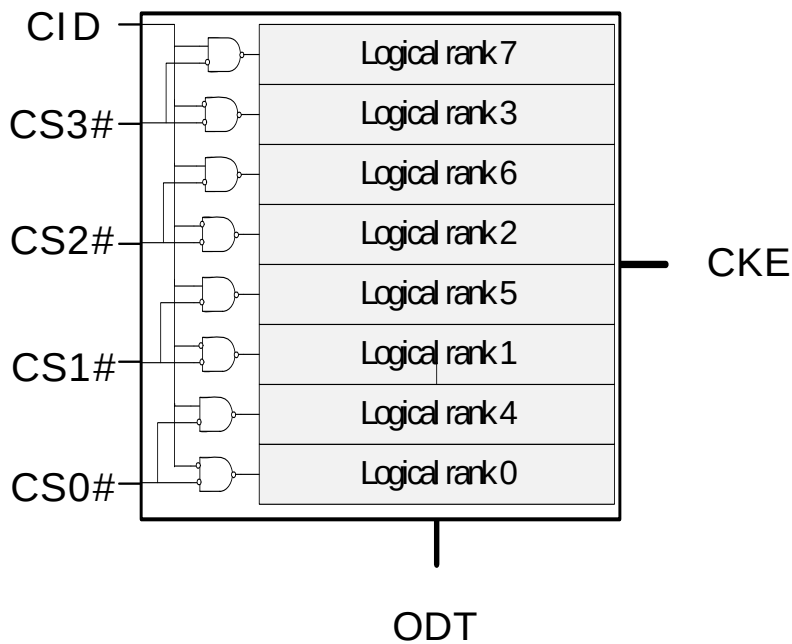


Figure 3 — 8-4-1-1 Device (8H)

Note that these diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied.

1.3 3DS SDRAM System Addressing

3DS addressing scheme for 3DS devices is explained in section 1.3. This document comprehends using these 3DS devices in RDIMM and LRDIMM applications with x4 or x8 3DS SDRAMs.

1.4 DDR3 3DS Stack Addressing Table

Table 2, Table 3 and Table 4 indicate the address and select pins that are used for different configurations of 3DS stacks.

3DS DDR3 devices may be derived from monolithic DDR3 devices. Therefore the address signals used within a logical rank are identical to the address signals used by a monolithic DRAM of the same density.

Table 2 DDR3 Address table: 2H 3D Stacked SDRAM

DDR3 3DS address table : 2H Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page size	MSB Address			Capacity	Page size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	4Gb	1KB	0	CS0#
							1	CS1#
4Gb	1KB	A15	A11	A9	8Gb	1KB	0	CS0#
							1	CS1#
8Gb	2KB	A15	A13	A11	16Gb	2KB	0	CS0#
							1	CS1#

Table 3 DDR3 Address table: 4H 3D Stacked SDRAM

DDR3 3DS address table : 4H Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page size	MSB Address			Capacity	Page size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	8Gb	1KB	0	CS0#
							1	CS1#
							2	CS2#
							3	CS3#
4Gb	1KB	A15	A11	A9	16Gb	1KB	0	CS0#
							1	CS1#
							2	CS2#
							3	CS3#
8Gb	2KB	A15	A13	A11	32Gb	2KB	0	CS0#
							1	CS1#
							2	CS2#
							3	CS3#

Table 4 DDR3 Address table: 8H 3D Stacked SDRAM

DDR3 3DS address table : 8H Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page size	MSB Address			Capacity	Page size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	16Gb	1KB	0	CS0# & CID
							1	CS1# & CID
							2	CS2# & CID
							3	CS3# & CID
							4	CS0# & NOT(CID)
							5	CS1# & NOT(CID)
							6	CS2# & NOT(CID)
							7	CS3# & NOT(CID)
4Gb	1KB	A15	A11	A9	32Gb	1KB	0	CS0# & CID
							1	CS1# & CID
							2	CS2# & CID
							3	CS3# & CID
							4	CS0# & NOT(CID)
							5	CS1# & NOT(CID)
							6	CS2# & NOT(CID)
							7	CS3# & NOT(CID)
8Gb	2KB	A15	A13	A11	64Gb	2KB	0	CS0# & CID
							1	CS1# & CID
							2	CS2# & CID
							3	CS3# & CID
							4	CS0# & NOT(CID)
							5	CS1# & NOT(CID)
							6	CS2# & NOT(CID)
							7	CS3# & NOT(CID)

1.5 Bank Selection

3DS devices can accommodate up to 64 independent banks. Figure 4 shows how these banks are selected.

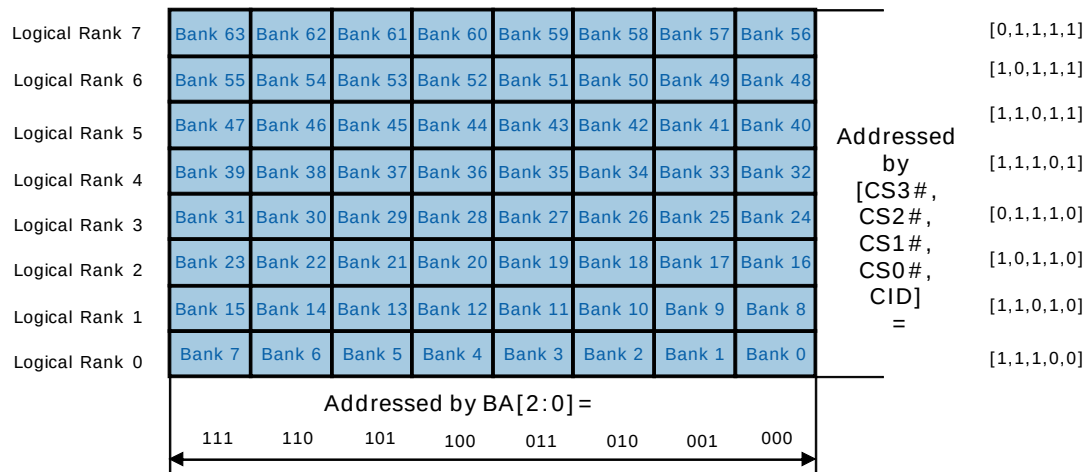


Figure 4 — Bank Selection

APPENDIX A: 3DS DIMM Pinout

Table 5 shows the TG assumption about the 3DS DIMM pinout (added to the TG consensus list on 8/4/2010) that was the basis for the 3D stacked SDRAM ballout definition.

Table 5 3DS DIMM Pinout

RDIMM¹	LRDIMM²	3DS DIMM
CKE0	CKE0	CKE0
CKE1	CKE1	CKE1
ODT0	ODT0	ODT0
ODT1	ODT1/CKE2	ODT1/A18/ID2 ³
S0#	S0#	S0#
S1#	S1#	S1#
S2#	S2#/A16	S2#/A16/ID0
S3#	S3#/A17	S3#/A17/ID1
TEST	TEST, CKE3	TEST

1.Passed JEDEC Standard

2.Passed JEDEC Standard

3.If required