

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR PRODUCTS,
INC.,

Plaintiffs,

v.

NETLIST, INC.,

Defendant.

Case No. _____

JURY TRIAL DEMANDED

COMPLAINT FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT

Plaintiffs Micron Technology, Inc. (“MTI”) and Micron Semiconductor Products, Inc. (“MSP”) (collectively, “Micron”) seek a declaration that Micron does not directly or indirectly infringe United States Patent No. 12,308,087 (the “’087 patent”) (attached as **Exhibit B**), either literally or under the doctrine of equivalents, as follows:

NATURE OF THE ACTION

1. This is an action for a declaratory judgment arising under the patent laws of the United States, Title 35 of the United States Code, and the Declaratory Judgment Act, 28 U.S.C. § 2201 et seq.

2. This action arises out of Netlist’s threatened assertions of patents against Micron. Specifically, Netlist accused Micron of infringing U.S. Patent Nos. 8,787,060 (“the ’060 patent”) and 9,318,160 (“the ’160 patent”) in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 22-cv-00203-JRG-RSP (E.D. Tex.). The U.S. Patent and Trademark Office (“Patent Office”) later invalidated, in *inter partes* reviews, all claims of these two patents in IPR2022-01427, IPR2022-01428, IPR2023-00883, and IPR2023-00882.

3. Netlist recently obtained a continuation patent—the '087 patent—from the same patent family as the invalidated '060 and '160 patents.

4. Micron seeks a declaratory judgment that it does not infringe the '087 patent.

THE PARTIES

5. Micron Technology, Inc. is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 8000 S. Federal Way, Boise, Idaho, 83716.

6. Micron Semiconductor Products, Inc. is a corporation organized and existing under the laws of the State of Idaho, with its principal place of business at 8000 S. Federal Way, Boise, Idaho, 83716.

7. Netlist, Inc. is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, California 92617.

JURISDICTION AND VENUE

8. This Court has subject matter jurisdiction over the claim for declaratory judgment of non-infringement under 28 U.S.C. §§ 1331, 1338(a), and 2201(a).

9. This Court has personal jurisdiction over Netlist, a corporation organized and existing under the laws of the State of Delaware.

10. Venue is proper in this District under 28 U.S.C. § 1391(b)–(c) because Netlist is subject to personal jurisdiction in this District.

11. An immediate, real, and justiciable controversy exists between Micron and Netlist as to whether Micron has infringed the '087 patent.

12. Netlist has alleged that Micron has infringed related patents, including the '060 and '160 patents.

13. Netlist also filed a complaint against Micron in the Eastern District of Texas alleging

infringement of the '087 patent, before it issued, in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Eastern District of Texas Case No. 2:25-cv-00552 by the same High Bandwidth Memory (HBM) products that Netlist alleged infringe its '060 and '160 patents.

14. Netlist also alleged that Samsung Electronics Co., Ltd.'s HBM products infringe the '060, '160 and '087 patents in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, Eastern District of Texas Case Nos. 2:21-cv-00463 and 2:25-cv-00553

15. Because this action presents an actual controversy with respect to the '087 patent, the Court may grant the declaratory relief sought pursuant to 28 U.S.C. § 2201 *et seq.*

BACKGROUND

A. Netlist's Prior Patent Infringement Lawsuits Against Micron

16. Netlist has pursued a litigation campaign against Micron and other suppliers of JEDEC standard-compliant memory modules for the past several years. Netlist has alleged infringement of multiple patents, including patents related to the '087 patent, based on the practice of JEDEC memory standards.

17. On June 10, 2022, Netlist filed a complaint in the Eastern District of Texas against Micron Technology, Inc. ("MTI"), Micron Semiconductor Products, Inc. ("MSP") and Micron Technology Texas, LLC ("MTT"), alleging that MTI, MSP, and MTT infringed upon six Netlist patents, including the '060 and '160 patents. *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 22-cv-00203 (E.D. Tex.) ("the EDTX-203 Case").

18. On April 12, 2023, Samsung Electronics, Co. Ltd. filed a petition for *Inter Partes* Review of the '060 and '160 patents. IPR2022-01428, IPR2022-01427. Micron joined these IPR proceedings. IPR2023-00882, IPR2023-00883.

19. On February 10, 2024, the Court for the Eastern District of Texas issued an order staying the EDTX-203 Case pending resolution of the IPR proceedings against the '060 and '160

patents. Subsequently, on April 1, 2024, the Patent Trial and Appeal Board (“PTAB”) issued Final Written Decisions finding all challenged claims of the ’060 and ’160 patents unpatentable.

B. Netlist’s Prosecution and Assertion of the ’087 Patent

20. Three months before Netlist filed the EDTX-203 Case, on March 14, 2022, Netlist filed U.S. Patent Application No. 17/694,649 (“the ’649 application”), which is a continuation of the applications that ultimately issued as the ’060 and ’160 patents.

21. On May 7, 2025, the Patent Office issued a written notice informing Netlist that the ’087 patent would issue on May 20, 2025.

22. On May 19, 2025, Netlist filed a complaint against MTI, MSP, and MTT in the Eastern District of Texas alleging infringement of the ’087 patent. *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 25-cv-00552 (E.D. Tex.) (“the EDTX-552 Case”). A copy of the complaint in the EDTX-552 Case is attached as **Exhibit A**. As alleged in Netlist’s complaint in the EDTX-552 Case, however, the ’087 patent did not exist at the time of Netlist’s complaint. The ’087 patent is scheduled to issue on May 20, 2025, *after* Netlist’s filing of the complaint in the EDTX-552 Case. Exhibit A, ¶ 20 (“The ’087 Patent issued on May 20, 2025”).¹

23. In the EDTX-552 Case, Netlist alleges that several of Micron’s current and future products, including Micron’s HBM3E, HBM4, and HBM4E products infringe one or more claims of the ’087 patent, including claim 1 of the ’087 patent. Exhibit A, ¶¶ 24, 27.

24. For at least the reasons explained in Count I, Micron’s HBM3E, HBM4, and HBM4E products do not infringe the claims of the ’087 patent.

COUNT I
(Declaration of Non-Infringement of the ’087 Patent)

25. Micron restates and incorporates by reference the preceding paragraphs as if fully set

¹ For at least these reasons, Netlist lacks standing in the EDTX-552 Case.

forth herein.

26. The Patent Office is scheduled to issue the '087 patent on May 20, 2025. Netlist has asserted an ownership interest in the '087 patent by asserting infringement in the EDTX-552 and - 553 Cases.

27. The '087 patent has six independent claims, *i.e.*, claims 1, 2, 12, 20, 21, and 22. Independent claim 1 reads as follows:

Element	Claim Language
Preamble	A dynamic random access memory (DRAM) package, comprising:
(a)	stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
(b)	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;
(c)	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;
(d)	a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A

Element	Claim Language
	conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;
(e)	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;
(f)	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;
(g)	wherein a first data interconnect of the first data interconnects is in electrically communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;
(h)	wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;
(i)	wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;
(j)	wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;
(k)	wherein the die interconnects further include first unidirectional

Element	Claim Language
	interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;
(l)	wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;
(m)	wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;
(n)	wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and
(o)	wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

28. Micron has not directly or indirectly infringed any claim of the '087 patent, either literally or under the doctrine of equivalents, at least because the Micron HBM3E, HBM4, or HBM4E products do not employ, incorporate, or otherwise make use of, all of the limitations of the claim of the '087 patent.

29. For example, claim 1 of the '087 patent requires “wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies” and “wherein a second C/A interconnect of the second C/A interconnects

is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies.” Micron’s HBM3E, HBM4, and HBM4E products do not satisfy these claim elements.

30. Micron, its customers, and its end users are not liable for infringement of the ’087 patent for any HBM3E, HBM4, or HBM4E products made, imported, or sold by Micron.

31. A substantial, immediate, and real controversy exists between Micron and Netlist regarding whether Micron or its customers or end users infringe the ’087 patent by making, using, selling, and/or offering for sale the Micron HBM3E, HBM4, and/or HBM4E products in the United States, or by importing the Micron HBM3E, HBM4, and/or HBM4E products into the United States. A judicial declaration is necessary to determine the parties’ respective rights regarding the ’087 patent.

32. Micron seeks a judgment declaring that Micron and its customers and end users do not infringe the ’087 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Micron HBM3E, HBM4, or HBM4E products in the United States, or by importing the Micron HBM3E, HBM4, or HBM4E products into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

JURY DEMAND

Micron demands a jury trial on all issues and claims so triable.

PRAYER FOR RELIEF

WHEREFORE, Micron prays for judgment and relief as follows:

- a) Declare that Micron does not directly or indirectly infringe the ’087 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’087 patent;
- b) Declare that Netlist is barred from seeking and/or enforcing injunctive relief against Micron (including its affiliates) or its direct or indirect customers and end-users in any

- jurisdiction with respect to any alleged infringement of the '087 patent;
- c) Enjoin Netlist from seeking and/or enforcing injunctive relief against Micron (including its affiliates) or its direct or indirect customers and end users in any jurisdiction with respect to any alleged infringement of the '087 patent;
 - d) Declare that judgment be entered in favor of Micron and against Netlist on each of Micron's claims;
 - e) Find that this is an exceptional case under 35 U.S.C. § 285;
 - f) Award Micron its costs and attorneys' fees in connection with this action;
 - g) Award Micron pre-judgment and post-judgment interest; and
 - h) Such further and additional relief as the Court deems just and proper.

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Of counsel:

Natalie Arbaugh
WINSTON & STRAWN LLP
2121 N. Pearl Street, Suite 900
Dallas, TX 75201
(214) 453 6500
NArbaugh@winston.com

David P. Enzminger
WINSTON & STRAWN LLP
333 South Grand Avenue, 38th Floor
Los Angeles, CA 90071-1543
(213) 615-1700
denzminger@winston.com

Michael R. Rueckheim
Ryuk Park
WINSTON & STRAWN LLP
255 Shoreline Drive, Suite 520
Redwood City, CA 94065
(650) 858 6500
MRueckheim@winston.com
RPark@winston.com

YOUNG CONAWAY STARGATT &
TAYLOR, LLP

/s/ Anne Shea Gaza

Anne Shea Gaza (No. 4093)
Daniel G. Mackrides (No. 7230)
Rodney Square
1000 North King Street
Wilmington, Delaware 19801
(302) 571-6600
agaza@ycst.com
dmackrides@ycst.com

*Attorneys for Plaintiffs Micron Technology,
Inc. and Micron Semiconductor Products, Inc.*