

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.

Plaintiff,

V.

**MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR
PRODUCTS, INC., MICRON
TECHNOLOGY TEXAS LLC,**

Defendants.

Civil Action No. _____

JURY TRIAL DEMANDED

COMPLAINT

1. Plaintiff Netlist, Inc. (“Netlist”), by its undersigned counsel, brings this action against defendants Micron Technology Inc. (“Micron Technology”), Micron Semiconductor Products, Inc. (“Micron Semiconductor”), and Micron Technology Texas, LLC (“Micron Texas”) (collectively, “Micron” or “Defendants”), Micron’s infringement of U.S. Patent No. 12,308,087 (“the ’087 Patent”).

2. Micron has also filed a series of retaliatory suits in its home state of Idaho, accusing Netlist of bad faith assertion of certain other Netlist patents under Idaho Code § 48-1703. *See Netlist, Inc. v. Micron Technology, Inc.*, No. 2:23-cv-628, Dkt. 1 ¶¶ 20-27; Dkt. 14 ¶¶ 23-31 (summarizing Micron’s pattern of filing retaliatory suits). It is only a matter of time before Micron brings another similar suit in Idaho state court on the ’087 Patent. Therefore, Netlist seeks a declaration that this suit was not brought in bad faith; a declaration that Netlist has not made bad

faith assertion of patent infringement under Idaho Code § 48-1703; and a declaration that Defendants are not entitled to relief under Idaho Code § 48-1703.

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Way, Suite 100, Irvine, CA 92617.

4. On information and belief, Micron makes dynamic random-access memory (“DRAM”), NAND Flash, and NOR Flash memory, and other memory products in semiconductor fabrication plants in the United States and other countries throughout the world. On information and belief, Micron sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives and mobile telecommunications markets.

5. On information and belief, Micron Technology is a corporation organized and existing under the laws of Delaware. On information and belief, Micron Technology has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Technology is registered to do business in the State of Texas, and can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

6. On information and belief, Micron Semiconductor is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Semiconductor has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Semiconductor can be served through

its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. On information and belief, Micron Texas is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Texas has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Texas also has a regular and established place of business at 950 West Bethany Drive, Suite 120, Allen, Texas 75013-3837. On information and belief, Micron Texas is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

8. On information and belief, Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. On information and belief, Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

9. On information and belief, Defendants have semiconductor fabrication plants in the United States and other countries throughout the world and manufacture memory products such as DRAM, NAND Flash, and NOR Flash at those plants. On information and belief, Defendants also use, sell, and offer for sale in the United States, import into the United States and/or export from the United States memory products, including DDR5 dual in-line memory modules (“DIMMs”). On information and belief, Defendants have at least used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district, *e.g.*, through sales and distribution channels managed by Micron Texas.

10. On information and belief, Defendants place, have placed, and contributed to placing Accused Instrumentalities into the stream of commerce via an established distribution channel knowing or understanding that such products would be sold and used in the United States, including in this judicial district. On information and belief, Defendants have also derived substantial revenues from infringing acts in this judicial district, including from the sale and use of the Accused Instrumentalities.

11. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

12. The Court has subject matter jurisdiction under 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

13. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

14. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patent-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

15. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b) because Defendants (1) have committed and continue to commit acts of patent

infringement in this District by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that infringe one or more claims of the Patents-in-Suit, and (2) have done and continue to do business in this District by maintaining regular and established places of business, including at least at 805 Central Expressway South, Suite 100, Allen, Texas 75013.

III. FACTUAL ALLEGATIONS

A. Background

16. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase. Netlist has secured multiple jury verdicts confirming the commercial success of its inventions. For example, in 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist \$303.15 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:21-cv-463, Dkt. 479. As another example, in May 2024, a jury in the Eastern District of Texas awarded Netlist \$445 million in damages against Micron. *See Netlist, Inc. v. Micron Technology Texas, LLC*, No. 2:22-cv-294, Dkt. 135. And in November 2024, a jury found that Samsung willfully infringed three other Netlist patents and awarded Netlist \$118 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-293, Dkt. 847.

17. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM.

Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. Netlist's pioneering NVDIMM products utilized the same on-module power management technology found on newer-generation DDR5 DIMMs. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

18. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

19. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

B. The '087 Patent

20. The '087 Patent is entitled "Memory Package Having Stacked Array Dies and Reduced Driver Load," and was filed on March 14, 2022 and assigned to Netlist, Inc. The '087 Patent issued on May 20, 2025 and claims priority to, among others, U.S. Application No. 13/288,850, filed Nov. 3, 2011, and U.S. Provisional No. 61/409,893, filed November 3, 2010.

21. Claim 1 of the '087 Patent provides:

[1pre] A dynamic random access memory (DRAM) package, comprising:

[1a] stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies

including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

[1b] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

[1c] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

[1d] a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

[1e] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

[1f] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

[1g] wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

[1h] wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

[1i] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

[1j] wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

[1k] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

[1l] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die;

[1m] wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

[1n] wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

[1o] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

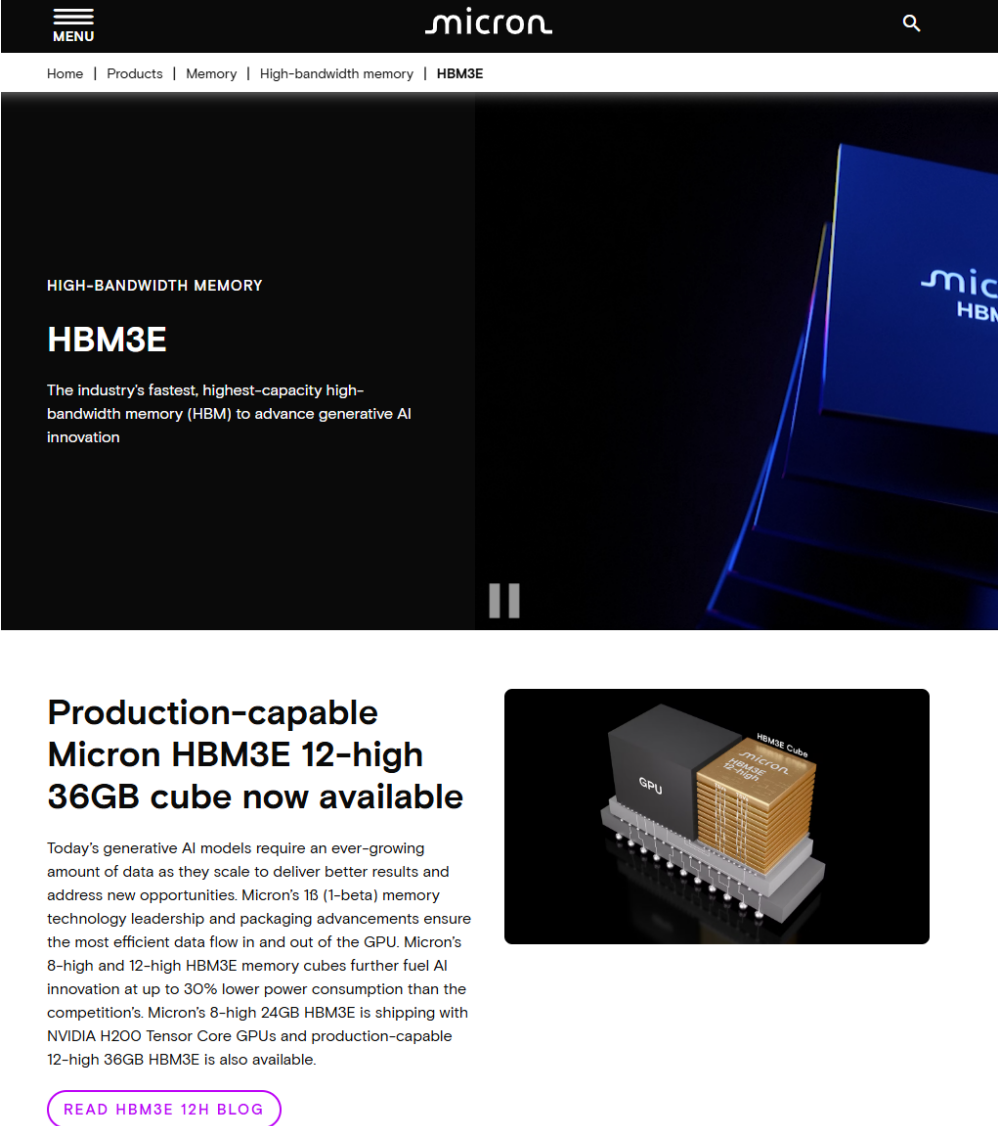
C. Micron's Infringing Activities

22. Defendants are worldwide semiconductor solution providers that primarily manufacture semiconductor memory products such as DRAM, DIMMs, and MCP (Multi-Chip Package), such as HBM. Defendants develop, manufacture, sell, offer to sell, import into the United States and export from the United States memory components and memory modules (including semi-finished ones) designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications as well as for use in consumer end products.

D. High Bandwidth Memory ("HBM")

23. HBM is a type of high-speed computer memory technology that relies in part on vertically-stacked memory dies and differs from the DDR4 or DDR5 DIMM formats described in the paragraphs above. Micron is a major supplier of HBM. Micron itself confirms that "Micron's 8-high and 12-high HBM3E memory cubes further fuel AI innovation at up to 30% lower power consumption than the competition's." <https://www.micron.com/products/memory/hbm/hbm3e>.

24. The Accused HBM Products include, without limitation, any Micron HBM3E, and newer products (e.g., HBM4; HBM4e¹) made, sold, used, offered for sale, and/or imported into the United States by Micron. By way of non-limiting example, the accused HBM products include the HBM3E products advertised on Micron's website:



HIGH-BANDWIDTH MEMORY

HBM3E

The industry's fastest, highest-capacity high-bandwidth memory (HBM) to advance generative AI innovation

Production-capable Micron HBM3E 12-high 36GB cube now available

Today's generative AI models require an ever-growing amount of data as they scale to deliver better results and address new opportunities. Micron's 1B (1-beta) memory technology leadership and packaging advancements ensure the most efficient data flow in and out of the GPU. Micron's 8-high and 12-high HBM3E memory cubes further fuel AI innovation at up to 30% lower power consumption than the competition's. Micron's 8-high 24GB HBM3E is shipping with NVIDIA H200 Tensor Core GPUs and production-capable 12-high 36GB HBM3E is also available.

[READ HBM3E 12H BLOG](#)

¹ Micron has announced development of HBM4e products in its Financial Results FQ1 2025 Report. ("Development work is well underway with multiple customers on HBM4E.").

25. On information and belief, the Accused HBM Products are compliant with the applicable memory standards promulgated by the Joint Electron Device Engineering Council (“JEDEC”).

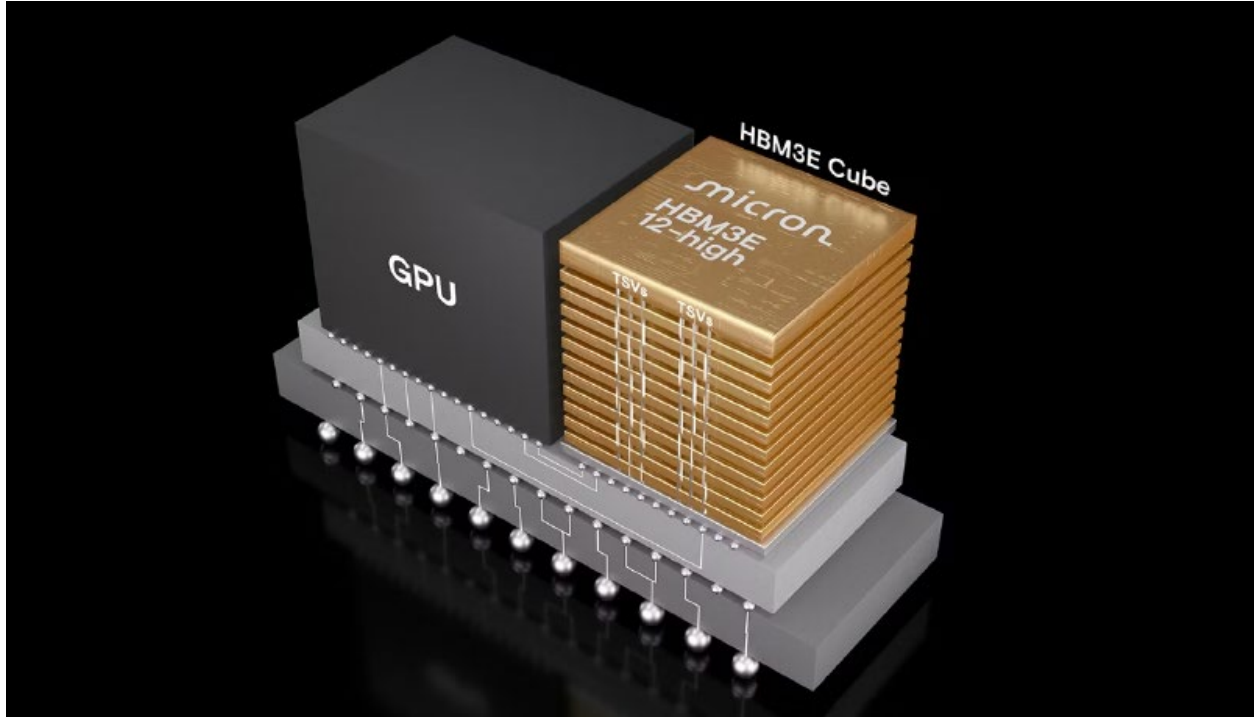
IV. **FIRST CLAIM FOR RELIEF**

26. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

27. On information and belief, Defendants directly infringed and are currently infringing at least one of the approved claims of the ’087 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure and operating mechanisms in relevant part infringe at least claim 1 of the ’087 Patent.

28. To the extent the preamble is limiting, the Accused HBM Products are a DRAM package. Additionally, as shown below, the Accused HBM Products each include stacked DRAM dies (*e.g.*, 8, 12, or 16 DRAM dies) including at least a first plurality and second plurality of DRAM dies, with each DRAM die of the stacked DRAM dies including C/A ports, data ports, and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells. *See, e.g.*, <https://www.micron.com/about/blog/applications/ai/microns-hbm3e-powering-the-future-of-ai-with-high-bandwidth-memory> (“HBM3E is highly energy-efficient because the data path between the host and memory is shorter. The DRAM communicates with the host through silicon vias or TSVs, which Girish explains as being similar to a toothpick through a burger. It takes power and data from the bottom die and moves it to the top memory layer. Micron’s HBM3E consumes 30%

less power than the competition because of the advanced CMOS technology innovation on the 1 β process node and advanced packaging innovations with up to 2 times TSVs coupled with 25% shrink in package interconnects.”).



29. The Accused HBM Products also include terminals with command and/or address (C/A) terminals and data terminals, via which the memory package communicates, e.g., control/address signals and data signals in response to the C/A signals, respectively. For example, the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation, and to receive second data signals in response to a second set of C/A signals associated with a memory write operation. To illustrate, JEDEC Standard No. 238A provides the following Command Truth Table listing the command and/or address signals associated with a memory read operation and memory write operation:

6.3.1 Command Truth Tables (cont'd)

Table 31 — Column Commands Truth Table

Command ⁴	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes
Column No Operation	CNOP	R	H	H	H	V	V	V	V	V	1, 2, 3
		F	V	V	V	V	V	V	V	V	
Read	RD	R	H	L	H	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Read w/ AP	RDA	R	H	L	H	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write	WR	R	H	L	L	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write w/ AP	WRA	R	H	L	L	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Mode Register Set	MRS	R	L	L	L	MA4	OP5	OP6	OP7	MA0	1, 3, 8, 9
		F	MA1	MA2	MA3	OP0	OP1	OP2	OP3	OP4	

NOTE 1

BA = Bank Address; CA = Column Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; MA = Mode Register Address; V = Valid Signal (either H or L, but not floating).

NOTE 2

C[7:0] must be driven to a valid signal level even if a stack ID address (SID) is not defined for a specific density, or if parity is disabled in the mode register. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6. C[7:0] are Don't Care when the device is in power-down or self refresh.

NOTE 3

Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

NOTE 4

All other command encodings not shown in the table are reserved for future use.

NOTE 5

PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a CNOP.

NOTE 6

The SID bits act as bank address bits in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. All other column commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7

HBM3 configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be consulted for details.

NOTE 8

All mode registers are write-only by default using the MRS command.

NOTE 9

Refer to the HBM3 Mode Register Overview table for MA4 of MRS.

30. The Accused HBM Products further include die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked array dies through the one or more TSVs. See

<https://www.micron.com/about/blog/applications/ai/microns-hbm3e-powering-the-future-of-ai-with-high-bandwidth-memory>; *see also* Micron HBM3E Product Brief.

31. As shown above, the Accused HBM Products also include a control die (also known as a “buffer die” or “logic die”) coupled between the terminals and the stacked DRAM dies. *See also, e.g.*, Micron Fiscal Q4 2023 Earnings Call Prepared Remarks at 6 (“The HBM product includes a logic interface die . . .”). The control die includes conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects.

32. The Accused HBM Products also have C/A interconnects in the claimed configuration. For example, a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not with any C/A port on any of the second plurality of DRAM dies. Similarly, a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not with any C/A port on any of the first plurality of DRAM dies.

33. The Accused HBM Products also have data interconnects in the claimed configuration. For example, a first data interconnect of the first data interconnects are in electrical communication with data ports on the first plurality of DRAM dies and not with any data port on any of the second plurality of DRAM dies. Further, each of the first data interconnects includes a first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein

the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die. Similarly, a second data interconnect of the second data interconnects is in electrical communication with data ports on the second plurality of DRAM dies and not with any data port on any of the first plurality of DRAM die. For example, as depicted above, some TSVs appear to only electrically interconnect to some of the dies in the stack, while others may electrically bypass certain groups of dies.

34. Additionally, the data conduits in the control die include a first conduit of the first data conduits coupled between the first data interconnect and a first data terminal of the data terminals (e.g., one or more data terminals), and a second conduit of the second data conduits coupled between the second data interconnect and the first data terminal (e.g., one or more data terminals). The control die also includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal (e.g., as shown above in the Command Truth Table of JESD 238A).

35. The Accused HBM Products further include first and second unidirectional die interconnects, for example, respective TSVs associated with unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. *See, e.g.*, JESD 238A (“Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c.”); *id.* (reproduced below). For example, the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects (e.g., RDQS_t/RDQS_c in response to the first set of C/A signals) and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects. As further

example, the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects (e.g., WDQS_t/WDQS_c in response to the second set of C/A signals) and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects.

6 Operation

6.1 HBM3 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32DQ(DWORD). The data bus operates at double data rate (DDR).

HBM3 utilizes two types of clock with different frequencies. The strobe frequency is twice the frequency of the command clock, requiring an HBM3 to have reset-type clock-divider in the WDQS clock tree (Figure 10). By dividing the WDQS, the operation speed of DRAM internal circuits in WDQS domain is reduced to half. The direction of the internal WDQS/2 transition may vary depending on vendor's choice. Command clock and WDQS are generated from the same PLL and RDQS clock is generated from WDQS. WDQS internal divider is initialized to be a pre-defined internal divider state after Self Refresh exit or Power-up or Power down exit sequence. The sum of preamble and postamble for both READ and WRITE operation is required to be an even number so that the internal divider's state, phase of internal WDQS/2, is maintained. Therefore, HBM3 WDQS does not require a specific sync operation before READ and WRITE operations. WDQS starts toggling before starting WRITE or READ operations for reducing ISI. During inactivity, WDQS/ RDQS are required to be static (WDQS/RDQS_t is Low, WDQS/RDQS_c is High). When WRITE training for unmatched DQ/DQS path, DQ should be shifted to align phase to the point where CK and WDQS are in sync.

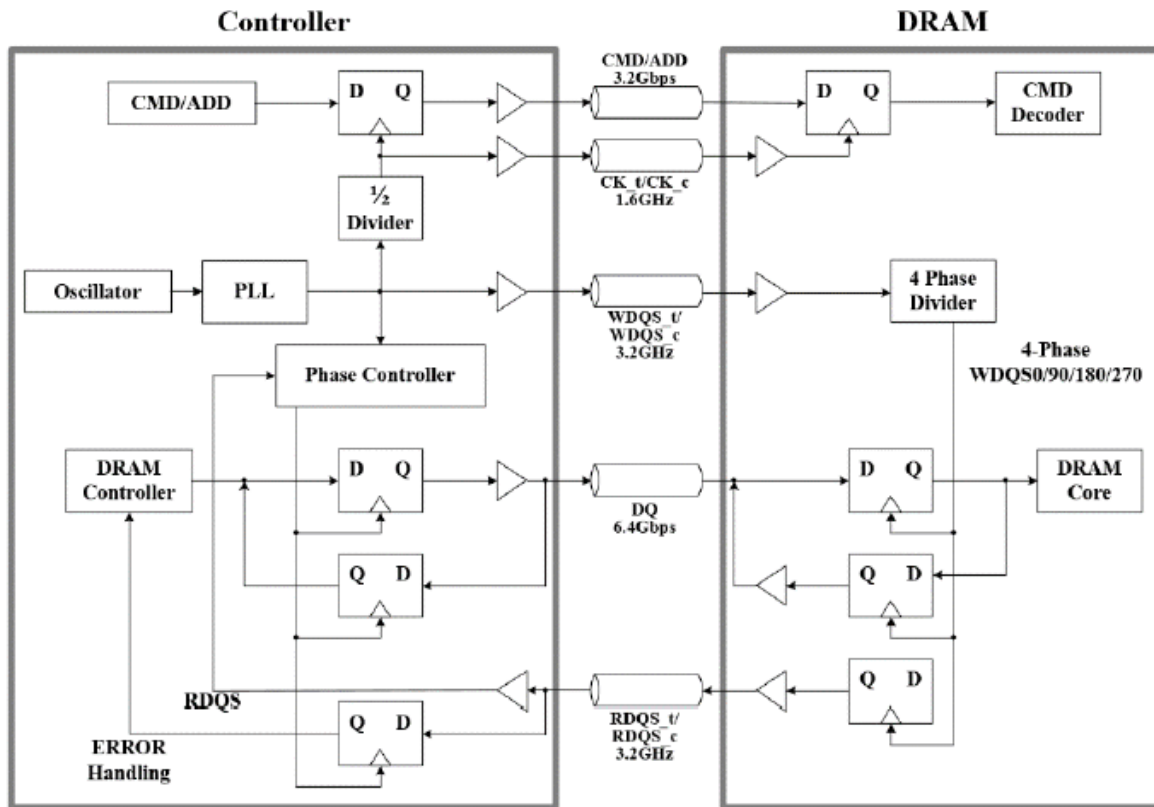


Figure 10 — High Level Block Diagram Example of Clocking Scheme

V. SECOND CLAIM FOR RELIEF

36. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

37. Netlist has not violated Idaho Code § 48-1703 by asserting the Patent-in-Suit against Micron.

VI. DEMAND FOR JURY TRIAL

38. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

VII. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Micron infringes the Patent-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Micron's infringement;

C. an award of damages resulting from Micron acts of infringement in accordance with 35 U.S.C. § 284;

D. that Micron's infringement of the Patent-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. a declaration that Netlist has not made a bad-faith assertion of patent infringement against Micron nor engaged in any unlawful, unfair, or deceptive act or practice in trade or commerce under the Idaho Consumer Protection Act, and is therefore compliant with Idaho Code § 48-1703;

I. a judgment that Micron is not entitled to any award of damages in the pursuit of this litigation pursuant to Idaho Code § 48-1706(b) and (d), § 48-1706(1)(c), Idaho Rule of Civil Procedure 54, and such other and additional provisions of the Idaho Rules of Civil Procedure and Idaho Code, or any other applicable authority;

J. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: May 19, 2025

Respectfully submitted,

/s/ Samuel F. Baxter

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