UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Patent No. 9,318,160
Issued: April 19, 2016
Filed: July 21, 2014
Inventor: Hyun Lee

Title: Memory Package with Optimized Driver Load and Method of Operation

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Inter Partes Review No. IPR2022-01427

DECLARATION OF DR. ANDREW WOLFE REGARDING U.S. PATENT NO. 9,318,160

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 9,318,160 ("the 160 Patent") (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including

Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM and flash memory,

in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the 160 Patent, I am relying upon certain basic legal principles that have been explained to me.

25. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 160 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims of the 160 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors"

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 160 PATENT

A. Effective Filing Date of the 160 Patent: No Earlier Than November 3, 2011

47. The 160 Patent resulted from a continuation application of U.S. Patent Application No. 13/288,850 ("850 Application") (Ex. 1002) and claims priority to U.S. Provisional Application No. 61/409,893 ("893 Provisional Application" or "893 Provisional") (Ex. 1005), filed November 3, 2010. Ex. 1001 (160 Patent) at (63) and (60).

48. In my opinion, as explained below, the effective filing date for the claims of the 160 Patent is no earlier than November 3, 2011. In any event, all of the prior art I rely upon for my invalidity opinions predates November 3, 2010.

1. Several Limitations in All Claims Are Unsupported by the 893 Provisional Application Filed November 3, 2010

49. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the 893 Provisional Application shows that the inventor actually invented what is claimed in each of the claims of the 160 Patent, and possessed the claimed subject matter, as of the provisional filing date of November 3, 2010. When considering that question, I have considered whether the 893 Provisional Application explicitly or inherently discloses all of the elements of each of the claims. To determine whether the provisional inherently discloses an

element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I understand that the knowledge of ordinary artisans may be used to inform what is actually in the provisional, but not to teach limitations that are not in the provisional, even if those limitations would be rendered obvious by the disclosure in the provisional.

50. Although the 893 Provisional Application lists more than a dozen patent and patent application numbers to be incorporated by reference, the 893 Provisional Application falls short of describing many elements included in the claims of the 160 Patent's claims, in many cases not even using any terms associated with an element. Much of the disclosure in the 160 Patent was added with the filing of the non-provisional 850 Application. Specifically, the 850 Application added to the 893 Provisional Application's disclosure Figures 1-5, all of columns 1-2, 5-17, and 21-28, and at least part of columns 3-4 and 18-20 of the 160 Patent, Ex. 1001. In my opinion, at least the following claim limitations are not disclosed by the 893 Provisional Application filed November 3, 2010:

a) Groups of Array Dies – Claims 1, 6, 10

51. Each of independent claims 1, 6, and 10 include one or more limitations requiring a memory package having stacked array dies that include "*a*

first group of array dies" and "*a second group of at least one array die*." Ex. 1001 (160 Patent), cls. 1, 6, 10.

52. The 893 Provisional Application does not itself mention groups within a stack of array dies. *See* Ex. 1005. The figures illustrate DRAM packages, which packages are also described in paragraphs [0006]-[0012] of the 893 Provisional Application. *Id.* Additionally, the title of the provisional is "Architecture for Memory Module with Packages of Three-Dimensional Stacked (3DS) Memory Chips." *Id.* at 1. In the specification, the 3DS DRAM package is described as including stacked DDR DRAM chips or dies. *Id.* at 5, ¶[0006]. However, the packages described in the 893 Provisional Application do not have groups of array dies within the stack as claimed in the 160 Patent. In particular, the illustrated dies are never separated into a first group and a second group.

53. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of the "*first group of array dies*" and "*second group of at least one array die*" as recited in the independent claims of the 160 Patent.

b) Die Interconnects Not in Electrical Communication with Some Array Dies – Claims 1, 6, 10

54. Each of independent claims 1, 6, and 10 include a limitation requiring first and second die interconnects, each being in electrical communication with a

respective group of array dies but not in electrical communication with another group of array dies. Ex. 1001 (160 Patent), cls. 1, 6, 10.

55. The 893 Provisional Application does not describe a die interconnect which is in electrical communication with one group of array dies but is not in electrical communication with another group of array dies. *See* Ex. 1005. Each of the interconnects disclosed is in electrical communication with all of the array dies.

56. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of first and second die interconnects, each being in electrical communication with a respective group of array dies but not in electrical communication with another group of array dies as recited in the independent claims of the 160 Patent.

c) Respective States of Data Conduits – Claims 5, 9, 11

57. Each of claims 5, 9, and 11 include a limitation requiring a control circuit controlling "respective states" of "data conduits." Ex. 1001 (160 Patent), cls. 5, 9, 11.

58. The 893 Provisional Application does not mention any "data conduit" or any specific "respective states" of such a "data conduit." *See* Ex. 1005.

59. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of a control circuit

controlling "respective states" of "data conduits" as recited in independent claims 5, 9, and 11 of the 160 Patent.

B. Person of Ordinary Skill in the Art

60. The 160 Patent identifies the relevant field of art as follows: "The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules." Ex. 1001 at 1:20-23. Based on that description of the field of art, my experience, and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 160 Patent in 2010 and 2011 ("Skilled Artisan" or "POSITA") would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked

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memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

C. Overview of the 160 Patent

61. The 160 Patent states that it "relates to systems and methods for reducing the load of drivers of memory packages." Ex. 1001 (160 Patent) at 1:21-23. The 160 Patent admits as prior art "FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used." *Id*. at 1:32-35 and Fig. 1B (reproduced below, annotated).

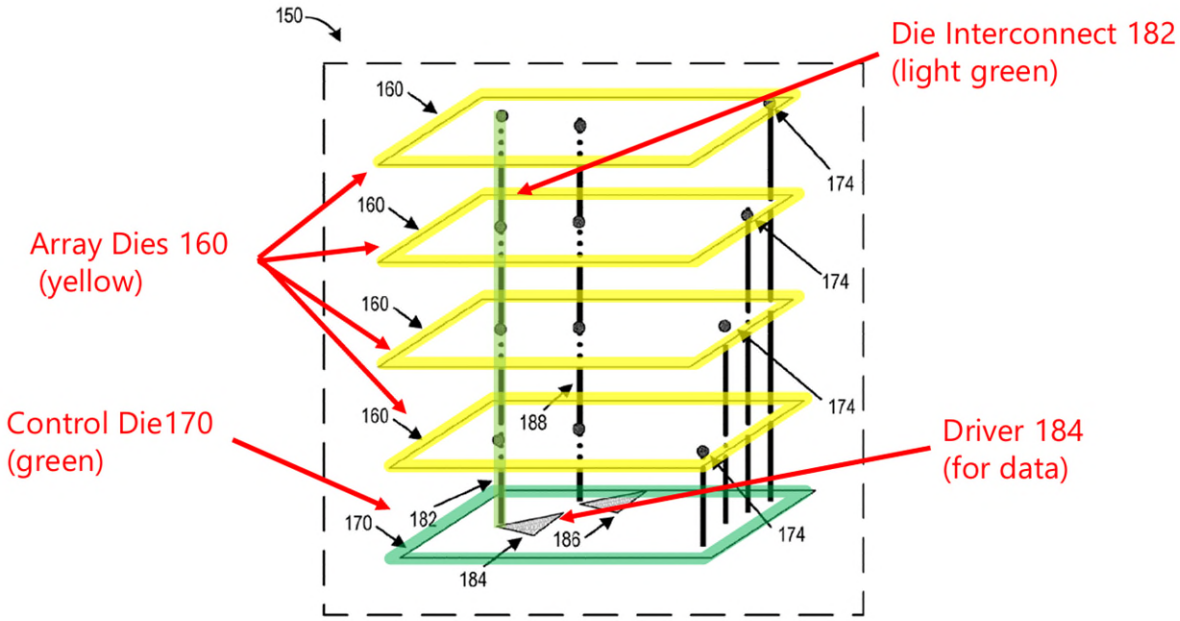
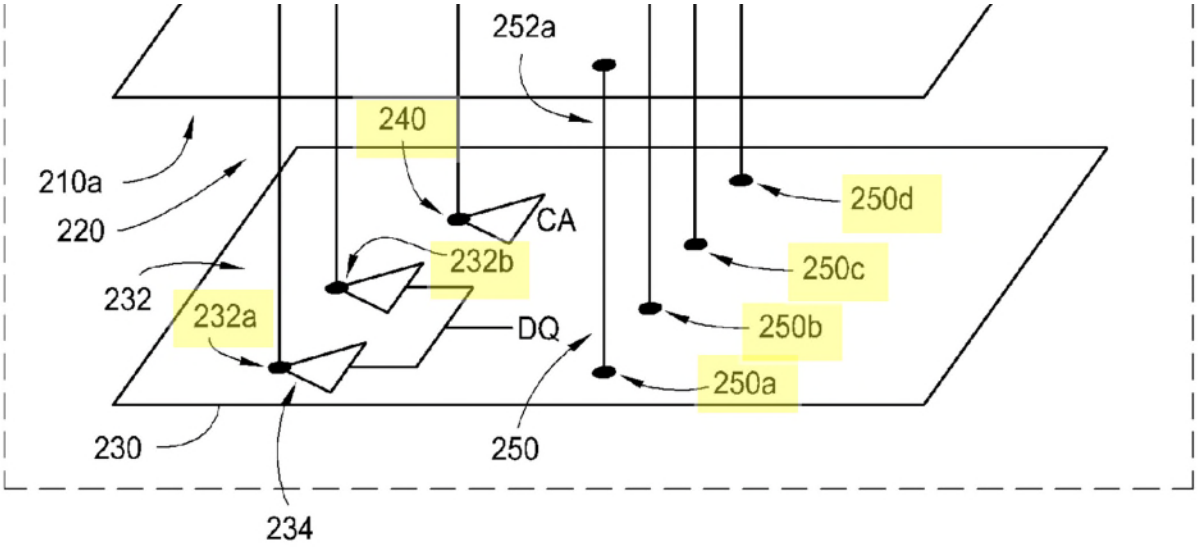


FIG. 1B

In particular, "FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 [(yellow)] and a control die 170 [(green)] that … [includes] a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182." Ex. 1001 (the 160 Patent) at 1:65-2:6. The 160 Patent explains that a problem with the prior-art memory package is that the data driver 184 has to drive a load that is "in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power." *Id*. at 2:10-17.

62. The 160 Patent discloses that each die interconnect has a corresponding "conduit" which is configured to transmit a signal to the die interconnect. Ex. 1001 (160 Patent), *e.g.*, at Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b, command/address conduits 240, and chip select conduits 250a-d), 6:51-62 (describing data conduits 232a and 232b), 9:31-63 (describing command/address conduits 240 and chip select conduits 250). A "conduit" may, but does not have to, include a driver to drive the load on the conduit. *Id*.; *see also* 6:63-65 ("In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2."),

21:3-5 ("The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.").



63. The 160 Patent solves the prior art's problem of having too much load on the data conduits by replacing one data driver of the prior art with two (or more) drivers 234 coupled to the same DQ data terminal, each of the drivers driving the data signal through a respective die interconnect (220a, 220b) that is in electrical communication with *a subset* of the array dies, thus reducing the overall load of each data conduit. Ex. 1001 (the 160 Patent) at 7:11-8:21 and Fig. 2 (reproduced below, annotated).

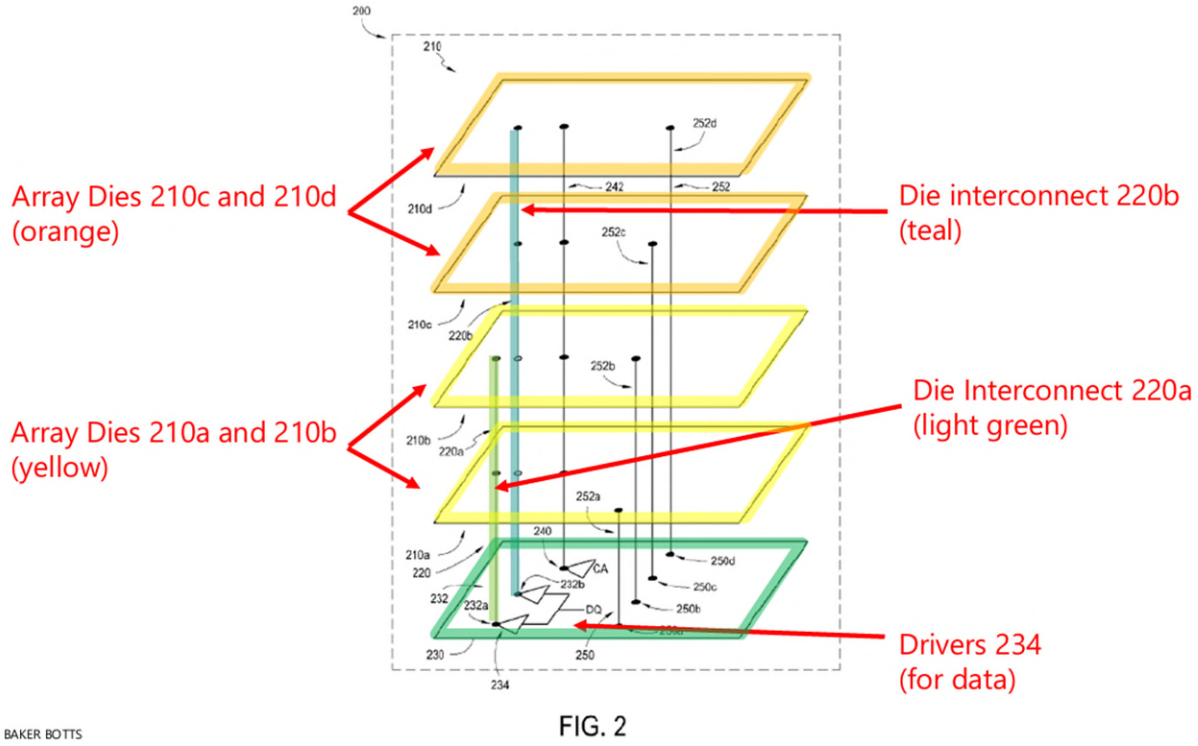


FIG. 2

64. In the example of Fig. 2, "die interconnect 220a [(light green)] may be in electrical communication with a data port from array die 210a [(yellow)] and a data port from array die 210b [(yellow)] (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c [(orange)] or any data ports from array die 210d [(orange)]." Ex. 1001 (the 160 Patent) at 5:66-6:4. The other "die interconnect 220b [(teal)] may be in electrical communication with a data port from array die 210c [(orange)] and a data port from array die 210d [(orange)] (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a [(yellow)] and array die 210b [(yellow)]… Despite not being in electrical communication with any data

ports from array die 210a and 210b [(yellow)], in some implementations, the die interconnect 220b [(teal)] may pass through the array dies 210a and 210b [(yellow)] (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b." *Id*. at 6:12-26.

65. In another example, the 160 Patent discloses selecting the number of array dies that are connected to a die interconnect in order to reduce the difference between the loads on the different data conduits. Ex. 1001 at Fig. 3 and Table 1 (reproduced below). Here, the memory package 300 includes eight array dies 310a-310h and a control die 330. *Id*. at 10:21-43. The control die includes six data conduits 332a-f with respective drivers 334a-334f, each driving a respective die interconnect 320a-f. *Id*. at 10:44-58. Each of the shorter interconnects 320a and 320b is connected to two array dies, and each of the longer interconnects 320c-f is connected to a single array die. *Id*.

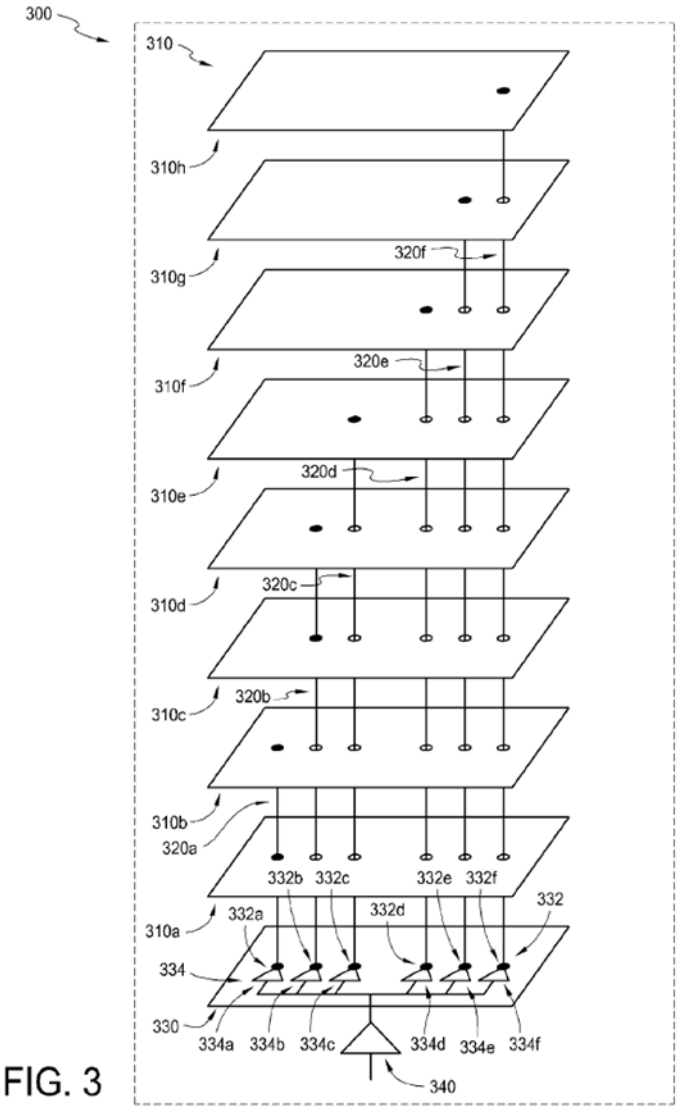


FIG. 3

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5 L	0.5
332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

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The 160 Patent describes that "Table 1 specifies the capacitive load values for each conduit 332 assuming … that the load of each of the array dies 310 is L, and that the load of each segment of the die interconnects 320 is 0.25L. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f." *Id*. at 12:59-67. The 160 Patent explains that, as can be seen from Table 1 above, "the maximum load of any conduit 332, using the example values previously described, is 3L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10L." *Id*. at 13:12-18. The 160 Patent further explains that such a die interconnect in electrical communication with each die "does not implement the teachings of this disclosure, but is in accordance with conventional configurations." Ex. 1001 (the 160 Patent) at 7:30-32.

D. The Prosecution History of the 160 Patent

66. The prosecution histories of the 160 Patent and the other patent applications in the family of the 160 Patent are discussed below, starting with the earliest filed application, the 893 Provisional Application.

1. Provisional Application No. 61/409,893 (Nov. 3, 2010)

67. The applicants filed Provisional Application No. 61/409,893 ("893 Provisional Application"), titled "Architecture for Memory Module with Packages of Three-Dimensional Stacked (3DS) Memory Chips," on November 3, 2010. Ex. 1005 at p. 14.

2. Application No. 13/288,850 (060 Patent)

68. The applicants filed U.S. Patent Application No. 13/288,850 ("850 Application"), titled "Method and Apparatus for Optimizing Driver Load in a Memory Package," on November 3, 2011. Ex. 1002 at p. 60. The 850 Application claims the benefit of the 893 Provisional Application, filed November 3, 2010. Ex. 1002 at pp. 60, 64. The 850 Application presented 34 claims at filing, 1-34. Ex. 1002 at pp. 43-50.

69. The International Search Report mailed January 30, 2013, indicated that Figures 2B and 2C of U.S. Patent Publication No. 2008/0025137 ("Rajan137") (Ex. 1011), reprinted below, were "of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone." Ex. 1002 at pp. 238-48.

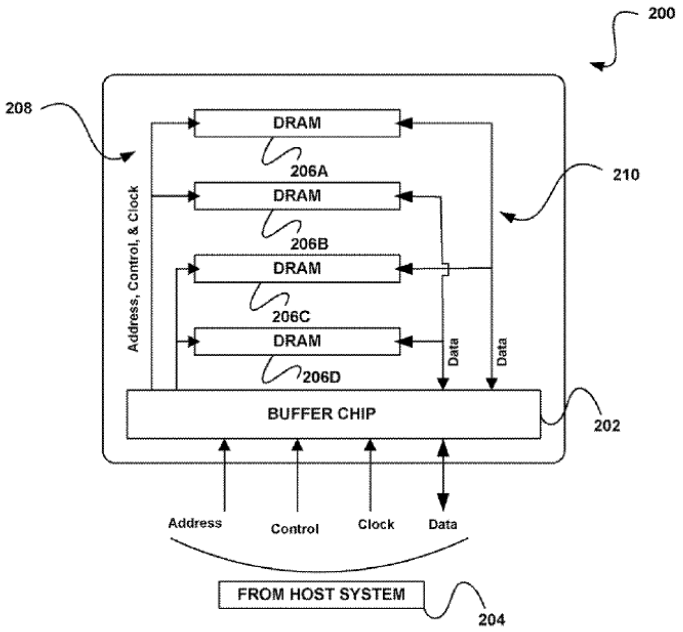


FIGURE 2B

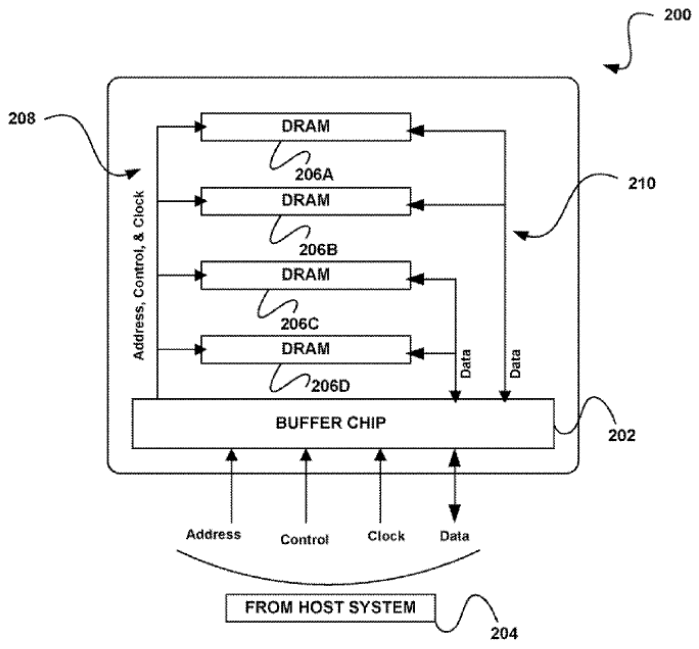


FIGURE 2C

Ex. 1011 (Rajan137), Figs.2B-2C.

70. A Restriction Requirement was issued on June 6, 2013, stating that Claims 1-28 cover "a memory package and a method for optimizing load in a memory package, classified in class 365, subclass 63," and Claims 29-34 cover "a memory module comprising a register device and a plurality of DRAM packages each comprising a plurality of DDR DRAM dies, classified in class 365, subclass 365/233.13." Ex. 1002 at p. 410.

71. On August 6, 2013, the applicants filed a response to the Restriction Requirement, amending Claims 1-34 and electing "without traverse the invention in Claims 1-28 as amended for examination" and amending Claims 29-34 "to include the particulars of claims 11-19 so that they related to the same subject matter as claims 11-19." Ex. 1002 at pp. 417-426.

72. The first Office Action was filed on October 11, 2013. Ex. 1002 at p. 433. Claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, and 34 were rejected as anticipated by US Pat. Pub. No. 2008/0025137 ("Rajan137") (Ex. 1011). *Id.* at pp. 437-42. Claims 6, 14, 25, and 26 were rejected as obvious over Rajan137 in view of Kirby (US 2011/0193226) (Ex. 1012). *Id.* at p. 442. Claims 30 and 32 were rejected as obvious over Rajan137 in view of Gervasi (US 2006/0259678) (Ex. 1013). *Id.* at pp. 442-43. Claims 8 and 22 were "objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims." *Id.* at p. 443.

73. On January 13, 2014, Applicant responded to the non-final Office Action by amending claims 8, 15-19, and 32, cancelling claims 5, 9, and 10, adding claims 35-37. Ex. 1002 at pp. 456-63. Applicant argued that Rajan137 did not anticipate the amended claims because Rajan137 "merely stacks DRAM circuits 206A-D, which are different from array dies." Ex. 1002 at p. 465. Applicant further contended that "[a]s a result, Rajan[137]'s buffer chip 202 also operates very differently from the control die in claim 1." *Id*. Applicant also provided the following arguments in response to the Examiner's rejection of claim 1:

> First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting claim 1, the Examiner states that Rajan (FIG. 2B) shows a memory package as recited in claim 1. The Examiner further cites Paragraph [0044] as disclosing the control die as recited in claim 1. Paragraph [0044] in Rajan, however, merely states:
>
> > As shown in each of such figures, the buffer chip 202 is placed electrically between an electronic host system 204 and a stack of DRAM circuits 206A-D. In the context of the present description, a stack may refer to any collection of memory circuits. Further, the buffer chip 202 may include any device capable of buffering a stack of circuits (e.g. DRAM circuits 206A-D, etc.). Specifically, the buffer chip 202 may be capable of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system 204. In this way, the stack of DRAM circuits 206A-D may appear as a smaller quantity of larger capacity DRAM circuits to the host system 204.

> Thus, the statements in this paragraph [0044] of Rajan says nothing about the existence of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals." According to this paragraph [0044], all that is required of the buffer chip 202 is the capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this requirement does not necessitate the use of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."
>
> Furthermore, according to paragraphs [0043] and [0044], this same capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system is required for each of the FIGS. 2A-2E, which show various configurations of a buffered stack of DRAM circuits 206A-D with the buffer chip 202. Since FIG. 2D of Rajan shows a single data bus between the buffer chip and all of the stacked DRAM circuits 206A-D (*Rajan, paragraph [0051]*), this capability of buffering the stack of DRAM circuits 206A-D, which also applies to the configuration in FIG. 2D, can not be said to imply the existence of first and second data conduits in the buffer chip 202 and a control circuit controlling the respective states of the first data conduit and the second data conduit in response to any received control signals, because the first and second data conduits would be coupled to a same data line in the single data bus in FIG. 2D and it would make no sense to try to control respective states or the first data conduit and the second data conduit.
>
> Therefore, Rajan fails to disclose each and every limitation in claim 1, and claim 1 is patentable over Rajan.

Ex. 1002 at pp. 465-67; *see also* Ex. 1011 (Rajan137) at Fig. 2D (discussed by applicant, reproduced below).

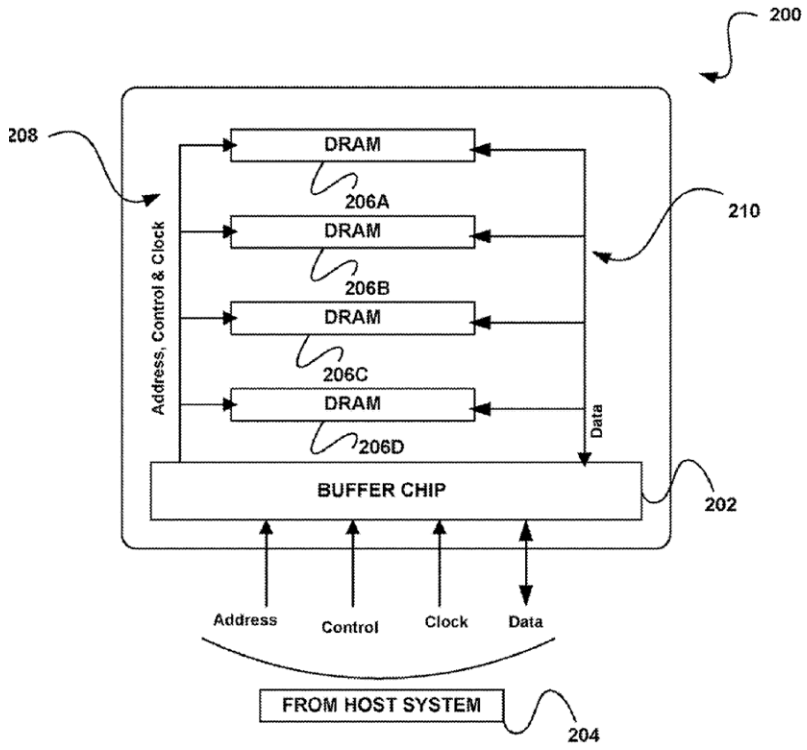


FIGURE 2D

74. On March 26, 2014, the Office issued a Notice of Allowance. Ex. 1002 at p. 474. The Examiner presented a few minor examiner's amendments but did not provide any statement on reasons for allowance. *Id.* at pp. 478-80.

75. On July 22, 2014, the 850 Application was issued as the 060 Patent with 34 claims. Ex. 1002 at pp. 483, 512.

3. The Prosecution History of the July 21, 2014 continuation application that issued as U.S. Patent No. 9,318,160

76. While the application for the 060 Patent (discussed above) was pending, the applicants filed a continuation application on July 21, 2014, which resulted in U.S. Patent No. 9,318,160. *See* Ex. 1006 at pp. 56, 58. Thus, it shares

the same disclosure and named inventors as the 060 Patent. The application for the 160 patent presented 9 claims at filing. Ex. 1006 at pp. 42-44.

77. On January 22, 2015, in a non-final Office Action, the Examiner rejected all claims under a nonstatutory double patenting rejection over the 060 Patent's claims. Ex. 1006 at pp. 73-77.

78. On July 22, 2015, the applicants cancelled Claims 1-9 and presented new Claims 10-29 to the Office for consideration and filed a terminal disclaimer. Ex. 1006 at pp. 84-90, 96.

79. On October 22, 2015, in a final Office Action, the Examiner again rejected all pending claims, citing insufficiencies in the terminal disclaimer, specifically because "[t]he terminal disclaimer identifies a party who is not the applicant." Ex. 1006 at pp.112-119.

80. On January 6, 2016, the applicants filed a terminal disclaimer with documentation showing the chain of title to the new applicant. Ex. 1006 at pp. 131-137, 143, 159-60.

81. On February 10, 2016, the Office issued a Notice of Allowance for the application for the 160 patent. Ex. 1006 at p. 171. The Examiner made two minor corrections in an Examiner's Amendment but made no statement of reasons for allowance. *Id.* at pp. 176-78. The 160 patent issued on April 19, 2016. *Id.* at pp. 185, 199.

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4. The Prosecution History of the April 11, 2016 continuation that issued as U.S. Patent No. 9,659,601

82. While the application for the 160 patent (discussed above) was pending, the applicants filed a continuation application on April 11, 2016, which resulted in U.S. Patent No. 9,659,601. *See* Ex. 1007 at pp. 59, 62. As a continuation of the 160 patent, the application for the 601 patent shares the same disclosure and named inventors as the 160 patent. The application resulting in the 601 patent presented 5 claims at filing, 1-5. Ex. 1007 at pp. 45-46.

83. On May 11, 2016, in a non-final Office Action, all claims were rejected for indefiniteness and non-statutory double patenting over the 160 patent and the 060 Patent. Ex. 1007 at pp. 66-74.

84. On September 12, 2016, the applicants amended Claims 1-5, added new Claims 6-21, and filed a terminal disclaimer. Ex. 1007 at pp. 101-109, 117.

85. On October 6, 2016, in a final Office Action, all pending claims were again rejected for non-statutory double patenting. Ex. 1007 at pp. 126-132. In response, the applicants refiled a terminal disclaimer that same day. Ex. 1007 at pp. 137-139.

86. On January 6, 2017, the applicants amended Claims 12, 16, and 21 and pointed to the terminal disclaimer that had been approved. Ex. 1007 at pp. 142-148.

87. On January 27, 2017, the Office issued a Notice of Allowance. Ex. 1007 at p. 152. No reasons were given for the allowance. *Id.* at p. 156. On February 14, 2017, the Examiner submitted a Supplemental Notice of Allowability with an Examiner's Amendment. Ex. 1007 at pp. 176-79. On April 7, 2017, another Supplemental Notice of Allowability was mailed to the applicants in response to an IDS filed by the applicants on March 27, 2017. Ex. 1007 at pp.194-199.

88. U.S. Patent No. 9,659,601 issued from the 288 Application on May 23, 2017. Ex. 1007 at pp. 170, 208.

5. The Prosecution History of the May 22, 2017 continuation application that issued as U.S. Patent No. 10,290,328

89. While the application for the 601 patent (discussed above) was pending, the applicants filed a continuation application on May 22, 2017, which resulted in U.S. Patent No. 10,290,328. Ex. 1008 at pp.58, 62. The application resulting in the 328 patent presented 10 claims at filing. Ex. 1008 at pp. 44-45.

90. On July 27, 2017, in a non-final Office Action, Claim 9 was rejected for being indefinite and all claims were rejected for nonstatutory double patenting over the 601 patent, the 160 patent, and the 060 Patent. Ex. 1008 at pp. 65-73.

91. On December 27, 2017, the applicants amended Claims 1-4, 6-7, and 9 and presented new Claims 11-20 and filed terminal disclaimers. Ex. 1008 at pp. 80-90.

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92. On February 26, 2018, in a final Office Action, and the follow-on final Office Action on May 31, 2018, pending Claims 1-20 were again rejected on the grounds of nonstatutory double patenting over the 601 patent and 160 patent. Ex. 1008 at pp. 105-112, 115-126.

93. On July 2, 2018, the applicants responded to the Office Action and filed new terminal disclaimers. Ex. 1008 at pp. 129-140.

94. On August 1, 2018, a Notice of Allowance was sent to the applicants. Ex. 1008 at pp. 147-53.

95. On October 29, 2018, the applicants filed a Request for Continued Examination along with an Information Disclosure Statement with over 100 references. Ex. 1008 at pp. 162-184.

96. On December 26, 2018, another Notice of Allowance was sent to the applicants with no statement on reasons for allowability. Ex. 1008 at pp. 213-217. On March 26, 2019, the applicants submitted an Amendment after Notice of Allowance, making amendments to Claims 1, 10, 12, and 19. Ex. 1008 at pp. 271-278.

97. U.S. Patent No. 10,290,328 issued on May 14, 2019. Ex. 1008 at pp. 220, 282.

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6. The Prosecution History of the May 14, 2019 continuation application that issued as U.S. Patent No. 10,902,886

98. While the application for the 328 patent (discussed above) was pending, the applicants filed a continuation application on May 14, 2019, which resulted in U.S. Patent No. 10,902,886. *See* Ex. 1009 at pp. 59, 65. The application that resulted in the 886 patent presented 1 claim at filing. Ex. 1009 at p. 14.

99. On October 3, 2019, Claim 1 was rejected as failing to comply with the written description requirement regarding "a printed circuit board" and for nonstatutory double patenting over the 060 Patent, the 160 patent, the 601 patent, and the 328 patent. Ex. 1009 at pp. 103-111.

100. On March 3, 2020, the applicants cancelled Claim 1 and submitted new Claims 2-21. Ex. 1009 at pp. 132-141.

101. On June 9, 2020, in a final Office Action, all pending claims were rejected for nonstatutory double patenting in view of the 328 patent, the 601 patent, the 160 patent, and the 060 Patent. Ex. 1008 at pp. 182-191.

102. On September 9, 2020, the applicants submitted a terminal disclaimer as well as a McKesson Statement, pointing to Application No. 15/470,856 and 13/970,606 as applications potentially containing information relevant to the pending application. Ex. 1009 at pp. 206-216.

103. On September 17, 2020, the Office issued a Notice of Allowance. Ex. 1009 at pp. 219-25.

104. On November 23, 2020, the Office issued a Corrected Notice of Allowability. Ex. 1009 at pp. 261-64.

105. On December 16, 2020, the applicants amended Claim 19. Ex. 1009 at pp. 279-285, 294-95.

106. U.S. Patent No. 10,902,886 issued on January 26, 2021. Ex. 1009 at pp. 231, 299.

7. Application No. 17/157,903 (abandoned)

107. The applicants filed U.S. Patent Application No. 17/157,903 ("903 Application"), titled "Memory Module with Buffered Memory Packages," on January 25, 2021. Ex. 1010 at p. 61. The 903 Application is a continuation of the 885 patent. Ex. 1010 at pp. 6-7, 64. The 903 Application presented 1 claim at filing. Ex. 1010 at p. 57.

108. On May 12, 2021, the claim was rejected as being indefinite and for nonstatutory double patenting in view of the 060 Patent, the 160 patent, the 601 patent, the 328 patent, and the 886 patent. Ex. 1010 at pp. 83-90.

109. On September 13, 2021, the applicant responded by cancelling Claim 1, submitting new Claims 2-21, and submitting a terminal disclaimer. Ex. 1010 at pp. 105-113.

110. On December 13, 2021, Claims 5 and 16 were objected to because of informalities and all pending claims were rejected for nonstatutory double

patenting over the 886 patent, the 601 patent, the 160 patent, and the 060 Patent. Ex. 1010 at pp.150-161.

111. The applicants did not respond to this rejection, and the application was deemed abandoned on July 6, 2022. Ex. 1010 at pp. 191-92.

E. Construction of Terms Used in the 160 Patent Claims

112. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the 160 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted some of the claim terms broadly for purposes of infringement, *see, e.g.*, Ex. 1044 at 63-68; Ex. 1046 at 63-69, and that a narrower interpretation may be more reasonable, in my opinion the claims are obvious under either interpretation, as shown by my analysis below.

IV. OVERVIEW OF THE PRIOR ART

113. Below is an overview of the primary prior art references that I considered when analyzing the validity of the claims of the 160 Patent.

A. Prior Art

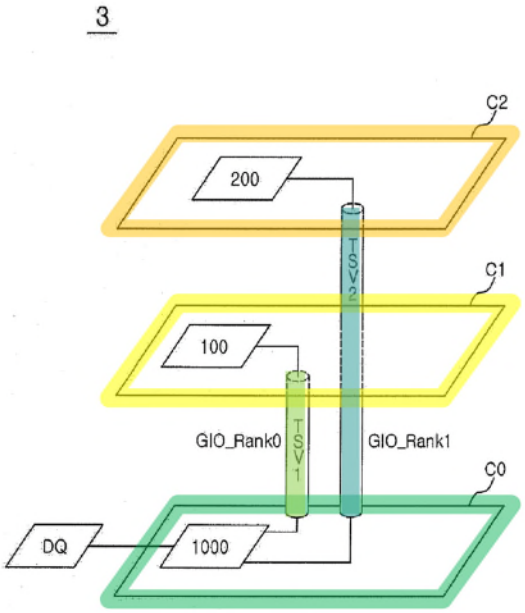
1. U.S. Patent Publication No. 2011/0103156 by Kim et al. (Ex. 1014)

114. U.S. Patent Application No. 12/648,997 by Kim et al. ("Kim"), titled "Data Input/Output Circuit and Semiconductor Memory Apparatus Having the

Same," was filed on December 29, 2009, and was published as U.S. Patent Pub. No. 2011/0103156 on May 5, 2011. Ex. 1014 (Kim) at 1. Kim was not cited during prosecution of the 160 Patent. *See* Ex. 1001 (the 160 Patent) at 2 ("U.S. PATENT DOCUMENTS").

115. Kim discloses that "a semiconductor memory apparatus 3 comprises a main chip C0 [(green)] and a plurality of slave chips C1 [(yellow)] and C2 [(orange)]. The chips C0, C1 and C2 are connected by TSVs [(light green and teal, respectively)]." Ex. 1014 (Kim) at [0047] and Fig. 5 (reproduced below, annotated). Kim explains that, "[a]lthough only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used." *Id*. at [0048].

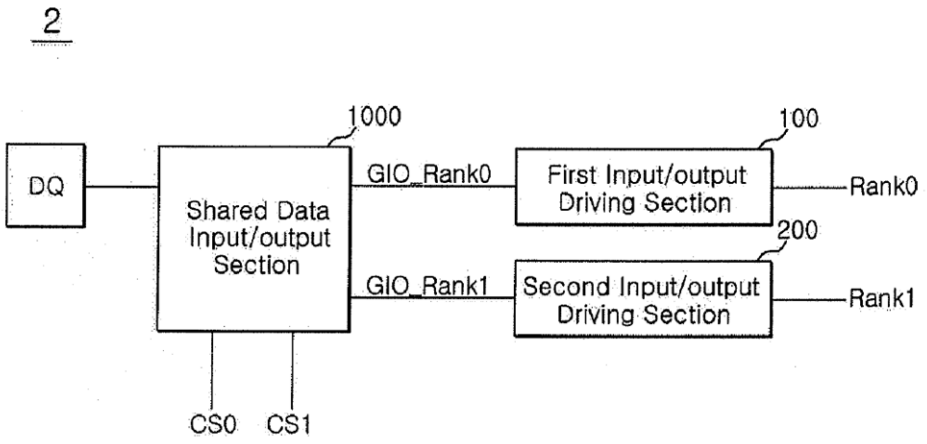
FIG.5



116. The main chip C0 (green) includes an input/output section (1000) that is shared by the slave chips C1 (yellow) and C2 (orange). Ex. 1014 (Kim) at [0048]. "When assuming that the first slave chip C1 is designated as the first rank Rank0 and the second slave chip C2 is designated as the second rank Rank1, the first chip selection signal CS0 becomes a signal for selecting the first slave chip C1, and the second chip selection signal CS1 becomes a signal for selecting the second slave chip C2. Data transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0 comprises a TSV TSV1 [(light green)] which connects the first slave chip C1 and the main chip C0. Data transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1 comprises a TSV TSV2 [(teal)] which connects the second slave chip C2 and the main chip C0." *Id*. at [0049].

117. Kim also explains that its inventive "semiconductor memory apparatus 2 may allow a read operation and a write operation to be selectively performed for one of the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, whereby it is possible to prevent a data collision from occurring." Ex. 1014 (Kim) at [0031] and Fig. 2 (reproduced below).

FIG.2



2. U.S. Patent No. 8,041,881 to Rajan et al. ("Rajan") (Ex. 1015)

118. U.S. Patent No. 8,041,881 to Rajan et al. ("Rajan"), titled "Memory Device with Emulated Characteristics," issued on October 18, 2011, from U.S. Patent Application No. 11/762,010 filed on June 12, 2007. Ex. 1015 (Rajan) at p.1. A continuation of Rajan is U.S. Patent No. 8,019,589 which was cited but not discussed during prosecution of the 060 Patent. *See, e.g.*, Ex. 1002 (the 060 Patent file history) at pp.437-45. The Examiner cited and discussed a different patent application from the same inventors (US2008/0025137, Ex. 1011) with a different disclosure, as discussed above in ¶¶ 69-75.

119. Rajan is directed to "an effective way to make use of low cost memory chips in manufacturing high capacity memory modules," including the use of a memory device including stacked DRAM chips (yellow and orange) and a buffer chip (green) for interfacing with a host system. Ex. 1015 (Rajan) at 1:51-60,

4:48-50 and Fig. 4 (reproduced below, annotated). Rajan discloses a number of ways for connecting the stacked DRAM chips (yellow and orange) and the buffer chip (green), including using two data busses (light green and teal) and a common bus for address, control, and clock signals. *Id*. at 2:6-7.

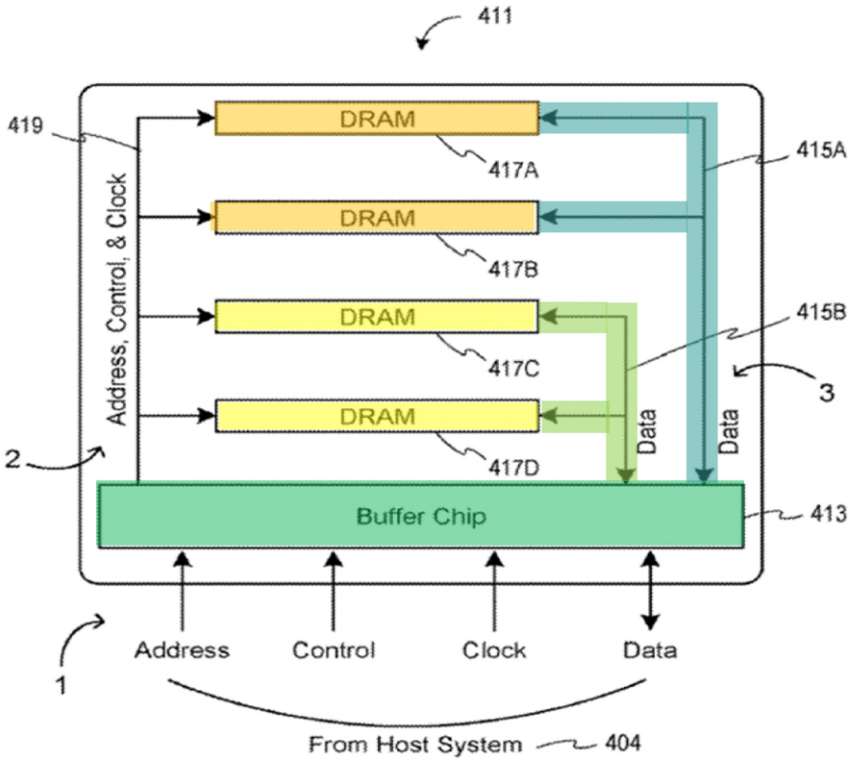


FIG. 4

120. Rajan further teaches that the interface may comply with JEDEC standards, and include "a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system, and a system

data signal interface for sending/receiving data signals to/from the host system." Ex. 1015 (Rajan) at 4:20-24, 14:11-18 and Fig. 18 (reproduced below). Rajan also discloses that "[t]he interface circuit includes emulation logic which operates according to the stored memory physical attributes and the stored system emulation attributes, to present to the system an interface to an emulated memory which differs in at least one attribute from the actual physical memory." *Id*. at 14:51-62.

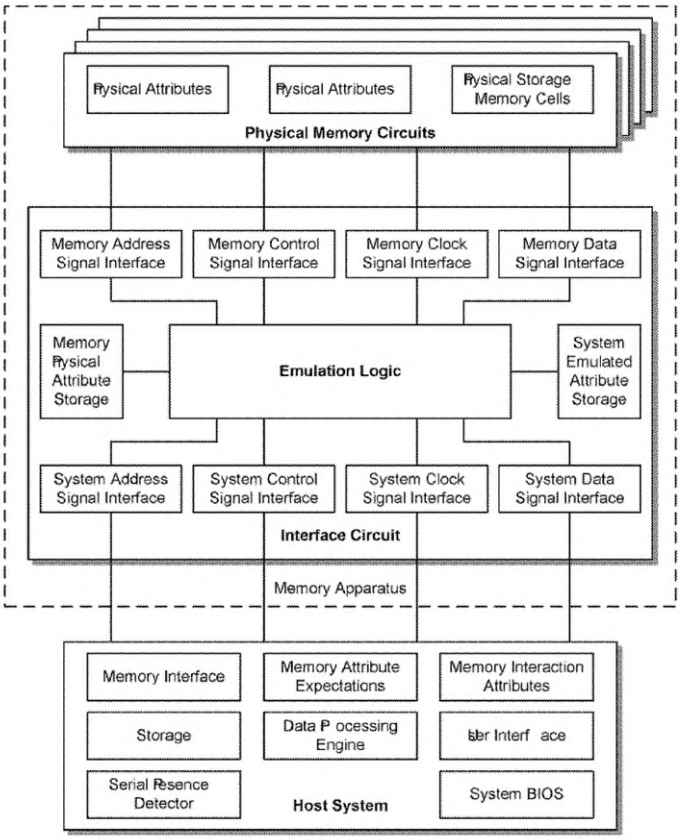


FIG. 18

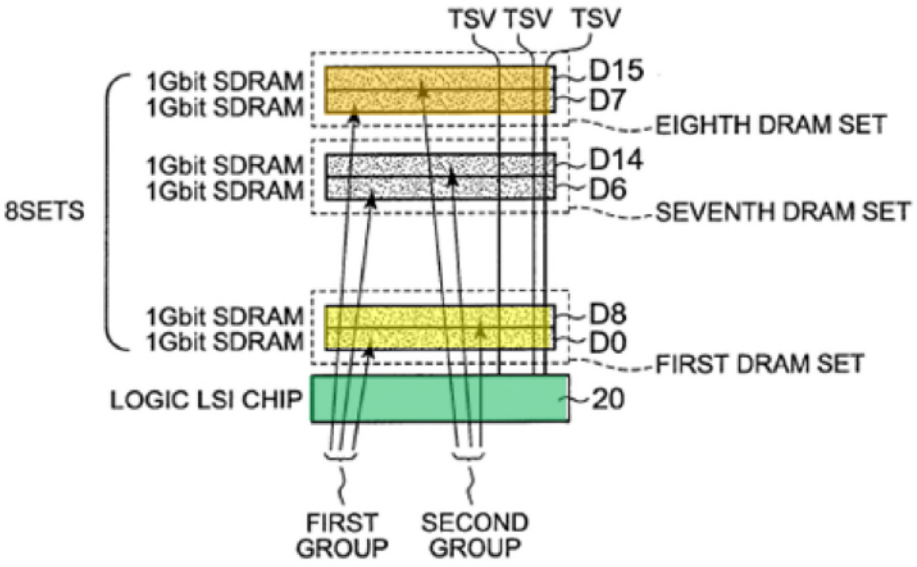
3. U.S. Patent Publication No. 2011/0026293 by Riho (Ex. 1016)

121. U.S. Patent Application No. 12/838,028 titled "Semiconductor Device" was filed on July 16, 2010, and published as U.S. Patent Publication No.

2011/0026293 by Riho ("Riho") on February 3, 2011. Ex. 1016 (Riho) at 1. Riho was not cited during prosecution of the 160 Patent. *See* Ex. 1001 (the 160 Patent) at 2 ("U.S. PATENT DOCUMENTS").

122. Riho discloses a memory package including a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15) "integrally packaged" and connected to the control chip by through-silicon vias (TSVs). Ex. 1016 (Riho) at Fig. 1 (reproduced below, annotated).

FIG. 1

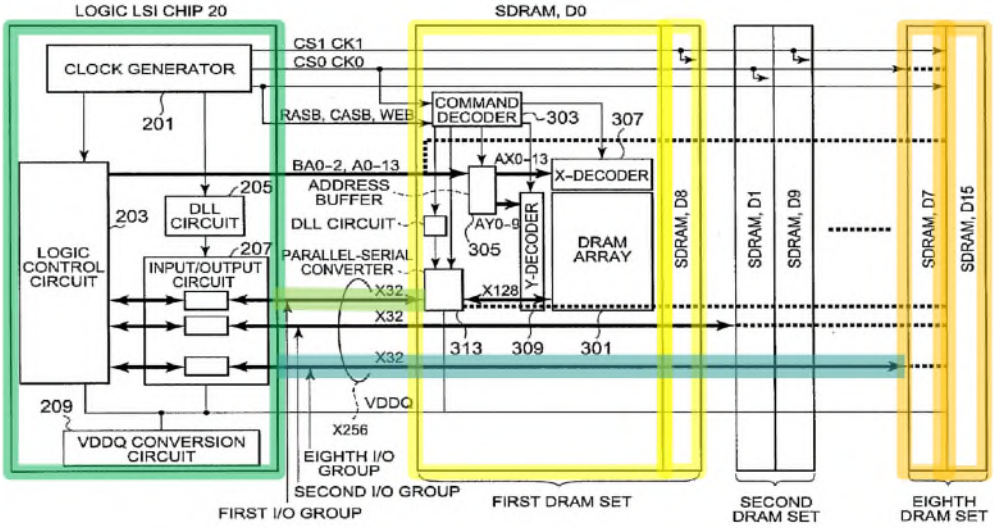


123. In particular, Riho discloses organizing the memory chips into pairs that share TSVs for data communication, such as a first DRAM set including SDRAM pair D0 and D8 (yellow) at the bottom of the stack up to the eighth DRAM set including SDRAM pair D7 and D15 (orange) at the top of the stack.

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Id. at Fig. 2 (reproduced below, showing internal structure of the stack, including (x32) data connections to SDRAM pair D0 and D8, light green, and to SDRAM pair D7 and D15, teal).

FIG. 2



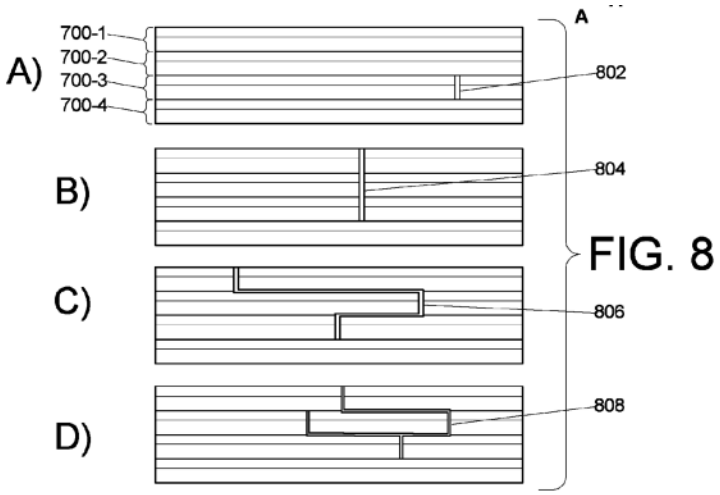
124. Riho explains that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 (Riho) at [0103]. Riho also discloses "a structure in which only either one of each of SDRAM pairs forming sets (DRAM sets) and sharing data signal DQ TSVs, respectively, is connected to the corresponding shared data signal DQ TSV while the other SDRAM is completely disconnected from the corresponding shared data signal DQ TSV, thereby not only compensating for phase variations of data signals DQ, but also reducing by half the

load capacitance of data buses formed by the data signal DQ penetrating through electrodes TSV." *Id*. at [0110].

4. U.S. Patent No. 7,969,192 to Wyman et al. (Ex. 1017)

125. U.S. Patent No. 7,969,192 to Wyman et al. ("Wyman"), titled "Variable Off-Chip Drive," issued on June 28, 2011, from U.S. Patent Application No. 12/732916 filed on March 26, 2010, as a division of an application filed in 2007. Ex. 1017 (Wyman) at 1. Wyman was not cited during prosecution of the 160 Patent. *See* Ex. 1001 (the 160 Patent) at 2 ("U.S. PATENT DOCUMENTS").

126. Wyman discloses that, "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 (Wyman) at 1:22-24. "The reduced path distances of stacked hybridized chips therefore require less drive to adequately drive a signal to an off-chip board and/or chip. These conditions warrant the use of restructuring the drive portion of existing chip architecture." *Id*. at 1:45-48. For example, Wyman discloses that longer interconnects in a stacked arrangement require larger drive. *Id*. at Fig. 8 (reproduced below).



127. In particular, Wyman teaches that a short "through-chip via connection (802) … would require minimal drive" (Fig. 8A) but "a longer through-chip via connection (804)" (Fig. 8B) has "increased resistance, capacitance and impedance …[which] might require additional drive." Ex. 1017 (Wyman) at 6:15-30. However, "the total drive … would be overkill." *Id*. at 6:44-50.

5. U.S. Patent Publication No. 2010/0195364 by Riho ("Riho2") (Ex. 1018)

128. U.S. Patent Application No. 12/656,485 by Riho ("Riho2"), titled "Semiconductor Device," was filed on February 1, 2010, and was published as U.S. Patent Pub. No. 2010/0195364 on August 5, 2010. Ex. 1018 (Riho2) at 1. Riho2 was not cited during prosecution of the 160 Patent. *See* Ex. 1001 (the 160 Patent) at 2 ("U.S. PATENT DOCUMENTS"). The Riho and Riho2 references have the same named inventor.

129. Riho2 discloses "a semiconductor device formed by stacking a plurality of chip dies." Ex. 1018 (Riho2) at [0003]. Riho2 explains that "the

fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the fac[t] that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips." *Id*. at 10.

130. To solve these problems, Riho2 discloses "a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097] and Fig. 7A (reproduced below).

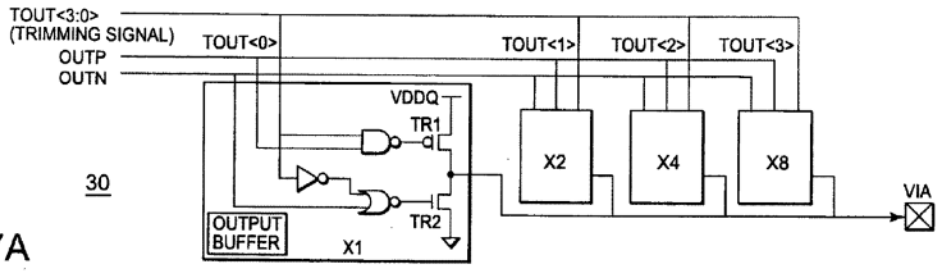


FIG. 7A

B. Background Technology

1. JEDEC Standards

131. In my opinion, a Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See supra* ¶ 60; Ex. 1023, p. 9 & Fig. 16; Ex. 1022, pp. 332-35, 318-20. For example, Riho discloses Double Data Rate (DDR) SDRAM memory devices. *See* Ex. 1016 at [0027]. A Skilled Artisan would have readily understood that these memories were already standardized by JEDEC and that these standard were available and well-known. *See, e.g.*, Ex. 1015 (Rajan) at 8:6-15 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals that a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals. For example, the JEDEC specification for DDR2 DRAM is known as JESD79-2B.") A Skilled Artisan would have also understood that JEDEC also standardized memory modules and corresponding interface circuits, such as "a register, an AMB, a buffer, or the like." *Id*. at 4:20-24.

132. Furthermore, a Skilled Artisan would have also been familiar with the standard developing process at JEDEC, including proposals for the standards that were being developed at the time. Indeed, the 893 Provisional describes a

"proposed three-dimensional stacking (3DS) standard for dual in-line memory modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC)." Ex. 1005 (the 893 Provisional) at [0004]. The 893 Provisional also describes "a DDR3 JEDEC standard register with a 'rank multiplication' circuit" as part of the "proposed 3DS-DIMM standard" to address the shortcomings of the existing JEDEC RDIMM and LRDIMM standards for memory modules. *Id*. at [0005].

133. Therefore, in my opinion, a Skilled Artisan would have been familiar with the technology described in the JEDEC standards that existed and were being developed at the time. Examples of such standards include the JEDEC standard for DDR3 memory devices, *see* Exhibits 1019-21, and the JEDEC specification for GDDR4 memory devices, *see* Exhibit 1035.

2. Electrical load and drivers

134. In my opinion, a Skilled Artisan also would have been familiar with the electrical loads of circuitry used in stacked memory devices and the corresponding driving requirements to drive the load of such circuitry. For example, the 160 Patent's description of the prior art explains that, "[g]enerally, a load exists on each of the drivers 134, 140, 184, and 186 [in the control chip of the stack, *see supra* ¶61,] by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the

array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power." Ex. 1001 (the 160 Patent) at 2:10-17.

135. Indeed, a Skilled Artisan would have understood that a capacitive load creates timing delays that have to be taken into account when designing the corresponding driving circuits, as was taught in textbooks at the time. *See, e.g.*, Ex. 1030 (Brown) at 132-138. Consider, for example, "an inverter N_1 that drives the inputs of *n* other inverters. Each of the other inverters contributes to the total capacitive loading on node *f*. … For simplicity, assume that each inverter contributes a capacitance C and that $C_n = n \times C$ … [The result is that] the propagation delay increases in direct proportion to *n*." *Id*. at p.134 (Fig. 3.55, reproduced below).

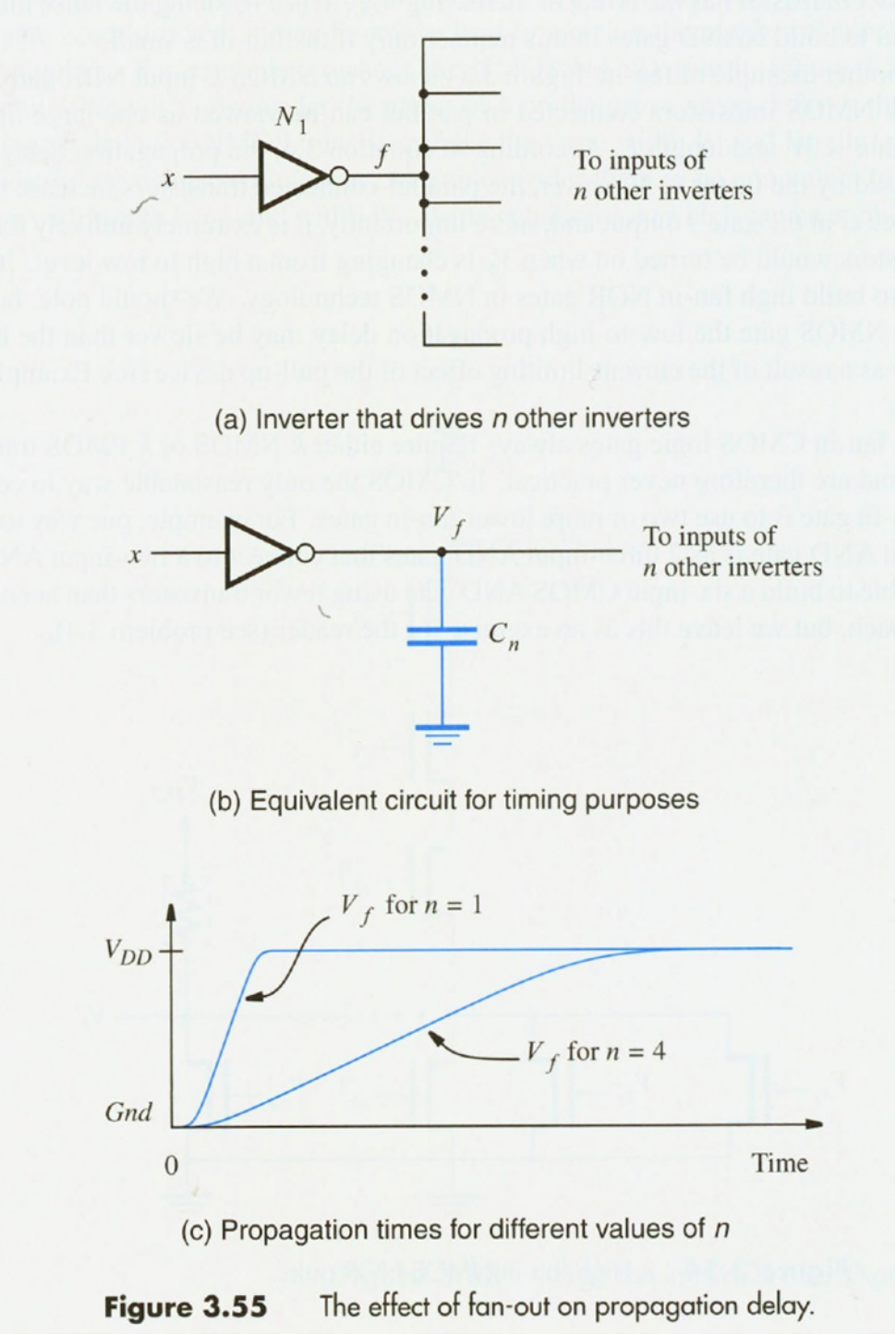


Figure 3.55 The effect of fan-out on propagation delay.

136. In order to "drive a large capacitive load, buffers are often used to improve performance." Ex. 1030 (Brown) at p.135. "Buffers can be created with different amounts of drive capability, depending on the sizes of the transistors ….

In general, because they are used for driving higher-than-normal capacitive loads, buffers have transistors that are larger than those in typical logic gates." *Id*. "In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices. Buffers can handle relatively large amounts of current flow because they are built with large transistors." *Id*. at 135-136. "In general, fan-out, capacitive loading, and current flow are important issues that the designer of a digital circuit must consider carefully. In practice, the decision as to whether or not buffers are needed in a circuit is made with the aid of CAD tools." *Id*. at 136. A well-known example of such buffers is a tri-state buffer, which has a third state that produces no output signal (called the "high-impedance state"). *Id*. at 136-138.

3. Rank multiplication

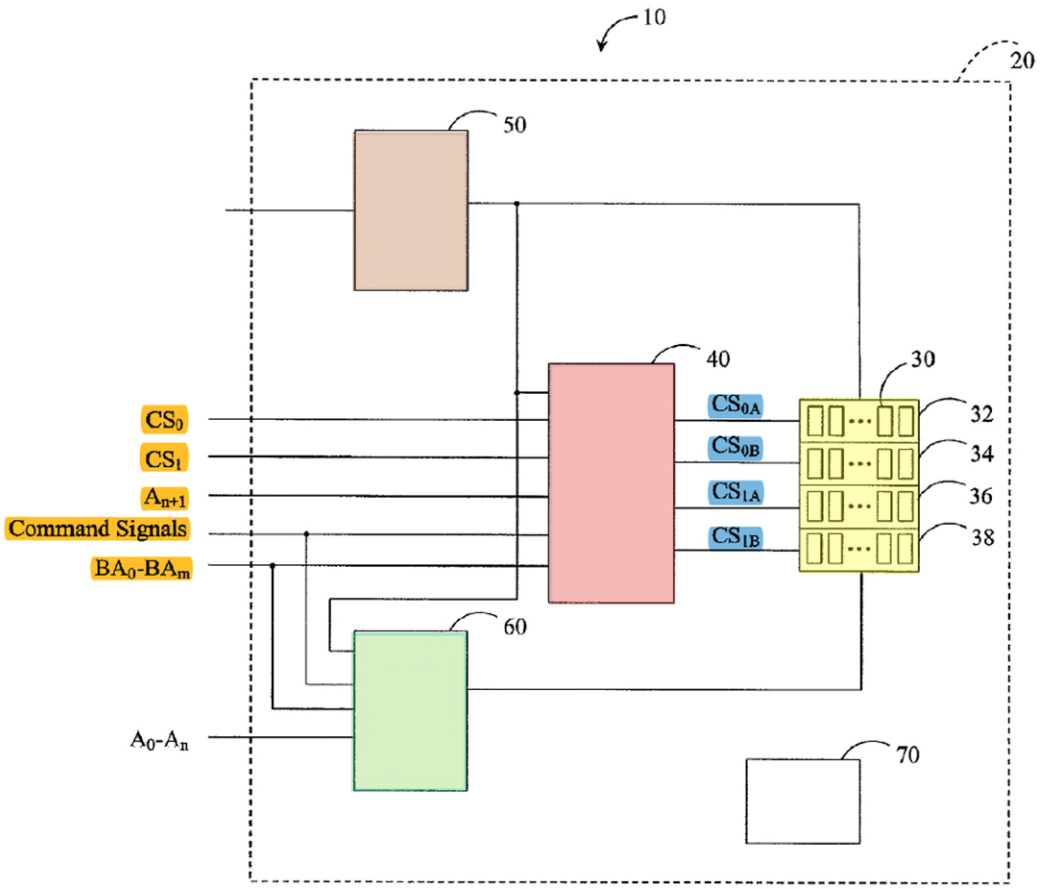
137. In my opinion, a Skilled Artisan also would have been familiar with "rank multiplication" at the time. For example, the 160 Patent discloses that rank multiplication was known at the time. Ex. 1001 (the 160 Patent) at 22:22-24 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537). For example, the '386 patent discloses that a memory module can appear to the computer system as if it has two ranks of higher density (and more expensive) memory devices, when in reality it physically has four ranks

of lower density (and less expensive) memory devices. Ex. 1028, 4:47-5:10, 32:58-33:16; *see also* Ex. 1041 (Bigler) at 2:15-19 ("Thus, from an environment outside of the common package 140, the multi-die memory 100 may… appear as a single memory unit or as a monolithic memory unit.") and 2:36-40 ("According to some embodiments according to the invention, the distribution of the groups 160, 170 of memory banks may for example allow for an increase of a data rate on some data connections within the common package 140."). This is commonly called "rank multiplication," and can result in substantial cost savings, providing a motivation to implement the technique in a wide range of memory packages and memory modules. (Indeed, I understand that Patent Owner's claims in the '386 and '537 patents were found invalid by even earlier prior art rendering obvious "rank multiplication." *See* Exs. 1029, 1032-33.)

138. In particular, the '386 patent (Ex. 1028) discloses that "the ranks of a memory module are selected or activated by address and command signals," which include "chip-select signals." Ex. 1028 at 2:34-38. In the'386 patent, a memory module (10) can include a number of memory devices (30, yellow) and a logic element (40, red) which receives a set of input control signals (orange), including address signals and two chip select signals (CS_0, CS_1), from a system memory controller (not shown). Ex. 1028 at 5:11-50 and Fig. 1A (reproduced below, annotated); *see also id*. at 6:63-7:5. In response, the logic element 40 generates

four chip select signals (blue, CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) to control the memory devices 30 (yellow). *Id*. at 7:6-8:45.

Figure 1A:



139. Therefore, the ***two*** chip select signals received by the logic element 40 from the system memory controller correspond to ***two*** ranks, but the memory devices (yellow) on the module are organized into ***four*** ranks 32, 34, 36, 38, which each receive a respective one of the ***four*** chip select signals (blue) generated by the logic element (40). *Id*. For example, the additional chip select signals are generated based on an address signal (A_{n+1}). *Id*. at 8:1-45. The '386 patent also

explains that, to implement this rank multiplication, an isolation device is needed to avoid certain data collisions. Ex. 1028 at 24:41-56. Such an isolation device (120) can selectively isolate the load of the memory devices to "reduce the load impedance of the memory module 10 on the computer system." *Id*. at 26:12-19 and Fig. 6D (reproduced below); *see also* Ex. 1031 (the '537 patent) at 6:48-62.

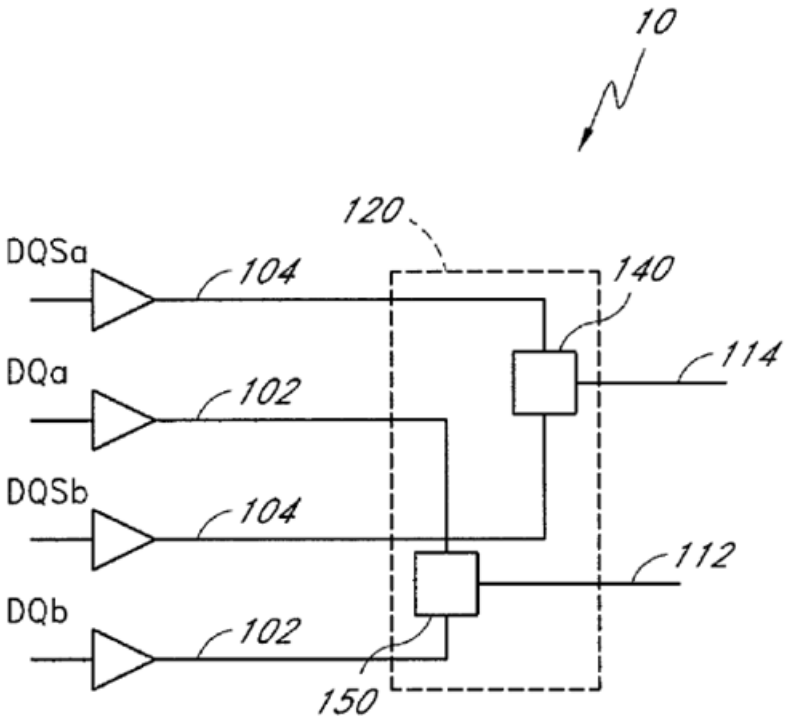


FIG. 6D

140. The '386 patent discloses an example where the rank multiplication is implemented in a logic device that can be combined with a register device and a PLL, but is a separate component from the memory devices. Ex. 1028 at 5:42-48 ("While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in

certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component."). A Skilled Artisan would have also understood that rank multiplication can be implemented within a single memory package. *See, e.g.,* Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack."); *see also* Ex. 1041 (Bigler) at 2:15-19 ("Thus, from an environment outside of the common package 140, the multi-die memory 100 may… appear as a single memory unit or as a monolithic memory unit."). Therefore, a Skilled Artisan would have also understood that rank multiplication can be implemented in either the memory package or in a separate module controller, or both. *See, e.g.,* Ex. 1001 (the 160 Patent) at Fig. 7 (reproduced below, showing a prior art module with rank multiplication implemented in both module controller 712 and memory package control chip 722) and 18:26-58 ("FIG. 7 schematically illustrates an example memory module 700 that has previously been proposed for the 3DS-DIMM standard. … The 3DS register 712 may include a DDR3 JEDEC standard

register with a 'rank multiplication' circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller. … The 3DS DRAM package 720 may comprise a plurality of array dies (e.g., 2, 4 or 8 DDR DRAM dies) and a controller die 722. The controller die 722 may include … a programmable secondary 1-to-2 rank decoder …").

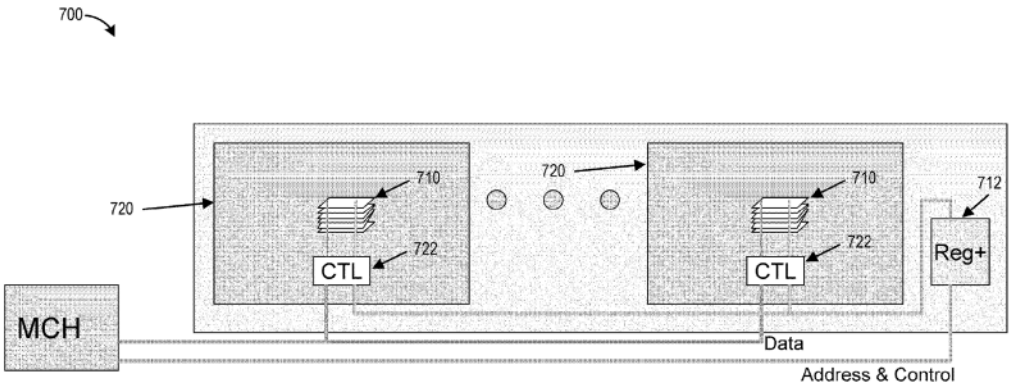


FIG. 7

C. The Combinations Relied on Here

141. The combinations analyzed here were obvious to a Skilled Artisan at the time and are straightforward applications of the teaching of the prior art. Each of the Grounds discussed below involves the combination of prior art references in view of the knowledge of a Skilled Artisan.

142. Ground 1 involves Kim in view of Rajan and Wyman.

143. Ground 2 involves Riho in view of Rajan and Riho2.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 160 PATENT

144. My analysis below is based on my understanding of the law and the other information discussed above, including the two Grounds discussed above.

A. Reasons to Combine for Ground 1

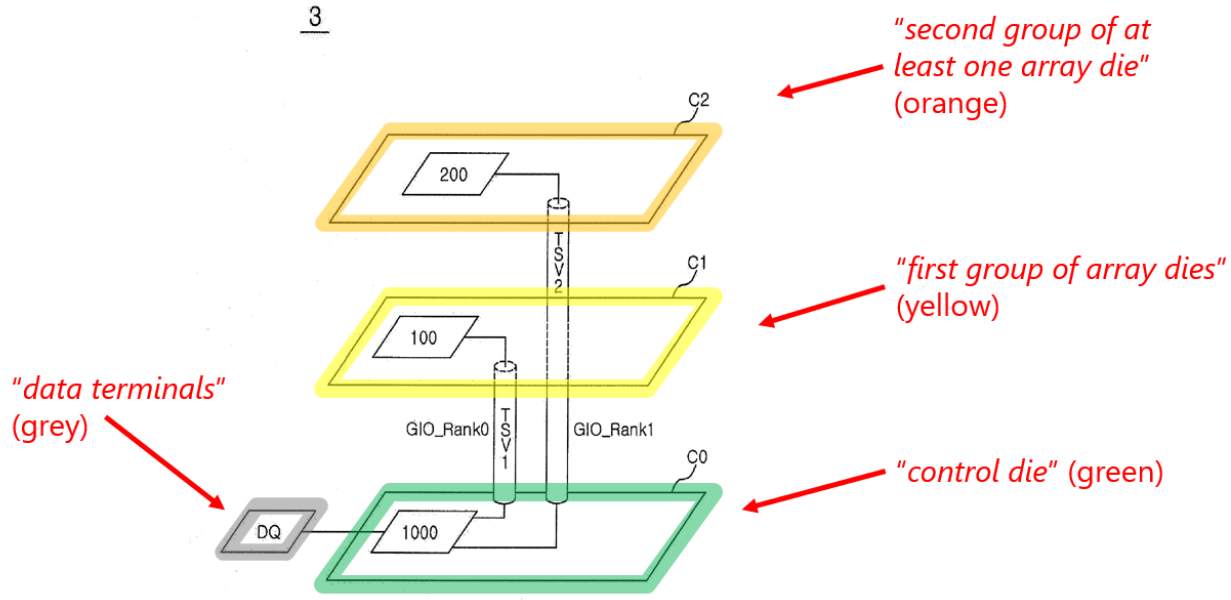
145. A Skilled Artisan would have been motivated to make the combinations in Ground 1 for at least the following reasons.

1. Ground 1: Kim in view of Rajan and Wyman

146. As mentioned above, Ground 1 involves Kim in view of Rajan and Wyman. *Supra* ¶142.

147. As discussed below in detail with reference to specific claim limitations, Kim discloses a memory package that includes stacked memory chips, like C1 (yellow) and C2 (orange), and a main chip C0 (green) including a shared data input/output section 1000. Ex. 1014 (Kim) at Fig. 5 (reproduced below, annotated). Kim expressly discloses a data pad DQ (grey) to communicate data with external devices (*data terminals*) and further explains that "write and read command signals [*control terminals*] [are] applied from a device external to the semiconductor memory apparatus." *Id*. at [0038]. A Skilled Artisan would have understood from this disclosure that Kim's memory package includes "*data terminals and control terminals*" as required by the 160 Patent claims.

FIG.5



148. Furthermore, the claimed terminals and corresponding data and control/address signals would have also been obvious over Kim in view of the teachings of Rajan. *See, e.g.*, Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, showing a memory package including stacked memory chips (yellow and orange) and a buffer chip (green) which has input/output terminals for data and control/address signals communicated with a host system).

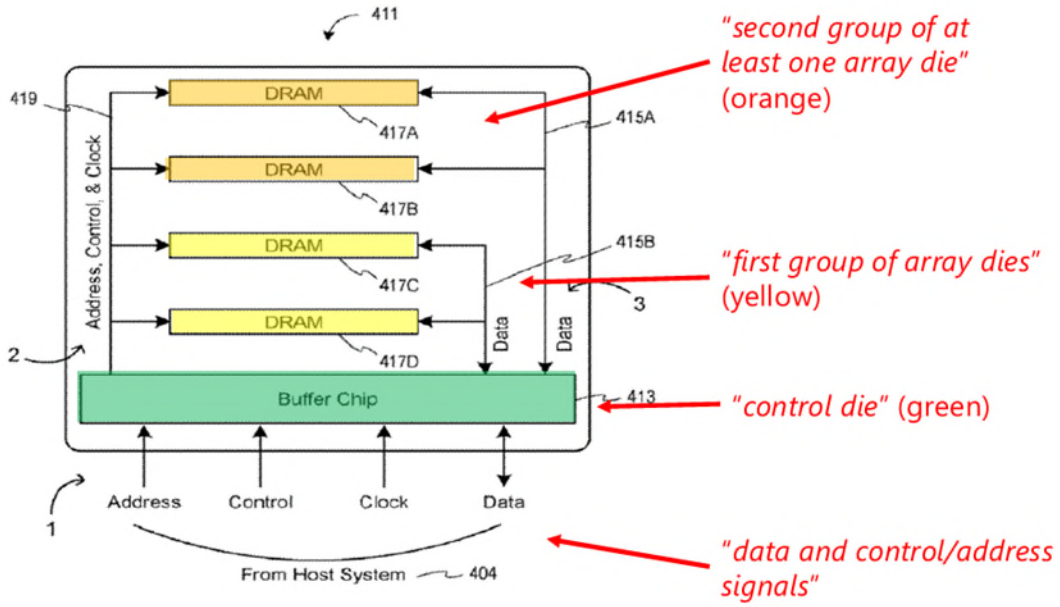


FIG. 4

149. For example, a Skilled Artisan would have been motivated to implement the functionality of a JEDEC compatible external data interface as suggested by Rajan in the control chip of Kim to make Kim's stacked memory package compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory."); *see also id.* at Fig. 18 (reproduced below, disclosing that an interface circuit includes emulation logic which interfaces, on one side with the host system and, on the other side, with the physical memory circuits).

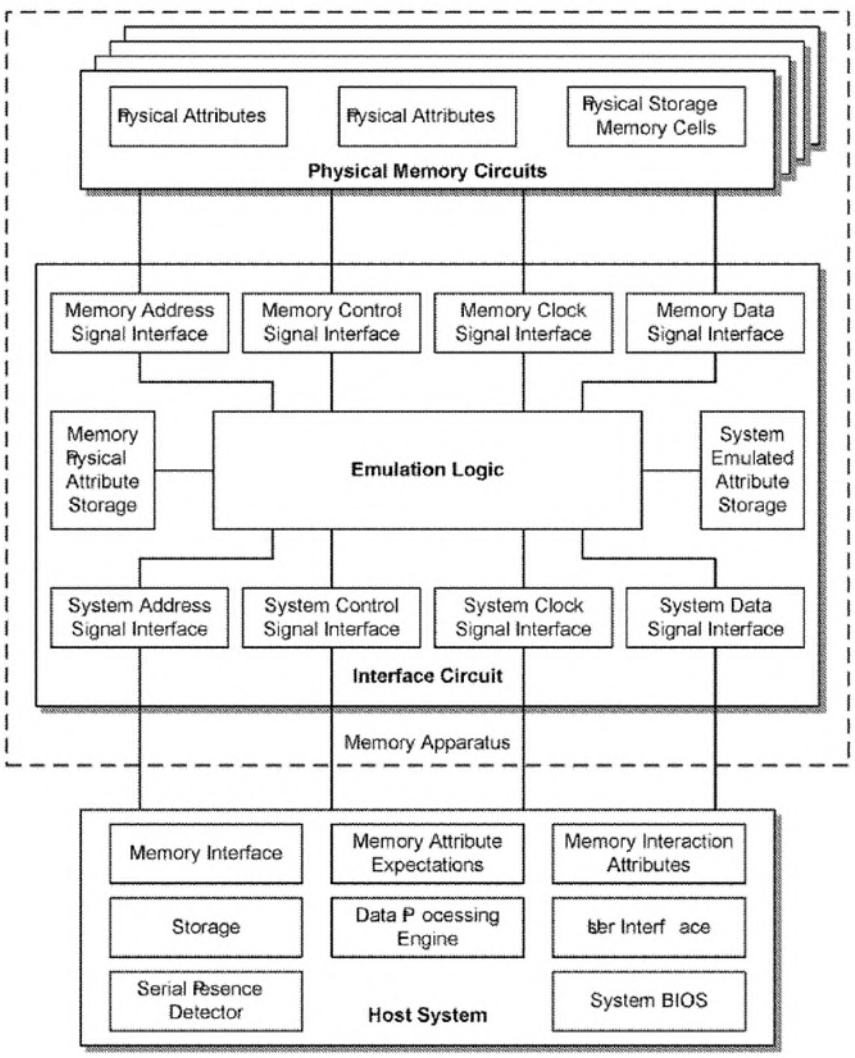


FIG. 18

150. Rajan is analogous art to Kim and the 160 Patent, as each is directed to the problem of effective operation of memory devices, including interfacing with stacked memory devices. Ex. 1015 (Rajan) at 1:51-60 ("What is needed, then, is an effective way to make use of low cost memory chips in manufacturing high capacity memory modules. … A memory subsystem is provided including an interface circuit adapted for communication with a system and a majority of address or control signals of a first number of memory circuits."), 4:48-50 ("In one

embodiment, the DRAM chips are stacked, and the buffer chip is placed electrically between them and the host system."); Ex. 1014 (Kim) at [0012] ("Various aspects of the present invention comprise a semiconductor memory apparatus capable of sharing a data input/output circuit."), [0050] ("It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked."); Ex. 1001 (160 Patent) at 1:20-23 ("The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:26-29 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

151. Therefore, a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about control and address signals for memory packages. Rajan discloses the same basic structure of a memory package like Kim and the 160 Patent: the package includes stacked memory chips and a shared interface circuit, called "buffer chip" in Rajan. Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated), 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses.").

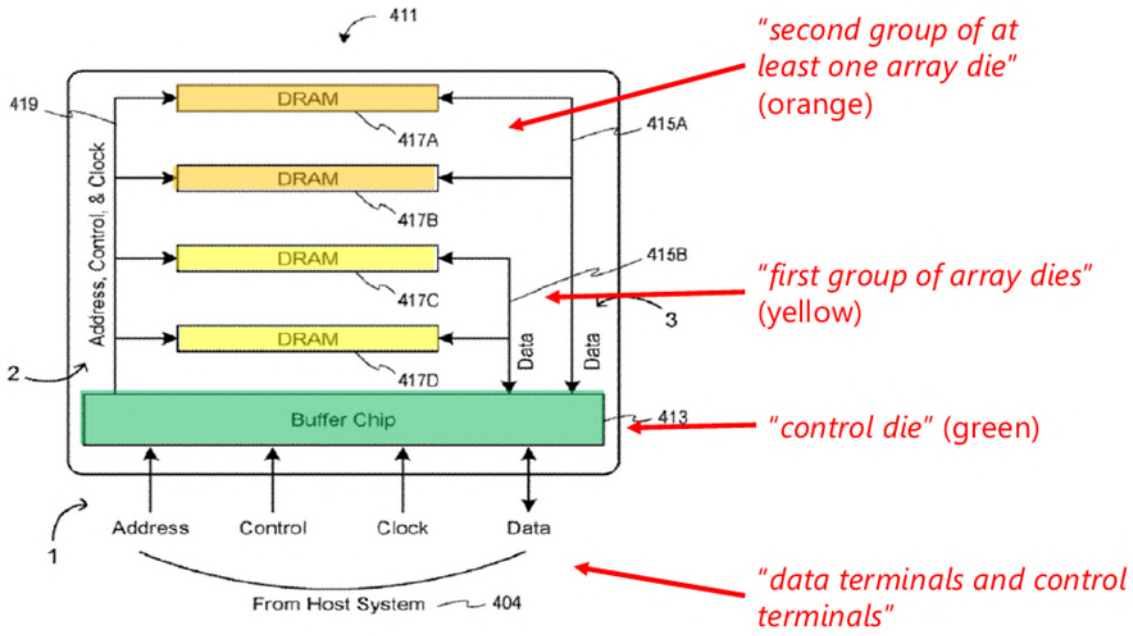


FIG. 4

152. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including the use of address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals

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for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below).

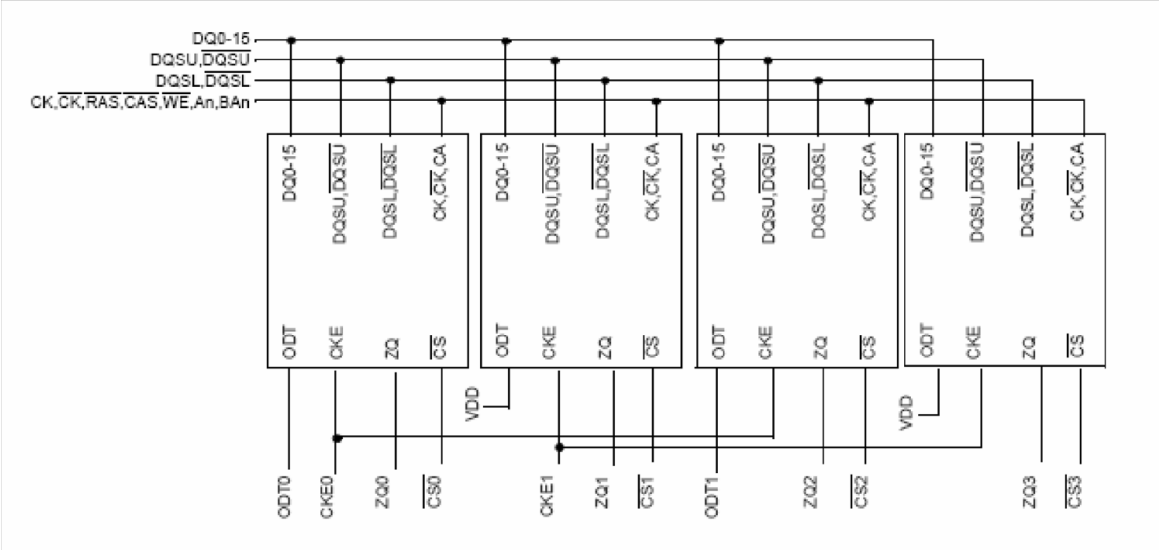


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

153. A Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control, and data terminals according to the JEDEC standards in Kim's memory package in order to use the package in JEDEC compliant systems. Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the admitted prior art referenced in the 160 Patent. *See, e.g.*, Ex. 1001 (the 160 Patent) at 22:22-24 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031

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(U.S. Pat. No. 7,532,537). As discussed above, the JEDEC standards were influential and well known. *See supra* ¶¶131-133; Ex. 1022, pp. 332-35, 318-20.

154. Furthermore, Kim explains that, "although only one main chip and two slave chips are shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used." Ex. 1014 (Kim) at [0048]; *see also id*. at [0050] ("It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked. While the semiconductor memory apparatuses having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks.").

155. A Skilled Artisan would have understood from this disclosure that Kim's invention can include more slave chips (and more ranks) and that some of those additional slave chips proposed by Kim can be in the same group as chips C1 or C2 and connected to TSV1 or TSV2, respectively. Furthermore, to the extent one might argue that Kim does not sufficiently disclose a group of multiple memory chips connected to the same TSV, it would have been obvious in light of Rajan, including Figure 4 of Rajan shown below.

156. As discussed above, both Rajan and Kim are analogous art to the 160 Patent, and a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about adding more chips (and ranks) in the stack as proposed by Kim. Ex. 1015 at Fig. 4 (reproduced below, annotated).

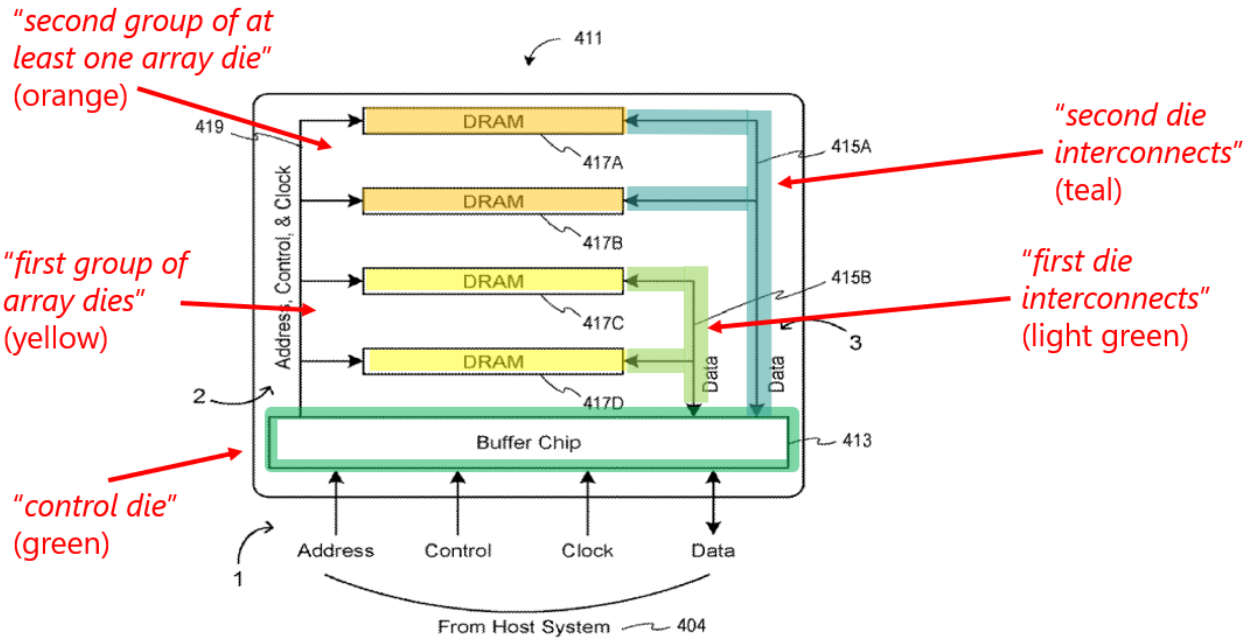


FIG. 4

157. For example, Rajan explains that "FIG. 4 illustrates another embodiment of a system 411 in which the buffer chip 413 is interfaced to a host system 404 and is coupled to the DRAM chips 417A-417D somewhat differently than in the system of FIG. 2 or 3. There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B. Each shared bus has two or more DRAM chips coupled to it."). *Id.* at 5:36-43.

158. A Skilled Artisan would have also understood that creating such a shared data bus (415A, 415B above) as taught by Rajan was well within the level of skill at the time using, e.g., TSV interconnects like Kim. *See, e.g.*, Ex. 1025 (Foster) at Fig. 5 (reproduced below, annotated, showing two dies 21 and 22 (yellow) in a first substack being coupled to signal lines 68 by TSV 30, and two other dies 23 and 24 (orange) in a second substack being coupled to signal lines 70 using TSV 30 and pass-through vias PTV 29 which have no connection to circuitry in dies 21 and 22 in the first substack).

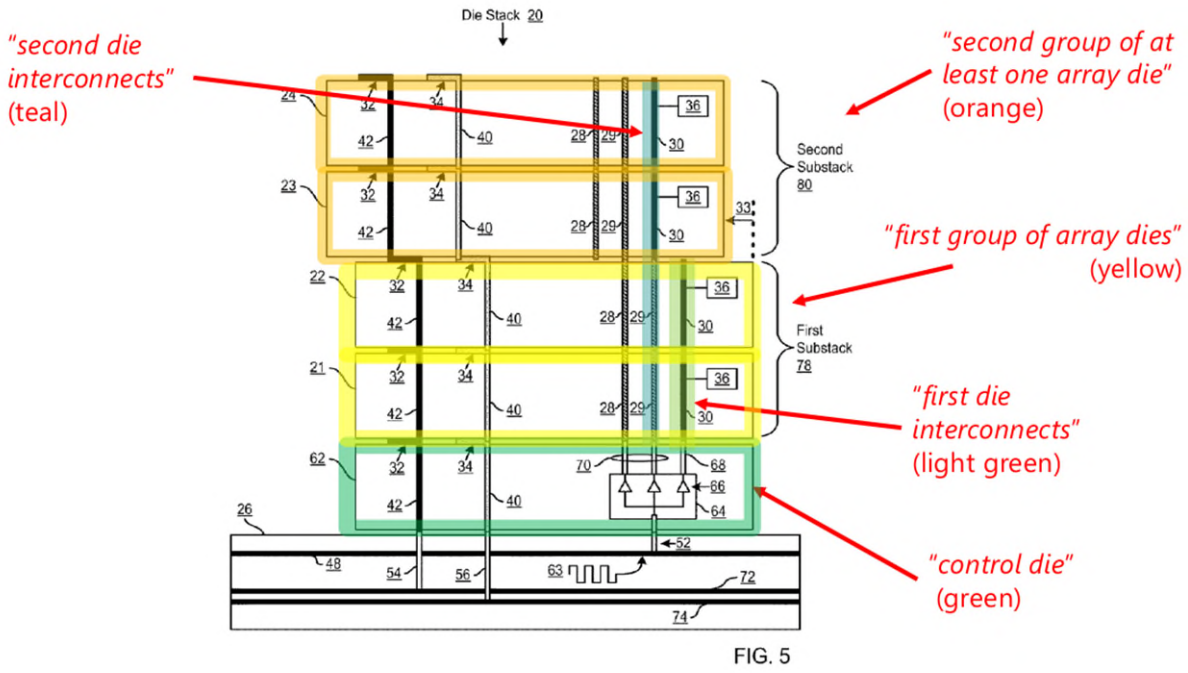


FIG. 5

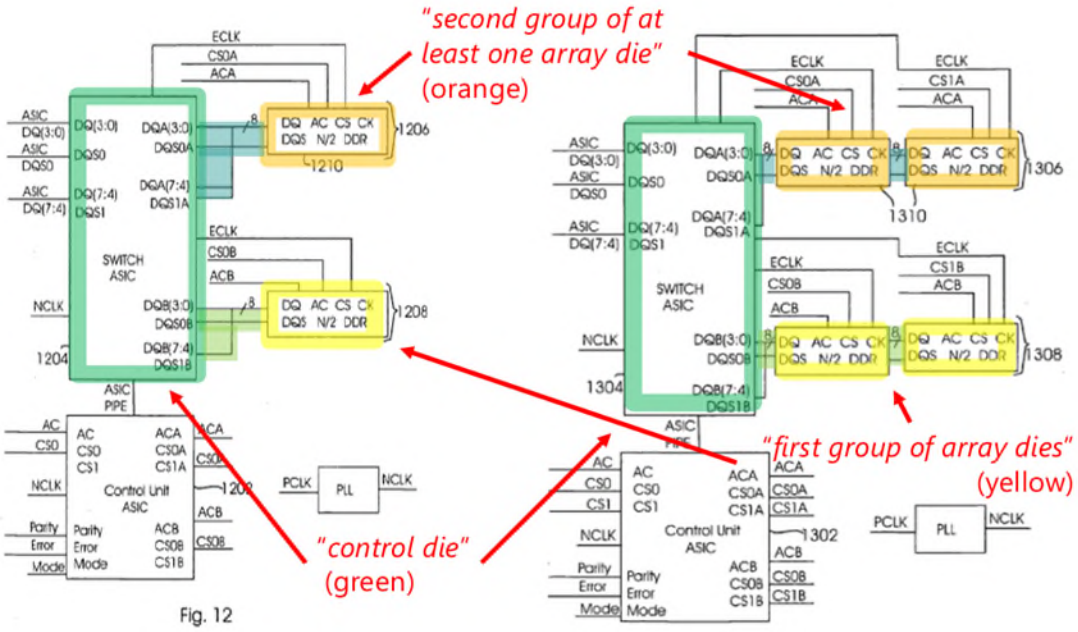
159. Therefore, a Skilled Artisan would have understood that there were a finite number of known ways to connect the additional dies, including sharing a through-silicon via by a subset of the dies, so it would have been obvious to a Skilled Artisan to follow this well know architecture when adding memory dies to

the stack as suggested by Kim. *See*, *e.g.*, Ex. 1015 (Rajan) at Figs. 2-6 (describing a finite number of different interconnections of stacked memory chips).

160. Furthermore, a Skilled Artisan would have been motivated to connect the additional dies to the existing interconnects TSV1 or TSV2 in Kim's device, because such an arrangement could use Kim's chips without changing the number of interconnects TSV1 and TSV2, thus without creating new TSVs, which would require space and additional circuitry. Such a use of the interconnects TSV1 and TSV2 would also allow emulating certain characteristics required by external devices. Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 3:52-61 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory. The interface circuit may emulate an interface to one version of a protocol such as DDR2 with 5-5-5 latency timing, while the physical memory chips are built to another version of the protocol such as DDR2 with 3-3-3 latency timing. The interface circuit may emulate an interface to a memory having a first capacity that is different than the actual combined capacity of the physical memory chips.").

161. Indeed, a Skilled Artisan would have understood that Rajan's emulation techniques, including rank multiplication techniques, used "fork-in-the-

road" arrangements where a two-rank arrangement has two data busses, and two more ranks can be added by sharing the existing two data busses of the two-rank arrangement. *See, e.g.*, Ex. 1026 (US 2006/0277355) at Figs. 12 and 13 (reproduced below, annotated, showing a switch ASIC connecting an 8-bit wide external DQ bus to two 8-bit wide internal busses DQA and DQB, and adding two more ranks in Figure 13 by sharing the DQA and DQB busses already used in the two-rank arrangement of Figure 12); Ex. 1027 at 77-82 (Final Written Decision analyzing Ellsberry).



162. A Skilled Artisan's understanding that rank multiplication techniques used "fork-in-the-road" arrangements is further evidenced by the admitted prior art referenced in the 160 Patent. *Supra* at ¶¶137-140; *see also* Ex. 1001 (the 160

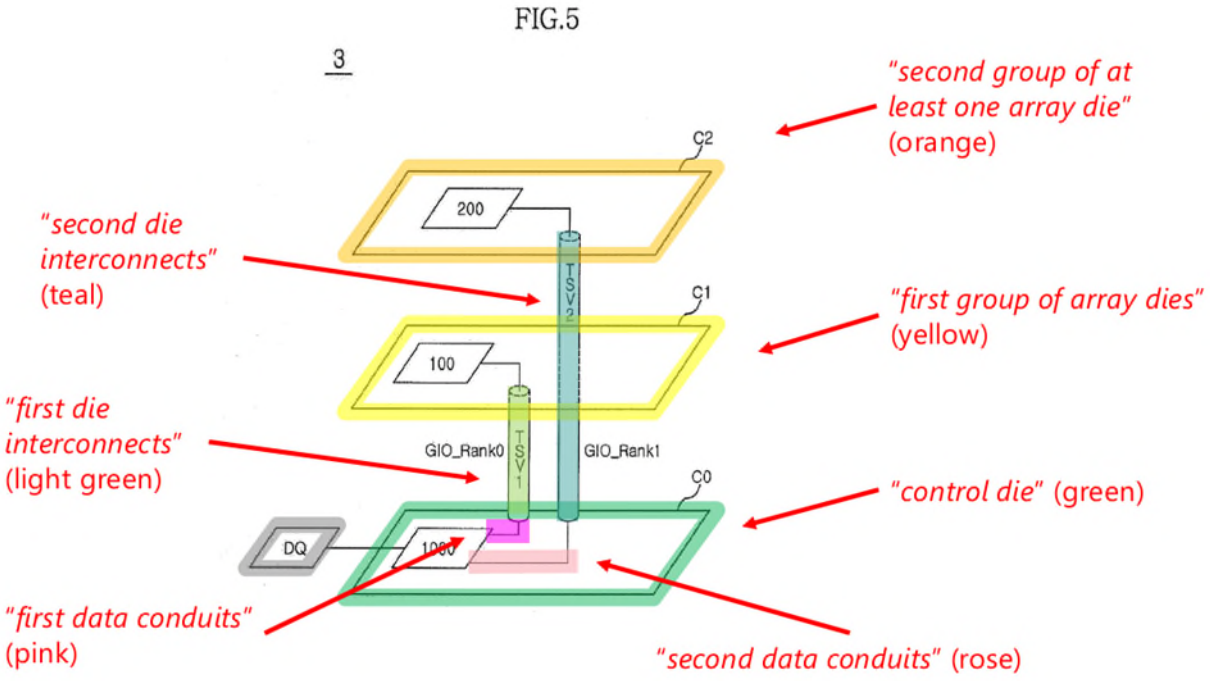
Patent) at 19:26-32, 22:19-42 (explaining that rank multiplication was well known prior art and incorporating by reference corresponding prior art patents disclosing fork-in-the-road arrangements, including Exhibits 1028 and 1031), 18:53-18:62 (describing prior-art memory package with a "programmable secondary 1-to-2 rank decoder" in the controller die of the memory package); *see also supra* at ¶¶137-140.

163. A Skilled Artisan would have been further motivated to use the interconnects TSV1 and TSV2 when adding more chips, because Kim explains that its structure of using two interconnects can avoid certain data collisions. Kim at Figs. 4A (explaining the problem of collision in the prior art), 4B (explaining the operation of the invention avoiding the collision), [0042-44] (same). Therefore, when adding more memory dies to Kim's stack, a Skilled Artisan would have been motivated to connect the additional dies to Kim's interconnects TSV1 and TSV2 as taught by Rajan to maintain Kim's data collision avoidance feature without creating additional TSVs.

164. For at least all these reasons, it would have been obvious to a Skilled Artisan to combine the teaching of Kim and Rajan to implement Kim's stacked memory package with the functionality of Rajan's interface circuit and inter-die connections.

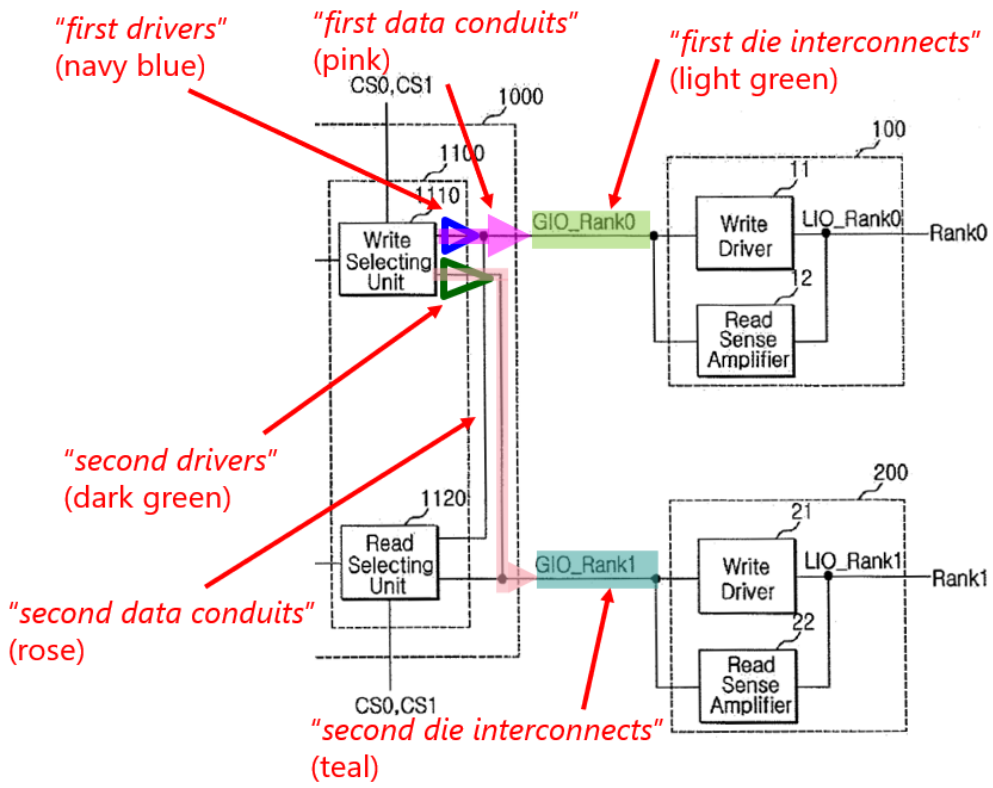
165. Wyman teaches to save power by using drivers that depend on the length (and load) of the connection in the stack. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.").

166. As expressly shown in annotated Fig. 5 of Kim (reproduced below), Kim discloses that TSV1 ("*first die interconnects*," light green) is shorter than TSV2 ("*second die interconnects*," teal). Ex. 1014 at Fig. 5 (reproduced below, annotated).



167. A Skilled Artisan would have understood that, due to the difference in length between TSV1 and TSV2, each of the "*first data conduits*" (pink) and the

"*second data conduits*" (rose) can include respective drivers that are optimized for driving the data signal through the corresponding TSV in an efficient way. For example, Wyman explains that "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 (Wyman) at 1:22-24. Therefore, a Skilled Artisan would have been motivated to follow the teaching of Wyman in the system of Kim and, instead of using a full capacity driver to drive both TSV1 and TSV2, implement respective drivers for each of TSV1 and TSV2 that are optimized for the length of the corresponding TSV as illustrated in annotated Fig. 3 of Kim. Ex. 1014 (Kim) at Fig. 3 (reproduced below in part, annotated, showing "*first drivers*," navy blue, corresponding to TSV1 and "*second drivers*," dark green, corresponding to TSV2). Implementing Kim's system in this manner avoids the "wasteful and inefficient" use of power as taught by Wyman.



168. Wyman is analogous art to the 160 Patent and Kim, as each is directed to the problem of efficient signaling between chips in a stacked arrangement. Ex. 1017 (Wyman) at 1:45-48 ("The reduced path distances of stacked hybridized chips therefore require less drive to adequately drive a signal to an off-chip board and/or chip. These conditions warrant the use of restructuring the drive portion of existing chip architecture."); Ex. 1001 (the 160 Patent) at 1:21-23 ("More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:26-29 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS)."); Ex. 1014 (Kim) at

[0003] ("Various embodiments of the present disclosure generally relate to a semiconductor memory apparatus, and more particularly, to data input/output of a semiconductor memory apparatus."), [0046] ("In order to increase the integration of a semiconductor apparatus, a three-dimensional (3D) semiconductor apparatus comprising a plurality of stacked chips has been developed. The stacked chips provide a structure that enables the 3D semiconductor apparatus to be packages in a single package. Recently, a through-silicon via (TSV) type semiconductor apparatus has been developed in which silicon vias are formed to pass through the plurality of stacked chips so that all of the chips are electrically connected to one another.").

169. A Skilled Artisan would have understood, and been motivated, to turn to analogous art, like Wyman teaching about efficiently driving signals between stacked devices, in order to implement the stacked devices of Kim. For example, Wyman discloses that longer interconnects in a stacked arrangement require additional drive. *See, e.g.*, Ex. 1017 (Wyman) at Fig. 8 (reproduced below).

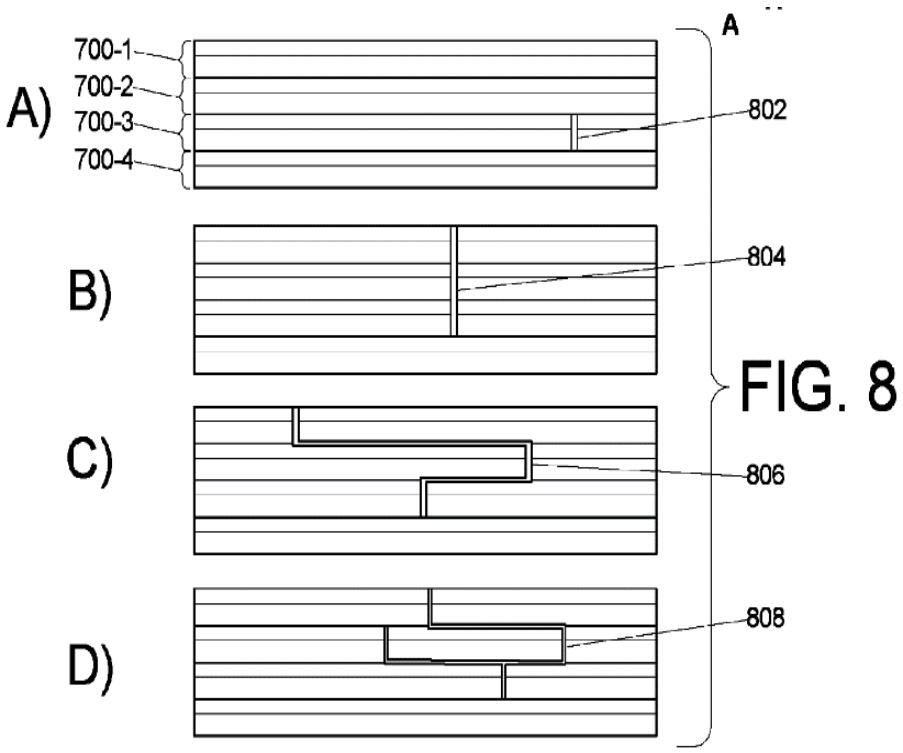


FIG. 8

Wyman explains that "FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3) … requir[ing] minimal drive … FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. …." *Id*. at 6:15-30. Thus, "the output drive current [can] be modified to meet the requirements of a particular output load." *Id.* at 7:13-18. However, Wyman recognizes that even with the "significantly longer connection (808) between the mother chip (700-4) with a fan

out to both daughter 2 (700-2) and daughter 3 (7001)," as shown in Fig. 8.D, using "the total drive … would be overkill." *Id.* at 6:44-50.

170. A Skilled Artisan would have understood from this disclosure that the longer the connection in a stack of chips, the more drive it requires, but using the "total drive" would be wasteful. Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use drivers of different strengths (i.e., "*first drivers*" having a "*first driver size*," and "*second drivers*" having a "*second driver size*") for Kim's different sized through-silicon vias TSV1 and TSV2. *See also supra* at ¶¶134-136 (explaining that different strengths are achieved by transistors of different sizes). In particular, a Skilled Artisan would have been motivated to drive the shorter TSV1 with a smaller driver and the longer TSV2 with a larger driver in order to use power in an efficient manner as taught by Wyman. Making such a combination was well within the level of skill, since Wyman itself teaches drivers of different sizes, and the combination would have provided nothing more than expected: a power efficient drive of signals through Kim's TSVs.

171. Therefore, it would have been obvious to a Skilled Artisan to implement Wyman's teaching of using drivers optimized for the length of the corresponding die interconnects in the memory package of Kim to save power.

B. Claims 1-20 Are Unpatentable Over Ground 1

172. As explained below, claims 1-20 are unpatentable over Ground 1 (Kim in view of Rajan and Wyman).

1. Claim 1 is Unpatentable

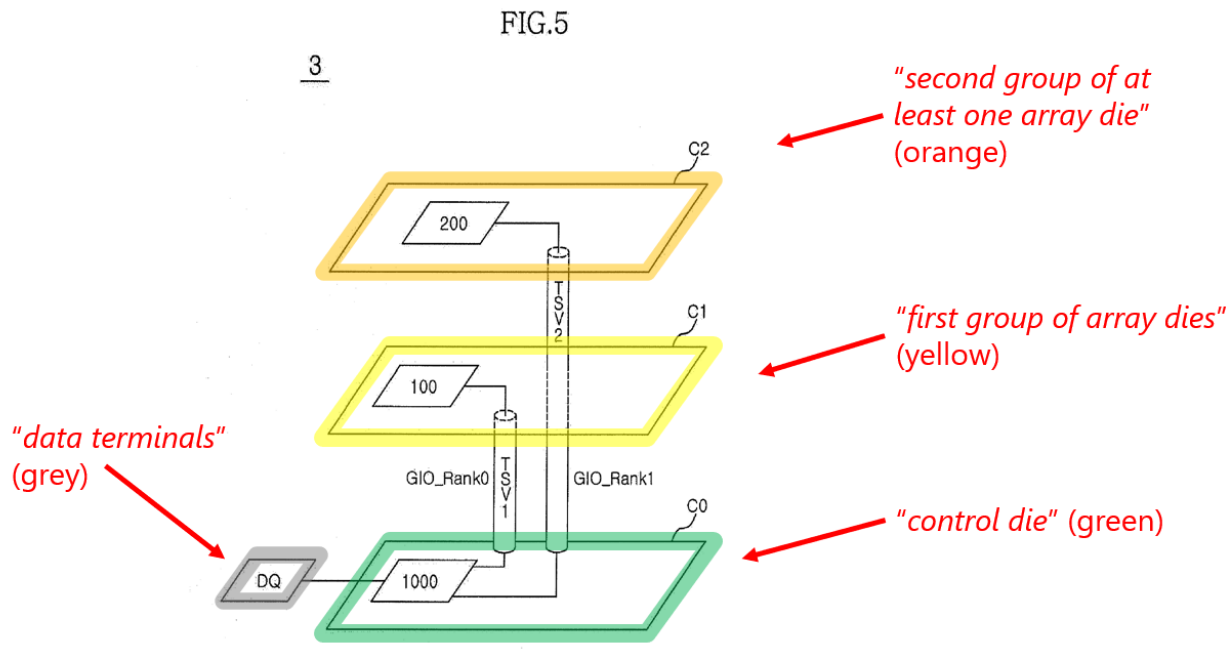
173. Claim 1 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [1.a] Preamble

174. The preamble of claim 1 requires "*[a] memory package, comprising*."

175. To the extent the preamble is limiting, the prior art references in Ground 1 teach this limitation to a Skilled Artisan.

176. Kim discloses a "*memory package*" including main chip C0 and stacked memory chips C1 and C2 as illustrated in Kim's Fig. 5. *See* Ex. 1014 at Fig. 5 (reproduced below, annotated).



177. For example, Kim explains that "a semiconductor memory apparatus 3 comprises a main chip C0 and a plurality of slave chips C1 and C2. The chips C0, C1 and C2 are connected by TSVs." Ex. 1014 at [0047]. Kim further explains that these "stacked chips provide a structure that enables the 3D semiconductor apparatus to be package[d] in a single package." *Id*. at [0046].

178. Therefore, Kim discloses a "*memory package.*"

179. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in Ground 1 satisfy "*[a] memory package, comprising*."

b) [1.b] Data Terminals and Control Terminals

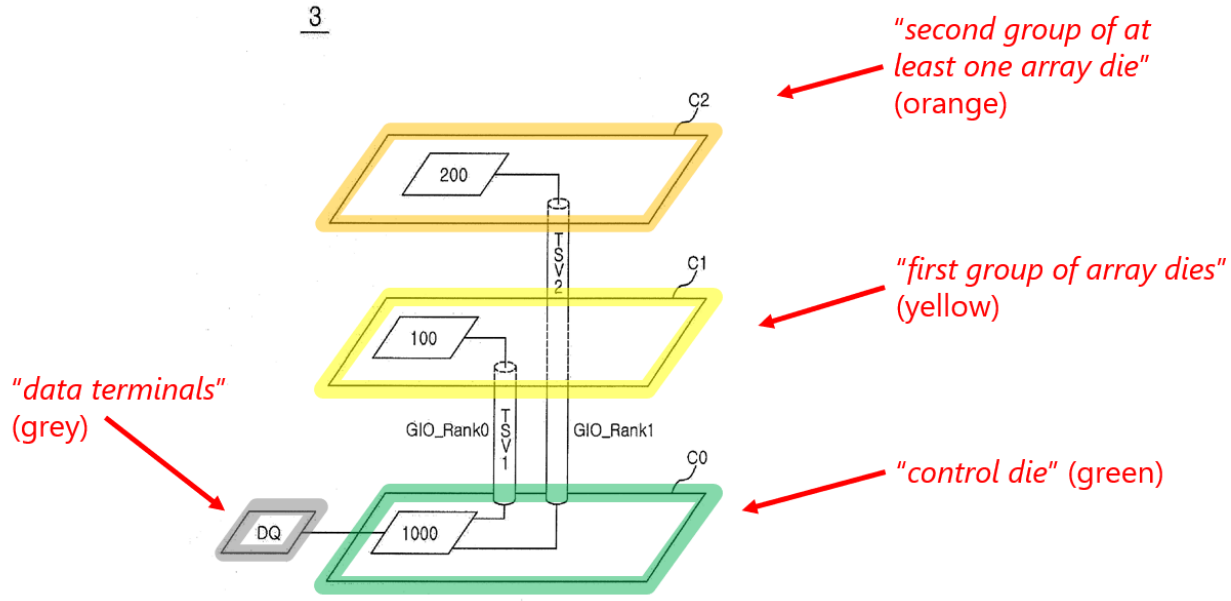
180. Claim 1 requires "*data terminals and control terminals.*"

181. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

182. Kim discloses to a Skilled Artisan that the stacked package of Fig. 5 includes "*data terminals and control terminals*."

183. For example, Kim discloses a data pad DQ which is an example of "*data terminals*." *See* Ex. 1014 at Fig. 5 (reproduced below, annotated, data pad DQ annotated grey).

FIG.5



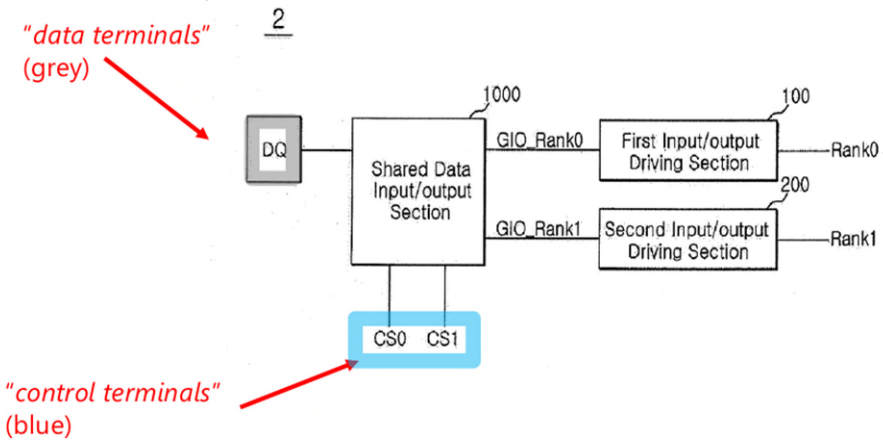
184. Kim explains that "[t]he data input/output section outputs the data transmitted from the rank selecting section through a data pad to an external device during a read operation, and outputs the data inputted to the data pad to the rank selecting section during a write operation." Ex. 1014 at Abstract; *see also id.* [0028] ("During a read operation, the shared data input/output section 1000 outputs data transmitted from the first input/output driving sections 100 and 200 through a data pad DQ…. During a write operation, the shared data input/output section 1000

transmits data inputted through the data pad DQ to one of the first and second input/output driving sections 100 and 200….").

185. A Skilled Artisan would have understood from this disclosure that Kim's data pad DQ is an example of "*data terminals*" through which data is communicated with external devices. A Skilled Artisan would have also understood that memory devices usually have multiple "*data terminals*." *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.3-12 (describing x4, x8, and x16 memory devices having 4, 8, and 16 DQ data terminals to communicate data with external devices). Therefore, Kim discloses and at least renders obvious the claimed "*data terminals*" to a Skilled Artisan.

186. Kim also discloses to a Skilled Artisan "*control terminals*" such as terminals for receiving chip selection command signals CS0 and CS1 from an external device. Ex. 1014 at Fig. 2 (reproduced below, annotated).

FIG.2



187. For example, Kim explains that "chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2." *Id.* at [0032]. A Skilled Artisan would have understood that "chip selection signals CS0 and CS1" are control signals because they are part of the command signals that control the memory device. *See* Ex. 1014 (Kim) at [0006] ("The semiconductor memory apparatus 1 controls the operations of the first and second chips using a chip selection command signal."); *see also* Ex. 1019 (JESD79-3C) at p.13 (disclosing that chip select signals are "considered part of the command code").

188. Indeed, a Skilled Artisan would have understood that chip selection signals from an external device are received at respective terminals of a memory package. For example, a Skilled Artisan would have been familiar with JEDEC standards for memory devices, including standards for stacked memory devices, and understood that standard memory devices include terminals for data and control signals, including terminals for chip select signals. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including data terminals (DQ) and chip select signal terminals CS0#-CSn#, where 'n' is the number of chips in the stack); Ex. 1023 at p.9, Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, the admitted prior art referenced in Figs. 1A and 1B of the 160 Patent also describes memory packages having terminals for chip selection signals.

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Ex. 1001 at 1:32-58 ("FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used … with the chip select ports 144 … configured to receive corresponding chip select signals to enable or select the array dies for data transfer."). Therefore, Kim discloses and renders obvious to a Skilled Artisan the claimed "*control terminals,*" for example, to receive chip select signals.

189. Kim also renders obvious to a Skilled Artisan "*control terminals*" to receive other command (and address) signals.

190. For example, Kim discloses "write and read command signals applied from a device external to the semiconductor memory apparatus 2." Ex. 1014 at [0038]. It would have been obvious to a Skilled Artisan from this disclosure, at least in view of Rajan, that "write and read command signals" can include control signals, including command and address signals, received via respective "*control terminals*" from an external controller. *Supra*, ¶¶146-164. For example, as discussed above, a Skilled Artisan would have understood that memory devices can comply with JEDEC standards at the time and such standards specify the address and command signals, such as RAS, CAS, and WE, and corresponding terminals, for read and write operations. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including terminals for RAS#, CAS#, and WE# and address signal terminals A0-A15), p.18 (describing read and write

operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read and Write commands with corresponding column address, CA); Ex. 1023 at p.9, Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, the 160 Patent also describes the prior art memory devices referenced in Figs. 1A and 1B as operating in response to command and address signals. Ex. 1001 at 1:32-58 ("FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used … [where] the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110.").

191. Therefore, Kim discloses and renders obvious this limitation to a Skilled Artisan.

192. To the extent one might argue that Kim does not sufficiently disclose the claimed "*data terminals and control terminals*," it would have been obvious to a Skilled Artisan in view of Rajan.

193. As previously discussed, a Skilled Artisan would have been motivated to look at analogous art to Kim, like Rajan, for details about control and address signals. *Supra* ¶¶146-171. Rajan discloses the same basic structure of a memory package like Kim and the 160 Patent: the package includes stacked memory chips

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Ex. 1091, p. 86

and a shared interface circuit, called "buffer chip" in Rajan. Ex. 1015 at 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses."), Fig. 4 (reproduced below, annotated).

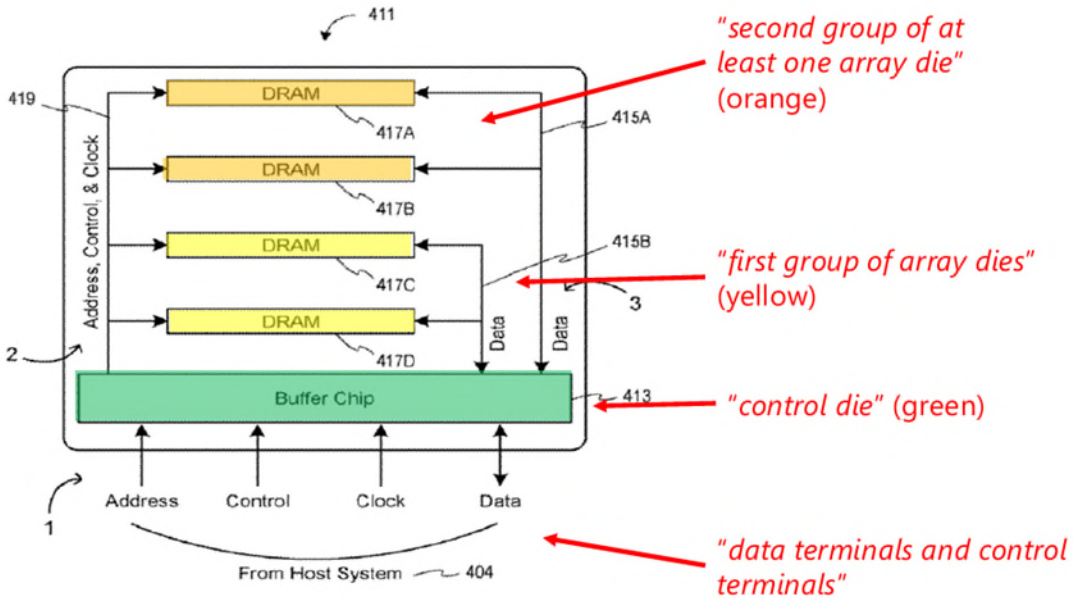


FIG. 4

In particular, the "interface circuit includes a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system, and a system data signal interface for sending/receiving data signals to/from the host system." *Id.* at 14:11-18 and Fig. 18 (reproduced below).

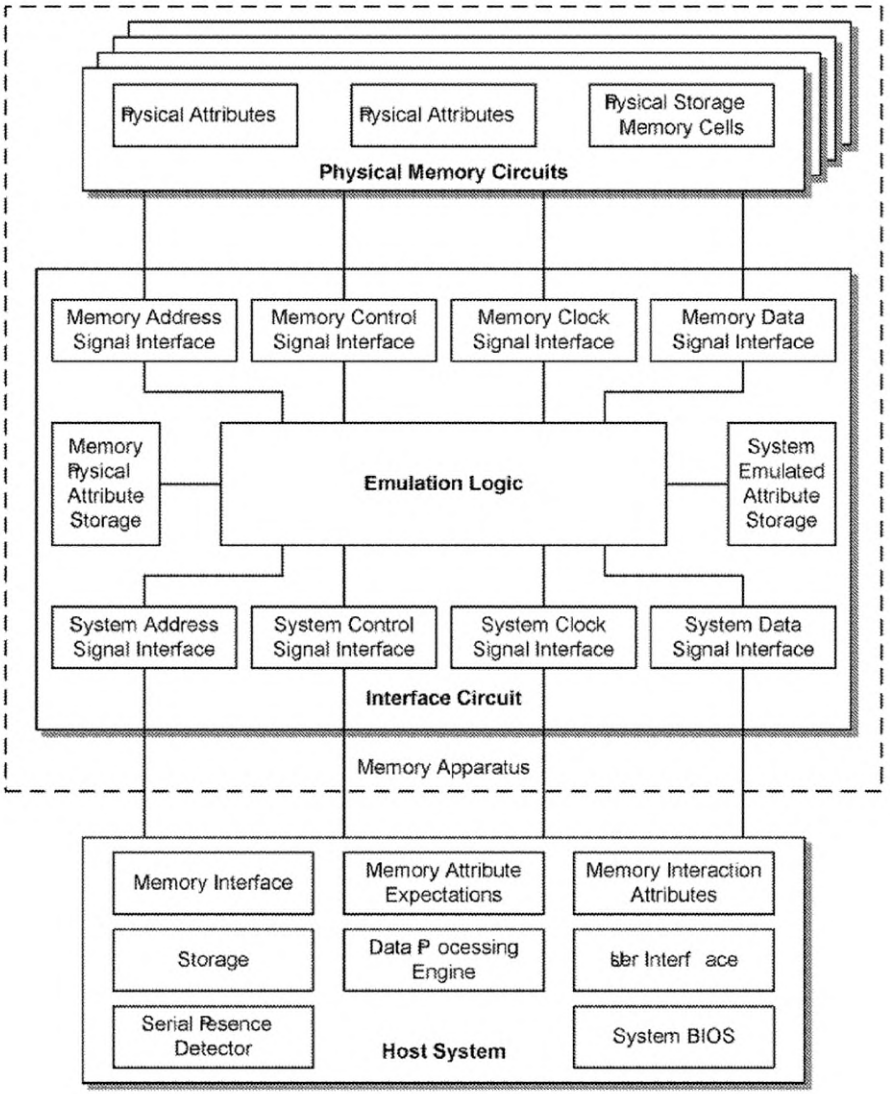


FIG. 18

194. In Rajan, "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 at 5:36-43, Figs. 4 and 18 (reproduced above). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards . .

..."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including terminals for address, control, and data signals); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, a Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control, and data terminals in Kim's memory package according to the JEDEC standards to enable the memory packages' use in JEDEC compliant systems.

195. Therefore, Kim and Rajan render obvious this limitation to a Skilled Artisan.

196. Accordingly, the prior art references in Ground 1 satisfy "*data terminals and control terminals.*"

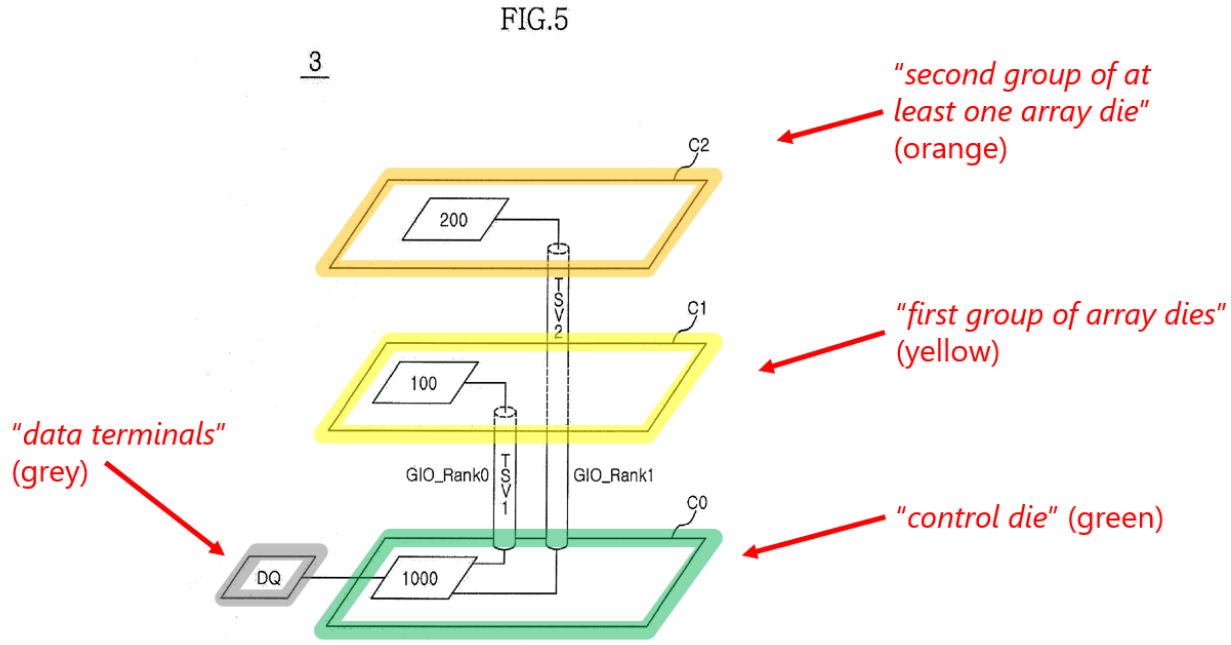
c) [1.c] Stacked Array Dies

197. Claim 1 requires "*stacked array dies including a first group of array dies and a second group of at least one array die.*"

198. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

199. Kim discloses to a Skilled Artisan "*stacked array dies including a first group of array dies* [including slave chip C1 (yellow)] *and a second group of*

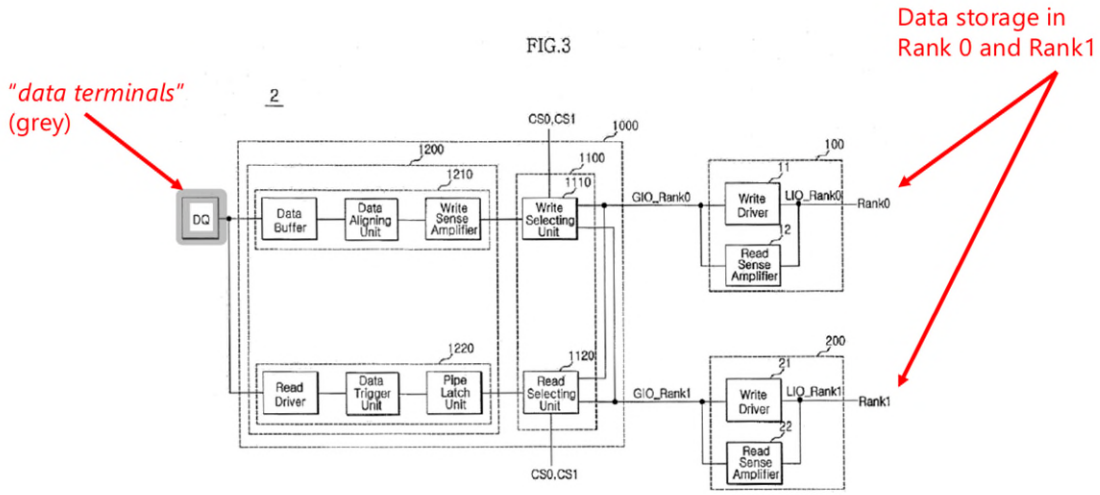
at least one array die [including slave chip C2 (orange)]." *See* Ex. 1014 at Fig. 5 (reproduced below, annotated).



200. For example, Kim explains that "FIG. 5 shows an exemplary embodiment in which one main chip C0 and two slave chips C1 and C2 are stacked. Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used." Ex. 1014 at [0048]. A Skilled Artisan would have understood that each referenced chip is a "*die*." *See, e.g.*, Ex. 1016 (Riho) at Abstract (describing stacked chips); Ex. 1018 (Riho2) (describing stacked "chip dies"). Therefore, Kim discloses "*stacked ... dies.*"

201. Kim further explains that the "first input/output driving section 100 stores data transmitted through the first data input/output line GIO_Rank0 in a

memory bank of a first rank Rank0 during a write operation, amplifies data stored in the memory bank of the first rank Rank0 and outputs the amplified data to the first data input/output line GIO_Rank0 during a read operation." *Id*. at [0026]. Likewise, Kim explains that the "second input/output driving section 200 stores data transmitted through the second data input/output line GIO_Rank1 in a memory bank of a second rank Rank1 during a write operation and amplifies data stored in the memory bank of the second rank Rank1 and outputs the amplified data to the second data input/output line GIO_Rank1 during a read operation." *Id.*; *see also id.* at Fig. 5 (reproduced above, annotated, showing the input/output driving sections 100 and 200 in the respective stacked slave chips C1 and C2), Fig. 3 (reproduced below, annotated, showing that each of the input/output driving sections 100 and 200 includes a Write Driver 11 and 21 and a Read Sense Amplifier 12 and 22, respectively).



202. A Skilled Artisan would have understood that Kim's "memory bank" where the data is stored includes a memory array. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.13 (explaining that the row address for Active commands and the column address for Read/Write commands "select one location out of the memory array in the respective bank"); *see also* Ex. 1023 (Jacob) at pp.1-2 & Fig. 2 (reproduced bellow, disclosing that the basic organization of DRAMs includes a memory array); Ex. 1022 (Jacob et al.) at 316-320 (same).

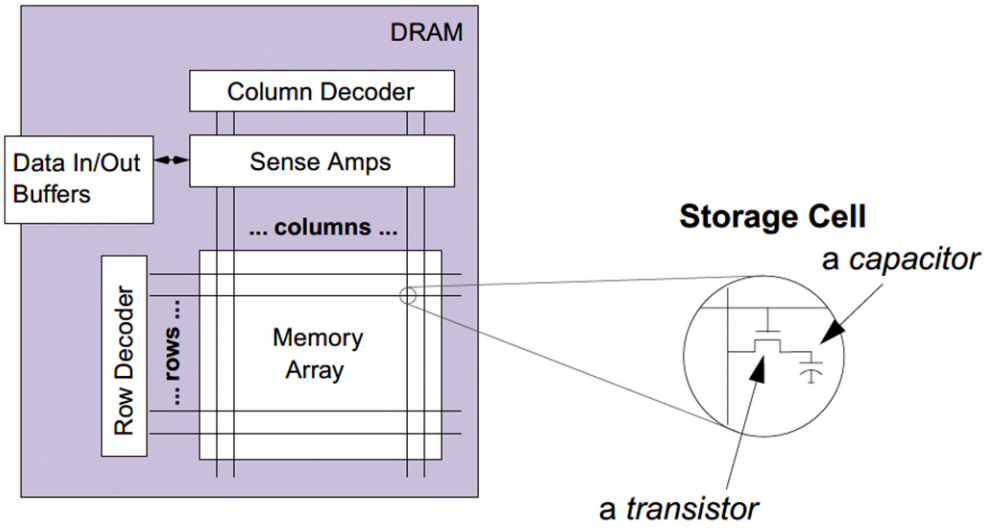


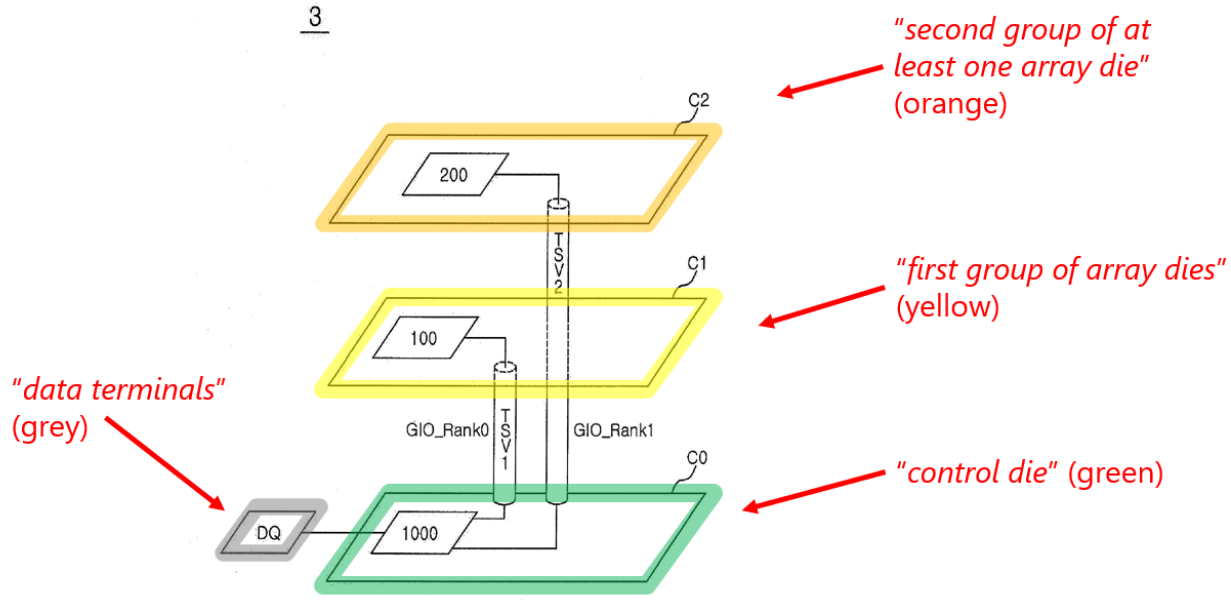
Figure 2: Basic Organization of DRAM Internals
The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

Therefore, Kim also discloses and renders obvious to a Skilled Artisan that the slave chips C1 and C2 are "*array dies*" as required by the claim.

203. Kim also discloses that slave chip C1 is in a "*first group of array dies*" coupled to through-silicon via TSV1, and slave chip C2 is in a "*second group*

of at least one array die" coupled to through-silicon via TSV2. Ex. 1014 at Fig. 5 (reproduced below, annotated).

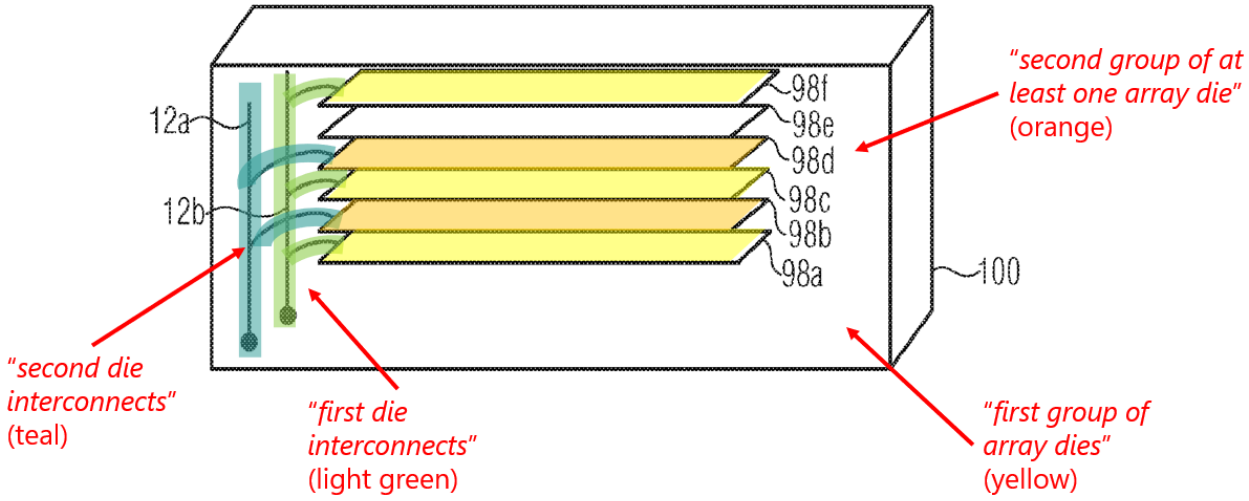
FIG.5



204. To the extent one might argue that the "*first group of array dies*" requires multiple slave chips being coupled to the through-silicon via TSV1, Kim discloses and renders obvious such an arrangement to a Skilled Artisan. For example, Kim explains that "although only one main chip and two slave chips are shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used." Ex. 1014 at [0048]. Furthermore, Kim explains that "the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked. While the semiconductor memory apparatuses having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill

in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks." *Id.* at [0050].

205. A Skilled Artisan would have understood from this disclosure that Kim's invention is not limited to the exemplary two slave chips C1 and C2 and two ranks and that the stack can include more slave chips and/or more ranks. A Skilled Artisan would have also understood that some of the additional slave chips proposed by Kim can be in the same group as chips C1 or C2 and connected to TSV1 or TSV2, respectively. Indeed, such an arrangement of multiple groups of the stacked dies, where each die in a group is connected to the same data interconnect, was commonly known and used to implement multiple ranks in memory stacks at the time. *See, e.g.*, Ex. 1024 (Ruckerbauer (US7,796,446)) at Fig. 5 (reproduced below, annotated), 9:14-18 ("[W]ithin the memory stack 100, a first sub set of memory dies is coupled to the first transfer data path 12a and a second sub set is coupled to the second transfer data path 12b. These different sub sets could, for example, be associated to different ranks within the stack 100.").



206. To the extent one might argue that Kim alone does not render obvious the additional chips in each group sharing the data connections TSV1 and TSV2, it would have been obvious in view of Rajan. As discussed above, a Skilled Artisan would have been motivated to look to Rajan for details about adding more chips to the stack as proposed by Kim. *Supra* ¶¶146-164. For example, Rajan explains that "FIG. 4 illustrates another embodiment of a system 411 in which the buffer chip 413 is interfaced to a host system 404 and is coupled to the DRAM chips 417A-417D somewhat differently than in the system of FIG. 2 or 3. There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B. Each shared bus has two or more DRAM chips coupled to it."). Ex. 1015 at 5:36-43, Fig. 4 (reproduced below, annotated).

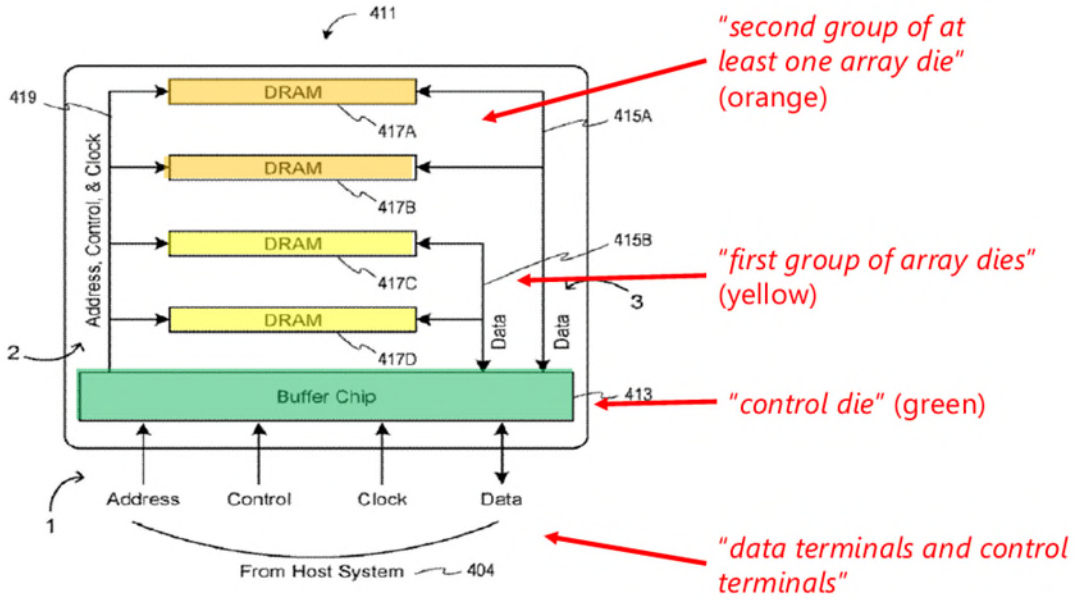


FIG. 4

207. A Skilled Artisan would have also understood that creating such a shared data bus as taught by Rajan was well within the level of skill at the time using, e.g., TSV interconnects like Kim. *See, e.g.*, Ex. 1025 (Foster) at Fig. 5 (reproduced below, annotated, showing two dies 21 and 22 in a first substack coupled to signal lines 68 by TSV 30, and two other dies 23 and 24 in a second substack coupled to signal lines 70 using TSV 30 and pass-through vias PTV 29 which have no connection to circuitry in dies 21 and 22 in the first substack).

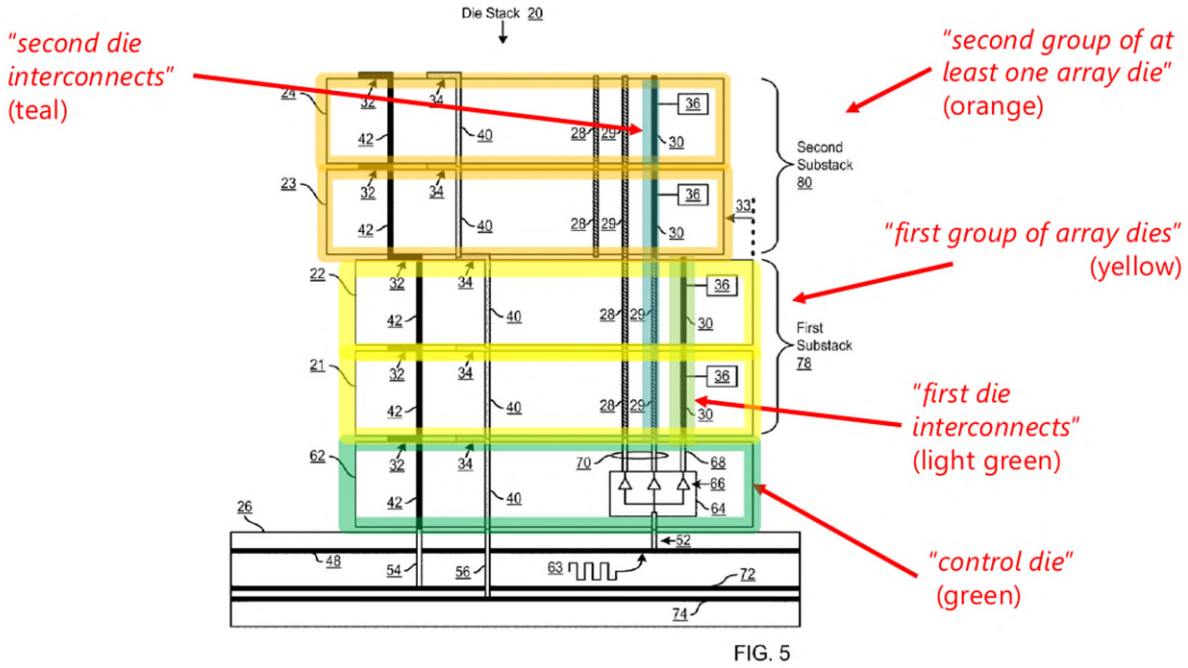


FIG. 5

208. Therefore, a Skilled Artisan would have understood that there were a finite number of known ways to connect the additional dies, including sharing a through-silicon via by a subset of the dies, so it would have been at least obvious to a Skilled Artisan to follow this well-known architecture when adding memory dies to the stack as suggested by Kim. *See*, *e.g.*, Ex. 1015 (Rajan) at Figs. 2-6.

209. Furthermore, a Skilled Artisan would have been motivated to connect the additional dies to the existing interconnects TSV1 or TSV2 in Kim's device, because such an arrangement could use Kim's chips without changing the interconnects TSV1 and TSV2 and without creating new TSVs which would require space and additional circuitry. Such a use of the interconnects TSV1 and TSV2 would also allow for the emulation of certain characteristics required by external devices. *Supra* at ¶¶137-140; *see, e.g.*, Ex. 1015 (Rajan) at 3:27-30 ("For

example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 3:52-61 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory. The interface circuit may emulate an interface to one version of a protocol such as DDR2 with 5-5-5 latency timing, while the physical memory chips are built to another version of the protocol such as DDR2 with 3-3-3 latency timing. The interface circuit may emulate an interface to a memory having a first capacity that is different than the actual combined capacity of the physical memory chips.").

210. Indeed, a Skilled Artisan would have understood that such rank multiplication techniques used "fork-in-the-road" arrangements where a two-rank arrangement has two data busses, and two more ranks can be added by sharing the existing data busses of the two-rank arrangement. *See, e.g.*, Ex. 1026 (Ellsberry) at Figs. 12, 13 (reproduced below, annotated, showing a switch ASIC connecting an 8-bit wide external DQ bus to two 8-bit wide internal busses DQA and DQB, and adding two more ranks in Figure 13 by sharing the DQA and DQB busses already used in the two-rank arrangement of Figure 12); Ex. 1027 at 77-82 (Final Written Decision analyzing Ellsberry).

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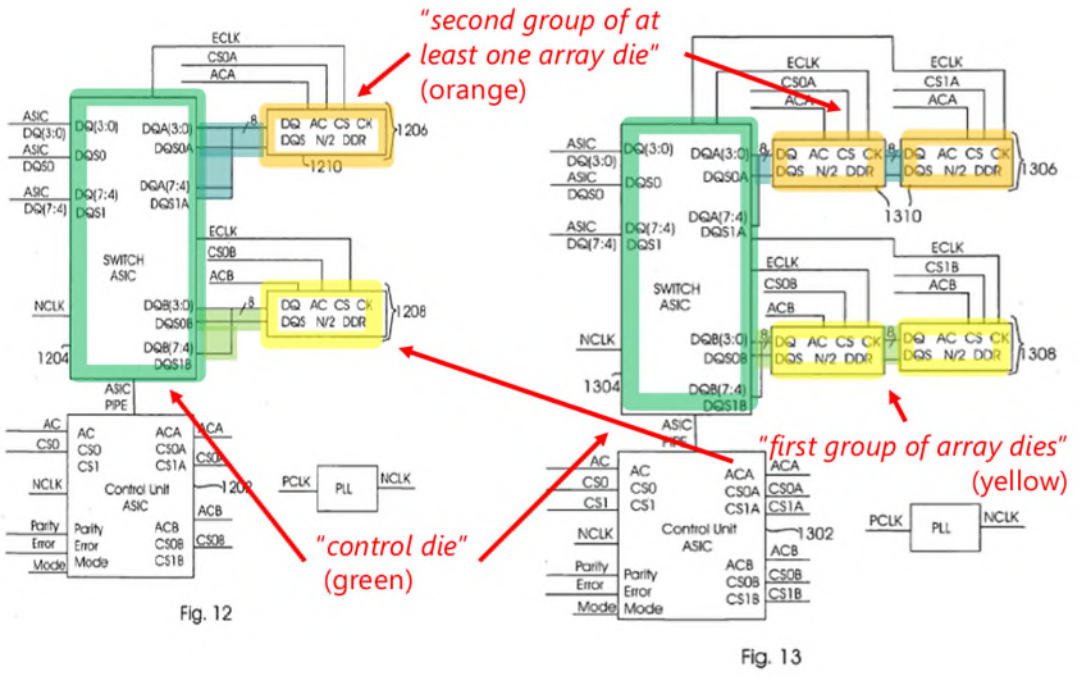


Fig. 12

Fig. 13

211. A Skilled Artisan's understanding that rank multiplication techniques used "fork-in-the-road" arrangements is further evidenced by the admitted prior art referenced in the 160 Patent. *Supra* at ¶¶137-140; *see also* Ex. 1001 (the 160 Patent) at 19:26-32, 22:19-42 (explaining that rank multiplication was well known prior art and incorporating by reference corresponding prior art patents disclosing fork-in-the-road arrangements, including Exhibits 1028 and 1031), 18:53-18:62 (describing prior art memory package with a "programmable secondary 1-to-2 rank decoder" in the controller die of the memory package); *see also* Ex. 1028 (US 7,289,386) at Fig. 6D (showing fork-in-the-road arrangement); Ex. 1031 (7,532,537) at Fig. 1 (same); *see also supra* at ¶¶137-140.

212. A Skilled Artisan would have been further motivated to use the interconnects TSV1 and TSV2 when adding more chips, because Kim explains that

its structure of using two interconnects can avoid certain data collisions. Ex. 1014 at Figs. 4A (explaining the problem of collision in the prior art), 4B (explaining the operation of the invention avoiding the collision), [0042-44] (same). Therefore, when adding additional chips, a Skilled Artisan would have been motivated to connect the additional dies to Kim's interconnects TSV1 and TSV2 as taught by Rajan to maintain Kim's data collision avoidance feature without creating additional TSVs.

213. Therefore, Kim discloses and renders obvious in view of Rajan this limitation to a Skilled Artisan.

214. Accordingly, the prior art references in Ground 1 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*."

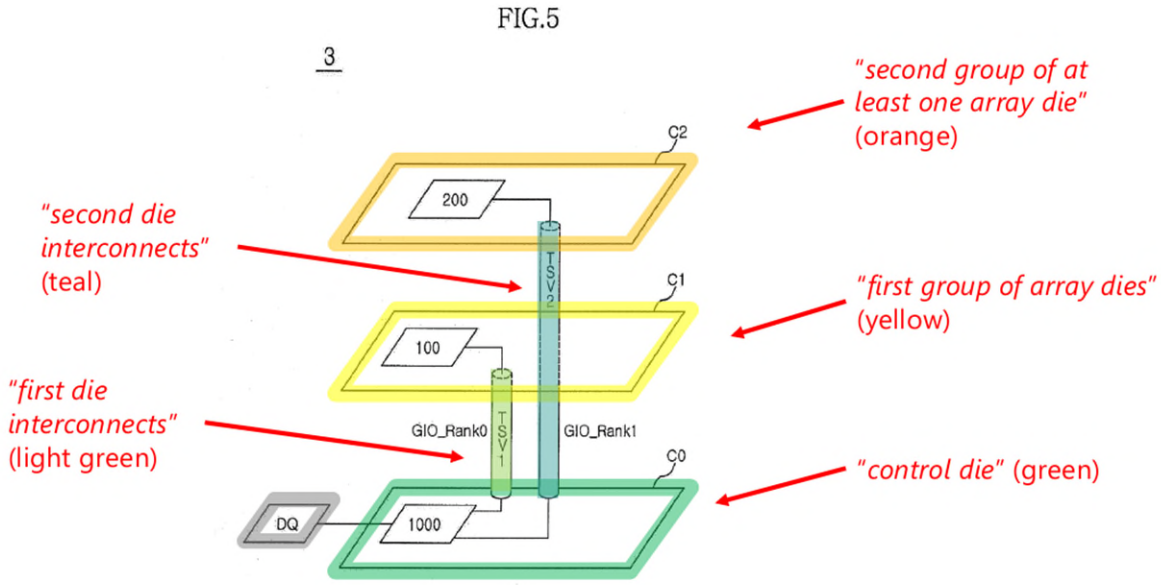
d) [1.d.1] and [1.d.2] Die Interconnects in Electrical Communication with Array Dies

215. Claim 1 requires "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

216. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

217. Kim discloses to a Skilled Artisan "*first die interconnects* [such as through-silicon via TSV1] *and second die interconnects* [such as through-silicon via TSV2]*, the first die interconnects* [like TSV1] *in electrical communication with the first group of array dies* [including slave chip C1] *and not in electrical communication with the second group of at least one array die* [including slave chip C2]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated), [0049] ("Data transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0 comprises a TSV TSV1 which connects the first slave chip C1 and the main chip C0."). As shown below, TSV1 does not extend up to C2 and thus is not "*in electrical communication*" with C2.

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218. For example, Kim explains that "[t]he rank selecting section is selectively connected to one of the first and second ranks in response to a chip selection signal, and outputs data to a connected rank or receives data from the connected rank." Ex. 1014 at Abstract. Kim further explains that "[t]he rank selecting unit 1100 distinguishes the read operation and the write operation for the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, and is selectively connected to the first and second data input/output lines GIO_Rank0 and GIO_Rank1. Thus, the read and write data may be transmitted through the first data input/output line GIO_Rank0 during the read and write operations of the first rank Rank0, and the read and write data may be transmitted through the second data input/output line GIO_Rank1 during the read and write operations of the second rank Rank1." *Id.* at [0045]. Kim elaborates that,

due to the selective coupling, "even when the read and write operations of the first and second ranks Rank0 and Rank1 are repeatedly performed, a data collision does not occur as can be alternately seen from FIG. 4B." *Id.*

219. A Skilled Artisan would have understood from this disclosure that the data collisions do not occur because, as depicted in Fig. 5 of Kim, the data input/output lines GIO_Rank0 through TSV1 are in electrical communication with chip C1 implementing Rank0, but are not in electrical communication with chip C2 implementing Rank1, and the data input/output lines GIO_Rank1 through TSV2 are in electrical communication with chip C2 implementing Rank1, but are not in electrical communication with chip C1 implementing Rank0.

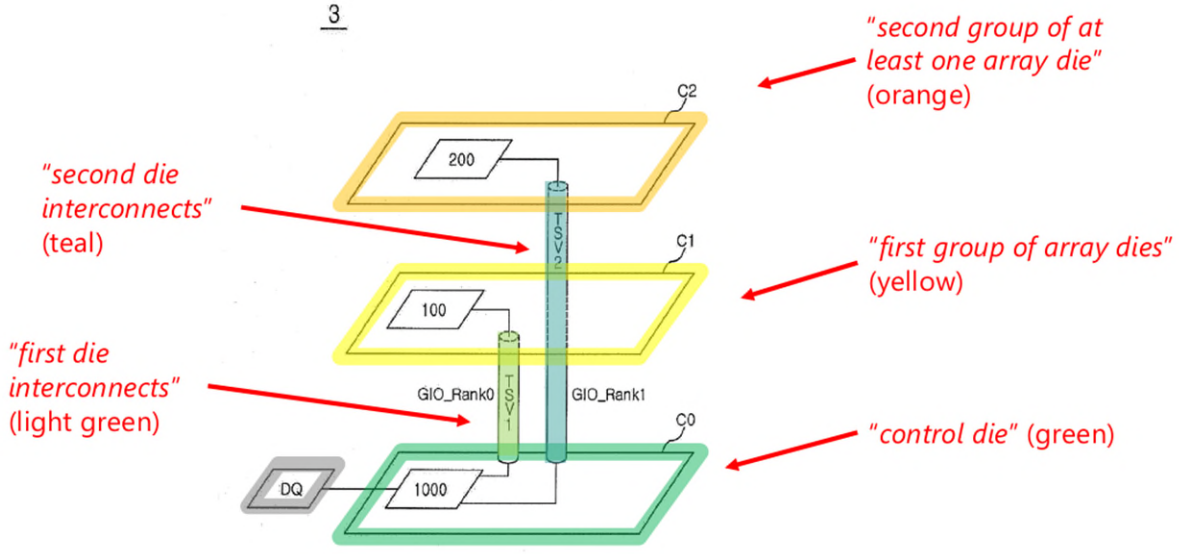
220. Furthermore, as discussed above with reference to claim element [1.b], a Skilled Artisan would have understood that each rank can write, store, and read multiple data signals, and each such data signal can be communicated on a respective TSV, resulting in multiple "*die interconnects*" to a given "*array die*." *Supra* ¶¶180-196; *see, e.g.*, Ex. 1019 (JESD79-3C) at pp.2-12 (describing x4, x8, and x16 memory devices); Ex. 1016, ¶[0030] (describing 256 TSVs per DRAM chip for data signals (DQ)).

221. Therefore, Kim discloses and renders obvious this limitation to a Skilled Artisan.

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222. Kim further discloses to a Skilled Artisan that "*the second die interconnects* [such as through-silicon via TSV2 are] *in electrical communication with the second group of at least one array die* [including chip C2] *and not in electrical communication with the first group of array dies* [including chip C1]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated), [0049] ("Data transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1 comprises a TSV TSV2 which connects the second slave chip C2 and the main chip C0.").

FIG.5



223. As shown above , TSV2 passes through C1 without being "*in electrical communication*" with C1 (e.g., TSV2 is not connected to input/output driving section 100 or anything else in C1). Furthermore, for the reasons discussed

immediately above with reference to the "*first die interconnects*" (like TSV1), a Skilled Artisan would have understood from Kim's disclosure that "*the second die interconnects*" (like TSV2) are in electrical communication with memory chip C2 (to communicate multiple data signals), but not with chip C1. *Supra* ¶¶217-221 (explaining that collisions are avoided due to selective connections); *see, e.g.*, Ex. 1014 at [0045] ("The rank selecting unit 1100 distinguishes the read operation and the write operation for the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, and is selectively connected to the first and second data input/output lines GIO_Rank0 and GIO_Rank1. Thus, the read and write data may be transmitted through the first data input/output line GIO_Rank0 during the read and write operations of the first rank Rank0, and the read and write data may be transmitted through the second data input/output line GIO_Rank1 during the read and write operations of the second rank Rank1. Therefore, even when the read and write operations of the first and second ranks Rank0 and Rank1 are repeatedly performed, a data collision does not occur as can be alternately seen from FIG. 4B.").

224. Therefore, Kim discloses this limitation to a Skilled Artisan.

225. Accordingly, the prior art references in Ground 1 satisfy "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical*

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communication with the second group of at least one array die," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

e) [1.e] Control Die

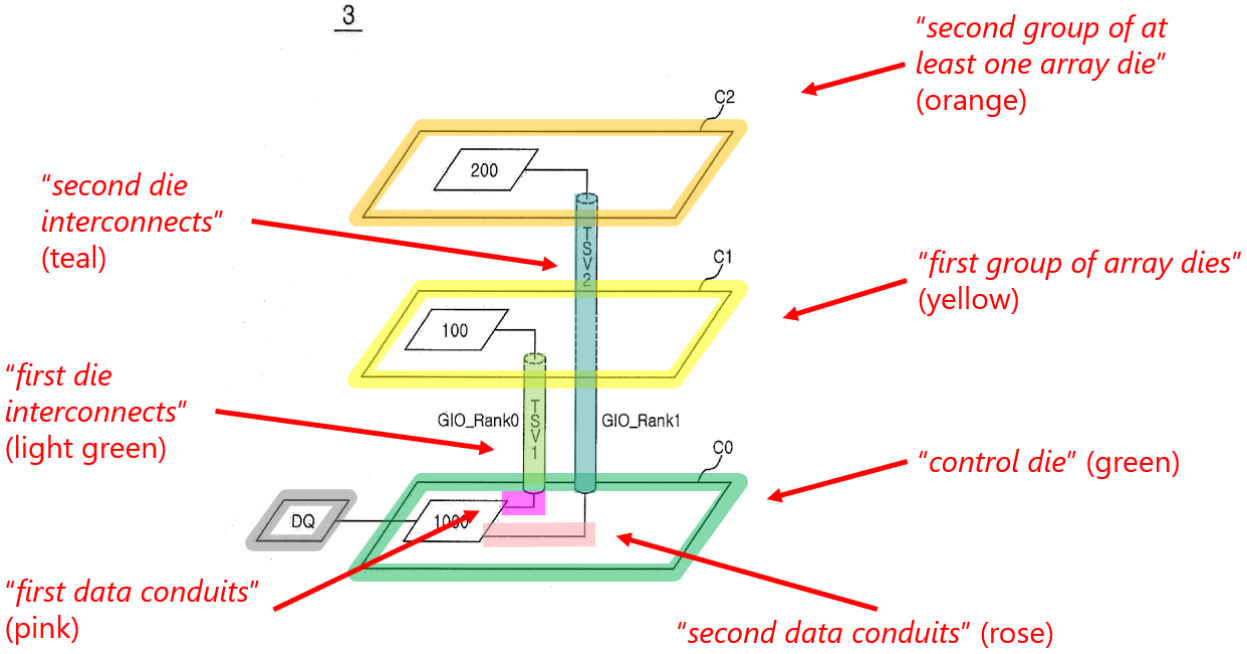
(1) [1.e.1] A Control Die Comprising

226. Claim 1 requires "*a control die comprising.*"

227. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

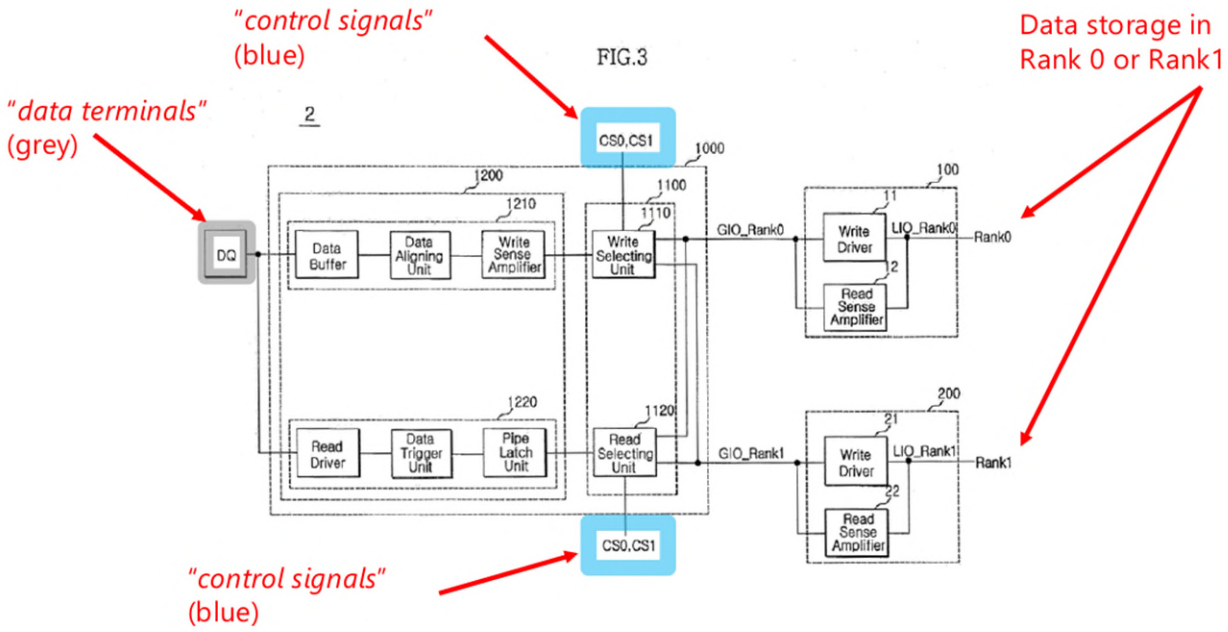
228. Kim discloses "*a control die*" such as main chip C0. *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).

FIG.5



229. For example, Kim discloses that, within the data input/output section 1000 on the main chip C0, "the write selecting unit 1110 and the read selecting

unit 1120 may be activated in response to internal write and read signals." Ex. 1014 at [0038], Fig. 3 (reproduced below, annotated).



230. Kim explains that the "internal write and read signals may be signals generated because write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered." *Id.* at [0038]. Kim further explains that "[t]he rank selecting unit 1100 distinguishes the read operation and the write operation for the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, and is selectively connected to the first and second data input/output lines GIO_Rank0 and GIO_Rank1." *Id.* at [0045]. As a result, "the read and write data may be transmitted through the first data input/output line GIO_Rank0 during the read and write operations of the first rank Rank0, and the read and write data may be transmitted through the second data

input/output line GIO_Rank1 during the read and write operations of the second rank Rank1." *Id.* at [0045].

231. A Skilled Artisan would have understood from this disclosure that the main chip C0 is a "*control die*" because it controls the operation of Kim's memory apparatus, including read and write operations in response to read and write commands from an external device.

232. Furthermore, in the combination of Kim and Rajan, the "*control die*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices on the memory module. *Supra* at ¶¶137-139, 146-164; *see also* Ex. 1015 (Rajan) at 6:30-7:67 (describing specific examples of rank multiplication).

233. Therefore, Kim discloses and renders obvious in light of Rajan this limitation to a Skilled Artisan.

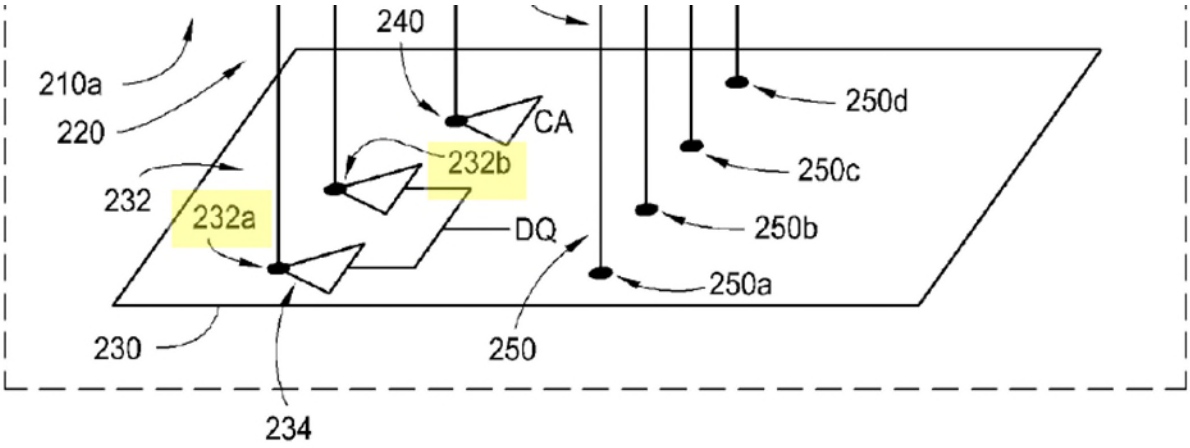
234. Accordingly, the prior art references in Ground 1 satisfy "*a control die comprising*."

(2) [1.e.2] and [1.e.3] First and Second Data Conduits

235. Claim 1 requires "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

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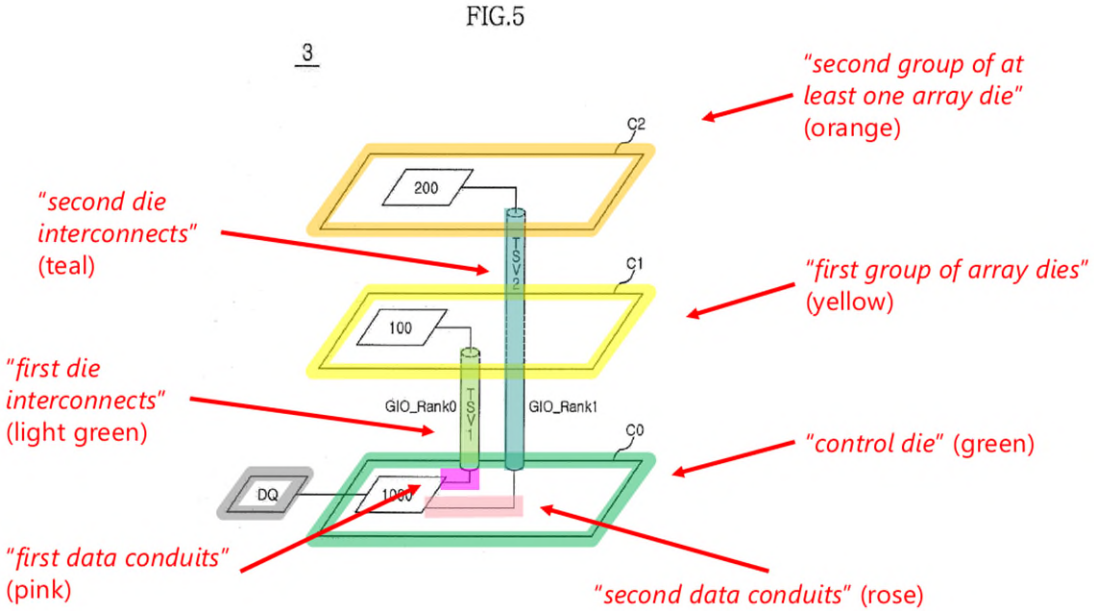
236. The prior art references in Ground 1 teach the claimed first and second "*data conduits*" to a Skilled Artisan. The 160 Patent discloses that "*data conduits*" are configured to transmit data signals to respective die interconnects. Ex. 1001 (160 Patent), *e.g.*, at 6:51-62, Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b).



"In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2." *Id*. 6:63-65. Similarly, "command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242" and "chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252." *Id*. at 9:31-63.

237. Kim discloses such "*first data conduits* [including signal lines (annotated pink below) for communicating data through data input/output section 1000] *between the first die interconnects* [such as TSV1 (annotated light green

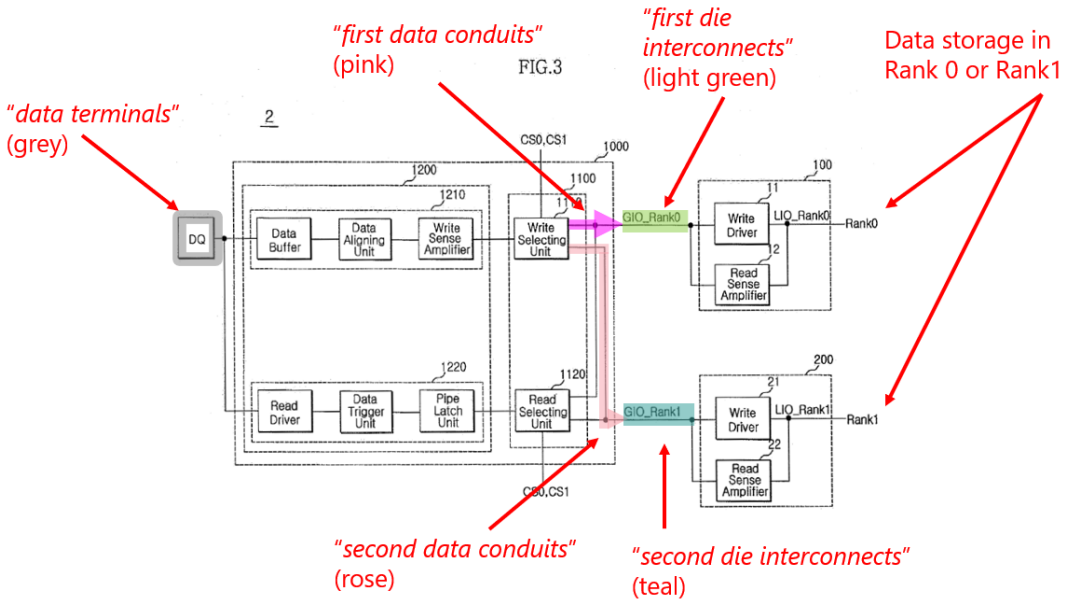
below)] *and the data terminals* [such as data pad DQ (annotated grey below)]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated). As discussed above with reference to claim elements [1.b] and [1.d], *supra* at ¶¶180-196, 215-225, a Skilled Artisan would have understood, and would have been obvious to her, that more than one data signal can be communicated between the control die (C0) and an array die (like C1 or C2) by using more die interconnects for TSV1, and for TSV2, each arranged as shown in Fig. 5 of Kim. *Id*. In such an arrangement, each die interconnect has a respective "*data conduit[]*" on the control die for transferring the corresponding data signal. *Id*.



238. For example, Kim discloses that "[d]ata transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0

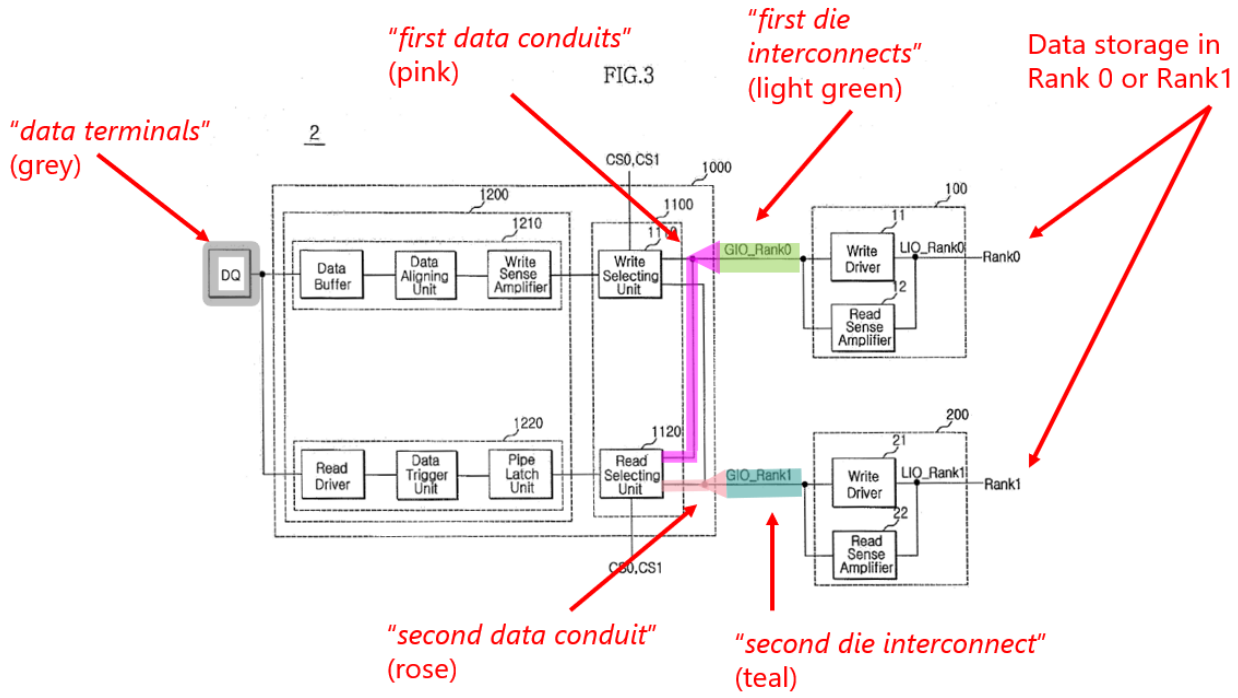
comprises a TSV TSV1 which connects the first slave chip C1 and the main chip C0." Ex. 1014 at [0049].

239. Kim explains that "[d]uring the write operation, when the first chip selection signal CS0 is enabled, the shared data input/output section 1000 outputs data, inputted through the data pad DQ, to the first data input/output line GIO_Rank0." *Id*. at [0030]; *see also id.* at Fig. 3 (reproduced below, annotated to show that "*first data conduits*" (colored pink) are active for a write operation to Rank0), [0035] ("During the write operation, the write selecting unit 1110 connects the first data input/output line GIO_Rank0 with the data input/output unit 1200 when the first chip selection signal CS0 is enabled, . . .").



240. Kim also explains that "[d]uring the read operation, when the first rank Rank0 is selected by the chip selection signals CS0 and CS1, that is, when a first chip selection signal CS0 is enabled, the shared data input/output section 1000

outputs data, transmitted through the first data input/output line GIO_Rank0, to the data pad DQ." *Id*. at [0029]; *see also id.* at Fig. 3 (reproduced below, annotated to show that "*first data conduits*" (colored pink) are active for a read operation from Rank0), [0036] ("During the read operation, the read selecting unit 1120 connects the first data input/output line GIO_Rank0 to the data input/output unit 1200 when the first chip selection signal CS0 is enabled, . . .").



241. Kim further explains that "[t]he write selecting unit 1110 and the read selecting unit 1120 may be realized using multiplexers which are connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1. While not shown in a

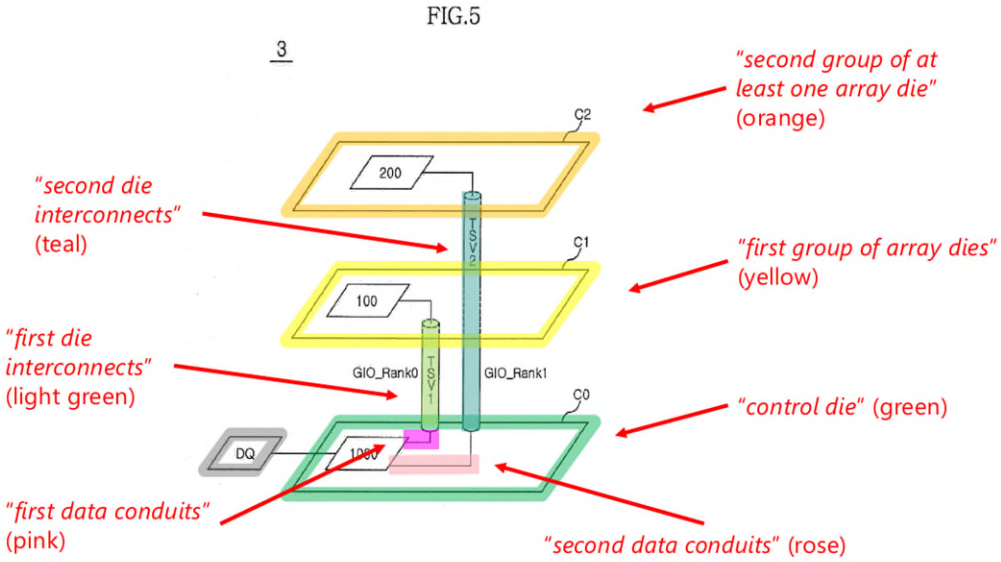
drawing, the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals." *Id*. at [0037-38].

242. A Skilled Artisan would have understood from this disclosure that the data conduits connecting the write selecting unit 1110 and the read selecting unit 1120 in data input/output section 1000 to a through-silicon via to Rank0 is between "*the first die interconnects*," e.g., TSV1, and a "*data terminal*," e.g., data pad DQ.

243. Therefore, Kim discloses "*first data conduits between the first die interconnects and the data terminals*" to a Skilled Artisan.

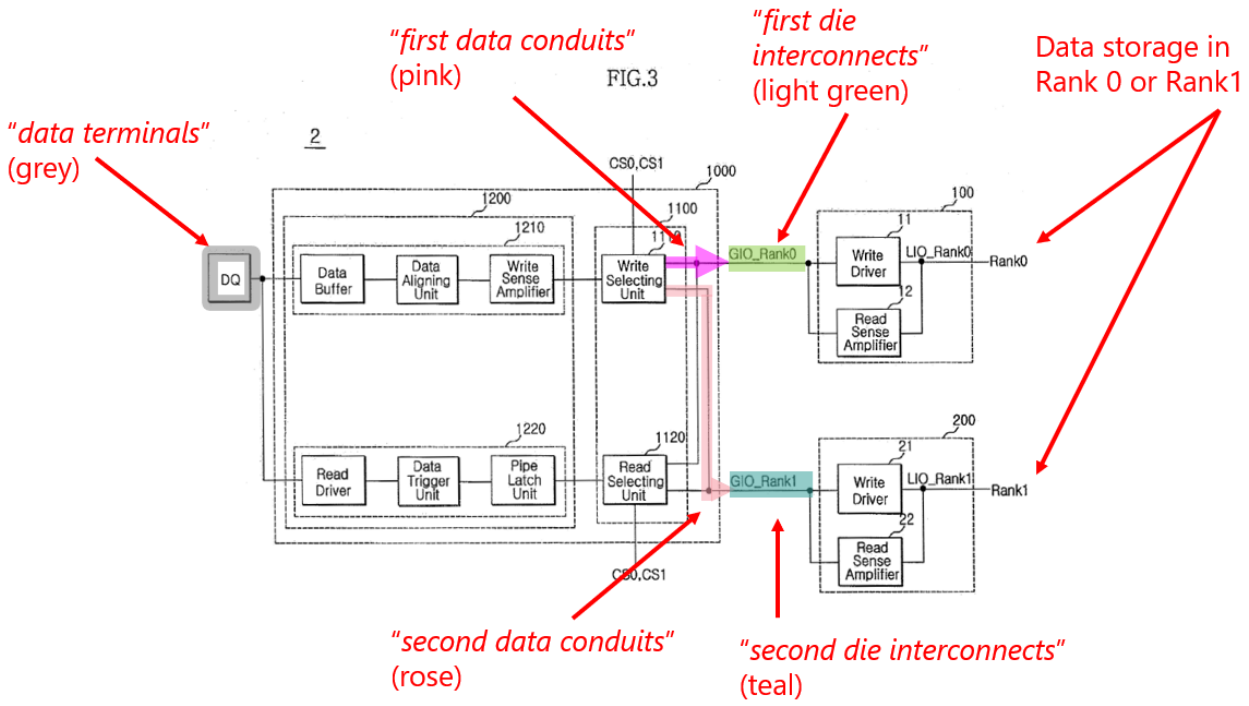
244. Kim also discloses and renders obvious to a Skilled Artisan "*second data conduits* [including signal lines (annotated rose below) for communicating data through data input/output section 1000] *between the second die interconnects* [such as TSV2 (annotated teal below)] *and the data terminals* [such as data pad DQ (annotated grey below)]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated). As discussed above, it would have been obvious to a Skilled Artisan to use multiple "*second data conduits*" and respective "*second die interconnects*" to communicate data signals between the control die (C0) and an array die (like C1 or C2).

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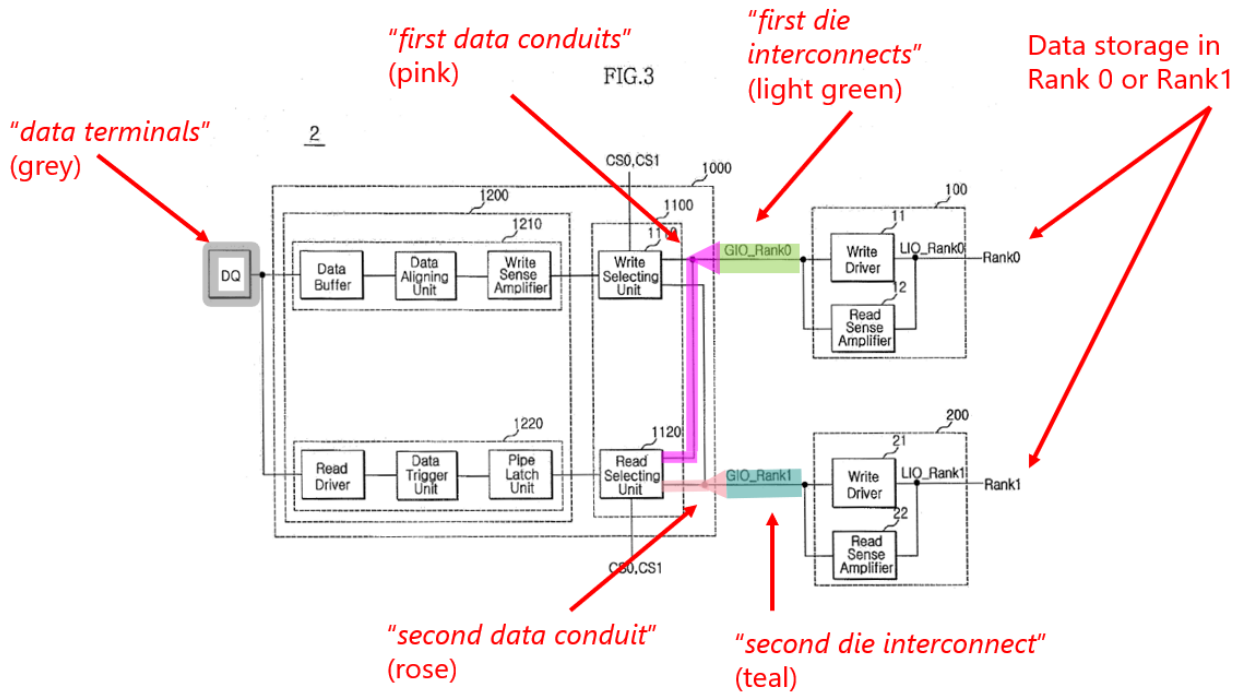


245. For example, Kim discloses that "[d]ata transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1 comprises a TSV TSV2 which connects the second slave chip C2 and the main chip C0." Ex. 1014 at [0049].

246. Kim explains that "during the write operation, when the second chip selection signal CS1 is enabled, the shared data input/output section 1000 outputs data, inputted through the data pad DQ, to the second data input/output line GIO_Rank1." *Id*. at [0030]; *see also id.* at Fig. 3 (reproduced below, annotated to show "*second data conduits*" (colored rose) are active for a write operation to Rank1), [0035] ("During the write operation, the write selecting unit 1110 . . . connects the second data input/output line GIO_Rank1 to the data input/output unit 1200 when the second chip selection signal CS1 is enabled.").



247. Kim also explains that "during the read operation, when the second rank Rank1 is selected by the chip selection signals CS0 and CS1, that is, when a second chip selection signal CS1 is enabled, the shared data input/output section 1000 outputs data transmitted through the second data input/output line GIO_Rank1 to the data pad DQ." *Id*. at [0029]; *see also id.* at Fig. 3 (reproduced below, annotated to show "*second data conduits*" (colored rose) are active for a read operation from Rank1), [0036] ("During the read operation, the read selecting unit 1120 . . . connects the second data input/output line GIO_Rank1 to the data input/output unit 1200 when the second chip selection signal CS1 is enabled.")



248. A Skilled Artisan would have understood from this disclosure that data conduits connecting the data input/output section 1000 to TSVs like TSV2 are between "*the second die interconnects*," e.g., TSV2, and the "*data terminals*," e.g., data pad DQ.

249. For the reasons discussed above with reference to claim limitation [1.b], Kim discloses that the data pad DQ is an example of "*data terminals*." *Supra* ¶¶180-196.

250. Therefore, Kim discloses "*second data conduits between the second die interconnects and the data terminals*" to a Skilled Artisan.

251. Therefore, the prior art references in Ground 1 satisfy "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

(3) [1.e.4] and [1.e.5] First and Second Drivers

252. Claim 1 requires "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size*."

253. These claim limitations, as written, lack proper antecedent basis for the terms "*the first data conduit*" and "*the second data conduit*," since claim elements [1.e.2] and [1.e.3] recite "*first data conduit**s***" and "*second data conduit**s***," making it unclear which of these plural "*conduit**s***" the singular terms "*the first data conduit*" and "*the second data conduit*" refer to. In any event, my analysis below shows that each of the "*first data conduits*" and "*second data conduits*" can include one or more drivers, *infra* ¶260, thus rendering this limitation obvious either way despite its ambiguity.

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254. Therefore, the prior art references in Ground 1 teach this limitation to a Skilled Artisan.

255. In particular, Kim in combination with Wyman renders obvious "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*."

256. As discussed above with reference to claim element [1.e.2], Kim discloses that each of the claimed "*first data conduits*" (pink) communicates, through data input/output section 1000, "*a data signal from a corresponding data terminal* [(grey) to TSV1 (light green) which, in turn, is electrically connected] *to the first group of array dies*." *Supra* ¶¶237-243; *see, e.g.*, Ex. 1014 at Figs. 3 and 5 (reproduced below, annotated).

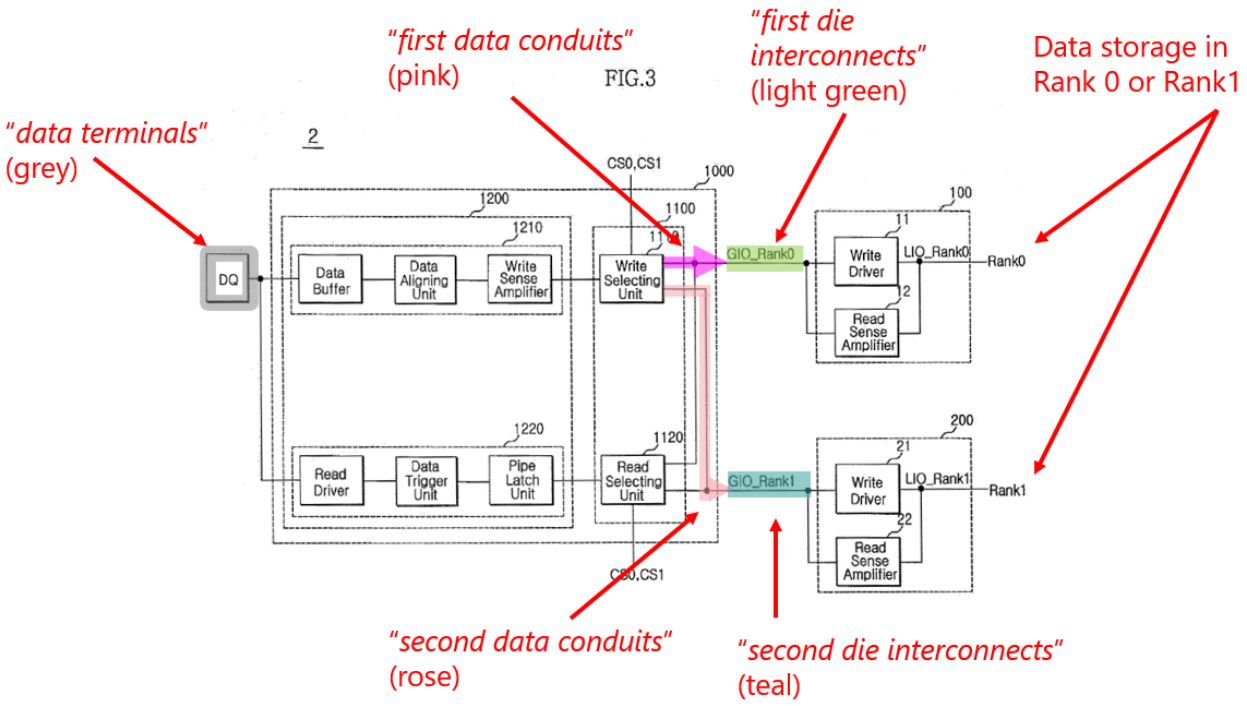
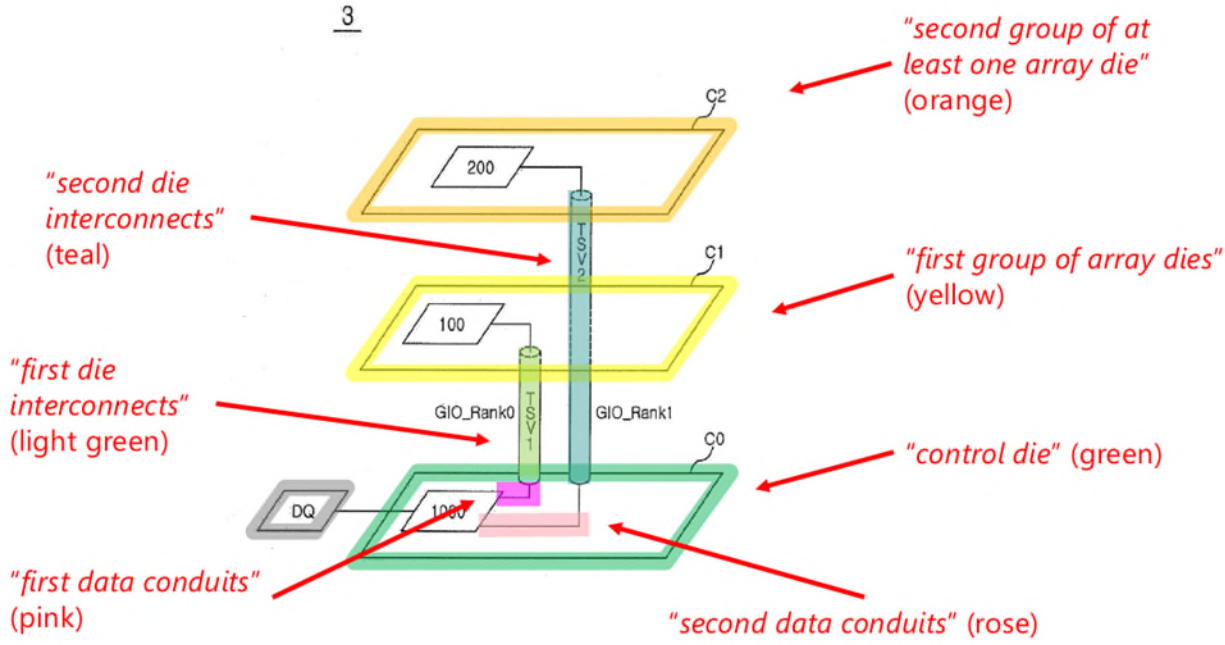


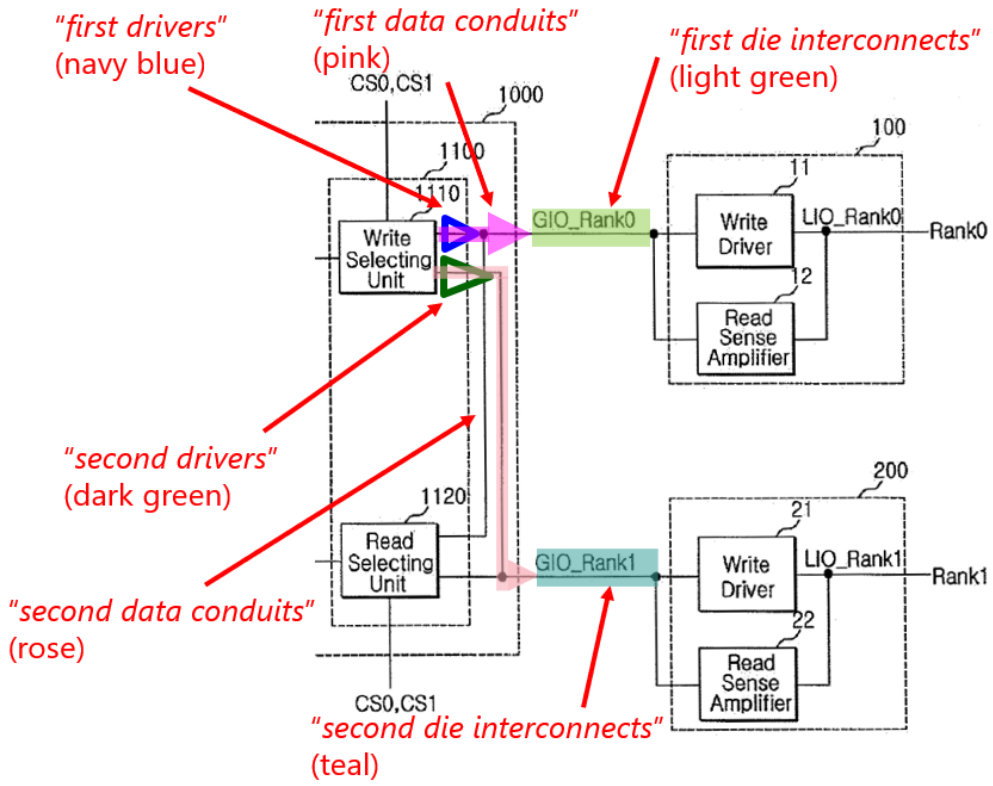
FIG.5



257. As expressly shown in this figure of Kim, the die interconnects like TSV1 (light green) coupled to the "*first data conduits*" (pink) are shorter than the die interconnects like TSV2 (teal) coupled to the "*second data conduits*" (rose). A

Skilled Artisan would have understood that, due to this difference in length of TSV1 and TSV2, each of the "*first data conduits*" and the "*second data conduits*" can include a respective driver that is optimized for driving the data signal through the corresponding TSV in an efficient way. For example, Wyman explains that, "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 at 1:22-24. Therefore, a Skilled Artisan would have been motivated to follow the teaching of Wyman in the system of Kim and avoid using full capacity drivers, thus saving power and not being "wasteful and inefficient." *Id*. Such an arrangement of having separate drivers (e.g., "*first drivers*" having a "*first driver size*," navy blue, and "*second drivers*" having a "*second driver size*," dark green) for each data conduit is illustrated in annotated (partial) Fig. 3 of Kim, reproduced below. *See* Ex. 1014 at Fig. 3 (reproduced below, in part, annotated).

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258. As discussed above, a Skilled Artisan would have understood and been motivated to turn to analogous art like Wyman to implement the stacked devices of Kim with efficient driving signals between the stacks. *Supra* ¶¶165-171. For example, Wyman discloses that longer interconnects in a stacked arrangement require larger driving force. Ex. 1017 at Figs. 7, 8 (reproduced below).

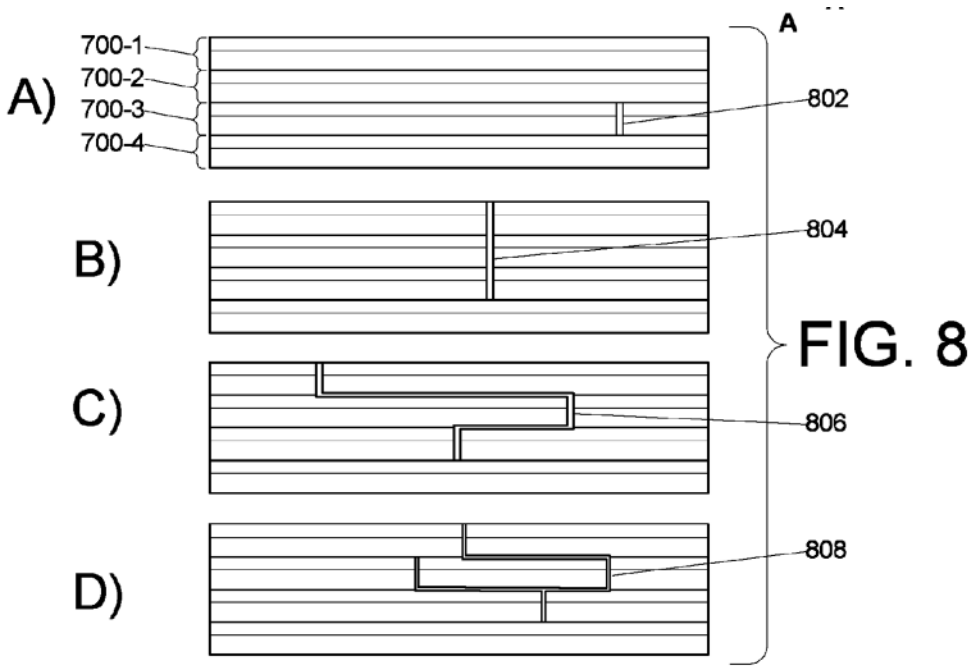


FIG. 8

259. Wyman explains that "FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3) … requir[ing] minimal drive … FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. …" *Id*. at 6:15-30. However, Wyman recognizes that even with the "significantly longer connection (808) between the mother chip (700-4) with a fan out to both daughter 2 (700-2) and daughter 3 (7001)," as shown in Fig. 8.D, using "the total drive … would be overkill." *Id*. at 6:44-50.

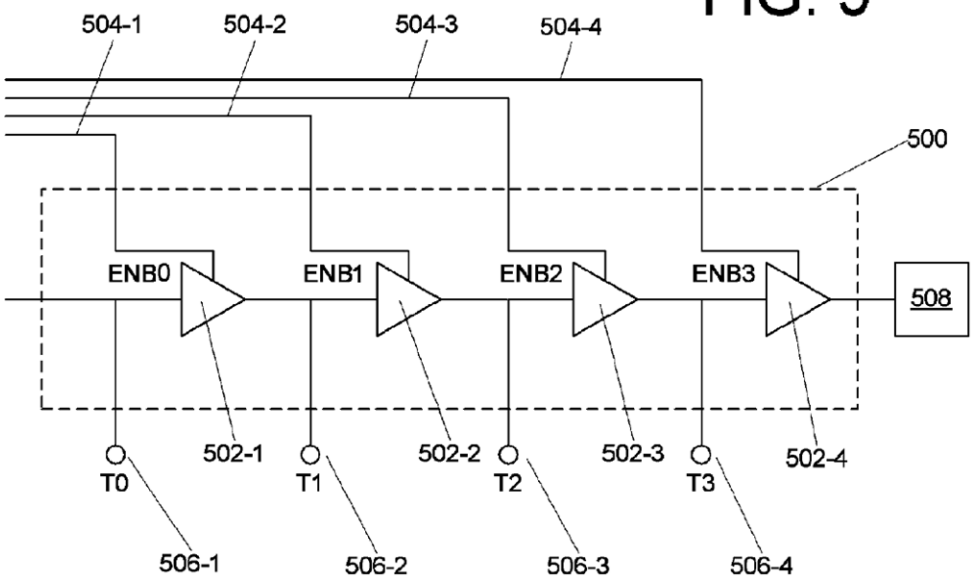
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260. A Skilled Artisan would have understood from this disclosure that the longer the connection in a stack of chips, the more drive it requires, but using the "total drive" would be wasteful. Ex. 1017 at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use drivers of different strengths (i.e., "*first drivers*" having a "*first driver size*" and "*second drivers*" having a "*second driver size*") for Kim's different sized through-silicon vias TSV1 and TSV2. Ex. 1017 (Wyman) at 2:61-65 ("Ultimately, instead of implementing a singular driver in the design phase, a designer need only supplement a few cascaded drivers in its place, thus allowing the designer to take full advantage of routing and which will ultimately result in power savings."). As discussed above, a Skilled Artisan would have been motivated to drive the shorter TSV1 with a smaller drive and the longer TSV2 with a larger drive to use power in an efficient manner as taught by Wyman. *Supra* ¶¶165-171; *see also* annotated partial Fig. 3 of Kim above. Making such a combination was well within the level of skill, since Wyman itself teaches drivers of different sizes, and the combination would have provided nothing more than expected: a power efficient drive of signals through Kim's TSVs. For example, Wyman discloses a circuitry that includes one or more drivers (502-1 to 502-4) that are selectively activated to achieve the optimal driving strength. Ex. 1017 at Fig. 5

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(reproduced below), 5:11-14 ("Similar to FIG. 2 through FIG. 4, a designer may now utilize and tap-off at five locations (506-1, 506-2, 506-3, 506-4, 508) depending on the drive requirements for a specific element or device.").

FIG. 5



See also id. at Figs. 10, 11 and 7:14-18 ("The circuitry of FIG. 10, FIG. 11, those of the prior figures, as well as the myriad of circuit variants thereof that can be configured to operate in a similar manner, advantageously allows the output drive current to be modified to meet the requirements of a particular output load."); *see also supra* at ¶¶134-136.

261. Therefore, the combination of Kim and Wyman renders obvious "*the first data conduit including first drivers each having a first driver size and*

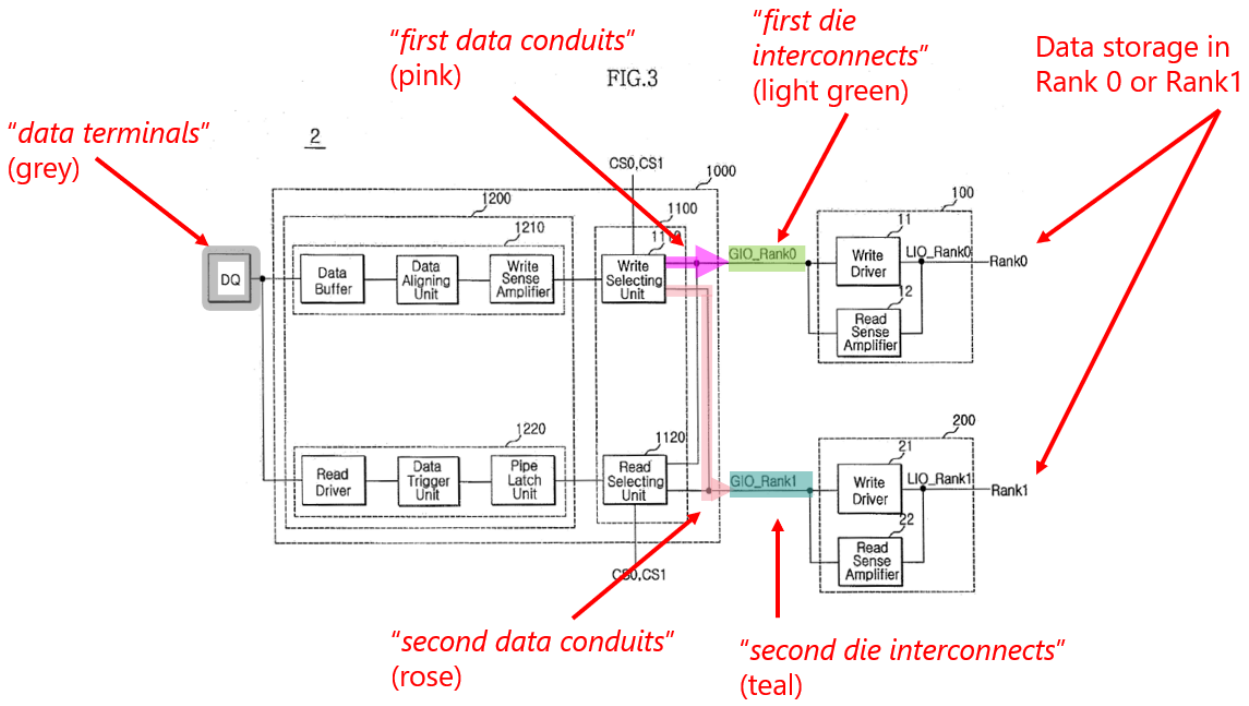
Samsung Electronics Co., Ltd.
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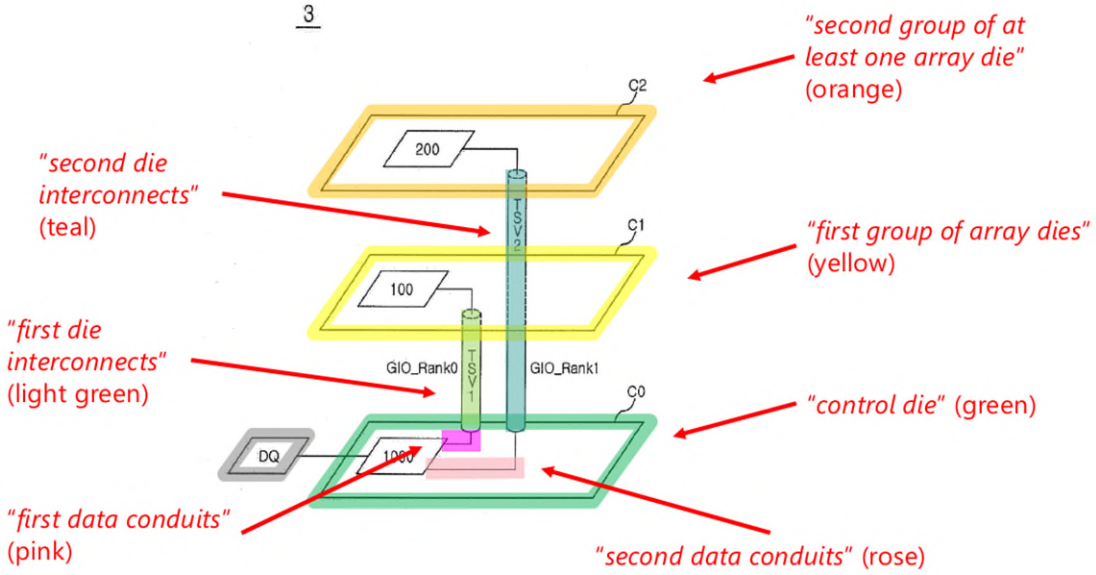
configured to drive a data signal from a corresponding data terminal to the first group of array dies" to a Skilled Artisan.

262. Kim in combination with Wyman also renders obvious "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size*."

263. As discussed above with reference to claim limitation [1.e.3], this limitation lacks the proper antecedent basis, but it is rendered obvious either way despite its ambiguity. *Supra* at ¶253. Kim discloses the claimed "*second data conduits*" (rose) to die interconnects like TSV2 to communicate "*a data signal from a corresponding data terminal* [to TSV2 which, in turn, is electrically connected] *to the second group of at least one array die*." *Supra* ¶¶244-251; *see, e.g.*, Ex. 1014 at Figs. 3 and 5 (reproduced below, annotated).

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264. As further discussed above with reference to the "*first drivers*" (claim element [1.e.4]), in light of the teaching of Wyman, it would have been obvious to a Skilled Artisan to use "*second drivers each having a second driver size*" to drive the signals through TSVs like TSV2. *Supra* ¶¶252-261. As also discussed above, a

Skilled Artisan would have been motivated to drive the longer TSV2 with a larger total drive and the shorter TSV1 with a smaller total drive to use power in an efficient manner as taught by Wyman. *See id.* Thus, the combination of Kim and Wyman teaches to a Skilled Artisan that "*the second driver size … [is] different from the first driver size*."

265. Therefore, the combination of Kim and Wyman renders obvious this limitation to a Skilled Artisan.

266. Accordingly, the prior art references in Ground 1 satisfy "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size*."

2. Claim 2 is Unpatentable

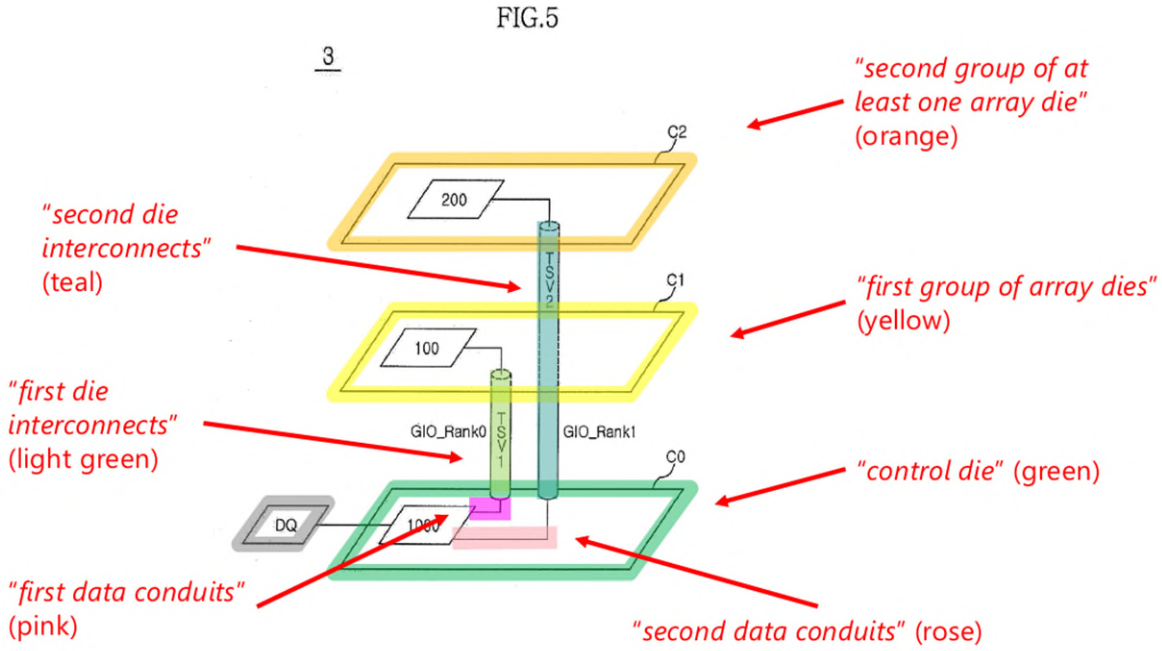
267. Claim 2 is unpatentable as the prior art references in Ground 1 render the claim obvious.

268. Claim 2 requires "*[t]he memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size*."

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269. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

270. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], Kim in combination with Wyman renders obvious that "*the second die interconnects* [like TSV2 (annotated teal below)] *are longer than the first die interconnects* [like TSV1 (annotated light green below)]*, and wherein the second driver size is larger than the first driver size*" because the longer TSV2 of Kim is driven with a larger drive than the shorter TSV1 as taught by Wyman. *Supra* ¶¶252-266; *see, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).



271. Therefore, the combination of Kim and Wyman renders obvious this limitation to a Skilled Artisan.

272. Accordingly, the prior art references in Ground 1 satisfy "*wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size*" limitation.

3. Claim 3 is Unpatentable

273. Claim 3 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [3.a] Second Die Interconnects are Longer than First Die Interconnects

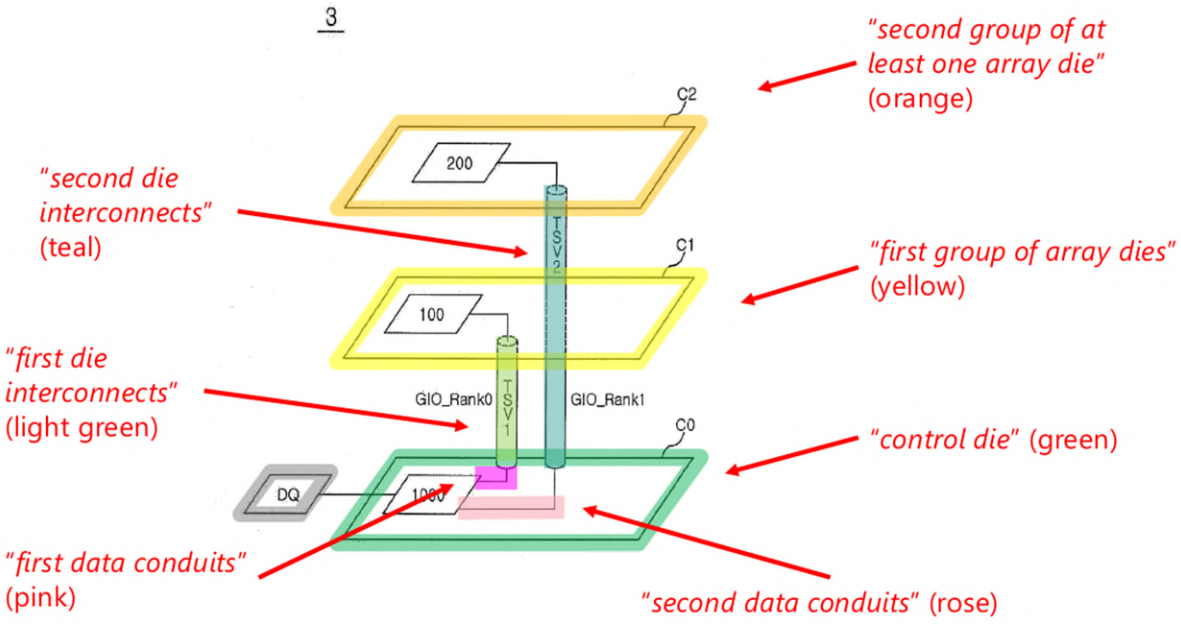
274. Claim 3 requires "*[t]he memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects*."

275. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

276. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], Kim discloses that "*the second die interconnects* [like TSV2 (annotated teal below)] *are longer than the first die interconnects* [like TSV1 (annotated light green below)]." *Supra* ¶¶252-266; *see, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).

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FIG.5



277. Therefore, Kim discloses this limitation.

278. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the second die interconnects are longer than the first die interconnects*" limitation.

b) [3.b] Number of Array Dies in the Second Group is Less Than Number of Array Dies in the First Group

279. Claim 3 also requires "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*."

280. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

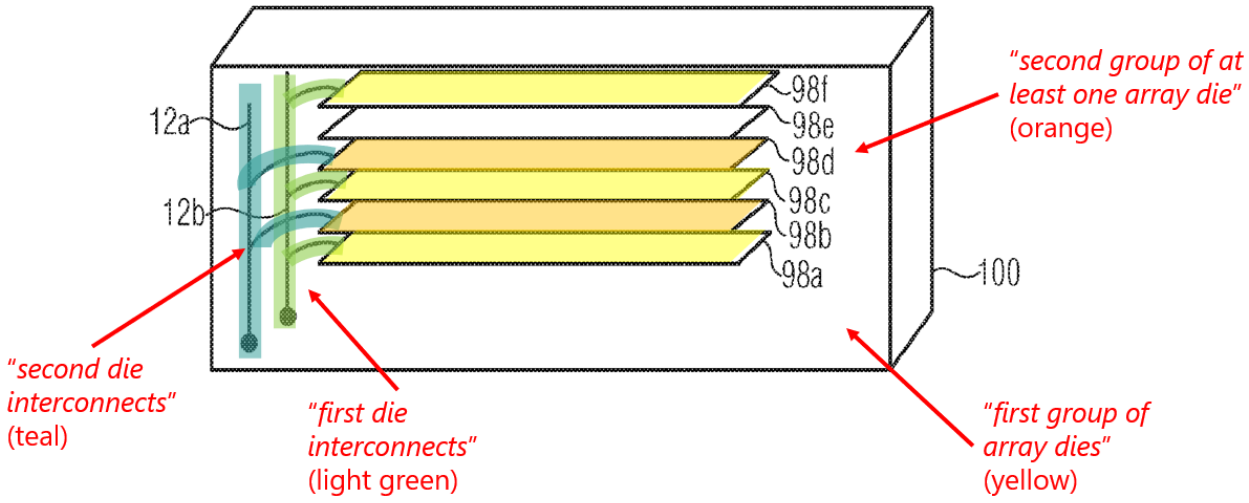
281. Kim in combination with Rajan renders obvious that "*a number of array dies in the second group of at least one array die* [coupled to TSV2] *is less than a number of array dies in the first group of array dies* [coupled to TSV1]."

282. For example, Kim discloses that, "although only one main chip and two slave chips are shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used." Ex. 1014 at [0048]. Furthermore, Kim explains that "[w]hile the semiconductor memory apparatuses having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks." *Id.* at [0050]; *see also id.* at [0027] ("The ranks can be defined in a variety of ways. For example, one chip may operate as a plurality of ranks and a plurality of chips may operate as a plurality of ranks.").

283. Furthermore, Rajan discloses that, in a memory stack, "the memory circuits may be symmetrical, meaning each has the same capacity, type, speed, etc., while in other embodiments they may be asymmetrical." Ex. 1015 at 2:62-65. For example, "each of the DRAM chips may have the same page size, regardless any differences in the capacities of the (asymmetrical) DRAM chips." *Id*. at 7:63-67.

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284. A Skilled Artisan would have understood from this disclosure that a memory stack can include chips of different capacities implementing one or more ranks. A Skilled Artisan would have also understood that, in such an "asymmetrical" stack, different number of array dies can be coupled to a TSV for data transmission, depending on the specific capacities of the memory chips and the specific arrangement of ranks. *See, e.g.*, Ex. 1024 (Ruckerbauer (US7,796,446)) at Fig. 5 (reproduced below, annotated), 9:14-18 ("[W]ithin the memory stack 100, a first sub set of memory dies is coupled to the first transfer data path 12a and a second sub set is coupled to the second transfer data path 12b. These different sub sets could, for example, be associated to different ranks within the stack 100.").



285. Therefore, a Skilled Artisan would have understood that the number of array dies in any given group is an obvious design choice, depending on the

configuration and mode of operation of the memory stack. *See* Ex. 1024 (Ruckerbauer) at 8:58-66. For example, the number of dies in one group can be less than the number of dies in another group. *See, e.g.*, *id.* at Fig. 5 (reproduced above, annotated, showing three dies in a first group of array dies (yellow) and two dies in a second group of array dies (orange)).

286. Furthermore, a Skilled Artisan would have understood that the load on a given TSV increases with the length of the TSV and with the number of dies connected to the TSV (i.e., the longer the TSV and the greater the number of dies connected to the TSV, the larger the load on the TSV), and driving a signal on a TSV having larger load requires a larger driver which uses more power. *Supra* at ¶¶134-136. For example, Wyman discloses that longer interconnects in a stacked arrangement require larger driving force. Ex. 1017 at Figs. 7, 8 (reproduced below).

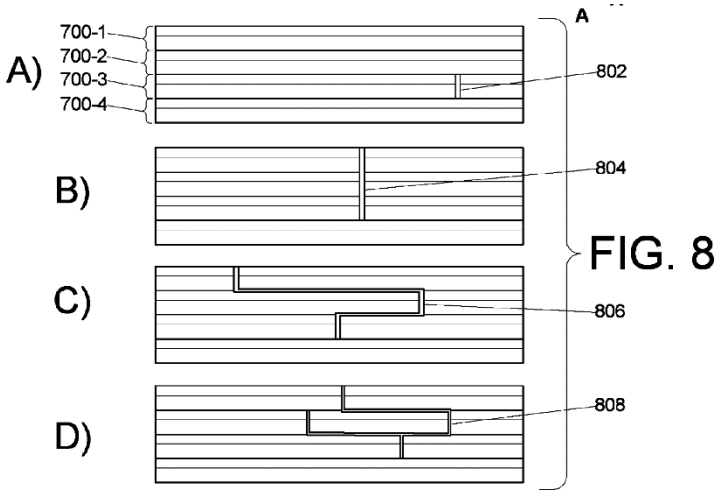


FIG. 8

287. Wyman explains that "FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3) … requir[ing] minimal drive … FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. …." *Id*. at 6:15-30. Wyman further explains that "[t]he circuitry of FIG. 10, FIG. 11, those of the prior figures, as well as the myriad of circuit variants thereof that can be configured to operate in a similar manner, advantageously allows the output drive current to be modified to meet the requirements of a particular output load. … For example, a circuit could be used to drive a large output load associated with the IC on a circuit board by turning all the transistor stages on. In addition, some of the transistors could be programmed to be off to thereby reduce the power requirements when only a small load is to be driven." *Id*. at 7:14-26.

288. Therefore, in an asymmetric arrangement where TSVs of different lengths are connected to different number of dies, a Skilled Artisan would have been motivated to arrange the stack in a way that a longer TSV has fewer dies connected to it in order to reduce the power requirements of driving the longer TSV. *See, e.g.*, Ex. 1017 (Wyman) at 2:61-65 ("Ultimately, instead of

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implementing a singular driver in the design phase, a designer need only supplement a few cascaded drivers in its place, thus allowing the designer to take full advantage of routing and which will ultimately result in power savings.").

289. Therefore, Kim in combination with Rajan and Wyman renders obvious this limitation to a Skilled Artisan.

290. Accordingly, the prior art references in Ground 1 satisfy the "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*" limitation.

4. Claim 4 is Unpatentable

291. Claim 4 is unpatentable as the prior art references in Ground 1 render the claim obvious.

292. Claim 4 requires "*[t]he memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.*"

293. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

294. Kim in combination with Wyman renders obvious that "*the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.*"

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295. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], the combination of Kim and Wyman teaches that a driver size in a stacked arrangement is related to the load (including the length of the TSV) on the respective driver. *Supra* ¶¶252-266. For example, Wyman explains that "[t]he circuitry of FIG. 10, FIG. 11, those of the prior figures, as well as the myriad of circuit variants thereof that can be configured to operate in a similar manner, advantageously allows the output drive current to be modified to meet the requirements of a particular output load. … For example, a circuit could be used to drive a large output load associated with the IC on a circuit board by turning all the transistor stages on. In addition, some of the transistors could be programmed to be off to thereby reduce the power requirements when only a small load is to be driven." Ex. 1017 at 7:14-26.

296. A Skilled Artisan would have understood from this disclosure that, in the combination of Kim and Wyman, "*the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*." *Supra* ¶¶134-136.

297. Accordingly, the prior art references in Ground 1 satisfy "*wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*."

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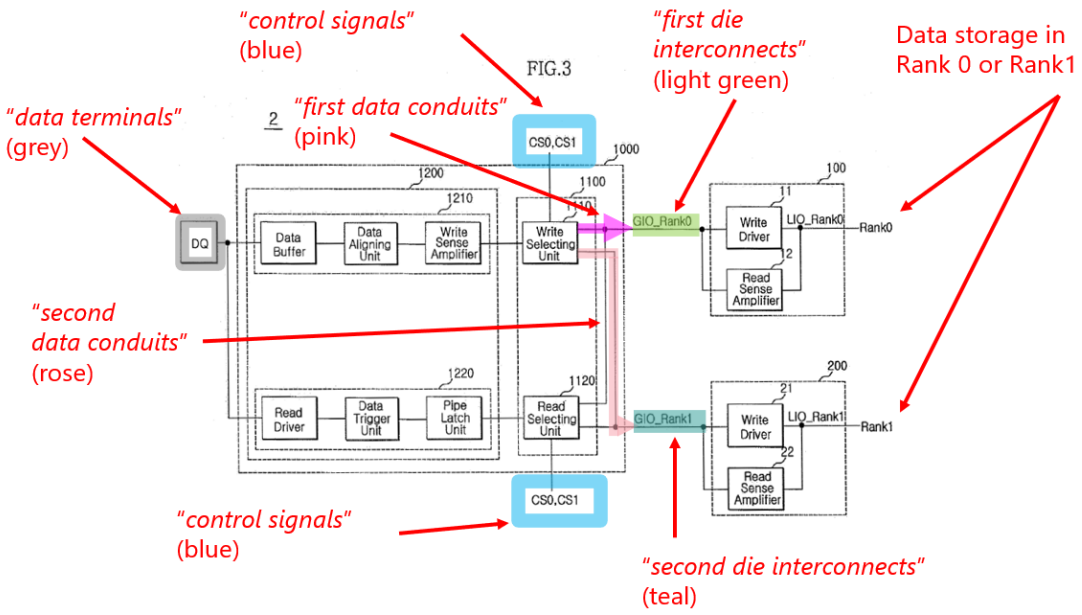
5. Claim 5 is Unpatentable

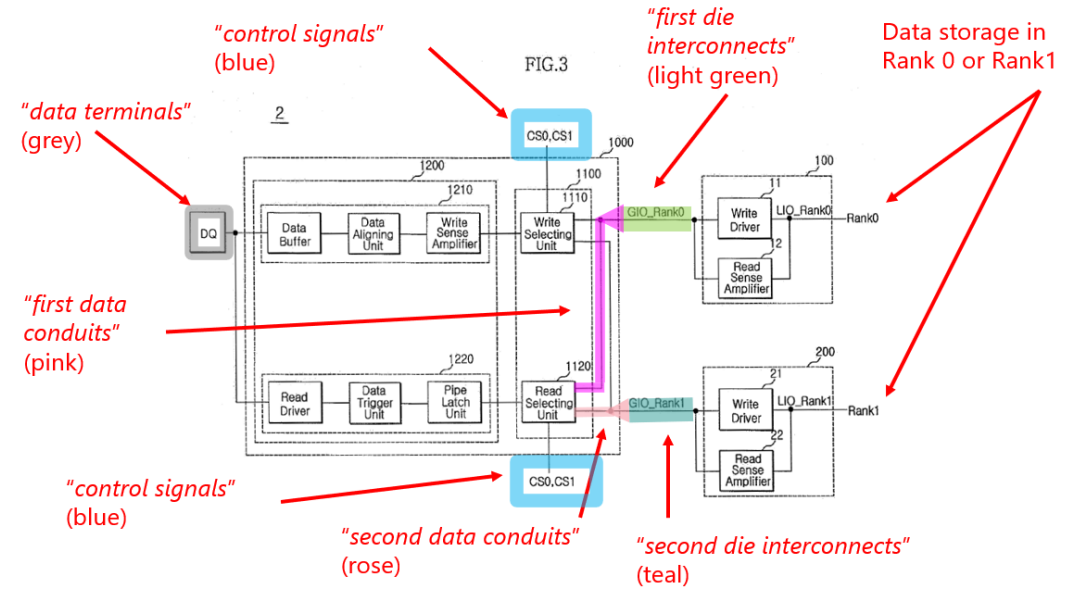
298. Claim 5 is unpatentable as the prior art references in Ground 1 render the claim obvious.

299. Claim 5 requires *"[t]he memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals*."

300. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

301. Kim discloses to a Skilled Artisan that "*the control die* [main chip C0] *further comprises a control circuit* [in rank selecting unit 1100] *to control respective states* [e.g., for communicating read and write data to and from one or the other] *of the first data conduits* [(annotated pink below) to TSV1] *and the second data conduits* [(annotated rose below) to TSV2] *in response to control signals* [including chip selection signal CS0 and CS1 and read and write command signals] *received via the control terminals* [from an external device]." *See, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





302. For example, Kim discloses that the "rank selecting unit 1100 includes a write selecting unit 1110 and a read selecting unit 1120. The write selecting unit 1110 is activated during the write operation and is connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1." Ex. 1014 at [0035]. Kim

explains that "[t]he read selecting unit 1120 is activated during the read operation and is connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1." *Id.* at [0036]. Kim discloses that "the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals," and that "[t]he internal write and read signals may be signals that are generated because write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered." *Id.* at [0038]. Likewise, Kim explains that "[t]he chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2 and buffered." *Id.* at [0032].

303. A Skilled Artisan would have understood from this disclosure that the rank selecting unit 1100 includes a control circuit that receives control signals, including chip selection signals and read and write command signals from an external device and, in response, controls the write and read selecting units 1110 and 1120 to direct the data transfer selectively to or from TSV1 through the "*first data conduits*" (pink) or to or from TSV2 through the "*second data conduits*" (rose). Therefore, the state of those "*data conduits*" is controlled to be active or not active and to transmit data in the read or write direction.

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304. Furthermore, as discussed above with reference to claim element [1.b], a Skilled Artisan would have understood that the chip selection and read and write command signals are "*received via the control terminals.*" *Supra* ¶¶180-196.

305. Therefore, Kim discloses this limitation to a Skilled Artisan.

306. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminal*" limitation.

6. Claim 6 is Unpatentable

307. Claim 6 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [6.a] Preamble

308. Claim 6 requires *"[a] memory package, comprising*."

309. To the extent the preamble is limiting, the prior art references in Ground 1 teach this limitation to a Skilled Artisan.

310. As shown in the table below, the preamble of claim 6 is identical to the preamble of claim 1:

Claim 1	**Claim 6**
[1.a] A memory package, comprising:	[6.a] A memory package, comprising:

311. As discussed above with reference to the preamble of claim 1, to the extent the preamble of claim 1 is limiting, the prior art references in Ground 1 satisfy "*[a] memory package, comprising*." *Supra* ¶¶174-179.

b) [6.b] Data Terminals and Control Terminals

312. Claim 6 requires "*data terminals and control terminals*."

313. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

314. As shown in the table below, claim limitation [6.b] is identical to claim limitation [1.b]:

Claim 1	**Claim 6**
[1.b] data terminals and control terminals	[6.b] data terminals and control terminals

315. As discussed above with reference to claim limitation [1.b], the prior art references in Ground 1 satisfy "*data terminals and control terminals*." *Supra* ¶¶180-196.

c) [6.c] Stacked Array Dies

316. Claim 6 requires "*stacked array dies including a first group of array dies and a second group of at least one array die*."

317. As shown in the table below, claim limitation [6.c] is identical to claim limitation [1.c]:

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Claim 1	**Claim 6**
[1.c] stacked array dies including a first group of array dies and a second group of at least one array die	[6.c] stacked array dies including a first group of array dies and a second group of at least one array die

318. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 1 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶197-214.

d) [6.d.1] and [6.d.2] First and Second Die Interconnects

319. Claim 6 requires "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

320. As shown in the table below, claim limitations [6.d.1] and [6.d.2] are identical to claim limitations [1.d.1] and [1.d.2], respectively:

Claim 1	**Claim 6**
[1.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,	[6.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
[1.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[6.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

321. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 1 satisfy "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶215-225.

e) [6.e] Second Die Interconnects are Longer than the First Die Interconnects

322. Claim 6 requires "*wherein the second die interconnects are longer than the first die interconnects*."

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323. As shown in the table below, claim limitation [6.e] is nearly identical to claim limitation [3.a]:

Claim 3	**Claim 6**
[3.a] . . ., wherein the second die interconnects are longer than the first die interconnects, and	[6.e] wherein the second die interconnects are longer than the first die interconnects, and

324. As discussed above with reference to claim limitation [3.a], the prior art references in Ground 1 satisfy "*wherein the second die interconnects are longer than the first die interconnects*." *Supra* ¶¶274-278.

f) [6.f] Number of Array Dies in the Second Group is Less than Number of Array Dies in the First Group

325. Claim 6 also requires "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*."

326. As shown in the table below, claim limitation [6.f] is identical to claim limitation [3.b]:

Claim 3	**Claim 6**
[3.b] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.	[6.f] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

327. As discussed above with reference to claim limitation [3.b], the prior art references in Ground 1 satisfy "*wherein a number of array dies in the second*

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group of at least one array die is less than a number of array dies in the first group of array dies." *Supra* ¶¶279-285.

7. Claim 7 is Unpatentable

328. Claim 7 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [7.a] A Control Die Comprising

329. Claim 7 requires *"[t]he memory package of claim 6, further comprising: a control die comprising*."

330. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

331. As shown in the table below, claim limitation [7.a] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 7**
[1.e.1] a control die comprising	[7.a] The memory package of claim 6, further comprising: a control die comprising

332. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 1 satisfy "*a control die comprising*." *Supra* ¶¶226-234.

b) [7.b.1] and [7.b.2] The First and Second Data Conduits

333. Claim 7 requires "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

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334. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

335. As shown in the table below, claim limitations [7.b.1] and [7.b.2] are identical to claim limitations [1.e.2] and [1.e.3], respectively:

Claim 1	**Claim 7**
[1.e.2] first data conduits between the first die interconnects and the data terminals, and [1.e.3] second data conduits between the second die interconnects and the data terminals,	[7.b.1] first data conduits between the first die interconnects and the data terminals, and [7.b.2] second data conduits between the second die interconnects and the data terminals,

336. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Ground 1 satisfy "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*." *Supra* ¶¶235-251.

c) [7.c.1] and [7.c.2] First and Second Drivers

337. Claim 7 also requires "*the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at*

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least one array die, the second driver size being different from the first driver size."

338. As shown in the table below, claim limitations [7.c.1] and [7.c.2] are nearly identical to claim limitations [1.e.4] and [1.e.5]:

Claim 1	**Claim 7**
[1.e.4] the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [1.e.5] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.	[7.c.1] the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [7.c.2] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.

339. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], the singular "*first data conduit*" and "*second data conduit*" lack antecedent basis, but those limitations are obvious even if they are interpreted to be plural "*first data conduit**s***" and plural "*second data conduit**s***." *See supra* ¶253. Thus, the prior art references in Ground 1 satisfy "*the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data*

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conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size." *Supra* ¶¶252-266.

8. Claim 8 is Unpatentable

340. Claim 8 is unpatentable as the prior art references in Ground 1 render the claim obvious.

341. Claim 8 requires "*[t]he memory package of claim 7, wherein the second driver size is larger than the first driver size.*"

342. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

343. As shown in the table below, claim 8 is very similar to claim 2:

Claim 2	**Claim 8**
[2] The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size.	[8] The memory package of claim 7, wherein the second driver size is larger than the first driver size.

344. As discussed above with reference to claim 2, the prior art references in Ground 1 satisfy "*wherein the second driver size is larger than the first driver size*." *Supra* ¶¶267-272.

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9. Claim 9 is Unpatentable

345. Claim 9 is unpatentable as the prior art references in Ground 1 render the claim obvious.

346. Claim 9 requires "*[t]he memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.*"

347. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

348. As shown in the table below, claim 9 is very similar to claim 5:

Claim 5	**Claim 9**
[5] The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.	[9] The memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.

349. As discussed above with reference to claim 5, the prior art references in Ground 1 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals*." *Supra* ¶¶298-306.

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350. The phrase "*the plurality of terminals*" lacks antecedent basis, but a Skilled Artisan would have understood that the "*control terminals*" from claim element [6.b] could also be "*one or more second terminals of the plurality of terminals*," the plurality of terminals including both the "*data terminals*" and the "*control terminals*" from [6.b]. *Supra* ¶¶312-315 (citing ¶¶180-196).

351. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals*" limitation.

10. Claim 10 is Unpatentable

352. Claim 10 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [10.a] Preamble

353. The preamble of claim 10 requires "*[a] memory module operable in a computer system with a system memory controller, comprising*."

354. To the extent the preamble is limiting, the prior art references in Ground 1 teach this limitation to a Skilled Artisan.

355. The combination of Kim and Rajan discloses a "*memory module operable in a computer system with a system memory controller.*"

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356. For example, Rajan discloses a "*memory module*," such as a DIMM, that includes stacked memory devices. *See, e.g.*, Ex. 1015 at Fig. 8 (reproduced below), 8:52-54 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804….").

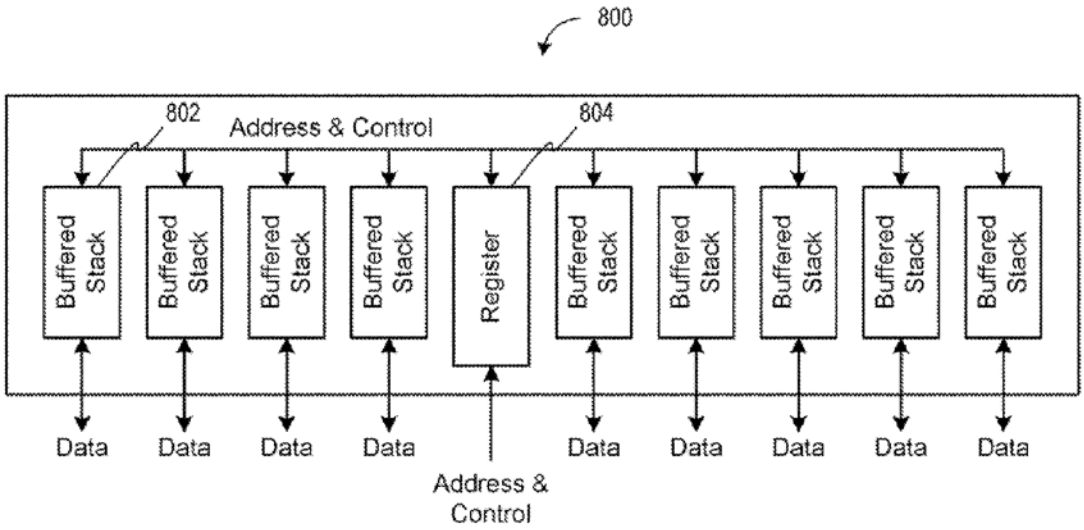


FIG. 8

357. Kim also discloses stacked memory devices. Ex. 1014 at [0050] ("It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked.").

358. As discussed above, a Skilled Artisan would have understood, and been motivated, to implement Kim's stacked memory devices in a memory module as disclosed by Rajan. *Supra* ¶¶146-164; *see, e.g.*, Ex. 1015 (Rajan) at 1:28-32 ("In other systems, groups of memory chips are first coupled into memory modules,

such as dual in-line memory modules (DIMMs), which are in turn coupled into a system by means of slots, sockets, or other connectors."), 15:3-12 ("The physical memory circuits employed in practicing this invention may be any type of memory whatsoever …. The physical memory circuits may be coupled to any type of memory module…."). For example, a Skilled Artisan would have been motivated to implement Kim's stacked devices in a DIMM format so that it can be used in systems that include sockets for DIMMs.

359. Rajan further explains that its "system may include a memory controller (not shown) through which it accesses the memory circuits," Ex. 1015 at 3:5-7, and that "[t]he system device which accesses the memory may be any type of system device, such as: desktop computer, laptop computer, workstation, server, consumer electronic device, television, personal digital assistant (PDA), mobile phone, printer or other peripheral device, etc.," *id.* at 15:13-17.

360. A Skilled Artisan would have understood from this disclosure that the "*memory module* [is] *operable in a computer system with a system memory controller.*" *See, e.g.*, Ex. 1037 (Rothman) at Fig. 1, 1:34-39 ("FB-DIMMs can be connected via high speed serial interfaces to a Memory Controller Hub (MCH). The AMB communicates with the MCH via the high speed serial interfaces and with RAM ICs on the DIMM via the internal memory bus. The AMB reads from and writes to the RAM as instructed by the MCH and can also be used to configure

the FB-DIMM."); Ex. 1022 at 315-20, Figure 7.2 (annotated below) ("Figure 7.2 illustrates [as of 2008] DRAM's place in a typical PC. An individual DRAM device typically connects indirectly to a CPU (i.e., a microprocessor) through a memory controller"), Figure 7.6 ("JEDEC style memory bus organization"). A POSITA would also know that the memory controller could be integrated into the CPU package (to the left in the figure below) rather than in a separate chip (as shown below); both were known options at the time.

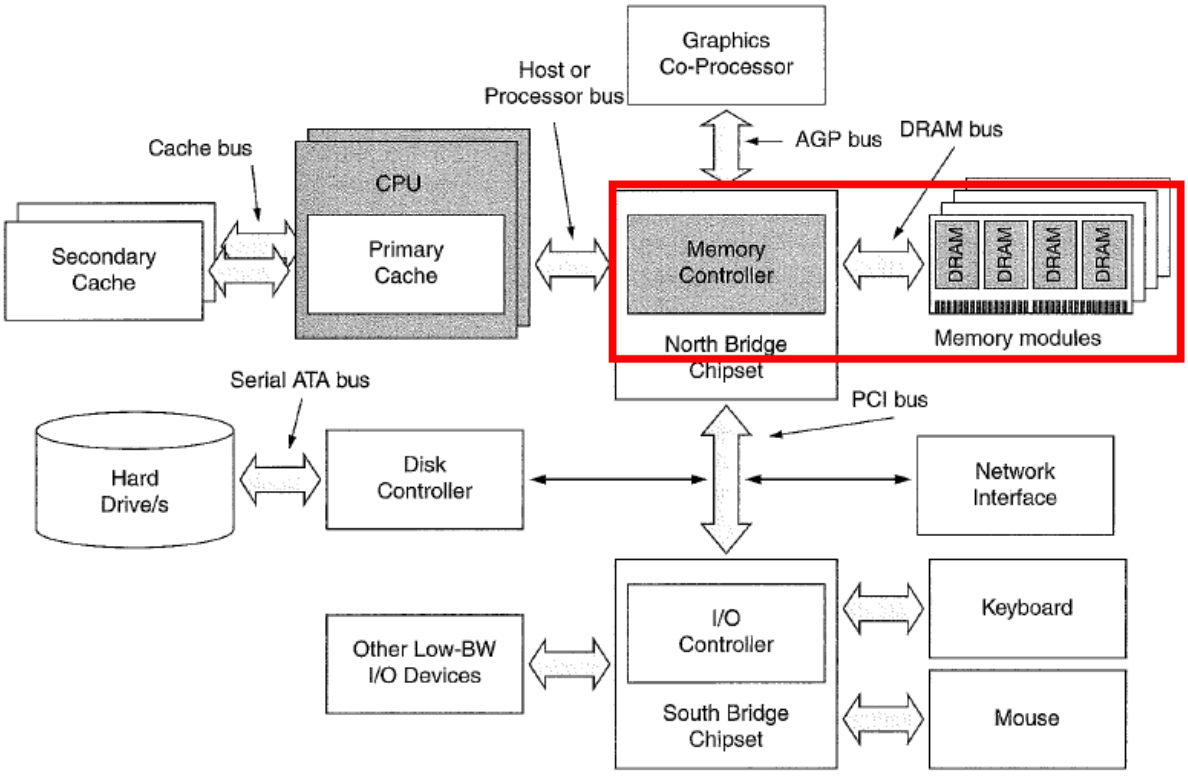


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

361. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

362. Accordingly, the prior art references in Ground 1 satisfy "*[a] memory module operable in a computer system with a system memory controller, comprising*."

b) [10.b] A Register Device

363. Claim 10 requires "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*."

364. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

365. The combination of Kim and Rajan discloses "*a register device configured to receive command/address signals from the system memory controller and to output control signals*."

366. For example, Rajan discloses a register 804 that receives command/address signals from the memory controller and outputs address and control signals to the buffered stacks. Ex. 1015 at Fig. 8 (reproduced below, showing the register receiving "Address & Control" signals per the JEDEC standard, *id.* at 4:20-24, would include command signals, *see* Ex. 1019 at 13, 33; Ex. 1023 at 9, Fig.16; Ex. 1022 at 318-20); Ex. 1015 at 8:52-58 ("FIG. 8 illustrates

a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level."); *see also* Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"), 43-44 ("Fully Buffered DIMM," "FB-DIMM," "Advanced Memory Buffer," "AMB").

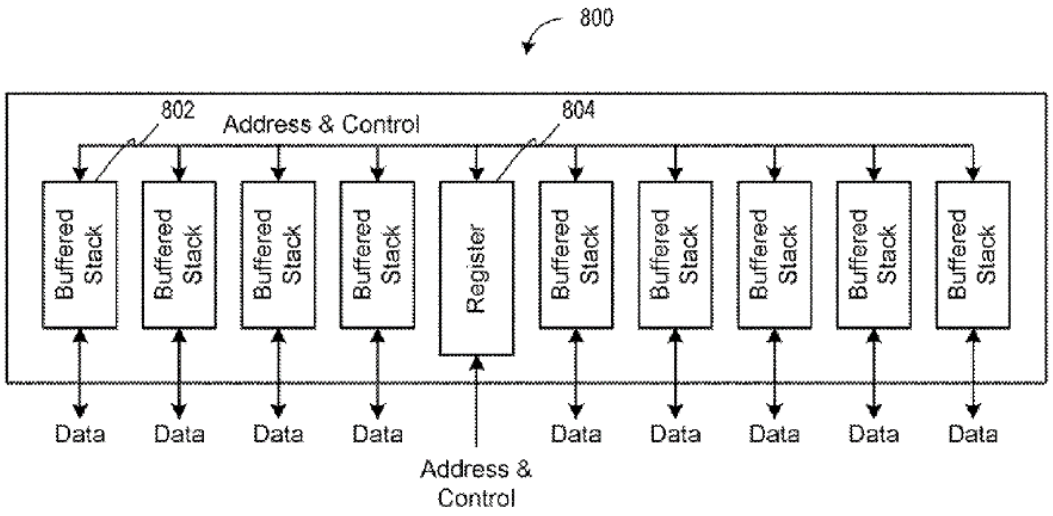


FIG. 8

Rajan also discloses that its register is generating "Address & Control" signals in response. *Id.*

367. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

368. Accordingly, the prior art references in Ground 1 satisfy the "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*" limitation.

c) [10.c] Plurality of DRAM packages

369. Claim 10 requires "*a plurality of DRAM packages, each DRAM package comprising*."

370. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

371. The combination of Kim and Rajan discloses a memory module including "*a plurality of DRAM packages*," such as buffered stacked DRAM circuits. Ex. 1015 at Fig. 8 (reproduced above), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention."); *see also supra* ¶¶174-179 (claim limitation [1.a], discussing relevant disclosure by Kim); Ex. 1022, at 315, 374 (DRAM "packages").

372. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

373. Accordingly, the prior art references in Ground 1 satisfy the "*a plurality of DRAM packages, each DRAM package comprising*" limitation.

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d) [10.d] Data Terminals

374. Claim 10 requires "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*."

375. As shown in the table below, claim limitation [10.d] is very similar to claim limitations [1.b] and [10.b]:

Claims 1, 10	**Claim 10**
[1.b] data terminals and control terminals; [10.b] a register device configured … to output control signals	[10.d] data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device;

376. As discussed above with reference to claim limitation [1.b], the prior art references in Ground 1 satisfy "*data terminals and control terminals*." *Supra* ¶¶180-196.

377. As discussed above with reference to claim limitation [10.b], Rajan discloses a register 804 that sends "Address & Control" signals to the DRAM packages. Ex. 1015 at Fig. 8 (reproduced below), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some

embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level.")

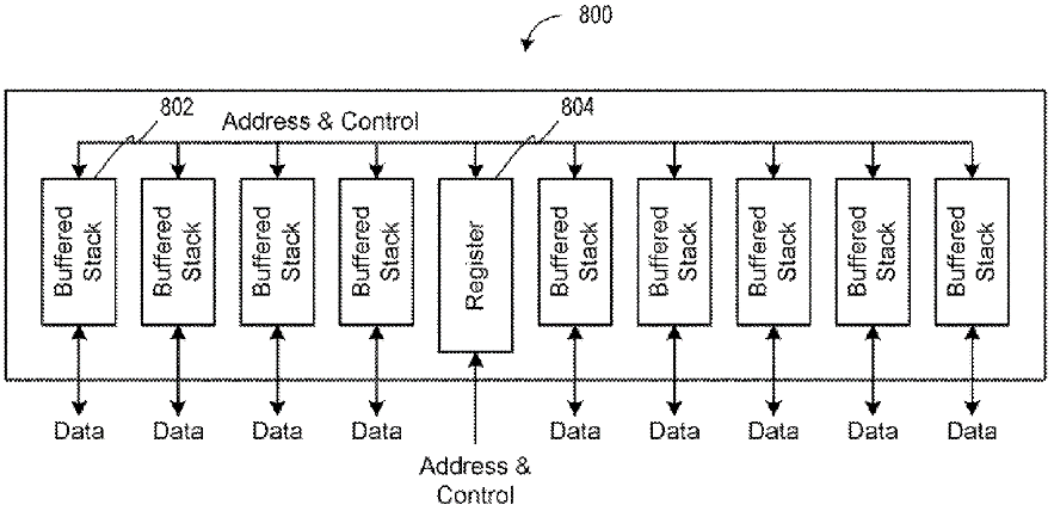


FIG. 8

As can also be seen in Fig. 8 above, Rajan discloses that each DRAM package communicates data signals with the system memory controller. Accordingly, it would have been obvious to a Skilled Artisan that the combination of Kim and Rajan includes data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device. *See also* Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"); Ex. 1019 at 6-13 (JEDEC standard for terminals for data, address, and control).

378. Therefore, Kim and Rajan disclose and render obvious this limitation to a Skilled Artisan.

379. Accordingly, the prior art references in Ground 1 satisfy the "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*" limitation.

e) [10.e] Stacked Array Dies

380. Claim 10 requires "*stacked array dies including a first group of array dies and a second group of at least one array die*."

381. As shown in the table below, claim limitation [10.e] is identical to claim limitation [1.c]:

Claim 1	**Claim 10**
[1.c] stacked array dies including a first group of array dies and a second group of at least one array die;	[10.e] stacked array dies including a first group of array dies and a second group of at least one array die;

382. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 1 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶197-214.

f) [10.f.1] and [10.f.2] First and Second Die Interconnects

383. Claim 10 requires "*die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second*

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die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies."

384. As shown in the table below, claim limitations [10.f.1] and [10.f.2] are nearly identical to claim limitations [1.d.1] and [1.d.2], respectively:

Claim 1	**Claim 10**
[1.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[10.f.1] die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [10.f.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

385. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 1 satisfy "*die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one*

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array die and not in electrical communication with the first group of array dies."

Supra ¶¶215-225.

g) [10.g] Control Die

(1) [10.g.1] A Control Die Including

386. Claim 10 requires "*a control die including*."

387. As shown in the table below, claim limitation [10.g.1] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 10**
[1.e.1] a control die comprising	[10.g.1] a control die including

388. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 1 satisfy "*a control die including*." *Supra* ¶¶226-234.

(2) [10.g.2] and [10.g.3] First and Second Data Conduits

389. Claim 10 requires "*first data conduits between the first die interconnects and data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

390. As shown in the table below, claim limitations [10.g.2] and [10.g.3] are identical to claim limitations [1.e.2] and [1.e.3], respectively:

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Claim 1	**Claim 10**
[1.e.2] first data conduits between the first die interconnects and the data terminals, and [1.e.3] second data conduits between the second die interconnects and the data terminals,	[10.g.2] first data conduits between the first die interconnects and data terminals, and [10.g.3] second data conduits between the second die interconnects and the data terminals,

391. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Ground 1 satisfy "*first data conduits between the first die interconnects and data terminals*," and "*second data conduits between the second die interconnects and the data terminals*." *Supra* ¶¶235-251.

h) [10.h.1] and [10.h.2] First and Second Drivers

392. Claim 10 requires "*the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size*," and "*the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die*."

393. As shown in the table below, claim limitations [10.h.1] and [10.h.2] is very similar to claim limitations [1.e.4] and [1.e.5]:

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Claims 1, 10	**Claim 10**
[1.e.4] the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [1.e.5] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size. [10.d] data terminals via which the DRAM package communicate data signals with the system memory controller…	[10.h.1] the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size, [10.h.2] the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die

394. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], the singular "*first data conduit*" and "*second data conduit*" lack antecedent basis, but those limitations are obvious even if they are interpreted to be plural "*first data conduit**s***" and plural "*second data conduit**s***." *See supra* ¶253. Thus, as discussed above with reference to claim limitations [1.e.4] and [1.e.5], the prior art references in Ground 1 satisfy "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data*

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conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size." *Supra* ¶¶252-262.

395. As discussed above with reference to claim limitation [10.d], the prior art references in Ground 1 satisfy "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*." *Supra* ¶¶374-379.

396. Accordingly, the prior art references in Ground 1 satisfy the "*the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size*," and "*the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die*" limitations.

11. Claim 11 is Unpatentable

397. Claim 11 is unpatentable as the prior art references in Ground 1 render the claim obvious.

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398. Claim 11 requires "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals*."

399. As shown in the table below, claim 11 is very similar to claim 5:

Claim 5	**Claim 11**
[5] The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.	[11] The memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals.

400. As discussed above with reference to claim 5, the prior art references in Ground 1 satisfy "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals*." *Supra* ¶¶298-306.

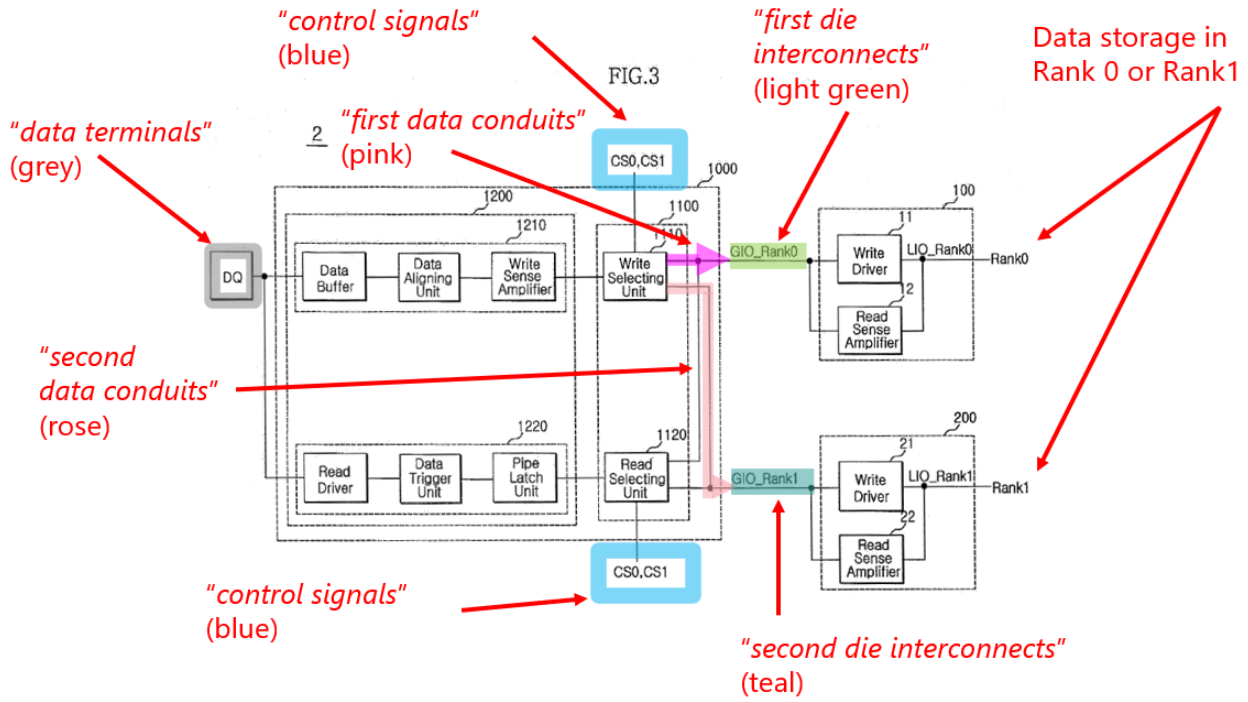
12. Claim 12 is Unpatentable

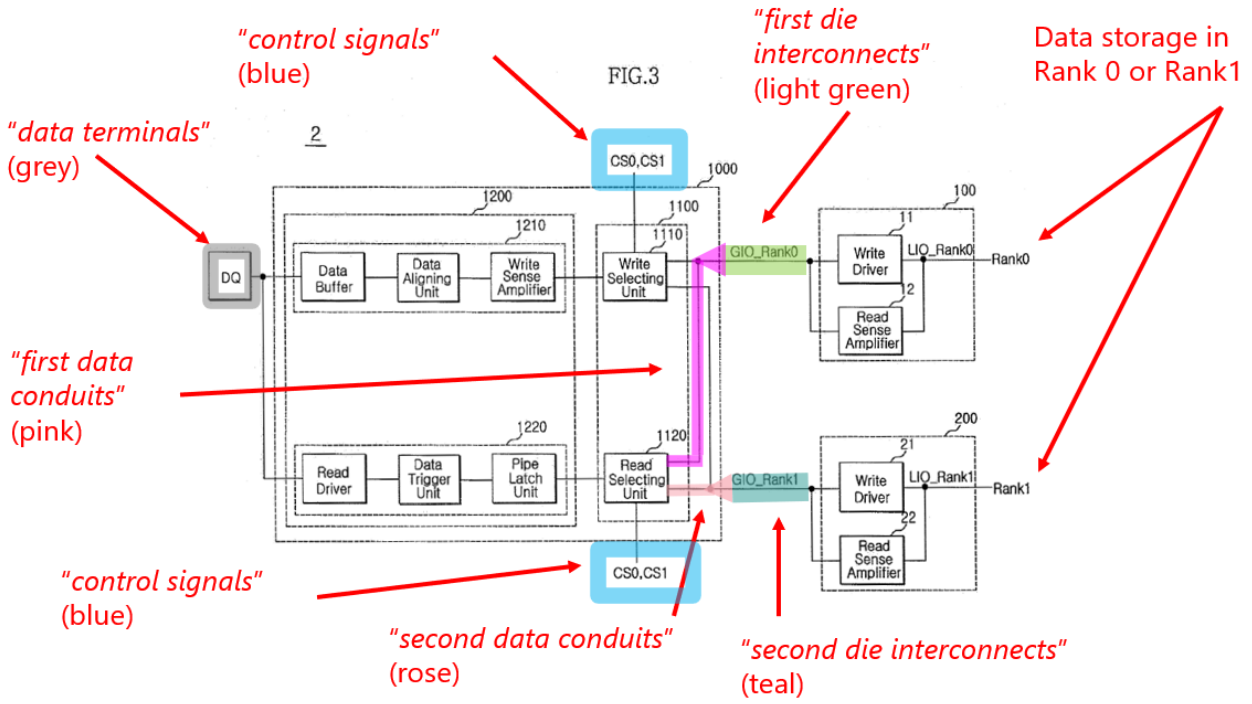
401. Claim 12 requires "*[t]he memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*."

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402. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

403. Kim in combination with Rajan discloses that "*the control signals* [from the register device] *include data path control signals generated by the register device* [such as chip select and read and write command signals as disclosed by Rajan], *the data path control signals being used to control the respective states of the first data conduits* [(annotated pink below)] *and second data conduits* [(annotated rose below)] [including controlling the direction of the data transfer for read or write and the selection of transferring the data through TSV1 or TSV2]." *See, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





404. For the reasons discussed above with reference to claim 5, Kim's rank selecting unit 1100 includes a control circuit that receives control signals, including chip selection signals and read and write command signals from an external device and, in response, controls the write and read selecting units 1110 and 1120 to direct the data transfer selectively to or from TSV1 through the "*first data conduits*" (pink) or to or from TSV2 through the "*second data conduits*" (rose). *Supra* ¶¶298-306. A Skilled Artisan would have understood that the chip selection signals and read and write command signals are "*data path control signals*" because they determine the direction of the data transfer (read or write) and also select the TSV (TSV1 or TSV2) through which data is transmitted from or to Rank0 or Rank 1, respectively. *See, e.g.*, Ex. 1001 (the 160 Patent) at 19:17-21

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("The data path control circuit (e.g., ODT, read/write data direction)…."). A Skilled Artisan would have understood that such a selection of TSV1 or TSV2 happens, for example, to avoid collisions. Ex. 1014 (Kim) at [0031] ("Accordingly, even though the first and second ranks Rank0 and Rank1 may comprise one data input/output circuit, the semiconductor memory apparatus 2 may allow a read operation and a write operation to be selectively performed for one of the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, whereby it is possible to prevent a data collision from occurring.").

405. Furthermore, in the combination of Kim and Rajan, the memory module can implement rank multiplication. *Supra* at ¶¶137-140, 146-164. For example, the register of the module can generate additional chip select signals and provide those to the stacked memory package. *Id*. Alternatively or in addition, the "*control circuit*" in the memory package may also implement rank multiplication. *Supra* at ¶140.

406. Therefore, Kim in view of Rajan discloses this limitation to a Skilled Artisan.

407. Accordingly, the prior art references in Ground 1 satisfy the "*memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to*

control the respective states of the first data conduits and the second data conduits" limitation.

13. Claim 13 is Unpatentable

408. Claim 13 is unpatentable as the prior art references in Ground 1 render the claim obvious.

409. Claim 13 requires "*[t]he memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*."

410. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

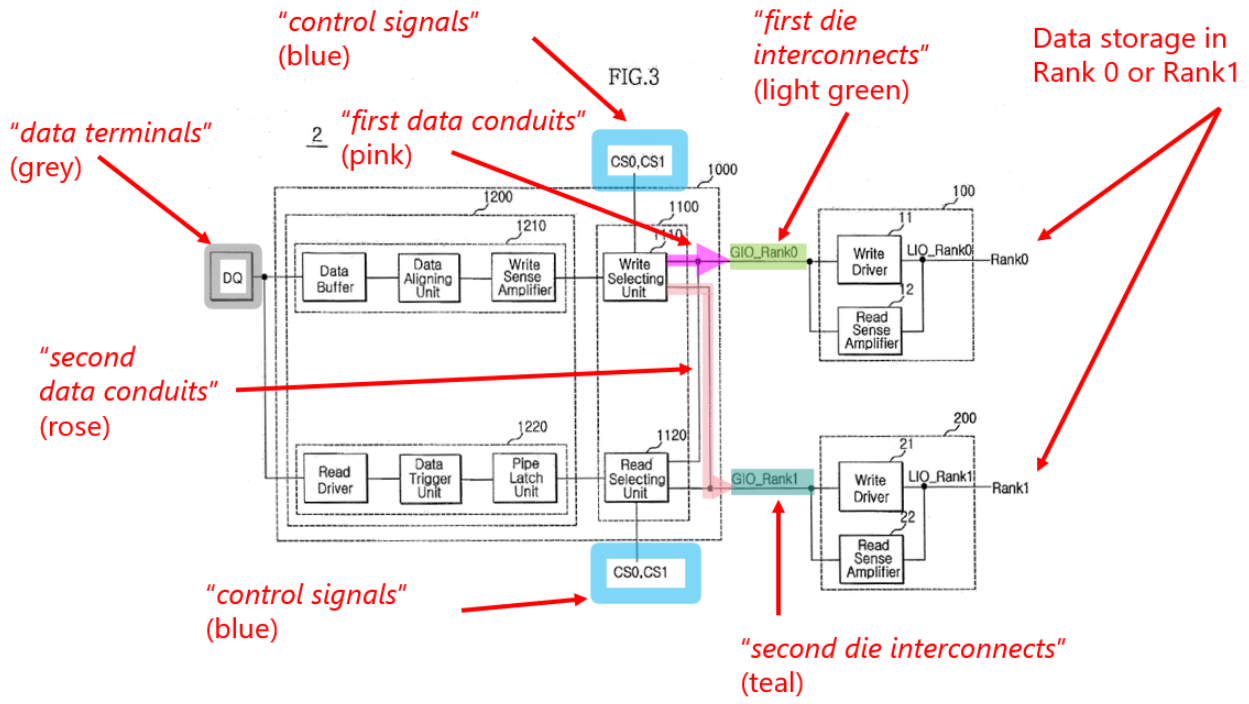
411. Kim discloses that "*the control die* [including rank selecting unit 1100] *is configured to generate data path control signals* [including internal write and read signals] *from at least some of the control signals* [including chip selection and read and write command signals from an external device]*, the data path control signals being used to control the respective states of the first data conduits and the second data conduits* [to or from TSV1 or TSV2]."

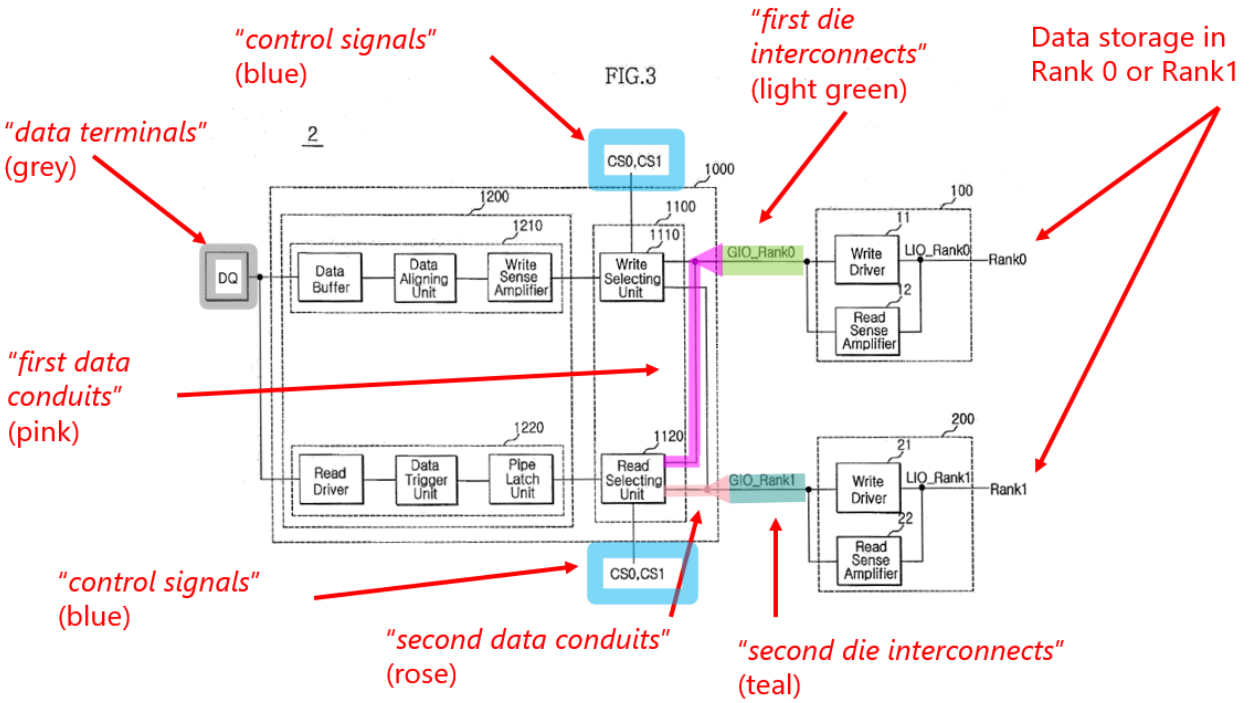
412. For example, Kim discloses that, "[w]hile not shown in a drawing, the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals. The internal write and read signals

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["*generate[d] data path control signals*"] may be signals that are generated because write and read command signals applied from a device external to the semiconductor memory apparatus 2 ["*received control signals*"] are buffered." Ex. 1014 at [0038].

413. A Skilled Artisan would have understood, that the internal write and read signals are "*data path control signals being used to control the respective states of the first data conduits and the second data conduits*" because they (1) determine the direction of data transfer through the data conduits, (2) select whether the data is passing through the read selecting unit 1120 or through the write selecting unit 1110 and (3) also select the corresponding data conduit section TSV1 or TSV2 through which the data is transferred. S*ee, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





414. Furthermore, the combination of Kim and Rajan renders obvious to a Skilled Artisan to generate the chip selection and other control signals and the corresponding read and write commands and their respective timing according to

the characteristics of the physical memory dies, while the memory package emulates one or more memory devices with different characteristics. *Supra* at ¶¶146-164; *see, e.g.*, Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). For example, the interface circuit can generate additional chip select signals for rank multiplication. *Supra* at ¶¶137-140; *see, e.g.*, Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

415. Therefore, Kim discloses and in view of Rajan renders obvious this limitation.

416. Accordingly, the prior art references in Ground 1 satisfy the "*memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*" limitation.

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14. Claim 14 is Unpatentable

417. Claim 14 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [14.a] Control Signals Include Address Signals

418. Claim 14 requires "*[t]he memory module of claim 10, wherein the control signals include address signals*."

419. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

420. Kim discloses and renders obvious, at least in view of Rajan, to a Skilled Artisan that "*the control signals include address signals*," such as those included in the "write and read command signals applied from a device external to the semiconductor memory apparatus." Ex. 1014 at [0038]; *supra* at ¶¶146-164. As discussed above with reference to claim limitation [1.b], and in light of the JEDEC standards, a Skilled Artisan would have understood and been obvious to her from the disclosure of Kim alone and in combination with Rajan that "write and read command signals" include chip-select signals and address signals identifying where to store or retrieve the data. *Supra* ¶¶180-196; Ex. 1019 (JESD79-3C) at pp.6-14 (describing package pinout for stacked DDR3 memories, including chip select terminals CSn#, command signal terminals RAS#, CAS# WE#, and address signal terminals A0-A15), p.18 (describing read and write

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operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read and Write commands with corresponding column address, CA); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Rajan also discloses the control signals include address signals, e.g., as required by the JEDEC standards. *Supra* ¶¶180-196; *see, e.g.*, Ex. 1015 (Rajan) at Figs. 4 (reproduced below, annotated) and 18 (reproduced further below).

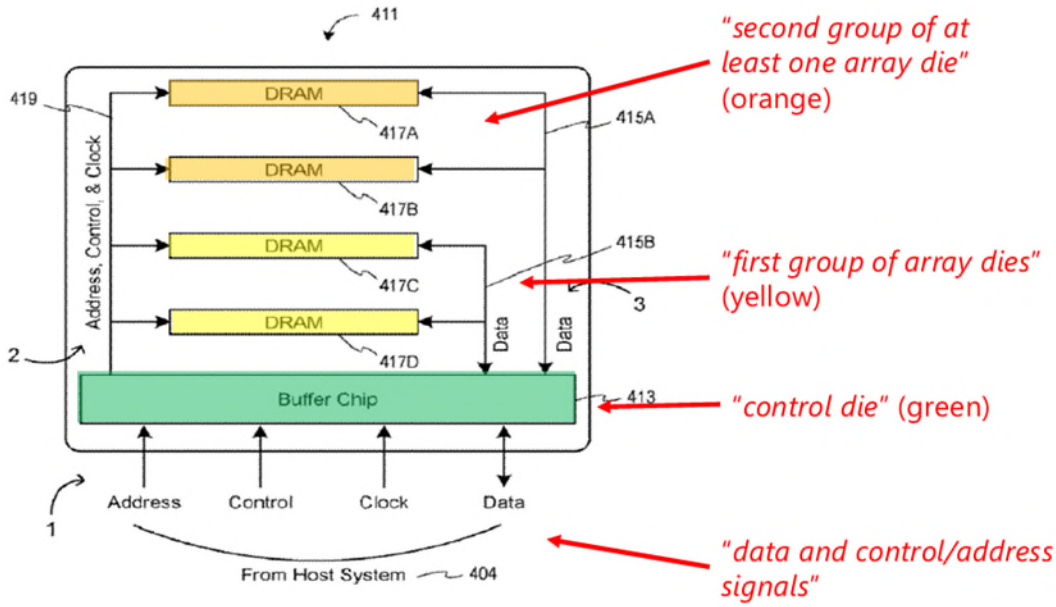


FIG. 4

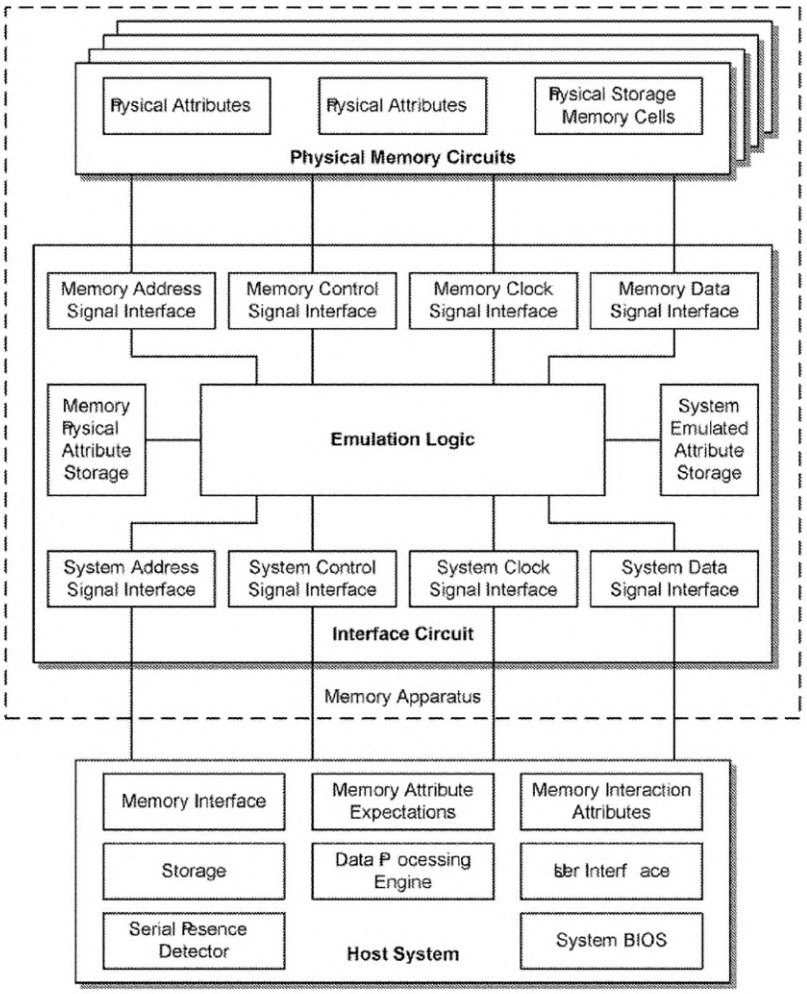


FIG. 18

421. Therefore, Kim alone and in combination with Rajan discloses this limitation to a Skilled Artisan.

422. Accordingly, the prior art references in Ground 1 satisfy "*wherein the control signals include address signals*."

b) [14.b] Control Die Provides the Address Signals

423. Claim 14 requires "*the control die provides the address signals to the plurality of array dies*."

424. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

425. As discussed immediately above, a Skilled Artisan would have understood that Kim's disclosure of "write and read command signals applied from a device external to the semiconductor memory apparatus" includes address signals, e.g., according to the JEDEC standards as taught by Rajan. Ex. 1014 at [0038]; *supra* at ¶420.

426. Kim discloses and renders obvious to a Skilled Artisan that "*the control die* [main chip C0] *provides the address signals* [for the read and write commands] *to the plurality of array dies.*"

427. For example, Kim discloses that, "if command signals are applied from an external device, the command signals are buffered by a buffer which is provided in the semiconductor memory apparatus." Ex. 1014 at [0032]. Kim also discloses that the "write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered." Ex. 1014 at [0038]. Kim explains that the stacked array dies can perform the corresponding write and read operations. *See id*. at [0029-30] ("Therefore, the read operation of the first rank Rank0 may be performed. … Therefore, the read operation of the second rank Rank1 may be performed…. Therefore, the write operation of the first rank Rank0

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may be performed. … Therefore, the write operation of the second rank Rank1 may be performed.").

428. A Skilled Artisan would have understood and it would have been obvious to her from this disclosure that Kim's main chip C0 buffers write and read command signals and the corresponding address signals, and that main chip C0 then provides those buffered signals to the stacked array dies enabling those dies to perform the corresponding read and write operations.

429. To the extent one might argue that Kim does not sufficiently disclose providing address signals to the stacked memories, it would have been obvious to a Skilled Artisan in view Rajan. Rajan discloses stacked memory chips with a buffer chip providing buffered address and control signals to each memory chip. *See* Ex. 1015 at Figs. 4 (reproduced below, annotated), 18 (reproduced below, annotated), 14:11-18 ("The interface circuit may be included in the buffer chip, for example. The interface circuit includes a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system, and a system data signal interface for sending/receiving data signals to/from the host system.").

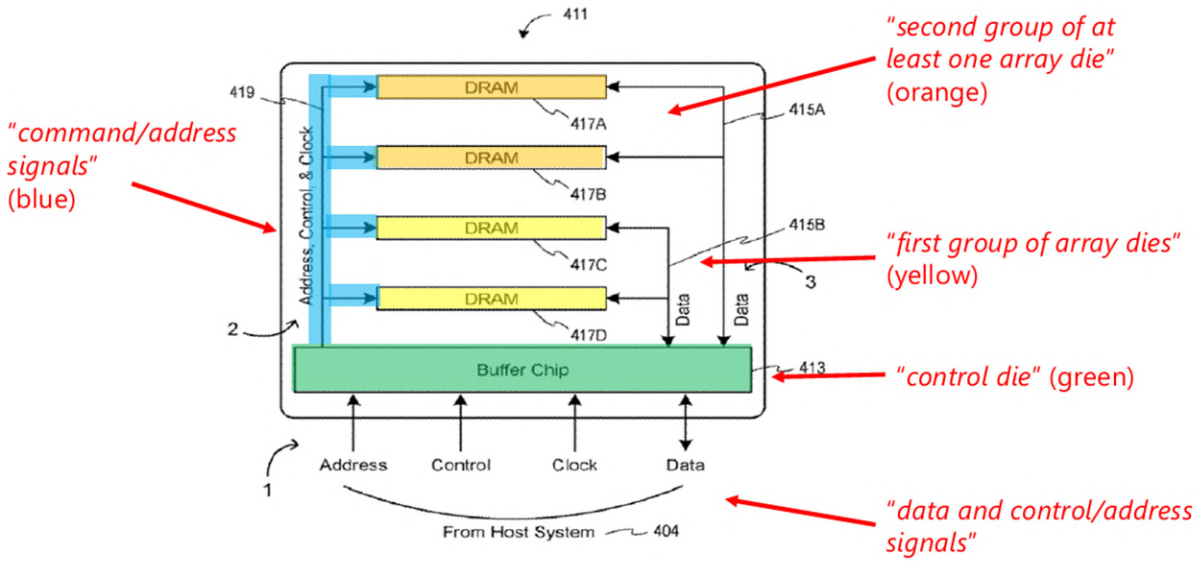


FIG. 4

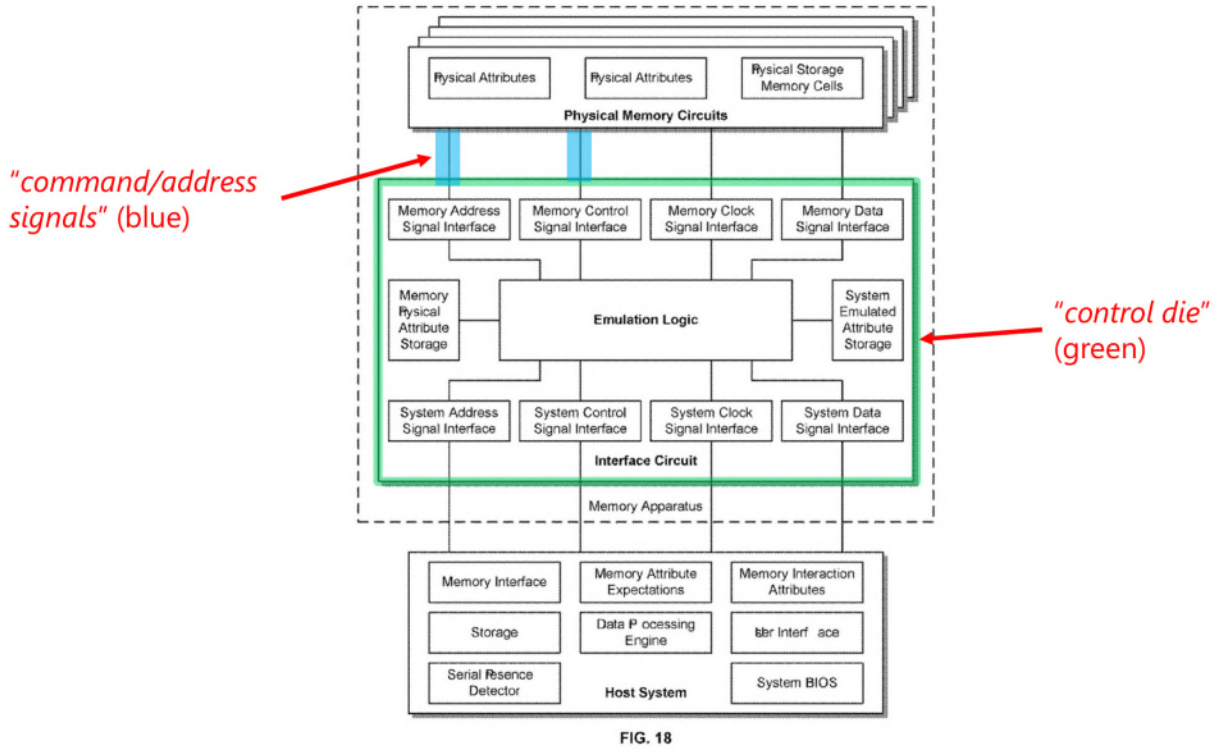
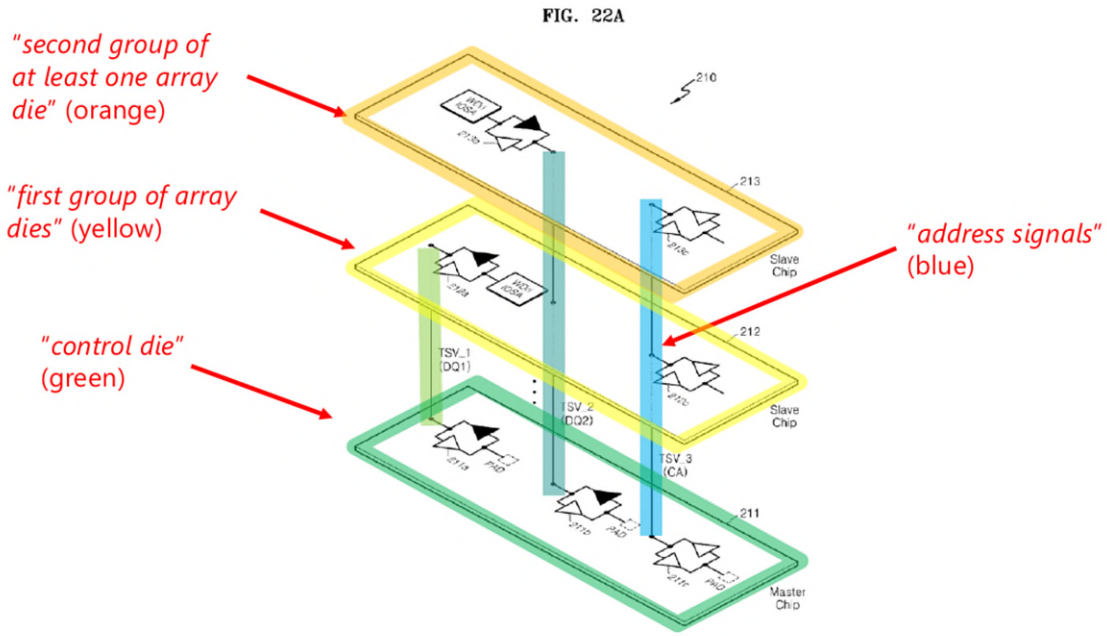


FIG. 18

Rajan also discloses that some of the address signals may be passed through to the physical memory devices "unaltered." Ex. 1015 (Rajan) at 14:55-60 ("The emulation logic may, in various embodiments, alter a timing, value, latency, etc. of

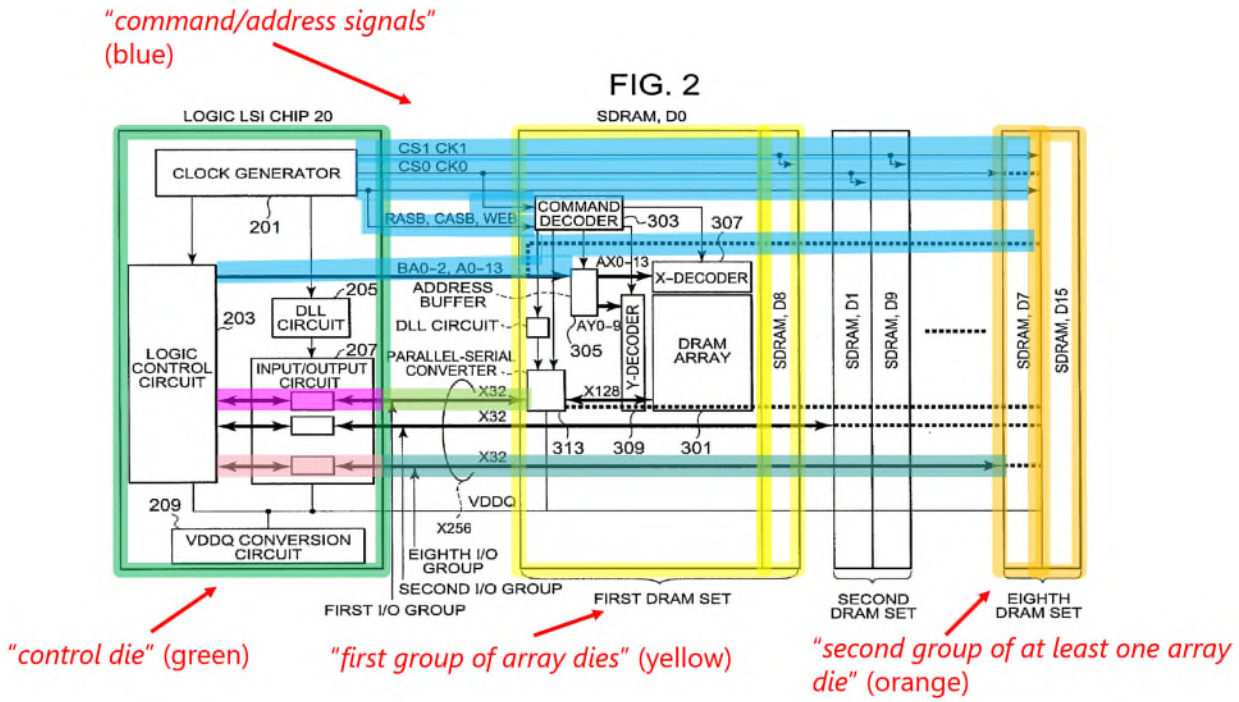
any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory. Some such signals may pass through unaltered, while others may be altered.").

430. A Skilled Artisan would have been motivated to provide the command/address signals to the memory chips in the stack, because such command and address signals were used by memory devices at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.13 (describing address and control signals for SDRAM devices, including chip-select signals). Providing the address and control signals to each memory chip in the stack was well within the level of skill and required nothing more than what was expected at the time: having the address and control signals available at each memory chip. *See, e.g.*, Ex. 1034 (Lee) at 21:49-52, Fig. 22A (reproduced below, annotated).



431. The prior art described in the 160 Patent, specifically Figs. 1A and 1B, demonstrate that providing address and control signals to each memory chip in the stack was well within the level of skill. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for address and command signals from the control chip), 1:41-44 ("Further, the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142."), 2:7-9 ("Further, the memory package 150 includes a driver 186 for driving command and/or address signals to each of the array dies 160 via another die interconnect 188.").

432. Riho further demonstrates that providing address and control signals to each memory chip in the stack was well within the level of skill. Riho discloses stacked memory chips with a control chip (20) providing address and control signals to each memory chip in the stack. Ex. 1016 at Fig. 2 (reproduced below, showing command decoder and address buffer in memory chip receiving corresponding command and address signals from the control chip 20), [0043] ("The 3-bit bank address signal BA0-2 and the 14-bit address signal A0-13 are supplied to all the SDRAMs D0 to D15 through the address TSVs."), and [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs.").



433. Therefore, Kim discloses and renders obvious this limitation in view of Rajan to a Skilled Artisan.

434. Accordingly, the prior art references in Ground 1 satisfy "*the control die provides the address signals to the plurality of array dies*."

15. Claim 15 is Unpatentable

435. Claim 15 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [15.a] Input Command/Address Signals Include First Chip Select Signals

436. Claim 15 requires "*[t]he memory module of claim 10, wherein the input command/address signals include first chip select signals*."

437. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

438. The combination of Kim and Rajan discloses that "*the input command/address signals include first chip select signals.*"

439. For the reasons discussed above, it would have been obvious to use Kim's memory devices in the memory module of Rajan, which includes "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*." *Supra* ¶¶363-368; *see also supra* ¶¶146-164.

440. Furthermore, Kim discloses that "chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2." Ex. 1014 at [0032]. Kim also discloses "write and read command signals applied from a device external to the semiconductor memory apparatus." *Id.* at [0038]. A Skilled Artisan would have understood that write and read command signals include chip select signals according to the JEDEC standards. Ex. 1019 (JESD79-3C) at p.13 ("Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code."). Indeed, Rajan also discloses using the JEDEC protocol. Ex. 1015 at 8:6-13 ("In various embodiments, it may be desirable to determine whether

the simulated DRAM circuit behaves according to a desired DRAM standard or other design specification. Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals that a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals.").

441. Therefore, Kim in combination with Rajan discloses this limitation to a Skilled Artisan.

442. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the input command/address signals include first chip select signals*" limitation.

b) [15.b] Register Device Configured to Perform Rank Multiplication

443. Claim 15 requires "*wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*."

444. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

445. The combination of Kim and Rajan discloses that "*the register device is configured to perform rank multiplication by generating second chip select*

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signals, from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies."

446. For example, as discussed above with reference to claim limitation [1.c], Rajan discloses emulating characteristics, including rank multiplication, which involves "*generating second chip select signals, from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals*." *Supra* ¶¶137-139, 197-214; *see, e.g.*, Ex. 1015 at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 6:30-7:67 (disclosing specific examples of rank multiplication). Rajan also explains that, in one implementation, "the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals." Ex. 1015 at 7:12-16. Rajan further discloses that "the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level." *Id.* at 8:56-58.

447. Rajan also discloses that the generated chip select signals are "*equal to a number of array dies in the plurality of array dies*." *Id*. at 6:34-38 ("In this instance, the extra address bits may be decoded by the buffer chip to individually

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select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

448. A Skilled Artisan would have understood from this disclosure that the register, such as an AMB, can "*perform rank multiplication by generating chip select signals*" for additional ranks from the input address signals. *Supra* at ¶¶137-140, *see also* Ex. 1001 (160 patent) at 18:33-39 ("The 3DS register 712 [in Figure 7] may include a DDR3 JEDEC standard register with a 'rank multiplication' circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller."), 22:19-25 (describing that rank multiplication was prior art: "Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537"); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537).

449. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

450. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals*

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greater than the first chip select signals and equal to a number of array dies in the plurality of array dies" limitation.

c) [15.c] Chip Select Die Interconnects

451. Claim 15 requires "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

452. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

453. Kim also discloses to a Skilled Artisan that "*the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies,"* such as "*die interconnects*" between the main chip C0 and the slave chips C1 and C2 which couple the buffered chip select signals CS0 and CS1 from the main chip C0 to slave chips C1 and C2, respectively, in order to perform read and write operations.

454. For example, Kim explains that "[d]uring the read operation, when the first rank Rank0 is selected by the chip selection signals CS0 and CS1, that is, when a first chip selection signal CS0 is enabled, … the read operation of the first rank Rank0 may be performed. Also, during the read operation, when the second rank Rank1 is selected by the chip selection signals CS0 and CS1, that is, when a second chip selection signal CS1 is enabled, … the read operation of the second

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rank Rank1 may be performed." Ex. 1014 at [0029]. Similarly, Kim explains that "[d]uring the write operation, when the first chip selection signal CS0 is enabled, … the write operation of the first rank Rank0 may be performed. Also, during the write operation, when the second chip selection signal CS1 is enabled, … the write operation of the second rank Rank1 may be performed." *Id*. at [0030]. Kim further explains that "the first chip selection signal CS0 becomes a signal for selecting the first slave chip C1, and the second chip selection signal CS1 becomes a signal for selecting the second slave chip C2." *Id*. at [0049].

455. A Skilled Artisan would have understood from this disclosure that the chip selection signal CS0, which is buffered on the main chip C0, is transmitted to slave chip C1 through a respective die interconnect to enable read and write operations from the first rank Rank0. Similarly, the chip selection signal CS1, which is buffered on the main chip C0, is transmitted to slave chip C2 through a respective die interconnect to enable read and write operations from the second rank Rank1.

456. To the extent one might argue that Kim does not sufficiently disclose die interconnects for the chip select signals, it would have been obvious to a Skilled Artisan in view of Rajan. For example, Rajan discloses that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the

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stack." *Supra* at ¶¶146-164; *see, e.g.*, Ex. 1015 (Rajan) at 6:34-38 and Fig. 4 (reproduced below, annotated).

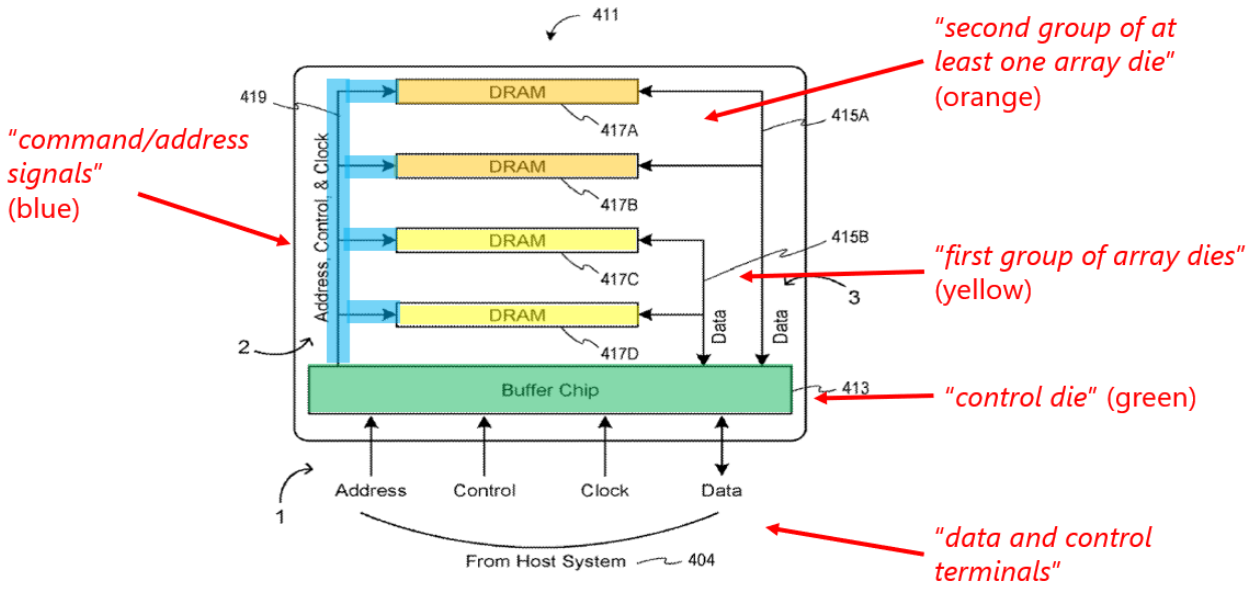


FIG. 4

457. Using separate chip select signals for selecting a chip in the stack, as described by Rajan, was well known at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Figs. 1-3 showing stacked DDR3 chips, each receiving a separate chip select signal), p.13 (explaining that chip select "provides for external Rank selection on systems with multiple Ranks"), Fig. 2 (reproduced below, annotated to indicate chip select signals); *see also* Ex. 1022 at 319 (the "chip-select bus … is essential in a JEDEC style memory system"); Ex. 1023 at 2-4, 9, Fig.16.

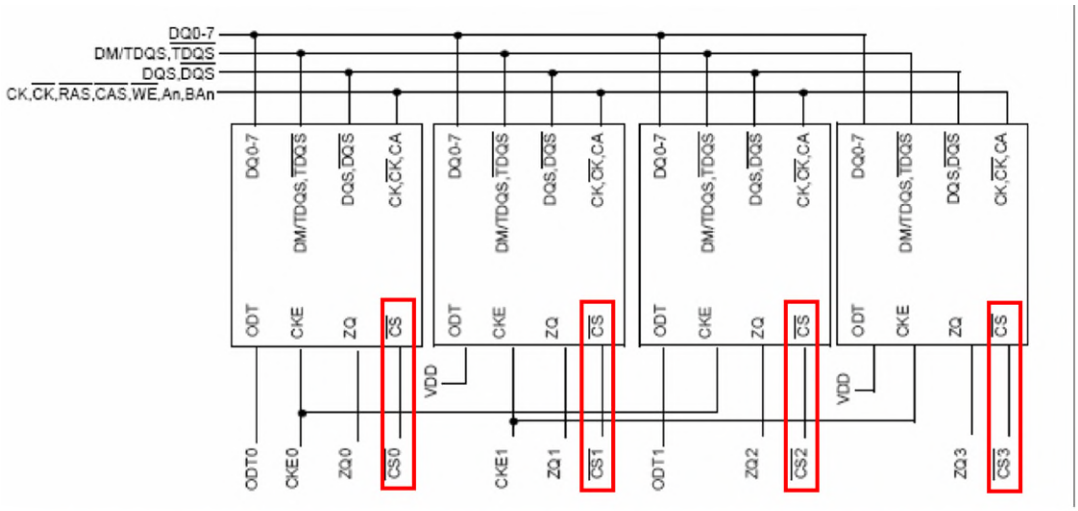


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

458. The prior art described in the 160 Patent, specifically Figs. 1A and 1B, demonstrate that transmitting separate chip select signals through die interconnects to select a chip in the stack was also well known at the time. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for chip select signals), 1:51-58 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.").

459. US 2011/0026293 to Riho ("Riho") further demonstrates that using interconnects for the chip select signals was well within the level of skill. *See, e.g.*, Ex. 1016 at [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are

supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs.").

460. Therefore, Kim discloses and renders obvious in view of Rajan this limitation to a Skilled Artisan.

461. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

16. Claim 16 is Unpatentable

462. Claim 16 is unpatentable as the prior art references in Ground 1 render the claim obvious.

a) [16.a] Control Signals Include Output Command/Address Signals Derived from the Input Command/Address Signals

463. Claim 16 requires "*[t]he memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals*."

464. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

465. As shown in the table below, claim limitation [16.a] is very similar to claim limitation [15.a]:

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Claim 15	**Claim 16**
[15.a] wherein the input command/address signals include first chip select signals	[16.a] The memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals,

466. For the reasons discussed above with reference to claim limitation [15.a], the prior art references in Ground 1 satisfy "*wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals.*" *Supra* ¶¶436-442.

467. For example, registered DIMMs with registers that derived output command/address signals from the input command/address signals were well known, including chip select signals according to the JEDEC standards. *See, e.g.,* Ex. 1015 (Rajan) at Fig. 8 (reproduced below).

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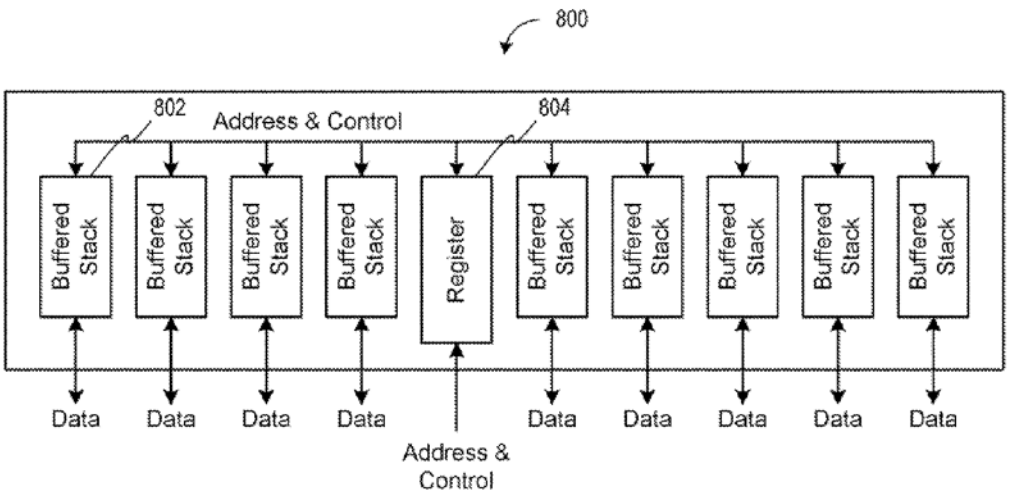


FIG. 8

468. Therefore, the combination of Kim and Rajan discloses and renders obvious this limitation to a Skilled Artisan.

469. Accordingly, the prior art references in Ground 1 satisfy the "*wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals*" limitation.

b) [16.b] Control Die is Configured to Perform Rank Multiplication

470. Claim 16 requires "*wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*."

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471. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

472. As shown in the table below, claim limitation [16.b] is very similar to claim limitation [15.b], with the exception that claim limitation [16.b] requires the control die (as opposed to the register device) to perform the rank multiplication:

Claim 15	**Claim 16**
[15.b] wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and	[16.b] wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and

473. As previously discussed, a Skilled Artisan would have understood that, either alternatively or in addition to the register of the module, the control circuit in the "*control die*" of the memory package may also implement rank multiplication. *Supra* ¶¶140, 405. Thus, for the reasons discussed above with reference to claim limitation [15.b], the prior art references in Ground 1 satisfy "*wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip*

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select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies." *Supra* ¶¶443-450. For example, a Skilled Artisan would have understood that the number of the chip select signals is equal to the number of the array dies in the stack. *Supra* at ¶447. Thus, when the output command/address signals from the register have less chip selects than the number of array dies in the stack, the additional chip select signals are generated by the control die. *Id*.

c) [16.c] Chip Select Die Interconnects

474. Claim 16 requires "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

475. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

476. As shown in the table below, claim limitation [16.c] is identical to claim limitation [15.c]:

Claim 15	**Claim 16**
[15.c] wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.	[16.c] wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.

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477. As discussed above with reference to claim limitation [15.c], the prior art references in Ground 1 satisfy "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*." *Supra* ¶¶451-461.

17. Claim 17 is Unpatentable

478. Claim 17 is unpatentable as the prior art references in Ground 1 render the claim obvious.

479. Claim 17 requires "*[t]he memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver*."

480. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

481. As shown in the table below, claim 17 is nearly identical to claim 4:

Claim 4	**Claim 17**
[4] The memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.	[17] The memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver.

482. As discussed above with reference to claim 4, the prior art references in Ground 1 satisfy "*wherein the first driver size and the second driver size are*

related to a first load on the first driver and a second load on the second driver." *Supra* ¶¶291-297.

18. Claim 18 is Unpatentable

483. Claim 18 is unpatentable as the prior art references in Ground 1 render the claim obvious.

484. Claim 18 requires "*[t]he memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.*"

485. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

486. The combination of Kim and Rajan discloses that "*the control signals include command/address signals, and the control die includes buffers to control timing of the command/address signals.*"

487. As discussed above for claim limitation [10.b], the combination of Kim and Rajan discloses "*the control signals include command/address signals*." *Supra* ¶¶363-368 (claim limitation [10.b]). Furthermore, Rajan discloses that the control chip receives command/address signals for a write command and holds those signals for an additional time to control timing of when the DRAMs receive those signals. Ex. 1015 at Fig. 11 (reproduced below), 10:12-19 ("The memory controller issues the write operation at t0. In FIG. 10, the write operation appeared

at the DRAM circuits one clock later at t1, due to the inherent delay through the buffer chip. But in FIG. 11, in addition to the inherent one clock delay, the buffer chip has added an extra two clocks of delay to the write operation, which is not issued to the DRAM chips until t0+1+2=t3.").

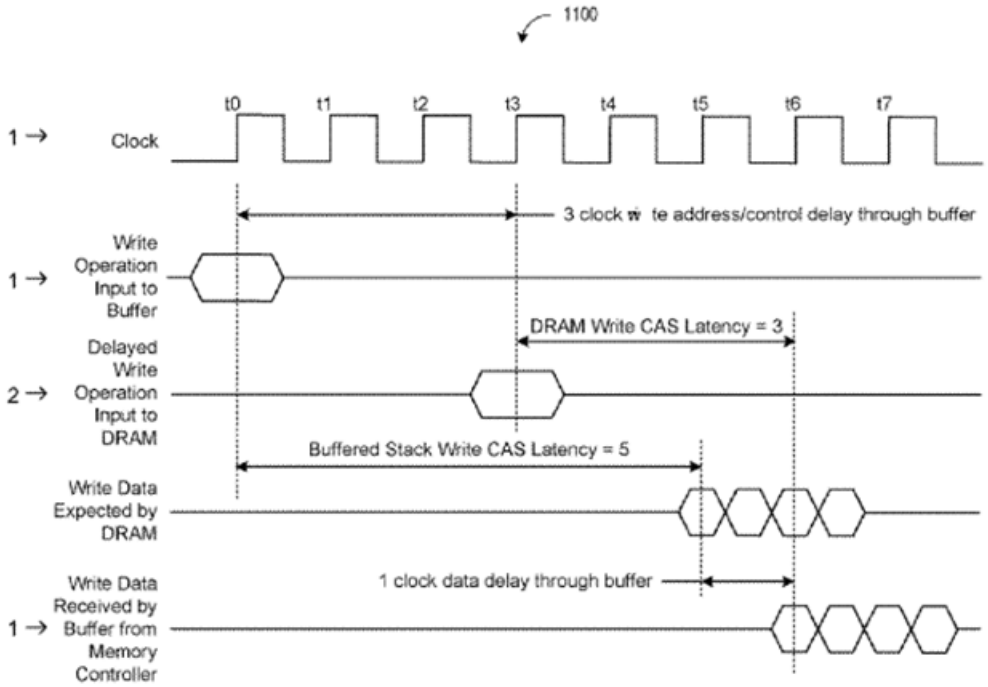


FIG. 11

488. A Skilled Artisan would have been motivated to implement this delay of command/address signals to emulate certain characteristics of JEDEC-standard memory devices as taught by Rajan. *See, e.g.*, Ex. 1015 (Rajan) at 9:61-10:4 ("In the specific example shown, the memory controller issues the write operation at t0. After a one clock cycle delay through the buffer chip, the write operation is issued to the DRAM chips at t1. Because the memory controller believes it is connected to memory having a read CAS latency of six clocks and thus a write CAS latency

of five clocks, it issues the write data at time t0+5=t5. But because the physical DRAM chips have a read CAS latency of four clocks and thus a write CAS latency of three clocks, they expect to receive the write data at time t1+3=t4. Hence the problem, which the buffer chip may alleviate by delaying write operations."); *see also* Ex. 1019, at 23-24 ("CAS latency").

489. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

490. Accordingly, the prior art references in Ground 1 satisfy "*wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals*."

19. Claim 19 is Unpatentable

491. Claim 19 is unpatentable as the prior art references in Ground 1 render the claim obvious.

492. Claim 19 requires "*[t]he memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals*."

493. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

494. As shown in the table below, claim 19 is very similar to claim 18:

Claim 18	**Claim 19**
[18] The memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.	[19] The memory module of claim 10, wherein the control die includes data buffers to control timing of the data signals.

495. For the same reasons discussed above with reference to claim 18, the prior art references in Ground 1 satisfy "*wherein the control die includes data buffers to control the timing of the data signals*." *Supra* ¶¶483-490. For example, Figure 9 of Rajan shows that emulating a CAS latency includes the control die buffering the data to and from the DRAMs and outputting it with a delay in order to control the timing of the data signals. Ex. 1015 at 8:59-9:45, Fig. 9 (reproduced below). I note that a Skilled Artisan would have understood that Fig. 9 has a small typographical error showing the CAS latency 908 ending at t5, instead of t6 as described in the specification. *Id*. at 9:25-31 ("In the example shown, the DRAM chips have a native CAS latency 906 of four clocks (from t1 to t5), and the total latency through the buffer chip is two clocks (one clock delay 902 from t0 to t1 for address and control signals, plus one clock delay 904 from t5 to t6 for data signals), and the buffer chip emulates a DRAM having a six clock CAS latency 908.").

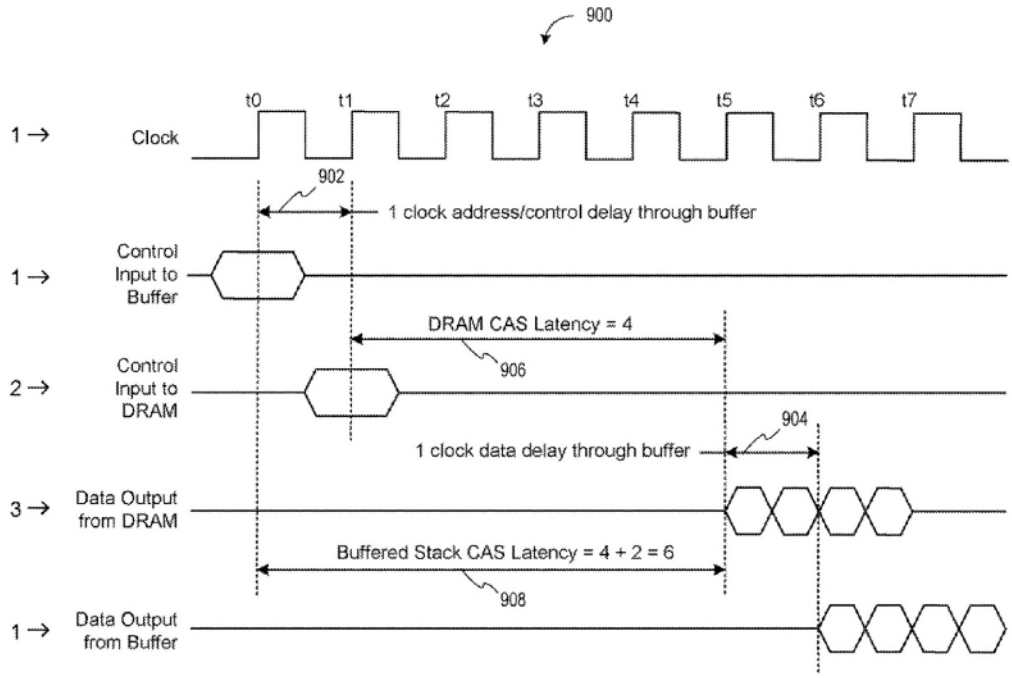


FIG. 9

496. Accordingly, the prior art references in Ground 1 satisfy "*wherein the control die includes data buffers to control the timing of the data signals*."

20. Claim 20 is Unpatentable

497. Claim 20 is unpatentable as the prior art references in Ground 1 render the claim obvious.

498. Claim 20 requires "*[t]he memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*."

499. The prior art references in Ground 1 teach this limitation to a Skilled Artisan.

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500. As shown in the table below, claim 20 is very similar to claim limitation [3.b]:

Claim 3	**Claim 20**
[3.b] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.	[20] The memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die.

501. As discussed above with reference to claim limitation [3.b], the prior art references in Ground 1 satisfy the "*wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*" limitation. *Supra* ¶¶279-285.

C. Reasons to Combine for Ground 2

502. A Skilled Artisan would have been motivated to make the combinations in Ground 2 for at least the following reasons.

1. Ground 2: Riho in view of Rajan and Riho2

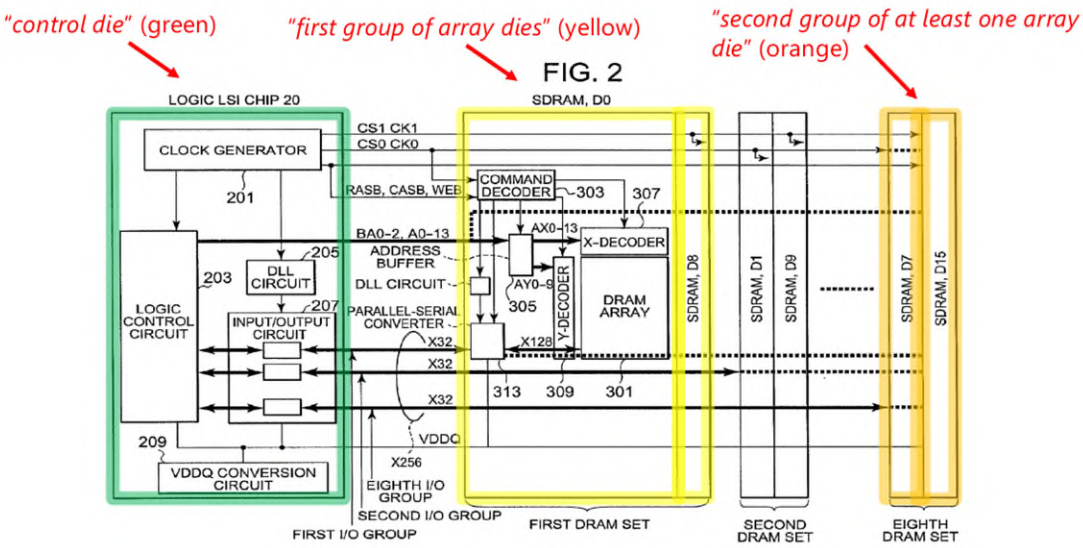
503. As mentioned above, Ground 2 involves Riho in view of Rajan and Riho2. *Supra* ¶143.

504. An overview of Riho and of Rajan is provided above. *See supra* ¶¶118-124.

505. Riho is similar to the 160 Patent. For example, the 160 Patent describes the claimed "*data terminals and control terminals*" by mentioning such

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terminals in passing without details and without illustrating them in the figures. Ex. 1001 at 5:10-14 ("Further, the memory package 200 may include input/output terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).") Riho, in a similar manner, discloses that, "[i]n the figure, external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20. I/O signal lines penetrating through the controlled chips, which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the external terminals." Ex. 1016 (Riho) at [0026]. In addition, Riho discloses that the logic LSI chip 20 communicates data signals (DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals), address signals (BA0-BA2 and A0-A13), and control signals (RASB, CASB, WEB, CS0CK0, CS1CK1,…) to the SDRAMs in the stack. *Id*. at [0030], Fig. 2 (reproduced below, annotated).



506. It would have been obvious at least in view of Rajan and/or via knowledge of the JEDEC standards to a Skilled Artisan from this disclosure that Riho's control chip 20 can have "*data terminals and control terminals*" at its lower side via which the memory package communicates data and control/address signals with one or more external devices and uses the received control/address signals to control the SDRAM chips in the stack. Such an arrangement of input/output terminals was well known at the time for stacked memory packages as explained, e.g., by Rajan. Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, showing that, in a stacked arrangement of DRAM devices, a buffer chip receives data and control/address signals from an external host system and controls the DRAM devices in the stack).

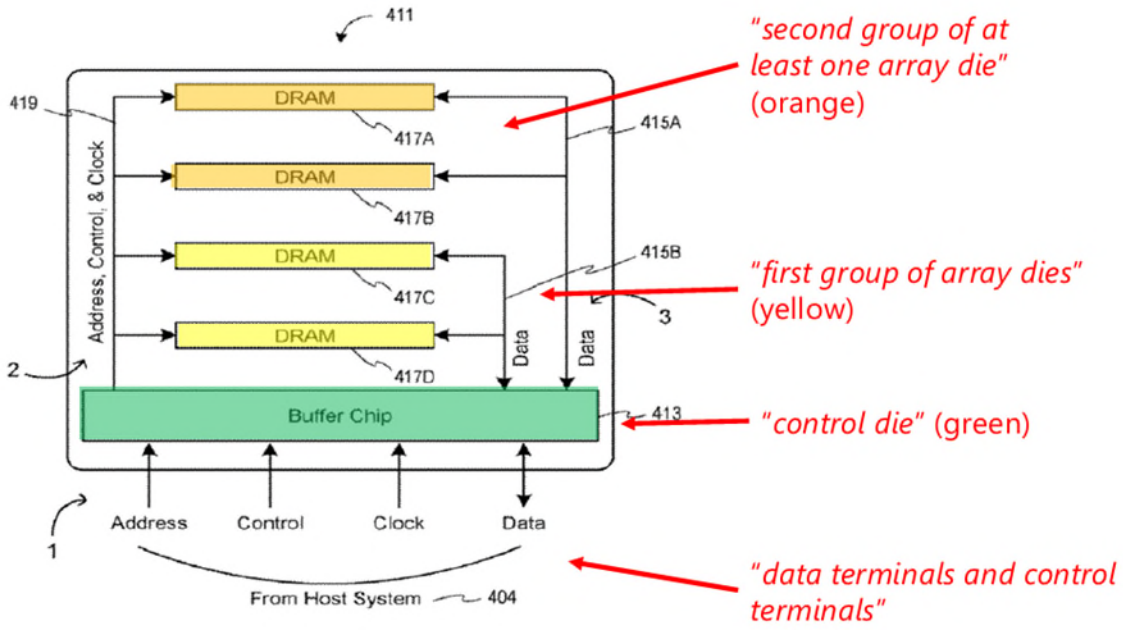


FIG. 4

507. Indeed, the claimed "*data terminals and control terminals*" and the corresponding data and control/address signals would have been obvious over Riho in view of the teachings of Rajan. For example, a Skilled Artisan would have been motivated to implement a JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make the Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory."); *see also id*. at Fig. 18 (reproduced below, disclosing that an

interface circuit includes emulation logic which interfaces, on one side with the host system and, on the other side, with the physical memory circuits, similar to Riho's logic control circuit 203, illustrated above).

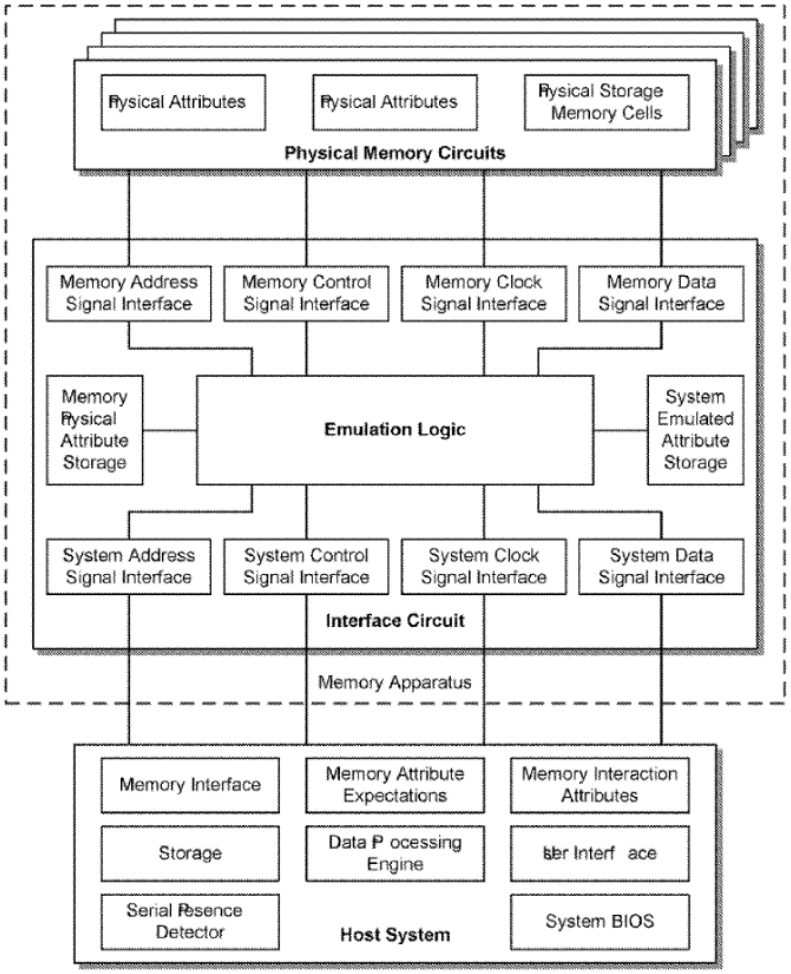


FIG. 18

508. Rajan is analogous art to Riho and the 160 Patent, as each is directed to the problem of effective operation of memory devices, including interfacing with stacked memory devices. Ex. 1015 (Rajan) at 1:51-60 ("What is needed, then, is an effective way to make use of low cost memory chips in manufacturing high capacity memory modules. … A memory subsystem is provided including an

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interface circuit adapted for communication with a system and a majority of address or control signals of a first number of memory circuits."), 4:48-50 ("In one embodiment, the DRAM chips are stacked, and the buffer chip is placed electrically between them and the host system."); Ex. 1016 (Riho) at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips."), [0012] ("According to this invention, when data signal DQ and data strobe signal DQS/B interconnections are formed by the penetrating through substrate vias, it is possible to minimize the skew between those interconnections. Further, when address, command, and clock interconnections are formed by the penetrating through substrate vias, it is also possible to minimize the skew between the address and clock interconnections and the skew between the command and clock interconnections."); Ex. 1001 (the 160 Patent) at 1:20-23 ("The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:26-29 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

509. Therefore, a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about how Riho's control chip can interface

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with a host system. Rajan discloses the same basic structure of a memory package like Riho and the 160 Patent: the package includes stacked memory chips and a common interface circuit, called "buffer chip" in Rajan. Ex. 1015 (Rajan) at 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses."), Fig. 4 (reproduced below, annotated).

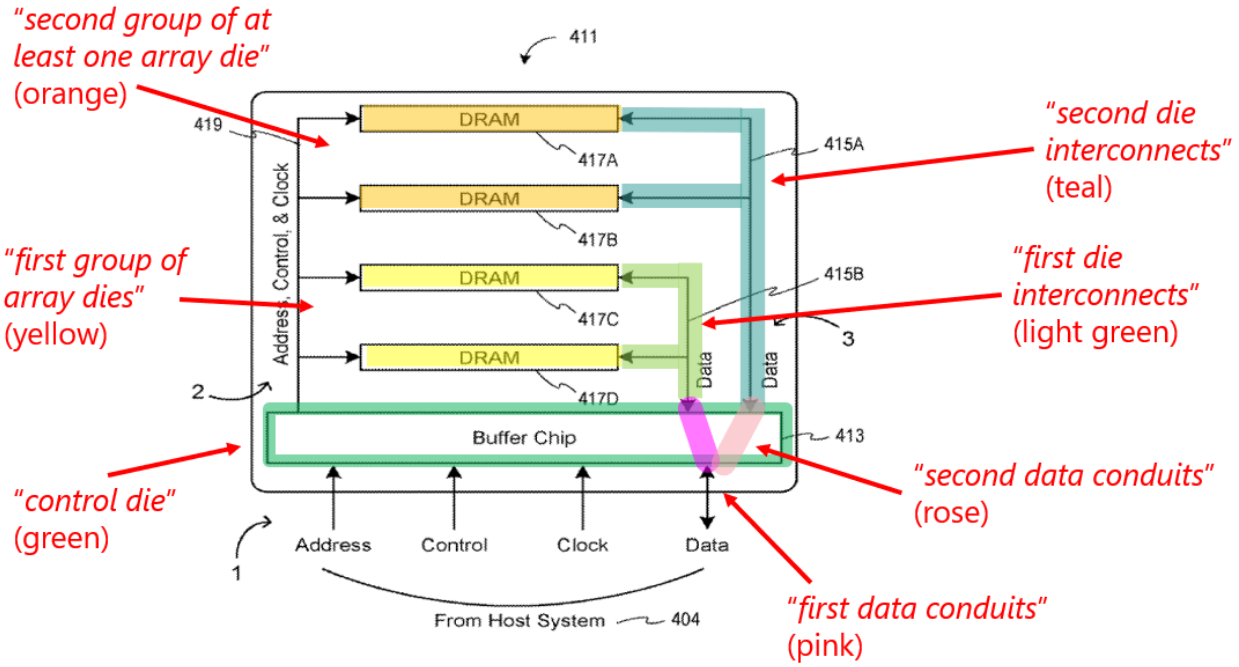


FIG. 4

510. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device

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Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below).

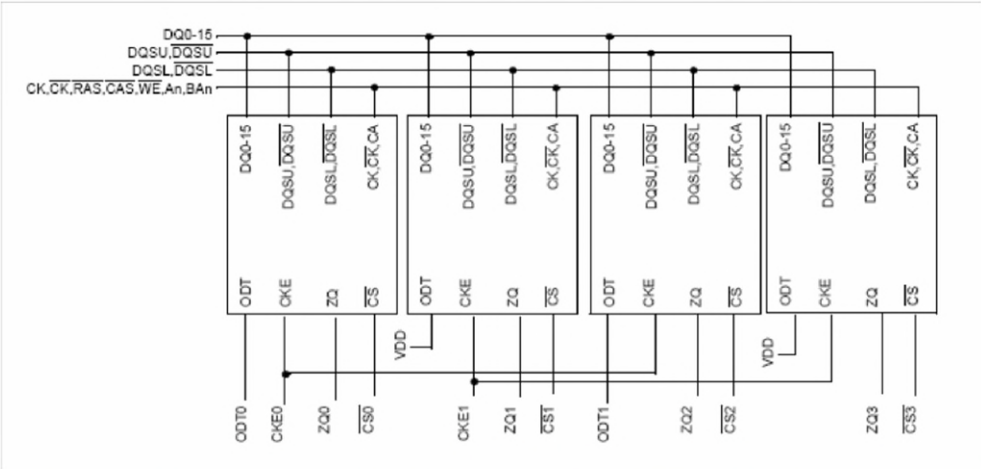


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

511. A Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control and data terminals according to the JEDEC standards in Riho's memory packages to use the packages in JEDEC compliant systems. For example, Rajan teaches that the "interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory." Ex. 1015 at 3:52-54, *see*

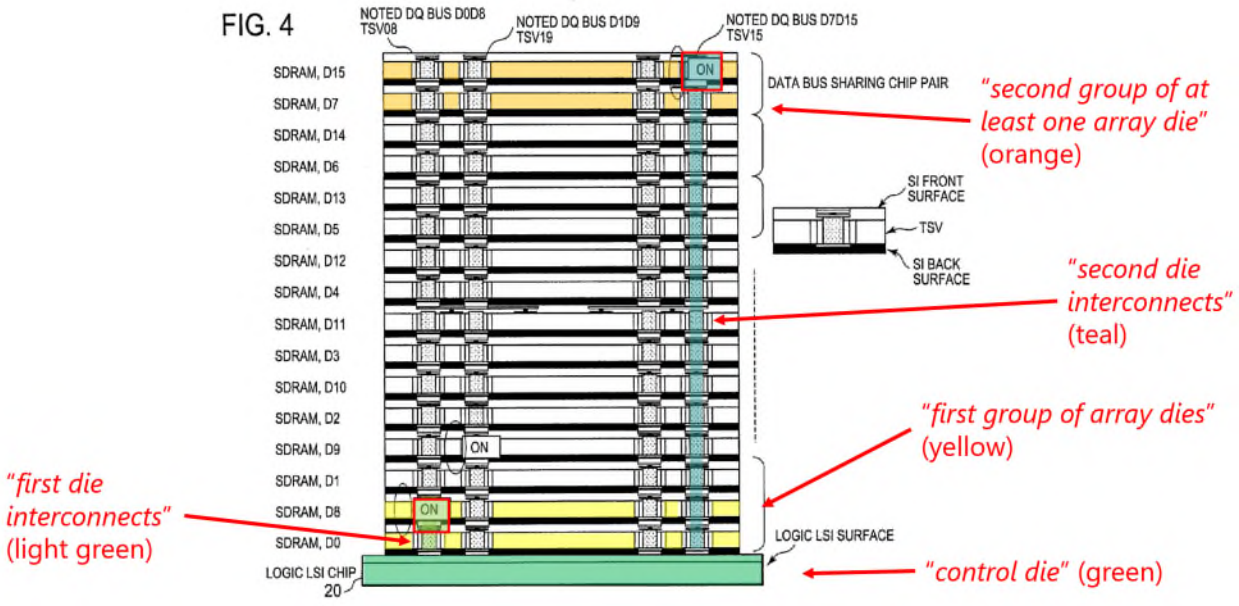
also id. at 6:30-7:67 (the interface circuit implementing rank multiplication). A Skilled Artisan would have also understood that a DDR3 SDRAM memory interface can include 4, 8, or 16 data terminals, and a GDDR3 memory can include 32 data terminals. *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.12-14 (describing pin-out for stacked DDR3 memory devices, Fig. 3 for x16 devices reproduced above); *see also* Ex. 1035 (JEDEC GDDR4 SGRAM Specification) at 2 ("The purpose of this Specification is to define the minimum set of requirements for JEDEC standard compatible 256 Mb through 1 Gb x32 GDDR4 SGRAM devices."). Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the admitted prior art referenced in the 160 Patent. *See, e.g.*, Ex. 1001 (the 160 Patent) at 22:22-24 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537). As discussed above, the JEDEC standards were influential and well known. *See supra* ¶¶131-133; Ex. 1022, pp. 332-35, 318-20.

512. Therefore, it would have been obvious to a Skilled Artisan to implement the functionality of a standardized interface as taught by Rajan in the stacked memory package of Riho to use Riho's memory package in standardized memory systems.

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513. An overview of Riho2 is provided above. *See supra* ¶¶128-130. As discussed below, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho, because Riho discloses differences in impedances and resistances for the different data signal DQ TSVs and Riho2 teaches to adjust the drive capacity according to such differences.

514. Riho discloses a memory package that includes stacked memory chips connected to a control chip by through-silicon vias (TSVs). Ex. 1016 (Riho) at Fig. 4 (reproduced below, annotated).



515. Riho explains that "[i]t is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in

manufacturing processes (TSV forming process, bump forming process, and TSV-bump connection process). That is, TSVs formed in different manufacturing processes may have different impedances due to manufacturing variations in the manufacturing processes." Ex. 1016 (Riho) at [0055]. Riho further explains that "it is also preferable to expect that when a plurality of signal lines are formed by a plurality of TSVs, the impedance of each signal line may be different from those of the others due to variations of inherent manufacturing processes." *Id.* at [0056]. For example, Riho describes that "the SDRAM chip located closer to the logic LSI chip 20 has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip 20 has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process." *Id.* at [0061].

516. A Skilled Artisan would have understood from this disclosure that differences in impedances and other variations in the through-silicon vias and the different positions of the SDRAM chips should be taken into account when designing the stacked structure of Riho.

517. Furthermore, a Skilled Artisan would have understood that, in a case where "it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the

silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another … , a configuration is provided to optimize the output drive capacity of output buffers according to the number of stacked chip dies." Ex. 1018 (Riho2) at [0096]. A Skilled Artisan would have also known how to optimize the drive capacity. For example, Riho2's "FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097], Fig. 7A (reproduced below).

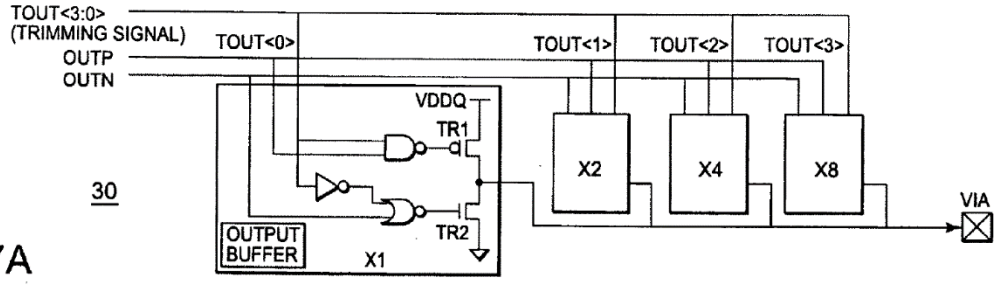


FIG. 7A

518. Therefore, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho, because Riho discloses differences in impedances and resistances for the different data signal DQ TSVs and Riho2 teaches to adjust the drive capacity according to such differences.

519. Riho2 is analogous art to Riho and the 160 Patent, as each is directed to the problem of communicating signals between stacked chips. *See, e.g.*, Ex. 1018 (Riho2) at [0003] ("This invention relates to a semiconductor device having a DRAM or the like, and particularly to a semiconductor device formed by stacking a plurality of chip dies."), [0010] ("Thus, the fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the face that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips."); Ex. 1016 (Riho) at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips."), [0012] ("According to this invention, when data signal DQ and data strobe signal DQS/B interconnections are formed by the penetrating through substrate vias, it is possible to minimize the skew between those interconnections."); Ex. 1001 (the 160 Patent) at 1:20-23 ("The present disclosure relates to memory devices and memory modules. More specifically, the

present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:26-29 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

520. Therefore, a Skilled Artisan would have been motivated to look at analogous art like Riho2, which is by the same inventor as Riho, to address the issues created by the variations in the TSV properties described by Riho. In particular, a Skilled Artisan would have been motivated to optimize the output drive capacity of output buffers as taught by Riho2. A Skilled Artisan would have also understood that such an optimization of driver capacity would save power compared to using full-capacity drivers, which would be wasteful and inefficient. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."); *see also id.* at 5:11-14, Fig.5; Ex. 1039 at Abstract ("In other embodiments, for example, differences in the termination impedance or driver drive-strength resulting from differences in the location of a die in a stack may be compensated for."), 7:46-49 ("One embodiment of a compensation circuit 400 that may compensate for both termination impedance and drive strength variations resulting from differences in die location is shown in FIG. 6."), and Fig. 6.

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521. Making such a combination was well within the level of skill, since Riho2 itself teaches drivers of different strengths, and the combination would have provided nothing more than expected: a power efficient drive of signals through Riho's TSVs.

522. Therefore, it would have been obvious to a Skilled Artisan to implement the functionality of optimized drivers as taught by Riho2 in the stacked memory package of Riho to make Riho's memory package more efficient.

D. Claims 1-20 Are Unpatentable Over Ground 2

523. As explained below claims 1-20 are unpatentable over Ground 2 (Riho in view of Rajan and Riho2).

1. Claim 1 is Unpatentable

524. Claim 1 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [1.a] Preamble

525. The preamble of claim 1 requires "*[a] memory package, comprising.*"

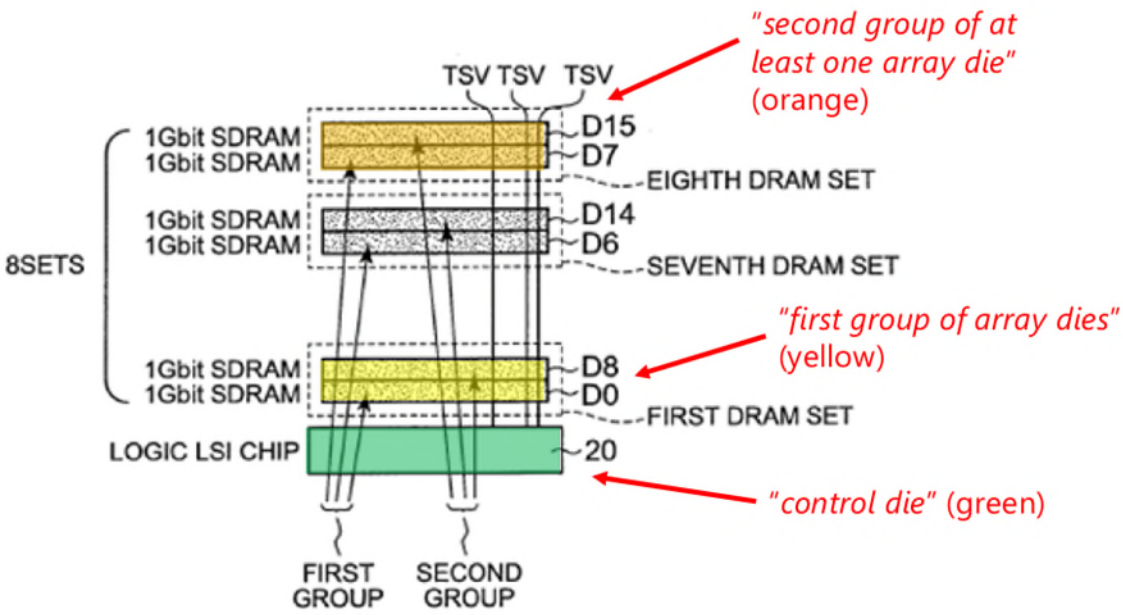
526. To the extent the preamble is limiting, the prior art references in Ground 2 teach this limitation to a Skilled Artisan.

527. Riho discloses a "*memory package*" including a control chip (logic LSI chip 20) and stacked SDRAM chips (D0-D15) "integrally packaged." Ex. 1016 at Fig. 1 (reproduced below, annotated), [0026] ("The illustrated semiconductor device [in FIG. 1] comprises a logic LSI chip 20 as a control chip

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and a plurality of SDRAM chips as controlled chips stacked on the logic LSI chip 20. The control chip may be also called a master chip (or active chip) while each controlled chip is a slave chip (or passive chip). For example, the semiconductor device comprising the master chip and the slave chips has a system-in-package structure in which those chips are assembled in layers and integrally packaged.").

FIG. 1



528. Therefore, Riho discloses a "*memory package*."

529. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in Ground 2 satisfy "*[a] memory package, comprising*."

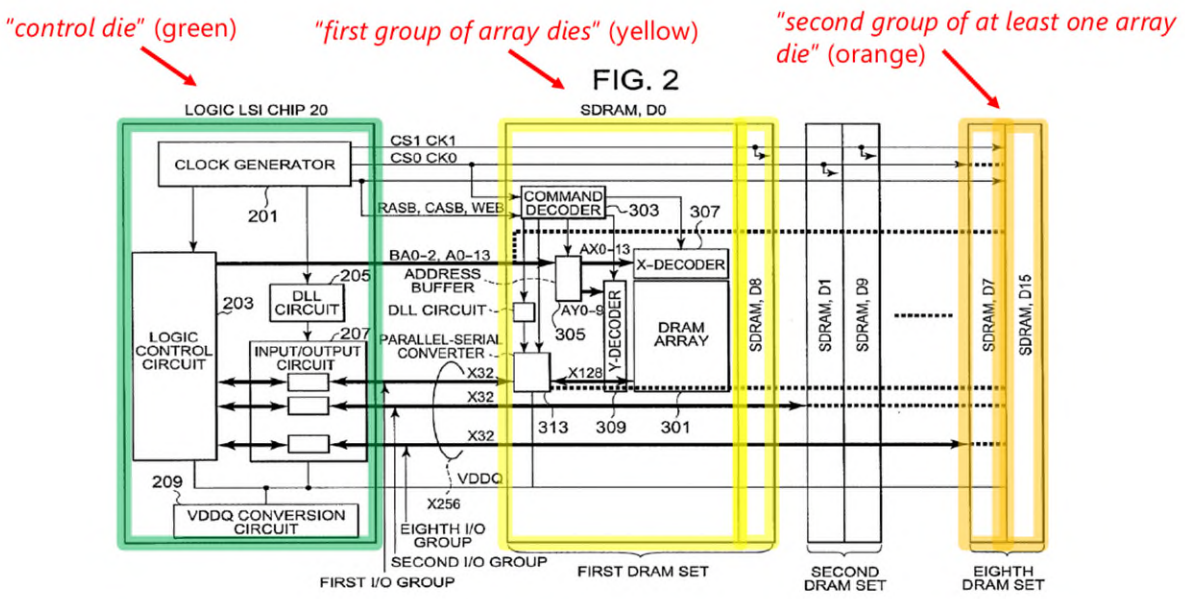
b) [1.b] Data Terminals and Control Terminals

530. Claim 1 requires "*data terminals and control terminals.*"

531. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

532. Riho discloses to a Skilled Artisan that the stacked memory package includes "*data terminals and control terminals*."

533. For example, with reference to Fig. 1, Riho discloses that, "external terminals (not illustrated) of the semiconductor device . . . are disposed on the lower side of the logic LSI chip 20," and that "[t]he external terminals are connected to the logic LSI chip 20." Ex. 1016 at [0026]. Riho further discloses that "I/O signal lines penetrating through the controlled chips . . . are connected to the logic LSI chip 20 and are not directly connected to the external terminals." *Id.* Riho also discloses that the logic LSI chip 20 communicates data signals (DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals), address signals (BA0-BA2 and A0-A13), and control signals (RASB, CASB, WEB, CS0CK0, CS1CK1,…) to the SDRAMs in the stack. *See id.* at [0030-31], Fig. 2 (reproduced below, annotated).



534. A Skilled Artisan would have understood from this disclosure that, e.g., in light of the teaching of Rajan and/or the Skilled Artisan's knowledge of the common JEDEC specifications, Riho's memory package can operate as a memory device so that logic LSI chip 20 has "*data terminals and control terminals*" at its lower side via which the memory package communicates data and control/address signals with one or more external devices and uses the received control/address signals to control the SDRAM chips in the stack. For example, a Skilled Artisan would have been motivated to use terminals in Riho's control die for external data and control/address signals as taught by Rajan. *Supra* at ¶¶503-512; *see, e.g.*, Ex. 1015 (Rajan) at Figs. 4 and 18 (reproduced below, annotated, showing that, in a stacked arrangement of DRAM devices, a buffer chip receives data and

control/address signals from an external host system and controls the DRAM devices in the stack).

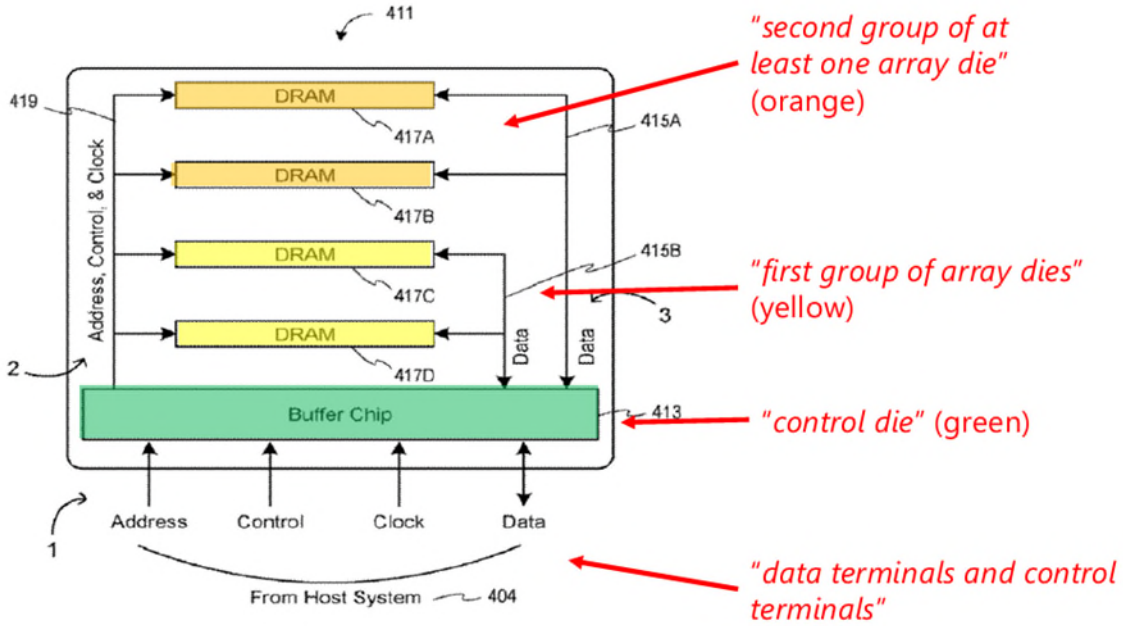


FIG. 4

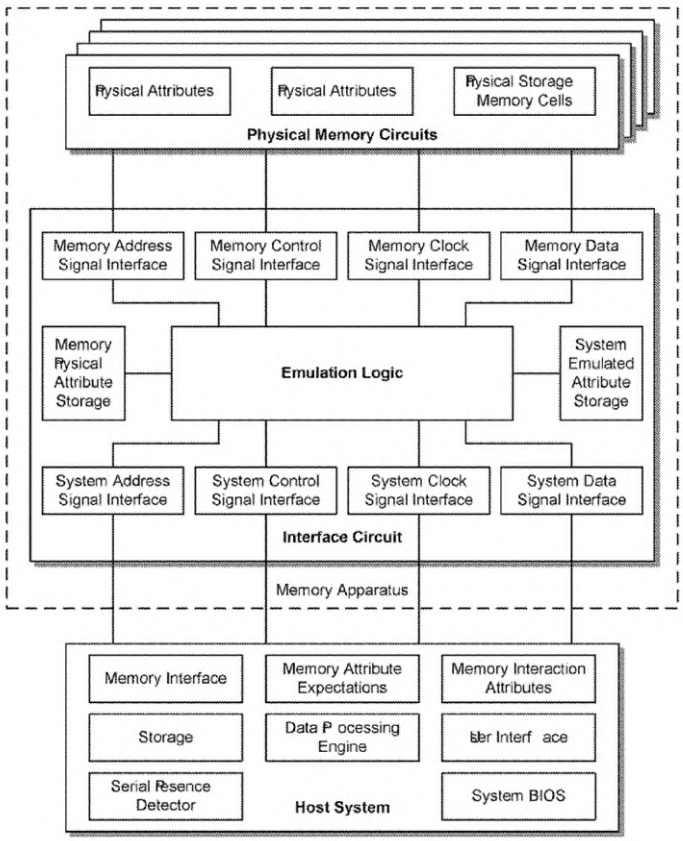


FIG. 18

535. Accordingly, it would have been obvious to a Skilled Artisan to combine Riho and Rajan and implement Riho's memory package with the terminals as disclosed by Rajan. *Supra* ¶¶503-522.

536. Therefore, Riho discloses and in view of Rajan renders obvious this limitation to a Skilled Artisan.

537. Accordingly, the prior art references in Ground 2 satisfy "*data terminals and control terminals.*"

c) [1.c] Stacked Array Dies

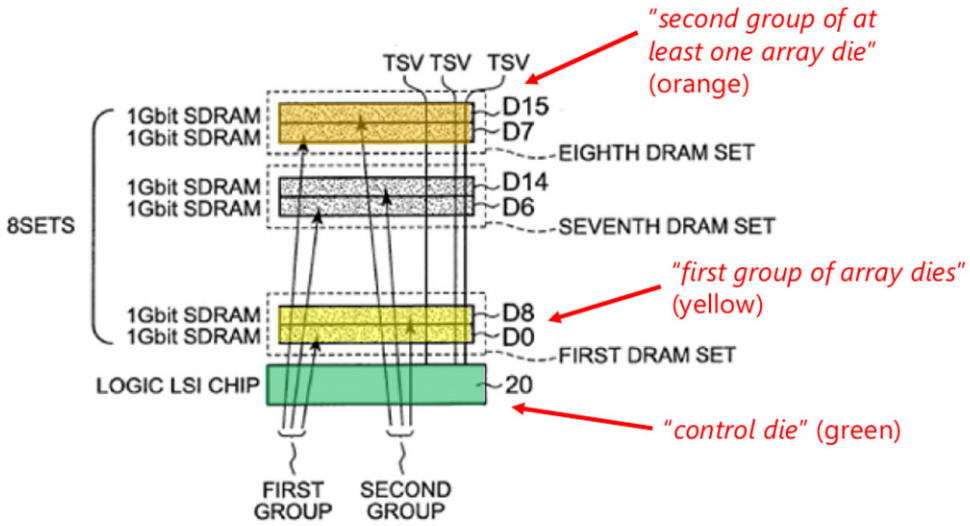
538. Claim 1 requires "*stacked array dies including a first group of array dies and a second group of at least one array die.*"

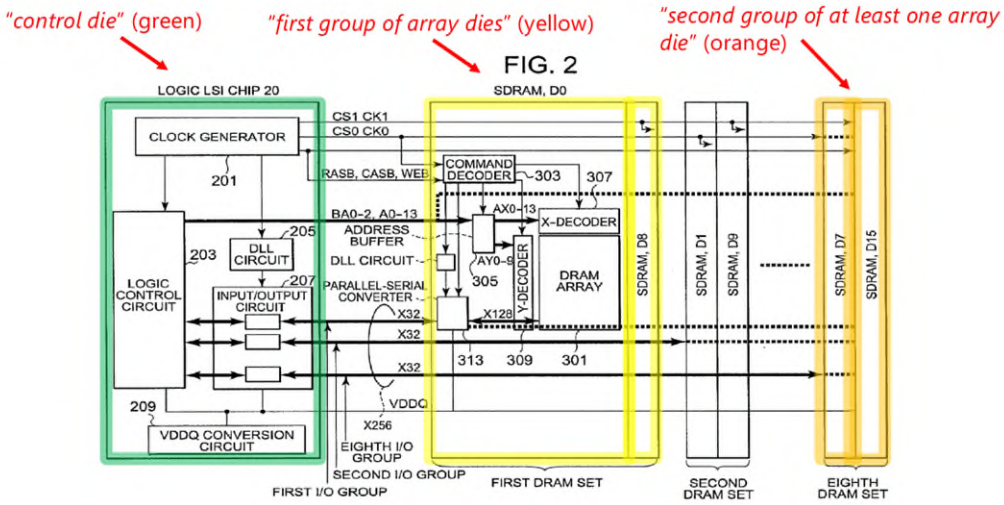
539. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

540. Riho discloses "*stacked array dies including a first group of array dies* [e.g., a first DRAM set including a pair of SDRAMs D0 and D8 sharing data signal DQ TSV08] *and a second group of at least one array die* [e.g., an eighth DRAM set including a pair of SDRAMs D7 and D15 sharing data signal DQ TSV715]." *See, e.g.*, Ex. 1016 at Fig. 1 (reproduced below, annotated, showing stacked SDRAMs including eight sets of SDRAM pairs), Fig. 2 (reproduced below, annotated, showing internal structure of SDRAMs, including a DRAM array and a parallel-serial conversion circuit 313 for communicating data with the logic chip 20).

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FIG. 1





541. For example, Riho discloses "*stacked array dies*," such as SDRAM chips D0-D15. *Id.* at Fig. 1 (reproduced above), [0027] ("FIG. 1 shows an example in which 16 SDRAM chips D0 to D15 each having a memory capacity of 1 Gbit are stacked on the logic LSI chip 20 operable as the control chip. Each of the illustrated SDRAM is a DDR (Double Data Rate) 3 synchronous dynamic

random access memory."). Riho further discloses that each of SDRAM chips D0-D15 include a respective DRAM array 301 and a parallel-serial converter 313. *See id.* at [0047] ("Herein, taking the SDRAM D0 as an example, the structure of the SDRAM chip used in this embodiment will be described. The illustrated SDRAM D0 comprises . . . a DRAM array 301 having a memory capacity of 2 Gbit, a command decoder 303, an address buffer 305, an X-decoder 307, a Y-decoder 309, a DLL circuit 311, and a parallel-serial conversion circuit 313."). Riho explains that "the DRAM array 301 inputs and outputs 128-bit (×128) data signals in parallel between itself and the parallel-serial conversion circuit 313. … The parallel-serial conversion circuit 313 sends and receives ×128-bit parallel data signals between itself and the DRAM array 301 and further sends and receives 32-bit (×32) parallel data signals between itself and the logic LSI chip 20." *Id*. at [0049].

542. A Skilled Artisan would have understood from this disclosure that each SDRAM chip in Riho is an "*array die*" because each chip includes a DRAM array and further includes a respective parallel serial conversion circuit 313, which communicate (x32) data between the DRAM array 301 and the control chip 20. A Skilled Artisan would have also understood that Riho's SDRAM chip includes a "*die*." *See, e.g.*, Ex. 1018 (Riho2) at Abstract and Fig. 1 (describing, similar to

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Riho, "stacked chip dies," each including a respective memory cell array 230 and IO circuits 2500-2531).

543. Riho also discloses (eight) groups of SDRAMs, including a "*first group of array dies*," such as the first DRAM set including SDRAMs D0 and D8, and a "*second group of at least one array die*," e.g., the eighth DRAM set including SDRAMs D7 and D15. Ex. 1016 at Fig. 1, [0029] ("In the illustrated example, the SDRAMs D0 and D8 form a first DRAM set located closest to the logic LSI chip 20, then, subsequent pairs of the SDRAMs D1 and D9, D2 and D10, D3 and D11, D4 and D12, D5 and D13, D6 and D14, and D7 and D15 form second to eighth DRAM sets, respectively. As seen in FIG. 1, the SDRAM D15 of the eighth DRAM set is disposed at a position farthest from the logic LSI chip 20."). Riho further explains that the SDRAMs in each DRAM set share respective data signal TSVs. *Id.* at [0045-46] ("… the data signal DQ TSVs for the SDRAM D0 are also used by the SDRAM D8 (first DRAM set). That is, the data signal DQ TSVs for the SDRAM D0 are commonly used by the first DRAM set (SDRAM D0 and SDRAM D8). … The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15."), [0062] ("The adjacent two SDRAMs of the first and second groups, such as, for example, the SDRAMs D0 and D8, D1 and D9, or D7 and D15, form a SDRAM

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pair or set (n-th DRAM set) sharing the corresponding data signal DQ TSVs, i.e. corresponding buses (n-th I/O group).").

544. Therefore, Riho discloses this limitation to a Skilled Artisan.

545. Accordingly, the prior art references in Ground 2 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*."

d) [1.d.1] and [1.d.2] Die Interconnects in Electrical Communication with Array Dies

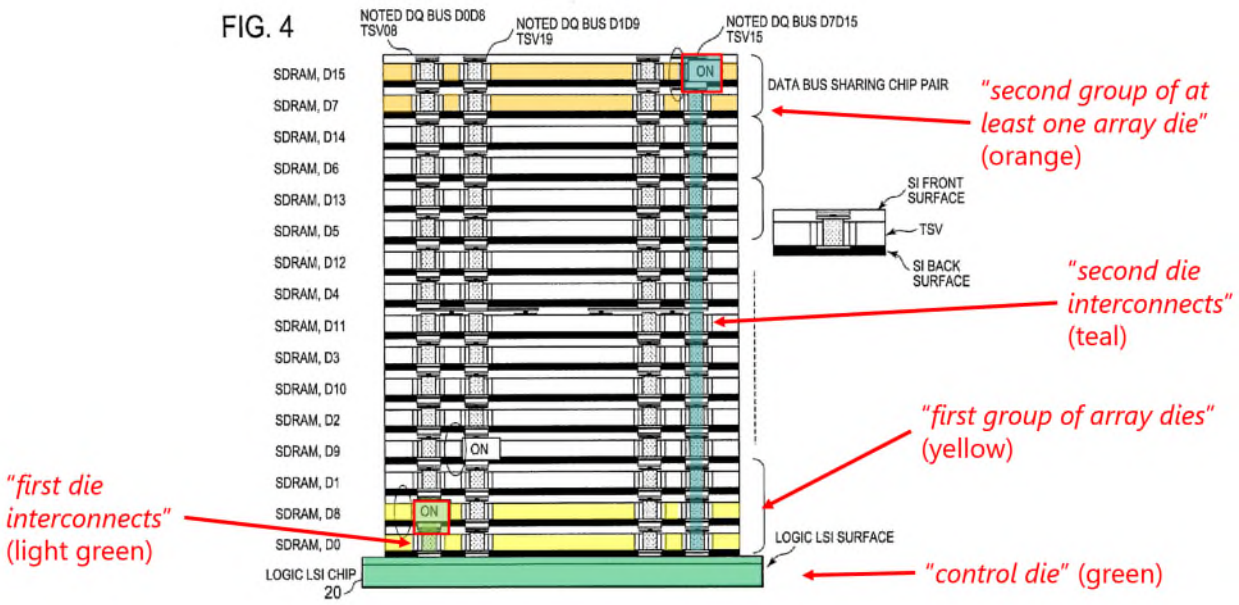
546. Claim 1 requires "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

547. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

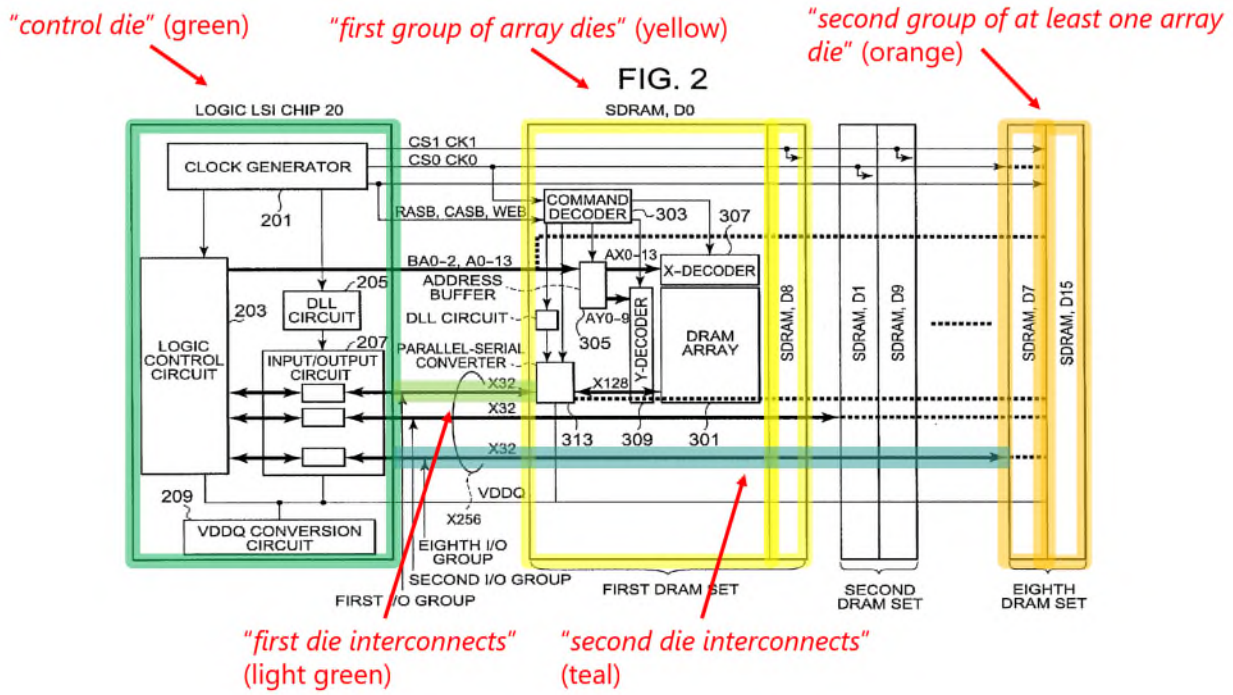
548. Riho discloses to a Skilled Artisan, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, "*first die interconnects* [e.g., data signal DQ TSV08] *and second die interconnects* [e.g., data signal DQ TSV715], *the first die interconnects* [TSV08] *in electrical communication with the first group of array dies* [the first DRAM set including SDRAMs D0 and D8] *and*

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not in electrical communication with the second group of at least one array die [all other SDRAMs, including the eighth DRAM set of SDRAMs D7 and D15]." *See, e.g.*, Ex. 1016 at Figs. 2, 4 (reproduced below, annotated).



549. For example, Riho explains that "SDRAM D0 (first DRAM set) and the input/output circuit 207 of the logic LSI chip 20 are connected to each other through the 32 data signal DQ TSVs as indicated by ×32 (first I/O group) in FIG. 2." Ex. 1016 at [0045], Fig. 2 (reproduced below annotated).



550. Riho further discloses that "the data signal DQ TSV08 includes a portion shared by the SDRAMs D0 and D8 and, in this connection, circuits formed at the front surfaces of the SDRAMs D0 and D8 and the data signal DQ TSV08 are in a conductive state (i.e. on state). On the other hand, the SDRAMs other than the SDRAMs D0 and D8 and the data signal DQ TSV08 are in a non-conductive state (i.e. off state)." Ex. 1016 at [0064].

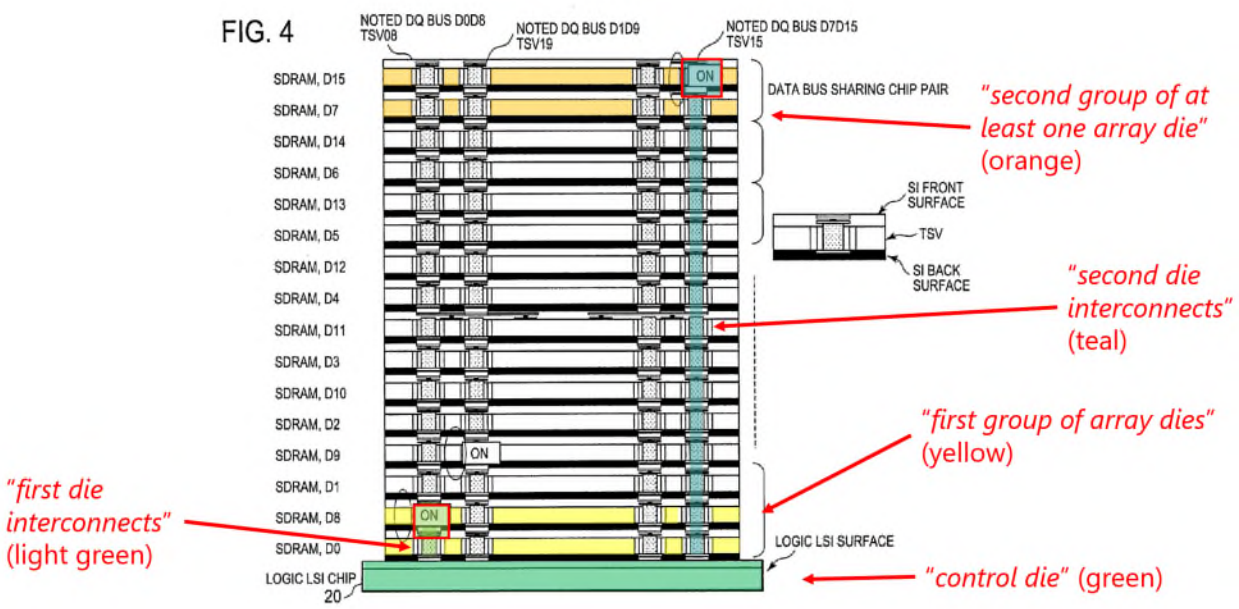
551. A Skilled Artisan would have understood from this disclosure that, at least under Netlist's apparent interpretation, Riho's data signal DQ TSV08 is "*in electrical communication with the first group of array dies*" including SDRAMs D0 and D8, which are set into a conductive "on state," and that DQ TSV08 is "*not in electrical communication*" with any other SDRAMs, including SDRAMs D7

and D15 in the "*second group of at least one array die*," which are in a non-conductive "off state."

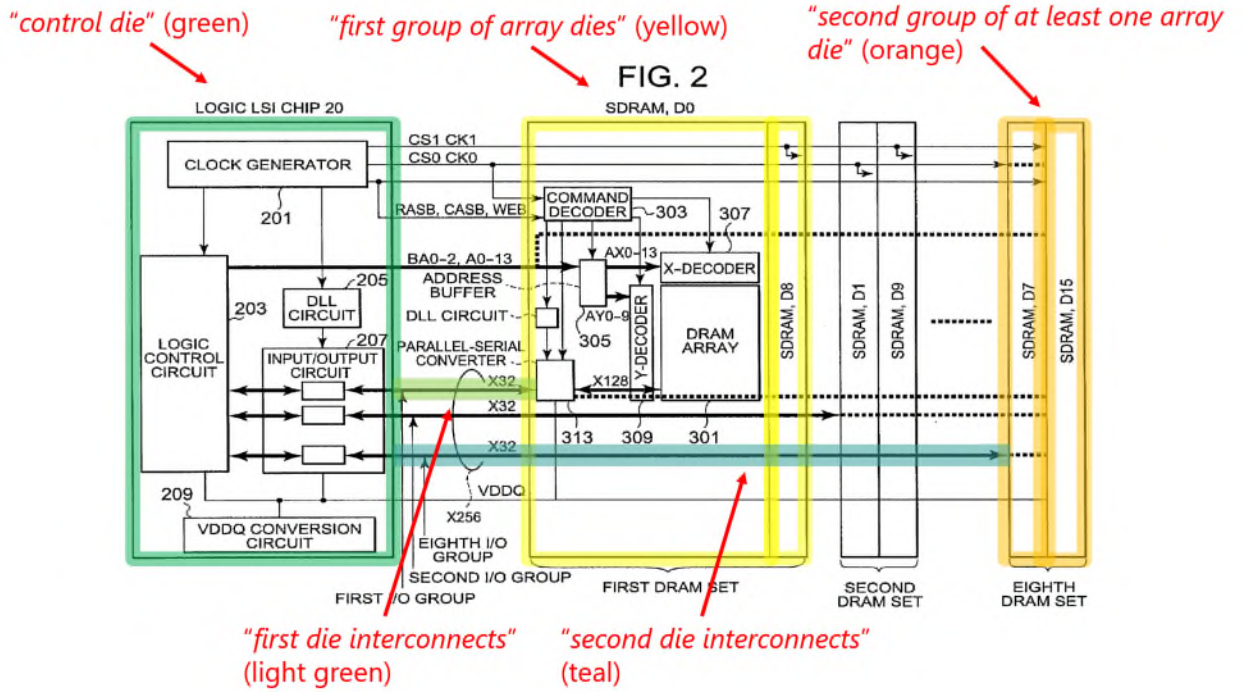
552. Therefore, Riho discloses "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*" to a Skilled Artisan.

553. Likewise, Riho discloses to a Skilled Artisan, at least under Netlist's apparent interpretation, that "*the second die interconnects* [TSV715 are] *in electrical communication with the second group of at least one array die* [the eighth DRAM set including SDRAMs D7 and D15] *and not in electrical communication with the first group of array dies* [the first DRAM set including SDRAMs D0 and D8]." *See, e.g.*, Ex. 1016 at Figs. 2, 4 (reproduced below annotated).

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554. For example, Riho explains that "data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15." Ex. 1016 at [0046], Fig. 2 (reproduced below, annotated).



555. Riho further explains that "the data signal DQ TSV715 and circuits formed at the front surfaces of the SDRAMs D7 and D15 are in a conductive state (i.e. on state)." Ex. 1016 at [0065].

556. For the reasons discussed immediately above with reference to the "*first die interconnects*" TSV08, a Skilled Artisan would have understood from Riho's disclosure that, at least under Netlist's apparent interpretation, data signal DQ TSV715 ("*the second die interconnects*") is in electrical communication with SDRAMs D7 and D15, but not with any other SDRAMs in the stack.

557. Therefore, Riho discloses "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*" to a Skilled Artisan.

558. Furthermore, it would have been obvious to a Skilled Artisan in view of Rajan that "*the first die interconnects* [(light green) for communicating data are] *in electrical communication with the first group of array dies* [including array dies D0 and D8 (yellow)] *and not in electrical communication with the second group of at least one array die* [including array dies D7 and D15 (orange)]," and "*the second die interconnects* [(teal) for communicating data are] *in electrical communication with the second group of at least one array die* [including array dies D7 and D15 (orange)] *and not in electrical communication with the first group of array dies* [including array dies D0 and D8 (yellow)]."

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559. Rajan teaches that memory dies in a stack are grouped such that first die interconnects (415B, light green) to communicate data are in electrical communication with a first group of dies (including dies 417C and 417D, yellow) and not in electrical communication with a second group of memory dies (including dies 417A and 417B, orange). Ex. 1015 (Rajan) at 5:36-43 ("There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B. Each shared bus has two or more DRAM chips coupled to it."), Fig. 4 (reproduced below, annotated). Rajan also teaches second die interconnects (415A, teal) to communicate data that are in electrical communication with the second group of dies (including dies 417A and 417B, orange) and not in electrical communication with the first group of memory dies (including dies 417C and 417D, yellow). *Id*.

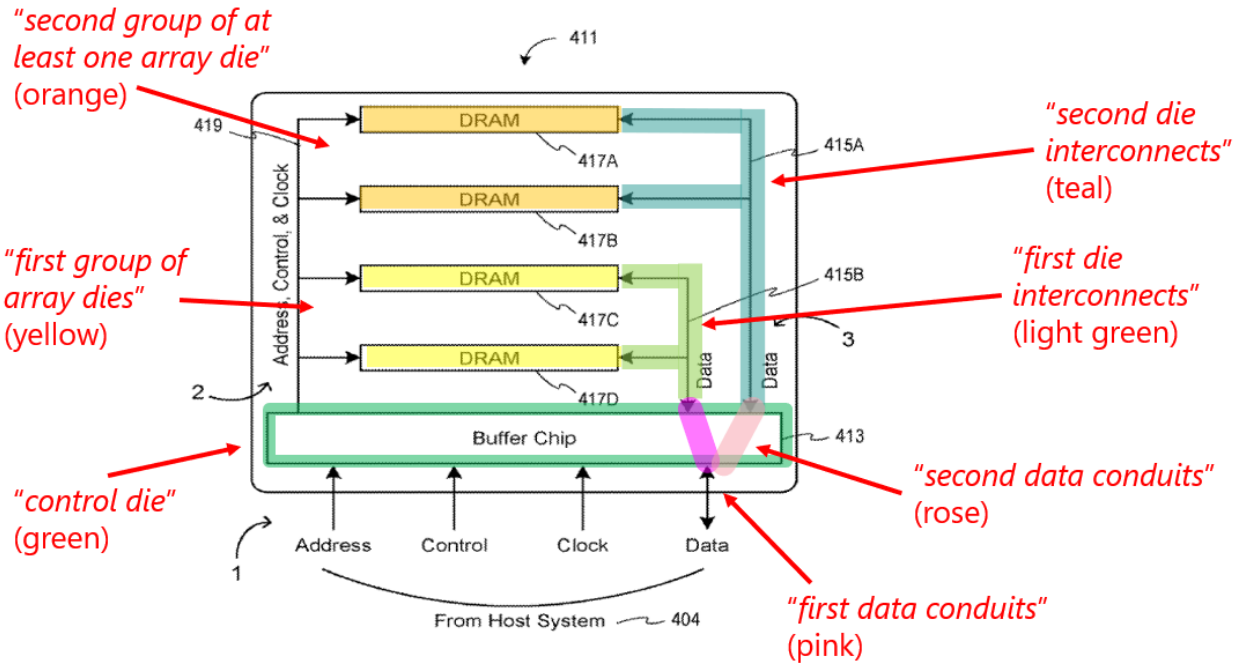


FIG. 4

560. As discussed above, Riho and Rajan are analogous art to the 060 Patent. *Supra* at ¶508. Furthermore, each of them is directed to memory stacks and pertinent to the problem of reducing load in systems using stacked memory devices. Ex. 1015 (Rajan) at 5:63-6:2 ("FIGS. 2 through 6 are not intended to be an exhaustive listing of all possible permutations of data paths, busses, and buffer chip configurations, and are only illustrative of some ways in which the host system device can be in electrical contact only with the load of the buffer chip and thereby be isolated from whatever physical memory circuits, data paths, busses, etc. exist on the (logical) other side of the buffer chip."); Ex. 1016 (Riho) at [0103] ("Further, by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs)

are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups."), Ex. 1001 (060 Patent) at ("More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules.").

561. A Skilled Artisan would have been motivated to look at analogous art like Rajan and apply the teaching of Rajan to the groups of dies in the stack of Riho such that each group of dies communicates data through respective die interconnects which are not in electrical communication with other dies in the stack because such an arrangement advantageously lowers the load on those die interconnects. *See*, *e.g.*, Ex. 1016 (Riho) at [0013] ("Further, when the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used.").

562. For at least the above reasons, these limitations were also obvious to a Skilled Artisan over Riho in light of Rajan.

563. Accordingly, the prior art references in Ground 2 satisfy "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical*

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communication with the second group of at least one array die," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

e) [1.e] Control Die

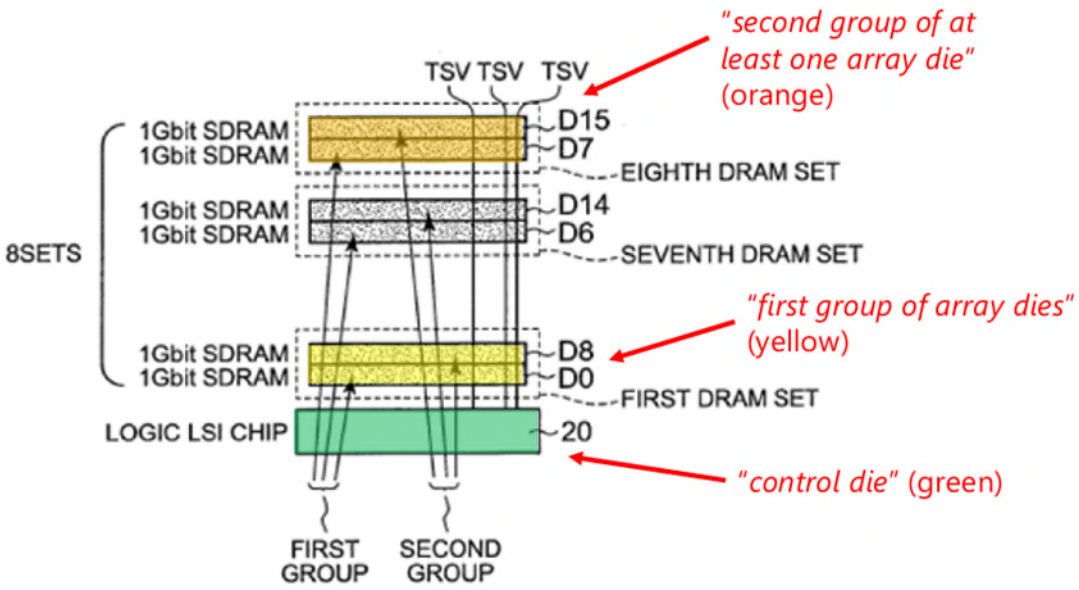
(1) [1.e.1] A Control Die Comprising

564. Claim 1 requires "*a control die comprising.*"

565. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

566. Riho discloses "*a control die*" including Logic LSI chip 20. *See, e.g.*, Ex. 1016 at Fig. 1 (reproduced below, annotated).

FIG. 1



567. For example, Riho discloses that the "illustrated semiconductor device comprises a logic LSI chip 20 as a control chip and a plurality of SDRAM chips as controlled chips stacked on the logic LSI chip 20." Ex. 1016 at [0026].

568. A Skilled Artisan would have understood from this disclosure that the logic LSI chip 20 includes a die which controls the operation of the stacked SDRAMs in Riho's semiconductor device.

569. Furthermore, in the combination of Riho and Rajan, the "*control die*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices. *Supra* at ¶¶137-139, 503-512.

570. Therefore, Riho discloses and in view of Rajan renders obvious this limitation to a Skilled Artisan.

571. Accordingly, the prior art references in Ground 2 satisfy "*a control die comprising*."

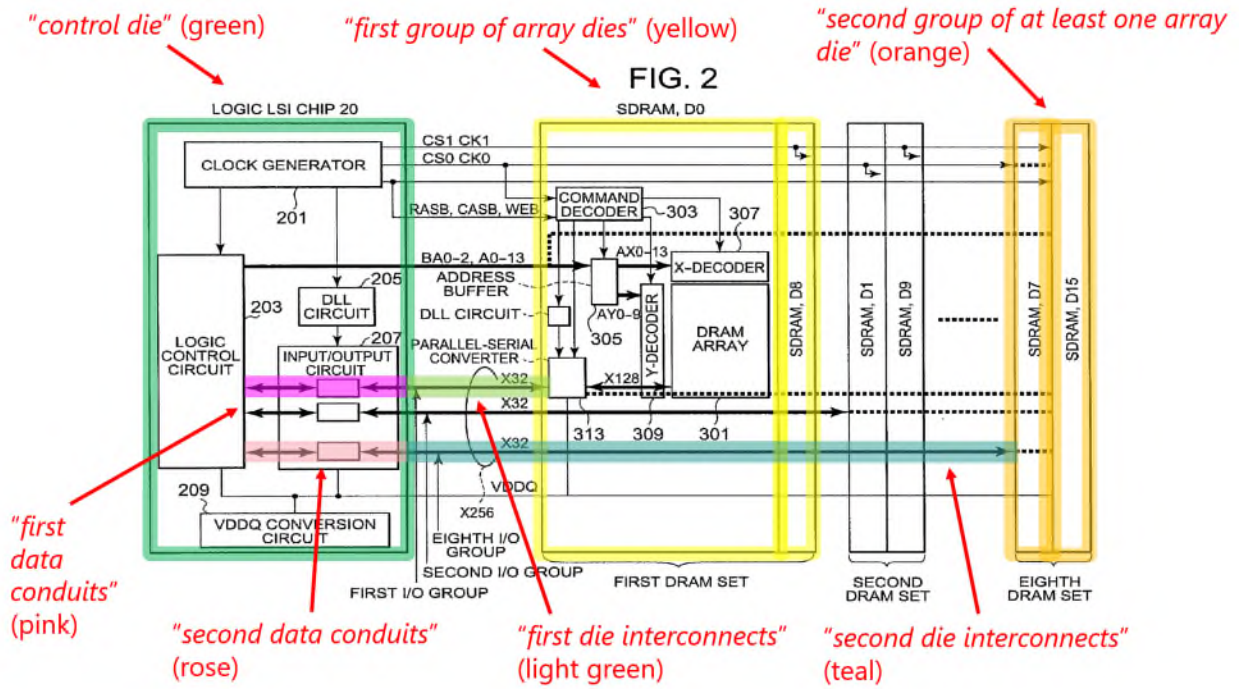
(2) [1.e.2] and [1.e.3] First and Second Data Conduits

572. Claim 1 requires "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

573. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

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574. Riho discloses and renders obvious to a Skilled Artisan "*first data conduits* [(pink)] *between the first die interconnects* [TSV08] *and the data terminals* [such as external data terminals of the control chip 20]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



575. For example, Riho discloses that "[t]he logic control circuit 203 provided in the logic LSI chip 20 … sends and receives data signals DQ between itself and the input/output circuit 207." *Id.* at [0039]. Riho also discloses that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total." *Id.* at [0040]. Riho further discloses that the input/output circuit 207 transmits or receives the data

signal DQ "as an I/O data signal," and that each DRAM set is allocated with a respective I/O group (×32 DQ signal bits) for a total of eight I/O groups. *Id.* For example, "[t]he SDRAM D0 (first DRAM set) and the input/output circuit 207 of the logic LSI chip 20 are connected to each other through the 32 data signal DQ TSVs as indicated by ×32 (first I/O group) in FIG. 2. The input/output circuit 207 includes interface circuits such as buffers corresponding to the SDRAM chips, respectively, so that data signals DQ are sent and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit." *Id.* at [0045].

576. Furthermore, as discussed above with reference to claim limitation [1.b], Riho discloses and renders obvious in view of Rajan to a Skilled Artisan that control chip 20 has input/output terminals for communicating data signals. *Supra* ¶¶530-537; *see also, e.g.*, Ex. 1016 at [0026] ("In the figure, external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20."); *see also* Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, expressly showing data connections with an external device of a host system).

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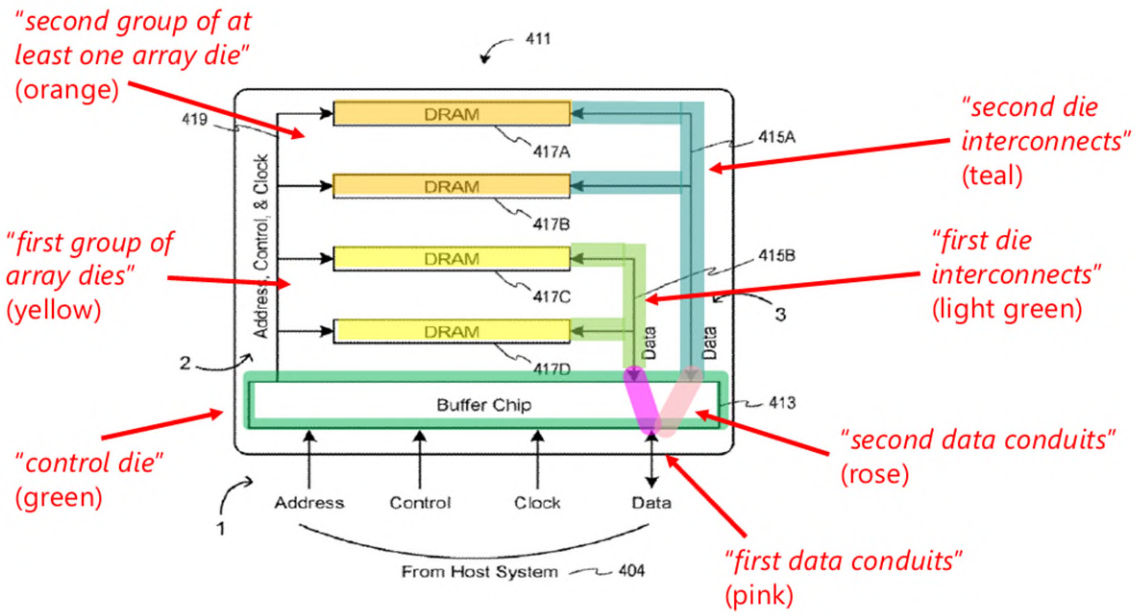
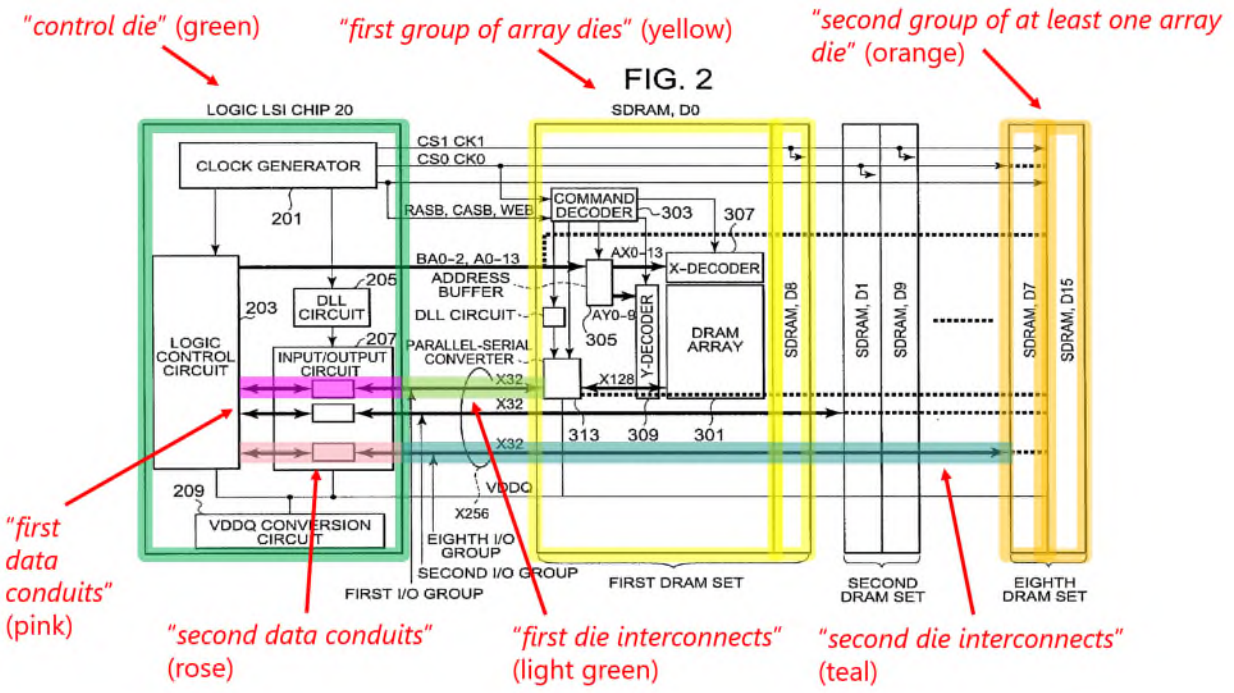


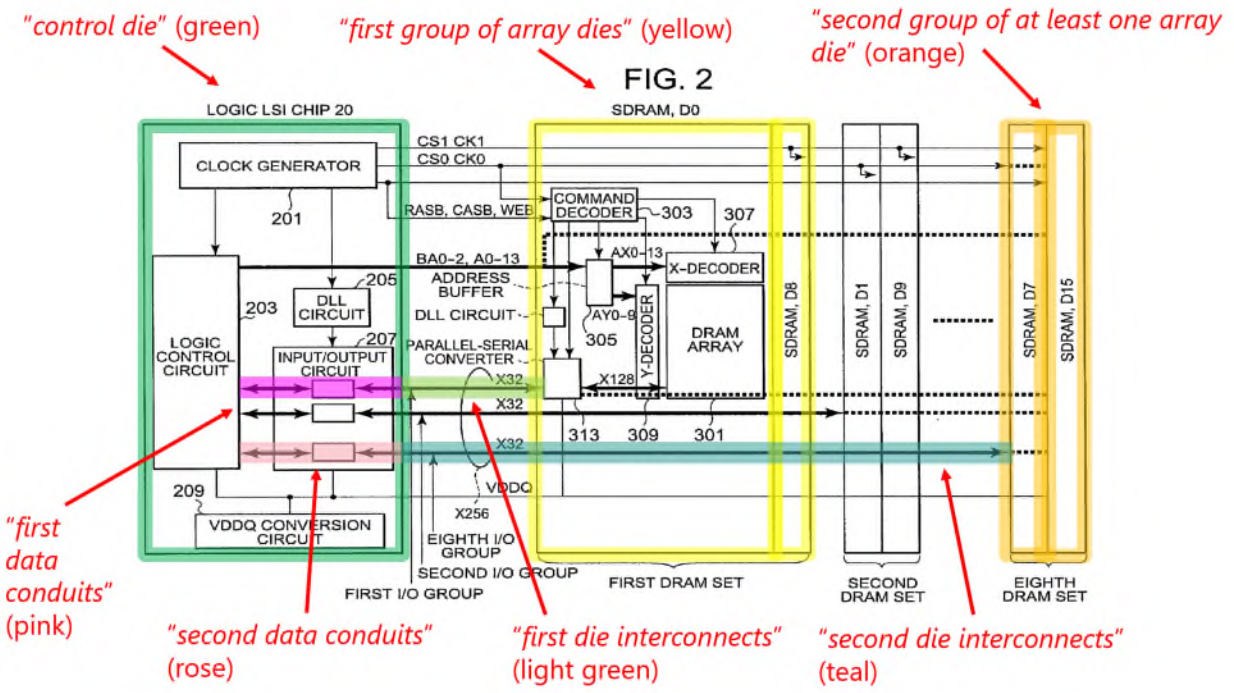
FIG. 4

577. A Skilled Artisan would have understood from this disclosure that the control chip 20 of Riho includes "*first data conduits*" (pink) including a portion of the input/output circuit 207 that is connected to the data signal DQ TSV08 ("*the first die interconnects*"), on one hand, and to a corresponding external data terminal of the control chip 20 ("*data terminals*") through which the corresponding data is transmitted, on the other hand. *See, e.g.*, Ex. 1016 (Riho) at Fig. 2 (reproduced below, annotated).



578. Therefore, Riho discloses and renders obvious in view of Rajan "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*" to a Skilled Artisan.

579. Riho alone or in combination with Rajan discloses and renders obvious to a Skilled Artisan "*second data conduits* [(rose)] *between the second die interconnects* [DQ TSV715 (teal)] *and the data terminals* [terminals of the control chip 20]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



580. For example, as discussed above with reference to the "*first data conduits*," Riho discloses that "[t]he logic control circuit 203 provided in the logic LSI chip 20 … sends and receives data signals DQ between itself and the input/output circuit 207." *Id.* at [0039]. Riho also discloses that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total." *Id.* at [0040]. Riho further discloses that the input/output circuit 207 transmits or receives the data signal DQ "as an I/O data signal," and that each DRAM set is allocated with a respective I/O group (×32 DQ signal bits) for a total of eight I/O groups. *Id.*; *see also id.* at [0046] ("The data signal DQ TSVs for the SDRAM D7 are provided between the

input/output circuit 207 of the logic LSI chip 20 and the SDRAM D7. The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15.").

581. As also discussed above with reference to the "*first data conduits*" (pink), a Skilled Artisan would have understood from Riho's disclosure that the control chip 20 includes "*second data conduits*" (rose) including a portion of the input/output circuit 207 that is connected to the data signal DQ TSV715 ("*the second die interconnects*"), on one hand, and to a corresponding external data terminal of the control chip 20 through which the corresponding data is transmitted, on the other hand.

582. The claim also requires that the "*second data conduits*" are coupled to the same "*data terminals*" as the "*first data conduits*." Such an arrangement of external data terminals in the control chip of Riho would have been obvious to a Skilled Artisan in view Rajan. *See, e.g.*, *supra* ¶¶137-139 (rank multiplication), 503-512 (obviousness of combining Rajan and Riho, including emulating different number of ranks). For example, a Skilled Artisan would have been motivated to implement a 32-bit wide or narrower JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC

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standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory."); *see also id.* at Fig. 18 (reproduced below, disclosing that an interface circuit includes emulation logic which interfaces with the host system on one side and with the physical memory circuits on the other side, similar to Riho's logic control circuit 203, illustrated above).

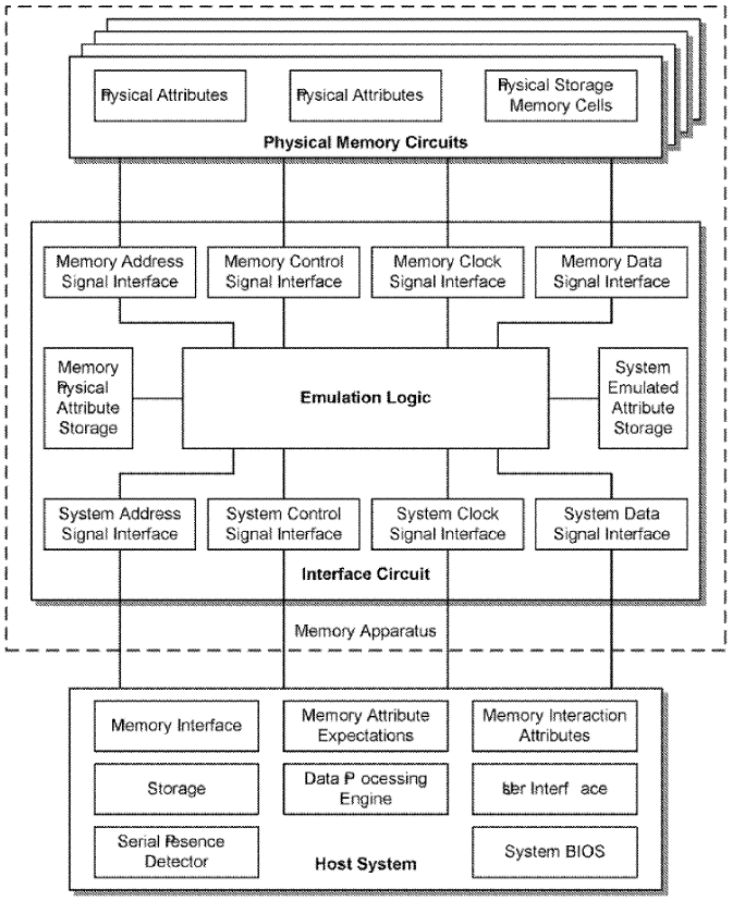


FIG. 18

583. For the reasons discussed above, a Skilled Artisan would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system. *Supra* ¶¶503-512. Rajan discloses the same basic structure of a memory package as Riho and the 160 Patent: the package includes stacked memory chips and a common interface circuit, called "buffer chip" in Rajan. Ex. 1015 at Fig. 4 (reproduced below, annotated), 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses.").

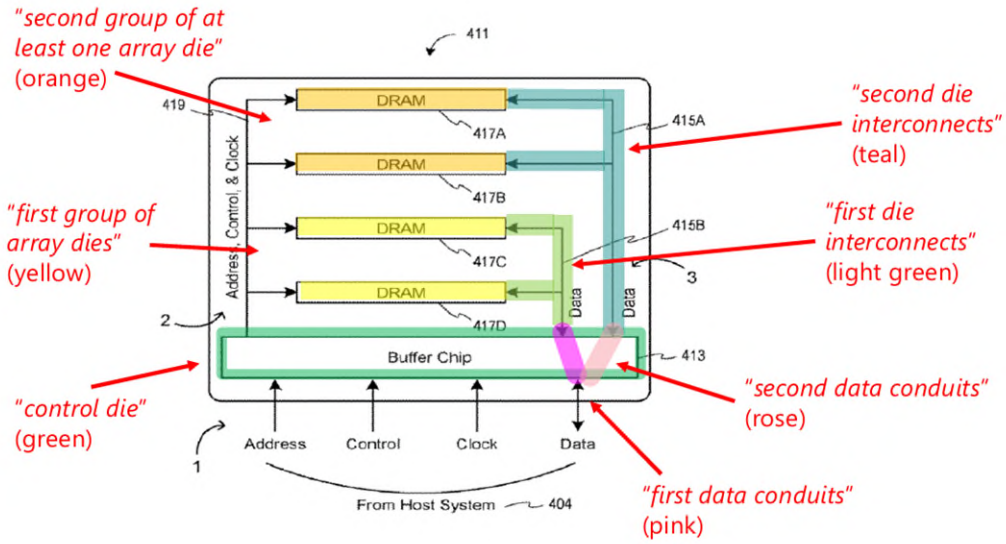


FIG. 4

584. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface

circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."), 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35.

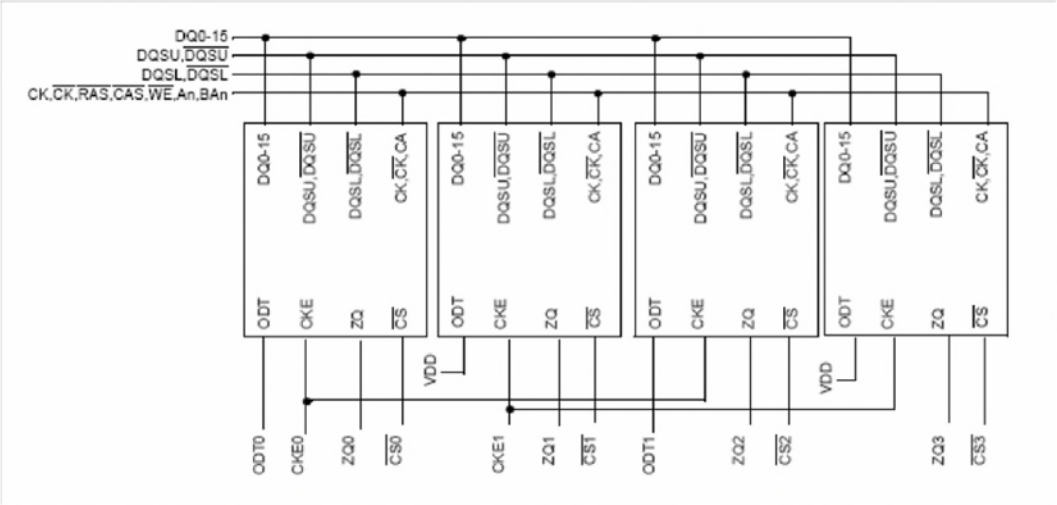


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

585. As discussed above, a Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control, and data terminals according to the JEDEC standards in Riho's memory packages to use the packages in JEDEC compliant systems. *Supra* ¶¶503-512. For example, Rajan teaches that the "interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory." Ex. 1015 at 3:52-54. A Skilled Artisan would have understood that a DDR3 SDRAM memory interface can include 4, 8, or 16 data terminals, and a GDDR3 memory can include 32 data terminals. *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.12-14 (describing pin-out for stacked DDR3 memory devices, Fig. 3 for x16 devices reproduced above); *see also* Ex. 1035 (JEDEC GDDR4 SGRAM Specification) at 2 ("The purpose of this Specification is to define the minimum set of requirements for JEDEC standard compatible 256 Mb through 1 Gb x32 GDDR4 SGRAM devices."). Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the admitted prior art referenced in the 160 Patent. *See, e.g.*, Ex. 1001 (the 160 Patent) at 22:22-24 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537).

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586. A Skilled Artisan would have understood that, in the combination of Riho and Rajan, where the memory package has, e.g., 32 external data terminals, those external data terminals would be connected to "[e]ach input/output circuit 207 [which] sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15." Ex. 1016 (Riho) at [0040]. That is, because the internal data communication between a given memory chip and the control chip happens on 32 parallel TSVs, those TSVs of each memory chip would be connected to the external 32 data terminals in order to communicate the data on the 32 data signal DQ TSVs.

587. Therefore, the combination of Riho and Rajan at least renders obvious that that the "*second data conduits*" are coupled to the same "*data terminals*" as the "*first data conduit*."

588. Accordingly, the prior art references in Ground 2 satisfy "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

(3) [1.e.4] and [1.e.5] First and Second Drivers

589. Claim 1 requires "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured*

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to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size."

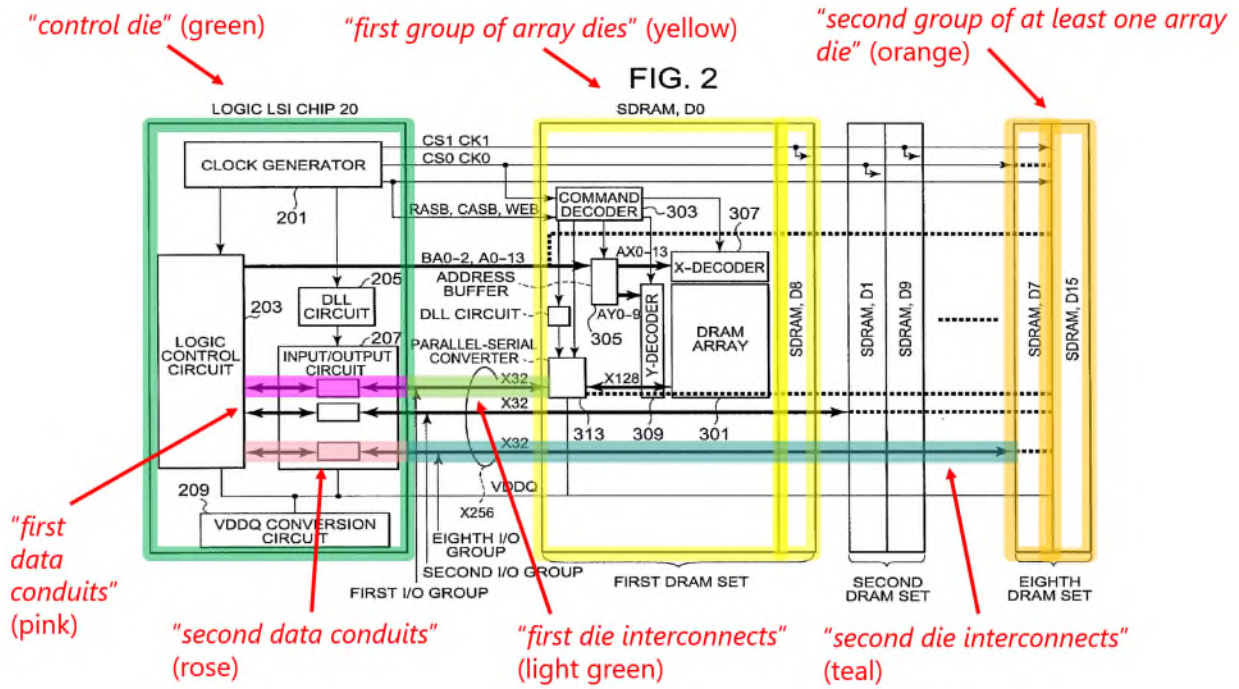
590. As previously noted, these claim limitations, as written, lack proper antecedent basis for the terms "*the first data conduit*" and "*the second data conduit*," since claim elements [1.e.2] and [1.e.3] recite "*first data conduit**s***" and "*second data conduit**s***," making it unclear which of these plural "*conduit**s***" the singular terms "*the first data conduit*" and "*the second data conduit*" refer to. *Supra* at ¶253. In any event, my analysis below shows that each of the "*first data conduits*" and "*second data conduits*" can include one or more drivers, *infra* ¶603, thus rendering this limitation obvious either way despite its ambiguity.

591. Riho discloses and renders obvious to a Skilled Artisan "*the first data conduit* [(pink)] *including first drivers* [in input/output circuit 207] *each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies* [including SDRAM chips D0 and D8]."

592. For example, Riho discloses that input/output circuit 207 includes buffers "*to drive a data signal from a corresponding data terminal to the first group of array dies*" that includes SDRAM chips D0 and D8. Ex. 1016 at [0045] ("The input/output circuit 207 includes interface circuits such as buffers corresponding to the SDRAM chips, respectively, so that data signals DQ are sent

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and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit. … That is, the data signal DQ TSVs for the SDRAM D0 are commonly used by the first DRAM set (SDRAM D0 and SDRAM D8).”), Fig. 2 (reproduced below, annotated); *see also id.* at [0040].



593. A Skilled Artisan would have understood from this disclosure that buffers in the input/output circuit 207 include “*first drivers each having a first driver size*” to drive the data signals to the first DRAM set including D0 and D8. *Supra* at ¶¶134-136; *see, e.g.*, Ex. 1030 (Brown) at 135-136 (“In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices. Buffers can handle relatively large amounts of current flow because they are built with large transistors.”). As

discussed above with reference to claim element [1.b], a Skilled Artisan would have understood that those data signals were received from an external device at the data terminals of the control chip 20. *Supra* ¶¶530-537.

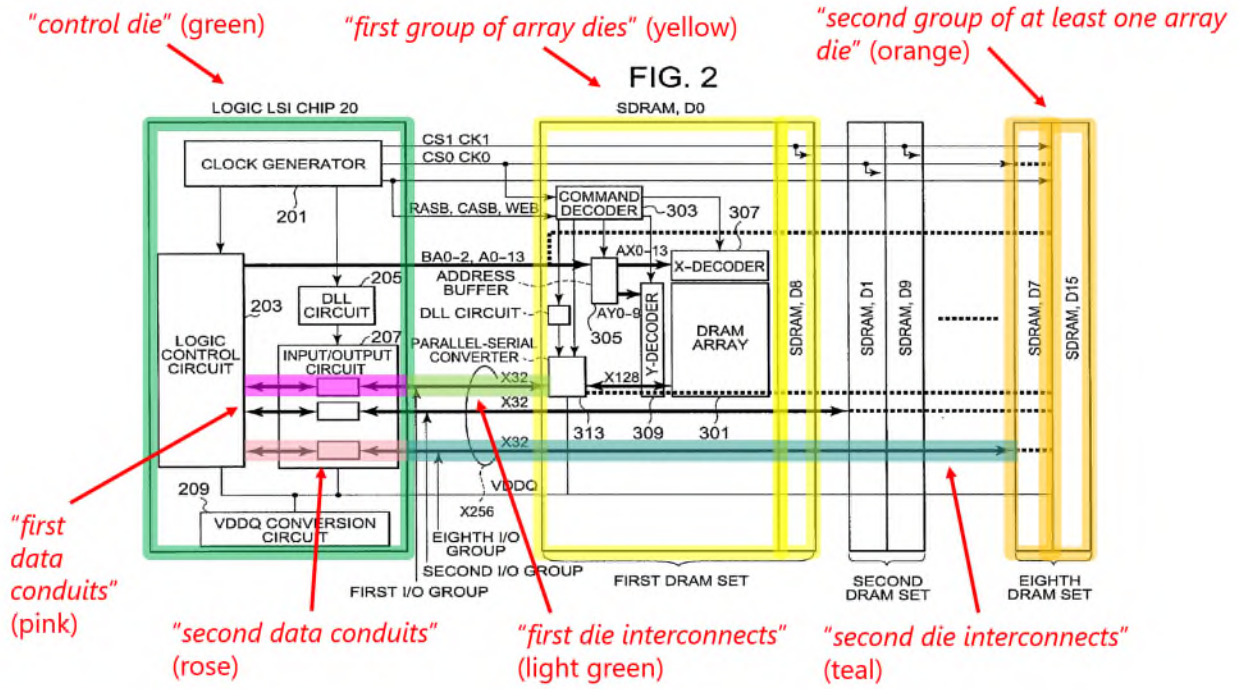
594. Therefore, Riho discloses and renders obvious "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*" to a Skilled Artisan.

595. Riho in combination with Riho2 renders obvious to a Skilled Artisan "*the second data conduit* [(rose)] *including second drivers* [in input/output circuit 207] *each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die* [including SDRAM chips 7 and 15]*, the second driver size being different from the first driver size.*"

596. For example, Riho discloses that input/output circuit 207 includes buffers "*to drive a data signal from a corresponding data terminal to the second group of at least one array die*" that includes SDRAM chips D7 and D15. Ex. 1016 at [0046] ("The data signal DQ TSVs for the SDRAM D7 are provided between the input/output circuit 207 of the logic LSI chip 20 and the SDRAM D7. The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are

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commonly used by the SDRAMs D7 and D15."), Fig. 2 (reproduced below, annotated); *see also id.* at [0040].



597. As discussed above with reference to the "*first data conduit including first drivers*," a Skilled Artisan would have understood from this disclosure that buffers in the input/output circuit 207 include "*second drivers each having a second driver size*" to drive the data signals to the second DRAM set including D7 and D15.

598. Riho further explains that "[i]t is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in manufacturing processes (TSV forming process, bump forming process, and TSV-

bump connection process). That is, TSVs formed in different manufacturing processes may have different impedances due to manufacturing variations in the manufacturing processes." Ex. 1016 (Riho) at [0055]. Riho further explains that "it is also preferable to expect that when a plurality of signal lines are formed by a plurality of TSVs, the impedance of each signal line may be different from those of the others due to variations of inherent manufacturing processes." *Id.* at [0056]. For example, Riho describes that "the SDRAM chip located closer to the logic LSI chip 20 has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip 20 has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process." *Id.* at [0061].

599. A Skilled Artisan would have understood from this disclosure that differences in impedances and other variations in the through silicon vias and the different positions of the SDRAM chips should be taken into account when designing the stacked structure of Riho.

600. Riho2 discloses that, in a case where "it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip

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dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another … , a configuration is provided to optimize the output drive capacity of output buffers according to the number of stacked chip dies." Ex. 1018 at [0096]. For example, Riho2's "FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097], Fig. 7A (reproduced below).

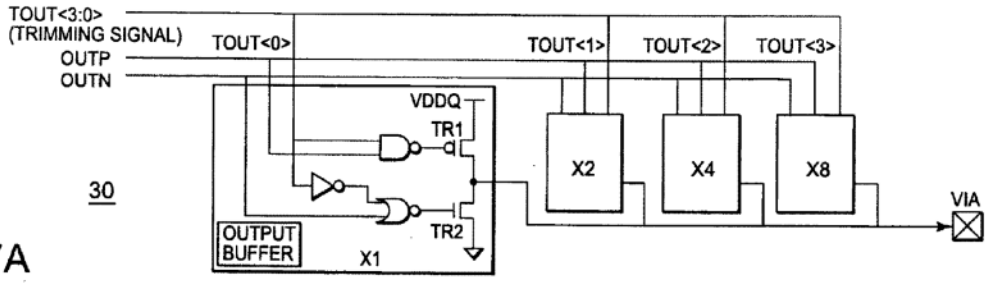


FIG. 7A

601. Therefore, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho, because Riho also discloses differences in impedances and resistances for the different data signal DQ TSVs. As a result of such optimization, "*the second driver size … [would be] different from the first driver size.*"

602. As discussed above, a Skilled Artisan would have also been motivated to look at Riho2 to address the issues created by the variations in the TSV properties described by Riho and to optimize the output drive capacity of output

buffers as taught by Riho2. *Supra* ¶¶503-522. A Skilled Artisan would have also understood that such an optimization of driver capacity would save power compared to using full-capacity drivers, which would be wasteful and inefficient. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.").

603. Making such a combination was well within the level of skill, since Riho2 itself teaches drivers of different sizes, and the combination would have provided nothing more than expected: a power efficient drive of signals through Riho's TSVs to different DRAM sets. For example, Riho2 discloses a circuitry that includes multiple drivers which are selectively activated to achieve the optimal driving strength. Ex. 1018 (Riho2) at [0096-97] ("FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In the example shown here, there are provided four output buffers X1, X2, X4, and X8 having mutually different drive capacities (the numerical values following the letter "X" indicate capacity ratios)."), Fig. 7A (reproduced below).

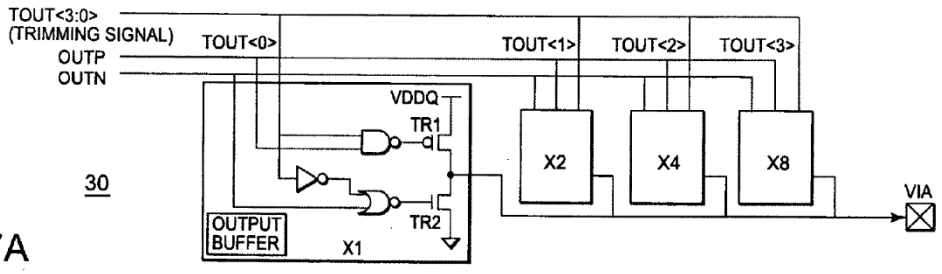


FIG. 7A

See also Ex. 1017 (Wyman) at Fig. 5 and 5:11-14 ("Similar to FIG. 2 through FIG. 4, a designer may now utilize and tap-off at five locations (506-1, 506-2, 506-3, 506-4, 508) depending on the drive requirements for a specific element or device.")

604. Indeed, compensating the driver strength for different positions of a die in a stack was well known at the time. *See, e.g.*, Ex. 1039 (Ma (U.S. Patent No. 9,160,349)) at Abstract ("In other embodiments, for example, differences in the termination impedance or driver drive-strength resulting from differences in the location of a die in a stack may be compensated for."), 7:46-49 ("One embodiment of a compensation circuit 400 that may compensate for both termination impedance and drive strength variations resulting from differences in die location is shown in FIG. 6."), and Fig. 6 (reproduced below).

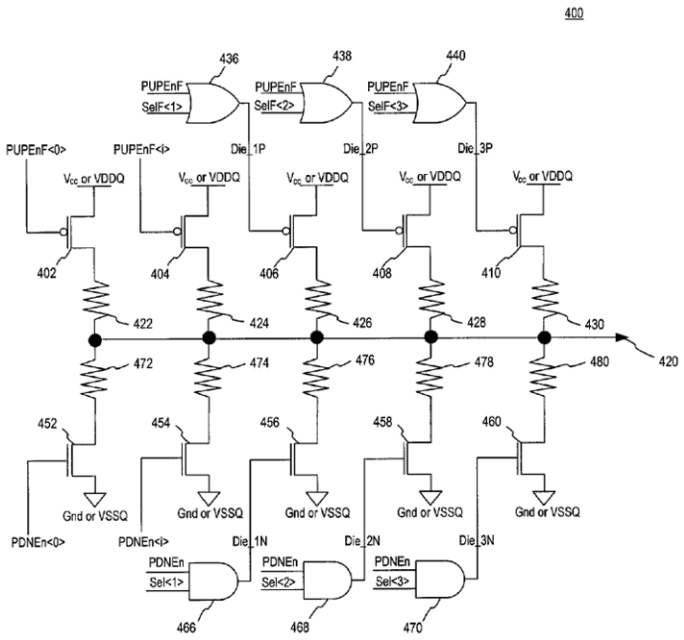


Figure 6

605. Therefore, the combination of Riho and Riho2 renders obvious this limitation to a Skilled Artisan.

606. Accordingly, the prior art references in Ground 2 satisfy "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size*."

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2. Claim 2 is Unpatentable

607. Claim 2 is unpatentable as the prior art references in Ground 2 render the claim obvious.

608. Claim 2 requires "*[t]he memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size*."

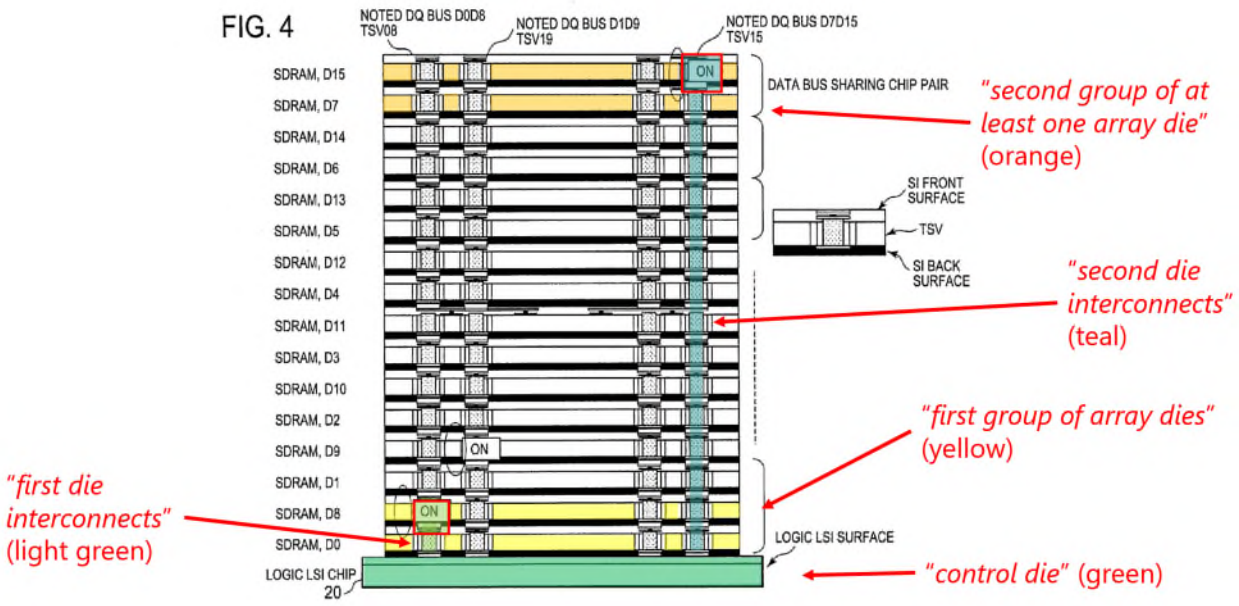
609. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

610. Netlist has asserted that TSVs which have equal length but the connected dies are in different locations in the stack satisfy the limitation of "*the second die interconnects are longer than the first die interconnects.*" Ex. 1044 (Netlist's Amended Complaint) at p.68 ("The second driver size is different from the first driver size, for example, to account for the different distances data signals have to travel to reach the respective array dies in the stack.").

611. Under such an interpretation, Riho discloses that "*the second die interconnects* [TSV715 (annotated teal below)] *are longer than the first die interconnects* [TSV08 (annotated light green below)]," because the SDRAM chips D7 and D15 coupled to TSV715 are farther away from the control chip 20 than the SDRAM chips D0 and D8 coupled to TSV08. *See, e.g.*, Ex. 1016 (Riho) at Fig. 4 (reproduced below annotated, showing that SDRAM chips D0 and D8 coupled to

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TSV08 are closest to control chip 20, and SDRAM chips D7 and D15 coupled to TSV715 are farthest from control chip 20).



612. Furthermore, as discussed above with reference to claim elements [1.d.1] and [1.d2], it would have been obvious to a Skilled Artisan to follow the teaching of Rajan for the data interconnection of dies in the stack of Riho. *Supra* at ¶¶558-562, *see also* Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated).

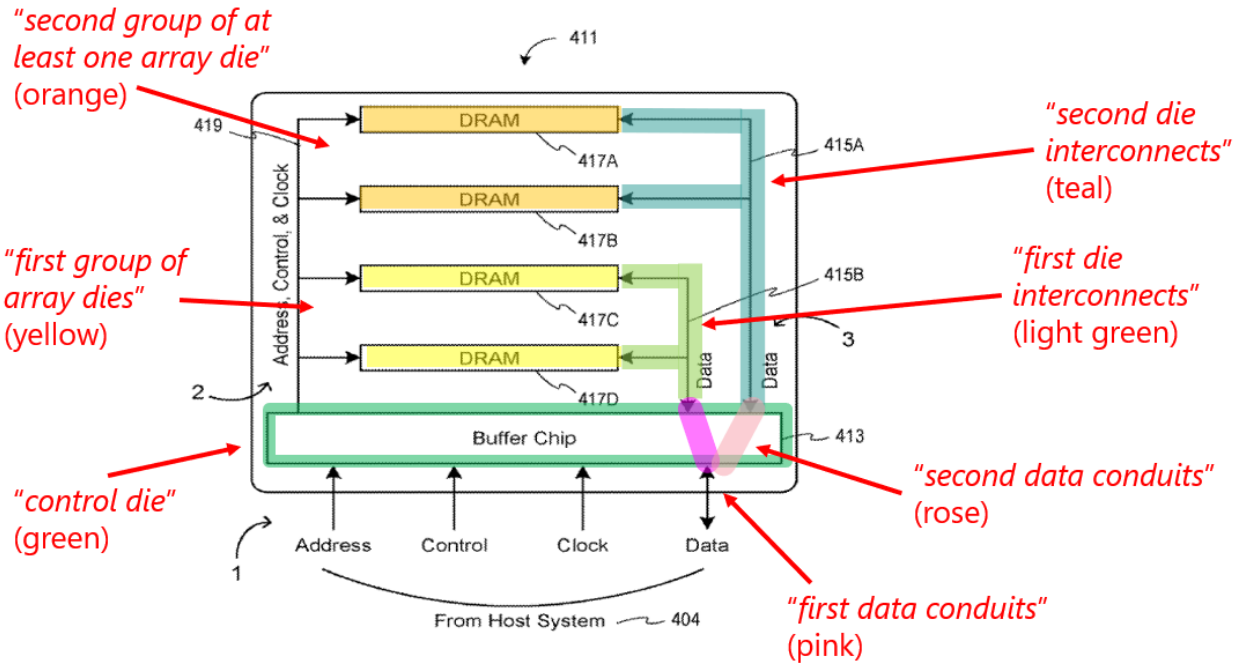


FIG. 4

613. As illustrated in Fig. 4 of Rajan, the second die interconnects (teal) are longer than the first die interconnects (light green). A Skilled Artisan would have understood that, by using shorter die interconnects for the first group of memory devices as taught by Rajan, the load on those die interconnects is advantageously reduced. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use shorter die interconnects for array dies that are closer to the control die in the stack of Riho in order to further reduce the load on those die interconnects. Such an arrangement would have advantageously reduced the driver size and corresponding power consumption in the stack of Riho.

614. In addition, as discussed above with reference to claim limitation [1.e.5], a Skilled Artisan would have understood that the farther away the SDRAM is from the control chip, the larger the "penetrating through resistance." *Supra* ¶¶595-606; Ex. 1016 (Riho) at [0061] ("As is clear from FIG. 3, the SDRAM chip located closer to the logic LSI chip 20 has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip 20 has a larger penetrating through resistance."). As also discussed above with reference to claim limitation [1.e.5], Riho2 teaches a Skilled Artisan to compensate for the variations in resistance. *Supra* ¶¶595-606; Ex. 1018 (Riho2) at [0097] ("FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance."). Furthermore, a Skilled Artisan would have understood that a larger resistance is compensated by a larger driver size. *See*, *e.g.*, Ex. 1039 (Ma) at 8:21-48 ("If the compensation circuit 400 is on the die closest to the substrate … transistors 406-410 or 456-460 are not turned ON. One the other hand, … if the compensation circuit 400 is on die #3, … all 5 transistors 402-410 are turned ON to drive the output terminal 420 high or all 5 transistors 452-460 are turned ON to drive the output terminal 420 low."); *see also* Ex. 1017 (Wyman) at 6:15-30 ("The increased resistance, capacitance and impedance of such a connection (804) might require additional drive …").

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615. Therefore, Riho in combination with Rajan and Riho2 renders obvious to a Skilled Artisan that *"the second driver size is larger than the first driver size.*"

616. Accordingly, the prior art references in Ground 2 satisfy "*wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size*" limitation.

3. Claim 3 is Unpatentable

617. Claim 3 is unpatentable as the prior art references in Ground 2 render the claim obvious.

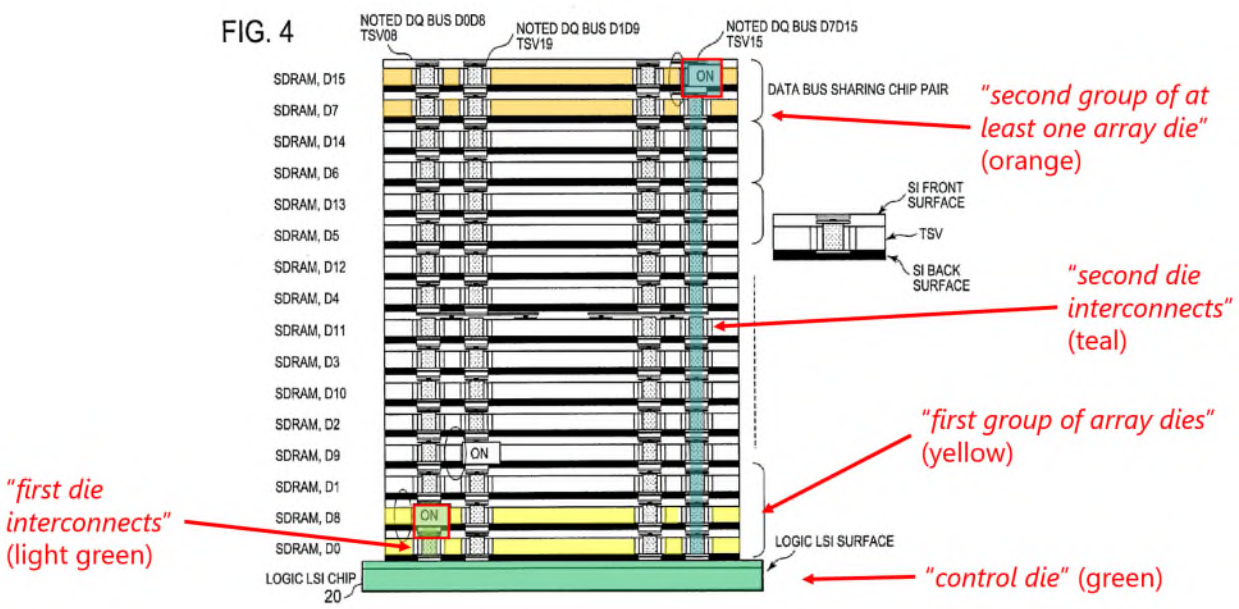
a) [3.a] Second Die Interconnects are Longer than First Die Interconnects

618. Claim 3 requires "*[t]he memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects*."

619. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

620. As discussed above with reference to claim 2, under Netlist's interpretation, Riho discloses that "*the second die interconnects* [TSV715 (annotated teal below)] *are longer than the first die interconnects* [TSV08 (annotated light green below)]." *See, e.g.,* Ex. 1016 (Riho) at Fig. 4 (reproduced below, annotated, showing that SDRAM chips D0 and D8 coupled to TSV08 are closest to control chip 20, and SDRAM chips D7 and D15 coupled to TSV715 are farthest from control chip 20).

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621. Therefore, Riho discloses this limitation.

622. Furthermore, as discussed above with reference to claim elements [1.d.1] and [1.d2], it would have been obvious to a Skilled Artisan to follow the teaching of Rajan for the data interconnection of dies in the stack of Riho. *Supra* at ¶¶558-562, *see also* Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated).

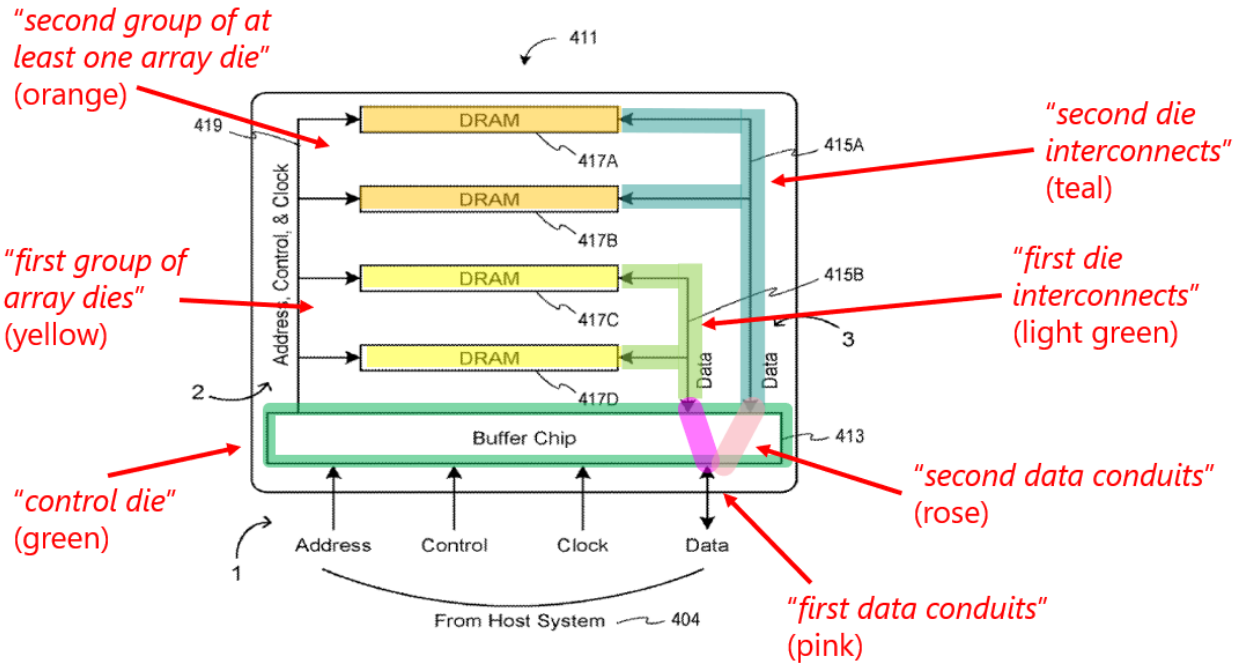


FIG. 4

623. As illustrated in Fig. 4 of Rajan, the second die interconnects (teal) are longer than the first die interconnects (light green). A Skilled Artisan would have understood that, by using shorter die interconnects for the first group of memory devices as taught by Rajan, the load on those die interconnects is advantageously reduced. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use shorter die interconnects for array dies that are closer to the control die in the stack of Riho in order to further reduce the load on those die interconnects. Such an arrangement would have advantageously reduced the driver size and corresponding power consumption in the stack of Riho.

624. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the second die interconnects are longer than the first die interconnects*" limitation.

b) [3.b] Number of Array Dies in the Second Group is Less Than Number of Array Dies in the First Group

625. Claim 3 also requires "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*."

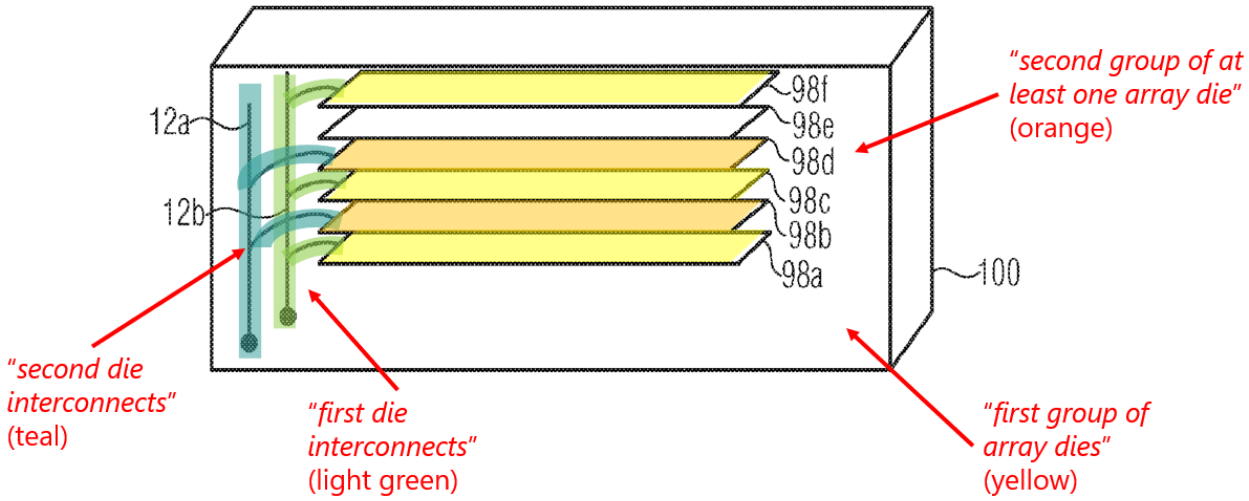
626. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

627. Riho in combination with Rajan renders obvious that "*a number of array dies in the second group of at least one array die* [coupled to TSV715] *is less than a number of array dies in the first group of array dies* [coupled to TSV08]."

628. For example, Riho explains that, "[i]t is apparent that the basic technical idea of this invention is not limited to the above-mentioned embodiments but may be modified and changed without departing from the scope and spirit of this invention. For example, although only the SDRAM chips are described in the embodiments, this invention is not limited thereto." Ex. 1016 (Riho) at [0135]. For example, "it may be a system in which DRAM chips and NAND flash memory chips are controlled by a single master chip." *Id*. at [0136]. Furthermore, Rajan discloses that, in a memory stack, "the memory circuits may be symmetrical,

meaning each has the same capacity, type, speed, etc., while in other embodiments they may be asymmetrical." Ex. 1015 (Rajan) at 2:62-65.

629. A Skilled Artisan would have understood from this disclosure that a memory stack can include memory chips of different types. A Skilled Artisan would have also understood that, in such an "asymmetrical" stack, different number of array dies can be coupled to a TSV for data transmission, depending on the specific types and arrangements of the memory chips. *See, e.g.*, Ex. 1024 (Ruckerbauer (US7,796,446)) at Fig. 5 (reproduced below, showing different number of dies coupled to different die interconnects) and 9:14-18 ("[W]ithin the memory stack 100, a first sub set of memory dies is coupled to the first transfer data path 12a and a second sub set is coupled to the second transfer data path 12b.").



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630. Therefore, a Skilled Artisan would have understood that the number of array dies in any given group is an obvious design choice, depending on the configuration and type of the memory chips in the stack. *See, e.g.*, Ex. 1024 (Ruckerbauer) at 8:58-66. For example, the number of dies in one group can be less than the number of dies in another group. *See, e.g.*, *Id*. at Fig. 5 (reproduced above, annotated).

631. Furthermore, a Skilled Artisan would have understood that the load on a given TSV increases with the length of the TSV and with the number of dies connected to the TSV (i.e., the longer the TSV and the greater the number of dies connected to the TSV, the larger the load on the TSV), and driving a signal on a TSV having larger load requires a larger driver which uses more power. *Supra* at ¶¶134-136. For example, Wyman explains that longer interconnects in a stacked arrangement require larger driving force and Riho2 discloses that differences in load result in timing differences. Ex. 1017 at 6:21-26 ("… a longer through-chip via connection …[with] increased resistance, capacitance and impedance of such a connection (804) might require additional drive"); Ex. 1018 at [0096] ("When the memory modules have mutually different numbers of stacked chip dies as in the first to fourth memory modules, it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves

(i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another.").

632. Therefore, in an asymmetric arrangement where TSVs of different lengths are connected to different number of dies, a Skilled Artisan would have been motivated to arrange the stack in a way that a longer TSV has fewer dies connected to it in order to reduce the power requirements of driving the longer TSV and to avoid timing differences (skew) due to differences in load. *See, e.g.*, Ex. 1017 (Wyman) at 2:61-65 ("Ultimately, instead of implementing a singular driver in the design phase, a designer need only supplement a few cascaded drivers in its place, thus allowing the designer to take full advantage of routing and which will ultimately result in power savings."); Ex. 1018 (Riho2) at [0050] ("In the illustrated structure, since the data signal DQ and data strobe signal DQS/B TSVs for all the DRAM sets corresponding to the respective I/O groups can be made substantially equal in length to each other, the skew between data signals DQ and data strobe signals DQS/B can be minimized.").

633. Accordingly, Riho in combination with Rajan renders obvious this limitation to a Skilled Artisan.

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634. Accordingly, the prior art references in Ground 2 satisfy the "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*" limitation.

4. Claim 4 is Unpatentable

635. Claim 4 is unpatentable as the prior art references in Ground 2 render the claim obvious.

636. Claim 4 requires "*[t]he memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*."

637. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

638. Riho in combination with Riho2 renders obvious to a Skilled Artisan that "*the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.*"

639. As discussed above with reference to claim limitation [1.e.5], it would have been obvious to use the different driver sizes of Riho2 to drive signals through the TSVs of different resistance and capacitance in the stack of Riho. *Supra* ¶¶595-606. A Skilled Artisan would have understood that these resistances and capacitances are related to the load on the respective driver. *Supra* ¶¶134-136; *see, e.g.*, Ex. 1018 (Riho2) at [0097] ("FIG. 7A shows a circuit configuration for

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optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance.").

640. Therefore, Riho in combination with Riho2 renders obvious this limitation to a Skilled Artisan.

641. Accordingly, the prior art references in Ground 2 satisfy "*wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver*."

5. Claim 5 is Unpatentable

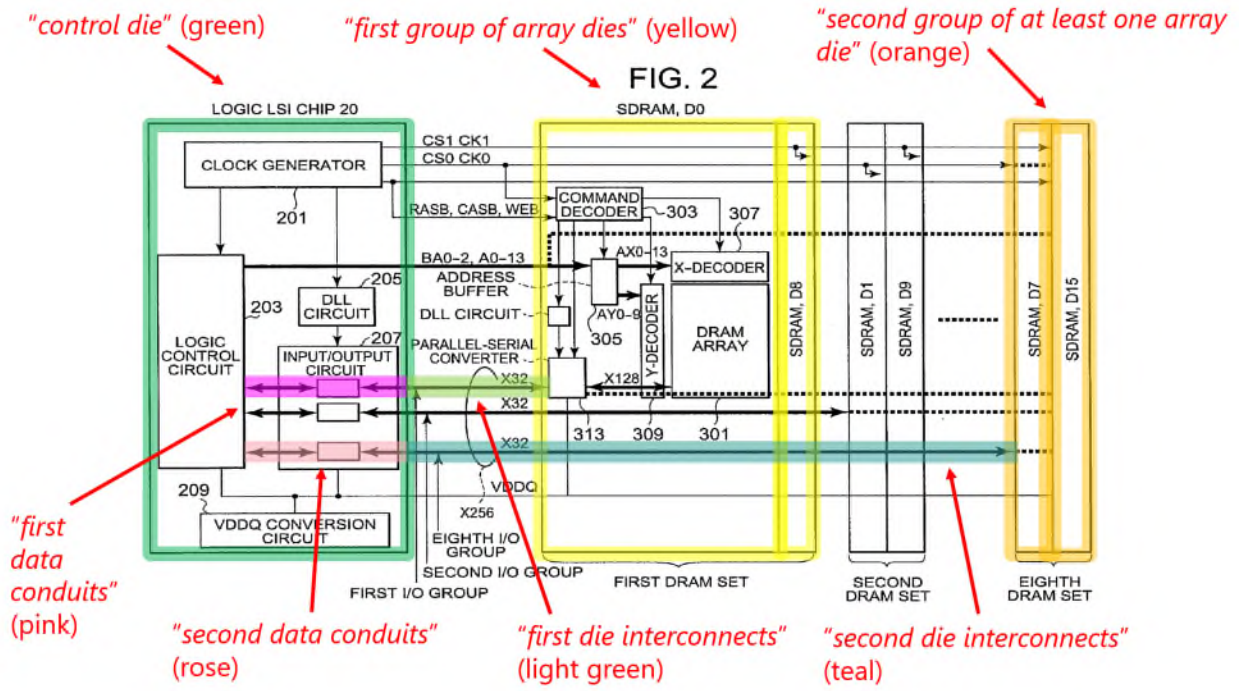
642. Claim 5 is unpatentable as the prior art references in Ground 2 render the claim obvious.

643. Claim 5 requires *"[t]he memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals*."

644. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

645. Riho discloses, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, that "*the control die* [control chip 20] *further comprises a control circuit* [including logic control circuit 203 and control circuit

in input/output circuit 207] *to control respective states* [for communicating data in the read or write direction] *of the first data conduits* [(pink) to SDRAMs D0 and D8 through DQ TSV08] *and the second data conduits* [(rose) to SDRAMs D7 and D15 through DQ TSV715] *in response to control signals* [including read and write command signals] *received via the control terminals* [from an external device]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



646. As discussed above, Riho discloses external terminals of its logic chip 20 and it would have been obvious at least in light of Rajan to have those external terminals receive address and control signals and control the memory chips in the stack based on those signals. *Supra* at ¶¶503-512. For example, Riho discloses that the "logic control circuit 203 provided in the logic LSI chip 20 outputs a 3-bit bank

address signal BA0-2 and a 14-bit address signal A0-13 and operates as a controller that sends and receives data signals DQ between itself and the input/output circuit 207." Ex. 1016 at [0039]. The input/output circuit 207 "sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively." *Id.* at [0040]. Moreover, the input/output circuit 207 "includes interface circuits such as buffers corresponding to the SDRAM chips, respectively, so that data signals DQ are sent and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit." *Id.* at [0045]. Riho further discloses that the "communications (read/write) of respective I/O groups are performed between the first control chip [i.e., logic LSI chip 20] and the second and third controlled chips [i.e., SDRAM chips]." *Id*. at [0053]; *see also* Ex. 1015 at 11:12-12:13, Fig. 14 (reproduced below, disclosing timing for forwarding commands to the memory devices during read and write operations); Ex. 1019 at 13, 23-24 ("CAS latency"), 33.

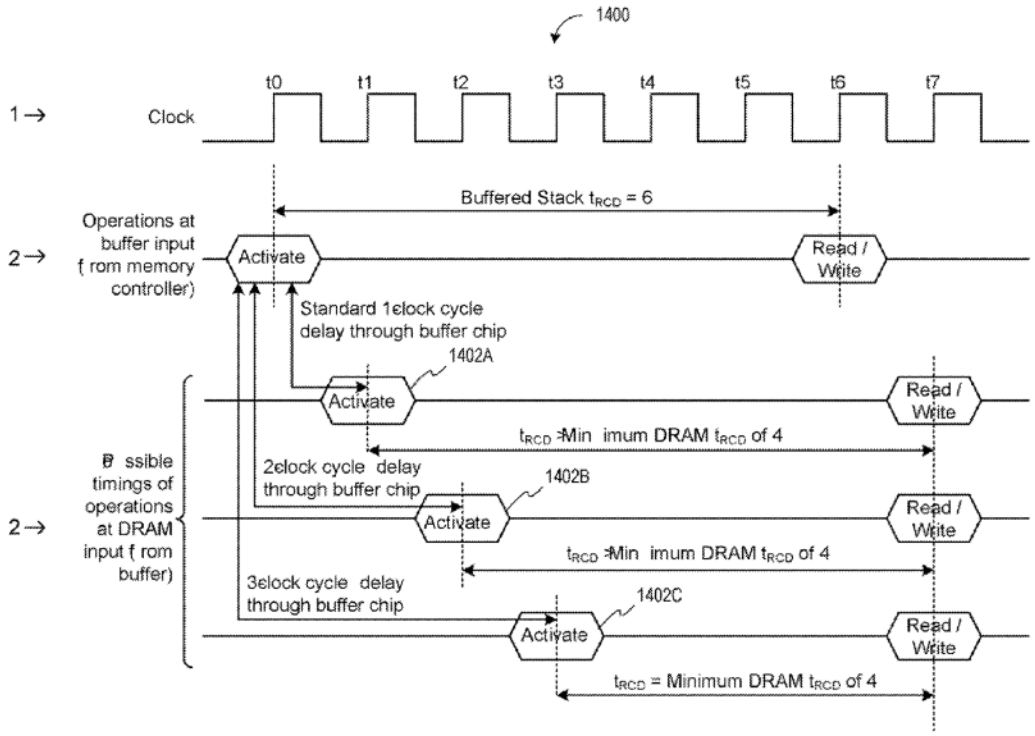


FIG. 14

647. A Skilled Artisan would have understood from this disclosure that the logic control circuit 203 and logic circuitry in input/output circuit 207 include a control circuit that receives control signals, including read and write command signals from an external device and, in response, controls the timing and direction of data transfer through the input/output circuit 207 to direct the data transfer selectively to or from DQ TSV08 through the "*first data conduits*" (pink) and to or from DQ TSV715 through the "*second data conduits*" (rose). Therefore, the state of those "*data conduits*" is controlled to be active or not active and to transmit data in the read or write direction.

648. Furthermore, as discussed above with reference to claim limitation [1.b], a Skilled Artisan would have understood that the read and write command signals are "*received via the control terminals*." *Supra* ¶¶530-537.

649. Therefore, Riho discloses this limitation to a Skilled Artisan.

650. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminal*" limitation.

6. Claim 6 is Unpatentable

651. Claim 6 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [6.a] Preamble

652. Claim 6 requires *"[a] memory package, comprising*."

653. To the extent the preamble is limiting, the prior art references in Ground 2 teach this limitation to a Skilled Artisan.

654. As shown in the table below, the preamble of claim 6 is identical to the preamble of claim 1:

Claim 1	**Claim 6**
[1.a] A memory package, comprising:	[6.a] A memory package, comprising:

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655. As discussed above with reference to the preamble of claim 1, to the extent the preamble of claim 1 is limiting, the prior art references in Ground 2 satisfy "*[a] memory package, comprising*." *Supra* ¶¶525-529.

b) [6.b] Data Terminals and Control Terminals

656. Claim 6 requires "*data terminals and control terminals*."

657. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

658. As shown in the table below, claim limitation [6.b] is identical to claim limitation [1.b]:

Claim 1	**Claim 6**
[1.b] data terminals and control terminals	[6.b] data terminals and control terminals

659. As discussed above with reference to claim limitation [1.b], the prior art references in Ground 2 satisfy "*data terminals and control terminals*." *Supra* ¶¶530-537.

c) [6.c] Stacked Array Dies

660. Claim 6 requires "*stacked array dies including a first group of array dies and a second group of at least one array die*."

661. As shown in the table below, claim limitation [6.c] is identical to claim limitation [1.c]:

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Claim 1	**Claim 6**
[1.c] stacked array dies including a first group of array dies and a second group of at least one array die	[6.c] stacked array dies including a first group of array dies and a second group of at least one array die

662. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 2 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶538-545.

d) [6.d.1] and [6.d.2] First and Second Die Interconnects

663. Claim 6 also requires "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

664. As shown in the table below, claim limitations [6.d.1] and [6.d.2] are identical to claim limitations [1.d.1] and [1.d.2], respectively:

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Claim 1	**Claim 6**
[1.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,	[6.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
[1.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[6.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

665. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 2 satisfy "*first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶546-563.

e) [6.e] Second Die Interconnects are Longer than the First Die Interconnects

666. Claim 6 requires "*wherein the second die interconnects are longer than the first die interconnects*."

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667. As shown in the table below, claim limitation [6.e] is nearly identical to claim limitation [3.a]:

Claim 3	Claim 6
[3.a] . . ., wherein the second die interconnects are longer than the first die interconnects, and	[6.e] wherein the second die interconnects are longer than the first die interconnects, and

668. As discussed above with reference to claim limitation [3.a], the prior art references in Ground 2 satisfy "*wherein the second die interconnects are longer than the first die interconnects*." *Supra* ¶¶618-624.

f) [6.f] Number of Array Dies in the Second Group is Less than Number of Array Dies in the First Group

669. Claim 6 also requires "*wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies*."

670. As shown in the table below, claim limitation [6.f] is identical to claim limitation [3.b]:

Claim 3	Claim 6
[3.b] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.	[6.f] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

671. As discussed above with reference to claim limitation [3.b], the prior art references in Ground 2 satisfy "wherein a number of array dies in the second

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group of at least one array die is less than a number of array dies in the first group of array dies." *Supra* ¶¶625-634.

7. Claim 7 is Unpatentable

672. Claim 7 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [7.a] A Control Die Comprising

673. Claim 7 requires *"[t]he memory package of claim 6, further comprising: a control die comprising*."

674. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

675. As shown in the table below, claim limitation [7.a] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 7**
[1.e.1] a control die comprising	[7.a] The memory package of claim 6, further comprising: a control die comprising

676. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 2 satisfy "*a control die comprising*." *Supra* ¶¶564-571.

b) [7.b.1] and [7.b.2] The First and Second Data Conduits

677. Claim 7 requires "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

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678. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

679. As shown in the table below, claim limitations [7.b.1] and [7.b.2] are identical to claim limitations [1.e.2] and [1.e.3], respectively:

Claim 1	**Claim 7**
[1.e.2] first data conduits between the first die interconnects and the data terminals, and [1.e.3] second data conduits between the second die interconnects and the data terminals,	[7.b.1] first data conduits between the first die interconnects and the data terminals, and [7.b.2] second data conduits between the second die interconnects and the data terminals,

680. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Ground 2 satisfy "*first data conduits between the first die interconnects and the data terminals*," and "*second data conduits between the second die interconnects and the data terminals*." *Supra* ¶¶572-588.

c) [7.c.1] and [7.c.2] First and Second Drivers

681. Claim 7 also requires "*the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at*

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least one array die, the second driver size being different from the first driver size."

682. As shown in the table below, claim limitations [7.c.1] and [7.c.2] are nearly identical to claim limitations [1.e.4] and [1.e.5]:

Claim 1	**Claim 7**
[1.e.4] the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [1.e.5] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.	[7.c.1] the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [7.c.2] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.

683. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], the singular "*first data conduit*" and "*second data conduit*" lack antecedent basis, but those limitations are obvious even if they are interpreted to be plural "*first data conduit**s***" and plural "*second data conduit**s***." *See supra* ¶590. Thus, the prior art references in Ground 2 satisfy "*the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data*

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conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size." *Supra* ¶¶589-606.

8. Claim 8 is Unpatentable

684. Claim 8 is unpatentable as the prior art references in Ground 2 render the claim obvious.

685. Claim 8 requires "*[t]he memory package of claim 7, wherein the second driver size is larger than the first driver size.*"

686. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

687. As shown in the table below, claim 8 is very similar to claim 2:

Claim 2	**Claim 8**
[2] The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size.	[8] The memory package of claim 7, wherein the second driver size is larger than the first driver size.

688. As discussed above with reference to claim 2, the prior art references in Ground 2 satisfy "*wherein the second driver size is larger than the first driver size*." *Supra* ¶¶607-616.

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9. Claim 9 is Unpatentable

689. Claim 9 is unpatentable as the prior art references in Ground 2 render the claim obvious.

690. Claim 9 requires "*[t]he memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.*"

691. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

692. As shown in the table below, claim 9 is very similar to claim 5:

Claim 5	**Claim 9**
[5] The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.	[9] The memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.

693. As discussed above with reference to claim 5, the prior art references in Ground 2 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals*." *Supra* ¶¶642-650.

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694. The phrase "*the plurality of terminals*" lacks antecedent basis, but a Skilled Artisan would have understood that the "*control terminals*" from claim element [6.b] could also be "*one or more second terminals of the plurality of terminals*," the plurality of terminals including both the "*data terminals*" and the "*control terminals*" from [6.b]. *Supra* ¶¶656-659 (citing ¶¶530-537).

695. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals*" limitation.

10. Claim 10 is Unpatentable

696. Claim 10 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [10.a] Preamble

697. The preamble of claim 10 requires "*[a] memory module operable in a computer system with a system memory controller, comprising*."

698. To the extent the preamble is limiting, the prior art references in Ground 2 teach this limitation to a Skilled Artisan.

699. The combination of Riho and Rajan discloses a "*memory module operable in a computer system with a system memory controller.*"

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700. As discussed above, it would have been obvious to combine the teaching of Riho and Rajan. *Supra* ¶¶503-512. For example, Riho discloses that stacked memory devices can be used in a memory module. Ex. 1016 at [0003-4]. Rajan discloses a "*memory module*," such as a DIMM, that includes stacked memory devices. *See, e.g.*, Ex. 1015 at Fig. 8 (reproduced below), 8:52-54 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804….").

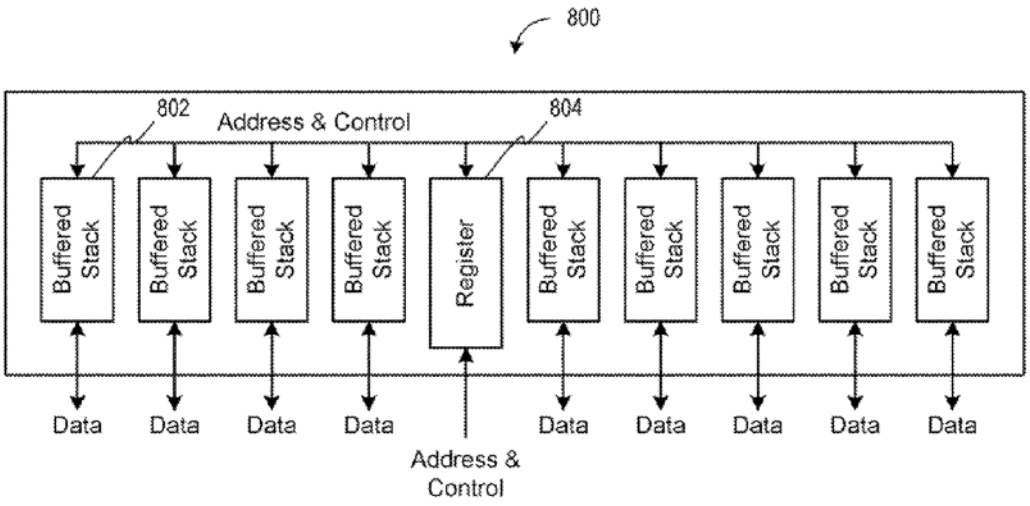


FIG. 8

701. Riho also discloses stacked memory devices. Ex. 1016 at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips.").

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702. As discussed above, a Skilled Artisan would have understood and been motivated to implement Riho's stacked memory devices in a memory module as disclosed by Rajan. *Supra* ¶¶503-512; *see, e.g.*, Ex. 1015 (Rajan) at 1:28-32 ("In other systems, groups of memory chips are first coupled into memory modules, such as dual in-line memory modules (DIMMs), which are in turn coupled into a system by means of slots, sockets, or other connectors."), 15:3-12 ("The physical memory circuits employed in practicing this invention may be any type of memory whatsoever … The physical memory circuits may be coupled to any type of memory module…"). For example, a Skilled Artisan would have been motivated to implement Riho's stacked devices in a DIMM format so that it can be used in systems that include sockets for DIMMs.

703. Rajan further explains that its "system may include a memory controller (not shown) through which it accesses the memory circuits," Ex. 1015 at 3:5-7, and that "[t]he system device which accesses the memory may be any type of system device, such as: desktop computer, laptop computer, workstation, server, consumer electronic device, television, personal digital assistant (PDA), mobile phone, printer or other peripheral device, etc.," *id.* at 15:13-17.

704. A Skilled Artisan would have understood from this disclosure that the "*memory module* [is] *operable in a computer system with a system memory controller*." *See, e.g.*, Ex. 1037 (Rothman) at Fig. 1, 1:34-39 ("FB-DIMMs can be

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connected via high speed serial interfaces to a Memory Controller Hub (MCH). The AMB communicates with the MCH via the high speed serial interfaces and with RAM ICs on the DIMM via the internal memory bus. The AMB reads from and writes to the RAM as instructed by the MCH and can also be used to configure the FB-DIMM."); Ex. 1022 at 315-20, Figure 7.2 (annotated below) ("Figure 7.2 illustrates [as of 2008] DRAM's place in a typical PC. An individual DRAM device typically connects indirectly to a CPU (i.e., a microprocessor) through a memory controller"), Figure 7.6 ("JEDEC style memory bus organization"). A Skilled Artisan would also know that the memory controller could be integrated into the CPU package (to the left in the figure below) rather than in a separate chip (as shown below); both were known options at the time.

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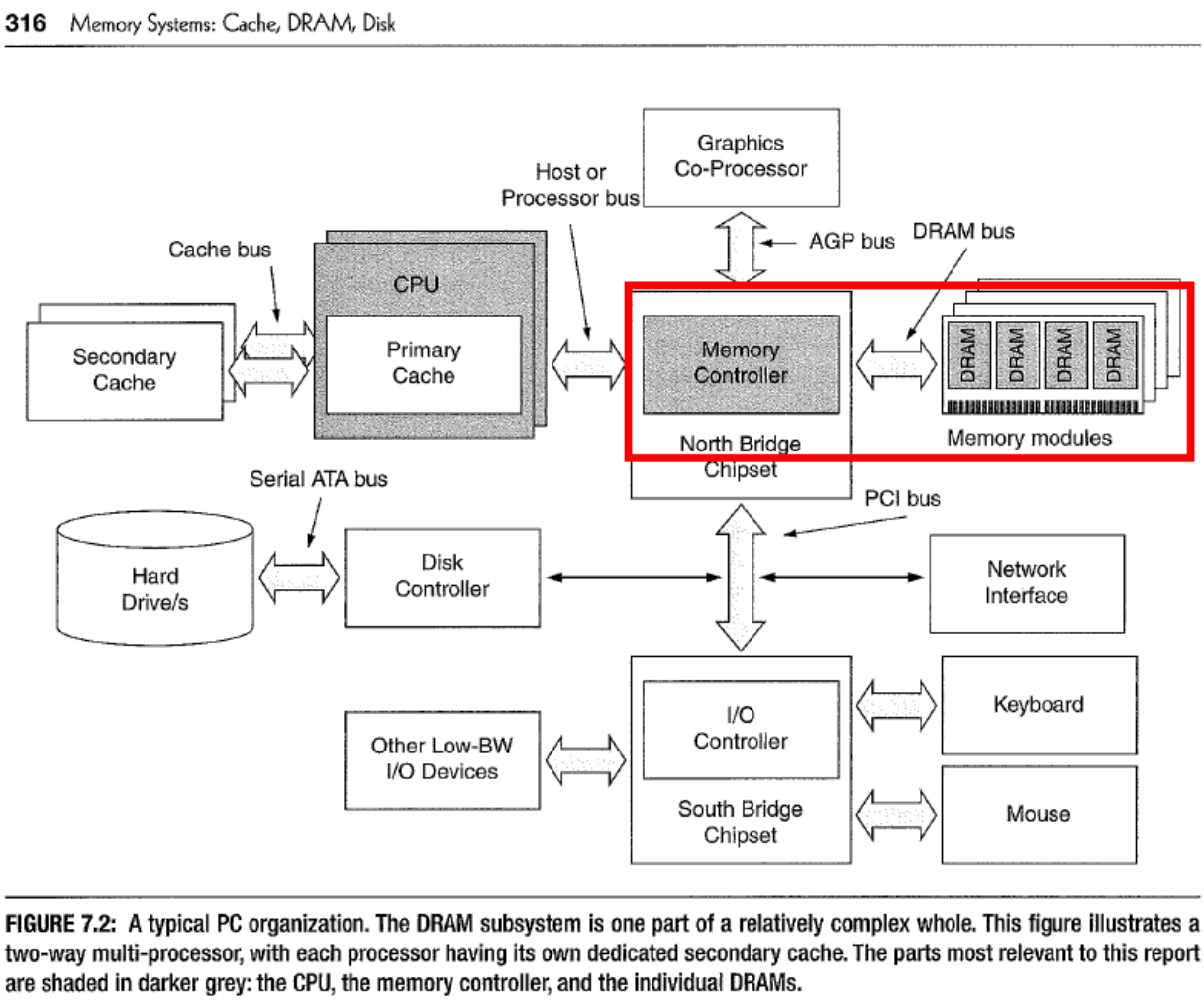


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

705. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

706. Accordingly, the prior art references in Ground 2 satisfy "*[a] memory module operable in a computer system with a system memory controller, comprising*."

b) [10.b] A Register Device

707. Claim 10 requires "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*."

708. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

709. The combination of Riho and Rajan discloses "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*."

710. For example, Rajan discloses a register 804 that receives command/address signals from the memory controller and outputs address and control signals to the buffered stacks. Ex. 1015 at Fig. 8 (reproduced below, showing the register receiving "Address & Control" signals per the JEDEC standard, *id.* at 4:20-24, would include command signals, *see* Ex. 1019 at 13, 33; Ex. 1023 at 9, Fig.16; Ex. 1022 at 318-20); Ex. 1015 at 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level."); *see*

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also Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"), 43-44 ("Fully Buffered DIMM," "FB-DIMM," "Advanced Memory Buffer," "AMB").

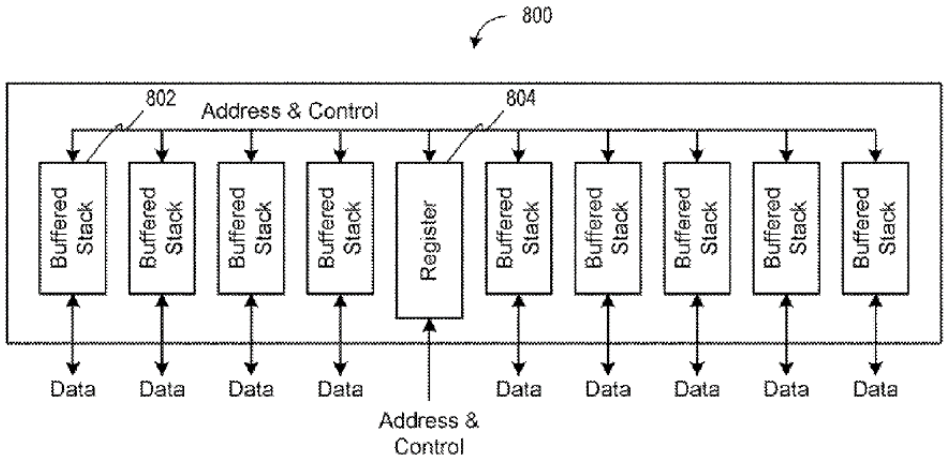


FIG. 8

711. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

712. Accordingly, the prior art references in Ground 2 satisfy the "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*" limitation.

c) [10.c] Plurality of DRAM packages

713. Claim 10 requires "*a plurality of DRAM packages, each DRAM package comprising*."

714. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

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715. The combination of Riho and Rajan discloses a memory module including "*a plurality of DRAM packages*," such as buffered stacked DRAM circuits. Ex. 1015 (Rajan) at Fig. 8 (reproduced below), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention."); *see also supra* ¶¶525-529 (claim limitation [1.a], discussing relevant disclosure by Riho); Ex. 1022, at 315, 374 (DRAM "packages").

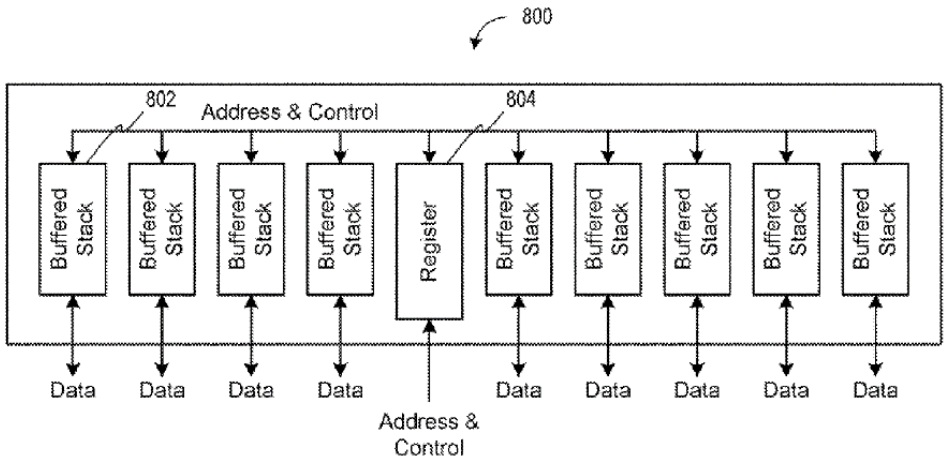


FIG. 8

716. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

717. Accordingly, the prior art references in Ground 2 satisfy the "*a plurality of DRAM packages, each DRAM package comprising*" limitation.

d) [10.d] Data Terminals

718. Claim 10 requires "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*."

719. As shown in the table below, claim limitation [10.d] is very similar to claim limitations [1.b] and [10.b]:

Claim 1	**Claim 10**
[1.b] data terminals and control terminals; [10.b] a register device configured … to output control signals	[10.d] data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device;

720. For the reasons discussed above with reference to claim limitations [1.b] and [10.b], the prior art references in Ground 2 satisfy "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*." *Supra* ¶¶530-537, 707-712.

721. As discussed above with reference to claim limitation [10.b], Rajan discloses a register 804 that sends "Address & Control" signals to the DRAM packages. Ex. 1015 at Fig. 8 (reproduced below), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits

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802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level.")

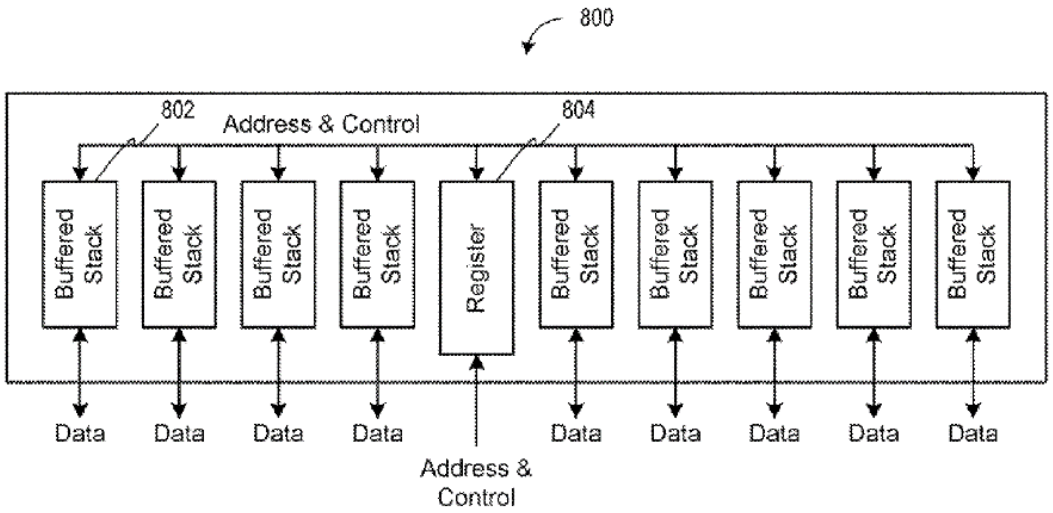


FIG. 8

As can also be seen in Fig. 8 above, Rajan discloses that each DRAM package communicates data signals with the system memory controller. Accordingly, it would have been obvious to a Skilled Artisan that the combination of Riho and Rajan includes data terminals via which the DRAM package communicates data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device. *See also* Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"); Ex. 1019 at 6-13 (JEDEC standard for terminals for data, address, and control).

722. Therefore, Riho and Rajan disclose and render obvious this limitation to a Skilled Artisan.

723. Accordingly, the prior art references in Ground 2 satisfy the "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*" limitation.

e) [10.e] Stacked Array Dies

724. Claim 10 requires "*stacked array dies including a first group of array dies and a second group of at least one array die*."

725. As shown in the table below, claim limitation [10.e] is identical to claim limitation [1.c]:

Claim 1	**Claim 10**
[1.c] stacked array dies including a first group of array dies and a second group of at least one array die;	[10.e] stacked array dies including a first group of array dies and a second group of at least one array die;

726. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 2 satisfy "*stacked array dies including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶538-545.

f) [10.f.1] and [10.f.2] First and Second Die Interconnects

727. Claim 10 requires "*die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical*

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communication with the first group of array dies and not in electrical communication with the second group of at least one array die," and "*the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

728. As shown in the table below, claim limitations [10.f.1] and [10.f.2] are nearly identical to claim limitations [1.d.1] and [1.d.2], respectively:

Claim 1	**Claim 10**
[1.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[10.f.1] die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [10.f.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

729. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 2 satisfy "*die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second*

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die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies." *Supra* ¶¶546-563.

g) [10.g] Control Die

(1) [10.g.1] A Control Die Including

730. Claim 10 requires "*a control die including*."

731. As shown in the table below, claim limitation [10.g.1] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 10**
[1.e.1] a control die comprising	[10.g.1] a control die including

732. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 2 satisfy "*a control die including*." *Supra* ¶¶564-571.

(2) [10.g.2] and [10.g.3] First and Second Data Conduits

733. Claim 10 requires "*first data conduits between the first die interconnects and data terminals*," and "*second data conduits between the second die interconnects and the data terminals*."

734. As shown in the table below, claim limitations [10.g.2] and [10.g.3] are identical to claim limitations [1.e.2] and [1.e.3], respectively:

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Claim 1	**Claim 10**
[1.e.2] first data conduits between the first die interconnects and the data terminals, and [1.e.3] second data conduits between the second die interconnects and the data terminals,	[10.g.2] first data conduits between the first die interconnects and data terminals, and [10.g.3] second data conduits between the second die interconnects and the data terminals,

735. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Ground 2 satisfy "*first data conduits between the first die interconnects and data terminals*," and "*second data conduits between the second die interconnects and the data terminals*." *Supra* ¶¶572-588.

h) [10.h.1] and [10.h.2] First and Second Drivers

736. Claim 10 requires "*the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size*," and "*the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die*."

737. As shown in the table below, claim limitations [10.h.1] and [10.h.2] is very similar to claim limitations [1.e.4] and [1.e.5]:

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Claims 1, 10	**Claim 10**
[1.e.4] the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [1.e.5] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size. [10.d] data terminals via which the DRAM package communicate data signals with the system memory controller…	[10.h.1] the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size, [10.h.2] the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die

738. As discussed above with reference to claim limitations [1.e.4] and [1.e.5], the singular "*first data conduit*" and "*second data conduit*" lack antecedent basis, but those limitations are obvious even if they are interpreted to be plural "*first data conduit**s***" and plural "*second data conduit**s***." *See supra* ¶590. Thus, the prior art references in Ground 2 satisfy "*the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies*," and "*the second data conduit including second drivers each having a second driver size and configured*

to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size." *Supra* ¶¶589-606.

739. As discussed above with reference to claim limitation [10.d], the prior art references in Ground 2 satisfy "*data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device*." *Supra* ¶¶718-723.

740. Accordingly, the prior art references in Ground 2 satisfy the "*the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size*," and "*the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die*" limitations.

11. Claim 11 is Unpatentable

741. Claim 11 is unpatentable as the prior art references in Ground 2 render the claim obvious.

742. Claim 11 requires "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to*

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control respective states of the first data conduits and the second data conduits in response to the control signals."

743. As shown in the table below, claim 11 is very similar to claim 5:

Claim 5	**Claim 11**
[5] The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.	[11] The memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals.

744. As discussed above with reference to claim 5, the prior art references in Ground 2 satisfy "*[t]he memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals*." *Supra* ¶¶642-650.

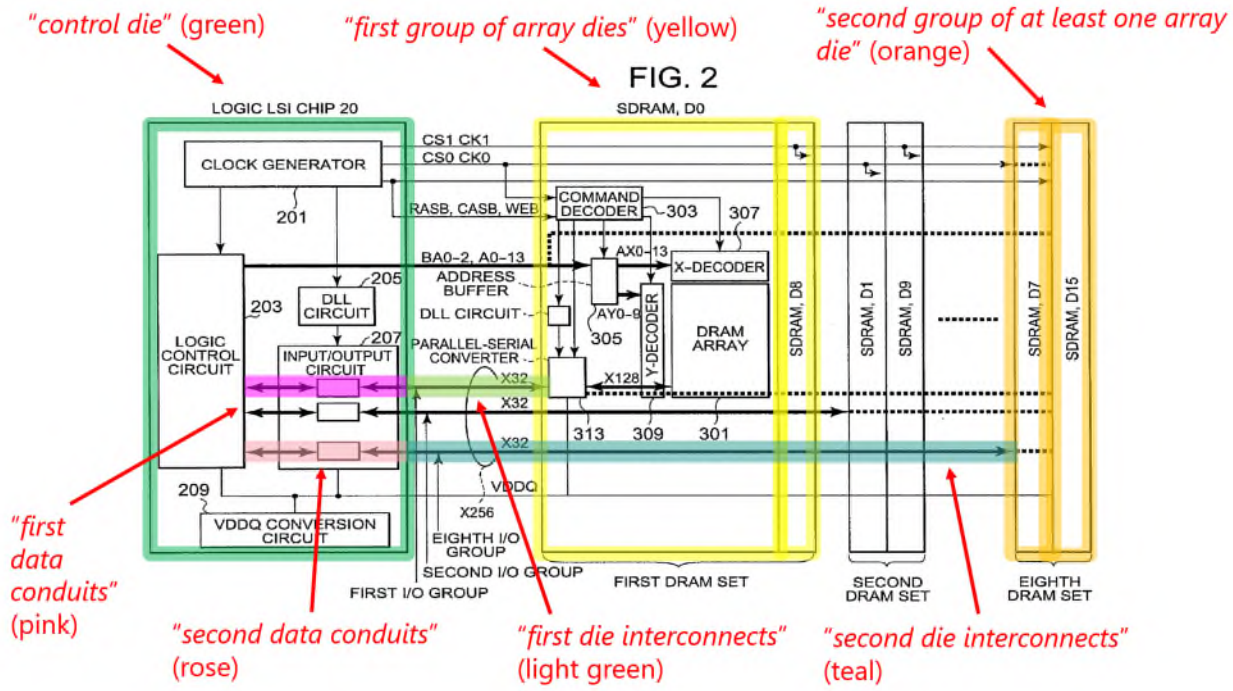
12. Claim 12 is Unpatentable

745. Claim 12 requires "*[t]he memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*."

746. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

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747. The combination of Riho and Rajan discloses to a Skilled Artisan that "*the control signals* [from the register device] *include data path control signals generated by the register device* [such as read and write command signals, including chip select signals], *the data path control signals being used to control the respective states of the first data conduits* [(annotated pink below)] *and second data conduits* [(annotated rose below)] [including controlling the timing and direction of the data transfer (read or write operations) and selectin the die(s) for the data transfer (in accordance with the chip select signals)]." *See, e.g.*, Ex. 1016 (Riho) at Fig. 2 (reproduced below, annotated).



748. For the reasons discussed above with reference to claim 5, Riho's logic control circuit 203 and input/output circuit 207 include a control circuit that

receives read and write commands from an external device and, in response, controls the direction and timing of the data transfer to or from DQ TSV08 through the "*first data conduits*" (pink) or to or from DQ TSV715 through the "*second data conduits*" (rose). *Supra* ¶¶642-650. A Skilled Artisan would have understood that the read and write command signals are "*data path control signals*," at least under Netlist's apparent interpretation, because they determine the direction and timing of the data transfer (read or write). *See, e.g.*, Ex. 1001 (the 160 Patent) at 19:17-21 ("The data path control circuit (e.g., ODT, read/write data direction)….").

749. Furthermore, in the combination of Riho and Rajan, the memory module can implement rank multiplication. *Supra* at ¶¶137-140, 503-512. For example, the register of the module can generate additional chip select signals and provide those to the stacked memory package. *Id*. Alternatively or in addition, the "*control circuit*" in the memory package may also implement rank multiplication. *Id*. at ¶140.

750. Therefore, Riho discloses, and in view of Rajan, renders obvious this limitation to a Skilled Artisan.

751. Accordingly, the prior art references in Ground 2 satisfy the "*memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to*

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control the respective states of the first data conduits and the second data conduits" limitation.

13. Claim 13 is Unpatentable

752. Claim 13 is unpatentable as the prior art references in Ground 2 render the claim obvious.

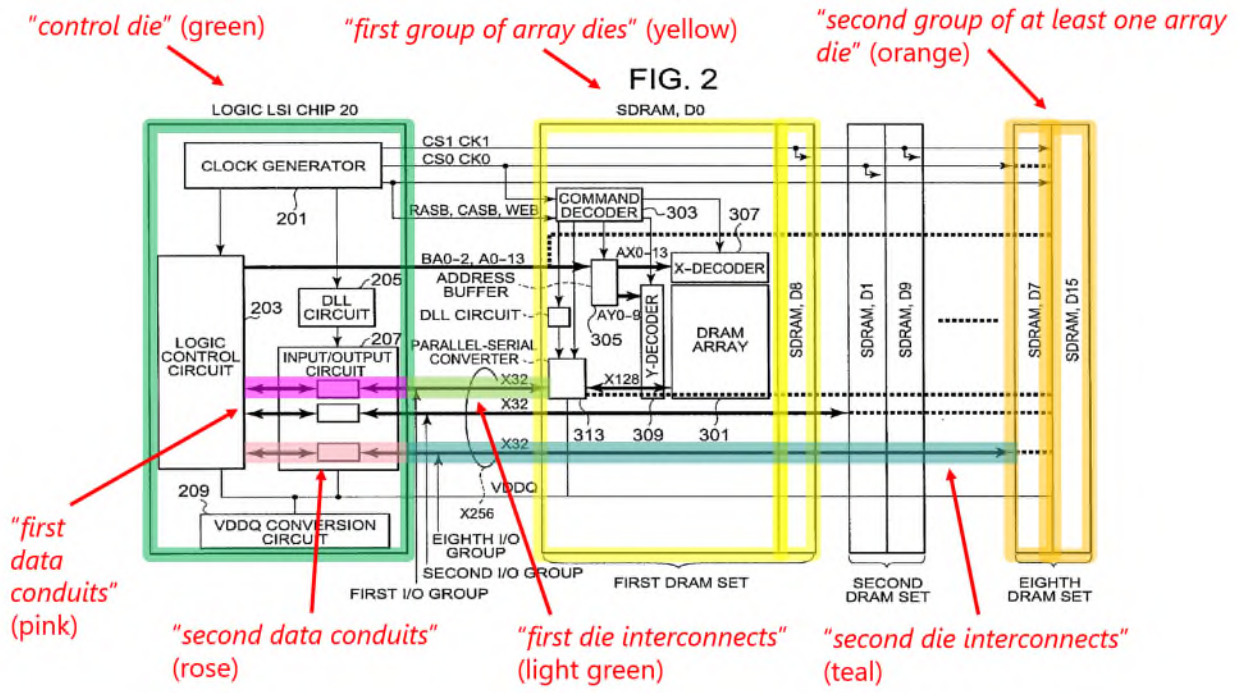
753. Claim 13 requires "*[t]he memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*."

754. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

755. Riho discloses and, in view of Rajan, renders obvious to a Skilled Artisan that "*the control die* [including logic control circuit 203 and control circuit in input/output circuit 207] *is configured to generate data path control signals* [including internal control signals for controlling the direction (read or write) and timing of, and selecting the die(s) for, the data transfer through input/output circuit 207] *from at least some of the control signals* [including write and read commands]*, the data path control signals being used to control the respective states of the first data conduits and the second data conduits* [to or from TSV08 and TSV715]."

756. For example, Riho discloses that the "logic control circuit 203 provided in the logic LSI chip 20 outputs a 3-bit bank address signal BA0-2 and a 14-bit address signal A0-13 and operates as a controller that sends and receives data signals DQ between itself and the input/output circuit 207." Ex. 1016 at [0039].

757. A Skilled Artisan would have understood that, in order to send and receive data through the input/output circuit 207 with the timing required for reading or writing the SDRAMs in the stack, the control circuit has to generate internal signals with the proper timing, and such signals are, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, "*data path control signals being used to control the respective states of the first data conduits and the second data conduits*" because the generated internal signals control the direction of the data transfer (read or write), select the data conduits and the corresponding die(s) for the read or write operation and determine the timing for the data transfer through the data conduits. *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



758. Furthermore, as discussed above, it would have been obvious to a Skilled Artisan to combine the stacked memory devices of Riho with the interface emulation of Rajan. *Supra* ¶¶503-512.

759. For example, Rajan explains that "[a]n example of an emulated protocol characteristic might be a timing, or a specific protocol such as DDR3. … The interface circuit may emulate the number of signals, type of signals, duration of signal assertion, and so forth." Ex. 1015 at 3:42-50. Rajan also discloses the example of "FIG. 10 [which] is a timing diagram illustrating a timing design 1000 of write data timing expected by a DRAM circuit in a buffered stack. Emulation of a larger capacity DRAM circuit having higher CAS latency (as in FIG. 9) may, in some implementations, create a problem with the timing of write operations. For

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example, with respect to a buffered stack of DDR2 SDRAM chips with a read CAS latency of four clocks which are used in emulating a single larger DDR2 SDRAM with a read CAS latency of six clocks, the DDR2 SDRAM protocol may specify that the write CAS latency 1002 is one less than the read CAS latency. Therefore, since the buffered stack appears as a DDR2 SDRAM with a read CAS latency of six clocks, the memory controller may use a buffered stack write CAS latency of five clocks 1004 when scheduling a write operation to the memory." Ex. 1015 at 9:46-60, Fig. 10 (reproduced below); *see also* Ex. 1019, at 23-24 ("CAS latency").

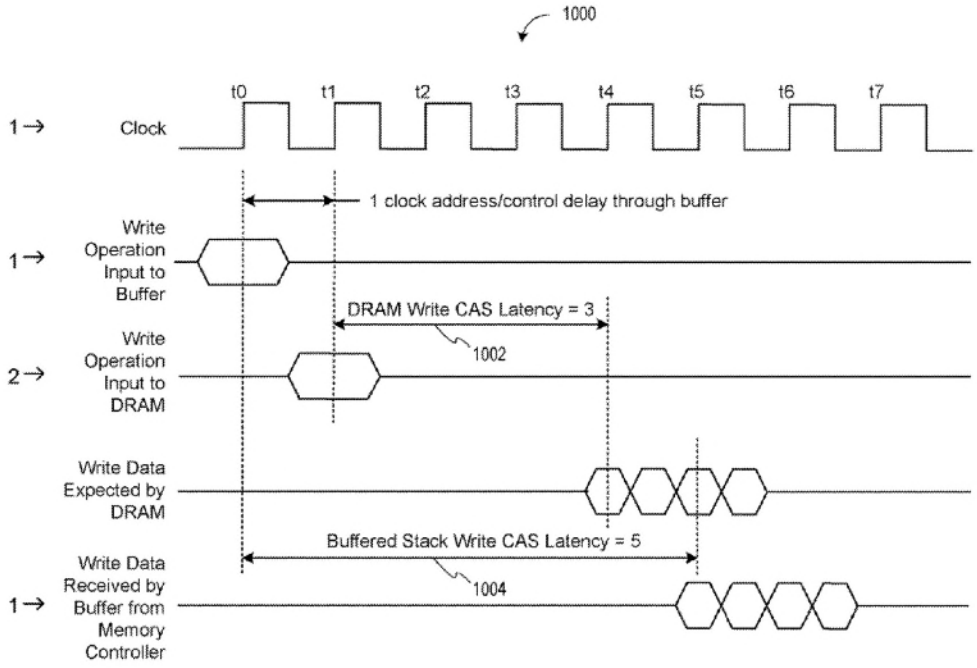


FIG. 10

760. Furthermore, the combination of Riho and Rajan renders obvious to a Skilled Artisan to generate the chip selection and other control signals and the corresponding read and write commands according to the characteristics of the

physical memory dies, while the memory package emulates a different number of more memory devices with different characteristics. *Supra* at ¶¶503-512; *see, e.g.*, Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). For example, the interface circuit can generate additional chip select signals for rank multiplication. *Supra* at ¶¶137-140; *see, e.g.*, Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack."). In such an implementation, the control chip would also generate internal signals, including chip select signals, to select the die(s) which perform the read or write operation and the corresponding data path(s) for the data transfer.

761. A Skilled Artisan would have understood from this disclosure that, when emulating an interface, Rajan's emulation logic generates the corresponding control signals, including data path control signals. *See, e.g.*, Ex. 1015 at Fig. 18 (reproduced below).

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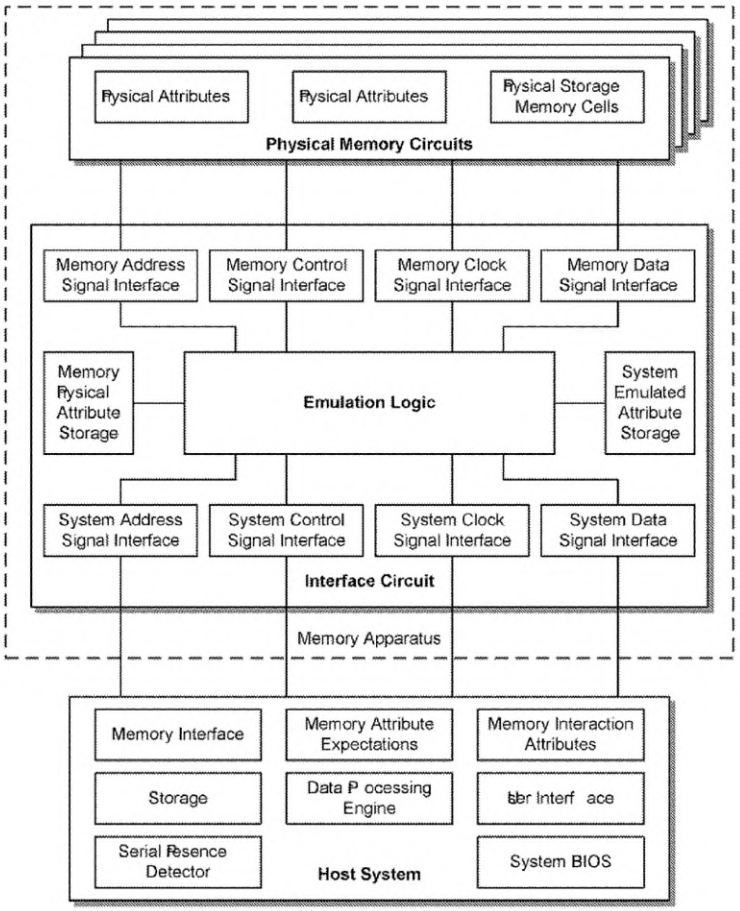


FIG. 18

762. Therefore, Riho discloses and, in combination with Rajan, renders obvious this limitation.

763. Accordingly, the prior art references in Ground 2 satisfy the "*memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits*" limitation.

14. Claim 14 is Unpatentable

764. Claim 14 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [14.a] Control Signals Include Address Signals

765. Claim 14 requires "*[t]he memory module of claim 10, wherein the control signals include address signals*."

766. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

767. Riho at least in view of Rajan renders obvious to a Skilled Artisan that read and write commands include chip-select signals and address signals identifying where to store or retrieve the data, as discussed above with reference to claim limitations [1.b] and [10.b], and in light of a Skilled Artisan's knowledge of the JEDEC standards. *Supra* ¶¶530-537, 707-712; Ex. 1015 (Rajan) at Figs. 4 and 18 (reproduced below, annotated); Ex. 1019 (JESD79-3C) at pp.6-14 (describing package pinout for stacked DDR3 memories, including chip select terminals CSn#, command terminals RAS#, CAS# and WE#, and address signal terminals A0-A15), p.18 (describing read and write operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read and Write commands with

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corresponding column address, CA); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35.

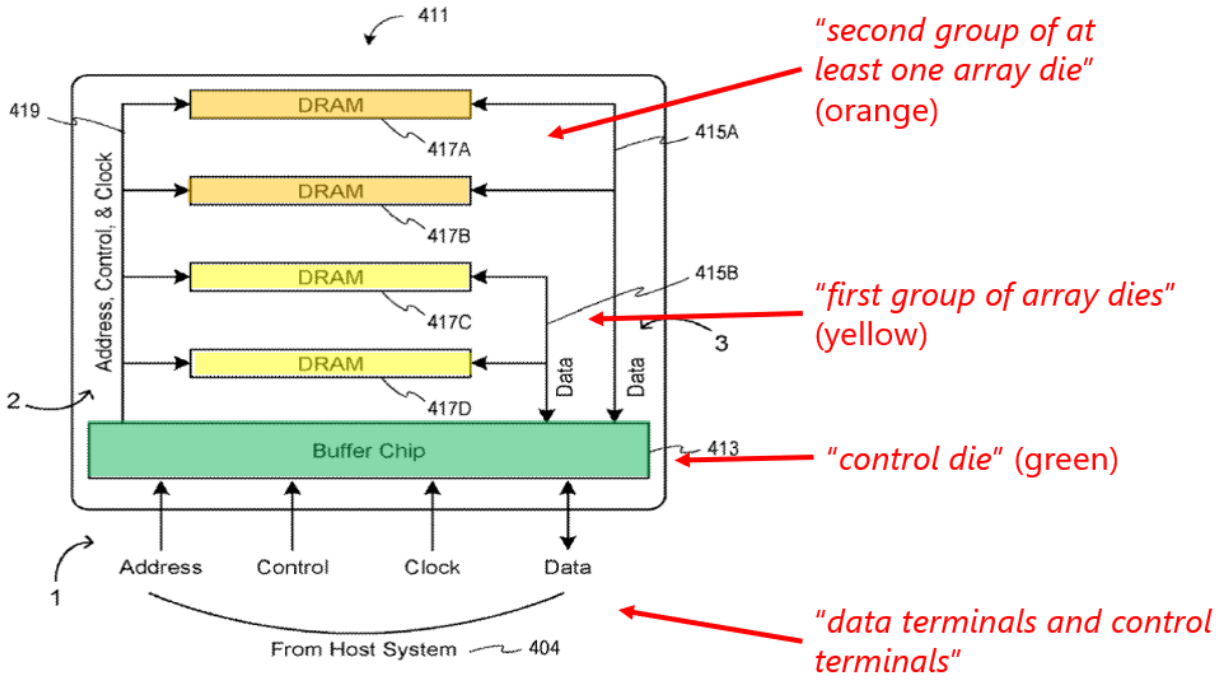


FIG. 4

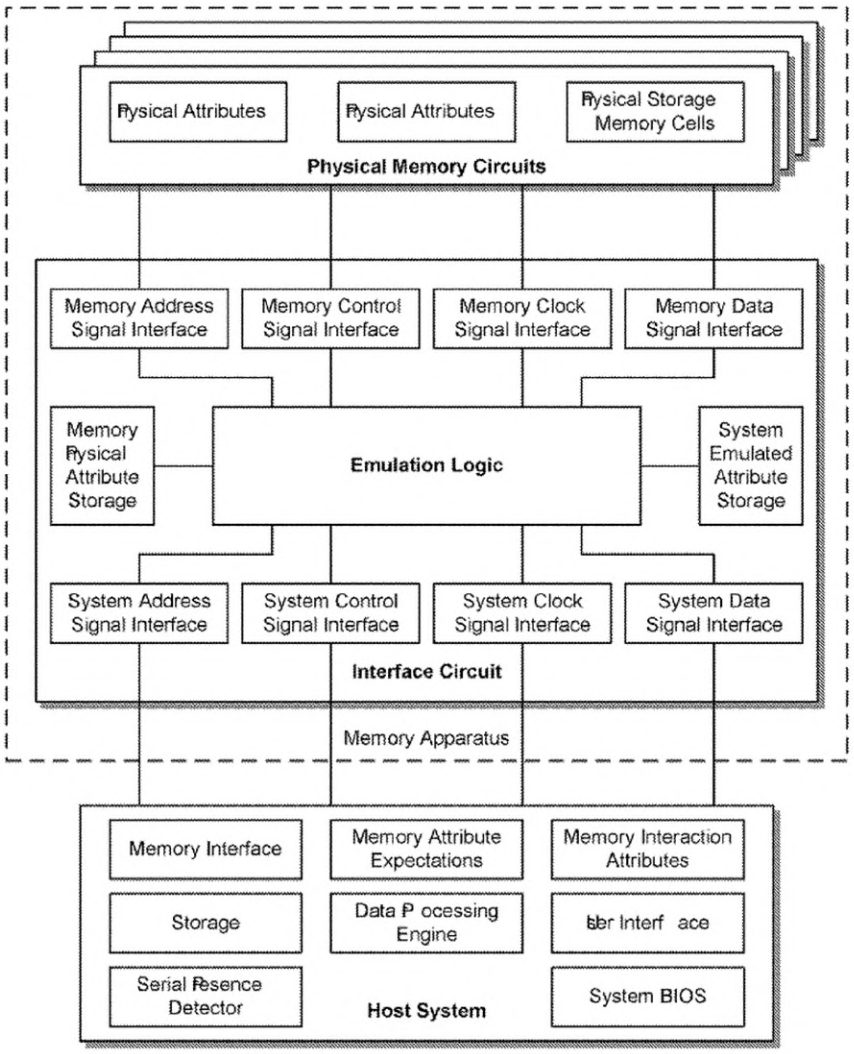


FIG. 18

768. Therefore, Riho at least in view of Rajan renders obvious this limitation to a Skilled Artisan.

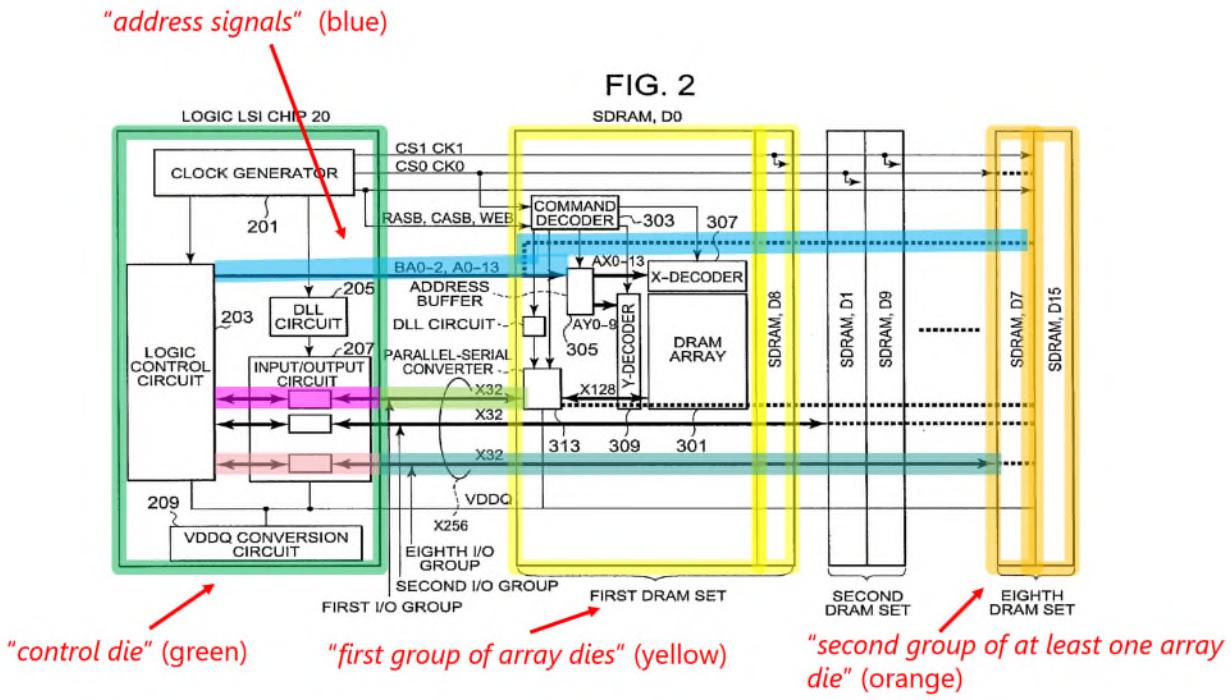
769. Accordingly, the prior art references in Ground 2 satisfy "*wherein the control signals include address signals*."

b) [14.b] Control Die Provides the Address Signals

770. Claim 14 requires "*the control die provides the address signals to the plurality of array dies*."

771. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

772. Riho discloses to a Skilled Artisan that "*the control die* [logic LSI chip 20, including logic control circuit 203] *provides the address signals* [(blue, including BA0-2, A0-13)] *to the plurality of array dies* [SDRAMs D0-D15]." *See, e.g.*, Ex. 1016 (Riho) at Fig. 2 (reproduced below, annotated), [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs."), [0043] ("The 3-bit bank address signal BA0-2 and the 14-bit address signal A0-13 are supplied to all the SDRAMs D0 to D15 through the address TSVs.").



773. For the reasons discussed above with reference to claim limitation [1.b], a Skilled Artisan would have been motivated to provide these command and address signals to the memory chips because they were standard signals used to control SDRAMs. *Supra* ¶¶530-537; *see, e.g.*, Ex. 1015 (Rajan) at 14:55-60 ("The emulation logic may, in various embodiments, alter a timing, value, latency, etc. of any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory. Some such signals may pass through unaltered, while others may be altered.").

774. Therefore, Riho discloses this limitation to a Skilled Artisan.

775. Accordingly, the prior art references in Ground 2 satisfy "*the control die provides the address signals to the plurality of array dies*."

15. Claim 15 is Unpatentable

776. Claim 15 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [15.a] Input Command/Address Signals Include First Chip Select Signals

777. Claim 15 requires "*[t]he memory module of claim 10, wherein the input command/address signals include first chip select signals*."

778. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

779. Riho discloses and, in view of Rajan, renders obvious that "*the input command/address signals include first chip select signals*."

780. For the reasons discussed above with reference to claim limitation [10.b], it would have been obvious to use Riho's memory devices in the memory module of Rajan, which includes "*a register device configured to receive input command/address signals from the system memory controller and to output control signals*." *Supra* ¶¶707-712; *see also supra* ¶¶503-512.

781. A Skilled Artisan would have understood that "*input command/address signals*" include chip select signals according to the JEDEC standards. Ex. 1019 (JESD79-3C) at p.13 ("Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.").

Indeed, Rajan also discloses using the JEDEC protocol. Ex. 1015 at 8:6-13 ("In various embodiments, it may be desirable to determine whether the simulated DRAM circuit behaves according to a desired DRAM standard or other design specification. Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals that a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals.").

782. Therefore, Riho in combination with Rajan discloses this limitation to a Skilled Artisan.

783. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the input command/address signals include first chip select signals*" limitation.

b) [15.b] Register Device Configured to Perform Rank Multiplication

784. Claim 15 requires "*wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*."

785. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

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786. The combination of Riho and Rajan discloses that "*the register device is configured to perform rank multiplication by generating second chip select signals, from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies.*"

787. For example, as discussed above with reference to claim limitation [1.c], Rajan discloses emulating characteristics, including rank multiplication, which involves "*generating second chip select signals, from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals*." *Supra* ¶¶137-139, 538-545; *see, e.g.*, Ex. 1015 at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 6:30-7:67 (disclosing specific examples of rank multiplication). Rajan also explains that, in one implementation, "the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals." Ex. 1015 at 7:12-16. Rajan further discloses that "the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level." *Id.* at 8:56-58.

788. Rajan also discloses that the generated chip select signals are "*equal to a number of array dies in the plurality of array dies*." *Id*. at 6:34-38 ("In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

789. A Skilled Artisan would have understood from this disclosure that the register, such as an AMB, can "*perform rank multiplication by generating chip select signals*" for additional ranks from the input address signals. *See supra* ¶¶137-140; *see also* Ex. 1001 (160 patent) at 18:33-39, 22:19-25 (admitting that rank multiplication was prior art); Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

790. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

791. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the register device is configured to perform rank multiplication by generating*

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second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies" limitation.

c) [15.c] Chip Select Die Interconnects

792. Claim 15 requires "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

793. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

794. Riho also discloses that "*the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

795. For example, Riho discloses that, "[o]f the two groups (chip selection groups), the first group (first controlled chips) is communication-controlled at a first access cycle by the first chip selection signal (first clock signal CS0CK0) output from the control chip 20 while the second group (second controlled chips) is communication-controlled at a second access cycle by the second chip selection signal (second clock signal CS1CK1) output from the control chip 20." Ex. 1016 at [0033]. Riho further explains that "[t]he first and second clock signals CS0CK0

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and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs." Ex. 1016 at [0038].

796. To the extent one might argue that Riho does not sufficiently disclose die interconnects for the chip select signals, it would have been obvious to a Skilled Artisan in view of Rajan. For example, Rajan discloses that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." Ex. 1015 at 6:34-38. Using separate chip select signals for selecting a chip in the stack, as described by Rajan, was well known at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Figs. 1-3 showing stacked DDR3 chips, each receiving a separate chip select signal), p.13 (explaining that chip select "provides for external Rank selection on systems with multiple Ranks"), Fig. 2 (reproduced below, annotated to indicate chip select signals); *see also* Ex. 1022 at 319 (the "chip-select bus … is essential in a JEDEC style memory system"); Ex. 1023 at 2-4, 9, Fig.16.

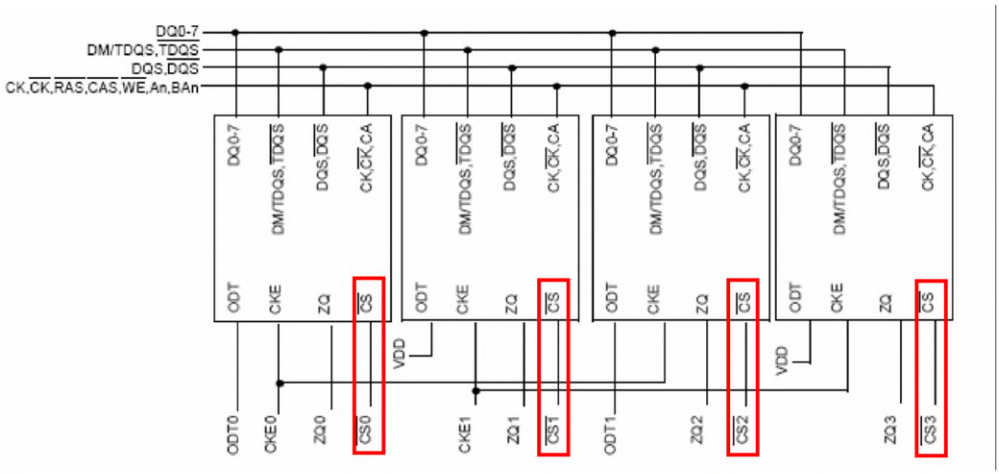


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

797. The prior art described in the 160 Patent, specifically Figs. 1A and 1B, demonstrate that transmitting separate chip select signals through die interconnects to select a chip in the stack was well known at the time. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for chip select signals), 1:51-58 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.").

798. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

799. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

16. Claim 16 is Unpatentable

800. Claim 16 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [16.a] Control Signals Include Output Command/Address Signals Derived from the Input Command/Address Signals

801. Claim 16 requires "*[t]he memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals*."

802. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

803. As shown in the table below, claim limitation [16.a] is very similar to claim limitation [15.a]:

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Claim 15	**Claim 16**
[15.a] wherein the input command/address signals include first chip select signals	[16.a] The memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals,

804. For the reasons discussed above with reference to claim limitation [15.a], the prior art references in Ground 2 satisfy "*wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals.*" *Supra* ¶¶777-783.

805. For example, registered DIMMs with registers that derived output command/address signals from the input command/address signals were well known, including chip select signals according to the JEDEC standards. *See, e.g.,* Ex. 1015 (Rajan) at Fig. 8 (reproduced below).

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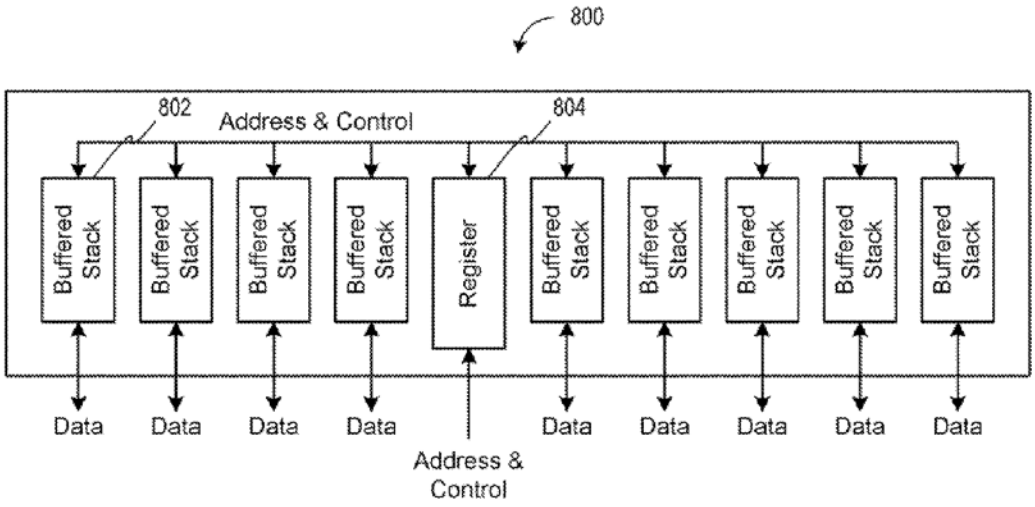


FIG. 8

806. Therefore, the combination of Riho and Rajan discloses and renders obvious this limitation to a Skilled Artisan.

807. Accordingly, the prior art references in Ground 2 satisfy the "*wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals*" limitation.

b) [16.b] Control Die is Configured to Perform Rank Multiplication

808. Claim 16 requires "*wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies*."

809. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

810. As shown in the table below, claim limitation [16.b] is very similar to claim limitation [15.b], with the exception that claim limitation [16.b] requires the control die (as opposed to the register device) to perform the rank multiplication:

Claim 15	**Claim 16**
[15.b] wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and	[16.b] wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and

811. As previously discussed, a Skilled Artisan would have understood that, either alternatively or in addition to the register of the module, the control circuit in the "*control die*" of the memory package may also implement rank multiplication *Supra* ¶¶140, 405. Thus, for the reasons discussed above with reference to claim limitation [15.b], the prior art references in Ground 2 satisfy "*wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip*

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select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies." *Supra* ¶¶784-791. For example, a Skilled Artisan would have understood that the number of the chip select signals is equal to the number of the array dies in the stack. *Supra* at ¶788. Thus, when the output command/address signals from the register have fewer chip selects than the number of array dies in the stack, the additional chip select signals are generated by the control die. *Id*.

c) [16.c] Chip Select Die Interconnects

812. Claim 16 requires "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*."

813. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

814. As shown in the table below, claim limitation [16.c] is very similar to claim limitation [15.c]:

Claim 15	**Claim 16**
[15.c] wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.	[16.c] wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.

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815. As discussed above with reference to claim limitation [15.c], the prior art references in Ground 2 satisfy "*wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies*." *Supra* ¶¶792-799.

17. Claim 17 is Unpatentable

816. Claim 17 is unpatentable as the prior art references in Ground 2 render the claim obvious.

817. Claim 17 requires "*[t]he memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver*."

818. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

819. As shown in the table below, claim 17 is nearly identical to claim 4:

Claim 4	**Claim 17**
[4] The memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.	[17] The memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver.

820. As discussed above with reference to claim 4, the prior art references in Ground 2 satisfy "*wherein the first driver size and the second driver size are*

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related to a first load on the first driver and a second load on the second driver." *Supra* ¶¶635-641.

18. Claim 18 is Unpatentable

821. Claim 18 is unpatentable as the prior art references in Ground 2 render the claim obvious.

822. Claim 18 requires "*[t]he memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.*"

823. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

824. The combination of Riho and Rajan discloses that "*the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

825. For example, Rajan discloses that the control chip receives command/address signals for a write command and holds those signals for an additional time to control timing of when the DRAMs receive those signals. Ex. 1015 at Fig. 11 (reproduced below), 10:12-19 ("The memory controller issues the write operation at t0. In FIG. 10, the write operation appeared at the DRAM circuits one clock later at t1, due to the inherent delay through the buffer chip. But in FIG. 11, in addition to the inherent one clock delay, the buffer chip has added an

extra two clocks of delay to the write operation, which is not issued to the DRAM chips until t0+1+2=t3.").

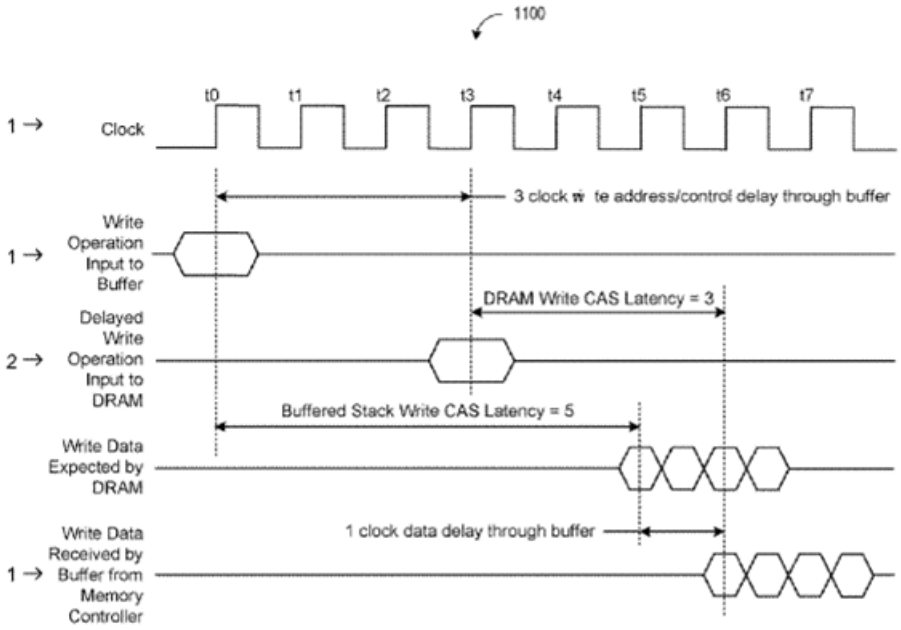


FIG. 11

826. A Skilled Artisan would have been motivated to implement this delay of command/address signals to emulate certain characteristics as taught by Rajan. *See, e.g.*, Ex. 1015 (Rajan) at 9:61-10:4 ("In the specific example shown, the memory controller issues the write operation at t0. After a one clock cycle delay through the buffer chip, the write operation is issued to the DRAM chips at t1. Because the memory controller believes it is connected to memory having a read CAS latency of six clocks and thus a write CAS latency of five clocks, it issues the write data at time t0+5=t5. But because the physical DRAM chips have a read CAS latency of four clocks and thus a write CAS latency of three clocks, they expect to

receive the write data at time t1+3=t4. Hence the problem, which the buffer chip may alleviate by delaying write operations.").

827. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

828. Accordingly, the prior art references in Ground 2 satisfy "*wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals*."

19. Claim 19 is Unpatentable

829. Claim 19 is unpatentable as the prior art references in Ground 2 render the claim obvious.

830. Claim 19 requires "*[t]he memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals*."

831. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

832. As shown in the table below, claim 19 is very similar to claim 18:

Claim 18	**Claim 19**
[18] The memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.	[19] The memory module of claim 10, wherein the control die includes data buffers to control timing of the data signals.

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833. As discussed above with reference to claim 18, the prior art references in Ground 2 satisfy "*wherein the control die includes data buffers to control the timing of the data signals*." *Supra* ¶¶821-828. For example, Figure 9 of Rajan shows that emulating a CAS latency includes the control die buffering the data to and from the DRAMs and outputting it with a delay in order to control the timing of the data signals. Ex. 1015 at 8:59-9:45, Fig. 9 (reproduced below); s*ee also supra* at ¶495 (discussing details of Fig. 9).

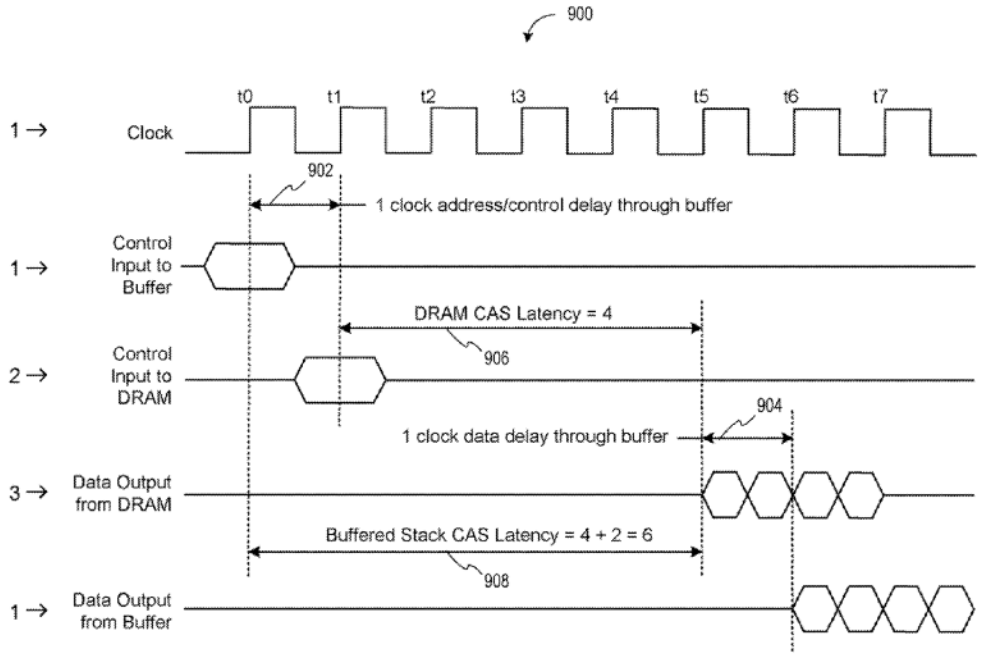


FIG. 9

834. Accordingly, the prior art references in Ground 2 satisfy "*wherein the control die includes data buffers to control the timing of the data signals*."

20. Claim 20 is Unpatentable

835. Claim 20 is unpatentable as the prior art references in Ground 2 render the claim obvious.

836. Claim 20 requires "*[t]he memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*."

837. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

838. As shown in the table below, claim 20 is very similar to claim limitation [3.b]:

Claim 3	**Claim 20**
[3.b] wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.	[20] The memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die.

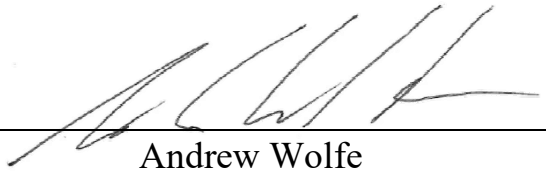
839. As discussed above with reference to claim limitation [3.b], the prior art references in Ground 2 satisfy the "*wherein the first group of array dies include a greater number of array dies than the second group of at least one array die*" limitation. *Supra* ¶¶618-622.

* * *

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I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 26, 2022



Andrew Wolfe

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 9,318,160 (issued April 19, 2016)
1002	File History of U.S. Patent No. 8,787,060 (Application No. 13/288,850 filed Nov. 3, 2011)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 61/409,893 (filed Nov. 3, 2010)
1006	File History of U.S. Patent Application No. 14/337,168 (filed July 21, 2014)
1007	File History of U.S. Patent Application No. 15/095,288 (filed Apr. 11, 2016)
1008	File History of U.S. Patent Application No. 15/602,099 (filed May 22, 2017)
1009	File History of U.S. Patent Application No. 16/412,308 (filed May 14, 2019)
1010	File History of U.S. Patent Application No. 17/157,903 (filed Jan. 25, 2021)
1011	U.S. Patent Application Publication No. 2008/0025137 to Rajan *et al.* (published Jan. 31, 2008)
1012	U.S. Patent Application Publication No. 2011/0193226 to Kirby *et al.* (filed Feb. 8, 2010, published Aug. 11, 2011)
1013	U.S. Patent Application Publication No. 2006/0259678 to Gervasi (published Nov. 16, 2006)
1014	U.S. Patent Application Publication No. 2011/0103156 to Kim *et al.* (filed Dec. 29, 2009, published May 5, 2011)

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Exhibit #	Description
1015	U.S. Patent No. 8,041,881 to Rajan *et al.* (filed June 12, 2007, issued Oct. 18, 2011)
1016	U.S. Patent Application Publication No. 2011/0026293 to Riho (filed July 16, 2010, published Feb. 3, 2011)
1017	U.S. Patent No. 7,969,192 to Wyman *et al.* (filed Mar. 26, 2010, issued June 28, 2011)
1018	U.S. Patent Application Publication No. 2010/0195364 to Riho (published Aug. 5, 2010) ("Riho2")
1019	JEDEC DDR3 SDRAM Standard, JESD79-3C (Nov. 2008)
1020	Declaration of Julie Carlson for JESD79-3C
1021	JEDEC MO-207, Square & Rectangular Die-Size, Ball Grid Array Family (Dec. 2010)
1022	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1023	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
1024	U.S. Patent No. 7,796,446 to Ruckerbauer *et al.* (issued Sept. 14, 2010)
1025	U.S. Patent No. 8,258,619 to Foster *et al.* (filed Nov. 12, 2009)
1026	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry *et al.* (published Dec. 7, 2006)
1027	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (Final Written Decision)
1028	U.S. Patent No. 7,289,386 to Bhakta *et al.* (issued Oct. 30, 2007)
1029	Affirmance of the Examiner's Decision on Reexamination of the '386 Patent (Feb. 25, 2015)
1030	Stephen Brown et al., Fundamentals of Digital Logic (2d ed. 2008)

Exhibit #	Description
1031	U.S. Patent No. 7,532,537 to Solomon *et al.* (issued May 12, 2009)
1032	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00667, Paper No. 38 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1033	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00668, Paper No. 36 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1034	U.S. Patent No. 8,471,362 to Lee (filed Apr. 5, 2011)
1035	JEDEC Graphics Double Data (GDDR4) SGRAM Specification (Nov. 2005)
1036	[omitted]
1037	U.S. Patent No. 7,890,811 to Rothman *et al.* (filed June 29, 2007, issued Feb. 15, 2011)
1038	Harold S. Stone, Microcomputer Interfacing (1982)
1039	U.S. Patent No. 9,160,349 to Ma (filed Aug. 27, 2009)
1040	[omitted]
1041	U.S. Patent No. 8,129,958 to Bigler *et al.* (filed Dec. 24, 2007)
1042	[omitted]
1043	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1044	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)
1045	Answer to Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 18, 2022)
1046	Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)

Exhibit #	Description
1047	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1048	Federal Court Management Statistics (Mar. 31, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1>

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory package, comprising:
1.b	data terminals and control terminals;
1.c	stacked array dies including a first group of array dies and a second group of at least one array die;
1.d.1	first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
1.d.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
1.e.1	a control die comprising
1.e.2	first data conduits between the first die interconnects and the data terminals, and
1.e.3	second data conduits between the second die interconnects and the data terminals,
1.e.4	the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies,
1.e.5	the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.
2	The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein the second driver size is larger than the first driver size.
3.a	The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and
3.b	wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.

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Ref. #	Listing of Challenged Claims
4	The memory package of claim 1, wherein the first driver size and the second driver size are related to a load on the first driver and a load on the second driver.
5	The memory package of claim 1, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via the control terminals.
6.a	A memory package, comprising:
6.b	data terminals and control terminals;
6.c	stacked array dies including a first group of array dies and a second group of at least one array die;
6.d.1	first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
6.d.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
6.e	wherein the second die interconnects are longer than the first die interconnects, and
6.f	wherein a number of array dies in the second group of at least one array die is less than a number of array dies in the first group of array dies.
7.a	The memory package of claim 6, further comprising: a control die comprising
7.b.1	first data conduits between the first die interconnects and the data terminals,
7.b.2	second data conduits between the second die interconnects and the data terminals,
7.c.1	the first data conduits including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies,

Ref. #	Listing of Challenged Claims
7.c.2	the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.
8	The memory package of claim 7, wherein the second driver size is larger than the first driver size.
9	The memory package of claim 7, wherein the control die further comprises a control circuit to control respective states of the first data conduits and the second data conduits in response to control signals received via one or more second terminals of the plurality of terminals.
10.a	A memory module operable in a computer system with a system memory controller, comprising
10.b	a register device configured to receive input command/address signals from the system memory controller and to output control signals; and
10.c	a plurality of DRAM packages, each DRAM package comprising:
10.d	data terminals via which the DRAM package communicate data signals with the system memory controller, and control terminals via which the DRAM package receive the control signals from the register device;
10.e	stacked array dies including a first group of array dies and a second group of at least one array die;
10.f.1	die interconnects including first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
10.f.2	the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
10.g.1	a control die including
10.g.2	first data conduits between the first die interconnects and data terminals, and
10.g.3	second data conduits between the second die interconnects and the data terminals,

Ref. #	Listing of Challenged Claims
10.h.1	the first data conduits including first drivers each having a first driver size, the second data conduits including second drivers each having a second driver size different from the first driver size,
10.h.2	the first drivers to drive first write data signals received from the system memory controller to one of the first group of array dies, the second drivers to drive second write data signals received from the system memory controller to one of the second group of at least one array die.
11	The memory module of claim 10, wherein the control die receives the control signals and further includes a control circuit to control respective states of the first data conduits and the second data conduits in response to the control signals.
12	The memory module of claim 11, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduits and the second data conduits.
13	The memory module of claim 11, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduits and the second data conduits.
14.a	The memory module of claim 10, wherein the control signals include address signals and
14.b	the control die provides the address signals to the plurality of array dies.
15.a	The memory module of claim 10, wherein the input command/address signals include first chip select signals,
15.b	wherein the register device is configured to perform rank multiplication by generating second chip select signals from at least some of the input command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and
15.c	wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.

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Ref. #	Listing of Challenged Claims
16.a	The memory module of claim 10, wherein the control signals include output command/address signals derived from the input command/address signals, the output command/address signals including first chip select signals,
16.b	wherein the control die is further configured to perform rank multiplication by generating second chip select signals from at least some of the output command/address signals, the second chip select signals having a number of chip select signals greater than the first chip select signals and equal to a number of array dies in the plurality of array dies, and
16.c	wherein the DRAM package further comprises chip select die interconnects for conducting the second chip select signals to respective ones of the plurality of array dies.
17	The memory module of claim 10, wherein the first driver size and the second driver size are related to a first load on the first driver and a second load on the second driver.
18	The memory module of claim 10, wherein the control signals include command/address signals, and the control die includes buffers to control the timing of the command/address signals.
19	The memory module of claim 10, wherein the control die includes data buffers to control the timing of the data signals.
20	The memory module of claim 10, wherein the first group of array dies include a greater number of array dies than the second group of at least one array die.

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