UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Patent No. 8,787,060
Issued: July 22, 2014
Filed: November 3, 2011
Inventor: Hyun Lee

Title: Method and Apparatus for Optimizing Driver Load in a Memory Package

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Inter Partes Review No. IPR2022-01428

DECLARATION OF DR. ANDREW WOLFE REGARDING U.S. PATENT NO. 8,787,060

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 8,787,060 ("the 060 Patent") (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including

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Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM and flash memory,

in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the 060 Patent, I am relying upon certain basic legal principles that have been explained to me.

25. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 060 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims of the 060 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors"

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 060 PATENT

A. Effective Filing Date of the 060 Patent: No Earlier Than November 3, 2011

47. The 060 Patent claims priority to U.S. Provisional Application No. 61/409,893 ("893 Provisional Application" or "893 Provisional") (Ex. 1005), filed November 3, 2010. Ex. 1001 (060 Patent) (60).

48. In my opinion, as explained below, the effective filing date for the claims of the 060 Patent is no earlier than November 3, 2011. In any event, all of the prior art I rely upon for my invalidity opinions predates November 3, 2010.

1. Several Limitations in All Claims Are Unsupported by the 893 Provisional Application Filed November 3, 2010

49. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the 893 Provisional Application shows that the inventor actually invented what is claimed in each of the claims of the 060 Patent, and possessed the claimed subject matter, as of the provisional filing date of November 3, 2010. When considering that question, I have considered whether the 893 Provisional Application explicitly or inherently discloses all of the elements of each of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I

understand that the knowledge of ordinary artisans may be used to inform what is actually in the provisional, but not to teach limitations that are not in the provisional, even if those limitations would be rendered obvious by the disclosure in the provisional.

50. Although the 893 Provisional Application lists more than a dozen patent and patent application numbers to be incorporated by reference, the 893 Provisional Application falls short of describing many elements included in the claims of the 060 Patent's claims, in many cases not even using any terms associated with an element. Much of the disclosure in the 060 Patent was added with the filing of the non-provisional application. Specifically, the non-provisional application added to the 893 Provisional Application's disclosure Figures 1-5, all of columns 1-2, 5-17, and 21-28, and at least part of columns 3-4 and 18-20 of the 060 Patent, Ex. 1001. In my opinion, at least the following claim limitations are not disclosed by the 893 Provisional Application filed November 3, 2010:

a) Groups of Array Dies – Claims 1, 11, 20, 29.

51. Each of independent claims 1, 11, and 20 include one or more limitations requiring a memory package having stacked array dies that include "*a first group of array dies*" and "*a second group of at least one array die*." Ex. 1001 (060 Patent), cls. 1, 11, 20, 29.

52. The 893 Provisional Application does not itself mention groups within a stack of array dies. *See* Ex. 1005. The figures illustrate DRAM packages, which packages are also described in paragraphs [0006]-[0012] of the 893 Provisional Application. *Id.* Additionally, the title of the provisional is "Architecture for Memory Module with Packages of Three-Dimensional Stacked (3DS) Memory Chips." *Id.* at 1. In the specification, the 3DS DRAM package is described as including stacked DDR DRAM chips or dies. *Id.* at 5, ¶[0006]. However, the packages described in the 893 Provisional Application do not have groups of array dies within the stack as claimed in the 060 Patent. In particular, the illustrated dies are never separated into a first group and a second group.

53. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of the "*first group of array dies*" and "*second group of at least one array die*" as recited in the independent claims of the 060 Patent.

b) Die Interconnects Not in Electrical Communication with Some Array Dies – Claims 1, 11, 20, 29

54. Each of claims 1, 11, 20 and 29 include a limitation requiring first and second die interconnects, each being in electrical communication with a respective group of array dies but not in electrical communication with another group of array dies. Ex. 1001 (060 Patent), cls. 1, 11, 20, 29.

55. The 893 Provisional Application does not describe a die interconnect which is in electrical communication with one group of array dies but is not in electrical communication with another group of array dies. *See* Ex. 1005. Each of the interconnects disclosed is in electrical communication with all of the array dies.

56. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of first and second die interconnects, each being in electrical communication with a respective group of array dies but not in electrical communication with another group of array dies as recited in the independent claims of the 060 Patent.

c) Respective States of Data Conduits – Claims 1, 11, 29

57. Each of claims 1, 11, and 29 include a limitation requiring a control circuit controlling "respective states" of "data conduits." Ex. 1001 (060 Patent), cls. 1, 11, 29.

58. The 893 Provisional Application does not mention any "data conduit" or any specific "respective states" of such a "data conduit." *See* Ex. 1005.

59. Thus, it is my opinion that Patent Owner cannot show that the 893 Provisional Application's disclosure supports the limitations of a control circuit controlling "respective states" of "data conduits" as recited in independent claims 1, 11, and 29 of the 060 Patent.

B. Person of Ordinary Skill in the Art

60. The 060 Patent identifies the relevant field of art as follows: "The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules." Ex. 1001 at 1:18-22. Based on that description of the field of art, my experience, and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 060 Patent in 2010 and 2011 ("Skilled Artisan" or "POSITA") would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories,

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including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

C. Overview of the 060 Patent

61. The 060 Patent states that it "relates to systems and methods for reducing the load of drivers of memory packages." Ex. 1001 (060 Patent) at 1:19-21. The 060 Patent admits as prior art "FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used." *Id*. at 1:30-33 and Fig. 1B (reproduced below, annotated).

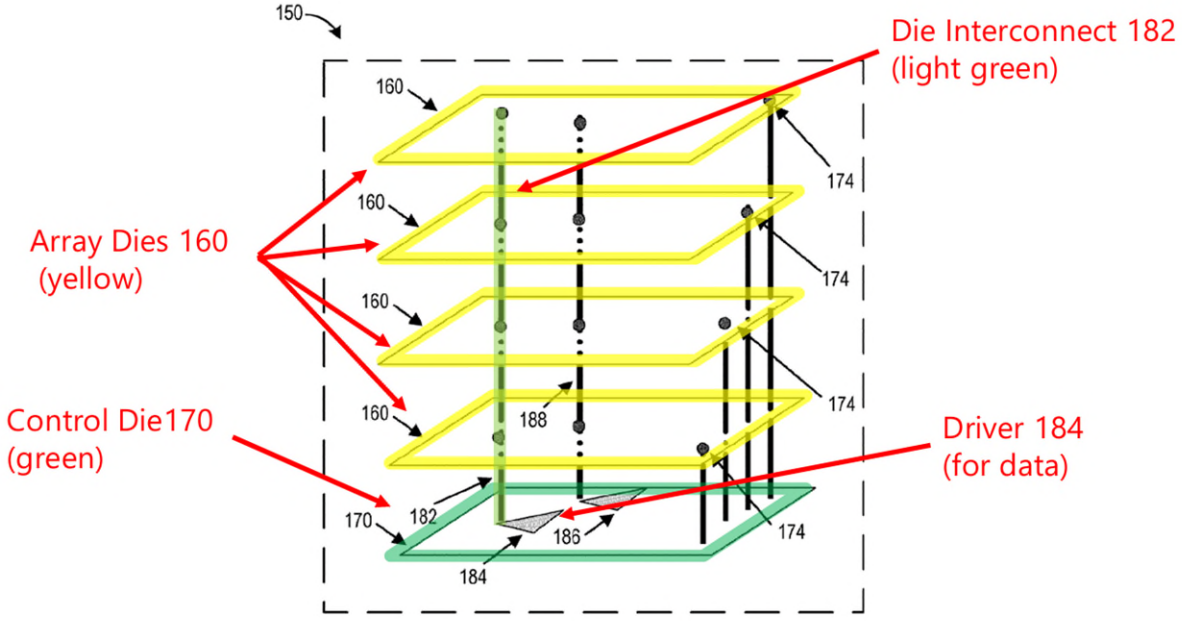
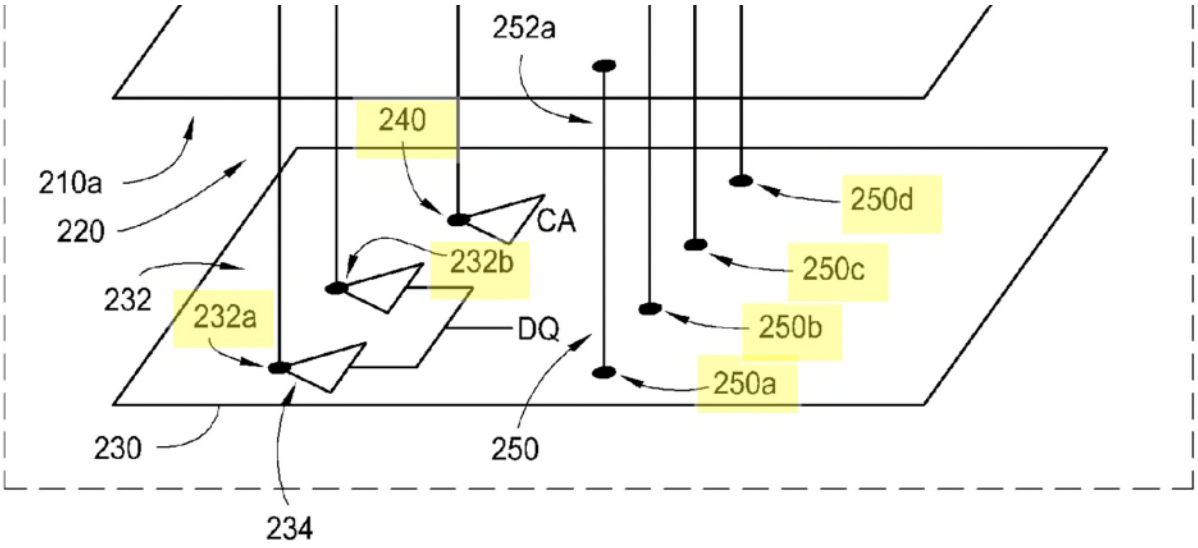


FIG. 1B

In particular, "FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 [(yellow)] and a control die 170 [(green)] that … [includes] a driver 184 that drives data signals to each of the array dies 160

along a corresponding die interconnect 182." Ex. 1001 (the 060 Patent) at 1:63-2:4. The 060 Patent explains that a problem with the prior-art memory package is that the data driver 184 has to drive a load that is "in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power." *Id*. at 2:8-15.

62. The 060 Patent discloses that each die interconnect has a corresponding "conduit" which is configured to transmit a signal to the die interconnect. Ex. 1001 (060 Patent), *e.g.*, at Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b, command/address conduits 240, and chip select conduits 250a-d), 6:48-59 (describing data conduits 232a and 232b), 9:28-60 (describing command/address conduits 240 and chip select conduits 250). A "conduit" may, but does not have to, include a driver to drive the load on the conduit. *Id*.; *see also* 6:60-62 ("In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2."), 21:18-20 ("The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.").



63. The 060 Patent solves the prior art's problem of having too much load on the data conduits by replacing one data driver of the prior art with two (or more) drivers 234 coupled to the same DQ data terminal, each of the drivers driving the data signal through a respective die interconnect (220a, 220b) that is in electrical communication with *a subset* of the array dies, thus reducing the overall load of each data conduit. Ex. 1001 (the 060 Patent) at 7:9-8:18 and Fig. 2 (reproduced below, annotated).

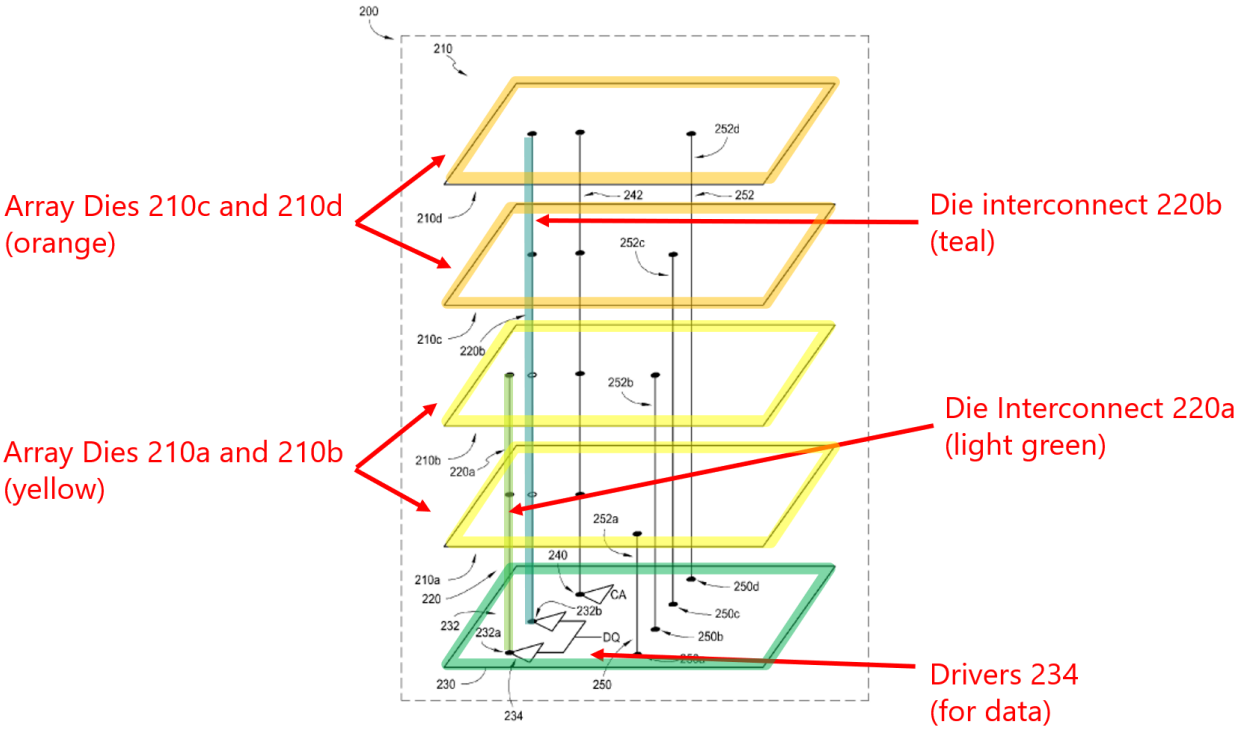


FIG. 2

64. In the example of Fig. 2, "die interconnect 220a [(light green)] may be in electrical communication with a data port from array die 210a [(yellow)] and a data port from array die 210b [(yellow)] (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c [(orange)] or any data ports from array die 210d [(orange)]." Ex. 1001 (the 060 Patent) at 5:63-6:1. The other "die interconnect 220b [(teal)] may be in electrical communication with a data port from array die 210c [(orange)] and a data port from array die 210d [(orange)] (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a [(yellow)] and array die

210b [(yellow)]… Despite not being in electrical communication with any data ports from array die 210a and 210b [(yellow)], in some implementations, the die interconnect 220b [(teal)] may pass through the array dies 210a and 210b [(yellow)] (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b." *Id*. at 6:9-15.

65. In another example, the 060 Patent discloses selecting the number of array dies that are connected to a die interconnect in order to reduce the difference between the loads on the different data conduits. Ex. 1001 at Fig. 3 and Table 1 (reproduced below). Here, the memory package 300 includes eight array dies 310a-310h and a control die 330. *Id*. at 10:18-40. The control die includes six data conduits 332a-f with respective drivers 334a-334f, each driving a respective die interconnect 320a-f. *Id*. at 10:41-55. Each of the shorter interconnects 320a and 320b is connected to two array dies, and each of the longer interconnects 320c-f is connected to a single array die. *Id*.

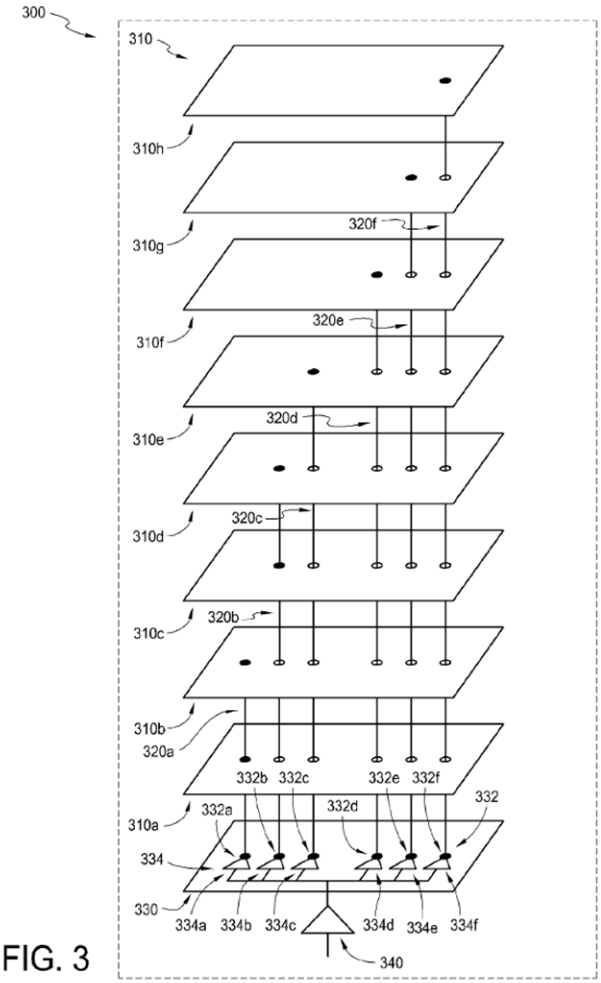


FIG. 3

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5 L	0.5
332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

"Table 1 specifies the capacitive load values for each conduit 332 assuming … that the load of each of the array dies 310 is L, and that the load of each segment of the

die interconnects 320 is 0.25L. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f." *Id*. at 12:52-13:18. "As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is 3L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10L." *Id*. at 13:19-25. The 060 Patent further explains that such a die interconnect in electrical communication with each die "does not implement the teachings of this disclosure, but is in accordance with conventional configurations." Ex. 1001 (the 060 Patent) at 7:22-29.

D. The Prosecution History of the 060 Patent

66. The prosecution histories of the 060 Patent and the other patent applications in the family of the 060 Patent are discussed below, starting with the earliest filed application, the 893 Provisional Application.

1. Provisional Application No. 61/409,893 (Nov. 3, 2010)

67. The applicants filed Provisional Application No. 61/409,893 ("893 Provisional Application"), titled "Architecture for Memory Module with Packages of Three-Dimensional Stacked (3DS) Memory Chips," on November 3, 2010. Ex. 1005 at p. 14.

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2. Application No. 13/288,850 (060 Patent)

68. The applicants filed U.S. Patent Application No. 13/288,850 ("850 Application"), titled "Method and Apparatus for Optimizing Driver Load in a Memory Package," on November 3, 2011. Ex. 1002 at p. 60. The 850 Application claims the benefit of the 893 Provisional Application, filed November 3, 2010. Ex. 1002 at pp. 60, 64. The 060 Application presented 34 claims at filing, 1-34. Ex. 1002 at pp. 43-50.

69. The International Search Report mailed January 30, 2013, indicated that Figures 2B and 2C of U.S. Patent Publication No. 2008/0025137 ("Rajan137") (Ex. 1011), reprinted below, were "of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone." Ex. 1002 at pp. 238-48.

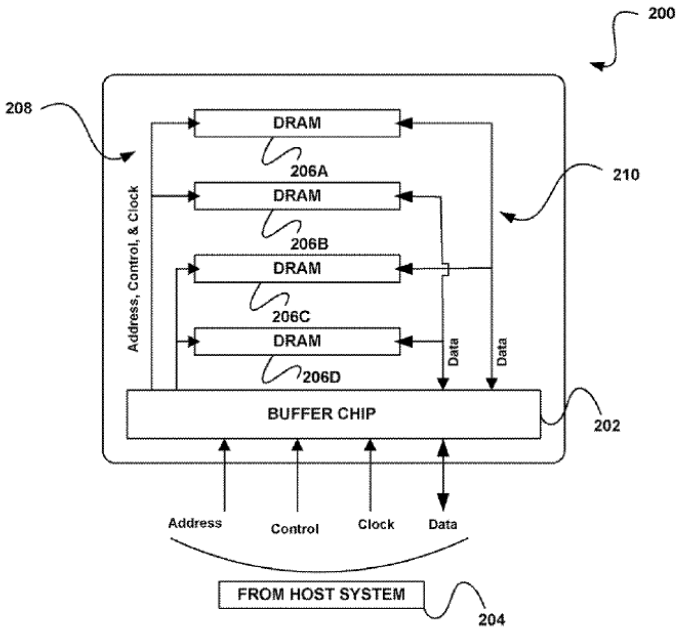


FIGURE 2B

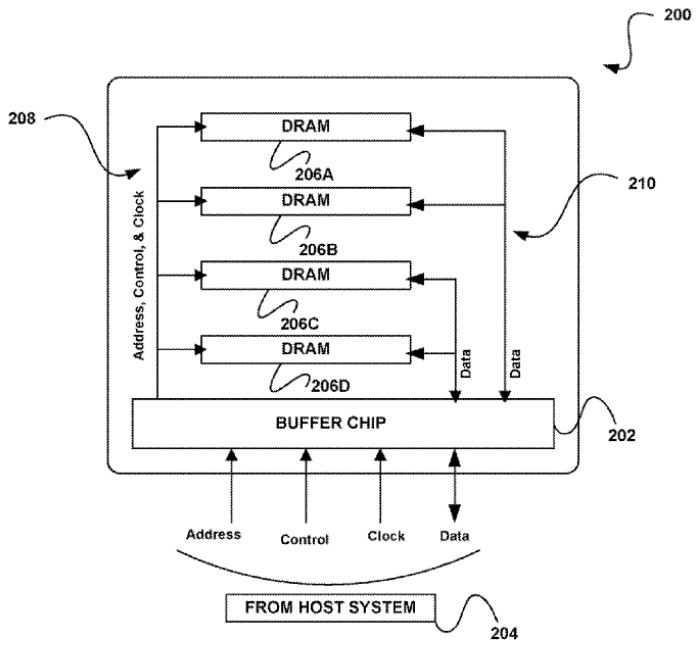


FIGURE 2C

Ex. 1011 (Rajan137), Figs.2B-2C.

70. A Restriction Requirement was issued on June 6, 2013, stating that Claims 1-28 cover "a memory package and a method for optimizing load in a memory package, classified in class 365, subclass 63," and Claims 29-34 cover "a memory module comprising a register device and a plurality of DRAM packages each comprising a plurality of DDR DRAM dies, classified in class 365, subclass 365/233.13." Ex. 1002 at p. 410.

71. On August 6, 2013, the applicants filed a response to the Restriction Requirement, amending Claims 1-34 and electing "without traverse the invention in Claims 1-28 as amended for examination" and amending Claims 29-34 "to include the particulars of claims 11-19 so that they related to the same subject matter as claims 11-19." Ex. 1002 at pp. 417-426.

72. The first Office Action was filed on October 11, 2013. Ex. 1002 at p. 433. Claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, and 34 were rejected as anticipated by US Pat. Pub. No. 2008/0025137 ("Rajan137") (Ex. 1011). *Id.* at pp. 437-42. Claims 6, 14, 25, and 26 were rejected as obvious over Rajan137 in view of Kirby (US 2011/0193226) (Ex. 1012). *Id.* at p. 442. Claims 30 and 32 were rejected as obvious over Rajan137 in view of Gervasi (US 2006/0259678) (Ex. 1013). *Id.* at pp. 442-43. Claims 8 and 22 were "objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims." *Id.* at p. 443.

73. On January 13, 2014, Applicant responded to the non-final Office Action by amending claims 8, 15-19, and 32, cancelling claims 5, 9, and 10, adding claims 35-37. Ex. 1002 at pp. 456-63. Applicant argued that Rajan137 did not anticipate the amended claims because Rajan137 "merely stacks DRAM circuits 206A-D, which are different from array dies." Ex. 1002 at p. 465. Applicant further contended that "[a]s a result, Rajan[137]'s buffer chip 202 also operates very differently from the control die in claim 1." *Id*. Applicant also provided the following arguments in response to the Examiner's rejection of claim 1:

> First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting claim 1, the Examiner states that Rajan (FIG. 2B) shows a memory package as recited in claim 1. The Examiner further cites Paragraph [0044] as disclosing the control die as recited in claim 1. Paragraph [0044] in Rajan, however, merely states:
>
> > As shown in each of such figures, the buffer chip 202 is placed electrically between an electronic host system 204 and a stack of DRAM circuits 206A-D. In the context of the present description, a stack may refer to any collection of memory circuits. Further, the buffer chip 202 may include any device capable of buffering a stack of circuits (e.g. DRAM circuits 206A-D, etc.). Specifically, the buffer chip 202 may be capable of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system 204. In this way, the stack of DRAM circuits 206A-D may appear as a smaller quantity of larger capacity DRAM circuits to the host system 204.

> Thus, the statements in this paragraph [0044] of Rajan says nothing about the existence of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals." According to this paragraph [0044], all that is required of the buffer chip 202 is the capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this requirement does not necessitate the use of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."
>
> Furthermore, according to paragraphs [0043] and [0044], this same capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system is required for each of the FIGS. 2A-2E, which show various configurations of a buffered stack of DRAM circuits 206A-D with the buffer chip 202. Since FIG. 2D of Rajan shows a single data bus between the buffer chip and all of the stacked DRAM circuits 206A-D (*Rajan, paragraph [0051]*), this capability of buffering the stack of DRAM circuits 206A-D, which also applies to the configuration in FIG. 2D, can not be said to imply the existence of first and second data conduits in the buffer chip 202 and a control circuit controlling the respective states of the first data conduit and the second data conduit in response to any received control signals, because the first and second data conduits would be coupled to a same data line in the single data bus in FIG. 2D and it would make no sense to try to control respective states or the first data conduit and the second data conduit.
>
> Therefore, Rajan fails to disclose each and every limitation in claim 1, and claim 1 is patentable over Rajan.

Ex. 1002 at pp. 465-67; *see also* Ex. 1011 (Rajan137) at Fig. 2D (discussed by applicant, reproduced below).

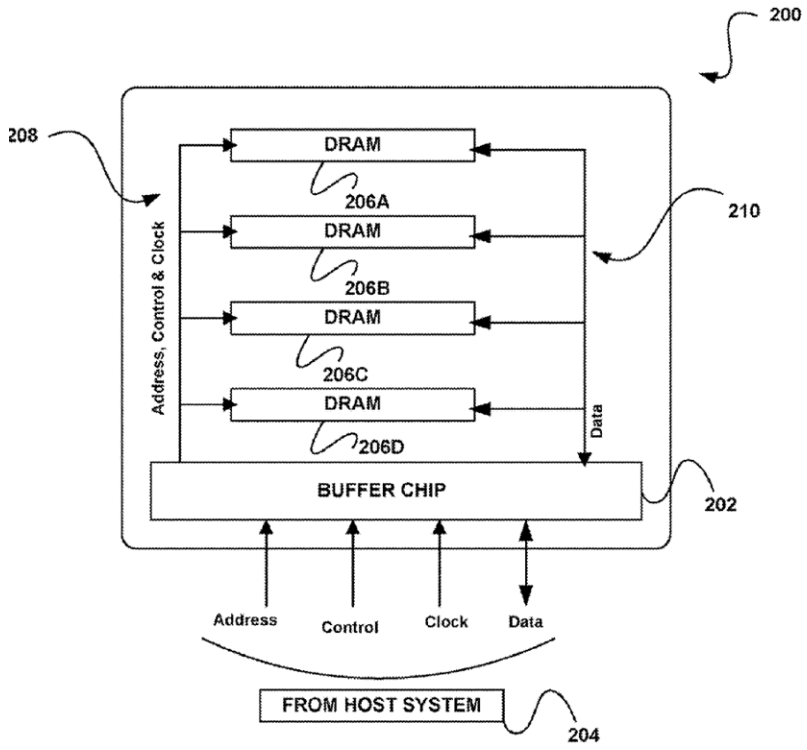


FIGURE 2D

74. On March 26, 2014, the Office issued a Notice of Allowance. Ex. 1002 at p. 474. The Examiner presented a few minor examiner's amendments but did not provide any statement on reasons for allowance. *Id.* at pp. 478-80.

75. On July 22, 2014, the 850 Application was issued as the 060 Patent with 34 claims. Ex. 1002 at pp. 483, 512; Ex. 1001 (060 Patent).

3. The Prosecution History of the July 21, 2014, continuation application that issued as U.S. Patent No. 9,318,160

76. While the application for the 060 Patent (discussed above) was pending, the applicants filed a continuation application on July 21, 2014, which resulted in U.S. Patent No. 9,318,160. *See* Ex. 1006 at pp. 56, 58. Thus, it shares

the same disclosure and named inventors as the 060 Patent. The application for the 160 patent presented 9 claims at filing. Ex. 1006 at pp. 42-44.

77. On January 22, 2015, in a non-final Office Action, the Examiner rejected all claims under a nonstatutory double patenting rejection over the 060 Patent's claims. Ex. 1006 at pp. 73-77.

78. On July 22, 2015, the applicants cancelled Claims 1-9 and presented new Claims 10-29 to the Office for consideration and filed a terminal disclaimer. Ex. 1006 at pp. 84-90, 96.

79. On October 22, 2015, in a final Office Action, the Examiner again rejected all pending claims, citing insufficiencies in the terminal disclaimer, specifically because "[t]he terminal disclaimer identifies a party who is not the applicant." Ex. 1006 at pp.112-119.

80. On January 6, 2016, the applicants filed a terminal disclaimer with documentation showing the chain of title to the new applicant. Ex. 1006 at pp. 131-137, 143, 159-60.

81. On February 10, 2016, the Office issued a Notice of Allowance for the application for the 160 patent. Ex. 1006 at p. 171. The Examiner made two minor corrections in an Examiner's Amendment but made no statement of reasons for allowance. *Id.* at pp. 176-78. The 160 patent issued on April 19, 2016. *Id.* at pp. 185, 199.

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4. The Prosecution History of the April 11, 2016 continuation that issued as U.S. Patent No. 9,659,601

82. While the application for the 160 patent (discussed above) was pending, the applicants filed a continuation application on April 11, 2016, which resulted in U.S. Patent No. 9,659,601. *See* Ex. 1007 at pp. 59, 62. As a continuation of the 160 patent, the application for the 601 patent shares the same disclosure and named inventors as the 160 patent. The application resulting in the 601 patent presented 5 claims at filing, 1-5. Ex. 1007 at pp. 45-46.

83. On May 11, 2016, in a non-final Office Action, all claims were rejected for indefiniteness and non-statutory double patenting over the 160 patent and the 060 Patent. Ex. 1007 at pp. 66-74.

84. On September 12, 2016, the applicants amended Claims 1-5, added new Claims 6-21, and filed a terminal disclaimer. Ex. 1007 at pp. 101-109, 117.

85. On October 6, 2016, in a final Office Action, all pending claims were again rejected for non-statutory double patenting. Ex. 1007 at pp. 126-132. In response, the applicants refiled a terminal disclaimer that same day. Ex. 1007 at pp. 137-139.

86. On January 6, 2017, the applicants amended Claims 12, 16, and 21 and pointed to the terminal disclaimer that had been approved. Ex. 1007 at pp. 142-148.

87. On January 27, 2017, the Office issued a Notice of Allowance. Ex. 1007 at p. 152. No reasons were given for the allowance. *Id.* at p. 156. On February 14, 2017, the Examiner submitted a Supplemental Notice of Allowability with an Examiner's Amendment. Ex. 1007 at pp. 176-79. On April 7, 2017, another Supplemental Notice of Allowability was mailed to the applicants in response to an IDS filed by the applicants on March 27, 2017. Ex. 1007 at pp.194-199.

88. U.S. Patent No. 9,659,601 issued from the 288 Application on May 23, 2017. Ex. 1007 at pp. 170, 208.

5. The Prosecution History of the May 22, 2017 continuation application that issued as U.S. Patent No. 10,290,328

89. While the application for the 601 patent (discussed above) was pending, the applicants filed a continuation application on May 22, 2017, which resulted in U.S. Patent No. 10,290,328. Ex. 1008 at pp.58, 62. The application resulting in the 328 patent presented 10 claims at filing. Ex. 1008 at pp. 44-45.

90. On July 27, 2017, in a non-final Office Action, Claim 9 was rejected for being indefinite and all claims were rejected for nonstatutory double patenting over the 601 patent, the 160 patent, and the 060 Patent. Ex. 1008 at pp. 65-73.

91. On December 27, 2017, the applicants amended Claims 1-4, 6-7, and 9 and presented new Claims 11-20 and filed terminal disclaimers. Ex. 1008 at pp. 80-90.

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92. On February 26, 2018, in a final Office Action, and the follow-on final Office Action on May 31, 2018, pending Claims 1-20 were again rejected on the grounds of nonstatutory double patenting over the 601 patent and 160 patent. Ex. 1008 at pp. 105-112, 115-126.

93. On July 2, 2018, the applicants responded to the Office Action and filed new terminal disclaimers. Ex. 1008 at pp. 129-140.

94. On August 1, 2018, a Notice of Allowance was sent to the applicants. Ex. 1008 at pp. 147-53.

95. On October 29, 2018, the applicants filed a Request for Continued Examination along with an Information Disclosure Statement with over 100 references. Ex. 1008 at pp. 162-184.

96. On December 26, 2018, another Notice of Allowance was sent to the applicants with no statement on reasons for allowability. Ex. 1008 at pp. 213-217. On March 26, 2019, the applicants submitted an Amendment after Notice of Allowance, making amendments to Claims 1, 10, 12, and 19. Ex. 1008 at pp. 271-278.

97. U.S. Patent No. 10,290,328 issued on May 14, 2019. Ex. 1008 at pp. 220, 282.

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6. The Prosecution History of the May 14, 2019 continuation application that issued as U.S. Patent No. 10,902,886

98. While the application for the 328 patent (discussed above) was pending, the applicants filed a continuation application on May 14, 2019, which resulted in U.S. Patent No. 10,902,886. *See* Ex. 1009 at pp. 59, 65. The application that resulted in the 886 patent presented 1 claim at filing. Ex. 1009 at p. 14.

99. On October 3, 2019, Claim 1 was rejected as failing to comply with the written description requirement regarding "a printed circuit board" and for nonstatutory double patenting over the 060 Patent, the 160 patent, the 601 patent, and the 328 patent. Ex. 1009 at pp. 103-111.

100. On March 3, 2020, the applicants cancelled Claim 1 and submitted new Claims 2-21. Ex. 1009 at pp. 132-141.

101. On June 9, 2020, in a final Office Action, all pending claims were rejected for nonstatutory double patenting in view of the 328 patent, the 601 patent, the 160 patent, and the 060 Patent. Ex. 1008 at pp. 182-191.

102. On September 9, 2020, the applicants submitted a terminal disclaimer as well as a McKesson Statement, pointing to Application No. 15/470,856 and 13/970,606 as applications potentially containing information relevant to the pending application. Ex. 1009 at pp. 206-216.

103. On September 17, 2020, the Office issued a Notice of Allowance. Ex. 1009 at pp. 219-25.

104. On November 23, 2020, the Office issued a Corrected Notice of Allowability. Ex. 1009 at pp. 261-64.

105. On December 16, 2020, the applicants amended Claim 19. Ex. 1009 at pp. 279-285, 294-95.

106. U.S. Patent No. 10,902,886 issued on January 26, 2021. Ex. 1009 at pp. 231, 299.

7. Application No. 17/157,903 (abandoned)

107. The applicants filed U.S. Patent Application No. 17/157,903 ("903 Application"), titled "Memory Module with Buffered Memory Packages," on January 25, 2021. Ex. 1010 at p. 61. The 903 Application is a continuation of the 885 patent. Ex. 1010 at pp. 6-7, 64. The 903 Application presented 1 claim at filing. Ex. 1010 at p. 57.

108. On May 12, 2021, the claim was rejected as being indefinite and for nonstatutory double patenting in view of the 060 Patent, the 160 patent, the 601 patent, the 328 patent, and the 886 patent. Ex. 1010 at pp. 83-90.

109. On September 13, 2021, the applicant responded by cancelling Claim 1, submitting new Claims 2-21, and submitting a terminal disclaimer. Ex. 1010 at pp. 105-113.

110. On December 13, 2021, Claims 5 and 16 were objected to because of informalities and all pending claims were rejected for nonstatutory double

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patenting over the 886 patent, the 601 patent, the 160 patent, and the 060 Patent. Ex. 1010 at pp.150-161.

111. The applicants did not respond to this rejection, and the application was deemed abandoned on July 6, 2022. Ex. 1010 at pp. 191-92.

E. Construction of Terms Used in the 060 Patent Claims

112. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the 060 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted some of the claim terms broadly for purposes of infringement, *see, e.g.*, Ex. 1044 at 63-68; Ex. 1046 at 63-69, and that a narrower interpretation may be more reasonable, in my opinion the claims are obvious under either interpretation, as shown by my analysis below.

113. I also understand that claim 7 may improperly include a method limitation (e.g., "wherein a first number of array dies … are selected in consideration of a load of the first die interconnect…") in an apparatus claim ("The memory package of claim 1…."). I understand that claiming both an apparatus, and method of using the apparatus, within a single claim, can make it unclear whether infringement occurs when one creates an infringing system, or whether infringement occurs when the user actually uses the system in an infringing

manner. But I do not believe this issue needs to be resolved for purposes of my invalidity analysis below, because regardless of whether claim 7 is interpreted as an apparatus claim or a mixed apparatus and method claim, in my opinion it is obvious in light of the prior art as discussed below.

IV. OVERVIEW OF THE PRIOR ART

114. Below is an overview of the primary prior art references that I considered when analyzing the validity of the claims of the 060 Patent.

A. Prior Art

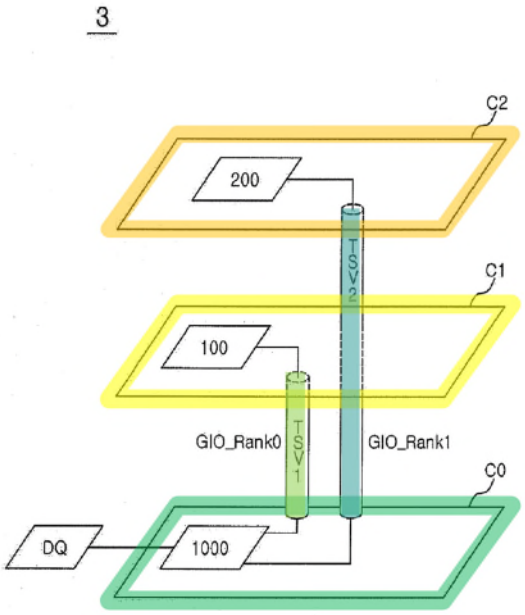
1. U.S. Patent Publication No. 2011/0103156 by Kim et al. (Ex. 1014)

115. U.S. Patent Application No. 12/648,997 by Kim et al. ("Kim"), titled "Data Input/Output Circuit and Semiconductor Memory Apparatus Having the Same," was filed on December 29, 2009, and was published as U.S. Patent Pub. No. 2011/0103156 on May 5, 2011. Ex. 1014 (Kim) at 1. Kim was not cited during prosecution of the 060 Patent. *See* Ex. 1001 (the 060 Patent) at 1-2 ("U.S. PATENT DOCUMENTS").

116. Kim discloses that "a semiconductor memory apparatus 3 comprises a main chip C0 [(green)] and a plurality of slave chips C1 [(yellow)] and C2 [(orange)]. The chips C0, C1 and C2 are connected by TSVs [(light green and teal, respectively)]." Ex. 1014 (Kim) at [0047] and Fig. 5 (reproduced below, annotated). Kim explains that, "[a]lthough only one main chip and two slave chips

are shown, it is to be understood that any number of main and slave chips may be used." *Id*. at [0048].

FIG.5

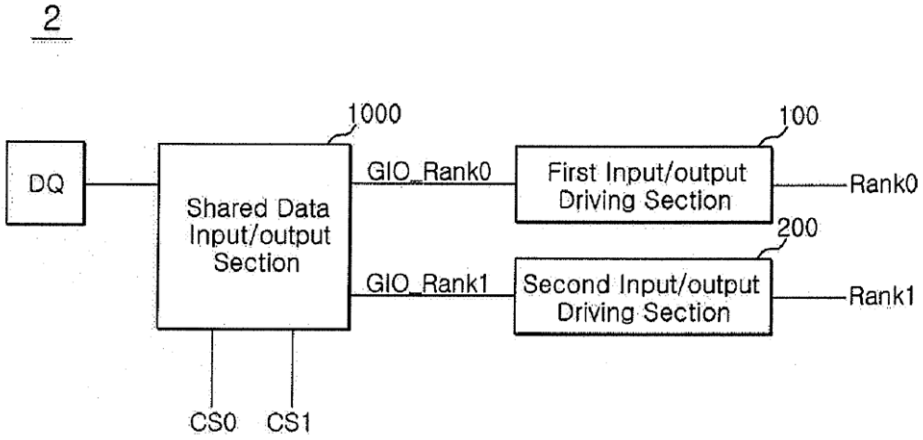


117. The main chip C0 (green) includes an input/output section (1000) that is shared by the slave chips C1 (yellow) and C2 (orange). Ex. 1014 (Kim) at [0048]. "When assuming that the first slave chip C1 is designated as the first rank Rank0 and the second slave chip C2 is designated as the second rank Rank1, the first chip selection signal CS0 becomes a signal for selecting the first slave chip C1, and the second chip selection signal CS1 becomes a signal for selecting the second slave chip C2. Data transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0 comprises a TSV TSV1 [(light green)]

which connects the first slave chip C1 and the main chip C0. Data transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1 comprises a TSV TSV2 [(teal)] which connects the second slave chip C2 and the main chip C0." *Id*. at [0049].

118. Kim also explains that its inventive "semiconductor memory apparatus 2 may allow a read operation and a write operation to be selectively performed for one of the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, whereby it is possible to prevent a data collision from occurring." Ex. 1014 (Kim) at [0031] and Fig. 2 (reproduced below).

FIG.2



2. U.S. Patent No. 8,041,881 to Rajan et al. ("Rajan") (Ex. 1015)

119. U.S. Patent No. 8,041,881 to Rajan et al. ("Rajan"), titled "Memory Device with Emulated Characteristics," issued on October 18, 2011, from U.S. Patent Application No. 11/762,010 filed on June 12, 2007. Ex. 1015 (Rajan) at p.1. A continuation of Rajan is U.S. Patent No. 8,019,589 which was cited but not discussed during prosecution of the 060 Patent. Ex. 1001 (the 060 Patent) at p.2. The Examiner cited and discussed a different patent application from the same inventors (US2008/0025137, Ex. 1011) with a different disclosure, as discussed above in ¶¶ 69-75.

120. Rajan is directed to "an effective way to make use of low cost memory chips in manufacturing high capacity memory modules," including the use of a memory device including stacked DRAM chips (yellow and orange) and a buffer chip (green) for interfacing with a host system. Ex. 1015 (Rajan) at 1:51-60, 4:48-50 and Fig. 4 (reproduced below, annotated). Rajan discloses a number of ways for connecting the stacked DRAM chips (yellow and orange) and the buffer chip (green), including using two data busses (light green and teal) and a common bus for address, control, and clock signals. *Id*. at 2:6-7.

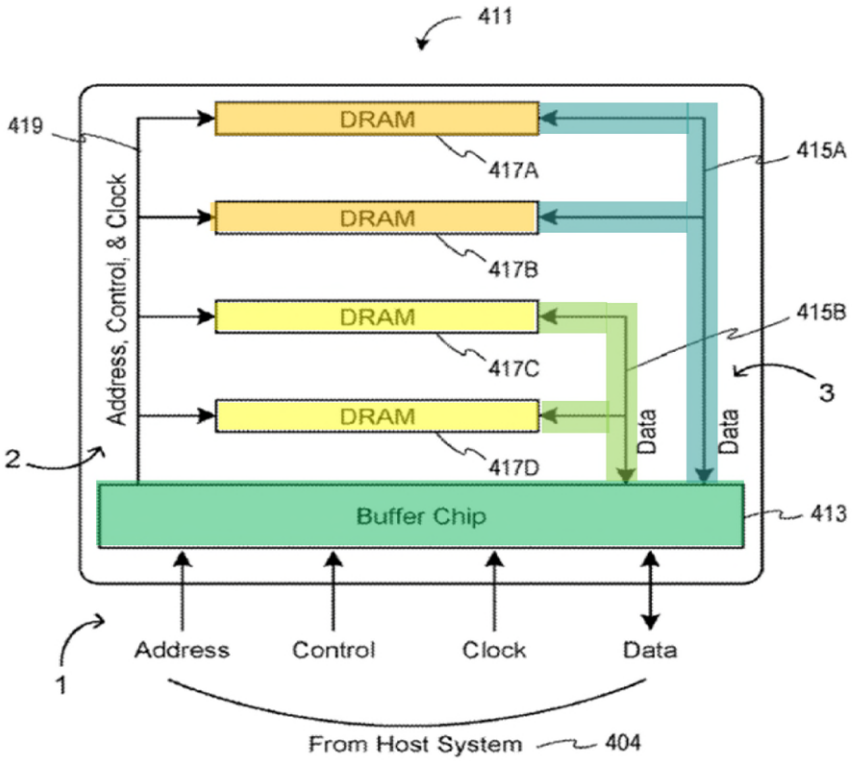


FIG. 4

121. Rajan further teaches that the interface may comply with JEDEC standards, and include "a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system, and a system data signal interface for sending/receiving data signals to/from the host system." Ex. 1015 (Rajan) at 4:20-24, 14:11-18 and Fig. 18 (reproduced below). Rajan also discloses that "[t]he interface circuit includes emulation logic which operates according to the stored memory physical attributes and the stored system emulation

attributes, to present to the system an interface to an emulated memory which differs in at least one attribute from the actual physical memory." *Id*. at 14:51-62.

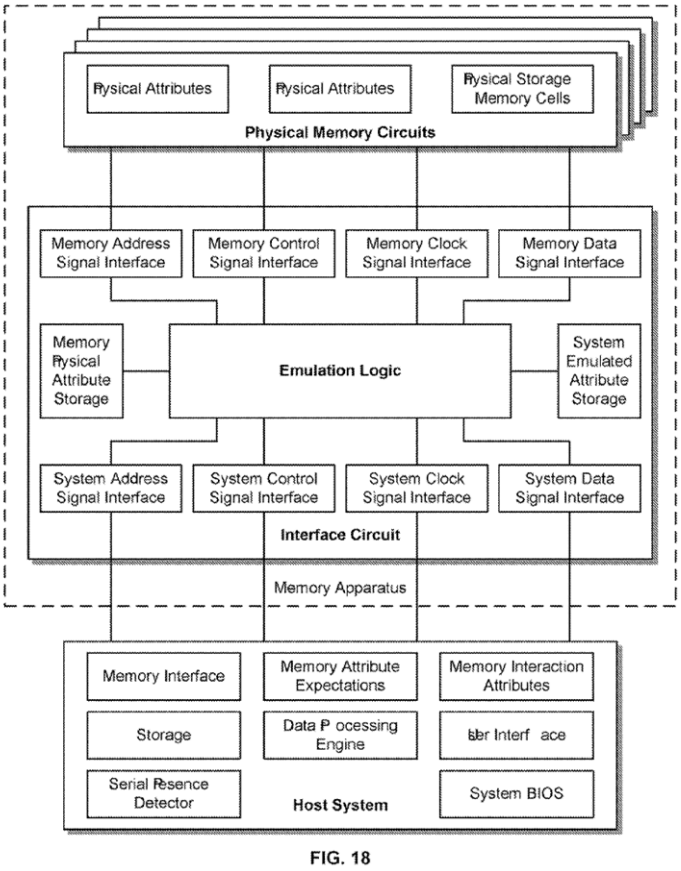


FIG. 18

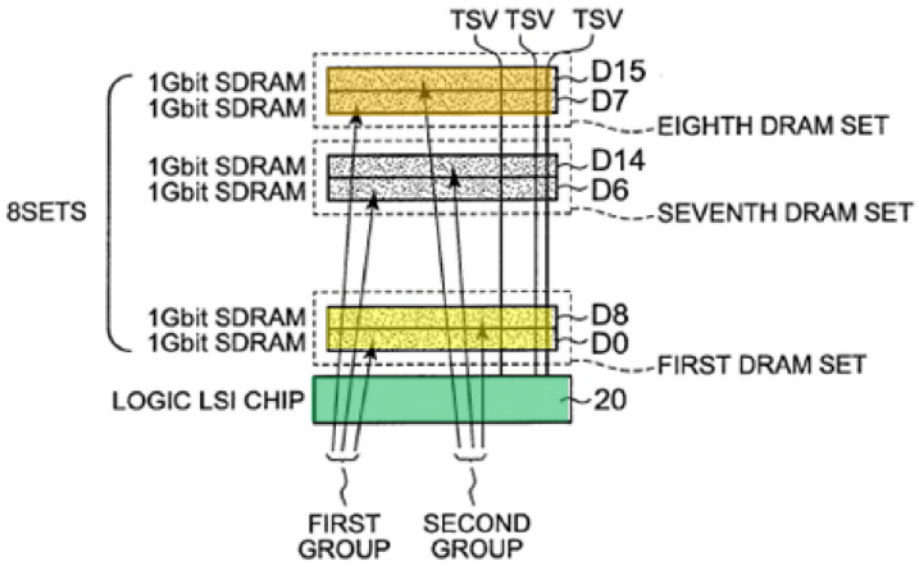
3. U.S. Patent Publication No. 2011/0026293 by Riho (Ex. 1016)

122. U.S. Patent Application No. 12/838,028 titled "Semiconductor Device" was filed on July 16, 2010, and published as U.S. Patent Publication No. 2011/0026293 by Riho ("Riho") on February 3, 2011. Ex. 1016 (Riho) at 1. Riho was not cited during prosecution of the 060 Patent. *See* Ex. 1001 (the 060 Patent) at 1-3 ("U.S. PATENT DOCUMENTS").

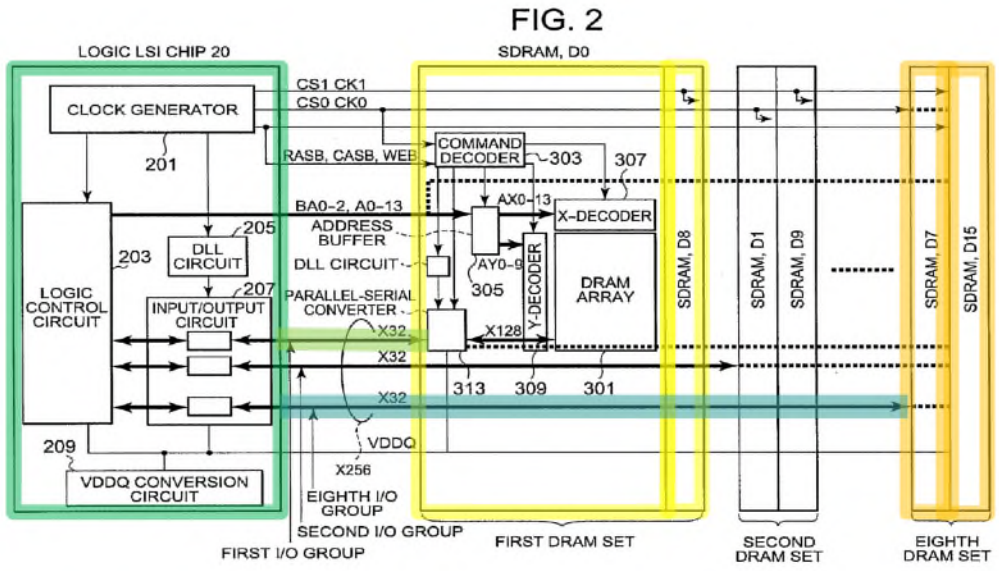
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123. Riho discloses a memory package including a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15) "integrally packaged" and connected to the control chip by through-silicon vias (TSVs). Ex. 1016 (Riho) at Fig. 1 (reproduced below, annotated).

FIG. 1



124. In particular, Riho discloses organizing the memory chips into pairs that share TSVs for data communication, such as a first DRAM set including SDRAM pair D0 and D8 (yellow) at the bottom of the stack up to the eighth DRAM set including SDRAM pair D7 and D15 (orange) at the top of the stack. *Id*. at Fig. 2 (reproduced below, showing internal structure of the stack, including (x32) data connections to SDRAM pair D0 and D8, light green, and to SDRAM pair D7 and D15, teal).

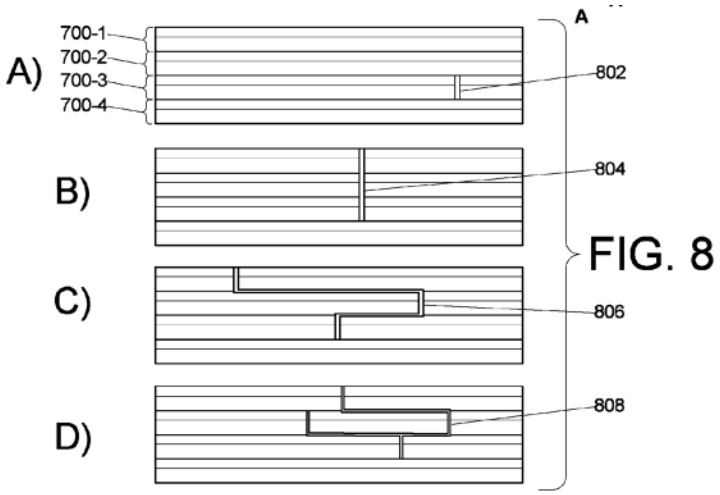


125. Riho explains that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 (Riho) at [0103]. Riho also discloses "a structure in which only either one of each of SDRAM pairs forming sets (DRAM sets) and sharing data signal DQ TSVs, respectively, is connected to the corresponding shared data signal DQ TSV while the other SDRAM is completely disconnected from the corresponding shared data signal DQ TSV, thereby not only compensating for phase variations of data signals DQ, but also reducing by half the load capacitance of data buses formed by the data signal DQ penetrating through electrodes TSV." *Id*. at [0110].

4. U.S. Patent No. 7,969,192 to Wyman et al. (Ex. 1017)

126. U.S. Patent No. 7,969,192 to Wyman et al. ("Wyman"), titled "Variable Off-Chip Drive," issued on June 28, 2011, from U.S. Patent Application No. 12/732916 filed on March 26, 2010, as a division of an application filed in 2007. Ex. 1017 (Wyman) at 1. Wyman was not cited during prosecution of the 060 Patent. *See* Ex. 1001 (the 060 Patent) at 1-2 ("U.S. PATENT DOCUMENTS").

127. Wyman discloses that, "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 (Wyman) at 1:22-24. "The reduced path distances of stacked hybridized chips therefore require less drive to adequately drive a signal to an off-chip board and/or chip. These conditions warrant the use of restructuring the drive portion of existing chip architecture." *Id*. at 1:45-48. For example, Wyman discloses that longer connections in a stacked arrangement require larger drive. *Id*. at Fig. 8 (reproduced below).



128. In particular, Wyman teaches that a short "through-chip via connection (802) … would require minimal drive" (Fig. 8A) but "a longer through-chip via connection (804)" (Fig. 8B) has "increased resistance, capacitance and impedance …[which] might require additional drive." Ex. 1017 (Wyman) at 6:15-30. However, "the total drive … would be overkill." *Id*. at 6:44-50.

5. U.S. Patent Publication No. 2010/0195364 by Riho ("Riho2") (Ex. 1018)

129. U.S. Patent Application No. 12/656,485 by Riho ("Riho2"), titled "Semiconductor Device," was filed on February 1, 2010, and was published as U.S. Patent Pub. No. 2010/0195364 on August 5, 2010. Ex. 1018 (Riho2) at 1. Riho2 was not cited during prosecution of the 060 Patent. *See* Ex. 1001 (the 060 Patent) at 1-2 ("U.S. PATENT DOCUMENTS"). The Riho and Riho2 references have the same named inventor.

130. Riho2 discloses "a semiconductor device formed by stacking a plurality of chip dies." Ex. 1018 (Riho2) at [0003]. Riho2 explains that "the

fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the fac[t] that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips." *Id*. at [0010].

131. To solve these problems, Riho2 discloses "a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097] and Fig. 7A (reproduced below).

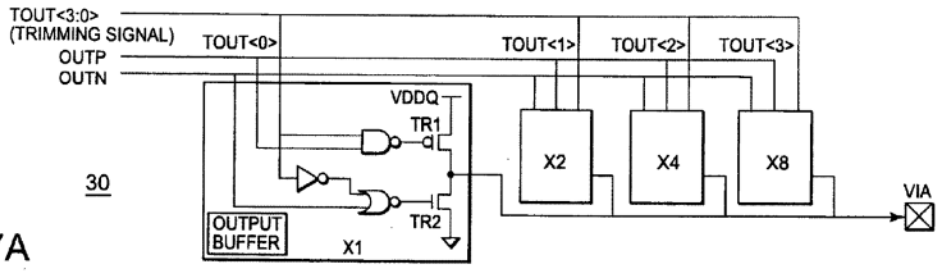


FIG. 7A

B. Background Technology

1. JEDEC Standards

132. In my opinion, a Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See supra* ¶ 60; Ex. 1023, p. 9 & Fig. 16; Ex. 1022, pp. 332-35, 318-20. For example, Riho discloses Double Data Rate (DDR) SDRAM memory devices. *See* Ex. 1016 at [0027]. A Skilled Artisan would have readily understood that these memories were already standardized by JEDEC. *See, e.g.,* Ex. 1015 (Rajan) at 8:6-15 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals that a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals. For example, the JEDEC specification for DDR2 DRAM is known as JESD79-2B.") A Skilled Artisan would have also understood that JEDEC also standardized memory modules and corresponding interface circuits, such as "a register, an AMB, a buffer, or the like." *Id*. at 4:20-24.

133. Furthermore, a Skilled Artisan would have also been familiar with the standard developing process at JEDEC, including proposals for the standards that were being developed at the time. Indeed, the 893 Provisional describes a "proposed three-dimensional stacking (3DS) standard for dual in-line memory

modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC)." Ex. 1005 (the 893 Provisional) at [0004]. The 893 Provisional also describes "a DDR3 JEDEC standard register with a 'rank multiplication' circuit" as part of the "proposed 3DS-DIMM standard" to address the shortcomings of the existing JEDEC RDIMM and LRDIMM standards for memory modules. *Id*. at [0005].

134. Therefore, in my opinion, a Skilled Artisan would have been familiar with the technology described in the JEDEC standards that existed and were being developed at the time. Examples of such standards include the JEDEC standard for DDR3 memory devices, *see* Exhibits 1019-21, and the JEDEC specification for GDDR4 memory devices, *see* Exhibit 1035.

2. Electrical load and drivers

135. In my opinion, a Skilled Artisan also would have been familiar with the electrical loads of circuitry used in stacked memory devices and the corresponding driving requirements to drive the load of such circuitry. For example, the 060 Patent's description of the prior art explains that, "[g]enerally, a load exists on each of the drivers 134, 140, 184, and 186 [in the control chip of the stack, *see supra* ¶61,] by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must

be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power." Ex. 1001 (the 060 Patent) at 2:8-15.

136. Indeed, a Skilled Artisan would have understood that a capacitive load creates timing delays that have to be taken into account when designing the corresponding driving circuits, as was taught in textbooks at the time. *See, e.g.,* Ex. 1030 (Brown) at 132-138. Consider, for example, "an inverter N_1 that drives the inputs of *n* other inverters. Each of the other inverters contributes to the total capacitive loading on node *f*. … For simplicity, assume that each inverter contributes a capacitance C and that $C_n = n \times C$ … [The result is that] the propagation delay increases in direct proportion to *n*." *Id*. at p.134 (Fig. 3.55, reproduced below).

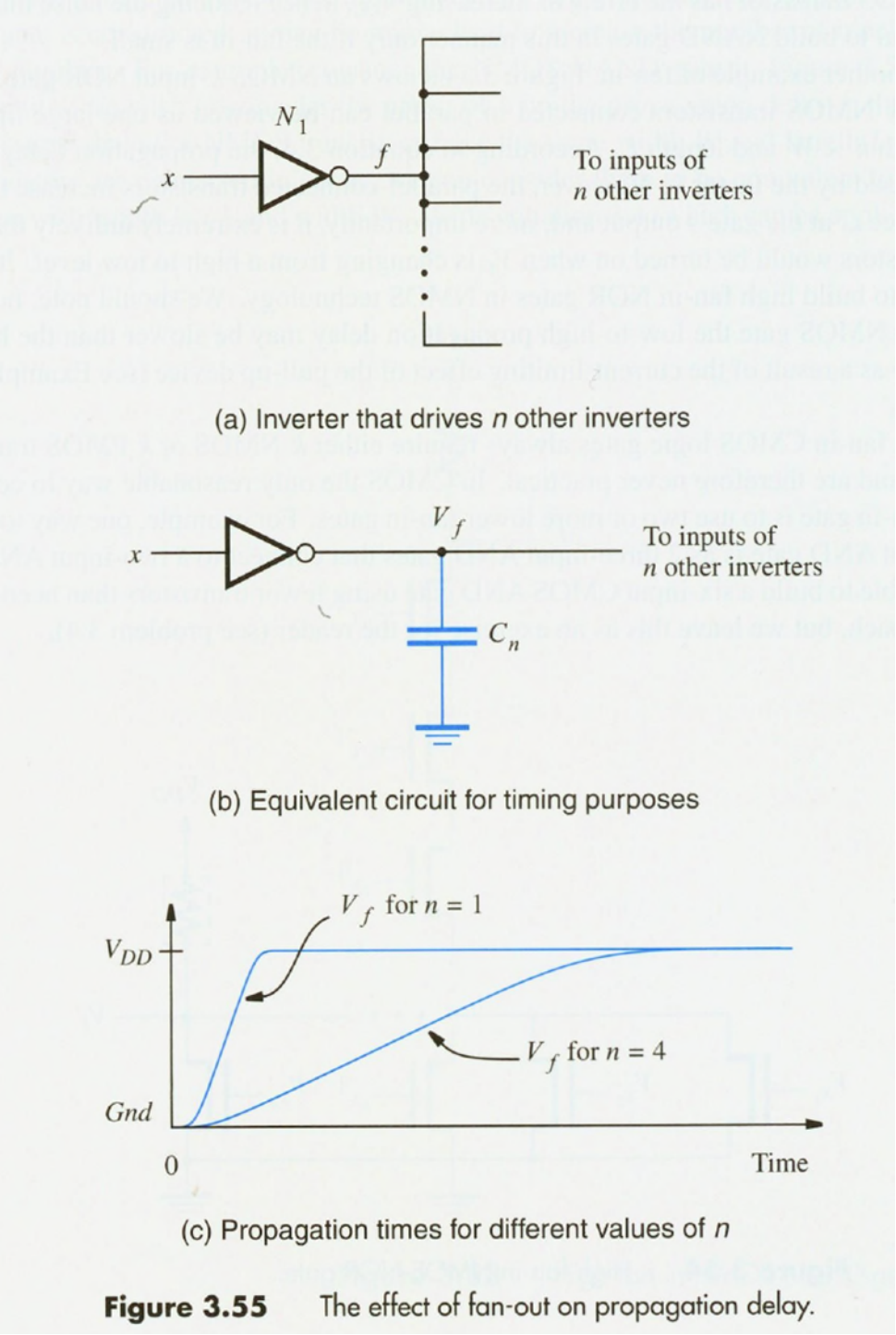


Figure 3.55 The effect of fan-out on propagation delay.

137. In order to "drive a large capacitive load, buffers are often used to improve performance." Ex. 1030 (Brown) at p.135. "Buffers can be created with different amounts of drive capability, depending on the sizes of the transistors ….

In general, because they are used for driving higher-than-normal capacitive loads, buffers have transistors that are larger than those in typical logic gates." *Id*. "In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices. Buffers can handle relatively large amounts of current flow because they are built with large transistors." *Id*. at 135-136. "In general, fan-out, capacitive loading, and current flow are important issues that the designer of a digital circuit must consider carefully. In practice, the decision as to whether or not buffers are needed in a circuit is made with the aid of CAD tools." *Id*. at 136. A well-known example of such buffers is a tri-state buffer, which has a third state that produces no output signal (called the "high-impedance state"). *Id*. at 136-138.

3. Rank multiplication

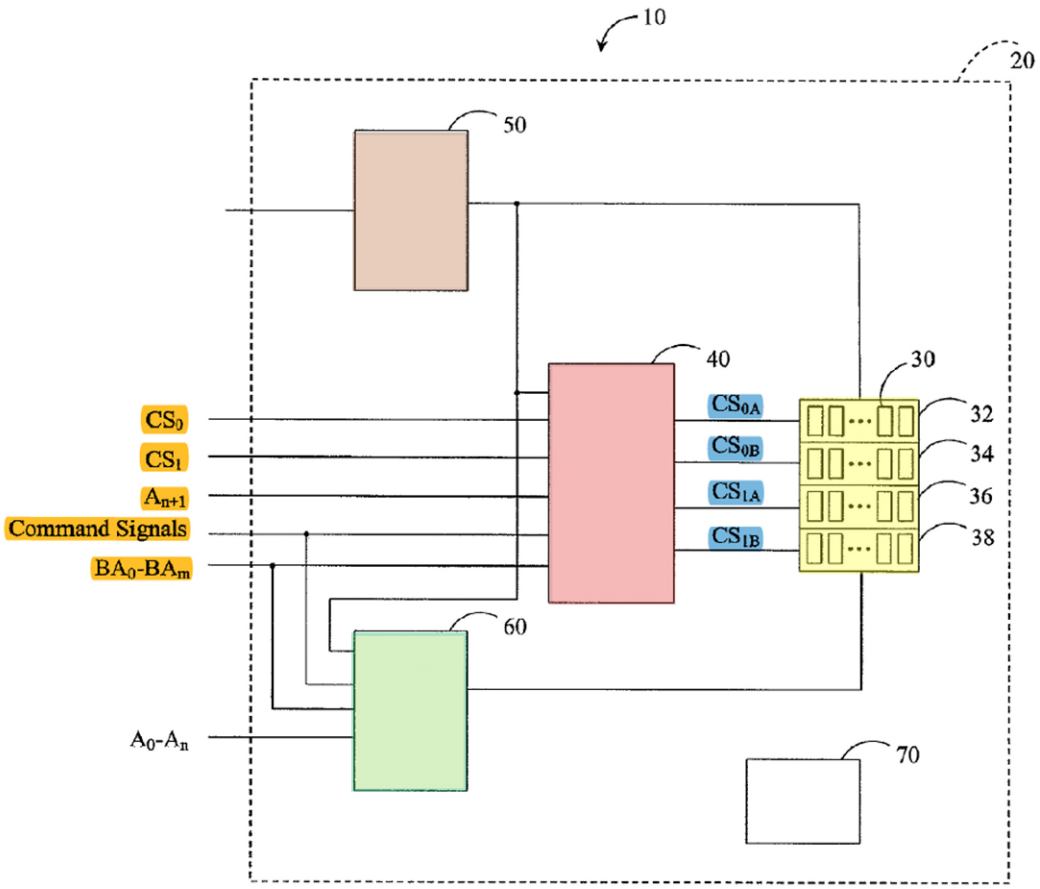
138. In my opinion, a Skilled Artisan also would have been familiar with "rank multiplication" at the time. For example, the 060 Patent discloses that rank multiplication was known at the time. Ex. 1001 (the 060 Patent) at 22:37-39 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537). For example, the '386 patent discloses that a memory module can appear to the computer system as if it has two ranks of higher density (and more expensive) memory devices complying with the JEDEC standard, when

in reality it physically has four ranks of lower density (and less expensive) memory devices. Ex. 1028, 4:47-5:10, 32:58-33:16; *see also* Ex. 1041 (Bigler) at 2:15-19 ("Thus, from an environment outside of the common package 140, the multi-die memory 100 may… appear as a single memory unit or as a monolithic memory unit.") and 2:36-40 ("According to some embodiments according to the invention, the distribution of the groups 160, 170 of memory banks may for example allow for an increase of a data rate on some data connections within the common package 140."). This is commonly called "rank multiplication," and can result in substantial cost savings, providing a motivation to implement the technique in a wide range of memory packages and memory modules. (Indeed, I understand that Patent Owner's claims in the '386 and '537 patents were found invalid by even earlier prior art rendering obvious "rank multiplication." *See* Exs. 1029, 1032-33.)

139. In particular, the '386 patent (Ex. 1028) discloses that "the ranks of a memory module are selected or activated by address and command signals," which include "chip-select signals." Ex. 1028 at 2:34-38. In the'386 patent, a memory module (10) can include a number of memory devices (30, yellow) and a logic element (40, red) which receives a set of input control signals (orange), including address signals and two chip select signals (CS_0, CS_1), from a system memory controller (not shown) complying with the JEDEC standard. Ex. 1028 at 5:11-50 and Fig. 1A (reproduced below, annotated); *see also id*. at 6:63-7:5. In response,

the logic element 40 generates four chip select signals (blue, CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) to control the memory devices 30 (yellow). *Id*. at 7:6-8:45.

Figure 1A:



140. Therefore, the ***two*** chip select signals received by the logic element 40 from the system memory controller correspond to ***two*** ranks, but the memory devices (yellow) on the module are organized into ***four*** ranks 32, 34, 36, 38, which each receive a respective one of the ***four*** chip select signals (blue) generated by the logic element (40). *Id*. For example, the additional chip select signals are generated based on an address signal (A_{n+1}). *Id*. at 8:1-45. The '386 patent also

explains that, to implement this rank multiplication, an isolation device is needed to avoid certain data collisions. Ex. 1028 at 24:41-56. Such an isolation device (120) can selectively isolate the load of the memory devices to "reduce the load impedance of the memory module 10 on the computer system." *Id*. at 26:12-19 and Fig. 6D (reproduced below); *see also* Ex. 1031 (the '537 patent) at 6:48-62.

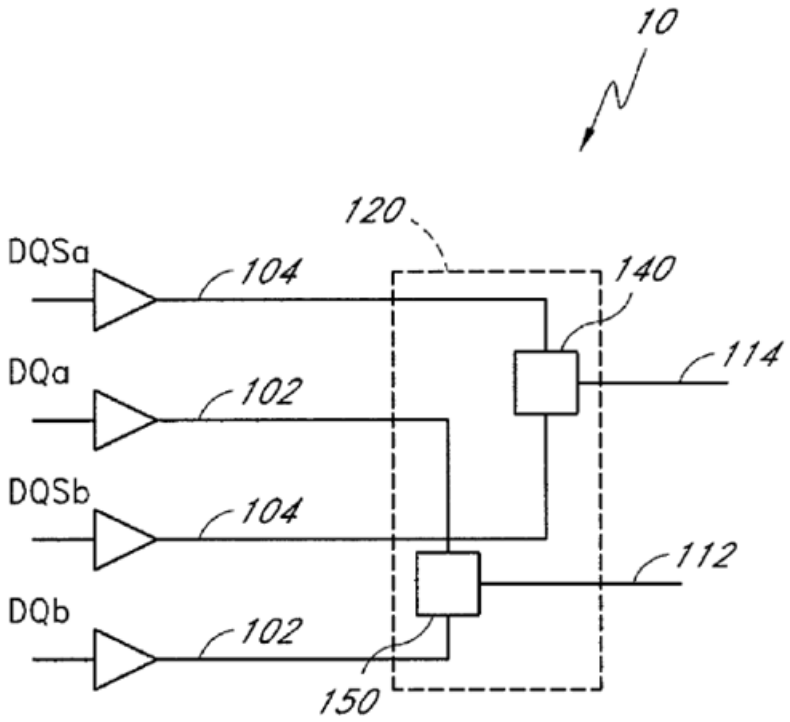


FIG. 6D

141. The '386 patent discloses an example where the rank multiplication is implemented in a logic device that can be combined with a register device and a PLL, but is a separate component from the memory devices. Ex. 1028 at 5:42-48 ("While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in

certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component."). A Skilled Artisan would have also understood that rank multiplication can be implemented within a single memory package. *See, e.g.,* Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack."); *see also* Ex. 1041 (Bigler) at 2:15-19 ("Thus, from an environment outside of the common package 140, the multi-die memory 100 may… appear as a single memory unit or as a monolithic memory unit."). Therefore, a Skilled Artisan would have also understood that rank multiplication can be implemented in either the memory package or in a separate module controller, or both. *See, e.g.,* Ex. 1001 (the 060 Patent) at Fig. 7 (reproduced below, showing a prior art module with rank multiplication implemented in both module controller 712 and memory package control chip 722) and 18:38-19:7 ("FIG. 7 schematically illustrates an example memory module 700 that has previously been proposed for the 3DS-DIMM standard. … The 3DS register 712 may include a DDR3 JEDEC standard

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register with a 'rank multiplication' circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller. … The 3DS DRAM package 720 may comprise a plurality of array dies (e.g., 2, 4 or 8 DDR DRAM dies) and a controller die 722. The controller die 722 may include … a programmable secondary 1-to-2 rank decoder …").

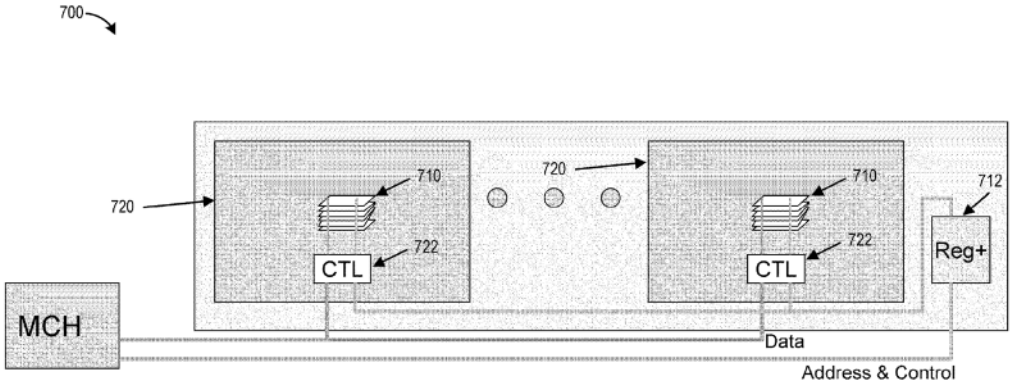


FIG. 7

C. The Combinations Relied on Here

142. The combinations analyzed here were obvious to a Skilled Artisan at the time and are straightforward applications of the teaching of the prior art. Each of the Grounds discussed below involves the combination of prior art references in view of the knowledge of a Skilled Artisan.

143. Ground 1 involves Kim in view of Rajan.

144. Ground 2 involves the references in Ground 1 (Kim in view of Rajan) in combination with Riho.

145. Ground 3 involves the references in Ground 1 (Kim in view of Rajan) in combination with Wyman.

146. Ground 4 involves Riho in view of Rajan.

147. Ground 5 involves the references in Ground 4 (Riho in view of Rajan) in combination with Riho2.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 060 PATENT

148. My analysis below is based on my understanding of the law and the other information discussed above, including the five Grounds discussed above.

A. Reasons to Combine for Grounds 1, 2, and 3

149. A Skilled Artisan would have been motivated to make the combinations in Grounds 1, 2 and 3 for at least the following reasons.

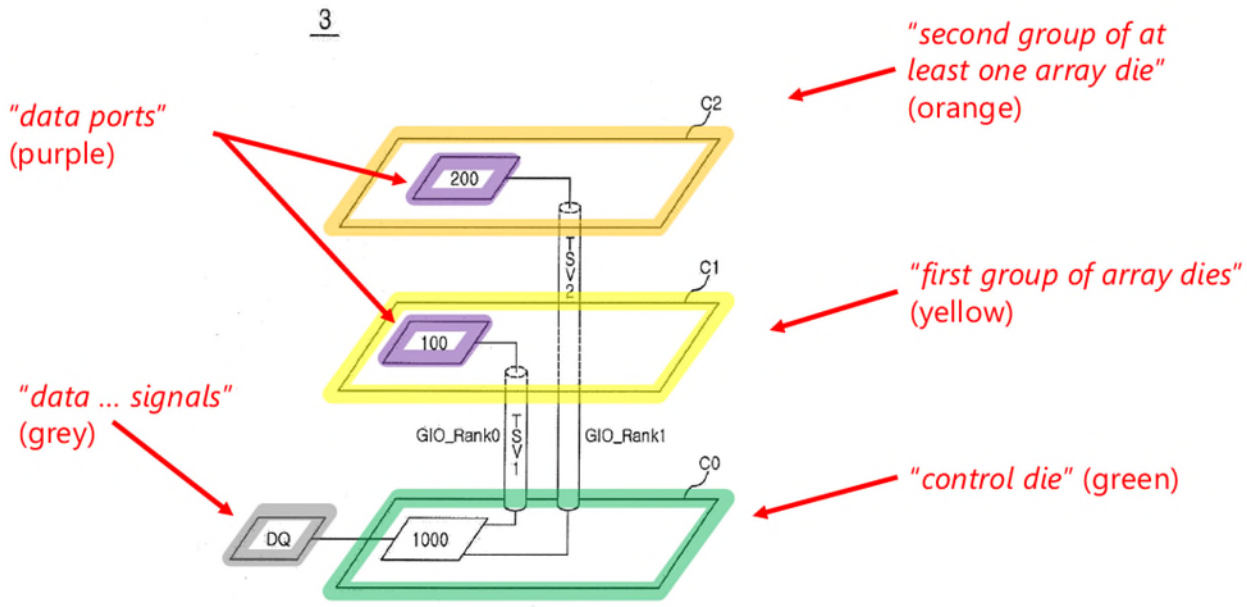
1. Ground 1: Kim in view of Rajan

150. As mentioned above, Ground 1 involves Kim in view of Rajan. *Supra* ¶143.

151. As discussed below in detail with reference to specific claim limitations, Kim discloses a memory package that includes stacked memory chips, like C1 (yellow) and C2 (orange), and a main chip C0 (green) including a shared data input/output section 1000. Ex. 1014 (Kim) at Fig. 5 (reproduced below,

annotated). Kim expressly discloses a data pad DQ (grey) to communicate data with external devices and further explains that "write and read command signals [are] applied from a device external to the semiconductor memory apparatus." *Id.* at [0038]. A Skilled Artisan would have understood from this disclosure that Kim's memory package includes "*input/output terminals"* to communicate "*data and control/address signals with one or more external devices*" as required by the 060 Patent claims.

FIG.5



152. Furthermore, the claimed terminals and corresponding data and control/address signals would have also been obvious over Kim in view of the teachings of Rajan. *See, e.g.*, Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, showing a memory package including stacked memory chips (yellow

and orange) and a buffer chip (green) which has input/output terminals for data and control/address signals communicated with a host system).

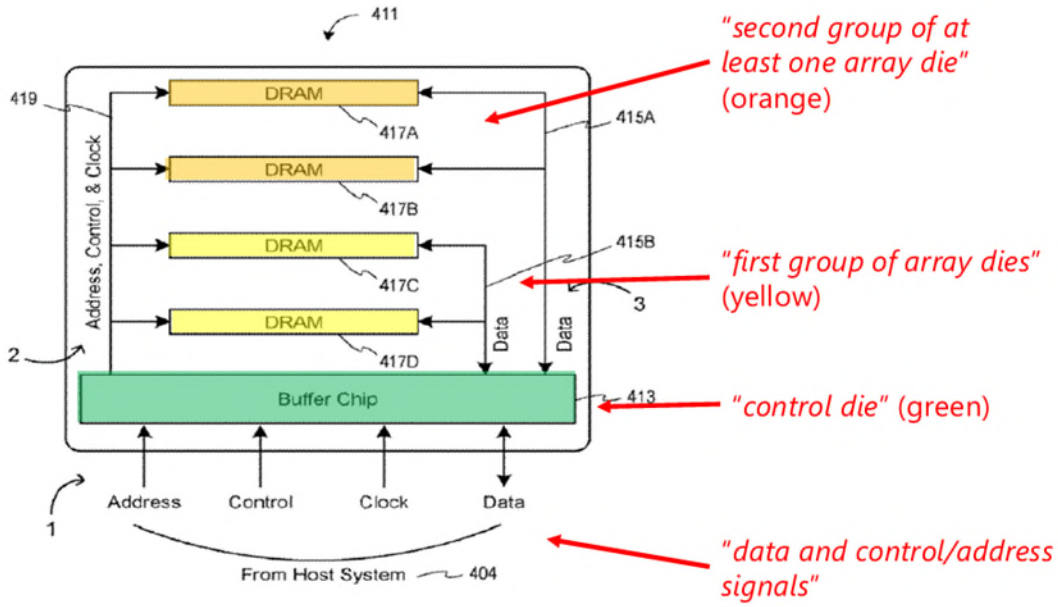


FIG. 4

153. For example, a Skilled Artisan would have been motivated to implement the functionality of a JEDEC compatible external interface as suggested by Rajan in the control chip of Kim to make Kim's stacked memory package compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory."); *see also id*. at Fig. 18 (reproduced below, disclosing that an

interface circuit includes emulation logic which interfaces, on one side with the host system and, on the other side, with the physical memory circuits).

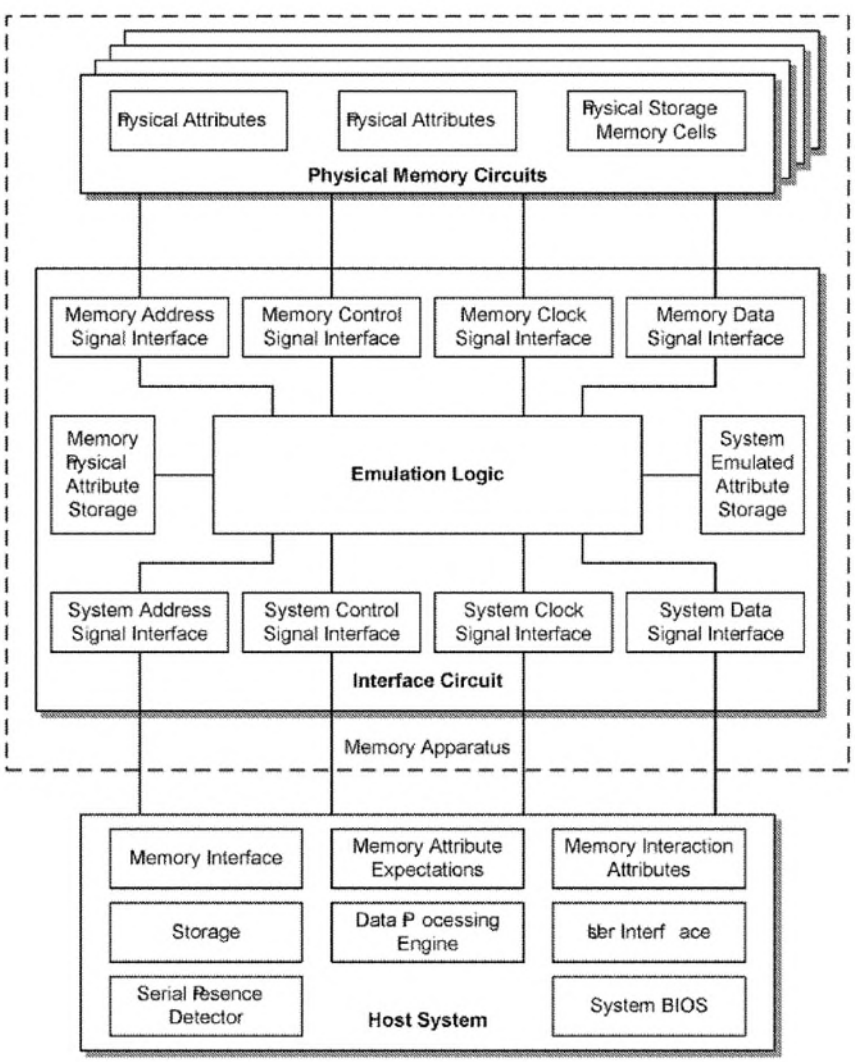


FIG. 18

154. Rajan is analogous art to Kim and the 060 Patent, as each is directed to the problem of effective operation of memory devices, including interfacing with stacked memory devices. Ex. 1015 (Rajan) at 1:51-60 ("What is needed, then, is an effective way to make use of low cost memory chips in manufacturing high capacity memory modules. … A memory subsystem is provided including an

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interface circuit adapted for communication with a system and a majority of address or control signals of a first number of memory circuits."), 4:48-50 ("In one embodiment, the DRAM chips are stacked, and the buffer chip is placed electrically between them and the host system."); Ex. 1014 (Kim) at [0012] ("Various aspects of the present invention comprise a semiconductor memory apparatus capable of sharing a data input/output circuit."), [0050] ("It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked."); Ex. 1001 (060 Patent) at 1:18-21 ("The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:23-26 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

155. Therefore, a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about control and address signals for memory packages. Rajan discloses the same basic structure of a memory package like Kim and the 060 Patent: the package includes stacked memory chips and a shared interface circuit, called "buffer chip" in Rajan. Ex. 1015 (Rajan) at Fig. 4

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(reproduced below, annotated), 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses.").

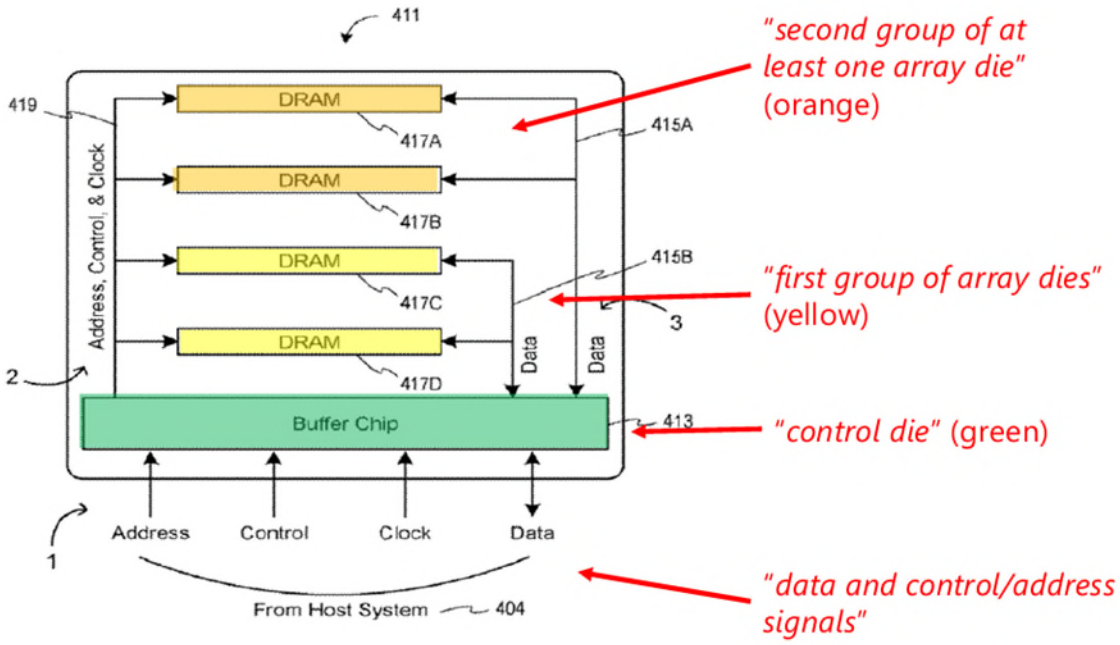


FIG. 4

156. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including the use of address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See,*

e.g., Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below).

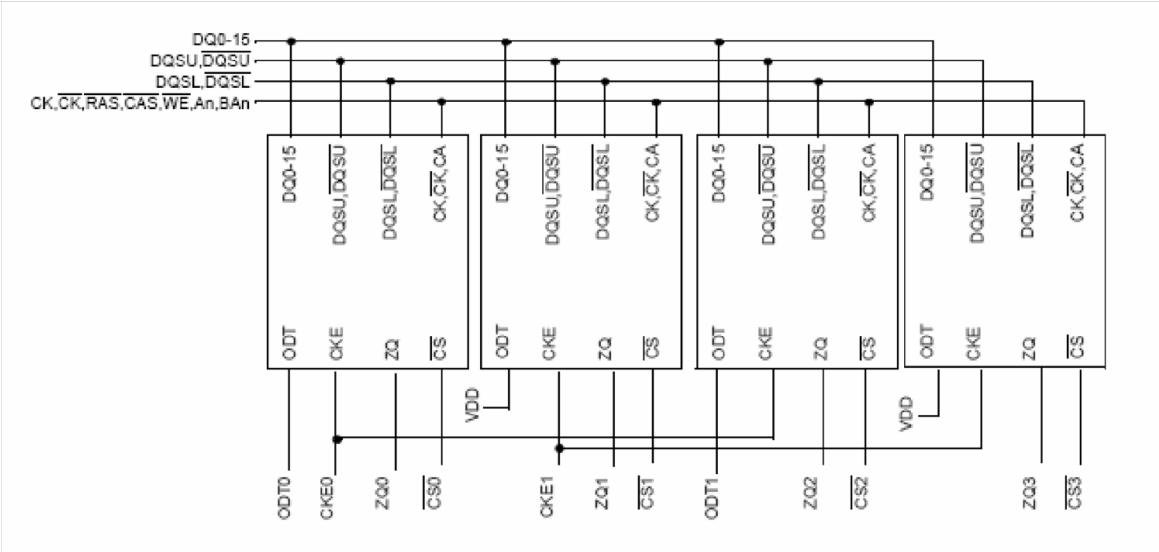


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

157. A Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control, and data terminals according to the JEDEC standards in Kim's memory package in order to use the package in JEDEC compliant systems. Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the prior art referenced in the 060 Patent. *See, e.g.*, Ex. 1001 (the 060 Patent) at 22:37-39 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat.

Nos. 7,289,386 and 7,532,537 ….”); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537). As discussed above, the JEDEC standards were influential and well known. *See supra* ¶¶ 132-134; Ex. 1022, pp. 332-35, 318-20.

158. Furthermore, Kim explains that, “although only one main chip and two slave chips are shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used.” Ex. 1014 (Kim) at [0048]; *see also id*. at [0050] (“It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked. While the semiconductor memory apparatuses having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks.”).

159. A Skilled Artisan would have understood from this disclosure that Kim’s invention can include more slave chips (and more ranks) and that some of those additional slave chips proposed by Kim can be in the same group as chips C1 or C2 and connected to TSV1 or TSV2, respectively. Furthermore, to the extent one might argue that Kim does not sufficiently disclose a group of multiple memory chips connected to the same TSV, it would have been obvious in light of Rajan, including Figure 4 of Rajan shown below.

160. As discussed above, both Rajan and Kim are analogous art to the 060 Patent, and a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about adding more chips (and ranks) in the stack as proposed by Kim. Ex. 1015 at Fig. 4 (reproduced below, annotated).

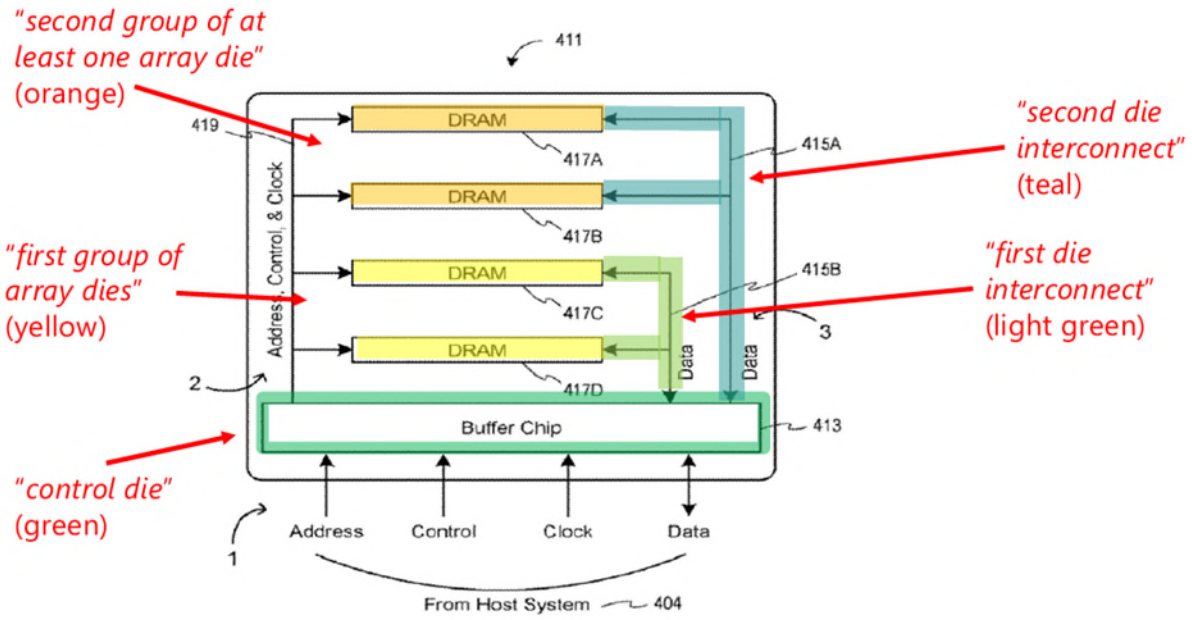


FIG. 4

161. For example, Rajan explains that "FIG. 4 illustrates another embodiment of a system 411 in which the buffer chip 413 is interfaced to a host system 404 and is coupled to the DRAM chips 417A-417D somewhat differently than in the system of FIG. 2 or 3. There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B. Each shared bus has two or more DRAM chips coupled to it." *Id.* at 5:36-43.

162. A Skilled Artisan would have also understood that creating such a shared data bus (415A, 415B above) as taught by Rajan was well within the level of skill at the time using, e.g., TSV interconnects like Kim. *See, e.g.*, Ex. 1025 (Foster) at Fig. 5 (reproduced below, annotated, showing two dies 21 and 22 (yellow) in a first substack being coupled to signal lines 68 by TSV 30, and two other dies 23 and 24 (orange) in a second substack being coupled to signal lines 70 using TSV 30 and pass-through vias PTV 29 which have no connection to circuitry in dies 21 and 22 in the first substack).

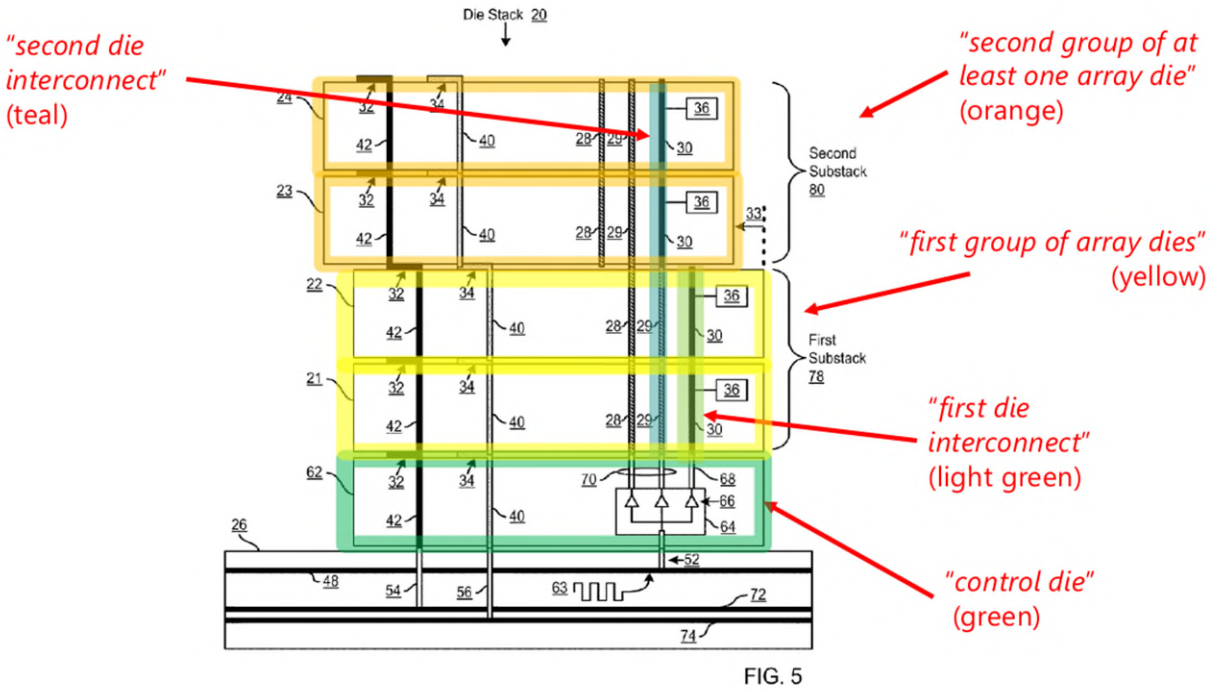


FIG. 5

163. Therefore, a Skilled Artisan would have understood that there were a finite number of known ways to connect the additional dies, including sharing a through-silicon via by a subset of the dies, so it would have been obvious to a

Skilled Artisan to follow this well know architecture when adding memory dies to the stack as suggested by Kim. *See*, *e.g.*, Ex. 1015 (Rajan) at Figs. 2-6 (describing a finite number of different interconnections of stacked memory chips).

164. Furthermore, a Skilled Artisan would have been motivated to connect the additional dies to the existing interconnects TSV1 or TSV2 in Kim's device, because such an arrangement could use Kim's chips without changing the number of interconnects TSV1 and TSV2, thus without creating new TSVs, which would require space and additional circuitry. Such a use of the interconnects TSV1 and TSV2 would also allow emulating certain characteristics required by external devices. Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 3:52-61 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory. The interface circuit may emulate an interface to one version of a protocol such as DDR2 with 5-5-5 latency timing, while the physical memory chips are built to another version of the protocol such as DDR2 with 3-3-3 latency timing. The interface circuit may emulate an interface to a memory having a first capacity that is different than the actual combined capacity of the physical memory chips.").

165. Indeed, a Skilled Artisan would have understood that Rajan's emulation techniques, including rank multiplication techniques, used "fork-in-the-road" arrangements where a two-rank arrangement has two data busses, and two more ranks can be added by sharing the existing two data busses of the two-rank arrangement. *See, e.g.*, Ex. 1026 (US 2006/0277355) at Figs. 12 and 13 (reproduced below, annotated, showing a switch ASIC connecting an 8-bit wide external DQ bus to two 8-bit wide internal busses DQA and DQB, and adding two more ranks in Figure 13 by sharing the DQA and DQB busses already used in the two-rank arrangement of Figure 12).

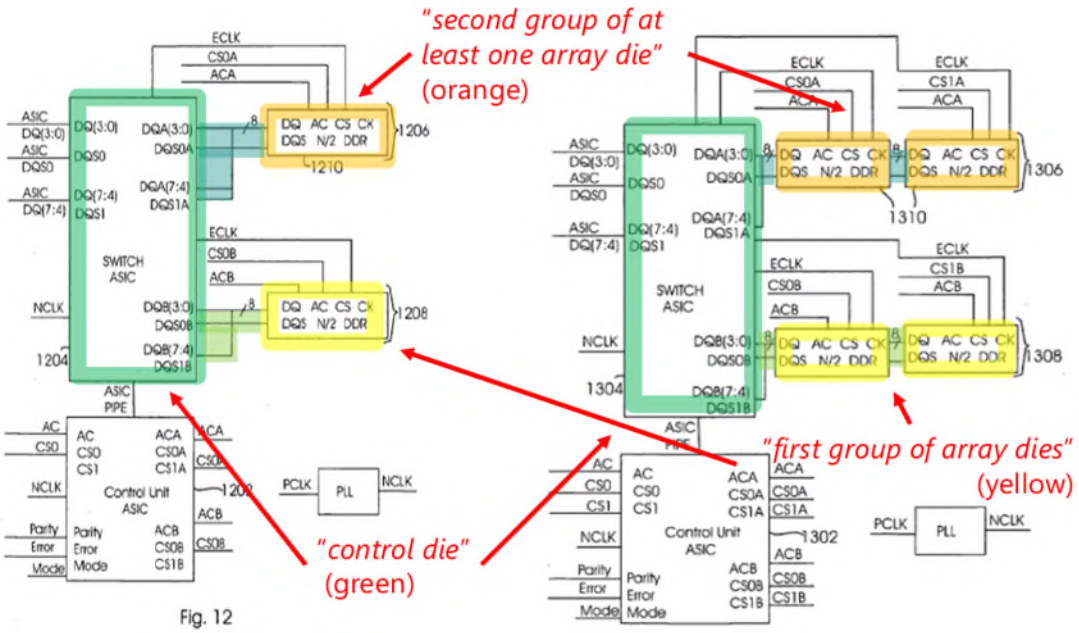


Fig. 12

Fig. 13

166. A Skilled Artisan's understanding that rank multiplication techniques used "fork-in-the-road" arrangements is further evidenced by the prior art

referenced in the 060 Patent. *See, e.g.*, Ex. 1001 (the 060 Patent) at 19:41-47, 22:34-57 (explaining that rank multiplication was well known prior art and incorporating by reference corresponding prior art patents disclosing fork-in-the-road arrangements, including Exhibits 1028 and 1031), 18:65-19:7 (describing prior-art memory package with a "programmable secondary 1-to-2 rank decoder" in the controller die of the memory package); *see also supra* at ¶¶138-141.

167. A Skilled Artisan would have been further motivated to use the interconnects TSV1 and TSV2 when adding more chips, because Kim explains that its structure of using two interconnects can avoid certain data collisions. Kim at Figs. 4A (explaining the problem of collision in the prior art), 4B (explaining the operation of the invention avoiding the collision), [0042-44] (same). Therefore, when adding more memory dies to Kim's stack, a Skilled Artisan would have been motivated to connect the additional dies to Kim's interconnects TSV1 and TSV2 as taught by Rajan to maintain Kim's data collision avoidance feature without creating additional TSVs.

168. For at least all these reasons, it would have been obvious to a Skilled Artisan to combine the teaching of Kim and Rajan to implement Kim's stacked memory package with the functionality of Rajan's interface circuit and inter-die connections.

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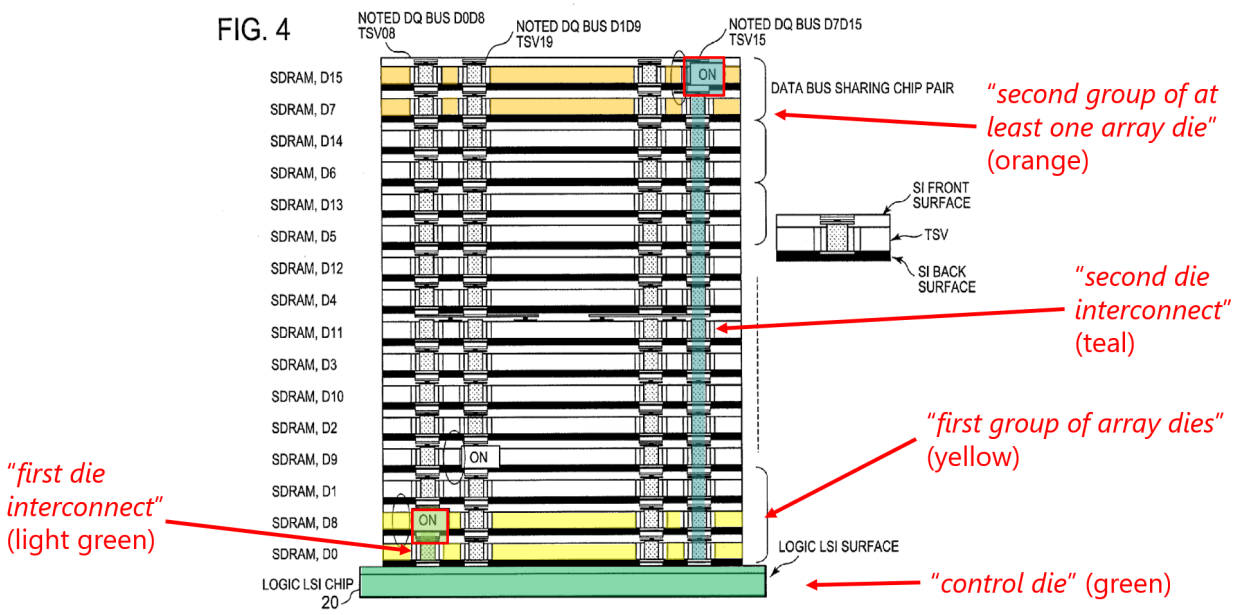
2. Ground 2: Ground 1 in view of Riho

169. As mentioned above, Ground 2 involves Ground 1(Kim in view of Rajan) in combination with Riho. *Supra* ¶144.

170. As discussed above in the combination of Ground 1, *supra* at ¶158, Kim explains that, "although only one main chip and two slave chips are shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used." Ex. 1014 (Kim) at [0048]; *see also id.* at [0050]. Therefore, a Skilled Artisan would have been motivated to look at analogous art for details about organizing memory stacks that include more than two memory chips as proposed by Kim.

171. Riho is analogous art to Kim, Rajan, and the 060 Patent, because Riho is also directed to the problem of effective operation of stacked memory devices. Ex. 1016 (Riho) at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips."). Riho discloses the same basic structure of a memory package like Kim, Rajan, and the 060 Patent: the package includes stacked memory chips and a shared interface circuit, called "logic LSI chip" in Riho. Ex. 1016 (Riho) at Fig. 4 (reproduced below, annotated), [0062] ("As shown in FIG. 4, the 16 SDRAMs D0, D8, D1, D9, D2, D10, D3, D11, D4,

D12, D5, D13, D6, D14, D7, and D15 are stacked in this order on the logic LSI chip 20.").



172. In particular, Riho discloses data sharing memory chip pairs, such as SDRAM pair D0 and D8 at the bottom of the stack (yellow), coupled to DQ bus D0D8 including TSV08, and SDRAM pair D7 and D15 at the top of the stack (orange), coupled to DQ bus D7D15 including TSV15. *Id.* Furthermore, Riho discloses that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 (Riho) at [0103]. Riho also discloses "a structure in which only either one of each of SDRAM pairs forming sets (DRAM sets) and

sharing data signal DQ TSVs, respectively, is connected to the corresponding shared data signal DQ TSV while the other SDRAM is completely disconnected from the corresponding shared data signal DQ TSV, thereby not only compensating for phase variations of data signals DQ, but also reducing by half the load capacitance of data buses formed by the data signal DQ penetrating through electrodes TSV." *Id*. at [0110].

173. Therefore, a Skilled Artisan would have been motivated to implement the data sharing memory chip pairs of Riho when adding more memory chips to the stack of Kim in order to reduce the load and compensate for phase variations as taught by Riho. For example, Riho explains in detail "the advantages in the write operation … [where the] load capacitance to 256 data signals DQ is reduced by half. Accordingly, the operating current is reduced and the high-frequency operation is achieved. Further, load capacitance variations of the data buses caused by a capacitance variation of (2±0.5) pF possessed by each DQ pin are also reduced. Therefore, SDRAM input set-up and hold margin are increased." Ex. 1016 (Riho) at [0119]; *see also id*. at [0120] (discussing advantages for read operation). As evidenced by Riho's disclosure, making such a combination was well within the level of skill and would have provided the predictable, advantageous result of having less phase variations and reduced load on the shared TSVs without the need of creating new TSVs for the additional memory chips.

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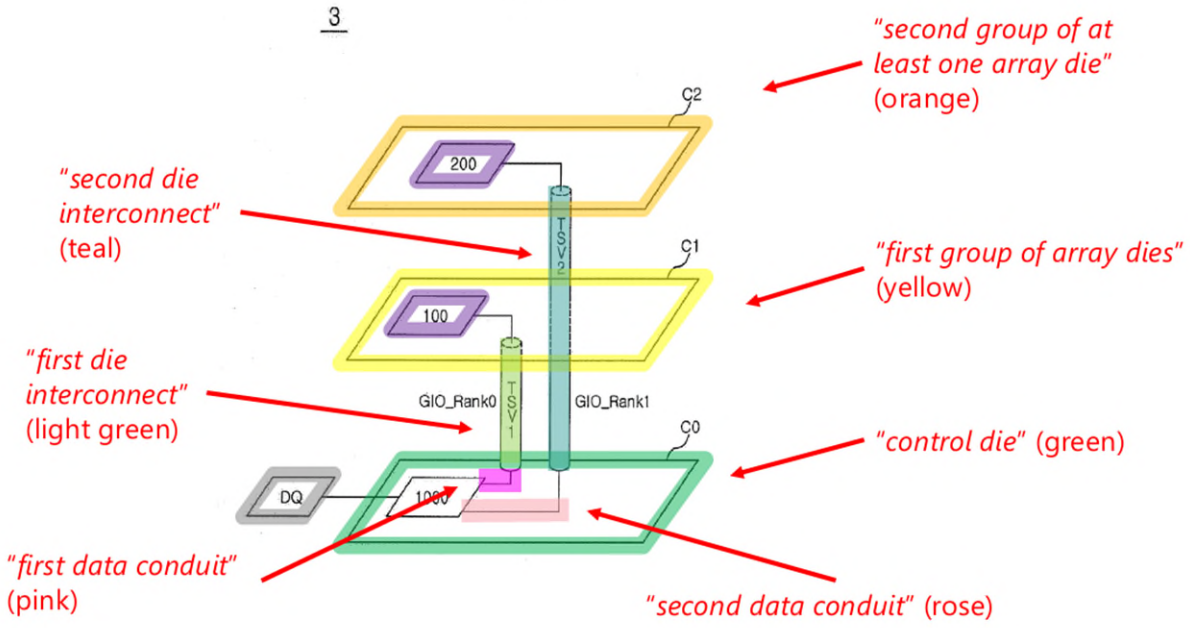
3. Ground 3: Ground 1 in view of Wyman

174. As mentioned above, Ground 3 involves Ground 1 (the combination of Kim and Rajan) in view of Wyman. *See supra* ¶145.

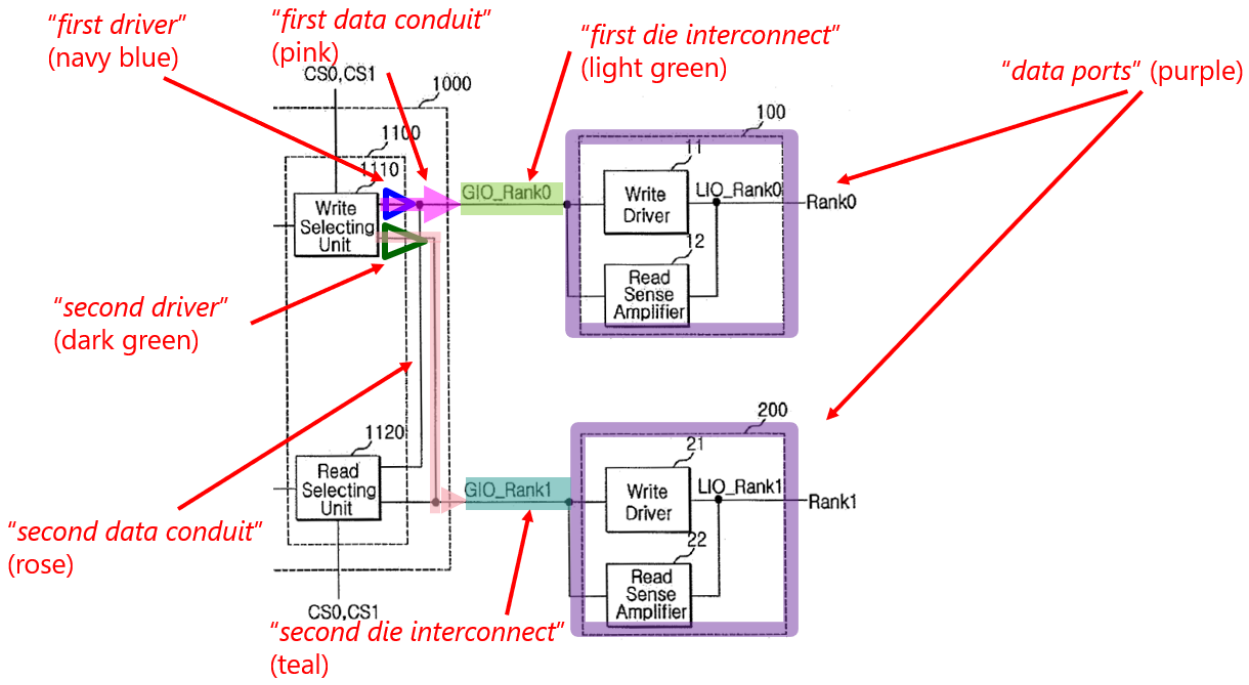
175. Wyman teaches to save power by using drivers that depend on the length (and load) of the connection in the stack. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.").

176. As expressly shown in annotated Fig. 5 of Kim (reproduced below), Kim discloses that TSV1 ("*first die interconnect*," light green) is shorter than TSV2 ("*second die interconnect*," teal). Ex. 1014 at Fig. 5 (reproduced below, annotated).

FIG.5



177. A Skilled Artisan would have understood that, due to the difference in length between TSV1 and TSV2, each of the "*first data conduit*" (pink) and the "*second data conduit*" (rose) can include a respective driver that is optimized for driving the data signal through the corresponding TSV in an efficient way. For example, Wyman explains that "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 (Wyman) at 1:22-24. Therefore, a Skilled Artisan would have been motivated to follow the teaching of Wyman in the system of Kim and, instead of using a full capacity driver to drive both TSV1 and TSV2, implement a respective driver for each of TSV1 and TSV2 that is optimized for the length of the corresponding TSV as illustrated in annotated Fig. 3 of Kim. Ex. 1014 (Kim) at Fig. 3 (reproduced below in part, annotated, showing a "*first driver*," navy blue, corresponding to TSV1 and a "*second driver*," dark green, corresponding to TSV2). Implementing Kim's system in this manner avoids the "wasteful and inefficient" use of power as taught by Wyman.



178. Wyman is analogous art to the 060 Patent and Kim, as each is directed to the problem of efficient signaling between chips in a stacked arrangement. Ex. 1017 (Wyman) at 1:45-48 ("The reduced path distances of stacked hybridized chips therefore require less drive to adequately drive a signal to an off-chip board and/or chip. These conditions warrant the use of restructuring the drive portion of existing chip architecture."); Ex. 1001 (the 060 Patent) at 1:19-21 ("More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:23-26 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS)."); Ex. 1014 (Kim) at [0003] ("Various embodiments of the present disclosure generally relate to a semiconductor memory apparatus, and more particularly, to data input/output of a

semiconductor memory apparatus."), [0046] ("In order to increase the integration of a semiconductor apparatus, a three-dimensional (3D) semiconductor apparatus comprising a plurality of stacked chips has been developed. The stacked chips provide a structure that enables the 3D semiconductor apparatus to be packages in a single package. Recently, a through-silicon via (TSV) type semiconductor apparatus has been developed in which silicon vias are formed to pass through the plurality of stacked chips so that all of the chips are electrically connected to one another.").

179. A Skilled Artisan would have understood, and been motivated, to turn to analogous art, like Wyman teaching about efficiently driving signals between stacked devices, in order to implement the stacked devices of Kim. For example, Wyman discloses that longer connections in a stacked arrangement require additional drive. *See, e.g.*, Ex. 1017 (Wyman) at Fig. 8 (reproduced below).

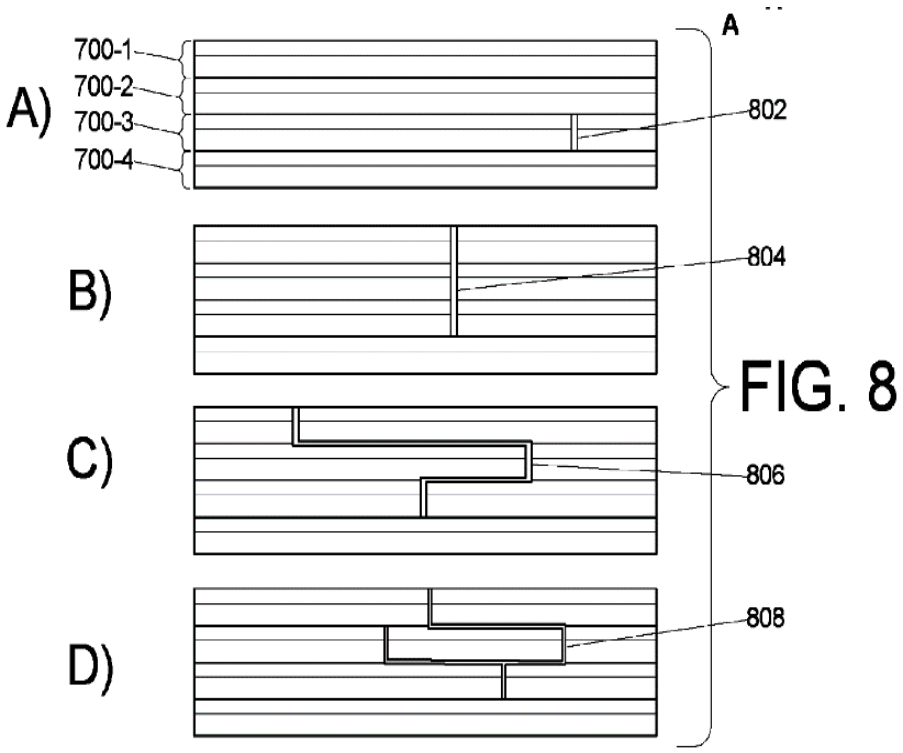


FIG. 8

Wyman explains that "FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3) … requir[ing] minimal drive … FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. …" *Id*. at 6:15-30. Thus, "the output drive current [can] be modified to meet the requirements of a particular output load." *Id.* at 7:13-18. However, Wyman recognizes that even with the "significantly longer connection (808) between the mother chip (700-4) with a fan

out to both daughter 2 (700-2) and daughter 3 (7001)," as shown in Fig. 8.D, using "the total drive … would be overkill." *Id.* at 6:44-50.

180. A Skilled Artisan would have understood from this disclosure that the longer the connection in a stack of chips, the more drive it requires, but using the "total drive" would be wasteful. Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use drivers of different strengths (i.e., a "*first driver*" having a "*first driver size*" and a "*second driver*" having a "*second driver size*") for Kim's different sized through-silicon vias TSV1 and TSV2. *See also supra* at ¶¶135-137 (explaining that different strengths are achieved by transistors of different sizes). In particular, a Skilled Artisan would have been motivated to drive the shorter TSV1 with a smaller driver and the longer TSV2 with a larger driver in order to use power in an efficient manner as taught by Wyman. Making such a combination was well within the level of skill, since Wyman itself teaches drivers of different sizes, and the combination would have provided nothing more than expected, a power efficient drive of signals through Kim's TSVs.

181. Therefore, it would have been obvious to a Skilled Artisan to implement Wyman's teaching of using drivers optimized for the length of the corresponding die interconnects in the memory package of Kim to save power.

B. Claims 1-34 Are Unpatentable Over Grounds 1-3

182. As explained below, claims 1-6, 8-14, 16-19, and 29-34 are unpatentable over Ground 1 (Kim in view of Rajan); claims 1-14, 16-19, and 29-34 are unpatentable over Ground 2 (Ground 1 in view of Riho); and claims 1-6 and 8-34 are unpatentable over Ground 3 (Ground 1 in view of Wyman).

1. Claim 1 is Unpatentable

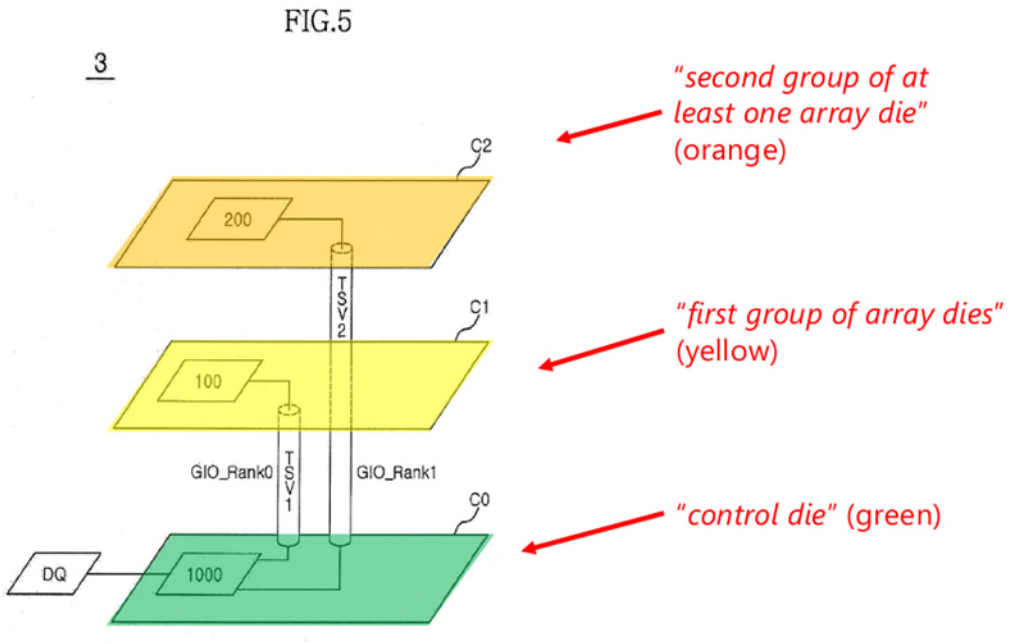
183. Claim 1 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [1.a] Preamble

184. The preamble of claim 1 requires "*[a] memory package, comprising*."

185. Kim discloses a "*memory package*" including main chip C0 and stacked memory chips C1 and C2 as illustrated in Kim's Fig. 5. *See* Ex. 1014 at Fig. 5 (reproduced below, annotated).

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186. For example, Kim explains that "a semiconductor memory apparatus 3 comprises a main chip C0 and a plurality of slave chips C1 and C2. The chips C0, C1 and C2 are connected by TSVs." Ex. 1014 at [0047]. Kim further explains that these "stacked chips provide a structure that enables the 3D semiconductor apparatus to be package[d] in a single package." *Id*. at [0046].

187. Therefore, Kim discloses a "*memory package.*"

188. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 1-3 satisfy "*[a] memory package, comprising*."

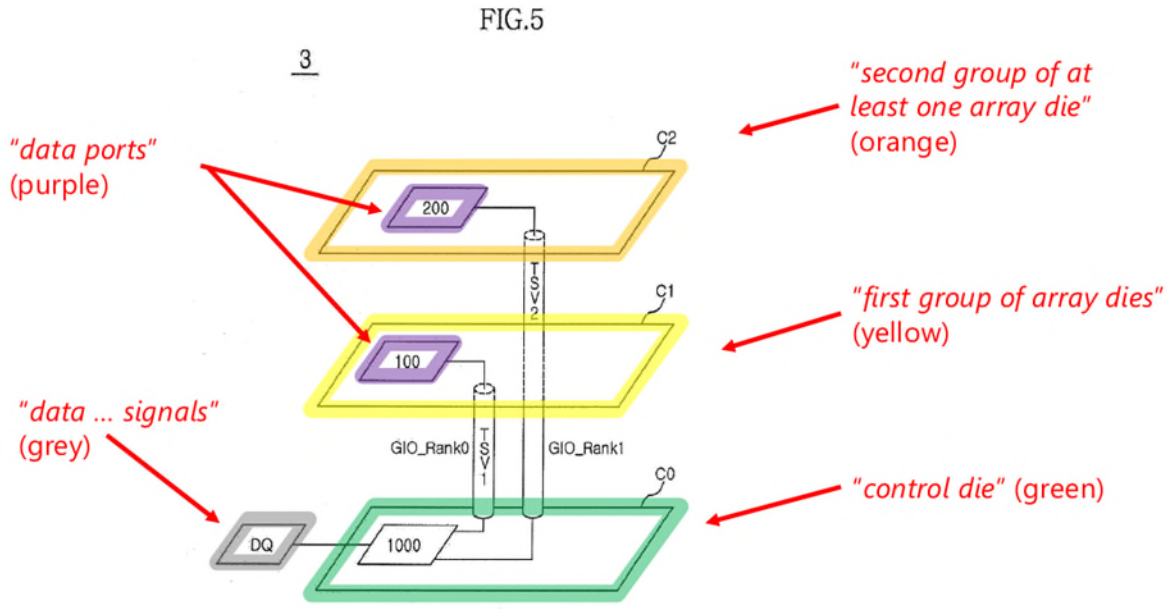
b) [1.b] Input/Output Terminals

189. Claim 1 requires "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices.*"

190. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

191. Kim discloses to a Skilled Artisan that the stacked package of Fig. 5 includes "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

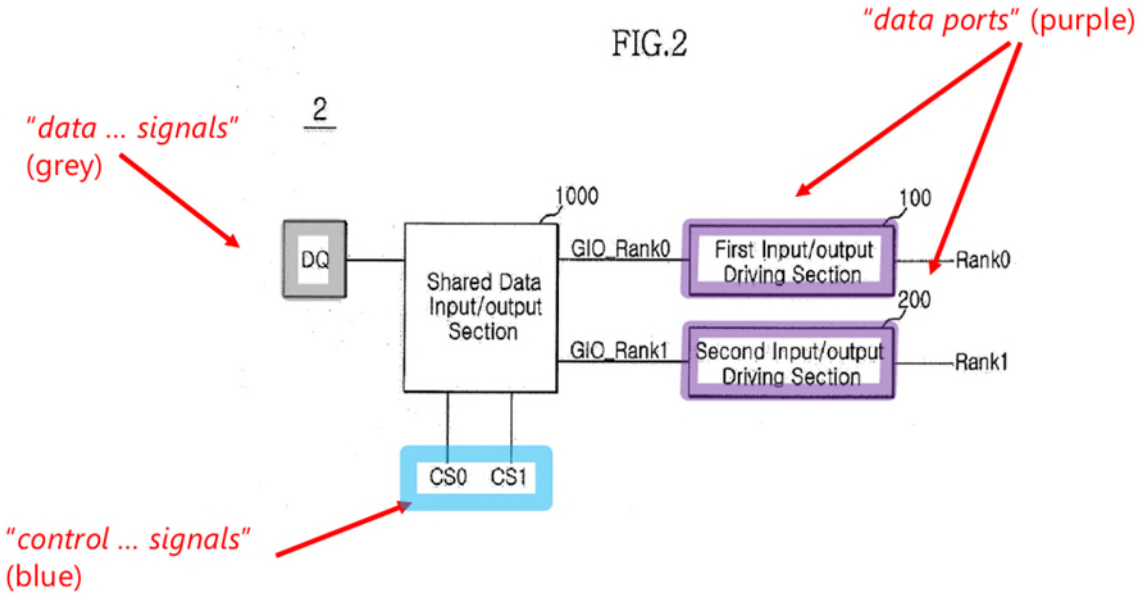
192. For example, Kim discloses a data pad DQ which is an example of "*input/output terminals via which the memory package communicates data … signals with one or more external devices*." *See* Ex. 1014 at Fig. 5 (reproduced below, annotated, data pad DQ annotated grey).



193. Kim explains that "[t]he data input/output section outputs the data transmitted from the rank selecting section through a data pad to an external device during a read operation, and outputs the data inputted to the data pad to the rank selecting section during a write operation." Ex. 1014 at Abstract; *see also id.* [0028] ("During a read operation, the shared data input/output section 1000 outputs data transmitted from the first input/output driving sections 100 and 200 through a data pad DQ…. During a write operation, the shared data input/output section 1000 transmits data inputted through the data pad DQ to one of the first and second input/output driving sections 100 and 200…."). Therefore, Kim discloses the claimed "*input/output terminals*" to communicate "*data … signals*."

194. Kim also discloses to a Skilled Artisan "*input/output terminals via which the memory package communicates …control … signals* [such as chip

selection control signals CS0 and CS1] *with one or more external devices*." Ex. 1014 at Fig. 2 (reproduced below, annotated).



195. For example, Kim explains that "chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2." *Id.* at [0032]. A Skilled Artisan would have understood that "chip selection signals CS0 and CS1" are control signals because they are part of the command signals that control the memory device. *See* Ex. 1014 (Kim) at [0006] ("The semiconductor memory apparatus 1 ***controls the operations*** of the first and second chips ***using a chip selection command signal***.") (emphasis added); *see also* Ex. 1019 (JESD79-3C) at p.13 (disclosing that chip select signals are "considered part of the command code"). Therefore, Kim discloses the claimed "*control ... signals.*"

196. A Skilled Artisan would have understood that chip selection signals from an external device are received at respective terminals of a memory package. Indeed, a Skilled Artisan would have been familiar with JEDEC standards for memory devices, including standards for stacked memory devices, and understood that standard memory devices include terminals for data and control signals, including terminals for chip select signals. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including data terminals (DQ) and chip select signal terminals CS0#-CSn#, where 'n' is the number of chips in the stack); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, the prior art referenced in Figs. 1A and 1B of the 060 Patent also describes memory packages having terminals for chip selection signals. Ex. 1001 at 1:30-56 ("FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used … with the chip select ports 144 … configured to receive corresponding chip select signals to enable or select the array dies for data transfer."). Therefore, Kim discloses to a Skilled Artisan the claimed "*input/output terminals*" to communicate "*control … signals.*"

197. Kim also renders obvious to a Skilled Artisan "*input/output terminals via which the memory package communicates … address signals with one or more external devices*."

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198. For example, Kim discloses "write and read command signals applied from a device external to the semiconductor memory apparatus 2." Ex. 1014 at [0038]. It would have been obvious to a Skilled Artisan from this disclosure, at least in view of Rajan, that "write and read command signals" can include address signals received via respective terminals from an external controller. *Supra*, ¶¶150-168. For example, as discussed above, a Skilled Artisan would have understood that memory devices can comply with JEDEC standards at the time and such standards specify the address and command signals, and corresponding terminals, for read and write operations. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including address signal terminals A0-A15), p.18 (describing read and write operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read and Write commands with corresponding column address, CA); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, the 060 Patent also describes the prior art memory devices referenced in Figs. 1A and 1B as operating in response to command and address signals. Ex. 1001 at 1:30-56 ("FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed

to be used … [where] the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110.").

199. Therefore, Kim discloses and renders obvious this limitation to a Skilled Artisan.

200. To the extent one might argue that Kim does not sufficiently disclose the claimed "*input/output terminals via which the memory package communicates … control/address signals with one or more external devices*," it would have been obvious to a Skilled Artisan in view of Rajan.

201. As previously discussed, a Skilled Artisan would have been motivated to look at analogous art to Kim, like Rajan, for details about control and address signals. *Supra* ¶¶150-163. Rajan discloses the same basic structure of a memory package like Kim and the 060 Patent: the package includes stacked memory chips and a shared interface circuit, called "buffer chip" in Rajan. Ex. 1015 at 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses."), Fig. 4 (reproduced below, annotated).

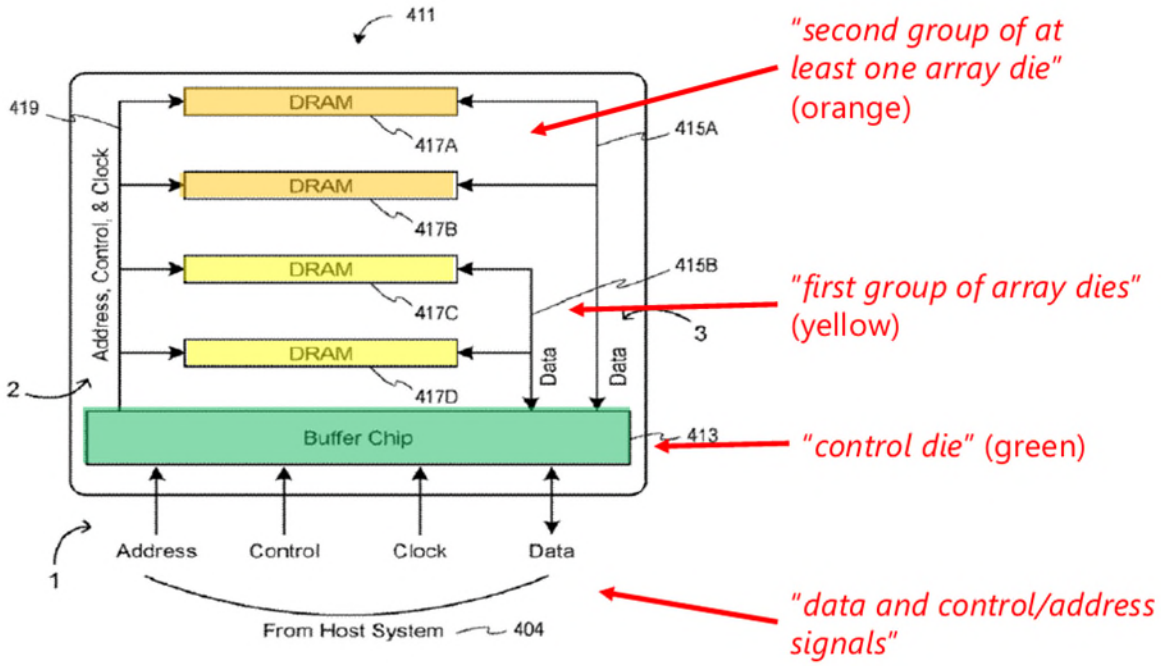


FIG. 4

In particular, the "interface circuit includes a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system, and a system data signal interface for sending/receiving data signals to/from the host system." *Id.* at 14:11-18 and Fig. 18 (reproduced below).

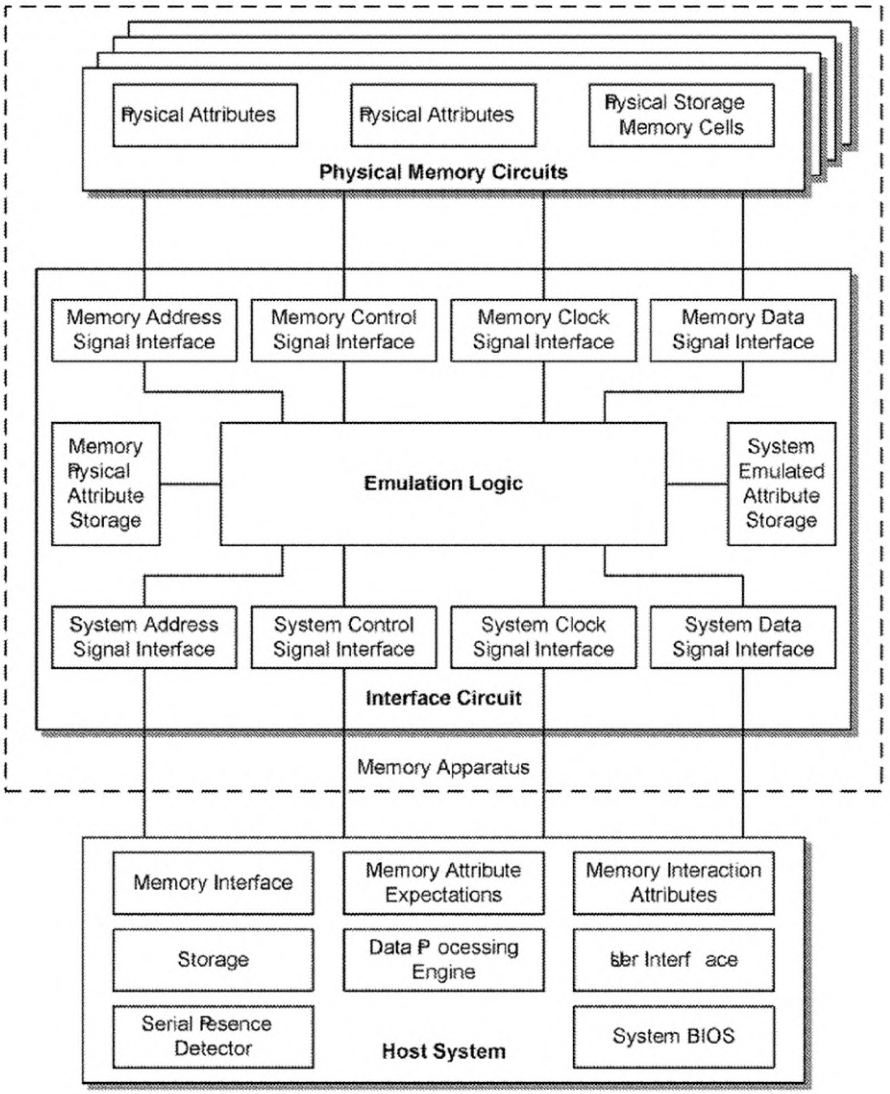


FIG. 18

202. In Rajan, "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 at 5:36-43, Figs. 4 and 18 (reproduced above). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards . .

..."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including terminals for address, control, and data signals); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Furthermore, a Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control, and data terminals in Kim's memory package according to the JEDEC standards to enable the memory packages' use in JEDEC compliant systems.

203. Therefore, Kim and Rajan render obvious this limitation to a Skilled Artisan.

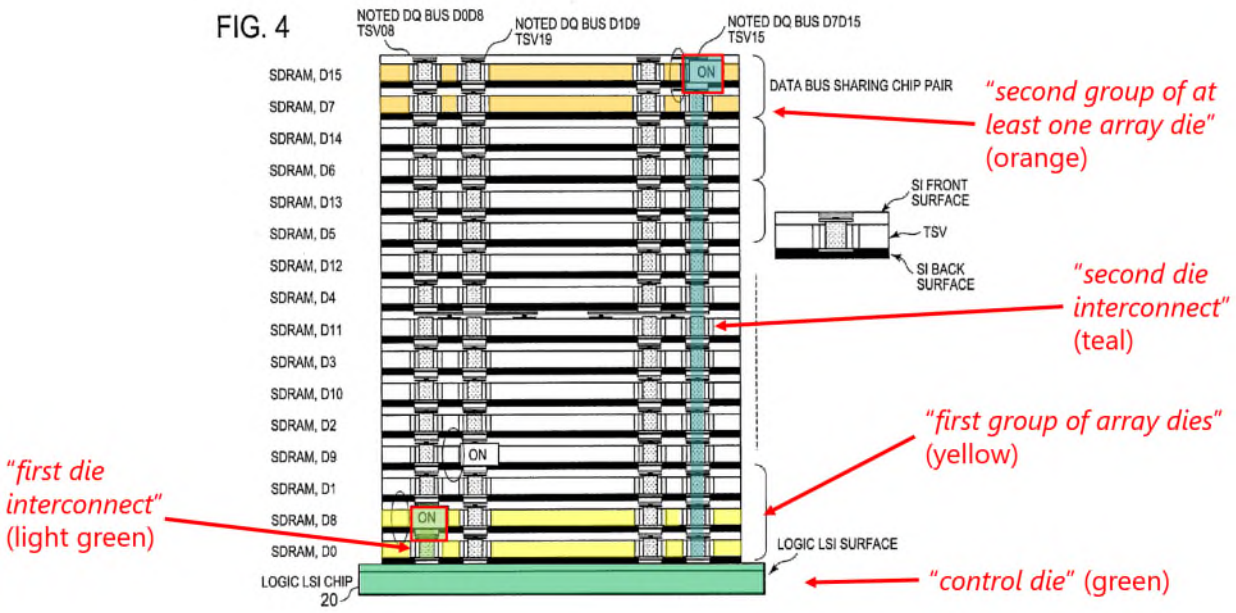
204. Additionally, the claimed "*input/output terminals via which the memory package communicates … control/address signals with one or more external devices*" would have been further obvious to a Skilled Artisan in view of Riho.

205. As discussed above, a Skilled Artisan would have been motivated to look at analogous art, like Riho, for details about control and address signals, not expressly discussed in Kim. *Supra* ¶¶169-173.

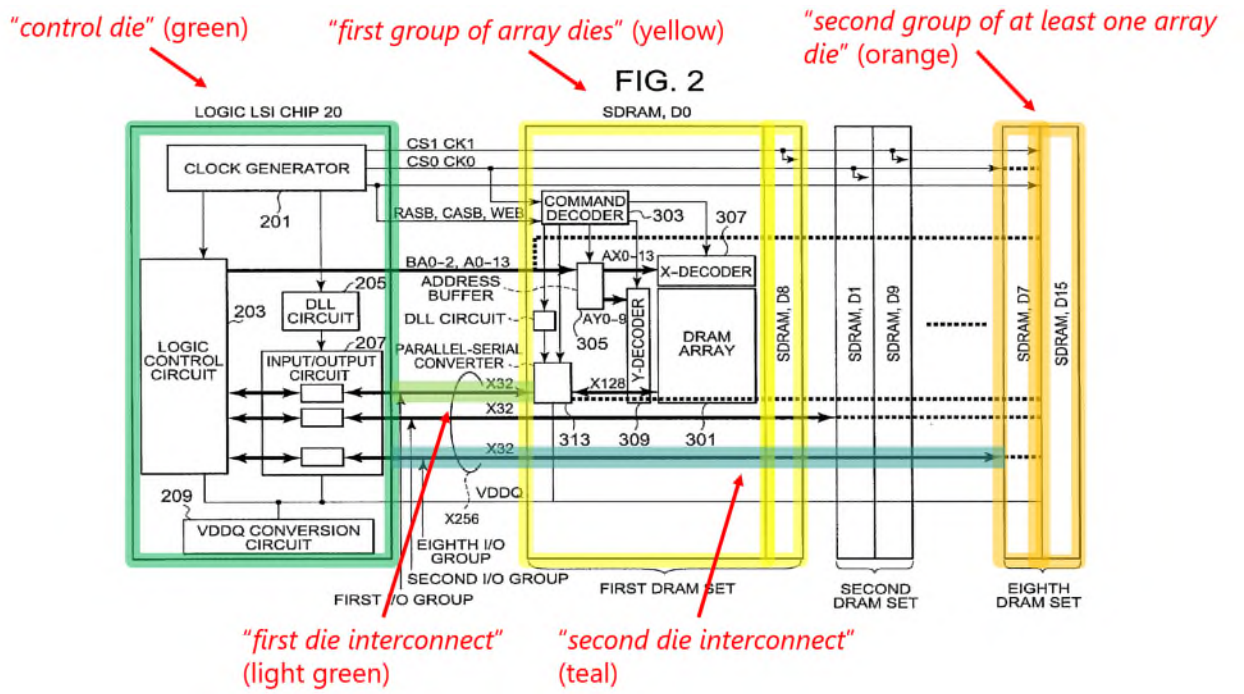
206. Riho discloses the same basic structure of a memory package like Kim and the 060 Patent: the package includes stacked memory chips and a shared interface circuit, called "logic LSI chip" in Riho. Ex. 1016 at Fig. 4 (reproduced

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below, annotated), [0062] ("As shown in FIG. 4, the 16 SDRAMs D0, D8, D1, D9, D2, D10, D3, D11, D4, D12, D5, D13, D6, D14, D7, and D15 are stacked in this order on the logic LSI chip 20.").



207. Riho further explains that, "[i]n the figure, external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20. I/O signal lines penetrating through the controlled chips, which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the external terminals." *Id*. at [0026]. Riho also discloses that the logic LSI chip 20 sends address (BA0-BA2 and A0-A13), command (RASB, CASB, WEB), control (CS0 CK0, CS1 CK1,…) signals to the SDRAMs in the stack. *Id*. at [0030], Fig. 2 (reproduced below).



208. A Skilled Artisan would have understood from this disclosure that Riho's logic chip 20 has "*input/output terminals* [at its lower side] *via which the memory package communicates … control/address signals with one or more external devices*" and uses the received control/address signals to control the SDRAM chips in the stack.

209. Therefore, Kim and Rajan in view of Riho further render obvious this limitation to a Skilled Artisan.

210. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices.*"

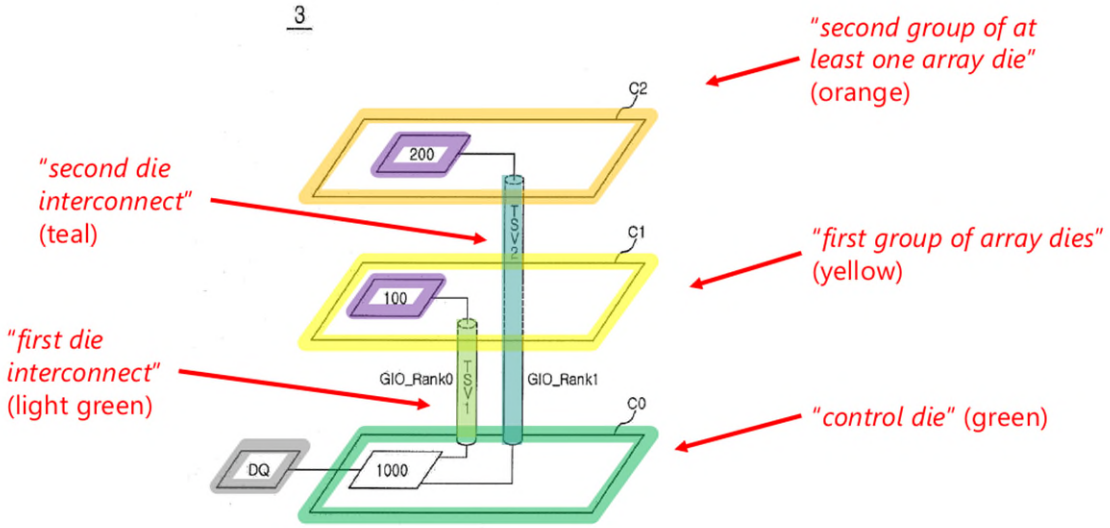
c) [1.c] Stacked Array Dies

211. Claim 1 requires "*a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports.*"

212. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

213. Kim discloses to a Skilled Artisan "*a plurality of stacked array dies including a first group of array dies* [including slave chip C1 (yellow)] *and a second group of at least one array die* [including slave chip C2 (orange)]*, each array die having data ports* [such as input/output driving sections 100 and 200 (purple), respectively]." *See* Ex. 1014 at Fig. 5 (reproduced below, annotated).

FIG.5



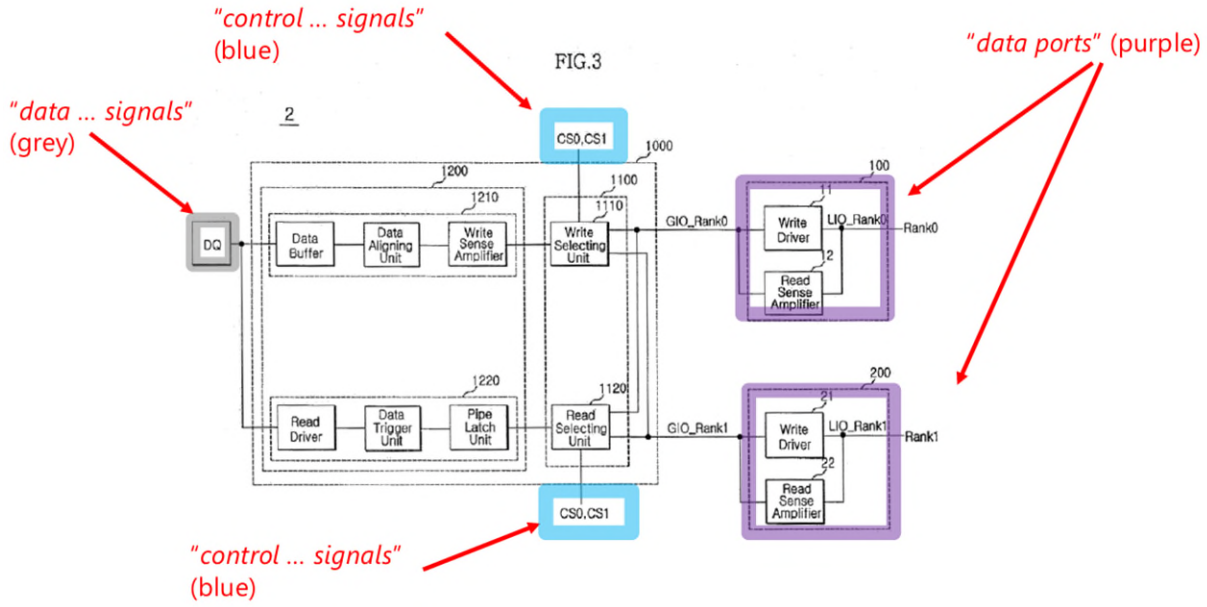
214. For example, Kim explains that "FIG. 5 shows an exemplary embodiment in which one main chip C0 and two slave chips C1 and C2 are

stacked. Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used." Ex. 1014 at [0048]. A Skilled Artisan would have understood that each referenced chip is a "*die*." *See, e.g.*, Ex. 1016 (Riho) at Abstract (describing stacked chips); Ex. 1018 (Riho2) (describing stacked "chip dies"). Therefore, Kim discloses "*a plurality of stacked … dies.*"

215. Kim further explains that the "first input/output driving section 100 stores data transmitted through the first data input/output line GIO_Rank0 in a memory bank of a first rank Rank0 during a write operation, amplifies data stored in the memory bank of the first rank Rank0 and outputs the amplified data to the first data input/output line GIO_Rank0 during a read operation." *Id*. at [0026]. Likewise, Kim explains that the "second input/output driving section 200 stores data transmitted through the second data input/output line GIO_Rank1 in a memory bank of a second rank Rank1 during a write operation and amplifies data stored in the memory bank of the second rank Rank1 and outputs the amplified data to the second data input/output line GIO_Rank1 during a read operation." *Id.*; *see also id.* at Fig. 5 (reproduced above, annotated, showing the input/output driving sections 100 and 200 in the respective stacked slave chips C1 and C2), Fig. 3 (reproduced below, annotated, showing that each of the input/output driving

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sections 100 and 200 includes a Write Driver 11 and 21 and a Read Sense Amplifier 12 and 22, respectively).



216. A Skilled Artisan would have understood from Kim's disclosure that each of the input/output driving sections 100 and 200 is a "*data port*" through which data is transmitted for storage and through which the stored data is retrieved from the slave chip.

217. A Skilled Artisan would have also understood that Kim's "memory bank" where the data is stored includes a memory array. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.13 (explaining that the row address for Active commands and the column address for Read/Write commands "select one location out of the memory array in the respective bank"); *see also* Ex. 1023 (Jacob) at pp.1-2 & Fig.

2 (reproduced bellow, disclosing that the basic organization of DRAMs includes a memory array); Ex. 1022 (Jacob et al.) at 316-320 (same).

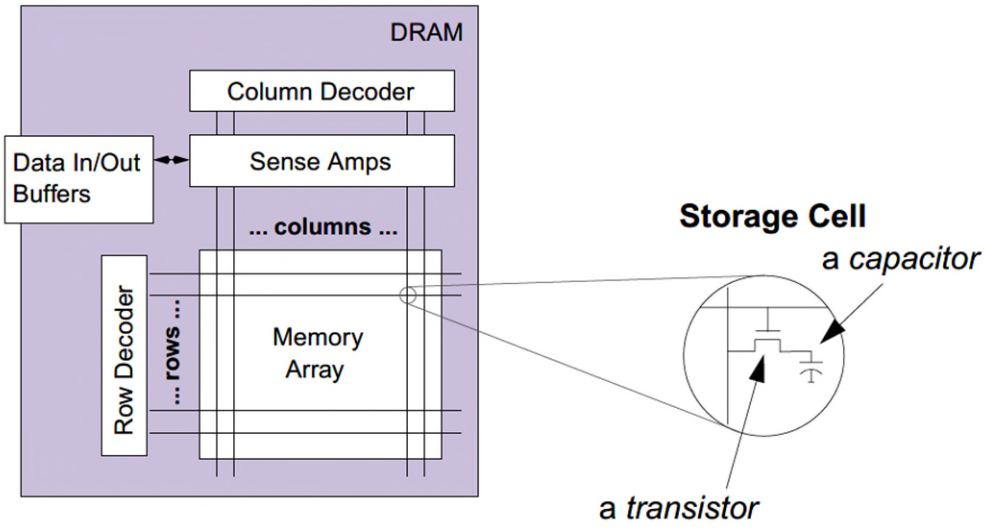


Figure 2: Basic Organization of DRAM Internals
The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

Therefore, Kim also discloses and renders obvious to a Skilled Artisan that the slave chips C1 and C2 are "*array dies*" as required by the claim.

218. Kim also discloses that slave chip C1 is in a "*first group of array dies*" coupled to through-silicon via TSV1, and slave chip C2 is in a "*second group of at least one array die*" coupled to through-silicon via TSV2. Ex. 1014 at Fig. 5 (reproduced above, annotated).

219. To the extent one might argue that the "*first group of array dies*" requires multiple slave chips being coupled to the through-silicon via TSV1, Kim discloses and renders obvious such an arrangement to a Skilled Artisan. For example, Kim explains that "although only one main chip and two slave chips are

shown [in Fig. 5], it is to be understood that any number of main and slave chips may be used." Ex. 1014 at [0048]. Furthermore, Kim explains that "the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked. While the semiconductor memory apparatuses having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks." *Id.* at [0050].

220. A Skilled Artisan would have understood from this disclosure that Kim's invention is not limited to the exemplary two slave chips C1 and C2 and two ranks and that the stack can include more slave chips and/or more ranks. A Skilled Artisan would have also understood that some of the additional slave chips proposed by Kim can be in the same group as chips C1 or C2 and connected to TSV1 or TSV2, respectively. Indeed, such an arrangement of multiple groups of the stacked dies, where each die in a group is connected to the same data interconnect, was commonly known and used to implement multiple ranks in memory stacks at the time. *See, e.g.*, Ex. 1024 (Ruckerbauer (US7,796,446)) at Fig. 5 (reproduced below, annotated), 9:14-18 ("[W]ithin the memory stack 100, a first sub set of memory dies is coupled to the first transfer data path 12a and a

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second sub set is coupled to the second transfer data path 12b. These different sub sets could, for example, be associated to different ranks within the stack 100.").

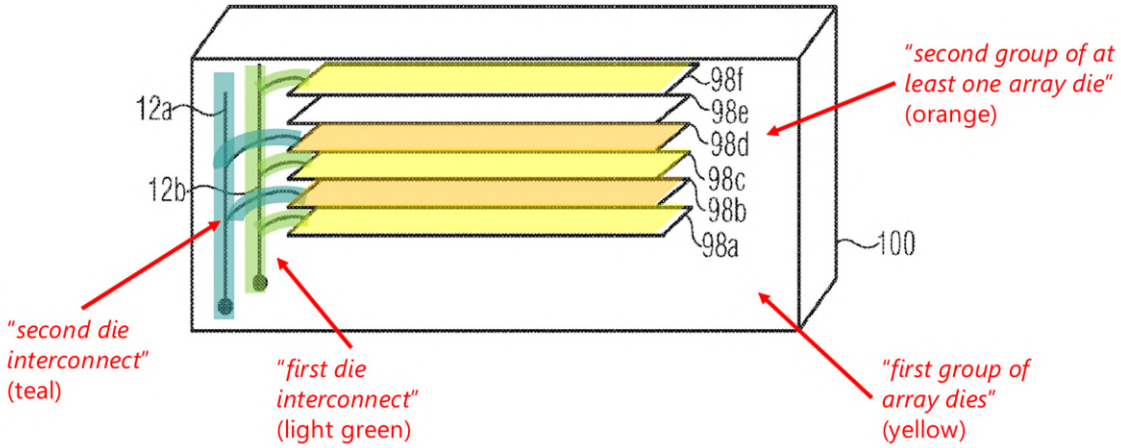


FIG 5

221. To the extent one might argue that Kim alone does not render obvious the additional chips sharing the data connections TSV1 and TSV2, it would have been obvious in view of Rajan. As discussed above, a Skilled Artisan would have been motivated to look to Rajan for details about adding more chips in the stack as proposed by Kim. *Supra* ¶¶150-168. For example, Rajan explains that "FIG. 4 illustrates another embodiment of a system 411 in which the buffer chip 413 is interfaced to a host system 404 and is coupled to the DRAM chips 417A-417D somewhat differently than in the system of FIG. 2 or 3. There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B.

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Each shared bus has two or more DRAM chips coupled to it."). *Id*. at 5:36-43, Fig. 4 (reproduced below, annotated).

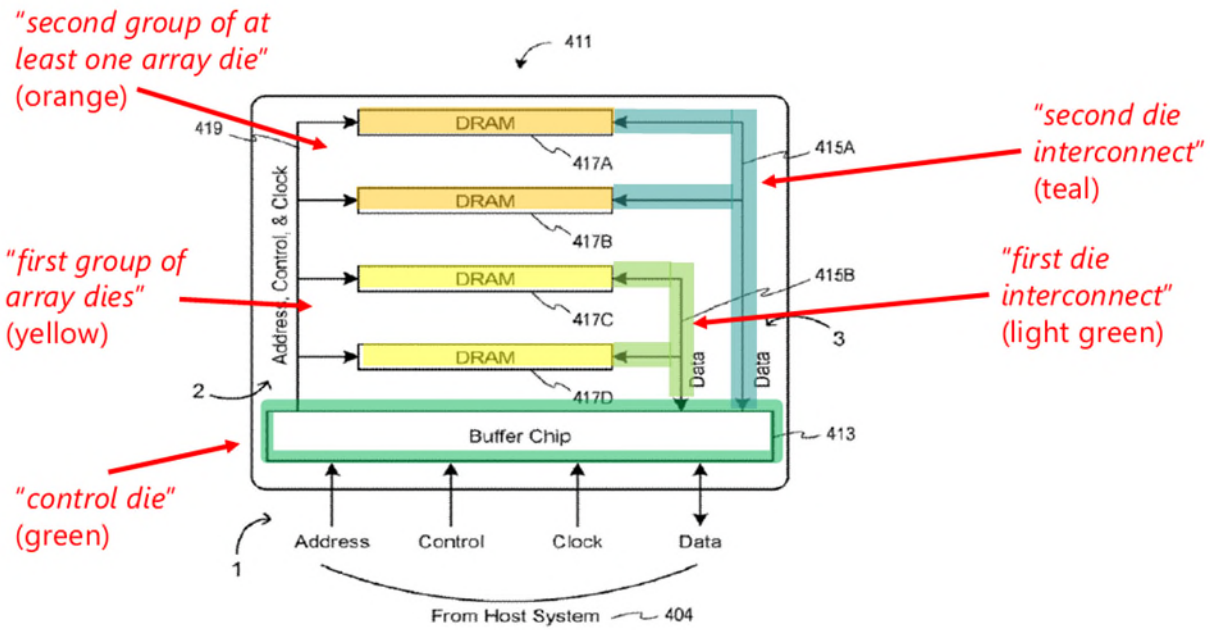


FIG. 4

222. A Skilled Artisan would have also understood that creating such a shared data bus as taught by Rajan was well within the level of skill at the time using, e.g., TSV interconnects like Kim. *See, e.g.*, Ex. 1025 (Foster) at Fig. 5 (reproduced below, annotated, showing two dies 21 and 22 in a first substack coupled to signal lines 68 by TSV 30, and two other dies 23 and 24 in a second substack coupled to signal lines 70 using TSV 30 and pass-through vias PTV 29 which have no connection to circuitry in dies 21 and 22 in the first substack).

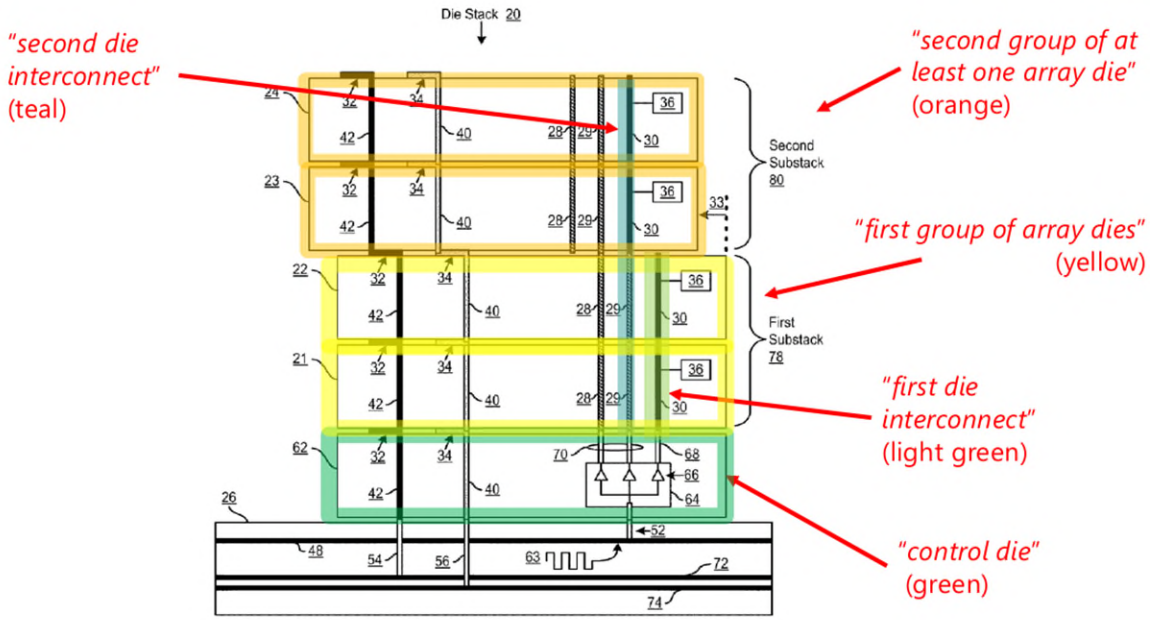


FIG. 5

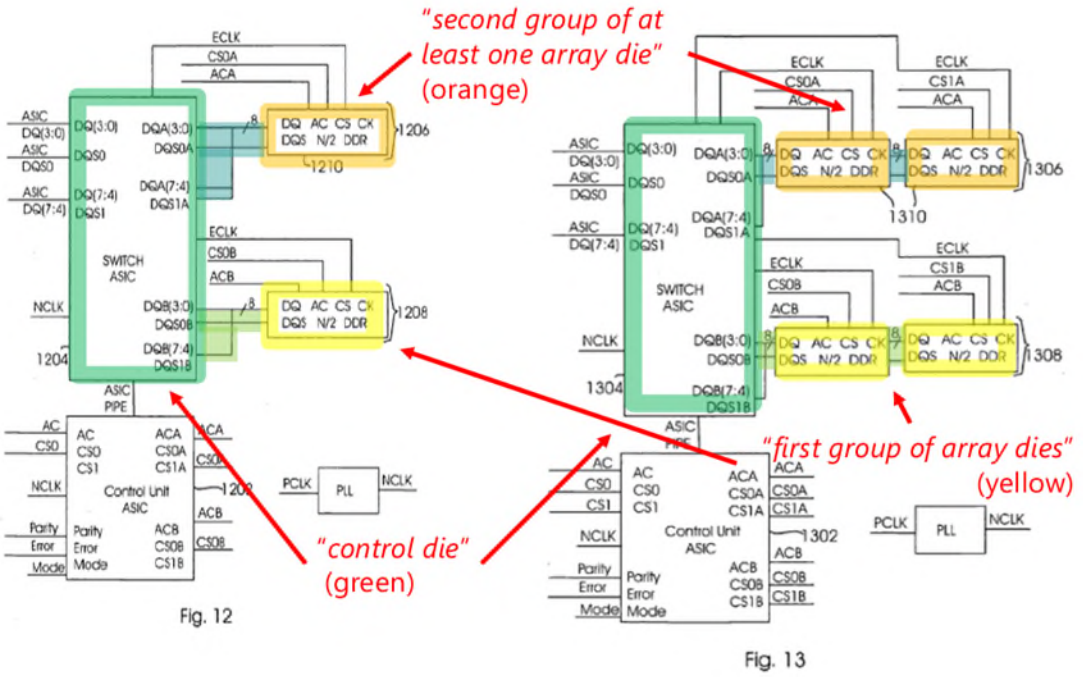
223. Therefore, a Skilled Artisan would have understood that there were a finite number of known ways to connect the additional dies, including sharing a via by a subset of the dies, so it would have been at least obvious to a Skilled Artisan to follow this well know architecture when adding memory dies to the stack as suggested by Kim. *See*, *e.g.*, Ex. 1015 at Figs. 2-6.

224. Furthermore, a Skilled Artisan would have been motivated to connect the additional dies to the existing interconnects TSV1 or TSV2 in Kim's device, because such an arrangement could use Kim's chips without changing the interconnects TSV1 and TSV2 and without creating new TSVs which would require space and additional circuitry. Such a use of the interconnects TSV1 and TSV2 would also allow for the emulation of certain characteristics required by external devices. *Supra* at ¶¶138-141; *see, e.g.*, Ex. 1015 (Rajan) at 3:27-30 ("For

example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 3:52-61 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory. The interface circuit may emulate an interface to one version of a protocol such as DDR2 with 5-5-5 latency timing, while the physical memory chips are built to another version of the protocol such as DDR2 with 3-3-3 latency timing. The interface circuit may emulate an interface to a memory having a first capacity that is different than the actual combined capacity of the physical memory chips.").

225. Indeed, a Skilled Artisan would have understood that such rank multiplication techniques used "fork-in-the-road" arrangements where a two-rank arrangement has two data busses, and two more ranks can be added by sharing the existing data busses of the two-rank arrangement. *See, e.g.*, Ex. 1026 (Ellsberry) at Figs. 12, 13 (reproduced below, annotated, showing a switch ASIC connecting an 8-bit wide external DQ bus to two 8-bit wide internal busses DQA and DQB, and adding two more ranks in Figure 13 by sharing the DQA and DQB busses already used in the two-rank arrangement of Figure 12); Ex. 1027 at 77-82 (Final Written Decision analyzing Ellsberry).

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226. A Skilled Artisan's understanding that rank multiplication techniques used "fork-in-the-road" arrangements is further evidenced by the prior art referenced in the 060 Patent. *Supra* at ¶¶138-141; *see also* Ex. 1001 (the 060 Patent) at 19:41-47, 22:34-57 (explaining that rank multiplication was well known prior art and incorporating by reference corresponding prior art patents disclosing fork-in-the-road arrangements, including Exhibits 1028 and 1031), 18:65-19:7 (describing prior art memory package with a "programmable secondary 1-to-2 rank decoder" in the controller die of the memory package); Ex. 1028 (US 7,289,386) at Fig. 6D (showing fork-in-the-road arrangement) and Ex. 1031 (7,532,537) at Fig. 1 (same); *see also supra* at ¶¶138-141.

227. A Skilled Artisan would have been further motivated to use the interconnects TSV1 and TSV2 when adding more chips, because Kim explains that its structure of using two interconnects can avoid certain data collisions. Ex. 1014 at Figs. 4A (explaining the problem of collision in the prior art), 4B (explaining the operation of the invention avoiding the collision), [0042-44] (same). Therefore, when adding additional chips, a Skilled Artisan would have been motivated to connect the additional dies to Kim's interconnects TSV1 and TSV2 as taught by Rajan to maintain Kim's data collision avoidance feature without creating additional TSVs.

228. Therefore, Kim discloses and renders obvious in view of Rajan this limitation to a Skilled Artisan.

229. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports*."

d) [1.d.1] and [1.d.2] Die Interconnects in Electrical Communication with Array Dies

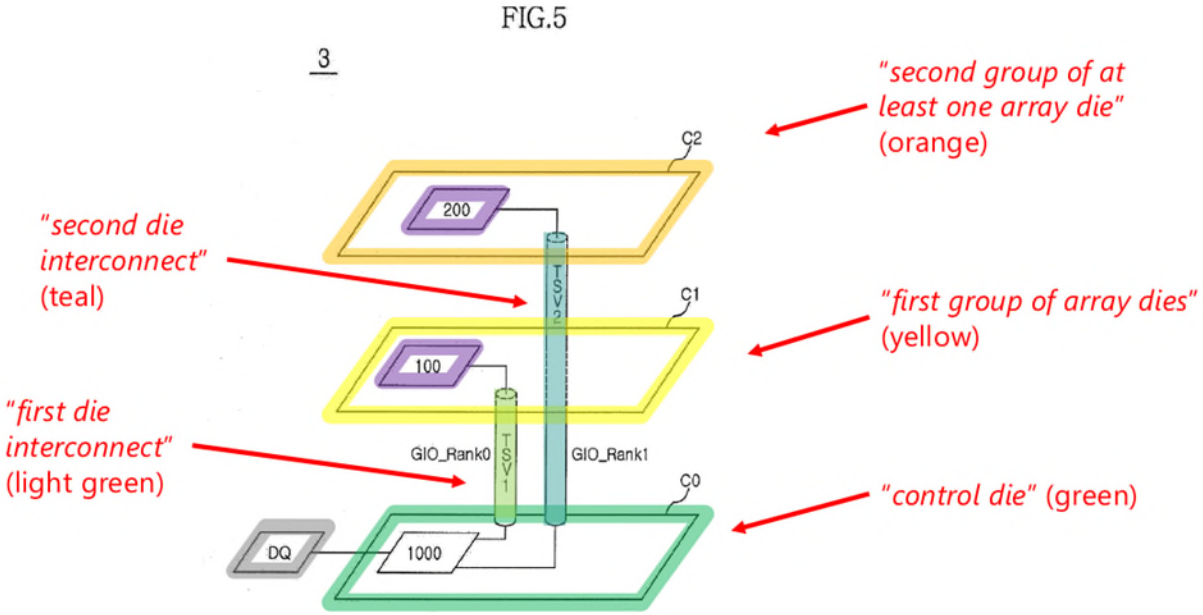
230. Claim 1 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnect in electrical*

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communication with the second group of at least one array die and not in electrical communication with the first group of array dies."

231. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

232. Kim discloses to a Skilled Artisan "*at least a first die interconnect* [through-silicon via TSV1] *and a second die interconnect* [through-silicon via TSV2]*, the first die interconnect* [TSV1] *in electrical communication with the first group of array dies* [including slave chip C1] *and not in electrical communication with the second group of at least one array die* [including slave chip C2]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated), [0049] ("Data transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0 comprises a TSV TSV1 which connects the first slave chip C1 and the main chip C0."). As shown below, TSV1 does not extend up to C2 and thus is not "*in electrical communication*" with C2.



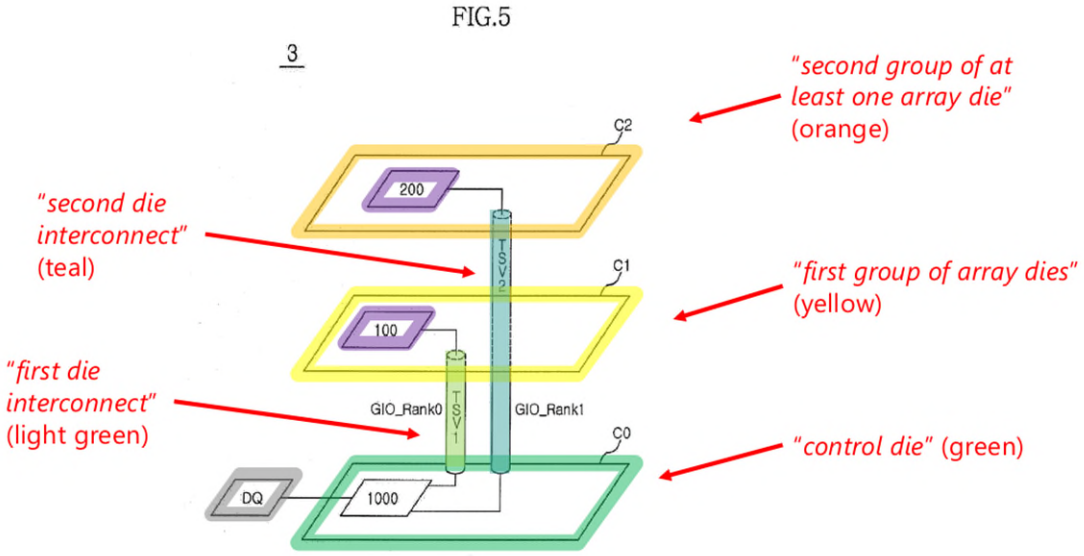
233. For example, Kim explains that "[t]he rank selecting section is selectively connected to one of the first and second ranks in response to a chip selection signal, and outputs data to a connected rank or receives data from the connected rank." Ex. 1014 at Abstract. Kim further explains that "[t]he rank selecting unit 1100 distinguishes the read operation and the write operation for the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, and is selectively connected to the first and second data input/output lines GIO_Rank0 and GIO_Rank1. Thus, the read and write data may be transmitted through the first data input/output line GIO_Rank0 during the read and write operations of the first rank Rank0, and the read and write data may be transmitted through the second data input/output line GIO_Rank1 during the read and write operations of the second rank Rank1." *Id.* at [0045]. Kim elaborates that,

due to the selective coupling, "even when the read and write operations of the first and second ranks Rank0 and Rank1 are repeatedly performed, a data collision does not occur as can be alternately seen from FIG. 4B." *Id.*

234. A Skilled Artisan would have understood from this disclosure that the data collisions do not occur because, as depicted in Fig. 5 of Kim, the data input/output lines GIO_Rank0 through TSV1 are in electrical communication with chip C1 implementing Rank0, but are not in electrical communication with chip C2 implementing Rank1, and the data input/output lines GIO_Rank1 through TSV2 are in electrical communication with chip C2 implementing Rank1, but are not in electrical communication with chip C1 implementing Rank0.

235. Therefore, Kim discloses this limitation to a Skilled Artisan.

236. Kim further discloses to a Skilled Artisan that "*the second die interconnect* [through-silicon via TSV2 is] *in electrical communication with the second group of at least one array die* [including chip C2] *and not in electrical communication with the first group of array dies* [including chip C1]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated), [0049] ("Data transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1 comprises a TSV TSV2 which connects the second slave chip C2 and the main chip C0.").



237. As shown above , TSV2 passes through C1 without being "*in electrical communication*" with C1 (e.g., there is no data port (purple) or anything else connected to TSV2 in C1). Furthermore, for the reasons discussed immediately above with reference to the "*first die interconnect*" TSV1, a Skilled Artisan would have understood from Kim's disclosure that "*the second die interconnect*" TSV2 is in electrical communication with chip C2, but not with chip C1. *Supra* ¶¶232-235.

238. Therefore, Kim discloses this limitation to a Skilled Artisan.

239. Accordingly, the prior art references in each of Grounds 1-3 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical communication with the second group of*

at least one array die and not in electrical communication with the first group of array dies."

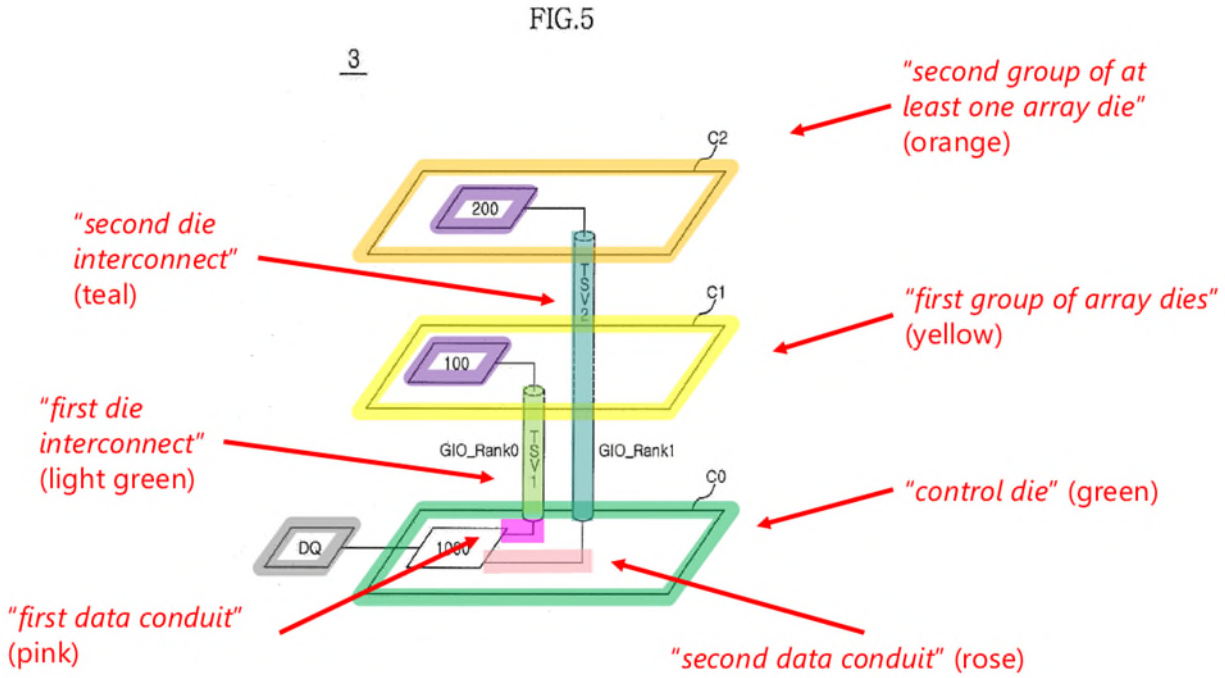
e) [1.e] Control Die

(1) [1.e.1] A Control Die Comprising

240. Claim 1 requires "*a control die comprising.*"

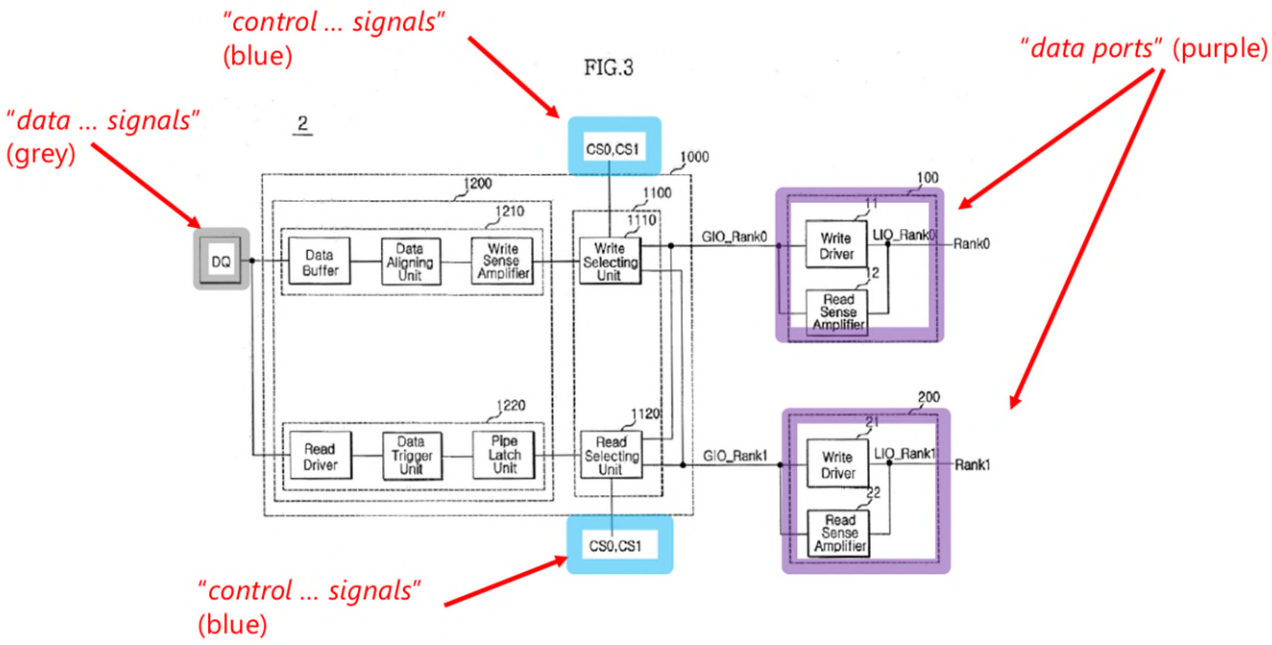
241. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

242. Kim discloses "*a control die*" including main chip C0. *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).



243. For example, Kim discloses that, within the data input/output section 1000 on the main chip C0, "the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals." Ex.

1014 at [0038], Fig. 3 (reproduced below, annotated). Kim explains that the "internal write and read signals may be signals generated because write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered." *Id.* at [0038]. Kim further explains that "[t]he rank selecting unit 1100 distinguishes the read operation and the write operation for the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, and is selectively connected to the first and second data input/output lines GIO_Rank0 and GIO_Rank1." *Id.* at [0045]. As a result, "the read and write data may be transmitted through the first data input/output line GIO_Rank0 during the read and write operations of the first rank Rank0, and the read and write data may be transmitted through the second data input/output line GIO_Rank1 during the read and write operations of the second rank Rank1." *Id.* at [0045].



244. A Skilled Artisan would have understood from this disclosure that the main chip C0 controls the operation of Kim's memory apparatus, including read and write operations in response to read and write commands from an external device.

245. Furthermore, in the combination of Kim and Rajan, the "*control die*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices on the memory module. *Supra* at ¶¶138-141, 150-168; *see also* Ex. 1015 (Rajan) at 6:30-7:67 (describing specific examples of rank multiplication).

246. Therefore, Kim discloses and renders obvious in light of Rajan this limitation to a Skilled Artisan.

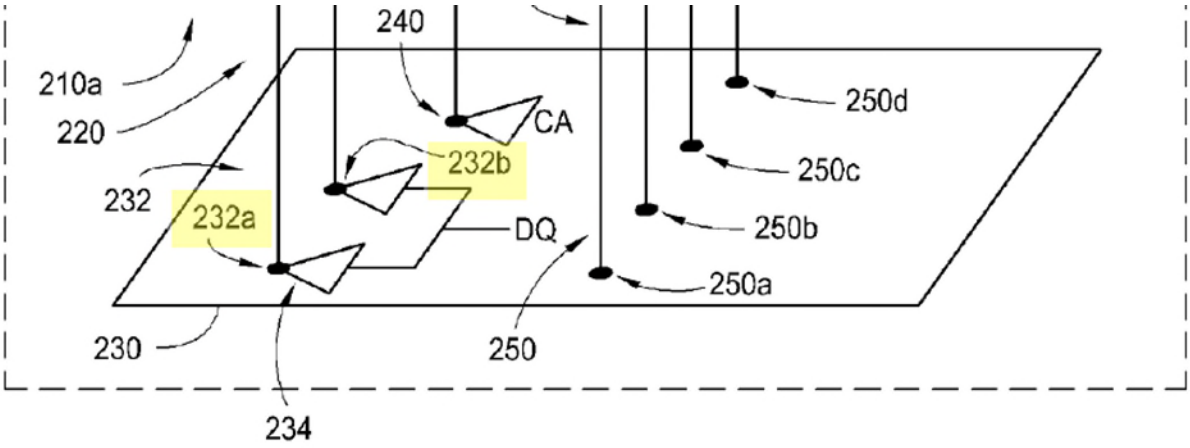
247. Therefore, the prior art references in each of Grounds 1, 2, and 3 satisfy "*a control die comprising*."

(2) [1.e.2] and [1.e.3] First and Second Data Conduit

248. Claim 1 requires "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal*."

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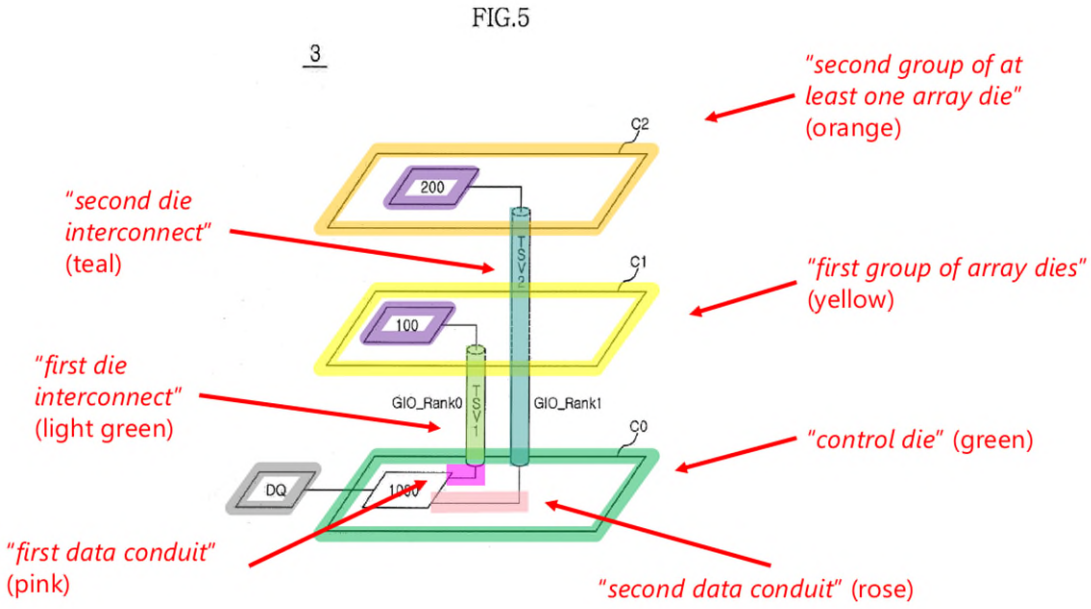
249. The prior art references in each of Grounds 1-3 teach the claimed first and second "*data conduits*" to a Skilled Artisan. The 060 Patent discloses that a "*data conduit*" is configured to transmit a data signal to a respective die interconnect. Ex. 1001 (060 Patent), *e.g.*, at 6:48-59, Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b).



"In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2." *Id*. 6:60-62. Similarly, "command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242" and "chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252." *Id*. at 9:28-60.

250. Kim discloses such "*at least a first data conduit* [including a signal line (annotated pink below) for communicating data through data input/output section 1000] *between the first die interconnect* [TSV1 (annotated light green)] *and*

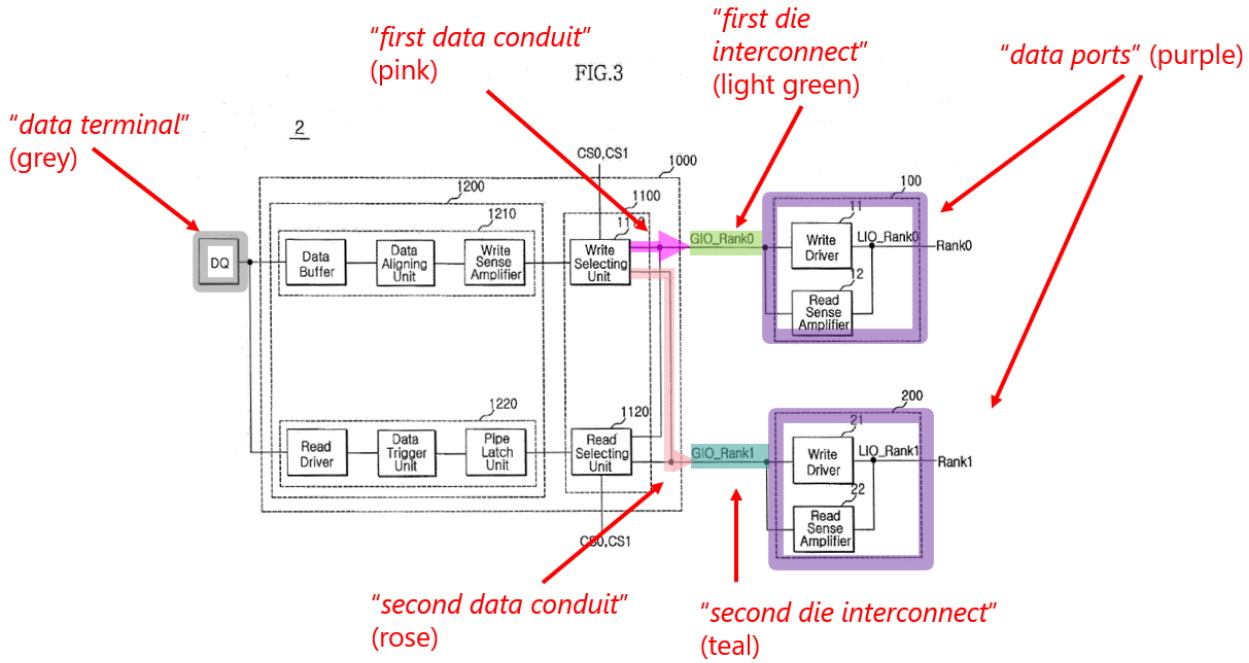
a first terminal [e.g., data pad DQ (annotated grey)] *of the plurality of input/output terminals*." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).



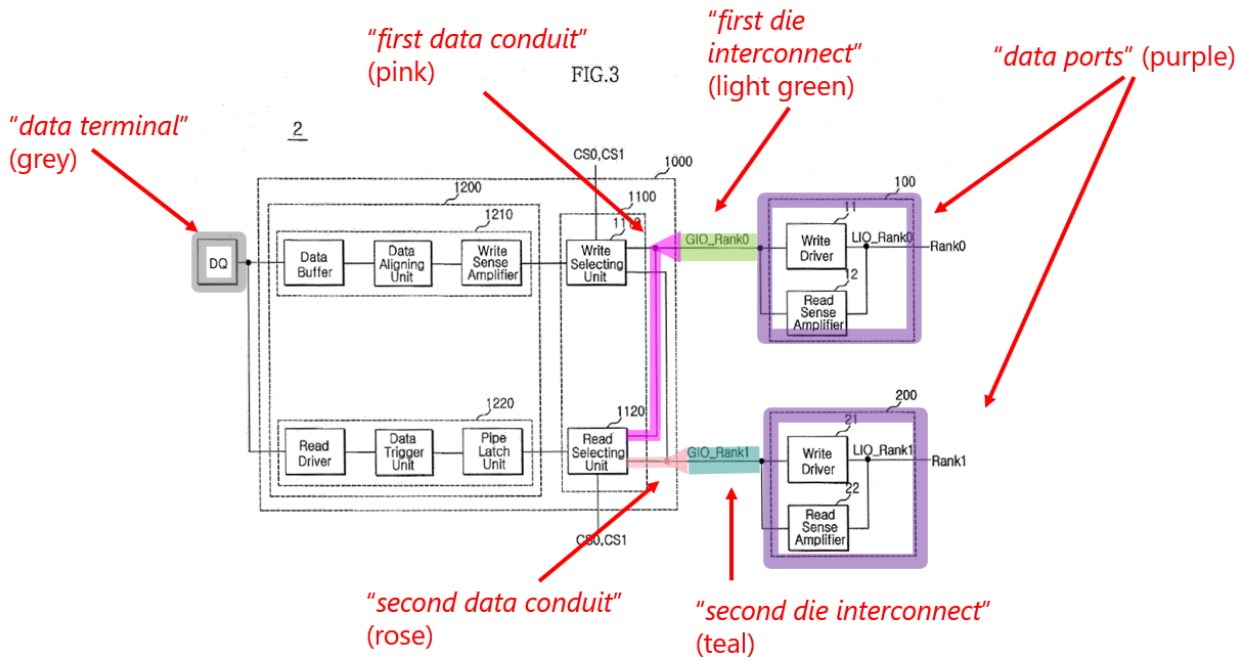
251. For example, Kim discloses that "[d]ata transmission between the first slave chip C1 and the main chip C0 is implemented through a first data input/output line GIO_Rank0. The first data input/output line GIO_Rank0 comprises a TSV TSV1 which connects the first slave chip C1 and the main chip C0." Ex. 1014 at [0049].

252. Kim explains that "[d]uring the write operation, when the first chip selection signal CS0 is enabled, the shared data input/output section 1000 outputs data, inputted through the data pad DQ, to the first data input/output line GIO_Rank0." *Id*. at [0030]; *see also id.* at Fig. 3 (reproduced below, annotated to show that a first "*data conduit*" (colored pink) is active for a write operation to

Rank0), [0035] ("During the write operation, the write selecting unit 1110 connects the first data input/output line GIO_Rank0 with the data input/output unit 1200 when the first chip selection signal CS0 is enabled, . . .").



253. Kim also explains that "[d]uring the read operation, when the first rank Rank0 is selected by the chip selection signals CS0 and CS1, that is, when a first chip selection signal CS0 is enabled, the shared data input/output section 1000 outputs data, transmitted through the first data input/output line GIO_Rank0, to the data pad DQ." *Id*. at [0029]; *see also id.* at Fig. 3 (reproduced below, annotated to show that a first "*data conduit*" (colored pink) is active for a read operation from Rank0), [0036] ("During the read operation, the read selecting unit 1120 connects the first data input/output line GIO_Rank0 to the data input/output unit 1200 when the first chip selection signal CS0 is enabled, . . .").

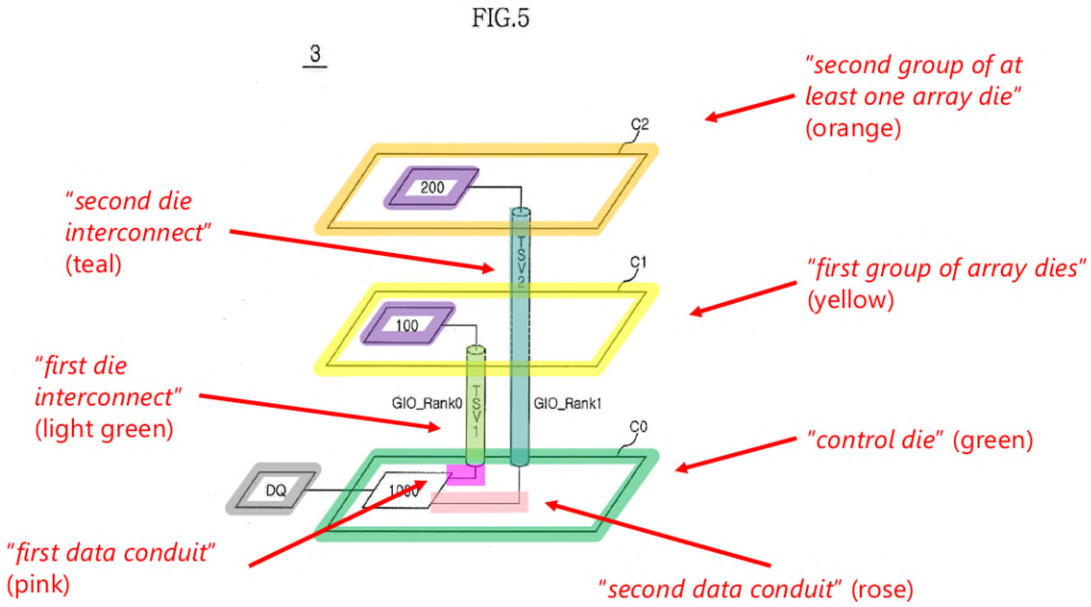


254. Kim further explains that "[t]he write selecting unit 1110 and the read selecting unit 1120 may be realized using multiplexers which are connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1. While not shown in a drawing, the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals." *Id*. at [0037-38].

255. A Skilled Artisan would have understood from this disclosure that the data conduit connecting the write selecting unit 1110 and the read selecting unit 1120 in data input/output section 1000 to a through-silicon via to Rank0 is between "*the first die interconnect*," e.g., TSV1, and a "*data terminal*," e.g., data pad DQ.

256. Therefore, Kim discloses "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*" to a Skilled Artisan.

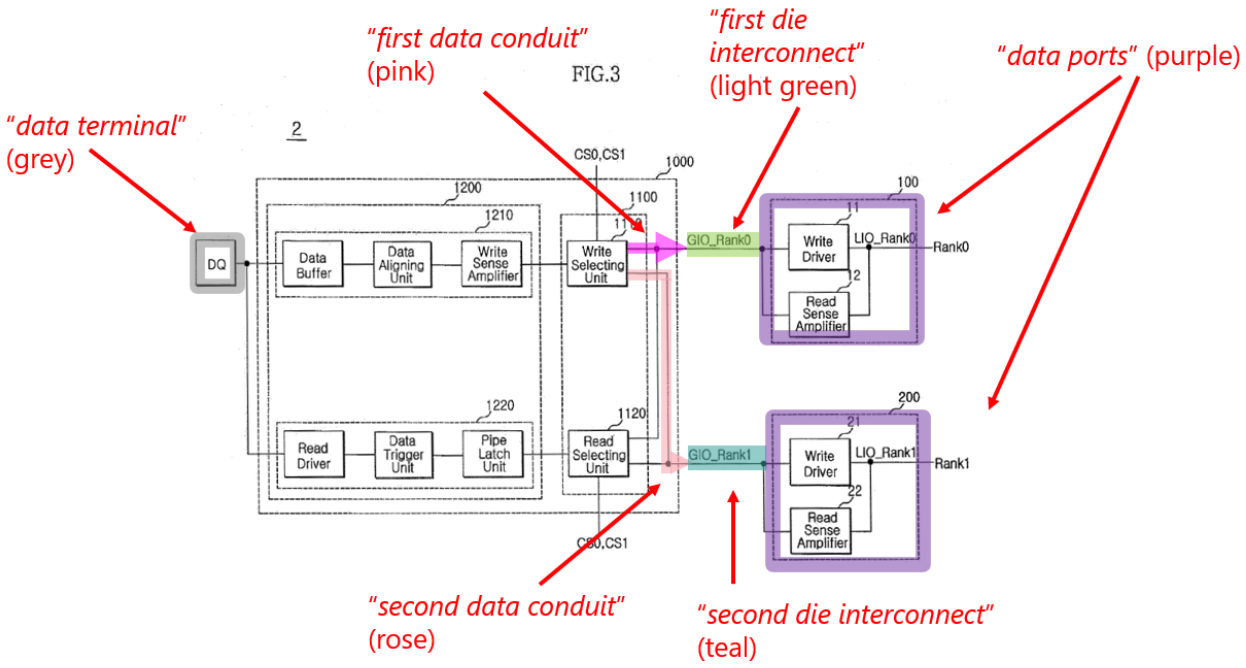
257. Kim also discloses "*at least a second data conduit* [including signal line (annotated rose below) for communicating data through data input/output section 1000] *between the second die interconnect* [TSV2 (annotated teal below)] *and the first terminal, the first terminal being a data terminal* [e.g., data pad DQ (annotated grey)]." *See, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).



258. For example, Kim discloses that "[d]ata transmission between the second slave chip C2 and the main chip C0 is implemented through a second data input/output line GIO_Rank1. The second data input/output line GIO_Rank1

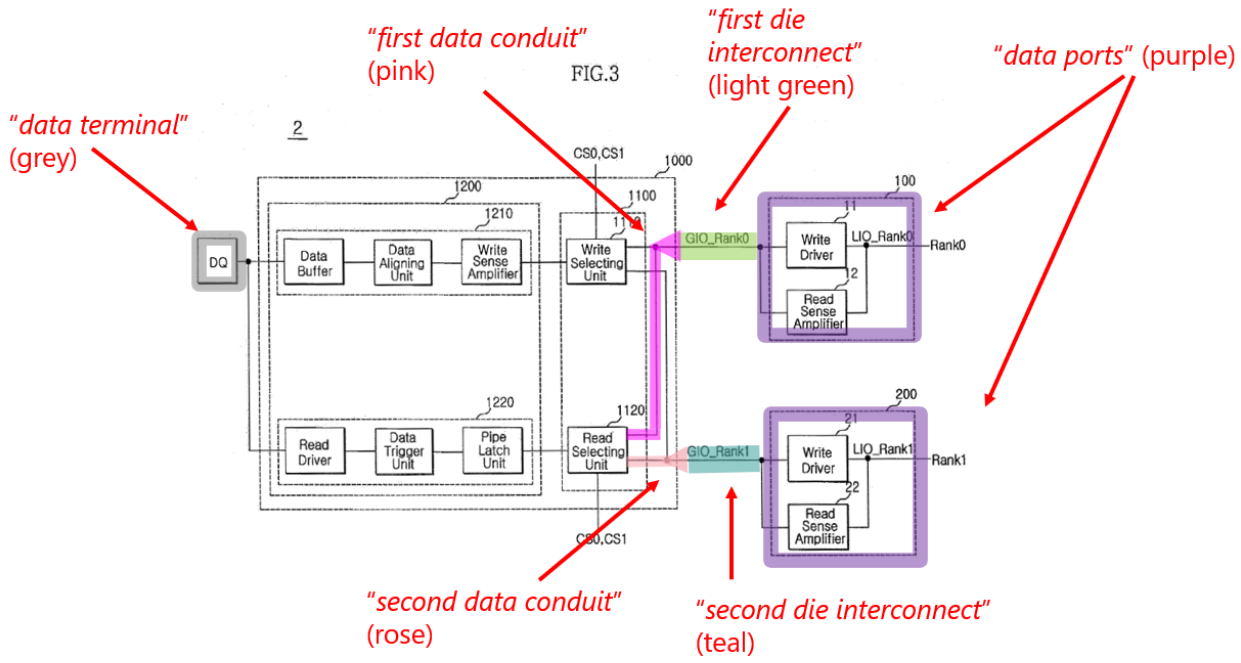
comprises a TSV TSV2 which connects the second slave chip C2 and the main chip C0." Ex. 1014 at [0049].

259. Kim explains that "during the write operation, when the second chip selection signal CS1 is enabled, the shared data input/output section 1000 outputs data, inputted through the data pad DQ, to the second data input/output line GIO_Rank1." *Id.* at [0030]; *see also id.* at Fig. 3 (reproduced below, annotated to show that a second "*data conduit*" (colored rose) is active for a write operation to Rank1), [0035] ("During the write operation, the write selecting unit 1110 . . . connects the second data input/output line GIO_Rank1 to the data input/output unit 1200 when the second chip selection signal CS1 is enabled.").



260. Kim also explains that "during the read operation, when the second rank Rank1 is selected by the chip selection signals CS0 and CS1, that is, when a

second chip selection signal CS1 is enabled, the shared data input/output section 1000 outputs data transmitted through the second data input/output line GIO_Rank1 to the data pad DQ." *Id*. at [0029]; *see also id.* at Fig. 3 (reproduced below, annotated to show that a second "*data conduit*" (colored rose) is active for a read operation from Rank1), [0036] ("During the read operation, the read selecting unit 1120 . . . connects the second data input/output line GIO_Rank1 to the data input/output unit 1200 when the second chip selection signal CS1 is enabled.")



261. A Skilled Artisan would have understood from this disclosure that a data conduit connecting the data input/output section 1000 to TSVs like TSV2 is between "*the second die interconnect*," e.g., TSV2, and the "*data terminal*," e.g., data pad DQ.

262. For the reasons discussed above with reference to claim limitation [1.b], Kim discloses that the data pad DQ is a "*data terminal*." *Supra* ¶¶189-210.

263. Therefore, Kim discloses "*at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal*" to a Skilled Artisan.

264. Therefore, the prior art references in each of Grounds 1, 2, and 3 satisfy "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal*."

(3) [1.e.4] Control Circuit

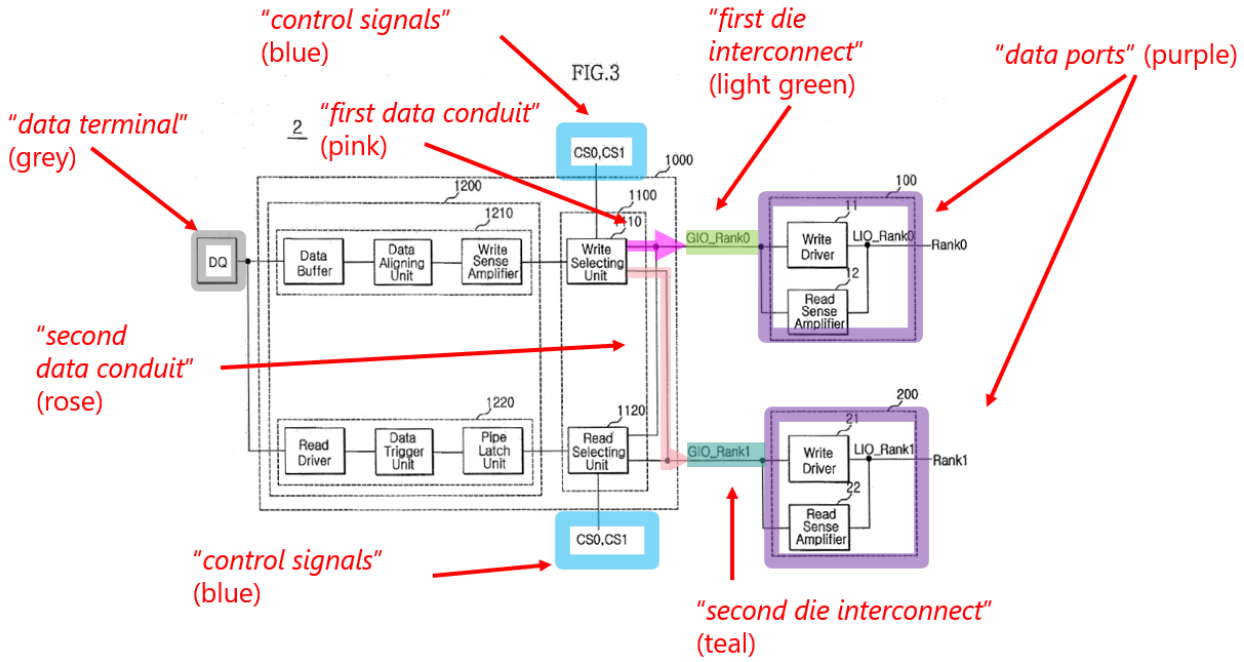
265. Claim 1 requires "*the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals*."

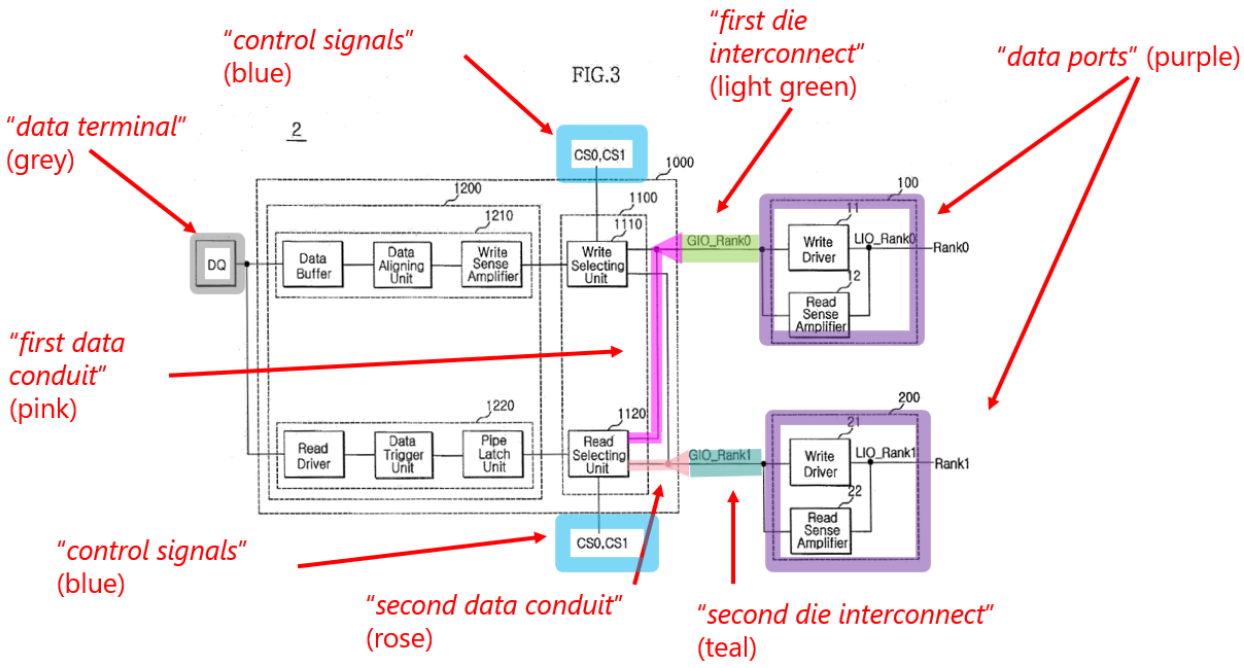
266. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

267. Kim discloses to a Skilled Artisan that "*the control die* [main chip C0 is] *further comprising a control circuit* [in rank selecting unit 1100] *to control respective states* [for communicating read and write data] *of the first data conduit*

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[(annotated pink below) to TSV1] *and the second data conduit* [(annotated rose below) to TSV2] *in response to control signals* [including chip selection signals CS0 and CS1 and read and write command signals pursuant to the JEDEC standard] *received via one or more second terminals of the plurality of terminals* [from an external device]." *See, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





268. For example, Kim discloses that the "rank selecting unit 1100 includes a write selecting unit 1110 and a read selecting unit 1120. The write selecting unit 1110 is activated during the write operation and is connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1." Ex. 1014 at [0035]. Kim explains that "[t]he read selecting unit 1120 is activated during the read operation and is connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1." *Id.* at [0036]. Kim discloses that "the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals," and that "[t]he internal write and read signals may be signals that are generated because write and read command signals applied from a device external to the

semiconductor memory apparatus 2 are buffered." *Id.* at [0038]. Likewise, Kim explains that "[t]he chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2 and buffered." *Id.* at [0032].

269. A Skilled Artisan would have understood from this disclosure that the rank selecting unit 1100 includes a control circuit that receives control signals, including chip selection signals and read and write command signals from an external device and, in response, provides internal read and write signals that control the write and read selecting units 1110 and 1120 to direct the data transfer selectively to or from TSV1 through the "*first data conduit*" (pink) or to or from TSV2 through the "*second data conduit*" (rose). Therefore, the state of those "*data conduits*" is controlled to be active or not active and to transmit data in the read or write direction.

270. Furthermore, as discussed above with reference to claim limitation [1.b], a Skilled Artisan would have understood that the chip selection and read and write command signals are "*received via one or more second terminals of the plurality of terminals.*" *Supra* ¶¶189-210. For example in the combination of Kim and Rajan, the "*control circuit*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices on the memory module.

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Supra at ¶¶138-141, 150-168; *see also* Ex. 1015 (Rajan) at 6:30-7:67 (describing specific examples of rank multiplication).

271. Therefore, Kim alone and in view of Rajan discloses this limitation to a Skilled Artisan.

272. Accordingly, the prior art references in each of Grounds 1, 2 and 3 satisfy "*the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals*."

2. Claim 2 is Unpatentable

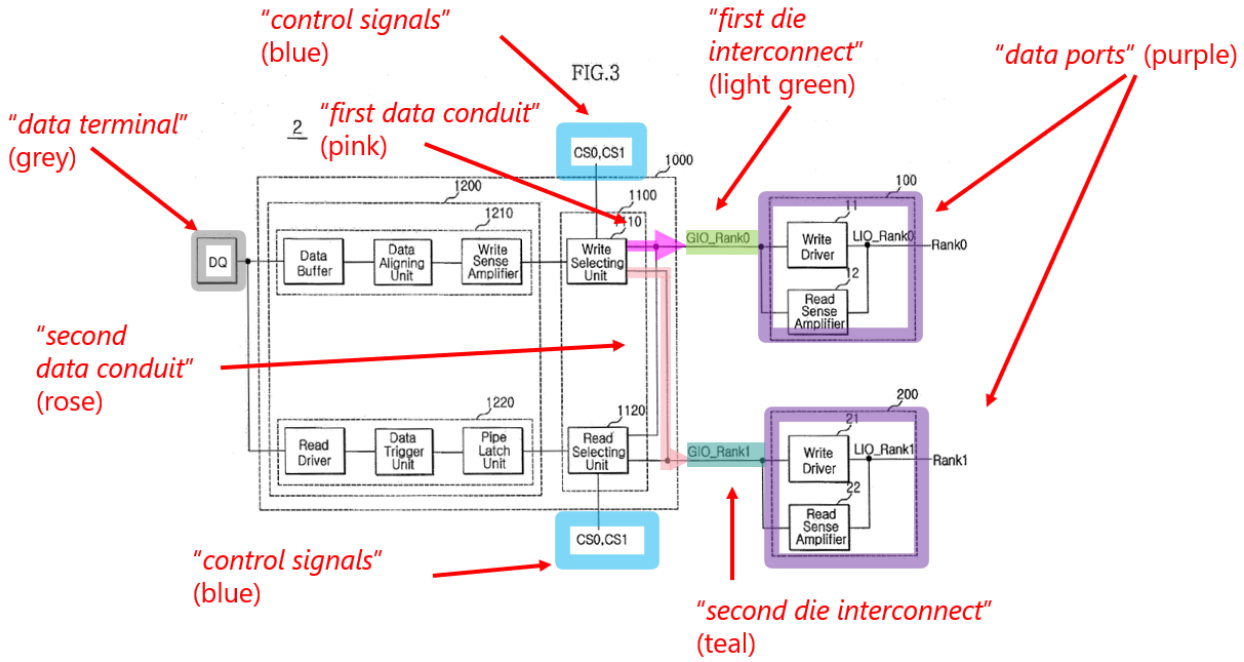
273. Claim 2 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

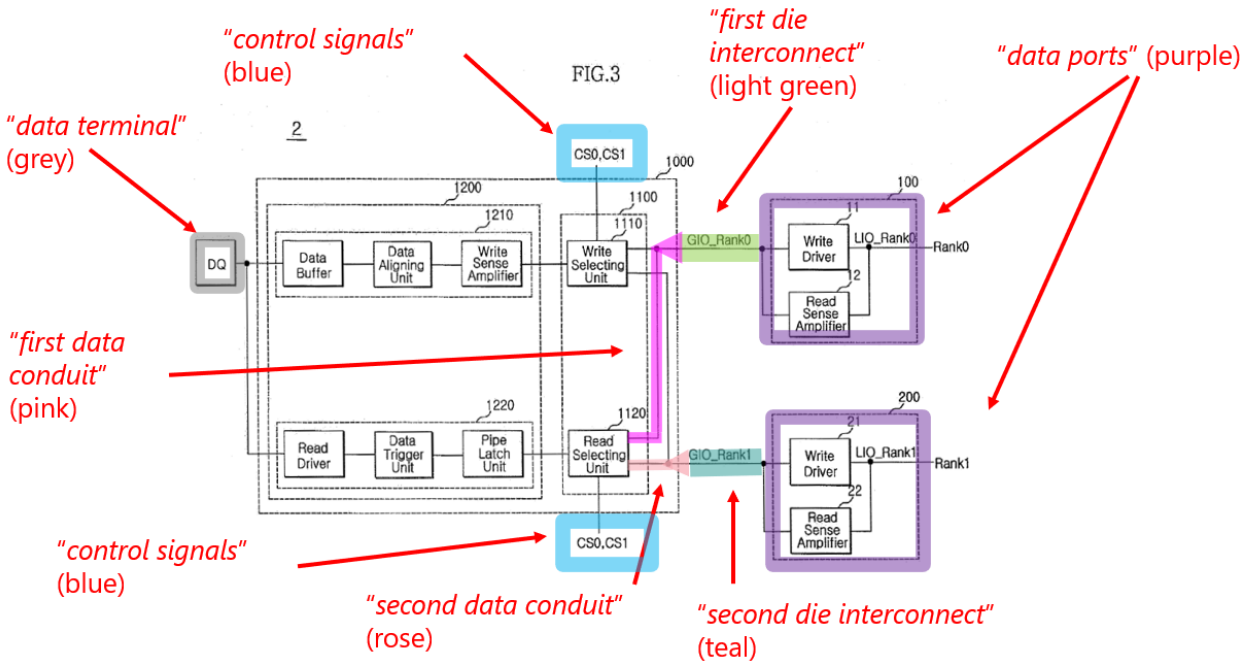
274. Claim 2 requires "*[t]he memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits*."

275. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

276. Kim discloses that "*the control signals* [from the external device] *include data path control signals* [such as chip select and read and write command signals pursuant to the JEDEC standard] *for controlling the first* [(annotated pink below)] *and second* [(annotated rose below)] *data conduits* [including controlling

the direction of the data transfer for read or write and the selection of transferring the data through either TSV1 or TSV2]." *See, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





277. For the reasons discussed above with reference to claim limitation [1.e.4], Kim's rank selecting unit 1100 includes a control circuit that receives control signals, including chip selection signals and read and write command signals from an external device and, in response, controls the write and read selecting units 1110 and 1120 to direct the data transfer selectively to or from TSV1 through the "*first data conduit*" (pink) or to or from TSV2 through the "*second data conduit*" (rose). *Supra* ¶¶265-272. A Skilled Artisan would have understood that the chip selection signals and read and write command signals disclosed in Kim are "*data path control signals*" because these signals determine the direction of the data transfer (read or write) and also select the TSV (TSV1 or TSV2) through which data is transmitted from or to Rank0 or Rank 1, respectively. A Skilled Artisan would have understood that such a selection of TSV1 or TSV2 happens, for example, to avoid collisions. Ex. 1014 (Kim) at [0031] ("Accordingly, even though the first and second ranks Rank0 and Rank1 may comprise one data input/output circuit, the semiconductor memory apparatus 2 may allow a read operation and a write operation to be selectively performed for one of the first and second ranks Rank0 and Rank1 in response to the chip selection signals CS0 and CS1, whereby it is possible to prevent a data collision from occurring.").

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278. Furthermore, in the combination of Kim and Rajan, the memory module can implement rank multiplication. *Supra* at ¶¶138-141, 150-168. For example, the register of the module can generate additional chip select signals and provide those to the stacked memory package. *Id*. Alternatively or in addition, the "*control circuit*" in the memory package may also implement rank multiplication. *Id*. at ¶141.

279. Therefore, Kim discloses this limitation to a Skilled Artisan.

280. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein the control signals include data path control signals for controlling the first and second data conduits.*" limitation.

3. Claim 3 is Unpatentable

281. Claim 3 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

282. Claim 3 requires "*[t]he memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals*."

283. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

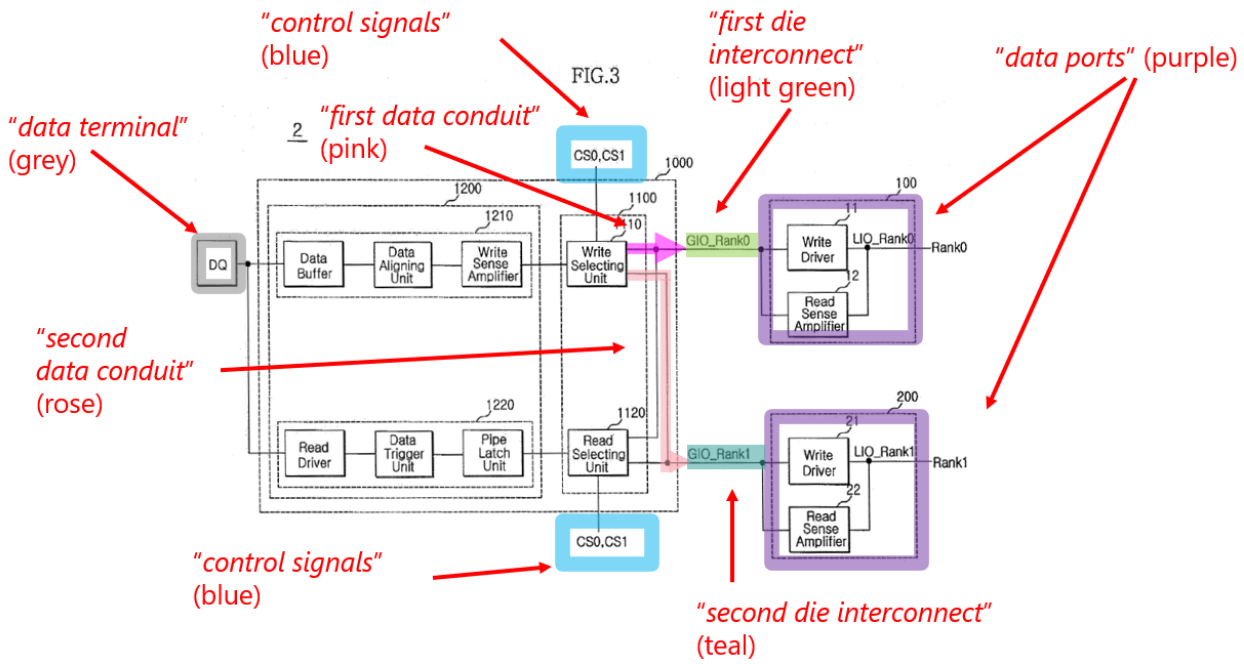
284. Kim discloses that "*the control circuit* [e.g., in rank selecting unit 1100] *is configured to generate data path control signals* [including internal write

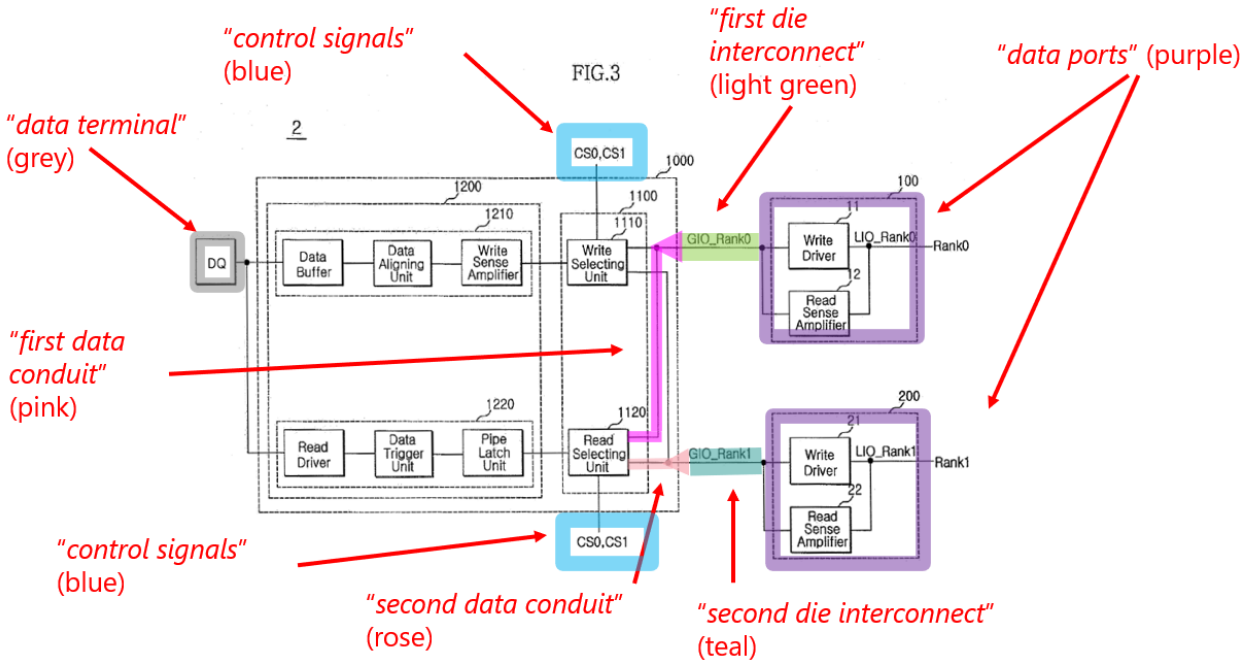
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and read signals] *for controlling the first and second data conduits* [to or from TSV1 or TSV2] *in response to the received control signals* [including chip selection and read and write command signals, from an external device, which may be buffered, e.g., by a register on the memory module]."

285. For example, Kim discloses that, "[w]hile not shown in a drawing, the write selecting unit 1110 and the read selecting unit 1120 may be activated in response to internal write and read signals. The internal write and read signals ["*generate[d] data path control signals*"] may be signals that are generated because write and read command signals applied from a device external to the semiconductor memory apparatus 2 ["*received control signals*"] are buffered." Ex. 1014 at [0038].

286. A Skilled Artisan would have understood, that the internal write and read signals are "*data path control signals for controlling the first and second data conduits in response to the received control signals*" because they (1) determine the direction of data transfer through the data conduits, (2) select whether the data is passing through the read selecting unit 1120 or through the write selecting unit 1110 and (3) also select the corresponding data conduit section TSV1 or TSV2 through which the data is transferred. *See, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





287. Furthermore, the combination of Kim and Rajan renders obvious to a Skilled Artisan to generate the chip selection and other control signals and the corresponding read and write commands and their respective timing according to the characteristics of the physical memory dies, while the memory package

emulates one or more memory devices with different characteristics. *Supra* at ¶¶150-168; *see, e.g.,* Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). For example, the interface circuit can generate additional chip select signals for rank multiplication. *Supra* at ¶¶138-141; *see, e.g.,* Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

288. Therefore, Kim discloses and in view of Rajan renders obvious this limitation.

289. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals*" limitation.

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4. Claim 4 is Unpatentable

290. Claim 4 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [4.a] Command/Address Signals

291. Claim 4 requires "*[t]he memory package of claim 3, wherein the control signals include command/address signals*."

292. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

293. Kim discloses and renders obvious, at least in view of Rajan, to a Skilled Artisan that "*the control signals include command/address signals*," such as "write and read command signals applied from a device external to the semiconductor memory apparatus." Ex. 1014 at [0038]; *supra* at ¶¶150-168. As discussed above with referenced to claim limitation [1.b], and in light of the well-known JEDEC standards, a Skilled Artisan would have understood and it would have been obvious to her from the disclosure of Kim alone and in combination with Rajan that "write and read command signals" include chip-select signals and address signals identifying where to store or retrieve the data. *Supra* ¶¶189-210; Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including chip select terminals CSn#, command signal terminals RAS#, CAS# WE#, and address signal terminals A0-A15), p.18 (describing read and write

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operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read and Write commands with corresponding column address, CA); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35. Rajan also discloses that the control signals include command and address signals, e.g., as required by the JEDEC standards. *Supra* at ¶¶150-168; *see, e.g.*, Ex. 1015 (Rajan) at Figs. 4 and 18 (reproduced below).

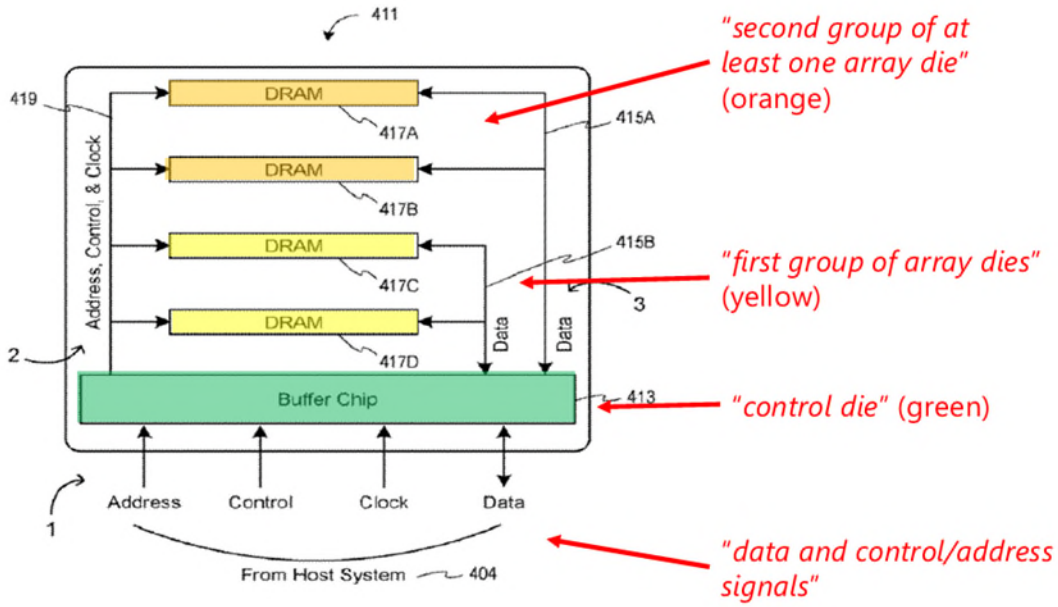


FIG. 4

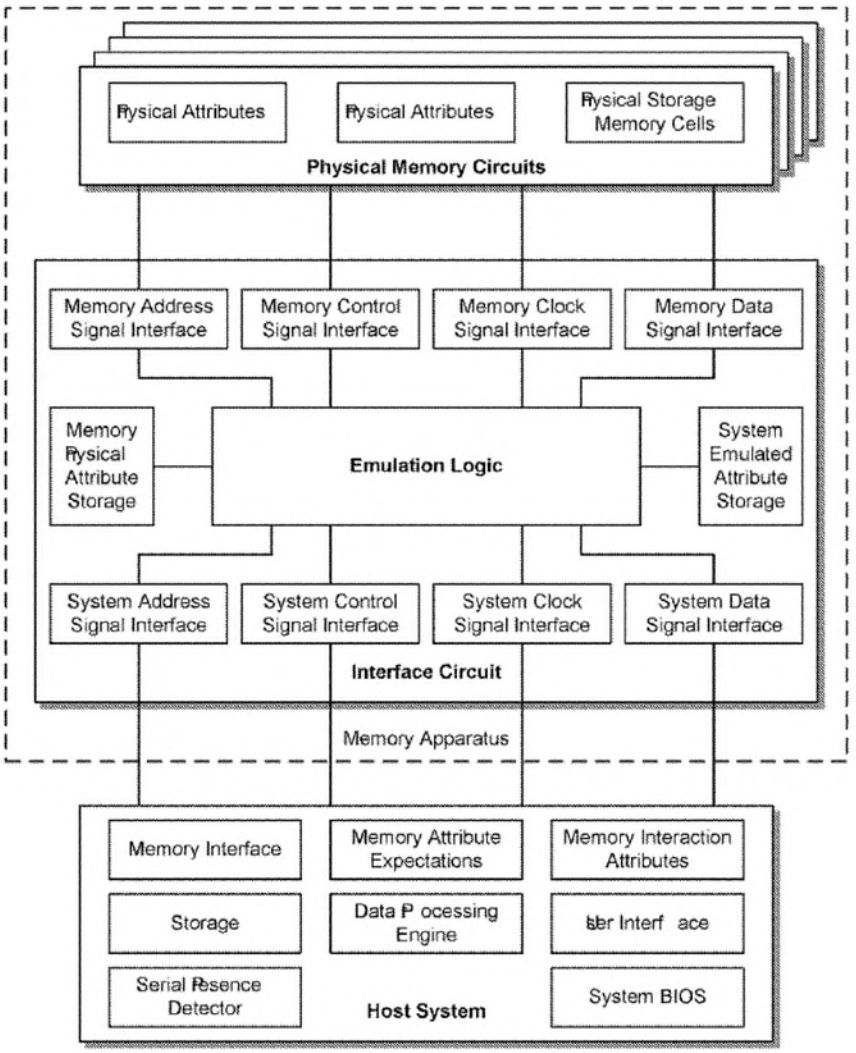


FIG. 18

294. Therefore, Kim discloses and renders obvious this limitation in view of Rajan to a Skilled Artisan.

295. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*[t]he memory package of claim 3, wherein the control signals include command/address signals*."

b) [4.b] Control Die Configured to Provide Command/Address Signals to Stacked Array Dies

296. Claim 4 further requires "*wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.*"

297. The prior art references in each of Grounds 1-3 teach this limitation to a Skilled Artisan.

298. As discussed immediately above, a Skilled Artisan would have understood that Kim's disclosure of "write and read command signals applied from a device external to the semiconductor memory apparatus" includes command and address signals, e.g., according to the JEDEC standards and/or as taught by Rajan. Ex. 1014 at [0038]; *supra* at ¶293.

299. Kim discloses and renders obvious to a Skilled Artisan that "*the control die* [main chip C0] *is configured to provide the command/address signals* [for the read and write commands] *to the plurality of stacked array dies*."

300. For example, Kim discloses that, "if command signals are applied from an external device, the command signals are buffered by a buffer which is provided in the semiconductor memory apparatus." Ex. 1014 at [0032]. Kim also discloses that the "write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered." Ex. 1014 at [0038]. Kim explains that the stacked array dies can perform the corresponding write and read operations. *See id*. at [0029-30] ("Therefore, the read operation of the first rank

Rank0 may be performed. … Therefore, the read operation of the second rank Rank1 may be performed…. Therefore, the write operation of the first rank Rank0 may be performed. … Therefore, the write operation of the second rank Rank1 may be performed.").

301. A Skilled Artisan would have understood and it would have been obvious to her from this disclosure that Kim's main chip C0 buffers write and read command signals and the corresponding address signals, and that main chip C0 then provides those buffered signals to the stacked array dies enabling those dies to perform the corresponding read and write operations.

302. To the extent one might argue that Kim does not sufficiently disclose providing command/address signals to the stacked memories, it would have been obvious to a Skilled Artisan in view Rajan. Rajan discloses stacked memory chips with a buffer chip providing buffered address and control signals to each memory chip. *See* Ex. 1015 at Figs. 4 (reproduced below, annotated), 18 (reproduced below), 14:11-18 ("The interface circuit may be included in the buffer chip, for example. The interface circuit includes a system address signal interface for sending/receiving address signals to/from the host system, a system control signal interface for sending/receiving control signals to/from the host system, a system clock signal interface for sending/receiving clock signals to/from the host system,

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and a system data signal interface for sending/receiving data signals to/from the host system.").

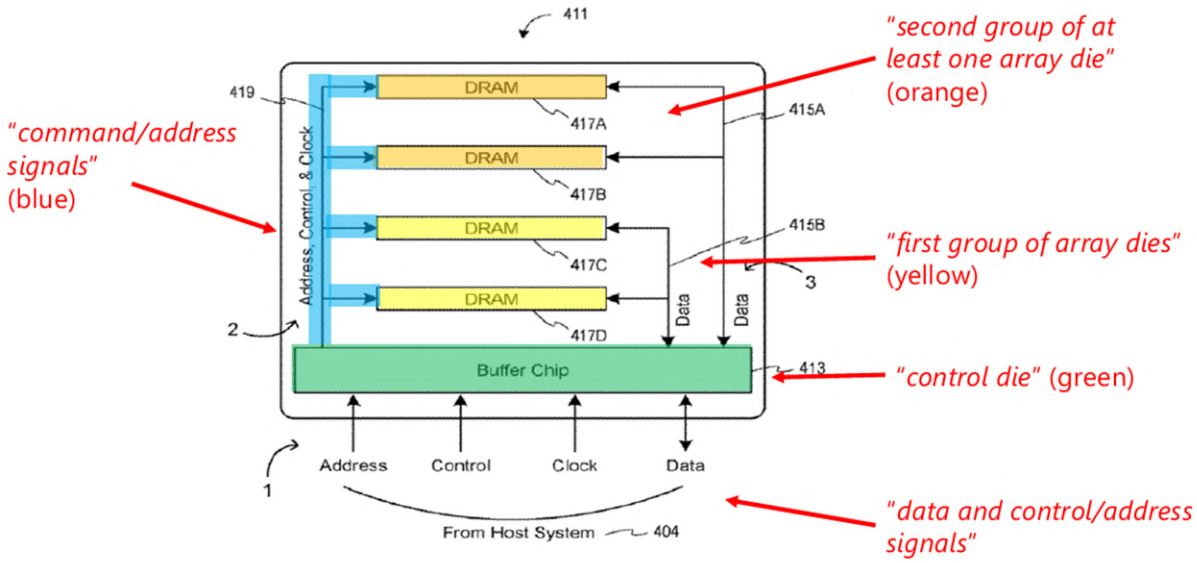


FIG. 4

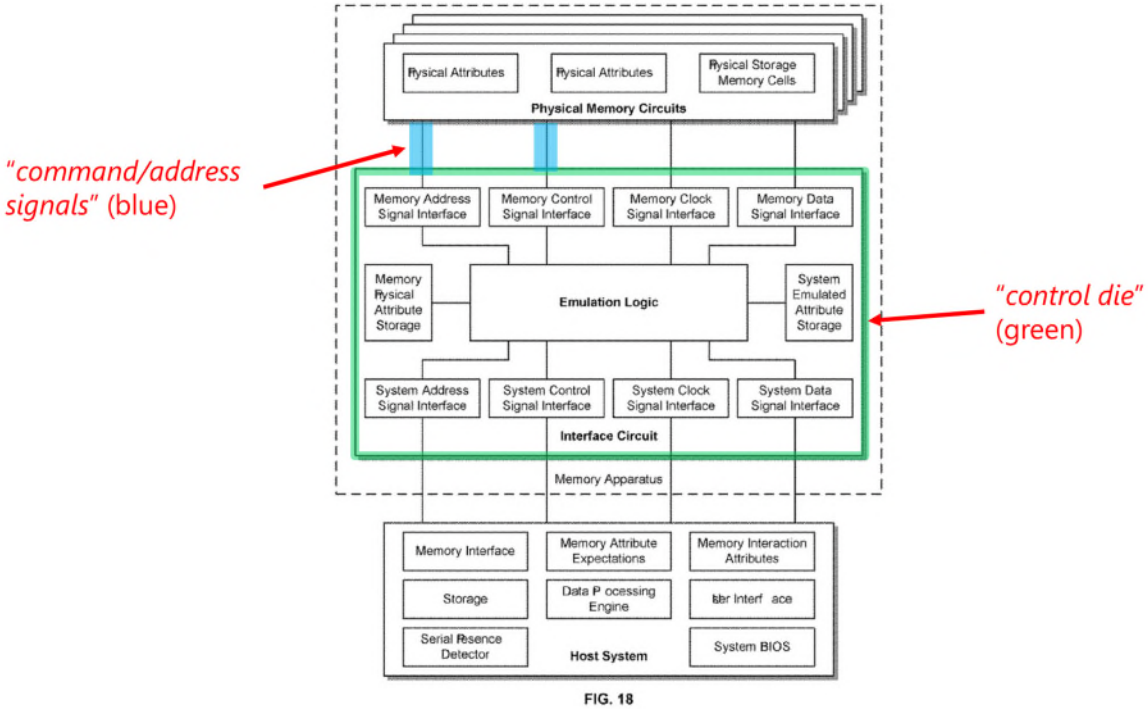
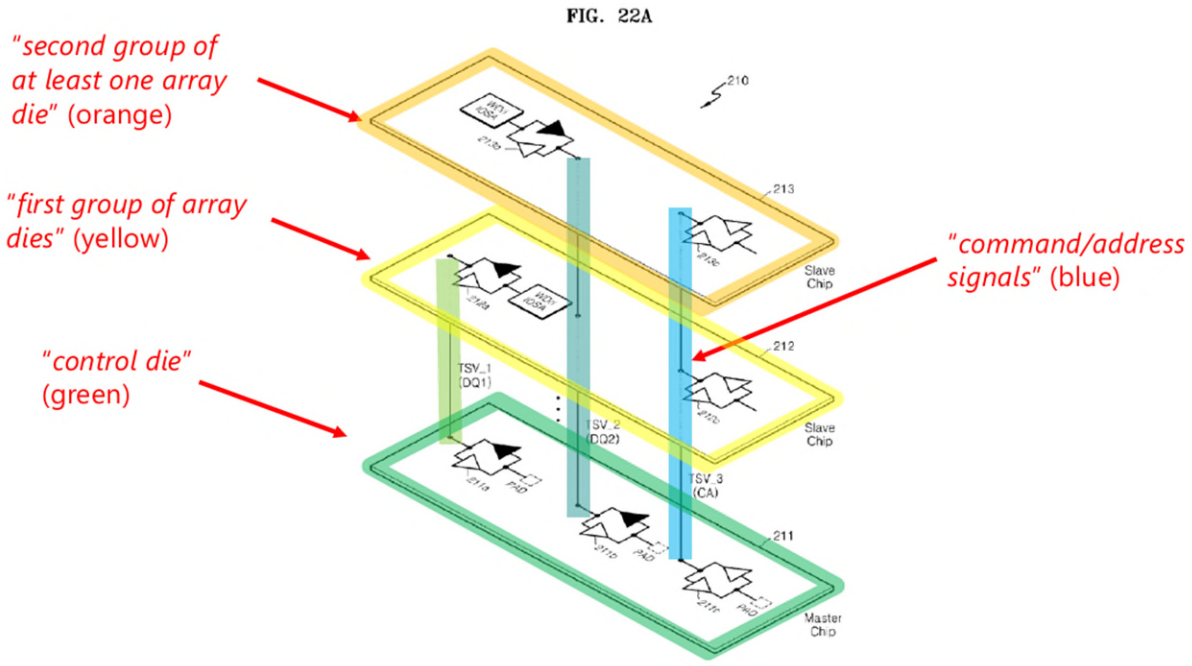


FIG. 18

Rajan also discloses that some of the command and address signals may be passed through to the physical memory devices "unaltered." Ex. 1015 (Rajan) at 14:55-60 ("The emulation logic may, in various embodiments, alter a timing, value, latency, etc. of any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory. Some such signals may pass through unaltered, while others may be altered.").

303. A Skilled Artisan would have been motivated to provide the command/address signals to the memory chips in the stack, because such command and address signals were used by memory devices at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.13 (describing address and control signals for SDRAM devices, including chip-select signals). Providing the address and control signals to each memory chip in the stack was well within the level of skill and required nothing more than what was expected at the time: having the address and control signals available at each memory chip. *See, e.g.*, Ex. 1034 (Lee) at Fig. 22A (reproduced below, annotated).

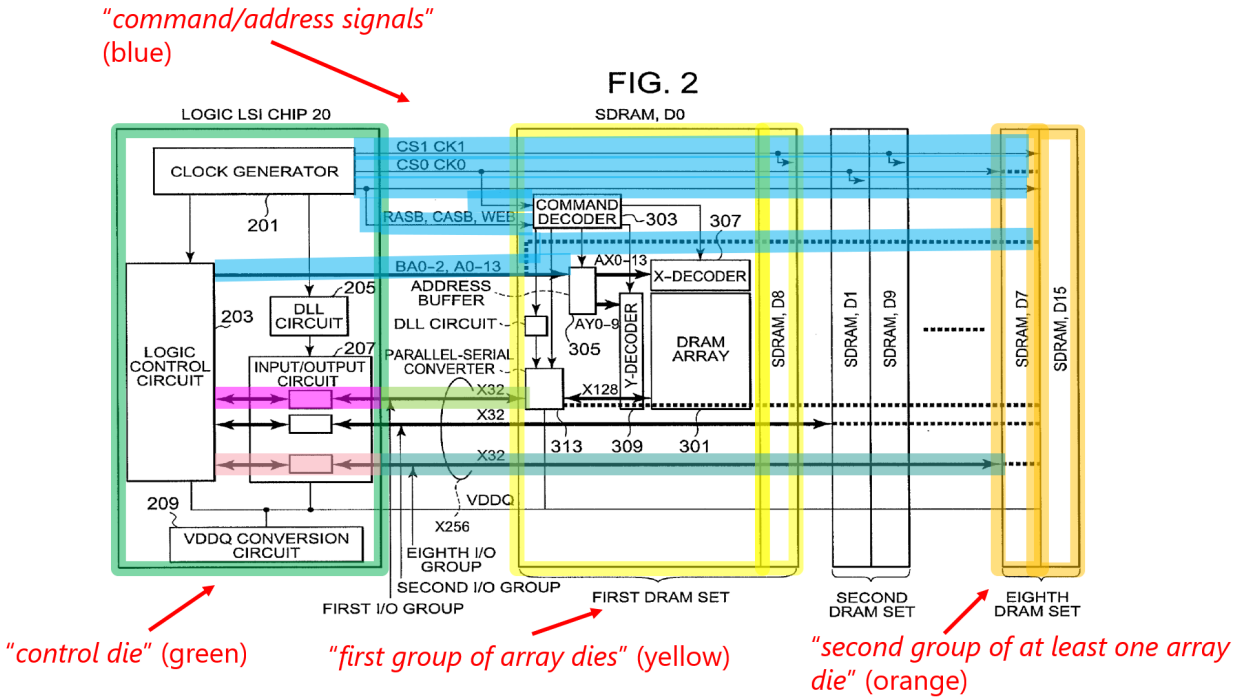
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304. The prior art described in the 060 Patent, specifically Figs. 1A and 1B, demonstrate that providing address and control signals to each memory chip in the stack was well within the level of skill. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for address and command signals from the control chip), 1:39-42 ("Further, the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142."), 2:5-8 ("Further, the memory package 150 includes a driver 186 for driving command and/or address signals to each of the array dies 160 via another die interconnect 188.").

305. Riho further demonstrates that providing address and control signals to each memory chip in the stack was well within the level of skill. Riho discloses stacked memory chips with a control chip (20) providing address and control

signals to each memory chip in the stack. Ex. 1016 at Fig. 2 (reproduced below, showing command decoder and address buffer in memory chip receiving corresponding command and address signals from the control chip 20), [0043] ("The 3-bit bank address signal BA0-2 and the 14-bit address signal A0-13 are supplied to all the SDRAMs D0 to D15 through the address TSVs."), and [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs.").



306. Therefore, Kim discloses and renders obvious this limitation in view of Rajan to a Skilled Artisan.

307. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies*."

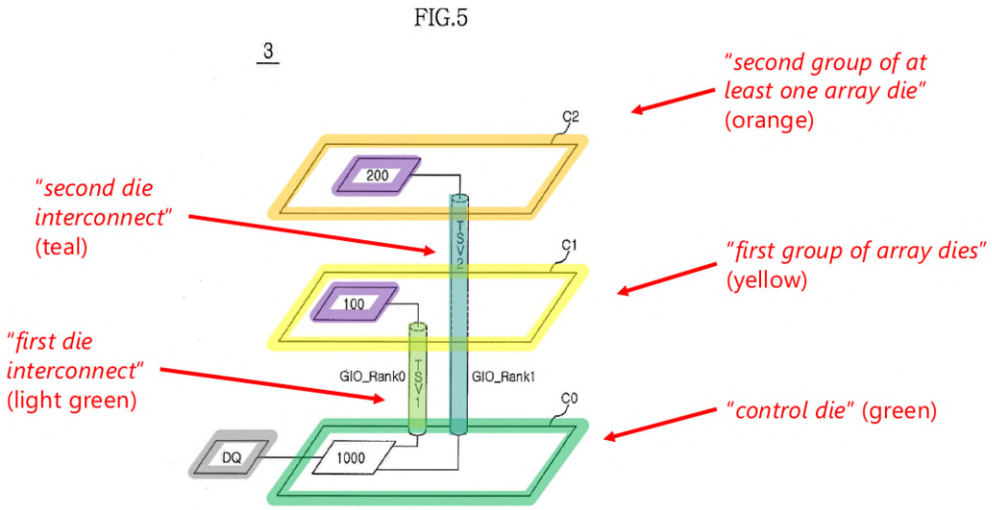
5. Claim 5 is Unpatentable

308. Claim 5 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

309. Claim 5 requires *"[t]he memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via*."

310. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

311. Kim discloses that "*the first die interconnect comprises a first through-silicon via* [TSV1 (annotated light green below)] *and wherein the second die interconnect comprises a second through-silicon via* [TSV2 (annotated teal below)]." *See, e.g.*, Ex. 1014 at [0046-49], Fig. 5 (reproduced below, annotated).



312. Therefore, Kim discloses this limitation to a Skilled Artisan.

313. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via*" limitation.

6. Claim 6 is Unpatentable

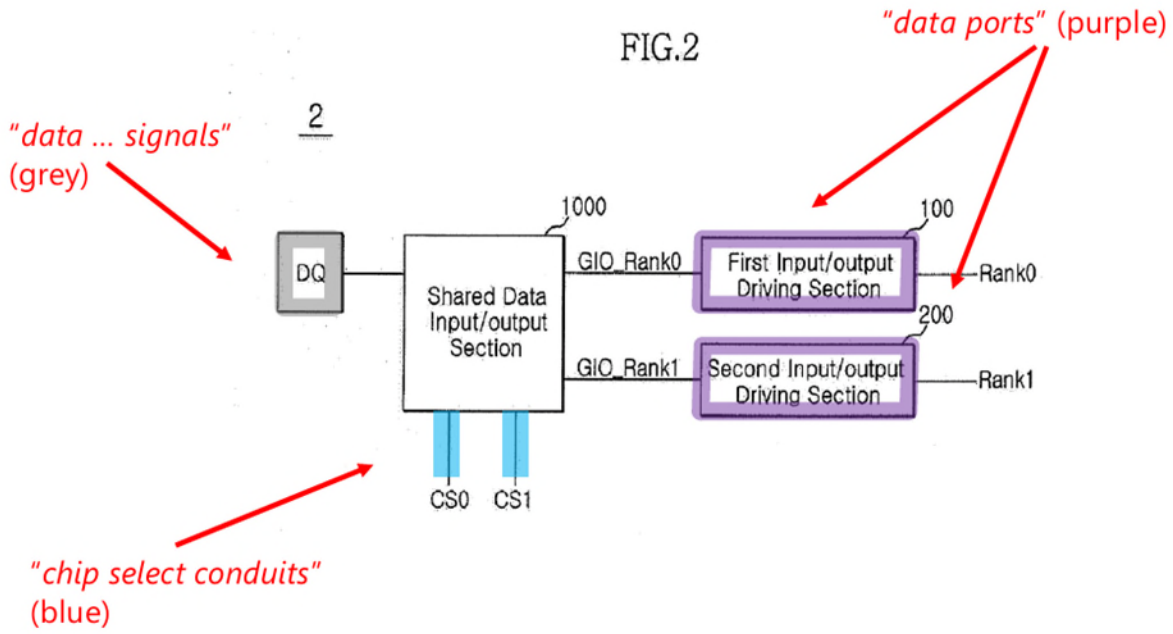
314. Claim 6 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [6.a] Chip-Select Conduits

315. Claim 6 requires *"[t]he memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising*."

316. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

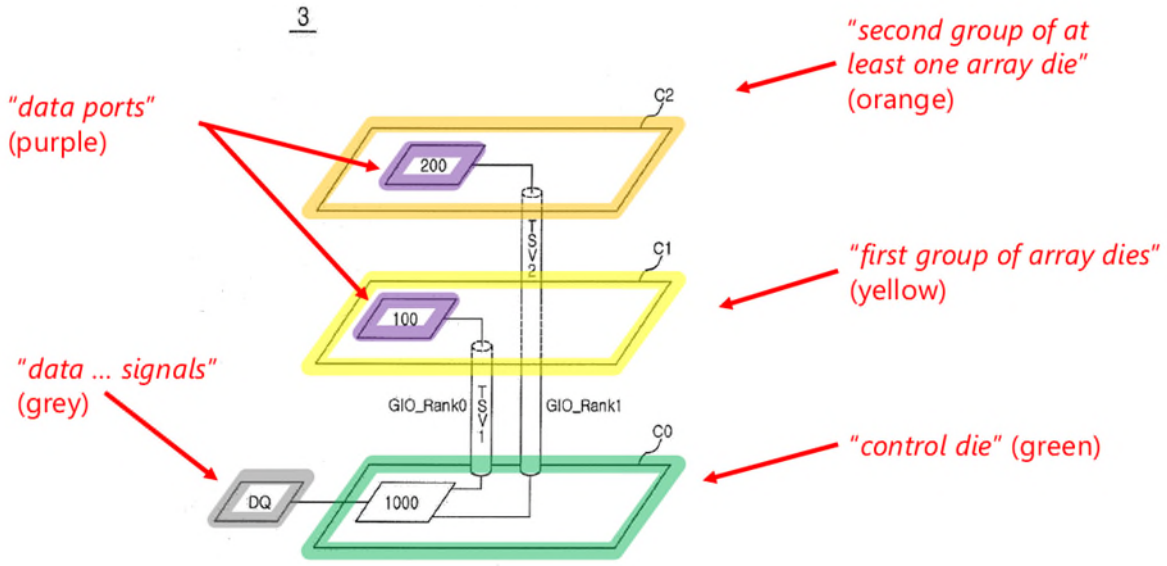
317. Kim discloses to a Skilled Artisan that "*the control die* [main chip C0] *further comprises chip-select conduits* [(annotated blue below) for conducting chip select signals like CS0 and CS1]." *See, e.g.*, Ex. 1014 at Fig. 2 (reproduced below, annotated, showing that chip select signals CS0 and CS1 are used by the shared data input/output section 1000).



318. For example, Kim discloses that the "chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2 and buffered….and may be utilized as internal signals." Ex. 1014 at [0032]. Kim further explains that "[d]uring a read operation, the shared data input/output section 1000 outputs data transmitted from the first input/output driving sections 100 and 200 through a data

pad DQ in response to chip selection signals CS0 and CS1." Ex. 1014 at [0028]. Likewise, Kim explains that "[d]uring a write operation, the shared data input/output section 1000 transmits data inputted through the data pad DQ to one of the first and second input/output driving sections 100 and 200 in response to the chip selection signals CS0 and CS1." *Id.* A Skilled Artisan would have understood that a "chip-select bus … is essential in a JEDEC style memory system, as it enables the intended recipient of a memory request." Ex. 1022 (Jacob) at 319; *see also* Ex. 1023 at pp.2-4, 9 & Fig.16 (same). As shown in Fig. 5 of Kim, the main chip C0 can include the shared data input/output section 1000 which selects TSV1 or TSV2 for a data transaction.

FIG.5



319. A Skilled Artisan would have understood from this disclosure that the main chip including the shared data input/output section 1000 buffers the chip

select signals CS0 and CS1 and includes "*chip-select conduits*" to conduct the buffered chip select signals CS0 and CS1 to other parts of the stack, including to the data input/output section 1000 and to the die-interconnects to the memory dies. *See also* the analysis for claim 12 (explaining that the chip select signal is received at the bottom surface of the control chip and provided to the top surface, *infra* at ¶¶435-443).

320. Furthermore, the combination of Kim and Rajan also renders obvious that the claimed "*chip-select conduits*" transmit the generated chip selection signals to corresponding die-interconnects if the memory package emulates one or more memory devices with different characteristics. *Supra* at ¶¶150-168; *see, e.g.,* Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). For example, the interface circuit can generate additional chip select signals for rank multiplication and the "*chip-select conduits*" transmit the generated chip select signals to corresponding die-interconnects. *Supra* at ¶¶138-141; *see, e.g.,* Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be

decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

321. Furthermore, as discussed above, a Skilled Artisan would have understood that the "buffered" chip select signals would have been driven to off-chip circuits, such as the memory dies in the stack. *Supra* at ¶¶135-137. Therefore, a Skilled Artisan would have understood, and been motivated, to include drivers in the "chip-select conduits" in order to transmit the chip select signal properly to the respective dies. *Id*.

322. Therefore, Kim discloses and in view of Rajan renders obvious this limitation to a Skilled Artisan.

323. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the control die further comprises chip-select conduits, the memory package further comprising*" limitation.

b) [6.b] Third Die Interconnects

324. Claim 6 requires "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies*."

325. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

326. Kim discloses to a Skilled Artisan "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of*

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stacked array dies," such as "*die interconnects*" between the main chip C0 and the slave chips C1 and C2 which couple the buffered chip select signals CS0 and CS1 from the main chip C0 to slave chips C1 and C2, respectively, to perform read and write operations.

327. For example, Kim explains that "[d]uring the read operation, when the first rank Rank0 is selected by the chip selection signals CS0 and CS1, that is, when a first chip selection signal CS0 is enabled, … the read operation of the first rank Rank0 may be performed. Also, during the read operation, when the second rank Rank1 is selected by the chip selection signals CS0 and CS1, that is, when a second chip selection signal CS1 is enabled, … the read operation of the second rank Rank1 may be performed." *Id*. at [0029]. Similarly, Kim explains that "[d]uring the write operation, when the first chip selection signal CS0 is enabled, … the write operation of the first rank Rank0 may be performed. Also, during the write operation, when the second chip selection signal CS1 is enabled, … the write operation of the second rank Rank1 may be performed." *Id*. at [0030]. Kim further explains that "the first chip selection signal CS0 becomes a signal for selecting the first slave chip C1, and the second chip selection signal CS1 becomes a signal for selecting the second slave chip C2." *Id*. at [0049].

328. A Skilled Artisan would have understood from this disclosure that the chip selection signal CS0, which is buffered on the main chip C0, is transmitted to

slave chip C1 through a respective die interconnect to enable read and write operations from the first rank Rank0. Similarly, the chip selection signal CS1, which is buffered on the main chip C0, is transmitted to slave chip C2 through a respective die interconnect to enable read and write operations from the second rank Rank1.

329. To the extent one might argue that Kim does not sufficiently disclose die interconnects for the chip select signals, it would have been obvious to a Skilled Artisan in view of Rajan. For example, Rajan discloses that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." *Supra* at ¶¶150-168; *see, e.g.*, Ex. 1015 (Rajan) at 6:34-38 and Fig. 4 (reproduced below, annotated).

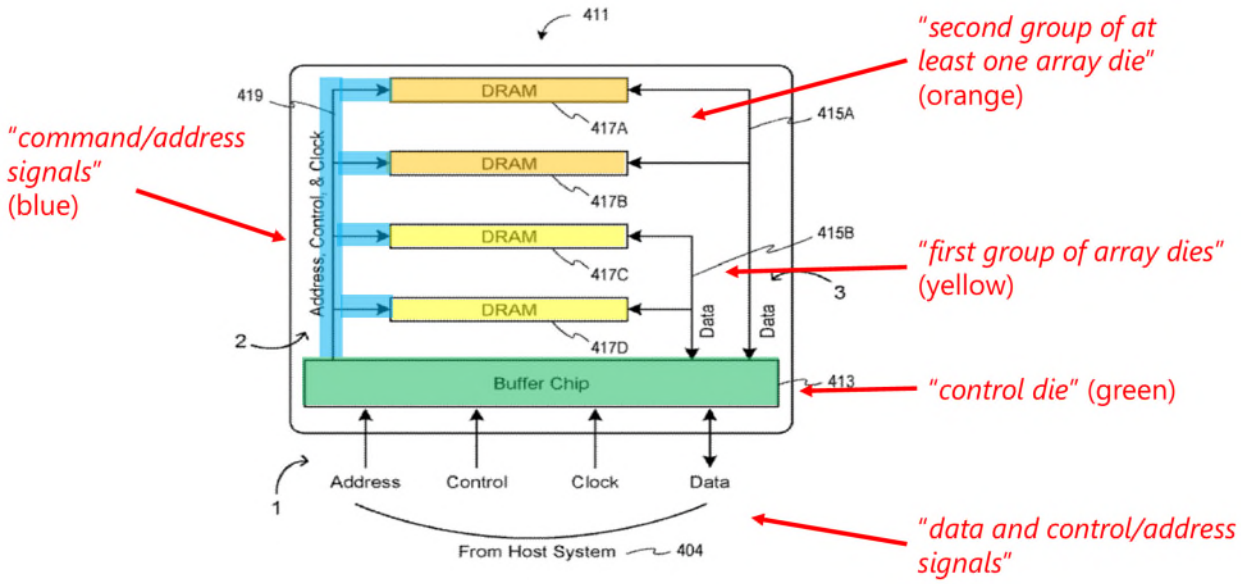


FIG. 4

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330. Using separate chip select signals for selecting a chip in the stack, as described by Rajan, was well known at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Figs. 1-3 showing stacked DDR3 chips, each receiving a separate chip select signal), p.13 (explaining that chip select "provides for external Rank selection on systems with multiple Ranks"), Fig. 2 (reproduced below, annotated to indicate chip select signals); *see also* Ex. 1022 at 319 (the "chip-select bus … is essential in a JEDEC style memory system"); Ex. 1023at 2-4, 9, Fig.16.

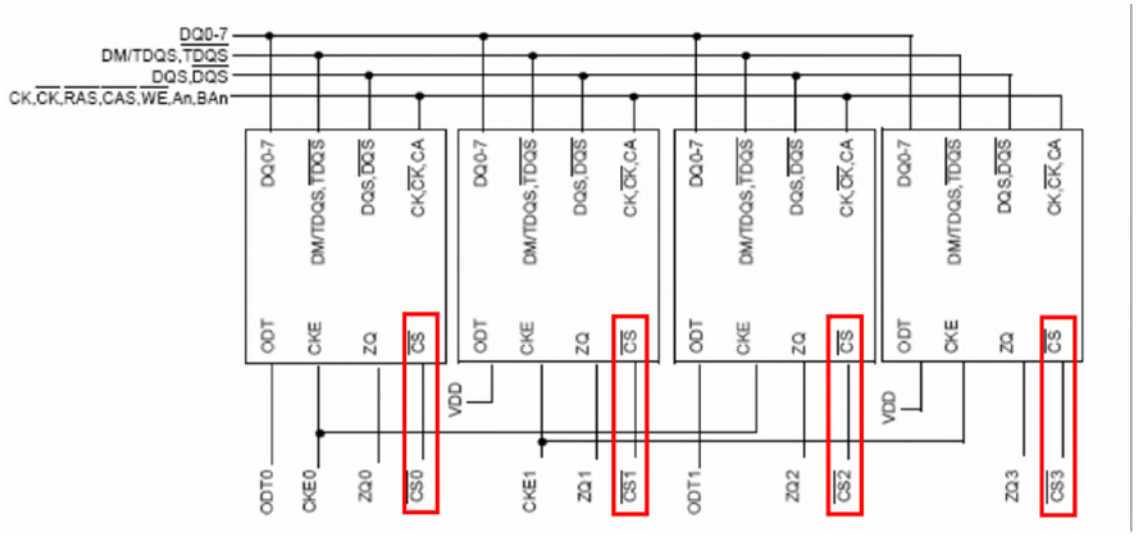


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

331. The prior art described in the 060 Patent, specifically Figs. 1A and 1B, demonstrate that transmitting separate chip select signals through die interconnects to select a chip in the stack was well known at the time. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for chip select signals), 1:49-56 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable

or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.").

332. US 2011/0026293 to Riho ("Riho") further demonstrates that using interconnects for the chip select signals was well within the level of skill. *See, e.g.*, Ex. 1016 at [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs.").

333. Therefore, Kim discloses and renders obvious in view of Rajan this limitation to a Skilled Artisan.

334. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies*" limitation.

7. Claim 7 is Unpatentable

335. Claim 7 is unpatentable as the prior art references in Ground 2 render the claim obvious.

a) [7.a] Selecting A First and Second Number of Array Dies Based on Load of Die Interconnects

336. Claim 7 requires *"[t]he memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in*

consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit." As discussed above, I understand that claim 7 may improperly mix a method claim with an apparatus claim, but I do not believe this issue needs to be resolved for purposes of my invalidity analysis below, because regardless of whether claim 7 is interpreted as an apparatus claim or a mixed apparatus and method claim, in my opinion it is obvious in light of the prior art as discussed below. *See supra* ¶ 113.

337. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

338. Kim, in view of Riho, renders obvious to a Skilled Artisan that "*a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit*."

339. As discussed above, a Skilled Artisan would have been motivated to use Riho's shared data signal TSVs in Kim's stack. *Supra* ¶¶169-173. For example, Riho discloses that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-

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silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 at [0103]. Riho explains the advantages in the write operation as follows: "The load capacitance to 256 data signals DQ is reduced by half. Accordingly, the operating current is reduced and the high-frequency operation is achieved. Further, load capacitance variations of the data buses caused by a capacitance variation of (2±0.5) pF possessed by each DQ pin are also reduced. Therefore, SDRAM input set-up and hold margin are increased." Ex. 1016 at [0119]. Likewise, Riho explains the advantages in the read operation: "Since the DQ load on the SDRAM chip side of the 256 data buses is reduced by half, the operating current is reduced and the high-frequency operation is achieved. It is also possible to remove capacitance variations of the data buses. It is possible to remove interference due to a reflected wave caused by L1 of the SDRAM D15. Logic LSI chip input set-up and hold margin are increased." *Id.* at [0120].

340. Riho further explains that, "since the data signal DQ and data strobe signal DQS/B TSVs for all the DRAM sets corresponding to the respective I/O groups can be made substantially equal in length to each other, the skew between data signals DQ and data strobe signals DQS/B can be minimized. This structure (equi-length interconnections) is very important in the stacked structure in which the plurality of DRAM sets are stacked in sequence with respect to the controller

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chip." Ex. 1016 at [0050]. Riho describes that "in this embodiment, each I/O group is formed by ×32 DQ signal bits and the controller chip can perform communication control of the plurality of I/O groups (×256 DQ signal bits) with a single synchronization signal and with high accuracy." Ex. 1016 at [0050]; *see also id.* at [0053-54].

341. A Skilled Artisan would have understood from this disclosure that, in the combination of Kim and Riho, "*a first number of* [two] *array dies in the first group of array dies* [sharing a data signal TSV] *and a second number of at least one array die* [i.e., two dies] *in the second group of at least one array die* [sharing another data signal TSV] *are selected in consideration of a load of the first die interconnect and a load of the second die interconnect* [including the load of each of those data signal TSVs] *so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit* [which a Skilled Artisan understood reduces skew between the data signals]." *Supra* at ¶¶135-137. For example, a Skilled Artisan would have understood that the larger the capacitive load, the larger the delay in the transition of the driven signal. Ex. 1030 (Brown) at p.134. Accordingly, a difference in load may result in different signal timing, resulting in a skew between different signals. For example, DQ and DQS signals should be synchronized, but a skew between them may result in an erroneous read of the data value. Ex. 1019 (JESD79-3C) at 13 ("The data strobes DQS, DQSL,

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and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes."). Thus, a Skilled Artisan would have also understood that, when each data (and strobe) signal TSV is made to have substantially the same length, and each data (and strobe) signal TSV is connected to the same number of two SDRAMs, the difference in load for driving the data (and strobe) signals on different TSVs is reduced. As a result, for example, "the skew between data signals DQ and data strobe signals DQS/B can be minimized." Ex. 1016 at [0050]. Riho further explains that "[t]his structure (equi-length interconnections) is very important in the stacked structure in which the plurality of DRAM sets are stacked in sequence with respect to the controller chip. This is because, in this embodiment, each I/O group is formed by ×32 DQ signal bits and the controller chip can perform communication control of the plurality of I/O groups (×256 DQ signal bits) with a single synchronization signal and with high accuracy." *Id*.

342. Therefore, Kim renders obvious in view of Riho this limitation to a Skilled Artisan.

343. Accordingly, the prior art references in Ground 2 satisfy the "*wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die*

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interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit" limitation.

b) [7.b] The First and Second Load

344. Claim 7 requires "*the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die*."

345. The prior art references in Ground 2 teach this limitation to a Skilled Artisan.

346. The combination of Kim and Riho discloses "*the first load including a load of the first die interconnect* [on one data signal TSV]*, and a load of the first group of array dies* [including a pair of SDRAM chips]*, and the second load including a load of the second die interconnect* [on another data signal TSV] *and a load of the second group of at least one array die* [including another pair of SDRAM chips]."

347. For example, Riho discloses that, "when the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used." Ex. 1016 at [0013].

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Riho further explains that "the load capacitance from the disconnected SDRAM becomes off so that it is possible to reduce by half the load of a data signal DQ." *Id.* at [0132].

348. A Skilled Artisan would have understood from this disclosure that the load for driving the data signals includes the load of the interconnecting vias and the load of the SDRAMs coupled to those vias. *Supra* at ¶¶135-137.

349. Therefore, Kim renders obvious in view of Riho this limitation to a Skilled Artisan.

350. Accordingly, the prior art references in Ground 2 satisfy "*the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die*" limitation.

8. Claim 8 is Unpatentable

351. Claim 8 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

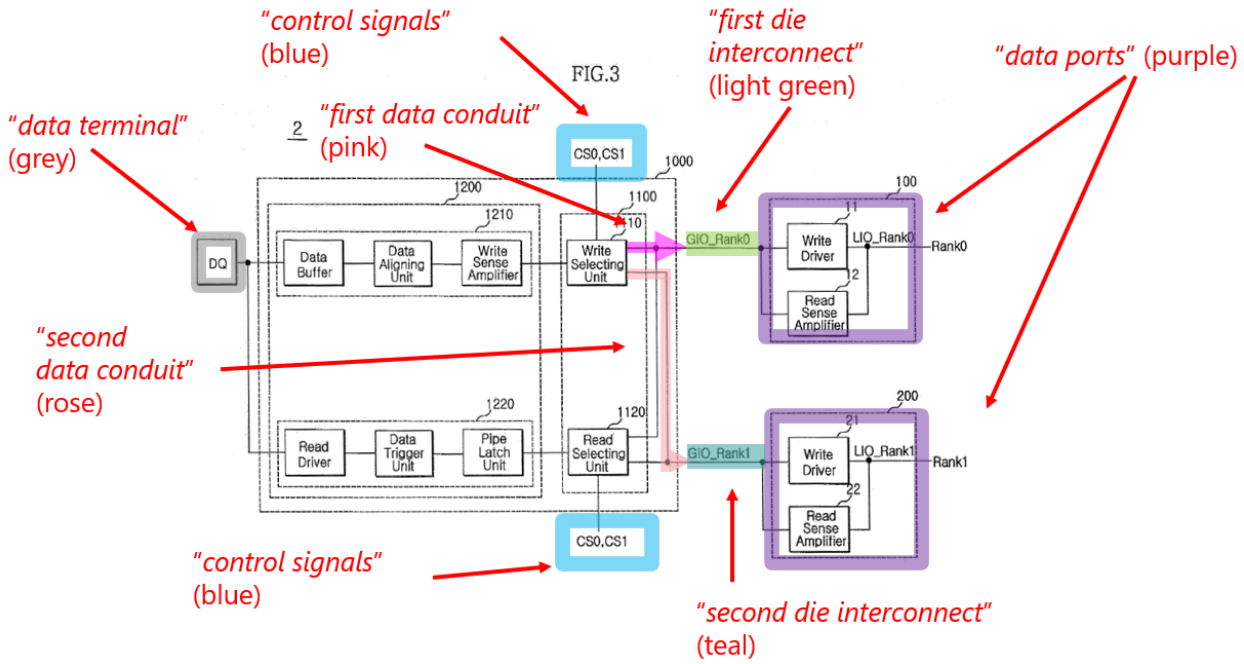
a) [8.a] Data Path Control Signals

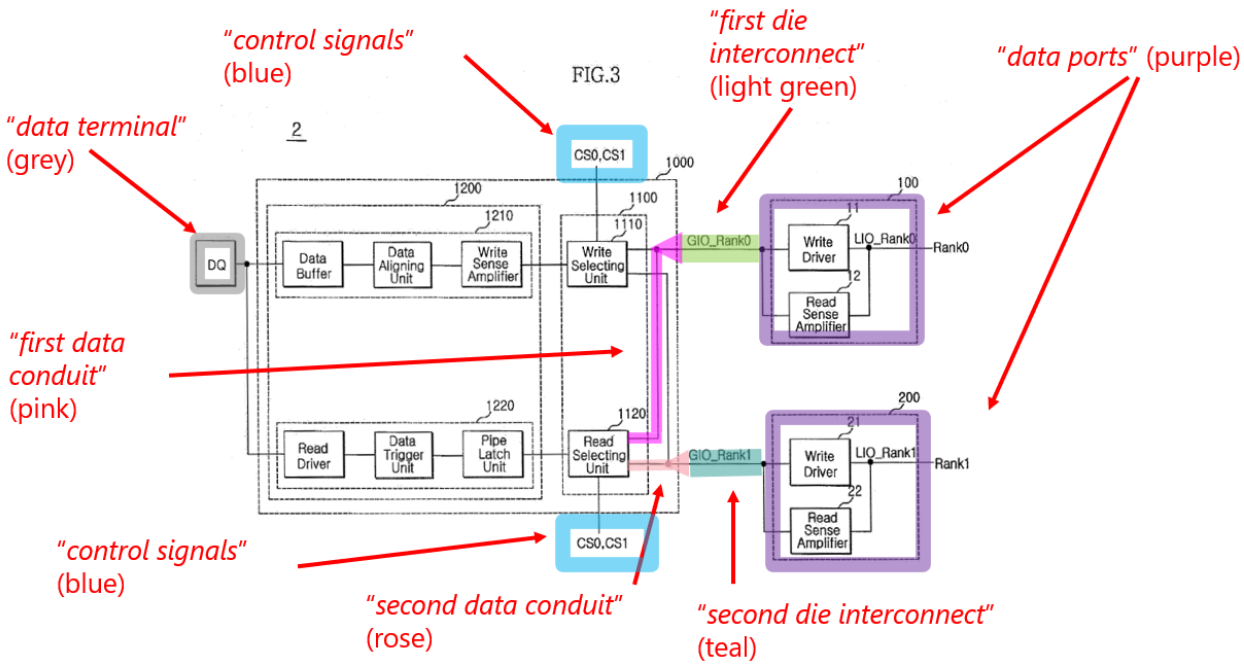
352. Claim 8 requires "*[t]he memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals*."

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353. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

354. Kim discloses that "*the respective states of the first data conduit* [(annotated pink below, connected to TSV1)] *and the second data conduit* [(annotated rose below, connected to TSV2)] *are controlled by one or more data path control signals*," such as the chip select and read and write command signals for the reasons discussed above with reference to claims 2 and 3. *Supra* ¶¶273-280 (claim 2), ¶¶281-289 (claim 3); *see, e.g.*, Ex. 1014 at Fig. 3 (reproduced below, annotated for write operations (first figure) and read operations (second figure)).





355. Therefore, Kim discloses this limitation to a Skilled Artisan.

356. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals*" limitation.

b) Control Die

(1) [8.b.1] Control Die is Configurable

357. Claim 8 requires "*wherein the control die is configurable to operate in any one of a first mode and a second mode*."

358. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

359. The combination of Kim and Rajan discloses to a Skilled Artisan that "*the control die is configurable to operate in any one of a first mode* [e.g., where

the number of ranks seen by the system is the same as the number of ranks in the stack] *and a second mode* [e.g., where Rajan's interface implemented in Kim's main chip C0 emulates an interface with fewer ranks than the number of ranks in the stack]."

360. For example, Rajan discloses that its "interface circuit includes emulation logic which operates according to the stored memory physical attributes and the stored system emulation attributes, to present to the system an interface to an emulated memory which differs in at least one attribute from the actual physical memory." Ex. 1015 at 14:51-55. Rajan explains that "[t]he emulation logic may, in various embodiments, alter a timing, value, latency, etc. of any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory. Some such signals may pass through unaltered, while others may be altered. The emulation logic may be embodied as, for example, hard wired logic, a state machine, software executing on a processor, and so forth." *Id.* at 14:55-62; *see also id.* at Fig. 18 (reproduced below).

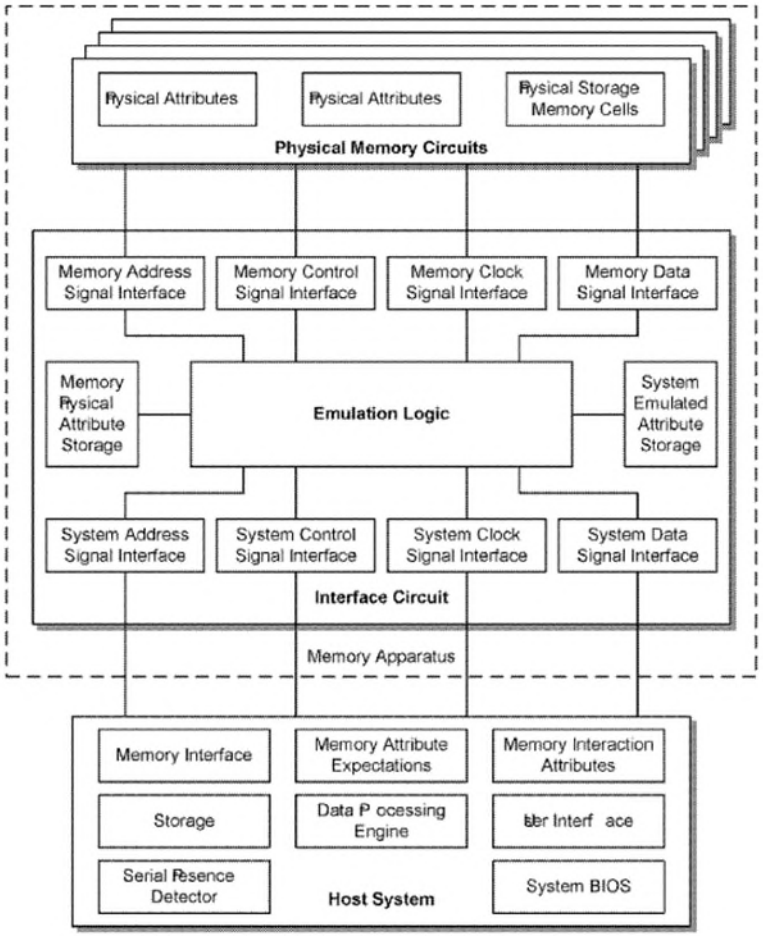


FIG. 18

361. A Skilled Artisan would have understood from this disclosure that Rajan's interface and its emulation logic can be configured "*to operate in any one of a first mode and a second mode*," depending on the memory's physical attributes and the system emulation attributes stored in the interface circuit.

362. Furthermore, as discussed above, a Skilled Artisan would have been motivated to combine the teaching of Kim and Rajan to emulate certain characteristics of the system interface. *Supra* ¶¶150-163. Accordingly, a Skilled Artisan would have also been motivated to implement Rajan's different modes of

interface operation in Kim's memory stack to allow the stack to operate in host systems having different memory attribute expectations and memory interaction attributes. *See, e.g.*, Ex. 1015 at Abstract ("A memory subsystem is provided including an interface circuit adapted for communication with a system."), Fig. 18 (reproduced above).

363. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

364. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the control die is configurable to operate in any one of a first mode and a second mode*" limitation.

(2) [8.b.2] First Mode

365. Claim 8 further requires "*wherein: in the first mode, the control die receives the data path control signals from the one or more external devices*."

366. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

367. Kim discloses that, "*in the first mode, the control die receives the data path control signals* [such as chip selection signals CS0 and CS1 and read and write commands] *from the one or more external devices*" for the reasons discussed above with reference to claim 2. *Supra* ¶¶273-280.

368. Therefore, Kim discloses this limitation to a Skilled Artisan.

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369. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein: in the first mode, the control die receives the data path control signals from the one or more external devices*."

(3) [8.b.3] Second Mode

370. Claim 8 further requires "*wherein: . . . in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices*."

371. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

372. The combination of Kim and Rajan renders obvious to a Skilled Artisan that, "*in the second mode* [where Rajan's interface implemented in Kim's main chip C0 emulates an interface with fewer ranks]*, the control die generates the data path control signals* [including chip selection signals] *from at least some of the control/address signals received from the one or more external devices.*"

373. As discussed above with reference to claim limitation [8.b.1], it would have been obvious to implement Rajan's interface emulation mode in Kim's main (interface) die to allow it to operate with systems having different attribute requirements, such as different number of ranks ("rank multiplication"). *Supra* ¶¶138-140, 357-364. Furthermore, Rajan discloses that, in such an emulation mode, the emulation logic can generate chip selection signals "*from at least some*

of the control/address signals received from the one or more external devices." For example, Rajan discloses that "the buffer chip may have four 512 Mb DRAM chips with which it emulates a single 2 Gb DRAM chip. The system will present fifteen row address bits, from which the buffer chip may use the fourteen low order bits (or, optionally, some other set of fourteen bits) to directly address the DRAM chips. The system will present three bank address bits, from which the buffer chip may use the two low order bits (or, optionally, some other set of two bits) to directly address the DRAM chips. During a row operation, the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals, and are stored for later reuse. And during a subsequent column operation, the stored bits are again used to generate the four DRAM chip select signals." Ex. 1015 at 7:4-21; *see also id*. at 7:22-67 (providing further examples of generating chip select signals from the received "*control/address signals*").

374. As also discussed above with reference to claim 2, the chip selection signals are "*data path control signals*" in the memory stack of Kim which uses the chip select signals to select the interconnect for the data transaction. *Supra* ¶¶273-280.

375. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

376. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein: . . . in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices*."

9. Claim 9 is Unpatentable

377. Claim 9 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

378. Claim 9 requires "*[t]he memory package of claim 1, wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address*."

379. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

380. Kim discloses to a Skilled Artisan that "*the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address*" for the reasons discussed above with reference to claim limitations [1.b] and [1.c] and claim 4. *Supra* ¶¶189-210 (claim limitation [1.b]), ¶¶211-229 (claim limitation [1.c]), ¶¶290-307 (claim 4).

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381. For example, Kim discloses to a Skilled Artisan that "*the control die* [is] *... configured to provide ... command/address signals to the ... array dies*" as discussed with reference to claim 4. *Supra* ¶¶290-307.

382. A Skilled Artisan would have also understood that Kim's control die includes "*command/address conduits*" for the same function. For example, Kim discloses that its control die buffers read and write command signals. *See* Ex. 1014 at [0032] ("In general, if command signals are applied from an external device, the command signals are buffered by a buffer which is provided in the semiconductor memory apparatus and may be utilized as internal signals."), [0038] ("While not shown in a drawing, … write and read command signals applied from a device external to the semiconductor memory apparatus 2 are buffered."). A Skilled Artisan would have understood from this disclosure that the command signals are transmitted from the buffer to the array dies through corresponding command conduits.

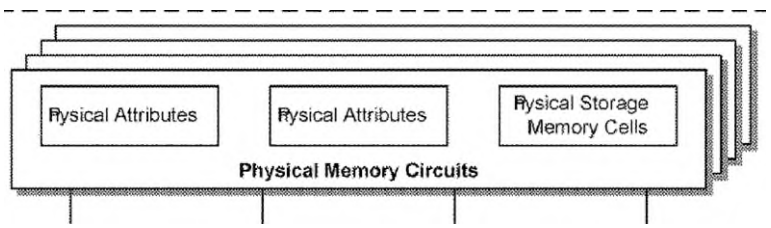
383. As discussed above with reference to claim limitations [1.b] and [1.c], a Skilled Artisan would have also understood that read and write commands include corresponding address signals "*including at least one memory cell address*." *Supra* ¶¶189-210 (claim limitation [1.b]), ¶¶211-229 (claim limitation [1.c]); *see also, e.g.*, Ex. 1019 (JESD79-3C) at p.13 ("Address Inputs: Provide the

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row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank.").

384. As further discussed with reference to claim limitations [1.b] and [1.c], it would have also been obvious to a Skilled Artisan in view of Rajan to include "*command/address conduits configured to provide corresponding command/address signals to the array dies*" in Kim's stack of memory devices. *Supra* ¶¶189-210 (claim limitation [1.b]), ¶¶211-229 (claim limitation [1.c]).

385. Rajan also discloses to a Skilled Artisan that "*the command/address signals include[] at least one memory cell address.*" *Supra* ¶¶189-210 (claim limitation [1.b]), ¶¶211-229 (claim limitation [1.c]). For example, Rajan discloses that "the individual DRAM chips in the stack may require only fourteen row address bits and three bank address bits for a row operation, and eleven column address bits and three bank address bits during a column operation." Ex. 1015 at 6:46-49; s*ee also id.* at Fig. 18 (reproduced below in part, showing that Physical Memory Circuits include Physical Storage Memory Cells).



386. Therefore, Kim and Rajan disclose and render obvious this limitation to a Skilled Artisan.

387. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address*" limitation.

10. Claim 10 is Unpatentable

388. Claim 10 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

389. Claim 10 requires "*[t]he memory package of claim 1, wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies*."

390. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

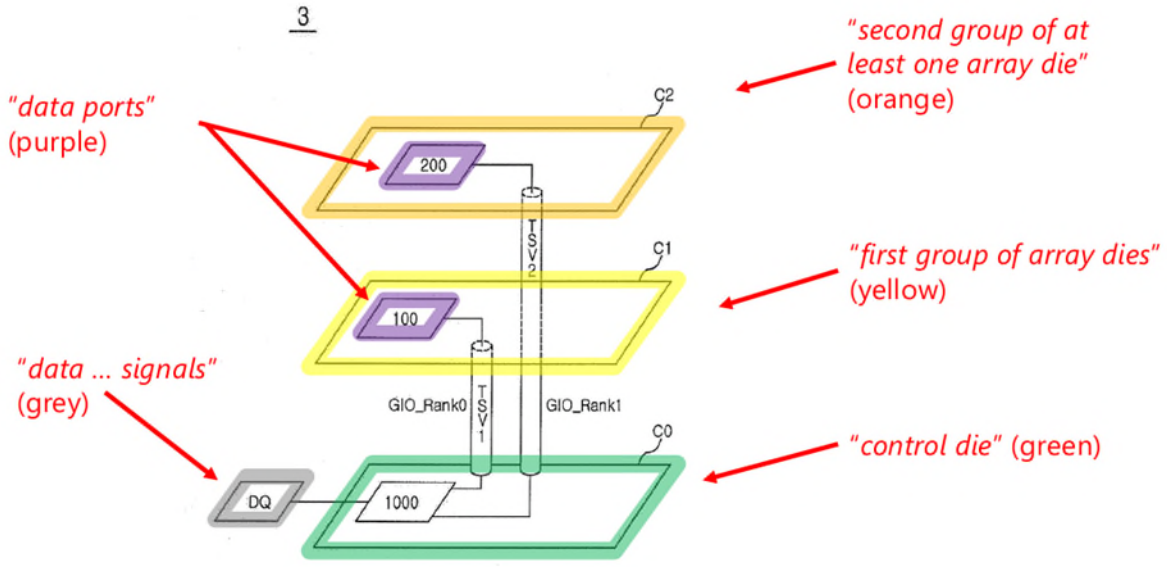
391. Kim discloses to a Skilled Artisan that "*the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies*" to provide power for the operation of the memory chips, including read and write operations.

392. For example, Kim discloses that the "first input/output driving section 100 [in chip C1] stores data transmitted through the first data input/output line

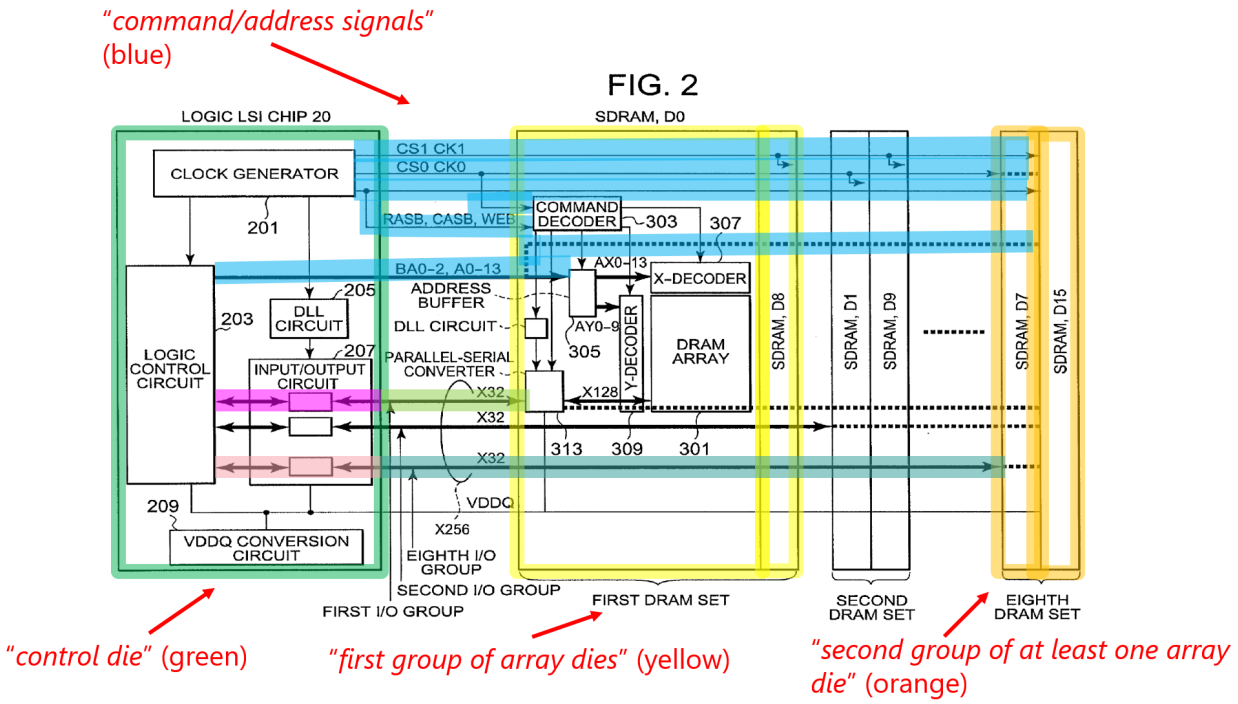
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GIO_Rank0 in a memory bank of a first rank Rank0 during a write operation, amplifies data stored in the memory bank of the first rank Rank0 and outputs the amplified data to the first data input/output line GIO_Rank0 during a read operation." Ex. 1014 at [0026]. Likewise, the "second input/output driving section 200 [in chip C2] stores data transmitted through the second data input/output line GIO_Rank1 in a memory bank of a second rank Rank1 during a write operation and amplifies data stored in the memory bank of the second rank Rank1 and outputs the amplified data to the second data input/output line GIO_Rank1 during a read operation." *Id.*; *see also id.* at Fig. 5 (reproduced below, annotated, showing first and second input/output driving sections 100 and 200 in stacked chips C1 and C2, respectively).

FIG.5



393. A Skilled Artisan would have understood from Kim's disclosure that each of the chips C1 and C2 receives power from the main chip C0, including a supply voltage and ground, and uses that power to perform the operations of storing, amplifying, and transmitting data. This Skilled Artisan's understanding is evidenced by Riho, which describes that "logic LSI chip 20 shown in FIG. 2 comprises … a VDDQ conversion circuit 209. From the VDDQ conversion circuit 209, a memory-driving main power supply voltage VDDQ is applied not only to the input/output circuit 207 and the logic control circuit 203 of the logic LSI chip 20, but also to the SDRAMs D0 to D15 stacked on the logic LSI chip 20." Ex. 1016 at [0036], Fig. 2 (reproduced below, annotated).



394. A Skilled Artisan would have also understood that applying a supply voltage, such as VDDQ, includes providing a corresponding ground signal to close the electric circuit. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.14 (listing supply voltages and corresponding grounds for SDRAMs).

395. Therefore, Kim discloses and renders obvious this limitation to a Skilled Artisan.

396. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies*" limitation.

11. Claim 11 is Unpatentable

397. Claim 11 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [11.a] Preamble

398. Claim 11 requires "*[a] memory package comprising*."

399. As shown in the table below, the preamble of claim 11 is identical to the preamble claim 1:

Claim 1	**Claim 11**
[1.a] A memory package comprising:	[11.a] A memory package comprising:

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400. As discussed above with reference to claim limitation [1.a], to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 1, 2, and 3 satisfy "*[a] memory package comprising*." *Supra* ¶¶184-188.

b) [11.b] Input/Output Terminals

401. Claim 11 requires "*[a] plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

402. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

403. As shown in the table below, claim limitation [11.b] is identical to claim limitation [1.b]:

Claim 1	**Claim 11**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[11.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;

404. As discussed above with reference to claim limitation [1.b], the prior art references in each of Grounds 1, 2, and 3 satisfy "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*." *Supra* ¶¶189-210.

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c) [11.c] Array Dies Arranged in a Stack

405. Claim 11 requires "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*."

406. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

407. As shown in the table below, claim limitation [11.c] is very similar to claim limitation [1.c]:

Claim 1	**Claim 11**
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, . . .;	[11.c] a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

408. As discussed above with reference to claim limitation [1.c], the prior art references in each of Grounds 1, 2, and 3 satisfy "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶211-229.

d) [11.d.1] and [11.d.1] Die Interconnects in Electrical Communication with the Array Dies

409. Claim 11 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical*

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communication with the second group of at least one array die and not in electrical communication with the first group of array dies."

410. The prior art references in Grounds 1-3 teach these limitations to a Skilled Artisan.

411. As shown in the table below, claim limitation [11.d.1] is identical to claim limitation [1.d.1], and claim limitation [11.d.2] is identical to claim limitation [1.d.2]:

Claim 1	**Claim 11**
[1.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,	[11.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
[1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[11.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

412. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in each of Grounds 1, 2, and 3 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in*

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electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die," and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶230-239.

e) Control Die

(1) [11.e.1] A Control Die Comprising

413. Claim 11 requires "*a control die comprising*."

414. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

415. As shown in the table below, claim limitation [11.e.1] is identical to claim limitation [1.e.1]:

Claim 1	**Claim 11**
[1.e.1] a control die comprising	[11.e.1] a control die comprising

416. As discussed above with reference to claim limitation [1.e.1], the prior art references in each of Grounds 1, 2, and 3 satisfy "*a control die comprising*." *Supra* ¶¶240-247.

(2) [11.e.2] and [11.e.3] First and Second Data Conduit

417. Claim 11 requires "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at*

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least a second data conduit between the second die interconnect and the first terminal, *and chip select conduits for providing chip select signals to respective array dies*."

418. The prior art references in Grounds 1-3 teach these limitations to a Skilled Artisan.

419. As shown in the table below, claim limitations [11.e.2] and [11.e.3] are nearly identical to claim limitations [1.e.2] and [1.e.3]:

Claim 1	**Claim 11**
[1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] at least a second data conduit between the second die interconnect and the first terminal, . . .	[11.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [11.e.3] at least a second data conduit between the second die interconnect and the first terminal, . . .

420. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in each of Grounds 1, 2, and 3 satisfy "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at least a second data conduit between the second die interconnect and the first terminal*." *Supra* ¶¶248-264. Furthermore, as discussed below with reference to claim element [15.a], a Skilled Artisan would have understood and it would have been obvious to her that each of

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the first and second data conduits can include a respective driver. *Infra* at ¶¶456-464.

(3) [11.e.4] Chip Select Conduits

421. Claim 11 requires "*chip select conduits for providing chip select signals to respective array dies*."

422. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

423. As shown in the table below, claim limitation [11.e.4] is very similar to claim limitations [6.a] and [6.b]:

Claim 6	**Claim 11**
[6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[11.e.4] chip select conduits for providing chip select signals to respective array dies;

424. As discussed above with reference to claim limitation [6.a] and [6.b], the prior art references in each of Grounds 1, 2, and 3 satisfy "*chip select conduits for providing chip select signals to respective array dies*." *Supra* ¶¶315-323 (claim limitation [6.a]), ¶¶324-334 (claim limitation [6.b]).

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(4) [11.e.5] Control Circuit

425. Claim 11 requires "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*."

426. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

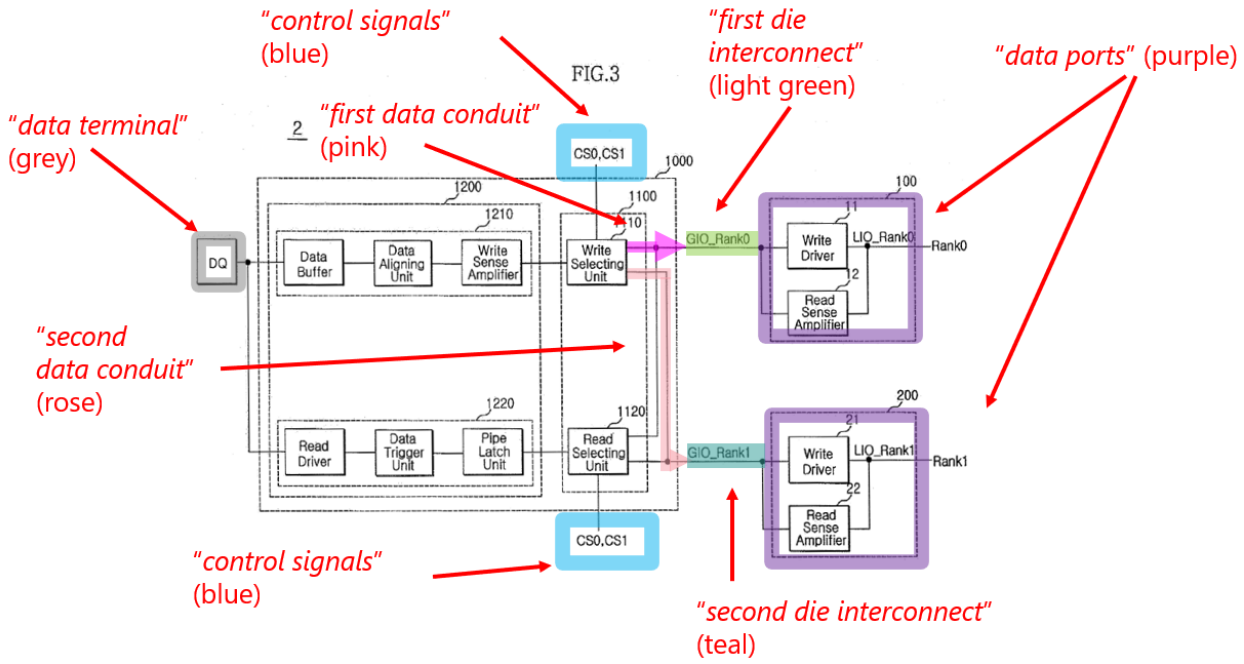
427. As shown in the table below, claim limitation [11.e.5] is very similar to claim limitation [1.e.4]:

Claim 1	**Claim 11**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.	[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

428. As discussed above with reference to claim limitation [1.e.4], the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.*" *Supra* ¶¶265-272.

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429. With respect to the "*driv[ing] a data signal to an array die selected by at least one of the chip-select signals*," Kim discloses, for example, that the "rank selecting unit 1100 includes a write selecting unit 1110 and a read selecting unit 1120. The write selecting unit 1110 is activated during the write operation and is connected to one of the first and second data input/output lines GIO_Rank0 and GIO_Rank1 in response to the chip selection signals CS0 and CS1." Ex. 1014 at [0035], Fig. 3 (reproduced below, annotated).



430. Kim also discloses that "data input/output unit 1200 may include a data input part 1210 … [which] may be activated during the write operation of the semiconductor memory apparatus 2 and … may comprise a data buffer, a data aligning unit and a write sense amplifier." *Id*. at [0040].

431. A Skilled Artisan would have understood from Kim's disclosure that a data signal is driven by data input part 1210, through write selecting unit 1110, to an array die in Rank0 or Rank1, as selected by the chip select signals. To the extent one might argue that this claim requires a separate driver for each of the first and second data conduits (pink and rose, respectively), it would have been obvious for the reasons discussed below with reference to claim element [15.a]. *Infra* at ¶¶455-464.

432. Furthermore, in the combination of Kim and Rajan, the "*control circuit*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices on the memory module. *Supra* at ¶¶138-140, 150-168.

433. Therefore, Kim discloses and in light of Rajan renders obvious this limitation to a Skilled Artisan

434. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*."

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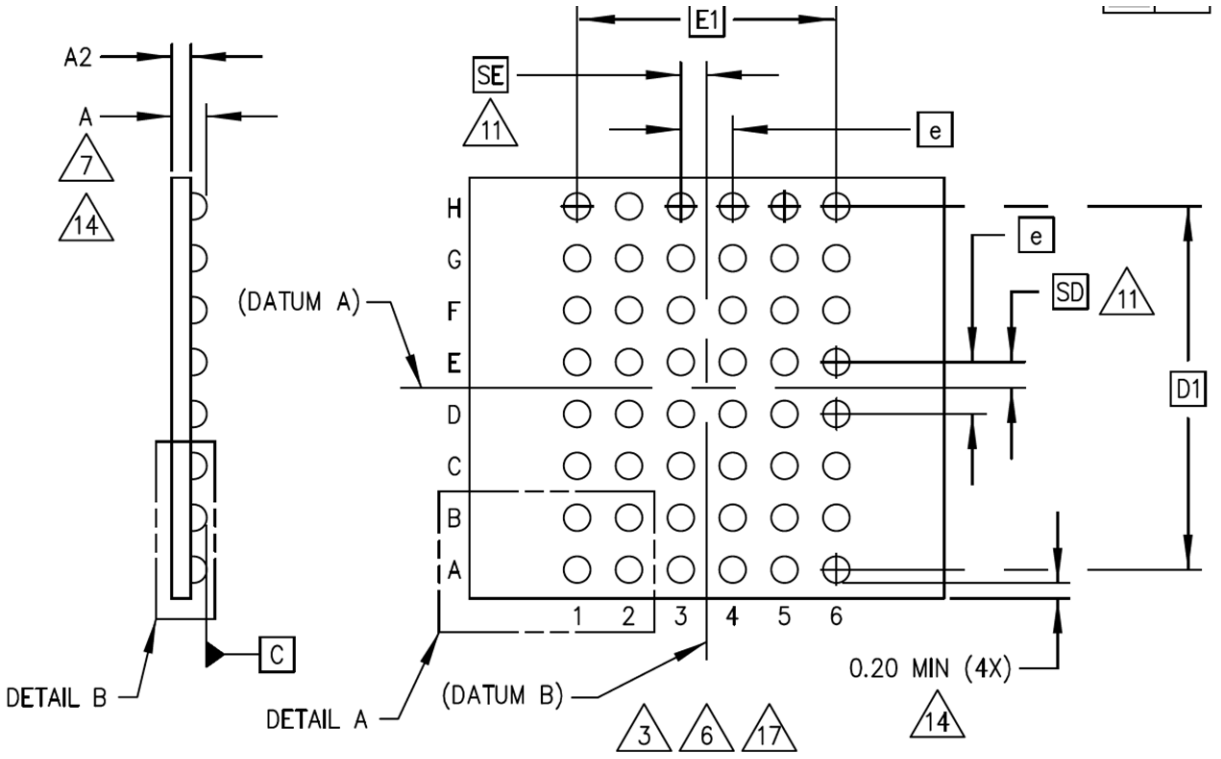
12. Claim 12 is Unpatentable

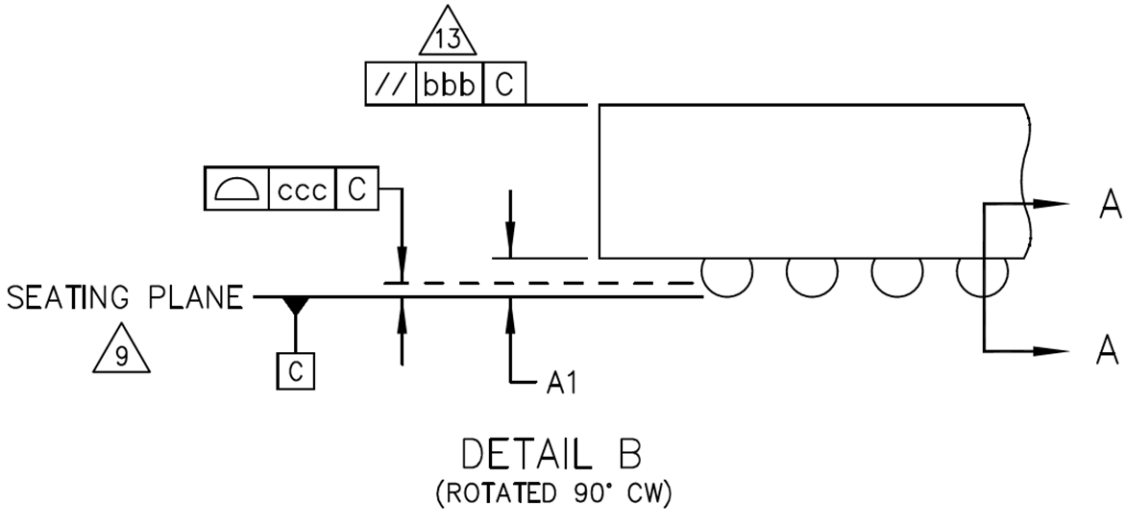
435. Claim 12 requires "*[t]he memory package of claim 11, wherein the chip select conduits pass through the control die*."

436. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

437. For example, the combination of Kim and Rajan renders obvious that "*the chip select conduits pass through the control die*." As discussed above, the combination of Kim and Rajan renders obvious to use terminals for chip select signals in the memory package of Kim. *Supra* at ¶¶150-168. Rajan also discloses that the interface may comply with JEDEC standards. Ex. 1015 at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for chip select signals at the bottom. *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.6-11. In particular, the standard describes a MO-207 package with solder balls at the bottom, including solder balls for chip select signals. *Id.*; *see also* Ex. 1021 (JEDEC MO-207 "Ball Grid Array" standard) at pp.1-2 (reproduced below in part); Ex. 1022 at 374 ("As DRAM device data rates increase to multiple hundreds of megabits per second, *Ball Grid*

Array (BGA) packages are needed to better control signal interconnects at the package level."), 476 ("*Fine Ball Grid Array* (FBGA) package … is required for the higher data rate DDR2 devices…").





DETAIL B
(ROTATED 90° CW)

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438. Therefore, a Skilled Artisan would have been motivated to use the standard chip select terminals at the bottom of Kim's memory package in accordance with the JEDEC standards to allow Kim's memory package to be used in standard JEDEC memory systems. In such an arrangement, a Skilled Artisan would have also been motivated to have the "*chip select conduits pass through the control die*," because the chip select signals are received at the bottom of the control die and are used to control the memory chips stacked at the top of control die. *See, e.g.*, Ex. 1014 at Figs. 3, 5. Indeed, as the 060 Patent admits, the command signals (including chip select signals) passing through the control die was disclosed by the prior-art JEDEC 3DS-DIMM proposal. Ex. 1001 at 19:55-56 ("the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720").

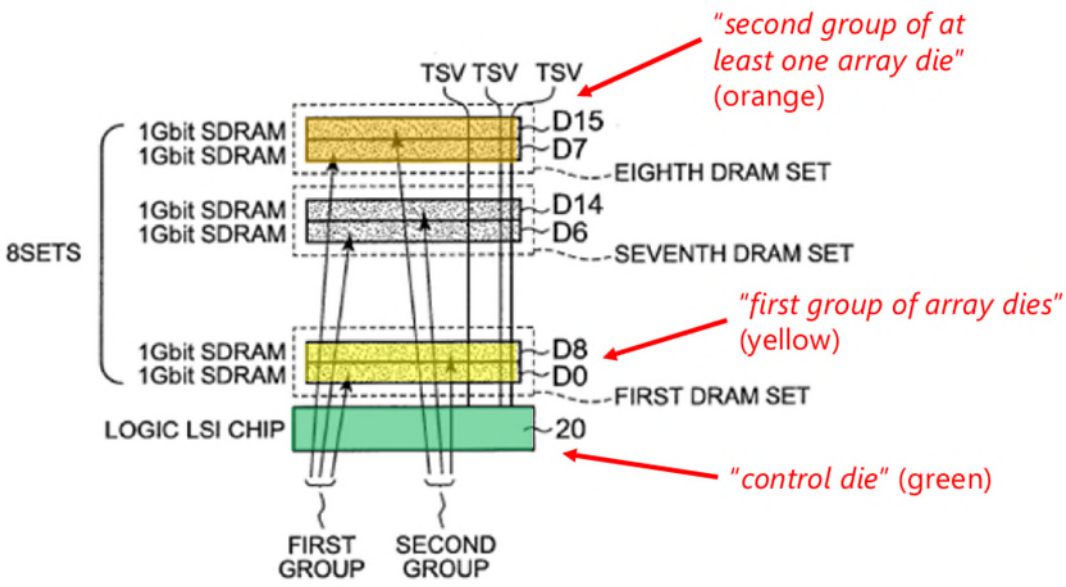
439. The combination of Kim and Riho also discloses that "*the chip select conduits pass through the control die*."

440. For example, Kim discloses receiving chip select signals from external devices. Ex. 1014 at [0032] ("The chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2 and buffered."). Riho discloses that "external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The

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external terminals are connected to the logic LSI chip 20. I/O signal lines penetrating through the controlled chips [e.g., SDRAMs D0-D8, D7-D15], which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the external terminals." Ex. 1016 at [0026], Fig. 1 (reproduced below, annotated).

FIG. 1



441. A Skilled Artisan would have understood from this disclosure that, in the combination, "*the chip select conduits pass through the control die*" because they are connecting the external chip select terminal at the lower side of the control chip to the SDRAMs coupled to the upper side of the control.

442. Therefore, Kim and Riho render obvious this limitation to a Skilled Artisan.

443. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*memory package of claim 11, wherein the chip select conduits pass through the control die*" limitation.

13. Claim 13 is Unpatentable

444. Claim 13 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

445. Claim 13 requires "*[t]he memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies*."

446. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

447. As discussed above, a Skilled Artisan would have understood that driving signals, including chip select signals, off-chip typically requires drivers. *Supra* at ¶¶135-137; *see e.g.*, Ex. 1030 at 135-136 ("In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices. Buffers can handle relatively large amounts of current flow because they are built with large transistors"). For example, Kim discloses that the "chip selection signals CS0 and CS1 are signals that may be generated as command signals applied from a device external to the semiconductor memory apparatus 2 and buffered." Ex. 1014 at [0032]. A Skilled

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Artisan would have understood from this disclosure that the chip select signals "buffered" on the control die (main chip) are driven to the array dies (slave chips) by drivers. *See, e.g.*, Ex. 1030 at 135 ("In circuits in which a logic gate has to drive a large capacitive load, buffers are often used to improve performance … Buffers can be created with different amounts of drive capability, depending on the sizes of the transistor"); Ex. 1038 (Stone) at p.68 ("The drivers commonly used for bus systems are tri-state drivers that have a low, high, and off (or high impedance) mode of operation."); Ex. 1017 (Wyman) at 1:14-20 ("Chips contain pads through which a signal can be driven off-chip to pins of another board and/or chip[.] The driver circuit must be designed with a predetermined output within a given tolerance range. This predetermined singular amplified drive signal must be sufficient to chive [sic: drive] the output signal the required distance accounting for such impediments as available real estate, heat, resistance, capacitance and impedance."). As discussed above with reference to claim 6, the buffered chip select signals are driven to the respective array dies by respective drivers. *Supra* ¶¶314-334; *see also* Ex. 1016 (Riho) at [0037] ("The clock generator 201 supplies a first clock signal CS0CK0 to the SDRAMs D0 to D7 (which belong to first controlled chips) forming a first group (chip selection group) and further supplies a second clock signal CS1CK1 to the SDRAMs D8 to D15 (which belong to second controlled chips) forming a second group (chip selection group).").

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448. Therefore, Kim alone and in combination with Rajan discloses and renders obvious this limitation to a Skilled Artisan.

449. Accordingly, the prior art references in each of Grounds 1, 2, and 3 satisfy the "*memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies*" limitation.

14. Claim 14 is Unpatentable

450. Claim 14 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

451. Claim 14 requires "*[t]he memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias*."

452. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

453. As shown in the table below, claim 14 is very similar to claim 5:

Claim 5	**Claim 14**
[5] The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.	[14] The memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.

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454. As discussed above with reference to claim 5, the prior art references in each of Grounds 1, 2, and 3 satisfy "*wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.*" *Supra* ¶¶308-313.

15. Claim 15 is Unpatentable

455. Claim 15 is unpatentable as the prior art references in Ground 3 render the claim obvious.

a) [15.a] First and Second Data Conduit and First and Second Driver

456. Claim 15 requires "*[t]he memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size*."

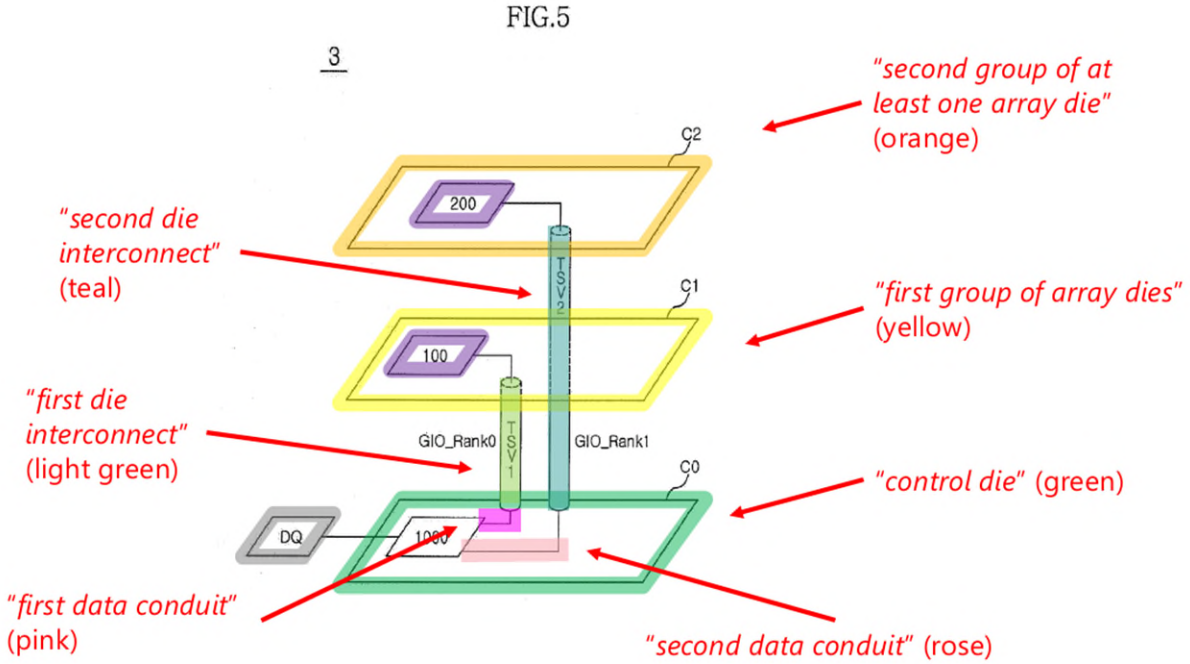
457. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

458. Kim in combination with Wyman renders obvious that "*the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size*."

459. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], Kim discloses the claimed "*first data conduit*" (annotated pink below) to

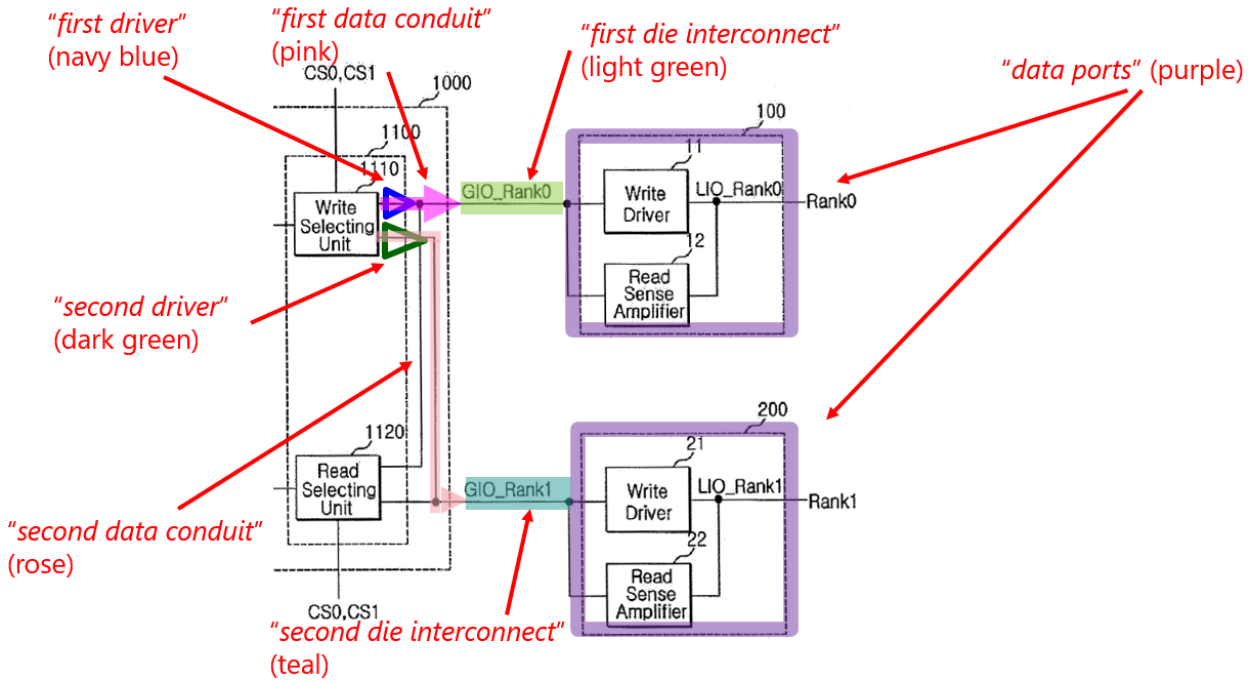
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TSV1 and the "*second data conduit*" (annotated rose below) to TSV2. *Supra* ¶¶248-264; *see, e.g.*, Ex. 1014 at Fig. 5 (reproduced below, annotated).



460. As expressly shown in this figure of Kim, TSV1 coupled to the "*first data conduit*" (pink) is shorter than TSV2 coupled to the "*second data conduit*" (rose). A Skilled Artisan would have understood that, due to this difference in length of TSV1 and TSV2, each of the "*first data conduit*" and the "*second data conduit*" can include a respective driver that is optimized for driving the data signal through the corresponding TSV in an efficient way. For example, Wyman explains that "[i]n instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required." Ex. 1017 at 1:22-24. Therefore, a Skilled Artisan would have been motivated to follow the teaching of Wyman in the system of Kim

and avoid using full capacity drivers, thus saving power and not being "wasteful and inefficient." *Id*. Such an arrangement of having separate drivers (e.g., a "*first driver*," navy blue below, and a "*second driver*, dark green below) for each data conduit is illustrated in annotated (partial) Fig. 3 of Kim, reproduced below. *See* Ex. 1014 at Fig. 3 (reproduced below, in part, annotated).



461. As discussed above, a Skilled Artisan would have understood and been motivated to turn to analogous art like Wyman to implement the stacked devices of Kim with efficient driving signals between the stacks. *Supra* ¶¶174-181. For example, Wyman discloses that longer connections in a stacked arrangement require larger driving force. Ex. 1017 at Figs. 7, 8 (reproduced below).

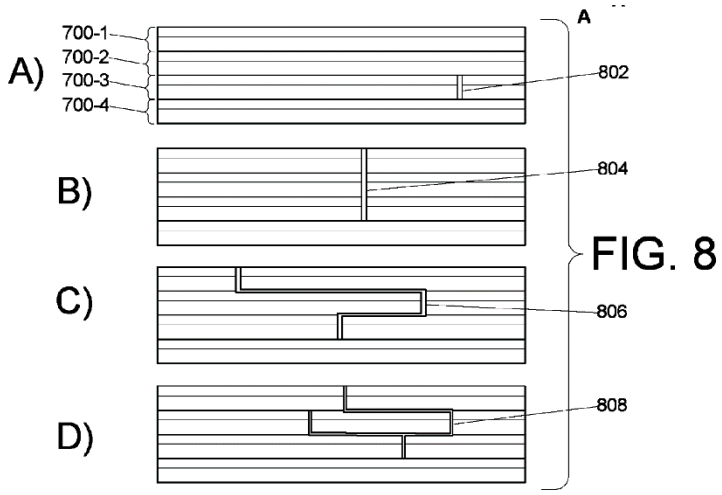


FIG. 8

Wyman explains that "FIG. 8A illustrates, in simplified form, a through-chip via connection (802) extending between the mother chip (700-4) and daughter 1 (700-3) … requir[ing] minimal drive … FIG. 8B illustrates, in simplified form, a longer through-chip via connection (804) extending directly between the mother chip (700-4) and daughter 3 (700-1) in a straight line. The increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A. …" *Id*. at 6:15-30. However, Wyman recognizes that even with the "significantly longer connection (808) between the mother chip (700-4) with a fan out to both daughter 2 (700-2) and daughter 3 (7001)," as shown in Fig. 8.D, using "the total drive … would be overkill." *Id*. at 6:44-50.

462. A Skilled Artisan would have understood from this disclosure that the longer the connection in a stack of chips, the more drive it requires, but using the "total drive" would be wasteful. Ex. 1017 at 1:22-24 ("In instances where chips are

stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."). Therefore, a Skilled Artisan would have been motivated to use drivers of different strengths (i.e., a "*first driver*" having a "*first driver size*" and a "*second driver*" having a "*second driver size*") for Kim's different sized through-silicon vias TSV1 and TSV2. As discussed above, a Skilled Artisan would have been motivated to drive the shorter TSV1 with a smaller driver and the longer TSV2 with a larger driver to use power in an efficient manner as taught by Wyman. *Supra* ¶¶174-181; *see also* annotated partial Fig. 3 of Kim above. Making such a combination was well within the level of skill, since Wyman itself teaches drivers of different strengths, and the combination would have provided nothing more than expected: a power efficient drive of signals through Kim's TSVs.

463. Therefore, the combination of Kim and Wyman renders obvious this limitation to a Skilled Artisan.

464. Accordingly, the prior art references in Ground 3 satisfy the "*the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size*" limitation.

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b) [15.b] First and Second Driver Size Less Than Driver Size Sufficient to Drive Signal

465. Claim 15 requires "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*."

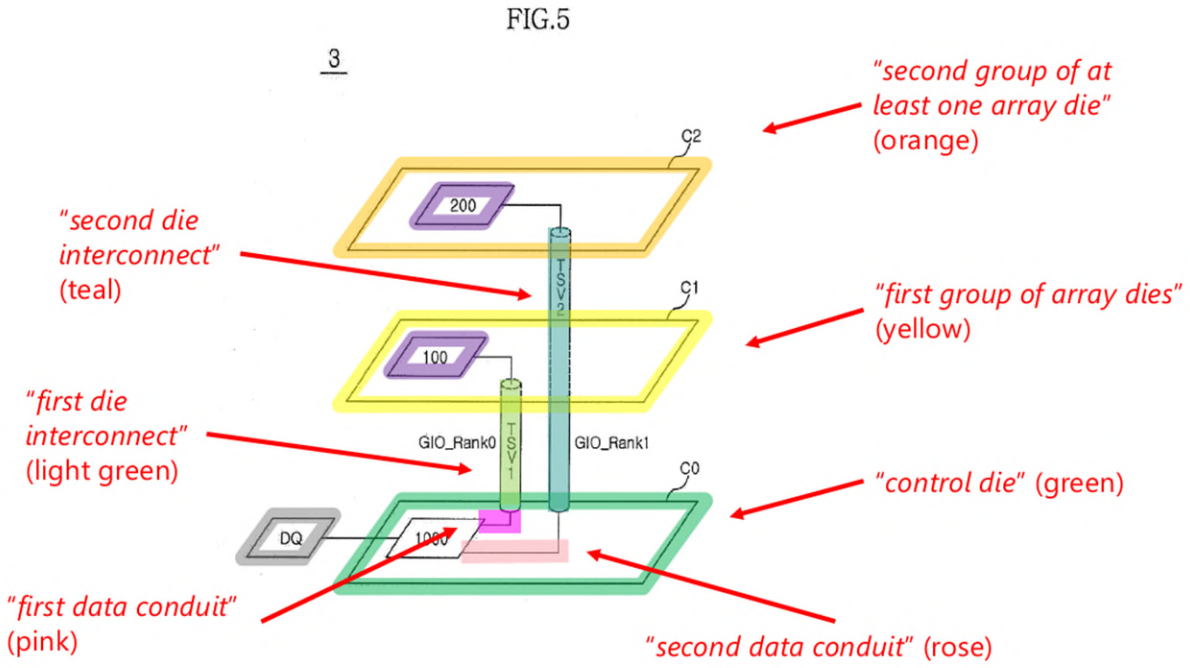
466. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

467. Kim in combination with Wyman renders obvious to a Skilled Artisan that "*the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.*"

468. For example, Wyman discloses to a Skilled Artisan that using a driver strength that is "overkill" is "wasteful and inefficient since far less power is required." Ex. 1017 at 6:47-50, 1:22-24. Therefore, for the reasons discussed above with reference to claim limitation [15.a], a Skilled Artisan would have been motivated to use a "*driver size*" that is required for efficient signal communication, but that would not produce a drive that is "overkill." *Supra* ¶¶456-464.

469. A Skilled Artisan would have also understood that the "*driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*" in

Kim's stacked system is larger than the "*driver size*" that is required for efficient signal communication through TSV1 and TSV2. *Supra,* ¶¶135-137. Indeed, each of TSV1 and TSV2 are coupled to circuitry in some, but not all, of the slave chips in the stack, thus requiring less strength than driving circuitry in all the slave chips. *See* Ex. 1014 at Fig. 5 (reproduced below, annotated).



Furthermore, Wyman explains that the "reduced path distances of stacked hybridized chips therefore require less drive to adequately drive a signal to an off-chip board and/or chip." Ex. 1017 (Wyman) at 1:45-47; *see also id*. at 6:57-60 ("By using the above approach, a designer could assess the amount of drive needed for to adequately supply the signal to the devices (902, 904, 906) as needed while using less than the total drive a drive circuit of the prior art might supply.").

470. Therefore, the combination of Kim and Wyman renders obvious this limitation to a Skilled Artisan.

471. Accordingly, the prior art references in Ground 3 satisfy the "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*" limitation.

16. Claim 16 is Unpatentable

472. Claim 16 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

473. Claim 16 requires "*[t]he memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals*."

474. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

475. As shown in the table below, claim 16 is very similar to claim limitations [1.e.4] and [8.b.3]:

Claims 1, 8	**Claim 16**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [8.b.3] in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.	[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.

476. As discussed above with reference to claim limitations [1.e.4] and [8.b.3], the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.*" *Supra* ¶¶265-272 (claim limitation [1.e.4]), 370-376 (claim limitation [8.b.3].

477. For example, as discussed above with reference to claim limitation [8.b.3], the combination of Kim and Rajan discloses that "*the chip select signal is generated using an address signal in the control/address signals*." *Supra* ¶¶138-140, 370-376; *see, e.g.*, Ex. 1015 at 7:4-21 ("As another example, the buffer chip may have four 512 Mb DRAM chips with which it emulates a single 2 Gb DRAM

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chip. The system will present fifteen row address bits, from which the buffer chip may use the fourteen low order bits (or, optionally, some other set of fourteen bits) to directly address the DRAM chips. The system will present three bank address bits, from which the buffer chip may use the two low order bits (or, optionally, some other set of two bits) to directly address the DRAM chips. During a row operation, the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals, and are stored for later reuse. And during a subsequent column operation, the stored bits are again used to generate the four DRAM chip select signals.").

478. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy the "*wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals*" limitation.

17. Claim 17 is Unpatentable

479. Claim 17 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

480. Claim 17 requires "*[t]he memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the*

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second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals."

481. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

482. As shown in the table below, claim 17 is very similar to claim limitations [1.e.4], [4.a], and [4.b]:

Claims 1, 4	**Claim 17**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[17] The memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.

483. As discussed above with reference to claim limitations [1.e.4], [4.a], and [4.b], the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals*

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received via second terminals of the plurality of terminals." *Supra* ¶¶265-272 (claim limitation [1.e.4]), ¶¶290-307 (claim 4).

18. Claim 18 is Unpatentable

484. Claim 18 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

485. Claim 18 requires "*[t]he memory package of claim 16, wherein the control/ address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal.*"

486. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

487. As shown in the table below, claim 18 is very similar to claim 2 and claim limitations [4.a] and [4.b]:

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Claims 2, 4	**Claim 18**
[2] The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[18] The memory package of claim 16, wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal.

488. As discussed above with reference to claims 2 and claim limitations [4.a] and [4.b], the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal*." *Supra* ¶¶273-280 (claim 2), ¶¶290-307 (claim limitations [4.a] and [4.b]); *see also* Ex. 1001 (the 060 Patent) at 15:48-67 (describing read/write command signals, including chip select signals controlling the data path).

19. Claim 19 is Unpatentable

489. Claim 19 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [19.a] Generate Data Path Control Signals

490. Claim 19 requires "*[t]he memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals*."

491. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

492. As shown in the table below, claim limitation [19.a] is very similar to claim 3 and claim limitations [1.e.4], [4.a], and [8.b.3]:

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Claims 1, 3-4, 8	**Claim 19**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [8.b.3] in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.	[19.a] The memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and

493. As discussed above with reference to claim 3 and claim limitations [1.e.4], [4.a], and [8.b.3], the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of*

terminals." *Supra* ¶¶265-272 (claim limitation [1.e.4]), ¶¶281-289 (claim 3), ¶¶291-295 (claim limitation [4.a]), ¶¶370-376 (claim limitation [8.b.3]).

b) [19.b] Control Circuit Controls Respective States of First Data Conduit

494. Claim 19 further requires "*wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals*."

495. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

496. As shown in the table below, claim limitation [19.b] is very similar to claim limitation [1.e.4] and claim 3:

Claims 1, 3	**Claim 19**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[19.b] wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.

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497. As discussed above with reference to claim limitation [1.e.4] and claim 3, the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.*" *Supra* ¶¶265-272 (claim limitation [1.e.4]), ¶¶281-289 (claim 3).

20. Claim 20 is Unpatentable

498. Claim 20 is unpatentable as the prior art references in Ground 3 render the claim obvious.

a) [20.a] Preamble

499. The preamble of claim 20 requires "*[a] method for optimizing load in a memory package comprising*."

500. To the extent the preamble is limiting, the prior art references in Ground 3 teach this limitation to a Skilled Artisan.

501. As shown in the table below, claim limitation [20.a] is very similar to claim limitation [1.a]:

Claim 1	**Claim 20**
[1.a] A memory package comprising:	[20.a] A method for optimizing load in a memory package comprising

502. As discussed above with reference to claim limitation [1.a], the prior art references in Ground 3 satisfy "*[a] memory package*," *supra* ¶¶184-188, and the specific steps for "*optimizing [the] load*" are discussed in the limitations below.

b) [20.b] Method Comprising

(1) [20.b.1] Array Dies Arranged in a Stack

503. Claim 20 requires "*a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die*."

504. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

505. As shown in the table below, claim limitation [20.b.1] is very similar to claim limitation [1.c]:

Claim 1	**Claim 20**
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, ...;	[20.b.1] a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die;

506. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 3 satisfy the "*a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die*" limitation. *Supra* ¶¶211-229.

(2) [20.b.2] Die Interconnects

507. Claim 20 requires "*at least a first die interconnect and a second die interconnect*."

508. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

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509. As shown in the table below, claim limitation [20.b.2] is very similar to claim limitations [1.d.1]-[1.d.2]:

Claim 1	**Claim 20**
[1.d.1] - [1.d.2] at least a first die interconnect and a second die interconnect, …;	[20.b.2] at least a first die interconnect and a second die interconnect,

510. As discussed above with reference to claim limitations [1.d.1]-[1.d.2], the prior art references in Ground 3 satisfy "*at least a first die interconnect and a second die interconnect*." *Supra* ¶¶230-239.

(3) [20.b.3] Control Die

511. Claim 20 requires "*a control die*."

512. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

513. As shown in the table below, claim limitation [20.b.3] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 20**
[1.e.1] a control die comprising	[20.b.3] a control die, and

514. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 3 satisfy "*a control die*." *Supra* ¶¶240-247.

(4) [20.b.4] Input/Output Terminals

515. Claim 20 requires "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

516. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

517. As shown in the table below, claim limitation [20.b.4] is identical to claim limitation [1.b]:

Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[20.b.4] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices,

518. As discussed above with reference to claim limitation [1.b], the prior art references in Ground 3 satisfy "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*." *Supra* ¶¶189-210.

c) [20.c] Method Further Comprising

519. Claim 20 requires "*the method comprising*."

520. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

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521. As shown in the table below, claim limitation [20.c] is very similar to claim limitation [20.a]:

Claim 20	**Claim 20**
[20.a] A method for optimizing load in a memory package comprising	[20.c] the method comprising:

522. As discussed above with reference to claim limitation [20.a], prior art references in Ground 3 satisfy "*the method comprising*." *Supra* ¶¶499-502.

d) [20.d] Signals

(1) [20.d.1] Receiving a Data Signal at a First Terminal

523. Claim 20 requires "*receiving a data signal at a first terminal of the plurality of input/output terminals*."

524. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

525. As shown in the table below, claim limitation [20.d.1] is very similar to claim limitation [1.b], [1.e.2], and [1.e.3]:

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Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices; [1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,	[20.d.1] receiving a data signal at a first terminal of the plurality of input/output terminals;

526. As discussed above with reference to claim limitation [1.b], [1.e.2], and [1.e.3], the prior art references in Ground 3 satisfy "*receiving a data signal at a first terminal of the plurality of input/output terminals*." *Supra* ¶¶189-210, ¶¶248-264.

(2) [20.d.2] Receiving Control Signals at Second Terminals

527. Claim 20 requires "*receiving control signals at second terminals of the plurality of input/output terminals*."

528. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

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529. As shown in the table below, claim limitation [20.d.2] is very similar to claim limitation [1.b] and [1.e.4]:

Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices; [1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.	[20.d.2] receiving control signals at second terminals of the plurality of input/output terminals;

530. As discussed above with reference to claim limitation [1.b] and [1.e.4], the prior art references in Ground 3 satisfy "*receiving control signals at second terminals of the plurality of input/output terminals*." *Supra* ¶¶189-210, 265-272.

(3) [20.d.3] Providing Chip Select Signals to Array Dies

531. Claim 20 requires "*providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and*."

532. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

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533. As shown in the table below, claim limitation [20.d.3] is very similar to claim limitations [4.a], [4.b], [6.a] and [6.b]:

Claims 4, 6	**Claim 20**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies. [6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[20.d.3] providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and

534. For the reasons discussed above with reference to claim limitations [4.a], [4.b], [6.a], and [6.b], the prior art references in Ground 3 satisfy "*providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals*." *Supra* ¶¶290-307, 314-334. For example, the chip select signals provided to the to the array dies are buffered or generated from the chip select signals received by the memory package. *Id*., *see also supra* at ¶¶138-141.

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(4) [20.d.4] Selecting Driver to Drive the Data Signal

535. Claim 20 requires "*selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals*."

536. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

537. As shown in the table below, claim limitation [20.d.4] is very similar to claim limitations [11.e.5] and [15.a]:

Claims 11 and 15	**Claim 20**
[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[20.d.4] selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals,

538. As discussed above with reference to claim limitations [11.e.5] and [15.a], the prior art references in Ground 3 satisfy "*selecting one of a first driver*

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and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals." *Supra* ¶¶425-434 (claim limitation [11.e.5]), ¶¶456-464 (claim limitation [15.a]).

e) [20.e.1] and [20.e.2] First and Second Die Interconnect

539. Claim 20 requires "*the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

540. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

541. As shown in the table below, claim limitations [20.e.1] and [20.e.2] are identical to claim limitations [1.d.1] and [1.d.2]:

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Claim 1	**Claim 20**
[1.d.1] the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[20.e.1] the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [20.e.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.

542. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 3 satisfy "*the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶230-239.

21. Claim 21 is Unpatentable

543. Claim 21 is unpatentable as the prior art references in Ground 3 render the claim obvious.

544. Claim 21 requires "*[t]he method of claim 20, further comprising selecting a first driver size for the first driver based, at least in part, on a load on*

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the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver."

545. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

546. As shown in the table below, claim 21 is very similar to claim limitation [15.a] and [15.b]:

Claim 15	**Claim 21**
[15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and [15.b] wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.	[21] The method of claim 20, further comprising: selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver.

547. For the reasons discussed above with reference to claim limitation [15.a] and [15.b], the combination of Kim and Wyman teaches that a driver size in a stacked arrangement is selected based on the load (including the length of the TSV). *Supra* ¶¶456-471; *see, e.g.,* Ex. 1017 (Wyman) at 7:13-18 ("The circuitry

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of FIG. 10, FIG. 11, those of the prior figures, as well as the myriad of circuit variants thereof that can be configured to operate in a similar manner, advantageously allows the output drive current to be modified to meet the requirements of a particular output load."); *see also supra* at ¶¶135-137. Therefore, the prior art references in Ground 3 satisfy the "*further comprising selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver*" limitation.

22. Claim 22 is Unpatentable

548. Claim 22 is unpatentable as the prior art references in Ground 3 render the claim obvious.

549. Claim 22 requires "*[t]he method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*."

550. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

551. As shown in the table below, claim 22 is very similar to claim limitation [15.b]:

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Claim 15	Claim 22
[15.b] wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.	[22] The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

552. As discussed above with reference to claim limitation [15.b], the prior art references in Ground 3 satisfy the "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*" limitation. *Supra* ¶¶465-471.

23. Claim 23 is Unpatentable

553. Claim 23 is unpatentable as the prior art references in Ground 3 render the claim obvious.

554. Claim 23 requires "*[t]he method of claim 20, further comprising generating the chip select signals from at least some of the control signals*."

555. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

556. As shown in the table below, claim 23 is very similar to claim 16:

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Claim 16	**Claim 23**
[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and	[23] The method of claim 20, further comprising generating the chip select signals from at least some of the control signals.

557. As discussed above with reference to claim 16, the prior art references in Ground 3 satisfy the "*further comprising generating the chip select signals from at least some of the control signals*" limitation. *Supra* ¶¶472-478.

24. Claim 24 is Unpatentable

558. Claim 24 is unpatentable as the prior art references in Ground 3 render the claim obvious.

559. Claim 24 requires "*[t]he method of claim 20, wherein the control signals include the chip-select signals*."

560. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

561. As shown in the table below, claim 24 is very similar to claim [4.a] and [4.b]:

Claim 4	**Claim 24**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[24] The method of claim 20, wherein the control signals include the chip-select signals.

562. As discussed above with reference to claim [4.a] and [4.b], the prior art references in Ground 3 satisfy "*wherein the control signals include the chip-select signals*." *Supra* ¶¶291-307. As further discussed above with reference to claim element [1.b], *supra* at ¶¶194-196, a Skilled Artisan would have understood that, according to the JEDEC standard, the signals indicating the "command" (e.g., read or write) include "CS#," i.e., the "*chip-select signal*." *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.13, 33.

25. Claim 25 is Unpatentable

563. Claim 25 is unpatentable as the prior art references in Ground 3 render the claim obvious.

564. Claim 25 requires "*[t]he method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias*."

565. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

566. As shown in the table below, claim 25 is very similar to claim 5:

Claim 5	**Claim 25**
[5] The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.	[25] The method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias.

567. As discussed above with reference to claim 5, the prior art references in Ground 3 satisfy this limitation. *Supra* ¶¶308-313.

26. Claim 26 is Unpatentable

568. Claim 26 is unpatentable as the prior art references in Ground 3 render the claim obvious.

569. Claim 26 requires "*[t]he method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die*."

570. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

571. As shown in the table below, claim 26 is very similar to claim 12:

Claim 12	**Claim 26**
[12] The memory package of claim 11, wherein the chip select conduits pass through the control die.	[26] The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die.

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572. As discussed above with reference to claim 12, the prior art references in Ground 3 satisfy this limitation. *Supra* ¶¶435-443.

573. Moreover, it was well known at the time to use through-silicon vias for passing signals through a die. *See*, *e.g.*, Ex. 1001 (the 060 Patent) at 1:49-2:7 and Figs. 1A and 1B (describing prior art using vias for chip select signals); Ex. 1014 at [0046] ("Recently, a through-silicon via (TSV) type semiconductor apparatus has been developed in which silicon vias are formed to pass through the plurality of stacked chips so that all of the chips are electrically connected to one another."); *see also* Ex. 1016 (Riho) at Fig. 1, [0030] (describing using TSVs for communicating data, address, and control signals, including chip select signals, in stacked die structure).

574. Therefore, it would have been obvious to a Skilled Artisan to use through-silicon vias in the control die so that "*the chip select conduits pass through the control die*" as discussed above with reference to claim 12. *Supra* ¶¶435-443.

575. Accordingly, the prior art references in Ground 3 satisfy "*[t]he method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die*."

27. Claim 27 is Unpatentable

576. Claim 27 is unpatentable as the prior art references in Ground 3 render the claim obvious.

a) [27.a] Generating Data Path Control Signals from Control Signals

577. Claim 27 requires "*[t]he method of claim 20, further comprising generating data path control signals from at least some of the control signals*."

578. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

579. As shown in the table below, claim limitation [27.a] is very similar to claim 3:

Claim 3	**Claim 27**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[27.a] The method of claim 20, further comprising generating data path control signals from at least some of the control signals,

580. As discussed above with reference to claim 3, the prior art references in Ground 3 satisfy this limitation. *Supra* ¶¶281-289.

b) [27.b] Data Path Control Signals Being Used to Select First and Second Driver

581. Claim 27 requires "*the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal*."

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582. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

583. As shown in the table below, claim limitation [27.b] is very similar to claim 3 and claim limitations [11.e.5] and [15.a]:

Claims 3, 11, 15	**Claim 27**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[27.b] the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal.

584. As discussed above with reference to claim 3 and claim limitations [11.e.5] and [15.a], the prior art references in Ground 3 satisfy "*the data path*

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control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal." *Supra* ¶¶281-289 (claim 3), ¶¶425-434 (claim limitation [11.e.5]), ¶¶456-464 (claim limitation [15.a]).

28. Claim 28 is Unpatentable

585. Claim 28 is unpatentable as the prior art references in Ground 3 render the claim obvious.

586. Claim 28 requires "*[t]he method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals*."

587. The prior art references in Ground 3 teach this limitation to a Skilled Artisan.

588. As shown in the table below, claim 28 is very similar to claim 3 and claim limitations [11.e.5] and [15.a]:

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Claims 3, 11 and 15	**Claim 28**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[28] The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals.

589. For the reasons discussed above with reference to claim [3] and claim limitations [11.e.5] and [15.a], the prior art references in Ground 3 satisfy "*wherein the one of the first driver and the second driver is selected using at least some of the control signals*." *Supra* ¶¶281-289 (claim 3), ¶¶425-434 (claim limitation [11.e.5]), ¶¶456-464(claim limitation [15.a]).

29. Claim 29 is Unpatentable

590. Claim 29 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

a) [29.a] Memory Module

591. The preamble of claim 29 requires "*[a] memory module operable via a memory control hub, comprising*."

592. To the extent the preamble is limiting, the prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

593. As discussed above, it would have been obvious to combine the teaching of Kim and Rajan. *Supra* ¶¶150-168. Rajan discloses a "*memory module*," such as a DIMM, that includes buffered memory device stacks. *See, e.g.*, Ex. 1015 at Fig. 8 (reproduced below), 8:52-54 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804….").

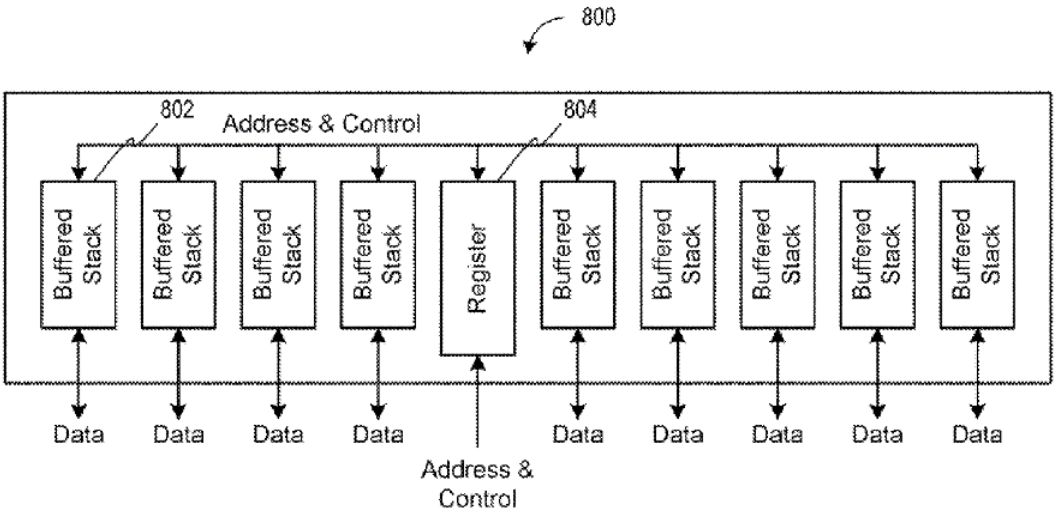


FIG. 8

594. Kim also discloses stacked memory devices. Ex. 1014 at [0050] ("It is to be understood that the shared data input/output section 1000 according to the embodiment of the present invention can be applied to a semiconductor memory apparatus in which a plurality of chips are stacked.").

595. Therefore, a Skilled Artisan would have understood, and been motivated, to implement Kim's stacked memory devices in a memory module as disclosed by Rajan. *See, e.g.*, Ex. 1015 (Rajan) at 1:28-32 ("In other systems, groups of memory chips are first coupled into memory modules, such as dual in-line memory modules (DIMMs), which are in turn coupled into a system by means of slots, sockets, or other connectors."), 15:3-12 ("The physical memory circuits employed in practicing this invention may be any type of memory whatsoever … The physical memory circuits may be coupled to any type of memory module…").

For example, a Skilled Artisan would have been motivated to implement Kim's stacked devices in a DIMM format so that it can be used in systems that include sockets for DIMMs.

596. Rajan further explains that its "system may include a memory controller (not shown) through which it accesses the memory circuits." Ex. 1015 (Rajan) at 3:5-7. A Skilled Artisan would have understood that Rajan's memory controller can include "*a memory control hub.*" *See, e.g.*, Ex. 1037 (Rothman) at Fig. 1, 1:34-39 ("FB-DIMMs can be connected via high speed serial interfaces to a Memory Controller Hub (MCH). The AMB communicates with the MCH via the high speed serial interfaces and with RAM ICs on the DIMM via the internal memory bus. The AMB reads from and writes to the RAM as instructed by the MCH and can also be used to configure the FB-DIMM."); Ex. 1022 at 315-20, Figure 7.2 (annotated below) ("Figure 7.2 illustrates [as of 2008] DRAM's place in a typical PC. An individual DRAM device typically connects indirectly to a CPU (i.e., a microprocessor) through a memory controller"), Figure 7.6 ("JEDEC style memory bus organization"). A POSITA would also know that the memory controller could be integrated into the CPU package (to the left in the figure below) rather than in a separate chip (as shown below); both were known options at the time.

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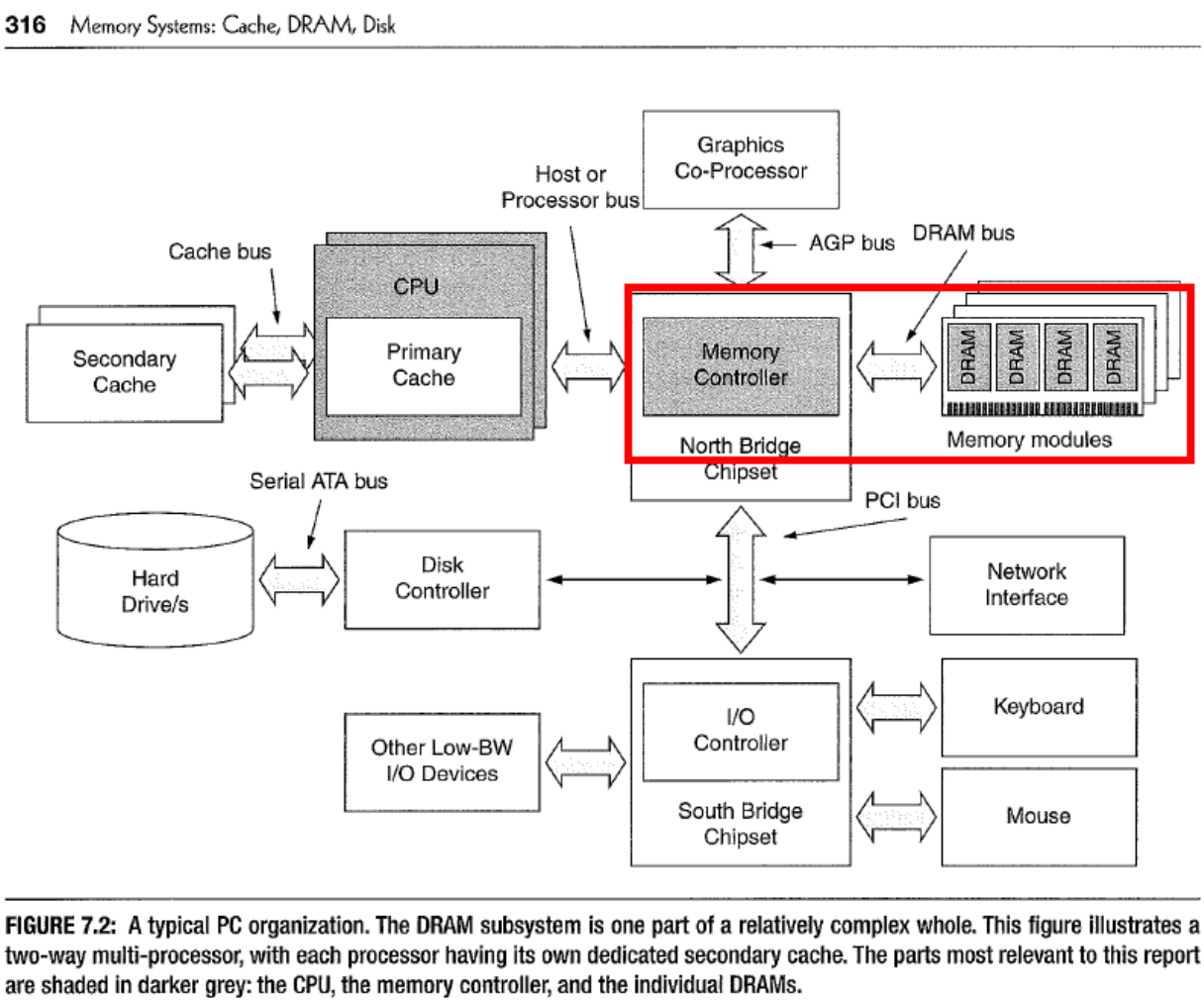


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

597. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

598. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*[a] memory module operable via a memory control hub, comprising*."

b) [29.b] Register Device

599. Claim 29 requires "*a register device configured to receive command/address signals from the memory control hub and to generate control signals*."

600. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

601. The combination of Kim and Rajan discloses "*a register device configured to receive command/address signals from the memory control hub and to generate control signals*."

602. For example, Rajan discloses a register 804 that receives command/address signals from the memory controller. Ex. 1015 at Fig. 8 (reproduced below), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level."); *see also* Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"), 43-44 ("Fully Buffered DIMM: Basics," "FB-DIMM," "Advanced Memory Buffer," "AMB").

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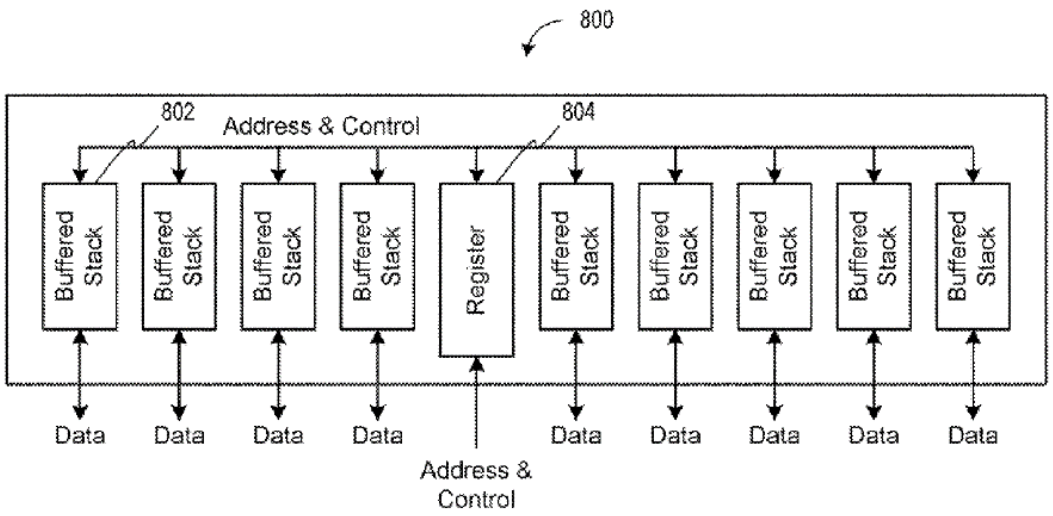


FIG. 8

Rajan also discloses that its register is generating "Address & Control" signals in response. *Id*., *see also* claim 30, *infra* at ¶¶642-649 (further discussing the register generating control signals).

603. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

604. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*a register device configured to receive command/address signals from the memory control hub and to generate control signals*."

c) [29.c] DRAM packages

605. Claim 29 requires "*a plurality of DRAM packages, each DRAM package comprising*."

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606. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

607. The combination of Kim and Rajan discloses a memory module including "*a plurality of DRAM packages,*" such as buffered stacked DRAM circuits. Ex. 1015 at Fig. 8 (reproduced above), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention."); *see also supra* ¶¶184-188 (claim limitation [1.a], discussing relevant disclosure by Kim); Ex. 1022, at 315, 374 (DRAM "packages").

608. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

609. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*a plurality of DRAM packages, each DRAM package comprising*."

d) [29.d] Terminals

(1) [29.d.1] Plurality of Data Terminals

610. Claim 29 requires "*a plurality of data terminals via which the DRAM package communicates data with the memory control hub*."

611. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

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612. As shown in the table below, claim limitation [29.d.1] is very similar to claim limitation [1.b]:

Claim 1	**Claim 29**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[29.d.1] a plurality of data terminals via which the DRAM package communicates data with the memory control hub, and

613. For the reasons discussed above with reference to claim limitation [1.b], the prior art references in Grounds 1, 2, and 3 satisfy "*a plurality of data terminals via which the DRAM package communicates data with the memory control hub*." *Supra* ¶¶189-210.

(2) [29.d.2] Plurality of Control Terminals

614. Claim 29 requires "*a plurality of control terminals to receive the control signals*."

615. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

616. As shown in the table below, claim limitation [29.d.2] is very similar to claim limitation [1.b]:

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Claim 1	Claim 29
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[29.d.2] a plurality of control terminals to receive the control signals;

617. For the reasons discussed above with reference to claim limitation [1.b], the prior art references in Grounds 1, 2, and 3 satisfy "*a plurality of control terminals to receive the control signals*." *Supra* ¶¶189-210.

e) [29.e] Array Dies in a Stack

618. Claim 29 requires "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*."

619. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

620. As shown in the table below, claim limitation [29.e] is very similar to claim limitation [1.c]:

Claim 1	Claim 29
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, . . .;	[29.e] a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die

621. For the reasons discussed above with reference to claim limitation [1.c], the prior art references in Grounds 1, 2, and 3 satisfy "*a plurality of array*

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dies arranged in a stack, including a first group of array dies and a second group of at least one array die." *Supra* ¶¶211-229.

f) [29.f] Die Interconnects

622. Claim 29 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

623. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

624. As shown in the table below, claim limitation [29.f] is identical to claim limitations [1.d.1] and [1.d.2]:

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Claim 1	**Claim 29**
[1.d.1]-[1.d.2] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[29.f] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

625. For the reasons discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Grounds 1, 2, and 3 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶230-239.

g) [29.g] Control Die

(1) [29.g.1] A Control Die Comprising

626. Claim 29 requires "*a control die comprising*."

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627. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

628. As shown in the table below, claim limitation [29.g.1] is identical to claim limitation [1.e.1]:

Claim 1	**Claim 29**
[1.e.1] a control die comprising	[29.g.1] a control die comprising

629. For the reasons discussed above with reference to claim limitation [1.e.1], the prior art references in Grounds 1, 2, and 3 satisfy "*a control die comprising*." *Supra* ¶¶240-247.

(2) [29.g.2] First and Second Data Conduit

630. Claim 29 requires "*at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and*."

631. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

632. As shown in the table below, claim limitation [29.g.2] is very identical to claim limitations [1.e.2] and [1.e.3]:

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Claim 1	**Claim 29**
[1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and [1.e.3] at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,	[29.g.2] at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and

633. For the reasons discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Grounds 1, 2, and 3 satisfy "*at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal*." *Supra* ¶¶248-264.

(3) [29.g.3] Chip Select Conduits

634. Claim 29 requires "*chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals*."

635. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

636. As shown in the table below, claim limitation [29.g.3] is very similar to claim limitations [4.a], [4.b], [6.a], and [6.b]:

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Claims 4, 6	**Claim 29**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies. [6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[29.g.3] chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

637. For the reasons discussed above with reference to claim limitations [4.a], [4.b], [6.a], and [6.b], the prior art references in Grounds 1, 2, and 3 satisfy "*chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals*." *Supra* ¶¶290-307, 314-334. For example, the chip select signals provided to the array dies are buffered or generated from the chip select signals received by the control die of the memory package. *Id*., *see also supra* at ¶¶138-141.

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(4) [29.g.4] Control Circuit

638. Claim 29 requires "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*."

639. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

640. As shown in the table below, claim limitation [29.g.4] is identical to claim limitation [11.e.5]:

Claim 11	**Claim 29**
[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.	[29.g.4] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

641. For the reasons discussed above with reference to claim limitation [11.e.5], the prior art references in Grounds 1, 2, and 3 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*." *Supra* ¶¶425-434.

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30. Claim 30 is Unpatentable

642. Claim 30 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

643. Claim 30 requires "*[t]he memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals*."

644. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

645. The combination of Kim and Rajan discloses that "*the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals.*"

646. For example, as discussed above with reference to claim limitation [1.c], Rajan discloses emulating characteristics, including rank multiplication. *Supra* ¶¶138-140, 211-229; *see, e.g.*, Ex. 1015 at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits.") and 6:30-7:67 (disclosing specific examples of rank multiplication). Rajan further discloses that "the DIMM may be an FB-DIMM, in which case the register is an

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AMB. In one embodiment the emulation is performed at the DIMM level." *Id.* at 8:56-58.

647. A Skilled Artisan would have understood from this disclosure that the AMB can perform rank multiplication, and generate chip select signals for additional ranks. *Supra* at ¶¶138-140*, see also* Ex. 1001 (060 Patent) at 18:45-51 ("The 3DS register 712 [in Figure 7] may include a DDR3 JEDEC standard register with a 'rank multiplication' circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller."), 22:34-40 (describing that rank multiplication was prior art: "Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537"); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537), Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

648. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

649. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*[t]he memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals*."

31. Claim 31 is Unpatentable

650. Claim 31 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

651. Claim 31 requires "*[t]he memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

652. The prior art references in Grounds 1-3 each teach this limitation to a Skilled Artisan.

653. As shown in the table below, claim 31 is very similar to claim limitations [29.b] and [29.g.4] and claims 2 and 30:

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Claims 2, 29, 30	**Claim 31**
[29.b] a register device configured to receive command/address signals from the memory control hub and to generate control signals; and [29.g.4] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [30] The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals. [2] The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.	[31] The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

654. For the reasons discussed above with reference to claim limitations [29.b] and [29.g.4] and claims 2 and 30, the prior art references in Grounds 1-3

satisfies this limitation. *Supra* ¶¶599-604 (claim limitation [29.b]), ¶¶630-633 (claim limitation [29.g.4]), ¶¶273-280 (claim 2), ¶¶642-649 (claim 30).

655. The combination of Kim and Rajan discloses to a Skilled Artisan that "*the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.*"

656. As discussed above with reference to claim limitations [29.b] and [29.g.4], the Kim and Rajan combination discloses a register device that generates chip select signals. *Supra* ¶¶599-604 (claim limitation [29.b]), ¶¶630-633 (claim limitation [29.g.4]). As further discussed above with reference to claim 2, the memory package receives the chip select signals which include "*data path control signals being used to control the respective states of the first data conduit and the second data conduit*." *Supra* ¶¶273-280.

657. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

658. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*[t]he memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

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32. Claim 32 is Unpatentable

659. Claim 32 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

660. Claim 32 requires "*[t]he memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal*."

661. The prior art references in Grounds 1-3 teaches this limitation to a Skilled Artisan.

662. As shown in the table below, claim 32 is very similar to claim 16:

Claim 16	**Claim 32**
[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.	[32] The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.

663. For the reasons discussed above with reference to claim limitation 16, the prior art references in Grounds 1, 2, and 3 satisfy this limitation. *Supra* ¶¶472-478.

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664. The combination of Kim and Rajan discloses to a Skilled Artisan that "*the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.*"

665. For example, as discussed above with reference to claim limitation [1.c] and claim 16, Rajan discloses that the control die emulates characteristics, including rank multiplication. *Supra* ¶¶211-229 (claim limitation [1.c]), ¶¶472-478 (claim 16); *see, e.g.*, Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."), 6:30-7:67 (disclosing examples of rank multiplication).

666. Furthermore, as discussed with reference to claim 16, Rajan also discloses "*generating the chip select signals from at least some of the control signals that include at least one address signal.*" *Supra* ¶¶472-478 (claim 16).

667. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

668. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*[t]he memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal*."

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33. Claim 33 is Unpatentable

669. Claim 33 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

670. Claim 33 requires "*[t]he memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

671. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

672. The combination of Kim and Rajan discloses that "*the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

673. As discussed above for claim limitation [4.a], the combination of Kim and Rajan discloses "*the control signals include command/address signals*." *Supra* ¶¶291-295 (claim limitation [4.a]). Furthermore, Rajan discloses that the control chip receives command/address signals for a write command and holds those signals for an additional time to control timing of when the DRAMs receive those signals. Ex. 1015 at Fig. 11 (reproduced below), 10:12-19 ("The memory controller issues the write operation at t0. In FIG. 10, the write operation appeared at the DRAM circuits one clock later at t1, due to the inherent delay through the

buffer chip. But in FIG. 11, in addition to the inherent one clock delay, the buffer chip has added an extra two clocks of delay to the write operation, which is not issued to the DRAM chips until t0+1+2=t3.").

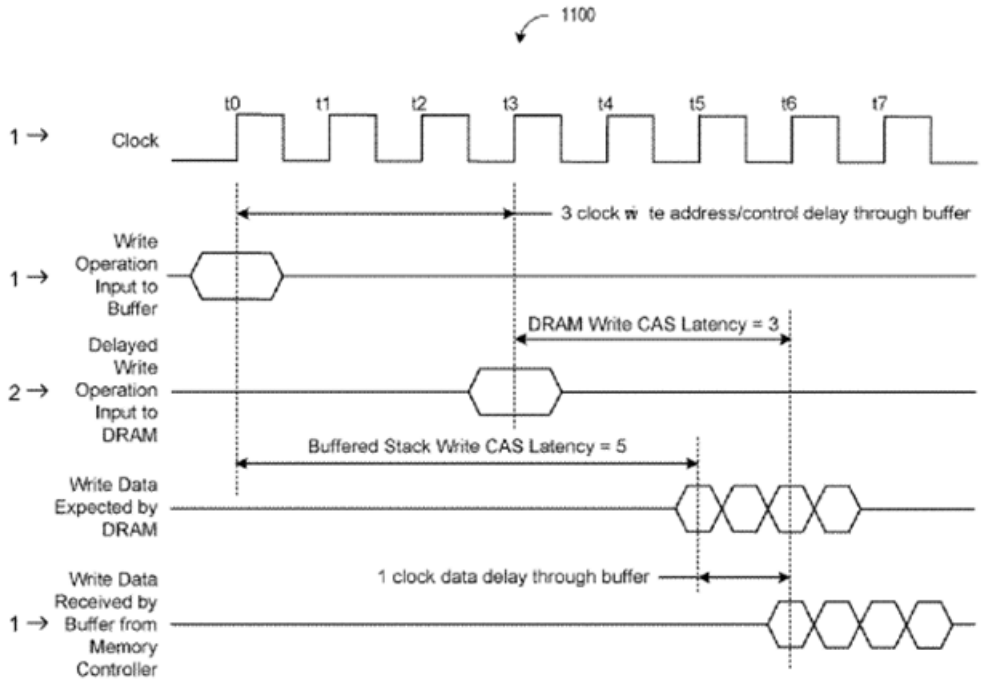


FIG. 11

674. A Skilled Artisan would have been motivated to implement this delay of command/address signals in Kim's device to emulate certain characteristics of JEDEC-standard memory devices as taught by Rajan. *See, e.g.*, Ex. 1015 (Rajan) at 9:61-10:4 ("In the specific example shown, the memory controller issues the write operation at t0. After a one clock cycle delay through the buffer chip, the write operation is issued to the DRAM chips at t1. Because the memory controller believes it is connected to memory having a read CAS latency of six clocks and thus a write CAS latency of five clocks, it issues the write data at time t0+5=t5.

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But because the physical DRAM chips have a read CAS latency of four clocks and thus a write CAS latency of three clocks, they expect to receive the write data at time t1+3=t4. Hence the problem, which the buffer chip may alleviate by delaying write operations."); *see also* Ex. 1019, at 23-24 ("CAS latency").

675. Therefore, the combination of Kim and Rajan renders obvious this limitation to a Skilled Artisan.

676. Accordingly, the prior art references in Grounds 1, 2, and 3 satisfy "*[t]he memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

34. Claim 34 is Unpatentable

677. Claim 34 is unpatentable as the prior art references in Grounds 1-3 render the claim obvious.

678. Claim 34 requires "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

679. The prior art references in Grounds 1-3 teach this limitation to a Skilled Artisan.

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680. As shown in the table below, claim 34 is very similar to claim limitation [1.e.4] and claim 3:

Claims 1 and 3	**Claim 34**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[34] The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

681. For the reasons discussed above with reference to claim limitation [1.e.4] and claim 3, the prior art references in Grounds 1, 2, and 3 satisfy "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*." *See* ¶¶265-272 (claim limitation [1.e.4]), ¶¶281-289 (claim 3).

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C. Reasons to Combine for Grounds 4 and 5

682. A Skilled Artisan would have been motivated to make the combinations in Grounds 4 and 5 for at least the following reasons.

1. Ground 4: Riho in view of Rajan

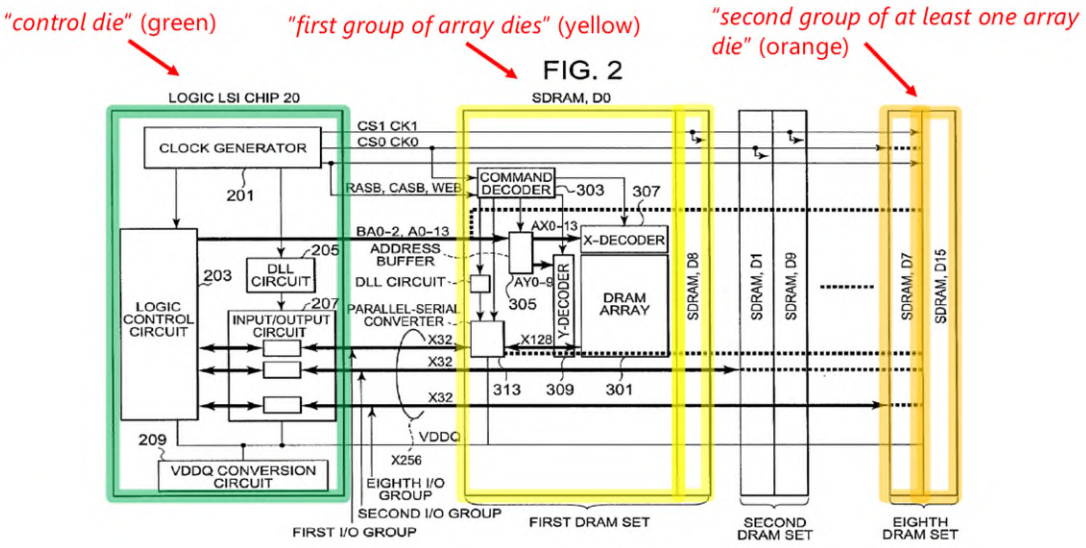
683. As mentioned above, Ground 4 involves Riho in view of Rajan. *Supra* ¶146.

684. An overview of Riho and of Rajan is provided above. *See supra* ¶¶119-125.

685. Riho is similar to the 060 Patent. For example, the 060 Patent describes the claimed "*input/output terminals*" by mentioning such terminals in passing without details and without illustrating them in the figures. Ex. 1001 at 5:7-11 ("Further, the memory package 200 may include input/output terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).") Riho, in a similar manner, discloses that, "[i]n the figure, external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20. I/O signal lines penetrating through the controlled chips, which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the

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external terminals." Ex. 1016 (Riho) at [0026]. In addition, Riho discloses that the logic LSI chip 20 communicates data signals (DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals), address signals (BA0-BA2 and A0-A13), and control signals (RASB, CASB, WEB, CS0CK0, CS1CK1,…) to the SDRAMs in the stack. *Id*. at [0030], Fig. 2 (reproduced below, annotated).



686. A Skilled Artisan would have understood from this disclosure that Riho's control chip 20 has "*input/output terminals* [at its lower side] *via which the memory package communicates data and control/address signals with one or more external devices*" and uses the received control/address signals to control the SDRAM chips in the stack. Such an arrangement of input/output terminals was well known at the time for stacked memory packages. *See, e.g.*, Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, showing that, in a stacked arrangement of

DRAM devices, a buffer chip receives data and control/address signals from an external host system and controls the DRAM devices in the stack).

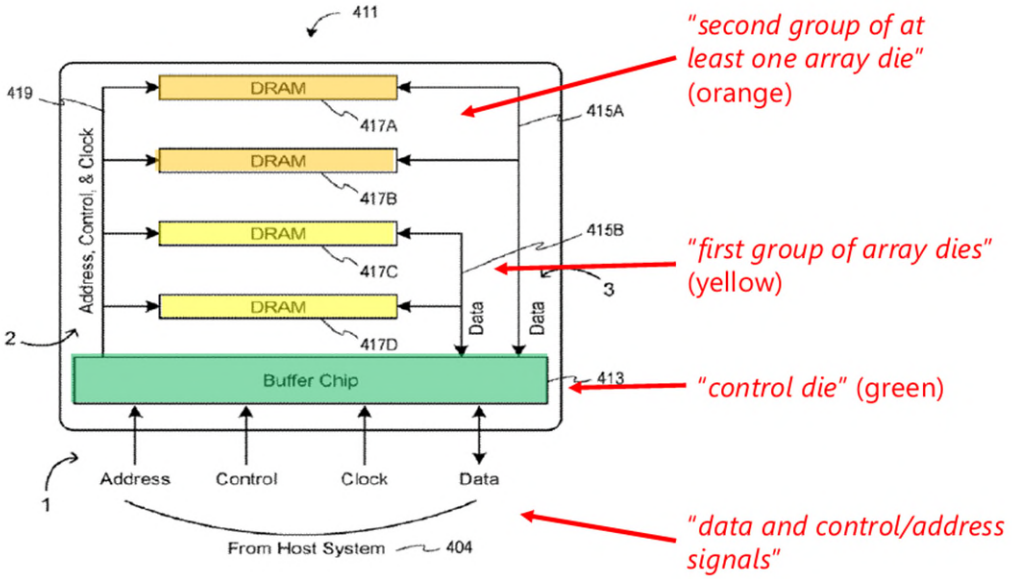


FIG. 4

687. Furthermore, the claimed "*input/output terminals*" and the corresponding "*data and control/address signals*" would have also been obvious over Riho in view of the teachings of Rajan. For example, a Skilled Artisan would have been motivated to implement a JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make the Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in

fact, DDR2 memory."); *see also id*. at Fig. 18 (reproduced below, disclosing that an interface circuit includes emulation logic which interfaces, on one side with the host system and, on the other side, with the physical memory circuits, similar to Riho's logic control circuit 203, illustrated above).

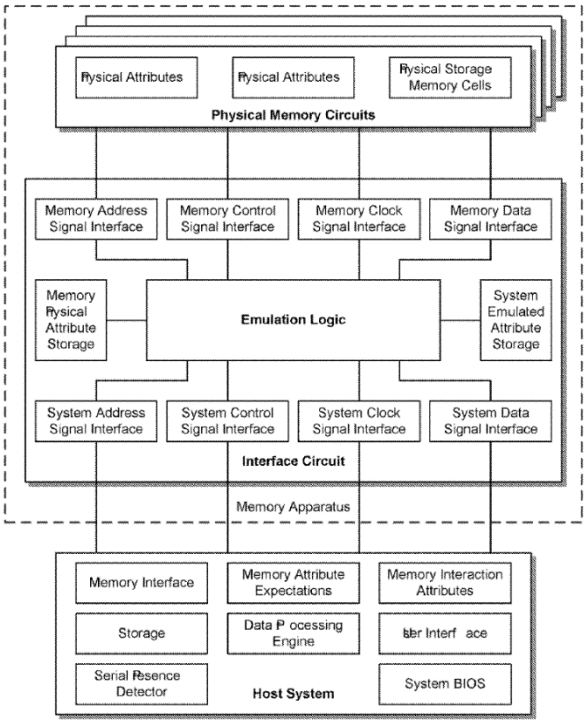


FIG. 18

688. Rajan is analogous art to Riho and the 060 Patent, as each is directed to the problem of effective operation of memory devices, including interfacing with stacked memory devices. Ex. 1015 (Rajan) at 1:51-60 ("What is needed, then, is an effective way to make use of low cost memory chips in manufacturing high capacity memory modules. … A memory subsystem is provided including an interface circuit adapted for communication with a system and a majority of address or control signals of a first number of memory circuits."), 4:48-50 ("In one

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embodiment, the DRAM chips are stacked, and the buffer chip is placed electrically between them and the host system."); Ex. 1016 (Riho) at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips."), [0012] ("According to this invention, when data signal DQ and data strobe signal DQS/B interconnections are formed by the penetrating through substrate vias, it is possible to minimize the skew between those interconnections. Further, when address, command, and clock interconnections are formed by the penetrating through substrate vias, it is also possible to minimize the skew between the address and clock interconnections and the skew between the command and clock interconnections."); Ex. 1001 (the 060 Patent) at 1:18-21 ("The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:23-26 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

689. Therefore, a Skilled Artisan would have been motivated to look at analogous art, like Rajan, for details about how Riho's control chip can interface with a host system. Rajan discloses the same basic structure of a memory package like Riho and the 060 Patent: the package includes stacked memory chips and a

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common interface circuit, called "buffer chip" in Rajan. Ex. 1015 (Rajan) at 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses."), Fig. 4 (reproduced below, annotated).

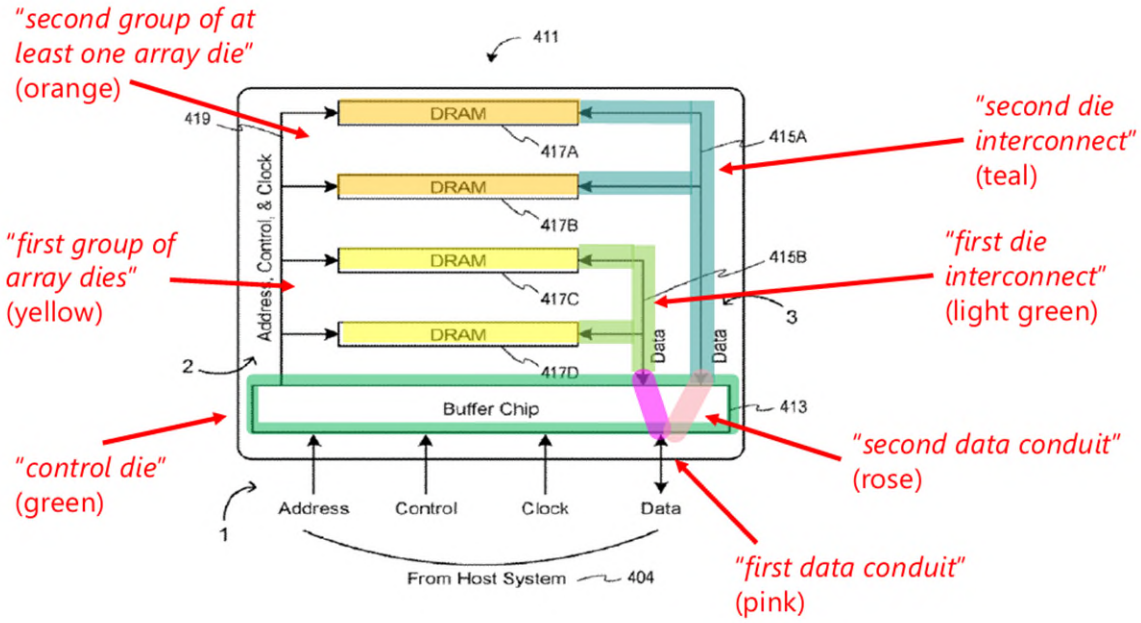


FIG. 4

690. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."). A Skilled Artisan would have understood that a JEDEC

standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below).

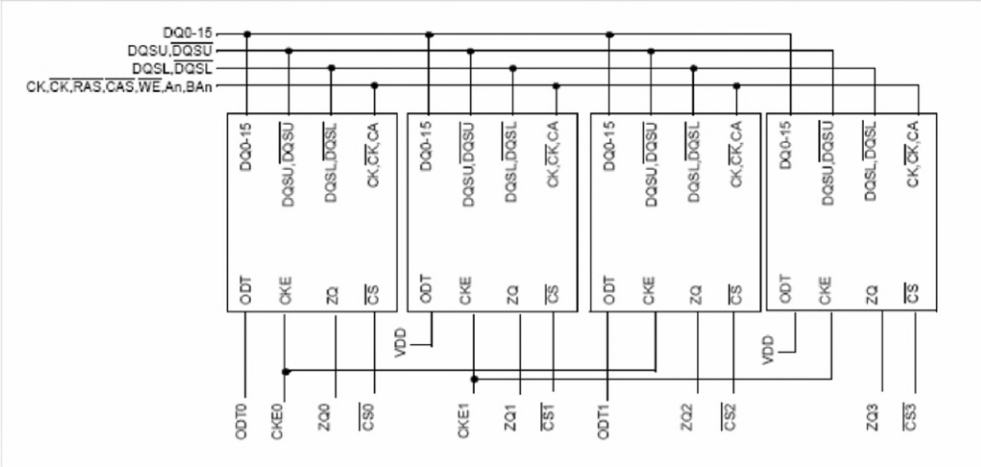


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

691. A Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control and data terminals according to the JEDEC standards in Riho's memory packages to use the packages in JEDEC compliant systems. For example, Rajan teaches that the "interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory." Ex. 1015 at 3:52-54, *see also id*. at 6:30-7:67 (the interface circuit implementing rank multiplication). A Skilled Artisan would have also understood that a DDR3 SDRAM memory

interface can include 4, 8, or 16 data terminals, and a GDDR4 memory can include 32 data terminals. *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.12-14 (describing pin-out for stacked DDR3 memory devices, Fig. 3 for x16 devices reproduced above); *see also* Ex. 1035 (JEDEC GDDR4 SGRAM Specification) at 2 ("The purpose of this Specification is to define the minimum set of requirements for JEDEC standard compatible 256 Mb through 1 Gb x32 GDDR4 SGRAM devices."). Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the prior art referenced in the 060 Patent. *See, e.g.*, Ex. 1001 (the 060 Patent) at 22:37-39 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537). As discussed above, the JEDEC standards were influential and well known. *See supra* ¶¶ 132-134; Ex. 1022, pp. 332-35, 318-20.

692. Therefore, it would have been obvious to a Skilled Artisan to implement the functionality of a standardized interface as taught by Rajan in the stacked memory package of Riho to use Riho's memory package in standardized memory systems.

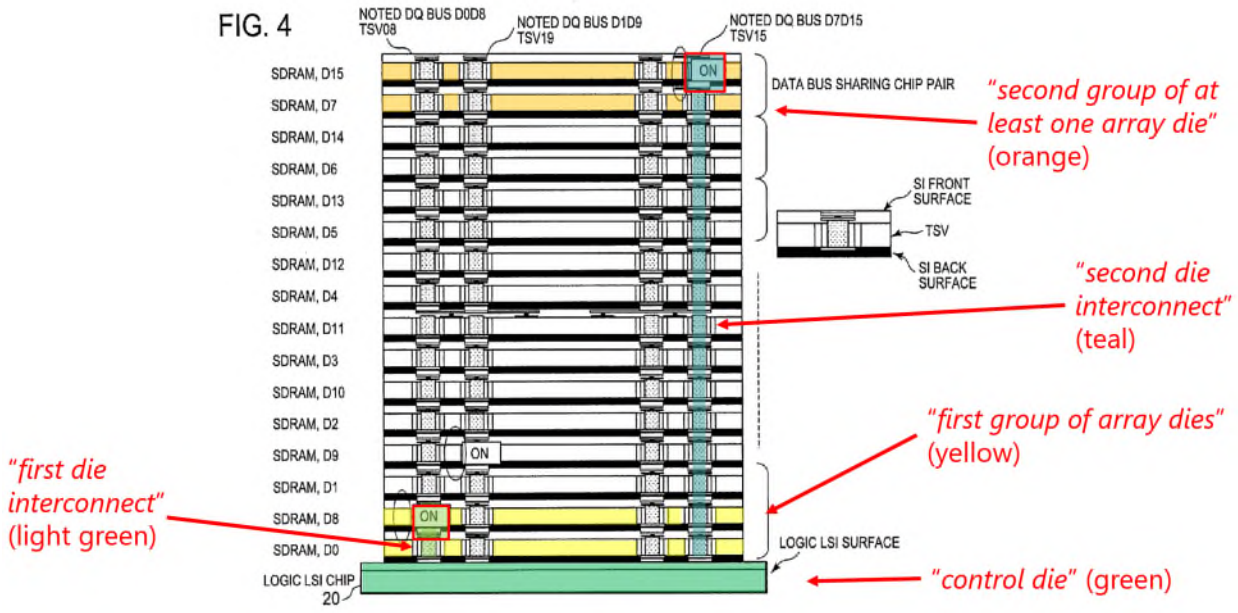
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2. Ground 5: Ground 4 in view of Riho2

693. As mentioned above, Ground 5 involves Ground 4 in view of Riho2. *Supra* ¶147.

694. An overview of Riho2 is provided above. *See supra* ¶¶129-131. As discussed below, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho, because Riho discloses differences in impedances and resistances for the different data signal DQ TSVs and Riho2 teaches to adjust the drive capacity according to such differences.

695. Riho discloses a memory package that includes stacked memory chips connected to a control chip by through-silicon vias (TSVs). Ex. 1016 (Riho) at Fig. 4 (reproduced below, annotated).



696. Riho explains that "[i]t is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in manufacturing processes (TSV forming process, bump forming process, and TSV-bump connection process). That is, TSVs formed in different manufacturing processes may have different impedances due to manufacturing variations in the manufacturing processes." Ex. 1016 (Riho) at [0055]. Riho further explains that "it is also preferable to expect that when a plurality of signal lines are formed by a plurality of TSVs, the impedance of each signal line may be different from those of the others due to variations of inherent manufacturing processes." *Id.* at [0056]. For example, Riho describes that "the SDRAM chip located closer to the logic LSI chip 20 has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip 20 has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process." *Id.* at [0061].

697. A Skilled Artisan would have understood from this disclosure that differences in impedances and other variations in the through-silicon vias and the different positions of the SDRAM chips should be taken into account when designing the stacked structure of Riho.

698. Furthermore, a Skilled Artisan would have understood that, in a case where "it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another … , a configuration is provided to optimize the output drive capacity of output buffers according to the number of stacked chip dies." Ex. 1018 (Riho2) at [0096]. A Skilled Artisan would have also known how to optimize the drive capacity. For example, Riho2's "FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097], Fig. 7A (reproduced below).

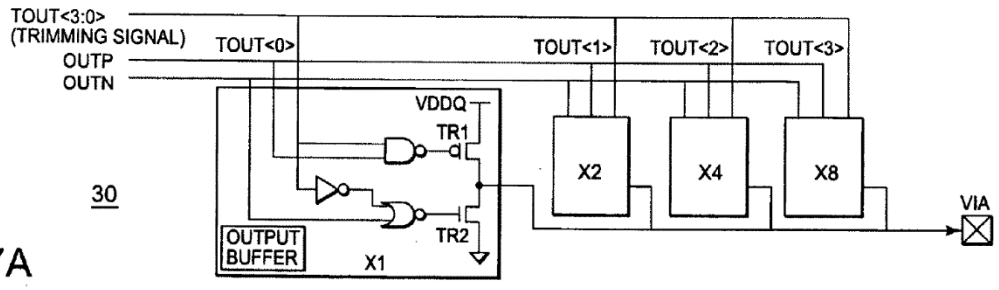


FIG. 7A

699. Therefore, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho, because Riho discloses differences in impedances and resistances for the different data signal DQ TSVs and Riho2 teaches to adjust the drive capacity according to such differences.

700. Riho2 is analogous art to Riho and the 060 Patent, as each is directed to the problem of communicating signals between stacked chips. *See, e.g.*, Ex. 1018 (Riho2) at [0003] ("This invention relates to a semiconductor device having a DRAM or the like, and particularly to a semiconductor device formed by stacking a plurality of chip dies."), [0010] ("Thus, the fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the face that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips."); Ex. 1016 (Riho) at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by

stacking a plurality of chips."), [0012] ("According to this invention, when data signal DQ and data strobe signal DQS/B interconnections are formed by the penetrating through substrate vias, it is possible to minimize the skew between those interconnections."); Ex. 1001 (the 060 Patent) at 1:18-21 ("The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules."), 5:23-26 ("As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).").

701. Therefore, a Skilled Artisan would have been motivated to look at analogous art like Riho2, which is by the same inventor as Riho, to address the issues created by the variations in the TSV properties described by Riho. In particular, a Skilled Artisan would have been motivated to optimize the output drive capacity of output buffers as taught by Riho2. A Skilled Artisan would have also understood that such an optimization of driver capacity would save power compared to using full-capacity drivers, which would be wasteful and inefficient. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."); *see also id.* at 5:11-14, Fig.5; Ex. 1039 at Abstract ("In other embodiments, for example, differences in the

termination impedance or driver drive-strength resulting from differences in the location of a die in a stack may be compensated for."), 7:46-49 ("One embodiment of a compensation circuit 400 that may compensate for both termination impedance and drive strength variations resulting from differences in die location is shown in FIG. 6."), and Fig. 6.

702. Making such a combination was well within the level of skill, since Riho2 itself teaches drivers of different strengths, and the combination would have provided nothing more than expected, a power efficient drive of signals through Riho's TSVs.

703. Therefore, it would have been obvious to a Skilled Artisan to implement the functionality of optimized drivers as taught by Riho2 in the stacked memory package of Riho to make Riho's memory package more efficient.

D. Claims 1-34 Are Unpatentable Over Grounds 4-5

704. As explained below claims 1-14, 16-19, and 29-34 are unpatentable over Ground 4 (Riho in view of Rajan), and claims 1-34 are unpatentable over Ground 5 (Ground 4 in view of Riho2).

1. Claim 1 is Unpatentable

705. Claim 1 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

a) [1.a] Preamble

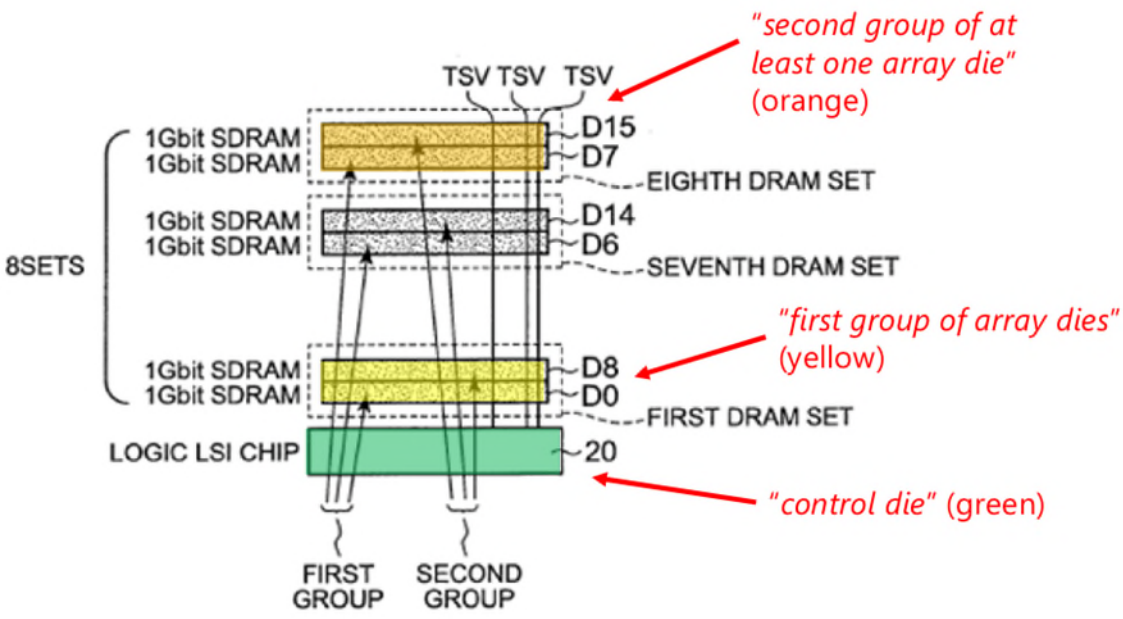
706. The preamble of claim 1 requires "*[a] memory package, comprising.*"

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707. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

708. Riho discloses a "*memory package*" including a control chip (logic LSI chip 20) and stacked SDRAM chips (D0-D15) "integrally packaged." Ex. 1016 at Fig. 1 (reproduced below, annotated), [0026] ("The illustrated semiconductor device [in FIG. 1] comprises a logic LSI chip 20 as a control chip and a plurality of SDRAM chips as controlled chips stacked on the logic LSI chip 20. The control chip may be also called a master chip (or active chip) while each controlled chip is a slave chip (or passive chip). For example, the semiconductor device comprising the master chip and the slave chips has a system-in-package structure in which those chips are assembled in layers and integrally packaged.").

FIG. 1



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709. Therefore, Riho discloses a "*memory package*."

710. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy "*[a] memory package, comprising*."

b) [1.b] Input/Output Terminals

711. Claim 1 requires "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices.*"

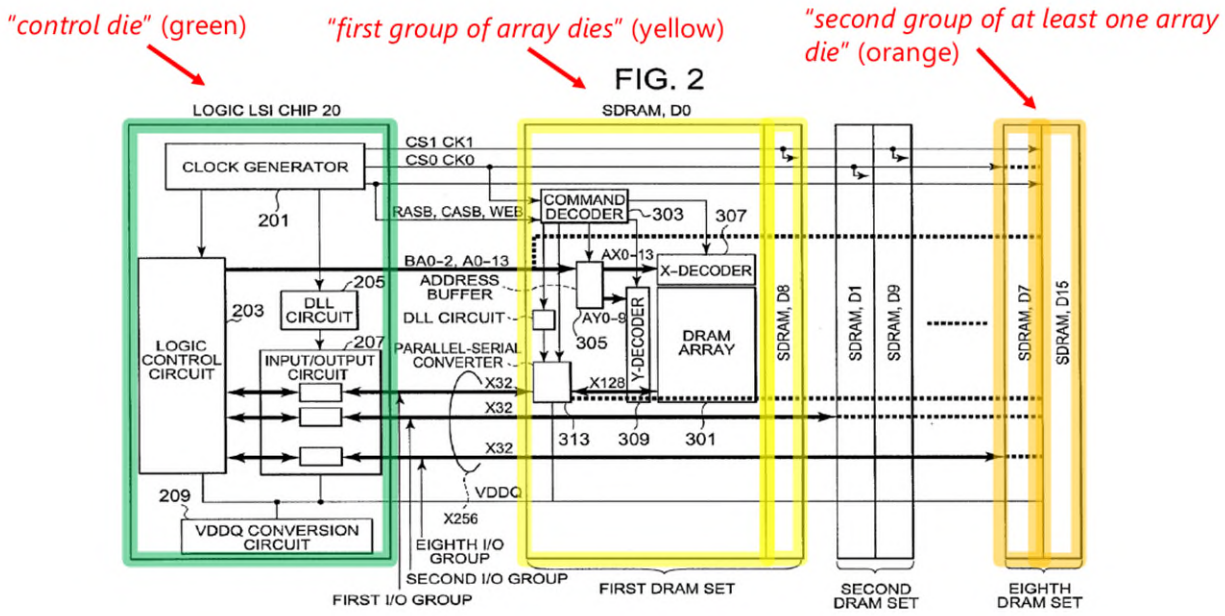
712. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

713. Riho discloses to a Skilled Artisan that the stacked package includes "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

714. For example, with reference to Fig. 1, Riho discloses that, "external terminals (not illustrated) of the semiconductor device . . . are disposed on the lower side of the logic LSI chip 20," and that "[t]he external terminals are connected to the logic LSI chip 20." Ex. 1016 at [0026]. Riho further discloses that "I/O signal lines penetrating through the controlled chips . . . are connected to the logic LSI chip 20 and are not directly connected to the external terminals." *Id.*

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Riho also discloses that the logic LSI chip 20 communicates data signals (DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals), address signals (BA0-BA2 and A0-A13), and control signals (RASB, CASB, WEB, CS0CK0, CS1CK1,…) to the SDRAMs in the stack. *See id.* at [0030-31], Fig. 2 (reproduced below, annotated).



715. It would have been obvious to a Skilled Artisan that Riho's logic LSI chip 20 can have "*input/output terminals* [at its lower side] *via which the memory package communicates data and control/address signals with one or more external devices*" and that chip 20 uses the received control/address signals to control the SDRAM chips in the stack. For example, a Skilled Artisan would have been motivated to use terminals in Riho's control die for external data and control/address signals as taught by Rajan and/or as specified in the well-known

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JEDEC specifications. *Supra at* ¶¶683-692. *See, e.g.,* Ex. 1015 (Rajan) at Figs. 4 and 18 (reproduced below, annotated, showing that, in a stacked arrangement of DRAM devices, a buffer chip receives data and control/address signals from an external host system and controls the DRAM devices in the stack).

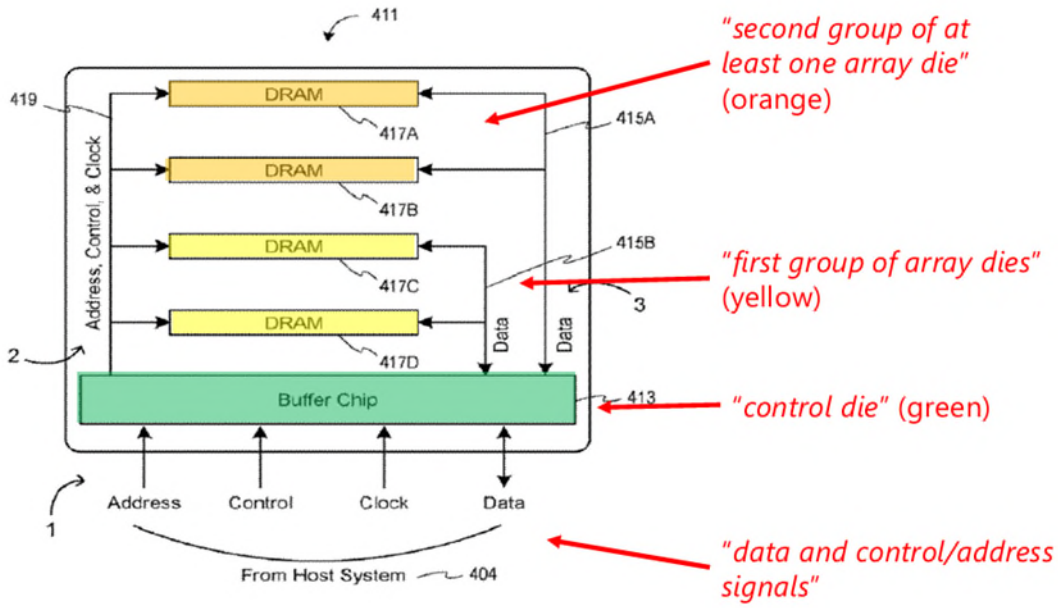


FIG. 4

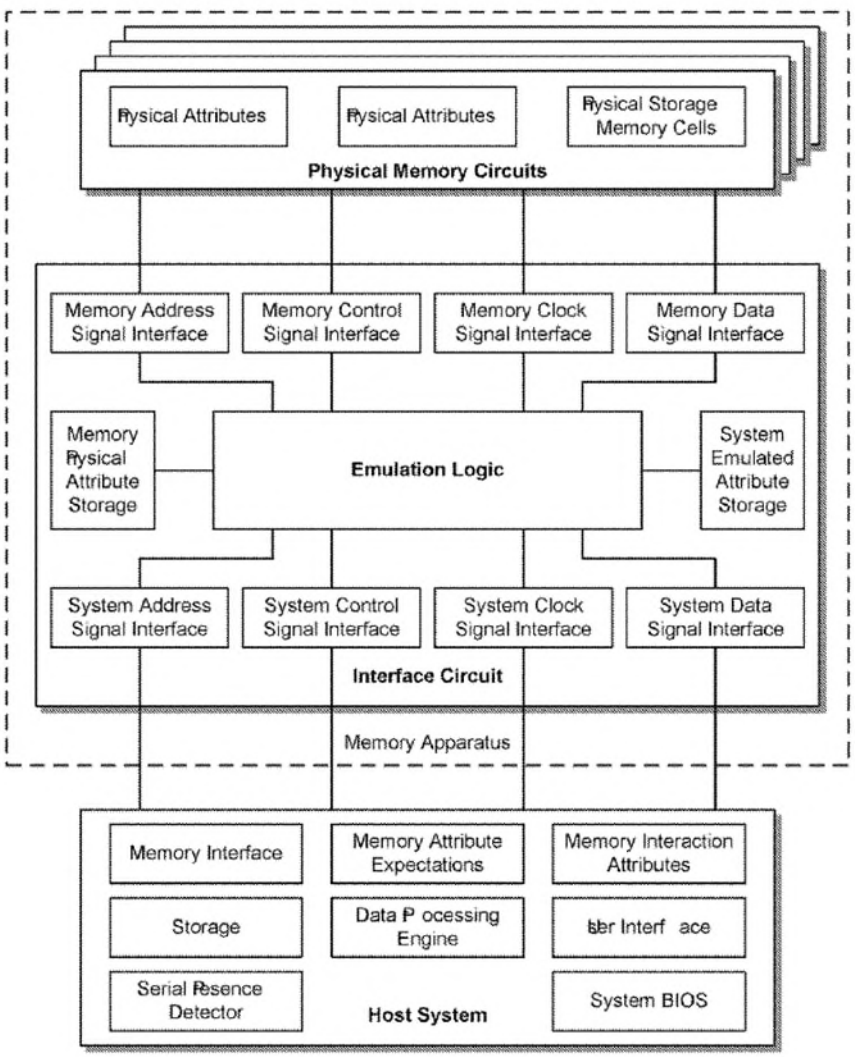


FIG. 18

716. Accordingly, it would have been obvious to a Skilled Artisan to combine Riho and Rajan and implement Riho's memory package with the terminals as disclosed by Rajan. *Supra,* ¶¶683-692.

717. Therefore, Riho discloses and in view of Rajan renders obvious this limitation to a Skilled Artisan.

718. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a plurality of input/output terminals via which the memory package*

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communicates data and control/address signals with one or more external devices."

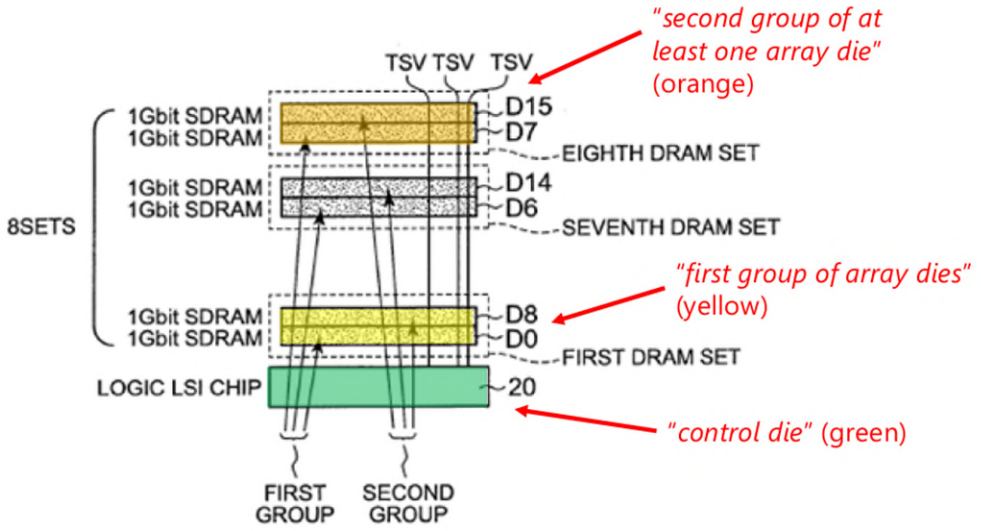
c) [1.c] Stacked Array Dies

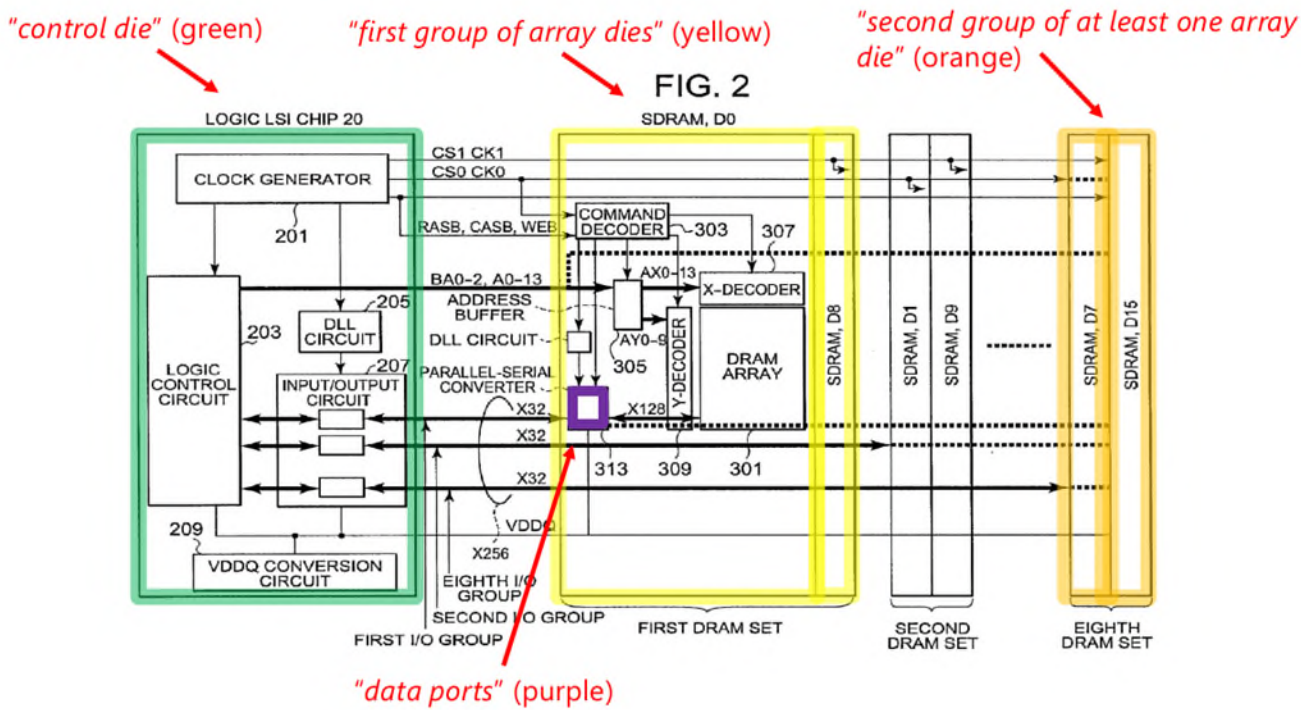
719. Claim 1 requires "*a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports.*"

720. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

721. Riho discloses "*a plurality of stacked array dies including a first group of array dies* [e.g., a first DRAM set including a pair of SDRAMs D0 and D8 sharing data signal DQ TSV08] *and a second group of at least one array die* [e.g., an eighth DRAM set including a pair of SDRAMs D7 and D15 sharing data signal DQ TSV715]*, each array die having data ports* [including a parallel-serial conversion circuit 313 in each SDRAM]." *See, e.g.*, Ex. 1016 at Fig. 1 (reproduced below, annotated, showing stacked SDRAMs including eight sets of SDRAM pairs), Fig. 2 (reproduced below, annotated, showing internal structure of SDRAMs, including a DRAM array and a parallel-serial conversion circuit 313 for communicating data with the logic chip 20).

FIG. 1





722. For example, Riho discloses "*a plurality of stacked array dies*," such as SDRAM chips D0-D15. *Id.* at Fig. 1 (reproduced above), [0027] ("FIG. 1 shows an example in which 16 SDRAM chips D0 to D15 each having a memory

capacity of 1 Gbit are stacked on the logic LSI chip 20 operable as the control chip. Each of the illustrated SDRAM is a DDR (Double Data Rate) 3 synchronous dynamic random access memory."). Riho further discloses that each of SDRAM chips D0-D15 include a respective DRAM array 301 and a parallel-serial converter 313. *See id.* at [0047] ("Herein, taking the SDRAM D0 as an example, the structure of the SDRAM chip used in this embodiment will be described. The illustrated SDRAM D0 comprises . . . a DRAM array 301 having a memory capacity of 2 Gbit, a command decoder 303, an address buffer 305, an X-decoder 307, a Y-decoder 309, a DLL circuit 311, and a parallel-serial conversion circuit 313."). Riho explains that "the DRAM array 301 inputs and outputs 128-bit (×128) data signals in parallel between itself and the parallel-serial conversion circuit 313. … The parallel-serial conversion circuit 313 sends and receives ×128-bit parallel data signals between itself and the DRAM array 301 and further sends and receives 32-bit (×32) parallel data signals between itself and the logic LSI chip 20." *Id*. at [0049].

723. A Skilled Artisan would have understood from this disclosure that each SDRAM chip in Riho is an "*array die*" because each chip includes a DRAM array and further includes respective "*data ports*," comprising parallel serial conversion circuit 313, which communicate (x32) data between the DRAM array 301 and the control chip 20. A Skilled Artisan would have also understood that

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Riho's SDRAM chip includes a "*die*." *See, e.g.*, Ex. 1018 (Riho2) at Abstract and Fig. 1 (describing, similar to Riho, "stacked chip dies," each including a respective memory cell array 230 and IO circuits 2500-2531).

724. Riho also discloses (eight) groups of SDRAMs, including a "*first group of array dies*," such as the first DRAM set including SDRAMs D0 and D8, and a "*second group of at least one array die*," e.g., the eighth DRAM set including SDRAMs D7 and D15. Ex. 1016 at Fig. 1, [0029] ("In the illustrated example, the SDRAMs D0 and D8 form a first DRAM set located closest to the logic LSI chip 20, then, subsequent pairs of the SDRAMs D1 and D9, D2 and D10, D3 and D11, D4 and D12, D5 and D13, D6 and D14, and D7 and D15 form second to eighth DRAM sets, respectively. As seen in FIG. 1, the SDRAM D15 of the eighth DRAM set is disposed at a position farthest from the logic LSI chip 20."). Riho further explains that the SDRAMs in each DRAM set share respective data signal TSVs. *Id.* at [0045-46] ("… the data signal DQ TSVs for the SDRAM D0 are also used by the SDRAM D8 (first DRAM set). That is, the data signal DQ TSVs for the SDRAM D0 are commonly used by the first DRAM set (SDRAM D0 and SDRAM D8). … The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15."), [0062] ("The adjacent two SDRAMs of the first and second groups, such as, for example, the SDRAMs D0 and D8, D1 and D9, or D7 and D15, form a SDRAM

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pair or set (n-th DRAM set) sharing the corresponding data signal DQ TSVs, i.e. corresponding buses (n-th I/O group).").

725. Therefore, Riho discloses this limitation to a Skilled Artisan.

726. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports*."

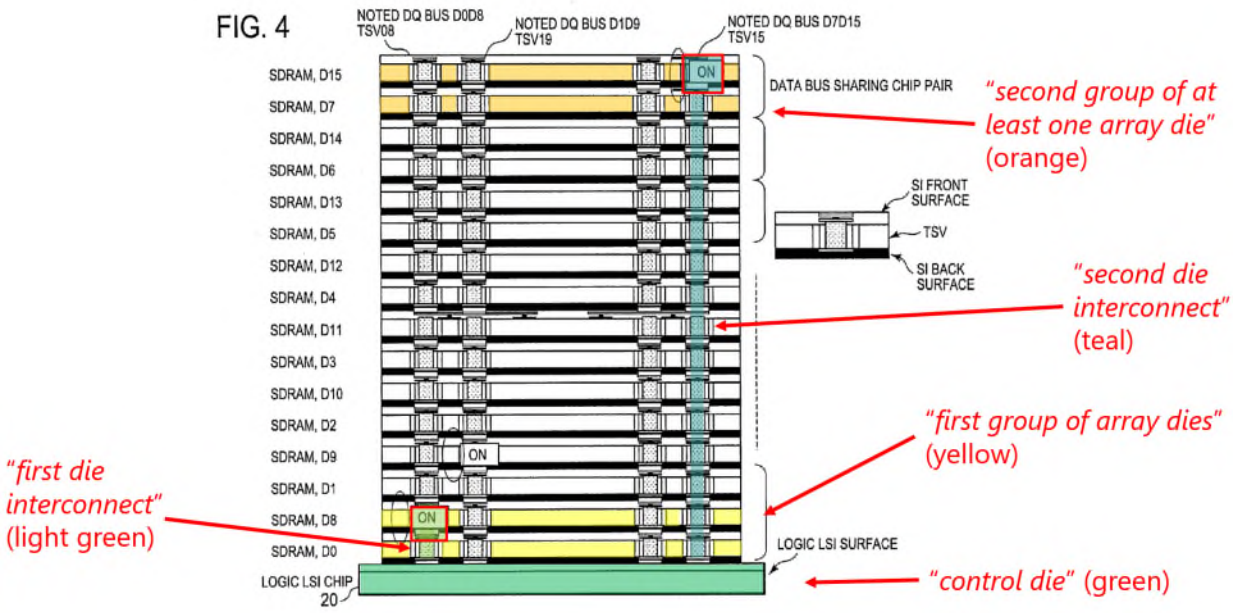
d) [1.d.1] and [1.d.2] Die Interconnects in Electrical Communication with Array Dies

727. Claim 1 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.*"

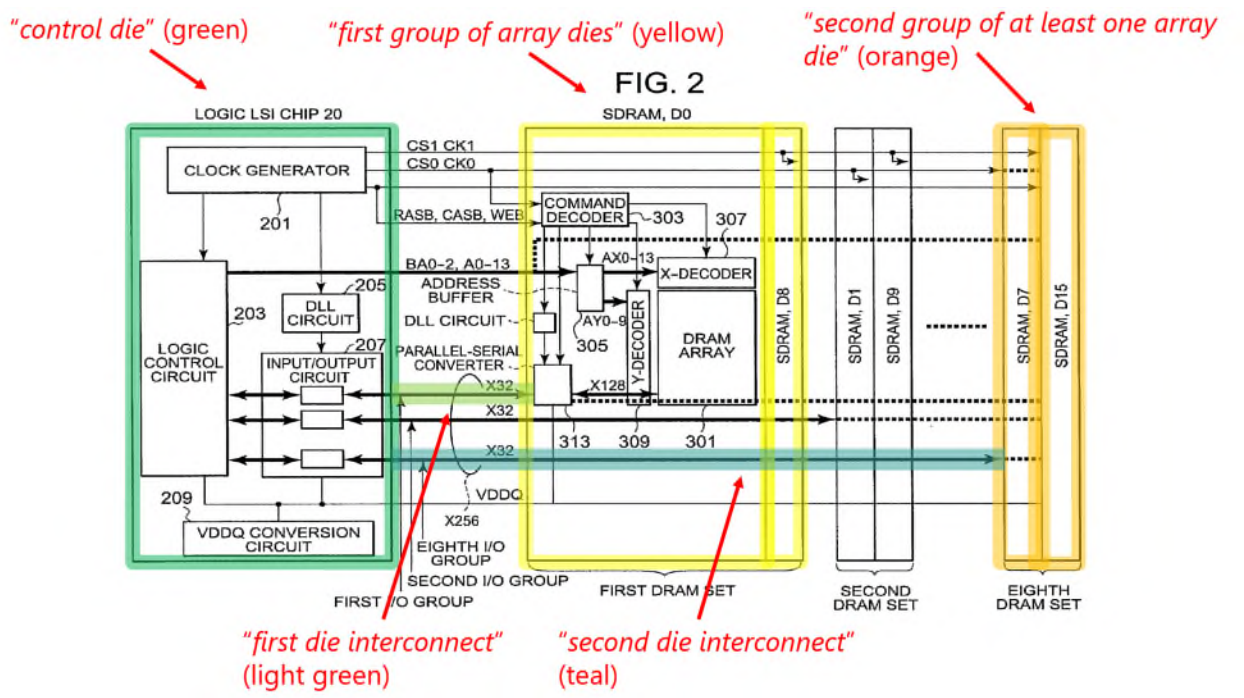
728. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

729. Riho discloses, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, "*at least a first die interconnect* [e.g., data signal DQ TSV08] *and a second die interconnect* [e.g., data signal DQ TSV715]*, the first die interconnect* [TSV08] *in electrical communication with the first group of array dies* [the first DRAM set including SDRAMs D0 and D8] *and not in electrical*

communication with the second group of at least one array die [all other SDRAMs, including the eighth DRAM set of SDRAMs D7 and D15]." *See, e.g.*, Ex. 1016 at Figs. 4, 2 (both reproduced below, annotated).



730. For example, Riho explains that "SDRAM D0 (first DRAM set) and the input/output circuit 207 of the logic LSI chip 20 are connected to each other through the 32 data signal DQ TSVs as indicated by ×32 (first I/O group) in FIG. 2." Ex. 1016 at [0045], Fig. 2 (reproduced below annotated).



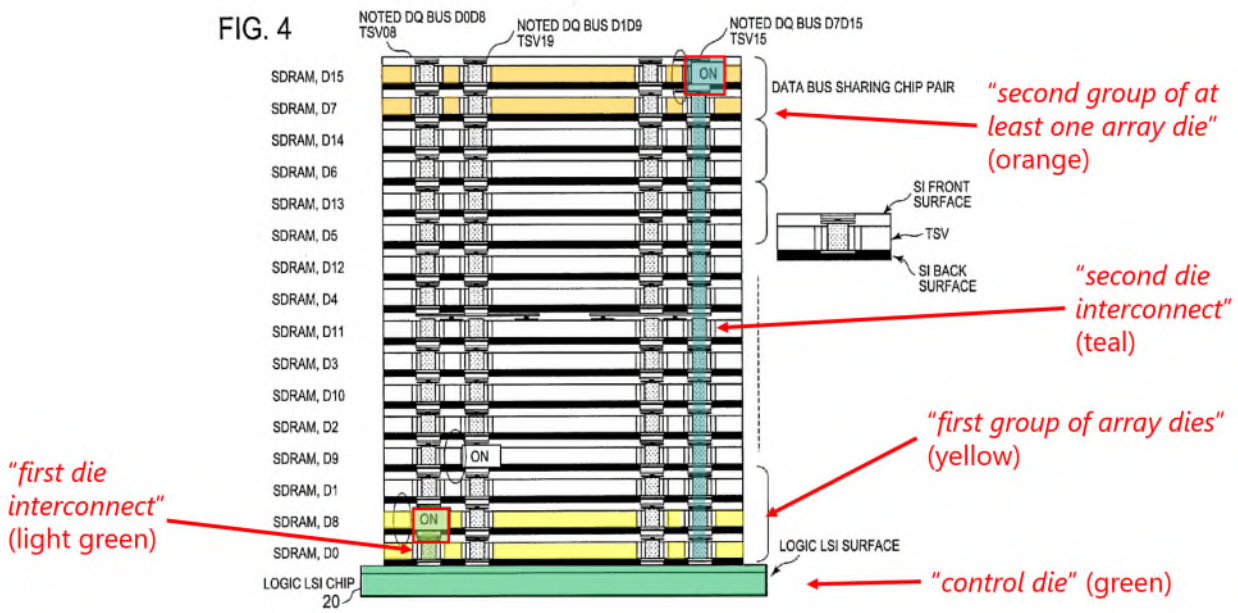
731. Riho further explains that "the data signal DQ TSV08 includes a portion shared by the SDRAMs D0 and D8 and, in this connection, circuits formed at the front surfaces of the SDRAMs D0 and D8 and the data signal DQ TSV08 are in a conductive state (i.e. on state). On the other hand, the SDRAMs other than the SDRAMs D0 and D8 and the data signal DQ TSV08 are in a non-conductive state (i.e. off state)." Ex. 1016 at [0064].

732. A Skilled Artisan would have understood from this disclosure that, at least under Netlist's apparent interpretation, Riho's data signal DQ TSV08 is "*in electrical communication with the first group of array dies*" including SDRAMs D0 and D8, which are set into a conductive "on state," and that DQ TSV08 is "*not in electrical communication*" with any other SDRAMs, including SDRAMs D7

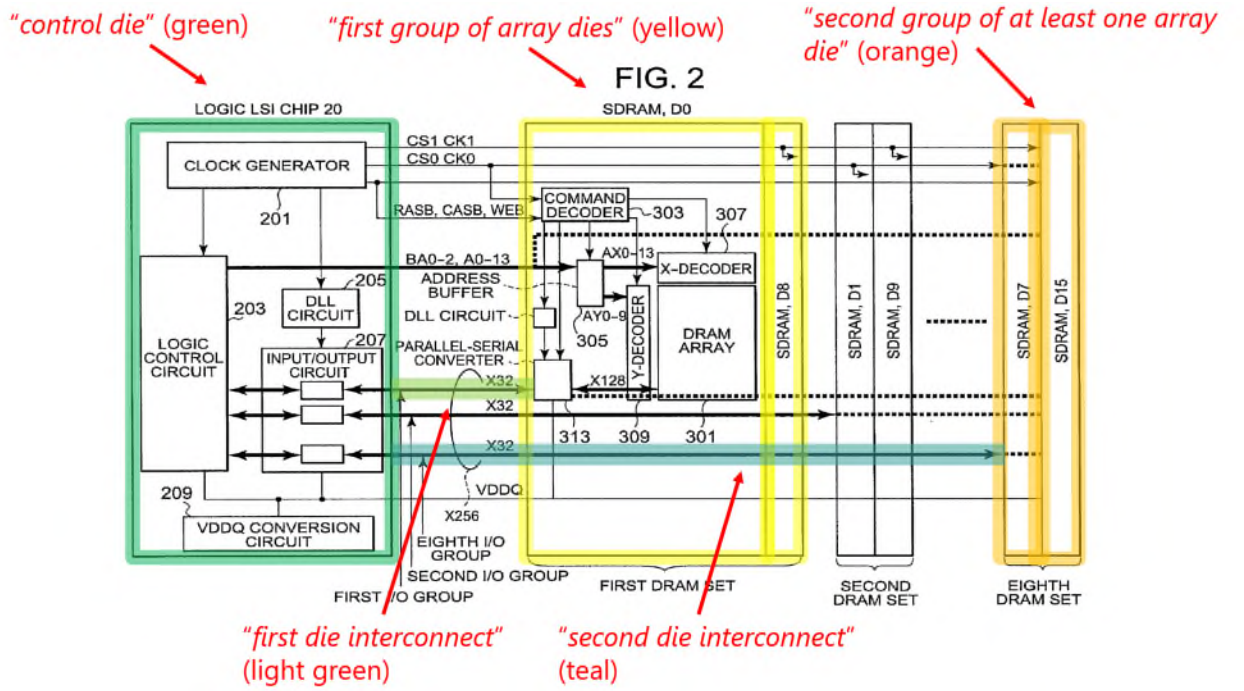
and D15 in the "*second group of at least one array die*," which are in a non-conductive "off state."

733. Therefore, Riho discloses "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*" to a Skilled Artisan.

734. Likewise, Riho discloses, at least under Netlist's apparent interpretation, that "*the second die interconnect* [TSV715 is] *in electrical communication with the second group of at least one array die* [the eighth DRAM set including SDRAMs D7 and D15] *and not in electrical communication with the first group of array dies* [the first DRAM set including SDRAMs D0 and D8]." *See, e.g.*, Ex. 1016 at Figs. 4, 2 (both reproduced below annotated).



735. For example, Riho explains that "data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15." Ex. 1016 at [0046], Fig. 2 (reproduced below, annotated).



736. Riho further explains that "the data signal DQ TSV715 and circuits formed at the front surfaces of the SDRAMs D7 and D15 are in a conductive state (i.e. on state)." Ex. 1016 at [0065].

737. For the reasons discussed immediately above with reference to the "*first die interconnect*" TSV08, a Skilled Artisan would have understood from Riho's disclosure that, at least under Netlist's apparent interpretation, data signal DQ TSV715 ("*the second die interconnect*") is in electrical communication with SDRAMs D7 and D15, but not with any other SDRAMs in the stack.

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738. Therefore, Riho discloses "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*" to a Skilled Artisan.

739. Furthermore, it would have been obvious to a Skilled Artisan in view of Rajan that "*the first die interconnect* [(light green) for communicating data is] *in electrical communication with the first group of array dies* [including array dies D0 and D8 (yellow)] *and not in electrical communication with the second group of at least one array die* [including array dies D7 and D15 (orange)]," and "*the second die interconnect* [(teal) for communicating data is] *in electrical communication with the second group of at least one array die* [including array dies D7 and D15 (orange)] *and not in electrical communication with the first group of array dies* [including array dies D0 and D8 (yellow)]."

740. Rajan teaches that memory dies in a stack are grouped such that a first die interconnect (415B, light green) to communicate data is in electrical communication with a first group of dies (including dies 417C and 417D, yellow) and not in electrical communication with a second group of memory dies (including dies 417A and 417B, orange). Ex. 1015 (Rajan) at 5:36-43 ("There is a shared address, control, and clock bus 419, and a plurality of shared data busses 415A and 415B. Each shared bus has two or more DRAM chips coupled to it."), Fig. 4 (reproduced below, annotated). Rajan also teaches a second die interconnect

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(415A, teal) to communicate data that is in electrical communication with the second group of dies (including dies 417A and 417B, orange) and not in electrical communication with the first group of memory dies (including dies 417C and 417D, yellow). *Id*.

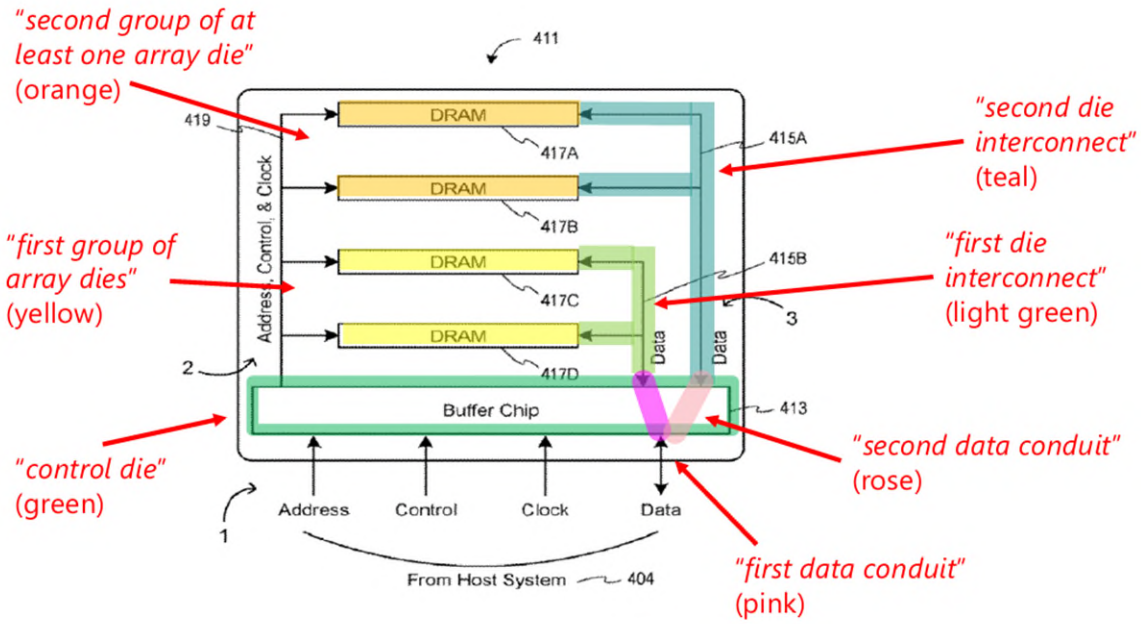


FIG. 4

741. As discussed above, Riho and Rajan are analogous art to the 060 Patent. *Supra* at ¶688. Furthermore, each is directed to memory stacks and pertinent to the problem of reducing load in systems using stacked memory devices. Ex. 1015 (Rajan) at 5:63-6:2 ("FIGS. 2 through 6 are not intended to be an exhaustive listing of all possible permutations of data paths, busses, and buffer chip configurations, and are only illustrative of some ways in which the host system device can be in electrical contact only with the load of the buffer chip and

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thereby be isolated from whatever physical memory circuits, data paths, busses, etc. exist on the (logical) other side of the buffer chip."); Ex. 1016 (Riho) at [0103] ("Further, by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups."), Ex. 1001 (060 Patent) at ("More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules.").

742. A Skilled Artisan would have been motivated to look at analogous art like Rajan and apply the teaching of Rajan to the groups of dies in the stack of Riho such that each group of dies communicates data through a respective die interconnect which is not in electrical communication with other dies in the stack because such an arrangement advantageously lowers the load on those die interconnects. *See*, *e.g.*, Ex. 1016 (Riho) at [0013] ("Further, when the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used."); *see also infra* at ¶¶833-849 (further explaining the advantages of reduced load in Riho due

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to connecting some but not all the dies to the die interconnects that communicate data).

743. For at least the above reasons, these limitations were also obvious to a Skilled Artisan over Riho in light of Rajan.

744. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

e) [1.e] Control Die

(1) [1.e.1] A Control Die Comprising

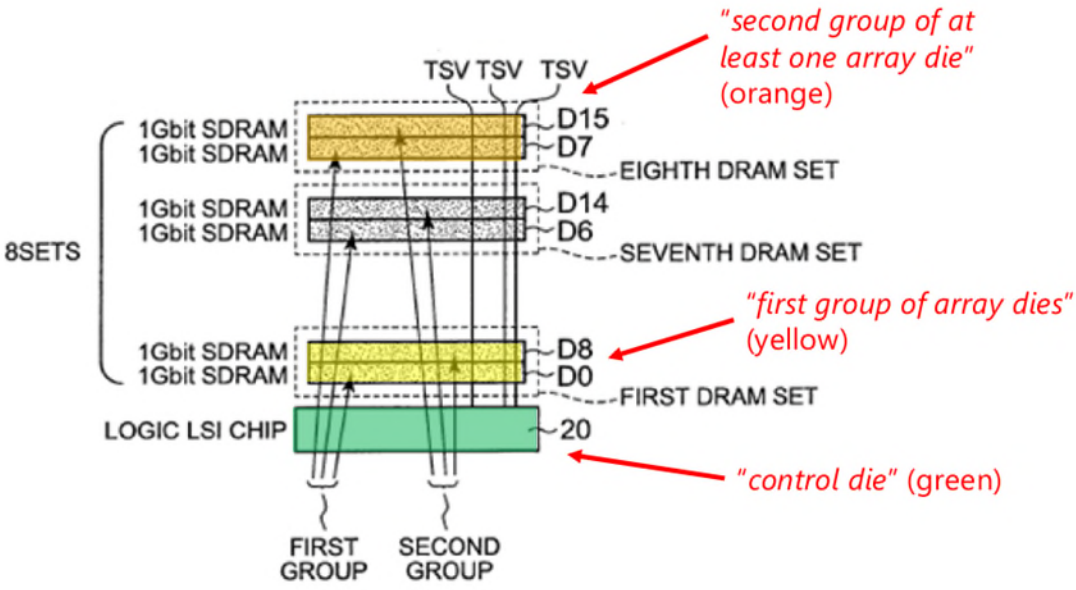
745. Claim 1 requires "*a control die comprising.*"

746. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

747. Riho discloses "*a control die*" including Logic LSI chip 20. *See, e.g.*, Ex. 1016 at Fig. 1 (reproduced below, annotated).

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FIG. 1



748. For example, Riho discloses that the "illustrated semiconductor device comprises a logic LSI chip 20 as a control chip and a plurality of SDRAM chips as controlled chips stacked on the logic LSI chip 20." Ex. 1016 at [0026].

749. A Skilled Artisan would have understood from this disclosure that the logic LSI chip 20 includes a die which controls the operation of the stacked SDRAMs in Riho's semiconductor device.

750. Furthermore, in the combination of Riho and Rajan, the "*control die*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices. *Supra* at ¶¶138-140, 683-692.

751. Therefore, Riho discloses and in view of Rajan renders obvious this limitation to a Skilled Artisan.

752. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a control die comprising*."

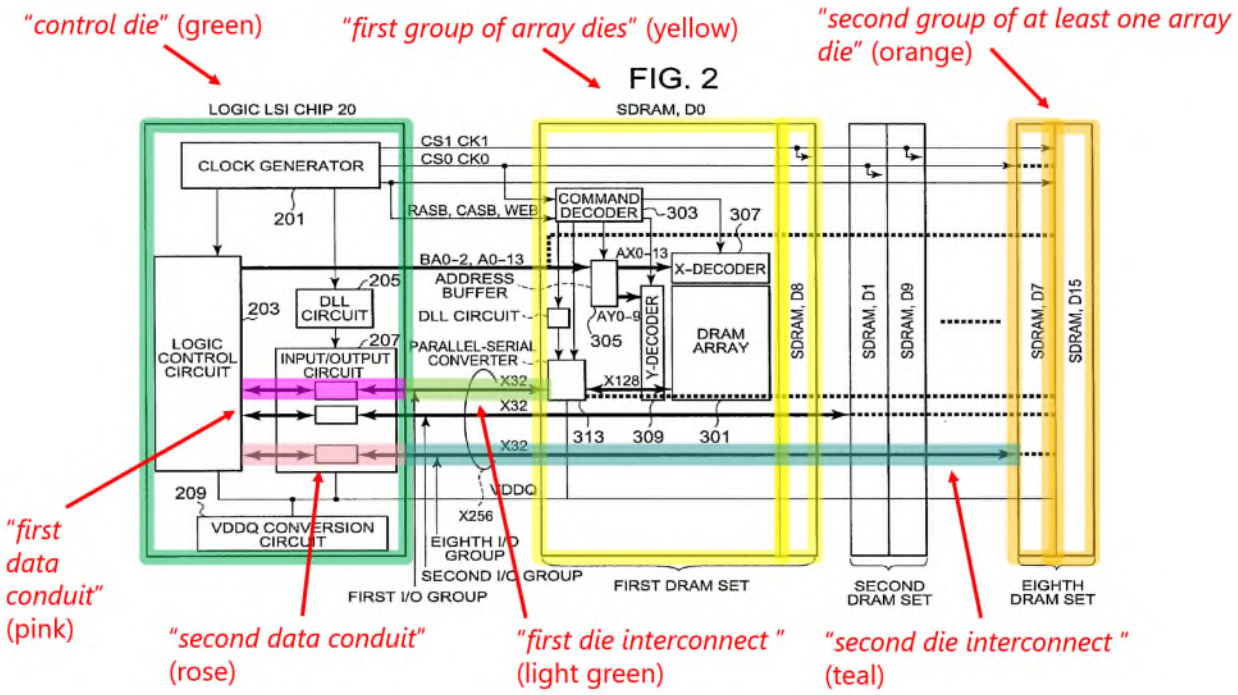
(2) [1.e.2] and [1.e.3] First and Second Data Conduit

753. Claim 1 requires "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals,"* and "*at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal*."

754. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

755. Riho discloses "*at least a first data conduit* [(pink)] *between the first die interconnect* [TSV08 (light green)] *and a first terminal* [e.g., an external data terminal] *of the plurality of input/output terminals* [of the control chip 20]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).

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756. For example, Riho discloses that "[t]he logic control circuit 203 provided in the logic LSI chip 20 … sends and receives data signals DQ between itself and the input/output circuit 207." *Id.* at [0039]. Riho also discloses that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total." *Id.* at [0040]. Riho further discloses that the input/output circuit 207 transmits or receives the data signal DQ "as an I/O data signal," and that each DRAM set is allocated with a respective I/O group (×32 DQ signal bits) for a total of eight I/O groups. *Id.* For example, "[t]he SDRAM D0 (first DRAM set) and the input/output circuit 207 of the logic LSI chip 20 are connected to each other through the 32 data signal DQ

TSVs as indicated by ×32 (first I/O group) in FIG. 2. The input/output circuit 207 includes interface circuits such as buffers corresponding to the SDRAM chips, respectively, so that data signals DQ are sent and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit." *Id.* at [0045].

757. Furthermore, as discussed above with reference to claim limitation [1.b], Riho discloses to a Skilled Artisan that control chip 20 has input/output terminals for communicating data signals. *Supra* ¶¶711-718; *see also, e.g.*, Ex. 1016 at [0026] ("In the figure, external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20."); *see also* Ex. 1015 (Rajan) at Fig. 4 (reproduced below, annotated, expressly showing data connections with an external device of a host system).

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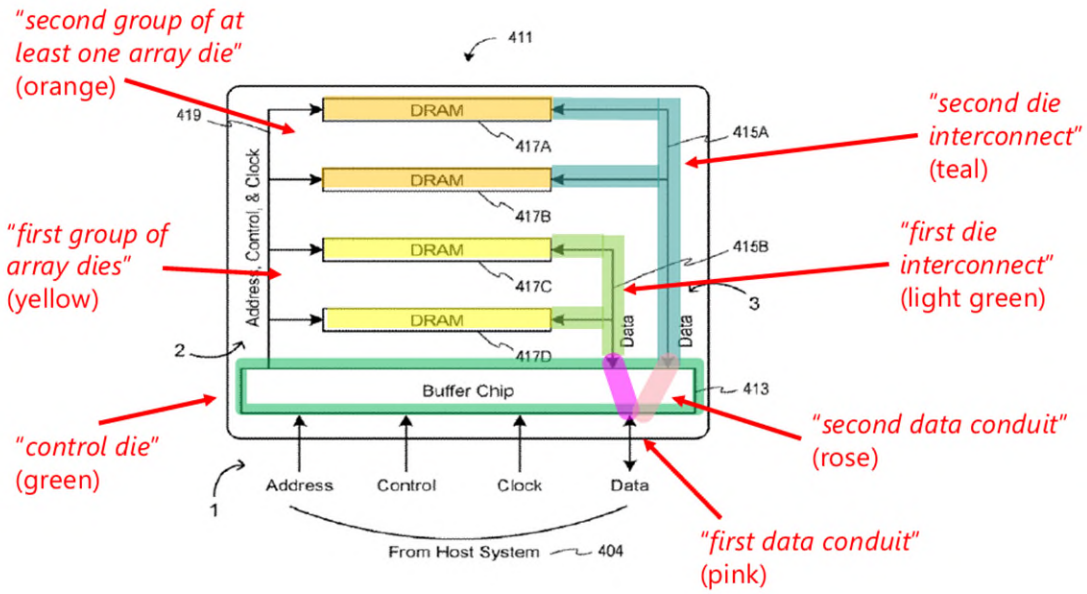
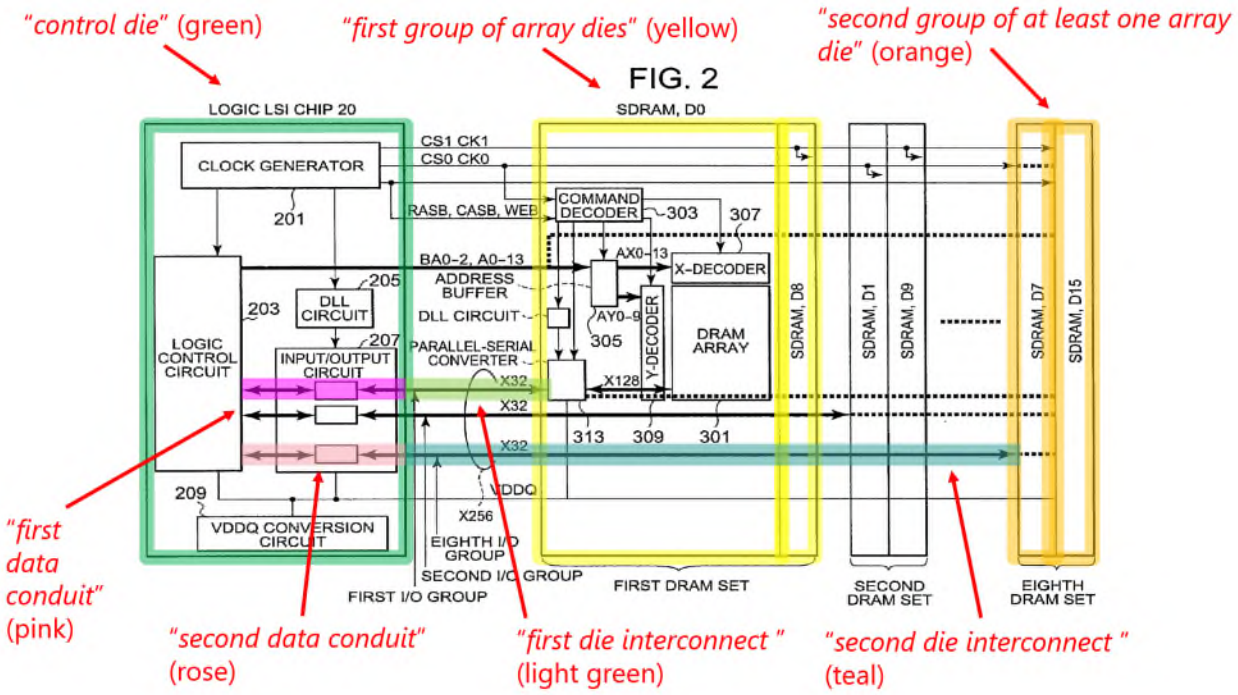


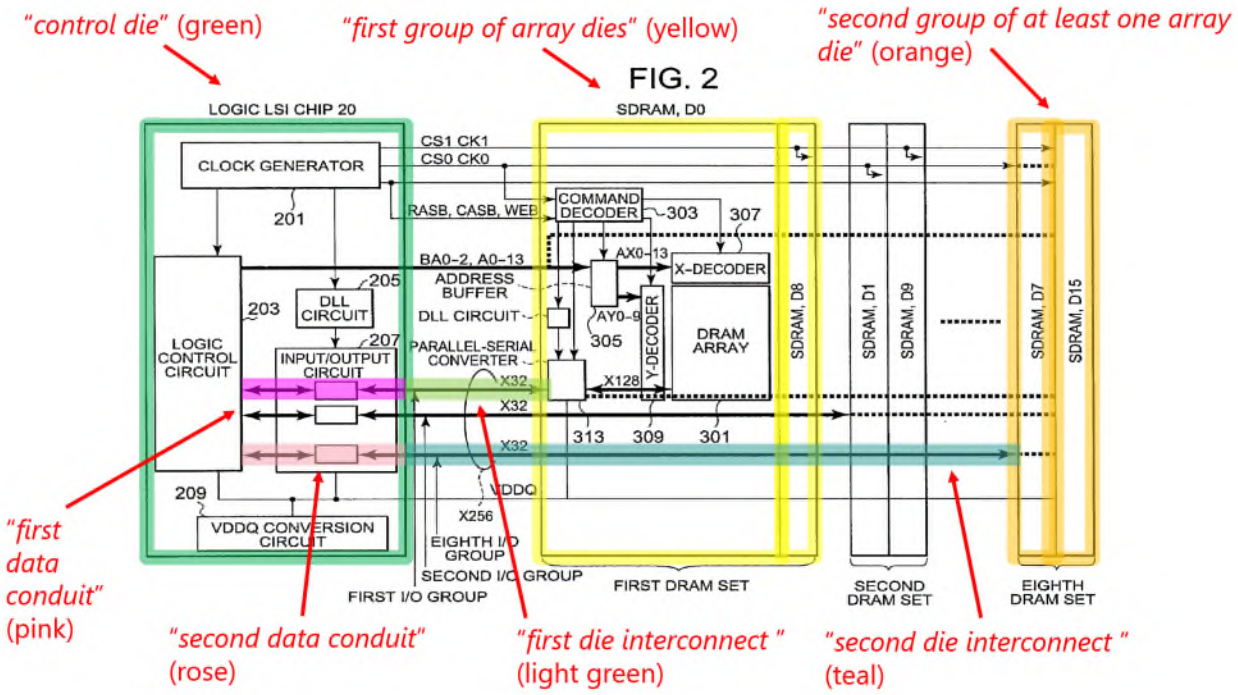
FIG. 4

758. A Skilled Artisan would have understood from this disclosure that the control chip 20 of Riho includes a "*first data conduit*" (pink) including a portion of the input/output circuit 207 that is connected to the data signal DQ TSV08 ("*the first die interconnect*"), on one hand, and to a corresponding external data terminal of the control chip 20 ("*a first terminal*") through which the corresponding data is transmitted, on the other hand. *See, e.g.*, Ex. 1016 (Riho) at Fig. 2 (reproduced below, annotated).



759. Therefore, Riho discloses "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*" to a Skilled Artisan.

760. Riho alone or in combination with Rajan discloses to a Skilled Artisan "*at least a second data conduit* [(rose)] *between the second die interconnect* [DQ TSV715 (teal)] *and the first terminal, the first terminal being a data terminal* [e.g., an external data terminal of the control chip 20]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



761. For example, as discussed above with reference to the "*first data conduit*," Riho discloses that "[t]he logic control circuit 203 provided in the logic LSI chip 20 … sends and receives data signals DQ between itself and the input/output circuit 207." *Id.* at [0039]. Riho also discloses that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total." *Id.* at [0040]. Riho further discloses that the input/output circuit 207 transmits or receives the data signal DQ "as an I/O data signal," and that each DRAM set is allocated with a respective I/O group (×32 DQ signal bits) for a total of eight I/O groups. *Id.*; *see also id.* at [0046] ("The data signal DQ TSVs for the SDRAM D7 are provided between the

input/output circuit 207 of the logic LSI chip 20 and the SDRAM D7. The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15.").

762. As also discussed above with reference to the "*first data conduit*" (pink), a Skilled Artisan would have understood from Riho's disclosure that the control chip 20 includes a "*second data conduit*" (rose) including a portion of the input/output circuit 207 that is connected to the data signal DQ TSV715 ("*the second die interconnect*"), on one hand, and to a corresponding external data terminal of the control chip 20 through which the corresponding data is transmitted, on the other hand.

763. The claim also requires that the "*second data conduit*" is coupled to the same "*first terminal*" as the "*first data conduit*." Such an arrangement of external data terminals in the control chip of Riho would have been obvious to a Skilled Artisan in view Rajan. *See, e.g.*, *supra* ¶¶138-140 (rank multiplication), 683-692 (obviousness of combining Rajan and Riho, including emulating different number of ranks). For example, a Skilled Artisan would have been motivated to implement a 32-bit wide or narrower JEDEC compatible external data interface as suggested by Rajan in the control chip of Riho to make Riho's stacked memory chip compatible with the corresponding JEDEC standard. *See, e.g.*, Ex. 1015 (Rajan) at 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC

standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."), 3:52-54 ("The interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory."); *see also id.* at Fig. 18 (reproduced below, disclosing that an interface circuit includes emulation logic which interfaces with the host system on one side and with the physical memory circuits on the other side, similar to Riho's logic control circuit 203, illustrated above).

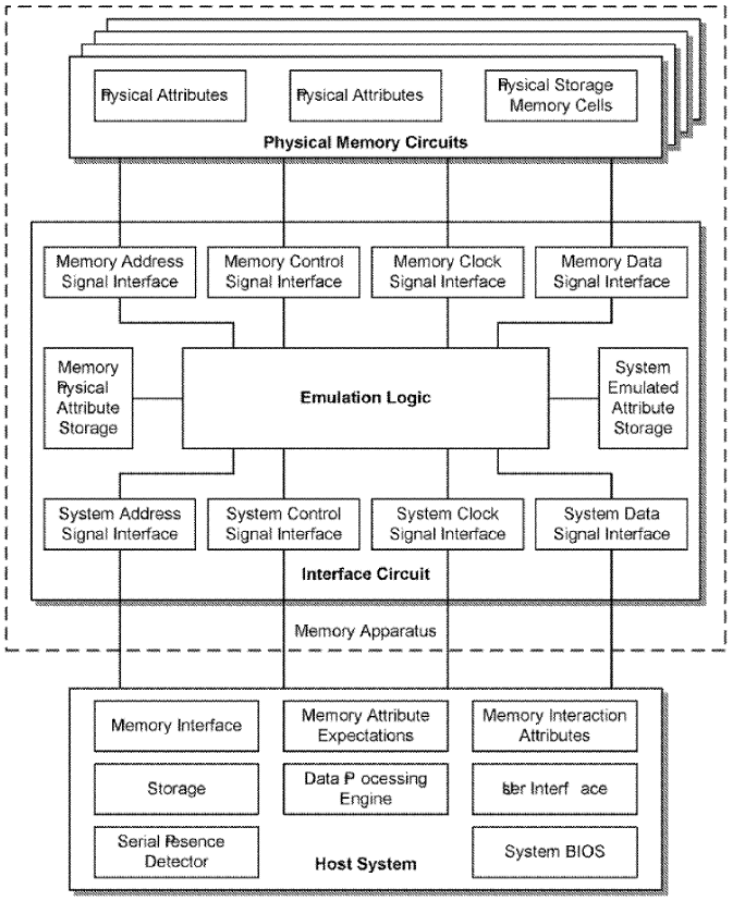


FIG. 18

764. For the reasons discussed above, a Skilled Artisan would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system. *Supra* ¶¶683-692. Rajan discloses the same basic structure of a memory package as Riho and the 060 Patent: the package includes stacked memory chips and a common interface circuit, called "buffer chip" in Rajan. Ex. 1015 at Fig. 4 (reproduced below, annotated), 2:6-7 ("FIG. 4 shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses.").

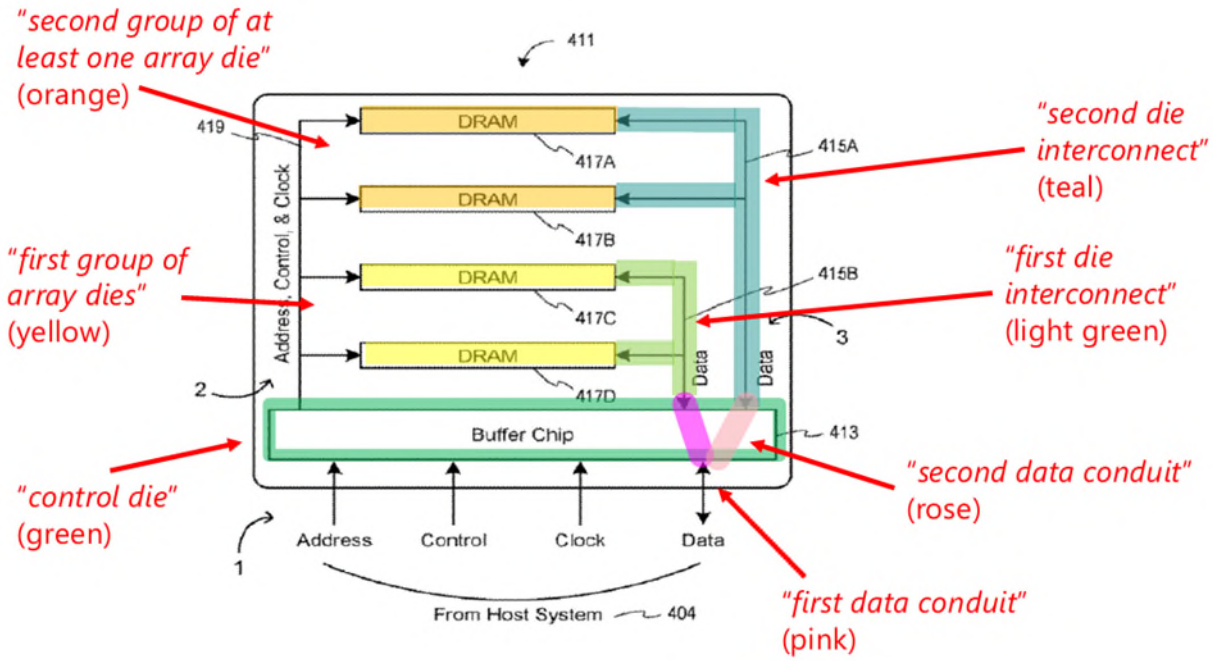


FIG. 4

765. Rajan describes that "the buffer chip 413 is interfaced to a host system 404," including address, control, and data signals. Ex. 1015 (Rajan) at 5:36-43, Fig. 4 (reproduced above, annotated). Rajan also discloses that the

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interface may comply with JEDEC standards. *See id.* at 4:20-24 ("The interface circuit may take the form of or incorporate, or be incorporated into, a register, an AMB, a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities."), 8:8-11 ("Behavior of many DRAM circuits is specified by the JEDEC standards, and it may be desirable to exactly emulate a particular JEDEC standard DRAM."). A Skilled Artisan would have understood that a JEDEC standard interface includes terminals for address, control, and data signals. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Fig. 3 describing package pinout for stacked DDR3 memories, including terminals DQ0-15 for x16 data signals, and terminals for control/address signals, including RAS, CAS, WE, An, and BAn), Fig. 3 (reproduced below); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35.

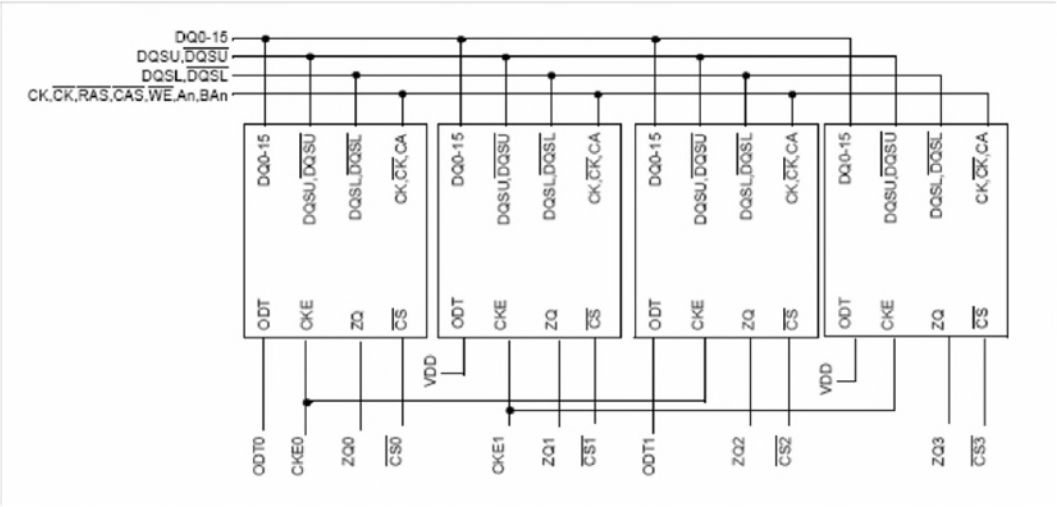


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

766. As discussed above, a Skilled Artisan would have been motivated to follow Rajan's suggestion and implement address, control and data terminals according to the JEDEC standards in Riho's memory packages to use the packages in JEDEC compliant systems. *Supra* ¶¶683-692. For example, Rajan teaches that the "interface circuit may present to the system device an emulated interface to e.g. DDR3 memory, while the physical memory chips are, in fact, DDR2 memory." Ex. 1015 at 3:52-54. A Skilled Artisan would have understood that a DDR3 SDRAM memory interface can include 4, 8, or 16 data terminals, and a GDDR4 memory can include 32 data terminals. *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.12-14 (describing pin-out for stacked DDR3 memory devices, Fig. 3 for x16 devices reproduced above); *see also* Ex. 1035 (JEDEC GDDR4 SGRAM Specification) at 2 ("The purpose of this Specification is to define the minimum set of requirements for JEDEC standard compatible 256 Mb through 1 Gb x32 GDDR4 SGRAM devices."). Making such a combination would have been well within the level of skill at the time, since emulating a standard JEDEC interface was known for years, as evidenced by Rajan and as also demonstrated by the prior art referenced in the 060 Patent. *See, e.g.*, Ex. 1001 (the 060 Patent) at 22:37-39 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537 …."); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537).

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767. A Skilled Artisan would have understood that, in the combination of Riho and Rajan, where the memory package has, e.g., 32 external data terminals, those external data terminals would be connected to "[e]ach input/output circuit 207 [which] sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15." Ex. 1016 (Riho) at [0040]. That is, because the internal data communication between a given memory chip and the control chip happens on 32 parallel TSVs, those TSVs of each memory chip would be connected to the external 32 data terminals in order to communicate the data on the 32 data signal DQ TSVs.

768. Therefore, the combination of Riho and Rajan at least renders obvious that that the "*second data conduit*" is coupled to the same "*first terminal*" as the "*first data conduit*."

769. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal*."

(3) [1.e.4] Control Circuit

770. Claim 1 requires "*the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in*

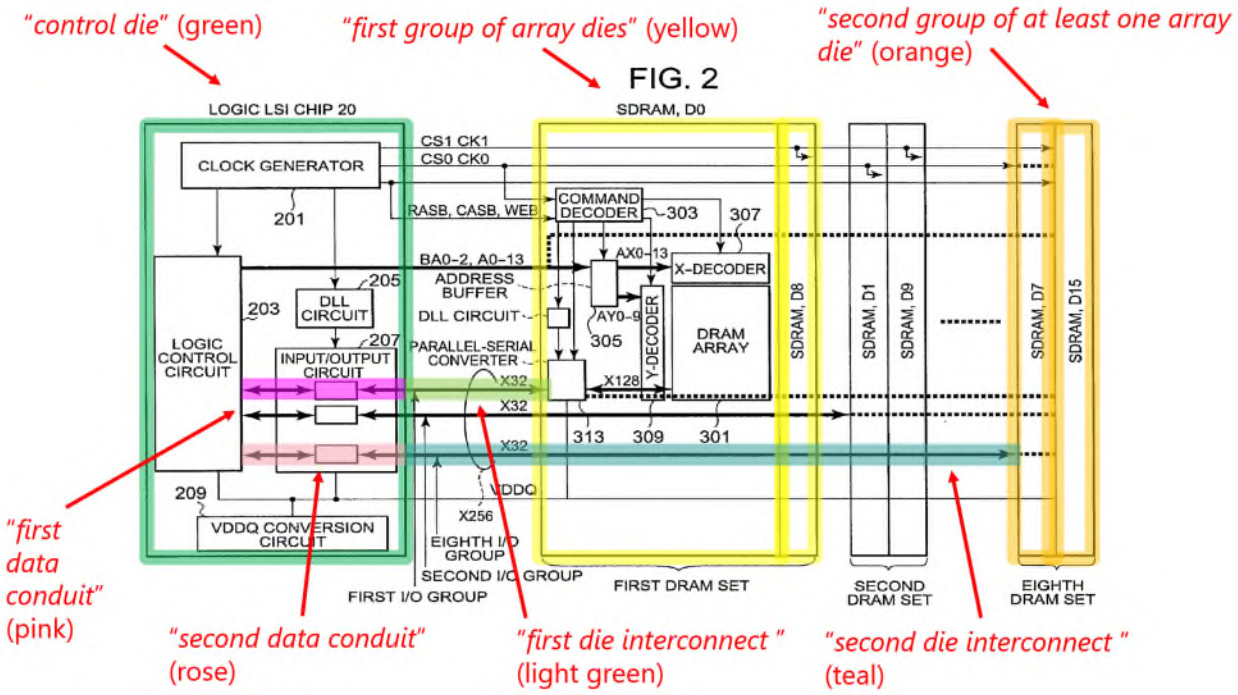
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response to control signals received via one or more second terminals of the plurality of terminals."

771. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

772. Riho discloses, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, that "*the control die* [control chip 20] *further* [comprises] *a control circuit* [including logic control circuit 203 and control circuit in input/output circuit 207] *to control respective states* [for communicating data in the read or write direction] *of the first data conduit* [(pink) to SDRAMs D0 and D8 through DQ TSV08] *and the second data conduit* [(rose) to SDRAMs D7 and D15 through DQ TSV715] *in response to control signals* [including read and write command signals] *received via one or more second terminals of the plurality of terminals* [from an external device]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).

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773. As discussed above, Riho discloses external terminals of its logic chip 20 and it would have been obvious at least in light of Rajan to have those external terminals receive address and control signals and control the memory chips in the stack based on those signals. *Supra* at ¶¶683-692. For example, Riho discloses that the "logic control circuit 203 provided in the logic LSI chip 20 outputs a 3-bit bank address signal BA0-2 and a 14-bit address signal A0-13 and operates as a controller that sends and receives data signals DQ between itself and the input/output circuit 207." Ex. 1016 at [0039]. The input/output circuit 207 "sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively." *Id.* at [0040]. Moreover, the input/output circuit 207 "includes interface circuits such as buffers corresponding to the SDRAM chips, respectively,

so that data signals DQ are sent and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit." *Id.* at [0045]. Riho further discloses that the "communications (read/write) of respective I/O groups are performed between the first control chip [i.e., logic LSI chip 20] and the second and third controlled chips [i.e., SDRAM chips]." *Id*. at [0053]; *see also* Ex. 1015 at 11:12-12:13, Fig. 14 (reproduced below, disclosing timing for forwarding commands to the memory devices during read and write operations); Ex. 1019 at 13, 23-24 ("CAS latency"), 33.

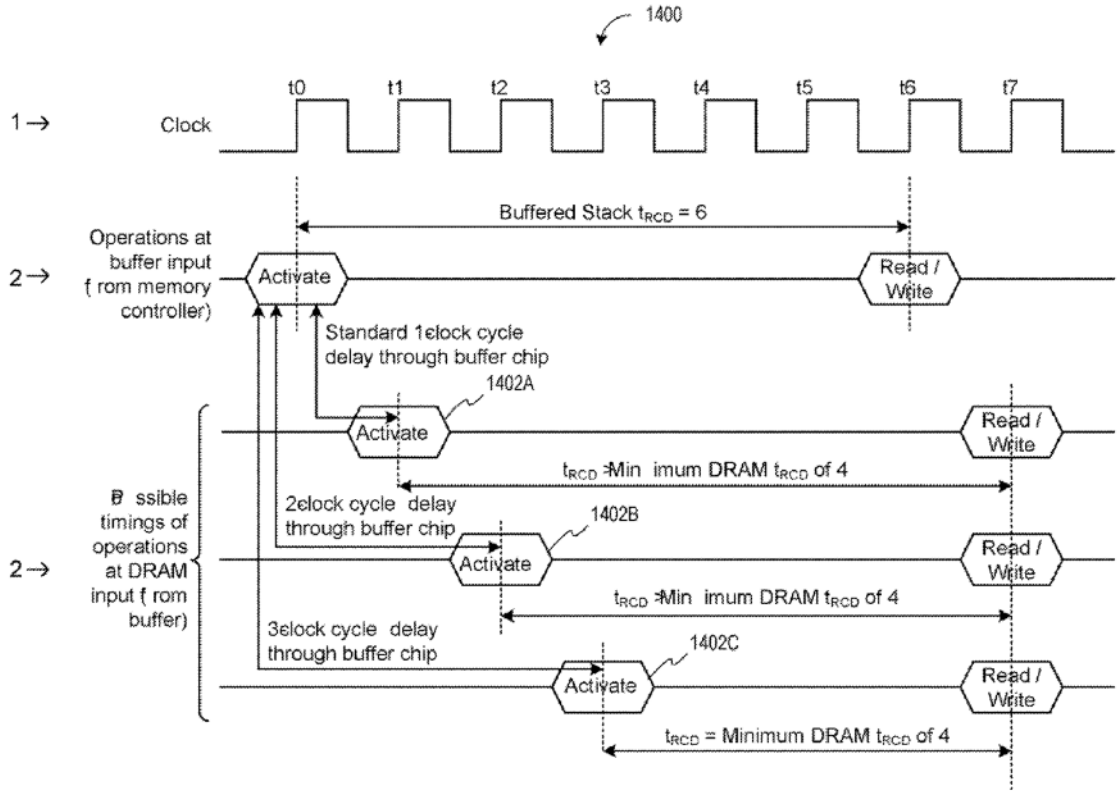


FIG. 14

774. A Skilled Artisan would have understood from this disclosure that the logic control circuit 203 and logic circuitry in input/output circuit 207 include a

control circuit that receives control signals, including read and write command signals from an external device and, in response, controls the timing and direction of data transfer through the input/output circuit 207 to direct the data transfer selectively to or from DQ TSV08 through the "*first data conduit*" (pink) and to or from DQ TSV715 through the "*second data conduit*" (rose). Therefore, the state of those "*data conduits*" is controlled to be active or not active and to transmit data in the read or write direction.

775. As discussed above with reference to claim limitation [1.b], a Skilled Artisan would have understood that the read and write command signals are "*received via one or more second terminals of the plurality of terminals*." *Supra* ¶¶711-718.

776. Furthermore, in the combination of Riho and Rajan, the "*control circuit*" may emulate one or more characteristics, such as the number of ranks (e.g., to implement rank multiplication), that are different from the characteristics of the physical memory devices on the memory module. *Supra* at ¶¶138-140, 683-692.

777. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

778. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*the control die further comprising a control circuit to control respective*

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states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."

2. Claim 2 is Unpatentable

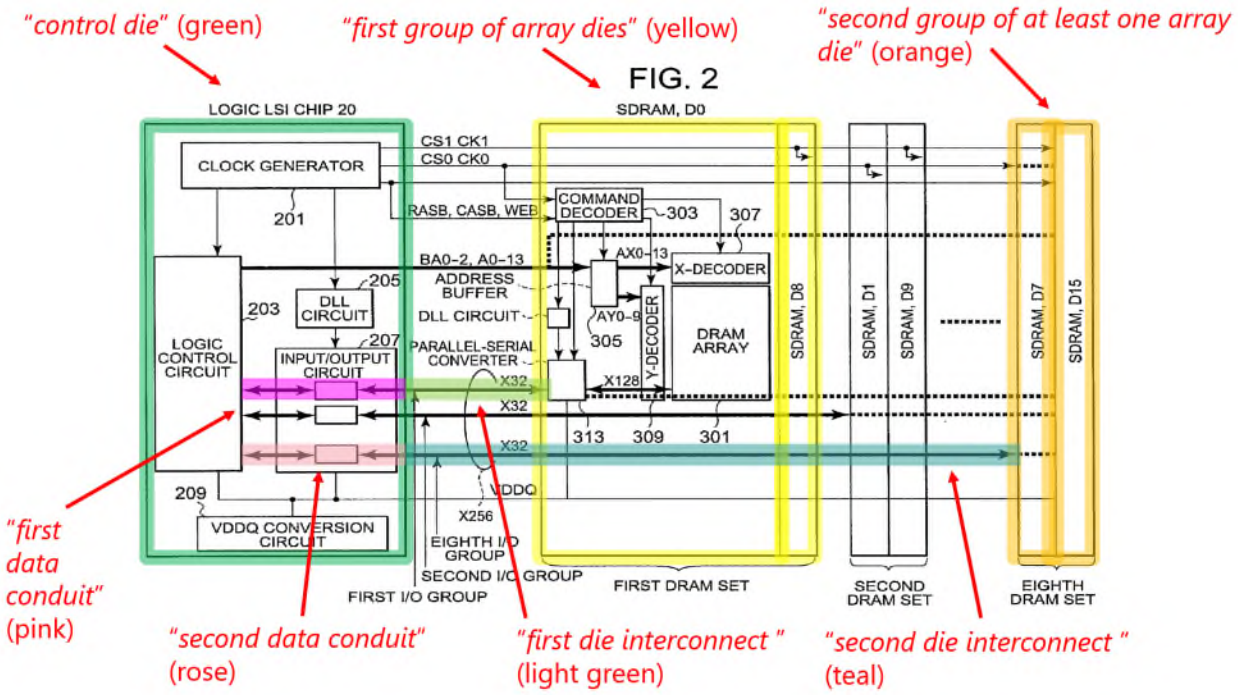
779. Claim 2 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

780. Claim 2 requires "*[t]he memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits*."

781. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

782. As discussed above, Riho discloses external terminals of its logic chip 20 and it would have been obvious at least in light of Rajan to have those external terminals receive address and control signals and control the memory chips in the stack based on those signals. *Supra* at ¶¶683-692. Riho also discloses to a Skilled Artisan, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, that "*the control signals* [from the external device] *include data path control signals* [such as read and write command signals, including chip select signals,] *for controlling the first* [(pink)] *and second* [(rose)] *data conduits* [including controlling the timing and direction of the data transfer (read or write)

and selecting the die(s) for the data transfer (in accordance with the chip select signals)]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



783. For the reasons discussed above with reference to claim limitation [1.e.4], Riho's logic control circuit 203 and input/output circuit 207 include a control circuit that receives read and write commands from an external device and, in response, controls the direction and timing of the data transfer to or from DQ TSV08 through the "*first data conduit*" (pink) or to or from DQ TSV715 through the "*second data conduit*" (rose). *Supra* ¶¶770-778. A Skilled Artisan would have understood that the read and write command signals are "*data path control signals*," at least under Netlist's apparent interpretation, because they determine the direction and timing of the data transfer (read or write). *See, e.g.*, Ex. 1001 (the

060 Patent) at 19:31-34 ("The data path control circuit (e.g., ODT, read/write data direction)….").

784. Furthermore, in the combination of Riho and Rajan, the memory module can implement rank multiplication. *Supra* at ¶¶138-141, 683-692. For example, the register of the module can generate additional chip select signals and provide those to the stacked memory package. *Id*. Alternatively or in addition, the "*control circuit*" in the memory package may also implement rank multiplication. *Id*. at ¶141.

785. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

786. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the control signals include data path control signals for controlling the first and second data conduits*" limitation.

3. Claim 3 is Unpatentable

787. Claim 3 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

788. Claim 3 requires "*[t]he memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.*"

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789. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

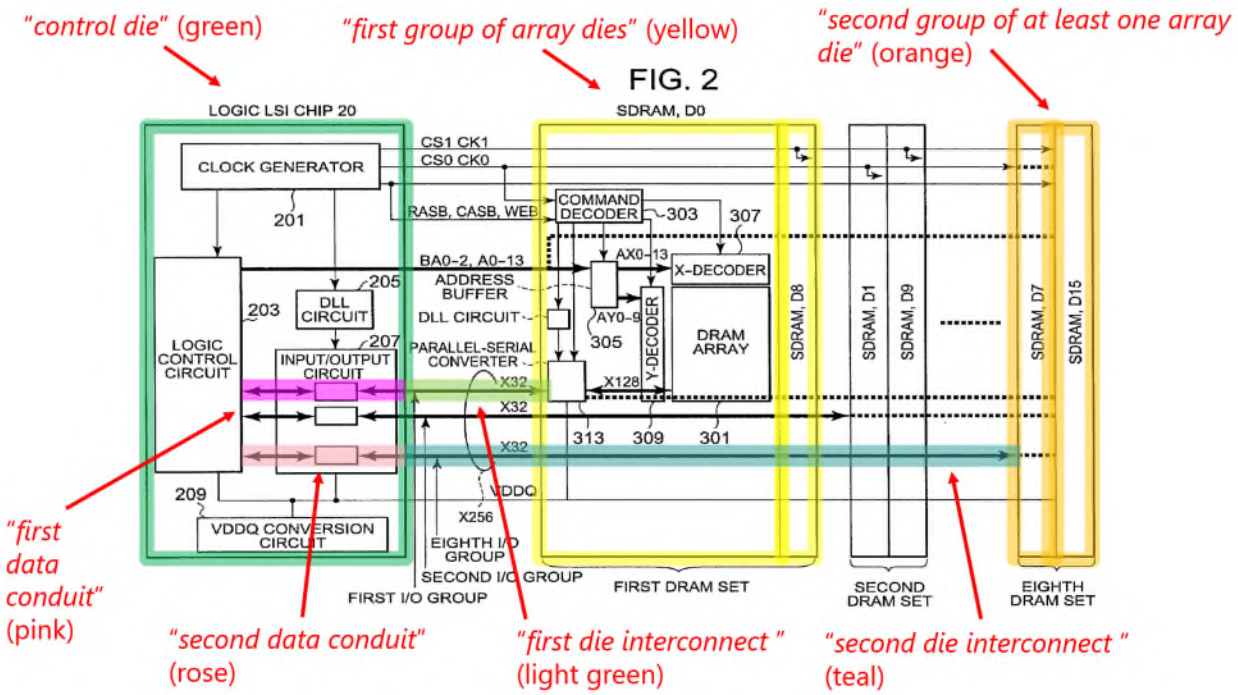
790. Riho discloses and, in view of Rajan, renders obvious to a Skilled Artisan, that "*the control circuit* [including logic control circuit 203 and control circuit in input/output circuit 207] *is configured to generate data path control signals* [including internal write and read signals] *for controlling the first and second data conduits* [to or from DQ TSV08 and DQ TSV715] *in response to the received control signals*."

791. For example, Riho discloses that the "logic control circuit 203 provided in the logic LSI chip 20 outputs a 3-bit bank address signal BA0-2 and a 14-bit address signal A0-13 and operates as a controller that sends and receives data signals DQ between itself and the input/output circuit 207." Ex. 1016 at [0039].

792. A Skilled Artisan would have understood that, in order to send and receive data through the input/output circuit 207 with the timing required for reading or writing the SDRAMs in the stack, the control circuit has to generate internal signals with the proper timing, and such signals are, at least under Netlist's apparent interpretation, Ex. 1044 at 63-68; Ex. 1046 at 63-69, "*data path control signals for controlling the first and second data conduits in response to the received control signals*" because the generated internal signals control the

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direction of the data transfer (read or write), select the data conduits and the corresponding die(s) for the read or write operation and determine the timing for the data transfer through the data conduits. *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



793. Furthermore, as discussed above, it would have been obvious to a Skilled Artisan to combine the stacked memory devices of Riho with the interface emulation of Rajan. *Supra* ¶¶683-692.

794. For example, Rajan explains that "[a]n example of an emulated protocol characteristic might be a timing, or a specific protocol such as DDR3. … The interface circuit may emulate the number of signals, type of signals, duration of signal assertion, and so forth." Ex. 1015 at 3:42-50. Rajan also discloses the

example of "FIG. 10 [which] is a timing diagram illustrating a timing design 1000 of write data timing expected by a DRAM circuit in a buffered stack. Emulation of a larger capacity DRAM circuit having higher CAS latency (as in FIG. 9) may, in some implementations, create a problem with the timing of write operations. For example, with respect to a buffered stack of DDR2 SDRAM chips with a read CAS latency of four clocks which are used in emulating a single larger DDR2 SDRAM with a read CAS latency of six clocks, the DDR2 SDRAM protocol may specify that the write CAS latency 1002 is one less than the read CAS latency. Therefore, since the buffered stack appears as a DDR2 SDRAM with a read CAS latency of six clocks, the memory controller may use a buffered stack write CAS latency of five clocks 1004 when scheduling a write operation to the memory." Ex. 1015 at 9:46-60, Fig. 10 (reproduced below); *see also* Ex. 1019, at 23-24 ("CAS latency").

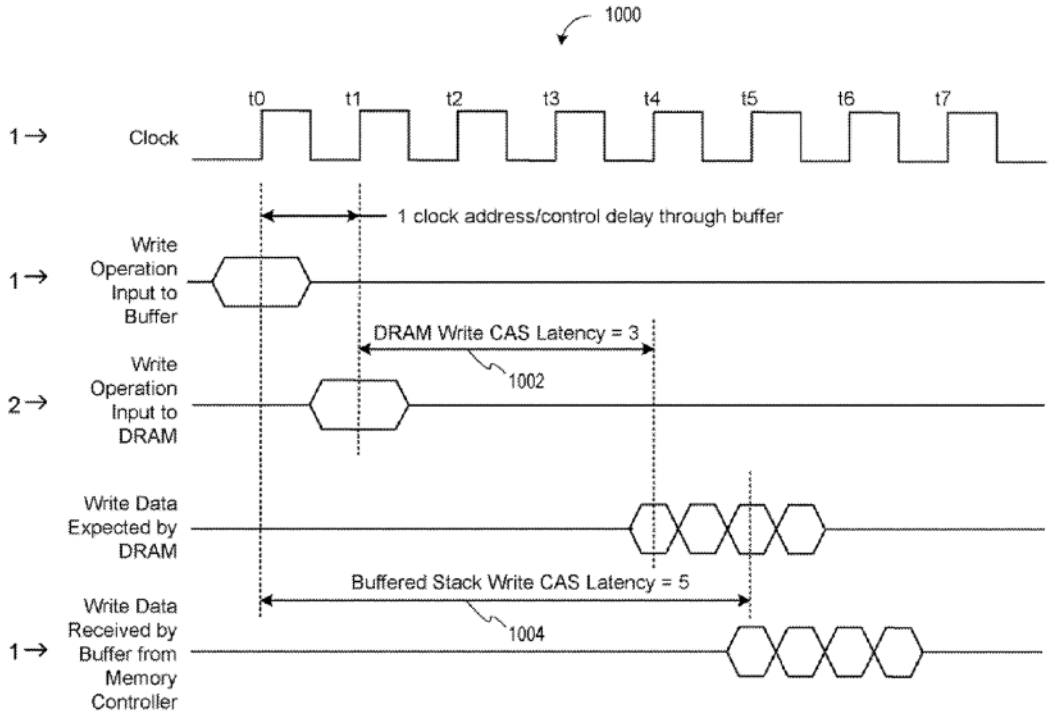


FIG. 10

795. Furthermore, the combination of Riho and Rajan renders obvious to a Skilled Artisan to generate the chip selection and other control signals and the corresponding read and write commands according to the characteristics of the physical memory dies, while the memory package emulates a different number of more memory devices with different characteristics. *Supra* at ¶¶150-168; *see, e.g.,* Ex. 1015 (Rajan) at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). For example, the interface circuit can generate additional chip select signals for rank multiplication. *Supra* at ¶¶138-141; *see, e.g.,* Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips

in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack."). In such an implementation, the control chip would also generate internal signals, including chip select signals, to select the die(s) which perform the read or write operation and the corresponding data path(s) for the data transfer.

796. A Skilled Artisan would have understood from this disclosure that, when emulating an interface, Rajan's emulation logic generates the corresponding control signals, including data path control signals. *See, e.g.*, Ex. 1015 at Fig. 18 (reproduced below).

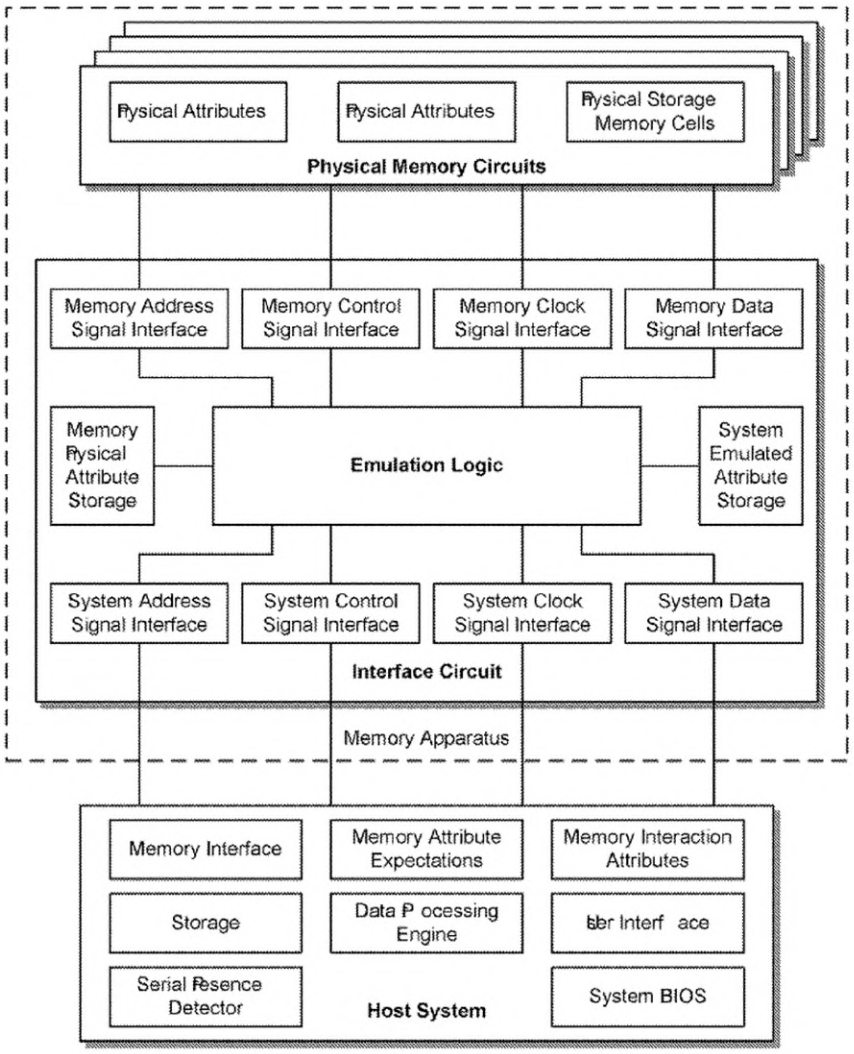


FIG. 18

797. Therefore, Riho discloses and, in combination with Rajan, renders obvious this limitation to a Skilled Artisan.

798. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals*" limitation.

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4. Claim 4 is Unpatentable

799. Claim 4 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

a) [4.a] Command/Address Signals

800. Claim 4 requires "*[t]he memory package of claim 3, wherein the control signals include command/address signals*."

801. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

802. Riho at least in view of Rajan renders obvious to a Skilled Artisan that read and write commands include chip-select signals and address signals identifying where to store or retrieve the data, as discussed above with referenced to claim limitation [1.b] and in light of the JEDEC standards. *Supra* ¶¶711-718 (claim limitation [1.b]); Ex. 1015 at Figs. 4 and 18 (reproduced below, annotated); Ex. 1019 at pp.6-14 (describing package pinout for stacked DDR3 memories, including chip select terminals CSn#, command terminals RAS#, CAS# and WE#, and address signal terminals A0-A15), p.18 (describing read and write operations beginning with an Active command with a row address followed by a Read or Write command selecting a starting column address in that row), p.33 (Command Truth Table describing an Activate command with a row address, RA, and Read

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and Write commands with corresponding column address, CA); Ex. 1023 at p.9 & Fig.16; Ex. 1022 at pp. 318-20, 332-35.

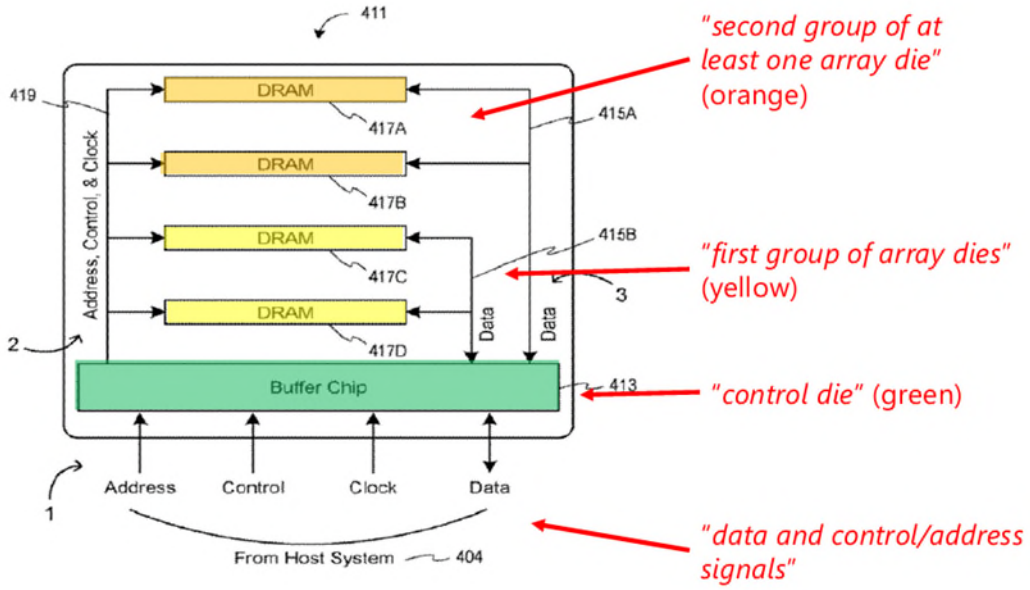


FIG. 4

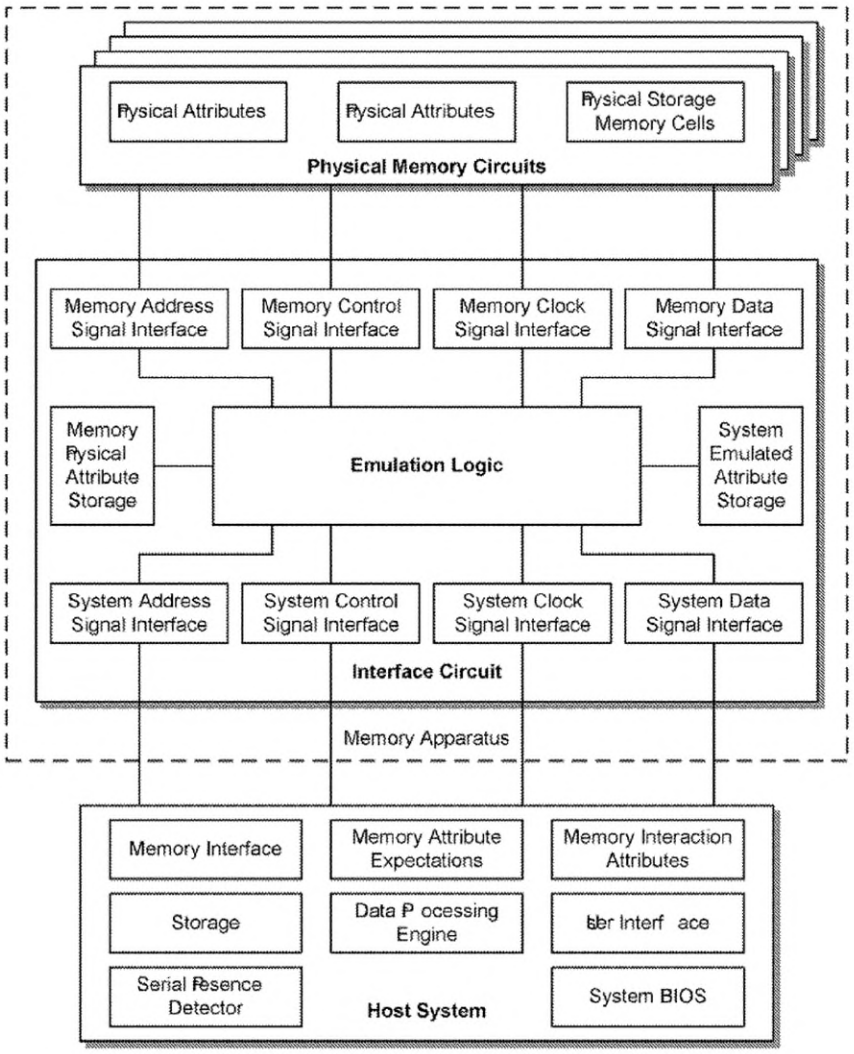


FIG. 18

803. Therefore, Riho at least in view of Rajan renders obvious this limitation to a Skilled Artisan.

804. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory package of claim 3, wherein the control signals include command/address signals*."

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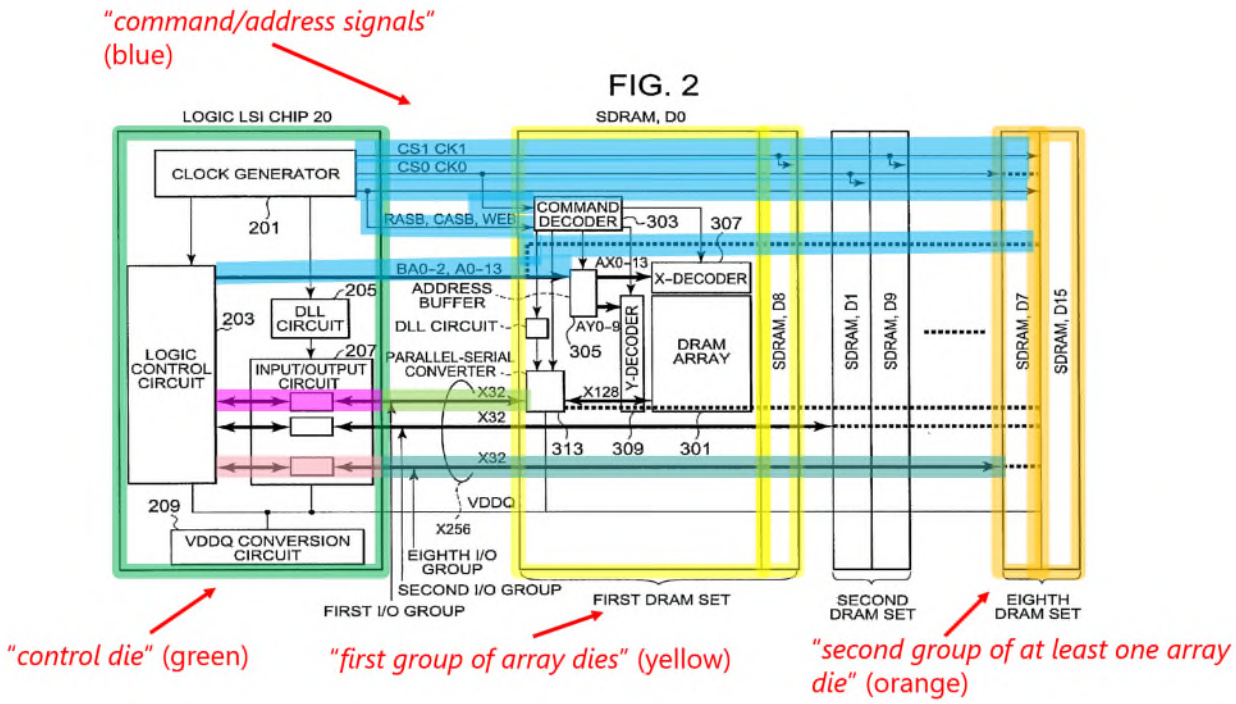
b) [4.b] Control Die Configured to Provide Command/Address Signals to Stacked Array Dies

805. Claim 4 also requires "*wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.*"

806. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

807. Riho discloses to a Skilled Artisan that "*the control die* [logic LSI chip 20] *is configured to provide the command/address signals* [including CS0CK0, CS1CK1, RASB, CASB, WEB, BA0-2, A0-13 (annotated blue in the figure below)] *to the plurality of stacked array dies* [D0-D15]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated), [0038] ("The first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs."), [0043] ("The 3-bit bank address signal BA0-2 and the 14-bit address signal A0-13 are supplied to all the SDRAMs D0 to D15 through the address TSVs.").

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808. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], a Skilled Artisan would have been motivated to provide these command and address signals to the memory chips because they were standard signals used to control SDRAMs. *Supra* ¶¶727-744.

809. Therefore, Riho discloses this limitation to a Skilled Artisan

810. Therefore, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies*."

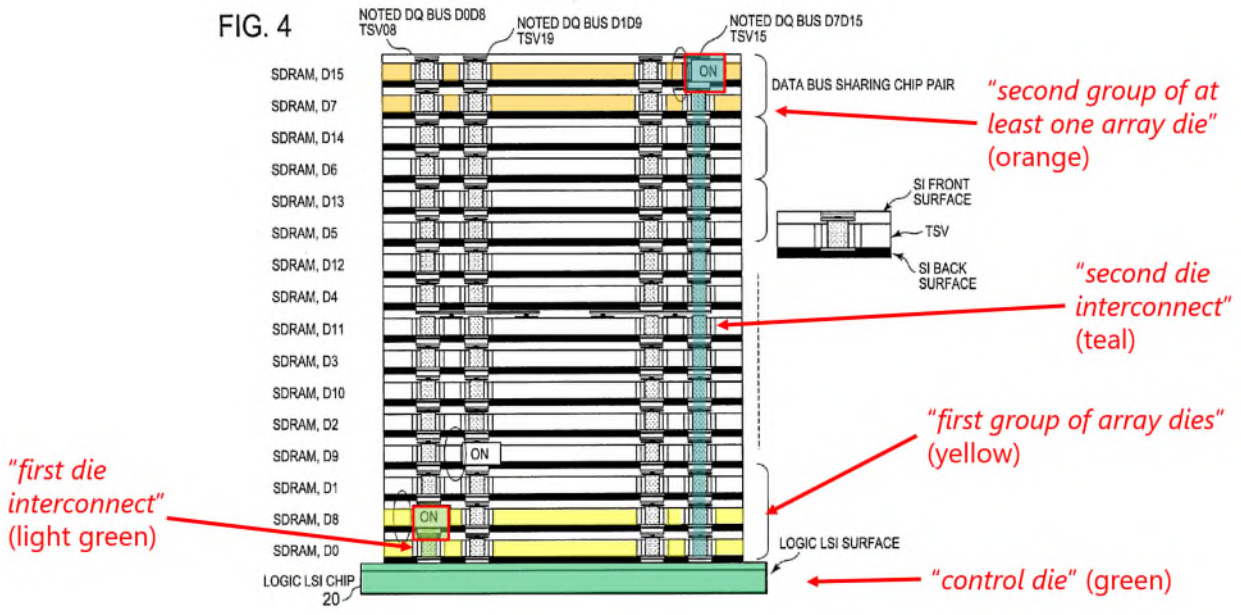
5. Claim 5 is Unpatentable

811. Claim 5 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

812. Claim 5 requires *"[t]he memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via*."

813. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

814. Riho discloses that "*the first die interconnect comprises a first through-silicon via* [TSV08] *and wherein the second die interconnect comprises a second through-silicon via* [TSV715]." *See, e.g.*, Ex. 1016 at [0030, 0063-64] and Fig. 4 (reproduced below, annotated).



815. Therefore, Riho discloses this limitation.

816. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first die interconnect comprises a first through-silicon via*

and wherein the second die interconnect comprises a second through-silicon via" limitation.

6. Claim 6 is Unpatentable

817. Claim 6 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

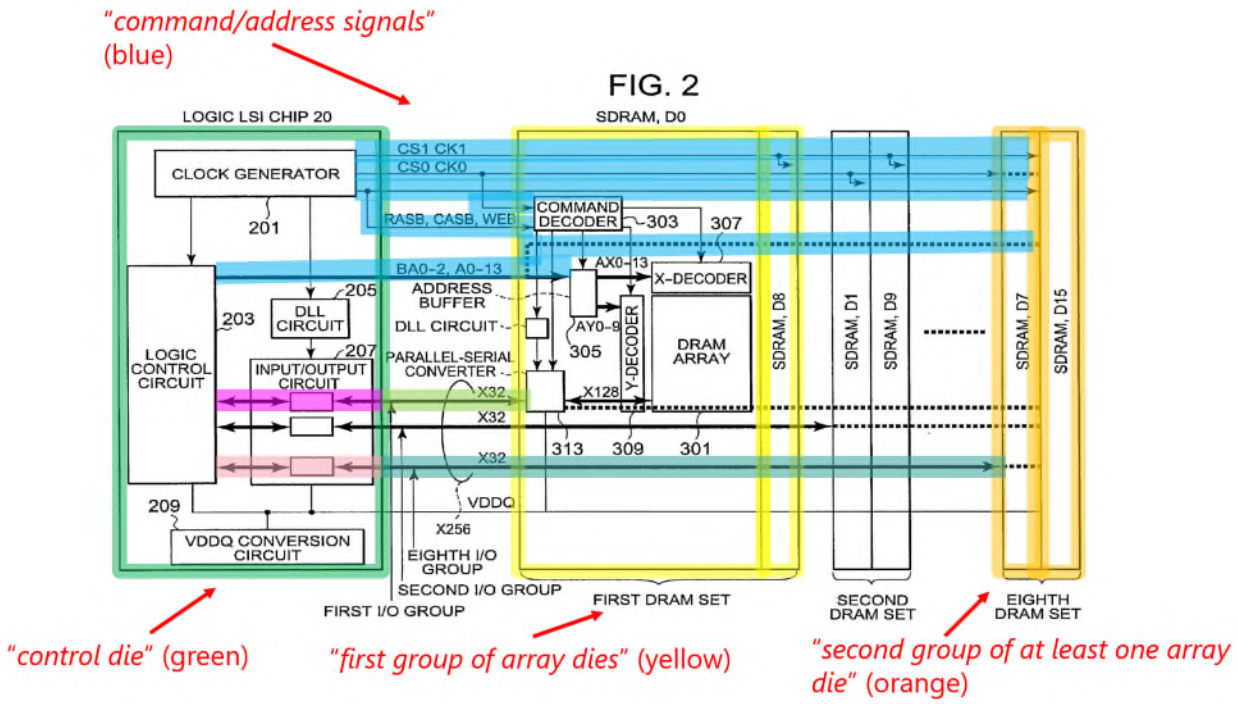
a) [6.a] Chip-Select Conduits

818. Claim 6 requires "*[t]he memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising*."

819. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

820. Riho discloses and, in view of Rajan, renders obvious that "*the control die* [control chip 20] *further comprises chip-select conduits* [for conducting chip selection signals like CS0CK0 and CS1CK1]." *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated, showing that chip selection signals CS0CK0 and CS1CK1, blue, are output by clock generator 201 on the control chip 20).

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See also the analysis for claim 12 (explaining that the chip select signal is received at the bottom surface of the control chip and provided to the top surface), *infra* at ¶¶929-935.

821. For example, Riho discloses that, "[o]f the two groups (chip selection groups), the first group (first controlled chips) is communication-controlled at a first access cycle by the first chip selection signal (first clock signal CS0CK0) output from the control chip 20 while the second group (second controlled chips) is communication-controlled at a second access cycle by the second chip selection signal (second clock signal CS1CK1) output from the control chip 20." Ex. 1016 at [0033].

822. A Skilled Artisan would have understood from Riho's disclosure that the control chip 20 includes "*chip-select conduits*" to conduct the chip selection signals CS0CK0 and CS1CK1 as shown above.

823. Furthermore, a Skilled Artisan would have understood that, in the combination of Riho and Rajan, the emulation logic of Rajan generated the chip selection signals as required for the specific emulation, and the chip select conduits of Riho's control chip were used to send those chip selection signals to the corresponding through-silicon vias. *See, e.g.*, Ex. 1015 at 7:12-19 ("During a row operation, the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals, and are stored for later reuse. And during a subsequent column operation, the stored bits are again used to generate the four DRAM chip select signals."). For example, Rajan discloses that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." Ex. 1015 at 6:34-38. This use of the chip select signal for selecting an SDRAM in a stack was well known at the time. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.12 (Figs. 1-3 showing stacked DDR3 chips, each receiving a separate chip select signal), p.13 (explaining that chip select provides rank selection), Fig. 2 (reproduced below, annotated).

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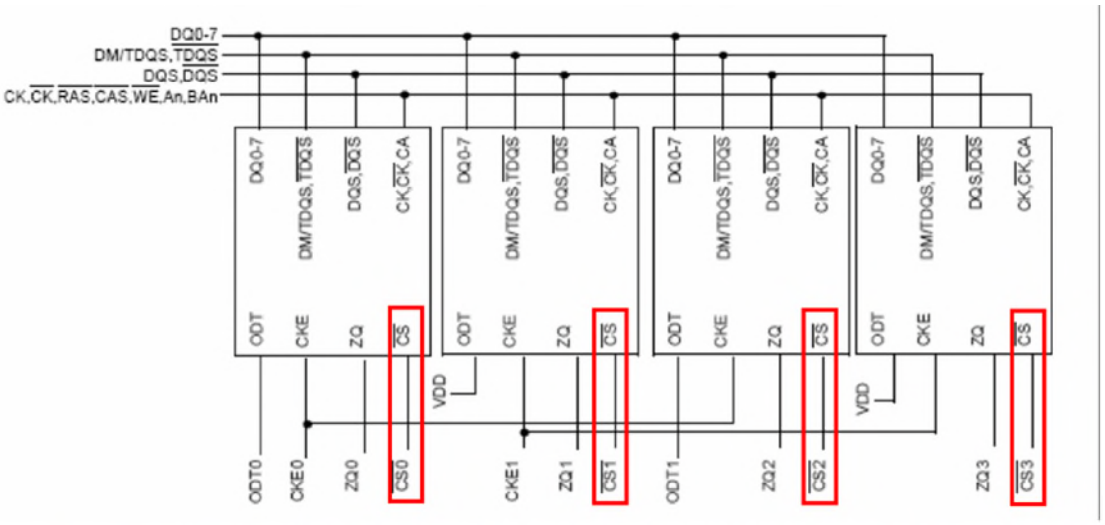


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

See also Ex. 1022 (Jacob et al.) at 318-321 (explaining the operation of chip select signals and stating the "chip-select bus … is essential in a JEDEC style memory system") and Ex. 1023 (Jacob) at pp.2-4, 9 & Fig.16 (same).

824. Furthermore, as discussed above, a Skilled Artisan would have understood that the chip select signals would have been driven to off-chip circuits, such as the memory dies in the stack. *Supra* at ¶¶135-137. Therefore, a Skilled Artisan would have understood, and been motivated, to include drivers in the "chip-select conduits" in order to transmit the chip select signal properly to the respective dies. *Id*.

825. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

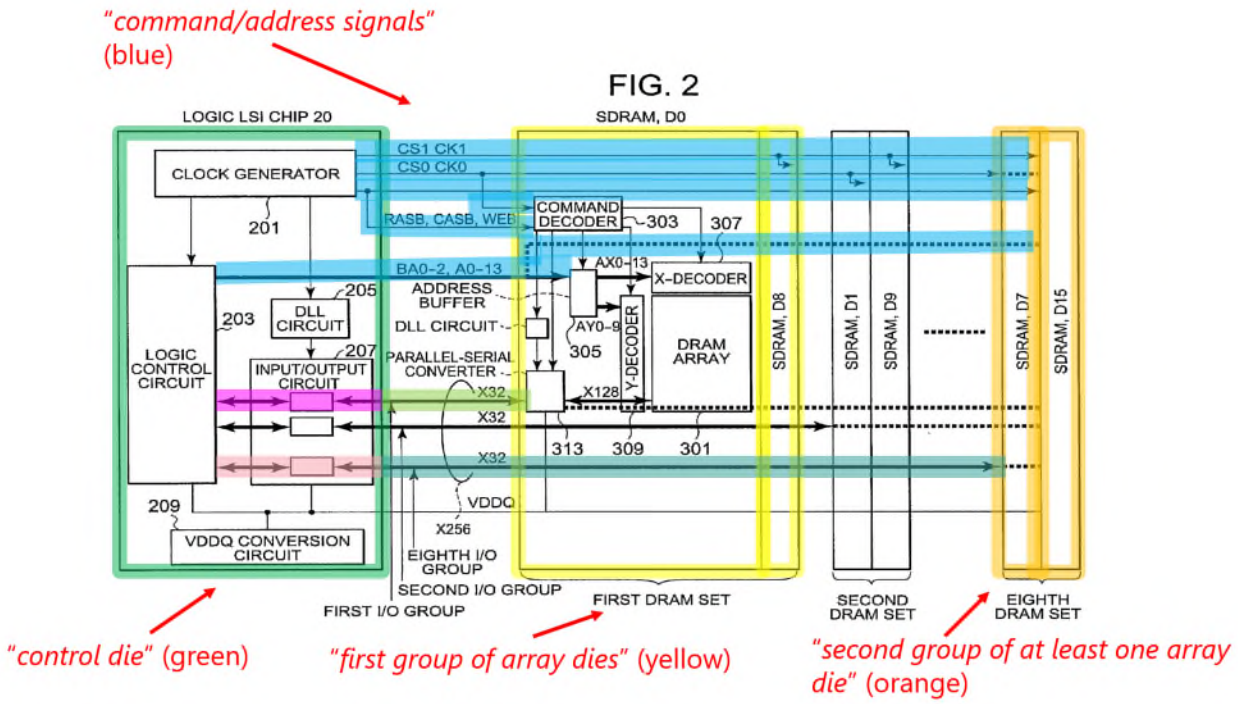
826. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the control die further comprises chip-select conduits, the memory package further comprising*" limitation.

b) [6.b] Third Die Interconnects

827. Claim 6 also requires "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies*."

828. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

829. Riho discloses "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.*" For example, Riho disclose that "[t]he first and second clock signals CS0CK0 and CS1CK1 are supplied to the SDRAMs D0 to D15 through the clock TSVs while the command signals are supplied to the SDRAMs D0 to D15 through the command TSVs." Ex. 1016 at [0038]; *see, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated, showing that chip selection signals CS0CK0 and CS1CK1, blue, are transmitted from the control chip die 20 to the SDRAM chip dies in the stack).



830. The prior art described in the 060 Patent, specifically Figs. 1A and 1B, demonstrate that transmitting separate chip select signals through die interconnects to select a chip in the stack was well known at the time. *See* Ex. 1001 at Figs. 1A, 1B (showing die interconnects for chip select signals), 1:49-56 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.").

831. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

832. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies*" limitation.

7. Claim 7 is Unpatentable

833. Claim 7 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

a) [7.a] Selecting A First and Second Number of Array Dies Based on Load of Die Interconnects

834. Claim 7 requires *"[t]he memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit*." As discussed above, I understand that claim 7 may improperly mix a method claim with an apparatus claim, but I do not believe this issue needs to be resolved for purposes of my invalidity analysis below, because regardless of whether claim 7 is interpreted as an apparatus claim or a mixed apparatus and method claim, in my opinion it is obvious in light of the prior art as discussed below. *See supra* ¶ 113.

835. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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836. Riho discloses to a Skilled Artisan that "*a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit.*"

837. As discussed above with reference to claim limitations [1.b] and [1.c], Riho discloses that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 at [0103]; *supra* ¶¶711-726. Riho explains the advantages in the write operation as follows: "The load capacitance to 256 data signals DQ is reduced by half. Accordingly, the operating current is reduced and the high-frequency operation is achieved. Further, load capacitance variations of the data buses caused by a capacitance variation of (2±0.5) pF possessed by each DQ pin are also reduced. Therefore, SDRAM input set-up and hold margin are increased." Ex. 1016 at [0119]. Likewise, Riho explains the advantages in the read operation: "Since the DQ load on the SDRAM chip side of the 256 data buses is reduced by half, the operating current is reduced and the high-frequency operation

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is achieved. It is also possible to remove capacitance variations of the data buses. It is possible to remove interference due to a reflected wave caused by L1 of the SDRAM D15. Logic LSI chip input set-up and hold margin are increased." *Id.* at [0120].

838. Riho further explains that, "since the data signal DQ and data strobe signal DQS/B TSVs for all the DRAM sets corresponding to the respective I/O groups can be made substantially equal in length to each other, the skew between data signals DQ and data strobe signals DQS/B can be minimized. This structure (equi-length interconnections) is very important in the stacked structure in which the plurality of DRAM sets are stacked in sequence with respect to the controller chip." Ex. 1016 at [0050]. Riho describes that "in this embodiment, each I/O group is formed by ×32 DQ signal bits and the controller chip can perform communication control of the plurality of I/O groups (×256 DQ signal bits) with a single synchronization signal and with high accuracy." Ex. 1016 at [0050].

839. Riho also explains that, if "communications (read/write) of respective I/O groups are performed between the first control chip and the second and third controlled chips …, the distance (first impedance) of a signal line connected between respective circuits of the first control chip and the second controlled chip differs from the distance (second impedance) of a signal line connected between respective circuits of the first control chip and the third controlled chip so that

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there are differences in signal arrival time and reflected wave quantity (using the respective chips as references)." Ex. 1016 at [0053]. Riho points out that, taking these differences into account, "the first and second impedances can be made substantially equal to each other by setting the distance of the signal line between the first control chip and the second controlled chip to be equal to the distance of the signal line between the first control chip and the third controlled chip." *Id*. at [0054].

840. A Skilled Artisan would have understood from this disclosure that "*a first number of* [two] *array dies in the first group of array dies* [sharing a data signal TSV] *and a second number of at least one array die* [i.e., two dies] *in the second group of at least one array die* [sharing another data signal TSV] *are selected in consideration of a load of the first die interconnect and a load of the second die interconnect* [including the load of each of those data signal TSVs] *so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit* [which a Skilled Artisan understood reduces skew between the data signals]." For example, a Skilled Artisan would have understood that, when each data signal TSV is made to have substantially the same length and each data signal TSV is connected to the same number of two SDRAMs, the difference in load for driving the data signals on different TSVs is reduced and, as a result, "the skew between data signals DQ and data strobe signals

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DQS/B can be minimized." Ex. 1016 at [0050]; *see also supra* at ¶¶135-137. Indeed, a Skilled Artisan would have understood that the larger the capacitive load, the larger the delay in the transition of the driven signal. Ex. 1030 (Brown) at p.134. Accordingly, a difference in load may result in different signal timing, resulting in a skew between different signals. For example, DQ and DQS signals should be synchronized, but a skew between them may result in an erroneous read of the data value. Ex. 1019 (JESD79-3C) at 13 ("The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes."). Thus, a Skilled Artisan would have also understood that, when each data (and strobe) signal TSV is made to have substantially the same length, and each data (and strobe) signal TSV is connected to the same number of two SDRAMs, the difference in load for driving the data (and strobe) signals on different TSVs is reduced. As a result, for example, "the skew between data signals DQ and data strobe signals DQS/B can be minimized." Ex. 1016 at [0050].

841. Therefore, Riho discloses this limitation to a Skilled Artisan.

842. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the*

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second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit" limitation.

b) [7.b] The First and Second Load

843. Claim 7 requires "*the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die*."

844. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

845. Riho also discloses to a Skilled Artisan **"***the first load including a load of the first die interconnect* [on data signal DQ TSV08]*, and a load of the first group of array dies* [including the pair of SDRAM chips D0 and D8]*, and the second load including a load of the second die interconnect* [on data signal DQ TSV715] *and a load of the second group of at least one array die* [including the pair of SDRAM chips D7 and D15]."

846. For example, Riho discloses that, "when the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used." Ex. 1016 at [0013].

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Riho further explains that "the load capacitance from the disconnected SDRAM becomes off so that it is possible to reduce by half the load of a data signal DQ." *Id*. at [0132]; *see also id.* at [0119-20].

847. A Skilled Artisan would have understood from this disclosure that the load for driving the data signals includes the load of the interconnecting vias and the load of the SDRAMs coupled to those vias. *Supra* at ¶¶135-137.

848. Therefore, Riho discloses this limitation to a Skilled Artisan.

849. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die*" limitation.

8. Claim 8 is Unpatentable

850. Claim 8 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

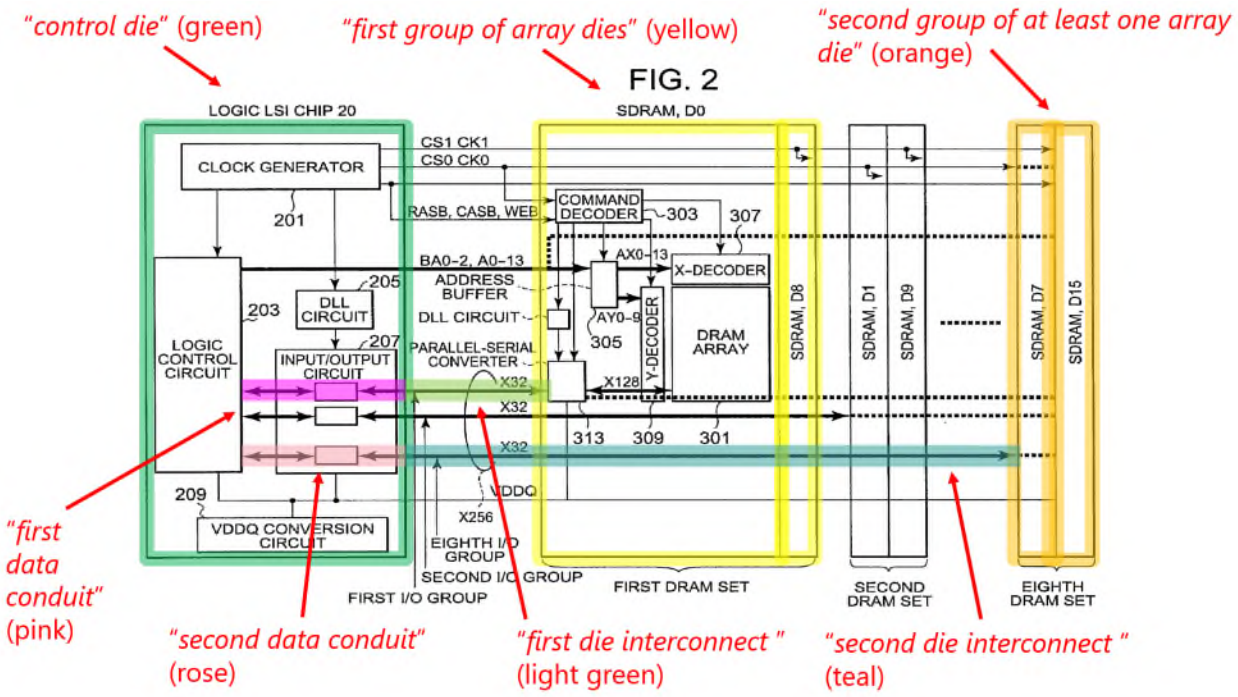
a) [8.a] Data Path Control Signals

851. Claim 8 requires "*[t]he memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals*."

852. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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853. Riho discloses that "*the respective states of the first data conduit* [(pink, connected to TSV08)] *and the second data conduit* [(rose, connected to TSV715)] *are controlled by one or more data path control signals*," such as read and write command signals for the reasons discussed above with reference to claims 2 and 3. *Supra* ¶¶779-786 (claim 2), ¶¶787-798 (claim 3); *see, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).



854. Therefore, Riho discloses this limitation to a Skilled Artisan.

855. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals*" limitation.

b) [8.b] Control Die is Configurable

(1) [8.b.1] First and Second Mode

856. Claim 8 requires "*wherein the control die is configurable to operate in any one of a first mode and a second mode*."

857. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

858. The combination of Riho and Rajan discloses to a Skilled Artisan that "*the control die is configurable to operate in any one of a first mode* [e.g., where the number and type of memory devices is known to the external controller] *and a second mode* [e.g., where the control die is emulating other characteristics, such as timing parameters and the number and type of memory devices in the stack]."

859. For example, Rajan discloses that its "interface circuit includes emulation logic which operates according to the stored memory physical attributes and the stored system emulation attributes, to present to the system an interface to an emulated memory which differs in at least one attribute from the actual physical memory." Ex. 1015 at 14:51-55. Rajan explains that "[t]he emulation logic may, in various embodiments, alter a timing, value, latency, etc. of any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory. Some such signals may pass through unaltered, while others may be altered." *Id.* at 14:55-62. Rajan further explains that, "[i]f the buffer chip is

emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." *Id*. at 6:30-38; *see also id.* at Fig. 18 (reproduced below, showing the emulation logic operating in accordance with attributes that are stored in the interface circuit).

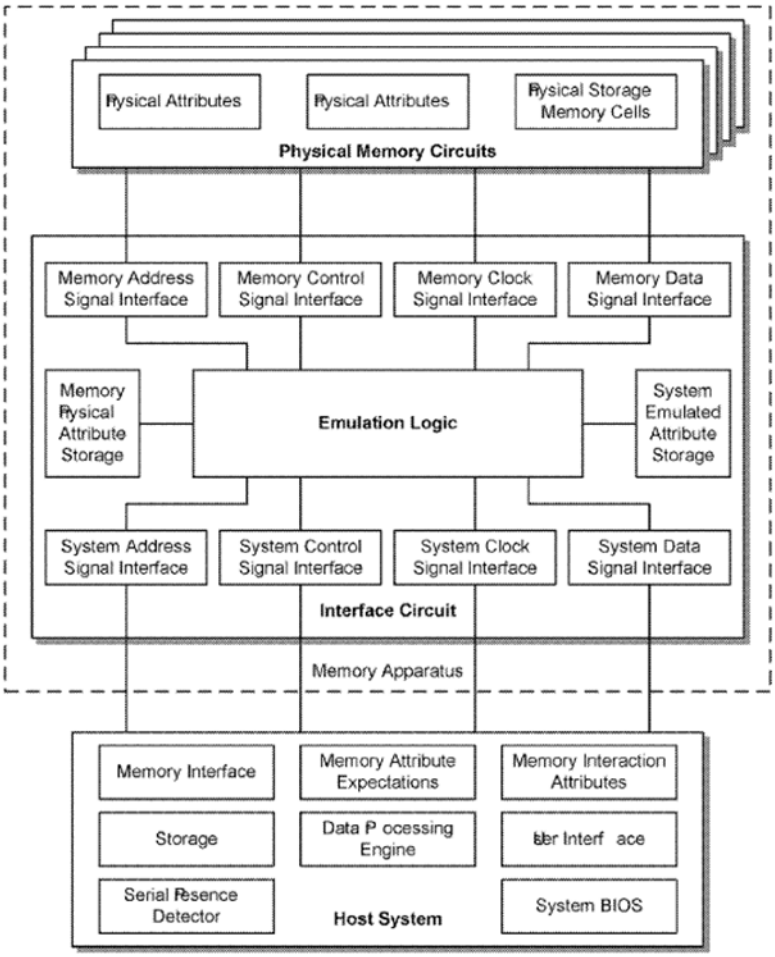


FIG. 18

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860. As discussed below in greater detail, because the Emulation Logic operates in accordance with attributes locally stored in the interface circuit, a Skilled Artisan would have understood that Rajan's interface and its emulation logic can be configured "*to operate in any one of a first mode and a second mode.*" *Infra* ¶¶864-875. Therefore, Rajan's emulation logic may be programmed to emulate different attributes depending on the memory's physical attributes and the system emulation attributes stored in the interface circuit. For example, the emulation logic can be programmed to emulate timing and latency parameters, or a different number or type of memory devices in one mode. In another mode, the external controller may know the actual timing parameters and the type and number of memory devices, e.g., the control "signals may pass through unaltered." Ex. 1015 (Rajan) at 14:59-60.

861. Furthermore, as discussed above, a Skilled Artisan would have also been motivated to implement Rajan's different modes of interface operation in Riho's memory stack to allow it to operate in host systems having different memory attribute expectations and memory interaction attributes. *Supra* ¶¶683-692; *see, e.g.*, Ex. 1015 at Abstract ("A memory subsystem is provided including an interface circuit adapted for communication with a system"), Fig. 18 (reproduced above).

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862. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

863. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein the control die is configurable to operate in any one of a first mode and a second mode, and wherein*" limitation.

(2) [8.b.2] First Mode

864. Claim 8 requires "*in the first mode, the control die receives the data path control signals from the one or more external devices; and*."

865. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

866. Riho discloses to a Skilled Artisan that, "*in the first mode, the control die receives the data path control signals* [such as read and write command signals] *from the one or more external devices*" for the reasons discussed above with reference to claim 2. *Supra* ¶¶779-786.

867. Therefore, Riho discloses this limitation to a Skilled Artisan.

868. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*in the first mode, the control die receives the data path control signals from the one or more external devices*."

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(3) [8.b.3] Second Mode

869. Claim 8 requires "*in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices*."

870. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

871. The combination of Riho and Rajan renders obvious to a Skilled Artisan, at least under Netlist's apparent construction, that "*in the second mode* [where Rajan's interface implemented in Riho's control chip emulates an interface with, e.g., different timing or different number and type of memory chips]*, the control die generates the data path control signals* [including internal control signals for controlling the direction (read or write) and timing of, and selecting the die(s) for, the data transfer through input/output circuit 207] *from at least some of the control/address signals received from the one or more external devices.*"

872. As discussed above with reference to claim limitation [8.b.1], it would have been obvious to implement Rajan's interface emulation mode in Riho's control (interface) chip to allow it to operate with systems having different attribute requirements. S*upra* ¶¶856-863. Furthermore, Rajan discloses that, in such an emulation mode, the emulation logic can generate chip selection signals "*from at least some of the control/address signals received from the one or more*

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external devices." For example, Rajan discloses that "the buffer chip may have four 512 Mb DRAM chips with which it emulates a single 2 Gb DRAM chip. The system will present fifteen row address bits, from which the buffer chip may use the fourteen low order bits (or, optionally, some other set of fourteen bits) to directly address the DRAM chips. The system will present three bank address bits, from which the buffer chip may use the two low order bits (or, optionally, some other set of two bits) to directly address the DRAM chips. During a row operation, the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals, and are stored for later reuse. And during a subsequent column operation, the stored bits are again used to generate the four DRAM chip select signals." Ex. 1015 at 7:4-21; *see also id*. at 7:22-67 (providing further examples of generating chip select signals from the received "*control/address signals*"). A Skilled Artisan would have understood that this combination implements rank multiplication. *Supra* at ¶¶138-141.

873. Rajan also discloses generating delayed read and write commands which are also used to control the direction of the data transmission. For example, Rajan discloses that "[t]he interface circuit may emulate an interface to one version of a protocol such as DDR2 with 5-5-5 latency timing, while the physical memory chips are built to another version of the protocol such as DDR2 with 3-3-3 latency

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timing." Ex. 1015 at 3:52-58; *see also id*. at 10:11-27 ("FIG. 11 is a timing illustrating a timing design 1100 showing how the buffer chip does this. The memory controller issues the write operation at t0. In FIG. 10, the write operation appeared at the DRAM circuits one clock later at t1, due to the inherent delay through the buffer chip. But in FIG. 11, in addition to the inherent one clock delay, the buffer chip has added an extra two clocks of delay to the write operation, which is not issued to the DRAM chips until t0+1+2=t3. Because the DRAM chips receive the write operation at t3 and have a write CAS latency of three clocks, they expect to receive the write data at t3+3=t6. Because the memory controller issued die write operation at t0, and it expects a write CAS latency of five clocks, it issues the write data at time t0+5=t5. After a one clock delay through the buffer chip, the write data arrives at the DRAM chips at t5+1=t6, and the timing problem is solved."), Fig. 11 (reproduced below).

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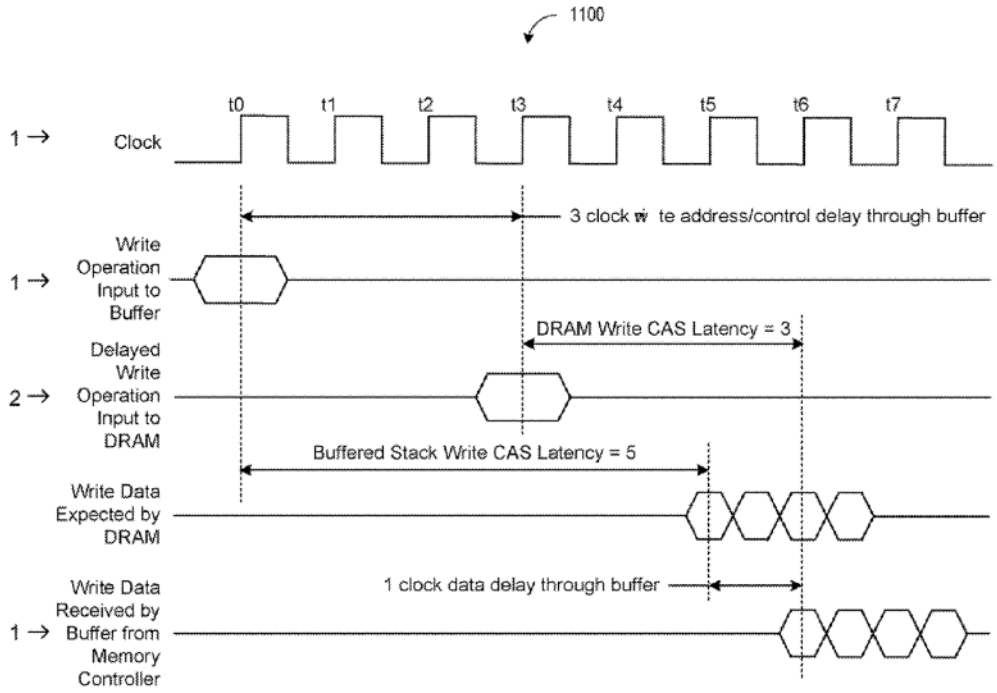


FIG. 11

874. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

875. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices*."

9. Claim 9 is Unpatentable

876. Claim 9 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

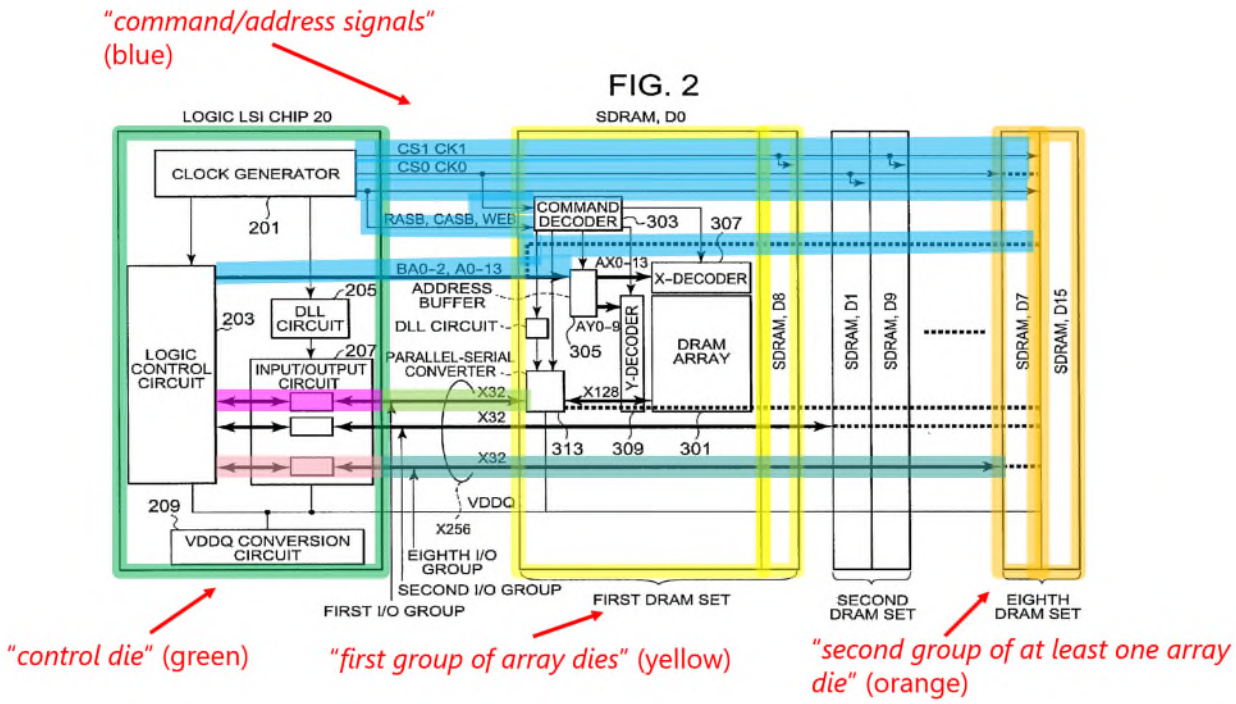
877. Claim 9 requires "*[t]he memory package of claim 1, wherein the control die further comprises command/address conduits configured to provide*

corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address."

878. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

879. Riho discloses that "*the control die* [control chip 20] *further comprises command/address conduits* [connecting clock generator 201 and logic control circuit 203 in control chip 20 to corresponding TSVs] *configured to provide corresponding command/address signals* [(blue)] *to the array dies* [SDRAM chips D0-D15]*, the command/address signals including at least one memory cell address* [in the respective DRAM array 301]" for the reasons discussed above with reference to claim limitations [1.b] and [1.c] and claim 4. *Supra* ¶¶711-726 (claim limitations [1.b-c]), ¶¶799-810 (claim 4); *see, e.g.*, Ex. 1016 at [0030, 0034, 0037-39, 0043-44] and Fig. 2 (reproduced below, annotated).

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880. For example, Riho discloses to a Skilled Artisan that "*the command/address signals include[] at least one memory cell address.*" Indeed, Riho explains that, "[i]n response to the address signals AX0-13 and AY0-9 given to the X- and Y-decoders 307 and 309, the DRAM array 301 inputs and outputs 128-bit (×128) data signals in parallel between itself and the parallel-serial conversion circuit 313." Ex. 1016 at [0049]; *see also id*. at Fig. 2 (reproduced above, annotated); Ex. 1019 at 13 ("A0-A15").

881. Therefore, Riho discloses this limitation to a Skilled Artisan.

882. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein the control die further comprises command/address conduits configured*

to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address" limitation.

10. Claim 10 is Unpatentable

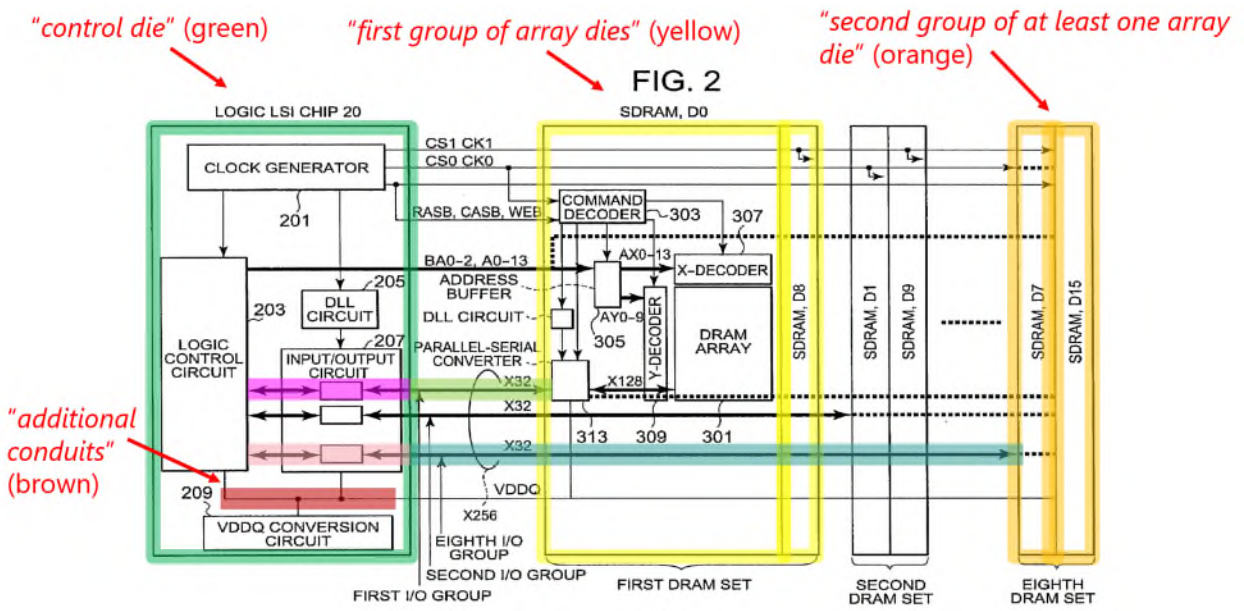
883. Claim 10 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

884. Claim 10 requires "*[t]he memory package of claim 1, wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies*."

885. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

886. Riho discloses to a Skilled Artisan that "*the control die further comprises one or more additional conduits* [(brown) from VDDQ conversion circuit 209] *configured to provide one or more of a supply voltage signal and a ground signal to the array dies* [SDRAM chips D0-D15]," for example, to provide power for the operation of the memory chips, including read and write operations. *See, e.g.*, Ex. 1016 at Fig. 2 (reproduced below, annotated).

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887. For example, Riho discloses that, the "logic LSI chip 20 shown in FIG. 2 comprises … a VDDQ conversion circuit 209. From the VDDQ conversion circuit 209, a memory-driving main power supply voltage VDDQ is applied not only to the input/output circuit 207 and the logic control circuit 203 of the logic LSI chip 20, but also to the SDRAMs D0 to D15 stacked on the logic LSI chip 20." Ex. 1016 at [0036]; *see also id.* at Fig. 2 (reproduced above, annotated).

888. A Skilled Artisan would have also understood that applying a VDDQ supply voltage includes providing a corresponding ground signal to close the electric circuit. *See, e.g.*, Ex. 1019 (JESD79-3C) at p.14 (listing supply voltages and corresponding grounds for SDRAMs).

889. Therefore, Riho discloses this limitation to a Skilled Artisan.

890. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies*" limitation

11. Claim 11 is Unpatentable

891. Claim 11 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

a) [11.a] Preamble

892. Claim 11 requires "*[a] memory package comprising*."

893. As shown in the table below, the preamble of claim 11 is identical to the preamble of claim 1:

Claim 1	**Claim 11**
[1.a] A memory package comprising:	[11.a] A memory package comprising:

894. As discussed above with reference to claim limitation [1.a], to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy "*[a] memory package comprising*." *Supra* ¶¶706-710.

b) [11.b] Input/Output Terminals

895. Claim 11 requires "*[a] plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

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896. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

897. As shown in the table below, claim limitation [11.b] is identical to claim limitation [1.b]:

Claim 1	**Claim 11**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[11.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;

898. As discussed above with reference to claim limitation [1.b], the prior art references in Grounds 4 and 5 satisfy "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*." *Supra* ¶¶711-718.

c) [11.c] Array Dies Arranged in a Stack

899. Claim 11 requires "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*."

900. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

901. As shown in the table below, claim limitation [11.c] is very similar to claim limitation [1.c]:

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Claim 1	Claim 11
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;	[11.c] a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

902. As discussed above with reference to claim limitation [1.c], the prior art references in Grounds 4 and 5 satisfy "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*." *Supra* ¶¶719-726.

d) [11.d.1] and [11.d.1] Die Interconnects in Electrical Communication with the Array Dies

903. Claim 11 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

904. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

905. As shown in the table below, claim limitation [11.d.1] is identical to claim limitation [1.d.1], and claim limitation [11.d.2] is identical to claim limitation [1.d.2]:

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Claim 1	**Claim 11**
[1.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,	[11.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
[1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[11.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

906. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Grounds 4 and 5 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die*," and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶727-744.

e) [11.e] Control Die

(1) [11.e.1] A Control Die Comprising

907. Claim 11 requires "*a control die comprising*."

908. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

909. As shown in the table below, claim limitation [11.e.1] is identical to claim limitation [1.e.1]:

Claim 1	**Claim 11**
[1.e.1] a control die comprising	[11.e.1] a control die comprising

910. As discussed above with reference to claim limitation [1.e.1], the prior art references in Grounds 4 and 5 satisfy "*a control die comprising*." *Supra* ¶¶745-752.

(2) [11.e.2] and [11.e.3] First and Second Data Conduit

911. Claim 11 requires "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals,*" and "*at least a second data conduit between the second die interconnect and the first terminal*, and *chip select conduits for providing chip select signals to respective array dies*."

912. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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913. As shown in the table below, claim limitation [11.e.2] and [11.e.3] are nearly identical to claim limitations [1.e.2] and [1.e.3]:

Claim 1	**Claim 11**
[1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] at least a second data conduit between the second die interconnect and the first terminal, . . .	[11.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [11.e.3] at least a second data conduit between the second die interconnect and the first terminal, . . .

914. As discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Grounds 4 and 5 satisfy "*at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals*," and "*at least a second data conduit between the second die interconnect and the first terminal*." *Supra* ¶¶753-769. Furthermore, as discussed below with reference to claim element [15.a], a Skilled Artisan would have understood and it would have been obvious to her that each of the first and second data conduits can include a respective driver. *Infra* at ¶¶950-962.

(3) [11.e.4] Chip Select Conduits

915. Claim 11 requires "*chip select conduits for providing chip select signals to respective array dies*."

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916. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

917. As shown in the table below, claim limitation [11.e.4] is very similar to claim limitations [6.a] and [6.b]:

Claim 6	**Claim 11**
[6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[11.e.4] chip select conduits for providing chip select signals to respective array dies;

918. As discussed above with reference to claim limitation [6.a] and [6.b], the prior art references in Grounds 4 and 5 satisfy "*chip select conduits for providing chip select signals to respective array dies*." *Supra* ¶¶818-832.

(4) [11.e.5] Control Circuit

919. Claim 11 requires "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*."

920. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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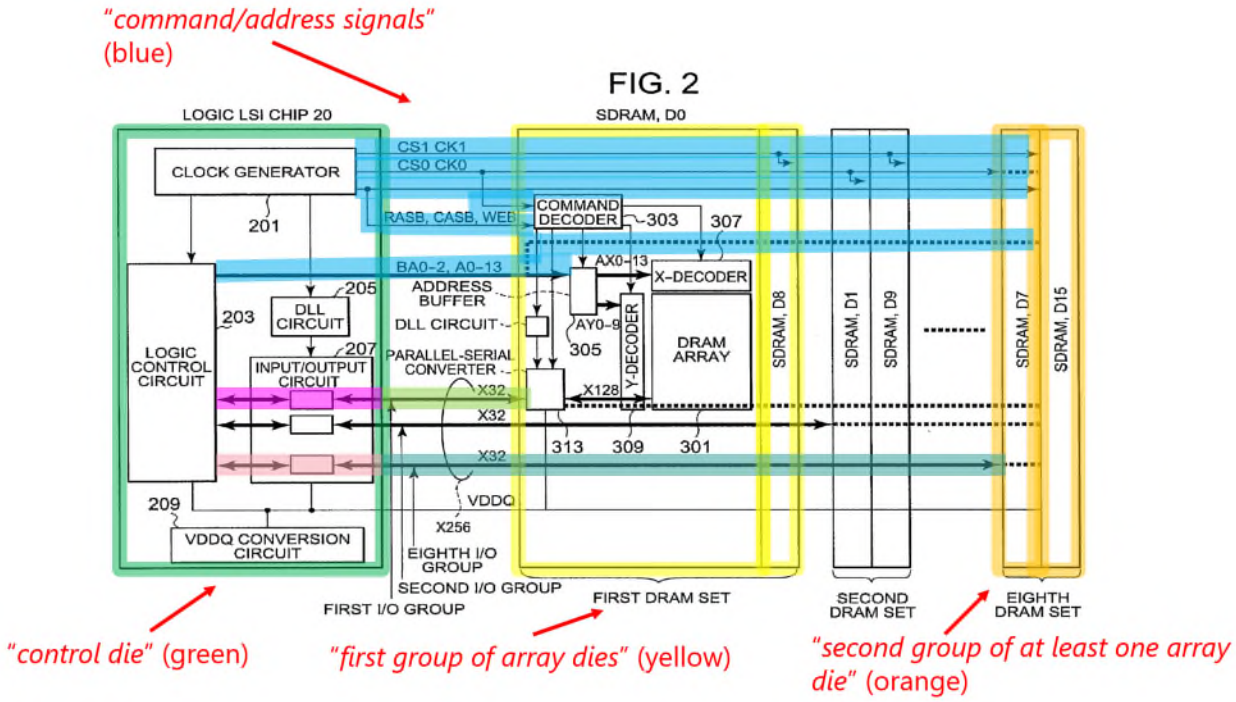
921. As shown in the table below, claim limitation [11.e.5] is very similar to claim limitation [1.e.4]:

Claim 1	**Claim 11**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.	[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

922. As discussed above with reference to claim limitation [1.e.4], the prior art references in Grounds 4 and 5 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.*" *Supra* ¶¶770-778.

923. With respect to the "*driv[ing] a data signal to an array die selected by at least one of the chip-select signals*," Riho discloses, for example, that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total." Ex. 1016 at [0040]. Riho explains that "[t]he data signal DQ is transmitted or received as an I/O data signal. The first DRAM set is allocated with a first I/O group (×32 DQ signal bits) and the second DRAM set is allocated with a second I/O group (×32 DQ signal bits). The

third to eighth DRAM sets are allocated with third to eighth I/O groups, respectively." *Id.*; *see also* Fig. 2 (reproduced below, annotated).



924. Riho also discloses that, "[o]f the two groups (chip selection groups), the first group (first controlled chips) is communication-controlled at a first access cycle by the first chip selection signal (first clock signal CS0CK0) output from the control chip 20 while the second group (second controlled chips) is communication-controlled at a second access cycle by the second chip selection signal (second clock signal CS1CK1) output from the control chip 20. Since the first and second groups are mutually exclusively controlled by the control chip 20 at the first and second access cycles, each of the TSVs corresponding to one I/O bit is shared by the first and second groups." *Id.* at [0033].

925. A Skilled Artisan would have understood from Riho's disclosure that a data signal is driven by the input/output circuit 207 to a corresponding SDRAM chip ("*an array die*") that is selected by the chip selection signals CS0CK0 and CS1CK1. *See, e.g.*, Ex. 1022 (Jacob et al.) at 318-321 (explaining the operation of chip select signals); Ex. 1023 (Jacob) at 2-4, 9 & Fig.16 (same).

926. Furthermore, a Skilled Artisan would have understood that, in the combination of Riho and Rajan, the emulation logic of Rajan generates the chip select signals that select the DRAM chips to which the data is driven. *See, e.g.*, Ex. 1015 at 6:30-38 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.").

927. Therefore, Riho discloses and, in view of Rajan, renders obvious this limitation to a Skilled Artisan.

928. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*wherein the control die further comprises a control circuit to control respective*

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states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals."

12. Claim 12 is Unpatentable

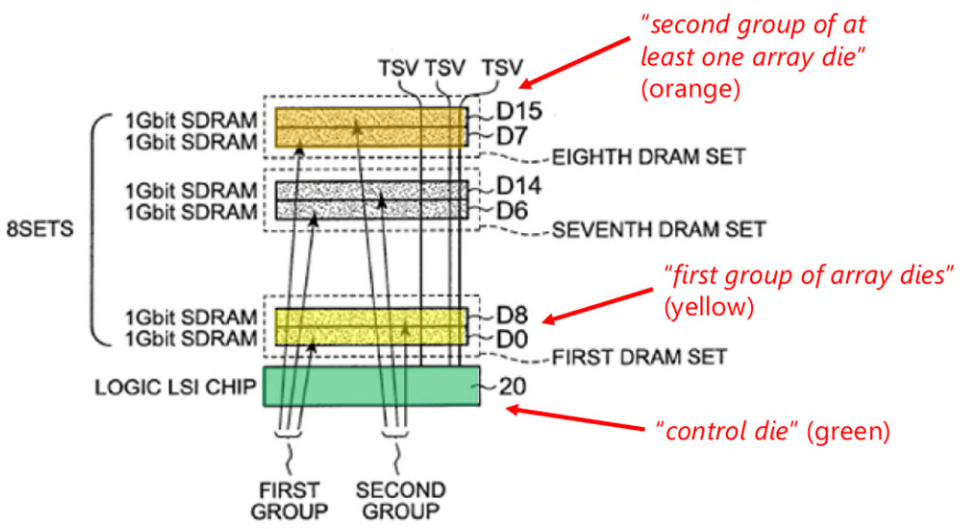
929. Claim 12 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

930. Claim 12 requires "*[t]he memory package of claim 11, wherein the chip select conduits pass through the control die*."

931. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

932. For example, Riho discloses that "external terminals (not illustrated) of the semiconductor device with the structure shown in FIG. 1 are disposed on the lower side of the logic LSI chip 20. The external terminals are connected to the logic LSI chip 20. I/O signal lines penetrating through the controlled chips [e.g., SDRAMs D0-D8, D7-D15], which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the external terminals." Ex. 1016 at [0026], Fig. 1 (reproduced below, annotated).

FIG. 1



933. A Skilled Artisan would have understood from this disclosure that, in the combination, "*the chip select conduits pass through the control die*" because they are connecting the external chip select terminal at the lower side of the control die to the SDRAMs coupled to the upper side of the control die.

934. Therefore, Riho discloses this limitation to a Skilled Artisan. In addition, the 060 Patent admits that this feature was disclosed by the prior-art JEDEC 3DS-DIMM proposal. Ex. 1001 at 19:55-56 ("the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720"); *see also* Ex. 1019 at 6-11 ("CS" terminals at bottom of "stacked" packages); Ex. 1021 at 1-2 (MO-207 JEDEC standard with solder balls at the bottom of the package, below); Ex. 1022 at 374 ("BGA"), 476 ("FBGA").

935. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*memory package of claim 11, wherein the chip select conduits pass through the control die*" limitation.

13. Claim 13 is Unpatentable

936. Claim 13 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

937. Claim 13 requires "*[t]he memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies*."

938. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

939. Riho discloses to a Skilled Artisan that "*the chip select conduits include drivers to drive the chip select signals to the respective array dies.*"

940. For example, Riho discloses that "[t]he clock generator 201 supplies a first clock signal CS0CK0 to the SDRAMs D0 to D7 (which belong to first controlled chips) forming a first group (chip selection group) and further supplies a second clock signal CS1CK1 to the SDRAMs D8 to D15 (which belong to second controlled chips) forming a second group (chip selection group)." Ex. 1016 at [0037]. Riho explains that "it is assumed that the SDRAMs D0 to D15 each have a total of 382 TSVs including 256 data signal (DQ) penetrating through substrate

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vias (TSVs), 32 data mask (DM) penetrating through substrate vias (TSVs), 64 data strobe signal (DQS/DQSB) penetrating through substrate vias (TSVs), 14 address penetrating through substrate vias (A0 to A13) (TSVs), 3 bank address penetrating through substrate vias (BA0 to BA2) (TSVs), 3 command signal penetrating through substrate vias (TSVs) (/RAS (RASB), /CAS (CASB), /WE (WEB)), and 10 control signal penetrating through substrate vias (TSVs) (CS0, CS1, CKE0, CKE1, CK0, CK1, /CK0, /CK1, ODT0, ODT1)." *Id*. at [0030]. Riho also discloses that the "I/O signal lines penetrating through the controlled chips, which will be described later, are connected to the logic LSI chip 20 and are not directly connected to the external terminals." *Id*. at [0026].

941. A Skilled Artisan would have understood from this disclosure that the clock generator 201 includes drivers which supply "a first clock signal CS0CK0 to the SDRAMs D0 to D7" and "a second clock signal CS1CK1 to the SDRAMs D8 to D15" by driving those signals through the corresponding TSVs (since those signals are not directly connected to the external terminals). A Skilled Artisan would have also understood that the chip select signals are driven from the control die to the array die by drivers. *Supra* at ¶¶135-137; *see also* Ex. 1030 at 135 ("In circuits in which a logic gate has to drive a large capacitive load, buffers are often used to improve performance … Buffers can be created with different amounts of drive capability, depending on the sizes of the transistor … In addition to their use

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for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices."); Ex. 1038 (Stone) at p.68 ("The drivers commonly used for bus systems are tri-state drivers that have a low, high, and off (or high impedance) mode of operation."); Ex. 1017 (Wyman) at 1:14-20 ("Chips contain pads through which a signal can be driven off-chip to pins of another board and/or chip[.] The driver circuit must be designed with a predetermined output within a given tolerance range. This predetermined singular amplified drive signal must be sufficient to chive the output signal the required distance accounting for such impediments as available real estate, heat, resistance, capacitance and impedance.").

942. Therefore, Riho discloses this limitation to a Skilled Artisan.

943. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies*" limitation.

14. Claim 14 is Unpatentable

944. Claim 14 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

945. Claim 14 requires "*[t]he memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias*."

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946. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

947. As shown in the table below, claim 14 is very similar to claim 5:

Claim 5	**Claim 14**
[5] The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.	[14] The memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.

948. As discussed above with reference to claim 5, the prior art references in Grounds 4 and 5 satisfy "*wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.*" *Supra* ¶¶811-816.

15. Claim 15 is Unpatentable

949. Claim 15 is unpatentable as the prior art references in Ground 5 render the claim obvious.

a) [15.a] First and Second Data Conduit and First and Second Driver

950. Claim 15 requires "*[t]he memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the*

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second data conduit comprises at least a second driver having a second driver size, and."

951. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

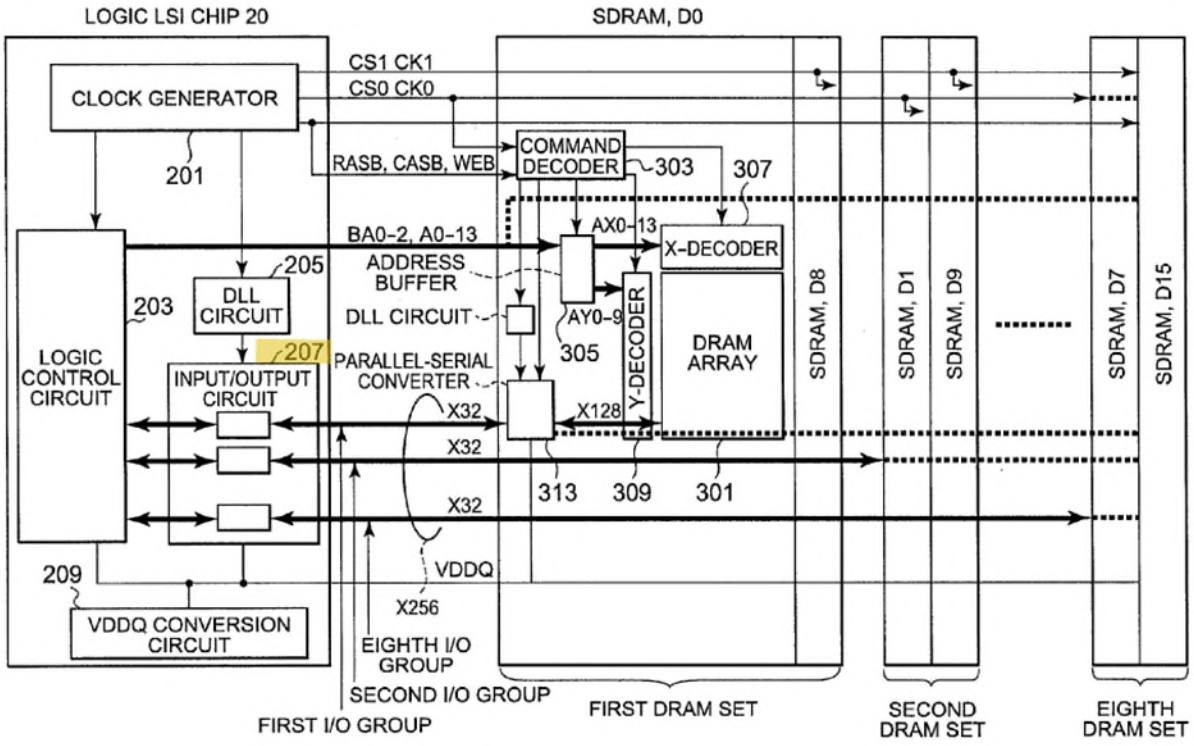
952. Riho in combination with Riho2 renders obvious to a Skilled Artisan that "*the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size.*"

953. For example, Riho discloses that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15, respectively, and thus sends and receives parallel data signals DQ of 256-bit width in total. The data signal DQ is transmitted or received as an I/O data signal." Ex. 1016 (Riho) at [0040] and Fig. 2 (reproduced below, annotated); *see also id.* at [0045-46] ("The input/output circuit 207 includes interface circuits such as buffers corresponding to the SDRAM chips, respectively, so that data signals DQ are sent and received between the SDRAM D0 and the logic control circuit 203 through the corresponding interface circuit. … That is, the data signal DQ TSVs for the SDRAM D0 are commonly used by the first DRAM set (SDRAM D0 and SDRAM D8). … The data signal DQ TSVs for the SDRAM D7 are provided between the input/output circuit 207 of the logic LSI chip 20 and the SDRAM D7.

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The data signal DQ TSVs for the SDRAM D7 are also formed by 32 TSVs and are commonly used by the SDRAMs D7 and D15.").

FIG. 2



A Skilled Artisan would have been motivated by this disclosure to implement drivers in input/output circuit 207 in order to drive the data signals off to the array dies. *Supra* at ¶¶135-137; see, e.g. Ex. 1030 (Brown) at 135-136 ("In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices. Buffers can handle relatively large amounts of current flow because they are built with large transistors."). Buffers are ordinarily used whenever digital signals are communicated between dies. *See id.*

954. Riho also explains that "[i]t is preferable to take into account that, practically, signal lines formed by through-silicon vias (TSVs) are not necessarily made equal in impedance to each other due to manufacturing variations in manufacturing processes (TSV forming process, bump forming process, and TSV-bump connection process). That is, TSVs formed in different manufacturing processes may have different impedances due to manufacturing variations in the manufacturing processes." Ex. 1016 (Riho) at [0055]. Riho further explains that "it is also preferable to expect that when a plurality of signal lines are formed by a plurality of TSVs, the impedance of each signal line may be different from those of the others due to variations of inherent manufacturing processes." *Id.* at [0056]. For example, Riho describes that "the SDRAM chip located closer to the logic LSI chip 20 has a smaller penetrating through resistance while the SDRAM chip located farther from the logic LSI chip 20 has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process." *Id.* at [0061].

955. A Skilled Artisan would have understood from this disclosure that differences in impedances and other variations in the through silicon vias and the different positions of the SDRAM chips should be taken into account when designing the stacked structure of Riho.

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956. Riho2 discloses that, in a case where "it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another … , a configuration is provided to optimize the output drive capacity of output buffers according to the number of stacked chip dies." Ex. 1018 at [0096]. For example, Riho2's "FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." *Id*. at [0097], Fig. 7A (reproduced below).

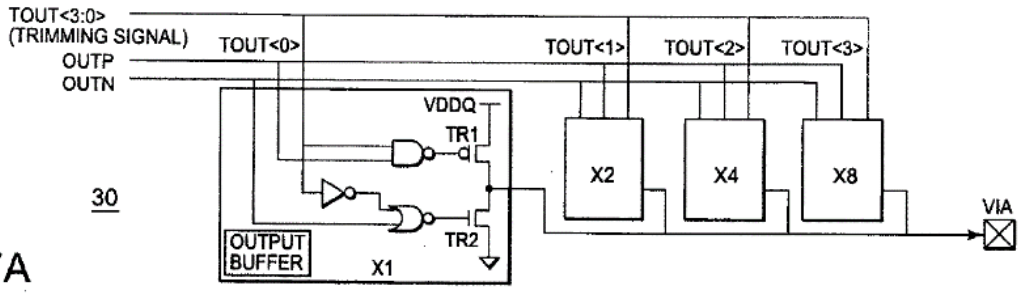


FIG. 7A

957. Therefore, a Skilled Artisan would have been motivated to optimize the drive capacity of output buffers as taught by Riho2 in the control chip of Riho,

because Riho also discloses differences in impedances and resistances for the different data signal DQ TSVs.

958. As discussed above, a Skilled Artisan would have also been motivated to look at Riho2 to address the issues created by the variations in the TSV properties described by Riho and to optimize the output drive capacity of output buffers as taught by Riho2. *Supra* ¶¶693-703. A Skilled Artisan would have also understood that such an optimization of driver capacity would save power compared to using full-capacity drivers, which would be wasteful and inefficient. *See, e.g.*, Ex. 1017 (Wyman) at 1:22-24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.").

959. Making such a combination was well within the level of skill, since Riho2 itself teaches drivers of different strengths, and the combination would have provided nothing more than expected, a power efficient drive of signals through Riho's TSVs. For example, Riho2 discloses a circuitry that includes multiple drivers which are selectively activated to achieve the optimal driving strength. Ex. 1018 (Riho2) at [0096-97] ("FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In the example shown here, there are provided four output

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buffers X1, X2, X4, and X8 having mutually different drive capacities (the numerical values following the letter "X" indicate capacity ratios)."), Fig. 7A (reproduced below).

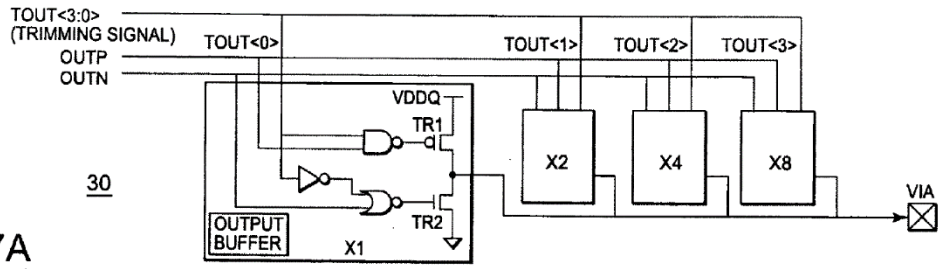


FIG. 7A

See also Ex. 1017 (Wyman) at Fig. 5 and 5:11-14 ("Similar to FIG. 2 through FIG. 4, a designer may now utilize and tap-off at five locations (506-1, 506-2, 506-3, 506-4, 508) depending on the drive requirements for a specific element or device.")

960. Indeed, compensating the driver strength for different positions of a die in a stack was well known at the time. *See, e.g.*, Ex. 1039 (Ma (U.S. Patent No. 9,160,349)) at Abstract ("In other embodiments, for example, differences in the termination impedance or driver drive-strength resulting from differences in the location of a die in a stack may be compensated for."), 7:46-49 ("One embodiment of a compensation circuit 400 that may compensate for both termination impedance and drive strength variations resulting from differences in die location is shown in FIG. 6."), and Fig. 6 (reproduced below).

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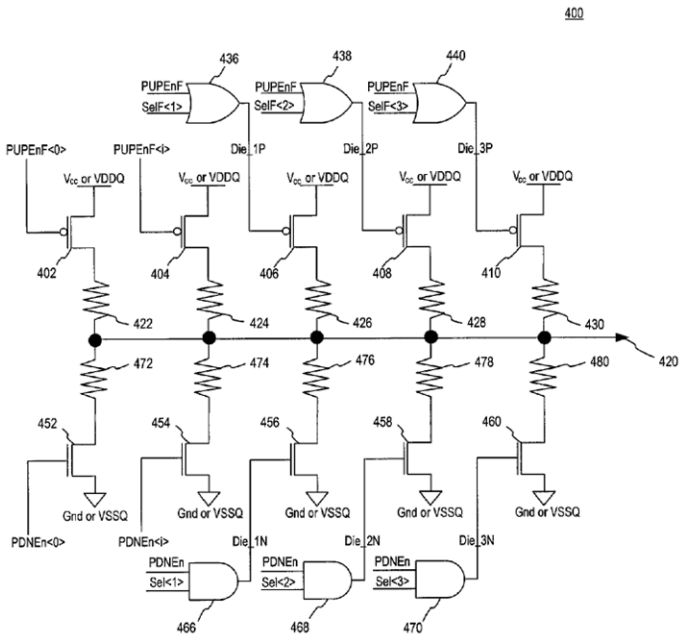


Figure 6

961. Therefore, the combination of Riho and Riho2 renders obvious this limitation to a Skilled Artisan.

962. Accordingly, the prior art references in Ground 5 satisfy the "*the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size*" limitation.

b) [15.b] First and Second Driver Size Less Than Driver Size Sufficient to Drive Signal

963. Claim 15 is unpatentable as the prior art references in Ground 5 render the claim obvious.

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964. Claim 15 requires "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*."

965. The prior art references in each of Ground 5 teach this limitation to a Skilled Artisan.

966. Riho discloses and, in combination with Riho2, renders obvious to a Skilled Artisan that "*the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.*"

967. For example, Riho discloses that, "by employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups." Ex. 1016 at [0103]; *see also id.* at [0013, 119-20].

968. A Skilled Artisan would have understood from this disclosure that the load in Riho is "*less than … along a die interconnect in electrical communication with each of the plurality of array dies*." Furthermore, as discussed above with

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reference to claim limitation [15.a], Riho2 teaches optimizing the driver size to drive a signal along TSVs. *Supra* ¶¶950-962, 135-137; *see also, e.g.*, Ex. 1018 at [0097] ("FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers … They have the same circuit configuration, but their transistors are of mutually different sizes."), Fig. 7A (reproduced below); *see also* Ex. 1017 at 6:44-50 ("In this instance, presume that the drive from tap "T2" (506-3) would be inadequate, but the total drive from the pad (508) would be overkill.").

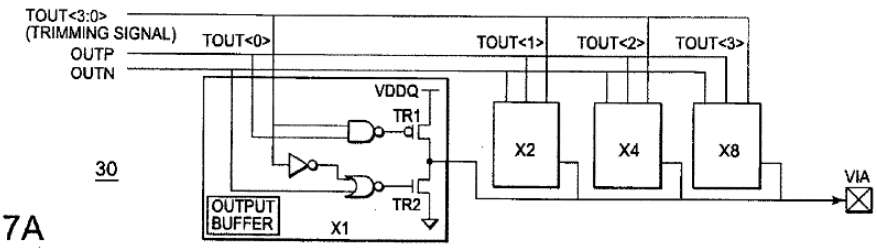


FIG. 7A

969. Therefore, a Skilled Artisan would have been motivated to use a "*driver size*" that is "optimized" for efficient signal communication as taught by Riho2.

970. Therefore, the combination of Riho and Riho2 renders obvious this limitation to a Skilled Artisan.

971. Accordingly, the prior art references in Ground 5 satisfy the "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication*

with each of the plurality of array dies without significant signal degradation" limitation.

16. Claim 16 is Unpatentable

972. Claim 16 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

973. Claim 16 requires "*[t]he memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals*."

974. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

975. As shown in the table below, claim 16 is very similar to claim limitations [1.e.4] and [8.b.3]:

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Claims 1, 8	**Claim 16**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [8.b.3] in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.	[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.

976. As discussed above reference to claim limitations [1.e.4] and [8.b.3], the prior art references in Grounds 4 and 5 satisfy "*wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.*" *Supra* ¶¶770-778 (claim limitation [1.e.4]), 869-875 (claim limitation [8.b.3]).

977. For example, as discussed above with reference to claim limitation [8.b.3], the combination of Riho and Rajan discloses that "*the chip select signal is generated using an address signal in the control/address signals*." *Supra* ¶¶869-875; *see, e.g.*, Ex. 1015 at 7:4-21 ("As another example, the buffer chip may have four 512 Mb DRAM chips with which it emulates a single 2 Gb DRAM chip. The

system will present fifteen row address bits, from which the buffer chip may use the fourteen low order bits (or, optionally, some other set of fourteen bits) to directly address the DRAM chips. The system will present three bank address bits, from which the buffer chip may use the two low order bits (or, optionally, some other set of two bits) to directly address the DRAM chips. During a row operation, the most significant bank address bit (or other unused bit) and the most significant row address bit (or other unused bit) are used to generate the four DRAM chip select signals, and are stored for later reuse. And during a subsequent column operation, the stored bits are again used to generate the four DRAM chip select signals.").

978. Therefore, Riho discloses or renders obvious in combination with Rajan this limitation to a Skilled Artisan.

979. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals*" limitation.

17. Claim 17 is Unpatentable

980. Claim 17 is unpatentable as the prior art references in each of Grounds 4 and 5 render the claim obvious.

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981. Claim 17 requires "*[t]he memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals*."

982. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

983. As shown in the table below, claim 17 is very similar to claim limitations [1.e.4], [4.a] and [4.b]:

Claims 1, 4	**Claim 17**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[17] The memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.

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984. As discussed above with reference to claim limitations [1.e.4], [4.a], and [4.b], the prior art references in Grounds 4 and 5 satisfy "*wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.*" *Supra* ¶¶770-778 (claim limitation [1.e.4]), ¶¶799-810 (claim limitations [4.a] and [4.b]).

18. Claim 18 is Unpatentable

985. Claim 18 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

986. Claim 18 requires "*[t]he memory package of claim 16, wherein the control/ address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal*."

987. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

988. As shown in the table below, claim 18 is very similar to claim 2 and claim limitations [4.a] and [4.b]:

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Claims 2, 4	**Claim 18**
[2] The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[18] The memory package of claim 16, wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal.

989. As discussed above with reference to claim 2 and claim limitations [4.a] and [4.b], the prior art references in Grounds 4 and 5 satisfy "*wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal*." *Supra* ¶¶779-786 (claim 2), ¶¶799-810 (claim limitations [4.a] and [4.b]); *see also* Ex. 1001 (the 060 Patent) at 15:48-67 (describing read/write command signals, including chip select signals controlling the data path).

19. Claim 19 is Unpatentable

990. Claim 19 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

a) [19.a] Generate Data Path Control Signals

991. Claim 19 requires "*[t]he memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and*."

992. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

993. As shown in the table below, claim limitation [19.a] is very similar to claim 3 and claim limitations [1.e.4], [4.a], and [8.b.3]:

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Claims 1, 3-4, 8	**Claim 19**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [4.a] The memory package of claim 3, wherein the control signals include command/address signals and [8.b.3] in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.	[19.a] The memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and

994. As discussed above with reference to claim 3 and claim limitations [1.e.4], [4.a], and [8.b.3], the prior art references in Grounds 4 and 5 satisfy "*wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of*

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terminals." *Supra* ¶¶770-778 (claim limitation [1.e.4]), ¶¶787-798 (claim 3), ¶¶800-804 (claim limitation [4.a]), ¶¶869-875 (claim limitation 8.b.3).

b) [19.b] Control Circuit Controls Respective States of First Data Conduit

995. Claim 19 further requires "*wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals*."

996. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

997. As shown in the table below, claim limitation [19.b] is very similar to claim limitation [1.e.4] and claim 3:

Claim 3	**Claim 19**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[19.b] wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.

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998. As discussed above with reference to claim limitation [1.e.4] and claim 3, the prior art references in Grounds 4 and 5 satisfy "*wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.*" *Supra* ¶¶770-778 (claim limitation [1.e.4]), ¶¶787-798 (claim 3).

20. Claim 20 is Unpatentable

999. Claim 20 is unpatentable as the prior art references in Ground 5 renders the claim obvious.

a) [20.a] Preamble

1000. The preamble of claim 20 requires "*[a] method for optimizing load in a memory package comprising*."

1001. To the extent the preamble is limiting, the prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1002. As shown in the table below, claim limitation [20.a] is very similar to claim limitation [1.a]:

Claim 1	**Claim 20**
[1.a] A memory package comprising:	[20.a] A method for optimizing load in a memory package comprising

1003. Accordingly, the prior art references in Ground 5 satisfy "*[a] memory package*," *supra* ¶¶693-703, 706-710, and the specific steps for "*optimizing [the] load*" are discussed in the limitations below.

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b) [20.b] Method Comprising

(1) [20.b.1] Array Dies Arranged in a Stack

1004. Claim 20 requires "*a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die*."

1005. The prior art references in Ground 5 each teaches this limitation to a Skilled Artisan.

1006. As shown in the table below, claim limitation [20.b.1] is identical to claim limitation [1.c]:

Claim 1	**Claim 20**
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;	[20.b.1] a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die;

1007. As discussed above with reference to claim limitation [1.c], the prior art references in Ground 5 satisfy the "*a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die*" limitation. *Supra* ¶¶719-726.

(2) [20.b.2] Die Interconnects

1008. Claim 20 requires "*at least a first die interconnect and a second die interconnect*."

1009. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

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1010. As shown in the table below, claim limitation [20.b.2] is very similar to claim limitations [1.d.1]-[1.d.2]:

Claim 1	**Claim 20**
[1.d.1] - [1.d.2] at least a first die interconnect and a second die interconnect, …;	[20.b.2] at least a first die interconnect and a second die interconnect,

1011. As discussed above with reference to claim limitations [1.d.1]-[1.d.2], the prior art references in Ground 5 satisfy "*at least a first die interconnect and a second die interconnect*." *Supra* ¶¶727-744.

(3) [20.b.3] Control Die

1012. Claim 20 requires "*a control die*."

1013. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1014. As shown in the table below, claim limitation [20.b.3] is nearly identical to claim limitation [1.e.1]:

Claim 1	**Claim 20**
[1.e.1] a control die comprising	[20.b.3] a control die, and

1015. As discussed above with reference to claim limitation [1.e.1], the prior art references in Ground 5 satisfy "*a control die*." *Supra* ¶¶745-752.

(4) [20.b.4] Input/Output Terminals

1016. Claim 20 requires "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*."

1017. The prior art references in Ground 5 teaches this limitation to a Skilled Artisan.

1018. As shown in the table below, claim limitation [20.b.4] is identical to claim limitation [1.b]:

Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[20.b.4] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices,

1019. As discussed above with reference to claim limitation [1.b], the prior art references in Ground 5 satisfy "*a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices*." *Supra* ¶¶711-718.

c) [20.c] Method Further Comprising

1020. Claim 20 requires "*the method comprising*."

1021. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

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1022. As shown in the table below, claim limitation [20.c] is very similar to claim limitation [20.a]:

Claim 20	**Claim 20**
[20.a] A method for optimizing load in a memory package comprising	[20.c] the method comprising:

1023. As discussed above with reference to claim limitation [20.a], the prior art references in Ground 5 satisfy "*the method comprising*." *Supra* ¶¶1000-1003.

d) [20.d] Signals

(1) [20.d.1] Receiving a Data Signal at a First Terminal

1024. Claim 20 requires "*receiving a data signal at a first terminal of the plurality of input/output terminals*."

1025. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1026. As shown in the table below, claim limitation [20.d.1] is very similar to claim limitation [1.b], [1.e.2], and [1.e.3]:

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Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices; [1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,	[20.d.1] receiving a data signal at a first terminal of the plurality of input/output terminals;

1027. As discussed above with reference to claim limitation [1.b], [1.e.2], and [1.e.3], the prior art references in Ground 5 satisfy "*receiving a data signal at a first terminal of the plurality of input/output terminals*." *Supra* ¶¶711-718, 753-769.

(2) [20.d.2] Receiving Control Signals at Second Terminals

1028. Claim 20 requires "*receiving control signals at second terminals of the plurality of input/output terminals*."

1029. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

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1030. As shown in the table below, claim limitation [20.d.2] is very similar to claim limitation [1.b] and [1.e.4]:

Claim 1	**Claim 20**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices; [1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.	[20.d.2] receiving control signals at second terminals of the plurality of input/output terminals;

1031. As discussed above with reference to claim limitation [1.b] and [1.e.4], the prior art references in Ground 5 satisfy "*receiving control signals at second terminals of the plurality of input/output terminals*." *Supra* ¶¶711-718, 770-778.

(3) [20.d.3] Providing Chip Select Signals to Array Dies

1032. Claim 20 requires "*providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and*."

1033. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

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1034. As shown in the table below, claim limitation [20.d.3] is very similar to claim limitations [4.a], [4.b], [6.a], and [6.b]:

Claims 4, 6	**Claim 20**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies. [6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[20.d.3] providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and

1035. For the reasons discussed above with reference to claim limitations [4.a], [4.b], [6.a], and [6.b], the prior art references in Ground 5 satisfy "*providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals*." *Supra* ¶¶799-810, 817-832. For example, the chip select signals provided to the to the array dies are buffered or generated from the chip select signals received by the memory package. *Id*., *see also supra* at ¶¶138-141.

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(4) [20.d.4] Selecting Driver to Drive the Data Signal

1036. Claim 20 requires "*selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals*."

1037. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1038. As shown in the table below, claim limitation [20.d.4] is very similar to claim limitations [11.e.5] and [15.a]:

Claims 11, 15	**Claim 20**
[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[20.d.4] selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals,

1039. As discussed above with reference to claim limitations [11.e.5] and [15.a], the prior art references in Ground 5 satisfy "*selecting one of a first driver*

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and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals." *Supra* ¶¶919-928 (claim limitation [11.e.5]), ¶¶950-962 (claim limitation [15.a]).

(5) [20.e.1] and [20.e.2] First and Second Die Interconnect

1040. Claim 20 requires "*the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

1041. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1042. As shown in the table below, claim limitations [20.e.1] and [20.e.2] are identical to claim limitations [1.d.1] and [1.d.2]:

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Claim 1	**Claim 20**
[1.d.1] the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[20.e.1] the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [20.e.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.

1043. As discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Ground 5 satisfy "*the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,*" and "*the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶727-744.

21. Claim 21 is Unpatentable

1044. Claim 21 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1045. Claim 21 requires "*[t]he method of claim 20, further comprising selecting a first driver size for the first driver based, at least in part, on a load on*

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the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver."

1046. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1047. As shown in the table below, claim 21 is very similar to claim limitation [15.a] and [15.b]:

Claim 15	**Claim 21**
[15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and [15.b] wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.	[21] The method of claim 20, further comprising: selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver.

1048. For the reasons discussed above with reference to claim limitation [15.a] and [15.b], the combination of Riho and Riho2 teaches that a driver size in a stacked arrangement is selected based on the load, including parasitic capacitance and resistance. *Supra* ¶¶950-971; *see, e.g.,* Ex. 1018 (Riho2) at [0097] ("FIG. 7A

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shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance."); *see also supra* at ¶¶135-137. Therefore, the prior art references in Ground 5 satisfy the "*further comprising selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver*" limitation.

22. Claim 22 is Unpatentable

1049. Claim 22 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1050. Claim 22 requires "*[t]he method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*."

1051. The prior art references in each of Ground 5 teach this limitation to a Skilled Artisan.

1052. As shown in the table below, claim 22 is very similar to claim limitation [15.b]:

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Claim 15	Claim 22
[15.b] wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.	[22] The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

1053. As discussed above with reference to claim limitation [15.b], the prior art references in Ground 5 satisfy the "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*" limitation. *Supra* ¶¶963-971.

23. Claim 23 is Unpatentable

1054. Claim 23 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1055. Claim 23 requires "*[t]he method of claim 20, further comprising generating the chip select signals from at least some of the control signals*."

1056. The prior art references in each of Ground 5 teach this limitation to a Skilled Artisan.

1057. As shown in the table below, claim 23 is very similar to claim 16:

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Claim 16	Claim 23
[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and	[23] The method of claim 20, further comprising generating the chip select signals from at least some of the control signals.

1058. As discussed above with reference to claim 16, Ground 5 satisfy the "*further comprising generating the chip select signals from at least some of the control signals*" limitation. *Supra* ¶¶972-979.

24. Claim 24 is Unpatentable

1059. Claim 24 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1060. Claim 24 requires "*[t]he method of claim 20, wherein the control signals include the chip-select signals*."

1061. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1062. As shown in the table below, claim 24 is very similar to claim [4.a] and [4.b]:

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Claim 4	**Claim 24**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.	[24] The method of claim 20, wherein the control signals include the chip-select signals.

1063. As discussed above with reference to claim [4.a] and [4.b], the prior art references in Ground 5 satisfy "*wherein the control signals include the chip-select signals*." *Supra* ¶¶800-810. A Skilled Artisan would have understood that, according to the JEDEC standard, the signals indicating the "*command*" (e.g., read or write) include "CS#," i.e., the "*chip-select signal*." *See, e.g.*, Ex. 1019 (JESD79-3C) at pp.13, 33.

25. Claim 25 is Unpatentable

1064. Claim 25 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1065. Claim 25 requires "*[t]he method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias*."

1066. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1067. As shown in the table below, claim 25 is very similar to claim 5:

Claim 5	**Claim 25**
[5] The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.	[25] The method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias.

1068. As discussed above with reference to claim 5, the prior art references in Ground 5 satisfy "*[t]he method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias*." *Supra* ¶¶811-816.

26. Claim 26 is Unpatentable

1069. Claim 26 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1070. Claim 26 requires "*[t]he method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die*."

1071. The prior art references in each of Ground 5 teach this limitation to a Skilled Artisan.

1072. As shown in the table below, claim 26 is very similar to claim 12:

Claim 12	**Claim 26**
[12] The memory package of claim 11, wherein the chip select conduits pass through the control die.	[26] The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die.

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1073. For the reasons discussed above with reference to claim 12, the prior art references in Ground 5 satisfy the "*wherein the chip select signals pass through through-silicon-vias in the control die*" limitation. *Supra* ¶¶929-935. For example, it was well known at the time to use through-silicon vias for passing signals through a die. *See*, *e.g.*, Ex. 1001 (the 060 Patent) at 1:49-2:7 and Figs. 1A and 1B (describing prior art using vias for chip select signals); Ex. 1014 at [0046] ("Recently, a through-silicon via (TSV) type semiconductor apparatus has been developed in which silicon vias are formed to pass through the plurality of stacked chips so that all of the chips are electrically connected to one another."); *see also* Ex. 1016 (Riho) at Fig. 1, [0030] (describing using TSVs for communicating data, address, and control signals, including chip select signals, in stacked die structure).

27. Claim 27 is Unpatentable

1074. Claim 27 is unpatentable as the prior art references in Ground 5 render the claim obvious.

a) [27.a] Generating Data Path Control Signals from Control Signals

1075. Claim 27 requires "*[t]he method of claim 20, further comprising generating data path control signals from at least some of the control signals*."

1076. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

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1077. As shown in the table below, claim limitation [27.a] is very similar to claim 3:

Claim 3	**Claim 27**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[27.a] The method of claim 20, further comprising generating data path control signals from at least some of the control signals,

1078. As discussed above with reference to claim 3, the "*further comprising generating data path control signals from at least some of the control signals*," limitation. *Supra* ¶¶787-798.

b) [27.b] Data Path Control Signals Being Used to Select First and Second Driver

1079. Claim 27 requires "*the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal*."

1080. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1081. As shown in the table below, claim limitation [27.b] is very similar to claim 3 and claim limitations [11.e.5] and [15.a]:

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Claims 3, 11, 15	**Claim 27**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[27.b] the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal.

1082. As discussed above with reference to claim 3 and claim limitations [11.e.5] and [15.a], the prior art references in Ground 5 satisfy "*the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal*." *Supra* ¶¶787-798 (claim 3), ¶¶919-928 (claim limitation [11.e.5]), ¶¶950-962 (claim limitation [15.a]).

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28. Claim 28 is Unpatentable

1083. Claim 28 is unpatentable as the prior art references in Ground 5 render the claim obvious.

1084. Claim 28 requires "*[t]he method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals*."

1085. The prior art references in Ground 5 teach this limitation to a Skilled Artisan.

1086. As shown in the table below, claim 28 is very similar to claim 3 and claim limitations [11.e.5] and [15.a]:

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Claims 3, 11 and 15	**Claim 28**
[3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals. [11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [15.a] The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and	[28] The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals.

1087. For the reasons discussed above with reference to claim 3 and claim limitations [11.e.5] and [15.a], the prior art references in Ground 5 satisfy "*wherein the one of the first driver and the second driver is selected using at least some of the control signals*." *Supra* ¶¶787-798 (claim 3), ¶¶919-928 (claim limitation [11.e.5]), ¶¶950-962 (claim limitation [15.a]).

29. Claim 29 is Unpatentable

1088. Claim 29 is unpatentable as the prior art references in each of Grounds 4 and 5 render the claim obvious.

a) [29.a] Memory Module

1089. The preamble of claim 29 requires "*[a] memory module operable via a memory control hub, comprising*."

1090. To the extent the preamble is limiting, the prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1091. The combination of Riho and Rajan discloses a "*memory module operable via a memory control hub.*"

1092. Riho discloses that stacked memory devices can be used in a memory module. Ex. 1016 at [0003-4]. As discussed above, it would have been obvious to combine the teaching of Riho and Rajan. *Supra* ¶¶683-692. Rajan discloses a "*memory module,*" such as a DIMM, that includes stacked memory devices. *See, e.g.*, Ex. 1015 at Fig. 8 (reproduced below), 8:52-54 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804….").

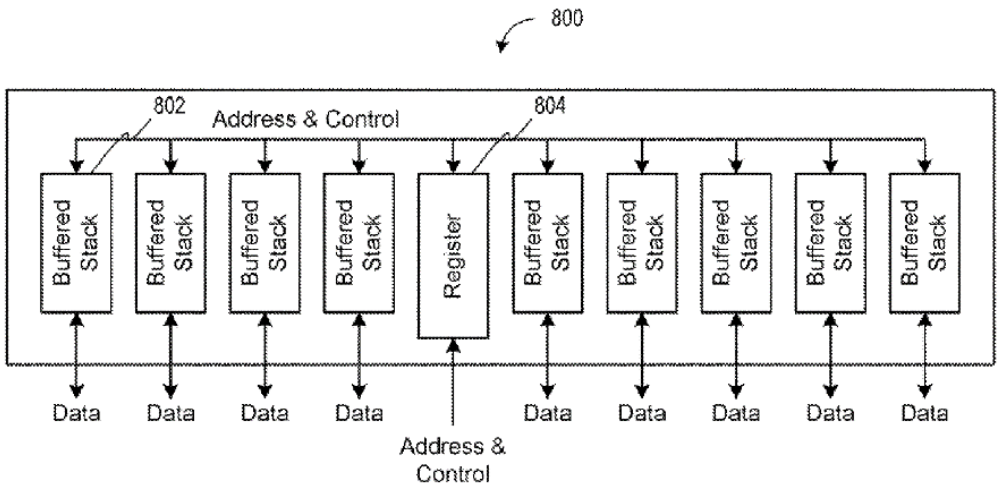


FIG. 8

1093. Riho also discloses stacked memory devices. *See, e.g.*, Ex. 1016 at [0002] ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips.").

1094. As discussed above, a Skilled Artisan would have understood and been motivated to implement Riho's stacked memory devices in a memory module as disclosed by Rajan. *Supra* ¶¶683-692; *see, e.g.*, Ex. 1015 at 1:28-32 ("In other systems, groups of memory chips are first coupled into memory modules, such as dual in-line memory modules (DIMMs), which are in turn coupled into a system by means of slots, sockets, or other connectors."), 15:3-12 ("The physical memory circuits employed in practicing this invention may be any type of memory whatsoever … The physical memory circuits may be coupled to any type of

memory module…"). For example, a Skilled Artisan would have been motivated to implement Riho's stacked devices in a DIMM format so that it can be used in systems that include sockets for DIMMs.

1095. Rajan further explains that its "system may include a memory controller (not shown) through which it accesses the memory circuits." Ex. 1015 at 3:5-7. A Skilled Artisan would have understood that Rajan's memory controller can include "*a memory control hub.*" *See, e.g.*, Ex. 1037 (Rothman) at Fig. 1, 1:34-39 ("FB-DIMMs can be connected via high speed serial interfaces to a Memory Controller Hub (MCH). The AMB communicates with the MCH via the high speed serial interfaces and with RAM ICs on the DIMM via the internal memory bus. The AMB reads from and writes to the RAM as instructed by the MCH and can also be used to configure the FB-DIMM."); Ex. 1022 at 315-20, Figure 7.2 (annotated below) ("Figure 7.2 illustrates [as of 2008] DRAM's place in a typical PC. An individual DRAM device typically connects indirectly to a CPU (i.e., a microprocessor) through a memory controller"), Figure 7.6 ("JEDEC style memory bus organization"). A POSITA would also know that the memory controller could be integrated into the CPU package (to the left in the figure below) rather than in a separate chip (as shown below); both were known options at the time.

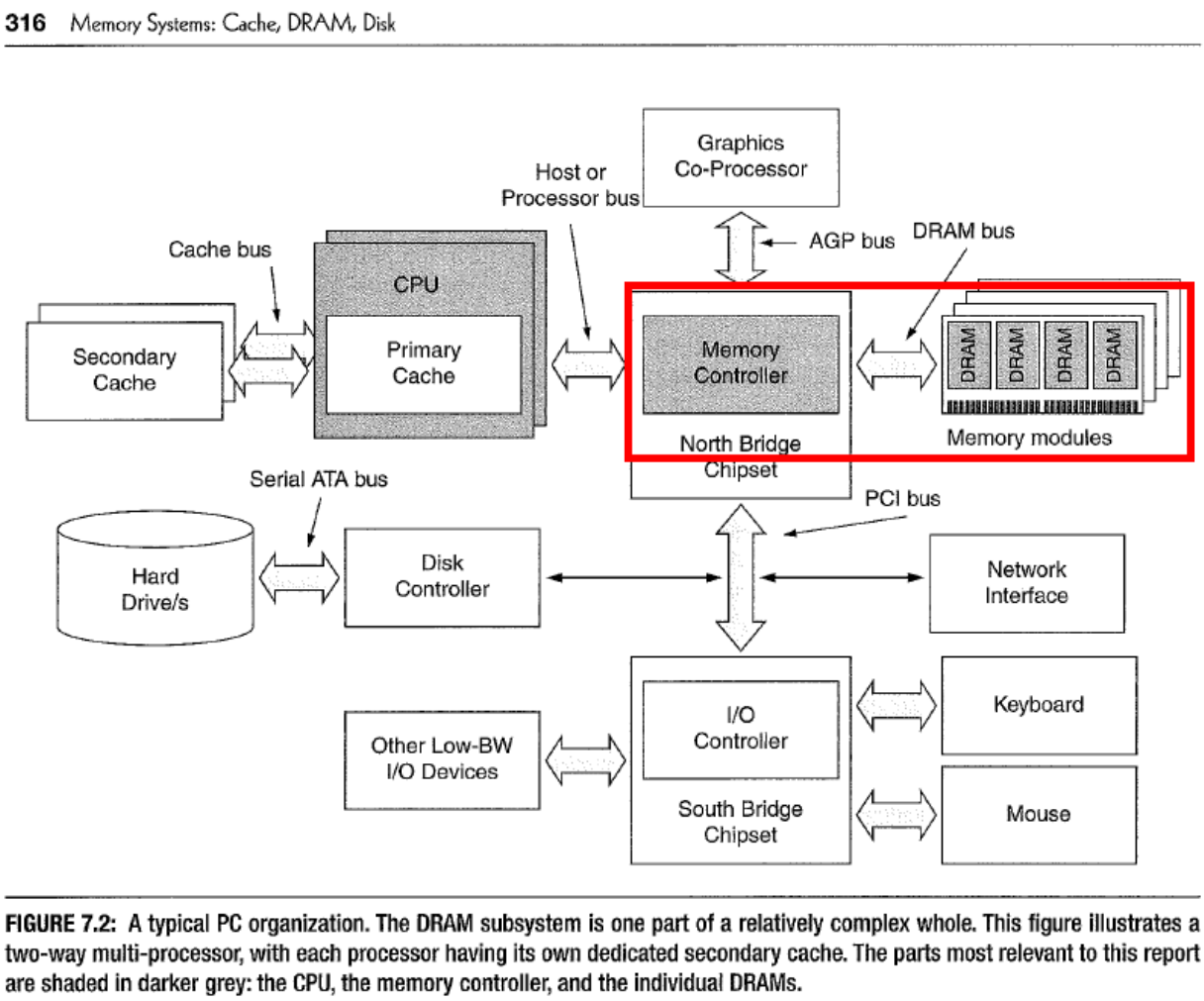


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

1096. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1097. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*[a] memory module operable via a memory control hub, comprising*."

b) [29.b] Register Device

1098. Claim 29 requires "*a register device configured to receive command/address signals from the memory control hub and to generate control signals*."

1099. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1100. The combination of Riho and Rajan discloses "*a register device configured to receive command/address signals from the memory control hub and to generate control signals*."

1101. For example, Rajan discloses a register 804 that receives command/address signals from the memory controller. Ex. 1015 at Fig. 8 (reproduced below), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention. The register performs the addressing and control of the buffered stacks. In some embodiments, the DIMM may be an FB-DIMM, in which case the register is an AMB. In one embodiment the emulation is performed at the DIMM level."); *see also* Ex. 1022 at 418-19 ("Registered Memory Module (RDIMM)"), 43-44 ("Fully Buffered DIMM," "FB-DIMM: Basics," "Advanced Memory Buffer," "AMB").

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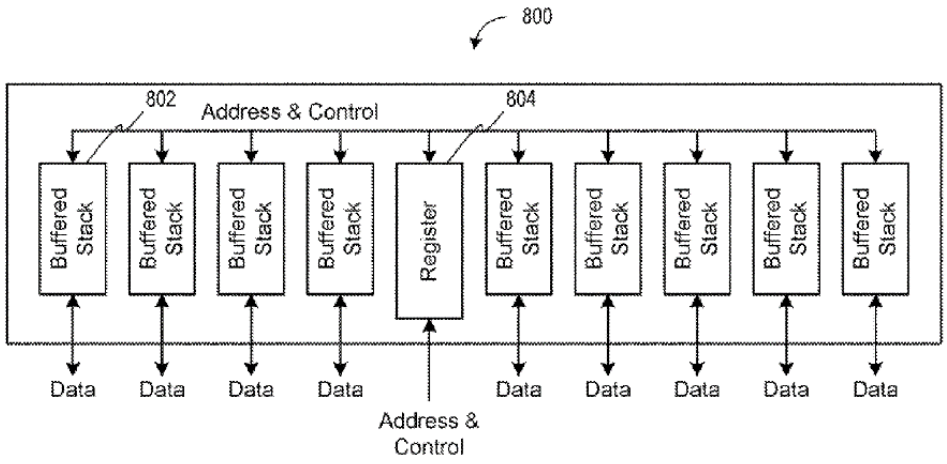


FIG. 8

Rajan also discloses that its register is generating "Address & Control" signals in response. *Id*.; *see also* claim 30, *infra* ¶¶1142-1149 (further discussing the register generating control signals).

1102. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1103. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*a register device configured to receive command/address signals from the memory control hub and to generate control signals; and*."

c) [29.c] DRAM packages

1104. Claim 29 requires "*a plurality of DRAM packages, each DRAM package comprising*."

1105. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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1106. The combination of Riho and Rajan discloses a memory module including "*a plurality of DRAM packages***,**" such as buffered stacked DRAM circuits. Ex. 1015 at Fig. 8 (reproduced above), 8:52-58 ("FIG. 8 illustrates a high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804, according to one embodiment of this invention."); *see also Supra* ¶¶706-710 (claim limitation [1.a], discussing relevant disclosure by Riho).

1107. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1108. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*a plurality of DRAM packages, each DRAM package comprising*."

d) [29.d] Terminals

(1) [29.d.1] Plurality of Data Terminals

1109. Claim 29 requires "*a plurality of data terminals via which the DRAM package communicates data with the memory control hub, and*."

1110. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1111. As shown in the table below, claim limitation [29.d.1] is very similar to claim limitation [1.b]:

Claim 1	**Claim 29**
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[29.d.1] a plurality of data terminals via which the DRAM package communicates data with the memory control hub, and

1112. For the reasons discussed above with reference to claim limitation [1.b], the prior art references in Grounds 4 and 5 satisfy "*a plurality of data terminals via which the DRAM package communicates data with the memory control hub*." *Supra* ¶¶711-718.

(2) [29.d.2] Plurality of Control Terminals

1113. Claim 29 requires "*a plurality of control terminals to receive the control signals*."

1114. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1115. As shown in the table below, claim limitation [29.d.2] is very similar to claim limitation [1.b]:

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Claim 1	Claim 29
[1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;	[29.d.2] a plurality of control terminals to receive the control signals;

1116. For the reasons discussed above with reference to claim limitation [1.b], the prior art references in Grounds 4 and 5 satisfy "*a plurality of control terminals to receive the control signals*." *Supra* ¶¶711-718.

e) [29.e] Array Dies in a Stack

1117. Claim 29 requires "*a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die*."

1118. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1119. As shown in the table below, claim limitation [29.e] is very similar to claim limitation [1.c]:

Claim 1	Claim 29
[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;	[29.e] a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die

1120. For the reasons discussed above with reference to claim limitation [1.c], the prior art references in Grounds 4 and 5 satisfy *a plurality of array dies*

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arranged in a stack, including a first group of array dies and a second group of at least one array die." *Supra* ¶¶719-726.

f) [29.f] First Die Interconnect

1121. Claim 29 requires "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*."

1122. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1123. As shown in the table below, claim limitation [29.f] is identical to claim limitations [1.d.1] and [1.d.2]:

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Claim 1	**Claim 29**
[1.d.1]-[1.d.2] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	[29.f] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

1124. For the reasons discussed above with reference to claim limitations [1.d.1] and [1.d.2], the prior art references in Grounds 4 and 5 satisfy "*at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies*." *Supra* ¶¶727-744.

g) [29.g] Control Die

(1) [29.g.1] A Control Die Comprising

1125. Claim 29 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1126. Claim 29 requires "*a control die comprising*."

1127. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1128. As shown in the table below, claim limitation [29.g.1] is identical to claim limitation [1.e.1]:

Claim 1	**Claim 29**
[1.e.1] a control die comprising	[29.g.1] a control die comprising

1129. For the reasons discussed above with reference to claim limitation [1.e.1], the prior art references in Grounds 4 and 5 satisfy "*a control die comprising*." *Supra* ¶¶745-752.

(2) [29.g.2] First and Second Data Conduit

1130. Claim 29 requires "*at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and*."

1131. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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1132. As shown in the table below, claim limitation [29.g.2] is nearly identical to claim limitations [1.e.2] and [1.e.3]:

Claim 1	**Claim 29**
[1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and [1.e.3] at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,	[29.g.2] at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and

1133. For the reasons discussed above with reference to claim limitations [1.e.2] and [1.e.3], the prior art references in Grounds 4 and 5 satisfy "*at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal*." *Supra* ¶¶753-769.

(3) [29.g.3] Chip Select Conduits

1134. Claim 29 requires "*chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals*."

1135. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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1136. As shown in the table below, claim limitation [29.g.3] is very similar to claim limitations [4.a], [4.b], [6.a], and [6.b]:

Claims 4, 6	**Claim 29**
[4.a] The memory package of claim 3, wherein the control signals include command/address signals and [4.b] wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies. [6.a] The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising: [6.b] third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.	[29.g.3] chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

1137. For the reasons discussed above with reference to claim limitations [4.a], [4.b], [6.a], and [6.b], the prior art references in Grounds 4 and 5 satisfy "*chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals*." *Supra* ¶¶799-810, 817-832. For example, the chip select signals provided to the array

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dies are buffered or generated from the chip select signals received by the memory package. *Id*., *see also supra* at ¶¶138-141.

(4) [29.g.4] Control Circuit

1138. Claim 29 requires "*wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals*."

1139. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1140. As shown in the table below, claim limitation [29.g.4] is identical to claim limitation [11.e.5]:

Claim 11	**Claim 29**
[11.e.5] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.	[29.g.4] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

1141. For the reasons discussed above with reference to claim limitation [11.e.5], the prior art references in Grounds 4 and 5 satisfy "*wherein the control die further comprises a control circuit to control respective states of the first data*

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conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals." *Supra* ¶¶919-928.

30. Claim 30 is Unpatentable

1142. Claim 30 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1143. Claim 30 requires "*[t]he memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals*."

1144. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1145. The combination of Riho and Rajan discloses that "*the **register** device is further configured to perform **rank multiplication** by generating the chip select signals, and wherein the control signals include the chip select signals.*"

1146. For example, as discussed above with reference to claim limitation [1.c], Rajan discloses emulating characteristics, including rank multiplication. *Supra* ¶¶138-140, 719-726; *see, e.g.*, Ex. 1015 at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits."). Rajan further discloses that "the DIMM may be an FB-DIMM, in which case the register

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is an AMB. In one embodiment the emulation is performed at the DIMM level." *Id.* at 8:56-58.

1147. A Skilled Artisan would have understood from this disclosure that the AMB can perform rank multiplication, and generate chip select signals for additional ranks. *See supra* ¶¶138-140; *see also* Ex. 1001 (060 Patent) at 18:45-51 ("The 3DS register 712 may include a DDR3 JEDEC standard register with a 'rank multiplication' circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller."), 22:34-40 (describing that rank multiplication was prior art: "Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 and 7,532,537"); Ex. 1028 (U.S. Pat. No. 7,289,386); Ex. 1031 (U.S. Pat. No. 7,532,537), Ex. 1015 (Rajan) at 6:30-7:67 ("If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.")

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1148. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1149. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*[t]he memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals*."

31. Claim 31 is Unpatentable

1150. Claim 31 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1151. Claim 31 requires "*[t]he memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

1152. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1153. As shown in the table below, claim 31 is very similar to claim limitations [29.b] and [29.g.4] and claims 2 and 30:

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Claims 2, 29, 30	**Claim 31**
[29.b] a register device configured to receive command/address signals from the memory control hub and to generate control signals; and [29.g.4] wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals. [30] The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals. [2] The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.	[31] The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

1154. For the reasons discussed above with reference to claim limitations [29.b] and [29.g.4] and claims 2 and 30, the prior art references in Grounds 4 and 5

satisfy this limitation. *Supra* ¶¶1098-1103 (claim limitation [29.b]), ¶¶1138-1141 (claim limitation [29.g.4]), ¶¶779-786 (claim 2), ¶¶1142-1149 (claim 30).

1155. The combination of Riho and Rajan discloses to a Skilled Artisan that "*the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.*"

1156. As discussed above with reference to claim limitations [29.b] and [29.g.4], the Riho and Rajan combination discloses a register device that generates chip select signals. *Supra* ¶¶1098-1103 (claim limitation [29.b]), ¶¶1138-1141 (claim limitation [29.g.4]). As further discussed above with reference to claim 2, the memory package receives the control signals which include "*data path control signals being used to control the respective states of the first data conduit and the second data conduit*." *Supra* ¶¶779-786.

1157. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1158. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*[t]he memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

32. Claim 32 is Unpatentable

1159. Claim 32 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1160. Claim 32 requires "*[t]he memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal*."

1161. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1162. As shown in the table below, claim 32 is very similar to claim 16:

Claim 16	**Claim 32**
[16] The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.	[32] The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.

1163. For the reasons discussed above with reference to claim 16, the prior art references in Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶972-979.

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1164. The combination of Riho and Rajan discloses to a Skilled Artisan that "*the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.*"

1165. For example, as discussed above with reference to claim limitation [1.c] and claim 16, Rajan discloses that the control die emulates characteristics, including rank multiplication. *Supra* ¶¶719-726 (claim limitation [1.c]), ¶¶972-979 (claim 16); *see, e.g.,* Ex. 1015 at 3:27-30 ("For example, the interface circuit may tell the system device that the number of emulated memory circuits is different than the actual number of physical memory circuits.").

1166. Furthermore, as discussed with reference to claim 16, Rajan also discloses "*generating the chip select signals from at least some of the control signals that include at least one address signal.*" *Supra* ¶¶972-979.

1167. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1168. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*[t]he memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal*."

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33. Claim 33 is Unpatentable

1169. Claim 33 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1170. Claim 33 requires "*[t]he memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

1171. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1172. The combination of Riho and Rajan discloses that "*the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

1173. For example, Rajan discloses that the control chip receives command/address signals for a write command and holds those signals for an additional time to control timing of when the DRAMs receive those signals. Ex. 1015 at Fig. 11 (reproduced below), 10:12-19 ("The memory controller issues the write operation at t0. In FIG. 10, the write operation appeared at the DRAM circuits one clock later at t1, due to the inherent delay through the buffer chip. But in FIG. 11, in addition to the inherent one clock delay, the buffer chip has added an

extra two clocks of delay to the write operation, which is not issued to the DRAM chips until t0+1+2=t3.").

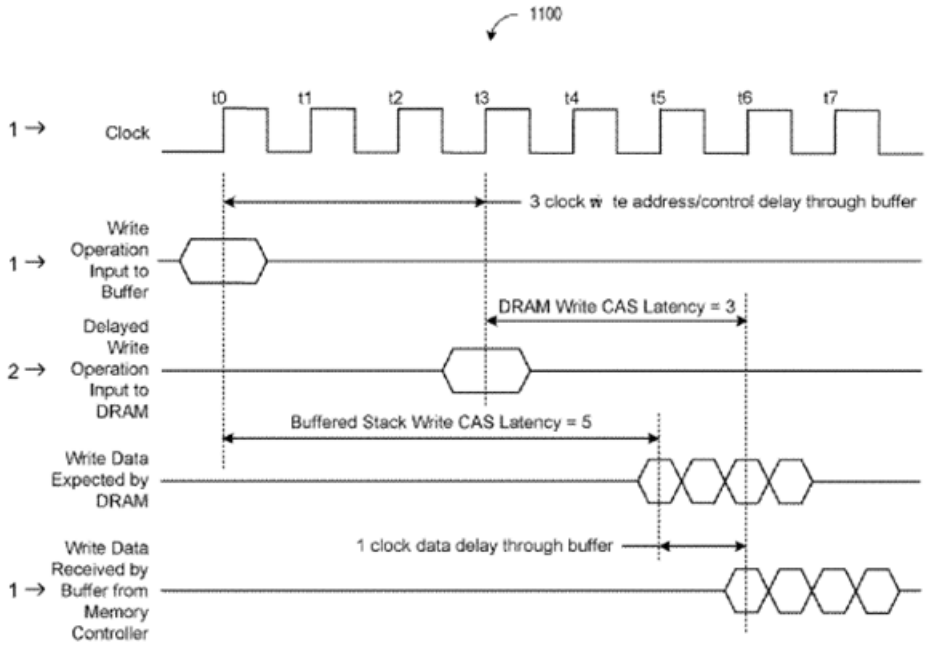


FIG. 11

1174. A Skilled Artisan would have been motivated to implement this delay of command/address signals in Riho's device to emulate certain characteristics as taught by Rajan. *See, e.g.,* Ex. 1015 at 9:61-10:4 ("In the specific example shown, the memory controller issues the write operation at t0. After a one clock cycle delay through the buffer chip, the write operation is issued to the DRAM chips at t1. Because the memory controller believes it is connected to memory having a read CAS latency of six clocks and thus a write CAS latency of five clocks, it issues the write data at time t0+5=t5. But because the physical DRAM chips have a read CAS latency of four clocks and thus a write CAS latency of three clocks, they

expect to receive the write data at time t1+3=t4. Hence the problem, which the buffer chip may alleviate by delaying write operations."); *see also* Ex. 1019, at 23-24 ("CAS latency").

1175. Therefore, the combination of Riho and Rajan renders obvious this limitation to a Skilled Artisan.

1176. Accordingly, the prior art references in Grounds 4 and 5 satisfy "*[t]he memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals*."

34. Claim 34 is Unpatentable

1177. Claim 34 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

1178. Claim 34 requires "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*."

1179. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1180. As shown in the table below, claim 34 is very similar to claim limitation [1.e.4] and claim 3:

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Claims 1, 3	**Claim 34**
[1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals. [3] The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.	[34] The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

1181. For the reasons discussed above with reference to claim limitation [1.e.4] and claim 3, the prior art references in Grounds 4 and 5 satisfy "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit*." *See* ¶¶770-778 (claim limitation [1.e.4]), ¶¶787-798 (claim 3).

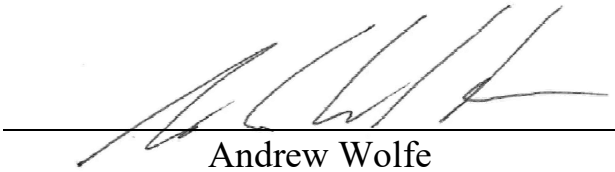
* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief

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are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 26, 2022



Andrew Wolfe

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 8,787,060 (issued July 22, 2014)
1002	File History of U.S. Patent No. 8,787,060 (Application No. 13/288,850 filed Nov. 3, 2011)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 61/409,893 (filed Nov. 3, 2010)
1006	File History of U.S. Patent Application No. 14/337,168 (filed July 21, 2014)
1007	File History of U.S. Patent Application No. 15/095,288 (filed Apr. 11, 2016)
1008	File History of U.S. Patent Application No. 15/602,099 (filed May 22, 2017)
1009	File History of U.S. Patent Application No. 16/412,308 (filed May 14, 2019)
1010	File History of U.S. Patent Application No. 17/157,903 (filed Jan. 25, 2021)
1011	U.S. Patent Application Publication No. 2008/0025137 to Rajan *et al.* (published Jan. 31, 2008)
1012	U.S. Patent Application Publication No. 2011/0193226 to Kirby *et al.* (filed Feb. 8, 2010, published Aug. 11, 2011)
1013	U.S. Patent Application Publication No. 2006/0259678 to Gervasi (published Nov. 16, 2006)
1014	U.S. Patent Application Publication No. 2011/0103156 to Kim *et al.* (filed Dec. 29, 2009, published May 5, 2011)

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Exhibit #	Description
1015	U.S. Patent No. 8,041,881 to Rajan *et al.* (filed June 12, 2007, issued Oct. 18, 2011)
1016	U.S. Patent Application Publication No. 2011/0026293 to Riho (filed July 16, 2010, published Feb. 3, 2011)
1017	U.S. Patent No. 7,969,192 to Wyman *et al.* (filed Mar. 26, 2010, issued June 28, 2011)
1018	U.S. Patent Application Publication No. 2010/0195364 to Riho (published Aug. 5, 2010) ("Riho2")
1019	JEDEC DDR3 SDRAM Standard, JESD79-3C (Nov. 2008)
1020	Declaration of Julie Carlson for JESD79-3C
1021	JEDEC MO-207, Square & Rectangular Die-Size, Ball Grid Array Family (Dec. 2010)
1022	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1023	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
1024	U.S. Patent No. 7,796,446 to Ruckerbauer *et al.* (issued Sept. 14, 2010)
1025	U.S. Patent No. 8,258,619 to Foster *et al.* (filed Nov. 12, 2009)
1026	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry *et al.* (published Dec. 7, 2006)
1027	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (Final Written Decision)
1028	U.S. Patent No. 7,289,386 to Bhakta *et al.* (issued Oct. 30, 2007)
1029	Affirmance of the Examiner's Decision on Reexamination of the '386 Patent (Feb. 25, 2015)
1030	Stephen Brown et al., *Fundamentals of Digital Logic* (2d ed. 2008)

Exhibit #	Description
1031	U.S. Patent No. 7,532,537 to Solomon *et al.* (issued May 12, 2009)
1032	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00667, Paper No. 38 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1033	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00668, Paper No. 36 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1034	U.S. Patent No. 8,471,362 to Lee (filed Apr. 5, 2011)
1035	JEDEC Graphics Double Data (GDDR4) SGRAM Specification (Nov. 2005)
1036	[omitted]
1037	U.S. Patent No. 7,890,811 to Rothman *et al.* (filed June 29, 2007, issued Feb. 15, 2011)
1038	Harold S. Stone, Microcomputer Interfacing (1982)
1039	U.S. Patent No. 9,160,349 to Ma (filed Aug. 27, 2009)
1040	[omitted]
1041	U.S. Patent No. 8,129,958 to Bigler *et al.* (filed Dec. 24, 2007)
1042	[omitted]
1043	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1044	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)
1045	Answer to Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 18, 2022)
1046	Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)

Exhibit #	Description
1047	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1048	Federal Court Management Statistics (Mar. 31, 2022), *available at* <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1>

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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory package, comprising:
1.b	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
1.c	a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
1.d.1	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
1.d.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
1.e.1	a control die comprising
1.e.2	at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and
1.e.3	at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,
1.e.4	the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.
2	The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.
3	The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.
4.a	The memory package of claim 3, wherein the control signals include command/address signals and
4.b	wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.

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Ref. #	Listing of Challenged Claims
5	The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.
6.a	The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising:
6.b	third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.
7.a	The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit,
7.b	the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.
8.a	The memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals,
8.b.1	wherein the control die is configurable to operate in any one of a first mode and a second mode, and wherein:
8.b.2	in the first mode, the control die receives the data path control signals from the one or more external devices; and
8.b.3	in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.
9	The memory package of claim 1, wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address.

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Ref. #	Listing of Challenged Claims
10	The memory package of claim 1, wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies.
11.a	A memory package, comprising:
11.b	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
11.c	a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;
11.d.1	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
11.d.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
11.e.1	a control die comprising
11.e.2	at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals,
11.e.3	at least a second data conduit between the second die interconnect and the first terminal, and
11.e.4	chip select conduits for providing chip select signals to respective array dies;
11.e.5	wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.
12	The memory package of claim 11, wherein the chip select conduits pass through the control die.
13	The memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies.

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Ref. #	Listing of Challenged Claims
14	The memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.
15.a	The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and
15.b	wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.
16	The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.
17	The memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.
18	The memory package of claim 16, wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal.
19.a	The memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and
19.b	wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.
20.a	A method for optimizing load in a memory package comprising
20.b.1	a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die,
20.b.2	at least a first die interconnect and a second die interconnect,
20.b.3	a control die, and

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Ref. #	Listing of Challenged Claims
20.b.4	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
20.c	the method comprising:
20.d.1	receiving a data signal at a first terminal of the plurality of input/output terminals;
20.d.2	receiving control signals at second terminals of the plurality of input/output terminals;
20.d.3	providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and
20.d.4	selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals,
20.e.1	the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
20.e.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.
21	The method of claim 20, further comprising: selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver.
22	The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.
23	The method of claim 20, further comprising generating the chip select signals from at least some of the control signals.
24	The method of claim 20, wherein the control signals include the chip-select signals.
25	The method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias.

Ref. #	Listing of Challenged Claims
26	The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die.
27.a	The method of claim 20, further comprising generating data path control signals from at least some of the control signals,
27.b	the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal.
28	The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals.
29.a	A memory module operable via a memory control hub, comprising:
29.b	a register device configured to receive command/address signals from the memory control hub and to generate control signals; and
29.c	a plurality of DRAM packages, each DRAM package comprising:
29.d.1	a plurality of data terminals via which the DRAM package communicates data with the memory control hub, and
29.d.2	a plurality of control terminals to receive the control signals;
29.e	a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;
29.f	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
29.g.1	a control die comprising
29.g.2	at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and
29.g.3	chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

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Ref. #	Listing of Challenged Claims
29.g.4	wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.
30	The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals.
31	The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.
32	The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.
33	The memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals.
34	The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

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