

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Case PGR2025-00071
Case IPR2025-01402
Patent 12,308,087

**DECLARATION OF DR. ANDREW WOLFE
REGARDING U.S. PATENT NO. 12,308,087**

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. (“Samsung”) as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 12,308,087 (“the ’087 Patent”) (EX1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years’ experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world’s leading institutions in those fields, including

Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM and flash memory,

in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

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named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of \$750.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the '087 Patent, I am relying upon certain basic legal principles that have been explained to me.

A. 35 U.S.C. §§ 102 and 103

25. I understand that for an invention claimed in a patent to be found patentable under 35 U.S.C. §§ 102 and 103, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the '087 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below

compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. In this declaration I focus on “obviousness.” My understanding of the legal standard for “obviousness” is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims of the '087 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being

associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors” suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or

derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art

references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was

obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

B. 35 U.S.C. § 112

47. I understand that under 35 U.S.C. § 112, the specification for the patent must (a) contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and (b) conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor(s) regard(s) as the invention.

48. I understand that a claim that lacks “written description” in the specification of the patent is invalid.

49. I understand that the written description inquiry looks to the four corners of the specification to discern the extent to which the inventor(s) had possession of the invention as broadly claimed. I understand that to the extent the specification purports to incorporate by reference, there must be a clear intent to

incorporate by reference that clearly identifies the referenced patent, application, or publication, and that “Essential material” (e.g., material necessary to provide written description) may only be incorporated by reference to a U.S. patent or U.S. patent application publication.

50. I understand that a specification that merely renders the invention *obvious* does *not* satisfy the written description requirement.

51. I understand that a patent that provides a “laundry list” disclosure does not provide adequate written description of every possible combination because such a disclosure would not reasonably lead those skilled in the art to any particular species. I understand that following a maze-like path, each step providing multiple alternative paths, is not a written description of what might have been described if each of the optional steps had been set forth as the only option.

52. I understand that hindsight (e.g., working backward from the knowledge of the claims) is not permitted to satisfy the written description requirement, and thus a patent lacks written description for a claim—even where the patent provides formal textual support for each individual limitation recited in the claims—if the patent nowhere describes the actual functioning invention that those limitations together define.

53. I understand that a patent owner cannot show written description support by picking and choosing claim elements from different embodiments that are never linked together in the specification. Thus, I understand that the written description requirement is not met when the specification provides at best disparate disclosures that an artisan might have been able to combine in order to make the claimed invention. I understand that one cannot disclose a forest in the original application, and then later pick a tree out of the forest and say here is my invention.

54. I understand that, for a negative claim limitation, silence is generally not disclosure. If it were, then every later-added negative limitation would be supported so long as the patent makes no mention of it. I understand that while a negative limitation need not be recited in the specification verbatim, there generally must be something in the specification that conveys to a skilled artisan that the inventor intended the exclusion, such as a discussion of disadvantages or alternatives. However, I understand that it is possible that the written description requirement may be satisfied when a skilled artisan would understand the specification as inherently disclosing a limitation. Thus, if a patent owner could establish that a particular limitation would always be understood by skilled artisans as being necessarily excluded from a particular claimed method or apparatus if that limitation is not mentioned, the written description requirement would be satisfied despite the specification's silence.

55. I understand that a claim that is “indefinite” is invalid.

56. I understand that a claim that is nonsensical is indefinite. I also understand that when claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention, they are indefinite.

57. I understand that indefiniteness of claims is not rendered unobjectionable merely because it *could* have been corrected. I understand that courts may not redraft claims, whether to make them operable or to sustain their validity. However, I understand that obvious minor typographical and clerical errors in patents—evident from the face of the patent—may in some circumstances be corrected by a judge, but only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims.

III. THE '087 PATENT

A. Person of Ordinary Skill in the Art

58. The '087 Patent claims priority back to a non-provisional application filed on November 3, 2011 (EX1069), and a provisional application filed on November 3, 2010 (EX1005). The '087 Patent identifies the relevant field of art as follows: “The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to a memory package having

stacked array dies and methods for reducing driver load in the memory package.” EX1001 at 1:30-35. Based on that description of the field of art, my experience, and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the '087 Patent in 2010 and 2011 (“Skilled Artisan” or “POSITA”) would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

59. My description of a POSITA above is consistent with the description I provided previously in my expert declarations about the related 060 (EX1069) and 160 (EX1071) patents. See EX1091, ¶60; EX1092, ¶60. I understand that the Board, in its Final Written Decisions finding the 060 and 160 patents invalid, agreed with my description of a POSITA “with the exception of the qualifier ‘at least,’ which introduces vagueness as to the amount of experience.” EX1072, 7-9; EX1073, 7-9.

B. Overview of the '087 Patent

60. The '087 Patent states that it “relates to memory devices and memory modules” and, more specifically, “a memory package having stacked array dies and methods for reducing driver load in the memory package.” EX1001 at 1:30-35. The '087 Patent admits as prior art “FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used.” *Id.* at 1:46-48 and Fig. 1B (reproduced below, annotated).

61. For simplicity, the annotation below of Figure 1B and the annotations further below of other figures in the '087 Patent are from my previous expert report on the related 060 Patent, given that the '087 Patent is a continuation of the 060 Patent and thus the figures in the 060 and '087 Patents are substantially identical. See EX1001 Figs.1-8 ('087 Patent); EX1069 Figs.1-8 (060 Patent). Also, Figures 1A and 1B are somewhat distorted in the '087 Patent, and thus those

figures are somewhat easier to read in the 060 Patent, as shown in the annotation of Figure 1B directly below.

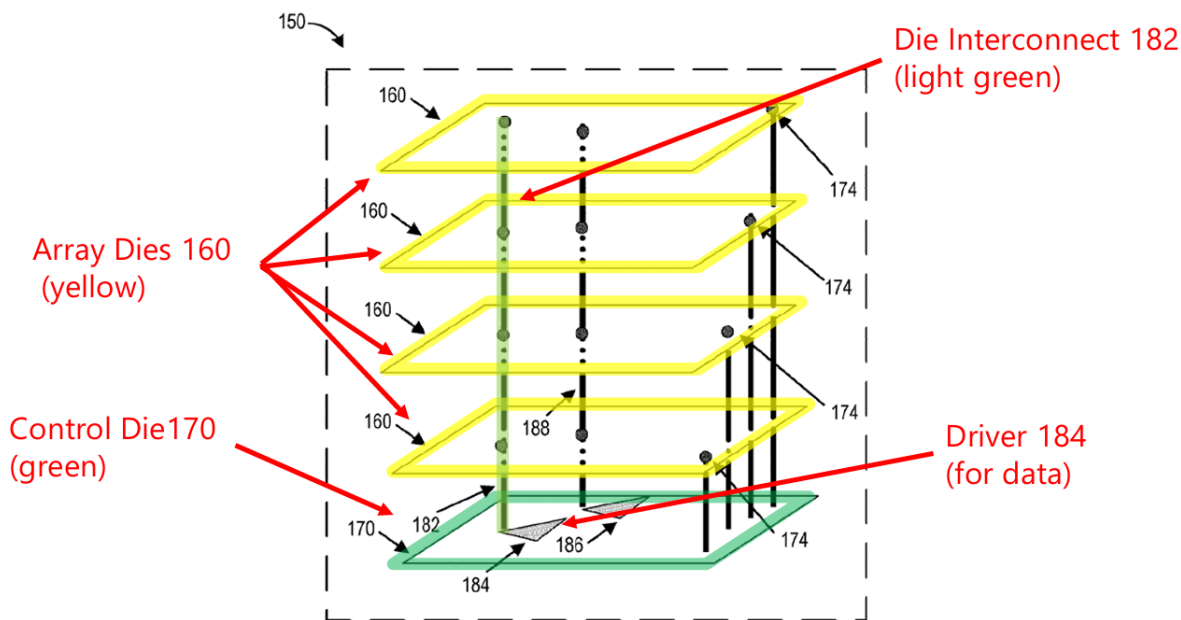


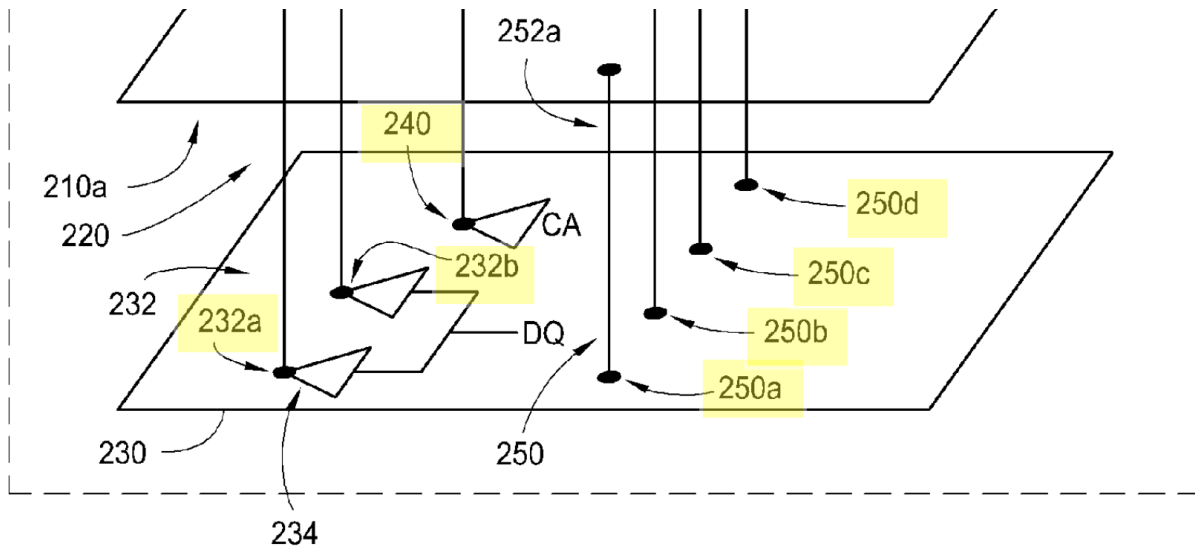
FIG. 1B

EX1092, ¶61.

62. In particular, “FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 [(yellow)] and a control die 170 [(green)] that ... [includes] a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182.” EX1001 at 2:13-22. The ’087 Patent explains that a problem with the prior-art memory package is that the data driver 184 has to drive a load that is “in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large

enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.” *Id.* at 2:25-32.

63. The '087 Patent discloses that each die interconnect has a corresponding “conduit” which is configured to transmit a signal to the die interconnect. EX1001, *e.g.*, at Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b, command/address conduits 240, and chip select conduits 250a-d), 6:35-47 (describing data conduits 232a and 232b), 9:18-51 (describing command/address conduits 240 and chip select conduits 250). A “conduit” may, but does not have to, include a driver to drive the load on the conduit. *Id.*; *see also* 6:48-50 (“In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2.”), 21:1-3 (“The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.”).



64. The '087 Patent solves the prior art's problem of having too much load on the data conduits by replacing one data driver of the prior art with two (or more) drivers 234 coupled to the same DQ data terminal, each of the drivers driving the data signal through a respective die interconnect (220a, 220b) that is in electrical communication with *a subset* of the array dies, thus reducing the overall load of each data conduit. EX1001 at 6:64-8:6 and Fig. 2 (reproduced below, annotated). This was a well-known and ordinary solution to driving multiple loads from a single signal.

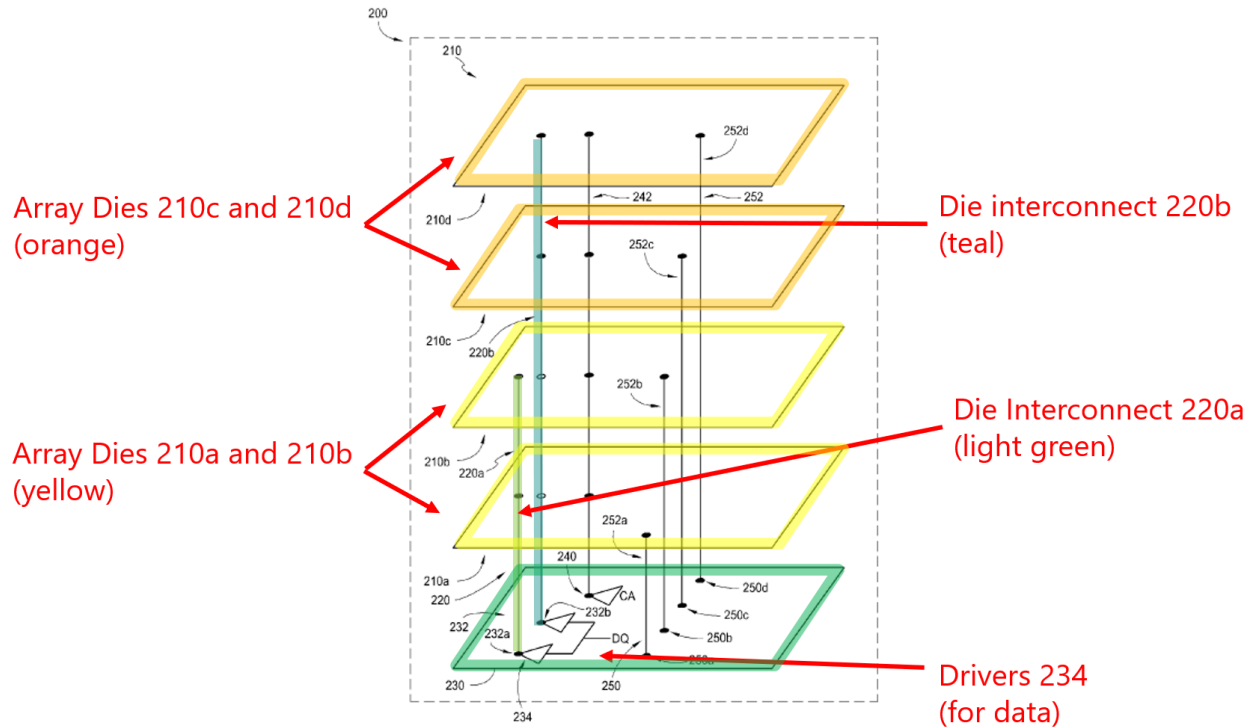


FIG. 2

65. In the example of Fig. 2, “die interconnect 220a [(light green)] may be in electrical communication with a data port from array die 210a [(yellow)] and a data port from array die 210b [(yellow)] (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c [(orange)] or any data ports from array die 210d [(orange)].” EX1001 at 5:48-53. The other “die interconnect 220b [(teal)] may be in electrical communication with a data port from array die 210c [(orange)] and a data port from array die 210d [(orange)] (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., 00) without being in electrical communication with any data ports from array die 210a [(yellow)] and array die

210b [(yellow)].... Despite not being in electrical communication with any data ports from array die 210a and 210b [(yellow)], in some implementations, the die interconnect 220b [(teal)] may pass through the array dies 210a and 210b [(yellow)] (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b.” *Id.* at 5:61-6:8.

66. In another example, the '087 Patent discloses selecting the number of array dies that are connected to a die interconnect in order to reduce the difference between the loads on the different conduits. EX1001 at Fig. 3 and Table 1 (reproduced below). Here, the memory package 300 includes eight array dies 310a-310h and a control die 330. *Id.* at 10:10-32. The control die includes six conduits 332a-f with respective drivers 334a-334f, each driving a signal along a respective die interconnect 320a-f. *Id.* at 10:27-47. Each of the shorter interconnects 320a and 320b is connected to two array dies, and each of the longer interconnects 320c-f is connected to a single array die. *Id.* “In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320.” *Id.* at 10:48-54. The capacitive load on each conduit is

calculated based on both the length of the interconnect and the number of connected array dies, as shown below in Table 1.

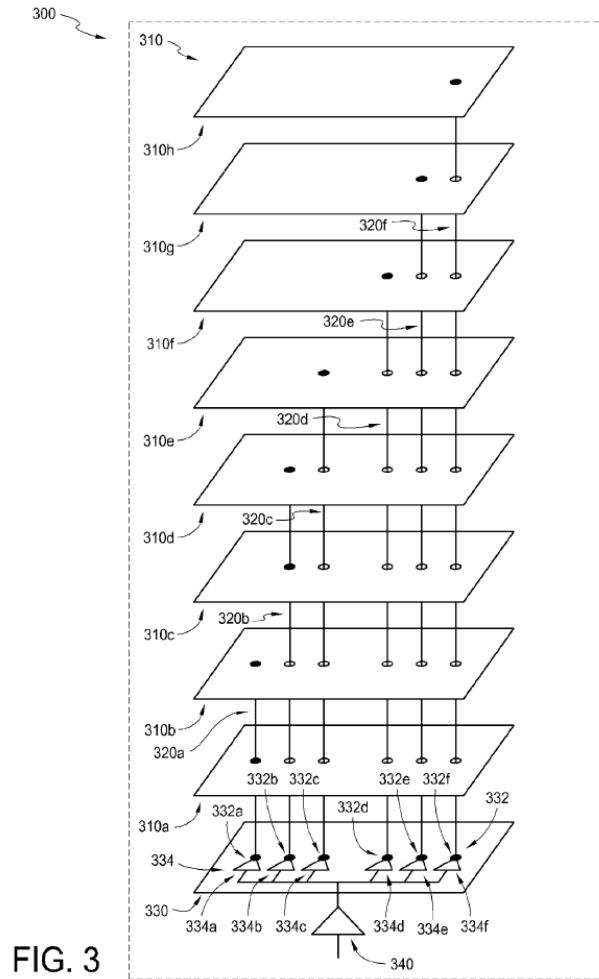


TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5 L	0.5
332b	2	4	3 L	0
332c	1	5	2.25 L	0.75
332d	1	6	2.5 L	0.5
332e	1	7	2.75 L	0.25
332f	1	8	3 L	0

“Table 1 specifies the capacitive load values for each conduit 332 assuming ... that the load of each of the array dies 310 is L , and that the load of each segment of the die interconnects 320 is $0.25L$. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f.” *Id.* at 12:49-66. “As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is $3L$, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be $10L$.” *Id.* at 13:1-7. The '087 Patent further explains that such a die interconnect in electrical communication with each die “does not implement the teachings of this disclosure, but is in accordance with conventional configurations.” EX1001 at 7:15-17.

67. Figure 4, reprinted below, “illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. . . . In some embodiments, the control die 230 may include the driver structure 400 in place of the combination of drivers 232 a and 232 b.” EX1001 at 15:8-16. “The driver structure 400 can include an input/output port 402 configured to receive or send a signal, such as a data signal. Signals received at the input/output port 402 can be provided to the drivers 404 a and 404 b. In turn, these drivers 404 a and 404 b can drive the signal to conduits 406 a and 406 b

respectively, which are in electrical communication with corresponding die interconnects.” *Id.* at 15:21-27. “In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404 a and 404 b, and 408 a and 408 b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal. In some implementations, the drivers 404 a and 404 b may drive a signal to the array die corresponding to the chip select signal, and not to array dies that do not correspond to a chip select signal.” *Id.* at 15:31-40.

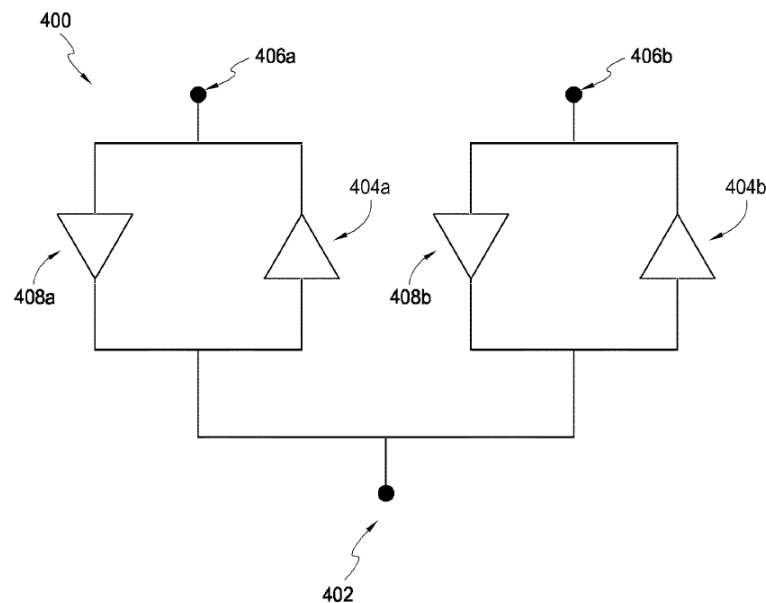


FIG. 4

C. The Prosecution History of the '087 Patent

68. The '087 Patent is the last of several continuation applications dating back to November 3, 2011, and a provisional application filed November 3, 2010, as shown below:

Related U.S. Application Data

- (63) Continuation of application No. 17/157,903, filed on Jan. 25, 2021, now abandoned, which is a continuation of application No. 16/412,308, filed on May 14, 2019, now Pat. No. 10,902,886, which is a continuation of application No. 15/602,099, filed on May 22, 2017, now Pat. No. 10,290,328, which is a continuation of application No. 15/095,288, filed on Apr. 11, 2016, now Pat. No. 9,659,601, which is a continuation of application No. 14/337,168, filed on Jul. 21, 2014, now Pat. No. 9,318,160, which is a continuation of application No. 13/288,850, filed on Nov. 3, 2011, now Pat. No. 8,787,060.
- (60) Provisional application No. 61/409,893, filed on Nov. 3, 2010.

EX1001 at 1-2.

69. In my previous expert declarations on the 060 and 160 Patents, I summarized the prosecution histories of all of the applications shown above. See EX1091, ¶¶ 67-111; EX1092, ¶¶ 66-111; *see also* EX1005, EX1070, EX1006-EX1010 (prosecution histories).

70. Since then, on April 1, 2024, the Board invalidated all claims of the 060 and 160 Patents, consistent with the opinions I offered about those patents in

my previous expert declarations. EX1072; EX1073. Specifically, for the 060 Patent, the Board (1) found Claims 1-6, 8-14, 16-19, and 29-34 unpatentable because they were obvious over U.S. Patent Publication No. 2011/0103156 to Kim (“Kim”) (EX1014) and U.S. Patent No. 8,041,881 to Rajan (“Rajan”) (EX1015), (2) found Claims 1-14, 16-19, and 29-34 unpatentable because they were obvious over Kim, Rajan, and U.S. Patent Publication No. 2011/0026293 to Riho (“Riho”) (EX1016), and (3) found Claims 1-6 and 8-34 unpatentable because they were obvious over Kim, Rajan, and U.S. Patent No. 7,969,192 to Wyman (“Wyman”) (EX1017). EX1072, 2-3, 74; EX1074. For the 160 Patent, the Board found Claims 1-20 unpatentable because they were obvious over Kim, Rajan, and Wyman. EX1073, 2-3, 67; EX1074. I understand that Netlist has appealed the Board’s decisions invalidating the claims of the 060 and 160 Patents. EX1075; EX1076.

71. Below is a summary of the prosecution history of the ’087 Patent (Application No. 17/694,649), which was filed as a continuation of the most recent application shown above (Application No. 17/157,903).

72. Application No. 17/694,649 was filed on March 14, 2022, as a continuation of the applications shown above. EX1002, 3-4, 58, 64.

73. On October 5, 2022, the Examiner rejected all pending claims for non-statutory double patenting as being “not patentably distinct” from claims in

U.S. Patent Nos. 8,787,060; 9,318,160; 9,659,601; 10,290,328; and 10,902,886.

EX1002, 45, 103-16.

74. On April 5, 2023, the applicants responded to this rejection by amending the pending claims and adding eighteen (18) more claims. EX1002, 143-52. The applicants also filed a terminal disclaimer over U.S. Patent Nos. 8,787,060; 9,318,160; 9,659,601; 10,290,328; and 10,902,886. EX1002, 150-51, 158-60, 163, 261-62.

75. On July 12, 2023, the Examiner issued a Final Rejection, rejecting all pending claims for failing to comply with the written description requirement under § 112(a). EX1002, 201-06. The Examiner stated that claim limitations, such as “a second plurality of TSVs” in the claimed interconnect lacked written description support because the specification disclosed that the “interconnect corresponds to only a TSV, not a plurality of TSVs.” *Id.* at 203-04. The Examiner also found certain limitations indefinite. *Id.* at 205.

76. On September 12, 2023, as part of a request for consideration under the After Final Consideration Pilot Program 2.0 (AFCP 2.0), EX1002, 221, the applicants responded to the Final Rejection. EX1002, 207-17. The applicants argued that the specification did support “a plurality of TSVs,” citing paragraph [0040] and FIGs. 2-3 of the application, EX 1002, 214-17. The applicants argued that the cited paragraph and figures provided written description support “that a die

interconnect can include a plurality of TSVs, one for each die, which the die interconnect either connects with or passes through.” *Id.* The applicants also amended the claims but did not remove the limitations at issue. *Id.* at 208-13.

77. On September 21, 2023, the Examiner granted the applicants’ request for consideration under AFCP 2.0, finding all of the rejections in the previous Final Rejection were overcome. EX1002, 245. The Examiner then issued a Notice of Allowance. *Id.* at 254-63.

78. On November 3, 2023, the applicants requested to further amend the claims “to be more consistent with the specification” and “for clarity and/or to address minor issues.” EX1002, 269-80. The Examiner entered the amendment on November 14, 2023, without comment. *Id.* at 281-82.

79. On December 21, 2023, the applicants filed a Request for Continued Examination (RCE), submitting further amendments to the claims. EX1002, 300, 304-13. Then, the Examiner issued another Notice of Allowance on January 22, 2024. *Id.* at 330-40.

80. On March 22, 2024, the applicants again requested to further amend the claims. EX1002, 341-52. The applicants stated that the amendments did not add new matter and “should not necessitate additional search or examination.” *Id.* at 350-52. The Examiner entered the amendment on April 1, 2024, *id.* at 355-56,

and issued a Supplemental Notice of Allowance again on April 15, 2024, *id.* at 368-69.

81. On April 1, 2024, as discussed above, *supra* ¶70, the Board found all claims of the 060 and 160 Patents invalid. EX1072, 73-74; EX1073, 67. As noted above, *supra* ¶¶73-74, the Examiner had previously rejected the pending claims for being “not patentably distinct” over claims in the 060 and 160 Patents, but accepted a terminal disclaimer to overcome that rejection, EX1002, 261-62.

82. On April 22, 2024, the applicants filed another Request for Continued Examination (RCE), submitting further amendments to the claims. EX1002, 372-82, 385-86. The applicants submitted the Board’s Final Written Decision invalidating the 060 Patent, but not the Board’s Final Written Decision invalidating the 160 Patent. *Id.* at 392.

83. I have not seen any evidence that the applicants or the Examiner discussed the Board’s Final Written Decisions invalidating the 060 and 160 Patents or discussed the prior art references in those Final Written Decisions (including Kim (EX1014), Rajan (EX1015), Riho (EX1016), and Wyman (EX1017)). *See generally* EX1002, 372-874.

84. On June 11, 2024, the Examiner rejected all pending claims for failing to comply with the written description requirement under § 112(a). EX1002, 425-

29. The Examiner stated that the specification did not support “at least one TSV in at least one first array die of the second plurality of array dies.” *Id.* at 427-28.

85. On December 9, 2024, an interview with the Examiner was conducted upon the applicants’ request. EX1002, 738. According to the interview summary, “[t]he Examiner agreed that the proposed amendments to the claims overcome the 112(a) rejections,” *id.*, without providing specific reasons. The Examiner also indicated that an updated search would be conducted once the formal response was filed. *Id.*

86. On December 12, 2024, the applicants submitted a response to the previous Office Action on June 11, 2024, with amendments to the claims, adding various new elements. EX1002, 746-76. Among the elements newly introduced in the amendments were:

- “[first/second] **unidirectional** interconnects” conducting **first/second signals** associated with the memory read/write operations
- “**power supply interconnects**” including a first/second supply voltage interconnect
- “wherein the one or more C/A signals do **not** include **any chip select signal**”
- “wherein the control die does **not** include **emulation logic**”

EX1002, 768-76. With respect to the 112(a)-rejection regarding “at least one TSV,” the applicants argued that the rejection was moot as the relevant limitations were replaced. *Id.* at 769.

87. On January 17, 2025, the applicants submitted supplemental amendments “to correct clerical/typographical errors and/or to address potential formality, clarity and/or antecedent basis issues.” EX 1002, 778-96.

88. On February 12, 2025, another interview with the Examiner was conducted upon the applicants’ request. EX1002, 800. According to the interview summary, “Applicant clarified support for the negative limitation in claim 1 (the last three lines) [i.e., “the control die does not include emulation logic”] and will consider to replace ‘at least first C/A interconnects’ in claim 1 ... with ‘first C/A interconnects and second C/A interconnects’ to overcome the 112(b) issue.” *Id.* The summary did not explain how the negative limitation was supported. *Id.* According to the applicants’ summary of the interview, the Examiner tentatively agreed that the applicants could send an email with a proposed amendment addressing the issues discussed during the interview. *Id.* at 803.

89. On March 20, 2025, the Examiner issued a Notice of Allowance. EX1002, 826-863. The claims were allowed after the Examiner further amended the claims upon authorization given by the applicants during an interview conducted on March 6, 2025. *Id.* at 832-53. The final amendment by the

Examiner included the change discussed during the previous interview, which was replacing “at least first C/A interconnects” with “first C/A interconnects and second C/A interconnects.” The following limitations were also added in the final amendment by the Examiner:

- “wherein ***a first C/A interconnect*** of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and ***not in electrical communication with*** any C/A port on any of ***the second plurality of DRAM dies***”
- “wherein ***a second C/A interconnect*** of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and ***not in electrical communication with*** any C/A port on any of ***the first plurality of DRAM dies***”

EX1002, 833. Neither the applicants nor the Examiner provided any specific explanations for the amendments or any specific support in the written description for the amendments.

90. On May 20, 2025, the application issued as U.S. Patent No. 12,308,087 with 28 claims. EX1001; EX1002, 810, 874.

D. Constructions of terms used in the '087 Patent claims

91. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the

patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the '087 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted the claims of the '087 Patent, and the related 060 and 160 Patents, broadly for purposes of infringement, *see, e.g.*, EX1083, 11-17; EX1084, 11-17; EX1089; EX1044 at 63-68; EX1046 at 63-69, in my opinion the claims of the '087 Patent are invalid under § 112 and also obvious in light of the prior art regardless of the precise interpretation of their plain and ordinary meaning, as shown by my analysis below.

92. I also understand that in district court litigation involving the related 060 and 160 Patents, the district court provided the following claim constructions for terms in those patents:

“array die” (’060 Patent, all claims; ’160 Patent, all claims)	“array die that is different from a DRAM circuit”
“chip select signal” (’060 Patent, Claims 11–14, 16–19, 20–21, 23–28)	Plain and ordinary meaning.
“chip select conduit” (’060 Patent, Claims 6, 11–14, 16–19)	Plain and ordinary meaning.

EX1068, 35; *see also id.* at 31-34. I also understand that infringement of the term “array die” is at issue in the appeal from that district court litigation. *See* EX1077, 34-45; EX1078, 45-54; EX1079, 1-6. The term “array die” does not appear in the claims of the '087 Patent, and the other terms above were given their plain and

ordinary meaning, so my analysis below is consistent with the claim constructions above and is not affected by the appeal involving infringement of the term “array die.”

93. I also understand that in another district court litigation involving the related 060 and 160 Patents, the district court provided the following claim constructions for the terms in those patents:

“electrical communication” (’060 Patent, Claims 1, 11, 20, 29; ’160 Patent, Claim 1)	Plain and ordinary meaning
“driver size” (’160 Claim 1)	“driver physical size”
Claim 7 (’060 Patent)	Not indefinite as a mixed-class claim

EX1066, 43; *see also id.* at 8-16 (“Based on the foregoing, the Court agrees with Netlist that ‘electrical communication’ is different from ‘electrical connection.’ The Court also agrees with Micron that the existence of data ports, without more, does not satisfy the ‘electrical communication’ requirement in the claims.”). The ’087 Patent does not have a claim like claim 7 above, which required, “wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data

conduit and a second load on the second data conduit” Claim 4 of the ’087 Patent, however, does use the term “driver size,” which is one of the terms construed above. My analysis below is consistent with the claim constructions above, including that “driver size” refers to “driver physical size.” In any event, in my opinion, the prior art also renders claim 4 of the ’087 Patent obvious if “driver size” were understood to refer to driver strength, and thus the precise construction of “driver size” does not affect my obviousness opinions here, as was also true with respect to my opinions about “driver size” for the 160 Patent.

94. In the Final Written Decisions involving the related 060 and 160 Patents, I understand that the Board applied the following claim constructions, which were consistent with the expert opinions about obviousness that I offered and that the Board ultimately agreed with:

- “*array die*”: “In our analysis below, we apply the district court’s construction [above], and we find that the combination of Kim, Rajan, and Wyman teaches array dies that are not DRAMs and, therefore, are ‘different from a DRAM circuit.’ Therefore, we need not address any further qualifications of the district court’s construction or construe the term ‘DRAM circuit’ to determine what Patent Owner actually disclaimed, if anything.” EX1073, 10; *see also* EX1072, 10 (similar).

- “*chip select*”: “Claims 15 and 16 recite that there are fewer ‘first chip selection signals’ than ‘second chip selection signals,’ and, therefore, each of the ‘first chip selection signals’ appears to apply to multiple array dies, which makes sense in the context of the ‘rank multiplication’ of claims 15 and 16. *See* Inst. Dec. 12. We apply this interpretation of the claim language below in addressing the patentability of claims 15 and 16.” EX1073, 11; *see also* EX1072, 11 (similar).
- “*group of array dies*”: “Petitioner argues that the phrase ‘a first group of array dies’ . . . can be just one die. . . . Patent Owner disagrees We need not resolve this dispute because . . . we find persuasive Petitioner’s contentions that the combination of Kim, Rajan, and Wyman teaches a first group that has multiple array dies.” EX1073, 12; *see also* EX1072, 11 (similar).
- “*driver size*”: “Neither party argues for an express construction of this term, but Patent Owner notes that a district court in related litigation construed ‘driver size’ as ‘driver physical size.’ As explained below in § II.D.2.e, we find that the combination of Kim, Rajan, and Wyman teaches the subject matter under this construction, and we need not address the construction of this term further.” EX1073, 12; *see also* EX1072, 12 (similar).

My analysis below is consistent with the claim constructions above, with the understanding that the terms “array die” and “group of array dies” do not appear in the claims of the ’087 Patent. In the ’087 Patent, the term “chip select signal” is only used as a negative limitation (e.g., “wherein the one or more C/A signals do not include any chip select signal”), and thus the specific claim construction issue discussed by the Board above for the 160 Patent does not directly impact my analysis for the ’087 Patent, which would be the same under either of the constructions considered by the Board above. The same is true with respect to the term “driver size”: my analysis for claim 4 of the ’087 Patent is consistent with the construction that “driver size” refers to “driver physical size,” but in my opinion the prior art also renders claim 4 of the ’087 Patent obvious if “driver size” were understood to refer to driver strength (given that strength and physical size can be correlated), and thus the precise construction of “driver size” does not affect my obviousness opinions here, as was also true with respect to my opinions about “driver size” for the 160 Patent.

IV. GROUNDS 1 AND 2: (1) LACK OF WRITTEN DESCRIPTION AND (2) INDEFINITENESS UNDER 35 U.S.C. §112

95. The ’087 Patent (EX1001) claims priority to a non-provisional application filed on November 3, 2011 (EX1070) and to a provisional application No. 61/409,893 filed on November 3, 2010 (EX1005) (the “893 Provisional Application” or the “893 Provisional”). The disclosure in the 893 Provisional is

much shorter than the '087 Patent and does not include the following disclosures that were added to the non-provisional application filed on November 3, 2011:

- Figures 1-5 of the '087 Patent
- Columns 1:5-3:41, 3:65-17:63, and 20:18-22:42 of the '087 Patent
- Parts of columns 17:65-20:17 of the '087 Patent (with other parts of 17:65-20:17 being similar to ¶¶[0004]-[0012] in the 893 Provisional Application)

Compare EX1005, with EX1001.

96. As explained below, and consistent with my understanding of the legal standards discussed above for written description, *supra* ¶¶47-54, in my opinion neither the '087 Patent nor the 893 Provisional provides written description support for any of the claims of the '087 Patent. I will refer to this as “Ground 1.”

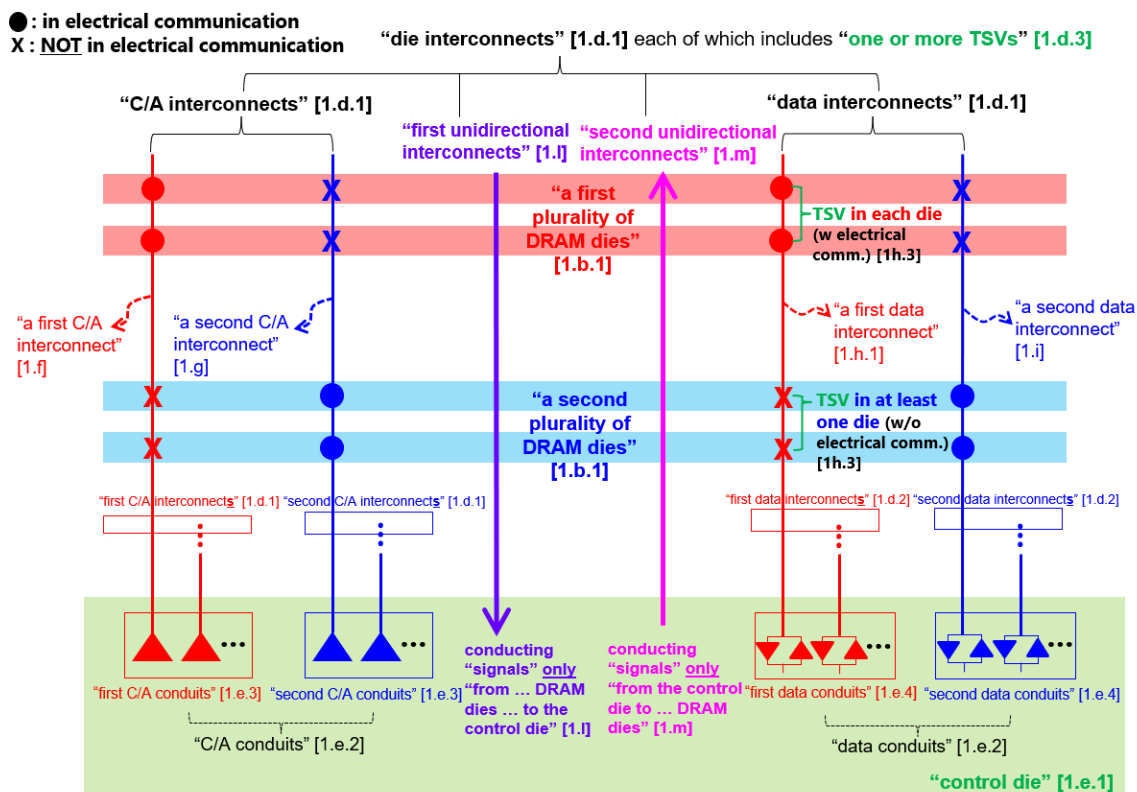
97. Furthermore, as explained below, and consistent with my understanding of the legal standards for indefiniteness, *supra* ¶¶55-57, in my opinion claims 24-28 of the '087 Patent are also indefinite given their contradictory and nonsensical requirements. I will refer to this as “Ground 2.”

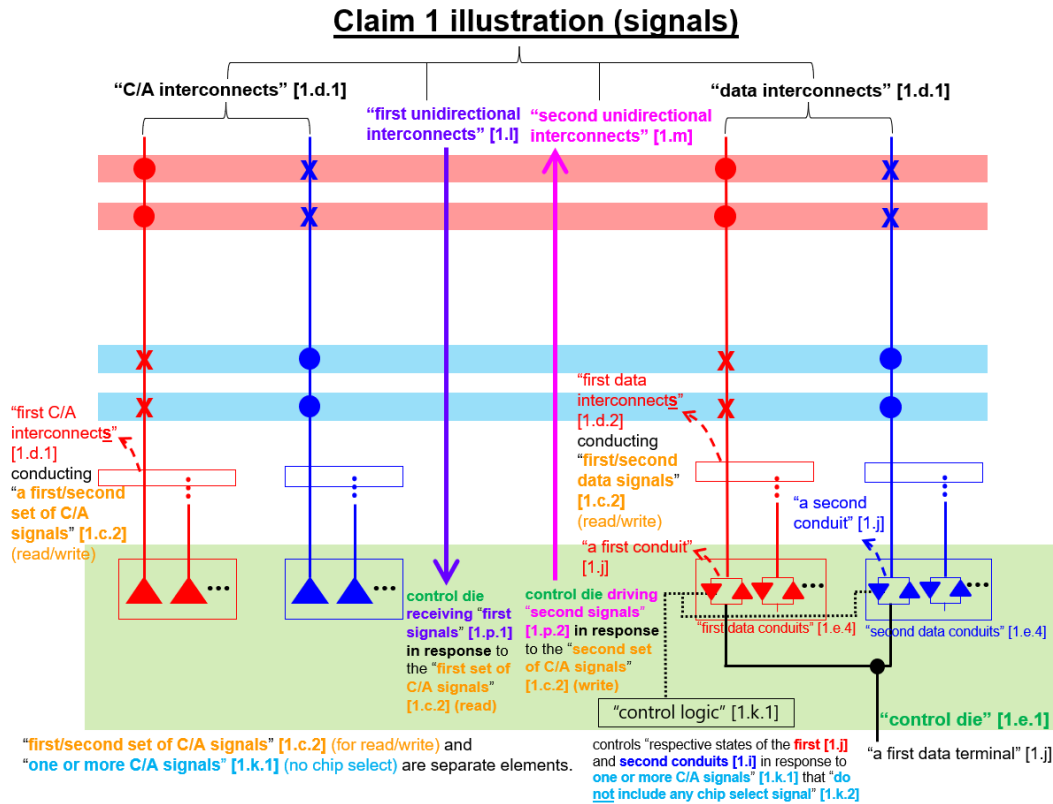
A. There is no written description for *all* of the claim requirements together (all claims)

98. The claim language of the '087 Patent is reprinted below, with labels, at the end of this declaration, starting on page 230. Each of the independent claims

of the '087 Patent (1, 9, 13, 20, 23, and 24) is extraordinarily long and complicated. To give a sense of that, I have prepared two illustrations of hypothetical memory packages directly below that show some of the many different specific features in claim 1. The first illustration below concerns the claimed structure, and the second illustration below concerns the claimed signals.

Claim 1 illustration (structure)





99. In my opinion, the '087 Patent nowhere describes the specific combination shown above, let alone all of the limitations required in any of the claims, each of which is similarly detailed and complex.

100. Instead, the '087 Patent discloses a "laundry list" of possibilities, which I understand is insufficient to satisfy the written description requirement. See *supra* ¶¶51-53. For example, the '087 Patent says over 250 times that certain features "may" or "can" be included in "some" embodiments (without ever identifying any particular embodiment), see, e.g., EX1001, 10:48 ("In *some* embodiments, the signal *can* be . . ."), and then the '087 Patent emphasizes that "such conditional language is *not generally intended to imply that features,*

elements and/or states are in any way required for one or more embodiments,”

EX1001, 23:18-:26. The '087 Patent never discloses the specific combination of limitations required in any of the claims.

101. In my opinion, as discussed above and further below, the '087 Patent does not reasonably convey to a POSITA that the named inventors of the '087 Patent actually invented what is claimed in the claims of the '087 Patent. It is notable that the '087 Patent emphasizes in its Title, Technical Field, and Summary of the invention that reducing driver “load” is part of the purported invention, EX1001, Title, 1:30-:35, 2:61-:62, yet none of the claims includes any limitations about reducing driver “load.” Instead, the claims of the '087 Patent appear to have been drafted in hindsight and not based on any combination of limitations actually described in the '087 Patent.

102. For comparison, reprinted below is Figure 2 of the '087 Patent, which does not disclose the claimed structure and signals illustrated above. For example, in Figure 2 below, 242 for command/address (C/A) signals is in electrical communication with **all** of the array dies 210 (as shown by the dark circles), contrary to the claimed structure illustrated above, where limitations [1.f]-[1.g] on the left **prohibit** electrical communication with some dies (as shown by the X's above), and where limitation [1.l] **also** requires a **unidirectional** interconnect going **down** (shown in purple above, i.e., from the DRAM die down to the controller die).

Those are just some differences between Figure 2 and the claimed structure and signals illustrated above. I discuss additional differences below.

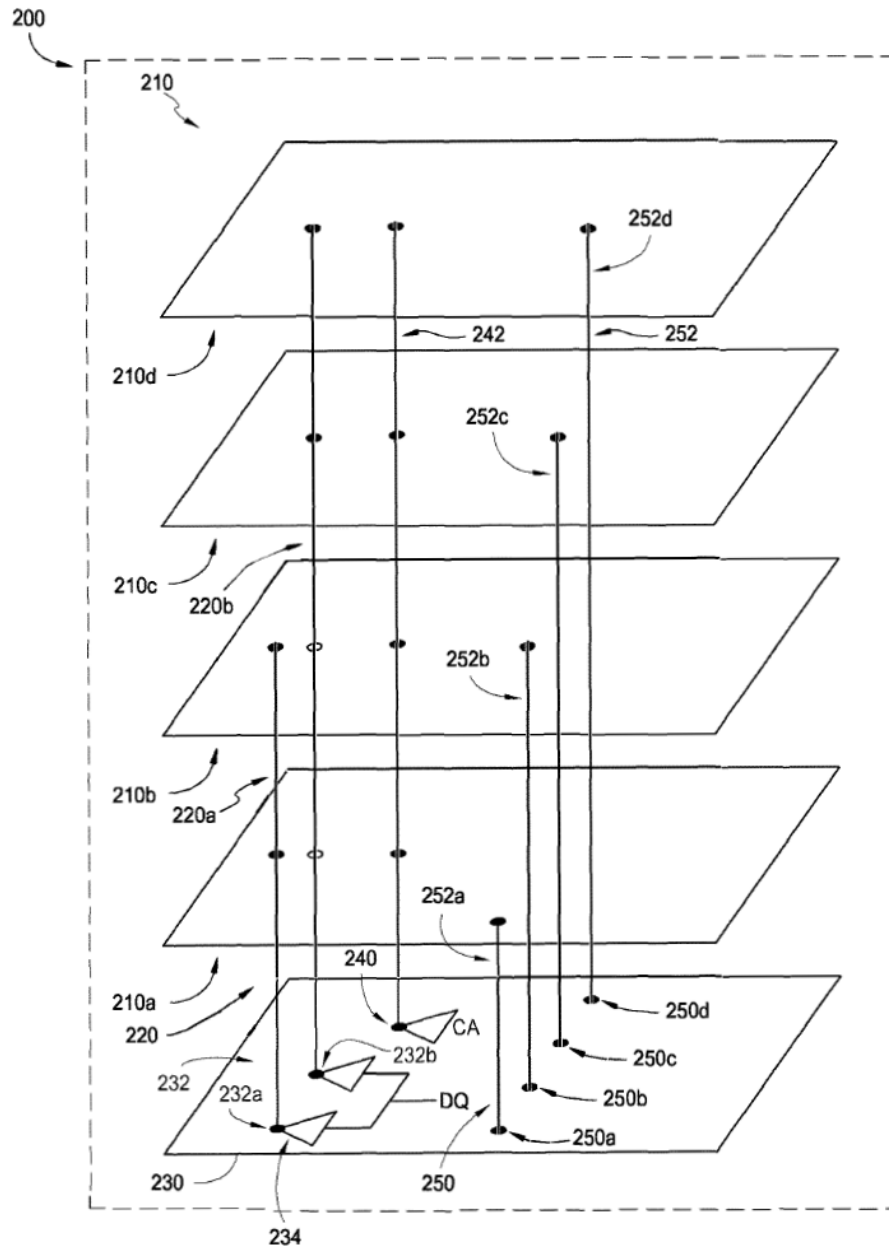


FIG. 2

EX1001, Fig.2.

103. To give a sense of the “laundry list” of possibilities disclosed by the ’087 Patent, I have prepared the chart below, which shows in the left column below that the ’087 Patent refers to various possibilities that could be combined in over 100 million different ways. In contrast, the claims of the ’087 Patent require an extraordinarily specific combination of features, as shown by just some of the claim requirements in the right column below. The chart below has seven rows (labeled A to G) for seven different features disclosed in the patent, and each row shows multiple options in the patent for that feature, resulting in over 100 million possible combinations. Some features in the claims are **not disclosed** at all, as shown by the red font and as explained in the sections further below.

<u>Possibilities in the ’087 Patent:</u>	<u>Possible embodiment(s) claimed</u>
A. Types of array dies – at least 6 possibilities: (1) DDR DRAM, (2) SDRAM, (3) flash, (4) SRAM, (5) GDDR SDRAM, or (6) other graphics memory. EX1001, 21:51-:58.	[1.b.1], [9.b.1], [13.b], [20.b], [23.b], [24.b]: “DRAM dies”
B. Type of interconnects – at least 5 possibilities: (1) wire, (2) conducting rod, (3) conducting trace, (4) vias, or (5) through-silicon vias (TSVs). EX1001, 8:13-:17.	[1.d.3], [9.b.3], [13.d], [20.d.3], [23.d.3], [24.e]: “through silicon vias (TSVs)” or “TSVs”
C. Subsets of dies – at least 2 possibilities: (1) two subsets (FIG. 2) or (2) six subsets (FIG. 3). EX1001, figs.2-3, 16:40-:55.	[1.b.1], [9.b.1], [13.g], [20.f.1], [23.f.1]: “a first [second] plurality of DRAM dies” or “a first [second] subset of the plurality of stacked DRAM dies”

<u>Possibilities in the '087 Patent:</u>	<u>Possible embodiment(s) claimed</u>
D. Interconnect(s) with selective electrical communication to subset of dies – at least $2^6=64$ possibilities: The specification lists 6 signals, each of which might (or might not) be conveyed by interconnects in selective electrical communication with a subset of dies, but a list of specific possible combinations is not disclosed: (1) data, (2) command, (3) address, (4) chip select, (5) supply voltage, or (6) ground voltage. EX1001, 10:32-:59.	[1.f], [1.g], [1.h.1], [1.i], [9.f.1], [9.g], [9.h], [9.i], [13.g], [13.h.1], [13.j], [13.k]: both “data interconnects” and “C/A interconnects” in selective electrical communication (combination not disclosed) [20.f.1], [20.f.2]: “data interconnects” in selective electrical communication [23.f.1], [23.f.2], [23.m.1], [23.m.2]: both “data interconnects” and “power supply interconnects” in selective electrical communication (combination not disclosed)

E. Bidirectional/unidirectional interconnects/conduits – at least $3^8=6,561$ possibilities: The specification discloses that interconnects/conduits for the following 6 signals might (or might not) be either (i) “bi-directional” or (ii) unidirectional going up (e.g., from the control die up to the array die(s)): (1) data, (2) command, (3) address, (4) chip select, (5) supply voltage, or (6) ground voltage. EX1001, 10:32-:59, 14:33-:51. In addition, the claims on the right claim at least “first signals” (a 7th category of signals) and “second signals” (an 8th category of signals), and further claim that at least the “first signals” are (iii) unidirectional going down (e.g., from the array die down to the control die), even though that is not disclosed in the specification. Thus, in total, there might be at least 8 different signals through an interconnect/conduit, each of which might (or might not be) either (i) bi-directional, (ii) unidirectional up, or (iii) unidirectional down.	[1.d.1]: command and/or address (C/A), unidirectional up; [1.c.2], [1.d.2]: data, bi-directional; [1.l], [1.n], [1.p.1]: “first signals” (not disclosed), unidirectional down (not disclosed); [1.m], [1.o], [1.p.2]: “second signals” (not disclosed), unidirectional up; [9.d.1], [9.e.1]: command and/or address (C/A), unidirectional up; [9.d.1], [9.e.1]: data, bi-directional; [9.d.2], [9.j.1]: “one or more signals” (not disclosed), unidirectional down on “first unidirectional interconnects” (not disclosed); [9.e.2], [9.j.2]: “one or more signals” (not disclosed), unidirectional up on “second unidirectional interconnects”; [13.g], [13.h.1]: data, bi-directional; [13.i]: command and/or address (C/A), unidirectional up; [13.o], [13.q]: “first signals” (not disclosed), unidirectional down (not disclosed); [13.p], [13.r]: “second signals” (not disclosed), unidirectional up; [20.c.2], [20.d.2]: data, bi-directional; [20.d.1]: command and/or address (C/A), unidirectional up; [20.k], [20.l.1]: “first signals” (not disclosed), unidirectional down (not disclosed); [20.k], [20.l.2]: “second signals” (not disclosed), unidirectional up; [23.d.2]: data, bi-directional;
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<u>Possibilities in the '087 Patent:</u>	<u>Possible embodiment(s) claimed</u>
	[23.d.1]: command and/or address (C/A), unidirectional up; [23.i-23.k], [23.l.1]: “first signals” (not disclosed), unidirectional down (not disclosed); [23.i-23.k], [23.l.2]: “second signals” (not disclosed), unidirectional up; [23.m.1], [23.m.2]: supply, unidirectional up [24.c], [24.i], [24.l]: data, bidirectional; [24.c], [24.h]: command and/or address (C/A), unidirectional up (conduit); [24.j], [24.m.2], [24.o.2]: “second”/“sixth” “signals” (not disclosed), unidirectional down (conduit) (not disclosed); [24.k], [24.n.2], [24.p.2]: “fourth”/“eighth” “signals” (not disclosed), unidirectional up (conduit)
F. Whether the “C/A signals” do <u>not</u> include any “chip select signals” – at least 2 possibilities: (1) The specification discloses that “a chip select signal” may be part of a control signal that controls a driver for a data conduit to drive a signal to the array die corresponding to the chip select signal. EX1001, 15:21-51. (2) Alternatively, the claims on the right claim controlling the data conduit with C/A signals that do <u>not</u> include any chip select signal.	[1.k.1-1.k.2], [20.h.1-20.h.2], [23.h.1-23.h.2]: “control respective states of the first data conduit and the second data conduit in response to one or more C/A signals . . . [that] do <u>not</u> include any chip select signal” (not disclosed)

<u>Possibilities in the '087 Patent:</u>	<u>Possible embodiment(s) claimed</u>
G. Whether the “control die” does <u>not</u> include emulation logic – at least 2 possibilities: (1) The specification discloses a “control die” with logic to perform rank multiplication. EX1001, 22:19-21. (2) Alternatively, the claims on the right claim a control die that does <u>not</u> include emulation logic.	[20.m], [23.n]: “the control die does <u>not</u> include emulation logic” (not disclosed)

104. As shown by the left column above, there are at least $6 \times 5 \times 2 \times 64 \times 6561 \times 2 \times 2 = 100,776,960$ possible combinations of features in the '087 Patent.

105. I understand that where the claims recite a specific combination that is not specifically disclosed in the specification and instead is drawn from millions of different possibilities, the claims lack written description. *See supra* ¶¶51-53. Thus, in my opinion, all of the claims of the '087 Patent lack written description for at least this reason. In addition, as discussed below, in my opinion the claims of the '087 Patent lack written description for other reasons as well.

B. Unidirectional interconnects/conduits for conducting signals down the stack (all claims)

106. Each of the independent claims, and thus all claims, require a unidirectional interconnect/conduit for conducting unspecified signals **down** the stack (e.g., that “conduct[s] signals **from** one or more DRAM dies [...] **to** the control die”) and not for conducting any signals up the stack (e.g., “**not** configured to conduct any signal **from** the control die **to** any of the stacked DRAM dies”). *See*

limitations [1.l], [9.d.2], [9.j.1], [13.o], [20.j], [20.k], [23.j], [23.k], [24.j]. In my opinion, the claimed unidirectional interconnect/conduit for conducting signals only **down** the stack is not disclosed in the 893 Provisional Application or the specification of the '087 Patent, as explained below.

1. Lack of written description in the 893 Provisional Application

107. The 893 Provisional Application (which is much shorter than the '087 Patent as explained above, *supra* ¶95) does not explain how stacked DRAM dies in a package are coupled to the control die or how signals from the control die are transferred to the DRAM dies. *See* EX1005. As such, it does not even mention “unidirectional” interconnects or conduits. *See id.*

108. For at least the foregoing reasons, the 893 Provisional Application does not provide written description support for these limitations.

2. Lack of written description in the '087 Patent

109. The specification of the '087 Patent discloses unidirectional interconnects/conduits for transmitting command/address (“C/A” or “CA”) and chip-select (CS) signals **up** from the control die to the array dies as shown by conduits 240 and 250, and die interconnects 242 and 252, in Figure 2. EX1001, 9:18-:36, Fig.2. But the specification has no disclosure of transmitting C/A or CS signals in the opposite direction, **down** the stack.

110. The specification also states that “the same die interconnects and the same corresponding data conduits may be used to transfer **data** both to and from the array dies 210. In such embodiments, the die interconnects may be **bi-directional**.” EX1001, 9:7-10 (emphasis added). “In alternative embodiments,” according to the specification, “separate die interconnects and corresponding data conduits may be used to transfer **data** to the array dies 210 and data from the array dies 210 to the control die 230” resulting in “double the number of die interconnects and data conduits.” *Id.* 9:10-17 (emphasis added). In my opinion, these disclosures do not provide written description support for the claim language for at least two reasons.

111. First, there is no disclosure of the negative limitation in the claims requiring that the die interconnect is “**not** configured to conduct **any** signal **from** the control die **to any** of the stacked DRAM dies” as required by claim [1.*l*] and as similarly required by the other independent claims. *See* [1.*l*], [9.d.2], [9.j.1], [13.o], [20.j], [20.k], [23.j], [23.k]. As explained above, my understanding is that silence is generally not disclosure sufficient to provide written description for a negative claim limitation. *See supra* ¶54. For example, nothing in the specification excludes a die interconnect from transferring data signals from a DRAM die to the control die during read operations and then transferring non-data signals from the control die to the DRAM die during other operations. Such a

shared use of a connection for different functions was known at the time (e.g., GDDR4 SGRAM using RDQS lines for transmitting read data strobes during read operations from the DRAM to the controller and using the same RDQS lines for transmitting Data Bus Inversion signals from the controller to the DRAM during write operations). See EX1035, 17-21. Moreover, given that bi-directional interconnects/conduits can transfer signals in the same direction as a unidirectional interconnect/conduit, two separate bi-directional interconnects/conduits can also transfer data signals as exactly described in the “alternative embodiments”—i.e., one bi-directional interconnect/conduit is “used to transfer data to the array dies 210” and the other bi-directional interconnect/conduit is “used to transfer data ... from the array dies 210 to the control die 230” resulting in “double the number of die interconnects and data conduits.” EX1001, 9:10-17. Considering that either bi-directional or unidirectional interconnects/conduits could be used as described for the “alternative embodiments,” the use of unidirectional interconnects/conduits in this disclosure is at most an obvious possibility, which I understand is insufficient to provide written description support. See *supra* ¶¶50-53.

112. Second, the disclosure is expressly limited to interconnects and conduits that “transfer **data**.” EX1001, 9:10-17 (emphasis added). But the signals conducted by the unidirectional interconnect/conduit going down are claimed separately from the “data signals” in [1.d.2] (and related claims)—which the

claims permit to be bidirectional. The claimed signal conducted down through the unidirectional interconnect/conduit is not a read data signal but rather is a signal “associated with the memory read operation” and a “set of C/A signals” in [1.p.1] (and related claims). The ’087 Patent does not disclose such a signal. For example, I understand that Netlist asserts, in district court, that the signals conducted by the claimed unidirectional interconnect/conduit going down can be read “data **strobes** RDQS_t/RDQS_c,” EX1083, 16, 42, 67-68; EX1084, 15, 41, 66-67; EX1087, 16; EX1088, 15, but that is nowhere disclosed in the ’087 Patent, which does not mention strobes or DQS. Also, as explained in the paragraph directly above, it was known that signal lines like RDQS did not need to be unidirectional. My understanding is that the written description requirement prohibits “picking and choosing” among disclosures in the patent to cobble together written description based on hindsight and obviousness. *See supra* ¶¶50-53. The ’087 Patent, in my opinion, does not disclose unidirectional interconnects conducting any signals associated with a read command **down** to the control die **in addition to** the separately claimed interconnects for “data signals” that may be bi-directional.

113. Similarly, with respect to Figure 3, the ’087 Patent allows for the possibility that a die interconnect “may not be bi-directional,” EX1001, 14:40-:51, but again does not disclose unidirectional interconnects conducting any signals

associated with a read command **down** to the control die **in addition to** the separately claimed interconnects for “data signals” that may be bi-directional. In particular, the specification discloses unidirectional interconnects for signals going **up** the stack: “the memory package 300 comprises one or more die interconnects 320 that are configured to enable a signal to be driven **to** the array dies 310 **without enabling a signal to be received from** the array dies 310 (e.g., the die interconnects 320 may not be bi-directional).” EX1001, 14:40-44. *Id* (emphasis added). Then the specification goes on to state, with respect to “certain embodiments” like the previous sentence (where there are interconnects that are unidirectional going up and thus are “not bi-directional”), that “the memory package 300 may include **additional die interconnects** (not shown) that are in electrical communication with the one or more **additional conduits** ... and that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.” EX1001, 14:45-51. During prosecution, Netlist, without any explanation, cited to this disclosure (which corresponds to ¶68 of the specification as filed) to support unidirectional interconnects/conduits going down the stack. EX1002, 771-72 (citing EX1002, 30-31 ¶68 (EX1001, 14:27-51)). But this disclosure fails to support the claim limitations, because it does not disclose unidirectional interconnects conducting any signals associated with a read command **down** to the control die **in addition to** the separately claimed

interconnects for “data signals” that may be bi-directional. The specific combination of requirements in the claims is just one of many different possible combinations in the “laundry list” disclosed by the ’087 Patent as explained above in ¶103, which I understand is insufficient to provide written description support. *See supra* ¶¶50-53.

114. For at least the foregoing reasons, in my opinion the ’087 Patent does not provide written description support for these limitations requiring unidirectional interconnects/conduits going down the stack.

C. Unidirectional first/second/fourth/sixth/eighth etc. signals (all claims)

115. Each of the independent claims, and thus all claims, require “signals” that are “associated with the memory read [write] operations” or a “set of C/A signals,” and are conducted via unidirectional interconnects or driven by unidirectional conduits. Those claimed signals are the “[first]/[second] signals” in Claims 1, 13, 20, and 23, “one or more signals” in Claim 9, and “[second]/[sixth] signals” and “[fourth]/[eighth] signals” in Claim 24 (collectively the “Unidirectional Signals”). *See* limitations [1.p.1], [1.p.2], [9.d.2], [9.e.2], [13.n], [20.l.1], [20.l.2], [23.l.1], [23.l.2], [24.m.2], [24.o.2], [24.n.2], [24.p.2].

116. These Unidirectional Signals are claimed separately from the “data signals” discussed above, *supra* ¶112, and separately from the “signals” having “at least 32 signals driven in parallel” (which includes data signals, EX1001, 15:12

(“32-bit memory package”)), all of which the claims permit to be bi-directional. See limitations [1.c.1], [9.b.2], [13.c], [20.c.1], [23.c.1], [24.c], [24.s.1]-[24.s.4]. These Unidirectional Signals are further claimed separately from any chip-select signal (e.g., “signals to select [one] DRAM die”). See limitations [6.a]-[6.b], [9.c], [13.l], [22.a]-[22.b], [25.b]-[25.e]. The claims also require that a first set of Unidirectional Signals associated with a memory read operation are sent **down** in response to a separately claimed first set of C/A signals, see limitations [1.p.1], [9.d.2], [13.n], [20.l.1], [23.l.1], [24.m.2], [24.o.2], and require that a second set of Unidirectional Signals are sent **up** in response to a separately claimed second set of C/A signals, see limitations [1.p.2], [9.e.2], [13.n], [20.l.2], [23.l.2], [24.n.2], [24.p.2]. In short, the Unidirectional Signals are claimed separately from the data, chip-select, and C/A signals.

117. In my opinion, there is no disclosure of these claim requirements in the 893 Provisional Application or the specification of the '087 Patent as explained below.

1. Lack of written description in the 893 Provisional Application

118. As discussed above, *supra* ¶107, the 893 Provisional Application does not disclose how the stacked DRAM dies are connected to one another or how signals are communicated between the DRAM dies and the control die, and the 893 Provisional Application does not mention “unidirectional” interconnects or

conduits. *See* EX 1005. Accordingly, it does not teach any of the Unidirectional Signals in the claims. *See id.*

119. For at least the foregoing reasons, the 893 Provisional Application does not provide written description support for these limitations.

2. Lack of written description in the '087 Patent

120. The specification of the '087 Patent does not provide written description support for these limitations because it only provides a “laundry list” of signals, which I understand is insufficient to satisfy the written description requirement. *See supra* ¶¶51-53. In particular, the specification states that the “signal” in the “die interconnect 320” in Figure 3 can “be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, *to name a few.*” EX1001, 10:34-36, 10:48-50 (emphasis added). This disclosure results in a large number of possible combinations, including at least the six signals listed (data, command, address, chip select, supply voltage, or ground voltage) plus the separately claimed (but not specifically disclosed) “first” and “second” signals, resulting in eight different possible signals, each of which could be conducted by either bi-directional, unidirectional going up, or unidirectional going down interconnects/conduits, resulting in $3^8 = 6,561$ possible combinations for just those eight signals — and there could be even more signals, resulting in even more possible combinations. There is no specific disclosure of the claimed

combination of signals, which as discussed above, *supra* ¶¶115-116, includes Unidirectional Signals claimed separately from the data, chip-select, and C/A signals, and a first set of Unidirectional Signals associated with a memory read operation that are sent **down** in response to a separately claimed first set of C/A signals, and a second set of Unidirectional Signals that are sent **up** in response to a separately claimed second set of C/A signals.

121. For at least the foregoing reasons, the '087 Patent does not provide written description support for any of the claimed Unidirectional Signals. In addition, the '087 Patent does not provide written description for the specific Unidirectional Signals discussed below, *infra* ¶¶122-125.

**3. “fifth,” “sixth,” and “eighth signals” (claims 24-28):
indefiniteness and lack of written description**

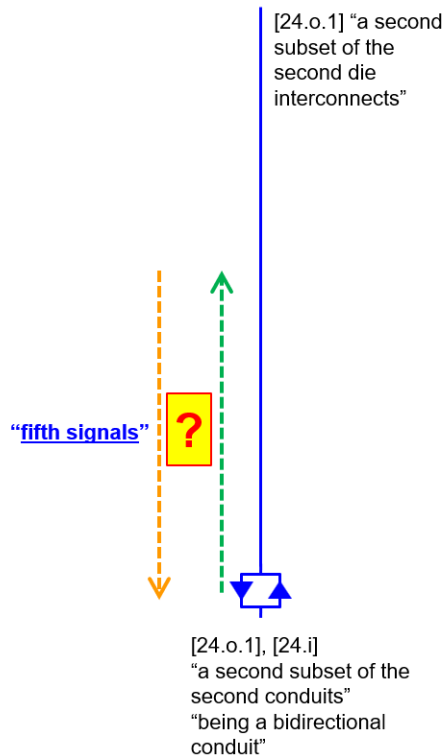
122. Claims 24-28 also require “*fifth*,” “*sixth*,” and “*eighth*” signals, which in my opinion do not have written description support in the '087 Patent, and which have contradictory and nonsensical requirements that in my opinion render the claims indefinite, *see supra* ¶¶56-57.

123. ***Fifth signals:*** I have prepared the illustration below to show the “fifth signals” in claim 24. According to claim 24, the “fifth signals” [24.o.1] are going **down** because they are received by a conduit via the respective interconnect “in response to” [24.o.1] “a third set of C/A signals for a memory **read** operation” [24.l], but they are also “associated with” [24.o.1] a “second set of C/A signals for

a memory **write** operation” [24.l], as shown below. But the specification of the '087 Patent does not disclose any signals like the claimed “fifth signals” that are associated with a **write** operation (i.e., going **up** to the array die), but sent **down** from the array die to the control die. Thus, in my opinion, there is no written description for the “fifth signals,” and the “fifth signals” are also indefinite given the contradictory requirements about whether those signals are going up or down.

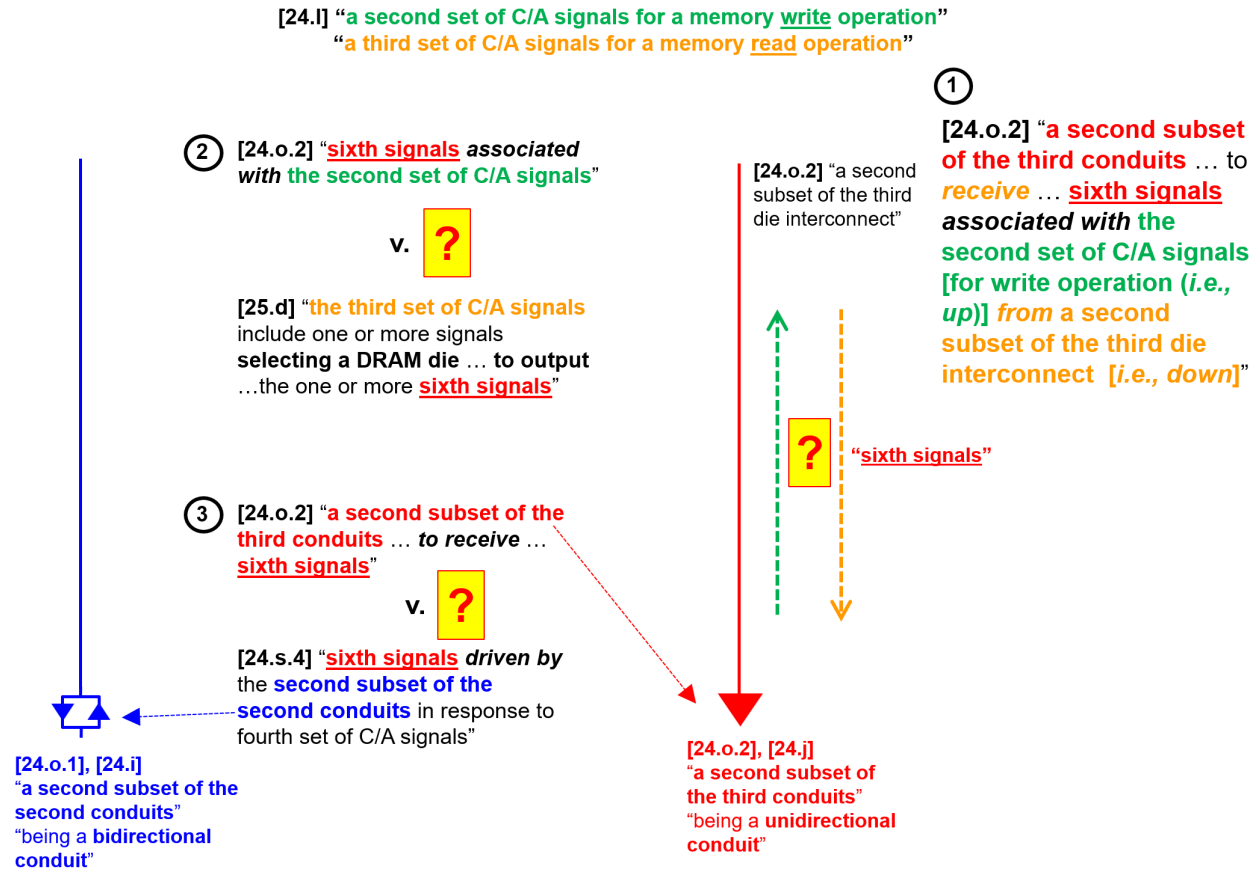
[24.l] “a second set of C/A signals for a memory **write** operation”
“a third set of C/A signals for a memory **read** operation”

[24.o.1] “in response to the third set of C/A signals [for read operation (i.e., down)], a second subset of the second conduits ... to **receive fifth signals** associated with the second set of C/A signals [for write operation (i.e., up)] via a second subset of the second die interconnects [i.e., down]”



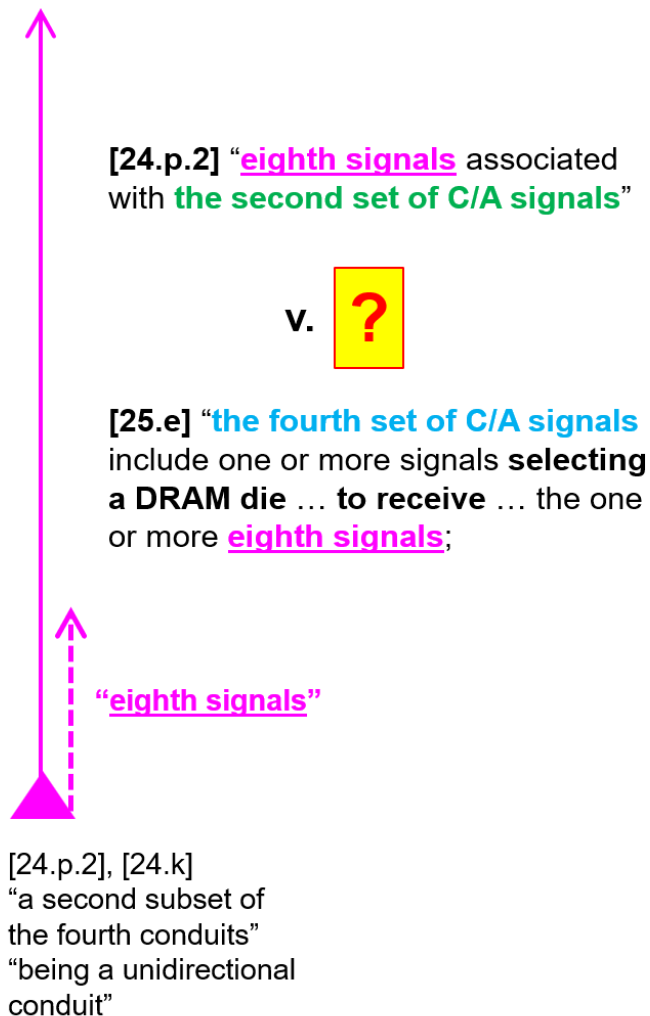
124. **Sixth signals:** I have prepared the illustration below to show the “sixth signals” in claim 24. As shown below (number 1), the “sixth signals” [24.o.2] are Unidirectional Signals received by the third conduits going **down**

[24.j], but they are “associated with” [24.o.2] a “second set of C/A signals for a memory **write** operation” going **up** [24.l]. As further shown below (number 2), the “sixth signals” are further associated with a “third set of C/A signals for a memory **read** operation” [24.l], [25.d]. Thus, the “sixth signals” are associated with both **read** and **write** operations. And as further shown below (number 3), the “sixth signals” are **received** by a “second subset of the **third** conduits” [24.o.2] “being a **unidirectional** conduit” [24.j], and **driven** by a “second subset of the **second** conduits” [24.s.4] “being a **bidirectional** conduit” [24.i]. Thus, the “sixth signals” are **received** by a **unidirectional** conduit but **driven** by a **bidirectional** conduit. In my opinion, there is no written description in the ’087 Patent for such “sixth signals,” and the “sixth signals” are also indefinite given all of the contradictory requirements about whether those signals are going up or down.



125. **Eighth signals:** I have prepared the illustration below to show the “eighth signals” in claims 24 and 25. The “eighth signals” are “associated with the *second* set of C/A signals” [24.p.2], [24.l], and also with “the *fourth* set of C/A signals” [24.p.2], [24.l], [25.e]. But the specification of the ’087 Patent does not disclose such a signal associated with two different operations. Thus, in my opinion, there is no written description in the ’087 Patent for such “eighth signals,” and the “eighth signals” are also indefinite given the contradictory requirements about which operation those signals are associated with.

[24.l] “a second set of C/A signals for a memory write operation”
“a fourth set of C/A signals for a memory write operation”



D. Multiple types of interconnects with selective electrical communication (claims 1, 9, 13, and 23)

126. Independent Claims 1, 9, 13, and 23 (and their dependents) require the combination of at least two different types of interconnects (i.e., “C/A,” “data,” and “supply voltage”), where each type of interconnect is in selective electrical communication with DRAM dies (or ports on those dies). See limitations [1.f], [1.g], [1.h.1], [1.i], [9.f.1], [9.g], [9.h], [9.i], [13.g], [13.h.1], [13.j], [13.k], [23.f.1],

[23.f.2], [23.m.1], [23.m.2]. But in my opinion this combination of limitations lacks written description support in the 893 Provisional Application and in the specification of the '087 Patent, as explained below.

1. Lack of written description in the 893 Provisional Application

127. The 893 Provisional Application (which is much shorter than the '087 Patent as explained above, *supra* ¶95) does not disclose any interconnects in electrical communication with only certain groups of DRAM dies. See EX1005. It does not even mention “interconnects.” See *id.* Accordingly, it does not disclose the combination of at least two different types of interconnects (i.e., “C/A,” “data,” and “supply voltage”), where each type of interconnect is in selective electrical communication with DRAM dies (or ports on those dies).

128. For at least the foregoing reasons, the 893 Provisional Application does not provide written description support for these limitations.

2. Lack of written description in the '087 Patent

129. The specification of the '087 Patent also does not disclose the combination of at least two different types of interconnects (i.e., “C/A,” “data,” and “supply voltage”), where each type of interconnect is in selective electrical communication with DRAM dies (or ports on those dies). Instead, the '087 Patent provides a “laundry list” of different interconnects for different signals that may (or may not) be in selective electrical communication: “[I]n *certtain* embodiments,

at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which *may* be in electrical communication with a different die interconnect 320,” EX1001, 10:21-:26 (emphasis added), and the “signal along a corresponding die interconnect 320” “*can* be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, *to name a few*,” EX1001, 10:35-:36, 10:48-:50 (emphasis added). Thus, the ’087 Patent does not disclose the claimed combination and instead would require “picking and choosing” among many possible combinations in the patent to cobble together written description based on hindsight and obviousness, which I understand is not sufficient to satisfy the written description requirement. *See supra* ¶¶50-53. For example, Figure 3 of the patent only shows selective electrical communication for *one* type of interconnect (i.e., for the signal supplied by the buffer 340). EX1001, FIG. 3. The claims, however, require a specific combination involving selective electrical communication for at least *two* different types of interconnects (i.e., “C/A,” “data,” and “supply voltage”), which is not disclosed by the ’087 Patent.

130. Selective electrical communication can provide the benefit of reducing electrical load, but it also has significant drawbacks, such as increasing chip size and complexity due to additional interconnects, conduits (and drivers),

and control signals for them. Thus, a POSITA would not automatically assume that just because the '087 Patent discloses selective electrical communication for one type of signal (as indicated in Figure 3), that the inventors actually invented a package with selective electrical communication for **two** different types of signals (as required by the claims of the '087 Patent). The specification provides no such disclosure, and in fact Figure 2 discloses the opposite (i.e., DQ data signals on die interconnects 220a and 220b that **are** in selective electrical communication, and CA signals on die interconnect 242 that are **not** in selective electrical communication). EX1001, Fig.2.

131. Furthermore, there is no disclosure of the unusual requirement in Claims 1 and 9 that there are “first” and “second” “C/A interconnects” in selective electrical communication with ports of the DRAM dies, but **both** the “first set of C/A signals” **and** the “second set of C/A signals” are conducted on the “**first** C/A interconnects” (while other signals may be on the “**second** C/A interconnects”). See limitations [1.d.1], [1.f]-[1.g], [9.d.1], [9.e.1], [9.h]-[9.i]. Those claim limitations create additional complexity neither suggested nor disclosed by the '087 Patent, such as different groups of DRAM dies receiving (potentially at the same time) different C/A signals, contrary to the teaching in Figure 2 that the same C/A signals are transmitted to all DRAM dies at the same time on die interconnect 242. EX1001, Fig.2. Similarly, Figure 3 does not teach different groups of

DRAM dies receiving (potentially at the same time) different C/A signals, and instead at most teaches the same signal (coming from pre-driver 340) being driven on different interconnects at the same time. EX1001, Fig.3.

132. For at least the foregoing reasons, the specification of the '087 Patent does not provide written description support for these limitations requiring multiple types of interconnects with selective electrical communication.

E. “C/A signals” that “do not include any chip select signal” (claims 1, 18, 20, and 23)

133. Independent Claims 1, 20, and 23 (and their dependents) require that a “first data conduit” is coupled “between the first data interconnect and ***a first data terminal,***” that a “second data conduit” is coupled “between the second data interconnect and ***the first data terminal,***” and that “respective states” of the first and second data conduits are controlled “in response to one or more C/A signals,” which “do **not** include any chip select signal.” See limitations [1.j]-[1.k.2], [20.g]-[20.h.2], [23.g]-[23.h.2]. Dependent Claim 18 has similar requirements. See limitations [18.a.1]-[18.a.2]. Accordingly, the claims require two data conduits that create what is sometimes referred to as a fork-in-the-road (*i.e.*, one end of each of the two data conduits is coupled with respective interconnects, while the other ends share the same interface terminal, as shown in Figure 4), which is controlled by “one or more C/A signals” that excludes “any chip select signal.” In my opinion, this negative limitation lacks written description support in the 893

Provisional Application and in the specification of the '087 Patent, as explained below.

1. Lack of written description in the 893 Provisional Application

134. The 893 Provisional Application (which is much shorter than the '087 Patent as explained above, *supra* ¶95) does not disclose “data conduits” or any logic controlling “respective states of” the data conduits, let alone the negative limitation that excludes “any chip select signal.” See EX1005.

135. For at least the foregoing reasons, the 893 Provisional Application does not provide written description support for this negative limitation.

2. Lack of written description in the '087 Patent

136. The specification of the '087 Patent also does not provide written description for the negative limitation where the states of the first and second data conduits are controlled “in response to one or more C/A signals” that “do not include any chip select signal.”

137. The '087 Patent provides affirmative examples of using the chip select signals, not prohibitions against including any chip select signal. EX1001, 15:31-:40, 16:5-:12. For example, Figure 4 of the '087 Patent, below, discloses data conduits with a fork-in-the-road configuration, consistent with the claim language discussed above requiring a fork-in-the-road, *supra* ¶133. Specifically,

Figure 4 discloses two data conduits (406a and 406b) and corresponding drivers (408a/404a and 408b/404b) that share the same terminal (402).

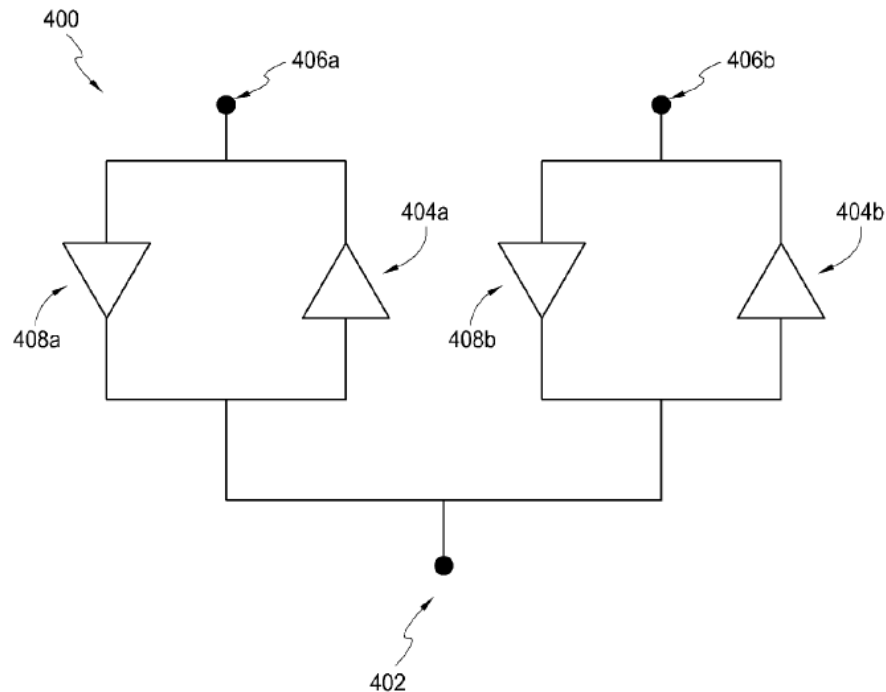


FIG. 4

EX1001, 15:21-30, FIG. 4. The specification of the '087 Patent explains that “operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal” that “may correspond to one or more of a command/address signal.” EX1001, 15:32-37. But the specification does not teach that this “command/address signal” excludes a chip select signal, as required by the claims. *Id.* To the contrary, the specification goes on to teach using the chip select signal: “In some implementations, the drivers 404a and 404b may drive a signal to the array die *corresponding to the chip select signal*, and not to array

dies that do not correspond to a chip select signal.” EX1001, 15:37-40 (emphasis added). During prosecution, Netlist pointed to this portion of the specification as providing support for the negative limitation, EX 1002, 771 (citing EX1002, 32 ¶73, which corresponds to EX1001, 15:31-51), but as discussed directly above, this part of the specification does not actually teach excluding a chip select signal from a particular set of signals, and it is my understanding that silence generally is not disclosure of a negative claim limitation, *supra* ¶54. Furthermore, in Figure 4, which has the fork-in-the-road configuration, a POSITA would understand that a chip-select signal is needed during read operations (i.e., going down) because the read drivers (408a and 408b) share the same output terminal (402), meaning only one read driver and one corresponding chip can be selected to drive read data at a time to the output terminal (402). Thus, the '087 Patent does not teach controlling Figure 4 in the read direction **without** a chip-select signal.

138. During prosecution, Netlist also cited to a separate embodiment where an **external** register device 812 provides “data path control signals” to “operate the data path control circuits” on the control die. EX1002, 771 (citing EX1002, 40 ¶100, 41-42 ¶105, which corresponds to EX1001, 21:4-14, 21:63-22:5). But my understanding is that “picking and choosing” among different embodiments does not satisfy the written description requirement. *See supra* ¶53. Furthermore, according to the specification, the “data path control circuits” of this embodiment

manage time slots to avoid data collisions among “**multiple**” memory packages 820” sharing the same “data bus 818.” EX1001, 21:31-:40, Fig.8. Thus, the “data path control signals,” which operates the “data path control circuits,” do not disclose controlling data drivers/conduits on the control die **within a single** DRAM package as claimed. And in any event, the disclosure for this embodiment again does not **exclude** using chip-select signals as part of the “data path control signals.” See EX1001, 21:4-14, 21:63-22:5. It is my understanding that silence generally is not disclosure of a negative claim limitation, *supra* ¶54, and here there is nothing to suggest that a chip-select signal would necessarily be excluded. To the contrary, a POSITA would be familiar with chip-select signals as a command signal, *see, e.g.*, EX1019, 13 (“CS# [Chip Select] is considered part of the command code”), so a POSITA would have no reason to assume that chip-select signals would necessarily be excluded from the disclosed “command/address signals,” EX1001, 22:1.

139. For at least the foregoing reasons, the '087 Patent does not provide written description support for the negative limitation that “one or more C/A signals do not include any chip select signal.”

F. “the control die does not include emulation logic” (claims 6, 20, and 23)

140. Independent Claims 20 and 23 (and their dependents) and dependent Claim 6 require that “the control die does not include emulation logic.” See

limitations [20.m], [23.n], [6.c]. The term “emulation logic” is not in the specification. As discussed below, Netlist suggests that the “emulation logic” referenced in the claims includes logic for “rank multiplication,” meaning the claims require the control die to exclude rank multiplication logic. In my opinion, this negative limitation lacks written description support in the 893 Provisional Application and in the specification of the ’087 Patent, as explained below.

1. Lack of written description in the 893 Provisional Application

141. The 893 Provisional does not use the term “emulation logic” at all. But as discussed below in ¶144, Netlist has suggested that “emulation logic” can be logic for “rank multiplication.” While the 893 Provisional Application teaches that a “3DS register” outside the DRAM package may contain a “rank multiplication” circuit, it does not teach the rank multiplication circuit is excluded from the control die. See EX1005, ¶5, Fig.2. To the contrary, it teaches that the control die may include logic for rank multiplication. EX1005, ¶6 (“The 3DS DRAM package comprises 2, 4 or 8 DDR DRAM dies and a controller die. **The controller die includes** data buffers, a data path timing controller, a secondary command/address buffer, **a programmable secondary 1-to-2 rank decoder**, and a data path signal (e.g., ODT, ODT, RTT) controller.”) (emphasis added); *id.* ¶10 (“[T]he controller die . . . provides selective isolation, a secondary address buffer, and **a second rank multiplication decoder . . .**”) (emphasis added).

142. For at least the foregoing reasons, the 893 Provisional Application does not provide written description support for this negative limitation.

2. Lack of written description in the '087 Patent

143. The specification of the '087 Patent also does not provide written description for the negative limitation that “the control die does not include emulation logic.”

144. The phrase “emulation logic” does not appear in the specification of the '087 Patent at all. Netlist has suggested that “emulation logic” can be logic for “rank multiplication.” In particular, during prosecution, to support this negative limitation, Netlist cited to two different disclosures for two different embodiments. EX1002, 772 (citing EX1002, 23-24 ¶46, which corresponds to EX1001, 9:52-64; and EX1002, 32 ¶108, which corresponds to EX1001, 22:18-42). Neither disclosure excludes rank multiplication from the control die.

145. The first disclosure does not expressly refer to emulation or rank multiplication and does not exclude emulation or rank multiplication from the control die: “In some embodiments, the control die 230 may include additional drivers that are configured to drive the chip select signals along the die interconnects 252. Alternatively, the chip select signals may be driven by drivers that are external to the control die 230. For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine

the chip select signals and drive the chip select signals to the array dies 210. As a second example, the chip select signals may be provided by an MCH. In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals” EX1001, 9:52-64.

146. The second disclosure expressly refers to rank multiplication: “In some embodiments, the register device 812 may be configured to perform rank multiplication. ***In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication.***” EX1001, 22:18-:21 (emphasis added). But that disclosure concerns the “JEDEC 3DS” embodiment in Figure 8, EX1001, 19:46-:50, Fig.8, and not the Figure 2 or 3 embodiment discussed in connection with several of the limitations above. My understanding is that the written description requirement cannot be satisfied by “picking and choosing” among disparate disclosures in the patent to cobble together written description based on hindsight and obviousness. *See supra* ¶¶51-53. Furthermore, this disclosure teaches the opposite of what the negative limitation requires, because this disclosure teaches that the control die ***may*** include rank multiplication logic (i.e., a type of emulation logic), even if the register also includes rank multiplication logic. EX1001, 22:18-:21 (“the control dies 822 may be configured to perform rank multiplication”).

147. It is my understanding that silence generally is not disclosure of a negative claim limitation, *supra* ¶54, and here there is nothing in either disclosure to suggest that emulation logic (e.g., for rank multiplication) must be excluded from the control die.

148. For at least the foregoing reasons, the '087 Patent does not provide written description support for the negative limitation that “the control die does not include emulation logic.”

G. The 893 Provisional Application filed November 3, 2010, also fails to disclose additional limitations

149. In my opinion, the 893 Provisional Application filed November 3, 2010, also fails to provide written description for additional limitations beyond the limitations discussed above.

150. The 893 Provisional Application is much shorter than the '087 Patent and only includes three figures, as explained above. *See supra* ¶95. The first two figures refer to prior art, while the third figure “schematically illustrates a memory module architecture in accordance with certain embodiments described herein.” EX1005, ¶3. Reprinted below is Figure 3 of the '087 Patent.

3DS-DIMM+ (Distributed Topology based HCDIMM)

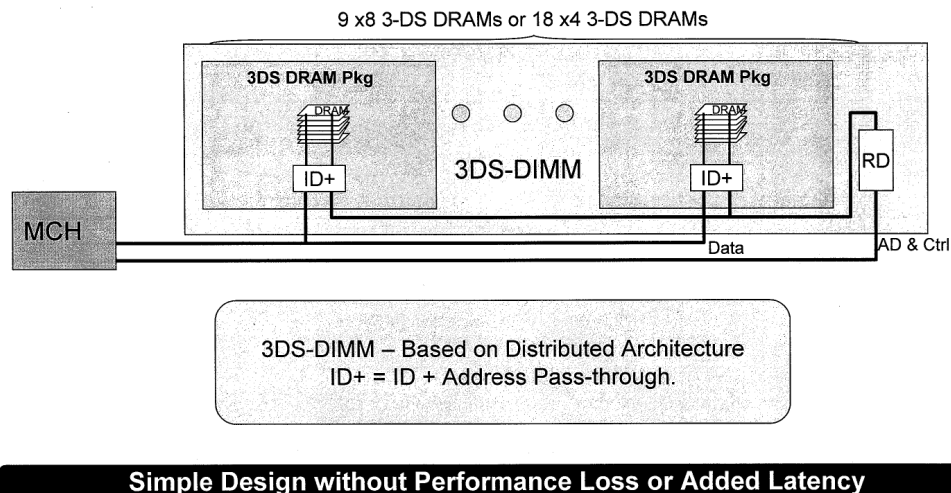


Figure 3

151. Consistent with the figure shown above, the 893 Provisional just discloses a **single** group of “DRAM chips or dies” in each package, EX1005, ¶¶[0006], [0010] & Figs.2-3, with no disclosure of subsets of dies—or electrical communication with only a subset of dies—in a given package. For example, Figure 3 above shows only one “Data” line going to **all** of the DRAM dies in a package, and only one “AD[DRESS] & Ctrl” line going to **all** of the DRAM dies in a package. That is in stark contrast to Figures 2 and 3 of the '087 Patent where there are multiple die interconnects, each in electrical communication with only a subset of all the dies in the stack. *See supra* ¶¶63-66. Thus, in my opinion, the 893 Provisional Application does not provide written description for any of the claims of the '087 Patent, all of which require a “first” and “second” “plurality of

DRAM dies” with “interconnects” in “electrical communication” with the “first” plurality but not the “second” plurality, and vice versa. See limitations [1.f]-[1.i], [9.f.1]-[9.i], [13.g]-[13.k], [20.f.1]-[20.f.2], [23.f.1]-[23.f.2], and [25.a.1]-[25.a.2].

V. OVERVIEW OF THE PRIOR ART

152. Below is an overview of the primary prior-art references that I considered (Keeth, Shaeffer, and Riho2) when analyzing the validity of the claims of the '087 Patent in light of Ground 3 (Keeth + Shaeffer) and Ground 4 (Ground 3 + Riho2).

A. U.S. Patent No. 9,123,552 to Keeth et al. (EX1047) (“Keeth”)

153. U.S. Patent Application No. 12/750,448 by Keeth et al. (“Keeth”), titled “Apparatuses Enabling Concurrent Communication Between an Interface Die and a Plurality of Dice Stacks, Interleaved Conductive Paths in Stacked Devices, and Methods for Forming and Operating the Same,” was filed on March 30, 2010, and was published as U.S. Patent Pub. No. 2011/0246746 on October 6, 2011. EX1047 (Keeth) at 1. Keeth issued as U.S. Patent No. 9,123,552 on September 1, 2015. *Id.*

154. Because Keeth was filed before the earliest claimed priority date of the '087 Patent (November 3, 2010), I understand that Keeth is prior art to the '087 Patent under at least 35 U.S.C. § 102(e) (pre-AIA). Alternatively, because the claims of the '087 Patent are not supported by the provisional application filed

November 3, 2010, *see supra* ¶¶95-151, I understand that Keeth is prior art under at least 35 U.S.C. § 102(a) (pre-AIA) because it was published on October 6, 2011, before the non-provisional application resulting in the '087 Patent was filed on November 3, 2011. Alternatively, because the claims of the '087 Patent lack written description and are not entitled to claim priority before the application for the '087 Patent was filed on March 14, 2022, as explained above, *see supra* ¶¶95-148, I understand that Keeth, which issued on September 1, 2015, is also prior art to the '087 Patent under 35 U.S.C. § 102(a)(2) (post-AIA).

155. Although Keeth was cited during prosecution of the '087 Patent, *see* EX1002, 71, Keeth was not discussed during prosecution (either alone or in the combinations with other references that I identify below as Grounds 3 and 4).

156. Keeth is directed to forming dice stacks (e.g., 520-523, yellow and orange below) on an interface die (e.g., 510, green) using “interleaving conductive paths” (e.g., 505-508) to connect with circuitry (e.g., IO Circuits 530-533 and 540-543) on alternating dice (e.g., 520 and 522, yellow; or 521 and 523, orange). EX1047 (Keeth) at Abstract, 5:24-6:29, Fig. 5 (below, annotated).

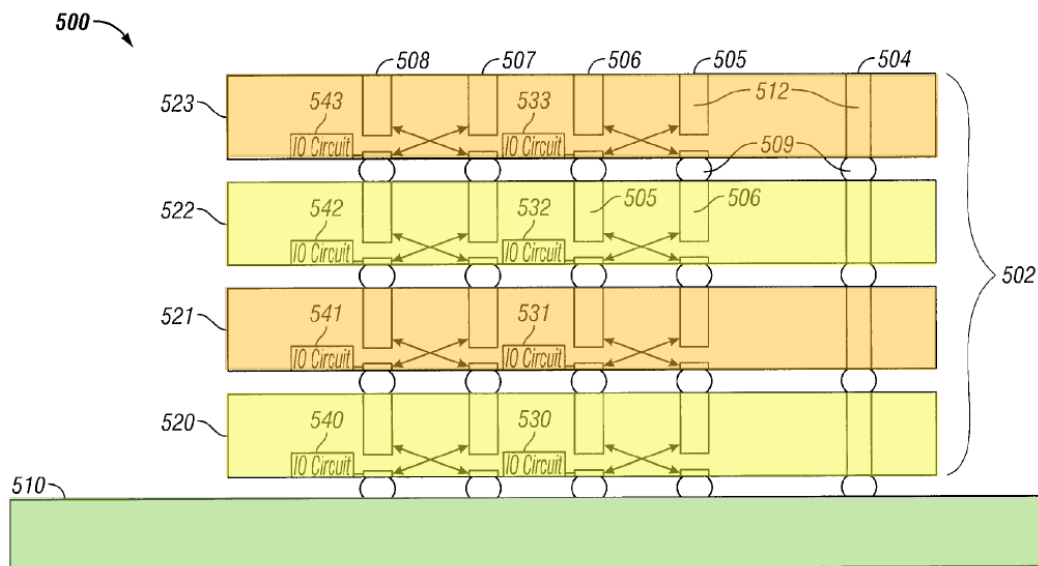


FIG. 5

The term “dice” used by Keeth is another way of saying “dies” (i.e., the plural of “die”). The ’087 Patent typically uses the term “dies” while Keeth typically uses the term “dice.” I use the two terms interchangeably in this declaration.

157. Such “interleaving conductive paths” can communicate data, address, and control information between the memory dice and the interface die. *Id.*, 3:5-8. According to Keeth, each memory die in the stack can be divided into memory partitions that are arranged into “vaults” and connected to corresponding “vault control” circuitry (212) in the interface die. *Id.* at 3:44-54, Fig. 2 (below, annotated).

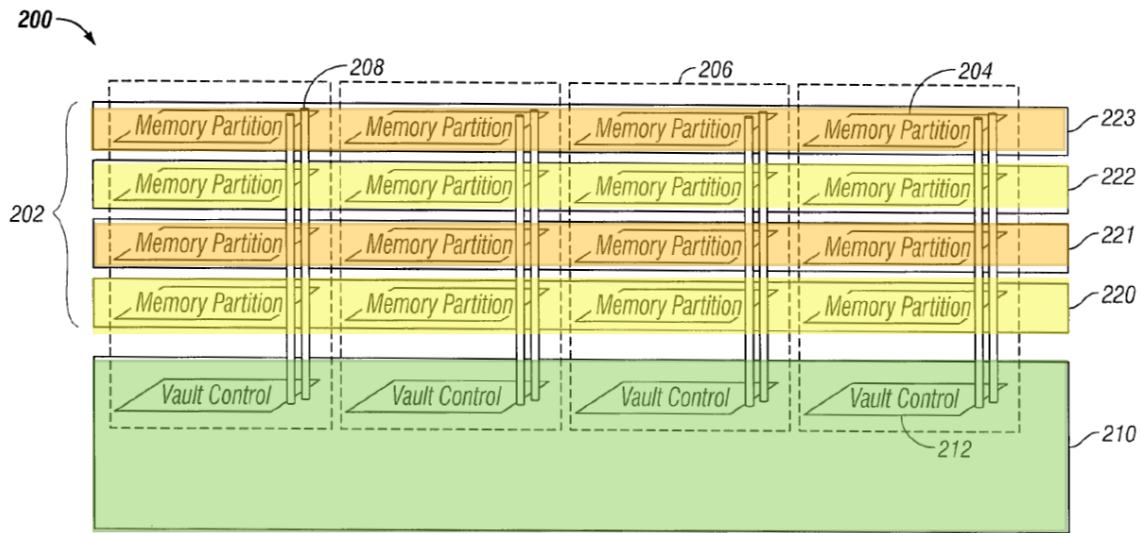


FIG. 2

B. U.S. Patent No. 9,665,507 to Shaeffer et al. (EX1048) (“Shaeffer”)

158. U.S. Patent Application No. 13/105,798 by Shaeffer et al. (“Shaeffer”), titled “Protocol Including a Command-Specified Timing Reference Signal,” was filed on May 11, 2011, and was published as U.S. Patent Pub. No. 2012/0023363 on January 26, 2012. EX1048 (Shaeffer) at 1. Shaeffer claims priority to Provisional Application No. 61/366,806 (“the 806 Provisional”), filed on July 22, 2010. EX1049. Shaeffer issued as U.S. Patent No. 9,665,507 on May 30, 2017. EX1048.

159. I have been informed that in order for a prior art reference to claim the benefit of the effective filing date of a provisional application, the provisional application must provide written description support for the specific portions of the non-provisional patent specification identified and relied on as prior art. The

provisional patent must also provide written description support for at least one claim in the non-provisional prior art patent. In this case, it is my opinion Shaeffer meets these requirements and is entitled to claim the benefit of the 806 Provisional as its effective filing date. There is no new material in Shaeffer compared to the 806 Provisional: every figure in Shaeffer appears in the 806 Provisional (*compare* EX1049, pp.39-45, *with* EX1048, pp.3-9), and the specification text in Shaeffer is substantially identical to the text of the 806 Provisional (*compare* EX1049, pp.5-27, *with* EX1048, 1:12-12:57). I understand that before issuing the Shaeffer patent, the Patent Office would have determined that the specification provided written description support for the issued claims, and given that the 806 Provisional is substantively identical to the specification of the Shaeffer patent, it is my opinion that the 806 Provisional would provide written description support for all of the issued claims as well. In addition, as shown below, I have identified written description support in the 806 Provisional for at least Claim 1 of Shaeffer. *See also* EX1050, pp.299-301 (appeal brief explaining Claim 1 of Shaeffer with reference to numbered paragraphs in non-provisional specification).

Claim 1 (EX1048, 12:60-13:12)	806 Provisional Support (EX1049)
1. A method of operation in a memory controller, the method comprising:	[0012] (pp.7-8); Fig. 3 (p.42)

Claim 1 (EX1048, 12:60-13:12)	806 Provisional Support (EX1049)
transmitting a read command which specifies that a memory device output data;	[0028]-[0031] (pp.14-15); Fig. 3 (p.42)
with the read command, transmitting information which specifies a duration of a preamble that is to be output prior to commencing outputting of the data;	[0030]-[0033] (pp.14-16); Fig. 3 (p.42)
receiving the preamble; and	[0030] (pp.14-15); Fig. 3 (p.42)
sampling the data output from the memory device in dependence on the preamble output from the memory device;	[0012]-[0013] (pp.7-8); Fig. 3 (p.42)
wherein the memory controller is to control multiple ranks of memory, and	[0010]-[0011] (pp.6-7); Fig. 3 (p.42)

Claim 1 (EX1048, 12:60-13:12)	806 Provisional Support (EX1049)
the method further comprises transmitting the information in a manner to specify that the memory device is to utilize the duration of the preamble that is to be output prior to commencing outputting the data in connection with a rank switch in consecutive memory operations	[0028]-[0030] (pp.14-15); Fig. 3 (p.42)

160. Because Shaeffer has an effective filing date from its provisional application filed July 22, 2010, that is before the earliest claimed priority date of the '087 Patent (November 3, 2010), I understand that Shaeffer is prior art to the '087 patent under at least 35 U.S.C. § 102(e) (pre-AIA). Alternatively, because the claims of the '087 Patent are not supported by the provisional application filed November 3, 2010, *see supra* ¶¶95-151, I understand that Shaeffer is prior art under at least 35 U.S.C. § 102(e) (pre-AIA) because it was filed on May 11, 2011, before the non-provisional application resulting in the '087 Patent was filed on November 3, 2011. Alternatively, because the claims of the '087 Patent lack written description and are not entitled to claim priority before the application for the '087 Patent was filed on March 14, 2022, as explained above, *see supra* ¶¶95-

148, I understand that Shaeffer, which issued on May 30, 2017, is also prior art to the '087 Patent under 35 U.S.C. § 102(a)(2) (post-AIA).

161. Shaeffer was not cited or discussed during prosecution of the '087 Patent. See EX1002.

162. Shaeffer discloses a “protocol for high speed signaling between a memory device and a memory controller.” EX1048 (Shaeffer) at 1:17-19. Shaeffer discloses specific signals and corresponding signal lines that are used to communicate through a chip-to-chip interface (118) to access the memory device for memory operations. *Id.* at 3:25-61, Fig. 1A (reproduced below). For example, Shaeffer teaches that, in response to a read command, the memory device can output a timing reference signal (TRS) on a signal line for error detection and correction information (EDC). *Id.*, at Abstract, 2:64-3:4, Fig. 4B.

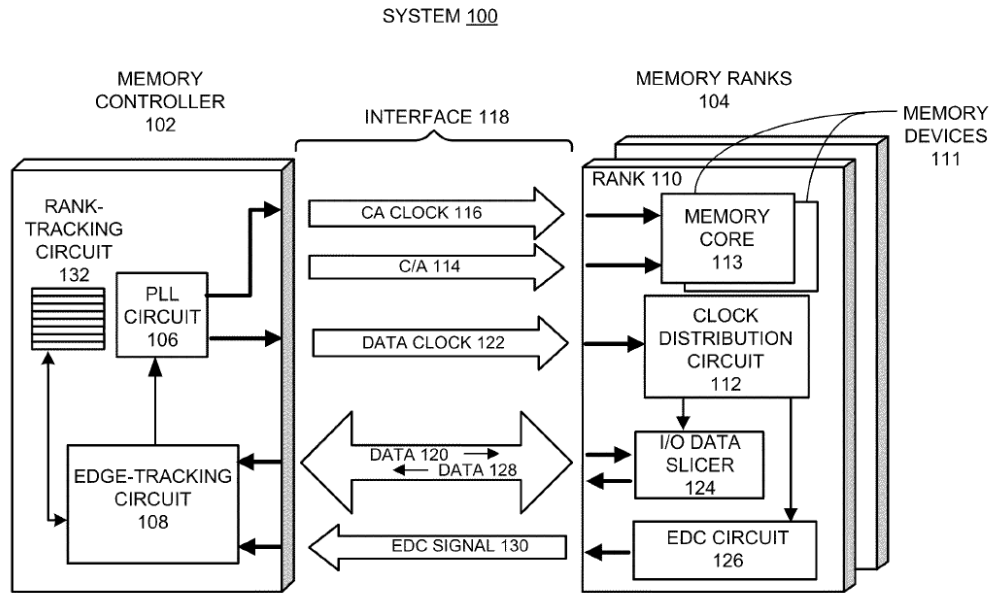


FIG. 1A

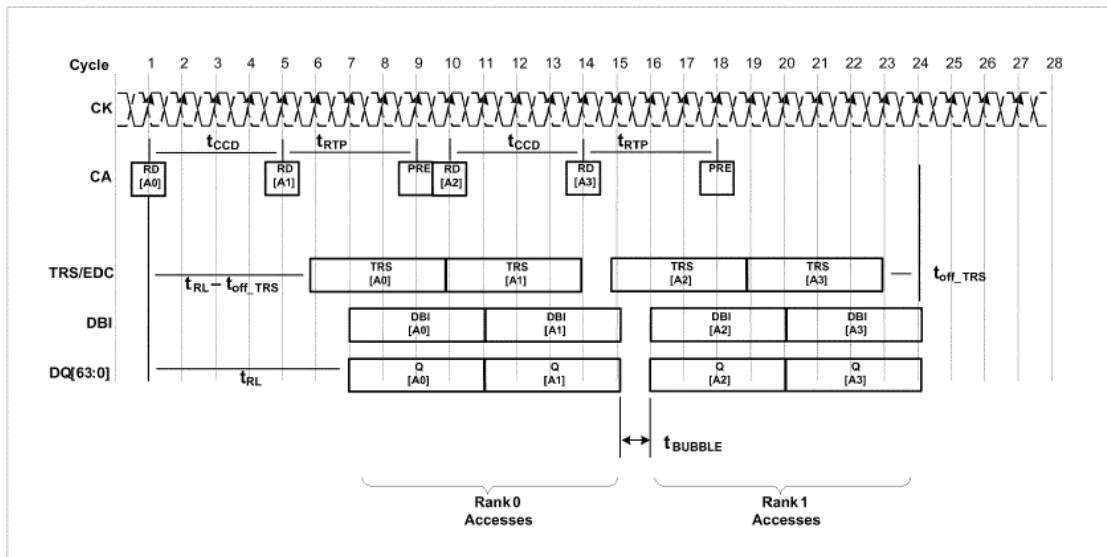


FIG. 4B

163. Shaeffer expressly teaches that these signaling techniques can be used with a memory controller stacked with the memory devices in a through-silicon via (TSV) stack. Id. 11:4-18.

C. **U.S. Patent Publication No. 2010/0195364 by Riho (“Riho2”) (EX1018)**

164. U.S. Patent Application No. 12/656,485 by Riho (“Riho2”), titled “Semiconductor Device,” was filed on February 1, 2010, and was published as U.S. Patent Pub. No. 2010/0195364 on August 5, 2010. EX1018 (Riho2) at 1. Riho2 issued as U.S. Patent No. 8,243,486 on August 14, 2012. EX1053.

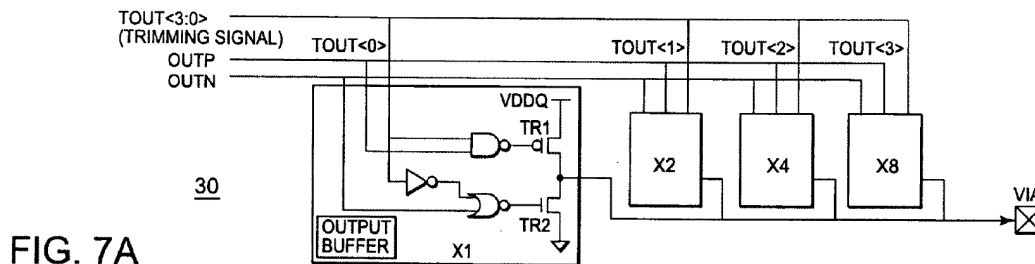
165. Because Riho2 was published on August 5, 2010, before the earliest claimed priority date of the ’087 Patent (November 3, 2010), I understand that Riho2 is prior art to the ’087 Patent under at least 35 U.S.C. § 102(a) (pre-AIA). Alternatively, because the claims of the ’087 Patent lack written description and are not entitled to claim priority before the application for the ’087 Patent was filed on March 14, 2022, as explained above, *see supra* ¶¶95-148, I understand that Riho2 is also prior art to the ’087 Patent under 35 U.S.C. § 102(a)(2) (post-AIA).

166. Although Riho2 was cited during prosecution of the ’087 Patent, *see* EX1002, 72, Riho2 was not discussed during prosecution (either alone or in the combinations with other references that I identify below as Ground 4).

167. Riho2 discloses “a semiconductor device formed by stacking a plurality of chip dies.” EX1018 (Riho2) at [0003]. Riho2 explains that “the fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to

ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the fac[t] that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips.” *Id.* at [0010].

168. To solve these problems, Riho2 discloses “a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance.” *Id.* at [0097] and Fig. 7A (reproduced below).



VI. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE '087 PATENT

169. My analysis below is based on my understanding of the law and the other information discussed above.

A. Reasons to Combine for Grounds 3 and 4

170. A Skilled Artisan would have been motivated to make the combinations in Grounds 3 and 4 for at least the following reasons.

1. Ground 3 combination: Keeth + Shaeffer

171. As discussed immediately below and further down with respect to specific claim limitations, it would have been obvious to a Skilled Artisan to combine the teaching of Keeth (EX1047) and Shaeffer (EX1048).

172. Keeth and Shaeffer are analogous art to the '087 Patent, as each is directed to stacked memory devices, and each is reasonably pertinent to the problem of improving memory operations in the stack, including their speed, signal timing, and/or bandwidth. EX1001 ('087 patent) at 1:33-34 (“the present disclosure relates to a memory package having stacked array dies”), 8:1-4 (“Advantageously, ... by using multiple data conduits instead of a single data conduit, the speed of the memory package ... can be increased.”), 21:26-28 (“controlling the timing of the command/address signals may reduce or slow signal degradation”); EX1047 (Keeth) at 1:55-60 (“In many embodiments, dice may be arranged in a stack on an interface die...”), 10:66-11:7 (“Selective structuring of connective paths in a stack of dice may thus be useful ... to increase the operational speed of elements in the stack(s)”), 5:63-67 (“By interleaving the conductive paths in the dice stack 502, the interface die 510 may access each die

(or a partition of each die) independently of the die above or below, and the interface die 510 may concurrently access dice 520 through 523, thereby increasing bandwidth.”); EX1048 (Shaeffer) at 11:12-18 (“memory controller 510 may be stacked with one or more memory devices 512 in a through-silicon via (TSV) stack”), 1:15-20 (“the present embodiments relate to a method, apparatus and protocol for high speed signaling between a memory device and a memory controller”), 2:23-26 (“methods, protocols and apparatus for performing timing updates for memory transactions between a memory controller and a memory device ”).

173. A Skilled Artisan would have been motivated to use advantageous signaling techniques from Shaeffer in the memory stacks of Keeth.

174. As discussed above, Keeth discloses a stack of memory dice (202) and an interface die (210) with multiple “vaults” and respective vault control circuits (212) to control memory “partitions” in the stack. EX1047 (Keeth) at 3:44-4:16, Fig. 2 (below, annotated).

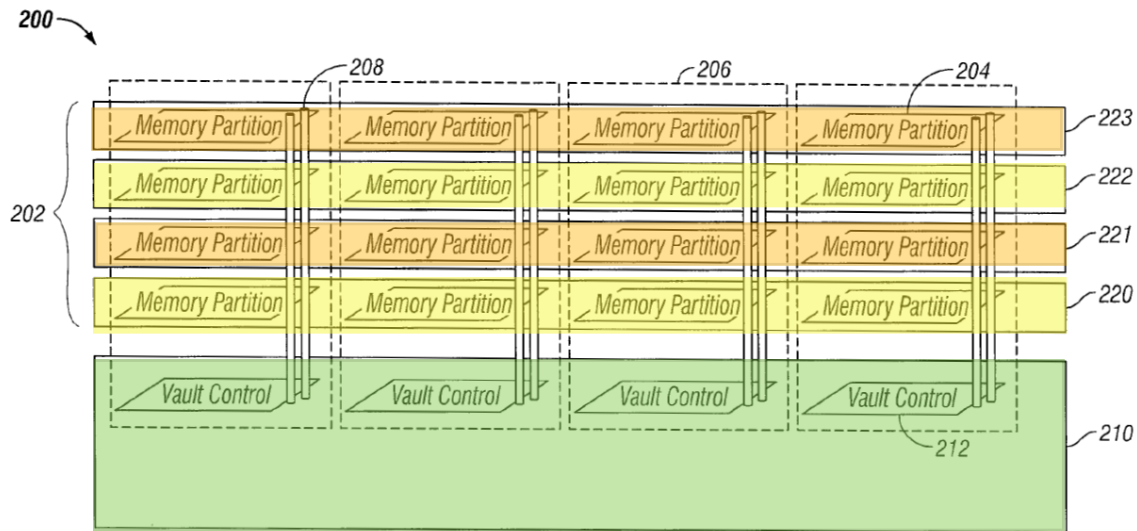


FIG. 2

175. Keeth's "control circuits 212 ... enable communication and control with the corresponding memory partition 204 ... via communicative paths 208." *Id.* 3:44-54. Such communicative paths "may communicate (e.g., transfer) information such as data, address, control, ID information, among other information." *Id.* 3:5-8. Keeth discloses that, by using its vaults and interleaving connections, "a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth," *id.* 4:4-16, and this may "increase the operational speed of elements in the stack(s)," *id.* at 10:66-11:7. Keeth further explains that, "with input/output circuitry connected to the interface die via interleaving conductive paths and command and/or address circuitry of the dice connected to the interface die via

interleaving conductive paths, each vault may be independently controlled.” *Id.* at 6:19-24.

176. Thus, a Skilled Artisan would have been motivated to use Keeth’s independently controlled vaults and interleaving connections in combination with other stacked memory architectures to keep these advantages. Keeth, however, does not provide the details of the signaling protocols. Accordingly, a Skilled Artisan would have been motivated to look for advantageous signaling protocols that can be used in Keeth’s memory vaults and interleaving connections.

177. Shaeffer discloses “apparatus and protocol for high speed signaling between a memory device and a memory controller” where the “memory controller ... may be stacked with one or more memory devices ... in a through-silicon via (TSV) stack.” EX1048 (Shaeffer) at 11:10-18, 11:19-24 (“In some embodiments, memory controller 510 is a local memory controller ... (which may be implemented in ... an application-specific integrated circuit (ASIC)...”). Thus Shaeffer, like Keeth, uses a TSV stack where the memory controller is stacked with the controlled memory dice. Accordingly, a Skilled Artisan would have been motivated to implement advantageous aspects of Shaeffer’s high speed signaling functionality in Keeth’s memory stack.

178. For example, Shaeffer discloses that high speed signaling can be achieved using connections for command/address signals (C/A 114) separate from connections for data signals (120/128). EX1048 (Shaeffer) at Fig. 1A.

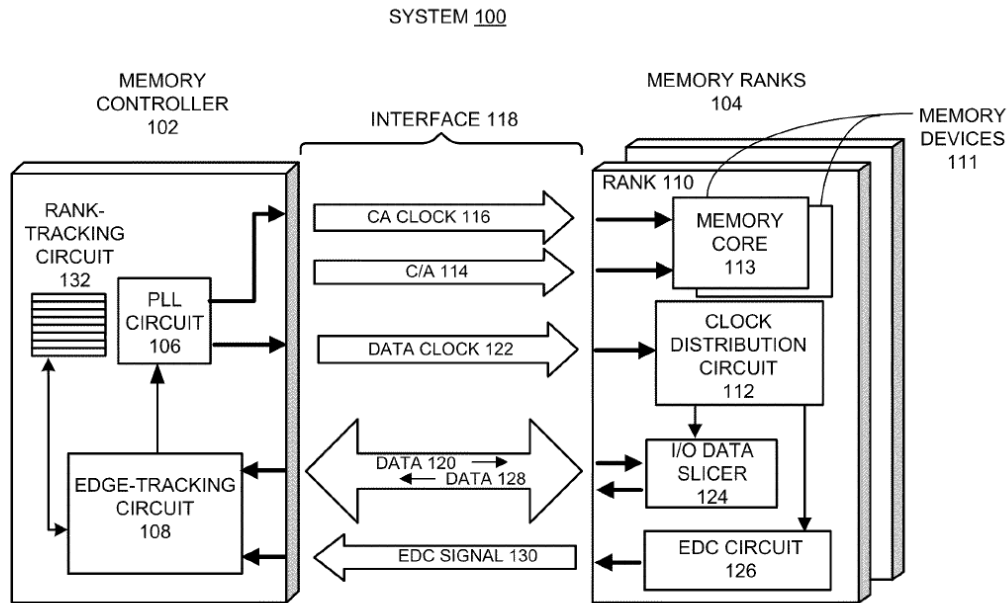


FIG. 1A

179. A Skilled Artisan would have understood that, by using separate C/A and data connections, the bandwidth of the data transfer can be increased, since C/A connections can be used to schedule further data transfer while the previous data transfers are still being communicated on the data connections. For example, as shown in Fig. 4B of Shaeffer, the data transfer (Q[A0] and Q[A1]) on data lines DQ[63:0] can be carried out for previous read commands (RD[A0] and RD[A1]) while new read commands (RD[A2] and RD[3]) are being received for subsequent read operations. EX1048 (Shaeffer) at Fig. 4B.

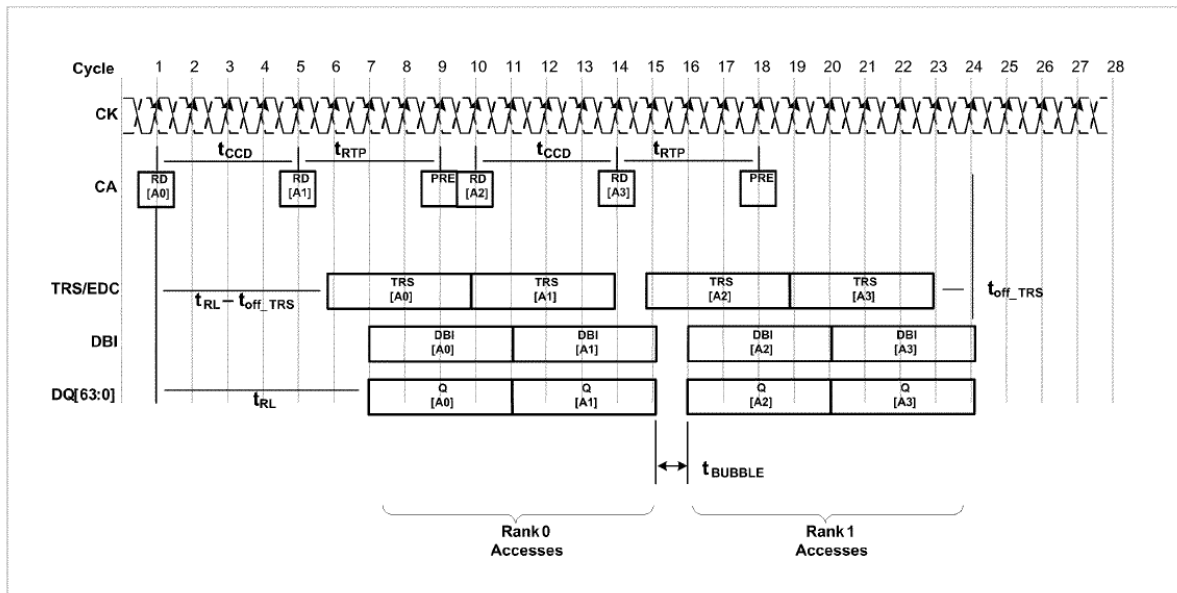


FIG. 4B

180. Furthermore, Keeth expressly teaches that the stacked memory devices can be similar to DDR3 SDRAM devices. EX1047 (Keeth) at 2:37-41 (“double-data-rate three synchronous dynamic random access memory (DDR3-SDRAM), or the like”). The corresponding JEDEC standards require separate C/A and data lines for DDR3 SDRAM. *See, e.g.*, EX1019 (JESD79-3C) at p.12, Fig. 3 (below, 4-stacked DDR3 memories having control/address (C/A) lines like RAS, CAS, WE, An, and BAn, separate from data lines DQ0-15).

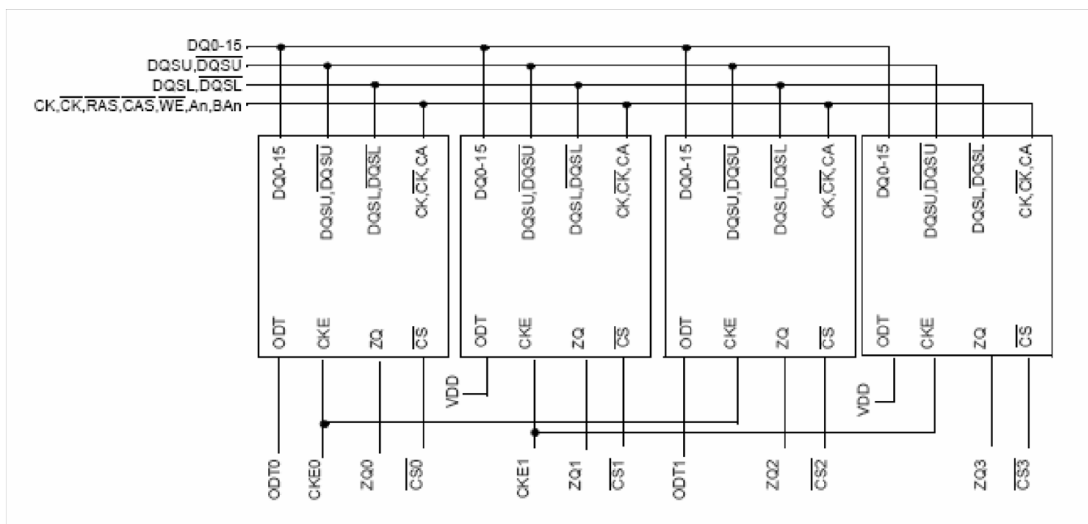
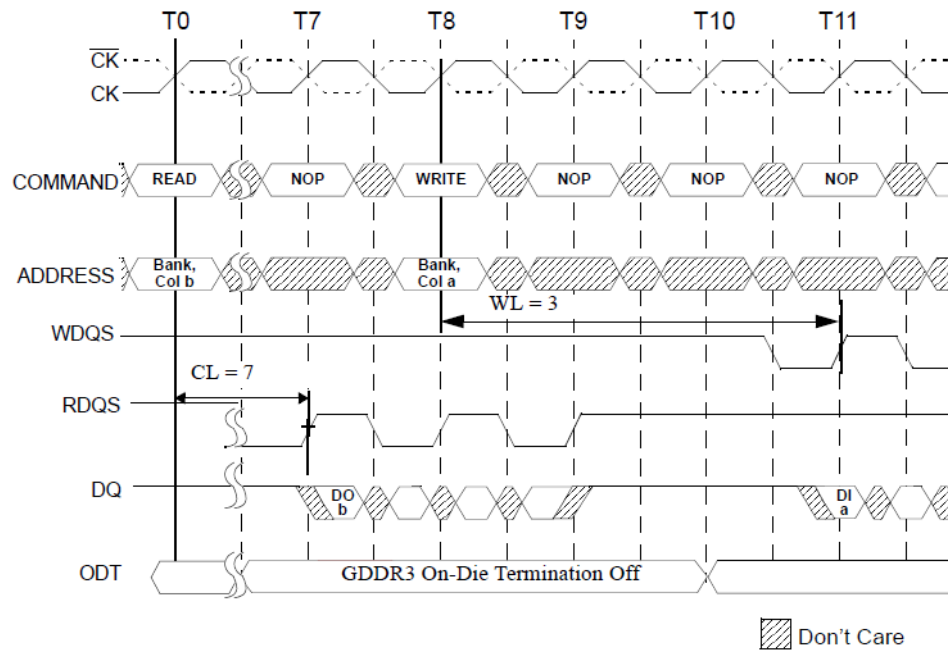


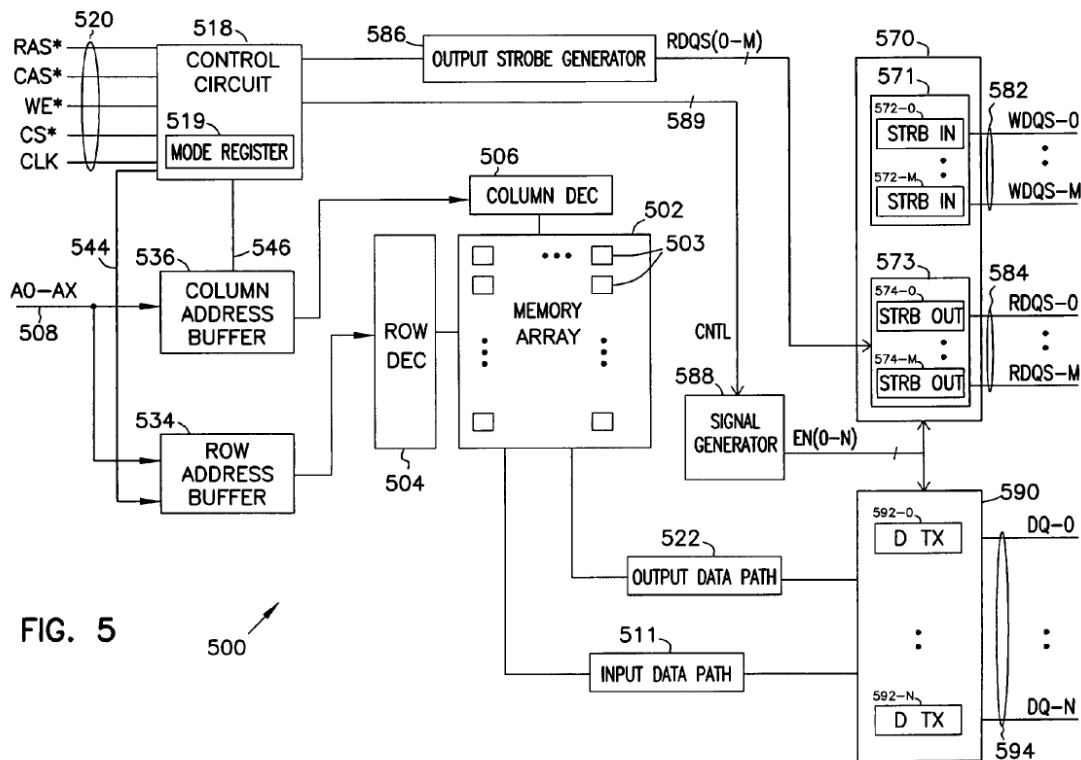
Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

181. Shaeffer similarly teaches that its memory devices can be “graphics double data rate (GDDR, GDDR2, GDDR3, GDDR4, GDDR5, and future generations) and double data rate (DDR2, DDR3 and future memory types).” EX1048 (Shaeffer) at 8:60-64. Like DDR memories, GDDR3 memory devices also used separate command, address, and data (DQ) lines. EX1036 (JESD 21-C 3.11.5.7) at 9 (reproduced below).

READ To WRITE



182. Memory device using separate lines for address (A0-AX), command (including RAS, CAS, WE) and data (DQ-0,...,DQ-N) signals was a well-known, widely used technique. See, e.g., EX1051 (Schnarr) at Fig. 5.



183. A Skilled Artisan would have understood that the same separate C/A and data connections can be used in a stack in order to communicate with memory dice using such separate C/A and data connections. Indeed, stacks of memory dice that used separate C/A and data lines (implemented by TSVs) were well known at the time. *See, e.g.,* EX1043 (US8,593,899 to Ide) at Fig. 4 (separate TSVs for data signals DQ0-DQ15 and for commands/address signals from Command Input buffer and Address Input buffer).

dice 520 through 523 may be connected to and utilize the interleaving conductive paths ... which may perhaps increase bandwidth and reduce queuing of signals.”

Id.

185. Shaeffer further teaches that timing updates may be required during memory operations to compensate for noise or drift in temperature or supply voltage. EX1048 (Shaeffer) at 2:10-22. Shaeffer discloses that such timing updates can be achieved using a timing reference signal (TRS) output by the memory device in response to a read command. *Id.* 2:23-49. “The TRS, in an embodiment, is conveyed from the memory device, to the memory controller via a signaling resource (i.e., signal traces, pins etc.,) that is also used to transfer error detection and correction information (EDC).” *Id.* 2:64-3:4, Fig. 4B (reproduced below).

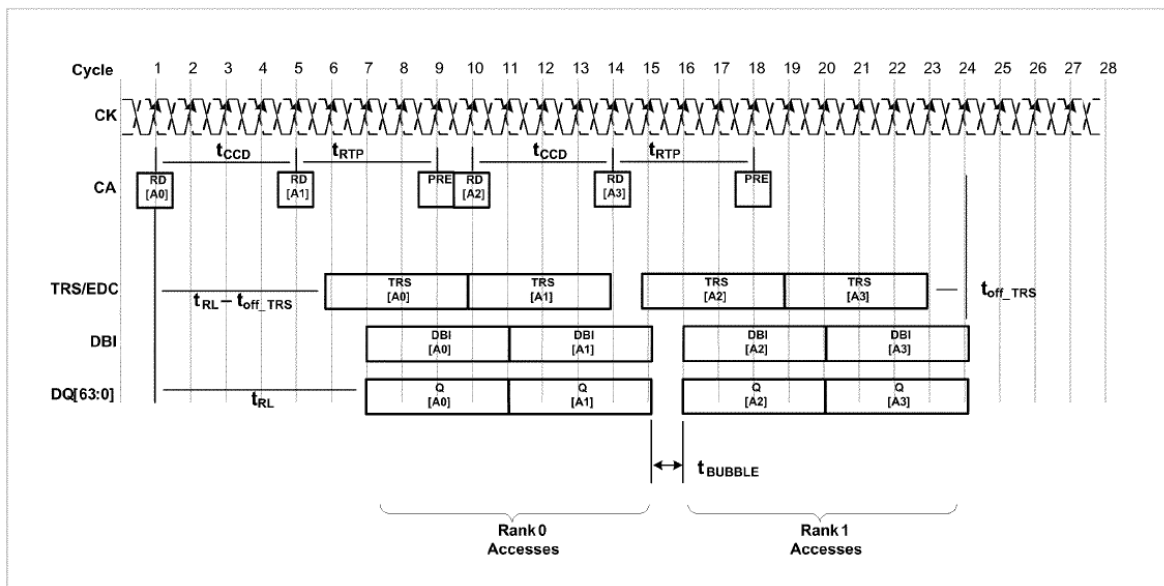


FIG. 4B

186. Therefore, a Skilled Artisan would have been also motivated to implement Shaeffer's signaling protocol, including EDC and TRS transmissions from the memory devices, in Keeth's memory stack in order to provide error detection and correction as well as timing updates to compensate for noise or drift in temperature or supply voltage.

187. Furthermore, Shaeffer teaches using a data clock or a data strobe (122) to help the memory devices to capture write data from the memory controller. EX1048 (Shaeffer) at Fig. 1A, ("write data 120 is directly clocked on rank 110 by data clock 122"), 9:1-9 ("a clock signal in the context of the instant description may be embodied as a strobe signal ... that conveys timing information, and is not limited to a signal that is strictly periodic. For example, a

timing reference may be a clock signal, which is periodic (however, it may be gated), or may be a strobe signal (that is aperiodic in the sense that it indicates when to sample data)").

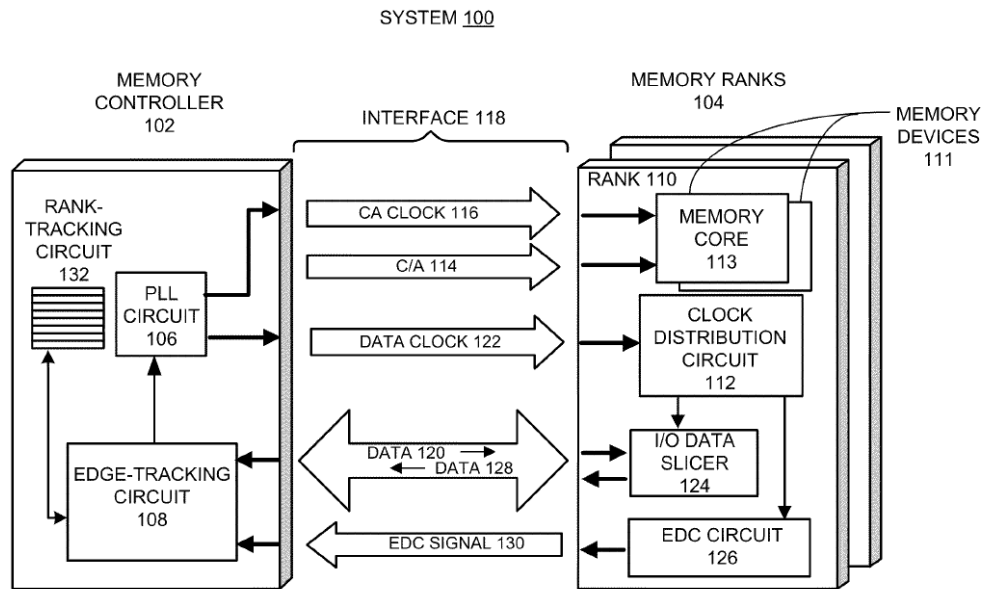


FIG. 1A

188. As shown in Fig. 1A of Shaeffer, the data clock/strobe 122 is a unidirectional signal from the control die to the memory die and is used for capturing write data. *Id.* Shaeffer teaches that its control die advantageously captures the read data with proper, rank-specific timing using an edge tracking circuit 108 and a rank tracking circuit 132. *Id.* at 3:62-4:6 (“to facilitate the memory controller switching between servicing read operations directed to different ranks, phase information for each individual rank can be stored at the memory controller”). Shaeffer expressly teaches that its techniques for high speed

signaling can be used in a TSV stack. *Id.* at 1:15-19 (“protocol for high speed signaling”), 11:4-15 (“embodiments of memory systems that may use one or more of the above-described ... techniques ...[include] a through-silicon via (TSV) stack.”). For example, unidirectional strobe signals for write operations (WDQS) were a standard, well-understood technique at the time used for high-speed write operations, as evidenced by Schnarr discussed above (disclosing separate RDQS and WDQS strobe lines for read and write operations, respectively). EX1051 (Schnarr) at 9:19-34 (“The write strobe signals (bits) WDQS-0 through WDQS-M on lines or strobe terminals 582 represent the timing information of the input data. ... The read strobe signals RDQS-0 through RDQS-M on lines or strobe terminals 584 represent the timing information of the data outputted from memory device 500.”), Fig. 5 (reproduced above). Furthermore, a Skilled Artisan would have understood that a strobe signal uses less power than a continuous clock signal. Therefore, a Skilled Artisan would have been motivated to implement Shaeffer’s write data strobe functionality and its read data capturing functionality in the memory stack of Keeth.

189. As evidenced by these prior art references, including industry standards, the use of certain aspects of Shaeffer’s signaling protocols—such as command/address lines being separate from the data lines, the use of timing reference and error detection signal lines, and write strobe signal lines—to

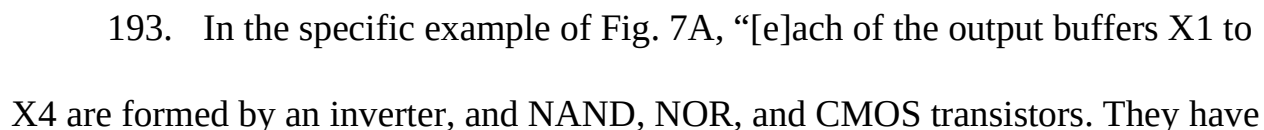
communicate with memory dice in a stack in the memory stack of Keeth was well within the level of skill at the time and a Skilled Artisan would have had a reasonable expectation of success in making the combination. For example, Keeth teaches that its interleaving paths can be used for control, address and data signals and Shaeffer discloses specific tools which can be used to implement its teaching about signaling protocol. EX1047 (Keeth) at 3:5-8 (“The conductive paths 106 may communicate (e.g., transfer) information such as data, address, control, ID information, among other information.”); EX1048 (Shaeffer) at 12:28-29 (“Devices and circuits described herein may be implemented using computer-aided design tools available in the art...”).

2. Ground 4 combination: Ground 3 + Riho2

190. Riho2 (EX1018) is analogous art to the '087 Patent and to the Keeth and Shaeffer references. As discussed above, Keeth and Shaeffer are analogous art to the '087 patent, as each is directed to stacked memory devices, and each is reasonably pertinent to the problem of improving memory operations in the stack, including their speed, signal timing, and/or bandwidth. *Supra*, ¶172. Riho2 is also directed to stacked memory devices and is reasonably pertinent to the same problem.

191. For example, Riho2 discloses “stacking a plurality of chip dies,” such as DRAM chips. EX1018 (Riho2) at [0003]. Riho2 explains that “the fabrication

FIG. 7A



the same circuit configuration, but their transistors are of mutually different sizes” and “trimming signals TOUT generated by the third ROM are ... controlling the number of output buffers to be activated.” *Id.* at [0097-98]. Thus, Riho2 teaches selecting the number of transistors and/or the size of the transistors that are included in the buffer which drives a signal, similar to the '087 Patent. EX1001 at 17:26-28 (“The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver.”).

194. A Skilled Artisan would have understood that the changes in the time constant are also present in the combination of Keeth and Shaeffer. In particular, signals are driven from the control die to the memory dies through conductive paths in the stack of the Keeth-Shaeffer combination. *Supra*, ¶¶175-178. These conductive paths include TSVs and joints and can couple to I/O circuits, and a Skilled Artisan would have understood that the load to be driven is determined by the parasitic capacitance and resistance on the interleaving conductive paths, including the load of the TSVs, joints, and the I/O circuits coupled to these interleaving paths. EX1047 (Keeth) at Fig. 7 (reproduced below).

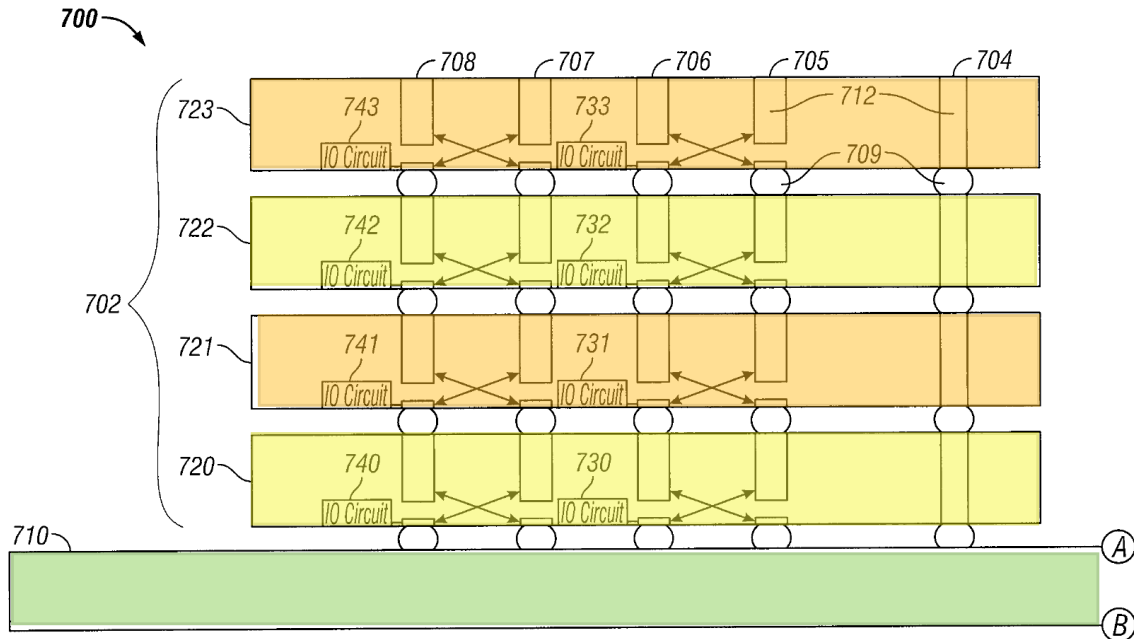


FIG. 7

195. For example, Keeth discloses that “conductive paths 704, 705, 706, 707, and 708 of the first dice stack 702 include joints 709 and TSVs 712, at least some of which extend entirely through the dice stack 702 and some of which connect with circuitry.” *Id.* at 7:37-45. Keeth further explains that the conductive paths “may entirely pass through or partially pass through the dice stack.” *Id.* 5:34-38.

196. A Skilled Artisan would have understood from Keeth’s disclosure that, as an example, the conductive path 706 can end in die 722 without passing through dies 722 and 723, and does not require a TSV in, nor a joint between, dies 722 and 723, because the last I/O circuit the conductive path 706 is connected to is I/O circuit 732 in die 722. *Id.* at Fig. 7. In contrast, conductive path 705 has to

pass through die 722, since it is coupled to I/O circuit 733 in die 723 above. Thus, in implementations where Keeth's conductive paths only "partially pass through" the stack, different conductive paths may have different length. Accordingly, a Skilled Artisan would have understood that the load and the corresponding time constant of the conductive paths would typically be different depending on their length, e.g., because they "extend entirely through" or "partially pass through" the stack.

197. Furthermore, Riho2 explains that "it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another." EX1018 (Riho2) at [0096]. A Skilled Artisan would have understood that such varying parasitic capacitance and resistance is inherent in the manufacturing process. EX1016 (Riho) at [0056] ("Further, it is also preferable to expect that when a plurality of signal lines are formed by a plurality of TSVs, the impedance of each signal line may be different from those of the others due to variations of inherent manufacturing processes."). A Skilled

Artisan would have also understood that “the SDRAM chip located closer to the ...[control die] has a smaller penetrating through resistance while the SDRAM chip located farther from the ...[control die] has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process.” *Id.* at [0061]. Accordingly, a Skilled Artisan would have also understood that the loads (and the corresponding delays) of the different conductive paths can vary due to manufacturing variations of the joints and TSVs and due to the different locations of the coupled I/O circuits from the control die.

198. Thus, a Skilled Artisan would have been motivated to look for techniques addressing these timing problems and implement a known, reliable solution, such as the driver-size optimization techniques of Riho2. A Skilled Artisan would have been motivated to implement Riho2’s optimization techniques because it may advantageously improve and stabilize high frequency memory operations despite the time-constant variations in the stack of the Keeth-Shaeffer combination. EX1018 (Riho2) at [0010-11]. A Skilled Artisan would have further understood that the driver-size optimization techniques of Riho2 can save power, thus providing additional motivation to their use in the combination of Keeth and Shaeffer. *See, e.g.*, EX1017 (Wyman) at 1:22-24 (“In instances where chips are

stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.”).

199. Furthermore, Riho2 discloses that, “[i]n practice, it has been found that various problems such as increased power consumption and deteriorated yield would occur when the data transfer speed from the DRAM chips is increased.” EX1018 (Riho2) at [0008]. To solve the problem of increased power consumption, Riho2 teaches that “data signals are transmitted and received through the 256 data transfer through electrodes formed in the 256 vias. In this case, each data transfer through electrode only need be capable of transmitting and receiving data signals at a data transfer rate of 400 Mbps (102.4 Gbit/256). ...This enables the memory module to stably communicate with the memory controller at a low power consumption, and provides a memory module having a data transfer speed of 12.8 Gbytes/sec.” *Id.* at [0052]. In addition to reducing power (and current), Riho2 further teaches that operating the memory chips at a lower frequency can also increase yield. *Id.* at [0148] (“Further, according to this invention, the data transfer speed of the memory module as a whole can be increased without the need of increasing the data transfer speed from the chip dies, which provides an advantage that the consumption current of the chip dies can be reduced. Still further, the chip dies can be operated at a low operating frequency, and thus the manufacturing yield of the chip dies can be enhanced.”).

200. Thus, a Skilled Artisan would have been motivated by the disclosure of Riho2 to operate Keeth's communication paths inside the stack at a rate that is lower than the "appropriate data transfer rates" with an external processor, which advantageously results in lower power consumption.

201. Operating the memory chips at a lower rate than the rate for communicating with a processor was well within the level of skill at the time. EX1023 (Jacob paper) at 19 ("As mentioned earlier, interleaving multiple memory banks has been a popular method used to achieve high bandwidth memory busses using low-bandwidth devices. The technique goes back at least to the mid-1960's . . ."). For example, Keeth discloses that its interface die includes "circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates." EX1047 (Keeth) at 3:62-67. A Skilled Artisan would have understood how to implement "circuitry ... to accommodate ... appropriate data rates," including parallel-to-serial and serial-to-parallel conversion circuits. *See, e.g.*, EX1018 (Riho2) at [0053] ("On the other hand, the memory controller has a parallel-serial conversion circuit (not shown). For example, during read data communication from the memory chip dies, the parallel-serial conversion circuit converts data transmitted by the chip dies at 400 Mbps into 1600-Mbps serial data signals and provides the same to a CPU or the like. Further, the memory controller also has a serial-parallel conversion circuit for

converting 1600-Mbps serial data signals from the CPU or the like into 400-Mbps parallel data and transmitting the same to the chip dies.”).

202. A Skilled Artisan would have also understood that implementing Riho2’s optimization techniques in the combination of Keeth and Shaeffer was well within the level of skill, and a Skilled Artisan would have had a reasonable expectation of success in making the combination. For example, Riho2 teaches specific implementations for the buffer circuit using different number of transistors and/or transistors of different sizes to achieve a range of available drive capacities. EX1018 (Riho2) at Fig. 7A and [0097-98]. A Skilled Artisan would have understood that this range of available drive capacities can be selected, e.g., by using computer-aided design tools for a specific design, such as the combination of Keeth and Shaeffer. EX1048 (Shaeffer) at 12:28-29 (“Devices and circuits described herein may be implemented using computer-aided design tools available in the art...”). A Skilled Artisan would have also understood that the selection of the transistors in Riho2’s buffer can be implemented not just by ROMs but also by other known ways, such as anti-fuses or breaking connections. EX1018 (Riho2) at [0041]. (“These ROMs 2700 to 2731 may be EEPROMs or may be configured as anti-fuses. The same applies to other ROMs to be described later.”); *see also* EX1017 (Wyman) at 5:34-44 (“disable any remaining downstream stage(s) by using a via to break one or more connections”).

B. Claims 1-28 Are Unpatentable Over Grounds 3 and 4

203. In my opinion, claims 1-28 of the '087 Patent are obvious in light of Grounds 3 and 4. I have compared each and every limitation in claims 1-28 to Grounds 3 and 4 and I have prepared a claim chart showing why each and every limitation is obvious in light of Grounds 3 and 4. See EX1093. In the paragraphs below, I focus on providing context and technical explanations related to specific limitations.

1. [1.b.2] C/A and data ports and DRAM memory cells

204. Claim 1 requires “*each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells.*”

205. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

206. Keeth discloses that the conductive paths between the memory dice and the control circuit in the stack can “communicate (e.g., transfer) information such as data, address, control, ID information, among other information.” EX1047 (Keeth) at 3:5-8. In the example of Fig. 5, “the command circuits and/or address circuits of each dice 520 through 523 may be connected to and utilize the interleaving conductive paths 505 through 508 in order to communicate command

and/or address signals between the interface die and dice 520 through 523 which may perhaps increase bandwidth and reduce queuing of signals.” *Id.* at 6:4-10, Fig. 5. A Skilled Artisan would have understood from this disclosure that “the command circuits and/or address circuits of each dice,” which may be located in “I/O Circuits” 530-533 in Fig. 5 below, include command and address “C/A ports” “to communicate command and/or address signals.” *Id.*

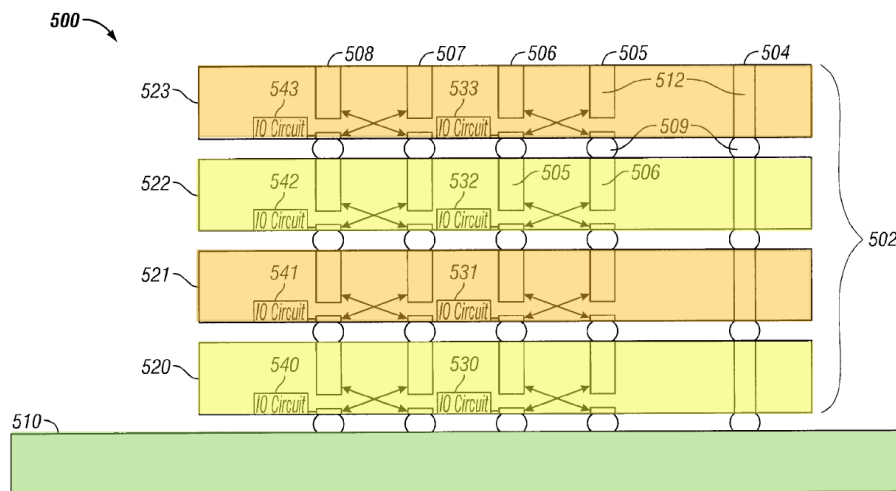


FIG. 5

207. Keeth also discloses that, “a first communication path in a vault may be connected to circuitry (e.g., input/output circuitry) of all odd partitions in the memory vault and pass through the even vaults without connecting to circuitry. A second communication path may connect to circuitry (e.g., input/output circuit) on the even partitions in the same vault and pass through the odd partitions without connecting to circuitry. By interleaving the connections, a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple

partitions in the vault and thereby improve bandwidth.” EX1047 (Keeth) at 4:4-

16. A Skilled Artisan would have understood from this disclosure that the input/output circuitry on each DRAM die, which may be located in “I/O Circuits” 530-533 in Fig. 5 above, also includes “*data ports*” in order to “access and send data to” the memory partitions. *Id.* As discussed above, a Skilled Artisan would have been motivated to have each DRAM die to include its “*C/A ports*” for communicating command and address signals separate from its “*data ports*” for communicating the data signals as taught by Shaeffer and was common at the time for DRAM devices. *Supra* at ¶¶178-184.

208. Also, both Keeth and Shaeffer disclose DRAM memory dice, and a Skilled Artisan would have understood that “*each DRAM die of the stacked DRAM dies includ[es] ... DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells.*” Keeth, for example, discloses “memory devices to store data” and that “[e]ach memory partition 204 may include a plurality of memory cells.” EX1047 (Keeth) at 1:11-13, 3:57-58; *see also* EX1048 (Shaeffer) at Fig. 1A (showing a memory core 113) and 3:20-24 (“each memory device 111 is a single chip having a memory core 113”). A Skilled Artisan would have understood that the data communicated with the DRAM devices through their “*data ports*” is stored in “*DRAM memory cells*,” making clear that “*the each DRAM die is configurable to transfer data*

between the data ports and the DRAM memory cells” in order to write and read data to and from the DRAM die. EX1048 (Shaeffer), e.g., at Fig. 4A (showing read and write data transfers). It was well known that “*data ports*,” like those of “Data In/Out Buffers” in Prof. Jacob’s textbook, and an array of storage cells were parts of the “[b]asic organization of DRAM internals.” EX1022 (Jacob) p.317 (Figure 7.3, reproduced below).

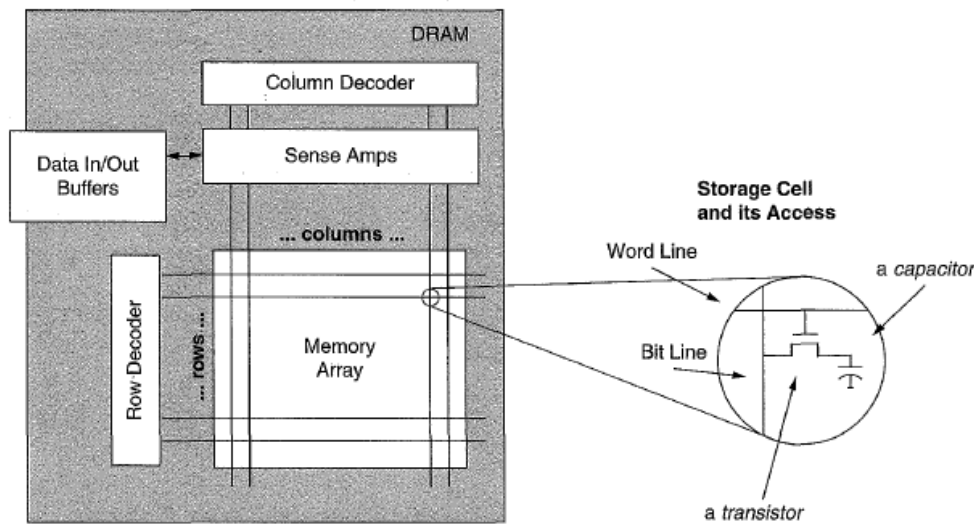


FIGURE 7.3: Basic organization of DRAM internals. The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

209. Like DRAM dies in general, DRAM dies in a stack also have an array of memory cells that store data and data ports through which that data is communicated. See, e.g., EX1043 (Ide) at Fig. 4 (below, showing data control circuit 54 to transfer data between the data ports coupled to the TSVs for data and the DRAM memory cell array 50).

212. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

213. “For example, a stack of memory dice may be connected to an interface die to provide input/output functionality with other components.” EX1047 (Keeth) at 1:58-60. In the example of Fig. 2, “[i]nterface die 210 may include additional circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates between the apparatus 200 and another device, such as processors or a memory controller in communication with the stack 202 by way of the interface die 210.” *Id.* at 3:62-67; *see also id.* at 3:9-16 (“apparatus 100 may be communicatively coupled with external devices, e.g., processors and memory controllers”), Fig. 10 (memory controller 1030). A Skilled Artisan would have understood from this disclosure that the package of the stacked DRAM dice has “*terminals*,” such as pins or balls, to provide electrical connections to communicate with other components, such as a processor or a memory controller, in order to write data into and read data from the stacked DRAM dice by sending address signals and/or command signals through “*C/A terminals*” and communicate the corresponding data through “*data terminals*.” EX1022 (Jacob) at 322 (“the address pins for most DRAMs are still multiplexed”) and 348 (“Increase DRAM Data Width ... the number of data pins has increased from x1 parts in the late 1980s to x32 parts”). Keeth also specifically mentions

that “the device may comprise a stacked memory device such as ... a DRAM, double-data-rate three synchronous dynamic random access memory (DDR3-SDRAM), or the like.” EX1047 (Keeth) at 2:37-43. A Skilled Artisan would have understood that a DRAM package similar to stacked DDR3-SDRAMs or the like has “*command and/or address (C/A) terminals*” “*to receive C/A signals via the C/A terminals*” for write or read operations from a processor or a memory controller, and “*data terminals*” “*to receive or output data signals via the data terminals in response to the (C/A) signals*” for the write or read operations. See, e.g., EX1019 (JESD79-3C) at pp.6-11 (“Package Pinout” including “Stacked ...Ballout” having data terminals DQ0, DQ1, ... and command/address terminals RAS#, CAS#, WE#, A0, A1, ...), p.33 (Command Truth table), p.56 (Read operation), pp.68-69 (Write operation); EX1048 (Shaeffer) at Fig. 4A (below outputting data signal, Q[A0] on DQ[63:0], in response to read C/A signal, RD[A0] on CA, and receiving data signal, D[A1] on DQ[63:0], in response to write C/A signal, WR[A1] on CA), 7:11-44.

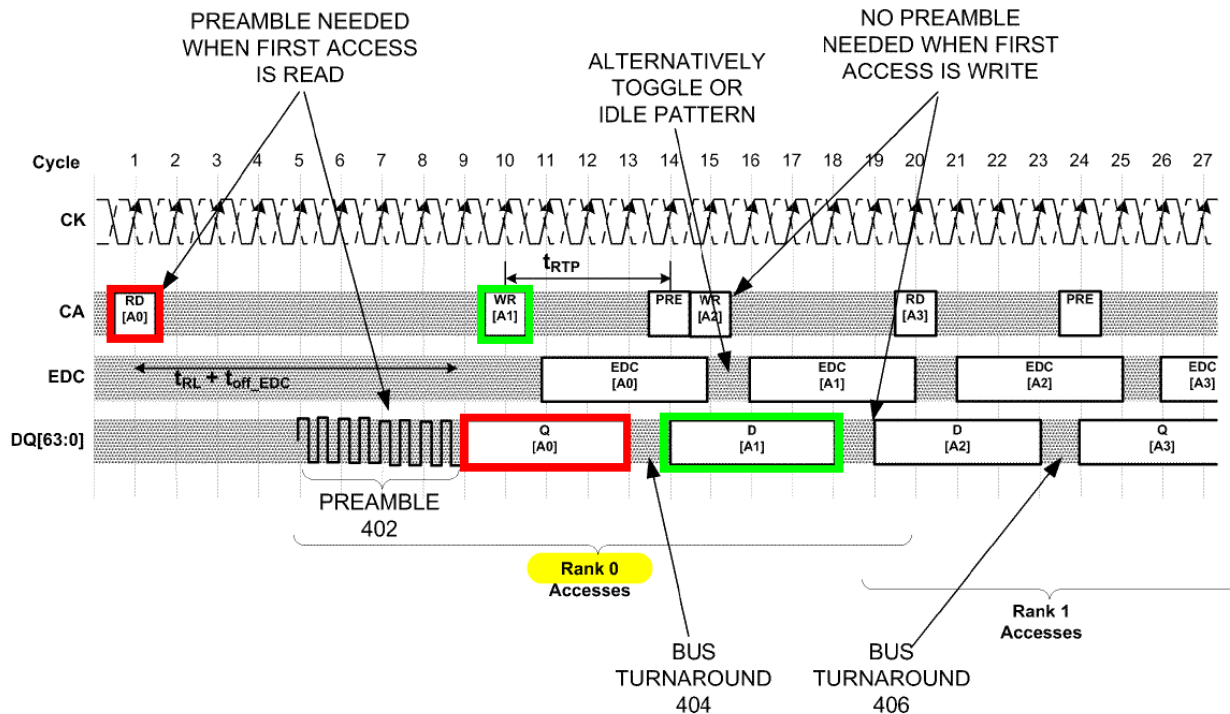


FIG. 4A

Further, for the reasons discussed above, a Skilled Artisan would have been motivated to use terminals for “C/A signals” that are separate from the “data terminals,” as it allowed pipelining the command and data traffic and was common practice at the time. *Supra* at ¶¶178-184; *see also* EX1043 (*Ide*) at 6:62-7:3, Fig. 4 (below, showing the package including stacked DRAM devices having data input/output terminals 14 for data bits DQ0-DQ15 separate from command and address terminals for command and address signals, including /RAS, /CAS, /WE, A0-An, BA0-BA2); *See also* EX1018 (*Riho2*) at Fig. 1 (reproduced below) and ¶[0035] (“There are provided, on the opposite surface of the stacking substrate 20 to the surface where the chip dies are mounted,

BGA (Ball Grid Array) terminals for external data signals, address signals, external control signals, and external clock signals...”).

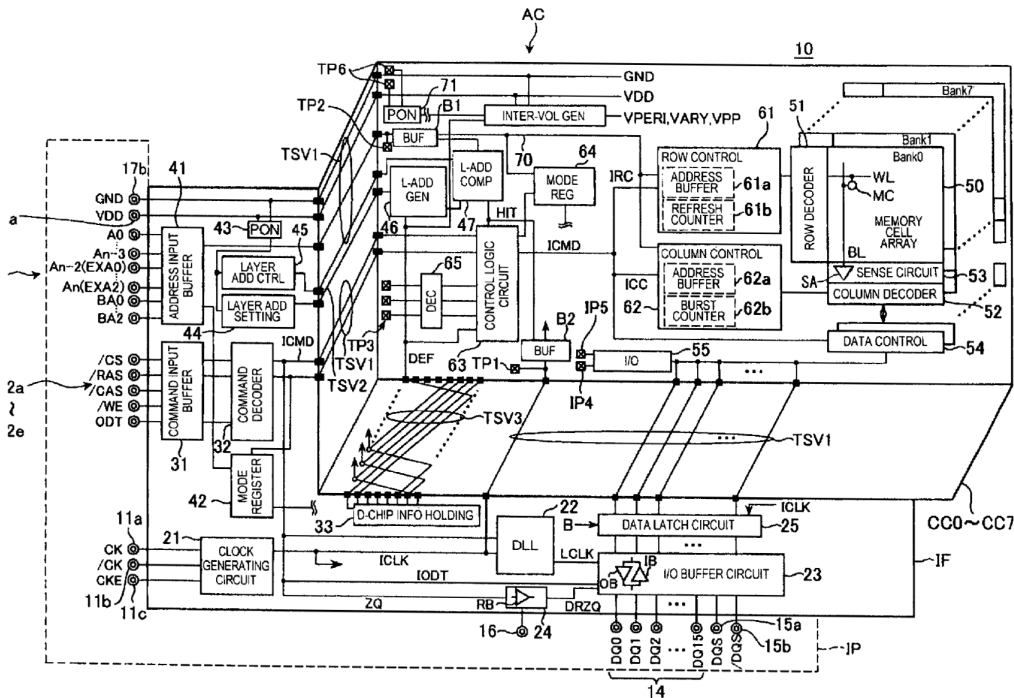


FIG.4

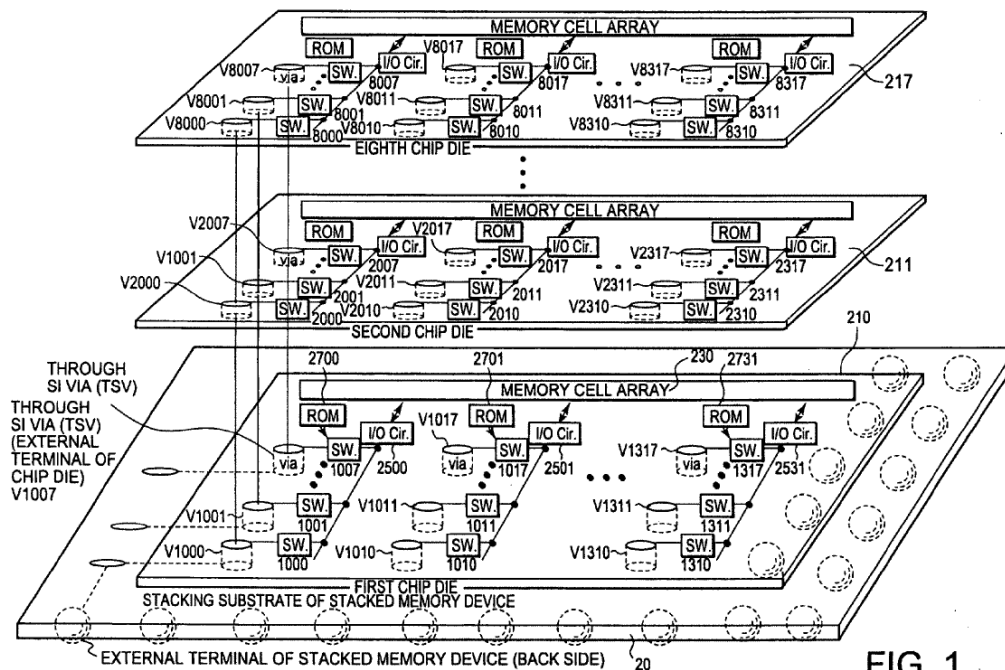


FIG. 1

214. Accordingly, the prior art references in each of Grounds 3 and 4 teach *“terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals.”*

3. [1.e.1] Control Die

215. Claim 1 requires *“a control die coupled between the terminals and the stacked DRAM dies.”*

216. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

217. Keeth discloses that the stack’s interface die is a *“control die”* because it includes control circuits to control memory vaults in the DRAM stack. EX1047 (Keeth) at Fig. 2 (below) and 3:44-54 (“Each die 220 through 223 may comprise a plurality of memory partitions 204 and interface die 210 may comprise control circuits 212 to enable communication and control with the corresponding memory partition 204 stacked above the respective control circuit via communicative paths 208.”).

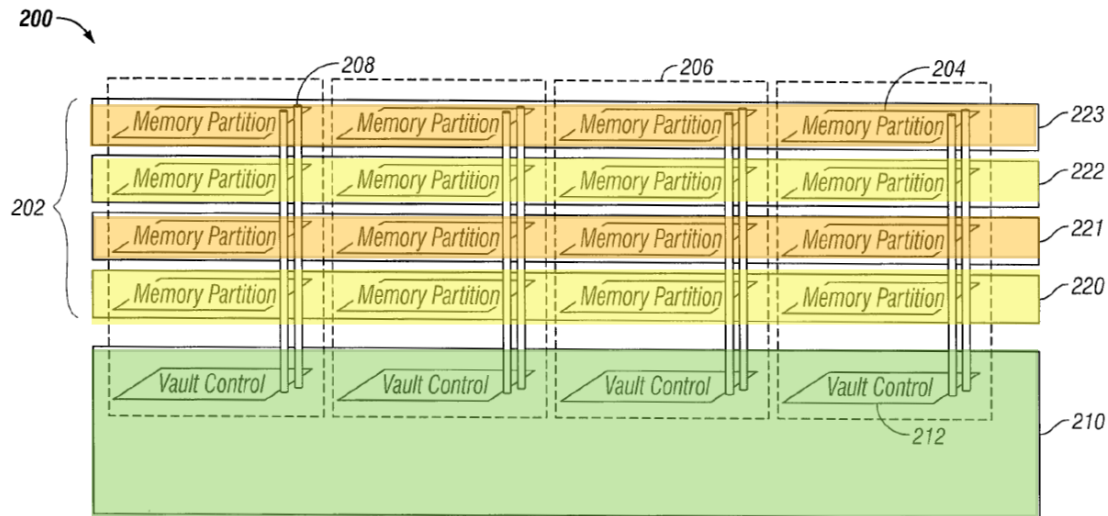


FIG. 2

Keeth also explains that its “[i]nterface die 210 may include additional circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates between the apparatus 200 and another device, such as processors or a memory controller in communication with the stack 202 by way of the interface die 210.” EX1047 (Keeth) at Fig. 2 and 3:62-67. A Skilled Artisan would have understood from this disclosure that Keeth’s “control die” is “coupled between the terminals [coupling to the other devices] and the stacked DRAM dies [in stack 202].” *Id.*, see also 2:61-3:20 and Fig. 1 (reproduced below, showing interface die 110 coupled between a stack 102 of memory dies and package substrate 114, which a Skilled Artisan would understand has the terminals to couple to other components).

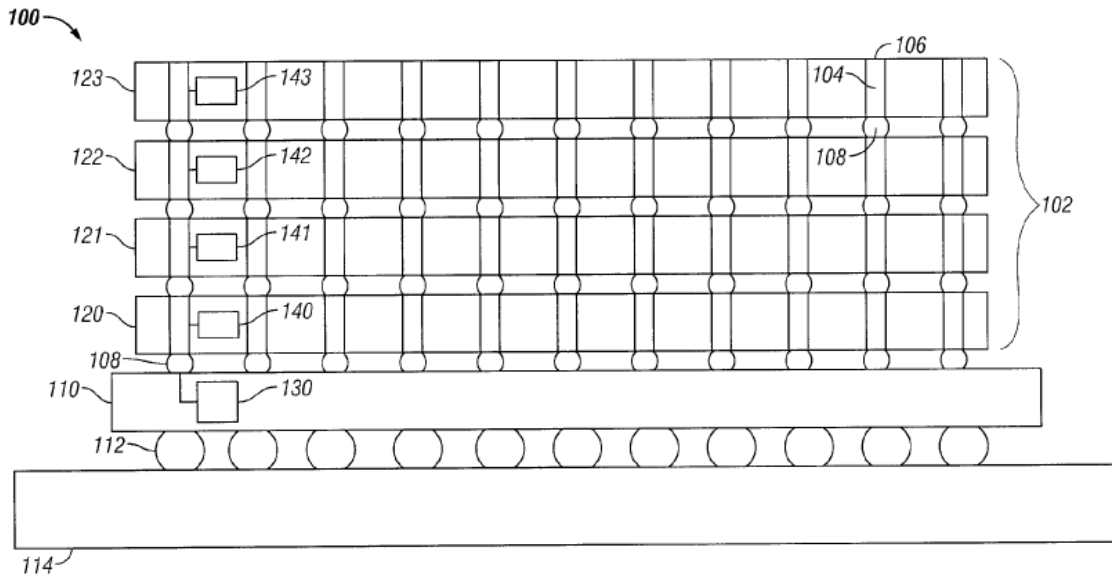


FIG. 1

218. Shaeffer also discloses a “control die” (local memory controller 510) that is “coupled between the terminals [of a package including local memory controller 510] and the stacked DRAM dies [512],” since a local memory controller is communicating with other parts of the system. EX1048 (Shaeffer) at 11:10-24 (“Memory controller 510 and each memory device 512 are individual integrated circuit devices, which may be included in a single chip-package. For example, memory controller 510 may be stacked with one or more memory devices 512 in a through-silicon via (TSV) stack ... [where] memory controller is a local memory controller”). Furthermore, the combination of Keeth and Shaeffer also discloses that the control die of the package is communicating with an external processor. EX1047 (Keeth) at 3:62-67.

219. Accordingly, the prior art references in each of Grounds 3 and 4 teach “*a control die coupled between the terminals and the stacked DRAM dies.*”

4. [1.e.2] Conduits

220. Claim 1 requires “*the control die including conduits, the conduits including C/A conduits and data conduits.*” The ’087 Patent states that conduits can be drivers to transmit a signal. EX1001, 4:33-34 (“conduit (e.g., driver)”), 6:39-40 (“conduit...to transmit a...signal”).

221. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

222. Keeth, for example, discloses that its interface die (“*control die*”) includes “components to control communication to and from” the memory dice. EX1047 (Keeth) at 3:21-26. Keeth also discloses “a command and/or addressing circuit of the interface die 510” in order “to communicate command and/or address signals between the interface die and dice 520 through 523.” *Id.* at 5:30-34, 6:4-10. Keeth further discloses that its interface die has “a vault control circuit” to “access and send data to” memory dice, including “driv[ing] data to partitions within the vaults.” *Id.* at 4:13-16, 6:16-19. A Skilled Artisan would have understood from these disclosures that, in Keeth’s interface die, the command and/or addressing circuit includes “*C/A conduits*” to conduct (e.g., transmit) respective command and address signals through the “*C/A interconnects*” to the memory dice, and the vault

control circuit includes “*data conduits*” to conduct (e.g., transmit and receive) respective data signals through the “*data interconnects*” to and from the memory dice. *Id.* at 3:62-67 (“Interface die 210 may include additional circuitry, e.g., buffers, and I/O drivers ...”).

223. Shaeffer similarly discloses that its controller die includes an I/O interface 518-1 coupled to links 514, and “[s]ignals corresponding to data and/or commands (such as request-for-data commands) may be communicated on one or more of the links 514.” EX1048 (Shaeffer) at Fig. 5 (reproduced below), 11:25-26, 12:4-7; *see also* 8:52-54 (“The above-described techniques and apparatus can be used in different systems having chips that that communicate with one another via chip-to-chip interfaces.”).

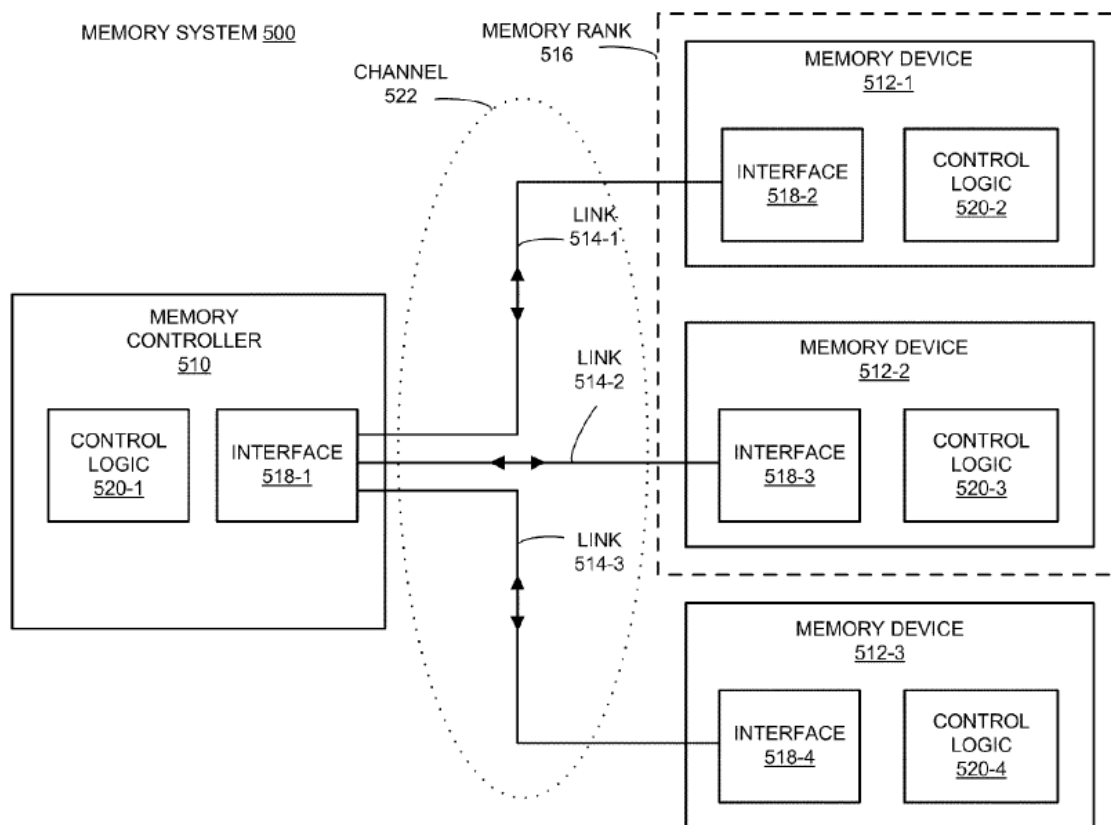
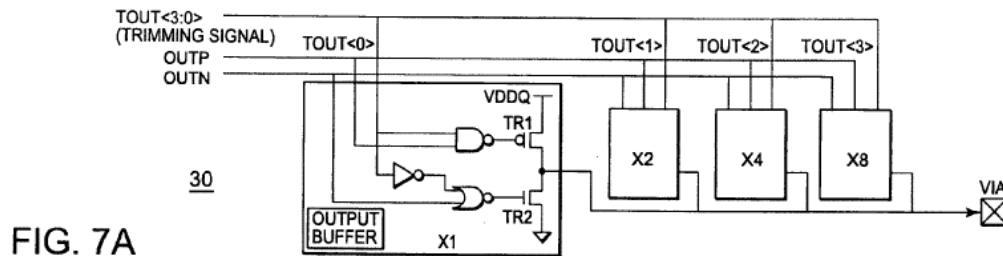


FIG. 5

A Skilled Artisan would have understood that such chip-to-chip interfaces include “C/A conduits” to conduct respective command and address signals and separate “data conduits” to conduct respective data signals. *See, e.g.*, EX1048 (Shaeffer) at Fig. 1A (Interface 118 including lines for C/A signals 114 separate from lines for data signals 120 and 128), Figs. 4A and 4B (showing CA signals and DQ (data) signals being transmitted at the same time). A Skilled Artisan would have also understood that such “conduits” would include drivers in order to drive the signals from one die to another. *See, e.g.*, EX1018 (Riho2) at ¶[0097] (“FIG. 7A shows a

circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30”) and Fig. 7A (reproduced below).



224. Accordingly, the prior art references in each of Grounds 3 and 4 teach “the control die including conduits, the conduits including C/A conduits and data conduits.”

5. [1.j] First/Second Conduits

225. Claim 1 requires “wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.”

226. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

227. For the reasons discussed above with reference to claim element [1.e.2], *supra* ¶¶220-224, and as [1.e.4] requires, the Keeth-Shaeffer combination discloses “a first conduit of the first data conduits is coupled ...[to] the first data interconnect” and “a second conduit of the second data conduits is coupled ...[to]

the second data interconnect” in order to conduct data signals between the control die and the memory devices. For the reasons discussed above with reference to claim elements [1.c.1], *supra* ¶¶211-214, and [1.e.1], *supra* ¶¶215-219, the combination also discloses “*a first data terminal of the data terminals*” to receive or output data signals according to commands from a processor. For example, Keeth discloses that “[i]nterface die 210 may include additional circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates between the apparatus 200 and another device, such as processors or a memory controller in communication with the stack 202 by way of the interface die 210.” EX1047 (Keeth) at 3:62-67. Keeth further discloses that “[p]artitions vertically aligned across multiple dice in the stack, together with the corresponding control circuit and electrical connections may constitute a “vault”... [and t]he partitions of a vault may share ... input/output data pins.” EX1047 (Keeth) at 1:65-2:10. Keeth further explains that “a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth.” *Id.* at 4:4-16. Similarly, Keeth discloses that “[b]y interleaving the conductive paths in the dice stack 502, the interface die 510 may access each die (or a partition of each die) independently of the die above or below, and the interface die 510 may concurrently access dice 520 through 523, thereby increasing bandwidth.” *Id.* at 5:63-67. A Skilled

Artisan would have understood from Keeth's disclosure that the bandwidth is improved by "access[ing] each die (or a partition of each die) independently" and "concurrently communicat[ing] with (e.g., access and send data to) multiple partitions," e.g., on a "*first data interconnect*" to an odd partition and on a "*second data interconnect*" to an even partition. *Id.* When these odd and even partitions can "share ... input/output data pins" as taught by Keeth, *id.* at 1:65-2:10, a Skilled Artisan would have understood, and been motivated, to couple both of the "*first data conduit ... coupled ...[to] the first data interconnect*" and the "*second conduit ... coupled ...[to] the second data interconnect*" to the same "*first data terminal*" in order to "improve bandwidth."

228. A Skilled Artisan would have understood from Keeth's disclosure that its memory stack can be "used in high-speed computers" and allows "access[ing] each die (or a partition of each die) independently" and "concurrently" "thereby improv[ing] bandwidth," and that these advantageous features can be implemented by coupling the "*first conduit*" and "*second conduit*" between the same "*first data terminal*" and the respective "*first data interconnect*" and "*second data interconnect*" in order to communicate data with a processor at the "appropriate data transfer rates" that are required in high-speed computers. EX1047 (Keeth) at 9:65-67, 4:4-16, 5:63-67, and 3:62-67 ("Interface die 210 may include additional circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information

at appropriate data transfer rates between the apparatus 200 and another device, such as processors or a memory controller in communication with the stack 202 by way of the interface die 210.”). Indeed, a Skilled Artisan would have also understood that such “appropriate data transfer rates” with a processor can be higher than the rate at which the communication paths operate inside the stack, thus the interface chip includes circuitry for data rate transformation. EX1056 (Loi Paper) at Abstract (“Historically, processor performance has increased at a much faster rate than that of main memory ... 3D integration based on TSV technology may provide a solution, as it enables ... orders-of-magnitude increase in memory interface bandwidth, speed and energy efficiency.”) and p.1 (“Note that stacked DRAM memory is still accessed using standard DRAM interfacing protocols. Hence protocol translation between processor memory accesses and DRAM transactions is still needed.”). Therefore, Keeth’s bandwidth is improved because the higher data rate with a processor on the “*first data terminal*” is accommodated by “independently” and “concurrently” using two lower-rate communication paths (“*first data interconnect*” and “*second data interconnect*”) with two partitions of a memory vault of Keeth.

229. Furthermore, as discussed above, a Skilled Artisan would have also understood that operating the communication paths inside the stack at a rate that is lower than the “appropriate data transfer rates” with an external processor in high-

speed computers advantageously results in lower power consumption and increased yield, as taught by Riho2. *Supra*, ¶¶198-202; *see also* EX1018 (Riho2) at [0008], [0052], [0148]. A Skilled Artisan would have understood from Keeth's disclosure alone or in view of the teaching of Riho2 that its interface die can include parallel-to-serial and serial-to-parallel conversion circuitry to achieve higher, "appropriate data transfer rates" with a processor while operating the memory dies at a lower data rate. *Supra*, ¶¶198-202; *see also* EX1047 at 3:62-67; EX1018 (Riho2) at ¶[0053]. Therefore, a Skilled Artisan would have been motivated to achieve higher data rate with a processor on the "*first data terminal*" by coupling it, through rate conversion circuitry, to a "*first conduit*" and "*second conduit*" for data signals, and independently and concurrently using respectively coupled communication paths ("*first data interconnect*" and "*second data interconnect*") at a lower rate inside the stack in order to save power.

230. Accordingly, the prior art references in each of Grounds 3 and 4 teach "*wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.*"

6. [1.k] Control Logic

a) [1.k.1] Control Logic

231. Claim 1 requires “*wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals.*”

232. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

233. As discussed above with reference to claim element [1.c.1], *supra* ¶¶211-214, the combination discloses “*command and/or address (C/A) terminals ... to receive C/A signals.*” Keeth further discloses that “[e]ach die 220 through 223 may comprise a plurality of memory partitions 204 and interface die 210 may comprise control circuits 212 to enable communication and control with the corresponding memory partition 204 stacked above the respective control circuit via communicative paths 208.” *Id.* at 3:44-54. Keeth further explains that “a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth.” *Id.*, 4:4-16. A Skilled Artisan would have understood from Keeth’s disclosure that the vault control circuit includes “*logic*” to control the states of “*the first and second conduits*” to “communicate with (e.g., access and send data to) multiple partitions

in the vault” *“in response to one or more C/A signals.”* For example, the state of each of the “conduits” in the “control die” can be a receiving state for accessing read data from a partition in response to a read command and a transmitting state for sending data to a partition in response to a write command.

234. Accordingly, the prior art references in each of Grounds 3 and 4 teach *“wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals.”*

b) [1.k.2] No Chip Select Signal

235. Claim 1 requires *“wherein the one or more C/A signals [for 1.k.1] do not include any chip select signal.”*

236. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

237. As discussed above with reference to claim element [1.k.1], *supra* ¶¶231-234, *“the first and second conduits”* are controlled *“in response to one or more C/A signals”* to communicate data with selected one or more dies in the stack. As also discussed above with reference to claim element [1.j], *supra* ¶¶225-230, *“the first and second conduits”* are coupled to the same *“first data terminal,”* essentially in a “fork-in-the-road” arrangement. It follows that *“the first and second conduits”* need to be controlled selectively in a way that there is no conflict

of the data transfers through the common “*first data terminal*.” The ’087 patent discloses that this selection is based on chip select signals. EX1001 at 15:31-16:25 (“This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal.”).

238. Based on its infringement contentions, Netlist’s interpretation of “*chip select signal*” does not include a so-called stack ID (“SID”) which is used to identify the target die in the stack. EX1089, 70-71 (Netlist infringement contentions); EX1083 (Netlist complaint) at p.13 n.1 (JESD 238A Command Truth Table including SID) and p.16 ¶34 (Netlist arguing that JESD 238A Command Truth Table does not include “chip select signal”); EX1084 at p.13 n.1, p.15 ¶34 (same); EX1087 at p.13 n.1, p.16 ¶34 (same); EX1088 at p.13 n.1, p.15 ¶34.

239. If Netlist’s apparent construction of “chip select signal” is used, Keeth also discloses that the target die of a read or write operation can be identified using “ID information.” EX1047 (Keeth) at 3:5-8 (“The conductive paths 106 may communicate (e.g., transfer) information such as data, address, control, ID information, among other information.”). Keeth further explains that the control die can use the “ID information” to reference individual dies in the stack. *Id.* at 3:21-38 (“The control circuit 130 may operate to retain the assigned ID information after the initialization of stack 102, such as in order for control circuit 130 to reference each die 120 through 123 by the ID information.”).

Accordingly, a Skilled Artisan would have understood that the “ID information” of Keeth along with command and address signals of read and write operations can be used to control “*the first and second conduits*” to receive or transmit data from and to specific dies without any additional “*chip select signal*.”

240. Alternatively, the combination of Keeth and Shaeffer also renders obvious this limitation independent of the construction of “*chip select signal*.” Shaeffer discloses different options for a protocol to transfer data between a memory die and the control die. EX1048 (Shaeffer) at Figs. 2-4B. For example, Shaeffer discloses “a timing preamble that precedes a data burst received by the controller via the data signaling resources.” *Id.* at 2:3-6. Shaeffer also discloses that, “in TRS mode, the TRS signal burst would be shifted to commence before the corresponding read data burst commences.” *Id.* at 10:3-19. A Skilled Artisan would have understood from Shaeffer’s disclosure that the state of each of “*the first and second conduits*” to receive or not (and to transmit or not) data through the “*first data interconnect*” or the “*second data interconnect*” in Keeth’s device can be controlled in response to command signals specifying read or write operations and using Shaeffer’s preamble or TRS signals without “*any chip select signal*.”

241. For example, in case of read operations, a Skilled Artisan would be motivated to select the state of each of “*the first and second conduits*” based on the

“timing preamble” or the “TRS signal burst,” because Shaeffer teaches that these signals are received before the actual data and provide timing for correctly capturing the data values. EX1048 (Shaeffer) at 2:36-44 (“...the controller will receive the TRS before receiving a first bit of the subsequent data. The controller, upon receipt of the TRS, can use the TRS for the sampling of the data...[and] to optimize a sampling point for the data at the input sampler of the controller device.”). Thus, the controller can know from the timing preamble or the TRS signal, which of the “*first data interconnect*” and the “*second data interconnect*” would conduct the read data, and can prevent data contentions.

242. For write operations, a Skilled Artisan would have understood that the data can be transmitted through both of “*the first and second conduits*,” and “each partition may have a different chip select line” to select the memory die acting upon the data. EX1047 (Keeth) at 2:6-10. That is, the chip select signals are used by the memory dies for selecting the target of a write operation, not to control the state of “*the first and second conduits*.” A Skilled Artisan would have been motivated to transmit the write data through both “*conduits*” because it allows faster operation. EX1026 (Ellsberry) at ¶[0033] (“In column mode operation, to meet system timing requirements, write data is sent to both ports ...”).

243. In sum, a Skilled Artisan would have been motivated to transmit write data on both of “*the first and second conduits*” for faster operation and to use the

existing “timing preamble” or the “TRS signal burst” of Shaeffer to avoid read data conflicts. Accordingly, the combination of Keeth and Shaeffer also renders obvious that “*the one or more C/A signals do not include any chip select signal.*”

244. Accordingly, the prior art references in each of Grounds 3 and 4 teach “*wherein the one or more C/A signals do not include any chip select signal.*”

7. [1.] First Unidirectional Interconnects

245. Claim 1 requires “*wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies.*”

246. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

247. The combination of Keeth and Shaeffer discloses that “*the die interconnects further include first unidirectional interconnects [(e.g., implementing the functionality of Shaeffer’s lines 130 in the combination)] configured to conduct [TRS/EDC] signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies.*” EX1048 (Shaeffer) at Figs. 1A and 4B (reproduced below).

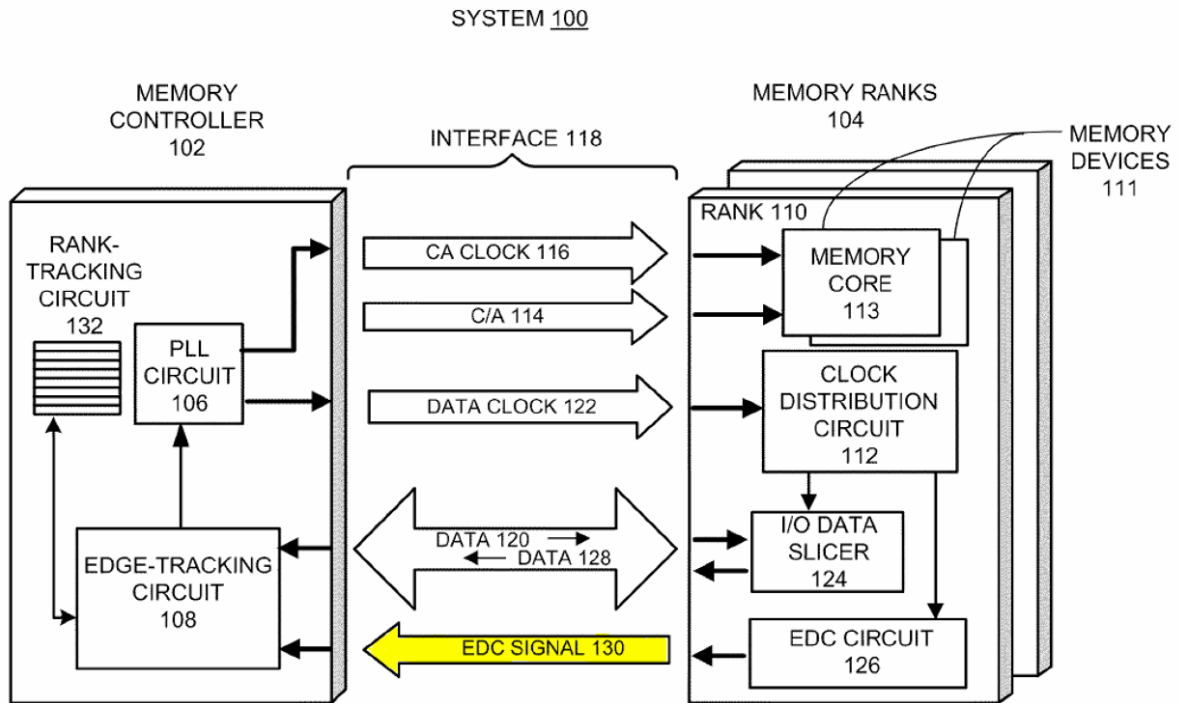


FIG. 1A

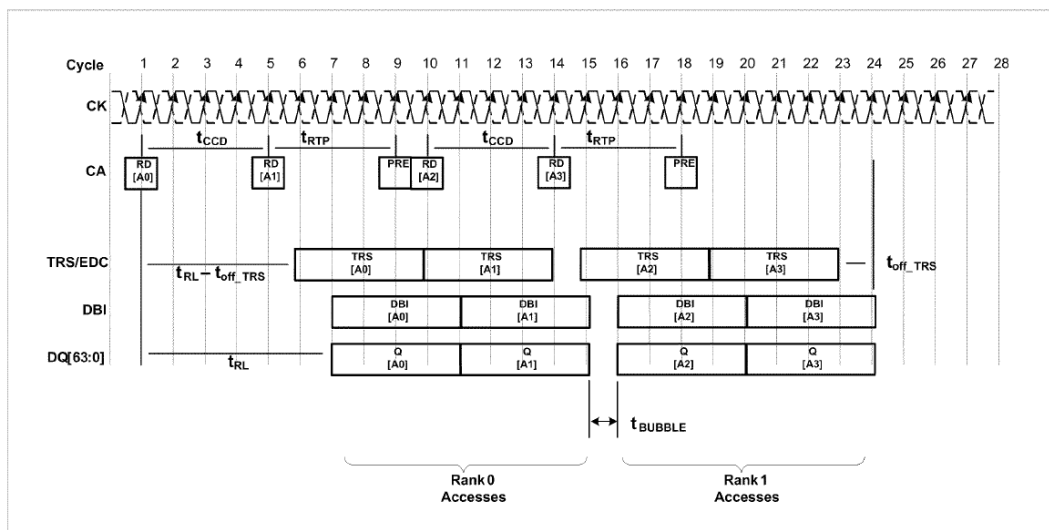


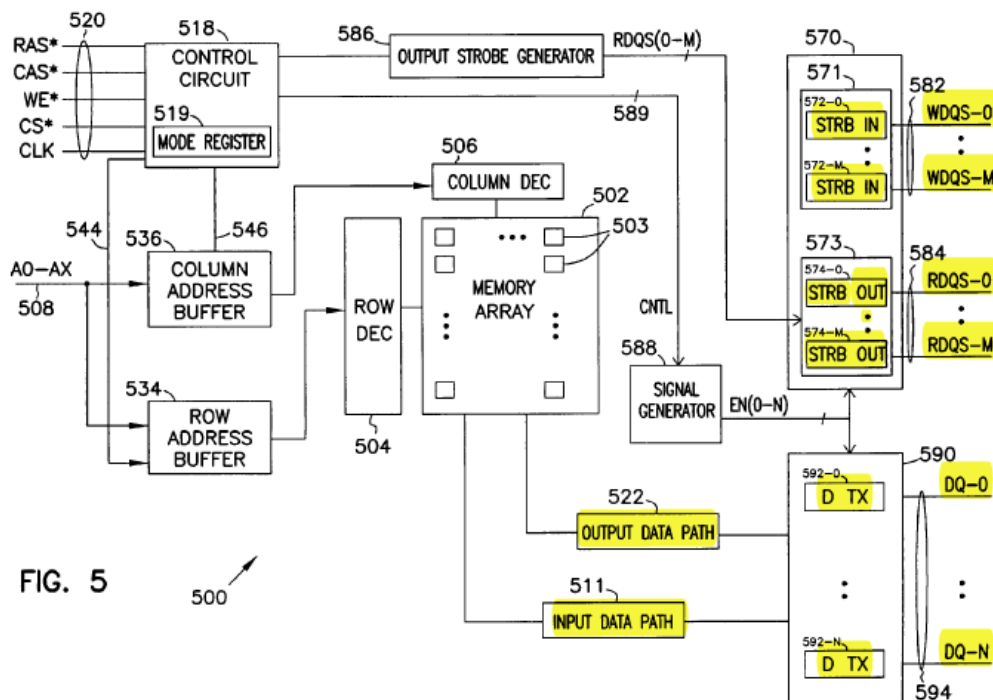
FIG. 4B

248. As discussed above, it would have been obvious to a Skilled Artisan to implement Shaeffer's signaling protocol, including its TRS/EDC signaling, in

Keeth's memory stack using its interleaving die interconnects between the interface die and the memory dice, e.g., in order to achieve independent control and increase bandwidth. *Supra*, ¶¶185-189. The lines 130 conduct the TRS/EDC signals in one direction, from the memory devices to the control (interface) die. EX1048 (Shaeffer) at 3:39-51 ("a transmitter circuit to transmit an EDC signal 130 back to memory controller 102"), 2:64-3:4 ("The TRS, in an embodiment, is conveyed from the memory device, to the memory controller via a signaling resource (i.e., signal traces, pins etc.,) that is also used to transfer error detection and correction information (EDC)."), 9:10-31 ("For example, during a read operation, the TRS signal is transmitted by a memory device over a first signal line and is to be received by the memory controller before the read data is received (over separate signal lines) so that the memory controller can adjust its timing alignment to properly receive the read data."). Thus, the combination *"include[s] first unidirectional interconnects [(for lines 130)] configured to conduct [TRS/EDC] signals from one or more DRAM dies of the stacked DRAM dies to the control die."*

249. Shaeffer discloses that the signal lines 130 conduct TRS/EDC signals from the memory die to the control die, but has no disclosure that the signal lines 130 are *"configured to conduct any signal from the control die to any of the stacked DRAM dies,"* thereby rendering obvious to use *"unidirectional*

interconnects.” EX1048 (Shaeffer) (in general). Furthermore, Shaeffer expressly discloses that the communication between the control die and the memory die can be “uni-directional.” *Id.* at 11:54-57 (“links 514 may be used for bi-directional and/or uni-directional communication between the memory controller 510 and one or more of the memory devices 512”). A Skilled Artisan would have also understood that unidirectional data timing signal lines, similar to lines 130 transmitting TRS signals, were well known at the time, for example, to time data transactions from memory devices. EX1051 (Schnarr) at Fig. 5 (reproduced below showing circuits STRB OUT 574-0 to 574-M for transmitting read strobe signals RDQS-0 to RDQS-M).



Thus, a Skilled Artisan would have understood from Shaeffer's disclosure that the signal lines 130, which are disclosed to transmit signals, such as TRS timing signals, only from the memory dies to the control die, are used for unidirectional communication. In the absence of a signal to be transmitted in the opposite direction, it would have been obvious that the signal lines 130 are “*not configured to conduct any signal from the control die to any of the stacked DRAM dies.*”

250. Accordingly, the prior art references in each of Grounds 3 and 4 teach “*wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies.*”

8. [1.m] Second Unidirectional Interconnects

251. Claim 1 requires “*wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die.*”

252. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

253. Shaeffer discloses that the signal lines 122 for data clock/strobe signals are transmitted from the control die to the memory dies, and has no

disclosure that the lines 122 are “*configured [to] conduct any signal from any of the stacked DRAM dies to the control die.*” EX1048 (Shaeffer) (in general).

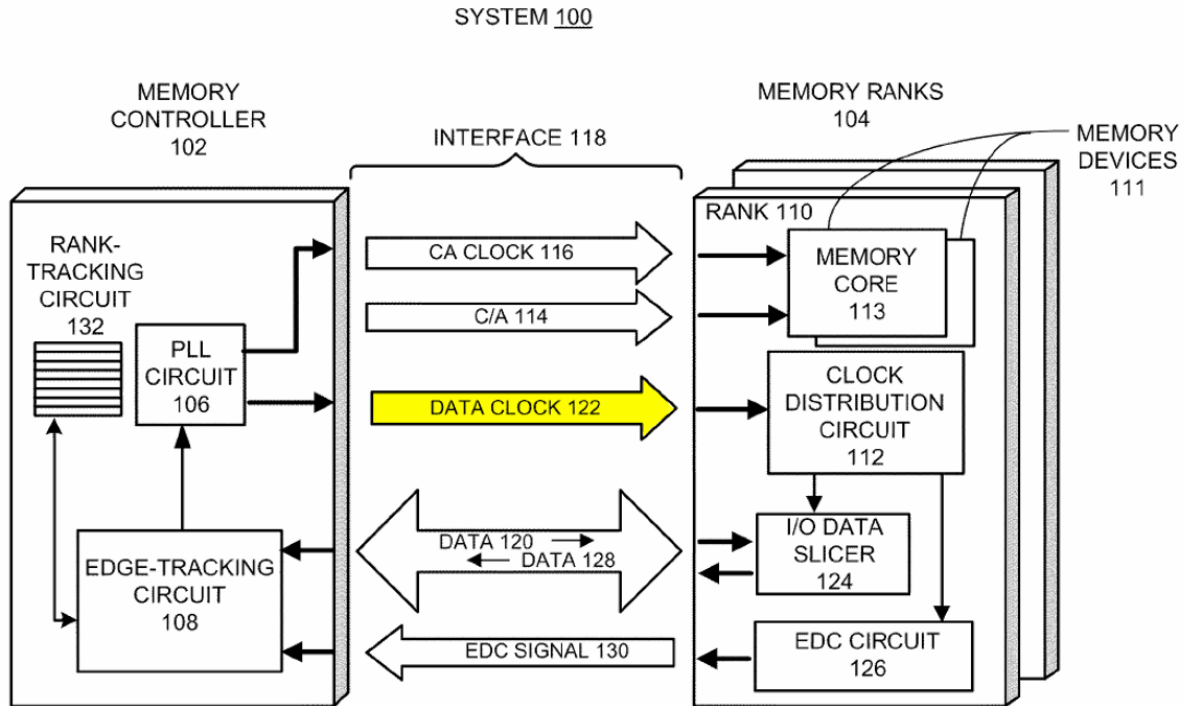


FIG. 1A

Shaeffer expressly discloses that the communication between the control die and the memory die can be “uni-directional.” *Id.* at 11:54-57 (“links 514 may be used for bi-directional and/or uni-directional communication between the memory controller 510 and one or more of the memory devices 512”). A Skilled Artisan would have understood that unidirectional strobe signals for write operations, similar to the write strobes of Shaeffer, were well known at the time. EX1051 (Schnarr) at Fig. 5 (reproduced above, showing unidirectional WDQS lines

coupled to STRB IN receiving circuits in the memory device). Thus, a Skilled Artisan would have understood from Shaeffer's disclosure that the signal lines 122, which are disclosed to transmit signals only from the controller to the memory dies, are used for unidirectional communication, and are *“not configured conduct any signal from any of the stacked DRAM dies to the control die.”*

254. Accordingly, the prior art references in each of Grounds 3 and 4 teach *“wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die.”*

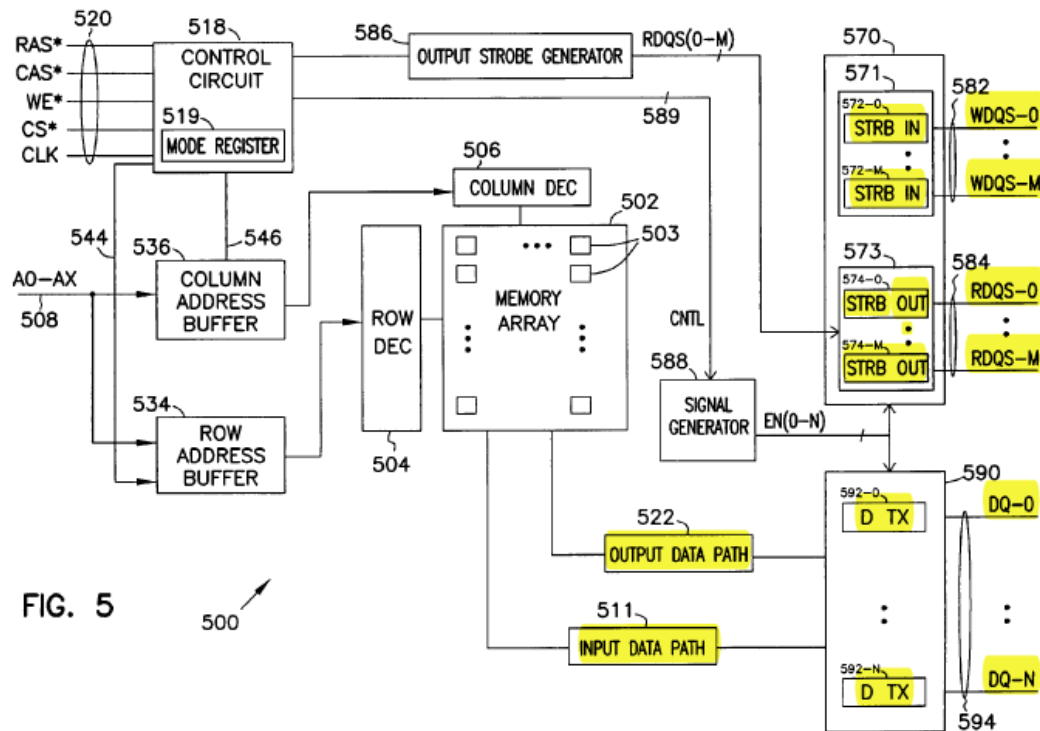
9. [1.p.2] Second Signals

255. Claim 1 requires *“in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.”*

256. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

257. A Skilled Artisan would have understood that the strobe signal 122 for write data is transmitted *“in response to the second set of C/A signals [for a write operation]”* to a memory device in order to “clock” the write data into the memory device, i.e., to indicate to the memory device when to sample the write

data signal. *Id.* at 3:35-39 (“write data 120 is directly clocked on rank 110 by data clock 122”) and 9:1-9 (“a strobe signal (that is aperiodic in the sense that it indicates when to sample data)”). A Skilled Artisan would have understood that such a write strobe signal was well known at the time. EX1051 (Schnarr) at Fig. 5 (reproduced below), 9:19-27 (“The write strobe signals (bits) WDQS-0 through WDQS-M on lines or strobe terminals 582 represent the timing information of the input data. An external source provides the WDQS-0 through WDQS-M signals together with the input data to memory device 500.”).



258. Accordingly, the prior art references in each of Grounds 3 and 4 teach “in response to the second set of C/A signals, drive second signals associated with

the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.”

10. [4.a] first/second driver

259. Claim 4 requires “[t]he DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size.”

260. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

261. The combination of Keeth and Shaeffer alone or in view of Riho2, renders obvious that “*the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size.*” As discussed above with reference to claim elements [1.e.2], *supra* ¶¶220-224, and [1.j], *supra* ¶¶225-230, and as [1.e.4] requires, the combination of Keeth and Shaeffer discloses “*the first conduit*” and “*the second conduit*” in a vault control circuit to transmit data to different partitions of Keeth’s memory devices. See, e.g., EX1047 (Keeth) at Fig. 2 (reproduced below).

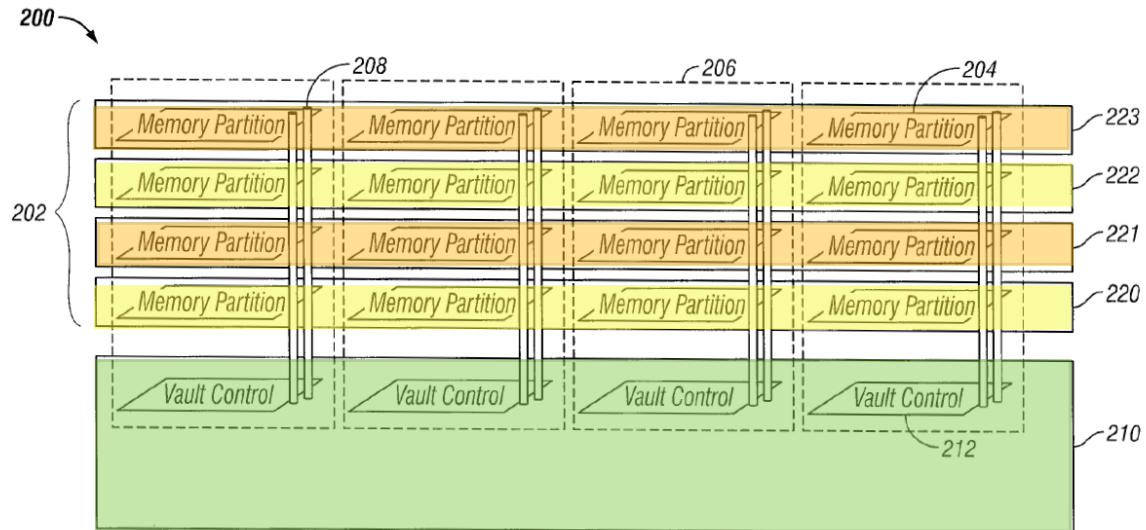


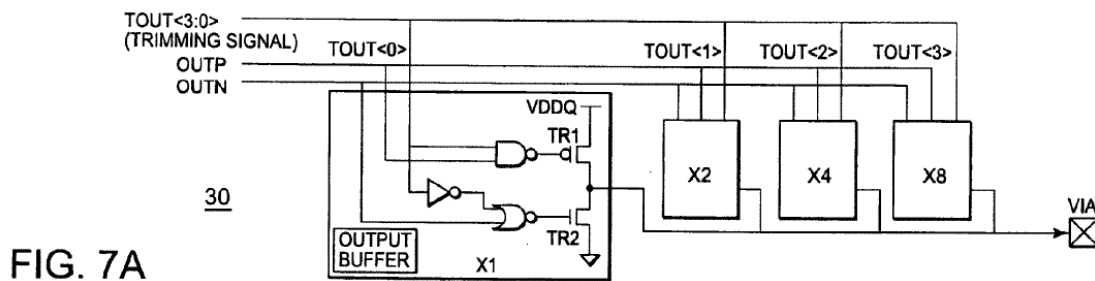
FIG. 2

262. For example, Keeth discloses that, “[b]y interleaving the connections, a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault.” *Id.* at 4:4-16, *see also* 6:9-19 (“Alternating dice in the stack 502 may be part of separate vaults. ... In the example, this construction allows the interface die 510 to concurrently access the first and second vaults and concurrently drive data to partitions within the vaults.”). A Skilled Artisan would have understood from Keeth’s disclosure of “concurrently ... send[ing] data to” and “concurrently driv[ing] data to partitions” by “*the first conduit*” and “*the second conduit*,” that these “*conduits*” include a respective “*first driver*” and “*second driver*,” because different data is stored in different partitions, and separate drivers are needed to drive different data signals concurrently.

263. A Skilled Artisan would have also understood that “*a first driver [is] configured to have a first driver size and ... a second driver [is] configured to have a second driver size,*” each driver size corresponding to the load (caused by capacitance and resistance) that has to be driven. *See, e.g.,* EX1030 (Brown) at 135-36 (“... to drive a large capacitive load, buffers are often used to improve performance.... Buffers can be created with different amounts of *drive capability*, depending on the sizes of the transistors In addition to their use for improving the speed performance of circuits, buffers are also used when high current flow is needed to drive external devices.... In general, fan-out, capacitive loading, and current flow are important issues that the designer of a digital circuit must consider carefully.”) (emphasis in original).

264. Furthermore, for the reasons discussed above, it would have been obvious to implement the driver-size optimization teaching of Riho2 in the combination of Keeth and Shaeffer, including using a driver whose size is optimized for the load to be driven. *Supra*, ¶¶190-202; EX1018 (Riho2) at Fig. 7A (reproduced below) and ¶[0097] (“FIG. 7A shows a circuit configuration for optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance. In the example shown here, there are provided four output buffers X1, X2, X4, and X8 having mutually different drive capacities

(the numerical values following the letter “X” indicate capacity ratios). Each of the output buffers X1 to X4 are formed by an inverter, and NAND, NOR, and CMOS transistors. They have the same circuit configuration, but their transistors are of mutually different sizes.”).



265. Accordingly, the prior art references in each of Grounds 3 and 4 teach “[t]he DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size.”

11. [4.b] first/second driver size

266. Claim 4 requires “the second driver size is different from the first driver size.”

267. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

268. The combination of Keeth and Shaeffer alone or in view of Riho2, renders obvious that “the second driver size is different from the first driver size.” My opinion is the same regardless of whether “driver size” refers to physical size,

or to strength, *see supra* ¶93, because the prior art renders obvious using a larger physical size to achieve greater driver strength. EX1030, 135-36 (“different amounts of *drive capability*” depending “the sizes of the transistors”); *see also* EX1072, 64-67.

269. For example, Keeth discloses that “conductive paths 704, 705, 706, 707, and 708 of the first dice stack 702 include joints 709 and TSVs 712, at least some of which extend entirely through the dice stack 702 and some of which connect with circuitry.” *Id.* at 7:37-45. Keeth further explains that the conductive paths “may entirely pass through or partially pass through the dice stack.” *Id.* 5:34-38.

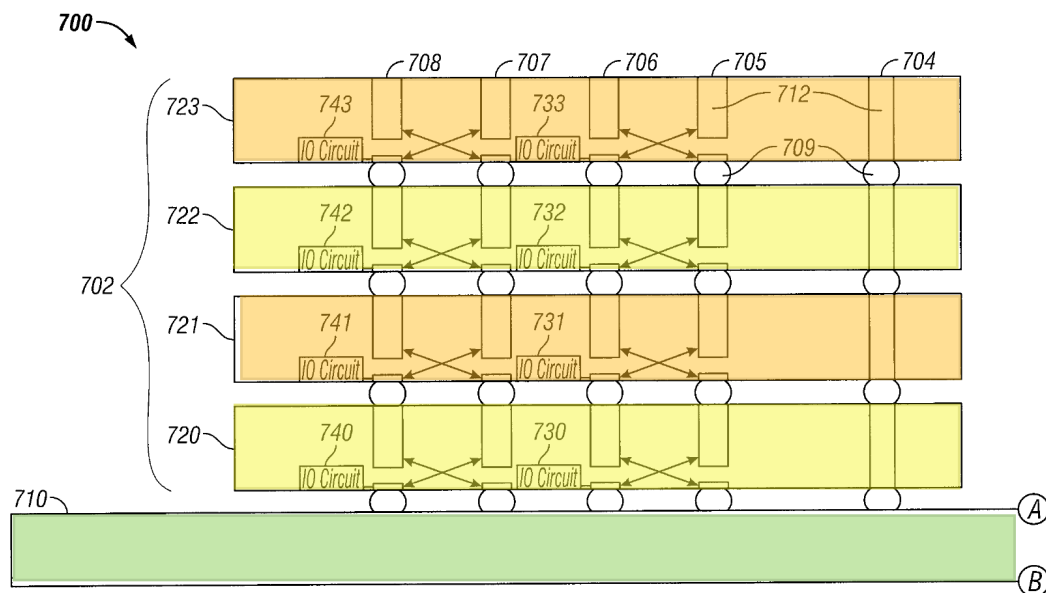


FIG. 7

270. A Skilled Artisan would have understood from Keeth’s disclosure that, as an example, the conductive path 706, starting from the control die 710, can

end in die 722 without passing through dies 722 and 723, and does not require a TSV in, nor a joint between, dies 722 and 723, because the last I/O circuit the conductive path 706 is connected to is I/O circuit 732 in die 722. *Id.* at Fig. 7. In contrast, conductive path 705 has to pass through die 722, since it is coupled to I/O circuit 733 in die 723 above. Thus, in implementations where some of Keeth's conductive paths only “partially pass through” the stack, different conductive paths may have different length. Accordingly, a Skilled Artisan would have understood that the load and the corresponding time constant of the conductive paths would be different depending on their length, e.g., because they “extend entirely through” or “partially pass through” the stack.

271. A Skilled Artisan would have also understood and been motivated to use a “*second driver size*” for Keeth's conductive paths that “extend entirely through” the stack “*that is different from the first size*” of those that “partially pass through” the stack in order to save power and to minimize the difference between their time constants, thus provide more reliable high-frequency operation, as it was commonly known at the time. EX1017 (Wyman) at 1:22-24 (“In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required.”); EX1072, 64-67; EX1030, 135-36 (“different amounts of *drive capability*” depending “the sizes of the transistors”); EX1018 (Riho2) at ¶¶[0010-11] (“These problems are attributable

to the fac[t] that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips. The present invention seeks to solve one or more of the above problems, or to improve upon those problems at least in part.”).

272. Furthermore, it would have been obvious to implement Riho2’s teaching about “optimizing the output drive capacity of output buffers” in the combination of Keeth and Shaeffer. *Supra*, ¶¶190-202; EX1018 (Riho2) at [0097]. For example, Riho2 teaches driver optimization in accordance with “a change in the time constant caused by parasitic capacitance and parasitic resistance.” *Id.* A Skilled Artisan would have understood that such variations in the time constant are also present in the combination of Keeth and Shaeffer. *Supra*, ¶¶194-196. For example, Keeth teaches conductive paths of different lengths causing different time constants, and a Skilled Artisan would have understood that further variations in the time constant are caused by differing positions in the stack, and by manufacturing variations of the TSVs, joints, and the coupled circuits. *Id.* Accordingly, she would have been motivated to implement the driver-size optimization techniques of Riho2 in the combination of Keeth and Shaeffer in order to avoid timing variations (which may lead to synchronization issues) and

ensure stable operation, in particular when the DRAM chips are operating at a high frequency. *Id.* ¶¶197-198. A Skilled Artisan would have also understood that the driver-size optimization techniques of Riho2 can save power, further motivating their use in the combination of Keeth and Shaeffer. *See, e.g.*, EX1017 (Wyman) at 1:22-24.

273. Accordingly, a Skilled Artisan would have understood that, due to these variations of capacitance and resistance, the load on the “*first data interconnect*” may be different from the load on the “*second data interconnect*” in the Keeth-Shaeffer combination, and she would have been motivated to use the teaching of Riho2 to optimize the driving capabilities of the respective “*first driver*” and “*second driver*” according to the load differences, resulting in “*the second driver size ...[being] different from the first driver size.*” *Supra*, ¶¶190-202; EX1018 (Riho2) [0097] (“mutually different drive capacities....transistors are of mutually different sizes”).

274. Accordingly, the prior art references in each of Grounds 3 and 4 teach “*the second driver size is different from the first driver size.*”

12. Claim 5

275. Claim 5 is unpatentable as the prior art references in each of Grounds 3 and 4 render the claim obvious.

276. Claim 5 requires “[t]he DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.”

277. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

278. As discussed above with reference to claim element [1.c.1], *supra* ¶¶211-214, DRAM packages with 32 data pins were well-known at the time. *See, e.g.*, EX1022 (Jacob) at 348 (“Increase DRAM Data Width ... the number of data pins has increased from x1 parts in the late 1980s to x32 parts”); EX1081 (data sheet for Mobile Low-Power DDR SDRAMs, including x32 devices); EX1040 (data sheet for x32 GDDR5 SGRAM). In fact, 32-bit wide memories were already standardized at the time. EX1035 (JESD21-C 3.11.5.8) at p.3 (standardized x32 GDDR4 memories). Thus, in order to be compatible with the data width of x32 memory packages used at the time, a Skilled Artisan would have been motivated for the DRAM package of the Keeth-Shaeffer combination to have 32 data terminals which can communicate 32 data signals in parallel. Accordingly, it would have been obvious for “*the first data signals include 32 or 64 signals ... subsequently output by the DRAM package in parallel* [in response to a read

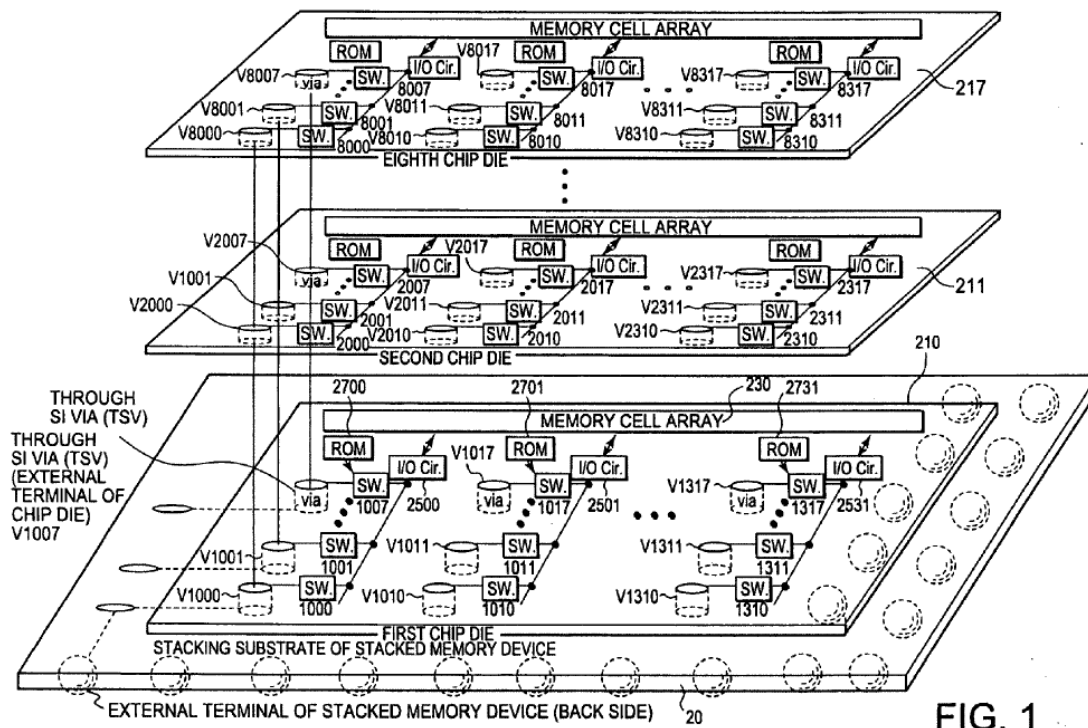
command], *and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel ... [during a write operation].*”

279. Furthermore, Keeth discloses that the “number of conductive paths ... may vary” and is not limited to its specific examples. EX1047 (Keeth) at 3:18-20; *see also id.*, 10:59-65 (“Various other configurations may include ... a fewer or greater number of interleaving conductive paths connecting various circuitry of dice with the circuitry of the interface die and passing through other dice to permit concurrent communication with dice in the stack.”). A Skilled Artisan would have understood from Keeth’s disclosure that the number of conductive paths for conducting data is a design choice. In particular, each die in a stack having 32 data lines coupled to it was a well-known design at the time. *See, e.g.*, EX1016 (Riho) at Fig. 2 (showing x32 data connection between a logic chip and each of the stacked SDRAMs) and [0033] (“Each SDRAM ... outputs a 32-bit data signal in parallel.”).

280. A Skilled Artisan would have also understood that having as many data interconnects between the vault control circuit and one of Keeth’s partitions as the number of the corresponding data terminals would advantageously simplify the interface circuitry. For a read operation, the number of data bits received in parallel from a memory partition are readily available to be output through the same number of data terminals in parallel without any re-grouping of those data

bits, thus maintaining high speed. For write operation, the number of data bits received in parallel on a number of data terminals are readily available to be transmitted through the same number of TSVs in parallel to a memory partition without any re-grouping of those data bits, thus maintaining high speed. Thus, a Skilled Artisan would have been motivated to match the standard number of 32 data terminals of the package by having 32 data interconnects coupled to one memory partition to conduct 32 data signals in parallel between the memory partition and the data terminals.

281. Alternatively, it would have been obvious to combine Keeth and Shaeffer with Riho2. *Supra*, ¶¶190-202. Riho2 also discloses 32-bit wide parallel data paths. EX1018 (Riho2), [0045]-[0047] (“32-bit”), Fig. 1 (reproduced below, showing 8 x32 TSVs for communicating data with 8 memory dies 210-217).



282. Accordingly, the prior art references in each of Grounds 3 and 4 teach
“[t]he DRAM package of claim 1, wherein the first data signals include 32 or 64
signals conducted via the first data interconnects in parallel and subsequently
output by the DRAM package in parallel, and wherein the second data signals
include 32 or 64 signals received by the DRAM package in parallel and
subsequently conducted via the first data interconnects in parallel.”

13. [6.a] First Set of C/A Signals Including a Chip Select Signal

283. Claim 6 requires “[t]he DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals.”

284. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

285. Keeth discloses that a DRAM die which is the target of a memory operation can be selected by “ID information.” *See, e.g.*, EX1047 (Keeth) at 3:5-8 (“The conductive paths 106 may communicate (e.g., transfer) information such as data, address, control, ID information, among other information.”). Keeth further explains that the control die can store and use the “ID information” to reference individual dies in the stack. *Id.* at 3:21-38 (“The control circuit 130 may operate to retain the assigned ID information after the initialization of stack 102, such as in order for control circuit 130 to reference each die 120 through 123 by the ID information.”). Keeth also discloses that, in other implementations, “each partition may have a different chip select line to prevent data contention.” *Id.* 2:6-10. Chip select signals were well known and commonly used to select a memory device to respond to a read or write command. EX1019 (JESD79-3C) at p.13 (“Chip Select: All commands are masked when CS# is registered HIGH”), pp.33-34 & n.1 (“All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock”), p.36 (“DESELECT...CS# HIGH”); EX1023, pp.2-3 (“chip-select”); EX1022, p.413 Fig.10.5. Therefore, Keeth discloses “*one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals*” in response to a read command.

286. Keeth also discloses that its stack “may be communicatively coupled with external devices, e.g., processors and memory controllers, through the interface die.” EX1047 (Keeth) at 3:9-20. A Skilled Artisan would have understood from the disclosure of Keeth that its “ID information” or chip select signals that are used to select the target die can be received as part of a “set of C/A signals” for a read or write command from the “processor” or “memory controller,” as it was usual at the time. *See, e.g.*, EX1019 (JESD79-3C) at p.12 (Figs. 1-3 showing a stack of 4 dies receiving four separate chip select signals CS0, CS1, CS2, and CS3). A Skilled Artisan would have been motivated to use such a direct control from the processor or memory controller for the target-die selection because it simplifies the circuitry on the interface die and allows for faster operation, because the interface die does not have to generate the “ID information” or chip select signals from other information (such as address signals). Indeed, such a direct die selection from the processor or memory controller has been proposed during JEDEC meetings. EX1082 (Proposed 3D Stacked DDR3 SDRAM Addressing) at p.3 (“Each logical rank may be implemented as a single die”) and p.4 (Figs. 1-3 showing CS0# to CS3# and CID signals from external controller to select the target rank).

287. Accordingly, the prior art references in each of Grounds 3 and 4 teach “[t]he DRAM package of claim 1, wherein: the first set of C/A signals include one

or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals.”

14. [6.c] No Emulation Logic

288. Claim 6 requires “*wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.*”

289. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

290. For example, as discussed for [6.a], *supra* ¶¶283-287, it would have been obvious to allow direct control by the external controller to select the target of memory read and write operations, because it obviates the need for emulation logic in the interface die, thereby simplifying its circuitry and operation. Furthermore, neither Keeth nor Shaeffer discloses the claimed “*emulation logic.*” See generally EX1047, EX1048. It was well known at the time that emulating a larger capacity DRAM is not required even when the interface emulates other characteristics, such as timing, signal type or number, or aspects of a protocol. EX1015 (Rajan) at 3:38-43 (“An example of an emulated electrical characteristic might be a signal, or a voltage level. An example of an emulated physical characteristic might be a number of pins or wires, a number of signals, or a memory capacity. An example

of an emulated protocol characteristic might be a timing, or a specific protocol such as DDR3.”).

291. Accordingly, the prior art references in each of Grounds 3 and 4 teach “*wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.*”

15. Claim 7

292. Claim 7 is unpatentable as the prior art references in each of Grounds 3 and 4 render the claim obvious.

293. Claim 7 requires “[t]he DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.”

294. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

295. For example, Keeth expressly teaches “prevent[ing] data contention.” EX1047 at 2:6-10 (“each partition may have a different chip select line to prevent data contention”). A Skilled Artisan would have understood that “data contention” is one type of “*signal collisions.*” EX1038 (Stone) at 89-90 (“If module A spews

forth a logic 0 while module B attempts to transmit a logic 1 at the same instant of time, we say there is a *bus conflict*.”) (emphasis in original). A Skilled Artisan also understood the disastrous effects of such collisions. *Id.* (“conflicts almost certainly result in a communication failure ... [and] can be more disastrous ... [as] there is a possibility of damaging the bus drivers ...”). Thus, a Skilled Artisan would have understood from the disclosure of Keeth the importance, and the need, to “*prevent signal collisions*” in the combination of Keeth and Shaeffer.

296. A Skilled Artisan also understood from the teaching of Keeth and Shaeffer how “*to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.*” For example, Shaeffer expressly discloses using timing parameters like t_{CCD} and t_{RTP} for “*timing of command/address signals [like RD [A0], RD [A1], PRE, RD [A3], WR [A1] WR [A2]] driven to the stacked DRAM dies,*” and timing parameters like t_{RL} and t_{off_EDC} for “*timing of data signals [on data lines DQ[63:0] communicated between the stacked DRAM dies and the data terminals*” in order “*to prevent signal collisions.*” EX1048 (Shaeffer) at Figs. 3-4B (reproduced below, showing the proper timing and the result of no signal collisions).

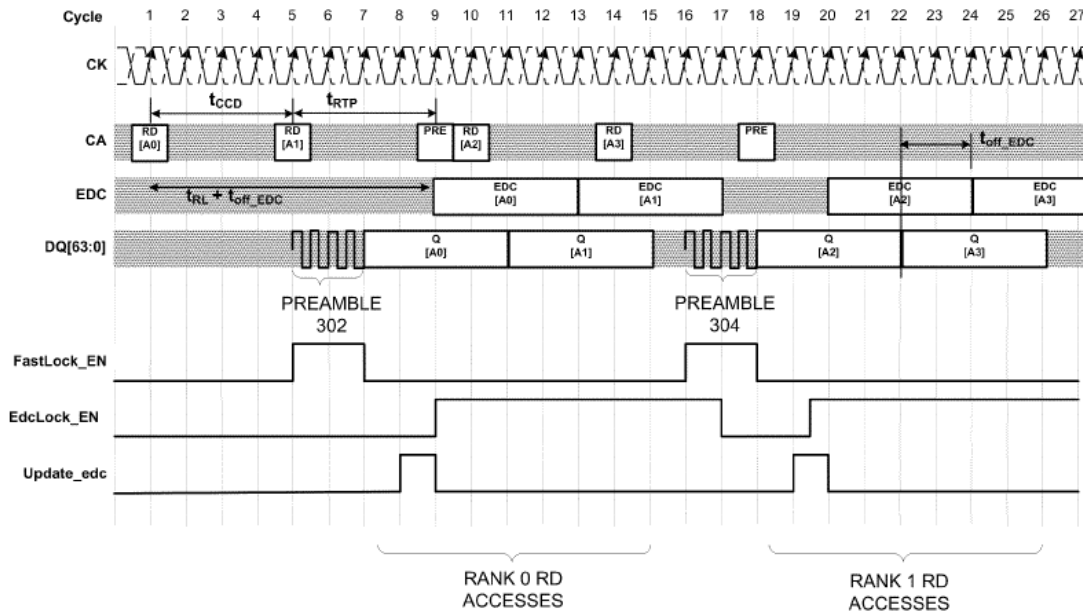


FIG. 3

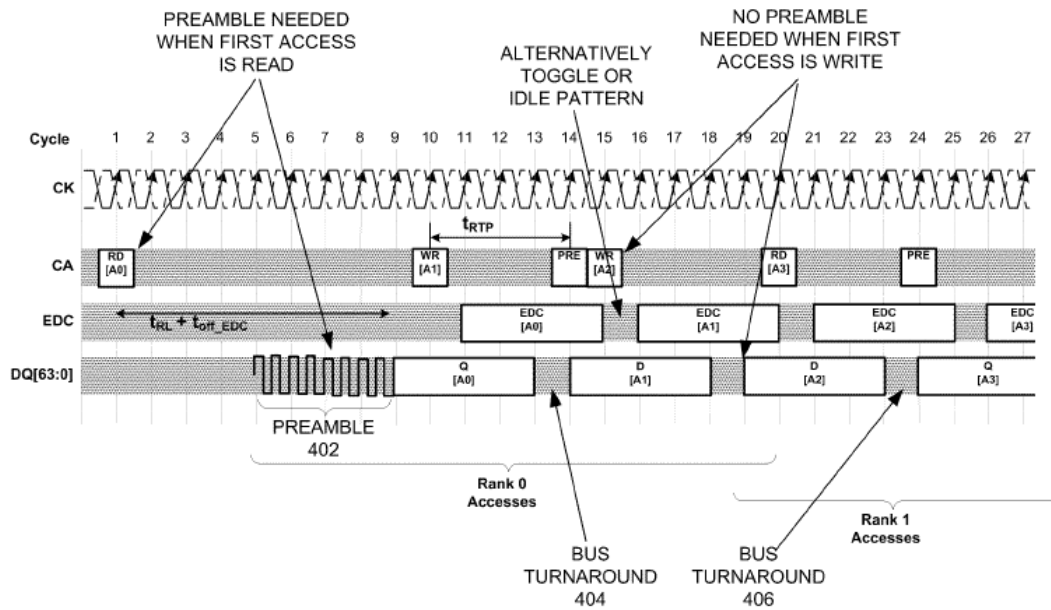


FIG. 4A

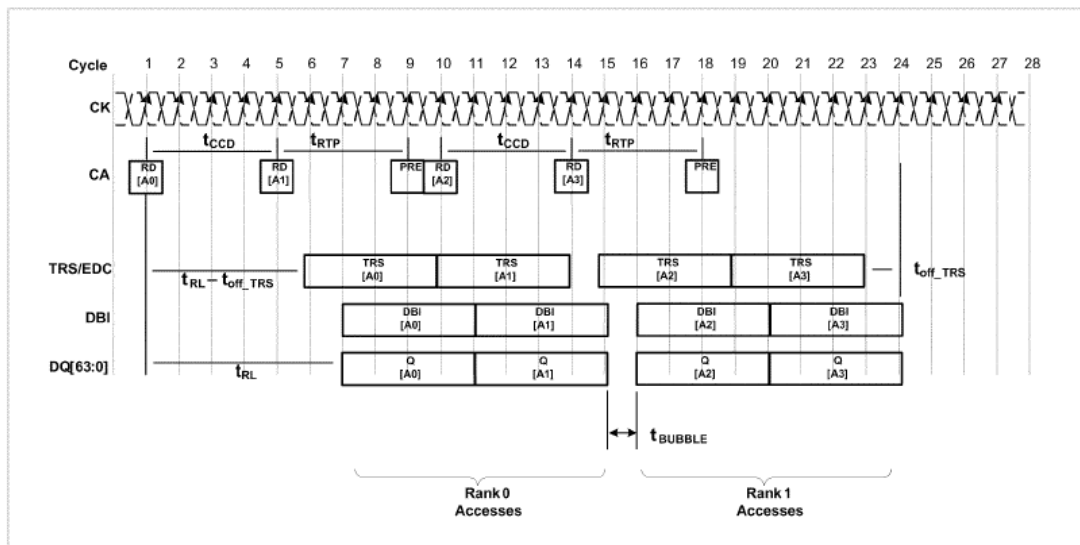


FIG. 4B

297. A Skilled Artisan would have also understood that these timing parameters were well known, standardized, and commonly used. *See, e.g.,* EX1019 (JESD79-3C) at p.165 (“t_{CCD}” defined as “CAS# to CAS# command delay”), p.62 (Figs. 33-34 showing t_{CCD} between Read commands), p.73 (Figs. 51-52 showing t_{CCD} between Write commands), p.165 (“t_{RTP}” defined as “Internal READ Command to PRECHARGE Command delay”), p.67 (Fig. 42 showing t_{RTP} between Read and Precharge commands), p.24 (defining the “overall Read Latency (RL)”), p.56 (Figs. 25-26 showing read latency (RL) delay between a read command and the corresponding data output). A Skilled Artisan would have understood that the exemplary timing parameters disclosed by Shaeffer are only that, a few examples of the many timing parameters a Skilled Artisan understood were commonly used “to prevent signal collisions.” *Id.* at 164-166

(Timing Parameters for Data Timing, Data Strobe Timing, Command and Address Timing). Applying such timing parameters to control memory dies “to prevent signal collisions” in a stack was also well known. See, e.g., EX1015 (Rajan) at Figs. 9-15 and 8:59-12:13; EX1045 (US8,244,971 to Rajan) at Figs. 9-15 and 10:14-13:35; EX1072, pp.34-38 (“persons of ordinary skill in the art knew how to deal with collisions”).

298. Accordingly, the prior art references in each of Grounds 3 and 4 teach “[t]he DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.”

16. [9.b.2] Interface Including Terminal

299. Claim 9 requires “the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals.”

300. As shown in the table below, claim element [9.b.2] is very similar to claim elements [1.c.1] and [1.e.1]:

Claim 1	Claim 9
[1.c.1] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, [1.e.1] a control die coupled between the terminals and the stacked DRAM dies,	[9.b.2] the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals,

301. For the same reasons that Grounds 3-4 teach a “*control die*” for claim elements [1.c.1] and [1.e.1], Grounds 3-4 also teach “*an interface*” for [9.b.2] (and similarly for [13.c]). See, e.g., EX1047 (Keeth) at Abstract (“Various embodiments include apparatuses, stacked devices and methods of forming dice stacks on an interface die.”). Thus, for the same reasons as with claim elements [1.c.1] and [1.e.1], Grounds 3-4 teach “*the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals.*”

17. [9.e.1] Second C/A and Data Interconnects

302. Claim 9 requires “*in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via*

the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects.”

303. The “*second data signals*” have no antecedent basis. It appears “*second signals*” should have been “*second data signals*.”

304. As shown in the table below, claim element [9.e.1] is very similar to claim elements [1.c.2], [1.d.1], [1.d.2], [1.f], [1.h.1], and [1.j]:

Claim 1	Claim 9
[1.d.1] ... the C/A interconnects including at least first C/A interconnects ... configured to conduct ... the second set of C/A signals, [1.f] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies ... [1.c.2] wherein the DRAM package is configured ... to receive second data signals in response to a second set of C/A signals ... [1.d.2] the data interconnects including at least first data interconnects ... configured to conduct ... the second data signals, [1.h.1] wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, [1.j] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, ...	[9.e.1] in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and

305. Because in Grounds 3-4, “*the first data interconnects ... [are] not in electrical communication with any data port on any of the second plurality of*

DRAM dies,” see limitation [1.h.1], it would have been obvious not to drive the same data signals which are driven on the first data interconnects “to any of the second plurality of DRAM dies via any of the data interconnects.” Thus, for the same reasons as with claim elements [1.c.2], [1.d.1], [1.d.2], [1.f], [1.h.1], and [1.j], Grounds 3-4 teach “in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects.”

18. [12.a] Consecutive First/Second Sets of C/A signals

306. Claim 12 requires “[t]he method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising.”

307. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan. See, e.g., EX1048 (Shaeffer) at Fig. 4A (reproduced below, where *the first set of C/A signals* [for a read operation, e.g., RD [A0],] and *the second set of C/A signals* [for a write operation, e.g., WR [A1],] are consecutive sets of C/A signals):

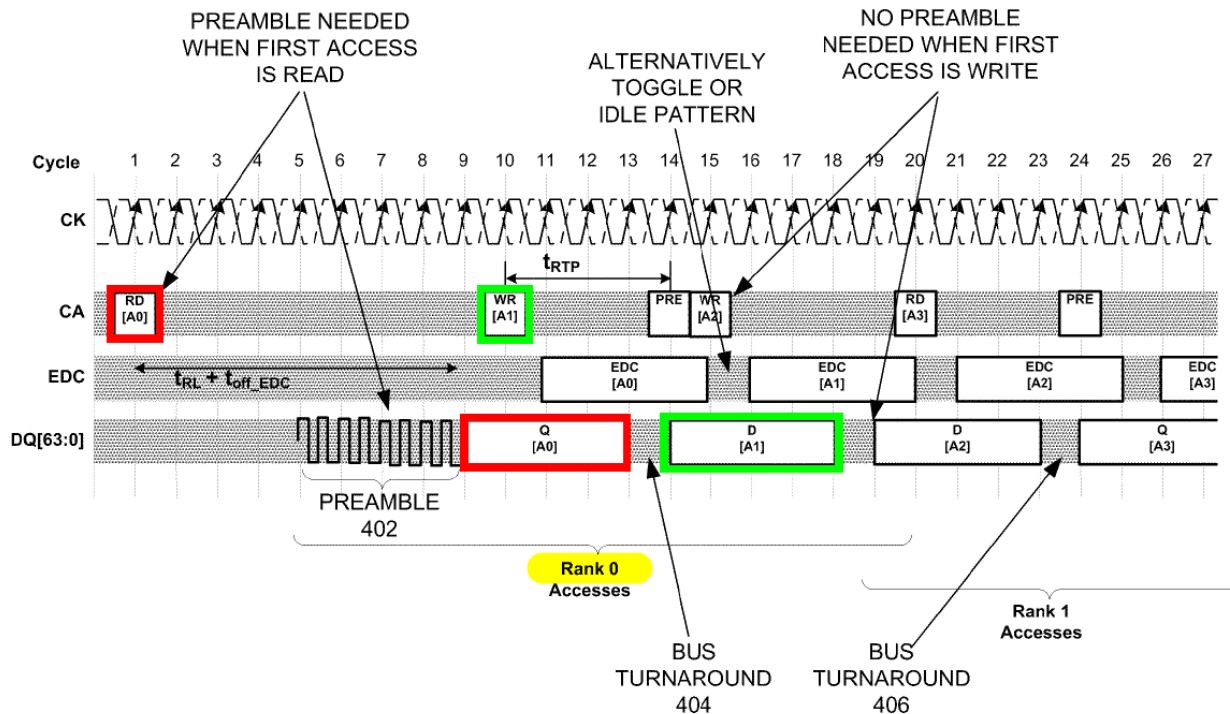


FIG. 4A

308. Accordingly, the prior art references in each of Grounds 3 and 4 teach “[t]he method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising.”

19. [12.b]-[12.c] First/Second Drivers

309. Claim 12 requires “enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals” and “enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals.”

310. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

311. For example, Keeth discloses that its interface die includes “components to control communication to and from” the memory dice. EX1047 (Keeth) at 3:21-26. Keeth further discloses that its interface die has “a vault control circuit” to “access ... data” from the memory dice. *Id.* at 4:13-16, 6:16-19. A Skilled Artisan would have understood from Keeth’s disclosures that the vault control circuit includes “*first drivers*” which are “*enabl[ed] ... to receive ... the first [(read)] data signals in response to the first set of C/A signals [for a read command]*” from the coupled memory dice through respective “*data interconnects*” and “*to ... drive*” those read data signals to the data terminals of the interface die. *Id.* at 3:62-67 (“Interface die 210 may include additional circuitry, e.g., buffers, and I/O drivers ...”). Shaeffer similarly discloses that its controller die includes an I/O interface 518-1 coupled to links 514, and “[s]ignals corresponding to data and/or commands (such as request-for-data commands) may be communicated on one or more of the links 514.” EX1048 (Shaeffer) at Fig. 5, 11:25-26, 12:4-7, 8:52-54.

312. Keeth also discloses that its interface die includes “components to control communication to and from” the memory dice. EX1047 (Keeth) at 3:21-26. Keeth further discloses that its interface die has “a vault control circuit” to “send data to” memory dice, including “driv[ing] data to partitions within the vaults.” *Id.* at 4:13-16, 6:16-19. A Skilled Artisan would have understood from

Keeth's disclosures that the vault control circuit includes "*second drivers*" that are "*enabl[ed] ... to receive ... the second [(write)] data signals in response to the second set of C/A signals [for a write command]*" and "*to ... drive the second [(write)] data signals*" through the corresponding "*data interconnects*" to the memory dice. *Id.* at 3:62-67 ("Interface die 210 may include additional circuitry, e.g., buffers, and I/O drivers ..."). Shaeffer similarly discloses that its controller die includes an I/O interface 518-1 coupled to links 514, and "[s]ignals corresponding to data and/or commands (such as request-for-data commands) may be communicated on one or more of the links 514." EX1048 (Shaeffer) at Fig. 5 (reproduced below), 11:25-26, 12:4-7, 8:52-54.

313. Accordingly, the prior art references in each of Grounds 3 and 4 teach "*enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals*" and "*enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals.*"

20. [12.d] Maintaining Non-Driving State

314. Claim 12 requires "*maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers.*"

315. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

316. Claim 12 depends from claim 9 which, like claim element [1.d.2] requires using the same “*first data interconnects*” for conducting “*the first [(read)] data signals*” and “*the second [(write)] data signals.*” See claim element [9.d.1] (“... receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects...”) and claim element [9.e.1] (“... driving the second data signals to the first plurality of DRAM dies via the first data interconnects...”). As discussed above, a Skilled Artisan was familiar with tristate buffers. See *supra* ¶¶58-59. A Skilled Artisan would have understood, and have been motivated, to use tristate buffers to drive and receive both write and read data through the same “*interconnects*” in order “*to prevent signal collisions,*” as evidenced by decades old textbooks. EX1038 (Stone) at pp.212-215. “The drivers commonly used for bus systems are tri-state drivers that have a low, high, and off (or high-impedance) mode of operation.” *Id.* at p.68. A Skilled Artisan would have understood that the “high-impedance” (off) mode is a “*non-driving state.*” *Id.* (“When all drivers are off, an undetermined bus line is free to float up or down or ...the bus line is held at the logic threshold... This [latter choice] reduces the charging delay ...”).

317. A Skilled Artisan also understood that, when there is no data to be driven — that is between memory read and write operations, such as during Shaeffer’s bus turnaround 404 on the bi-directional DQ[63:0] data line — the

tristate drivers are put into the high-impedance state (*“maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first [(read)] data signals by the first drivers and before receiving of the second [(write)] data signals by the second drivers”*). EX1038 (Stone) at p.151 (“At the end of the memory of the cycle, the DMA controller ... places its bus drivers in high-impedance mode.”). This avoids potentially “disastrous” bus conflicts with other drivers on the same data lines. *Id.* at pp.89-90 (“when tri-state drivers engage in a bus conflict ... there is a possibility of damaging the bus drivers ...). A Skilled Artisan would have also understood that turning the drivers off (into a high-impedance mode) between data transfers saves power since the drivers are not using current used to drive the load on the die *“interconnects.”* Accordingly, *“maintaining each of the ... drivers in a non-driving state”* between data transfers was the standard way of operation at the time for DDR memory taught by Keeth, *supra* ¶213, and Shaeffer. EX1019 (JESD79-3C) at p.63 (Fig. 36, reproduced below, showing the DQ lines being held at the threshold (middle) level between data transactions, indicating that all drivers are turned off when no read or write data is driven); EX1048 (Shaeffer), 8:60-64, Fig.4A (bus turnaround 404 after driving of read data (red) and before receiving write data (green) on the bi-directional DQ[63:0] data line).

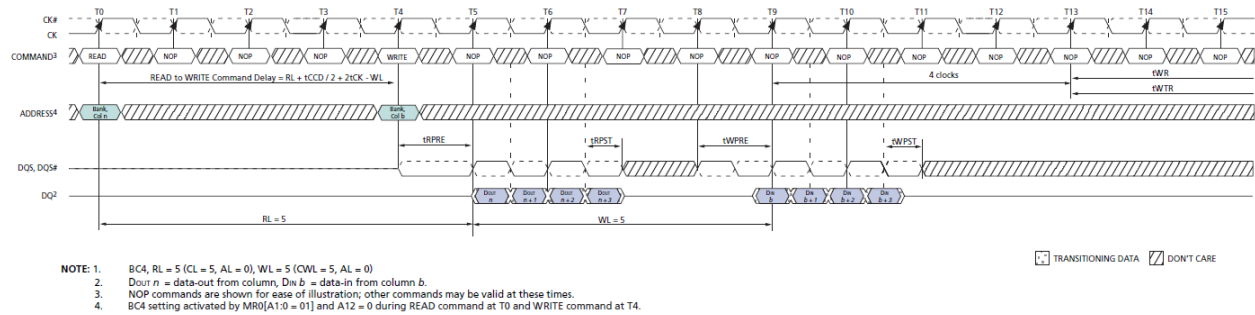


Figure 36 — READ (BC4) to WRITE (BC4) OTF

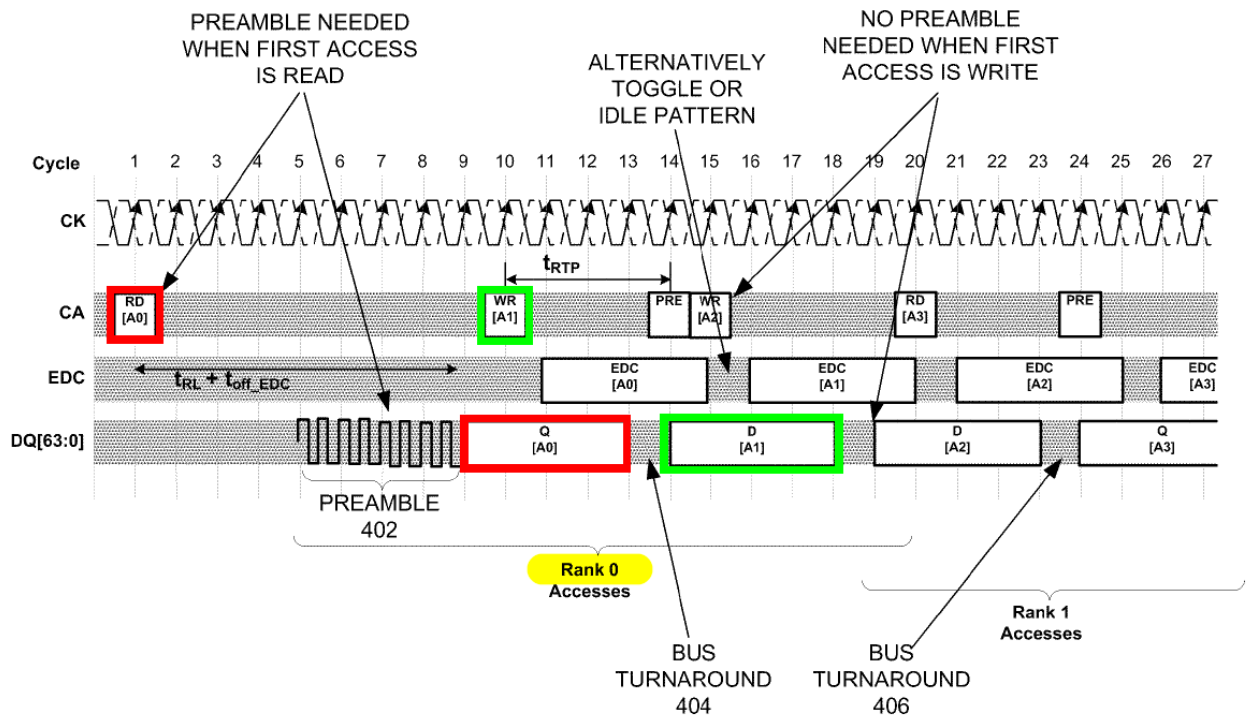


FIG. 4A

318. Accordingly, the prior art references in each of Grounds 3 and 4 teach “maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers.”

21. [13.b] Stacked DRAM Dies

319. Claim 13 requires “*a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port.*”

320. As shown in the table below, claim element [13.b] is very similar to claim elements [1.b.1], [1.b.2], and [1.d.2]:

Claim 1	Claim 13
[1.b.1] stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, [1.b.2] each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells; [1.d.2] ... the first data interconnects configured to conduct the first data signals and the second data signals,	[13.b] a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;

321. Claim element [1.d.2] requires the same “*first data interconnects*” to conduct both read data (“*first data signals*”) and write data (“*second data signals*”), thus these die interconnects and the corresponding data ports on each DRAM die are “*bi-directional*.” Furthermore, a Skilled Artisan would have understood that data ports on DRAM devices are commonly implemented as being bi-directional, as taught by Shaeffer. EX1048 (Shaeffer) at Figs. 1A and 4A (below, showing bi-directional data exchange between a controller and memory, including read data (red) and write data (green) on the same bi-directional DQ[63:0] data lines); EX1019 at p.3 (bi-directional DQ pins), p.13 (“DQ...Bi-directional data bus”). Thus, for the same reasons as with claim elements [1.b.1], [1.b.2], and [1.d.2], Grounds 3-4 teach “*a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port.*”

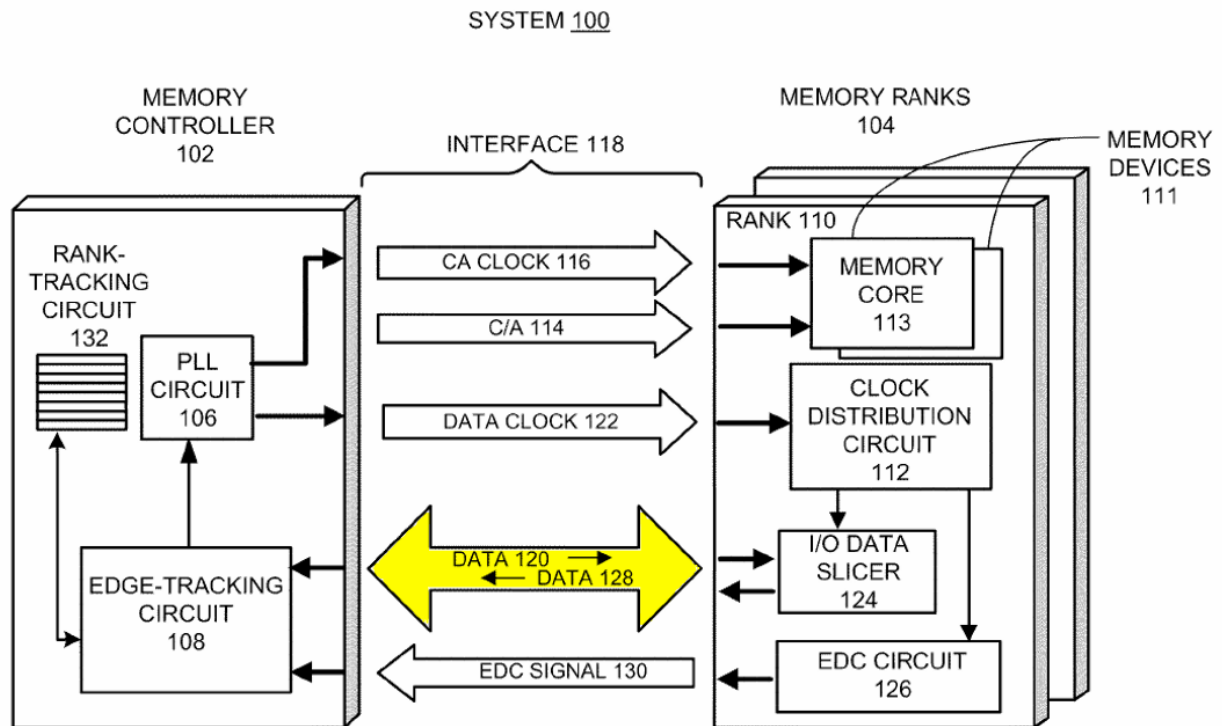


FIG. 1A

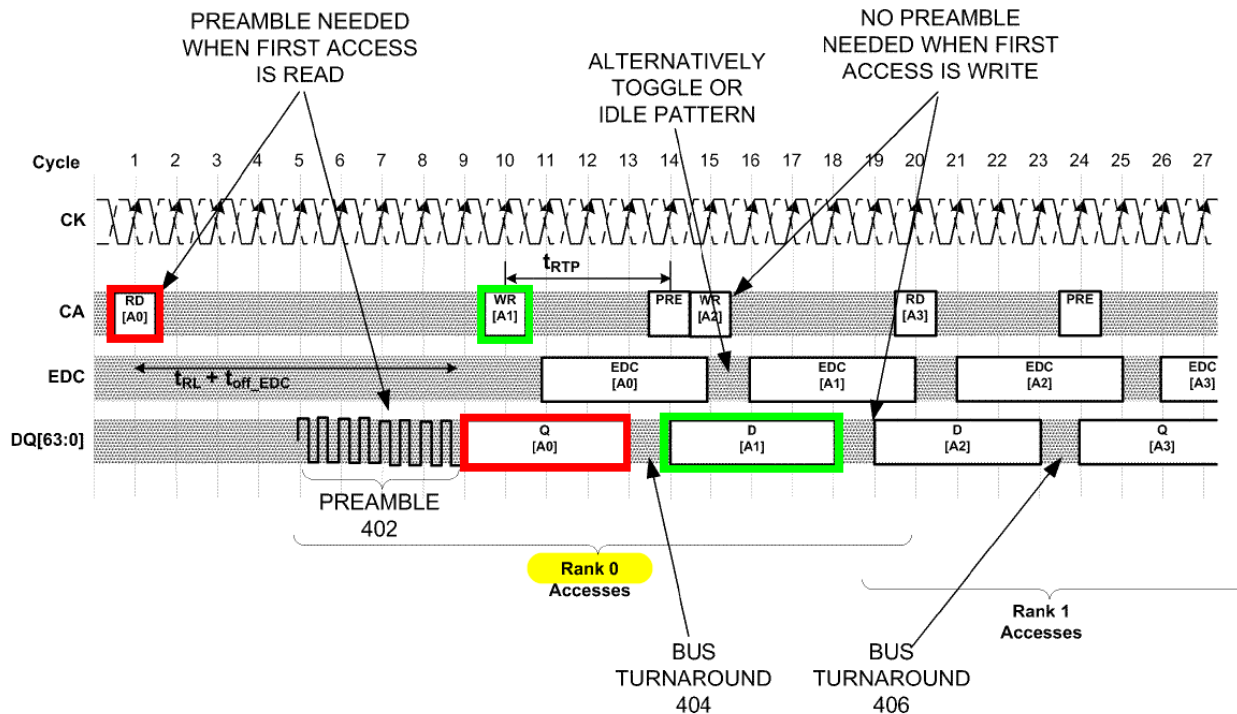


FIG. 4A

22. [13.i] First/Second Set of C/A Signals

322. Claim 13 requires “the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects.”

323. As shown in the table below, claim element [13.i] is very similar to claim elements [1.c.1] and [1.d.1]:

Claim 1	Claim 13
[1.c.1] ... wherein the DRAM package is configured to receive C/A signals via the C/A terminals ... [1.d.1] ... the C/A interconnects including at least first C/A interconnects ... configured to conduct the first set of C/A signals and the second set of C/A signals,	[13.i] the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects;

324. As [1.d.1] requires, Keeth discloses interleaving conductive paths for the C/A signals to alternating dies in the stack, such as *first C/A interconnects* [e.g., “a first conductive path” to “odd dice,” EX1047, claims 39, 42, included in “conductive paths 507” (red) below] *and second C/A interconnects* [e.g., “a second conductive path” to “even dice,” *id.*, included in “conductive paths 508” (blue) below].

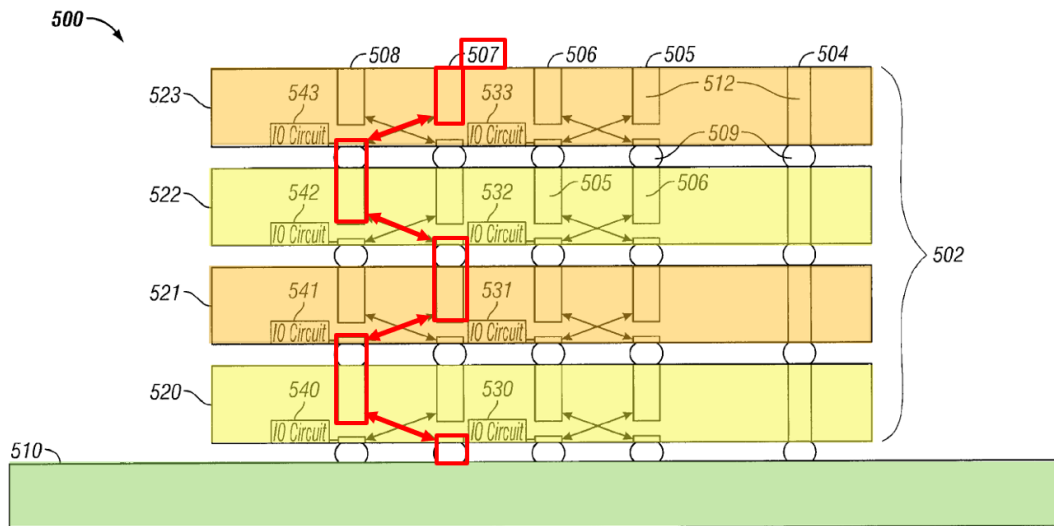


FIG. 5

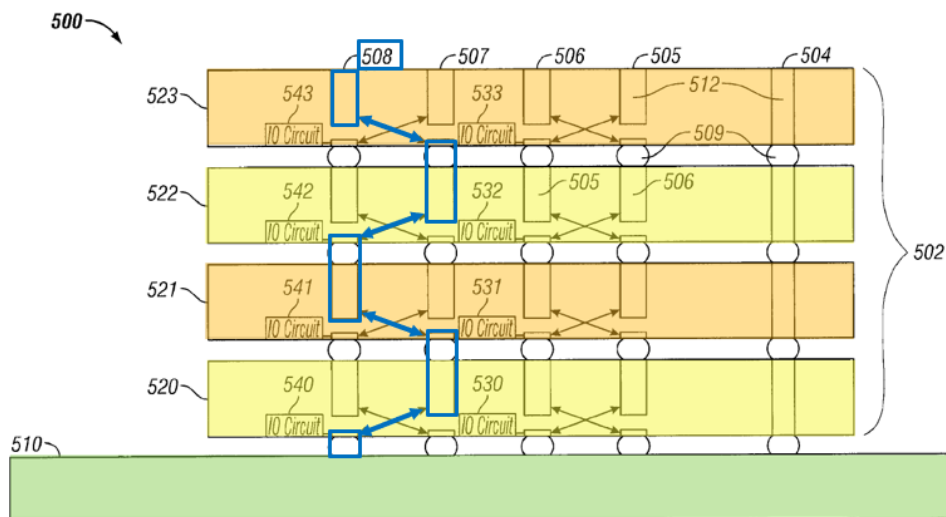


FIG. 5

EX1047, Fig.5. Shaeffer teaches transmitting two sets of C/A signals (e.g., for read and write) to the same rank, and thus on the same C/A interconnections, such as RD[A0] (red below) followed by WR[A1] (green below) both to rank 0 (highlighted in yellow):

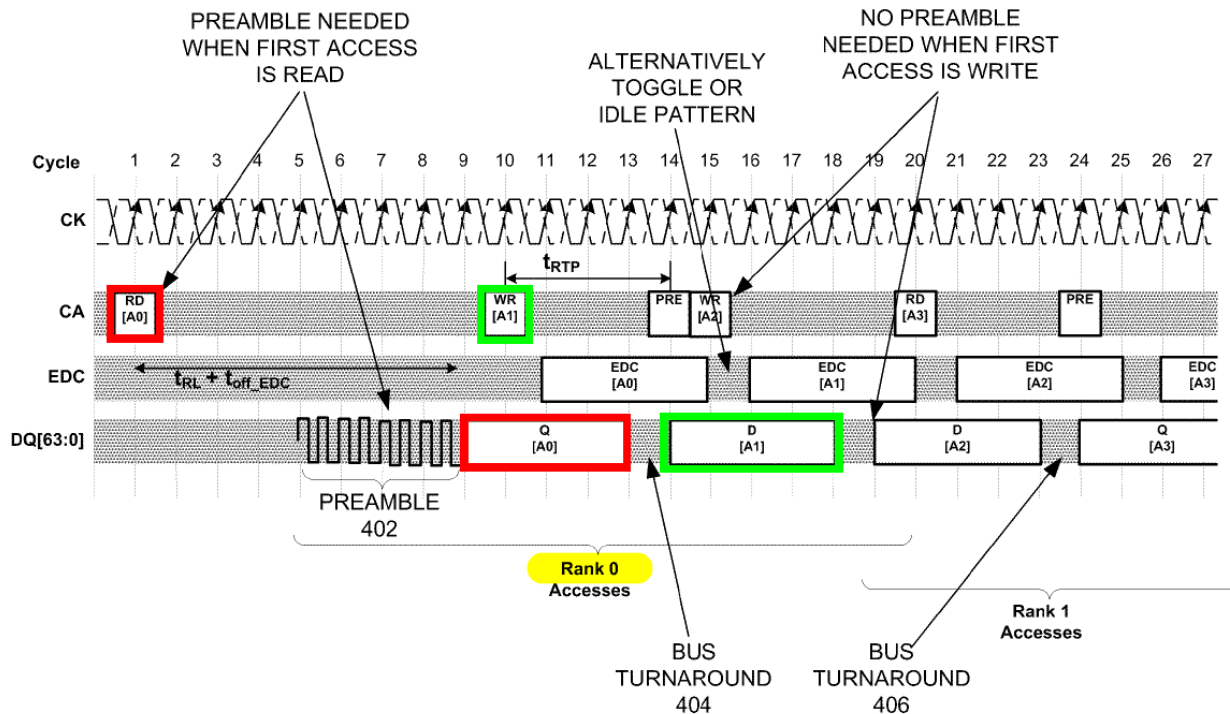


FIG. 4A

EX1048, Fig.4A, 7:11-8:39. Shaeffer also teaches two sets of C/A signals that are directed to different ranks (ranks 0 and 1), in which case those C/A signals may be conducted by different C/A interconnects (e.g., Keeth's 507 (red) above in Fig.5 coupled to rank 0, and Keeth's 508 (blue) above in Fig.5 coupled to rank 1). For example, Shaeffer teaches a read command, such as RD[A0], to rank 0, followed by a write command, such as WR[A2], to rank 1, as shown above in Figure 4A.

EX1048 (Shaeffer) at 7:11-8:39, FIG. 4A; *see also id.* at Fig. 5 (showing separate links 514-1 and 514-2 coupled to separate memory devices 512-1 and 512-2 in the same rank). Furthermore, Shaeffer teaches that the precise sequence of commands and ranks is not limited to just the example shown in Figure 4A. *See, e.g.,* EX1048

(Shaeffer) at 12:49-57 (“The foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art.”). For example, in Figure 3, the second command in the sequence is a read command RD[A1] to rank 0, while in Figure 4A the second command in the sequence is a write command WR[A1] to rank 0 (followed by a write command WR[A2] to rank 1). *Id.* Figs.3, 4A, 5:50-67, 8:32-9:10 (teaching that Shaeffer’s disclosure is not limited to “the embodiments illustrated in FIGS. 3 and 4 [which] only illustrate two memory transactions on a given rank”). Thus, Shaeffer teaches that either a read or write command can target rank 0, and then the next consecutive command can be a write command to rank 1. It was standard for DDR memory devices, which both Keeth and Shaeffer identify as exemplary memory devices, EX1047 (Keeth) at 2:40-41; EX1048 (Shaeffer) at 8:60-64, to perform a read followed consecutively by a write, *see* EX1019 (JESD79-3C) pp.63, 65 (READ to WRITE), as well as other sequences such as READ to READ, *id.* pp.62, 64, WRITE to WRITE, *id.* pp.73, 75-76, and WRITE to READ, *id.* pp.72, 74-75; EX1023, pp.2-3; EX1022, p.413. Similarly, the ’087 Patent teaches that “DDR3” is an embodiment, EX1001, at 4:53, and the ’087 Patent does not disclose any particular sequence of commands (and in fact does not

include any timing diagrams at all), consistent with the fact that Skilled Artisans already knew how to time commands properly to avoid “collisions,” as explained above, *supra* ¶¶295-297. Thus, Grounds 3-4 teach that the first read command (i.e., “a first set of C/A signals”) and the subsequent write command (i.e., “a second set of C/A signals”) can be consecutive commands, to different ranks, conducted “via the first C/A interconnects [e.g., on Keeth’s 507 (red) above in Fig.5, coupled to rank 0, for the read command]” and “the second C/A interconnects [e.g., on Keeth’s 508 (blue) above in Fig.5, coupled to rank 1, for the consecutive write command],” respectively. Accordingly, for the same reasons as with claim elements [1.c.1] and [1.d.1], Grounds 3-4 teach “the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects.”

23. [13.I] First/Second Signals to Select First/Second DRAM Die

325. Claim 13 requires “the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the

second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals.”

326. As shown in the table below, claim element [13.i] is very similar to claim elements [6.a] and [6.b]:

Claim 6	Claim 13
[6.a] The DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and [6.b] the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;	[13.i] the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

327. As discussed with reference to claim element [6.a], *supra* ¶¶283-287, Grounds 3-4 teach C/A signals including a signal to select a DRAM die. Also, as discussed with reference to claim element [13.i], *supra* ¶¶322-324, the combination of Keeth and Shaeffer teaches a read command and a consecutive write command directed to DRAM dies in different ranks (e.g., ranks 0 and 1). In such a case, a Skilled Artisan would have understood that “*the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies* [e.g., a DRAM die in rank 0 to which the read command is

directed]” and that “*the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies [e.g., another DRAM die in rank 1 to which the consecutive write command is directed].*” Thus, for the same reasons as with claim elements [6.a] and [6.b], Grounds 3-4 teach “*the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals.*”

24. [13.m] First/Second Data Signals

328. Claim 13 requires “*the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface.*”

329. As shown in the table below, claim element [13.m] is very similar to claim elements [1.d.2] and [1.j]:

Claim 1	Claim 13
[1.d.2] ... the first data interconnects configured to conduct the first data signals and the second data signals, [1.j] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;	[13.m] the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

330. As discussed with reference to claim element [13.i], *supra* ¶¶322-324, the combination of Keeth and Shaeffer teaches a read command (e.g., “a first set of C/A signals”) directed to rank 0 and a consecutive write command (e.g., “a second set of C/A signals”) directed to rank 1, and thus the “first” and “second set of C/A signals” are conducted “via the first” and “second C/A interconnects,” respectively. In such a case, the data signals associated with the two sets of C/A signals are also conducted by the respective data interconnects. Namely, a Skilled Artisan would have understood from the disclosures of Keeth and Shaeffer that “first data signals associated with the first set of C/A signals” are driven “between the first data interconnects [coupled to rank 0] and the interface” and that “second data signals associated with the second set of C/A signals” are driven “between the second data interconnects [coupled to rank 1] and the interface.” Thus, for the

same reasons discussed with claim elements [1.d.2] and [1.j], Grounds 3-4 teach “the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface.”

25. [13.r] typographical error

331. Limitation [13.r] requires “the control die is configurable to drive the one or more second signals to the second DRAM die ene or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects.”

332. In my opinion, the underlined phrase above, “ene or more DRAM dies of the plurality of stacked DRAM dies-,” is a typographical error. As explained above, I understand that obvious minor typographical and clerical errors in patents—evident from the face of the patent—may be corrected if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims. *See supra* ¶57. Applying that two-part test, in my opinion the claim may reasonably be corrected by simply deleting the

underlined phrase, which appears to have been inadvertently added when the patent was printed.

333. First, the face of the patent indicates that the underlined phrase is a typographical error. The inclusion of garbled word “ene” along with the random hyphen “-” at the end of the phrase suggests a typographical error.

334. The phrase renders the limitation grammatically incorrect and disrupts sentence structure, resulting in a nonsensical limitation. Further, the phrase introduces redundancy by attempting to further modify “the second DRAM die.” In this claim element, “the second DRAM die” is already identified as the destination of the “the one or more second signals” driven by “the control die.” The extra language in the phrase, which ambiguously references “DRAM dies of the plurality of stacked DRAM dies,” adds no meaningful content and only confuses the reader. This is especially so, given that “the second DRAM die” is already defined in earlier in the claim as being included in “in the first plurality of stacked DRAM dies.” EX1001 at 26:31-32. Removing the phrase resolves all these problems in the claim language.

335. The language in other claim limitations further supports the proposed correction. For example, within Claim 13 itself, a structurally parallel limitation appears in [13.q], immediately before this claim element, [13.r]. That limitation recites that “the control die is configurable to receive the one or more first signals

from the first DRAM die via the one or more of the first unidirectional interconnects.” While “the first DRAM die” in [13.q] corresponds to “the second DRAM die” in [13.r], no additional language comes after “the first DRAM die.” Thus, the limitation is unambiguous as to identifying the DRAM die (i.e., “the first DRAM”) that drives “one or more first signals” via “the first unidirectional interconnects.” This parallel limitation supports the proposed correction to remove the underlined phrase after “the second DRAM die,” which makes it confusing to identify the DRAM die that receives the “one or more second signals” “via the one or more of the second unidirectional interconnects.” Similar limitations in other claims also do not include any confusing phrase between the DRAM die that receives a signal and the unidirectional interconnects that conduct the signal to the DRAM die. *See, e.g.*, 26:51-54 (Claim 9) (“driving one or more signals ... **to the first plurality of DRAM dies via one or more of the second unidirectional interconnects**”), 31:46-49 (Claim 20) (“the control die is configured to drive one or more second signals ... **to the one or more DRAM dies via one or more of the second unidirectional interconnects.**”). Claim 1 has a phrase (“of the stacked DRAM dies”) between the DRAM that receives “signals” (“one or more DRAM dies”) and the interconnects that conduct the “signals” (“via the second unidirectional interconnects”). But the phrase in Claim 1 clearly modifies “one or

more DRAM dies” that receive “signals” “via the second unidirectional interconnects,” unlike the garbled and confusing phrase in Claim 13.

336. Second, the prosecution history does not suggest a different interpretation of the claims. In fact, the Examiner issued a Notice of Allowance that includes the amendment of Claim 12 in the application (which issued as Claim 13) as follows, which does not include the garbled text that appears in the patent for Claim 13:

the control die is configurable to drive the one or more second signals to the second DRAM die ~~one or more DRAM dies of the plurality of stacked DRAM dies~~ via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

Ex. 1002 at 841.

337. This indicates that both the Examiner and the applicant did not intend to include the garbled text at issue.

338. For the foregoing reasons, the inclusion of the underlined phrase in limitation [13.r] appears to be a typographical error that may reasonably be corrected by simply deleting the underlined phrase.

26. [13.u] TSVs Not in Electrical Communication

339. Claim 13 requires “*each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical*”

communication with and is not connected to any data port on the corresponding DRAM die.”

340. As shown in the table below, claim element [13.u] is very similar to claim element [1.h.3]:

Claim 1	Claim 13
[1.h.3] wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;	[13.u] each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

341. Keeth discloses to a Skilled Artisan that, when a TSV is “*not connected to*” a data port, it is “*not in electrical communication with*” that data port. For example, FIG. 7 of Keeth shows “[f]irst and third conductive paths 705 and 707 may . . . pass through . . . dice 720 and 722.” EX1047 (Keeth) at 7:11-13, Figs. 5 and 7 (below). Moreover, Keeth discloses that its interleaving conductive paths pass through every other die “without connecting to any circuitry” on those dies. EX1047 (Keeth) at 5:39-62, Figs. 5 and 7.

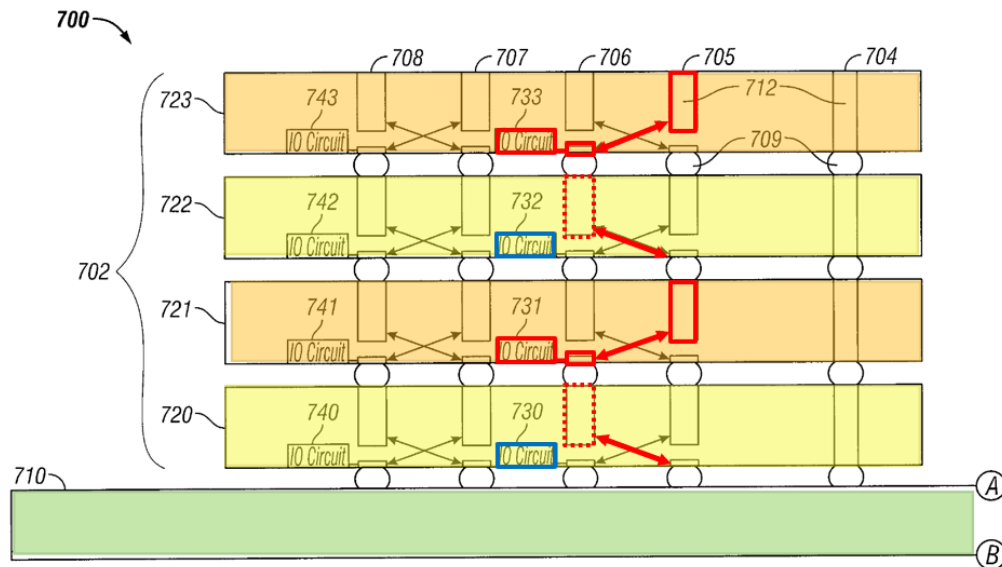


FIG. 7

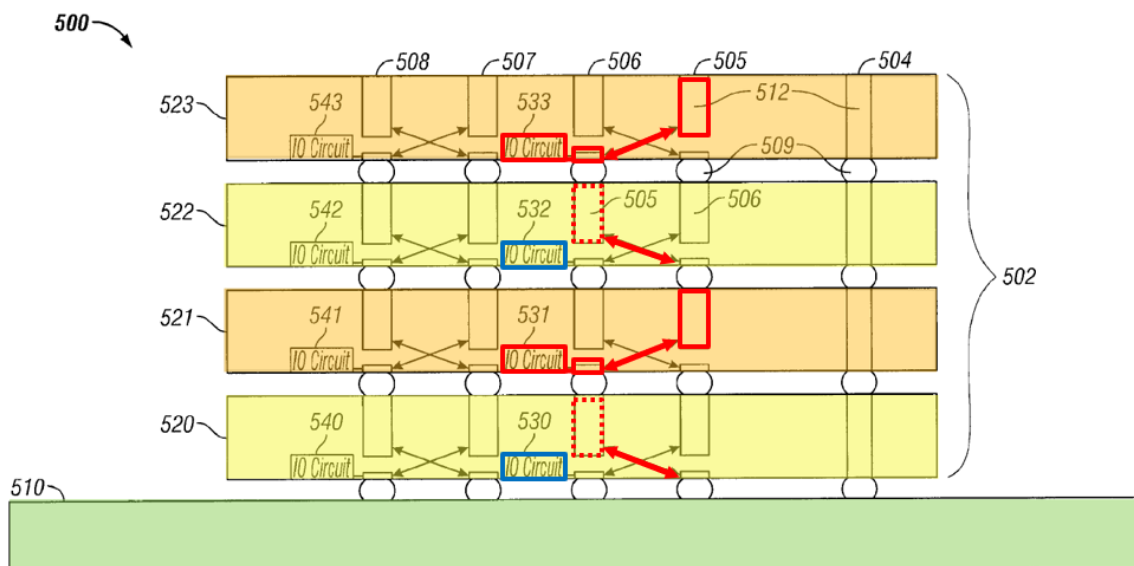


FIG. 5

Thus, for the same reasons as with claim element [1.h.3], Grounds 3-4 teach “*each of the at least one second TSV* [e.g., a TSV in dashed red above] *in a corresponding DRAM die of the at least one second DRAM die* [e.g., yellow] *is not*

in electrical communication with and is not connected to any data port on the corresponding DRAM die [e.g., blue].”

27. [23.c.1] Terminals

342. Claim 23 requires “*terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals.*”

343. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

344. The combination of Keeth and Shaeffer alone or in view of Riho2 also renders obvious the “*terminals including ... power supply terminals.*” As claim element [1.a] requires, both Keeth and Shaeffer discloses a package including DRAM dies, such as DDR3 DRAMs, and a Skilled Artisan would have understood that DRAMs require power supply for their operation and, for that purpose, DRAM packages include power supply terminals. *See, e.g.,* EX1048 (Shaeffer) at 1:58-61 (“For computer systems, ... which contain numerous ranks of memory, idle power may be an issue. At any given time at most one rank is actively accessed, while all other ranks are idle but still consuming idle power.”), 8:60-64 (“The memory devices can include...double data rate....DDR3 and future memory

types”); EX1018 (Riho2), ¶[0102], Fig.8 (“VDDQ”); *see also*, EX1019 (JESD79-3C) at pp.3-11 (DDR3 SDRAM Package Pinout including power supply terminals, such as VDD, VDDQ), p.14 (describing VDD and VDDQ as “Power Supply”).

345. Accordingly, the prior art references in each of Grounds 3 and 4 teach *“terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals.”*

28. [23.m.1] First Supply Voltage Interconnect

346. Claim 23 requires *“wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies.”*

347. The prior art references in each of Grounds 3 and 4 teach this limitation to a Skilled Artisan.

348. As an initial matter, the term *“the power supply interconnects”* lacks antecedent basis because this is the first time *“power supply interconnects”* are mentioned. In any event, a Skilled Artisan would have understood that each of the *“DRAM dies”* requires power supply for its operation, and the DRAM package

includes at least one “*power supply terminal*” to receive such power, as discussed above with reference to claim element [23.c.1], *supra* ¶¶342-345. A Skilled Artisan would have also understood that the power received at the “*power supply terminal*” is coupled “*to each of the ... DRAM dies*” by a “*supply voltage interconnect.*” *Id.*, see also EX1048 (Shaeffer) at 2:16-8 (“supply voltage and temperature may drift, which can cause the delay of the circuitry in the individual ranks to change”).

349. Furthermore, Riho2 expressly discloses such a “*power supply terminal*” (VDDQ) and a “*supply voltage interconnect*” for the supply voltage VDDQ0. EX1018 (Riho2) at Fig. 8 (reproduced below). Riho2 also explains that such a “*supply voltage interconnect*” can be implemented, for example, by TSVs. *Id.* at (“The supply voltage conversion circuit PS supplies four supply voltages VDDQ0 (1.8V, 1.5V, 1.2V, and 0.9V) appropriate for the first to fourth memory modules (for the types of stacked memory devices) shown in FIG. 7(B), from a power supply VDDQ given, exclusively for the output transistors, to the through electrodes (TSV) corresponding to the terminals (BGA) of the stacked memory devices or the supply terminals of the chip dies.”). This was a standard, well known technique at the time. See, e.g., EX1016 (Riho) at Fig. 2 and [0036] (“From the VDDQ conversion circuit 209, a memory-driving main power supply voltage VDDQ is applied not only to the input/output circuit 207 and the logic

control circuit 203 of the logic LSI chip 20, but also to the SDRAMs D0 to D15 stacked on the logic LSI chip 20.”) and [0030] (“It is needless to say that power supply penetrating through substrate vias (TSVs) are also provided in addition to the above-mentioned TSVs.”). Thus, the Keeth-Shaeffer combination alone or in view of Riho2 renders obvious that “*power supply interconnects include a first supply voltage interconnect ..., wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies*”

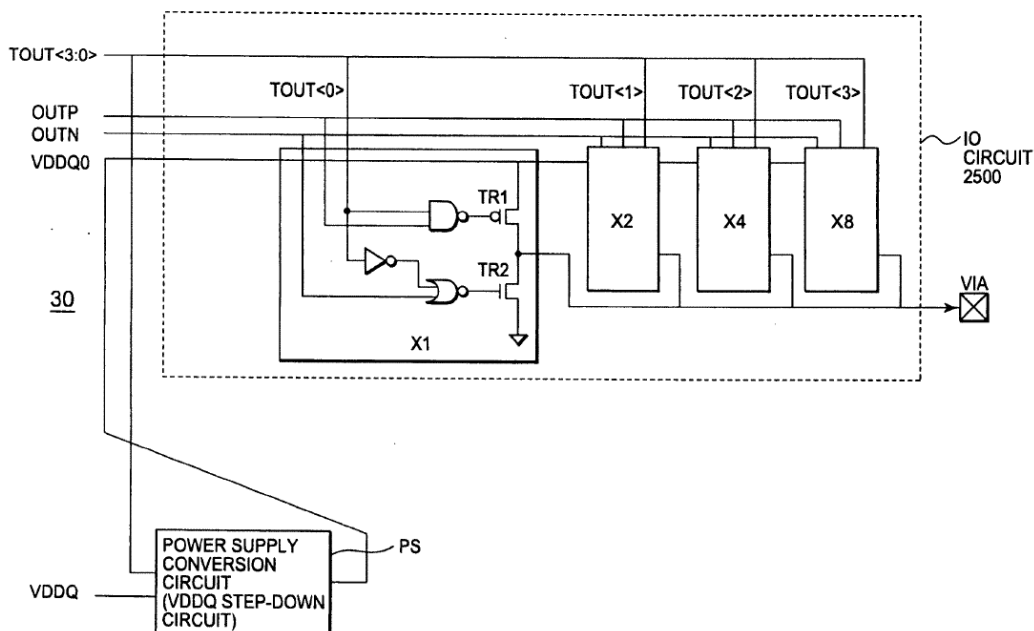
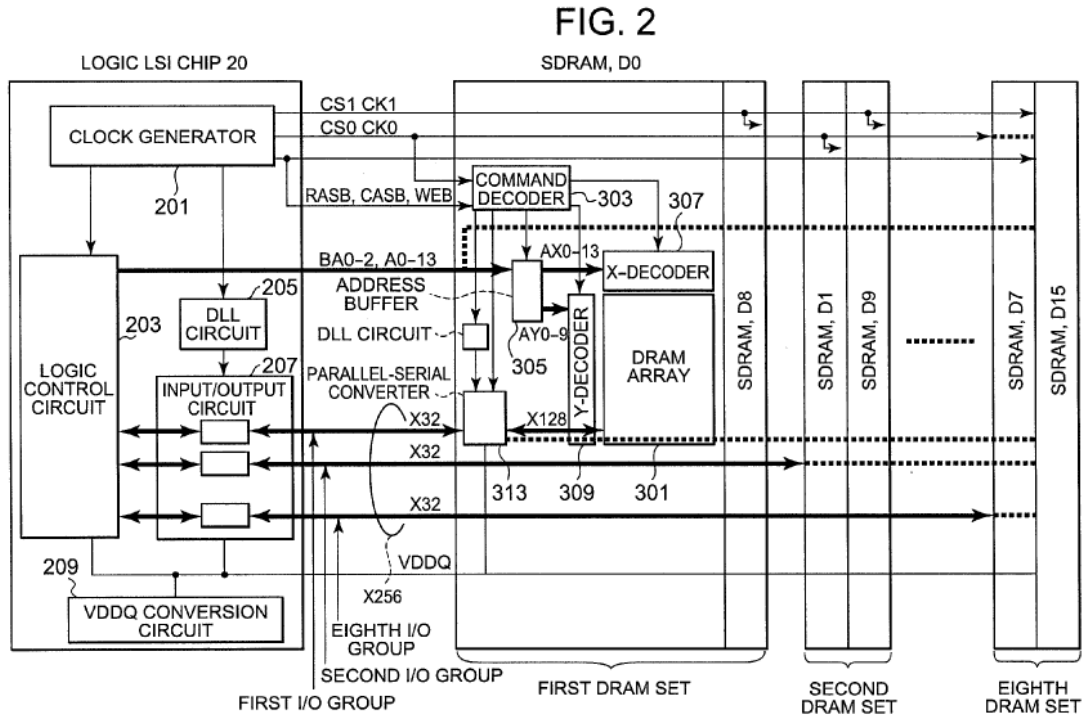
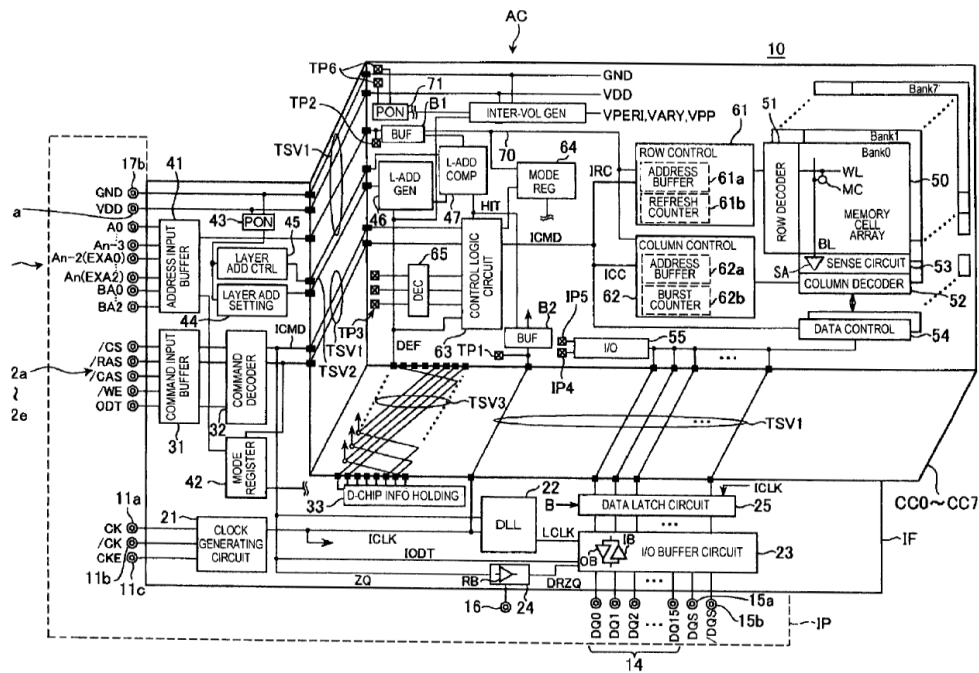


FIG. 8



EX1043 (Ide) at Fig. 4 (separate TSVs for VDD).



350. Furthermore, Keeth discloses using interleaving conductive paths which connect with circuitry on alternating dice of the stack. EX1047 (Keeth) at Abstract (“the conductive paths may be arranged to connect with circuitry on alternating dice of the stack”). A Skilled Artisan would have understood that Keeth’s interleaving conductive path can also be used as “*a first supply voltage interconnect*” to provide supply voltage to, say, odd dice in the stack, and the other interleaving conductive path of the pair can be used as “*a second supply voltage interconnect*” to provide supply voltage to the, say, even dice in the stack. Like the other interleaving conductive paths of Keeth, such a “*first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies.*” *Id.* at 4:4-16 (“For example, a first communication path in a vault may be connected to circuitry (e.g., input/output circuitry) of all odd partitions in the memory vault and pass through the even vaults without connecting to circuitry. A second communication path may connect to circuitry (e.g., input/output circuit) on the even partitions in the same vault and pass through the odd partitions without connecting to circuitry.”).

351. Keeth also discloses that, by using such interleaving conductive paths, its interface die “may access each die (or a partition of each die) independently of the die above or below.” *Id.* at 5:63-67. A Skilled Artisan would have been

motivated by Keeth's disclosure of independent operation of odd and even dies to use a pair of interleaving conductive paths as "*a first supply voltage interconnect*" and "*a second supply voltage interconnect*," because the interleaving conductive paths for the supply voltage is compatible with the independent operation of odd and even dies in the stack. For example, even if one conductive path breaks down and cannot supply voltage to say, the even dies in the stack, the other conductive path in a pair of interleaving conductive paths can still deliver power to the odd dies, and vice versa. A Skilled Artisan would have also understood that, due to the independent operation of the odd and even dies, the supply voltage might become noisy, e.g., due to "power supply induced jitter (PSIJ)," if both the odd and even dies are connected to the same interconnect. EX1048 (Shaeffer) at 4:11-14; *see also id.* at 2:18-19 ("Moreover, high-frequency power supply noise can also shift the timing of the ranks"). A Skilled Artisan would have also understood that "power noise is of a bigger concern in the 3D-DRAM than in a single DRAM since it has multiple ranks which can be operated almost at the same time," including refresh operations which create "the largest VDD/VSS noise." EX1059 (Kang IEEE Paper) at pp.4-5. Thus, a Skilled Artisan would have been motivated to lower power supply noise by using Keeth's pair of interleaving conductive paths to provide supply voltage to odd and even dies separately.

352. Accordingly, the prior art references in each of Grounds 3 and 4 teach *“wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies.”*

29. [24.j] Unidirectional Third Conduit

353. Claim 24 requires *“each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect.”*

354. As shown in the table below, claim element [24.j] is very similar to claim elements [1.l] and [1.p.1]:

Claim 1	Claim 24
[1.I] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies; [1.p.1] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and	[24.j] each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

355. A Skilled Artisan would have understood that “*a signal received from a corresponding third die interconnect,*” such as the TRS/EDC signals of Shaeffer, are driven to “*the interface*” by “*a unidirectional conduit*” which is “*not configurable to drive any signal to the corresponding third die interconnect*” because the “*third*” die interconnects are only used to conduct the TRS/EDC signals from the memories to the control die. *See, e.g.,* EX1047 (Keeth) at 3:44-51 (“... interface die 210 may comprise control circuits 212 to enable communication and control with the corresponding memory partition 204 stacked above the respective control circuit via communicative paths 208.”). Thus, for the same reasons as with claim elements [1.I] and [1.p.1], Grounds 3-4 teach “*each of the*

third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect.”

30. [24.k] Unidirectional Fourth Conduit

356. Claim 24 requires “*each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect.*”

357. As shown in the table below, claim element [24.k] is very similar to claim elements [1.m] and [1.p.2]:

Claim 1	Claim 24
[1.m] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;	[24.k] each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;
[1.p.2] in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.	

358. It would have been obvious to a Skilled Artisan to use “a *unidirectional conduit ... to drive a [unidirectional data clock/strobe (122)] signal*” to a unidirectional “*fourth die interconnect,*” since a unidirectional driver has sufficient capability to drive signals to a unidirectional interconnect, and Shaeffer does not teach conducting any signal in the opposite direction on line 122. See *supra* ¶253. Thus, for the same reasons as with claim elements [1.m] and [1.p.2], Grounds 3-4 teach “*each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect.*”

31. [24.I] First/Second/Third/Fourth Set of C/A Signals

359. Claim 24 requires “*the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation.*”

360. As shown in the table below, claim element [24.I] is very similar to claim elements [1.c.1] and [1.c.2]:

Claim 1	Claim 24
[1.c.1] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, [1.c.2] wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;	[24.I] the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;

361. Furthermore, a Skilled Artisan would have understood that DRAM devices are accessed repeatedly during normal operation for read and write operations. *See supra* ¶324. Thus, for the same reasons as with claim elements [1.c.1] and [1.c.2], Grounds 3-4 teach “*the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation.*”

32. [24.m.2] Second Signals

362. Claim 24 requires “*a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface.*”

363. “[A] *first subset of the third die interconnect*” is indefinite because a singular “*third die interconnect*” cannot have a “*subset.*” Also, “***the third die interconnect***” is not introduced earlier in the claim. However, Netlist’s infringement contentions in the district court litigation on this patent appear to interpret this limitation as “*a first subset of the third die interconnect[s]*” (plural). See EX1089 at 149 (citing prior infringement analysis from claim 1 and referring to RDQS signal). Using Netlist’s interpretation of this limitation, it corresponds to “*first unidirectional interconnects*” of the “*first plurality of DRAM dies*” in claim 1, and claim element [24.m.2] would be very similar to claim elements [1.b.1], [1.e.2], [1.l] and [1.p.1]:

Claim 1	Claim 24
[1.b.1] ... a first plurality of DRAM dies ... [1.e.2] the control die including conduits ... [1.l] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies; [1.p.1] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and	[24.m.2] a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;

364. For the same reasons as with claim elements [1.b.1], [1.e.2], [1.l] and [1.p.1], Grounds 3-4 teach “*a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface.*”

33. [24.n.2] Fourth Signals

365. Claim 24 requires “*a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect.*”

366. For the same reasons discussed above, *supra* ¶363, “a first subset of the fourth die interconnect” is indefinite because the singular term cannot have a “subset” and is not properly introduced. However, Netlist’s infringement contentions in the district court litigation appear to interpret this limitation as “a first subset of the fourth die interconnect[s]” (plural). See EX1089 at 150 (citing prior infringement analysis from claim 1 and referring to WDQS signal). Using Netlist’s interpretation of this limitation, it corresponds to “second unidirectional interconnects” of the “first plurality of DRAM dies” in claim 1, and claim element [24.n.2] would be very similar to claim elements [1.b.1], [1.e.2], [1.m] and [1.p.2]:

Claim 1	Claim 24
[1.b.1] ... a first plurality of DRAM dies ... [1.e.2] the control die including conduits ... [1.m] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die; [1.p.2] in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.	[24.n.2] a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect[s];

367. For the same reasons as with claim elements [1.b.1], [1.e.2], [1.m] and [1.p.2], Grounds 3-4 teach “*a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect.*”

34. [24.o.1] Fifth Signals

368. Claim 24 requires “*in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface.*”

369. As explained above (¶¶122-123), “*fifth signals associated with the second set of C/A signals*” in claim 24 is indefinite and lacks written description because it refers to “*the second set of C/A signals*” for a write operation in a claim element that requires a “*response to the third set of C/A signals*” for a read operation. However, Netlist’s infringement contentions in the district court litigation appear to interpret the “*fifth signal*” as associated with the “*third set of C/A signals,*” meaning associated with a read operation instead of a write operation. See EX1089 at 151 (citing prior infringement analysis from claim 1 and

referring to RDQS signal). Using Netlist's interpretation of this limitation, the "*fifth signals*" correspond to read "*data signals*" from one of "*the second plurality of DRAM dies*."

370. Using Netlist's interpretation of Claim 24, the prior art references in each of Grounds 3 and 4 teach limitation [24.o.1] for the same reasons described in limitations [1.b.1], [1.c.1], [1.d.1], [1.d.2], [1.e.3] and [1.e.4]:

Claim 1	Claim 24
[1.b.1] ... a second plurality of DRAM dies [1.c.1] ... data signals ... [1.d.1] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, [1.d.2] the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, [1.e.3] the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, [1.e.4] the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;	[24.o.1] in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and

371. Accordingly, the prior art references in each of Grounds 3 and 4 teach
“in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth

signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface.”

35. [24.o.2] Sixth Signals

372. Claim 24 requires “*a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface.*”

373. For the same reasons discussed above, *supra* ¶¶363, “*a second subset of the third die interconnect*” is indefinite because the singular term cannot have a “subset” and is not properly introduced. However, Netlist’s infringement contentions in the district court litigation appear to interpret this limitation as “*a second subset of the third die interconnect[s]*” (plural). See EX1089 at 149 (citing prior infringement analysis from claim 1 and referring to RDQS signal). Using Netlist’s interpretation of this limitation, it corresponds to “*first unidirectional interconnects*” of the “*second plurality of DRAM dies*” in claim 1.

374. As explained above (¶¶122, 124), “*one or more sixth signals associated with the second set of C/A signals*” in claim 24 is indefinite and lacks written description because it refers to “*the second set of C/A signals*” for a write operation and requires “*driv[ing] the one or more sixth signals to the interface,*” but no signal associated with a write operation is disclosed being sent from the

memory to the interface. Furthermore, claim element [24.s.4] requires that “*the sixth signals [are] driven by ... the second conduits in response to the fourth set of C/A signals*” contrary to the limitations of [24.o.2]. This limitation is also inconsistent with [25.d], associating the “*sixth signals*” with “*the third set of C/A signals.*” However, Netlist’s infringement contentions in the district court litigation appear to interpret the “*one or more sixth signals*” as associated with the “*third set of C/A signals,*” meaning associated with a read operation instead of a write operation. See EX1089 at 151 (citing prior infringement analysis from claim 1 and referring to RDQS signal). Using Netlist’s interpretation of this limitation, the “*one or more sixth signals*” correspond to “*signals*” analogous to “*first signals associated with the memory read operation*” in claim 1 but from one of “*the second plurality of DRAM dies.*”

375. Using Netlist’s interpretation of Claim 24, the prior art references in each of Grounds 3 and 4 teach limitation [24.o.2] for the same reasons described in limitations [1.b.1], [1.e.2], [1.l] and [1.p.1]:

Claim 1	Claim 24
[1.b.1] ... a second plurality of DRAM dies, [1.e.2] the control die including conduits ... [1.f] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies; [1.p.1] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and	[24.o.2] a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;

376. Accordingly, the prior art references in each of Grounds 3 and 4 teach
“a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface.”

36. [24.p.2] Eighth Signals

377. Claim 24 requires *“a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect.”*

378. For the same reasons discussed above, *supra* ¶363, “*a second subset of the fourth die interconnect*” is indefinite because the singular term cannot have a “subset” and is not properly introduced. However, Netlist’s infringement contentions in the district court litigation appear to interpret this limitation as “*a second subset of the fourth die interconnect[s]*” (plural). See EX1089 at 152 (citing prior infringement analysis from claim 1 and referring to WDQS signal). Using Netlist’s interpretation of this limitation, it corresponds to “*second unidirectional interconnects*” of the “*second plurality of DRAM dies*” in claim 1.

379. As explained above (¶¶122, 125), “*one or more eighth signals associated with the second set of C/A signals*” in claim 24 are indefinite and lack written description, because here these signals are associated with “*the second set of C/A signals*” but claim element [25.e] associates “*the one or more eighth signals*” with “*the fourth set of C/A signals.*” However, Netlist’s infringement contentions in the district court litigation appear to interpret “*second set of C/A signals*” as interchangeable with the “*fourth set of C/A signals.*” See EX1089 at 152 (citing prior infringement analysis from claim 1 and referring to WDQS signal). Using Netlist’s interpretation of this limitation, the “*one or more eighth signals*” correspond to “*signals*” analogous to “*second signals associated with the memory write operation*” in claim 1, but to one of “*the second plurality of DRAM dies.*”

380. Using Netlist’s interpretation of Claim 24, the prior art references in each of Grounds 3 and 4 teach limitation [24.p.2] for the same reasons described in limitations [1.b.1], [1.e.2], [1.m] and [1.p.2]:

Claim 1	Claim 24
[1.b.1] ... a second plurality of DRAM dies ... [1.e.2] the control die including conduits ... [1.m] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured [to] conduct any signal from any of the stacked DRAM dies to the control die; [1.p.2] in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.	[24.p.2] a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect;

381. Accordingly, the prior art references in each of Grounds 3 and 4 teach “a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect.”

37. [24.q] Distinct Conduits

382. Claim 24 requires “*each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits.*”

383. As shown in the table below, claim element [24.q] is very similar to claim elements [1.e.3], [1.j], [1.l] and [1.m]:

Claim 1	Claim 24
[1.e.3] the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, [1.j] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal; [1.l] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies; [1.m] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;	[24.q] each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

384. Furthermore, Keeth discloses that the odd and even dies in the stack can be operated independently, *see supra* ¶¶227-228, and a Skilled Artisan would have understood that such independent operations require distinct “conduits” for the corresponding signals. EX1047 (Keeth) at 5:63-6:10 (“By interleaving the conductive paths in the dice stack 502, the interface die 510 may access each die

(or a partition of each die) independently of the die above or below, and the interface die 510 may concurrently access dice 520 through 523, thereby increasing bandwidth. For example, apparatus 500 may access both I/O circuits 540 and 541 of dice 520 and 521 concurrently from the interface die 510 to reduce the possibility of queuing data, and perhaps resulting in increasing bandwidth. Similarly, in some embodiments, the command circuits and/or address circuits of each dice 520 through 523 may be connected to and utilize the interleaving conductive paths 505 through 508 in order to communicate command and/or address signals between the interface die and dice 520 through 523 which may perhaps increase bandwidth and reduce queuing of signals.”). Thus, for the same reasons as with claim elements [1.e.3], [1.j], [1.l] and [1.m], Grounds 3-4 teach “*each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits.*”

38. [24.s.3] Fifth Signals Including 32 Signals

385. Claim 24 requires “*the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel.*”

386. The “*fifth signals*” term is indefinite and lack written description for the reasons discussed above. *Supra*, ¶¶ 122-123, 369. However, if “*fifth signals*”

is interpreted consistent with Netlist's infringement contentions (as discussed above, *supra*, ¶ 369), then claim limitation [24.s.3] is substantially similar to claim 5 as shown by the comparison below, and thus obvious for the reasons already given for the claim:

Claim 5	Claim 24
[5] The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.	[24.s.3] the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

387. As explained above, under Netlist's interpretation the "*fifth signals*" in Claim 24 correspond to read "*data signals*" from one of "*the second plurality of DRAM dies.*" *Supra*, ¶ 369. Thus, for the same reasons discussed above with reference to Claim 5, *supra* ¶¶275-282, the prior art references in Grounds 3-4 satisfy "*the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel.*" *See supra* ¶¶ 275-282.

39. [24.s.4] Sixth Signals Including 32 Signals

388. Claim 24 requires “*the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.*”

389. The “*sixth signals*” term is indefinite and lack written description for the reasons discussed above. *Supra*, ¶¶ 122, 124, 374. However, if “*sixth signals*” is interpreted consistent with Netlist’s infringement contentions (as discussed above, *supra*, ¶ 374), then claim limitation [24.s.4] is substantially similar to claim 5 as shown by the comparison below, and thus obvious for the reasons already given for the claim:

Claim 5	Claim 24
[5] The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.	[24.s.4] the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

390. As explained above, under Netlist’s interpretation, the “*sixth signals*” correspond to “*signals*” analogous to “*first signals associated with the memory read operation*” in claim 1 but from one of “*the second plurality of DRAM dies.*”

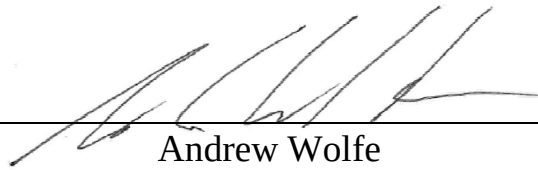
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in claim 1. *Supra*, ¶ 374. Thus, for the same reasons discussed above with reference to Claim 5, *supra* ¶¶275-282, the prior art references in Grounds 3-4 satisfy “*the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel.*” See *supra* ¶¶ 275-282.

* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 23, 2025



Andrew Wolfe

EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 12,308,087
1002	File History of U.S. Patent No. 12,308,087 (Application No. 17/694,649), <i>available at</i> "><https://patentcenter.uspto.gov/applications/17694649/ifw/docs?application=>
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 61/409,893 (filed Nov. 3, 2010)
1006	File History of U.S. Patent Application No. 14/337,168 (filed July 21, 2014)
1007	File History of U.S. Patent Application No. 15/095,288 (filed Apr. 11, 2016)
1008	File History of U.S. Patent Application No. 15/602,099 (filed May 22, 2017)
1009	File History of U.S. Patent Application No. 16/412,308 (filed May 14, 2019)
1010	File History of U.S. Patent Application No. 17/157,903 (filed Jan. 25, 2021)
1011	U.S. Patent Application Publication No. 2008/0025137 to Rajan <i>et al.</i> (published Jan. 31, 2008)
1012	U.S. Patent Application Publication No. 2011/0193226 to Kirby <i>et al.</i> (filed Feb. 8, 2010, published Aug. 11, 2011)
1013	U.S. Patent Application Publication No. 2006/0259678 to Gervasi (published Nov. 16, 2006)
1014	U.S. Patent Application Publication No. 2011/0103156 to Kim <i>et al.</i> (filed Dec. 29, 2009, published May 5, 2011)
1015	U.S. Patent No. 8,041,881 to Rajan <i>et al.</i> (filed June 12, 2007, issued Oct. 18, 2011)
1016	U.S. Patent Application Publication No. 2011/0026293 to Riho (filed July 16, 2010, published Feb. 3, 2011)

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Exhibit #	Description
1017	U.S. Patent No. 7,969,192 to Wyman <i>et al.</i> (filed Mar. 26, 2010, issued June 28, 2011)
1018	U.S. Patent Application Publication No. 2010/0195364 to Riho (published Aug. 5, 2010) (“Riho2”)
1019	JEDEC DDR3 SDRAM Standard, JESD79-3C (Nov. 2008)
1020	Declaration of Julie Carlson for JESD79-3C
1021	JEDEC MO-207, Square & Rectangular Die-Size, Ball Grid Array Family (Dec. 2010)
1022	Bruce Jacob <i>et al.</i> , <u>Memory Systems: Cache, DRAM, Disk</u> (2008)
1023	Bruce Jacob, <i>Synchronous DRAM Architectures, Organizations, and Alternative Technologies</i> (Dec. 10, 2002)
1024	U.S. Patent No. 7,796,446 to Ruckerbauer <i>et al.</i> (issued Sept. 14, 2010)
1025	U.S. Patent No. 8,258,619 to Foster <i>et al.</i> (filed Nov. 12, 2009)
1026	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry <i>et al.</i> (published Dec. 7, 2006)
1027	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (Final Written Decision)
1028	U.S. Patent No. 7,289,386 to Bhakta <i>et al.</i> (issued Oct. 30, 2007)
1029	Affirmance of the Examiner’s Decision on Reexamination of the ’386 Patent (Feb. 25, 2015)
1030	Stephen Brown <i>et al.</i> , <i>Fundamentals of Digital Logic</i> (2d ed. 2008)
1031	U.S. Patent No. 7,532,537 to Solomon <i>et al.</i> (issued May 12, 2009)
1032	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00667, Paper No. 38 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1033	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00668, Paper No. 36 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1034	U.S. Patent No. 8,471,362 to Lee (filed Apr. 5, 2011)

Declaration of Dr. Andrew Wolfe Regarding U.S. Patent No. 12,308,087

Exhibit #	Description
1035	JEDEC Graphics Double Data (GDDR4) SGRAM Specification (Nov. 2005), <i>available at</i> https://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm , https://web.archive.org/web/20081031052145/http://www.jedec.org/download/search/3_11_05_08R16A.pdf >
1036	JEDEC Graphics Double Data (GDDR3) Specific SGRAM Functions (May 2005), <i>available at</i> https://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm , https://www.jedec.org/standards-documents/docs/sdram-3110507 >
1037	U.S. Patent No. 7,890,811 to Rothman <i>et al.</i> (filed June 29, 2007, issued Feb. 15, 2011)
1038	Harold S. Stone, <i>Microcomputer Interfacing</i> (1982)
1039	U.S. Patent No. 9,160,349 to Ma (filed Aug. 27, 2009)
1040	GDDR5 SGRAM 1Gb (32Mx32) datasheet (Nov. 2009), <i>available at</i> https://web.archive.org/web/20101228025544/http://hynix.com/datasheet/eng/graphics/details/graphics_26_H5GQ1H24AFR.jsp?menu1=01&menu2=04&menu3=05&menuNo=1&m=3&s=4&RK=26 , https://web.archive.org/web/20101125165921/http://hynix.com/inc/pdfDownload.jsp?path=/datasheet/pdf/graphics/H5GQ1H24AFR(Rev1.0).pdf >
1041	U.S. Patent No. 8,120,958 to Bigler <i>et al.</i> (filed Dec. 24, 2007)
1042	Transcript of deposition of Andrew Wolfe, Ph.D. (June 27–28, 2023) (EX2025 in IPR2022-01427 and -01428)
1043	U.S. Patent No. 8,593,899 to Ide (filed Feb. 28, 2011, issued Nov. 26, 2013)
1044	Amended Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)
1045	U.S. Patent No. 8,244,971 to Rajan <i>et al.</i> (filed Oct. 30, 2007, issued Aug. 14, 2012)
1046	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
1047	U.S. Patent No. 9,123,552 to Keeth <i>et al.</i> (filed Mar. 30, 2010, issued Sept. 1, 2015)

Declaration of Dr. Andrew Wolfe Regarding U.S. Patent No. 12,308,087

Exhibit #	Description
1048	U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> (provisional filed July 22, 2010, nonprovisional filed May 11, 2011, issued May 30, 2017)
1049	Provisional Application No. 61/366,806 (filed July 22, 2010) to U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> , available at https://patentcenter.uspto.gov/applications/61366806/ifw/docs?application= >
1050	Application No. 13/105,798 (filed May 11, 2011) to U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> , available at https://patentcenter.uspto.gov/applications/13105798/ifw/docs?application= >
1051	U.S. Patent No. 7,664,216 to Schnarr (issued Feb. 16, 2010)
1052	Transcript of deposition of Michael C. Brogioli, Ph.D. (Sept. 27–28, 2023) in IPR2022-01427 and -01428
1053	U.S. Patent No. 8,243,486 to Riho (filed Feb. 1, 2010, published Aug. 5, 2010 [EX1018], issued Aug. 14, 2012) (“Riho2”)
1054	Netlist’s Technology Tutorial
1055	JEDEC JESD79 Standard for Double Data Rate (DDR) SDRAM (June 2000)
1056	Loi <i>et al.</i> , <i>An efficient distributed memory interface for many-core platform with 3D stacked DRAM</i> , Design, Automation & Test in Europe Conference & Exhibition (2010), available at https://ieeexplore.ieee.org/document/5457230 >
1057	U.S. Patent No. 7,286,436 to Bhakta <i>et al.</i> (filed March 7, 2005)
1058	U.S. Patent No. 7,619,912 to Bhakta <i>et al.</i> (effectively filed July 1, 2005)
1059	U. Kang <i>et al.</i> , <i>8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology</i> , IEEE Journal of Solid-State Circuits (Jan. 2010), available at https://ieeexplore.ieee.org/document/5357550 >
1060	U.S. Patent Application Publication No. 2010/0110748 A1 to Best (filed Apr. 17, 2008)
1061	Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00418, Paper 30 (PTAB Aug. 28, 2023) (U.S. Patent No. 8,301,833)
1062	U.S. Patent No. 7,024,518 to Halbert <i>et al.</i> (issued Apr. 4, 2006)

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Exhibit #	Description
1063	Dictionary definition for “electrical”
1064	Dictionary definition for “communication”
1065	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 45 (PTAB Oct. 18, 2023)
1066	Claim Construction Order, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00203, ECF No. 249 (E.D. Tex. Oct. 22, 2023)
1067	Petitioner’s Demonstratives for Oral Argument on January 11, 2024
1068	Claim Construction Order, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463, ECF No. 114 (E.D. Tex. Dec. 14, 2022) (EX2004 in IPR2022-01427 and -01428)
1069	U.S. Patent No. 8,787,060 (issued July 22, 2014)
1070	File History of U.S. Patent No. 8,787,060 (Application No. 13/288,850 filed Nov. 3, 2011)
1071	U.S. Patent No. 9,318,160 (issued Apr. 19, 2016)
1072	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01428, Paper 48 (PTAB Apr. 1, 2024) (U.S. Patent No. 8,787,060)
1073	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01427, Paper 48 (PTAB Apr. 1, 2024) (U.S. Patent No. 9,318,160)
1074	Order Denying Director Review, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01427 and -01428, Paper 52 (PTAB June 17, 2024)
1075	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-2241 (Fed. Cir. Aug. 20, 2024) (appeal from IPR2022-01428 of U.S. Patent No. 8,787,060)
1076	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-2240 (Fed. Cir. Aug. 20, 2024) (appeal from IPR2022-01427 of U.S. Patent No. 9,318,160)
1077	Samsung’s Principal Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. Dec. 16, 2024)
1078	Netlist’s Responsive Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. Mar. 28, 2025)

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Exhibit #	Description
1079	Samsung's Reply Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. May 19, 2025)
1080	U.S. Patent No. 7,545,663 to Ikeda <i>et al.</i> (issued June 9, 2009)
1081	Micron datasheet for 2Gb: x16, x32 Mobile LPDDR SDRAM (Nov. 2010), available at https://web.archive.org/web/20101225095025/http://www.micron.com/products/ProductDetails.html?product=products/dram/mobile_lp_dram/MT46H128M16LFCK-5+IT
1082	JEDEC Ballot for 3D Stacked DDR3 SDRAM Addressing, Item No. 1655.10 (Sept. 2010)
1083	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00553 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)
1084	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:25-cv-00552 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)
1085	Complaint in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1086	Complaint in <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1087	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00557 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1088	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:25-cv-00558 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1089	Netlist's infringement contentions against Samsung in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00557 (E.D. Tex. July 16, 2025) (U.S. Patent No. 12,308,087)
1090	[omitted]
1091	Declaration of Dr. Andrew Wolfe in IPR2022-01427 (EX1003 in IPR2022-01427)
1092	Declaration of Dr. Andrew Wolfe in IPR2022-01428 (EX1003 in IPR2022-01428)

Declaration of Dr. Andrew Wolfe Regarding U.S. Patent No. 12,308,087

Exhibit #	Description
1093	Invalidity claim chart by Dr. Andrew Wolfe

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A dynamic random access memory (DRAM) package, comprising:
1.b.1	stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies,
1.b.2	each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
1.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,
1.c.2	wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;
1.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
1.d.2	the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals,
1.d.3	each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;
1.e.1	a control die coupled between the terminals and the stacked DRAM dies,
1.e.2	the control die including conduits, the conduits including C/A conduits and data conduits,
1.e.3	the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects,

Ref. #	Listing of Challenged Claims
1.e.4	the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;
1.f	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;
1.g	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;
1.h.1	wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies,
1.h.2	each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies,
1.h.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;
1.i	wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;
1.j	wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

Ref. #	Listing of Challenged Claims
1.k.1	wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals,
1.k.2	wherein the one or more C/A signals do not include any chip select signal;
1.l	wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;
1.m	wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die;
1.n	wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;
1.o	wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and
1.p.1	wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and
1.p.2	in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.
2	The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

Ref. #	Listing of Challenged Claims
3	The DRAM package of claim 2, wherein the stacked DRAM dies include 16 stacked DRAM dies.
4.a	The DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and
4.b	the second driver size is different from the first driver size.
5	The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.
6.a	The DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and
6.b	the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;
6.c	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.
7	The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.
8	The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.
9.a	A method, comprising:

Ref. #	Listing of Challenged Claims
9.b.1	at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports,
9.b.2	the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals,
9.b.3	the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies,
9.b.4	the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects,
9.c	receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;
9.d.1	in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and
9.d.2	receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

Ref. #	Listing of Challenged Claims
9.e.1	in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and
9.e.2	driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;
9.f.1	wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies,
9.f.2	each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies,
9.f.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;
9.g	wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;
9.h	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

Ref. #	Listing of Challenged Claims
9.i	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;
9.j.1	wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and
9.j.2	the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies;
9.k	wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and
9.l	wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.
10	The method of claim 9, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
11	The method of claim 9, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.
12.a	The method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:
12.b	enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;
12.c	enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and
12.d	maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;
12.e	wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.
13.a	A dynamic random access memory (DRAM) package, comprising:

Ref. #	Listing of Challenged Claims
13.b	a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;
13.c	an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals;
13.d	die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and
13.e	a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;
13.f	wherein: the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;
13.g	each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;
13.h.1	each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies,
13.h.2	each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

Ref. #	Listing of Challenged Claims
13.i	the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects;
13.j	a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies;
13.k	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;
13.l	the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;
13.m	the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;
13.n	the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;

Ref. #	Listing of Challenged Claims
13.o	the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;
13.p	the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;
13.q	the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;
13.r	the control die is configurable to drive the one or more second signals to the second DRAM die one or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;
13.s	each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;
13.t	a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and
13.u	each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.
14	The DRAM package of claim 13, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.

Ref. #	Listing of Challenged Claims
15	The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.
16	The DRAM package of claim 13, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.
17.a.1	The DRAM package of claim 13, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects,
17.a.2	wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:
17.b	the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;
17.c	the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;
17.d	each of the first data conduits are placed in a non-driving state after driving the first data signals;
17.e	each of the second data conduits are placed in a non-driving state after driving the second data signals; and
17.f	data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.
18.a.1	The DRAM package of claim 13, wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits,

Ref. #	Listing of Challenged Claims
18.a.2	wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.
19	The DRAM package of claim 13, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel.
20.a	A dynamic random access memory (DRAM) package, comprising:
20.b	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
20.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals,
20.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;
20.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
20.d.2	the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,

Ref. #	Listing of Challenged Claims
20.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and
20.e.1	a control die coupled between the terminals and the stacked DRAM dies,
20.e.2	the control die including conduits coupled to respective ones of the die interconnects;
20.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,
20.f.2	the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;
20.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;
20.h.1	wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,
20.h.2	wherein the one or more C/A signals do not include any chip select signal;
20.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;
20.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;

Ref. #	Listing of Challenged Claims
20.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and
20.l.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and
20.l.2	wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;
20.m	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.
21	The DRAM package of claim 20, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
22.a	The DRAM package of claim 20, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and
22.b	the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.
23.a	A dynamic random access memory (DRAM) package, comprising:
23.b	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
23.c.1	terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,

Ref. #	Listing of Challenged Claims
23.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;
23.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
23.d.2	the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,
23.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and
23.e.1	a control die coupled between the terminals and the stacked DRAM dies,
23.e.2	the control die including conduits coupled to respective ones of the die interconnects;
23.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,
23.f.2	the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;
23.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

Ref. #	Listing of Challenged Claims
23.h.1	wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,
23.h.2	wherein the one or more C/A signals do not include any chip select signal;
23.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;
23.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;
23.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects;
23.l.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and
23.l.2	wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;
23.m.1	wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and
23.m.2	wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and
23.n	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

Ref. #	Listing of Challenged Claims
24.a	A dynamic random access memory (DRAM) package, comprising:
24.b	stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;
24.c	an interface via which the DRAM package receives C/A signals and receives or outputs data signals;
24.d.1	a control die coupled between the interface and the stacked DRAM dies,
24.d.2	the control die including signal conduits and logic configured to control at least some of the signal conduits; and
24.e	die interconnects, each die interconnect of the die interconnects coupled between at least one corresponding conduit in the control die and one corresponding signal port in each of a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;
24.f	wherein: the signal conduits include first conduits, second conduits, third conduits and fourth conduits;
24.g	the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;
24.h	each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;
24.i	each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;
24.j	each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

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24.k	each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;
24.l	the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;
24.m.1	in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and
24.m.2	a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;
24.n.1	in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and
24.n.2	a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;
24.o.1	in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and

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24.o.2	a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;
24.p.1	in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and
24.p.2	a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect;
24.q	each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;
24.r	each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;
24.s.1	the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;
24.s.2	the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;
24.s.3	the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and
24.s.4	the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

Ref. #	Listing of Challenged Claims
25.a.1	The DRAM package of claim 24, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of a first subset of DRAM dies and not in electrical communication with any signal port of any of the second subset of DRAM dies,
25.a.2	wherein each of the second subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of the second subset of DRAM dies and not in electrical communication with any signal port of any of the first subset of DRAM dies, and wherein:
25.b	the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;
25.c	the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;
25.d	the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals;
25.e	the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals;
25.f	the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and
25.g	the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.
26.a.1	The DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals,

Ref. #	Listing of Challenged Claims
26.a.2	wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:
26.b	the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;
26.c	the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and
26.d	the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;
26.e	a conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.
27	The DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
28	The DRAM package of claim 27, wherein the stacked DRAM dies include 16 stacked DRAM dies.