

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Case IPR2025-01402

Patent 12,308,087

**PETITION FOR INTER PARTES REVIEW OF
U.S. PATENT NO. 12,308,087**

TABLE OF CONTENTS

	Page
I. PETITIONER’S MANDATORY NOTICES	1
A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))	1
B. Related Matters (37 C.F.R. § 42.8(b)(2)).....	1
C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3)).....	3
D. Service Information (37 C.F.R. § 42.8(b)(4))	3
II. INTRODUCTION	3
III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR POST GRANT REVIEW	4
A. Standing (§42.104(a)).....	4
B. Identification of Challenge (§42.104(b))	4
IV. BACKGROUND ON THE ’087 PATENT.....	4
A. The ’087 Patent	4
1. Technical Overview	4
2. Prosecution History.....	7
B. Estoppel from IPRs against the related 160 and 060 Patents.....	8
C. Person of Ordinary Skill in the Art (“Skilled Artisan” or “POSITA”)	9
V. CLAIM CONSTRUCTION.....	10
VI. ARGUMENT.....	11
A. Grounds 3 and 4 (all claims are obvious).....	11
1. Overview of the prior art.....	11
a) <u>Keeth</u> (EX1047).....	11
b) <u>Shaeffer</u> (EX1048).....	12
c) <u>Riho2</u> (EX1018).....	14
2. Ground 3 combination: Keeth (EX1047) and Shaeffer (EX1048).....	15
3. Ground 4 combination: Ground 3 further in view of Riho2 (EX1018).....	24
4. Claim 1	28

a)	[1.a]-[1.b.1] Stacked DRAM dies.....	28
b)	[1.b.2] C/A and data ports and DRAM memory cells	30
c)	[1.c.1] Terminals.....	34
d)	[1.c.2] First/second data signals	37
e)	[1.d.1] C/A interconnects.....	38
f)	[1.d.2] Data interconnects.....	42
g)	[1.d.3] TSVs.....	45
h)	[1.e.1] Control die.....	47
i)	[1.e.2] Conduits	49
j)	[1.e.3] C/A conduits.....	51
k)	[1.e.4] Data conduits.....	52
l)	[1.f] First C/A interconnect and electrical communication	52
m)	[1.g] Second C/A interconnect and electrical communication	54
n)	[1.h.1] First data interconnect and electrical communication	55
o)	[1.h.2] TSVs in first data interconnects.....	57
p)	[1.h.3] TSVs and electrical communication.....	59
q)	[1.i] Second data interconnect and electrical communication	61
r)	[1.j] First/second conduit.....	62
s)	[1.k.1] control logic	64
t)	[1.k.2] no chip select signal	65
u)	[1.l] first unidirectional interconnects	67
v)	[1.m] second unidirectional interconnects.....	70
w)	[1.n] control die and first unidirectional interconnects	72
x)	[1.o] control die and second unidirectional interconnects	74
y)	[1.p.1] First signals	75

	z) [1.p.2] Second signals.....	78
5.	Claim 2.....	79
6.	Claim 3.....	80
7.	Claim 4.....	80
	a) [4.a] First/second driver.....	80
	b) [4.b] Different driver size	82
8.	Claim 5.....	83
9.	Claim 6.....	86
	a) [6.a] First set of C/A signals including a chip select signal.....	86
	b) [6.b] Second set of C/A signals including a chip select signal.....	87
	c) [6.c] No emulation logic.....	88
10.	Claim 7.....	88
11.	Claim 8.....	91
12.	Claims 9-11	92
13.	Claim 12.....	95
	a) [12.a] Consecutive C/A signals	95
	b) [12.b]-[12.c] First/second drivers	96
	c) [12.d] Non-driving state	97
	d) [12.e] Not to receive or drive any signal	99
14.	Claims 13-22	99
15.	Claim 23.....	105
	a) [23.c.1] Power supply terminals.....	106
	b) [23.m.1] first supply voltage interconnect.....	107
	c) [23.m.2] second supply voltage interconnect.....	110
16.	Claims 24-28.....	110
VII.	CONCLUSION	121

TABLE OF AUTHORITIES

Page(s)

Cases

<i>Beable Educ., Inc. v. Achieve3000, Inc.</i> , IPR2021-01169, Paper 34 (PTAB Jan. 3, 2023), <i>aff'd</i> , No. 23-1605 (Fed. Cir. July 10, 2024).....	102
<i>In re Riggs</i> , 131 F.4th 1377 (Fed. Cir. 2025).....	13
<i>Mobile Tech, Inc. v. InVue Security Prods. Inc.</i> , IPR2018-00481, Paper 29 (PTAB July 16, 2019).....	9
<i>SoftView LLC v. Apple Inc.</i> , 108 F.4th 1366 (Fed. Cir. 2024).....	9

Statutes

35 U.S.C. § 102(a) (pre-AIA)	11, 14
35 U.S.C. § 102(e) (pre-AIA)	11, 12

Regulations

37 C.F.R § 42.8(b)(1).....	1
37 C.F.R § 42.8(b)(2).....	1
37 C.F.R. § 42.100(b)	10
37 C.F.R. § 42.104(a).....	4
37 C.F.R. § 42.104(b)	4
37 C.F.R. § 42.73(d)(3).....	8
37 C.F.R. § 42.73(d)(3)(i)	8
37 C.F.R. § 42.8(b)(3).....	3
37 C.F.R. § 42.8(b)(4).....	3

EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 12,308,087
1002	File History of U.S. Patent No. 12,308,087 (Application No. 17/694,649), <i>available at</i> https://patentcenter.uspto.gov/applications/17694649/ifw/docs?application= >
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 61/409,893 (filed Nov. 3, 2010)
1006	File History of U.S. Patent Application No. 14/337,168 (filed July 21, 2014)
1007	File History of U.S. Patent Application No. 15/095,288 (filed Apr. 11, 2016)
1008	File History of U.S. Patent Application No. 15/602,099 (filed May 22, 2017)
1009	File History of U.S. Patent Application No. 16/412,308 (filed May 14, 2019)
1010	File History of U.S. Patent Application No. 17/157,903 (filed Jan. 25, 2021)
1011	U.S. Patent Application Publication No. 2008/0025137 to Rajan <i>et al.</i> (published Jan. 31, 2008)
1012	U.S. Patent Application Publication No. 2011/0193226 to Kirby <i>et al.</i> (filed Feb. 8, 2010, published Aug. 11, 2011)
1013	U.S. Patent Application Publication No. 2006/0259678 to Gervasi (published Nov. 16, 2006)
1014	U.S. Patent Application Publication No. 2011/0103156 to Kim <i>et al.</i> (filed Dec. 29, 2009, published May 5, 2011)
1015	U.S. Patent No. 8,041,881 to Rajan <i>et al.</i> (filed June 12, 2007, issued Oct. 18, 2011)
1016	U.S. Patent Application Publication No. 2011/0026293 to Riho (filed July 16, 2010, published Feb. 3, 2011)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

Exhibit #	Description
1017	U.S. Patent No. 7,969,192 to Wyman <i>et al.</i> (filed Mar. 26, 2010, issued June 28, 2011)
1018	U.S. Patent Application Publication No. 2010/0195364 to Riho (published Aug. 5, 2010) (“Riho2”)
1019	JEDEC DDR3 SDRAM Standard, JESD79-3C (Nov. 2008)
1020	Declaration of Julie Carlson for JESD79-3C
1021	JEDEC MO-207, Square & Rectangular Die-Size, Ball Grid Array Family (Dec. 2010)
1022	Bruce Jacob <i>et al.</i> , <u>Memory Systems: Cache, DRAM, Disk</u> (2008)
1023	Bruce Jacob, <i>Synchronous DRAM Architectures, Organizations, and Alternative Technologies</i> (Dec. 10, 2002)
1024	U.S. Patent No. 7,796,446 to Ruckerbauer <i>et al.</i> (issued Sept. 14, 2010)
1025	U.S. Patent No. 8,258,619 to Foster <i>et al.</i> (filed Nov. 12, 2009)
1026	U.S. Patent Application Publication No. 2006/0277355 to Ellsberry <i>et al.</i> (published Dec. 7, 2006)
1027	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (Final Written Decision)
1028	U.S. Patent No. 7,289,386 to Bhakta <i>et al.</i> (issued Oct. 30, 2007)
1029	Affirmance of the Examiner’s Decision on Reexamination of the ’386 Patent (Feb. 25, 2015)
1030	Stephen Brown <i>et al.</i> , <i>Fundamentals of Digital Logic</i> (2d ed. 2008)
1031	U.S. Patent No. 7,532,537 to Solomon <i>et al.</i> (issued May 12, 2009)
1032	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00667, Paper No. 38 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1033	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00668, Paper No. 36 (PTAB July 18, 2018) (Final Written Decision for 537 Patent)
1034	U.S. Patent No. 8,471,362 to Lee (filed Apr. 5, 2011)

Exhibit #	Description
1035	JEDEC Graphics Double Data (GDDR4) SGRAM Specification (Nov. 2005), <i>available at</i> https://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm , https://web.archive.org/web/20081031052145/http://www.jedec.org/download/search/3_11_05_08R16A.pdf
1036	JEDEC Graphics Double Data (GDDR3) Specific SGRAM Functions (May 2005), <i>available at</i> https://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm , https://www.jedec.org/standards-documents/docs/sdram-3110507
1037	U.S. Patent No. 7,890,811 to Rothman <i>et al.</i> (filed June 29, 2007, issued Feb. 15, 2011)
1038	Harold S. Stone, <i>Microcomputer Interfacing</i> (1982)
1039	U.S. Patent No. 9,160,349 to Ma (filed Aug. 27, 2009)
1040	GDDR5 SGRAM 1Gb (32Mx32) datasheet (Nov. 2009), <i>available at</i> https://web.archive.org/web/20101228025544/http://hynix.com/datasheet/eng/graphics/details/graphics_26_H5GQ1H24AFR.jsp?menu1=01&menu2=04&menu3=05&menuNo=1&m=3&s=4&RK=26 , https://web.archive.org/web/20101125165921/http://hynix.com/inc/pdfDownload.jsp?path=/datasheet/pdf/graphics/H5GQ1H24AFR(Rev1.0).pdf
1041	U.S. Patent No. 8,120,958 to Bigler <i>et al.</i> (filed Dec. 24, 2007)
1042	Transcript of deposition of Andrew Wolfe, Ph.D. (June 27–28, 2023) (EX2025 in IPR2022-01427 and -01428)
1043	U.S. Patent No. 8,593,899 to Ide (filed Feb. 28, 2011, issued Nov. 26, 2013)
1044	Amended Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)
1045	U.S. Patent No. 8,244,971 to Rajan <i>et al.</i> (filed Oct. 30, 2007, issued Aug. 14, 2012)
1046	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
1047	U.S. Patent No. 9,123,552 to Keeth <i>et al.</i> (filed Mar. 30, 2010, issued Sept. 1, 2015)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

Exhibit #	Description
1048	U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> (provisional filed July 22, 2010, nonprovisional filed May 11, 2011, issued May 30, 2017)
1049	Provisional Application No. 61/366,806 (filed July 22, 2010) to U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> , available at https://patentcenter.uspto.gov/applications/61366806/ifw/docs?application= >
1050	Application No. 13/105,798 (filed May 11, 2011) to U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> , available at https://patentcenter.uspto.gov/applications/13105798/ifw/docs?application= >
1051	U.S. Patent No. 7,664,216 to Schnarr (issued Feb. 16, 2010)
1052	Transcript of deposition of Michael C. Brogioli, Ph.D. (Sept. 27–28, 2023) in IPR2022-01427 and -01428
1053	U.S. Patent No. 8,243,486 to Riho (filed Feb. 1, 2010, published Aug. 5, 2010 [EX1018], issued Aug. 14, 2012) (“Riho2”)
1054	Netlist’s Technology Tutorial
1055	JEDEC JESD79 Standard for Double Data Rate (DDR) SDRAM (June 2000)
1056	Loi <i>et al.</i> , <i>An efficient distributed memory interface for many-core platform with 3D stacked DRAM</i> , Design, Automation & Test in Europe Conference & Exhibition (2010), available at https://ieeexplore.ieee.org/document/5457230 >
1057	U.S. Patent No. 7,286,436 to Bhakta <i>et al.</i> (filed March 7, 2005)
1058	U.S. Patent No. 7,619,912 to Bhakta <i>et al.</i> (effectively filed July 1, 2005)
1059	U. Kang <i>et al.</i> , <i>8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology</i> , IEEE Journal of Solid-State Circuits (Jan. 2010), available at https://ieeexplore.ieee.org/document/5357550 >
1060	U.S. Patent Application Publication No. 2010/0110748 A1 to Best (filed Apr. 17, 2008)
1061	Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00418, Paper 30 (PTAB Aug. 28, 2023) (U.S. Patent No. 8,301,833)
1062	U.S. Patent No. 7,024,518 to Halbert <i>et al.</i> (issued Apr. 4, 2006)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

Exhibit #	Description
1063	Dictionary definition for “electrical”
1064	Dictionary definition for “communication”
1065	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 45 (PTAB Oct. 18, 2023)
1066	Claim Construction Order, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00203, ECF No. 249 (E.D. Tex. Oct. 22, 2023)
1067	Petitioner’s Demonstratives for Oral Argument on January 11, 2024
1068	Claim Construction Order, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463, ECF No. 114 (E.D. Tex. Dec. 14, 2022) (EX2004 in IPR2022-01427 and -01428)
1069	U.S. Patent No. 8,787,060 (issued July 22, 2014)
1070	File History of U.S. Patent No. 8,787,060 (Application No. 13/288,850 filed Nov. 3, 2011)
1071	U.S. Patent No. 9,318,160 (issued Apr. 19, 2016)
1072	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01428, Paper 48 (PTAB Apr. 1, 2024) (U.S. Patent No. 8,787,060)
1073	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01427, Paper 48 (PTAB Apr. 1, 2024) (U.S. Patent No. 9,318,160)
1074	Order Denying Director Review, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-01427 and -01428, Paper 52 (PTAB June 17, 2024)
1075	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-2241 (Fed. Cir. Aug. 20, 2024) (appeal from IPR2022-01428 of U.S. Patent No. 8,787,060)
1076	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-2240 (Fed. Cir. Aug. 20, 2024) (appeal from IPR2022-01427 of U.S. Patent No. 9,318,160)
1077	Samsung’s Principal Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. Dec. 16, 2024)
1078	Netlist’s Responsive Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. Mar. 28, 2025)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

Exhibit #	Description
1079	Samsung’s Reply Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. May 19, 2025)
1080	U.S. Patent No. 7,545,663 to Ikeda <i>et al.</i> (issued June 9, 2009)
1081	Micron datasheet for 2Gb: x16, x32 Mobile LPDDR SDRAM (Nov. 2010), available at < https://web.archive.org/web/20101225095025/http://www.micron.com/products/ProductDetails.html?product=products/dram/mobile_lp_dram/MT46H128M16LFCK-5+IT >
1082	JEDEC Ballot for 3D Stacked DDR3 SDRAM Addressing, Item No. 1655.10 (Sept. 2010)
1083	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00553 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)
1084	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:25-cv-00552 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)
1085	Complaint in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1086	Complaint in <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1087	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00557 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1088	Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:25-cv-00558 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
1089	Netlist’s infringement contentions against Samsung in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00557 (E.D. Tex. July 16, 2025) (U.S. Patent No. 12,308,087)
1090	[omitted]
1091	Declaration of Dr. Andrew Wolfe in IPR2022-01427 (EX1003 in IPR2022-01427)
1092	Declaration of Dr. Andrew Wolfe in IPR2022-01428 (EX1003 in IPR2022-01428)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

Exhibit #	Description
1093	Invalidity claim chart by Dr. Andrew Wolfe

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A dynamic random access memory (DRAM) package, comprising:
1.b.1	stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies,
1.b.2	each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
1.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,
1.c.2	wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;
1.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
1.d.2	the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals,
1.d.3	each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;
1.e.1	a control die coupled between the terminals and the stacked DRAM dies,
1.e.2	the control die including conduits, the conduits including C/A conduits and data conduits,
1.e.3	the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects,

Ref. #	Listing of Challenged Claims
1.e.4	the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;
1.f	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;
1.g	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;
1.h.1	wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies,
1.h.2	each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies,
1.h.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;
1.i	wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;
1.j	wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

Ref. #	Listing of Challenged Claims
1.k.1	wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals,
1.k.2	wherein the one or more C/A signals do not include any chip select signal;
1.l	wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;
1.m	wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die;
1.n	wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;
1.o	wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and
1.p.1	wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and
1.p.2	in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.
2	The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

Ref. #	Listing of Challenged Claims
3	The DRAM package of claim 2, wherein the stacked DRAM dies include 16 stacked DRAM dies.
4.a	The DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and
4.b	the second driver size is different from the first driver size.
5	The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.
6.a	The DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and
6.b	the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;
6.c	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.
7	The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.
8	The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.
9.a	A method, comprising:

Ref. #	Listing of Challenged Claims
9.b.1	at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports,
9.b.2	the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals,
9.b.3	the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies,
9.b.4	the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects,
9.c	receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;
9.d.1	in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and
9.d.2	receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

Ref. #	Listing of Challenged Claims
9.e.1	in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and
9.e.2	driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;
9.f.1	wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies,
9.f.2	each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies,
9.f.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;
9.g	wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;
9.h	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

Ref. #	Listing of Challenged Claims
9.i	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;
9.j.1	wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and
9.j.2	the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies;
9.k	wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and
9.l	wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.
10	The method of claim 9, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
11	The method of claim 9, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.
12.a	The method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:
12.b	enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;
12.c	enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and
12.d	maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;
12.e	wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.
13.a	A dynamic random access memory (DRAM) package, comprising:

Ref. #	Listing of Challenged Claims
13.b	a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;
13.c	an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals;
13.d	die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and
13.e	a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;
13.f	wherein: the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;
13.g	each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;
13.h.1	each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies,
13.h.2	each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

Ref. #	Listing of Challenged Claims
13.i	the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects;
13.j	a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies;
13.k	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;
13.l	the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;
13.m	the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;
13.n	the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;

Ref. #	Listing of Challenged Claims
13.o	the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;
13.p	the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;
13.q	the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;
13.r	the control die is configurable to drive the one or more second signals to the second DRAM die one or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;
13.s	each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;
13.t	a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and
13.u	each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.
14	The DRAM package of claim 13, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.

Ref. #	Listing of Challenged Claims
15	The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.
16	The DRAM package of claim 13, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.
17.a.1	The DRAM package of claim 13, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects,
17.a.2	wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:
17.b	the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;
17.c	the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;
17.d	each of the first data conduits are placed in a non-driving state after driving the first data signals;
17.e	each of the second data conduits are placed in a non-driving state after driving the second data signals; and
17.f	data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.
18.a.1	The DRAM package of claim 13, wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits,

Ref. #	Listing of Challenged Claims
18.a.2	wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.
19	The DRAM package of claim 13, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel.
20.a	A dynamic random access memory (DRAM) package, comprising:
20.b	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
20.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals,
20.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;
20.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
20.d.2	the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,

Ref. #	Listing of Challenged Claims
20.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and
20.e.1	a control die coupled between the terminals and the stacked DRAM dies,
20.e.2	the control die including conduits coupled to respective ones of the die interconnects;
20.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,
20.f.2	the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;
20.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;
20.h.1	wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,
20.h.2	wherein the one or more C/A signals do not include any chip select signal;
20.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;
20.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;

Ref. #	Listing of Challenged Claims
20.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and
20.l.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and
20.l.2	wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;
20.m	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.
21	The DRAM package of claim 20, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
22.a	The DRAM package of claim 20, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and
22.b	the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.
23.a	A dynamic random access memory (DRAM) package, comprising:
23.b	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;
23.c.1	terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,

Ref. #	Listing of Challenged Claims
23.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;
23.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,
23.d.2	the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,
23.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and
23.e.1	a control die coupled between the terminals and the stacked DRAM dies,
23.e.2	the control die including conduits coupled to respective ones of the die interconnects;
23.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,
23.f.2	the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;
23.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

Ref. #	Listing of Challenged Claims
23.h.1	wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,
23.h.2	wherein the one or more C/A signals do not include any chip select signal;
23.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;
23.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;
23.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects;
23.l.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and
23.l.2	wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;
23.m.1	wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and
23.m.2	wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and
23.n	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

Ref. #	Listing of Challenged Claims
24.a	A dynamic random access memory (DRAM) package, comprising:
24.b	stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;
24.c	an interface via which the DRAM package receives C/A signals and receives or outputs data signals;
24.d.1	a control die coupled between the interface and the stacked DRAM dies,
24.d.2	the control die including signal conduits and logic configured to control at least some of the signal conduits; and
24.e	die interconnects, each die interconnect of the die interconnects coupled between at least one corresponding conduit in the control die and one corresponding signal port in each of a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;
24.f	wherein: the signal conduits include first conduits, second conduits, third conduits and fourth conduits;
24.g	the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;
24.h	each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;
24.i	each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;
24.j	each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

Ref. #	Listing of Challenged Claims
24.k	each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;
24.l	the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;
24.m.1	in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and
24.m.2	a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;
24.n.1	in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and
24.n.2	a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;
24.o.1	in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and

Ref. #	Listing of Challenged Claims
24.o.2	a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;
24.p.1	in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and
24.p.2	a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect;
24.q	each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;
24.r	each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;
24.s.1	the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;
24.s.2	the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;
24.s.3	the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and
24.s.4	the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

Ref. #	Listing of Challenged Claims
25.a.1	The DRAM package of claim 24, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of a first subset of DRAM dies and not in electrical communication with any signal port of any of the second subset of DRAM dies,
25.a.2	wherein each of the second subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of the second subset of DRAM dies and not in electrical communication with any signal port of any of the first subset of DRAM dies, and wherein:
25.b	the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;
25.c	the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;
25.d	the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals;
25.e	the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals;
25.f	the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and
25.g	the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.
26.a.1	The DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals,

Ref. #	Listing of Challenged Claims
26.a.2	wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:
26.b	the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;
26.c	the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and
26.d	the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;
26.e	a conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.
27	The DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.
28	The DRAM package of claim 27, wherein the stacked DRAM dies include 16 stacked DRAM dies.

I. PETITIONER’S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 12,308,087.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, PGR2025-00071 (U.S. Patent No. 12,308,087)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-01427, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-00883, *appeal docketed*, No. 2024-2240 (Fed. Cir. Aug. 20, 2024) (U.S. Patent No. 9,318,160)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-01428, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-00882, *appeal docketed*, No. 2024-2241 (Fed. Cir. Aug. 20, 2024) (U.S. Patent No. 8,787,060)

Petition for Inter Partes Review of U.S. Patent No. 12,308,087

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex.), *appeal docketed*, No. 2024-2203 (Fed. Cir. Aug. 13, 2024) (U.S. Patent Nos. 8,787,060 and 9,318,160)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (U.S. Patent Nos. 8,787,060 and 9,318,160)
- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,308,087)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:25-cv-00557 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:25-cv-00558 (E.D. Tex. filed May 20, 2025) (U.S. Patent No. 12,308,087)
- U.S. Patent Application No. 19/212,638

The following proceedings are no longer pending:

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:25-cv-00553 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:25-cv-00552 (E.D. Tex. filed May 19, 2025) (U.S. Patent No. 12,308,087)

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is: Eliot D. Williams (Reg. No. 50,822),

DLSamsungNetlistIPRs@BakerBotts.com, (202) 639-1334, Baker Botts L.L.P.,
700 K Street, N.W., Washington, D.C. 20001.

Back-up Counsel are:

1) Theodore W. Chandler (Reg. No. 50,319),

DLSamsungNetlistIPRs@BakerBotts.com, (213) 202-5702

2) Ferenc Pazmandi (Reg. No. 66,216),

DLSamsungNetlistIPRs@BakerBotts.com, (415) 291-6255

3) Mark A. Speegle (Reg. No. 77,512),

DLSamsungNetlistIPRs@BakerBotts.com, (512) 322-2536

The fax number for lead and backup counsel is (202) 639-7890.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to

DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

If PGR2025-00071 is not instituted, then Petitioner respectfully requests trial in this IPR on claims 1-28 of U.S. Patent No. 12,308,087 (“’087 Patent”) (EX1001). See Paper No. 3 (ranking petitions).

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR POST GRANT REVIEW

A. Standing (§42.104(a))

If PGR2025-00071 is not instituted, then the '087 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the below-identified grounds.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-28 of the '087 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	Omitted in this IPR. See Paper No. 3 (ranking petitions).		
2			
3	1-28	103(a)	<u>Keeth</u> + <u>Shaeffer</u>
4	1-28	103(a)	Ground 3 + <u>Riho2</u>

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above starting on page vi.

IV. BACKGROUND ON THE '087 PATENT

A. The '087 Patent

1. Technical Overview

The '087 Patent relates to “a memory package having stacked array dies.” EX1001, 1:30-35. The '087 Patent admits as prior art “FIGS. 1A and 1B [which]

schematically illustrate examples of existing memory package designs.” EX1001, 1:46-48, 2:13-22, Fig.1B (below); EX1003, ¶¶60-61.¹

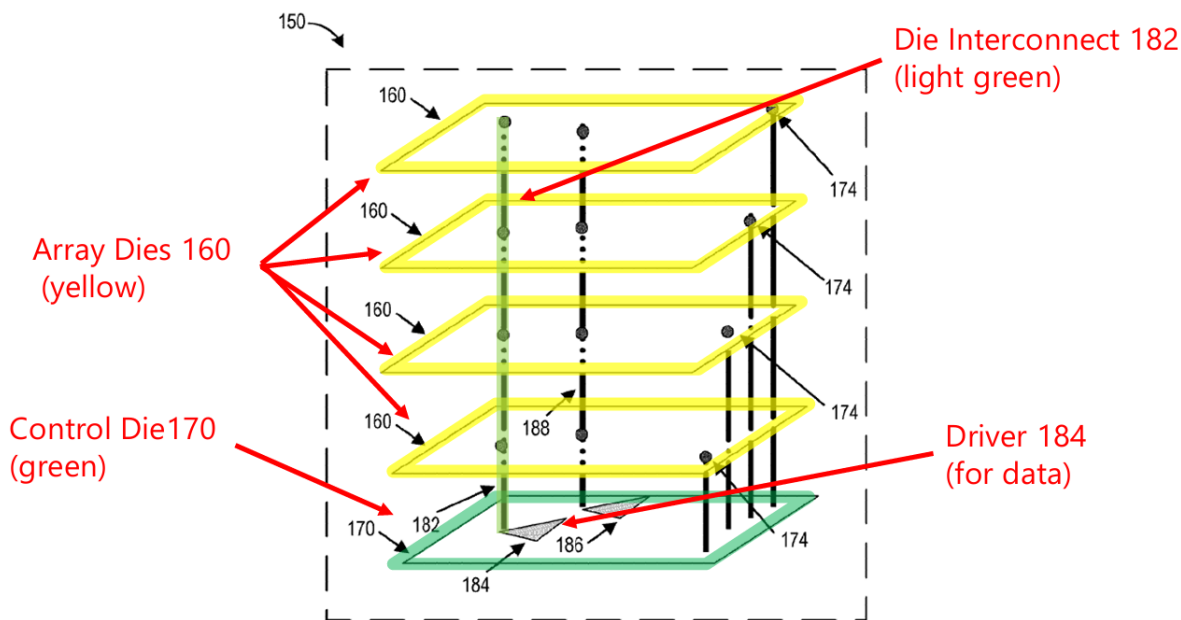
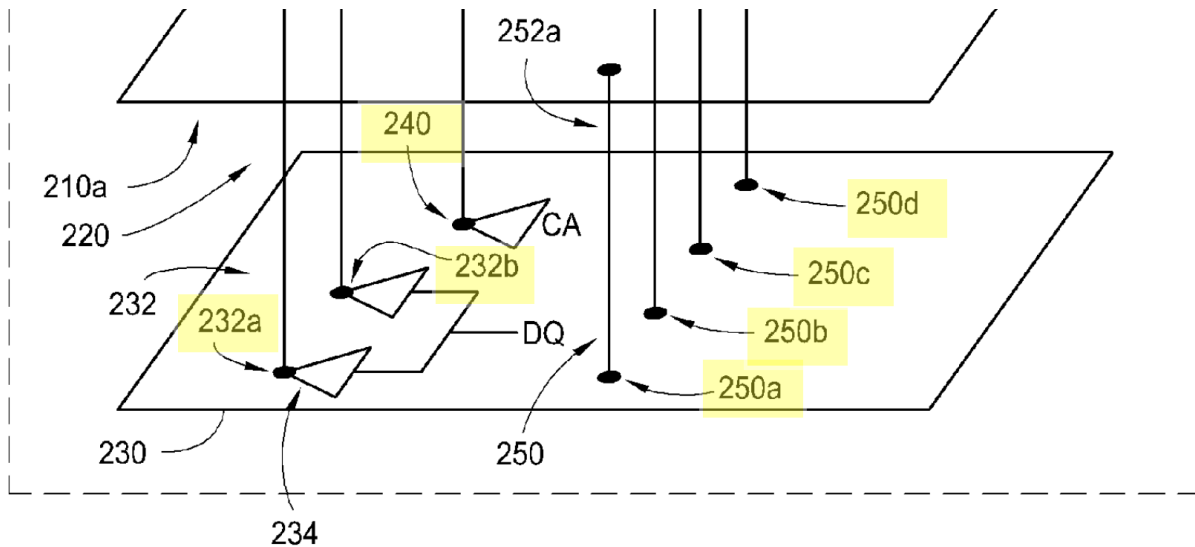


FIG. 1B

In the '087 Patent, each die interconnect has a corresponding “conduit” (e.g., 232a below), which may include a driver (e.g., 234), configured to transmit a signal to the die interconnect. EX1001, 4:33-34, 6:35-50.

¹ The annotated figures in this section are from prior proceedings involving the related 060 Patent, which has the same figures as the '087 Patent. EX1003, ¶61.

In addition, unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.



The problem identified by the '087 Patent is that a “load” exists on each conduit (e.g., driver), and “to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.” EX1001, 2:25-32.

As shown by Figure 2 (below), the '087 Patent purports to improve upon the prior art (e.g., Figure 1B) by replacing **one** data driver (e.g., driver 184 in Figure 1B) with **two** or more drivers 234 coupled to the same DQ data terminal, each driving the data signal through a respective die interconnect (220a, 220b) in electrical communication with a **subset** of the array dies (e.g., 210a and 210b (yellow), or 210c and 210d (orange)), thereby reducing the overall load on each driver. EX1001, 5:48-6:21, 6:64-8:6, Fig.2 (below).

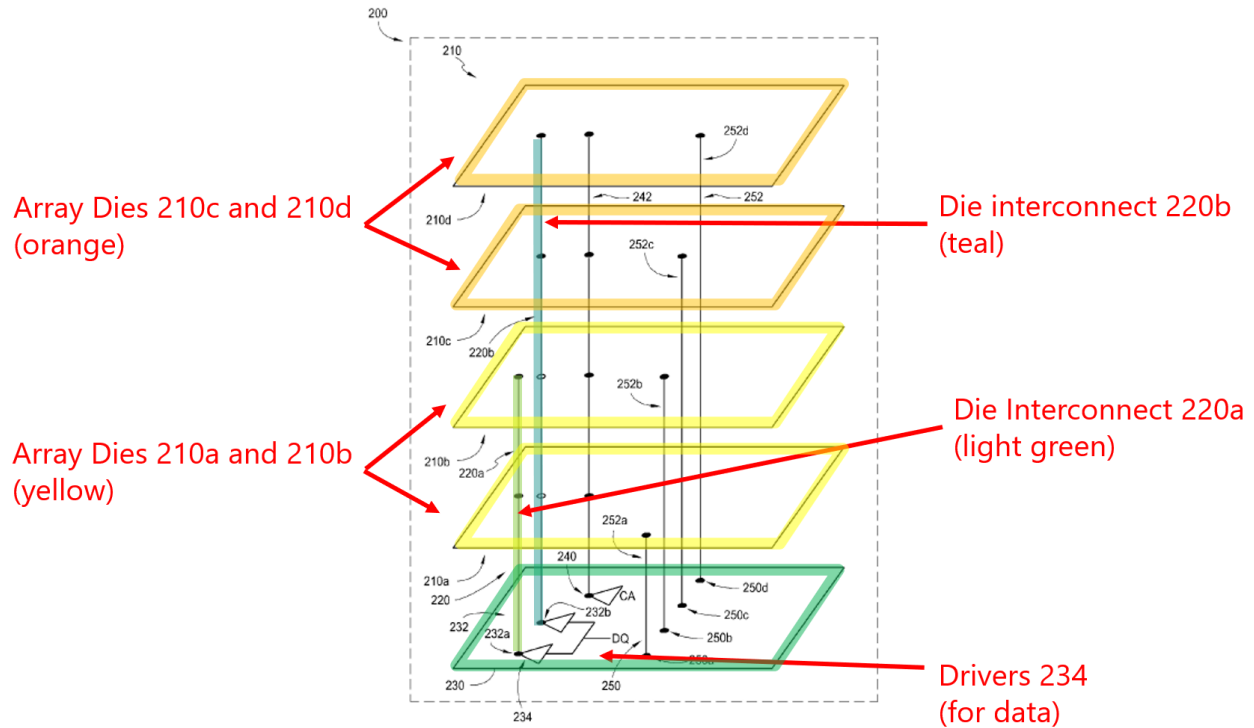


FIG. 2

2. Prosecution History

The '087 Patent, owned by Netlist, claims priority through a series of continuation applications to the 160 Patent and to the 060 Patent filed November 3, 2011. See EX1001.

During prosecution of the '087 Patent, the Examiner rejected all claims for being “not patentably distinct” from claims of the 160 and 060 Patents. EX1002, 45, 103-16. Netlist overcame that rejection by filing a terminal disclaimer. EX1002, 158-60, 163, 261-62.

Before the '087 Patent issued on May 20, 2025, the Board found — in response to IPRs filed by Petitioner supported by the opinions of Dr. Wolfe, the

same expert in this proceeding — that all claims of the 160 and 060 Patents were obvious. EX1072-74; EX1003, ¶¶68-70.

Netlist submitted the Board’s Final Written Decision for the 060 Patent, but inexplicably not for the 160 Patent. EX1002, 392. Remarkably, neither Netlist nor the Examiner ever discussed either Final Written Decision, or the prior art in those decisions. EX1003, ¶83.

Netlist repeatedly amended the claims during prosecution without showing support in the written description for all of the combined limitations in the amended claims; at most Netlist purported to identify support for a few isolated limitations. *See, e.g.*, EX1002, 738, 746-76, 768-76, 778-96, 800-03, 826-63; EX1003, ¶¶85-89. The Examiner allowed the claims without identifying written description for all of the combined limitations, and without distinguishing the claims from the invalidated claims of the 160 and 060 Patents. EX1002, 826-63; EX1003, ¶¶89-90.

B. Estoppel from IPRs against the related 160 and 060 Patents

As a result of the Final Written Decisions invalidating all claims of the related 160 and 060 Patents, EX1072-74, Netlist is “precluded from taking action inconsistent with [those] adverse judgment[s],” 37 C.F.R. §42.73(d)(3), including, but not limited to, “obtaining . . . [a] claim that is not patentably distinct from a finally refused or canceled claim,” *id.* §42.73(d)(3)(i); *SoftView LLC v. Apple Inc.*,

108 F.4th 1366 (Fed. Cir. 2024). Netlist is also “bound...by any subsidiary factual determinations that were actually litigated and essential to the judgment[s]” in those prior proceedings. *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, at 18 (PTAB July 16, 2019).

C. Person of Ordinary Skill in the Art (“Skilled Artisan” or “POSITA”)

Petitioner proposes the following definition of a POSITA, which is consistent with the definition adopted by the Board for the related 160 and 060 Patents, “with the exception of the qualifier ‘*at least*,’ which introduces vagueness as to the amount of experience.” EX1072, 7-9; EX1073, 7-9; EX1003, ¶59.

Petitioner does not object to omitting “at least” from the following definition.

A POSITA in the field of the ’087 Patent in 2010 and 2011 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor’s degree in such engineering disciplines and *at least* three years working in the field. EX1003, ¶58. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would

also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

Id.

V. CLAIM CONSTRUCTION

In related litigation, Netlist appears to have interpreted some claim language broadly for purposes of infringement, *see* EX1083, 11-17; EX1084, 11-17; EX1089; EX1044, 63-68; EX1046, 63-69, but Petitioner contends that no express constructions are needed for this proceeding because the claims are invalid regardless of their precise interpretation. EX1003, ¶¶91-94. Thus, Petitioner's Grounds below simply apply the "ordinary and customary meaning" of the claims of the '087 Patent. 37 C.F.R. §42.100(b). The constructions of certain terms in district court for the related 060 and 160 Patents (such as for "*array die*," which is not a term in the '087 claims) do not impact Petitioner's arguments here. EX1003, ¶¶92-93; EX1068, 31-35; EX1066, 8-16, 43; EX1077, 34-45; EX1078, 45-54; EX1079, 1-6. Similarly, the Board's constructions for the related 060 and 160 Patents do not impact Petitioner's arguments here. EX1072, 10-12; EX1073, 10-12; EX1003, ¶¶93-94. In particular, Petitioner's obviousness arguments here for

“*driver size*” apply regardless of whether that refers to “driver physical size,” as the Board previously assumed, or to driver strength. *Id.*

VI. ARGUMENT

A. Grounds 3 and 4 (all claims are obvious)

1. Overview of the prior art

a) Keeth (EX1047)

“Keeth” (EX1047) is a patent that is prior art under §102(e) (pre-AIA) because it was filed before the 893 Provisional (EX1005), and is prior art under §102(a) (pre-AIA) because it was published before the non-provisional for the '087 Patent which is not entitled to priority to the 893 Provisional. Although Keeth was cited during prosecution, EX1002, 71, Keeth was not discussed, EX1003, ¶155.

Keeth is generally directed to forming dice stacks on an interface die using interleaving conductive paths. EX1047, Abstract, 5:24-6:29, Fig.5 (below); EX1003, ¶¶156-157.

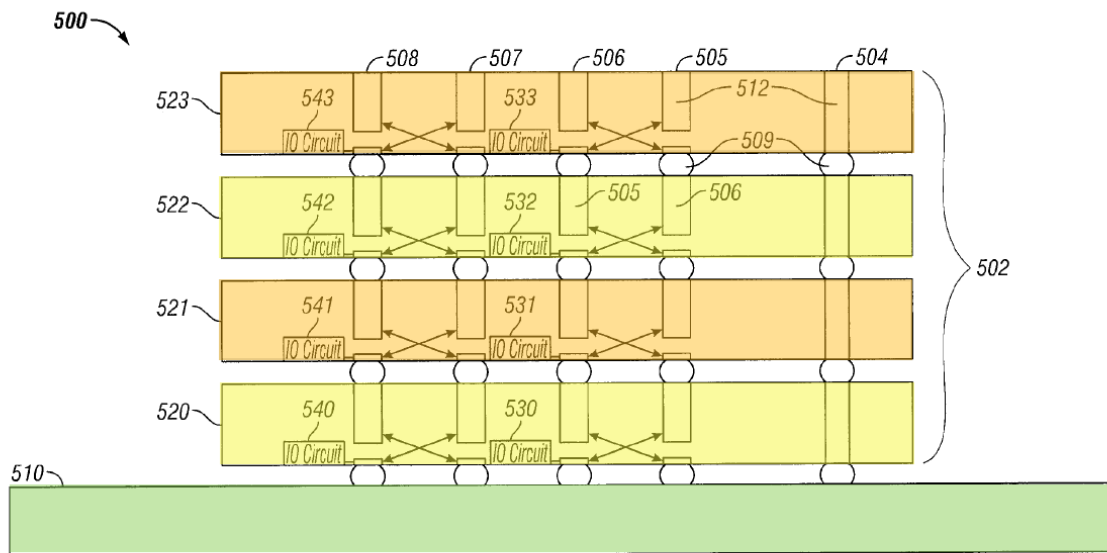


FIG. 5

b) **Shaeffer (EX1048)**

“Shaeffer” (EX1048) is a patent that is prior art under at least §102(e) (pre-AIA) because it was filed before the non-provisional for the '087 Patent which is not entitled to priority to the 893 Provisional (EX1005), and because its provisional filing date is before the 893 Provisional filing date, and its provisional (EX1049) has the same disclosure as Shaeffer itself (EX1048) and thus provides written description for all of the claims and disclosure of Shaeffer for the same reasons that Shaeffer itself does, see EX1003, ¶159; see also EX1050, pp.299-301. For example, written description for claim 1 of Shaeffer (EX1048) is found in Figure 3 and paragraphs [0010]-[0013] and [0028]-[0033] of the provisional (EX1049). EX1003, ¶159. Thus, all of the disclosure in Shaeffer, which is also in its

provisional, is prior art as of its provisional filing date. *In re Riggs*, 131 F.4th 1377, 1384-86 (Fed. Cir. 2025).

Shaeffer was not cited or discussed during prosecution. EX1003, ¶161.

Shaeffer discloses a “protocol for high speed signaling between a memory device and a memory controller” using specific signals and corresponding signal lines to communicate through a chip-to-chip interface to access the memory device for memory operations. EX1048, 1:17-19, 3:25-61, Fig.1A (below); EX1003, ¶¶162-163.

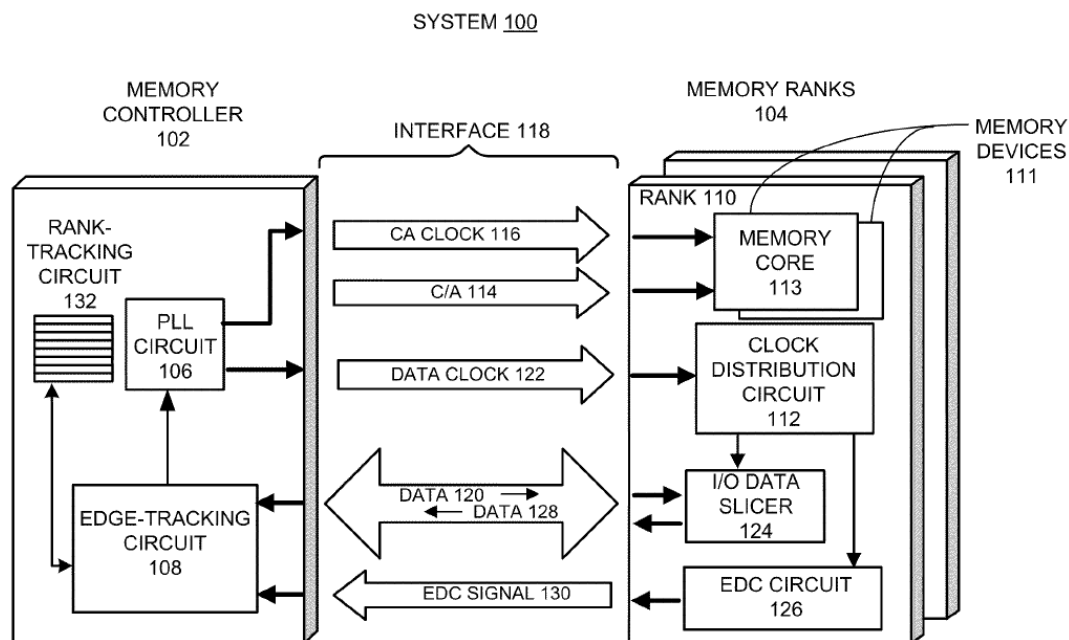
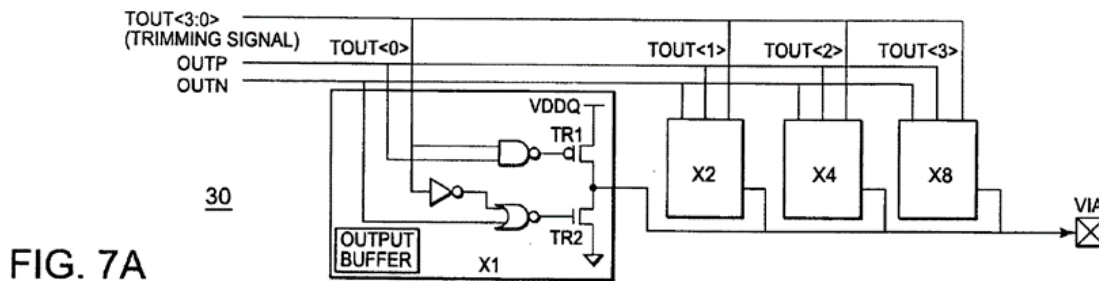


FIG. 1A

c) **Riho2** (EX1018)

“Riho2” (EX1018) is a published application (later issued as a patent (EX1053)), and is prior art under at least §102(a) (pre-AIA) because it was published before the filing of the 893 Provisional for the '087 Patent. Although Riho2 was cited during prosecution, EX1002, 72, Riho2 was not discussed, EX1003, ¶166.

Riho2 recognizes that the capacitive load will increase “as the number of stacked chips is increased,” and thus discloses a circuit for optimizing drive capacity “according to a change in the time constant caused by parasitic capacitance and parasitic resistance.” EX1018, ¶¶[0003, 0010, 0097], Fig.7A (below); EX1003, ¶¶167-168.



2. **Ground 3 combination: Keeth (EX1047) and Shaeffer (EX1048)**

A POSITA would have been motivated to combine the teachings of Shaeffer (EX1048) about signaling techniques with the memory stacks of Keeth (EX1047).² EX1003, ¶173. Keeth teaches stacks of memory dice³ (e.g., 202) with independently controlled vaults (e.g., using vault control circuits 212 in interface die 210) and interleaving connections provide advantages such as increased bandwidth and speed. *See* EX1047, 3:5-8, 3:44-54, 4:4-16, 5:39-46, 6:19-24, 10:66-11:7, Figs.2 & 5 (both below); *see also* EX1003, ¶¶156-157, 174-176. But Keeth does not provide details of the signaling protocols. EX1003, ¶176. Accordingly, a POSITA would have been motivated to look for advantageous signaling protocols—such as those in Shaeffer—that can be used in Keeth’s memory vaults and interleaving connections. *Id.*

² Keeth and Shaeffer are each analogous art to the ’087 Patent, because they are all directed to stacked memory devices and are pertinent to improving memory operations in the stack. EX1003, ¶172; *see also* EX1001, 1:33-34, 8:1-4, 21:26-28; EX1047, 1:55-60, 10:66-11:7, 5:63-67; EX1048, 11:12-18, 2:23-26.

³ “Dice” are the same as “dies.” EX1003, ¶156.

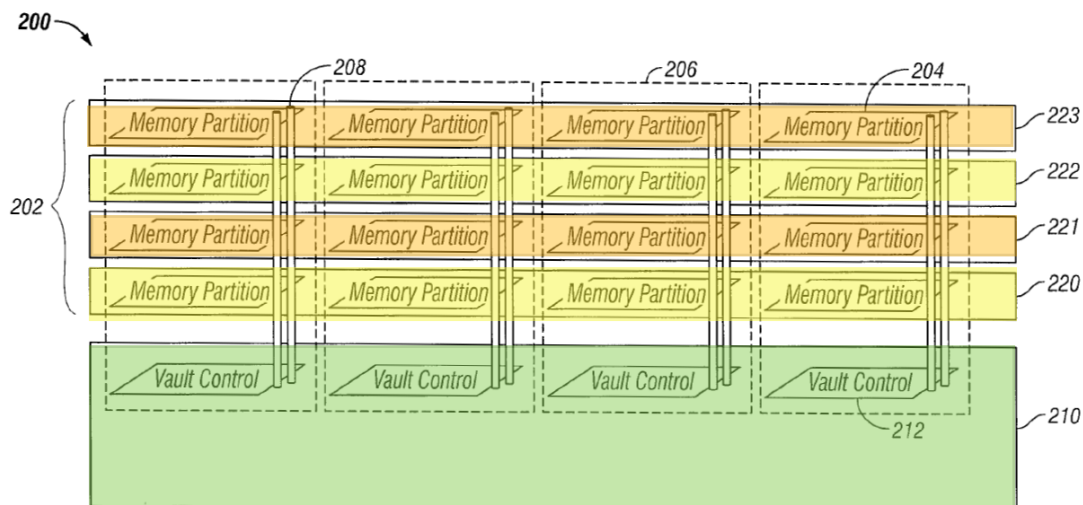


FIG. 2

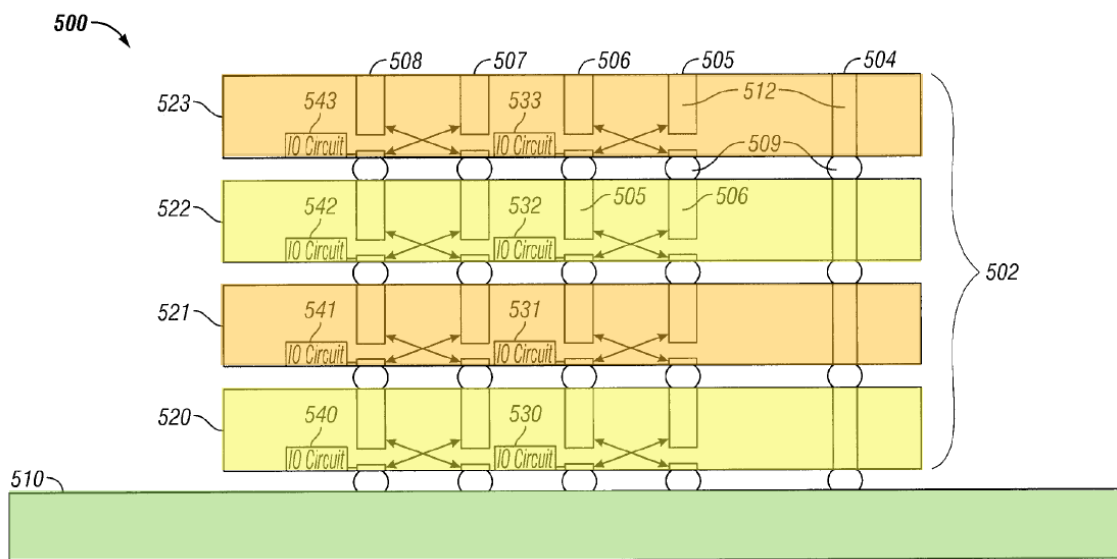


FIG. 5

Shaeffer meets this need by disclosing “apparatus and protocol for high speed signaling between a memory device and a memory controller” where the “memory controller...may be stacked with one or more memory devices...in a through-silicon via (TSV) stack.” EX1048, 11:4-18, 11:19-24, 1:17-19; EX1003,

¶¶162-163, 177-178. Thus Shaeffer, like Keeth, uses a TSV stack where the memory controller is stacked with the controlled memory dice. *Id.* Accordingly, a POSITA would have been motivated to implement advantageous aspects of Shaeffer's high speed signaling functionality in Keeth's memory stack. *Id.*

One such feature from Shaeffer is high-speed signaling using connections for command/address signals (C/A 114) separate from connections for data signals (120/128). EX1048, 3:25-61, Fig.1A (below); EX1003, ¶¶162, 178.

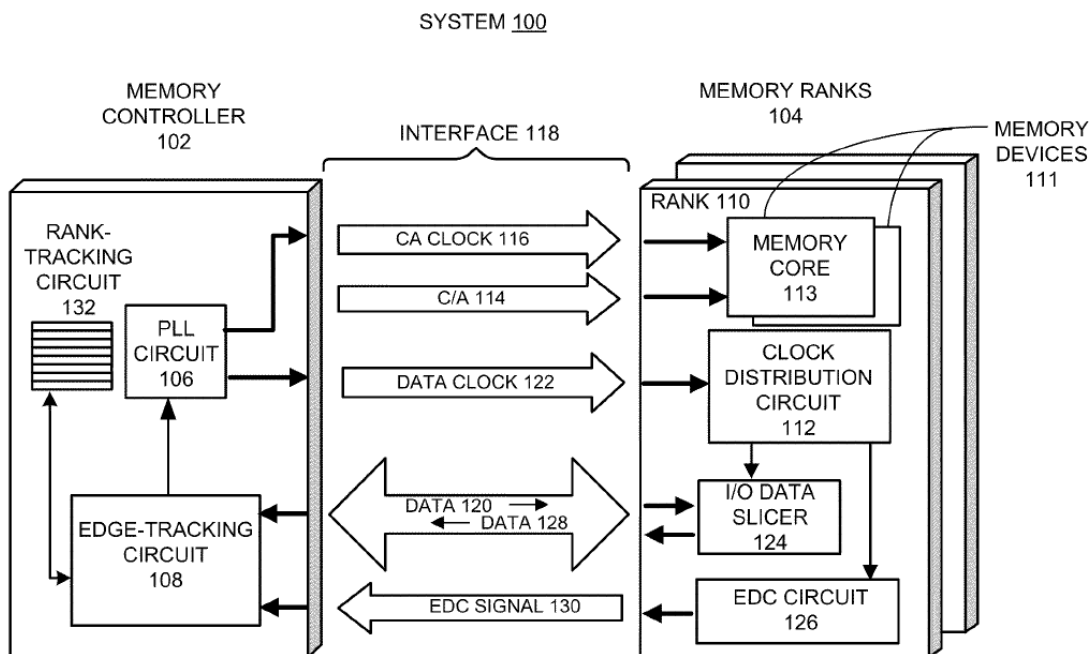


FIG. 1A

A POSITA would have understood that, by using separate C/A and data connections, the bandwidth of the data transfer can be increased, since C/A connections can be used to schedule further data transfer while the previous data

transfers are still being communicated on the data connections. EX1003, ¶179.

This is shown in Figure 4B of Shaeffer (below). *Id.*; EX1048, Fig.4B.

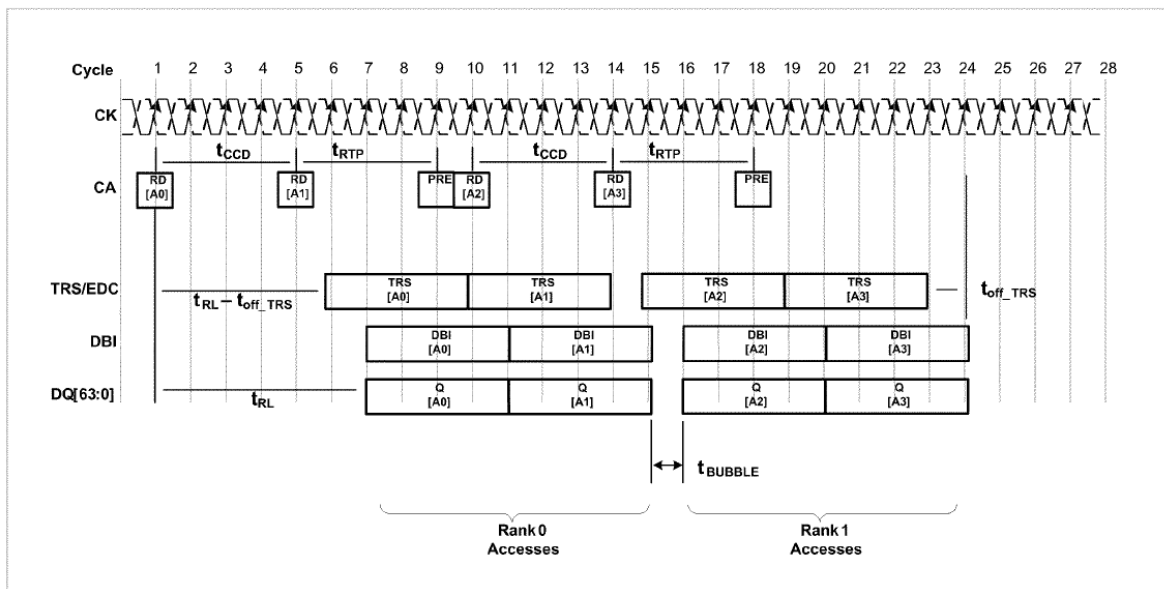


FIG. 4B

The use of Shaeffer's separate C/A and data lines is supported by Keeth's teaching that its stacked memory devices can be similar to DDR3 SDRAM devices. EX1047, 2:37-41; EX1003, ¶180. The JEDEC standard for DDR3 SDRAM requires separate C/A and data lines. *Id.*; *see also* EX1019 (JESD79-3C), p.12, Fig.3 (below, 4-stacked DDR3 memories having control/address C/A lines like RAS, CAS, WE, An, and BAn, separate from data lines DQ0-15).

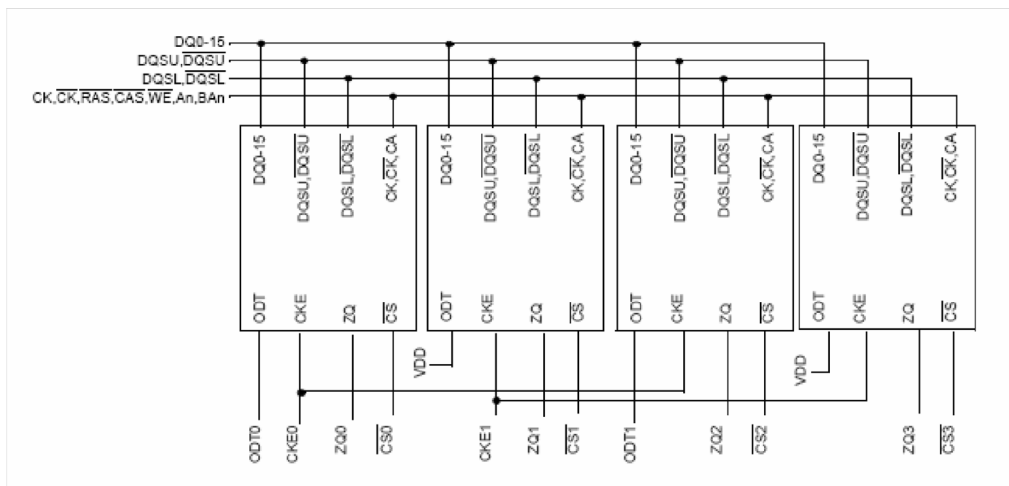
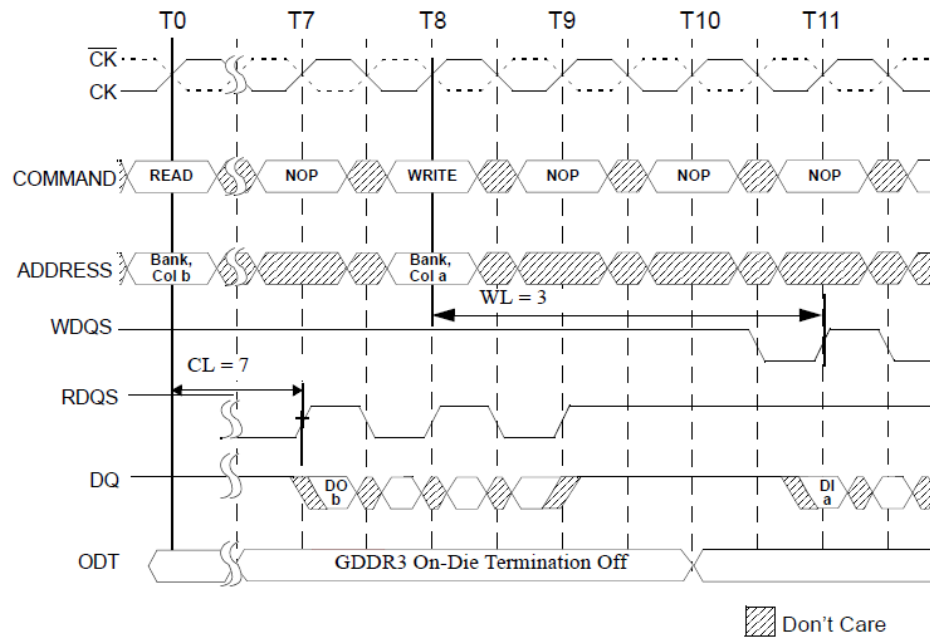


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

Shaeffer similarly teaches that its memory devices can be “graphics double data rate (GDDR, GDDR2, GDDR3, GDDR4, GDDR5, and future generations) and double data rate (DDR2, DDR3 and future memory types).” EX1048, 8:60-64; EX1003, ¶¶181-182. Like DDR memories, GDDR3 memory devices also used separate command, address, and data (DQ) lines. EX1036 (JESD 21-C 3.11.5.7), p.9 (below).

READ To WRITE



Such memory devices using separate lines for address (A0-AX, below left), command (including RAS, CAS, WE, upper left) and data signals (DQ, bottom right) were well-known. *See, e.g.*, EX1051 ([Schnarr](#)), Fig.5 (below); EX1003, ¶182.

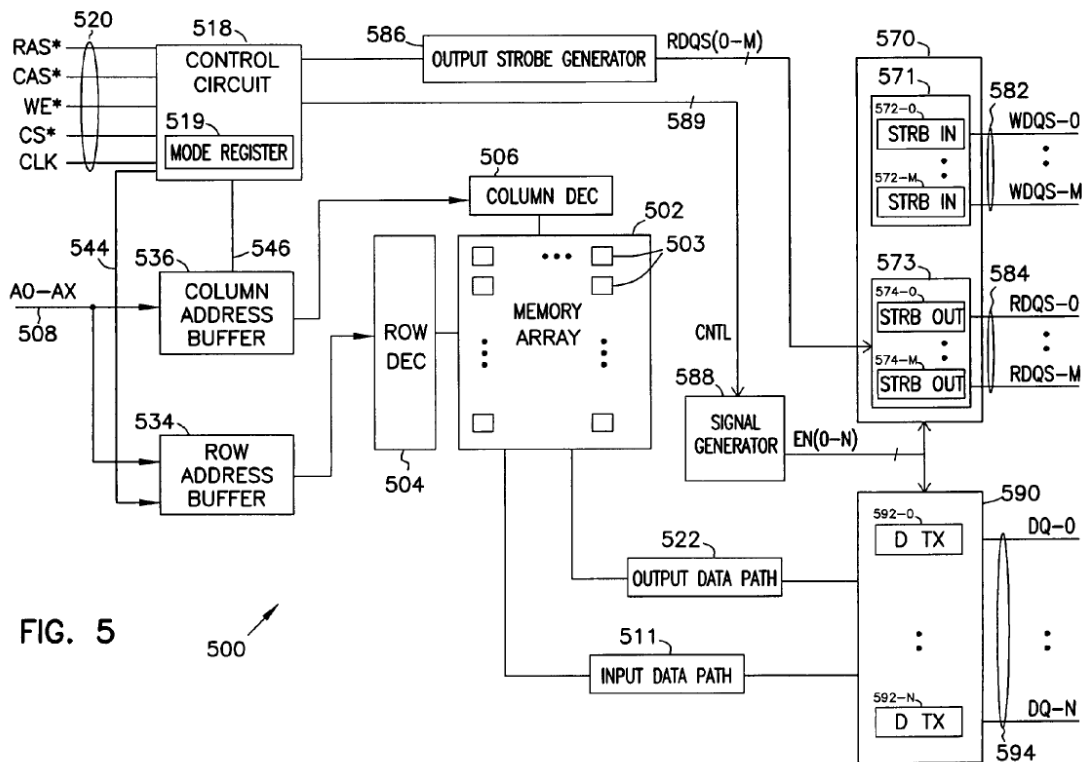


FIG. 5

A POSITA would have understood that such separate C/A and data connections can be used in a stack in order to communicate with memory dice. *Id.*, ¶183.

Indeed, stacks of memory dice using separate C/A and data lines (implemented by TSVs) were well-known. *Id.*; see, e.g., EX1043 (Ide), Fig.4 (below, with separate TSVs for address (upper left), command (left), and data signals DQ0-D15 (bottom)).

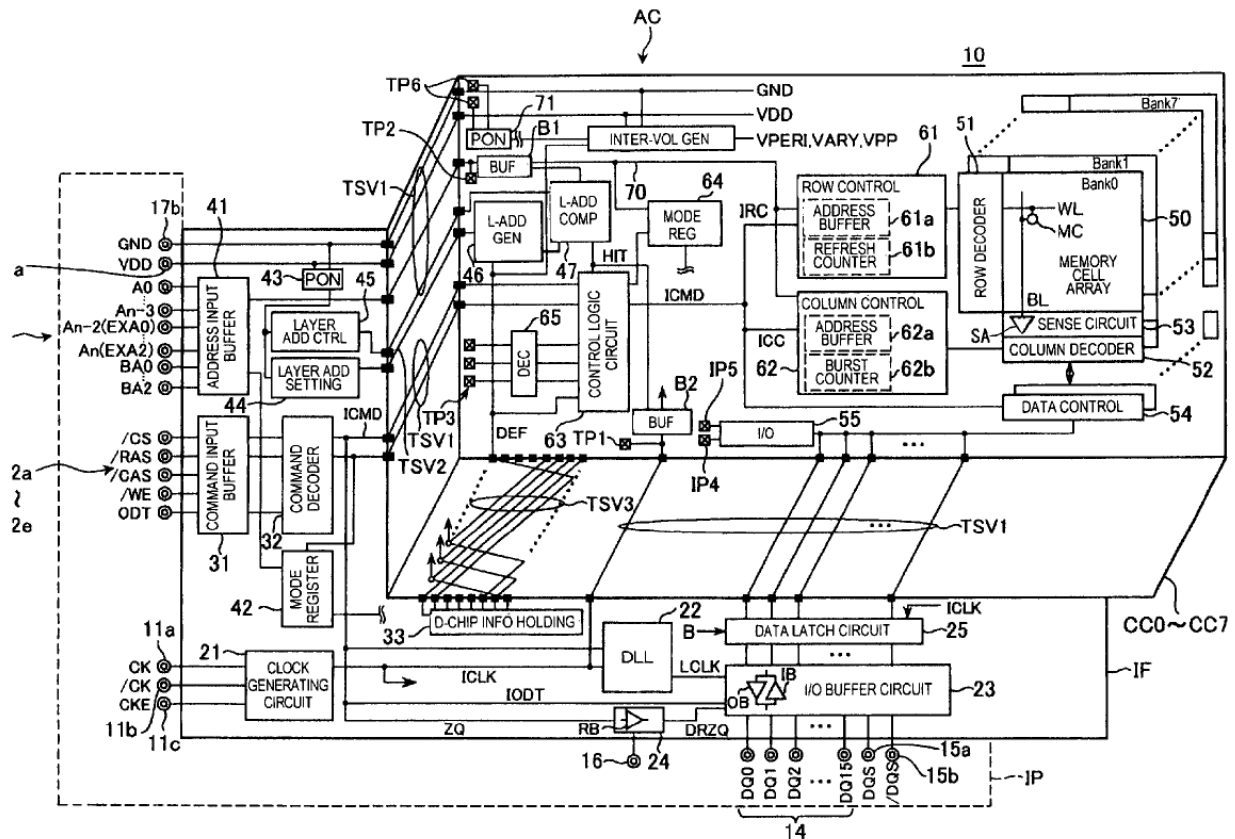


FIG. 4

A POSITA would thus have been motivated to implement Keeth's interleaving connections with command/address signals separate from data signals, which increases bandwidth and allows access to odd and even dies independently and concurrently. EX1003, ¶184; EX1047, 5:63-6:10.

A POSITA would have been also motivated to utilize Shaeffer's timing reference signal (TRS) in Keeth. EX1003, ¶¶185-186. Shaeffer teaches the advantages of using a TRS to compensate for noise or drift in temperature or supply voltage output by the memory device in response to a read command. *Id.*; EX1048, 2:10-22, 2:23-49. The TRS, as taught by Shaeffer, "is also used to

transfer error detection and correction information (EDC).” *Id.*, 2:64-3:4, Fig.4B (above p.18); EX1003, ¶185.

A POSITA would further have been motivated to implement Shaeffer’s write data strobe functionality and its read data capturing functionality in the memory stack of Keeth. EX1003, ¶188. Shaeffer teaches using a data clock/strobe (122) to help the memory devices to capture write data from the memory controller. EX1048, Fig.1A, 9:1-9 (“clock...may be a strobe”); EX1003, ¶187. As shown in Figure 1A of Shaeffer (above p.17), the data clock/strobe 122 is a unidirectional signal from the control die to the memory die and is used for capturing write data. *Id.*, ¶188. Shaeffer teaches that its control die advantageously captures the read data with proper, rank-specific timing using an edge tracking circuit 108 and a rank tracking circuit 132. EX1048, 3:62-4:6. Such unidirectional strobe signals for write operations (WDQS) were a standard, well-understood technique at the time used for high-speed write operations, as evidenced by Schnarr discussed above. EX1051, 9:19-34, Fig.5 (above p.21) (disclosing separate unidirectional RDQS and WDQS strobe lines for read and write, respectively); EX1003, ¶188. Furthermore, a POSITA would have understood that a strobe signal uses less power than a continuous clock signal. *Id.*

Lastly, as evidenced by these prior art references, including industry standards, implementing Shaeffer’s signaling protocols in the memory stack of

Keeth was well within the level of skill at the time and a POSITA would have a reasonable expectation of success in making the combination. EX1003, ¶189; EX1047, 3:5-8; EX1048, 12:28-29.

3. Ground 4 combination: Ground 3 further in view of Riho2 (EX1018)

A POSITA would have been further motivated to combine the optimization techniques from Riho2 (EX1018) with Keeth and Shaeffer (Ground 3). EX1003, ¶¶190-202.⁴ As Riho2 explains, “the fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product.” EX1018, [0003]. One reason for this is that “as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the [TSVs] and via-to-via connections proportional to the thickness of the stacked chips.” *Id.* Riho2 discloses solutions for addressing such issues, which a POSITA would be motivated to use in combination with Keeth and Shaeffer. EX1003, ¶¶198-201.

⁴ Riho2 is analogous art to the '087 Patent, Keeth, and Shaeffer because they all are directed to stacked memory devices (such as DRAM chips) and pertinent to improving bandwidth and speed. EX1003, ¶¶190-191; EX1018, [0003], [0010-11].

One such issue that a POSITA would have recognized is changes in the time constant in the combination of Keeth and Shaeffer. *Id.*, ¶¶194-196. The conductive paths in the stack of the Keeth-Shaeffer combination include TSVs and joints, which can couple to I/O circuits, and a POSITA would have understood that the load to be driven on these paths is determined by the parasitic capacitance and resistance on the interleaving conductive paths. EX1047, 5:34-38, 7:37-45, Fig.7 (below); EX1003, ¶¶194-196, 175-178. Keeth further explains that the conductive paths “may entirely pass through or partially pass through the dice stack,” and therefore may have different lengths. EX1047, 5:34-38; EX1003, ¶196. Accordingly, a POSITA would have understood that the load and the corresponding time constant of the conductive paths would typically be different based on their different lengths. *Id.*

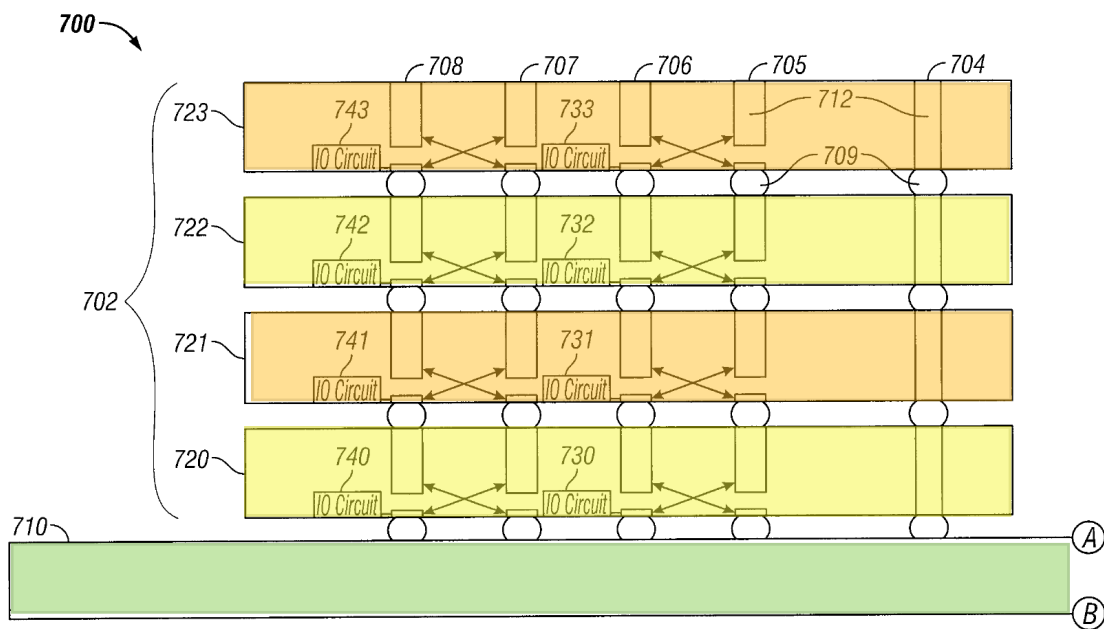
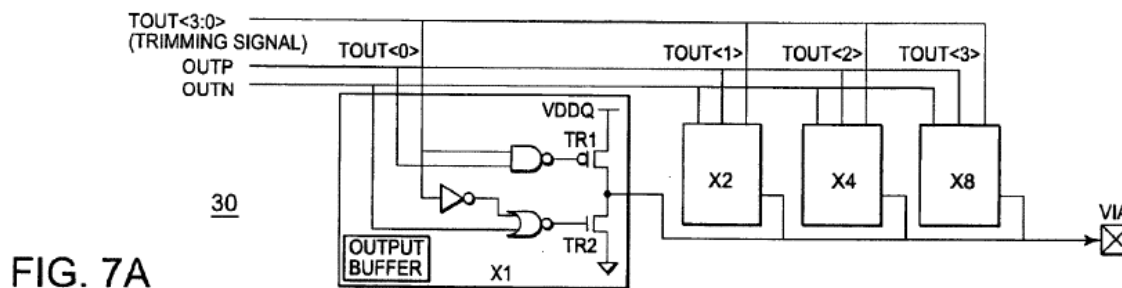


FIG. 7

A POSITA would thus have been motivated to look for techniques addressing these timing problems, such as the driver-size optimization techniques of Riho2, which would advantageously improve and stabilize high frequency memory operations despite the time-constant variations, and additionally reduce power consumption. EX1003, ¶198; EX1018, [0010-11]; *see also* EX1017 (Wyman), 1:22-24. In particular, Riho2 teaches “optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance.” EX1018, [0097-98], Fig.7A (below); EX1003, ¶¶192-193. Riho2 teaches varying the number of transistors and/or the size of the transistors used to drive a signal, similar to the '087 Patent. *Id.*; EX1001, 17:26-28.



Riho2 further explains that “it is necessary to take into consideration that the parasitic capacitance and parasitic resistance,” and that “the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another.” EX1018, [0096]; EX1003, ¶197. A POSITA would have understood

that such varying parasitic capacitance and resistance is inherent in the manufacturing process. *Id.*; see also EX1016 (Riho), [0056].

Implementing Riho2's driver-size optimization with Keeth and Shaeffer was well within the level of skill for a POSITA who would have a reasonable expectation of success in making the combination. EX1003, ¶202. For example, Riho2 teaches specific implementations using different number of transistors and/or transistors of different sizes, which could be selected using computer-aided design tools for a specific design, as taught for the combination of Keeth and Shaeffer. *Id.*; EX1018, Fig.7A, [0097-98]; EX1048, 12:28-29. The selection of the transistors in Riho2's buffer can also be implemented not just by ROMs but also by other known ways, such as anti-fuses or breaking connections. EX1018, [0041]; EX1017, 5:34-44; EX1003, ¶202.

A POSITA would also be motivated to implement Riho2's teachings about reducing power consumption. EX1018, [0008]; EX1003, ¶¶199-200. To solve the problem of power consumption while maintaining high bandwidth, Riho2 teaches that using a large number of data signals (e.g., 256) while limiting data transmission and reception speeds to “a data transfer rate of 400 Mbps (102.4 Gbit/256)” can “enable[] the memory module to stably communicate with the memory controller at a low power consumption, and provides a memory module having a data transfer speed of 12.8 Gbytes/sec.” EX1018, [0052]; EX1003, ¶199.

In addition to reducing power (and current), Riho2 further teaches that operating the memory chips at a lower frequency can also increase yield. *Id.*; EX1018, [0148]. Operating the memory chips at a lower rate than the rate for communicating with a processor was well within the level of skill at the time, and consistent Keeth's discloses that its interface die includes "circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates." EX1047, 3:62-67; EX1003, ¶201; *see also* EX1023, 19 ("[t]he technique goes back at least to the mid-1960's"); EX1018, [0053].

4. **Claim 1**

a) ***[1.a]-[1.b.1] Stacked DRAM dies***

To the extent the preamble is limiting, Grounds 3-4 teach "[a] *dynamic random access memory (DRAM) package* [e.g., Keeth's memory package 100 below]." EX1047, Figs.1, 10 (below), 2:37-41 ("DRAM"). Keeth discloses its DRAM "dice stack 102" and "an interface die 110" can be implemented in "a package" to be coupled to external devices, e.g., "memory controllers." EX1047, 2:61-3:20; EX1048, 8:60-64 ("DRAM"), 11:10-12 ("single chip-package").

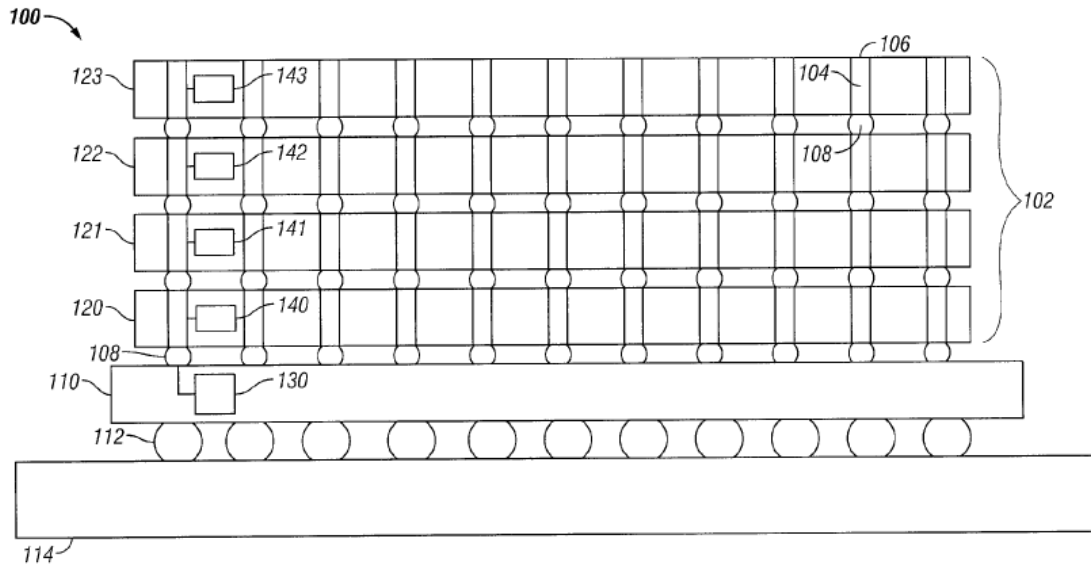


FIG. 1

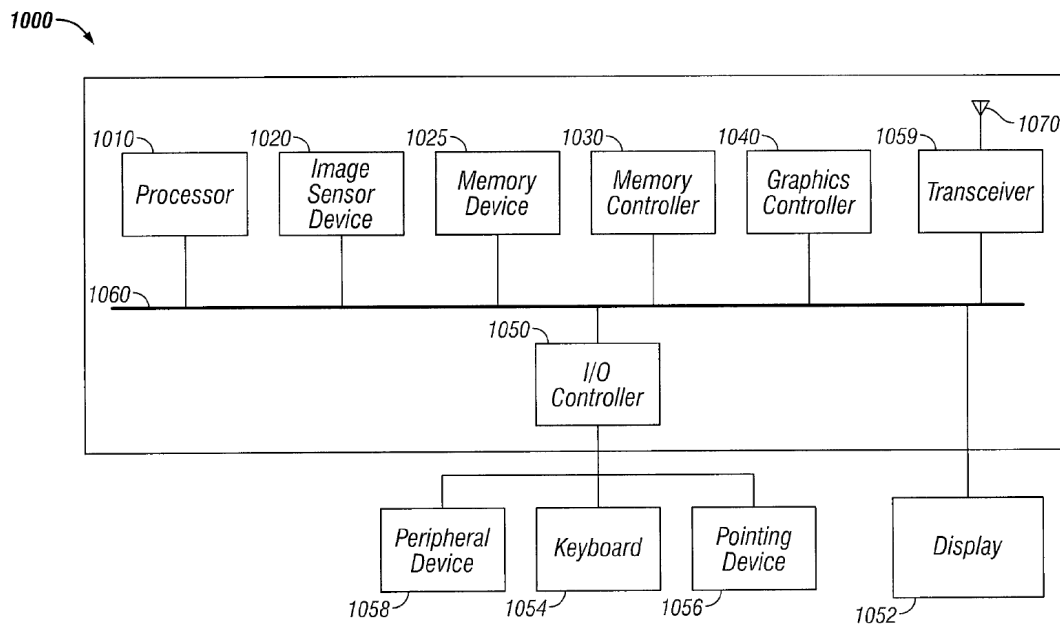


FIG. 10

Grounds 3-4 also teach “*stacked DRAM dies* [e.g., stacked dies 200 or 500 below] *including at least a first plurality of DRAM dies* [e.g., odd dies 221/223 or 521/523 (orange)] *and a second plurality of DRAM dies* [e.g., even dies 220/222 or

520/522 (yellow)].” EX1047, Figs.2, 5 (below, annotated), 1:55-64 (“stack”),
5:24-62 (“alternating dice in the stack”).

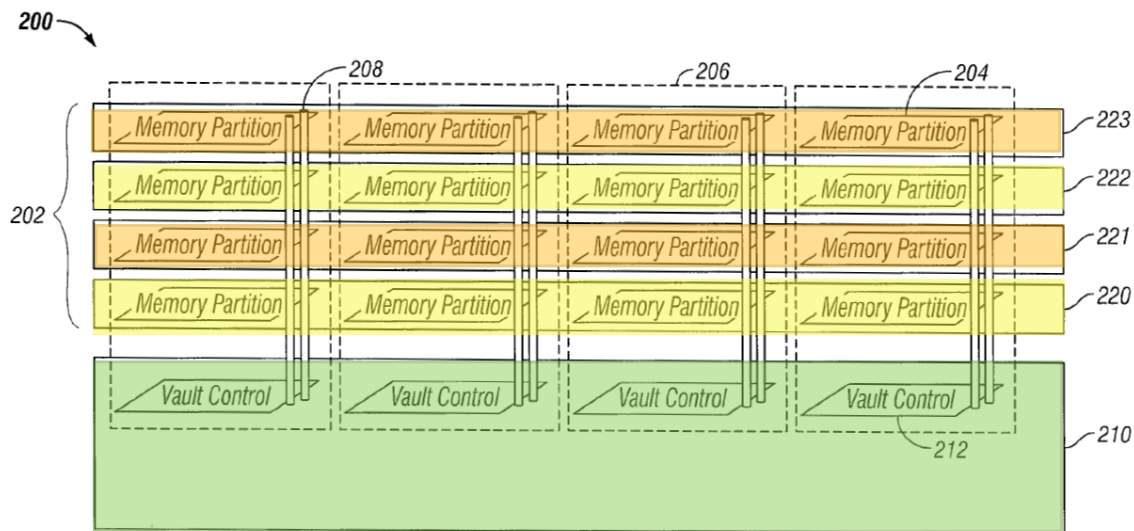


FIG. 2

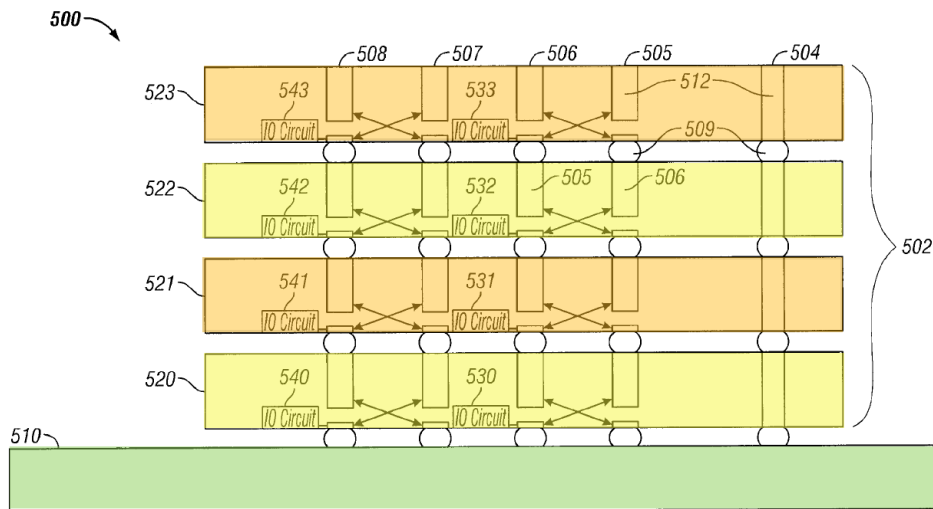


FIG. 5

b) [1.b.2] C/A and data ports and DRAM memory cells

Grounds 3-4 teach “each DRAM die of the stacked DRAM dies including C/A ports [e.g., “**command** circuits and/or **address** circuits,” EX1047, 6:4-10, in

“I/O Circuits” 540-543 in Fig.5 below], *data ports* [e.g., “input/output circuitry,” EX1047, 4:4-16, in “I/O Circuits” 530-533 below] and *DRAM memory cells* [e.g., “a plurality of memory cells,” EX1047, 3:57-58], wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells [e.g., for read/write].”

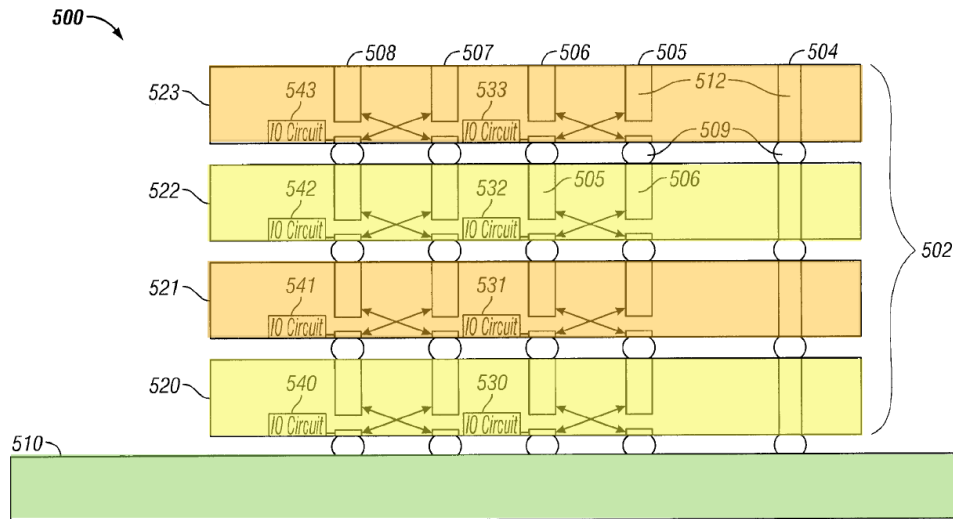


FIG. 5

Keeth discloses the “conductive paths” between the stacked DRAM dies and the interface die can “communicate (e.g., transfer) information such as data, address, [and] control.” EX1047, 3:5-8. And “the command circuits and/or address circuits of each DRAM die” are “connected to...the conductive paths...in order to communicate command and/or address signals.” *Id.*, 6:4-10. The conductive paths are also “connected to...input/output circuitry” in each DRAM die for the interface die to “concurrently...access and send data to” those dies. *Id.*, 4:4-16. Accordingly, a POSITA would understand that the “command circuits

and/or address circuits” include “*C/A ports*” “to communicate command and/or address signals,” and the “input/output circuitry” includes “*data ports*” to “access [from] and send data to” the memory dies and that these signal “*ports*” are in “I/O Circuits” in Figures 5 and 7 to connect the memory dies with the conductive paths. *Id.*, Figs.5 (above), 7; EX1003, ¶¶206-207; *see also supra* pp.17-22 (“*C/A ports*” separate from “*data ports*”).

Keeth also discloses “*DRAM memory cells*” in each die to store data. EX1047, 1:11-13, 3:57-58 (each memory die including “[DRAM] memory cells”); *see also* EX1048, Fig.1A (“memory core 113”), 3:20-24 (“each memory device 111...having a memory core 113”). These “*DRAM memory cells*” store data communicated through the “*data ports*” during, for example, read/write, thus “[t]he *each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells.*” EX1048, Fig.4A (read/write data transfers); EX1003, ¶¶208-209; *see also* EX1022, 317 (Fig.7.3 below, “DRAM internals” including “Data In/Out Buffers” and “[DRAM] storage cell”); EX1043, Fig.4 (annotated below, data (orange) from TSVs in a stack transferred between data control 54 (red) and DRAM cell 50 (blue)).

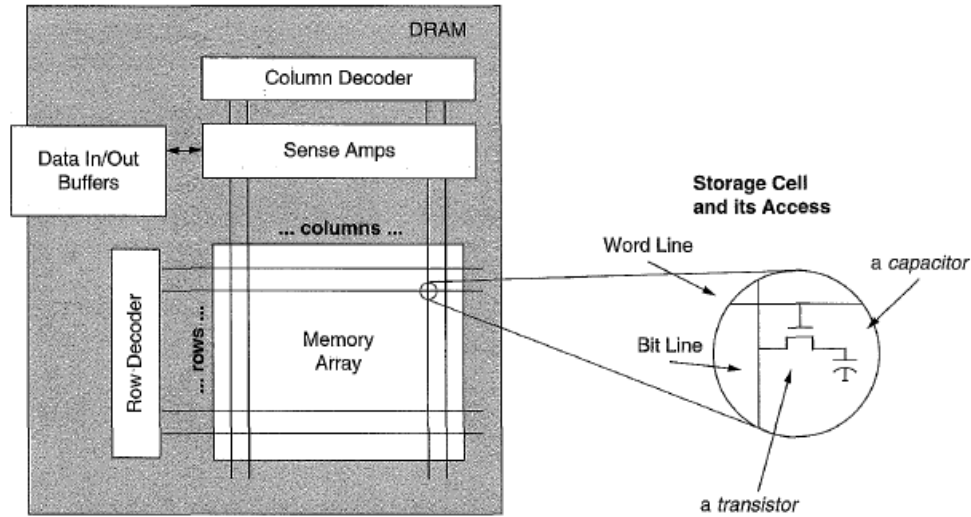


FIGURE 7.3: Basic organization of DRAM internals. The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

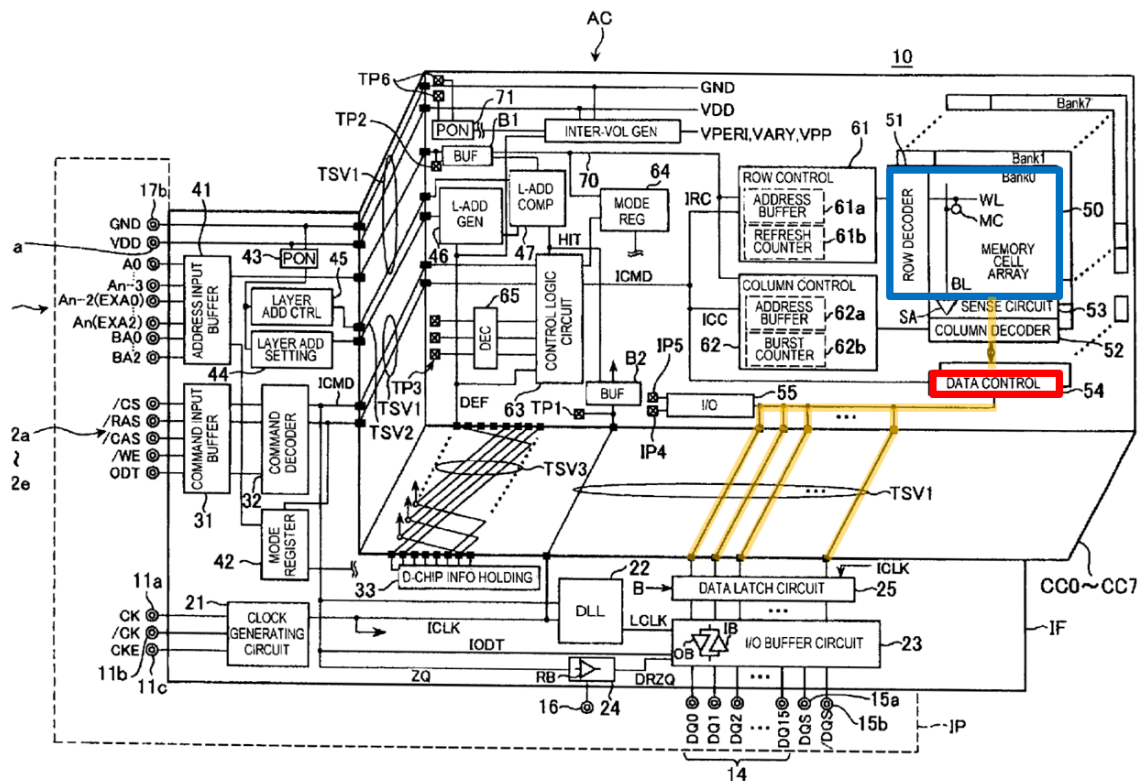
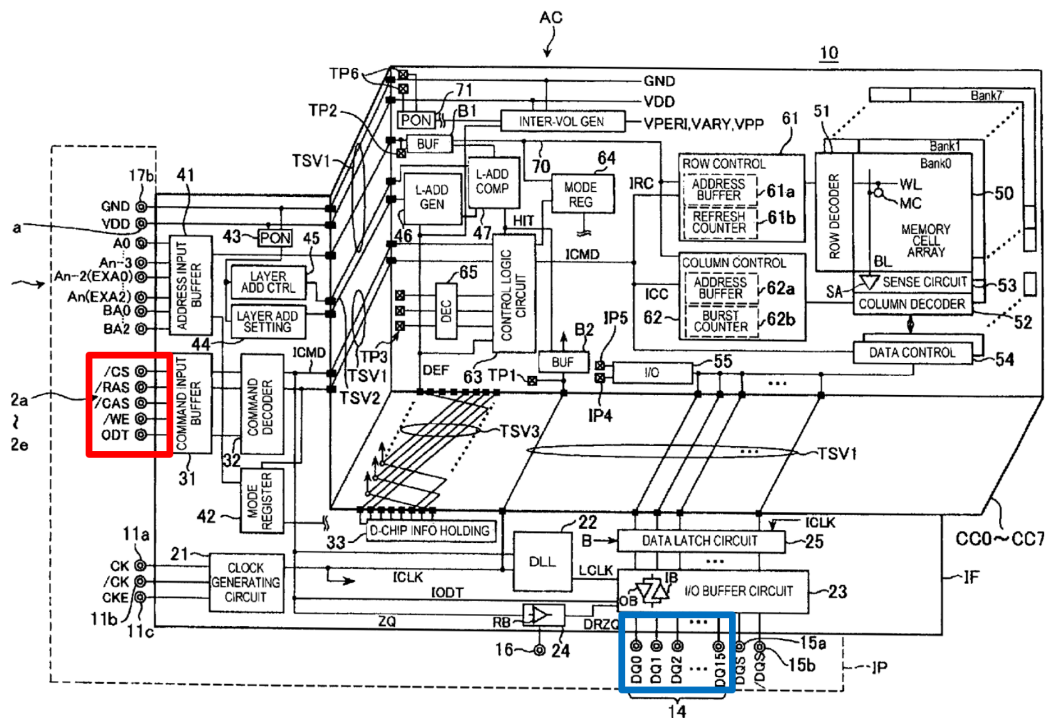


FIG.4

c) **[1.c.1] Terminals**

Grounds 3-4 teach “*terminals including command and/or address (C/A) terminals and data terminals* [e.g., on Keeth’s interface die to communicate C/A and data signals between the stacked DRAM dies and an external memory controller], *wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals* [e.g., for read/write].”

Keeth’s interface die includes “buffers, and I/O drivers” to communicate C/A and data signals between the DRAM dies in the package and an external device, “such as...a memory controller.” EX1047, 3:62-67, 3:9-15, 1:58-60 (“[M]emory dice may be connected to an interface die to provide input/output functionality with other components.”), Fig.10. Keeth also teaches its DRAM dies may include “DDR3-SDRAM.” EX1047, 2:37-43. Communication of C/A and data signals between DDR3-SDRAM dies and a memory controller uses “*terminals*” on the package (e.g., pins or balls), including “*C/A terminals*” to “*receive C/A signals*” and “*data terminals*” to “*receive or output data signals*,” as was standardized. EX1019, 6-11 (“Package Pinout” including “Stacked...Ballout” having data terminals (DQ0, DQ1...) and command/address terminals (RAS#, CAS#...)); EX1022, 322 (“address pins”), 348 (“data pins”); EX1043, 6:62-7:3, Fig.4 (below, the memory package having “*C/A terminals*” (red) for “*C/A signals*,”



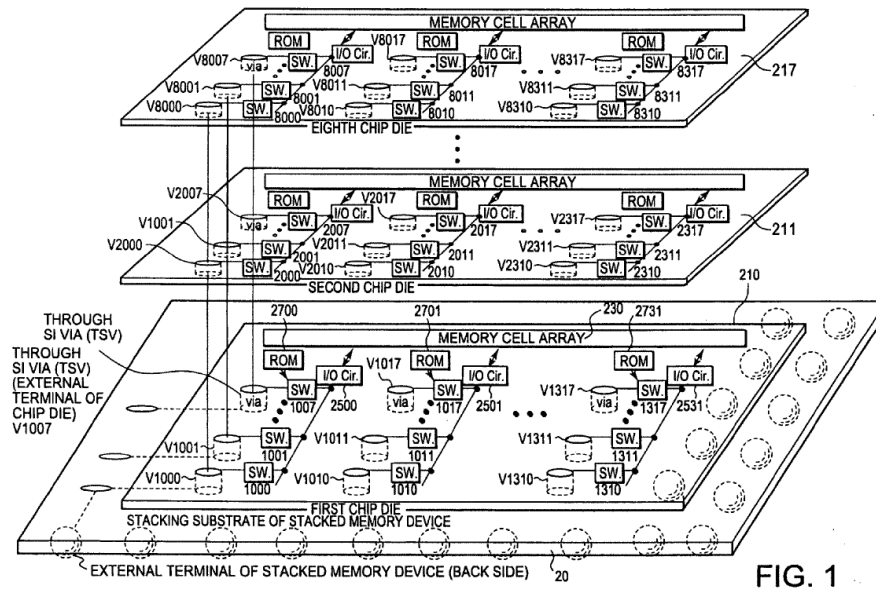


FIG. 1

It was also standardized to “*receive or output data signals...in response to the (C/A) signals,*” such as for read/write. EX1019, 56, 68-69 (DRAM outputting/receiving data in response to read/write C/A signals), 33 (command truth table). Shaeffer also discloses outputting/receiving data signals “*in response to the (C/A) signals*” for read/write. EX1048, Fig.4A (below, outputting/receiving data signal, Q[A0]/D[A1], in response to read/write C/A signal, RD[A0]/WR[A1]), 7:11-44; EX1003, ¶213.

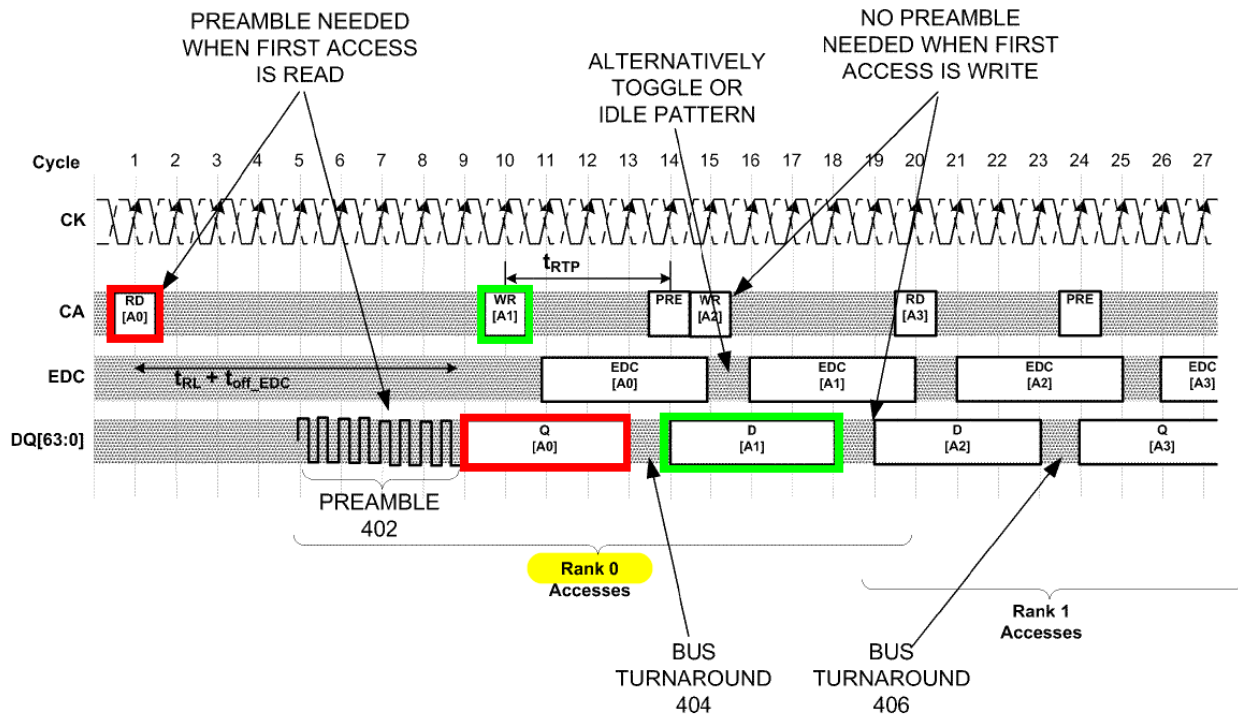


FIG. 4A

d) [1.c.2] First/second data signals

Grounds 3-4 teach “wherein the DRAM package is configured to output first data signals [e.g., Q[A0] below] in response to a first set of C/A signals associated with a memory read operation [e.g., RD[A0]] and to receive second data signals [e.g., D[A1]] in response to a second set of C/A signals associated with a memory write operation [e.g., WR[A1]]” for the reasons discussed above for [1.c.1] (pp.34-37). EX1048, Fig.4A (below).

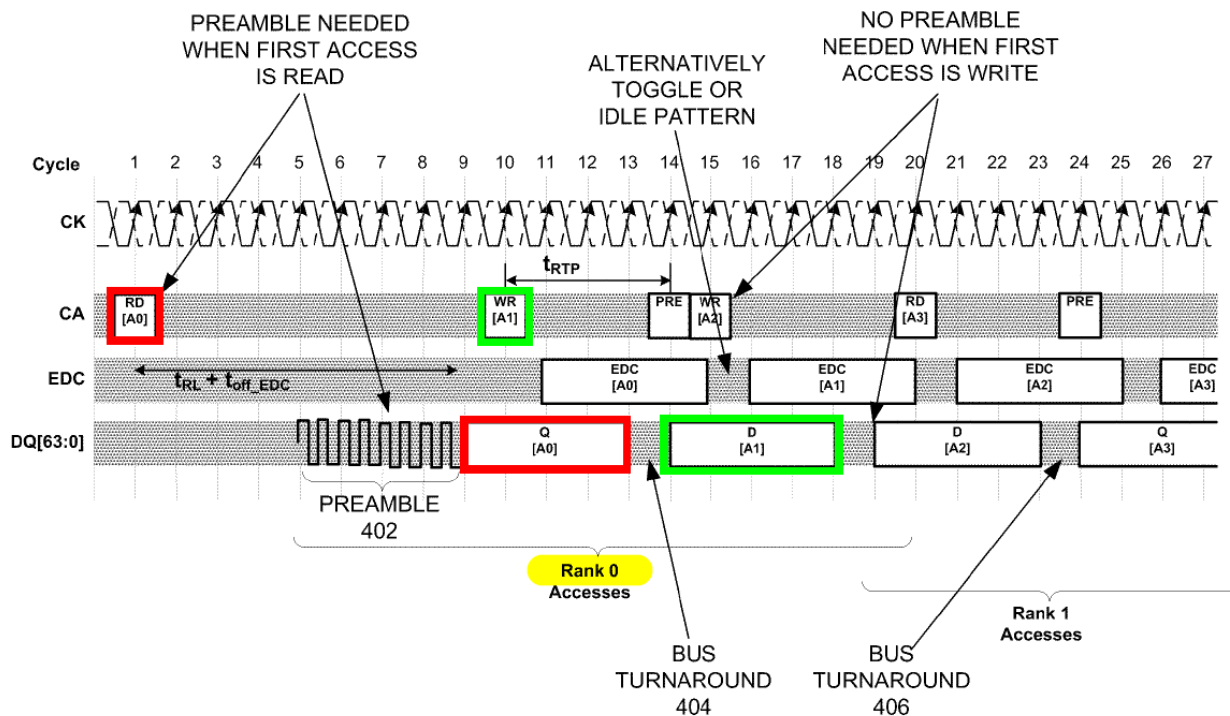


FIG. 4A

e) [1.d.1] C/A interconnects

Grounds 3-4 teach “die interconnects including C/A interconnects [e.g., “conductive paths” for “address, control,” EX1047, 3:5-8] and data interconnects [e.g., “conductive paths” for “data,” *id.*], the C/A interconnects including at least first C/A interconnects [e.g., “a first conductive path” to “odd dice,” EX1047, claims 39, 42, included in “conductive paths 507” (red) below] and second C/A interconnects [e.g., “a second conductive path” to “even dice,” *id.*, included in “conductive paths 508” (blue)].” EX1047, Fig.5 (annotated below).

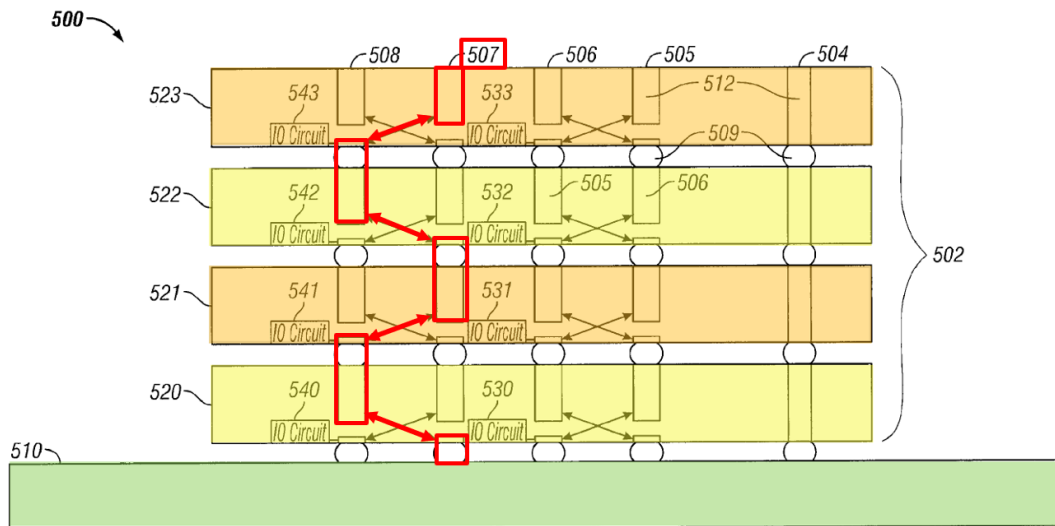


FIG. 5

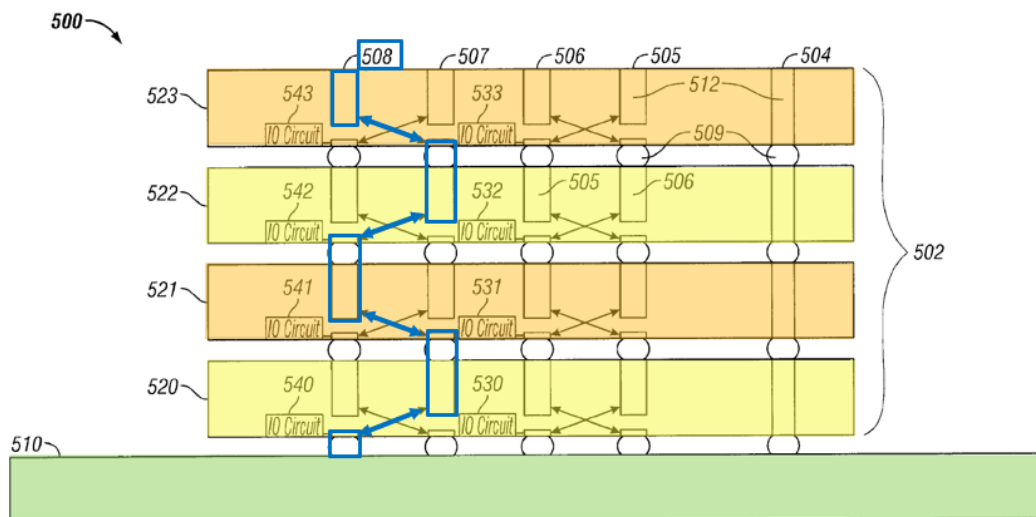


FIG. 5

Keeth teaches its “conductive paths”—via which the stacked DRAM dies and the interface die communicate signals—include “C/A interconnects” conducting “address, control” signals and “data interconnects” conducting “data” signals. EX1047, 2:61-3:8. Keeth also explains that its “interleaving conductive paths 505 through 508” can be “utilize[d]” for “command and/or address signals,”

where the “C/A interconnects” includes “first” and “second C/A interconnects” coupled to odd and even dies, respectively. EX1047, 6:4-10, claims 39, 42, 6:19-24 (“[E]ach vault may be independently controlled” when “interleaving conductive paths” are used for C/A signals), Abstract (“alternating dice of the stack”), 4:4-12 (“first communication path...connected to...odd partitions” and “second communication path...connect[ed] to...even partitions”), Fig.5 (above).

Grounds 3-4 further teach “the first C/A interconnects configured to conduct the first set of C/A signals [e.g., RD[A0] to Rank 0 below] and the second set of C/A signals [e.g., WR[A1] to Rank 0].” EX1048, Fig.4A (below).

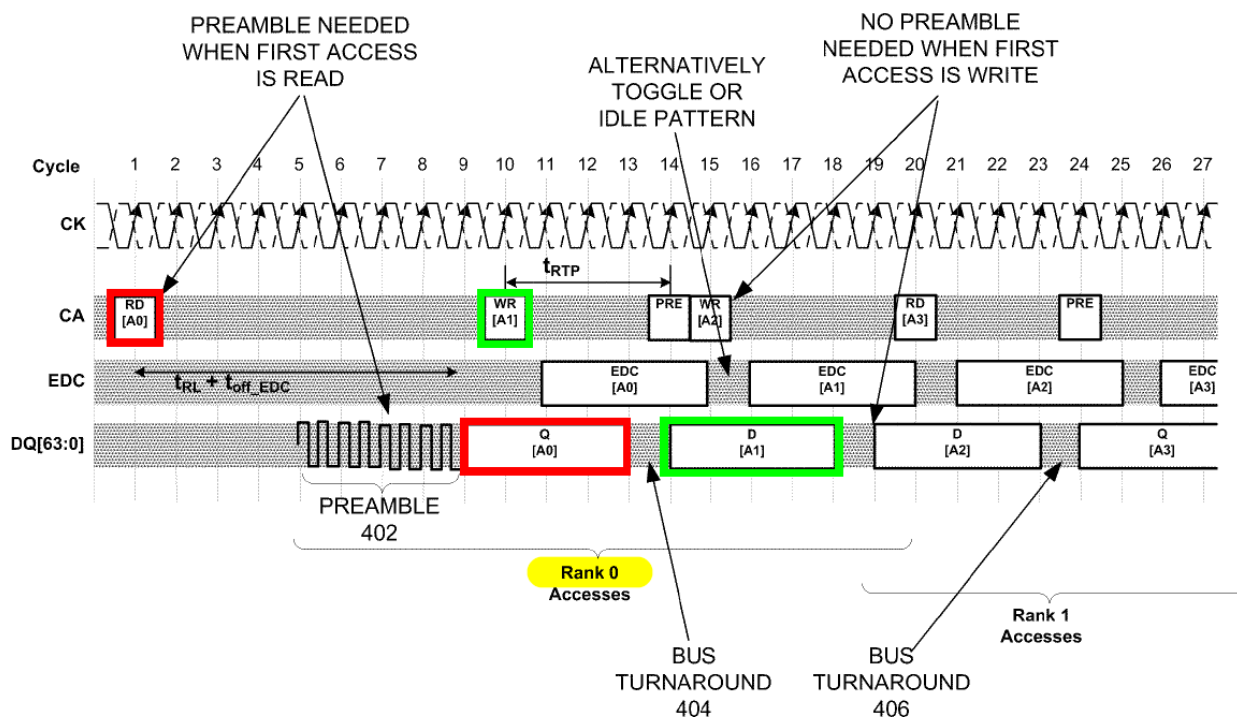


FIG. 4A

Shaeffer discloses transmitting the “*first set of C/A signals*” for read (RD[A0]) and then the “*second set of C/A signals*” for write (WR[A1]) to the **same** rank of memory (or Keeth’s “odd dice” in the combination), thereby conducting those C/A signals via the **same** C/A interconnects (i.e., “*the first C/A interconnects*” coupled to the “odd dice”). EX1048, Fig.4A (above), 7:11-44, 3:20-21 (“each rank 110” including “memory devices 111”), Fig.1A (below), 3:25-30 (“[T]ransmitting command/address (C/A) 114...to rank 110 over a chip-to-chip interconnect 118”).

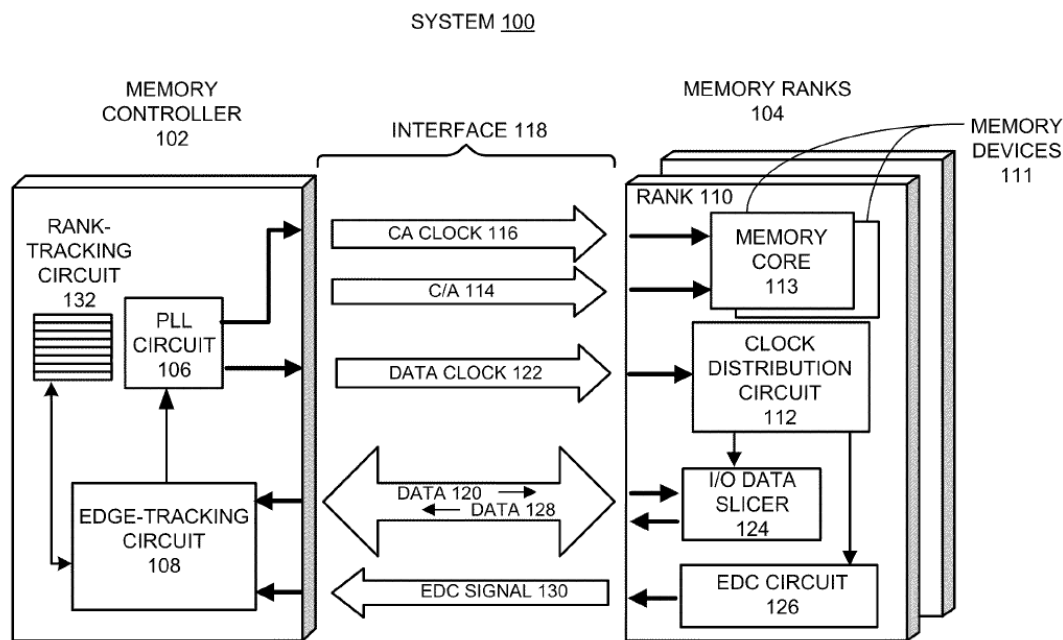


FIG. 1A

Such consecutive memory read/write operations to the same rank were well known. EX1019, 63 (Fig.35 below, READ (T0) and WRITE (T6) directed to the same rank of memory), 13 (“Rank”), 33-34 & n.1.

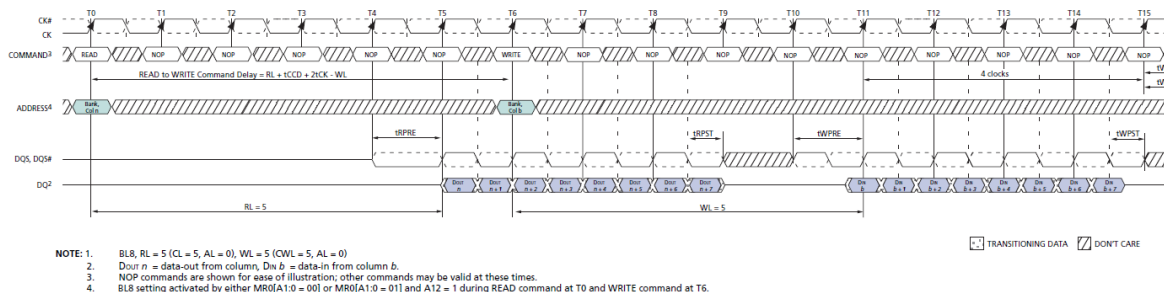


Figure 35 — READ (BL8) to WRITE (BL8)

f) [1.d.2] Data interconnects

Grounds 3-4 teach “the data interconnects including at least first data interconnects [e.g., “conductive paths” for “data,” EX1047, 3:5-8, to odd dies, included in “conductive paths 505” (red) below] and second data interconnects [e.g., “conductive paths” for “data,” *id.*, to even dies, included in “conductive paths 506” (blue) below].” EX1047, Fig.5 (annotated below).

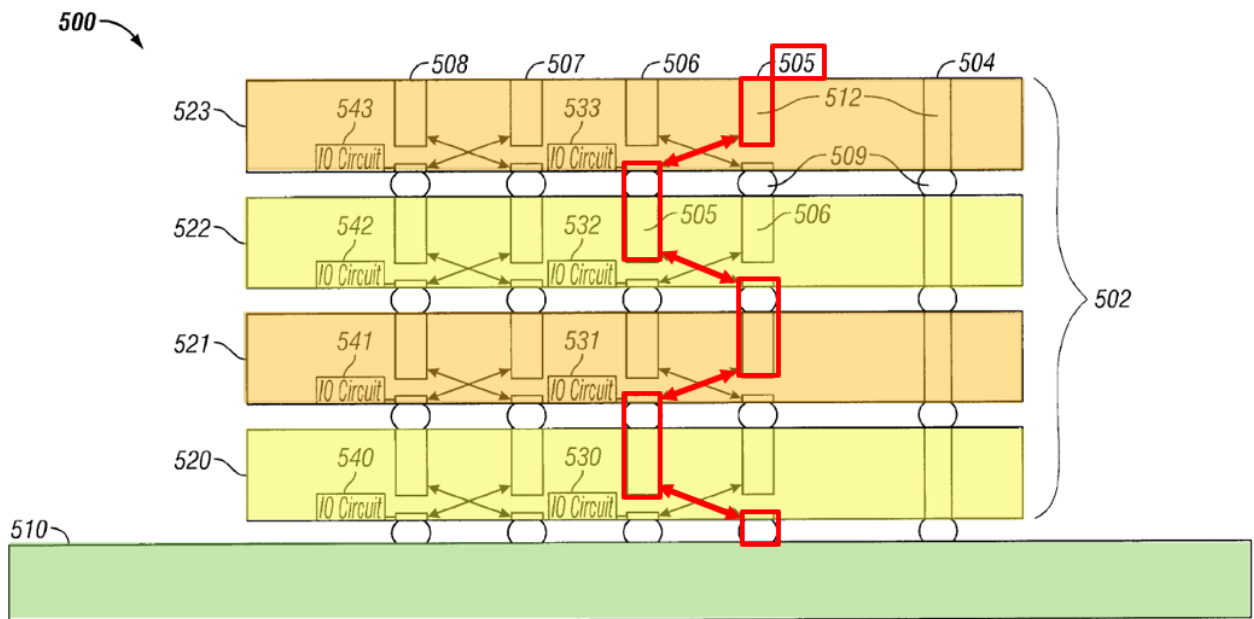


FIG. 5

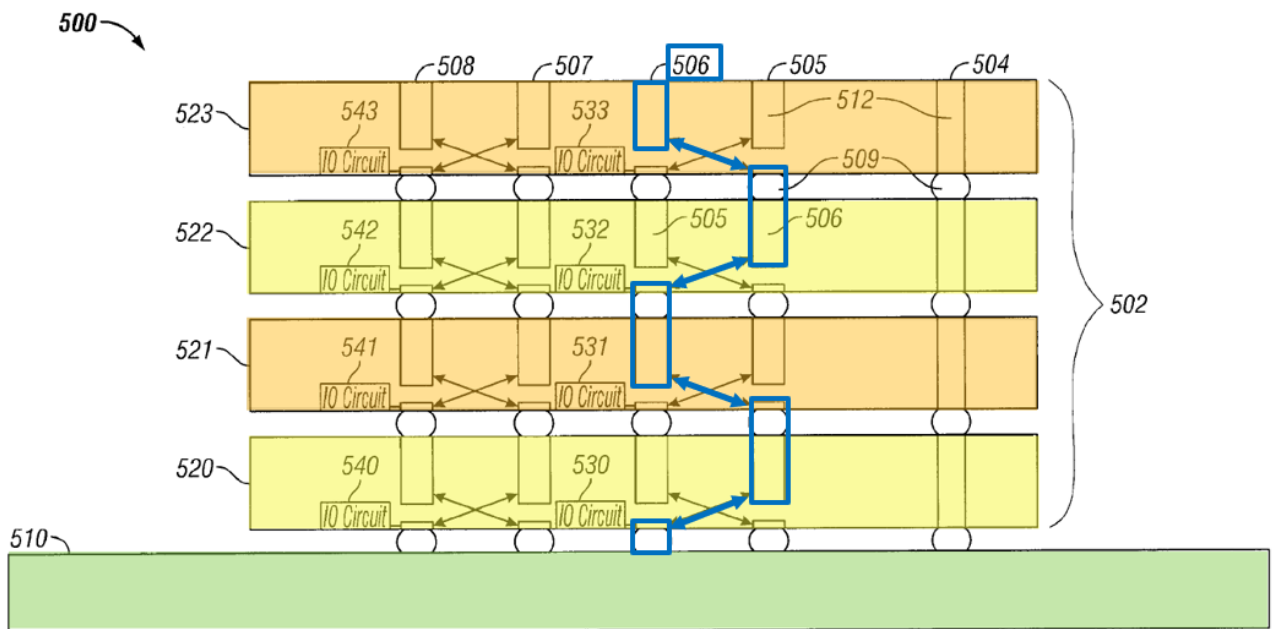


FIG. 5

Similar to the “C/A interconnects,” Keeth teaches using its “interleaving [] connections...[to] concurrently...access and send **data** to[] multiple partitions,”

where the “data interconnects” include “first” and “second data interconnects” coupled to odd and even dies, respectively. EX1047, 4:12-16, 5:63-6:4 (“[I]nterleaving the conductive paths in the dice stack 502...reduce[s] the possibility of queuing data...resulting in increasing bandwidth.”), Abstract, 4:4-12, Fig.5 (above).

Grounds 3-4 further teach “the first data interconnects configured to conduct the first data signals [e.g., read data Q[A0] from Rank 0 below] and the second data signals [e.g., write data D[A1] to Rank 0].” EX1048, Fig.4A (below).

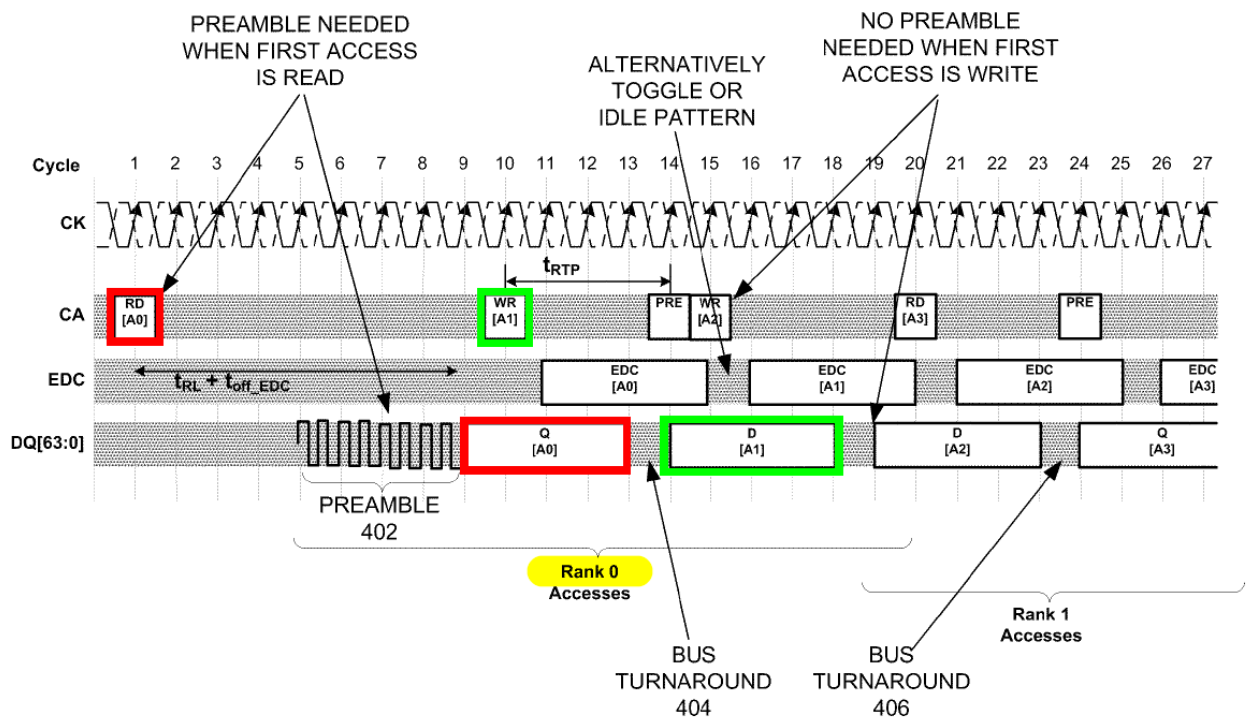


FIG. 4A

As discussed above for [1.d.1] (pp.38-42), Shaeffer teaches both “first” and “second set of C/A signals” are directed to the **same** rank. Accordingly, the “first”

(Q[A0]) and “second data signals” (D[A1]) are read from and written to the **same** rank of memory (or Keeth’s “odd dice” in the combination), and thus conducted by the **same** data interconnects (i.e., “the first data interconnects” coupled to the “odd dice”). EX1048, Fig.4A (above, both Q[A0] and D[A1] conducted by DQ[63:0]).

g) **[1.d.3] TSVs**

Grounds 3-4 teach “each of the die interconnects including one or more through silicon vias (TSVs) [e.g., TSVs 512/712 below] in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals [e.g., by “electrical connections,” EX1047, 2:5] to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs.” EX1047, Figs.5, 7 (below), 7:40 (“TSVs 712”).

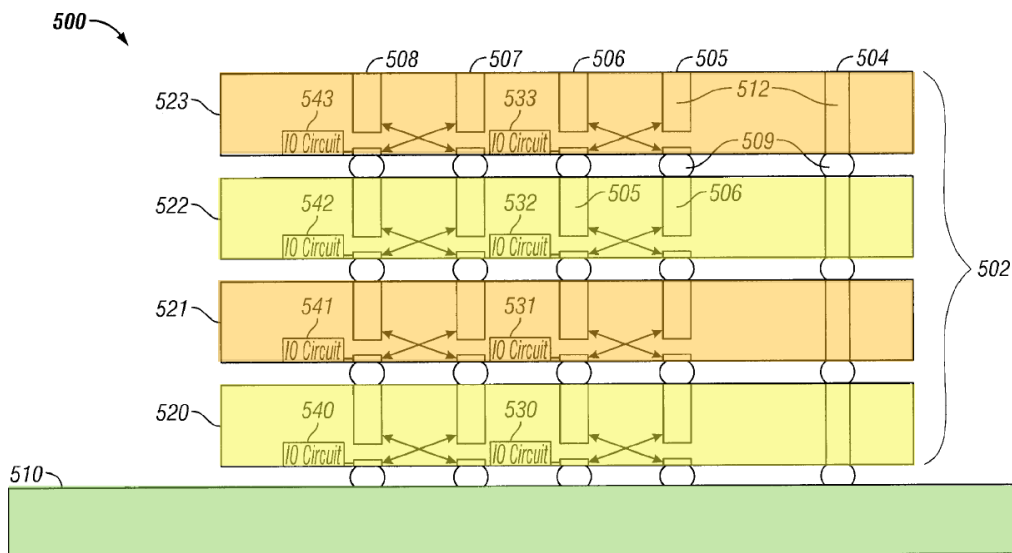


FIG. 5

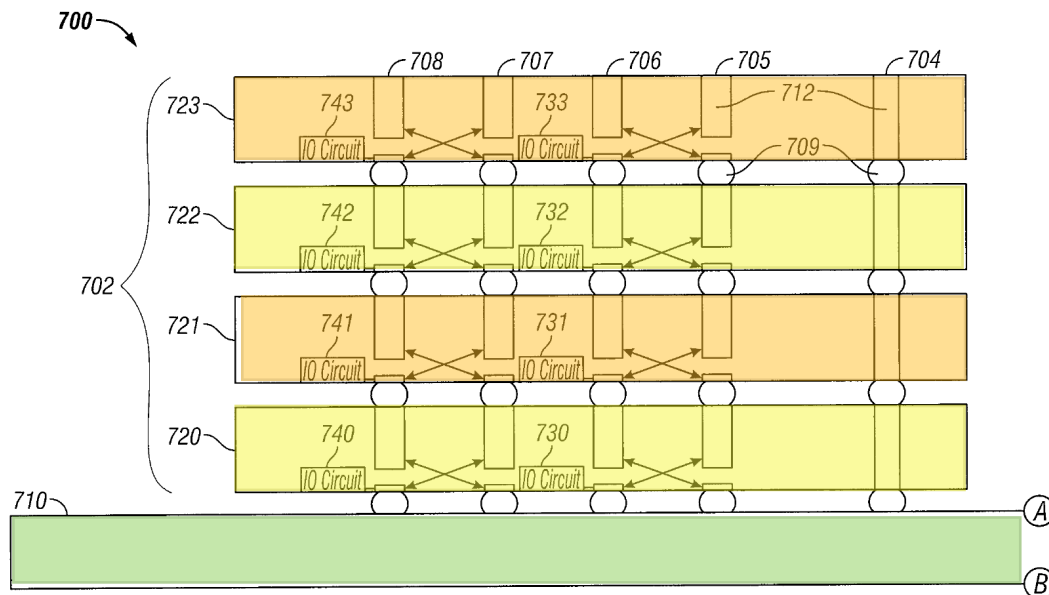


FIG. 7

Keeth discloses that each die interconnect may include “through silicon vias (TSV)” in stacked DRAM dies, EX1047, 1:60-64, which establish “electrical connections,” and thus are used to “conduct signals to and/or from” the stacked DRAM dies, EX1047, 1:65-2:10, 5:34-38 (“conductive paths...include TSVs.”), Figs.6A, 6B (below), 6:30-52 (explaining TSVs 505/506 connected to dies 523/522 in Figs. 6A-B).

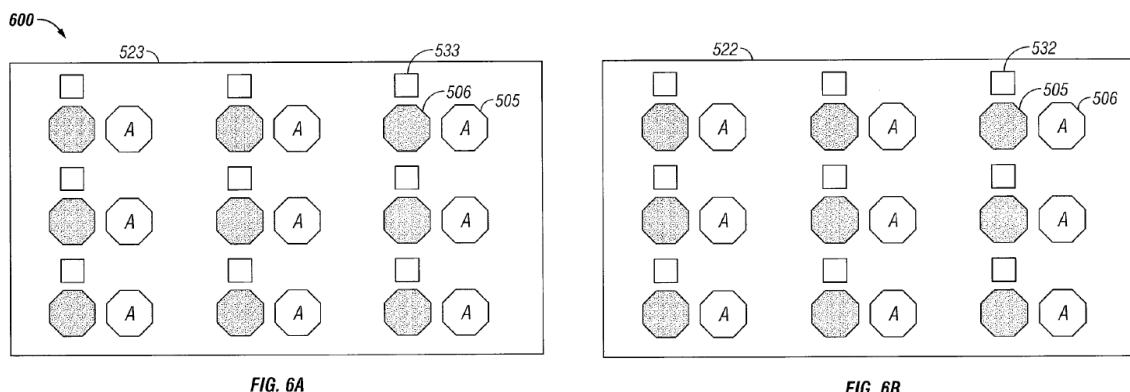


FIG. 6A

FIG. 6B

Similarly, Shaeffer discloses a “through-silicon via (TSV)” to communicate signals with DRAM dies. EX1048, 11:12-15.

h) **[1.e.1] Control die**

Grounds 3-4 teach “a control die [e.g., Keeth’s “interface die” or Shaeffer’s “[local] memory controller”] *coupled between the terminals and the stacked DRAM dies.*” As discussed above for [1.c.1] (pp.34-37), Grounds 3-4 teach the “terminal” via which stacked DRAM dies communicate signals with external devices, e.g., memory controllers. Keeth’s “interface die 210” includes “control circuits 212 to enable communication” between the stacked DRAM dies and the external devices and to control the stacked DRAM dies, EX1047, 3:44-54, Fig.2 (below), thus it is “*coupled between the terminals* [for communication with external devices] *and the stacked DRAM dies.*” See also EX1047, Fig.1 (below, interface die 110 coupled between memory stack 102 and package substrate 114, which may include “terminals”), 2:61-3:20 (“apparatus 100...coupled with external devices...through the interface die”); EX1003, ¶217.

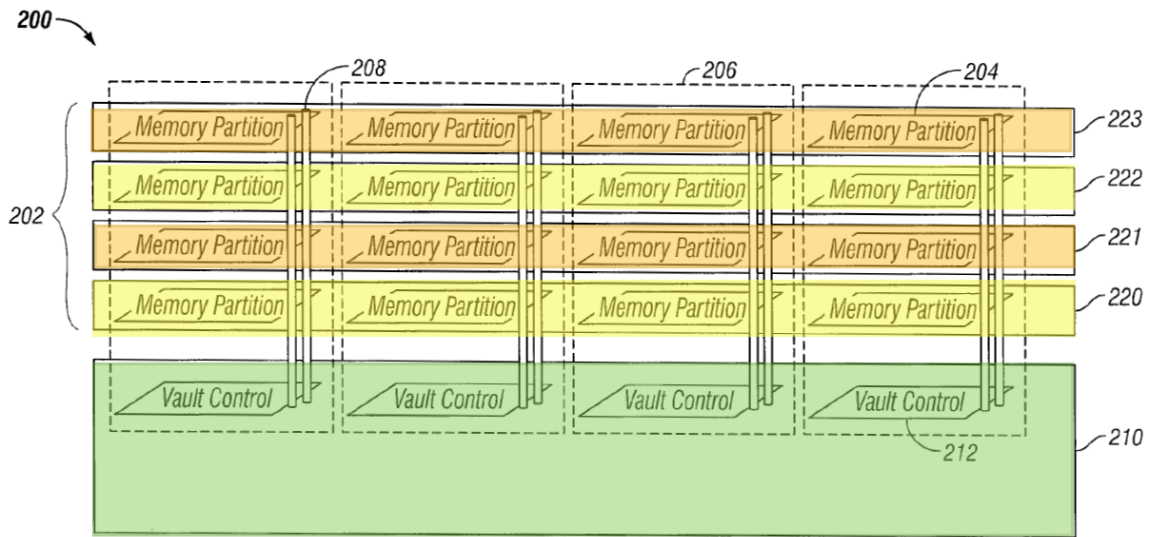


FIG. 2

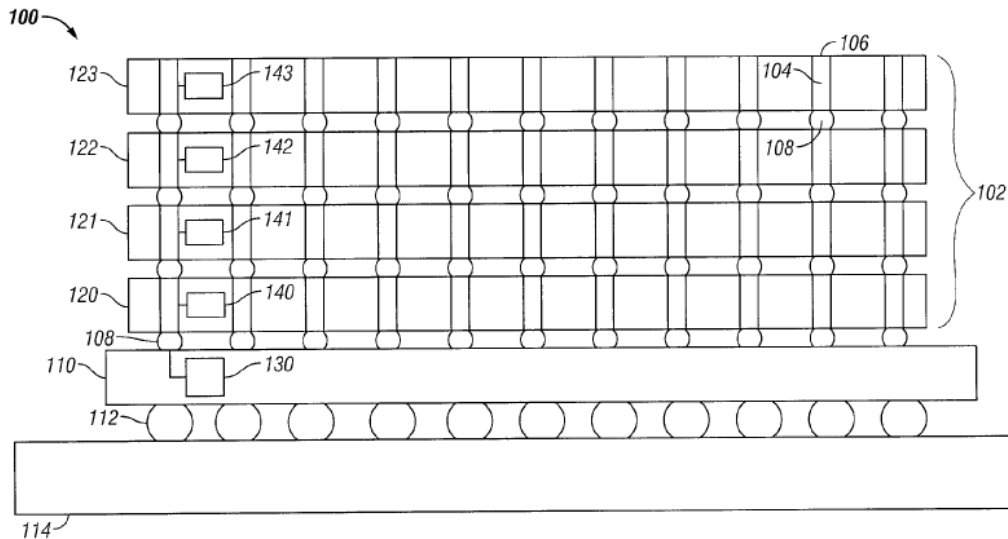


FIG. 1

Similarly, Shaeffer discloses “[local] memory controller 510...stacked with...memory devices 512,” EX1048, 11:10-18, and also coupled with “terminals” to communicate with external processors, EX1048, 11:19-20. EX1003, ¶218.

i) **[1.e.2] Conduits**

Grounds 3-4 teach “*the control die including conduits, the conduits including C/A conduits* [e.g., included in Keeth’s “command and/or addressing circuit” or Shaeffer’s “I/O interface 518-1”] *and data conduits* [e.g., included in Keeth’s “vault control circuit” or Shaeffer’s “I/O interface 518-1”].” The ’087 Patent states that conduits can be drivers to transmit a signal. EX1001, 4:33-34 (“conduit (e.g., driver)”), 6:39-40 (“conduit...to transmit a...signal”). As discussed above for [1.d.1] and [1.d.2] (pp.38-45), Grounds 3-4 teach “C/A” and “data” “interconnects” to conduct respective C/A and data signals between the “control die” and the “stacked DRAM dies.” Keeth further discloses that its “interface die” (i.e., “control die”) includes “a command and/or addressing circuit” for transmitting C/A signals, EX1047, 5:30-34, 6:4-10, and “a vault control circuit” to “access and send data to” memory dies, including “driv[ing] data to” the dies, *id.*, 4:13-16, 6:16-19. Similarly, Shaeffer teaches its “[local] memory controller 510” [i.e., “control die”] may include an I/O interface 518-1,” which transmits “[s]ignals corresponding to data and/or commands” via “the links 54.” EX1048, 11:25-26, 12:4-7, Fig.5 (below), 8:52-54 (“chip-to-chip interfaces”).

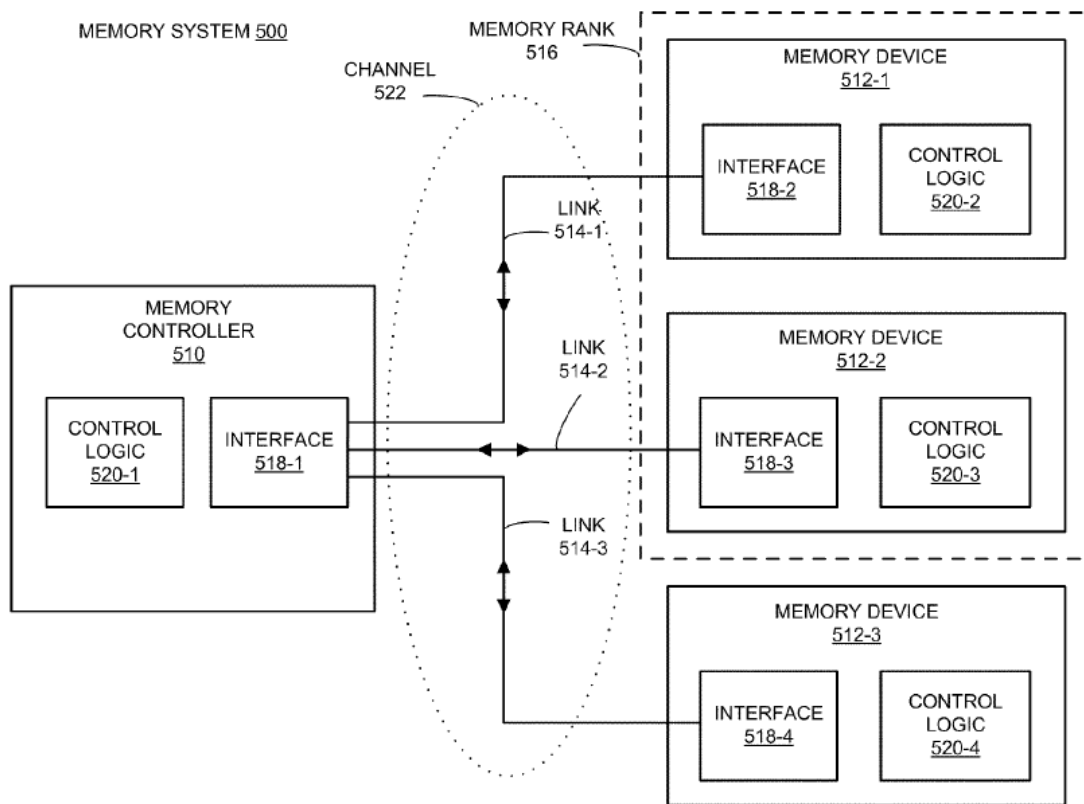
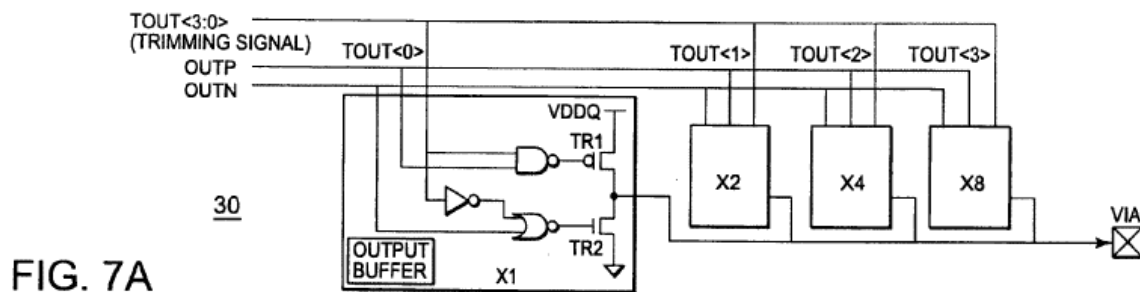


FIG. 5

Keeth's "command and/or addressing circuit" (for C/A) and "vault control circuit" (for data), and Shaeffer's "I/O interface 518-1" (for both C/A and data), include "C/A" and "data" "conduits" to transmit/receive C/A and data signals to/from respective "C/A" and "data" "interconnects." EX1047, 3:62-67 ("Interface die 210 may include...buffers, and I/O drivers."); EX1003, ¶222-223. The "C/A" and "data" "conduits" are separate from one another, *see* EX1048, Fig.1A (separate interface 118 for C/A signals 114 and data signals 120-128), Figs.4A, 4B (C/A and data signals transmitted concurrently, indicating they are driven by their own conduits), and include drivers, *see, e.g.*, EX1047, 3:62-67 ("drivers");

EX1018, Fig.7A (below showing drivers (“output buffer”)), ¶[0097] (“optimizing the output drive capacity of output buffers provided in the interface circuit 30”).

EX1003, ¶223.



j) [1.e.3] C/A conduits

Grounds 3-4 teach “the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects” for the reasons discussed above for [1.e.2] and [1.d.1] (pp.49-51, 38-42). To conduct respective C/A signals to the “first” and “second” “C/A interconnects,” the “C/A conduits” also include “at least first” and “second” “C/A conduits,” coupled to “respective ones of the first” and “second” “C/A interconnects.” See also EX1047, 6:19-24 (“conductive paths” for C/A signals coupled to their respective “command and/or address circuitry” on the interface die so “each vault may be independently controlled”); EX1048, 12:15-19 (“separate command link” for “commands”).

k) **[1.e.4] Data conduits**

Grounds 3-4 teach “*the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects*” for the reasons discussed above for [1.e.2] and [1.d.2] (pp.49-51, 42-45). To conduct respective data signals to the “*first*” and “*second data interconnects*,” the “*data conduits*” also include “*at least first*” and “*second*” “*data conduits*,” coupled to “*respective ones of the first*” and “*second*” “*data interconnects*.” EX1047, 6:16-19 (“interface die 510 to...**concurrently drive** data to partitions”); EX1048, 12:4-7 (“[D]ata...communicated on one or more of the links 514”).

l) **[1.f] First C/A interconnect and electrical communication**

Grounds 3-4 teach “*a first C/A interconnect of the first C/A interconnects* [e.g., included in “conductive paths 507” (red) below from [1.d.1] (pp.38-42)] *is in electrical communication with corresponding C/A ports* [e.g., included in I/O Circuits 543/541 (red) from [1.b.2] (pp.30-33)] *on the first plurality of DRAM dies* [e.g., odd dies 523/521 (orange) from [1.b.1] (pp.28-30)] *and not in electrical communication with any C/A port* [e.g., included in I/O Circuits 542/540 (blue) from [1.b.2] (pp.30-33)] *on any of the second plurality of DRAM dies* [e.g., even dies 522/520 (yellow) from [1.b.1] (pp.28-30)].” EX1047, Fig.5 (annotated below).

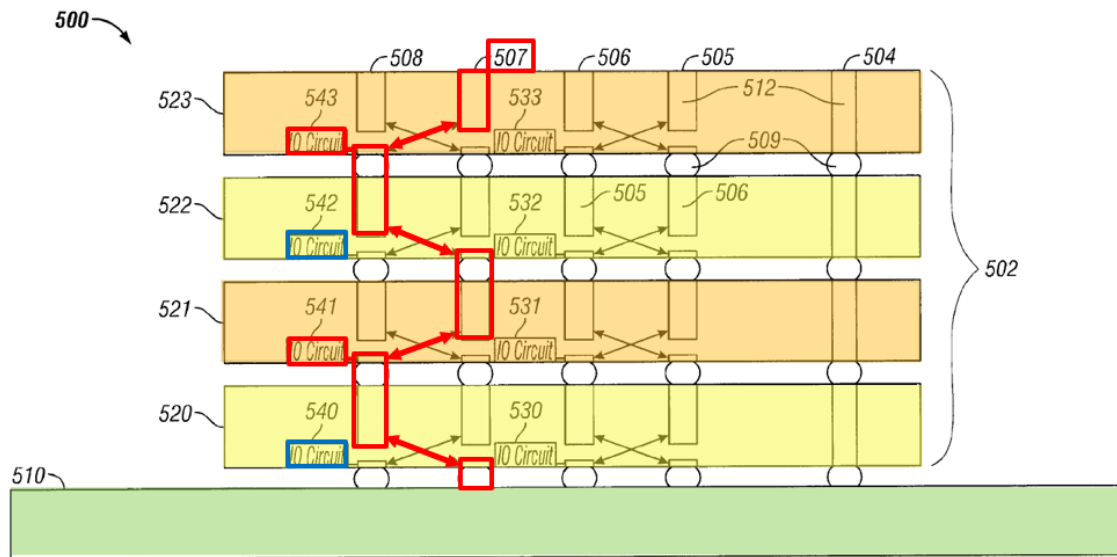


FIG. 5

As explained above for [1.b.2] and [1.d.1] (pp.30-33, 38-42), Keeth's "conductive paths" for "address, control," EX1047, 3:5-8, include "*first C/A interconnects*," and each DRAM die includes "*C/A ports* [e.g., "command circuits and/or address circuits" in "I/O Circuits" above]" to communicate C/A signals. Also, as shown above, Keeth's conductive paths implement interleaving connections, where the paths are coupled to alternating dies. EX1047, Fig.5 (above), 4:4-9 ("[A] first communication path in a vault may be connected to circuitry...of all odd partitions in the memory vault and pass through the even vaults without connecting to circuitry."), 6:30-41, Abstract ("conductive paths...arranged to connect with circuitry on alternating dice of the stack"). Keeth also teaches when the conductive paths are coupled to I/O Circuits, they are "*in electrical communication with*" each other. *Id.* 6:4-10 ("[C]ommand circuits

and/or address circuits [in I/O Circuits]...connected to...the interleaving conductive paths...in order to **communicate** command and/or address signals”).

m) ***[1.g] Second C/A interconnect and electrical communication***

Grounds 3-4 teach “*wherein a second C/A interconnect of the second C/A interconnects [e.g., included in “conductive paths 508” (blue) below from [1.d.1] (pp.38-42)] is in electrical communication with corresponding C/A ports [e.g., included in I/O Circuits 542/540 (blue) from [1.b.2] (pp.30-33)] on the second plurality of DRAM dies [e.g., even dies 522/520 (yellow) from [1.b.1] (pp.28-30)] and not in electrical communication with any C/A port [e.g., included in I/O Circuits 543/541 (red) from [1.b.2] (pp.30-33)] on any of the first plurality of DRAM dies [e.g., odd dies 523/521 (orange) from [1.b.1] (pp.28-30)],*” as explained above for [1.f] (pp.52-54). EX1047, Fig.5 (annotated below), 4:9-16 (“[A] second communication path may connect to circuitry...on the even partitions...and pass through the odd partitions without connecting to circuitry.”).

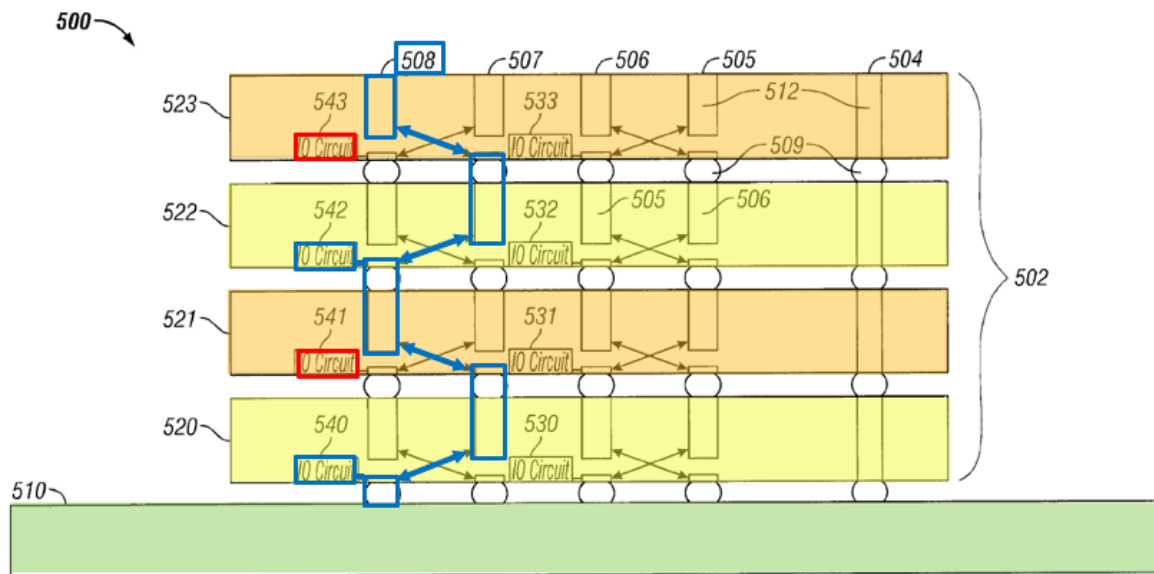


FIG. 5

n) **[1.h.1] First data interconnect and electrical communication**

Grounds 3-4 teach “wherein a first data interconnect of the first data interconnects [e.g., included in “conductive paths 505” (red) below from [1.d.2] (pp.42-45)] is in electrical communication with corresponding data ports [e.g., included in I/O Circuits 533/531 (red) from [1.b.2] (pp.30-33)] on the first plurality of DRAM dies [e.g., odd dies 523/521 (orange) from [1.b.1] (pp.28-30)] and not in electrical communication with any data port [e.g., included in I/O Circuits 532/530 (blue) from [1.b.2] (pp.30-33)] on any of the second plurality of DRAM dies [e.g., even dies 522/520 (yellow) from [1.b.1] (pp.28-30)].” EX1047, Figs.5, 7 (annotated below), 7:7-20 (interleaving connections in Fig.7).

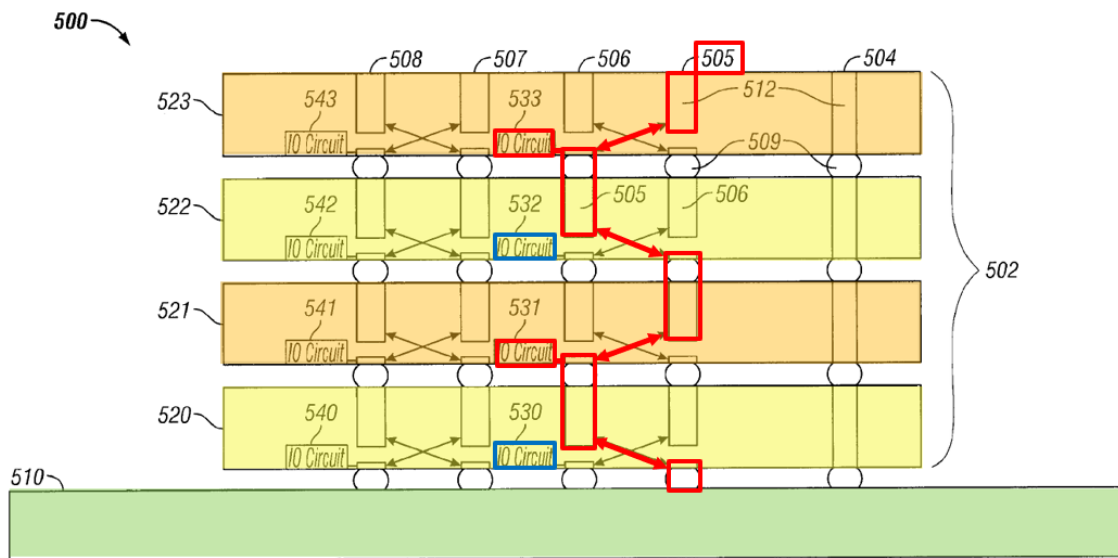


FIG. 5

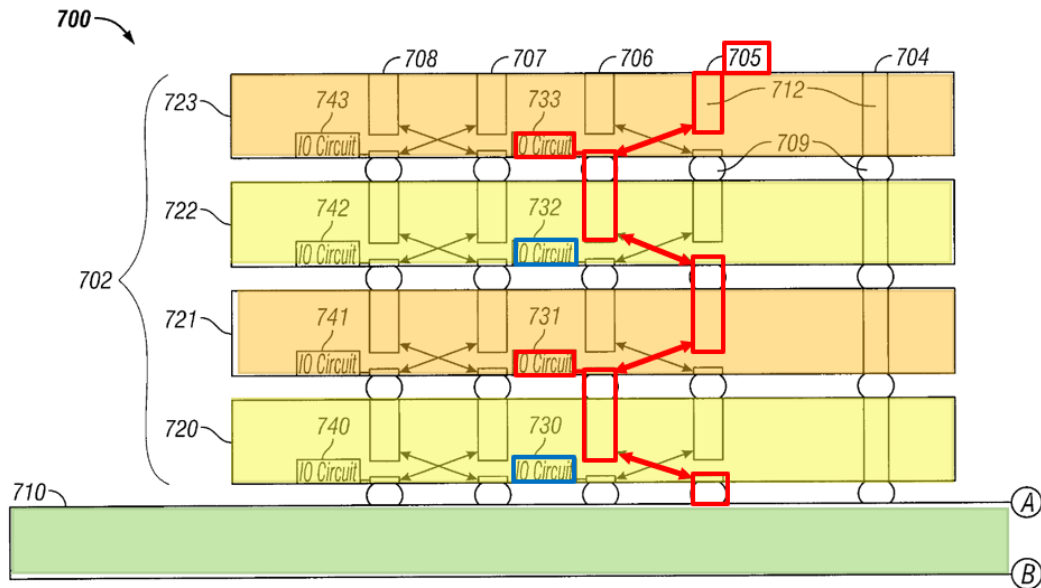


FIG. 7

As explained above for [1.b.2] and [1.d.2] (pp.30-33, 42-45), Keeth's “conductive paths” for “data,” EX1047, 3:5-8, include “*first data interconnects*,” and each DRAM die includes “*data ports* [e.g., “input/output circuitry” in “I/O Circuits” above]” to communicate data signals. Also, similar to [1.f]-[1.g] (pp.52-

55), Keeth's interleaving connections meet this limitation of selective data interconnects. As shown above, the conductive paths 505 (which include "*a first data interconnect*") are coupled to, thus "*in electrical communication with,*" I/O Circuits 533/531 (which include "*corresponding data ports*") on odd dies 523/521 ("*first plurality of DRAM dies*"), but are not coupled to, thus "*not in electrical communication with any data port,*" on even dies 522/520 ("*second plurality of DRAM dies*"). EX1047, Fig.5 (above), 4:4-9, 6:16-19 ("interface die 510 to concurrently...drive data to partitions"), Abstract, 6:30-41 (explaining TSVs are connected or disconnected with circuitry on a corresponding die for interleaving connection).

o) ***[1.h.2] TSVs in first data interconnects***

Grounds 3-4 teach "*each of the first data interconnects including a first respective set of TSVs [e.g., TSVs 512 (solid/dashed red) in "conductive paths 505" below], the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies [e.g., a TSV (solid red) in each odd die of 523/521 (orange)] and at least one TSV in at least one DRAM die of the second plurality of DRAM dies [e.g., at least one TSV (dashed red) in at least one even die of 522/520 (yellow)].*" EX1047, Fig.5 (annotated below).

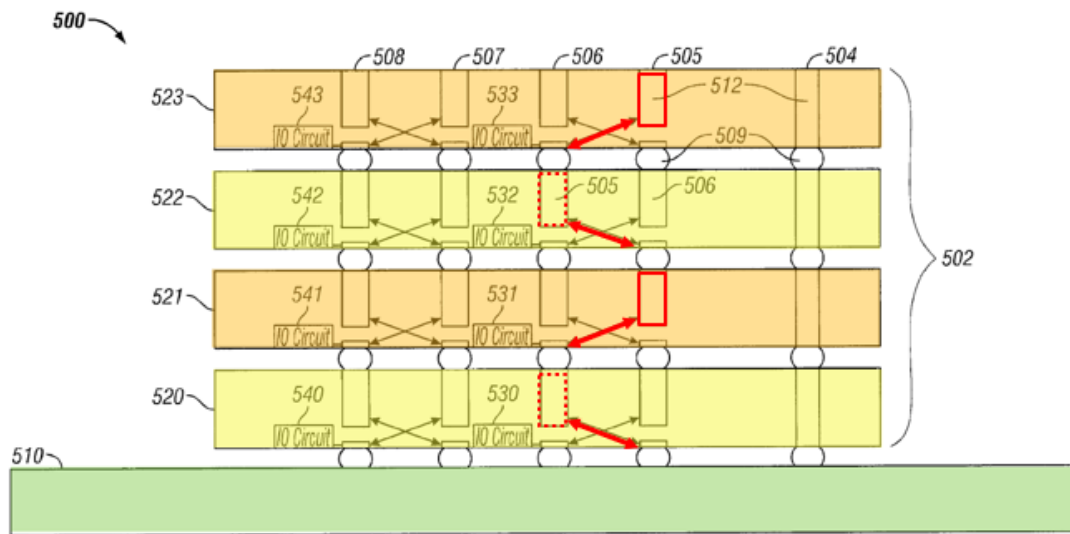


FIG. 5

As discussed above for [1.d.3] (pp.45-47), each DRAM die includes a TSV for each die. EX1047, Fig.5 (above), 5:34-38 (“[T]he conductive paths...may include TSVs”). Thus, when “the conductive paths...entirely pass through...the dice stack 502,” EX1047, 5:34-38, each conductive path includes a respective set of TSVs (512), including “a TSV in each DRAM die of the first plurality of DRAM dies [e.g., odd dies] and at least one TSV in at least one DRAM die of the second plurality of DRAM dies [e.g., even dies].” See also EX1047, Fig.7 (annotated below), 7:37-45 (“conductive paths 704 [through] 708” including “TSVs 712”).

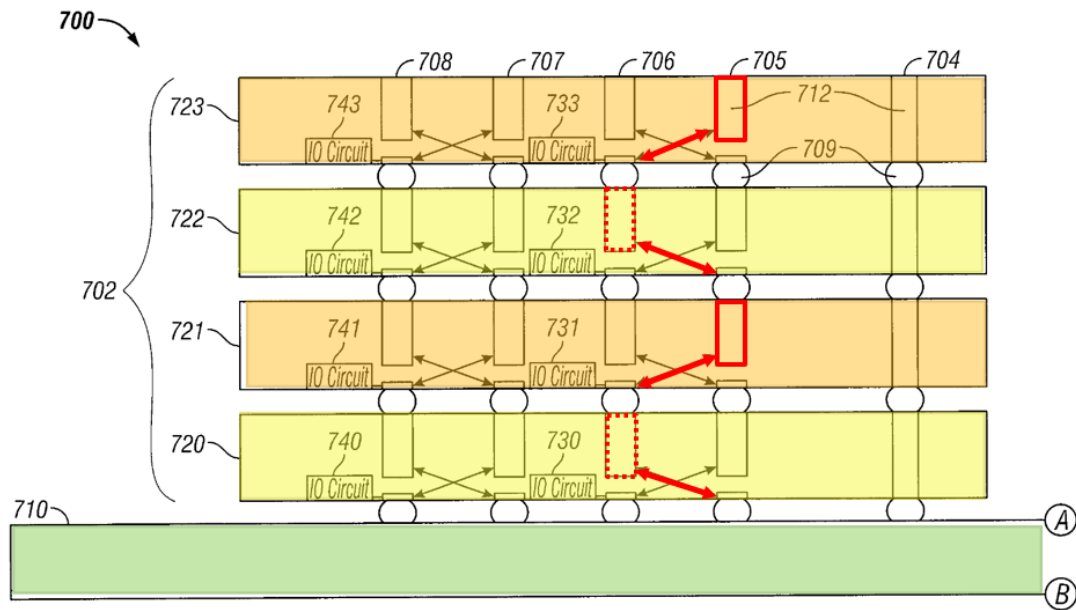


FIG. 7

p) **[1.h.3] TSVs and electrical communication**

Grounds 3-4 teach “wherein the TSV in the each DRAM die of the first plurality of DRAM dies [e.g., the TSV (solid red) in each odd die of 523/521 (orange) below, from [1.h.2] (pp.57-59)] is in electrical communication with a corresponding data port on the each DRAM die [e.g., a corresponding data port included in I/O Circuits 533/531 (solid red) (from [1.h.1] (pp.55-57) is in electrical communication with the TSVs (solid red)], and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies [e.g., at least one TSV (dashed red) in at least one even die of 522/520 (yellow) from [1.h.2] (pp.57-59)] is not in electrical communication with any data port on the at least one DRAM die [e.g., any data port included in I/O Circuits 532/530 (blue) (from [1.h.1] (pp.55-57)

is not in electrical communication with the at least one TSV (dashed red)].”

EX1047, Figs.5, 7 (annotated below), 1:60-64 (“TSVs” for “[e]lectrical connection”), 7:7-20 (interleaving connections in 702), 7:37-45 (“TSVs 712”).

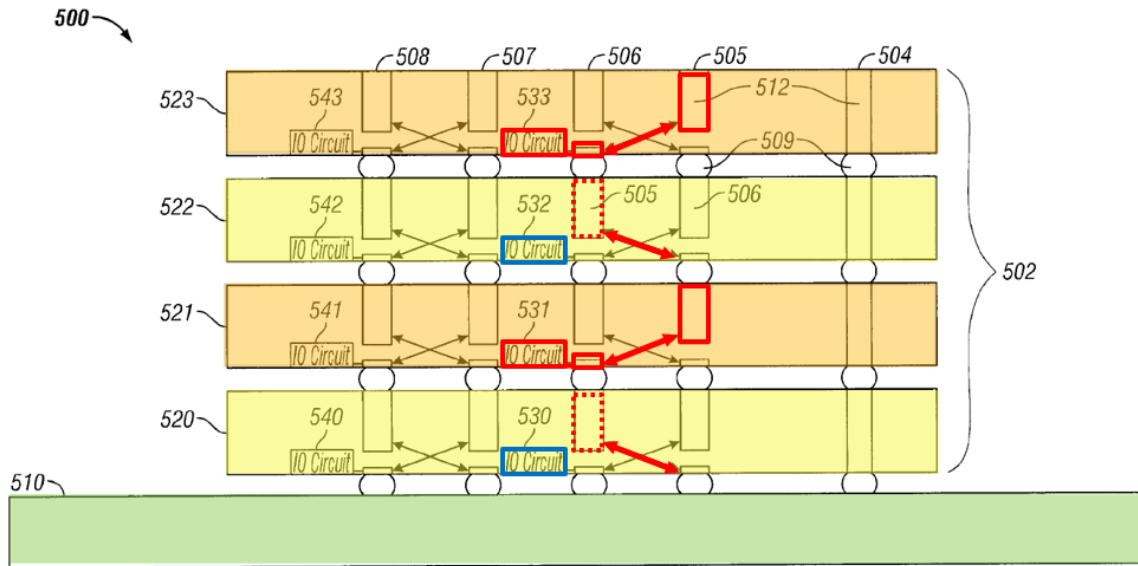


FIG. 5

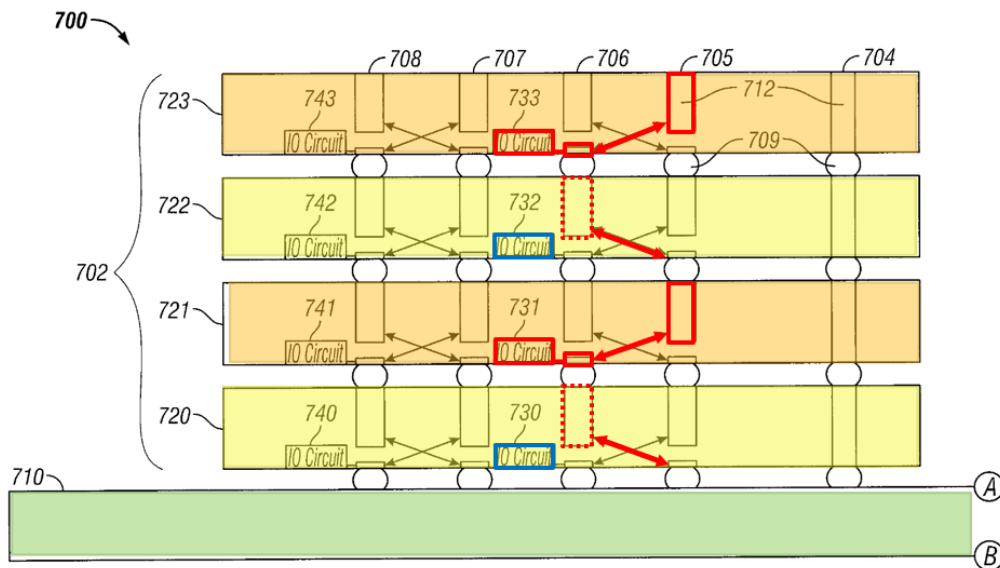


FIG. 7

q) ***[1.i] Second data interconnect and electrical communication***

Grounds 3-4 teach “*wherein a second data interconnect of the second data interconnects [e.g., included in “conductive paths 506” (blue) below, from [1.d.2] (pp.42-45)] is in electrical communication with corresponding data ports [e.g., included in I/O Circuits 532/530 (blue) from [1.b.2] (pp.30-33)] on the second plurality of DRAM dies [e.g., even dies 522/520 (yellow) from [1.b.1] (pp.28-30)] and not in electrical communication with any data port [e.g., included in I/O Circuits 533/531 (red) from [1.b.2] (pp.30-33)] on any of the first plurality of DRAM dies [e.g., odd dies 523/521 (orange) from [1.b.1] (pp.28-30)],*” as explained above for [1.h.1] (pp.55-57). EX1047, Figs.5, 7 (annotated below), 4:9-16 (“[A] second communication path may connect to circuitry...on the even partitions...and pass through the odd partitions without connecting to circuitry.”), 7:7-20.

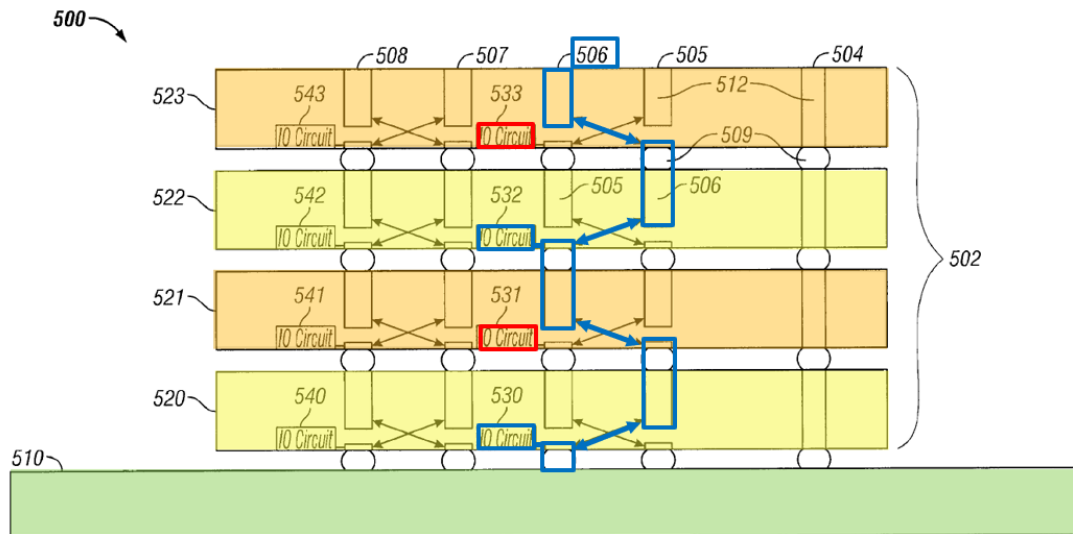


FIG. 5

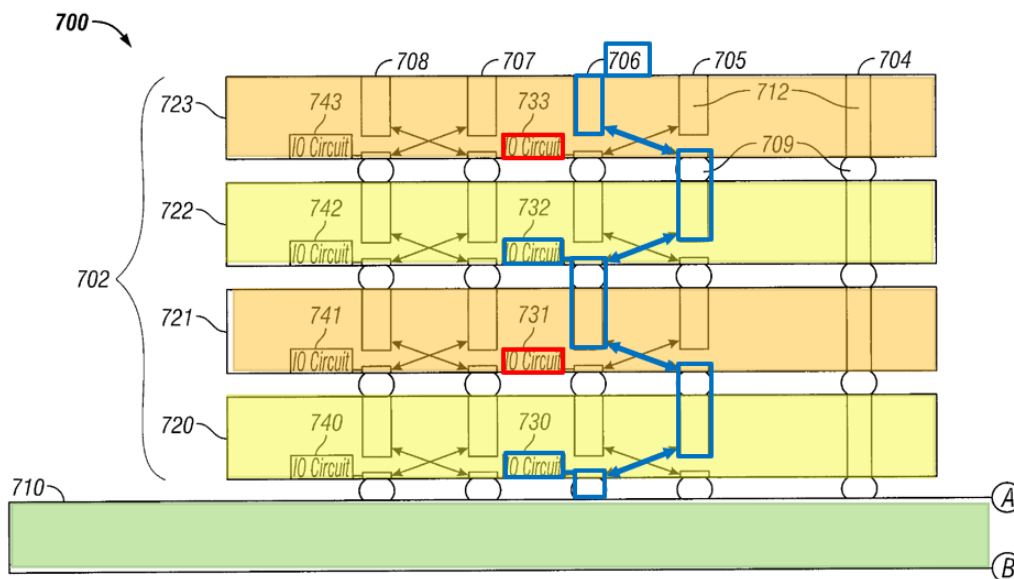


FIG. 7

r) **[1.j] First/second conduit**

Grounds 3-4 teach “wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the

second data interconnect and the first data terminal [e.g., to improve bandwidth while preserving power].” For the reasons discussed above for [1.e.2] and [1.e.4], (pp.49-51, 52), Grounds 3-4 disclose “*a first*” and “*second*” “*conduit...coupled ...[to]*” the “*first*” and “*second*” “*data interconnect*,” respectively, to communicate data between the control die and stacked DRAM dies via the respective “*data interconnect[s]*.” Also, for the reasons discussed above for [1.c.1] and [1.e.1], (pp.34-37, 47-48), Grounds 3-4 disclose “*a first data terminal*” to communicate data with an external device, such as a processor. Keeth also teaches the stacked DRAM dies “may share...input/output data pins” on the interface die to improve bandwidth. EX1047, 1:65-2:10. Bandwidth improves by “concurrently...access[ing] and send[ing] data to...multiple partitions” (e.g., odd and even dies) that share the I/O data pins. *Id.*, 4:4-16, 5:63-67 (“[T]he interface die 510 may concurrently access dice 520 through 523, thereby increasing bandwidth.”); EX1003, ¶227. Thus, a POSITA would have been motivated to couple the “*first conduit*” (connected to the “*first data interconnect*” to access, e.g., the odd dies) and the “*second conduit*” (connected to the “*second data interconnect*” to access, e.g., the even dies) to the same “*first data terminal*” (so that the even and odd dies share I/O data pins to improve bandwidth), as this limitation requires. *Id.* Further, such coupling would allow for communication at “appropriate data transfer rates” with a processor, EX1047, 3:62-67, which may be

higher (e.g., for high-speed computers) than those inside the stacked DRAM package. EX1056, Abstract, 1; EX1003, ¶228. Namely, the higher data rate with a processor on the “*first data terminal*” is accommodated by two lower-rate communication paths comprising the “*first*” and “*second conduit*” leading to respective dies (e.g., odd and even dies). *Id.* As discussed above (pp.27-28), operating internal paths at lower rates than the external processor’s rate reduces power and increases yield. EX1018, ¶¶[0008], [0052], [0148]; EX1003, ¶229. Also, it was within the skill in the art to implement such a down rate-conversion by using, for example, parallel-to-serial and serial-to-parallel converters. EX1018, ¶[0053]; *supra* pp.27-28; EX1003, ¶229.

s) **[1.k.1] control logic**

Grounds 3-4 teach “*wherein the control die further includes control logic [e.g., in “vault control circuit 212” below] configurable to control respective states of the first and second conduits [e.g., receiving/transmitting] in response to one or more C/A signals received via one or more of the C/A terminals.*” As discussed above for [1.c.1] (pp.34-37), the grounds disclose “*C/A terminals...to receive C/A signals.*” Keeth further teaches that its “interface die 210” includes “vault control circuit 212” to “concurrently...access and send data to” multiple dies. EX1047, 4:4-16, Fig.2 (annotated below), 3:44-54 (“control circuits 212 to enable communication and control with the corresponding memory partition 204

stacked”). The “vault control circuit 212” includes “*control logic*” to control the states of the “*first and second conduits*” to communicate with multiple dies “*in response to one or more C/A signals,*” e.g., for read/write. EX1003, ¶233. For example, the “*control logic*” controls the state of each conduit to be a receiving (or transmitting) state to read data from (or write data to) a die in response to a read (or write) command. *Id.*

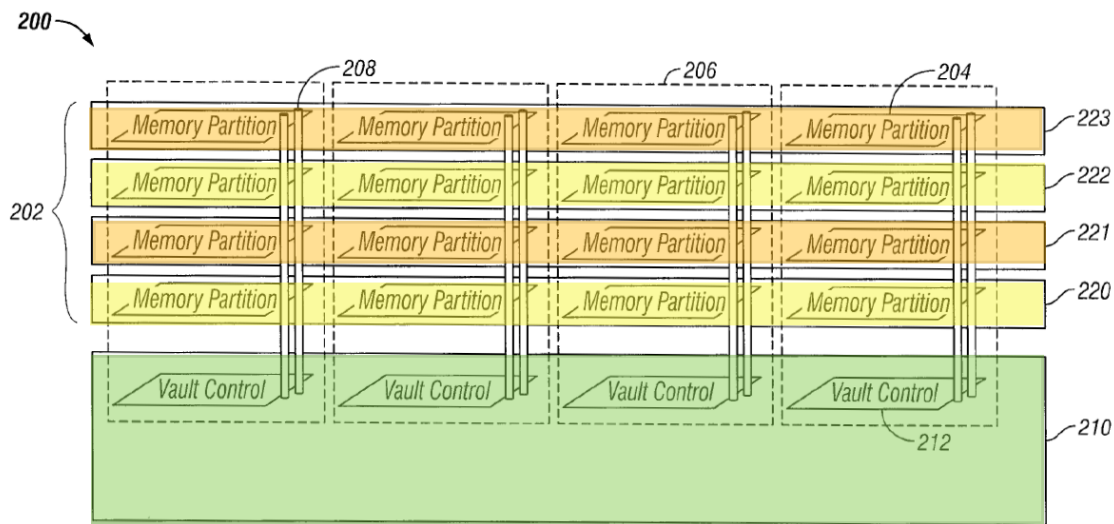


FIG. 2

t) **[1.k.2] no chip select signal**

Grounds 3-4 teach “*wherein the one or more C/A signals [for 1.k.1 directly above] do not include any chip select signal [e.g., instead using TRS signals (for read) or sending data on both conduits and then using a separate chip select signal directly applied to the DRAM dies (for write)].*” As [1.j] (pp.62-64) requires, the “*first and second conduits*” are tied to the same “*first data terminal,*” essentially in

a “fork-in-the-road” arrangement. Thus, those “*conduits*” need to be selectively controlled to prevent data collisions through the “*first data terminal*.” See, e.g., EX1001, 15:31-16:25 (data drivers controlled by “a chip select signal” to “drive a signal to the array die corresponding to the chip select signal”); EX1003, ¶237. Netlist contends limitation [1.k.2] is satisfied by stack ID (SID) information, EX1089, 70-71, which Keeth also teaches, EX1047, 3:5-8, 3:21-38 (“ID information...for control circuit...to reference each die”). EX1003, ¶¶238-239. Grounds 3-4 also teach additional ways for controlling the “*first and second conduits*” without “*any chip select signal*,” while preventing data collisions. EX1003, ¶¶240-243. For example, for read operations, Shaeffer discloses using “timing preamble,” like “TRS signal burst,” that precedes the “corresponding read data.” EX1048, 2:3-6, 10:3-19, Figs.2-4B. Shaeffer further teaches such a preamble signal provides timing information to correctly capture the data. EX1048, 2:36-44. Accordingly, a POSITA would have been motivated to control the state of “*the first and second conduits*” during read operations based on the “timing preamble” or the “TRS signal burst” (i.e., without “*a chip select signal*”), so that read data are correctly captured and transmitted without a collision. EX1003, ¶¶240-241. For write operations, data can be transmitted from the “*first data terminal*” through both “*first and second conduits*,” and then “each partition may have a different chip select line” to select the memory die to receive the data.

EX1047, 2:6-10; EX1003, ¶242. Thus, “*a chip select signal*” is directly applied to the memory dies without being involved in controlling the “*first and second conduits*.” *Id.* Also, a POSITA would have been motivated to transmit write data via both “*conduits*” for a faster operation. EX1026, ¶[0033] (“[T]o meet system timing requirements, write data is sent to both ports.”); EX1003, ¶242. Thus, Grounds 3-4 teach controlling the “fork-in-the-road” without “*a chip select signal*” for both read and write. EX1003, ¶243.

u) ***[1.1] first unidirectional interconnects***

Grounds 3-4 teach “*wherein the die interconnects further include first unidirectional interconnects [e.g., Shaeffer’s “interface 118” for TRS/EDC Signal 130 below as implemented in Keeth’s die interconnects] configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die [e.g., TRS/EDC Signal 130] and not configured to conduct any signal from the control die to any of the stacked DRAM dies.*” EX1048, Figs.1A, 4B (below).

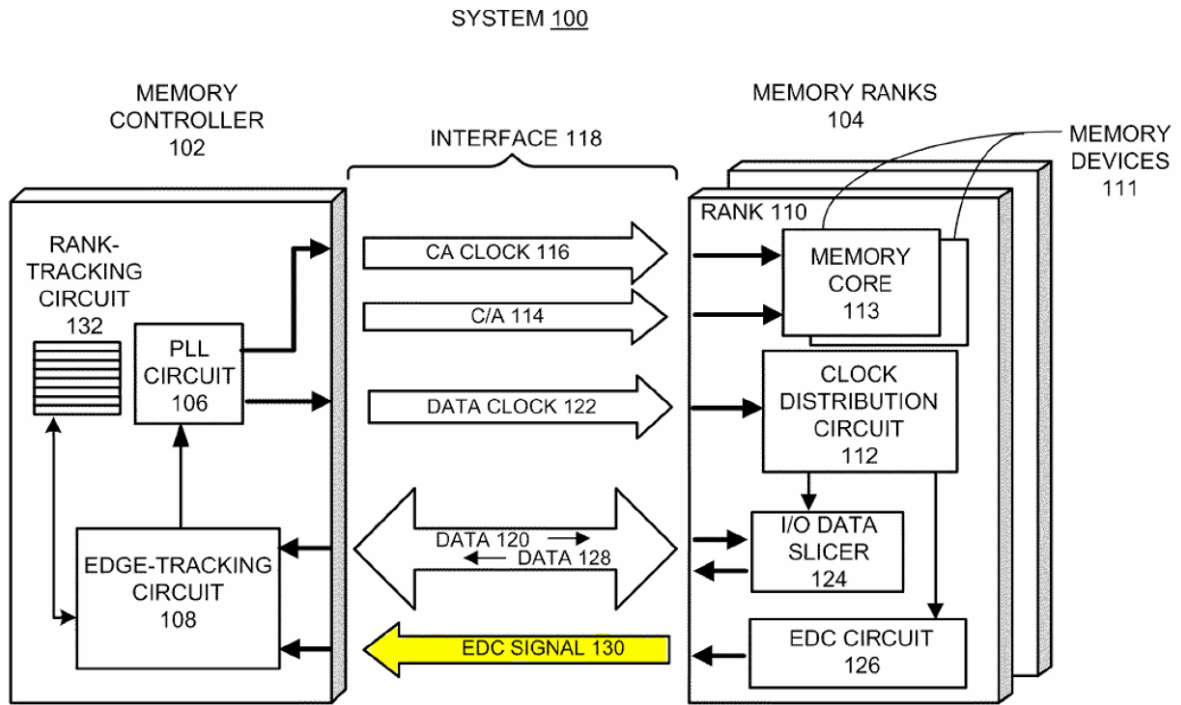


FIG. 1A

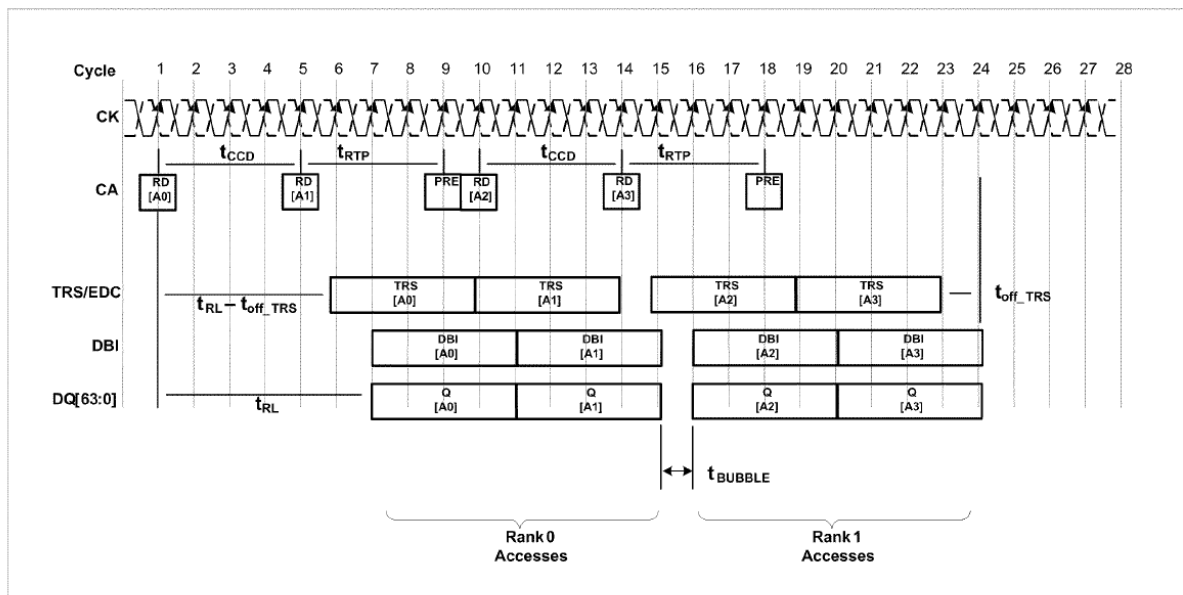
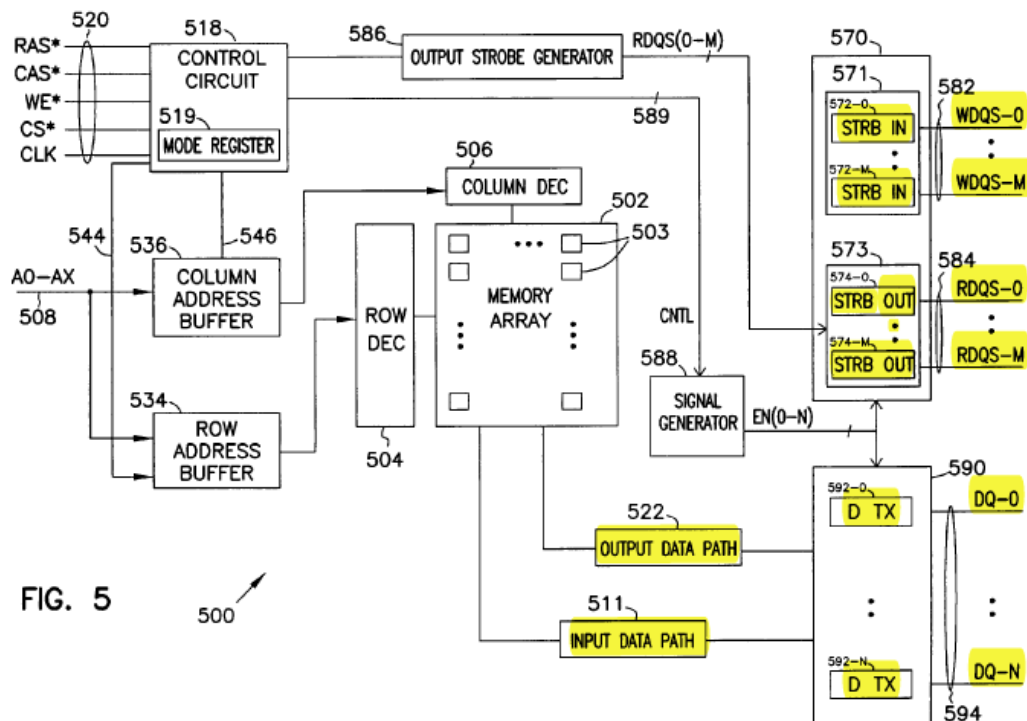


FIG. 4B

As discussed above (pp.11-24), a POSITA would have implemented Shaeffer's TRS/EDC signaling in Keeth's die interconnects. As shown in Fig.1A above, Shaeffer discloses TRS/EDC Signal 130 is conducted via interface 118 unidirectionally from memory dies to the control die. EX1048, 2:64-3:4 (transmitting TRS), 3:39-51 (transmitting EDC), 11:54-57 (interface may be "unidirectional"); EX1003, ¶¶247-248. Unidirectional signals from memory dies to a controller, like TRS/EDC, were also well known in the art, for example, to time data transactions. See, e.g., EX1051, Fig.5 (below, read strobe signals RDQS-0-M); EX1003, ¶249.



Thus, the interface for TRS/EDC Signal 130, when implemented in Keeth's stacked memory as interconnects to transmit the signal only from memory dies to the control die, is "*configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal*" in reverse. EX1003, ¶¶247-249.

v) ***[1.m] second unidirectional interconnects***

Grounds 3-4 teach "*wherein the die interconnects further include second unidirectional interconnects [e.g., Shaeffer's "interface 118" for "Data Clock 122" below as implemented in Keeth's die interconnects] configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies [e.g., "Data Clock 122"] and not configured [to] conduct any signal from any of the stacked DRAM dies to the control die.*" EX1048, Fig.1A (below).

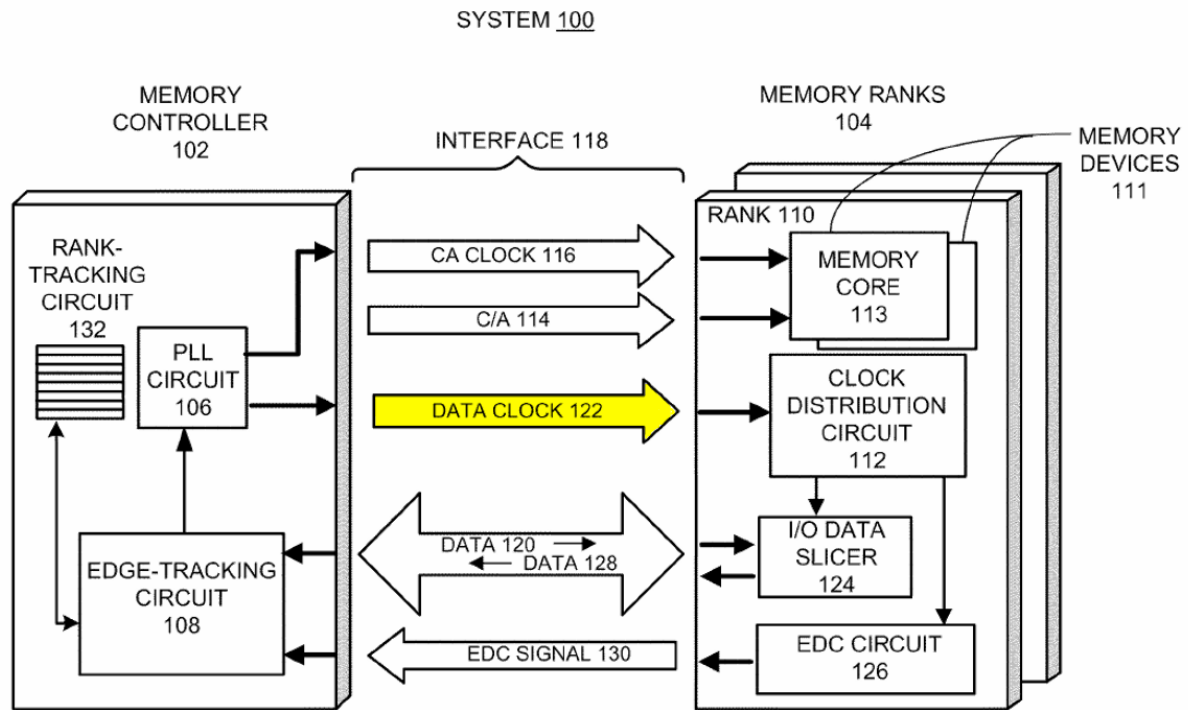


FIG. 1A

As discussed above (pp.11-24), the combination of Shaeffer's signaling and Keeth's die interconnects would have been obvious. As shown in Fig.1A above, Shaeffer discloses Data Clock 122, which may be implemented as a write strobe signal, is conducted via interface 118 unidirectionally from the control die to memory dies. EX1048, 9:1-10 (Data Clock used as "a strobe signal" to "sample data"), 3:35-38 (write data "directly clocked by" Data Clock), 11:54-57 (interface may be "uni-directional"); EX1003, ¶253. Write strobe signals, unidirectional to memory dies, were also well known. *See, e.g.,* EX1051, Fig. 5 (below, WDQS-0-M); EX1003, ¶253.

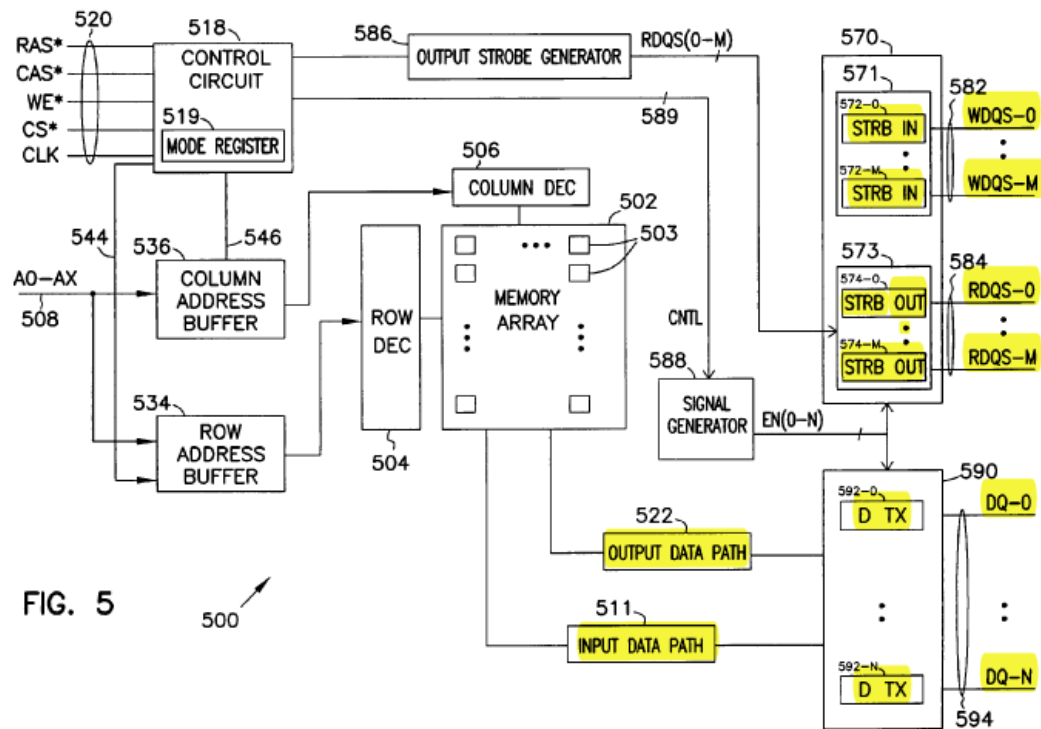


FIG. 5

Thus, the interface for Data Clock 122, when implemented in Keeth's stacked memory as interconnects to transmit a write strobe signal only from the control die to memory dies, is *"configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured [to] conduct any signal"* in reverse. *Id.*

w) **[1.n] control die and first unidirectional interconnects**

Grounds 3-4 teach *"wherein the control die is configured to receive signals [e.g., TRS/EDC Signal 130 below] from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects [e.g., Shaeffer's "interface 118" for TRS/EDC Signal 130 as implemented in Keeth's die interconnects] and is*

not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects” for the reasons explained for [1.I] (pp.67-70).

EX1048, Figs.1A, 4B (below, “memory controller 102” receiving TRS/EDC Signal 130 via “interface 118” from “memory devices 111,” without driving back any signal via the same interconnects).

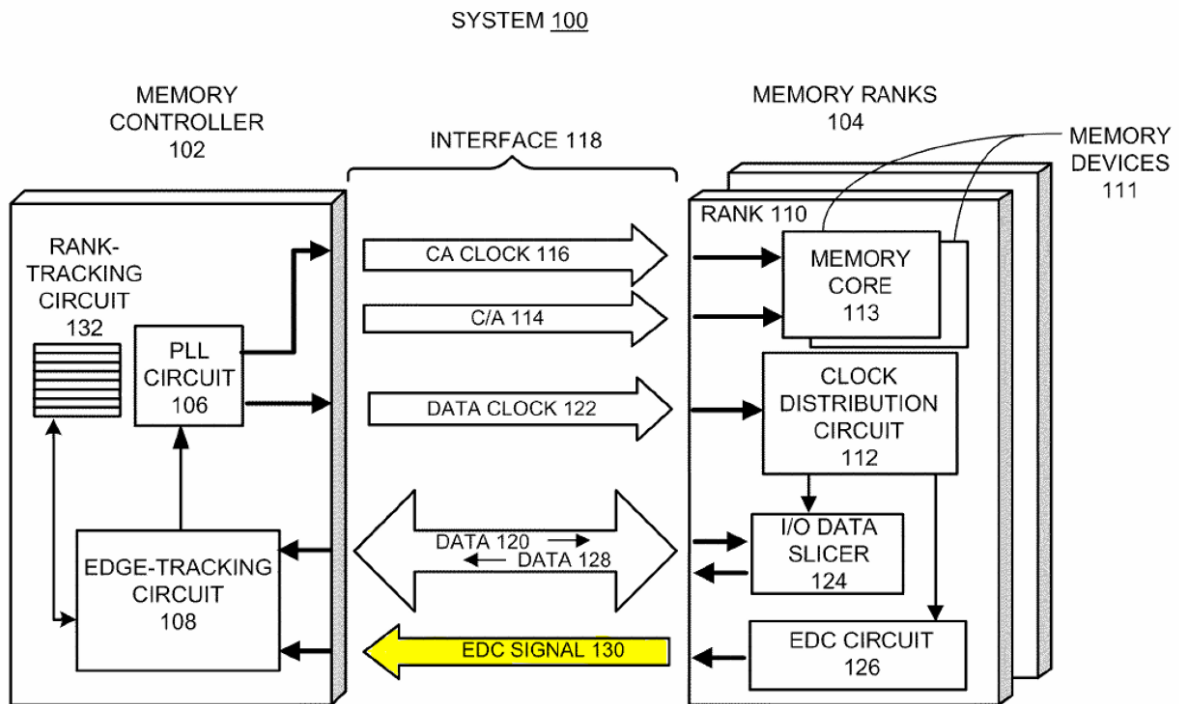


FIG. 1A

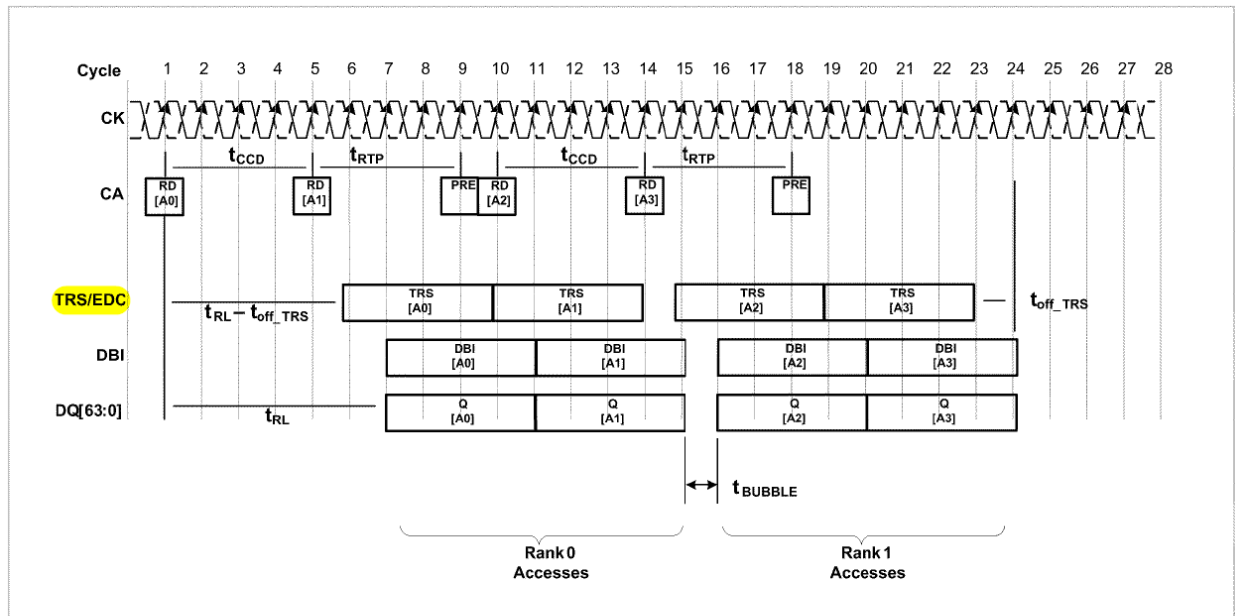


FIG. 4B

x) **[1.o] control die and second unidirectional interconnects**

Grounds 3-4 teach “wherein the control die is configured to drive signals [e.g., “Data Clock 122” below] to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects [e.g., Shaeffer’s “interface 118” for “Data Clock 122” as implemented in Keeth’s die interconnects] and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects” for the reasons explained for [1.m] (pp.70-72). EX1048, Fig.1A (below, “memory controller 102” driving “Data Clock 122” via “interface 118” to “memory devices 111,” without receiving back any signal via the same interconnects).

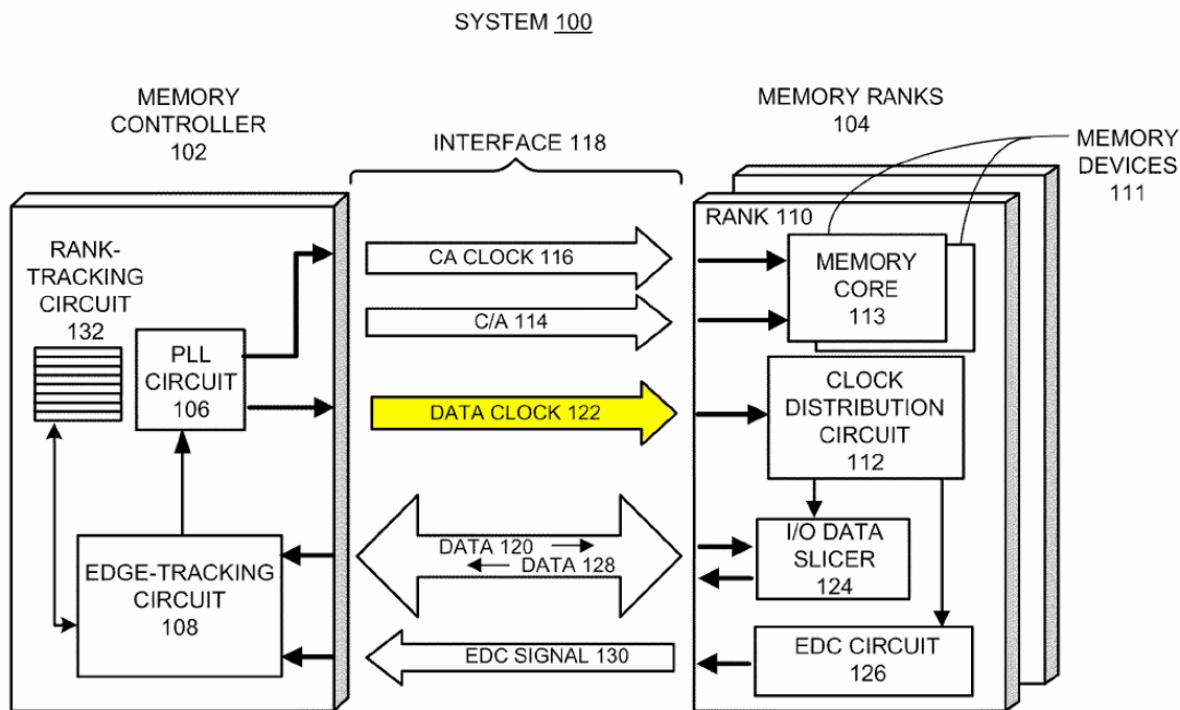


FIG. 1A

y) **[1.p.1] First signals**

Grounds 3-4 teach “*wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation [e.g., TRS/EDC Signal 130 below] from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects [Shaeffer’s “interface 118” for TRS/EDC Signal 130 as implemented in Keeth’s die interconnects].*” EX1048, Fig.1A (below).

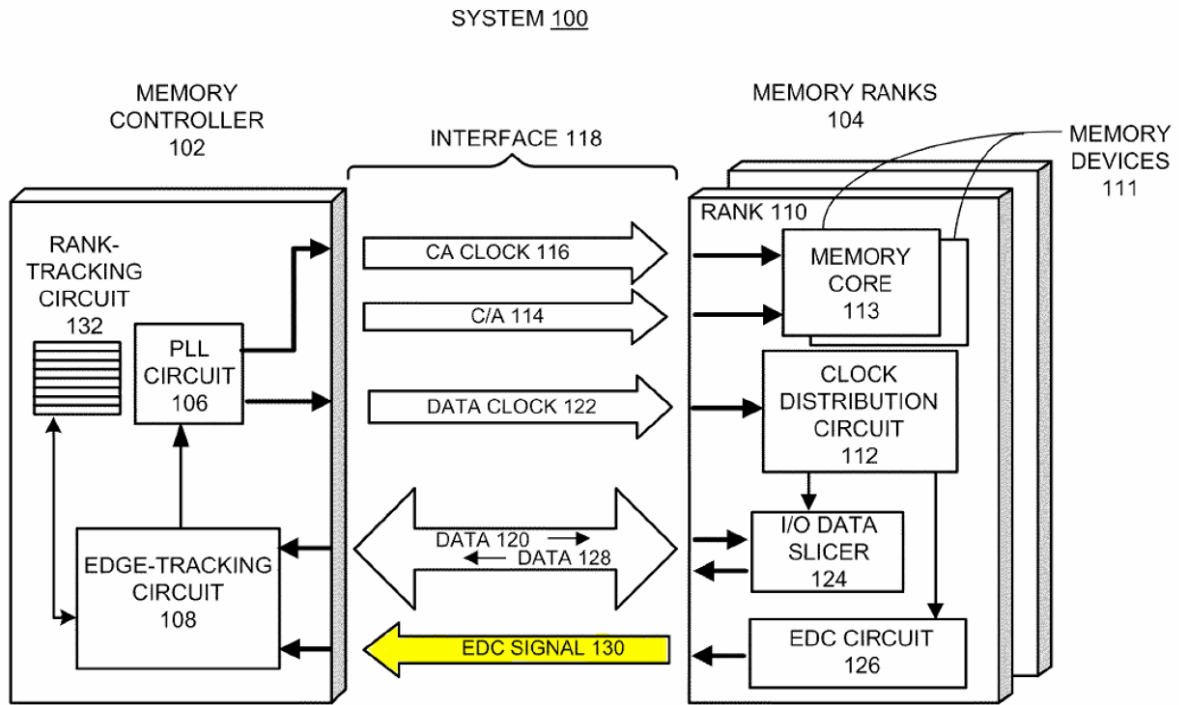


FIG. 1A

For the reasons discussed above for [1.l] and [1.n] (pp.67-70, 72-74), Grounds 3-4 disclose “the control die [] configured to...receive first signals...from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects.” Also, TRS/EDC Signal (i.e., “first signals”) is “associated with the memory read operation” and received “in response to the first set of C/A signals [for read operation per [1.c.2] (pp.37-38)].” EX1048, Fig.4B (below, TRS [A0]/[A1] received from memory devices in Rank 0 in response to read operation, RD [A0]/[A1]), 9:61-10:2 (“[A] TRS signal is output by the memory device, prior to a corresponding first bit of [read] data.”), Fig.3 (below, EDC similar to TRS), 5:14-16 (“EDC signal 208 associated with data burst 206”).

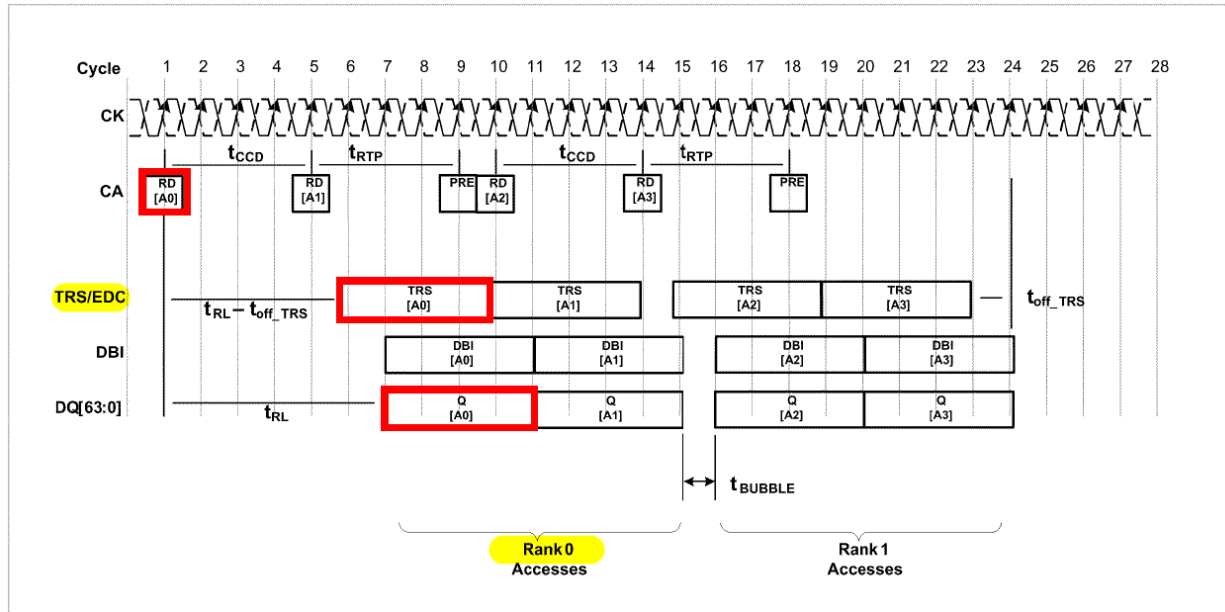


FIG. 4B

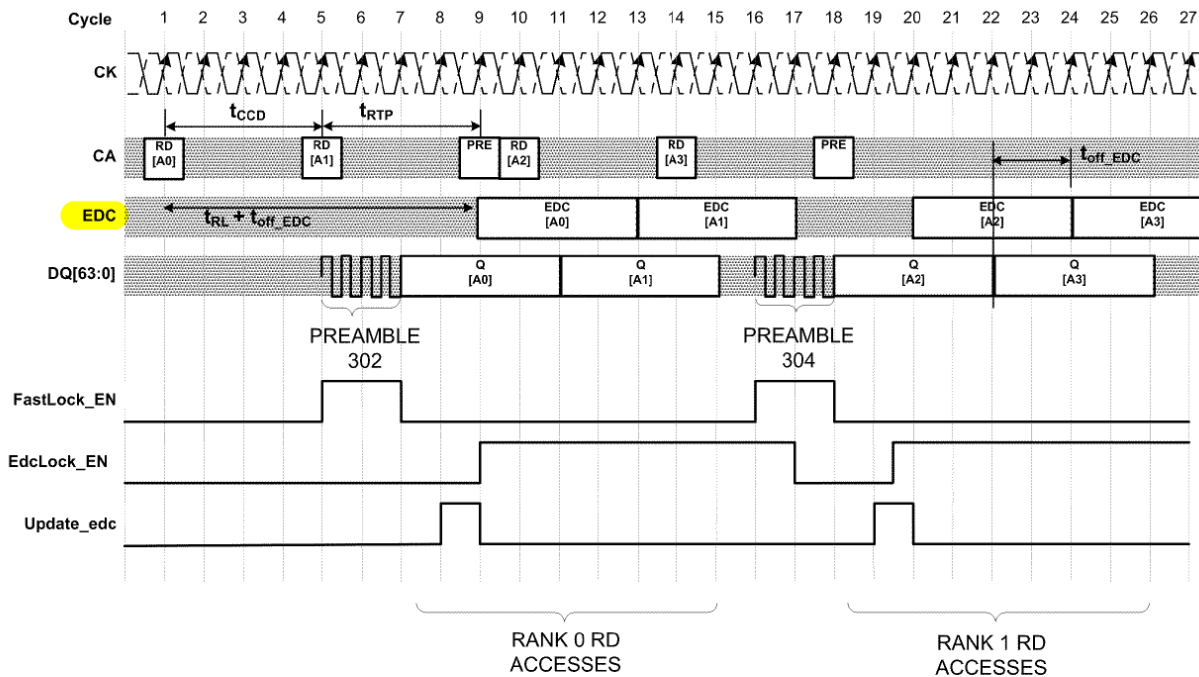


FIG. 3

z) **[1.p.2] Second signals**

Grounds 3-4 teach “in response to the second set of C/A signals, drive second signals associated with the memory write operation [e.g., “Data Clock 122” below used as a write strobe signal] to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects [e.g., Shaeffer’s “interface 118” for “Data Clock 122” as implemented in Keeth’s die interconnects].” EX1048, Fig.1A (below).

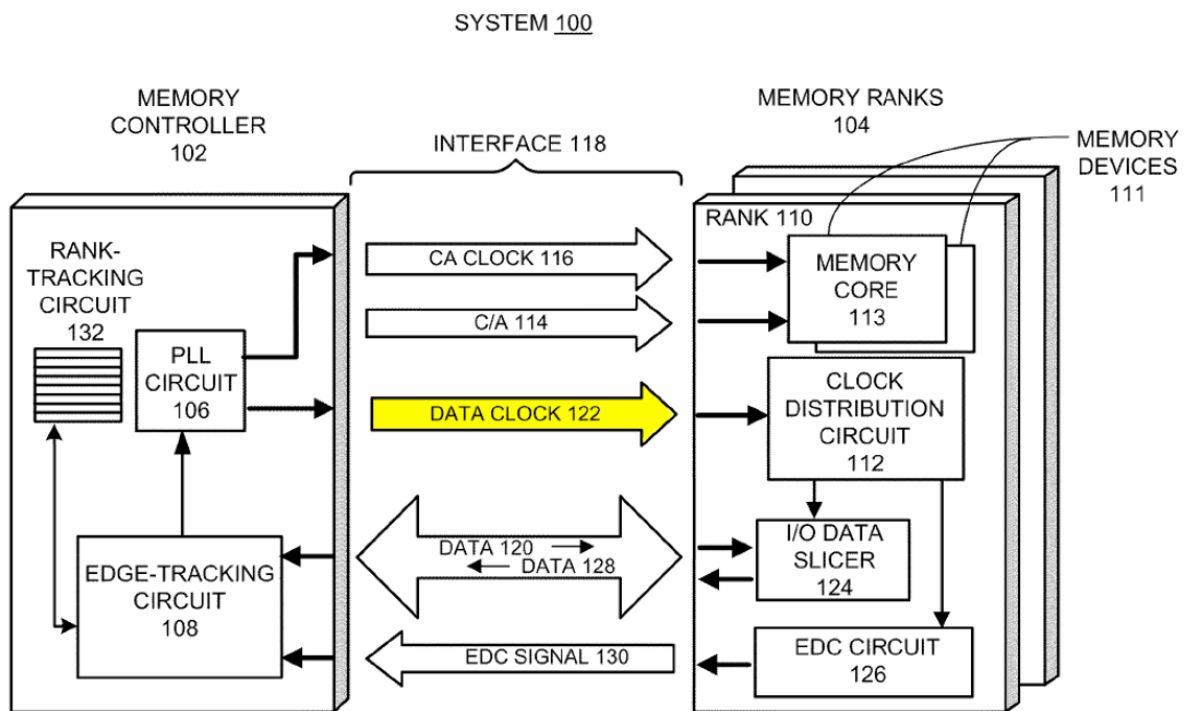


FIG. 1A

For the reasons discussed above for [1.m] and [1.o] (pp.70-72, 74-75), Grounds 3-4 disclose “the control die [] configured to...drive second signals...to one or more DRAM dies of the stacked DRAM dies via the second unidirectional

interconnects.” Also, Data Clock 122 used as a write strobe signal (i.e., “*second signals*”) is “*associated with the memory write operation*” to indicate to the memory device when to “sample [write] data,” EX1048, 9:1-10, and thus are driven “*in response to the second set of C/A signals* [for write operation per [1.c.2] (pp.37-38)].” EX1048, 3:35-38 (write data “directly clocked by” Data Clock); EX1003, ¶257.

5. Claim 2

Grounds 3-4 teach “[t]he DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.” Keeth discloses four dies in a stack as an example and explains that “[v]arious other configurations may include...[a] greater number of dice in the stack,” which a POSITA would understand includes “*at least 8 stacked DRAM dies.*” EX1047, 10:59-65. Having 8 or 16 DRAM dies in a stack was also expressly taught by Riho2 and well-known. EX1018, Fig.7B (below, a stack with 8 or 16 dies), ¶¶[0094]-[0095] (“eight chip dies” and “16 chip dies”); *see also* EX1045, 24:20-23 (“the stack” including “8 or more DRAM circuits”).

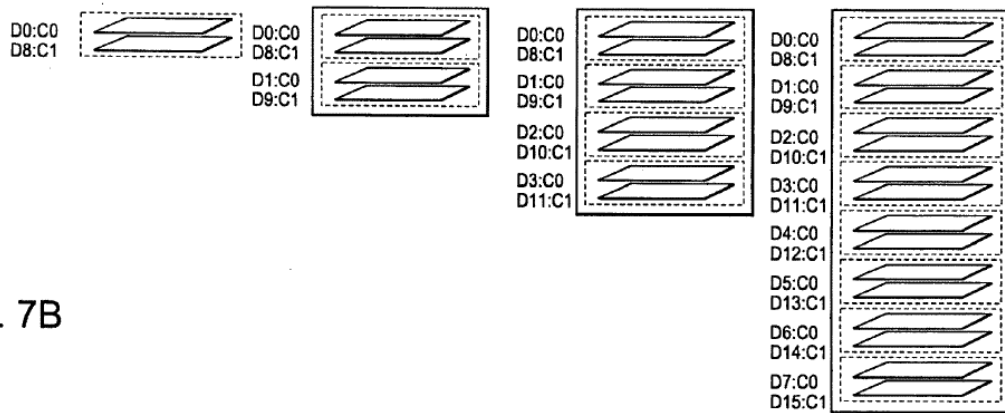


FIG. 7B

6. Claim 3

Grounds 3-4 teach “[t]he DRAM package of claim 2, wherein the stacked DRAM dies include 16 stacked DRAM dies” for the reasons discussed above for Claim 2 (pp.79-80). See also EX1045, 24:35-37 (“16 DRAM circuits”).

7. Claim 4

a) [4.a] First/second driver

Grounds 3-4 teach “[t]he DRAM package of claim 1, wherein: the first conduit includes a first driver [e.g., to drive data to odd dies] configured to have a first driver size [e.g., optimized for the load leading to the odd dies] and the second conduit includes a second driver [e.g., to drive data to even dies] configured to have a second driver size [e.g., optimized for the load leading to the even dies].”

As discussed above for [1.e.2], [1.e.4] and [1.j] (pp.49-51, 52, 62-64), Grounds 3-4 disclose the “first” and “second conduit” in a “vault control circuit 212” to transmit data to Keeth’s different dies (e.g., odd and even dies). EX1047, Fig.2 (below).

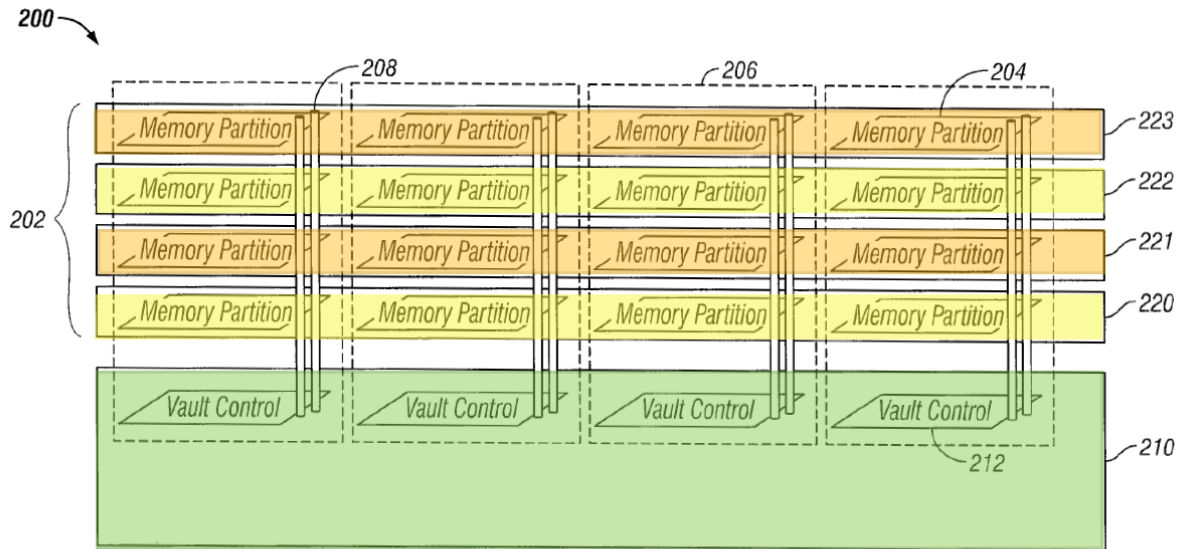
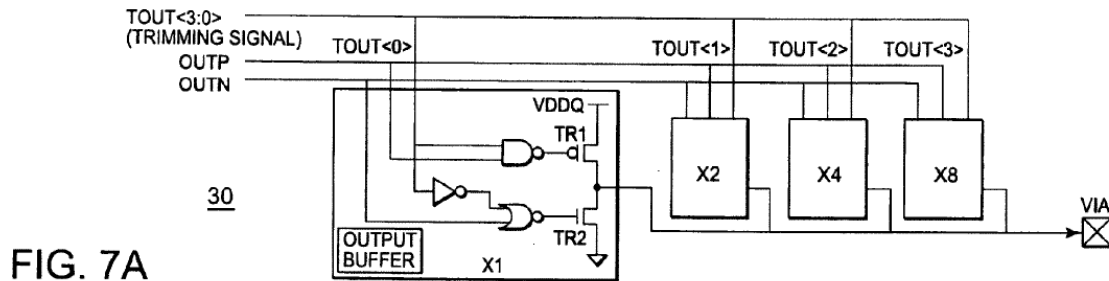


FIG. 2

Keeth also discloses “[b]y interleaving the connections, a vault control circuit may concurrently...access and send data to...multiple partitions.” *Id.*, 4:4-16, 6:9-19 (“concurrently driv[ing] data to partitions”). Thus, the “conduits” include respective “*first*” and “*second*” “*driver[s]*” because different dies store different data, and separate drivers are needed to drive the data “concurrently.” EX1003, ¶¶261-263. The “*first*” and “*second*” “*driver[s]*” also “*have a first driver size*” and “*a second driver size,*” respectively, which Riho2 teaches optimizing according to the respective load (caused by capacitance and resistance). EX1018, Fig.7A (below), ¶[0097] (“optimizing the output drive capacity of output buffers [X1-X4 in Fig. 7A]” considering “parasitic capacitance and...resistance” and “[e]ach of the output buffers” having “mutually different sizes”); *supra* pp.24-28,

49-51; EX1030, 135-36 (“[b]uffers...with different amounts of *drive capability*, depending on the sizes of the transistors”); EX1003, ¶264.



b) **[4.b] Different driver size**

Grounds 3-4 teach “the second driver size is different from the first driver size [e.g., to optimize the driver size considering different loads].” Keeth discloses the conductive paths driven by the “first” and “second” “driver[s]” may have different loads, depending on whether the conductive paths “entirely pass through or partially pass through the dice stack.” EX1047, 4:39-41; EX1003, ¶¶268-270. Thus, a POSITA would understand that “the second driver size is different from the first driver size” to optimize the drivers’ drivability, size, and power consumption, considering the different loads. EX1030, 135-36 (“different amounts of *drive capability*” depending “the sizes of the transistors”); EX1017, 1:22-28 (with “shorter runs” (i.e., less load), low drivability is desired to reduce “power consumption”); EX1072, 64-67; EX1003, ¶¶268-271. Similarly, Riho2 teaches driver size optimization to account for “a change in the time constant caused by parasitic capacitance and resistance.” EX1018, ¶[0097]; EX1003, ¶272. A

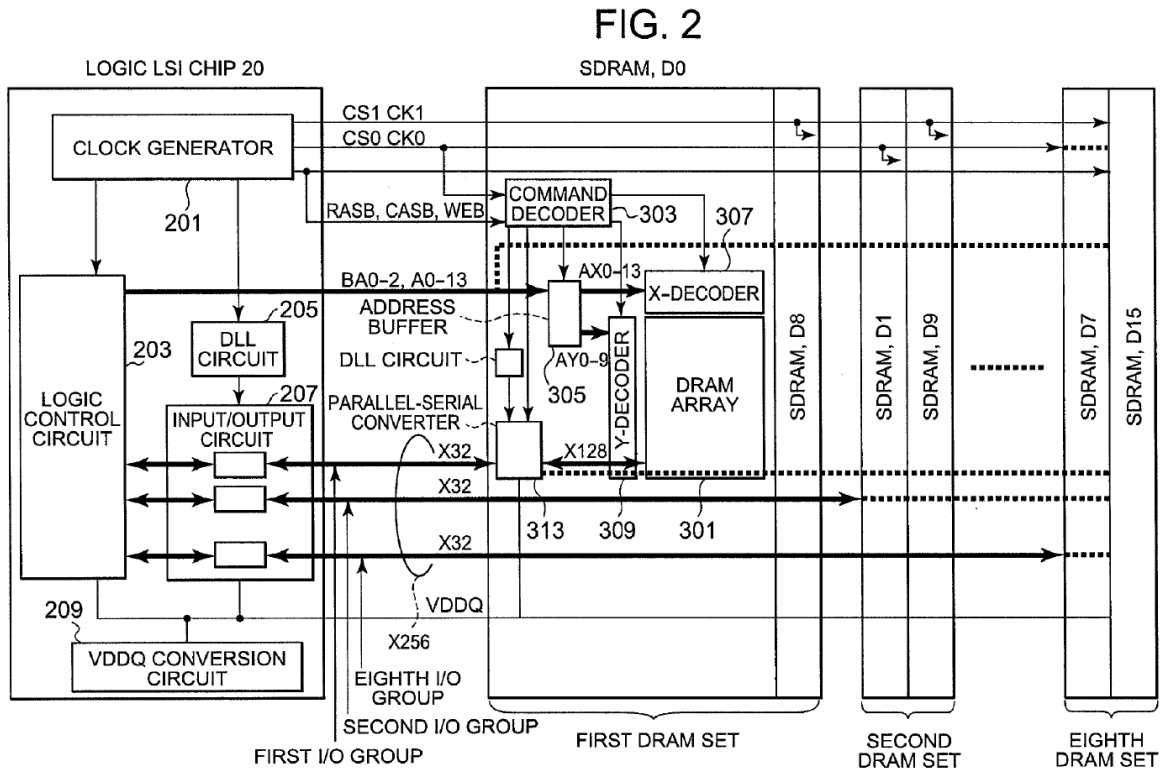
POSITA would have implemented Riho2's optimization technique in the Keeth and Shaeffer combination to avoid timing variations caused by, for example, the different lengths (and thus different parasitic capacitance/resistance) of Keeth's conductive paths, especially when the DRAM dies operate at a high frequency, EX1018, ¶¶[0010]-[0011], and also to save power, EX1017, 1:22-28. *Supra* pp.24-28; EX1003, ¶272. Such implementation would have resulted in the “*first*” and “*second*” “*driver[s]*” having “mutually different sizes.” EX1018, ¶[0097]; EX1003, ¶273.

8. Claim 5

Grounds 3-4 teach “[*t*]he DRAM package of claim 1, wherein the first data signals [for read operation per [1.c.2] (pp.37-38)] include 32 or 64 signals conducted via the first data interconnects in parallel [e.g., for speed and simplicity] and subsequently output by the DRAM package in parallel [e.g., to comply with standards], and wherein the second data signals [for write operation per [1.c.2] (pp.37-38)] include 32 or 64 signals received by the DRAM package in parallel [e.g., as was standard] and subsequently conducted via the first data interconnects in parallel [e.g., for speed and simplicity].” DRAM packages with 32 pins were common and standardized at the time. *See, e.g.*, EX1022, 348 (“x32 parts”); EX1081, 1 (“x32 configuration”), EX1040, 5 (“x32”); EX1035, 2 (standardized “x32 GDDR4”); EX1003, ¶278. Thus, for compatibility, a POSITA

would have been motivated for the Keeth-Shaeffer DRAM package to have 32 data terminals, so that “*the [first/second] data signals includ[ing] 32 or 64 signals*” are “[*output/received*] by the DRAM package in parallel.” *Id.*

Further, Keeth discloses that the “number of conductive paths [i.e., “[*first/second*] data interconnects”]...may vary.” EX1047, 3:18-20, 10:59-65 (“a fewer or greater number of interleaving conductive paths...to permit concurrent communication with dice in the stack.”). Matching the number (e.g., 32) of the “*data interconnects*” to that of data terminals of the package simplifies the interface circuitry, enabling 32 data signals to be communicated in parallel between the interface die and DRAM dies without regrouping, thus maintaining high speed. EX1003, ¶¶279-280. Also, it was well-known that stacked DRAM dies communicate data signals with 32 interconnects. *See, e.g.*, EX1016, Fig.2 (below, “x32” data interconnects between Logic LSI Chip 20 and stacked SDRAMs D0-D15), ¶[0033] (“Each SDRAM...outputs a 32-bit data signal in parallel.”); EX1003, ¶279.



Further, Riho2 in Ground 4 teaches 32-bit wide parallel data paths. EX1018, [0045]-[0047] (“32-bit”), Fig.1 (below, x32 interconnects (TSVs) for communicating data with memory dies 210-217); EX1003, ¶281.

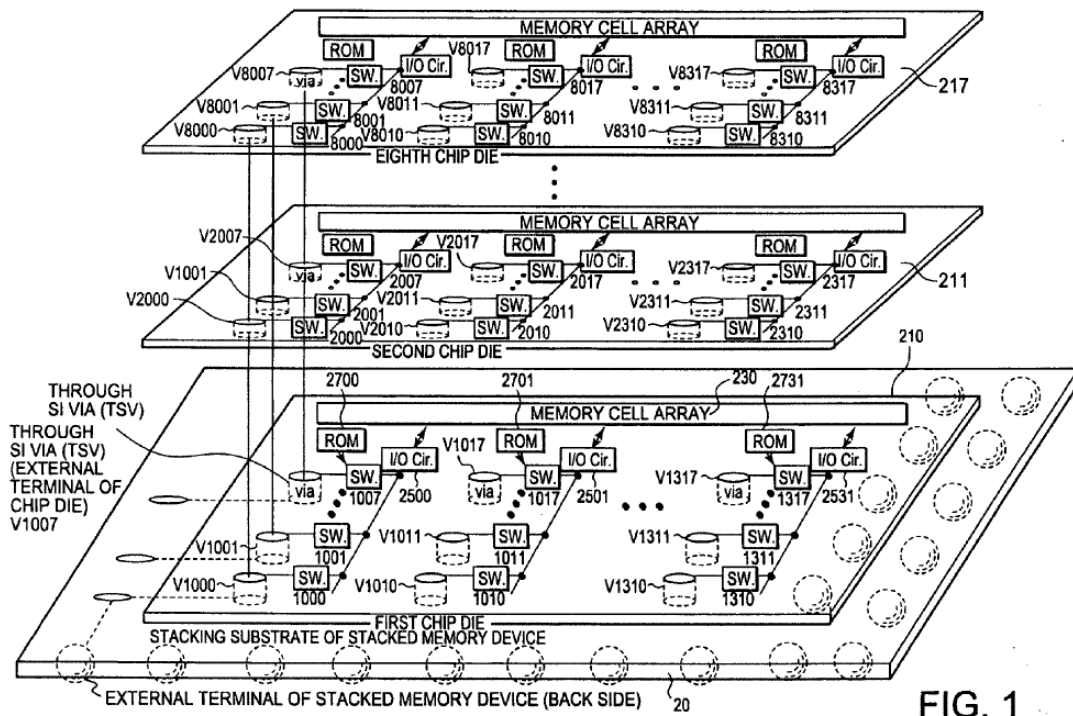


FIG. 1

Accordingly, a POSITA would have been motivated for each of “first” and “second” “data interconnects” to have 32 interconnects, allowing “the [first/second] data signals includ[ing] 32 or 64 signals” to be “conducted via the [first/second] data interconnects in parallel” with speed and simplicity. EX1003, ¶¶279-281.

9. Claim 6

- a) **[6.a] First set of C/A signals including a chip select signal**

Grounds 3-4 teach “[t]he DRAM package of claim 1, wherein: the first set of C/A signals [for read operation per [1.c.2] (pp.37-38)] include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first

data signals [e.g., Keeth's "ID information" or "chip select" signals]." Keeth discloses "ID information" selects a DRAM die to which read/write operation is directed. EX1047, 3:5-8, 3:21-38 ("referenc[ing] each die 120 through 123 by the ID information"). Keeth also teaches a "chip select" signal to select a DRAM die and to "prevent data contention," EX1047, 2:6-10, which was well known, EX1019, 13 ("Chip Select: All commands are masked when CS# is...HIGH"), 33-34 & n.1, 36 ("DESELECT...CS# HIGH"); EX1023, 2-3 ("chip-select"); EX1022, 413 Fig.10.5; EX1003, ¶285. Keeth further discloses that the stacked dies "may be communicatively coupled with external devices, e.g., processors and memory controllers, through the interface die." EX1047, 3:9-20. Thus, Keeth's "ID information" or "chip select" signals would be received as part of "*C/A signals*" for read/write from the external controller, as usual at the time. EX1019, 12 (Figs.1-3); EX1003, ¶286. Such direct control from a memory controller to select a DRAM die removes the need to generate a chip select signal within the package, resulting in faster operations. EX1082, 3, 4 (Figs.1-3, CS0#-CS3#, CID signals directly from a processor to select a target rank, which may include "a single die"); EX1003, ¶286.

b) ***[6.b] Second set of C/A signals including a chip select signal***

Grounds 3-4 teach "*the second set of C/A signals* [for write operation per [1.c.2] (pp.37-38)] *include one or more signals to select one DRAM die among the*

first plurality of DRAM dies to receive the second data signals [e.g., Keeth’s “ID information” or “chip select” signals]” for the same reasons above for [6.a] (pp.86-87).

c) ***[6.c] No emulation logic***

Grounds 3-4 teach “*wherein the control die [from [1.e.1] (pp.47-48)] does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies [e.g., for speed and simplicity]*” for the reasons discussed above for [6.a] (pp.86-87). As explained, it would have been obvious for an external controller to directly select a DRAM die using “ID information” or “chip select” signals, thereby obviating the need for any emulation logic (which creates chip select signals) from the interface die, thus simplifying the circuitry and maintaining high speed. *See generally* EX1047, EX1048 (no emulation logic used); EX1003, ¶290.

10. Claim 7

Grounds 3-4 teach “[t]he DRAM package of claim 1, wherein the control die [e.g., Shaeffer’s “[local] memory controller 510” from [1.e.1] (pp.47-48)] is further configured to control timing of command/address signals driven to the stacked DRAM dies [e.g., using t_{CCD} to control timing between RD [A0]/[A2] and RD [A1]/[A3], and using t_{RTP} to control timing between RD [A1]/[A3] and PRE

below in Fig.4B] *and/or timing of data signals communicated between the stacked DRAM dies and the data terminals* [e.g., using t_{RL} and t_{off_TRS} to control data signals on DQ[63:0] below in Fig.4B] *to prevent signal collisions.*” EX1048, Figs.3-4B (below); EX1047, 2:6-10 (“prevent[ing] data contention”); EX1038, 89-90 (“bus conflict”); EX1003, ¶¶295-296.

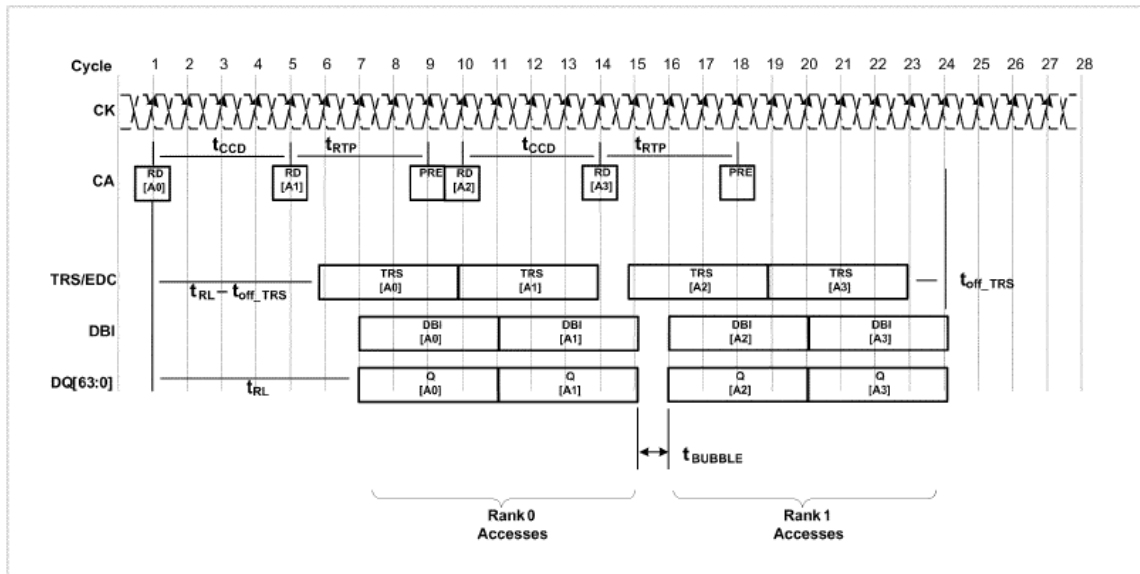


FIG. 4B

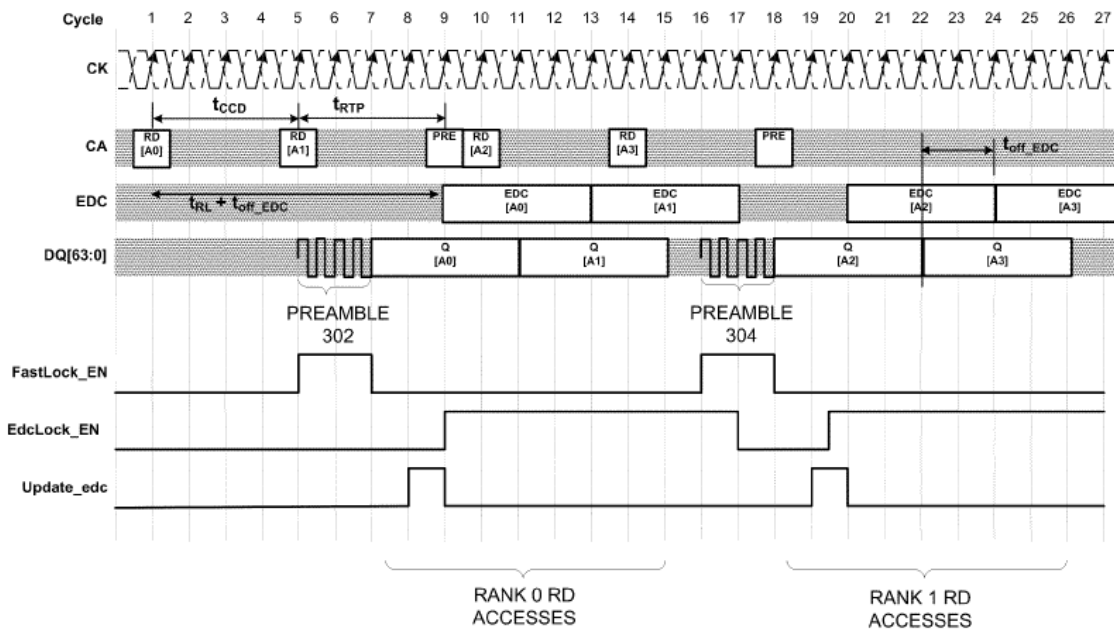


FIG. 3

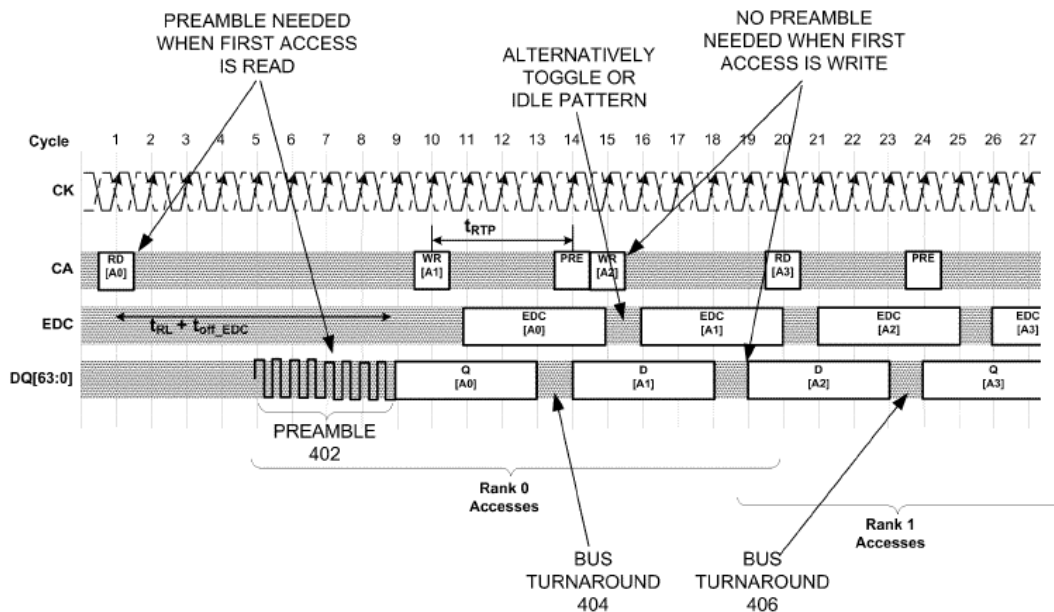


FIG. 4A

Shaeffer's control of the timing of signals by its "*control die*" was well-known and standardized. See, e.g., EX1019, 165 (" t_{CCD} "), 62 (t_{CCD} between Read

Commands), 165 (“ t_{RTP} ”), 67 (t_{RTP} between Read and Precharge Commands), 24 (“Read Latency (RL)”), 56 (RL delay between Read Command and the corresponding data); EX1003, ¶297. Also, applying these timing parameters to control signals is important to “*prevent signal collisions*,” which have “disastrous” effects, EX1038, 89-90, and thus were commonly used in stacked memory devices, *see, e.g.*, EX1015, Figs.9-15, 8:59-12:13; EX1045, Figs.9-15, 10:14-13:35; EX1072, 34-38 (“[POSITAs] knew how to deal with collisions”); EX1003, ¶297.

11. Claim 8

Grounds 3-4 teach “[*t*]he DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies [e.g., at least one even die of 522/520 (yellow) below, from [1.h.2] (pp.57-59)] *has at least one electrical connection leading from the at least one TSV* [e.g., connectors (purple) making an electrical connection from at least one TSV (dashed red) from [1.h.2] (pp.57-59) to “joints 509,” EX1047, 5:34-36], *the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die* [e.g., the connectors in purple are not electrically coupled to any data port included in I/O Circuits 532/530 (blue) on at least one even die of 522/520 (yellow) from [1.h.1] (pp.55-57)].” EX1047, Figs.5 (below), 7, 7:7-20.

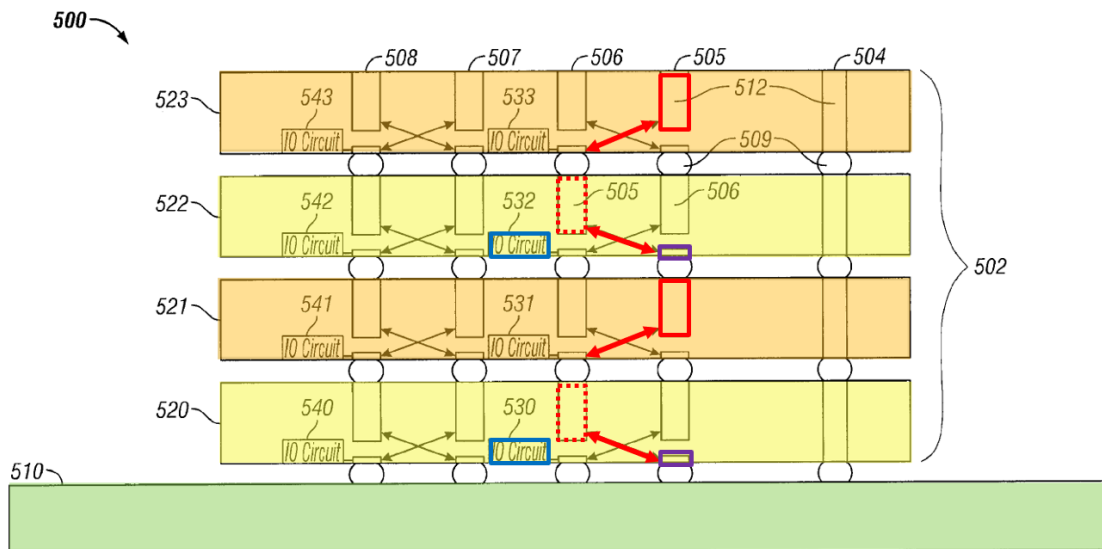


FIG. 5

12. Claims 9-11

The limitations of claims 9-11 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Grounds 3-4 for at least the same reasons discussed above.

This limitation in claims 9-11...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[9.a]-[9.b.1]	[1.a]-[1.b.2] ⁵

⁵ Transferring data “in response to C/A signals received at the C/A ports” was a standardized operation at the time, EX1019, 33, 56, 68-69, as disclosed by Shaeffer, EX1048, Figs. 3-4B, and explained for [1.c.1] (pp.34-37) (“to receive or output data signals...in response to the (C/A) signals”).

This limitation in claims 9-11...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[9.b.2]	[1.c.1], [1.e.1] ⁶
[9.b.3]	[1.d.1], [1.d.3]
[9.b.4]	[1.d.1]-[1.d.2], [1.l]-[1.m]
[9.c]	[1.c.1]-[1.c.2], [6.a]-[6.b]
[9.d.1]	[1.c.2], [1.d.1]-[1.d.2], [1.e.2], [1.f], [1.j]
[9.d.2]	[1.p.1]
[9.e.1] ⁷	[1.c.2], [1.d.1]-[1.d.2], [1.f], [1.h.1], [1.j] ⁸

⁶ Keeth’s “*control die*” ([1.e.1], pp.47-48) includes an “*interface*” ([9.b.2]/[13.c]/[24.c]) with “*terminals*” ([1.c.1], pp.34-37). See EX1047, Abstract (“*interface*”); EX1003, ¶¶300-301.

⁷ The “*second data signals*” have no antecedent basis. It appears “*second signals*” should have been “*second data signals*.” EX1003, ¶303.

⁸ Because Grounds 3-4 teach “*the first data interconnects...[are] not in electrical communication with any data port on any of the second plurality of DRAM dies*” in [1.h.1], it would have been obvious not to drive any data signals that are conducted via “*the first data interconnects*” “*to any of the second plurality of DRAM dies via any of the data interconnects*.” EX1003, ¶305.

This limitation in claims 9-11...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[9.e.2]	[1.p.2] ⁹
[9.f.1]	[1.h.1]
[9.f.2]	[1.h.2]
[9.f.3]	[1.h.3]
[9.g]	[1.i]
[9.h]	[1.f]
[9.i]	[1.g]
[9.j.1]	[1.l]
[9.j.2]	[1.m]
[9.k]	[5]
[9.l]	[5]
[10]	[2]
[11]	[5]

⁹ To the extent that “*one or more signals*” in [9.e.2] refers to a different signal than “*one or more signals*” in [9.d.2], [9.e.2] is substantially similar to [1.p.2] and obvious for the same reasons above.

13. Claim 12

a) *[12.a] Consecutive C/A signals*

Grounds 3-4 teach “[t]he method of claim 9, wherein the first set of C/A signals [e.g., RD[A0] below in Fig.4A for read] and the second set of C/A signals [e.g., WR[A1] in Fig.4A for write] are consecutive sets of C/A signals, the method further comprising,” EX1048, Fig.4A (below, RD[A0] and WR[A1] are consecutive commands), as it was the well-known, standardized operation, see, e.g., EX1019, 63 (Fig.36 below, consecutive read (at T0) and write (at T4) commands).

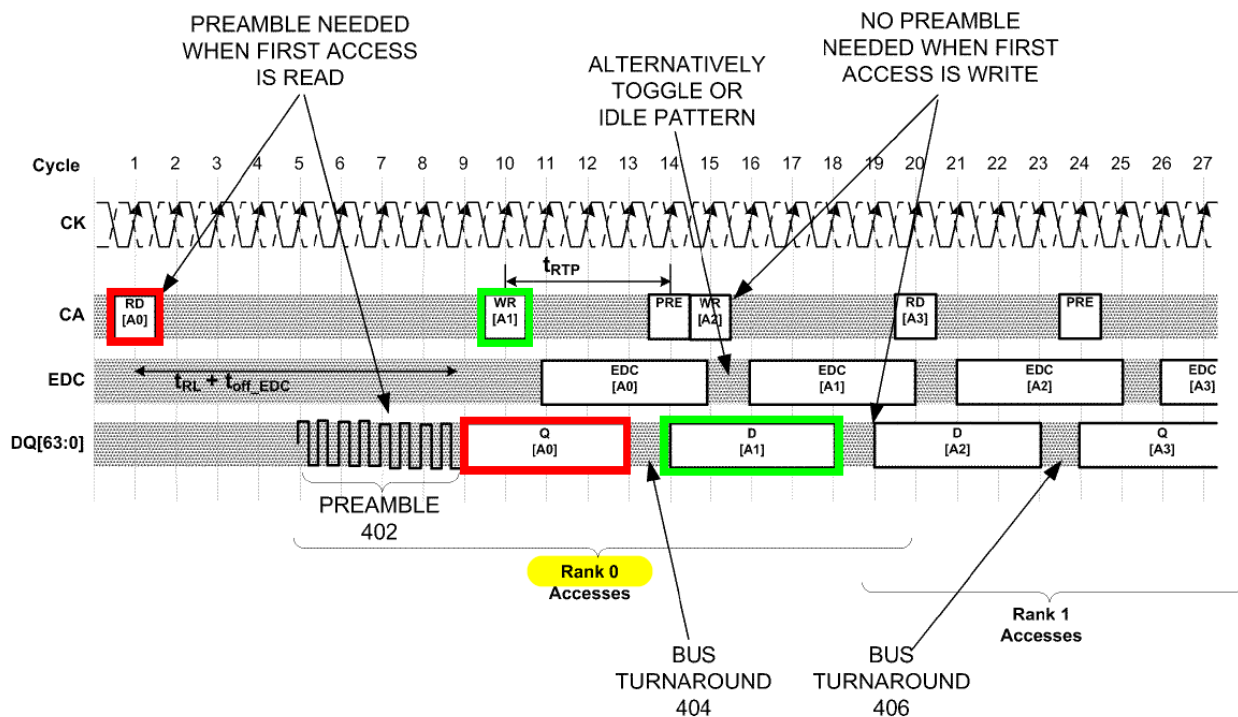


FIG. 4A

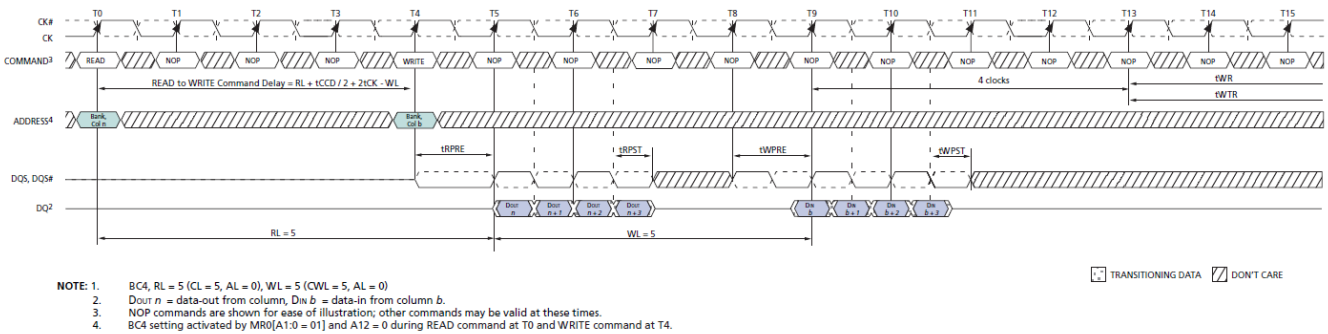


Figure 36 — READ (BC4) to WRITE (BC4) OTF

b) [12.b]-[12.c] First/second drivers

Grounds 3-4 teach “enabling first drivers [e.g., read drivers in Keeth’s “vault control circuit”] to receive and drive the first data signals in response to the first set of C/A signals [for read operation per [9.c]]” and “enabling second drivers [e.g., write drivers in Keeth’s “vault control circuit”] to receive and drive the second data signals in response to the second set of C/A signals [for write operation per [9.c]]” for the reasons discussed above for [1.c.1] (pp.34-37), [1.e.2] (pp.49-51), [1.j] (pp.62-64), and [4.a] (pp.80-81).

Keeth’s “vault control circuit” is used to “access [from] and send data to” the memory dies, EX1047, 4:13-16, 6:16-19, and includes read/write drivers (i.e., “first[/second] drivers”) “enabl[ed]...to receive and drive” respective read/write data signals between the memory dies and the data terminals on the interface die. See also EX1047, 3:62-67 (“Interface die 210 may include...buffers, and I/O drivers.”); EX1048, Fig.5, 11:25-26 (“I/O interface”), 12:4-7 (data signals

“communicated on one or more of the links 514” coupled to I/O interface), 8:52-54 (“chip-to-chip interfaces”); EX1003, ¶¶311-312.

c) **[12.d] Non-driving state**

Grounds 3-4 teach “*maintaining each of the first drivers and the second drivers in a non-driving state* [e.g., a “high-impedance mode” of a tri-state buffer during Shaeffer’s bus turnaround 404] *after driving of the first data signals by the first drivers* [for read operation per [12.b]] *and before receiving of the second data signals by the second drivers* [for write operation per [12.c]]” for the reasons discussed above for [1.d.2] (pp.42-45) and claim 7 (pp.88-91) and the following: Claim 12 depends from claim 9, which, like [1.d.2] (pp.42-45), requires using the same “*first data interconnects*” for conducting both the “*first*” and “*second data signals*.” See [9.d.1], [9.e.1]. When conducting two different data signals on the same data interconnects, a POSITA would understand to use “tri-state” drivers “*to prevent signal collisions*,” as taught in the art. See, e.g., *supra* pp.9-10; EX1038, 212-215; EX1003, ¶¶58-59, 316. Such “tri-state drivers [] have a low, high, and off (or high-impedance) mode of operation.” EX1038, 68. A POSITA would understand that the “high-impedance” (off) mode is a “*non-driving state*,” where the driver’s output is “free to float up or down.” *Id.*; EX1003, ¶316. Also, when no data is driven, for example, between read and write operations, tri-state drivers are “place[d]...in high-impedance mode,” EX1038, 151, which not only avoids

“disastrous” data conflicts, but also saves power, *id.*, 89-90; EX1003, ¶317.

Accordingly, “*maintaining each of the...drivers in a non-driving state*” between data transfers was the standard way of operation for DDR memory taught by Keeth (discussed above, pp.34-37), see EX1019, 63 (Fig.36 below, DQ lines being held the middle (threshold) level between read and write data transactions, indicating drivers are turned off and in “*a non-driving state*”), and as taught by Shaeffer, EX1048, 8:60-64, Fig.4A (bus turnaround 404, below, after read (red) and before write (green) on bi-directional DQ[63:0] data lines); EX1003, ¶317.

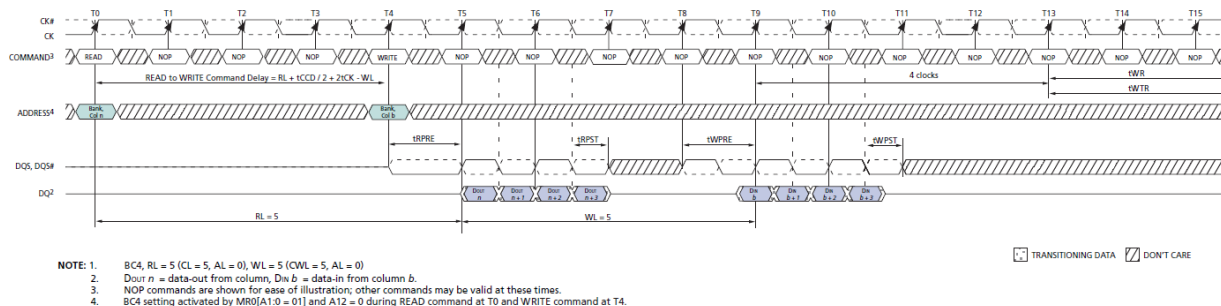


Figure 36 — READ (BC4) to WRITE (BC4) OTF

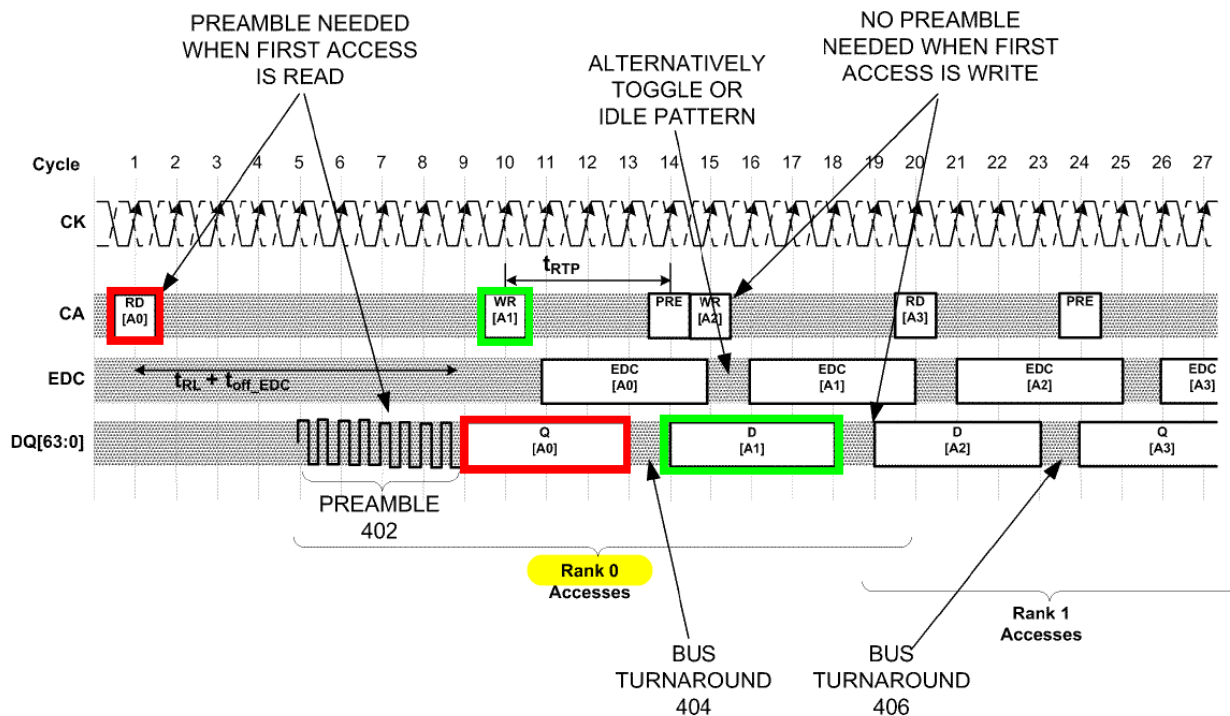


FIG. 4A

d) [12.e] Not to receive or drive any signal

Grounds 3-4 teach “wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal [e.g., a tri-state buffer in a “high-impedance” mode with its output “free to float up or down,” EX1038, 68]” for the reasons discussed above for [12.d] (pp.97-99).

14. Claims 13-22

The limitations of claims 13-22 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Grounds 3-4 for at least the same reasons discussed above:

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[13.a]	[1.a]
[13.b]	[1.b.1]-[1.b.2], [1.d.2] ¹⁰
[13.c]	[1.c.1], [1.e.1] ¹¹
[13.d]	[1.d.3]
[13.e]	[1.e.1]-[1.e.4]
[13.f]	[1.d.1]-[1.d.2], [1.l]-[1.m]
[13.g]	[1.d.2], [1.h.1] ¹²
[13.h.1]	[1.i] ¹³
[13.h.2]	[1.b.1]

¹⁰ [1.d.2] requires the same “*first data interconnects*” to conduct both read data (“*first data signals*”) and write data (“*second data signals*”), thus these die interconnects and the corresponding “*data ports*” are “*bi-directional*,” as with Grounds 3-4. EX1048, Figs.1A, 4A (bi-directional data interface 120/128 and DQ[63:0]); EX1019, 3, 13 (bi-directional DQ pins); EX1003, ¶321.

¹¹ See p.93 n.6.

¹² See p.100 n.10.

¹³ See p.100 n.12.

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[13.i]	[1.c.1], [1.d.1] ¹⁴
[13.j]	[1.f]
[13.k]	[1.g]
[13.l]	[6.a]-[6.b] ¹⁵
[13.m]	[1.d.2], [1.j] ¹⁶

¹⁴ Shaeffer also teaches two sets of C/A signals for different ranks, thereby conducted via different C/A interconnects (e.g., a “*first*” (e.g., read to rank0) and “*second set of C/A signals*” (e.g., consecutive write to rank 1) “*via the first*” (red) and “*second C/A interconnects*” (blue), respectively, shown above for [1.d.1] (pp.38-42)). EX1048, 5:50-67, 7:11-8:39, 8:60-64, 12:49-57, Figs.3, 4A, 5; EX1003, ¶324; *id.* ¶¶295-297.

¹⁵ As discussed above (p.101, n.14), Shaeffer teaches two sets of C/A signals for different ranks, in which case the “*first*” and “*second set of C/A signals*” include respective “*signals to select*” a DRAM die in the respective “*subset of the plurality of stacked DRAM dies* [e.g., in the respective rank].” EX1003, ¶327.

¹⁶ See p.101 n.14. When Shaeffer’s two sets of C/A signals are directed to different ranks, the corresponding “*first*” and “*second data signals*” are conducted by the “*first*” and “*second data interconnects*,” respectively. EX1003, ¶330.

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[13.n]	[1.p.1]-[1.p.2]
[13.o]	[1.l]
[13.p]	[1.m]
[13.q]	[1.n]
[13.r] ¹⁷	[1.o]
[13.s]	[1.h.2]
[13.t]	[1.h.3]
[13.u]	[1.h.3] ¹⁸
[14]	[2]

¹⁷ The phrase “*ene or more DRAM dies of the plurality of stacked DRAM dies-*” in [13.r] was not part of the claim language allowed during prosecution. EX1002, 841 (bottom). This phrase is an obvious typographical error, introduced during the printing of the patent, which should be deleted to correct the error. EX1003, ¶¶331-338; *Beable Educ., Inc. v. Achieve3000, Inc.*, IPR2021-01169, Paper 34, 11 (PTAB Jan. 3, 2023), *aff’d*, No. 23-1605 (Fed. Cir. July 10, 2024).

¹⁸ Keeth discloses a TSV “*not connected to,*” and thus “*not in electrical communication with*” a data port. EX1047, Figs.5, 7, 7:11-13 (TSVs “pass[ing] through...dice”), 5:39-62 (“without connecting to any circuitry”); EX1003, ¶341.

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[15]	[3]
[16]	[8] ¹⁹
[17.a.1]	[1.j]
[17.a.2]	[1.k.1], [12.a] ²⁰
[17.b]	[4.a], [12.b]
[17.c]	[4.a], [12.c] ²¹
[17.d]	[12.d]
[17.e]	[12.d] ²²
[17.f]	[12.e]
[18.a.1]	[1.j]
[18.a.2]	[1.k.1]-[1.k.2]

¹⁹ See p.103 n.18. Keeth discloses TSVs “without connecting to any circuitry” [including “*memory cells*”] on alternating dies. EX1047, 5:39-62.

²⁰ See p.101 n.14.

²¹ See p.102 n.16.

²² As explained above for [12.d] (pp.97-99), the drivers are turned off (i.e., in “*a non-driving state*”) when no data are driven, including “*after driving the second data signals.*”

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[19]	[5] ²³
[20.a]	[1.a]
[20.b]	[1.b.2]
[20.c.1]	[1.c.1]
[20.c.2]	[1.c.2], [5]
[20.d.1]	[1.d.1]
[20.d.2]	[1.d.2]
[20.d.3]	[1.d.3]
[20.e.1]	[1.e.1]
[20.e.2]	[1.e.2]-[1.e.4]
[20.f.1]	[1.d.2], [1.h.1]
[20.f.2]	[1.i]
[20.g]	[1.j]
[20.h.1]	[1.k.1]
[20.h.2]	[1.k.2]
[20.i]	[1.l]-[1.m]
[20.j]	[1.n]-[1.o]
[20.k]	[1.n]-[1.o]
[20.l.1]	[1.p.1]

²³ See p.102 n.16.

This limitation in claims 13-22...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[20.l.2]	[1.p.2]
[20.m]	[6.c]
[21]	[2]
[22.a]	[5], [6.a]
[22.b]	[5], [6.b]

15. **Claim 23**

Claim 23 adds new limitations [23.c.1] (“*power supply terminals*”) and [23.m.1]-[23.m.2], which are disclosed by Grounds 3-4, as explained further below. The other limitations of claim 23 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Grounds 3-4 for at least the same reasons discussed above:

This limitation in claims 23...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[23.a]	[1.a]
[23.b]	[1.b.2]
[23.c.1]	See below
[23.c.2]	[1.c.2], [5]
[23.d.1]	[1.d.1]
[23.d.2]	[1.d.2]

This limitation in claims 23...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[23.d.3]	[1.d.3]
[23.e.1]	[1.e.1]
[23.e.2]	[1.e.2]-[1.e.4]
[23.f.1]	[1.d.2], [1.h.1]
[23.f.2]	[1.i]
[23.g]	[1.j]
[23.h.1]	[1.k.1]
[23.h.2]	[1.k.2]
[23.i]	[1.l]-[1.m]
[23.j]	[1.n]-[1.o]
[23.k]	[1.n]-[1.o]
[23.l.1]	[1.p.1]
[23.l.2]	[1.p.2]
[23.m.1]	See below
[23.m.2]	See below
[23.n]	[6.c]

a) ***[23.c.1] Power supply terminals***

Grounds 3-4 teach [23.c.1] because [23.c.1] is substantially similar to [1.c.1] (pp.34-37), except [23.c.1] also requires “*power supply terminals*,” which is also taught by Grounds 3-4. As discussed above for [1.a] (pp.28-30), Keeth and

Shaeffer disclose a DRAM package, e.g., for DDR3 DRAMs, which include “*power supply terminals*” to provide power supply for the memory operation, as was standardized at the time. See EX1048, 1:58-61 (“memory....consuming...power”), 8:60-64; EX1018, ¶[0102], Fig.8 (VDDQ); EX1019, 3-11 (DDR3 SDRAM Package Pinout including “*power supply terminals*,” such as for VDD, VDDQ), 14 (describing VDD and VDDQ as “Power Supply”); EX1003, ¶344.

b) ***[23.m.1] first supply voltage interconnect***

Grounds 3-4 teach “*wherein the power supply interconnects*”²⁴ [to provide supply voltages, e.g., VDDQ, to the DRAM dies] *include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies* [e.g., implementing Keeth’s interleaving conductive paths to reduce power noise].” The “*power supply interconnects*” are needed to provide supply voltages to the stacked DRAM dies. See EX1048, 2:16-8 (“supply voltage”); EX1018, Fig.8 (below), ¶[0102] (providing “supply voltages

²⁴ “*the power supply interconnects*” lack antecedent basis because this term first appears in this limitation.

VDDQ0” via “TSV” to the “stacked memory devices”); EX1016, Fig.2 (below), ¶[0036] (“VDDQ...to the SDRAMs”), ¶[0030] (“power supply penetrating...TSVs”), EX1043, Fig. 4 (below, TSVs for VDD); EX1003, ¶¶348-349.

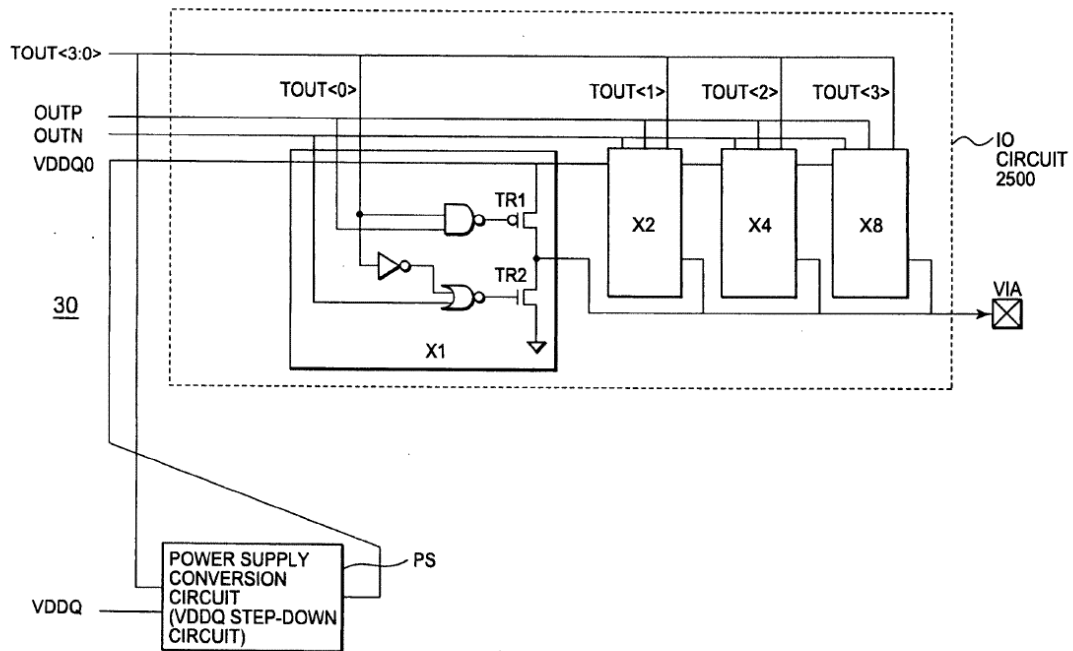


FIG. 8

FIG. 2

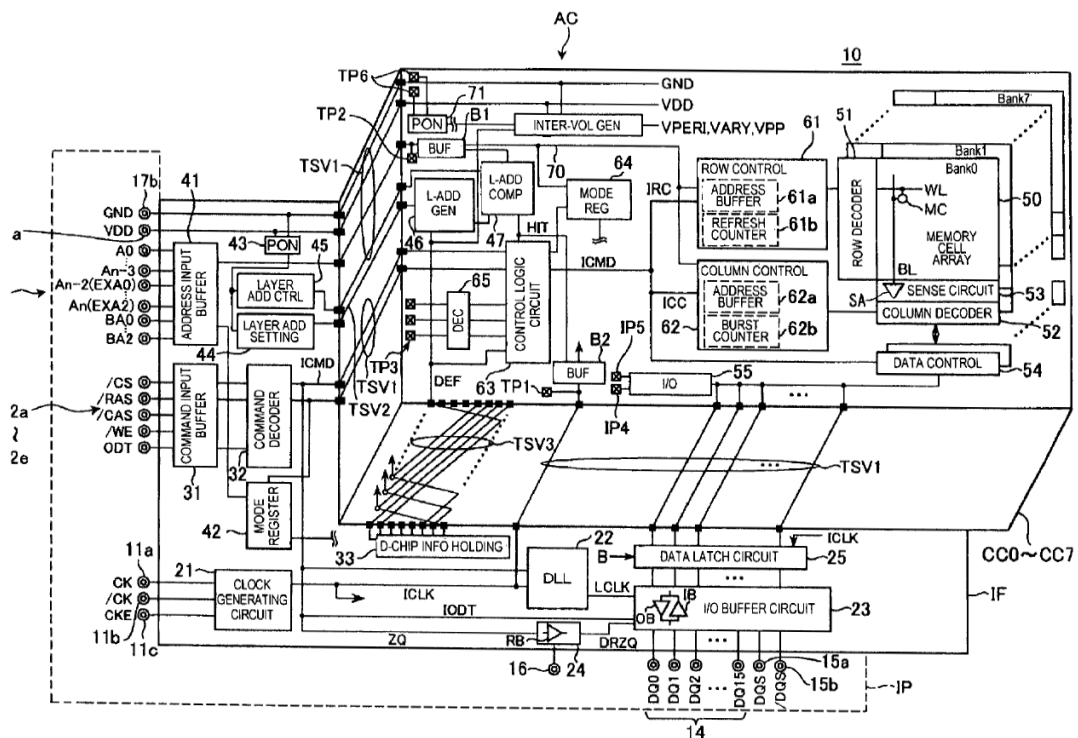
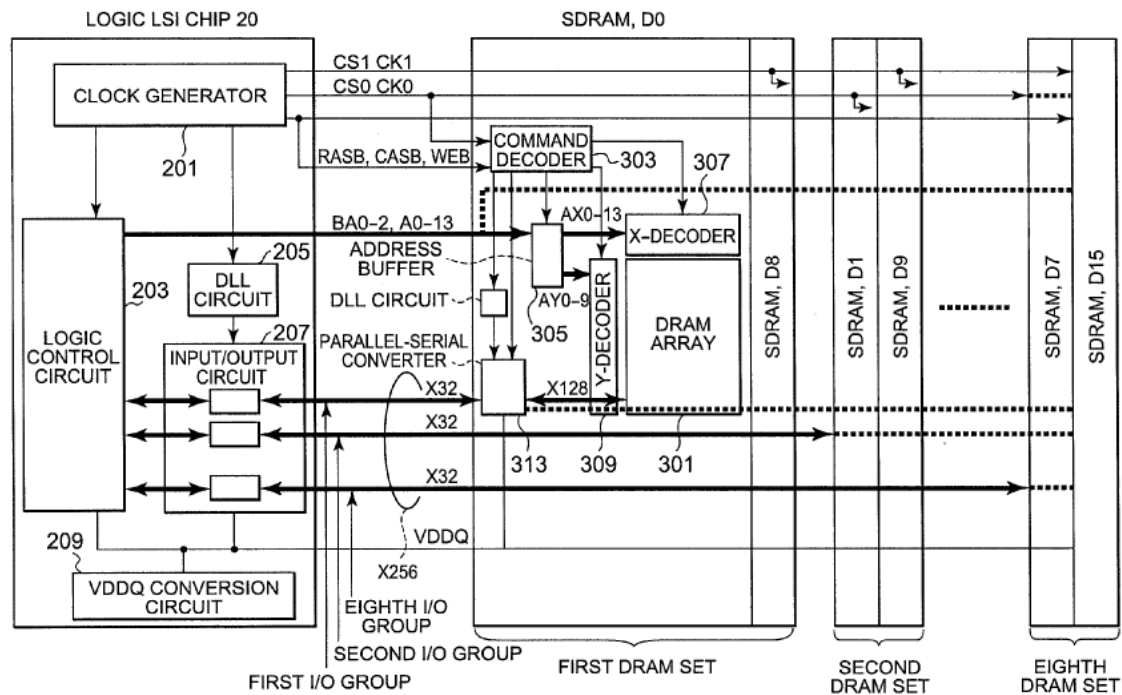


FIG.4

Keeth's teaching of interleaving conductive paths, thus allowing dies to operate independently, as discussed above (e.g., pp.38-45), would have motivated a POSITA to interleave the "*power supply interconnects*" as well to permit independent operation and to enhance stability and minimize power cross-noise, which is "a bigger concern in the 3D-DRAM." EX1059, 4-5; EX1048, 4:11-14 ("power supply induced jitter"), 2:18-19 ("high-frequency power supply noise"); EX1003, ¶¶350-351. Like the other interleaving conductive paths discussed above (e.g., pp.38-45), "*the power supply interconnects*" include a "*first*" and "*second supply voltage interconnect*," where the "*first*" conducts "*a supply voltage received at a power supply terminal*" only to "*each of the first plurality of DRAM dies*" as claimed. See EX1047, 4:4-16; EX1003, ¶¶350-351.

c) ***[23.m.2] second supply voltage interconnect***

Grounds 3-4 also teach "*wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies* [e.g., implementing Keeth's interleaving conductive paths to reduce power noise]" for the reasons explained directly above for [23.m.1] (pp.107-110).

16. Claims 24-28

Under Netlist's interpretation in district court, see EX1089, 144-63, the limitations of claims 24-28 are substantially identical to earlier limitations, as

shown in the following table, and thus obvious in light of Grounds 3-4 for at least the same reasons discussed above:

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.a]		[1.a]
[24.b]	<i>“stacked DRAM dies”</i>	[1.b.1] <i>“stacked DRAM dies”</i>
	<i>“first portion of the signal ports” “to receive C/A signals”</i>	[1.b.2] <i>“C/A ports”</i>
	<i>“second portion of the signal ports” “to transfer data”</i>	[1.b.2] <i>“data ports”</i>
[24.c]		[1.c.1] ²⁵
[24.d.1]		[1.e.1]
[24.d.2]		[1.e.2], [1.k.1]
[24.e]		[1.e.2]-[1.e.4], [1.d.3]

²⁵ See p.93 n.6.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.f]	<i>“first conduits”</i>	[1.e.2] <i>“C/A conduits”</i>
	<i>“second conduits”</i>	[1.e.2] <i>“data conduits”</i>
	<i>“third conduits”</i>	[1.e.2] <i>“conduits”</i> that conduct signals from [1.l] <i>“first unidirectional interconnects”</i>
	<i>“fourth conduits”</i>	[1.e.2] <i>“conduits”</i> that conduct signals to [1.m] <i>“second unidirectional interconnects”</i>
[24.g]	<i>“first die interconnects [conduits]”</i>	[1.d.1] <i>“C/A interconnects”</i> [1.e.3] <i>“C/A conduits”</i>
	<i>“second die interconnects [conduits]”</i>	[1.d.1] <i>“data interconnects”</i> [1.e.4] <i>“data conduits”</i>
	<i>“third die interconnects [conduits]”</i>	[1.l] <i>“first unidirectional interconnects”</i> [1.e.2] <i>“conduits”</i>
	<i>“fourth die interconnects [conduits]”</i>	[1.m] <i>“second unidirectional interconnects”</i> [1.e.2] <i>“conduits”</i>
[24.h]		[1.d.1], [1.e.3] ²⁶

²⁶ Shaeffer discloses C/A signals unidirectional to DRAM dies. EX1048, Fig.1A, 3:25-28 (C/A 114). Thus, *“first conduits,”* which correspond to *“C/A conduits”* and drive C/A signals to DRAM dies, are also *“unidirectional”* in that direction. See EX1019, 13 (“Input” only C/A pins).

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.i]	<i>“to drive a signal [write data] to...or to receive a signal [read data] from the [same] corresponding second die interconnect”</i>	[1.d.2] <i>“the first data interconnects configured to conduct the first [read] data signals and the second [write] data signals”</i>
	<i>“second conduits”</i>	[1.e.4] <i>“data conduits”</i> ²⁷
[24.j]		[1.l], [1.p.1] ²⁸
[24.k]		[1.m], [1.p.2] ²⁹

²⁷ Given *“data interconnects”* are bi-directional, see p.100 n.10, *“data conduits”* coupled to the *“data interconnects”* are also bi-directional.

²⁸ The *“signal received from a corresponding third die interconnect [e.g., Shaeffer’s TRS/EDC]”* is driven to the *“interface”* by *“third conduits”* that are *“unidirectional”* because signals like TRS/EDC—unidirectional to the control die as explained for [1.l] (pp.67-70)—are not transferred back to the stacked DRAM dies. See EX1047, 3:44-51; EX1003, ¶355.

²⁹ The *“fourth conduits”* are *“unidirectional”* and *“drive a signal [such as Shaeffer’s Data Clock 122 for write strobe] received from the interface to a corresponding fourth die interconnect,”* but not in reverse, because Shaeffer’s write strobe signals are unidirectional to the stacked DRAM dies, as explained for

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.l]		[1.c.1]-[1.c.2] ³⁰
[24.m.1]	<i>“a first subset of the first conduits”</i>	[1.e.3] <i>“first C/A conduits”</i>
	<i>“a first subset of the first die interconnects”</i>	[1.d.1] <i>“first C/A interconnects”</i>
	<i>“a first subset of the second conduits”</i>	[1.e.4] <i>“first data conduits”</i>
	<i>“a first subset of the second die interconnects”</i>	[1.d.2] <i>“first data interconnects”</i>
	<i>“first signals associated with the first set of C/A signals [for a memory read operation]”</i>	[1.d.2] <i>“first [read] data signals”</i>

[1.m] (pp.70-72), and a unidirectional conduit has sufficient capability to drive signals to interconnects, and Shaeffer does not teach conducting any signal in the opposite direction on line 122. EX1003, ¶358.

³⁰ DRAM devices are accessed repeatedly during normal operation for read and write operations (i.e., *“to receive...a first[/second/third/fourth] set of C/A signals for a memory read[/write] operation”*). EX1003, ¶¶324, 361.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.m.2]	<i>“a first subset of the third conduits”</i>	[1.e.2] <i>“conduits”</i> coupled to [1.l] <i>“first unidirectional interconnects”</i> of the [1.b.1] <i>“first plurality of DRAM dies”</i>
	<i>“a first subset of the third die interconnect”</i> ³¹	[1.l] <i>“first unidirectional interconnects”</i> of the [1.b.1] <i>“first plurality of DRAM dies”</i>
	<i>“one or more second signals associated with the first set of C/A signals [for a memory read operation]”</i>	[1.p.1] <i>“first signals associated with the memory read operation”</i>
[24.n.1]	<i>“third signals associated with the second set of C/A signals [for a memory write operation]”</i>	[1.d.2] <i>“second [write] data signals”</i>
	<i>“the first subset of the first [/second] conduits [/die interconnects]”</i>	[1.d.1], [1.d.2], [1.e.3], [1.e.4], see [24.m.1] above

³¹ Because an interconnect (singular) cannot have a subset, this claim is indefinite. EX1003, ¶363. However, under Netlist’s interpretation in district court, EX1089, 149, this limitation is substantially similar to the limitations to the right. EX1003, ¶¶363-364.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.n.2]	<i>“a first subset of the fourth conduits”</i>	[1.e.2] <i>“conduits”</i> coupled to [1.m] <i>“second unidirectional interconnects”</i> of the [1.b.1] <i>“first plurality of DRAM dies”</i>
	<i>“a first subset of the fourth die interconnect”</i> ³²	[1.m] <i>“second unidirectional interconnects”</i> of the [1.b.1] <i>“first plurality of DRAM dies”</i>
	<i>“fourth signals associated with the second set of C/A signals [for a memory write operation]”</i>	[1.p.2] <i>“second signals associated with the memory write operation”</i>

³² See p.115 n.31; EX1003, ¶¶366-367; EX1089, 150.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.o.1]	<i>“a second subset of the first conduits”</i>	[1.e.3] <i>“second C/A conduits”</i>
	<i>“a second subset of the first die interconnects”</i>	[1.d.1] <i>“second C/A interconnects”</i>
	<i>“a second subset of the second conduits”</i>	[1.e.4] <i>“second data conduits”</i>
	<i>“a second subset of the second die interconnects”</i>	[1.d.2] <i>“second data interconnects”</i>
	<i>“fifth signals associated with the second [or maybe third?] set of C/A signals”³³</i>	[1.c.1] <i>“[read] data signals”</i> from one of the [1.b.1] <i>“second plurality of DRAM dies.”</i>

³³ The claim language is indefinite as written. However, under Netlist’s interpretation in district court, EX1089, 151, this limitation is substantially similar to the limitations to the right. EX1003, ¶¶369-371.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.o.2]	<i>“a second subset of the third conduits”</i>	[1.e.2] <i>“conduits”</i> coupled to [1.l] <i>“first unidirectional interconnects”</i> of the [1.b.1] <i>“second plurality of DRAM dies”</i>
	<i>“a second subset of the third die interconnect”</i> ³⁴	[1.l] <i>“first unidirectional interconnects”</i> of the [1.b.1] <i>“second plurality of DRAM dies”</i>
	<i>“one or more sixth signals associated with the second [or maybe third?] set of C/A signals”</i> ³⁵	<i>“signals”</i> analogous to [1.p.1] <i>“first signals associated with the memory read operation”</i> but from one of the [1.b.1] <i>“second plurality of DRAM dies”</i>
[24.p.1]	<i>“seventh signals associated with the fourth set of C/A signals [for a memory write operation]”</i>	[1.c.1] <i>“[write] data signals”</i> from one of the [1.b.1] <i>“second plurality of DRAM dies.”</i>
	<i>“the second subset of the first [/second] conduits [/die interconnects]”</i>	[1.d.1], [1.d.2], [1.e.3], [1.e.4], see [24.o.1] above

³⁴ See p.115 n.31; EX1003, ¶373.

³⁵ See p.117 n.33; EX1003, ¶¶374-376; see also EX1089, 151.

This limitation in claims 24-28...		...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.p.2]	<i>“a second subset of the fourth conduits”</i>	[1.e.2] <i>“conduits”</i> coupled to [1.m] <i>“second unidirectional interconnects”</i> of the [1.b.1] <i>“second plurality of DRAM dies”</i>
	<i>“a second subset of the fourth die interconnect”</i> ³⁶	[1.m] <i>“second unidirectional interconnects”</i> of the [1.b.1] <i>“second plurality of DRAM dies”</i>
	<i>“one or more eighth signals associated with the second [or maybe fourth?] set of C/A signals”</i> ³⁷	<i>“signals”</i> analogous to [1.p.2] <i>“second signals associated with the memory write operation”</i> but from one of the [1.b.1] <i>“second plurality of DRAM dies”</i>
[24.q]		[1.e.3], [1.j], [1.l]-[1.m] ³⁸
[24.r]		[1.d.1], [1.j], [1.l]-[1.m] ³⁹
[24.s.1]		[5]
[24.s.2]		[5]

³⁶ See p.115 n.31; EX1003, ¶378.

³⁷ See p.117 n.33; EX1003, ¶¶379-381; *see also* EX1089, 152.

³⁸ Keeth’s independent operation of even/odd dies, EX1047, 5:63-6:10, requires distinct *“conduits”* for the corresponding signals. EX1003, ¶384.

³⁹ Similar to note 38 on p.119, Keeth’s independent operation of even/odd dies requires distinct *“die interconnects.”*

This limitation in claims 24-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[24.s.3]	[5] ⁴⁰
[24.s.4]	[5] ⁴¹
[25.a.1]	[1.b.1], [1.h.1]
[25.a.2]	[1.b.1], [1.i]
[25.b]	[6.a]
[25.c]	[6.b]
[25.d]	[6.a] ⁴²
[25.e]	[6.b] ⁴³
[25.f]	[1.j]
[25.g]	[1.k.1]-[1.k.2]
[26.a.1]	[12.a]
[26.a.2]	[1.k.1]

⁴⁰ See p.117 n.33; EX1003, ¶¶386-387.

⁴¹ See p.118 n.35; EX1003, ¶¶389-390.

⁴² See pp.117-118, nn.33, 35. Under Netlist’s interpretation, a selection signal like [6.a] is applied to the “*second plurality of DRAM dies.*”

⁴³ See p.119 n.37. Under Netlist’s interpretation, a selection signal like [6.b] is applied to the “*second plurality of DRAM dies.*”

This limitation in claims 24-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[26.b]	[12.b]
[26.c]	[12.c]
[26.d]	[12.d]
[26.e]	[12.e]
[27]	[2]
[28]	[3]

VII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-28 be canceled as unpatentable.

Dated: August 25, 2025

/Eliot D. Williams/

Eliot D. Williams

Reg. No. 50,822

BAKER BOTTS L.L.P.

700 K Street, N.W.

Washington, D.C. 20001

T: (202) 639-1334

F: (202) 639-1167

Theodore W. Chandler

Reg. No. 50,319

BAKER BOTTS L.L.P.

1801 Century Park East

Suite 2400

Los Angeles, CA 90067

T: (213) 202-5702

F: (213) 202-5732

Ferenc Pazmandi
Reg. No. 66,216
BAKER BOTTS L.L.P.
101 California Street
Suite 3200
San Francisco, CA 94111
T: (415) 291-6255
F: (415) 291-6355

Mark A. Speegle
Reg. No. 77,512
BAKER BOTTS L.L.P.
401 South First Street, Suite 1300
Austin, Texas 78704
T: (512) 322-2536
F: (512) 322-3636

Counsel for Petitioner
Samsung Electronics Co., Ltd.

CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24(a)(1)(i) (“14,000 words”) because it contains 13,833 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24(a)(1).

Dated: August 25, 2025

/Eliot D. Williams/

Eliot D. Williams

Reg. No. 50,822

BAKER BOTTS L.L.P.

700 K Street, N.W.

Washington, D.C. 20001

T: (202) 639-1334

F: (202) 639-1167

Counsel for Petitioner

Samsung Electronics Co., Ltd.

CERTIFICATE OF SERVICE

I hereby certify that on this 25th day of August, 2025, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

Jamie J. Zheng, Ph.D., Esq.
Netlist, Inc.
111 Academy Way, Suite 100
Irvine, CA 92617-3046
(650) 521-4828

Dated: August 25, 2025

/Eliot D. Williams/
Eliot D. Williams
Reg. No. 50,822
BAKER BOTTS L.L.P.
700 K Street, N.W.
Washington, D.C. 20001
T: (202) 639-1334
F: (202) 639-1167

Counsel for Petitioner
Samsung Electronics Co., Ltd.