

Claim 1 of U.S. Patent No. 8,787,060 vs. Claim 1 of U.S. Patent No. 12,308,087

1. A dynamic random access memory (DRAM) package, comprising:

a stacked DRAM dies including at least a first plurality of ~~input/output~~ DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals ~~via which the memory package communicates data and control~~/including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more ~~external devices~~through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

~~a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;~~

~~at least a first die~~ a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

~~wherein a first C/A interconnect and a second die interconnect, of the first die interconnect~~ C/A interconnects is in electrical communication with corresponding C/A ports on the first groupplurality of arrayDRAM dies and not in electrical communication with any C/A port on any of the second group of at least one array die, the plurality of DRAM dies;

~~wherein a second dieC/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second groupplurality of at least one array dieDRAM dies and not in electrical communication with any C/A port on any of the first groupplurality of arrayDRAM dies; and~~

~~a control die comprising at least a first data~~ wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV

in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first ~~die~~data interconnect and a first data terminal of the plurality of input/output data terminals, and ~~at least~~ a second ~~data~~ conduit of the second data conduits is coupled between the second ~~die~~data interconnect and the first data terminal, ~~the first terminal being a data terminal;~~

wherein the control die further ~~comprising a~~includes control ~~circuit~~logic configurable to control respective states of the first ~~data conduit~~ and the second data ~~conduit~~conduits in response to ~~control~~one or more C/A signals received via one or more ~~second terminals of the plurality of terminals of the~~ C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies

to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

Claim 1 of U.S. Patent No. 9,318,160 vs. Claim 1 of U.S. Patent No. 12,308,087

1. A dynamic random access memory (DRAM) package, comprising:

~~data terminals and control terminals;~~

stacked ~~array~~DRAM dies including at least a first ~~group~~plurality of ~~array~~DRAM dies and a second ~~group~~plurality of ~~at least one array~~DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

die interconnects ~~and second die~~including C/A interconnects, ~~the first and data~~ interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first group plurality of array DRAM dies and not in electrical communication with any C/A port on any of the second group of at least one array die, the plurality of DRAM dies;

wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second group plurality of at least one array die DRAM dies and not in electrical communication with any C/A port on any of the first group plurality of array DRAM dies; and

wherein a control die comprising first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on

the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

wherein a first conduit of the first data conduits is coupled between the first ~~die~~ interconnects and data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second ~~die~~ interconnects data interconnect and the first data terminal;

wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

wherein the die interconnects further include first ~~data conduit~~ including unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first drivers each having a first driver size and unidirectional interconnects and is not configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

wherein the control die is configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size; signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.