

U.S. Patent No. 12,308,087 – Claim 1 v. Claim 9

1.—9. A method, comprising: at a dynamic random access memory (DRAM) package;

comprising:

including stacked DRAM dies, the stacked DRAM dies including ~~at least~~ a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including ~~C/A~~command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

~~terminals including command and/or address (C/A) terminals and data terminals,~~
~~wherein in response to C/A signals received at the C/A ports,~~ the DRAM package ~~is~~
~~configured to receive C/A signals further including an interface, via the~~which the DRAM
package receives C/A ~~terminals and is further configured to receive or output data signals,~~
~~and via the data terminals in response to which the (C/A) signals, wherein the~~ DRAM
package ~~is configured to output first~~receives or outputs data signals in response to ~~a first set~~
~~of C/A signals associated with a memory read operation and to receive second data signals in~~
~~response to a second set of C/A signals associated with a memory write operation;~~

C/A signals received via the interface, the interface including terminals, the DRAM
package further including die interconnects~~including C/A interconnects and data~~
~~interconnects, the C/A interconnects including at least first C/A interconnects and second C/A~~
~~interconnects, the first C/A interconnects configured to conduct the first set of C/A signals~~
~~and the second set of C/A signals, the data interconnects including at least first data~~
~~interconnects and second data interconnects, the first data interconnects configured to~~
~~conduct the first data signals and the second data signals,~~ each of the die interconnects

including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies ~~and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;~~

~~a control, the die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits interconnects including C/A ~~conduits and data conduits~~interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A ~~conduits~~interconnects including at least first C/A ~~conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects~~, the data ~~conduits including at least first data conduits coupled to respective ones of the interconnects including first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~~~

~~wherein, receiving via the interface a first set of C/A interconnects signals for a memory read operation and a second set of C/A signals for a memory write operation, the first C/A interconnects is in electrical communication with corresponding set of C/A ports on signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies;~~

~~wherein a to respond to the second set of C/A signals; in response to the first set of C/A interconnect of the second signals, driving the first set of C/A interconnects is in electrical communication with corresponding signals to C/A ports ~~on~~ of the second first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM dies~~

~~and not in electrical communication with any C/A port on any die~~ first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects; in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies;

wherein a first data interconnect of the first ~~via the first C/A interconnects, receiving~~ second signals associated with the second set of C/A signals from the interface, driving the second data interconnects is in electrical communication with corresponding data ports on signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects; wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the ~~second plurality of stacked~~ DRAM dies, each of the first data interconnects including a first respective set of TSVs, the ~~first~~ respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die; wherein ~~a second data interconnect each~~ of the second data

interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies; wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies; wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies; wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies; wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.

~~wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;~~

~~wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;~~

~~wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;~~

~~wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;~~

~~wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;~~

~~wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and~~

~~wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.~~

U.S. Patent No. 12,308,087 – Claim 1 v. Claim 13

13. 1. A dynamic random access memory (DRAM) package, comprising:

a plurality of stacked DRAM dies ~~including at least a first plurality of DRAM dies and a second plurality of DRAM dies~~, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;

~~terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;~~

~~die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals~~ an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs

data signals, the interface including terminals, the terminals including C/A terminals and data terminals;

die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the ~~stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs~~plurality of stacked DRAM dies;

and a control die coupled between the ~~terminals~~interface and the plurality of stacked DRAM dies, the control die including ~~conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A~~signal conduits coupled, respectively, to ~~respective ones~~the die interconnects;

wherein:

the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;

each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;

each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM

dies, each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects~~and second C/A conduits coupled to respective ones of the second~~, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects,~~the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~;

~~wherein~~ a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies;

wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;

~~wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies; each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at~~

~~least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;~~

~~wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;~~

~~wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;~~

~~wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;~~

~~wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;~~

~~wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked~~

~~DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;~~

~~wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;~~

~~wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and~~

~~wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals~~ the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation to, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;

the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;

the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

the control die is configurable to drive the one or more ~~DRAM dies of the stacked~~ DRAM dies via second signals to the second DRAM die and one or more DRAM dies of the plurality of stacked DRAM dies via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;

a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and

each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

U.S. Patent No. 12,308,087 – Claim 1 v. Claim 20

1. — ~~20.~~ A dynamic random access memory (DRAM) package, comprising: stacked DRAM dies ~~including at least a first plurality of DRAM dies and a second plurality of DRAM dies~~, each DRAM die of the stacked DRAM dies including ~~C/A ports~~, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells; terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and ~~is further configured to receive or output~~ receives or outputs data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a ~~first~~ set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation;

, n being 32 or 64; die interconnects including C/A interconnects and data interconnects, the C/A interconnects including ~~at least first C/A interconnects and second C/A interconnects, the first~~ first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including ~~at least a first data interconnects and second data interconnects, the first~~ set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal, signal, wherein each ~~of the~~ die interconnect of the die interconnects ~~including~~ includes one or more ~~through silicon vias (TSVs)~~ in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies ~~in the stacked DRAM dies~~ through the one or more TSVs; and a control die coupled between the

terminals and the stacked DRAM dies, the control die including conduits, ~~the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A die interconnects and second C/A conduits coupled to respective ones of the second C/A~~; wherein the data interconnects, ~~the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~

~~wherein~~ include at least a first C/A data interconnect ~~of~~ and a second data interconnect, the first C/A ~~interconnects is~~ data interconnect configured to be in electrical communication with a corresponding C/A ~~ports on the~~ data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any C/A data port ~~on~~ of any of ~~the second plurality of DRAM dies;~~

~~wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second~~ a second plurality of DRAM dies ~~and not in electrical communication with any C/A port on any of the first plurality of stacked~~ DRAM dies;

~~wherein a first, the second~~ data interconnect ~~of the first data interconnects is~~ configured to be in electrical communication with a corresponding data ~~ports on the first port of each of a second~~ plurality of DRAM dies and not in electrical communication with any data port ~~on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the~~

~~each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;~~

~~wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;~~

~~wherein~~ of any of the first plurality of DRAM dies; wherein the conduits include at least a first data conduit ~~of and a second data conduit~~, the first data conduits is being coupled between the first data interconnect and a first data terminal of the data terminals, and ~~a second conduit of the second data~~ conduits is conduit being coupled between the second data interconnect and the first data terminal; wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second conduits data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal; wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects; wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects; wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive

one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects; wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

~~wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;~~

~~wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;~~

~~wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;~~

~~wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and~~

~~wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.~~

U.S. Patent No. 12,308,087 – Claim 1 v. Claim 23

~~1-23.~~ A dynamic random access memory (DRAM) package, comprising: stacked DRAM dies ~~including at least a first plurality of DRAM dies and a second plurality of DRAM dies,~~ each DRAM die of the stacked DRAM dies including ~~C/A ports,~~ data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells; terminals including command and/or address (C/A) terminals, data terminals, and datapower supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output a first n-bit-wide data signal~~signal via the data terminals~~ in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal~~signal via the data terminals~~ in response to a second set of C/A signals associated with a memory write operation;

, n being 32 or 64; die interconnects including C/A interconnects and data interconnects, the C/A interconnects including ~~at least first C/A interconnects and second C/A interconnects,~~ the first a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including ~~at least a first data interconnects and second data interconnects,~~ the first set of data interconnects configured to conduct the first n-bit-wide data signal~~signal~~ and the second n-bit-wide data signal~~signal,~~ wherein each of the die interconnect of the die interconnects ~~including~~includes one or more ~~through silicon vias (TSVs)~~ in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies ~~in the stacked DRAM dies~~ through the one or more TSVs; and a control die coupled between the

terminals and the stacked DRAM dies, the control die including conduits, ~~the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A die interconnects and second C/A conduits coupled to respective ones of the second C/A; wherein the data interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~

~~wherein include at least a first C/A data interconnect of and a second data interconnect,~~ the first ~~C/A interconnects is~~ data interconnect configured to be in electrical communication with a corresponding C/A ports on the data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any ~~C/A data port on of any of the second plurality of DRAM dies;~~

~~wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second a second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of stacked DRAM dies;~~

~~wherein a first, the second data interconnect of the first data interconnects is configured to be~~ in electrical communication with a corresponding data ports on the first port of each of a second plurality of DRAM dies and not in electrical communication with any data port ~~on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the~~

~~each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;~~

~~wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;~~

~~wherein~~ of any of the first plurality of DRAM dies; wherein the conduits include at least a first data conduit ~~of and a second data conduit~~, the first data conduits is being coupled between the first data interconnect and a first data terminal of the data terminals, and ~~a second conduit of~~ the second data ~~conduits is~~ conduit being coupled between the second data interconnect and the first data terminal; wherein the control die further includes control logic configurable to control respective states of the first data conduit and ~~the~~ second ~~conduits~~ data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal; wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects; wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects; wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and wherein, in response to the second set of C/A signals, the control die is configured to drive one or

more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects; wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

~~wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;~~

~~wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die;~~

~~wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to~~

~~drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;~~

~~wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and~~

~~wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.~~

24. 1. A dynamic random access memory (DRAM) package, comprising:

stacked DRAM dies ~~including at least a first plurality of DRAM dies and a second plurality of DRAM dies,~~ wherein each DRAM die of the stacked DRAM dies ~~including C/A ports, data~~ includes signal ports and DRAM memory cells, ~~wherein the each DRAM die and~~ is configurable to ~~transfer data between the data ports and the DRAM memory cells;~~

~~terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation~~ a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;

~~die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;~~

~~a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~

~~wherein a first C/A~~ an interface via which the DRAM package receives C/A signals and receives or outputs data signals;

~~a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;~~ a control die coupled between the interface and the stacked DRAM dies, the control die including signal conduits and logic configured to control at least some of the signal conduits; and

~~die interconnects, each die interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;~~

~~wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;~~

~~wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at~~

~~least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;~~

~~wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;~~

~~wherein a first conduit of the first data conduits is interconnects coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;~~

~~wherein the control die further includes at least one corresponding conduit in the control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals,~~

~~wherein the one or more C/A signals do not include any chip select signal and one corresponding signal port in each of a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;~~

~~wherein:~~

~~the signal conduits include first conduits, second conduits, third conduits and fourth conduits;~~

the die interconnects ~~further include first~~ include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;

each of the first conduits being a unidirectional ~~interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die conduit configurable to drive a signal to a corresponding first die interconnect~~ and not ~~configured~~ configurable to conduct ~~receive~~ any signal from the ~~control die to any of the stacked DRAM dies~~ corresponding first die interconnect;

~~wherein the each of the second conduits being a bidirectional conduit~~ configurable to drive a signal to a corresponding one of the second die interconnects ~~further include second~~ or to receive a signal from the corresponding second die interconnect;

each of the third conduits being a unidirectional ~~interconnects configured~~ conduit configurable to conduct ~~signals~~ drive a signal received from ~~the control~~ a corresponding third die interconnect to ~~one or more DRAM dies of the stacked DRAM dies~~ the interface and not ~~configured~~ conduct configurable to drive any signal from any of the stacked ~~DRAM dies to the control~~ corresponding third die interconnect;

~~wherein the control die is configured to receive signals from one or more DRAM dies~~ each of the ~~stacked DRAM dies via the first~~ fourth conduits being a unidirectional ~~interconnects and is not configured~~ conduit configurable to drive ~~any~~ a signal ~~to any of~~ received from the ~~stacked DRAM dies via any of the first unidirectional interconnects;~~

~~wherein the control interface to a corresponding fourth die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects interconnect and is not configured configurable to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and the corresponding fourth die interconnect;~~

~~wherein the control die is configured to, the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;~~

~~in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the memory read operation from first set of C/A signals via a DRAM die first subset of the stacked DRAM dies via the first unidirectional second die interconnects; and in responseto drive the first signals to the second set of C/A signals, drive interface; and a first subset of the third conduits is configured to receive one or more second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;~~

~~in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third~~

signals to the first subset of the second die interconnects; and a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;

in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;

in response to the fourth set of C/A signals, ~~the second unidirectional interconnects~~, a subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eighth signals to a second subset of the fourth die interconnect;

each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;

the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;

the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;

the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.