IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC. and SAMSUNG ELECTRONICS AMERICA, INC.,	)	
Plaintiffs,	)	C.A. No. _____
v.	)	**DEMAND FOR JURY TRIAL**
NETLIST, INC.,	)	
Defendant.	)	

COMPLAINT FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT AND UNENFORCEABILITY; BREACH OF CONTRACT

Plaintiffs Samsung Electronics Co., Ltd. ("SEC"), Samsung Semiconductor, Inc. ("SSI") and Samsung Electronics America, Inc. ("SEA," and together with SEC and SSI, "Samsung") seek a declaration that Samsung does not directly or indirectly infringe United States Patent No. 9,824,035 ("the '035 patent") (Exhibit 1), either literally or under the doctrine of equivalents; a declaration that the '035 patent is unenforceable due to inequitable conduct and unclean hands; and, alternatively, a ruling that Defendant Netlist, Inc. ("Netlist") has breached contractual obligations owed to Samsung, including obligations to license its allegedly essential '035 patent to Samsung and its affiliates on reasonable and non-discriminatory ("RAND") terms and conditions, as follows:

NATURE OF THE ACTION

1. This is an action for a declaratory judgment arising under the patent laws of the United States, Title 35 of the United States Code, and the Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.* and state contract law.

2. This action arises out of Netlist's repeated assertions of patents against Samsung after Netlist unilaterally attempted to terminate an agreement in which Netlist granted Samsung a perpetual, paid-up, worldwide license to Netlist patents, including the '035 patent. Following Netlist's purported termination of the parties' license agreement, since 2021 Netlist has engaged in a multi-forum patent infringement campaign against Samsung. Recently, Netlist filed its latest action, a complaint with the International Trade Commission ("ITC") alleging that Samsung infringes numerous patents, including the '035 patent, and seeking an exclusion order for certain Samsung memory module products. In this action, Samsung seeks a declaratory judgment that it does not infringe the '035 patent and that the '035 patent is unenforceable due to inequitable conduct and unclean hands.

3. Alternatively, Samsung seeks relief for Netlist's breaches of contractual obligations owed to Samsung, including obligations to license the '035 patent to Samsung and its affiliates on RAND terms and conditions. Netlist has insisted the '035 patent is necessarily infringed by the practice of certain standards promulgated by the Joint Electron Device Engineering Council ("JEDEC") and implemented by the Samsung memory modules at issue in this case.

THE PARTIES

4. Samsung Electronics Co., Ltd. is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129, Samsung-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 443-742, Republic of Korea.

5. Samsung Semiconductor, Inc. is a corporation organized and existing under the laws of the State of California, with its principal place of business at 3655 North First Street, San Jose, California 95134.

6. Samsung Electronics America, Inc. is a corporation organized and existing under the laws of the State of New York, with its principal place of business located at 700 Sylvan Ave., Englewood Cliffs, New Jersey 07632.

7. On information and belief, Netlist, Inc. is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 175 Technology Drive, Suite 150, Irvine, California 92618.

JURISDICTION AND VENUE

8. This Court has subject matter jurisdiction over the claim for declaratory judgment of non-infringement and unenforceability (Counts I and III) under 28 U.S.C. §§ 1331, 1338(a), and 2201(a).

9. This Court has subject matter jurisdiction over the breach of contract claim (Count II) pursuant to 28 U.S.C. § 1367. The breach of contract claim forms part of the same case or controversy as the claim for declaratory judgment of non-infringement asserted by Samsung in this action.

10. This Court has personal jurisdiction over Netlist, a corporation organized and existing under the laws of the State of Delaware.

11. Venue is proper in this District under 28 U.S.C. § 1391(b)–(c) because Netlist is subject to personal jurisdiction in this District.

12. An immediate, real, and justiciable controversy exists between Samsung and Netlist as to whether Samsung has infringed the ’035 patent and whether the ’035 patent is unenforceable.

A. Netlist’s Assertion of the ’035 Patent and Related Patent

13. On September 30, 2025, Netlist filed a complaint with the ITC alleging that Samsung infringes six patents, including the ’035 patent, related to dual in-line memory modules

("DIMM"), a type of dynamic random access memory ("DRAM"). Netlist's complaint accuses Samsung DDR5 multiplexed rank dual in-line memory modules ("MRDIMM") of infringing the '035 patent. The ITC has not yet instituted the investigation.

14. As described below, Netlist's ITC action followed Netlist's assertion against Samsung of a related patent, U.S. Patent No. 10,268,608 ("the '608 patent") in the Eastern District of Texas. *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:22-cv-293-JRG (E.D. Tex.) (the "EDTX II Action"). The '608 patent is a continuation of the '035 patent. On November 12, 2024, the Eastern District of Texas held a trial to determine whether, *inter alia*, Samsung infringed the '608 patent. The jury returned a verdict favorable to Netlist. *See* EDTX II Action, D.I. 847.

15. Netlist has also asserted the '035 and '608 patents against Samsung's competitor, Micron Technology Inc ("Micron"). On April 28, 2021, Netlist filed a complaint against Micron in the U.S. District Court for the Western District of Texas alleging infringement of the '035 and '608 patents. *Netlist, Inc. v. Micron Tech. Inc.*, C.A. No. 22-cv-00136, D.I. 1. On December 23, 2021, Micron filed a petition for *inter partes* review of the '035 patent, IPR2022-00236, and the Patent Trial and Appeal Board ("PTAB") ultimately found claims 1, 10–13, and 21–22 of the '035 patent unpatentable for obviousness. Netlist's case against Micron remains pending.

B. Netlist's Notice of Infringement and Litigation Campaign Against Samsung and the Industry

16. In 2015, Netlist and SEC entered into a Joint Development and License Agreement (the "Agreement" or "JDLA"). The Agreement contains a patent cross-license provision, granting Samsung a license to Netlist's entire patent portfolio, including the '035 patent. On July 15, 2020, Netlist wrote to Samsung, alleging that Samsung had breached the Agreement

and stating that "Netlist is hereby terminating, effective immediately, the Agreement including the patent license granted to Samsung . . . ."

17. After Netlist unilaterally declared that Samsung was no longer licensed to Netlist's patent portfolio, Netlist issued a "Notice of Infringement" letter to Samsung and subsequently began a years-long, multi-forum patent infringement litigation campaign against Samsung.

18. Specifically, Netlist sued Samsung four times in the Eastern District of Texas on numerous patents related to memory modules. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:21-cv-463-JRG, D.I. (E.D. Tex.) (the "EDTX I Action"); *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:22-cv-293-JRG, D.I. 1 (E.D. Tex.) (the "EDTX II Action"); *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:25-cv-557-JRG, D.I. 1 (E.D. Tex.) ("the EDTX III Action"); *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:25-cv-748 (E.D. Tex.), D.I. 1 ("the EDTX IV Action").

19. Netlist has also filed suit against Samsung in Germany, asserting two patents against some of the same products at issue in this case. *Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, Nos. 4c O 31/22, 4c O 45/22 (Düsseldorf Regional Court).

20. Netlist has also sued numerous other memory module manufacturers or customers. For instance, from 2016 to 2020, Netlist asserted numerous patents in multiple forums in litigation against a competitor of Samsung, SK hynix. *Netlist, Inc. v. SK hynix America Inc. et al.*, No. 8:16-cv-1605 (C.D. Cal. 2016); *Netlist, Inc. v. SK hynix, Inc. et al.*, No. 8:17-cv-1030 (C.D. Cal. 2017); *In re Certain Memory Modules and Components Thereof, and Products Containing the Same*, No. 337-TA-1023 (U.S.I.T.C. 2016); *In re Certain Memory Modules and Components Thereof*, No. 337-TA-1089 (U.S.I.T.C. 2017); *Netlist, Inc. v. SK hynix Inc. et al.*,

No. 6:20-cv-194 (W.D. Tex. 2020); *Netlist, Inc. v. SK hynix America Inc. et al.*, No. 6:20-cv-525 (W.D. Tex. 2020).

21. Netlist has also recently asserted patents in multiple litigations against Micron, which is a competitor of Samsung with respect to at least certain memory products. *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 6:21-cv-430 (W.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 6:21-cv-431 (W.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:22-cv-203-JRG (E.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:22-cv-294-JRG (E.D. Tex.). *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:25-cv-558-JRG (E.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:25-cv-749-JRG (E.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:25-cv-863-JRG (E.D. Tex.). Netlist also filed suit against Micron in Germany.

22. Netlist has also filed infringement suits against Google in the Northern District of California, *Netlist, Inc. v. Google LLC*, No. 3:09-cv-05718-RS (N.D. Cal.), and in Germany. Netlist also named Google, along with Super Micro Computer, Inc., in the ITC complaint against Samsung.

C. Netlist's Threats of Future Infringement Actions

23. Furthermore, between May 2020 and the present, Netlist has made demands that Samsung take a second license to Netlist's portfolio of patents based on Netlist's claim that it terminated the fully paid-up, worldwide patent license granted in the Agreement.

24. For instance, as noted above, on October 15, 2020, Netlist issued a "Notice of Infringement" to Samsung and demanded that Samsung take a second license to Netlist's patents. Specifically, Netlist demanded that "Samsung and its subsidiaries honor third-party intellectual property rights" and engage in "formal licensing discussions"—"reserv[ing] all rights and remedies" with respect to enforcing its patents against Samsung.

25. On June 7, 2022, Netlist again demanded that Samsung take a second license to Netlist's patent portfolio. In the same correspondence, Netlist identified a number of Netlist patents that are, according to Netlist, essential to implement JEDEC standards and would require a license from Netlist for Netlist's entire DIMM patent portfolio. On information and belief, the DIMM patent portfolio to which Samsung will need another license, according to Netlist, includes the '035 patent.

26. On June 4, 2023, Netlist again contacted Samsung, touting its broad patent portfolio and alleging that Netlist owns other patent that it had not yet asserted against Samsung that cover memory technologies. Netlist demanded that Samsung take a license to Netlist's entire patent portfolio; otherwise, according to Netlist, Samsung would be liable for future damages awards and penalties.

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27. Accordingly, as set forth herein, Netlist has sought to enforce the '035 patent and patents in the same patent family as the '035 patent against Samsung products currently being sold and used throughout the United States. Because this action presents an actual controversy with respect to the '035 patent, the Court may grant the declaratory relief sought pursuant to 28 U.S.C. § 2201 *et seq*.

BACKGROUND

A. Netlist's Extraordinary License Demand and Infringement Threats

28. As noted, on November 12, 2015, Netlist and SEC entered into the JDLA. The Agreement contains cross-license, joint development, and product supply provisions. In the Agreement, Netlist granted SEC and its subsidiaries, including SSI and SEA, a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by Netlist or any of its

subsidiaries having an effective first filing date on or prior to November 12, 2020. The license extends through the expiration of the last to expire of the licensed patents.

29. SEC similarly granted Netlist and its subsidiaries a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by SEC or any of its subsidiaries having an effective first filing date on or prior to November 12, 2020.

30. The Agreement required SEC to make a payment to Netlist of $8 million subject to the terms and conditions therein. SEC made this payment to Netlist, except for a portion that was remitted as tax withholding to the Korean tax authorities, which later refunded the withheld portion to Netlist.

31. Since 2020, Netlist has taken extraordinary actions to back out of its grant of a patent license to Samsung.

32. On May 27, 2020, Netlist's Chief Licensing Officer, Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC and alleged that Samsung materially breached the Agreement by "repeatedly fail[ing] to fulfill Netlist's request for NAND and DRAM products throughout the term of the Agreement" and, allegedly, by improperly deducting withholding taxes. Netlist did not allege, and has never alleged, that Samsung breached the Agreement in any way related to the patent cross-license. In the same letter—which was the first time Netlist raised its breach allegations—Mr. Frechette informed Mr. Sung that Netlist had filed a complaint in U.S. District Court for the Central District of California with respect to the alleged breach by Samsung and provided a copy of the complaint for reference.

33. On May 28, 2020, the U.S. District Court for the Central District of California docketed Netlist's breach of contract complaint against SEC. *Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 8:20-cv-00993-MCS (C.D. Cal.) ("Breach Action").

34. Netlist subsequently wrote to SEC to terminate the Agreement, including the patent license to SEC and its subsidiaries. On July 15, 2020, Netlist's Chief Licensing Officer, Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC and stated that "Netlist is hereby terminating, effective immediately, the Agreement including the patent license granted to Samsung . . . ."

35. One week later, on July 22, 2020, Netlist amended its complaint in the Breach Action, seeking a declaration that the license it granted Samsung, but not the license Samsung granted Netlist, was terminated. In the Breach Action, Netlist sought monetary damages and a declaration "that Netlist has terminated the Agreement pursuant to Section 13.2 and that Samsung's licenses and rights under the agreement have ceased."

36. Netlist then issued a "Notice of Infringement" to Samsung and a demand that Samsung take a second license to Netlist's patents. Specifically, on October 15, 2020, Netlist stated that because it had terminated the Agreement, "Samsung is no longer licensed to any of Netlist's portfolio of patents." Netlist further asserted that its patents relate to DIMM products. Netlist then alleged: "Despite the termination of the Joint Development and License Agreement, Samsung continues to unlawfully utilize Netlist's innovations and to infringe Netlist's patents." Netlist concluded the letter by demanding that "Samsung and its subsidiaries honor third-party intellectual property rights" and engage in "formal licensing discussions." Netlist further stated that it "reserves all rights and remedies" with respect to the alleged infringement.

37. Netlist resumed its communications with Samsung in 2021. On February 2, 2021, Netlist's Chief Licensing Counsel, Mr. Marc J. Frechette, indicated by email that Samsung must take a *second* license, coupled with the demand that Netlist "be made whole" for any alleged breach asserted in the Breach Action.

38. Accordingly, Netlist seeks to double-dip, with a demand that Samsung take a second license to Netlist's patents.

39. On October 14, 2021, the court in the Breach Action issued a confidential order granting summary judgment in favor of Netlist on Netlist's Third Claim for Relief, which sought a declaration that Netlist terminated Samsung's license effective July 20, 2020. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 8:20-cv-00993-MCS, D.I. 186 (C.D. Cal.). The court also granted summary judgment in Netlist's favor that Samsung was liable for certain alleged breaches of other provisions in the Agreement. *See id.*

40. Beginning on December 1, 2021, the court in the Breach Action held a jury trial on damages for one of the alleged breaches, the alleged failure to fulfill Netlist's orders for NAND and DRAM products. On December 3, 2021, the jury returned a verdict in Samsung's favor, finding that Netlist failed to prove that it suffered any damages for this alleged breach. *See* Breach Action, D.I. 276. The court in the Breach Action concluded that Netlist was not entitled to damages for the remaining alleged breach (the withholding of taxes) as a matter of law and awarded to Netlist nominal damages of $1.00 for each alleged breach (for a total of $2.00). *Id.*, D.I. 306, ¶¶ 1–2.

41. Despite losing at trial, Netlist issued a press release claiming to be "very pleased with the overall outcome of the case as it confirmed that Samsung no longer has a valid license to Netlist patents and therefore requires a licensing agreement." Netlist Provides Update on Action in Federal Court Against Samsung, https://investors.netlist.com/websites/netlist/English/2120/us-press-release.html?airportNewsID=a661884d-0025-46ea-a055-bae8d8e4570b (last visited Nov. 1, 2025).

42. SEC challenged the summary judgment ruling in the Breach Action on appeal to the Ninth Circuit. *Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, Nos. 22-55209 & 22-55247 (9th Cir.). SEC maintained that it did not breach the Agreement, that the Agreement has not been terminated, and that it continues to hold a paid-up, worldwide, non-exclusive license to Netlist's patents, including the '035 patent.

43. The Ninth Circuit agreed that patent cross-licensing was a distinct aim of the JDLA, independent of the joint development project: "[T]he JDLA has two stated purposes: (1) developing a new NVDIMM-P product (i.e., the [joint development project]), and (2) patent cross-licensing. The title and preamble of the agreement exclusively reference these two topics, and each substantive section corresponds entirely to one of the two goals." D.I. 192, Ex. A at 3–4 (emphasis added). The Ninth Circuit remanded the case to (a) resolve an ambiguity in the supply provision in Section 6.2 of the JDLA and (b) determine whether any breach of that provision by Samsung was material such that Netlist could terminate the agreement. Following the Ninth Circuit's remand, a jury trial was held. On May 17, 2024, the jury issued its verdict, adopting Netlist's proffered meaning of the disputed provision and finding that Samsung's breach of that provision was material. *See* Breach Action, D.I. 556.

44. In post-trial briefing, Samsung requested a new trial. The district court granted Samsung's motion on account of implied juror bias. *Id.*, D.I. 640 at 16.

45. On March 24, 2025, the district court held a new trial, and the jury again adopted Netlist's proffered meaning of the disputed provision. See *id.*, D.I. 769. Samsung appealed the judgment to the United States Court of Appeals for the Ninth Circuit. *Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 25-5531 (9th Cir.).

B. Netlist's Patent Infringement Lawsuits

46. Over the past decade, Netlist has pursued a litigation campaign against Samsung and other suppliers of memory modules, component suppliers, and users of memory modules (aside from Samsung).

1. Netlist's Lawsuits Against Samsung

47. As noted above, on October 15, 2021, Samsung filed a declaratory judgment action against Netlist in this District for a declaration that, *inter alia*, certain Samsung DIMM products did not infringe, *inter alia*, the patents that Netlist included in its "Notice of Infringement" letter. Delaware -1453 Litigation, D.I. 1. In particular, the complaint sought declarations of non-infringement with respect to United States Patent Nos. 10,217,523 (the "'523 patent"), 10,474,595 (the "'595 patent"), 9,858,218 (the "'218 patent"), and 7,619,912 (the "'912 patent"). *Id.* Netlist moved to dismiss Samsung's declaratory judgment claims, arguing that no case or controversy existed because there was no imminent threat of Netlist filing suit against Samsung on the patents-in-suit. *Id.*, D.I. 11 at 3–4. Samsung later amended its complaint, *id.*, D.I. 14, and Netlist moved to dismiss Samsung's First Amended Complaint, *id.*, D.I. 24.

48. On August 1, 2022, the Court in the Delaware -1453 Litigation denied-in-part and granted-in-part Netlist's motion to dismiss Samsung's declaratory judgment claims. The Court found that it has jurisdiction on the patents included in the "Notice of Infringement" letter because, once the Central District of California granted summary judgment in favor of Netlist in the Breach Action, "Netlist's threats became more immediate." *Id.*, D.I. 37 at 4. However, the Court dismissed, *inter alia*, Samsung's declaratory judgment claim of non-infringement related to the '912 patent. *Id.*, D.I. 37. The Court reasoned that the patent had been "the subject of litigation in [the Northern District of California] for over a decade," so Samsung's declaratory judgment claim regarding that patent in Delaware was not "an efficient use of judicial resources." *Id.* at 6.

In reaching its decision, the Court accepted Netlist's argument that Samsung's "collateral action [in Delaware] should be dismissed in favor of the much more advanced Northern District case." *Id*. at 3; *see also id*., D.I. 11 at 3–5; D.I. 28 at 1–3, 8–10 (Netlist arguing that litigation on the '912 patent should proceed in the Northern District of California).

49. Following the Court's order in the Delaware -1453 Litigation, Netlist counterclaimed against Samsung for infringement of all remaining patents. Netlist alleged that Samsung infringed the patents by making, using, selling, offering to sell, and/or importing DDR4 DIMM products. *Id.*, D.I. 40, ¶ 30. Netlist also sought treble damages based on Samsung's alleged willful infringement. *Id*., D.I. 45 ¶ 101. Netlist subsequently expanded its infringement allegations to include Samsung's DDR5 products. *Id*., D.I. 132-1, Ex. 16 at 2.

50. Netlist later asserted counterclaims against Google in the Delaware -1453 Litigation for infringement of the same patents, *i.e.*, the '523, '595, and '218 patents. *Id.*, D.I. 45. Netlist's infringement allegations relate to Google's use of Samsung's DIMM products.

51. On December 20, 2021, Netlist filed a lawsuit against SEC, SSI, and SEA in the Eastern District of Texas alleging direct and indirect infringement of three patents. EDTX I Action, D.I. 1. Netlist alleged that the defendants infringe in connection with the making, selling, using, and/or importing of DDR4 DIMM memory modules, *see id.* ¶¶ 40, 53, and DDR5 memory modules, *see id.* ¶ 68.

52. Netlist filed the EDTX I Action the same day that it moved to dismiss the Delaware Litigation based on, *inter alia*, an alleged lack of any case or controversy over Samsung's declaratory judgment claims. *See* Delaware -1453 Litigation, D.I. 11 at 3 (arguing that the case did not involve a "substantial controversy of sufficient immediacy").

53. Netlist also filed a second suit against Samsung in Texas. The same day the court in the Delaware -1453 Litigation dismissed Samsung's declaratory judgment claims involving the '912 patent—reasoning that litigating the patent in the Northern District of California would be the most efficient use of judicial resources—Netlist filed suit against Samsung on the '912 patent in the Eastern District of Texas. *See* EDTX II Action, D.I. 1. Netlist later amended its complaint to include three additional patents. Netlist alleged that Samsung infringed its patents by making, using, selling, offering to sell, and/or importing DDR4 DIMM memory modules. *Id.* ¶ 34.

54. On May 19, 2025, Netlist filed a third infringement suit—the day before the patent-in-suit had issued from the U.S. Patent and Trademark Office ("Patent Office")—against Samsung in the Texas, asserting a continuation patent of two patents that Netlist asserted against Samsung in the EDTX I Action. *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:25-cv-553-JRG, D.I. 1 (E.D. Tex.). The next day, shortly after midnight, Netlist filed another infringement suit in the Eastern District of Texas, again alleging infringement of the same patent. EDTX III Action, D.I. 1 (E.D. Tex.). On July 8, 2025, Netlist filed an amended complaint in the EDTX III action, adding an additional patent and a Samsung distributor. *Id.*, D.I. 14.

55. Similar to its complaint in the EDTX III Action, Netlist filed another infringement suit against Samsung seconds after the patent issued on July 29, 2025, at midnight EDT. EDTX IV Action, Dkt. 1.

56. As noted, on September 30, 2025, Netlist filed a complaint with the ITC. Netlist seeks an exclusion order from the Commission related to Samsung's alleged infringement of six patents, including the '035 patent.

57. Netlist also filed suit against Samsung in Germany, asserting two patents against Samsung's DDR4 DIMM memory modules. *Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, Nos. 4c O 31/22, 4c O 45/22 (Düsseldorf Regional Court).

2. Netlist's Lawsuits Against Third Parties

58. Netlist has also pursued litigation campaigns against other suppliers of JEDEC standard-compliant memory modules, component suppliers, and users of memory modules. For instance, Netlist engaged in a years-long, multi-forum litigation campaign against SK hynix, a competitor of Samsung. Between 2016 and 2020, Netlist filed six patent infringement suits against SK hynix, the first two in the Central District of California. *See Netlist, Inc. v. SK hynix America Inc. et al.*, No. 8:16-cv-1605 (C.D. Cal. 2016); *Netlist, Inc. v. SK hynix, Inc. et al.*, No. 8:17-cv-1030 (C.D. Cal. 2017). Netlist also filed two complaints against SK hynix with the ITC. *See In re Certain Memory Modules and Components Thereof, and Products Containing the Same*, No. 337-TA-1023 (U.S.I.T.C. 2016); *In re Certain Memory Modules and Components Thereof*, No. 337-TA-1089 (U.S.I.T.C. 2017). Finally, Netlist filed two infringement suits against SK hynix in the Western District of Texas, *Netlist, Inc. v. SK hynix Inc. et al.*, No. 6:20-cv-194 (W.D. Tex. 2020); *Netlist, Inc. v. SK hynix America. et al.*, No. 6:20-cv-525 (W.D. Tex. 2020).

59. In these suits, Netlist accused SK hynix DIMM memory modules of infringing certain Netlist patents.

60. Netlist has also accused Google of infringing the '912 patent in connection with DDR4 DIMM products. *See Netlist, Inc. v. Google Inc.*, No. 3:09-cv-05718-RS (N.D. Cal.). Netlist seeks an injunction in that case, which would preclude Google from using the standard-compliant DIMM memory modules supplied by SSI to Google. Netlist also seeks an injunction against Google in the Delaware -1453 Litigation. D.I. 127 at 11.

61. Netlist has also asserted the ’912 patent against Inphi, a chip supplier. *See Netlist, Inc. v. Inphi Corp.*, No. 2:09-cv-6900 (C.D. Cal. 2009).

62. As noted above, Netlist has also recently asserted patents in multiple litigations in Texas against Micron, which is a competitor of Samsung with respect to at least certain of the memory products at issue. In some of the Micron litigations, Netlist accuses the same type of memory modules at issue in this case.

C. Netlist’s Standard Essential Allegations

63. As noted above, Netlist sued Micron in the Western District of Texas, alleging infringement of the ’035 patent. *Netlist, Inc. v. Micron Tech. Inc.*, C.A. No. 22-cv-00136, D.I. 1. In that action, Netlist contended that the ’035 patent was essential to JEDEC DIMM standards, alleging that “Netlist’s innovative LRDIMM technology has since been adopted by JEDEC in its DDR4 LRDIMM standard that is used by companies throughout the industry.” *Id.* ¶ 23. In other words, in its action against Micron, Netlist attempted to show infringement of the ’035 patent by demonstrating that the JEDEC standard reads on the ’035 patent and therefore Micron’s standard-compliant products necessarily infringed. *Id.* ¶¶ 77–91.

64. In the present action, Samsung seeks declarations that Samsung’s DIMMs that comply with the DDR5 standards or any standard requiring materially similar functionality (“Samsung DDR5 DIMMs”), do not infringe the ’035 patent.

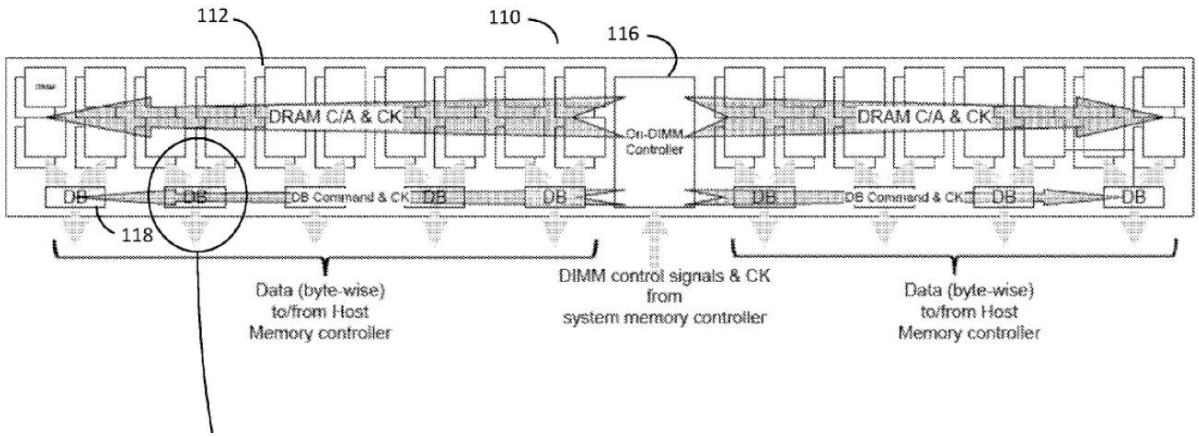
65. If, as Netlist contends, the ’035 patent is essential to any of the JEDEC standards (which they are not), Netlist is obligated to license the patent on RAND terms. As discussed below, Netlist has failed to offer such a license to Samsung.

D. Overview of the ’035 Patent

66. The ’035 patent issued on November 21, 2017, from U.S. Application No. 15/426,064, which was filed on February 7, 2017. The ’035 patent is a continuation of U.S.

Patent Application Ser. No. 14/846,993, to be issued as U.S. Patent No. 9,563,587, which is a continuation of U.S. Patent Application Ser. No. 13/952,599, filed Jul. 27, 2013, issued as U.S. Patent No. 9,128,632, which claims priority to U.S. Provisional Patent Application No. 61/676,883, filed on Jul. 27, 2012.

67. The ’035 patent relates to computer memory modules. ’035 Patent 1:34–36. The disclosed memory module includes multiple memory devices 112, data buffers 118, and a module control device 116, shown in Figure 2C below:



68. Module control device 116 is located at the center of memory module 110. Several memory devices 112 share a respective data buffer 118. *Id.*, 8:31–34. Figure 2C illustrates that data buffers 118 and their associated memory devices 112 are distributed across the memory module at varying distances from the module control device 116. These varying distances result in “unbalanced wire lengths” and different propagation delays—stated otherwise, control signals may take longer to reach farther away memory devices. *Id.*, 2:25–28. Conventional systems used “leveling mechanisms for write and/or read operations” in memory controllers to compensate for such delays. *Id.*, 2:25–28. The ’035 patent alleges, however, that these techniques no longer accurately ensure “proper timing of the control and/or data signals received and/or transmitted by the memory modules.” *Id.*, 2:28–33.

69. The ’035 patent purports to solve this alleged problem using a signal alignment circuit in each data buffer to determine transmission timing. *Id.*, 10:4–18, 15:14–21. Transmission timing is determined based on time information obtained from a prior write operation. *Id.* Using that timing information, the signal alignment circuit calculates the time interval for subsequent read operations. *Id.*

70. For at least the reasons explained in Count I, Samsung DDR5 MRDIMMs (“the Samsung Memory Modules”), do not infringe the claims of the ’035 patent.

E. Netlist Has Breached Contractual Obligations Owed to Samsung

1. JEDEC and Semiconductor Memory Standards

71. JEDEC is an independent, non-profit semiconductor engineering trade association and standardization body based in the United States. Over 300 companies in the computer and electronics industries are currently members of JEDEC, including Samsung and Netlist.

72. JEDEC has become the global leader in developing open standards and publications for a broad range of semiconductor technologies, including memory products. As relevant here, JEDEC develops standards for semiconductor memory chips and modules, including standards implemented by Samsung’s products.

73. JEDEC’s semiconductor memory standards enable interoperability, *i.e.*, the ability of memory products made by different manufacturers to work together with computer and electronic devices made by others. JEDEC standards are widely implemented, and, for many types of semiconductor memory products, it is imperative that they comply with JEDEC standards in order to be commercially viable.

74. Member companies participate in JEDEC’s standard-setting process through over 50 committees and subcommittees that address various technological areas. Through

a collaborative process, members contribute to and vote on technical proposals for incorporation into JEDEC standards. Upon committee and board approval, new standards are promulgated and made available to the public.

75. In some cases, JEDEC members own patents covering the technology they or others seek to have included in a JEDEC standard. A patent that includes a claim or claims that would necessarily be infringed by the use, sale, offer for sale, or disposition of a portion of a product in order to be compliant with an industry standard is referred to as a "standard essential patent" or an "SEP."

76. Each owner of an SEP can, unless restrained, demand and obtain exorbitant royalties for the use of its patent, far in excess of the value, if any, that the patented technology would command had it not been incorporated into a standard. If unwilling to pay such excessive royalties, firms wishing to implement the standard face the risk of being foreclosed from using any portion of the standard, including unpatented and public domain technologies. This threat of foreclosure, if left unchecked, puts a manufacturer's investment in developing standard-compliant products at risk and, in effect, permits the possibility that the SEP holder may capture up to the value of the standard as a whole for each unique implementer, rather than the true value of its specific contribution to the standard, independent of the incorporation of the technology into the standard. The exploitation of SEPs to extract unreasonable or discriminatory royalties is referred to as patent "hold-up."

77. The problem of "hold-up" is exacerbated in the context of standards, like those at issue here, as to which there are large numbers of SEPs and many different firms that claim to hold SEPs. The problem is likewise compounded when the products at issue, like those at

issue here, may be required to implement multiple standards. The resulting problem of excessive aggregate royalties is referred to as "royalty stacking."

78. In order to mitigate these risks, JEDEC—like many other standard-setting organizations—has adopted a Patent Policy that seeks to ensure that owners of SEPs license those patents to manufacturers of standard-compliant products on RAND terms and conditions. Every firm that is a member of a JEDEC committee or a participant in a JEDEC committee meeting, including Netlist, agrees to abide by the JEDEC Patent Policy.

> *All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy ("Patent Policy").*

Ex. 2 (JEDEC Manual No. 21T) § 8.2.2.1.

79. Pursuant to the JEDEC Patent Policy, as a condition of committee membership or participation, all JEDEC committee members agree to disclose "Potentially Essential Patents" relevant to the work of the committee:

> *All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member . . . .*

Id. § 8.2.3.

80. The requirement to disclose "Potentially Essential Patents" extends to disclosing pending patent applications. *Id.* § 8.2.1.

81. JEDEC committee members also agree to license "Essential Patent Claims" on RAND terms and conditions:

> *All Committee Members, as a condition of committee membership or committee Participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.*

Id. § 8.2.2.1.

82. JEDEC committee members also agree to license on RAND terms any "Essential Patent Claims" included in their patent applications:

> For any Essential Patent Claims held or controlled by the entity, *pending[,] or anticipated to be filed*, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments: . . . A license will be offered . . . under reasonable terms and conditions that are free of any unfair discrimination.

Id. § 8.2.5 (emphasis added).

83. The JEDEC Patent Policy defines "Potentially Essential Patent" as a patent that is reasonably believed to contain one or more Essential Patent Claims. *Id*. § 8.2.1. "Essential Patent Claim" is further defined as those "Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC standard." *Id.*

84. The JEDEC Patent Policy provides that the disclosure of Potentially Essential Patents "shall be made as early as reasonably possible" and documented by submission to JEDEC of either a "License Assurance/Disclosure Form" or a "Notice of Refusal." *Id*. § 8.2.3.

85. A License Assurance/Disclosure Form (also known as a "Letter of Assurance" or "LOA") states that the committee member commits to license its SEPs to all potential licensees on RAND terms. On the contrary, a Notice of Refusal states that the member is not "willing to offer to license Essential Patent Claims . . . on RAND terms to all Potential Licensees." *Id*. § 8.2.3.1. In order to be effective, any such LOA or Notice of Refusal must be delivered to the JEDEC Legal Department within thirty (30) calendar days of a draft specification's completion. *Id.*

86. Member companies who disclose and agree to license their patents on RAND terms do so via the aforementioned "LOA" identifying the relevant JEDEC standard(s) and making one of the two following commitments specified by the JEDEC Patent Policy:

> *For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:*
>
> *(i) A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; or*
>
> *(ii) A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.*

Id. § 8.2.5.

87. According to JEDEC's Patent Policy, disclosures and commitments with respect to one patent are deemed to include all patents claiming priority to the same filing. *Id*. § 8.2.1. Committee members are therefore obligated to license on RAND terms later-issuing SEPs that claim priority to patents disclosed to JEDEC.

88. If a committee member who owns or controls patents essential (or potentially essential) to JEDEC standards does not disclose and agree to license them before the ballot closes, or notify the committee of an intention not to license through a "Notice of Refusal," the committee member will be deemed to have agreed to offer licenses on RAND terms:

> *If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form (see Annex A.3) at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of*

> *its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.*

Id. § 8.2.5.

89. The JEDEC Patent Policy provides that it is to be interpreted and governed under the laws of the State of New York. *Id*. § 8.2.10. Although the JEDEC Manual 21 has been updated and amended from time to time, upon information and belief, all of the relevant provisions of the JEDEC Patent Policy have been materially the same at all times relevant hereto.

2. Netlist's RAND Commitments

90. Netlist alleges that it owns over 100 patents and patent applications related to memory technologies.

91. Netlist is also a member of JEDEC and has joined a number of JEDEC technical committees over time. After years of membership in JEDEC, Netlist withdrew from membership in JEDEC briefly in 2011 after submitting Notices of Refusal for a number of Netlist patents. JEDEC reinstated Netlist later in 2011 following Netlist's submission of LOAs for the same patents Netlist had previously refused to license on RAND terms.

92. Netlist again withdrew from membership in JEDEC committees JC-40, JC-42, and JC-45 in 2015, after submitting Notices of Refusal for many of its patents. In May 2018, Netlist requested from the JEDEC board of directors that Netlist be reinstated in those committees. The JEDEC board of directors approved the request on the condition that Netlist would agree to be bound by the JEDEC Patent Policy regarding work conducted in JC-40, JC-42, and JC-45 during the time Netlist had not participated in the committees, since and including February 27, 2015. Netlist agreed in writing to the JEDEC board of directors' terms, and JEDEC reinstated Netlist on August 14, 2018, retroactive to February 27, 2015.

93. Upon information and belief, therefore, at the time that the JEDEC standards were drafted and approved by JEDEC, Netlist was a member, attended the meetings, and/or was deemed a member of the JC-40, JC-42, and JC-45 committees that developed those standards.

94. To date, and on information and belief, Netlist has disclosed that at least 42 of its patents are essential or potentially essential to JEDEC standards.

95. Netlist is obligated to license the ’035 patent on RAND terms to implementers of certain DDR4 and DDR5 standards, to the extent the ’035 patent is essential to those standards. In fact, in its action against Micron related to the ’035 patent, Netlist acknowledged that it had a duty to license the patent on RAND terms, noting that it had committed to license the ’035 patent on RAND terms to implementers of JEDEC standards. *Netlist, Inc. v. Micron Technology Inc.*, C.A. No. 22-cv-00136, D.I. 1 ¶ 26 (“Netlist ‘committed’ the Asserted Patents to various JEDEC standards pursuant to the JEDEC Patent Policy, which sets certain obligations for owners of patents (like the Asserted Patents) that it reasonably believes are essential to one or more JEDEC standards,” i.e., an obligation that “[a] license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination . . . .”).

96. Further, on information and belief, Netlist submitted a Letter of Assurance for U.S. Patent No. 9,128,632 (“the ’632 patent”) on April 7, 2016, related to JEDEC committee JC-40 and DDR4 LRDIMM and RDIMM components. The ’035 patent is a continuation of the ’632 patent. Therefore, under the JEDEC Patent Policy, the commitments in the ’632 Letter of Assurance extend to the ’035 patent. Ex. 2 (JEDEC Manual No. 21T) § 8.2.1.

97. The commitments that Netlist has made to license its SEPs on RAND terms constitute binding contractual obligations that may be enforced by firms seeking to implement the JEDEC standards, such as Samsung.

3. Netlist's Failure to Comply with Its RAND Obligations

98. Although Netlist accepted the benefits of its membership in JEDEC to induce JEDEC to incorporate technologies over which Netlist claims to have patents into JEDEC standards, Netlist has failed to fulfill its corresponding contractual commitments. Despite voluntarily undertaking the obligation to license its alleged SEPs on RAND terms, Netlist has made licensing demands of Samsung that violate its RAND commitment.

99. For instance, by email dated February 2, 2021, Netlist demanded that Samsung enter a second license to patents that Samsung previously licensed from Netlist, coupled with a demand to "be made whole" for any alleged breach under the Agreement. Specifically, Netlist stated that "Samsung will require a new license to our patent portfolio"—which would include the '035 patent—and requested "[d]amages that Netlist has incurred as a result of Samsung's material decrease of product supply to Netlist following Q1 2017 and how Netlist might be made whole."

100. Further, Netlist has brought an ITC action against Samsung on the '035 patent, seeking an exclusion order from the Commission. Such an exclusion request, in addition to Netlist's failure to offer Samsung a license on RAND terms, violates Netlist's commitment to license its alleged SEPs on RAND terms and conditions.

101. Accordingly, and as discussed elsewhere herein, Netlist has breached its obligations under the JEDEC Patent Policy.

COUNT I
(Declaration of Non-Infringement of the ’035 Patent)

102. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

103. The Patent Office issued the ’035 patent, titled “Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers,” on November 21, 2017. On information and belief, Netlist claims to own all rights, title, and interest in the ’035 patent. A true and correct copy of the ’035 patent is attached hereto as Exhibit 1.

104. The ’035 patent issued with 22 claims. In 2023, the PTAB determined that claims 1, 10–13, and 21–22 of the ’035 patent are unpatentable for obviousness. *See* IPR2022-00236. Claim 1 reads as follows:

Element	**Claim Language**
preamble	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
(a)	a module board having edge connections for coupling to respective signal lines in the memory bus;
(b)	a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and
(c)	memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
(d)	a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic

Element	Claim Language
	is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

105. Samsung has not directly or indirectly infringed any claim of the ’035 patent, either literally or under the doctrine of equivalents, at least because the Samsung Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claim of the ’035 patent.

106. For example, claim 1 requires “wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation … .” The Samsung Memory Modules do not satisfy the requirements of claim 1 for at least the reason that the alleged “timing information” is not obtained during a “second memory operation” because the timing information is set based on trainings that are not a “memory operation.” For example, during MDQS Receive Enable (MRE) and MDQS Read Delay (MRD) training the data/strobe signal lines cannot be used to transmit data from the host controller to the memory devices or receive data from the memory devices in the memory modules and send it to the host controller.

107. The Samsung Memory Modules do not infringe any of claims 2–22 at least because these claims depend directly or indirectly from claim 1.

108. Samsung, its customers, and its end users are not liable for infringement of the ’035 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

109. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the ’035 patent by

making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties' respective rights regarding the '035 patent.

110. Samsung seeks a judgment declaring that Samsung and its customers and end users do not infringe the '035 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT II
(Alternative Claim for Breach of Contract)

111. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

112. In the alternative, if the JEDEC-compliant Samsung Memory Modules infringe any claim of the '035 patent, the '035 patent is a standard-essential patent, and Netlist has breached its contractual obligations to license any such patent claim to Samsung on RAND terms and conditions.

113. Under the JEDEC Patent Policy, Netlist has a contractual commitment to offer implementers of the JEDEC standards, including Samsung, licenses to any Essential Patent Claims (as defined in the JEDEC Patent Policy) on RAND terms and conditions. This contractual commitment is on-going. Netlist continues to have an obligation to license its SEPs to Samsung on RAND terms, notwithstanding any breach of the Agreement or any termination of the license contained therein. Having entered the Agreement, Samsung showed that it is a willing licensee.

114. Netlist has acknowledged in litigation that it has a RAND duty related to the '035 patent. Netlist also submitted a Letter of Assurance to the JC-40 committee in which

Netlist promised to make available to implementers of the DDR4 standards a license to the ’632 patent “under reasonable terms and conditions that are demonstrably free of any unfair discrimination.” Under the JEDEC Patent Policy, those commitments extend to the claims of the ’035 patent, to the extent they are essential to the JEDEC standards.

115. The JEDEC Patent Policy and/or Letters of Assurance constitute a valid and binding contract between Netlist and JEDEC.

116. Samsung is a third-party beneficiary to the JEDEC Patent Policy and/or Letters of Assurance, and to Netlist’s RAND obligations thereunder. Participation in JEDEC committees and the standard-setting process is expressly conditioned on a commitment to license essential patents to third-party implementers on RAND terms. Ex. 2 (JEDEC Manual No. 21T) § 8.2.2.1. The JEDEC Patent Policy is therefore intended to benefit third-party implementers of JEDEC standards, such as Samsung, and the obligations under the JEDEC Patent Policy, including the RAND obligations, are intended to be enforceable by third-party implementers of the JEDEC standards. Third-party implementers, such as Samsung, are also the only parties who could recover for Netlist’s breach of its obligations under the JEDEC Patent Policy.

117. Samsung has relied on the JEDEC Patent Policy and/or Letters of Assurance, including the RAND obligations set forth therein, in designing, manufacturing, and selling standard-compliant products, including the Samsung Memory Modules, and Samsung has supported the JEDEC standard based on its understanding and expectation that JEDEC members, including Netlist, will abide by their obligations.

118. In ongoing litigation, Netlist and Samsung dispute whether Samsung has a license to Netlist’s patents, including the ’035 patent, under the Agreement. Netlist has taken the position that Samsung’s license under the Agreement has been terminated, while Samsung

maintains that the termination was not effective and that it has a license to the ’035 patent. As set forth above, Netlist has demanded that Samsung enter a second license to patents that Samsung previously licensed from Netlist, specifically demanding that because of the alleged JDLA termination “Samsung will require a new license to our patent portfolio,” which would include the ’035 patent.

119. Although Netlist accepted the benefits of its membership in JEDEC, Netlist has failed to fulfill its corresponding contractual commitments. In particular, since the date of Netlist’s purported termination of the JDLA to the present, Netlist has failed to offer Samsung a license to patents that Netlist alleges are essential to the JEDEC standards, including the ’035 patent, on RAND terms and conditions. The licensing demands Netlist has made of Samsung, including in or around February 23, 2023, and June 4, 2023, violate its RAND commitment.

120. If the data buffer and associated training modes required by JEDEC specifications, such as DRAM-to-DB Read Delay (MRD) Training Mode as defined in JESD82-32 for DDR4 and JESD82-521 for DDR5, infringe the ’035 patent, then the patent is essential. To the extent the ’035 patent is essential to any of the JEDEC standards, Netlist has breached its contractual obligations to license such patent to Samsung on RAND terms and conditions.

121. As a result of Netlist’s breaches of contract, Samsung has been injured in its business or property because it has been denied access to a license to Netlist’s claimed SEP on RAND terms, a license that can only be obtained from Netlist. Netlist’s conduct threatens Samsung with imminent loss of customers and potential customers, loss of goodwill and product image, loss of sales, litigation costs, uncertainty in business planning, and uncertainty among customers and potential customers.

COUNT III
(Declaration of Unenforceability of the ’035 Patent Due to Inequitable Conduct & Unclean Hands)

122. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

123. On information and belief, at least the following people associated with Netlist were substantively involved in the prosecution of the application that issued as the ’035 patent: Hyun Lee; Jayesh Bhakta; Gail Sasaki; and patent prosecution counsel Jamie Zheng (collectively “Netlist Individuals Substantively Involved in the ’035 Patent Prosecution”).

124. Hyun Lee and Jayesh Bhakta are the named inventors of the ’035 patent and signed oaths that were submitted with the application attesting to being the inventors of the alleged invention(s) claimed in the application.

125. On information and belief, Gail Sasaki was, during the prosecution of the application that issued as the ’035 patent, an employee and/or contractor for Netlist who signed the power of attorney for the application that issued as the ’035 patent.

126. Jamie Zheng is the prosecuting attorney for the application that issued as the ’035 patent.

127. On information and belief, each of the Netlist Individuals Substantively Involved in the ’035 Patent Prosecution is an individual associated with the filing and prosecution of the application that issued as the ’035 patent.

A. Netlist Attends JEDEC Meetings

128. On information and belief Netlist representatives, including Hyun Lee, attended dozens of JEDEC meetings for years and listened to technological presentations from other JEDEC members. Then, Netlist incorporated key concepts from presentations that Netlist’s

JEDEC representatives learned during meetings into the patent family that includes the ’035 patent.

129. For example, on information and belief, Mr. Hyun Lee, an inventor of the ’035 patent, regularly attended JEDEC meetings for at least the JC-40 committee in 2011 and 2012, as well as before and after that timeframe, including the meetings occurring on December 8, 2011, in San Diego, California; on Mar. 5, 2012, in Hong Kong, China; and on June 4, 2012, in Washington, D.C. Similarly, Netlist regularly sent individuals to attend meetings for the JC-45 committee.

130. During the December 8, 2011 JC-40 meeting in San Diego, JEDEC member Intel Corporation (“Intel”) presented and discussed Committee Item Number 158.01 (“DDR4 LRDIMM Proposal”). On information and belief, the draft of Committee Item Number 158.01 was created by employees of Intel and circulated at or before, and discussed at, the JC-40 committee meeting on December 8, 2011, that Hyun Lee attended.

131. Intel also presented two other items in subsequent JC-40 meetings in 2012, Committee Item Number 0311.14 (“Proposed DDR4 DB Training Modes”) at the March 25, 2012 meeting and Committee Item Number 0311.12 (“Proposed DDR DB Buffer Control Words”) at the June 4, 2012 meeting. On information and belief, drafts of Committee Item Number 0311.14 and Committee Item Number 0311.12 were created by employees of Intel and circulated at or before, and discussed at, the JC-40 committee meetings on March 5, 2012, and June 4, 2012, respectively, both of which Hyun Lee attended.

132. On information and belief, and based on Netlist’s alleged scope of the ’035 patent, each of the JC-40 presentations, Committee Item Numbers 158.01, 0311.14, and 0311.12, disclose materially the same structure and functionality that Netlist has accused of infringing the

claims of the ’035 patent. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee attended these presentations and was aware of their content.

133. On information and belief, Hyun Lee shared JEDEC presentations with at least Jayesh Bhakta before the application that issued as the ’035 patent was filed.

B. Prosecution of the ’035 Patent

134. On information and belief, after attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist’s California office and hurriedly completed drafting the provisional application to which the ’035 patent claims priority, naming himself as the inventor, and had U.S. Provisional App. No. 61/676,883 filed on July 27, 2012. Netlist filed a request to correct inventorship on September 26, 2012, adding Jay R. Bhakta as a co-inventor.

135. Netlist filed the application, No. 15/426,064, which ultimately issued as the ’035 patent, on Nov. 21, 2017.

136. The inventors and others knew of these JEDEC presentations before the application that issued as the ’035 patent was even filed. Netlist did not submit an information disclosure statement for the ’035 patent. Netlist did not otherwise disclose these JEDEC presentations to the examiner.

C. Netlist Accuses Products that Implement the Disclosed Structures and Training Modes

137. Netlist subsequently attempted to claim LRDIMM training and similar concepts in the ’035 patent that were disclosed in the Intel JC-40 presentations from 2011 and 2012, with Netlist claiming priority for these concepts to the provisional application filed on July 27, 2012. On information and belief, Netlist did not invent the full scope of the claims in the

’035 patent, as it represented to the Patent Office in its applications for those patents. Upon information and belief, Netlist simply took certain ideas about the function of LRDIMMs and other DIMMs from presentations that Mr. Hyun Lee, among other Netlist JEDEC representatives, attended as early as 2011.

138. The JEDEC presentations are not cumulative of other art or information before the examiner of the application that issued as the ’035 patent. For example, in a Final Written Decision for IPR2022-00236, the Patent Office relied on a combination of U.S. Patent Publication 2010/0312925A1 to Osani and U.S. Patent No. 8,020,022 to Tokuhiro to invalidate multiple claims of the ’035 patent. In particular, Osani discloses a module structure that mirrors the structure disclosed in Committee Item Number 158.01. Tokuhiro discloses JEDEC’s DDR3 write leveling mechanism, which the Patent Office determined is a “second memory operation” as claimed in the ’035 patent.

139. The Patent Office would not have allowed at least one claim of the ’035 patent to issue had it been aware of the JEDEC presentations and standards, at least because it would have found a claim obvious over that art, for similar reasons that it found the claims invalid in IPR2022-00236.

140. On information and belief, Netlist Individuals Substantively Involved in the ’035 Patent Prosecution, for instance at least Hyun Lee, recognized the materiality of that art and specifically intended to deceive the Patent Office into believing that the claims of the ’035 patent are patentable by withholding that art from the examiner during prosecution of the application that issued as the ’035 patent; and Netlist Individuals Substantively Involved in the ’035 Patent Prosecution, for instance at least Jamie Zheng, specifically intended to deceive the Patent Office into believing that the claims of the ’035 patent are patentable by foregoing presenting the pending

claims in the application to Hyun Lee and electing not to ask Hyun Lee for relevant, material art such as relevant JEDEC presentations, such that they could forego submitting such art to the examiner during prosecution of the application that issued as the ’035 patent.

* * * *

141. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the prosecution of the ’035 patent that renders the ’035 patent unenforceable.

142. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist has unclean hands in relation to its assertion of the ’035 patent that renders the ’035 patent unenforceable.

JURY DEMAND

Samsung demands a jury trial on all issues and claims so triable.

PRAYER FOR RELIEF

WHEREFORE, Samsung prays for judgment and relief as follows:

(a) Declare that Samsung does not directly or indirectly infringe the ’035 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’035 patent;

(b) In the alternative, declare that Netlist is liable for breach of contract; and

(1) Grant injunctive relief requiring that any Netlist demand that Samsung take a license to the ’035 patent—to the extent the patent is found to be essential to the JEDEC standards—must be on reasonable terms and conditions that are demonstrably free from any unfair discrimination;

(2) Enjoin Netlist from further demanding excessive, non-RAND royalties from Samsung for alleged infringement of the ’035 patent;

(3) Declare that Netlist is barred from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end-users in any jurisdiction with respect to any alleged infringement of the ’035 patent;

(4) Enjoin Netlist from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end users in any jurisdiction with respect to any alleged infringement of the ’035 patent;

(5) Compensate Samsung for all damages caused by Netlist’s breaches of contract, including breaches of its RAND obligations;

(c) Declare that the ’035 patent is unenforceable due to inequitable conduct and/or unclean hands;

(d) Declare that judgment be entered in favor of Samsung and against Netlist on Samsung’s claims;

(e) Find that this is an exceptional case under 35 U.S.C. § 285;

(f) Award Samsung pre-judgment and post-judgment interest;

(g) Award Samsung its costs and attorneys’ fees in connection with this action; and

(h) Such further and additional relief as the Court deems just and proper.

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November 11, 2025

EXHIBIT 1

US009824035B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 9,824,035 B2**
(45) **Date of Patent: *Nov. 21, 2017**

(54) **MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Hyun Lee**, Ledera Ranch, CA (US); **Jayesh R. Bhakta**, Cerritos, CA (US)

(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/426,064**

(22) Filed: **Feb. 7, 2017**

(65) **Prior Publication Data**

US 2017/0147514 A1 May 25, 2017

Related U.S. Application Data

(63) Continuation of application No. 14/846,993, filed on Sep. 7, 2015, now Pat. No. 9,563,587, which is a (Continued)

(51) **Int. Cl.**

G06F 3/00	(2006.01)
G06F 12/00	(2006.01)
G06F 13/00	(2006.01)
G06F 13/16	(2006.01)
G06F 3/06	(2006.01)
G11C 8/18	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 13/1673*** (2013.01); ***G06F 3/0613*** (2013.01); ***G06F 3/0656*** (2013.01); ***G06F 3/0659*** (2013.01); ***G06F 3/0683*** (2013.01); ***G06F 13/1642*** (2013.01); ***G11C 8/18*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,884,619 B1 * 2/2011 Chong G01R 31/3016 324/601
8,214,616 B2 * 7/2012 Ware G06F 13/1684 711/104

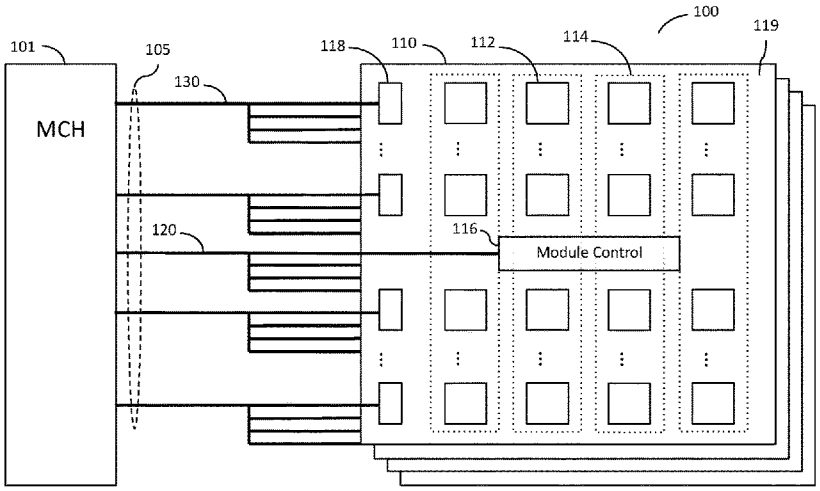
(Continued)

Primary Examiner — Michael Sun
(74) *Attorney, Agent, or Firm* — Maschoff Brennan

(57) **ABSTRACT**

A memory module is operatable in a memory system with a memory controller. The memory module comprises a module control device mounted on the module board to receive command signals from the memory controller and to output module command signals and module control signals, and memory devices mounted on the module board to perform a first memory operation in response to the module command signals. The memory module further comprises a plurality of buffer circuits distributed across a surface of the module board. Each respective buffer circuit is associated with a respective set of the memory devices and includes logic that is configured to obtain timing information based on signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals through the each respective buffer circuit in accordance with the timing information.

22 Claims, 26 Drawing Sheets



Related U.S. Application Data

continuation of application No. 13/952,599, filed on Jul. 27, 2013, now Pat. No. 9,128,632.

(60) Provisional application No. 61/676,883, filed on Jul. 27, 2012.

(56) **References Cited**

U.S. PATENT DOCUMENTS

8,565,033	B1 *	10/2013	Manoharajah	G11C 29/028 365/129
8,949,519	B2 *	2/2015	Rajan	G11O 5/02 365/189.2
2002/0039323	A1 *	4/2002	Tokutome	G11C 7/1066 365/233.12
2006/0077731	A1 *	4/2006	Ware	G11C 5/04 365/194
2007/0217559	A1 *	9/2007	Stott	G11C 7/1051 375/355
2008/0037412	A1 *	2/2008	Geile	G06F 17/14 370/208
2010/0271092	A1 *	10/2010	Zerbe	G06F 13/4243 327/161
2012/0256639	A1 *	10/2012	Pausini	G01R 31/31709 324/613
2014/0029370	A1 *	1/2014	Koshizuka	G11C 7/1051 365/233.13

* cited by examiner

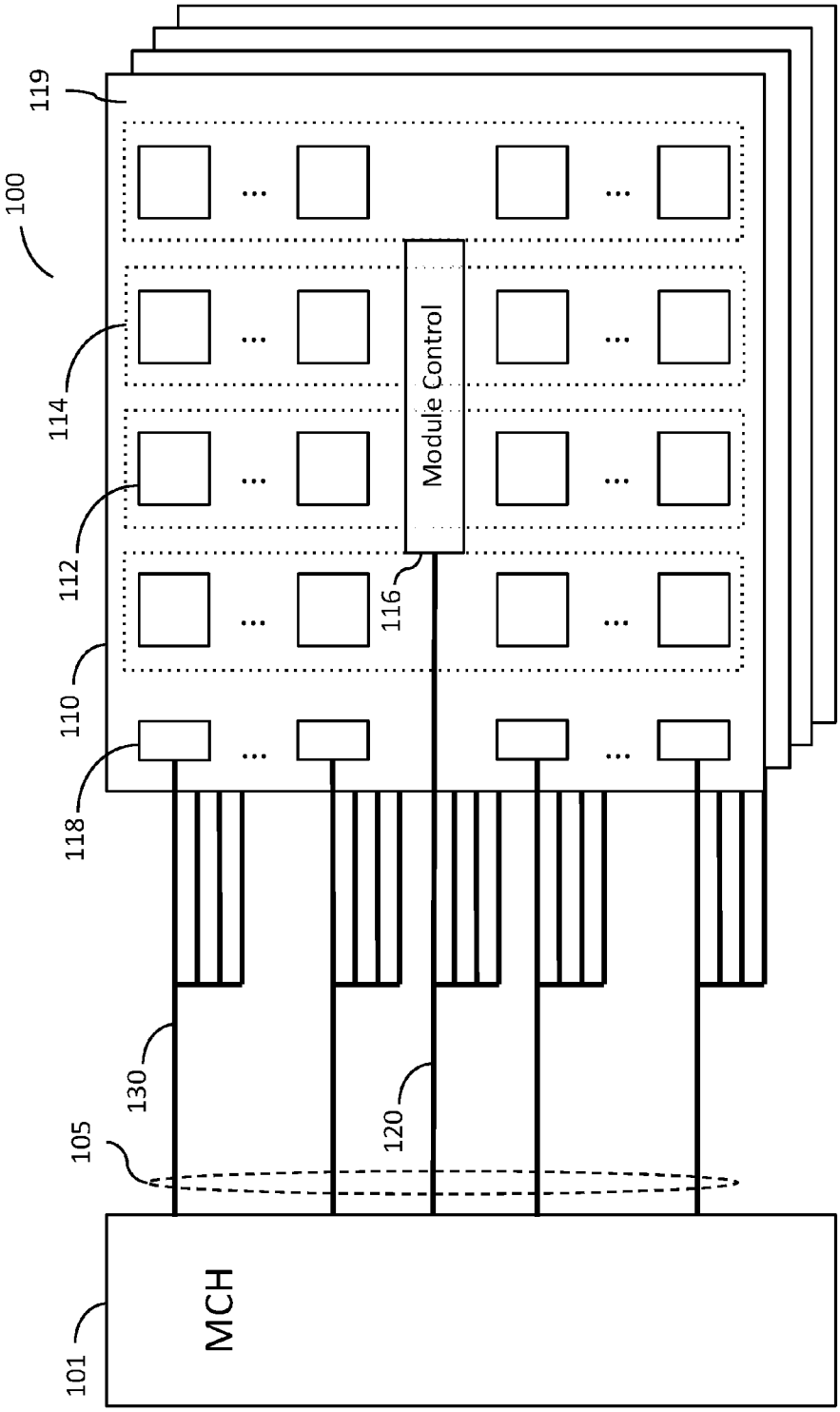


FIG. 1

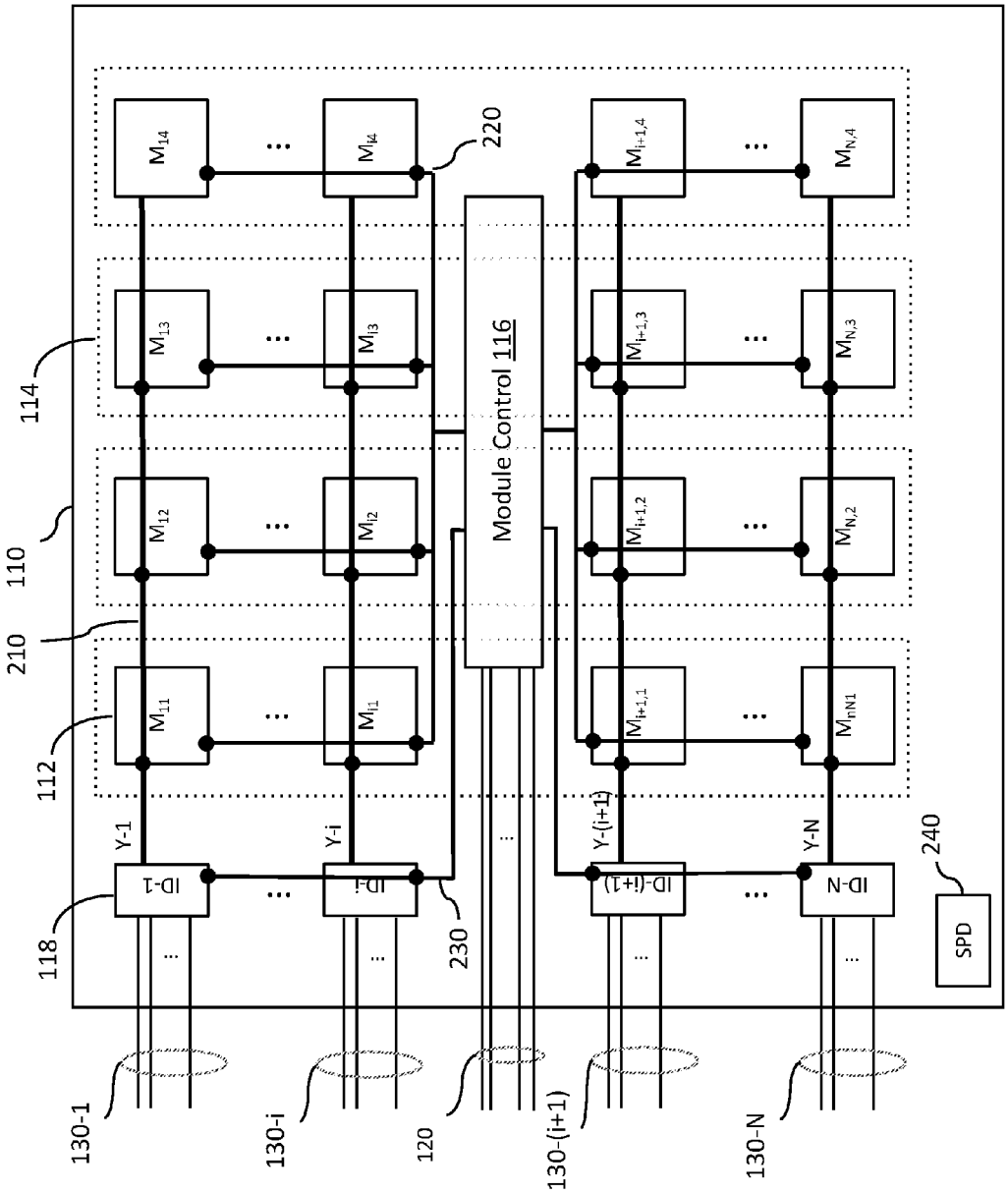
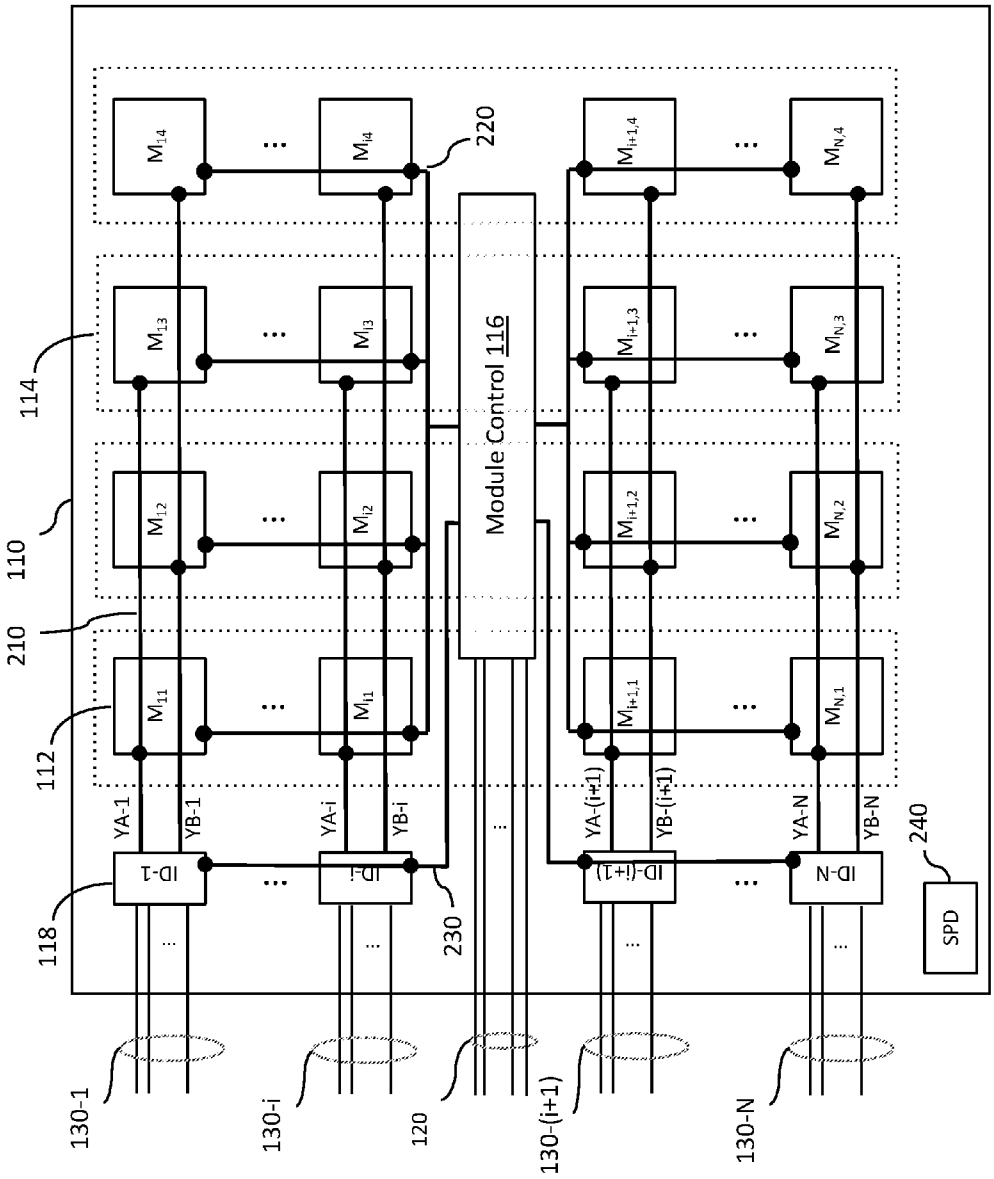

Module Control 116
SPD
ID-1
ID-i
ID-(i+1)
ID-N
Y-1
Y-i
Y-(i+1)
Y-N
M11
M12
M13
M14
M1i
M1i+1,1
M1i+1,2
M1i+1,3
M1i+1,4
MiN1
MN,2
MN,3
MN,4
110
112
114
118
120
130-1
130-i
130-(i+1)
130-N
210
220
230
240

FIG. 2A



Module Control 116
220
230
240
SPD
110
112
114
118
210
YA-1
YB-1
YA-i
YB-i
YA-(i+1)
YB-(i+1)
YA-N
YB-N
ID-1
ID-i
ID-(i+1)
ID-N
130-1
130-i
120
130-(i+1)
130-N

FIG. 2B

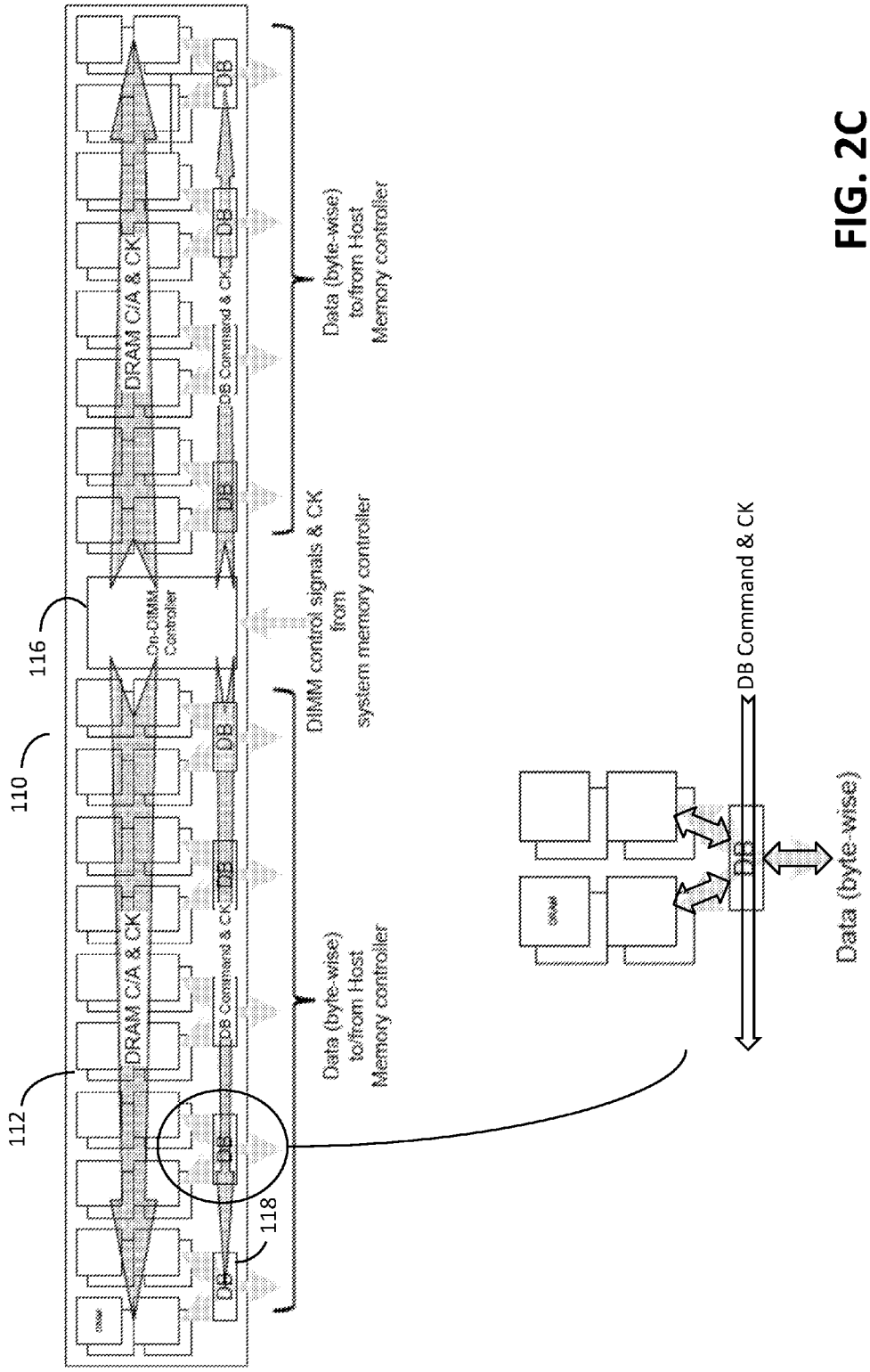

112
110
116
118
DRAM C/A & CK
DRAM C/A & CK
On-DIMM Controller
DB Command & CK
DB Command & CK
DB
DB
DB
DB
DB
DB
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
Data (byte-wise) to/from Host Memory controller
DB Command & CK
DB
Data (byte-wise)

FIG. 2C

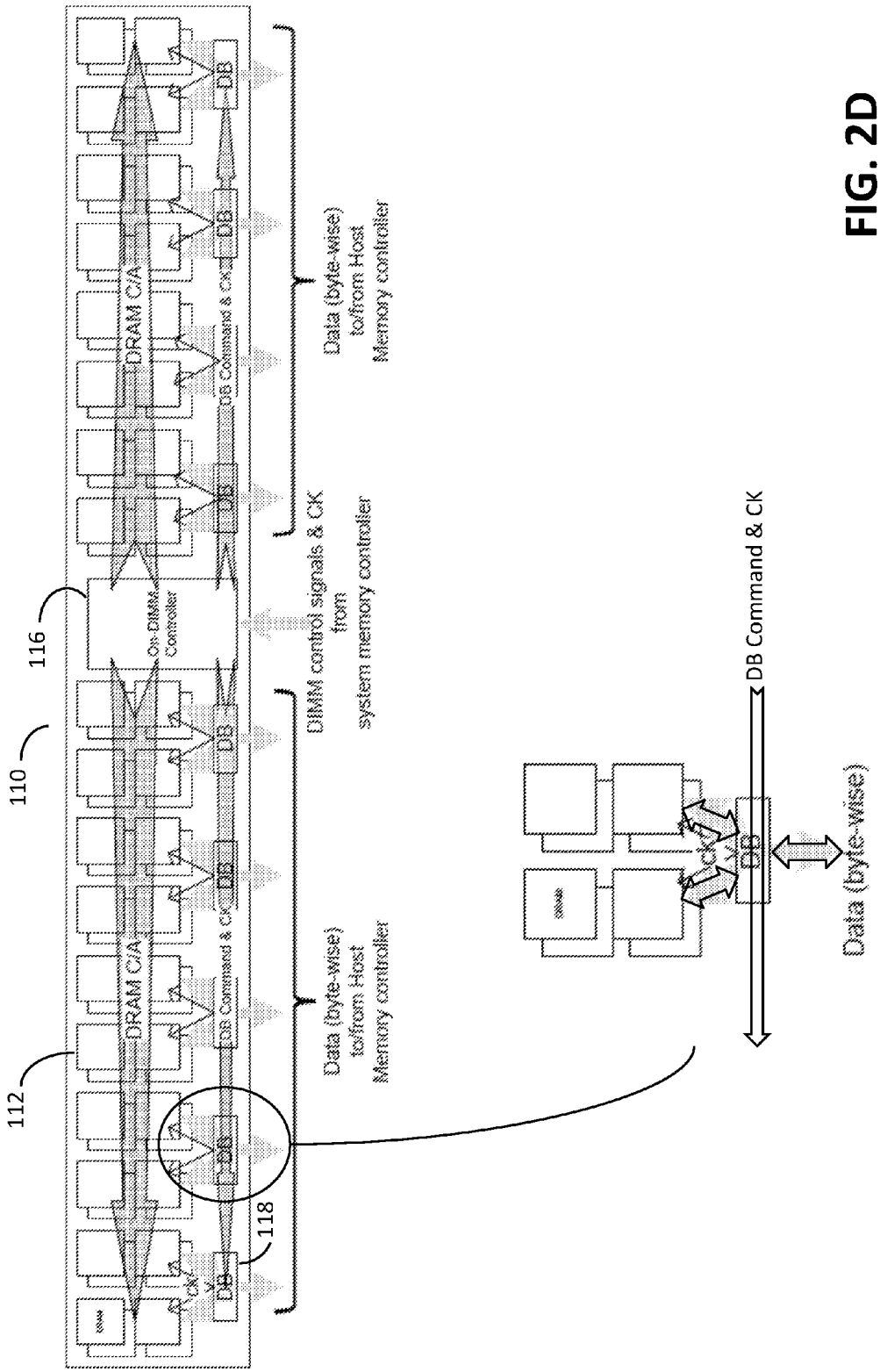

110
112
116
118
DRAM C/A
DRAM C/A
On-DIMM Controller
DB Command & CK
DB Command & CK
DB
DB
DB
DB
DB
DB
DB
CK
V
Data (byte-wise) to/from Host Memory controller
Data (byte-wise) to/from Host Memory controller
DIMM control signals & CK from system memory controller
DB Command & CK
Data (byte-wise)

FIG. 2D

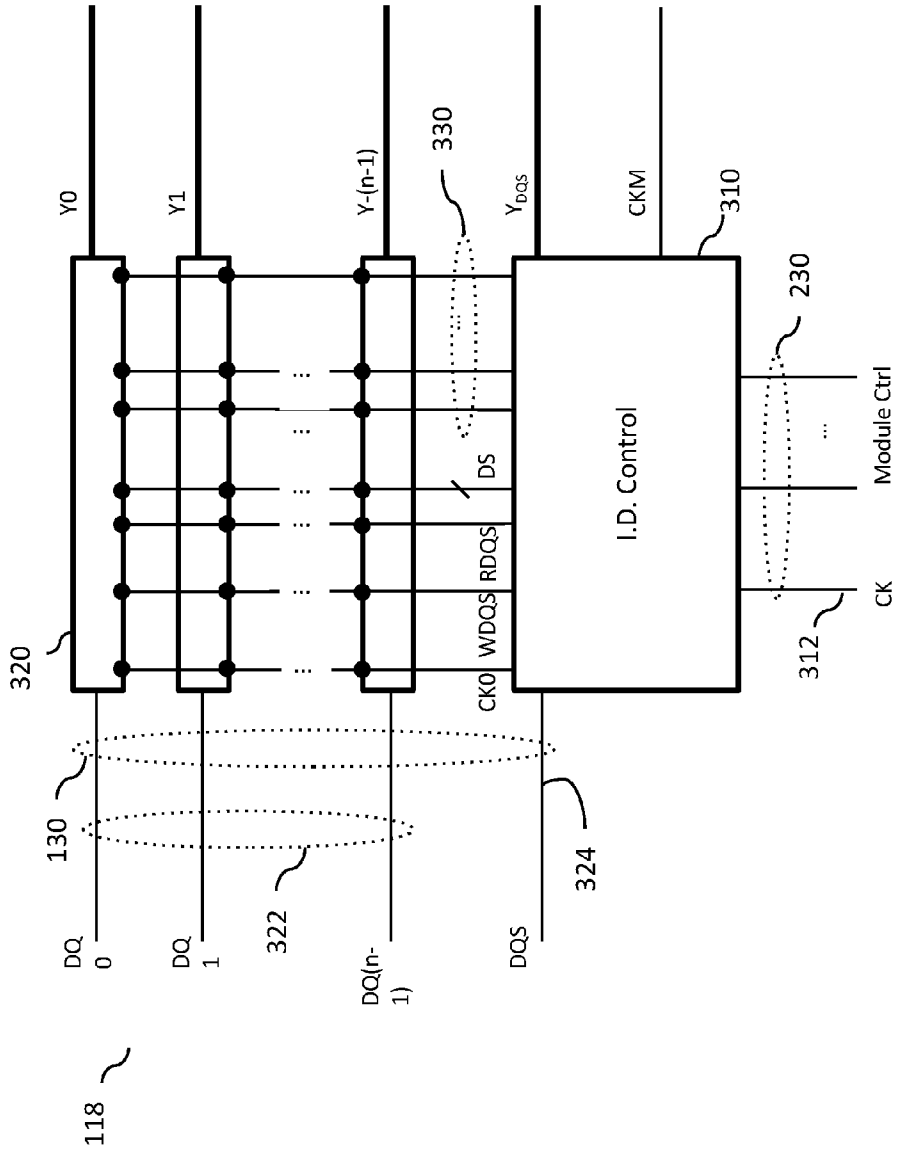

118
DQ 0
DQ 1
DQ(n-1)
DQS
130
322
324
320
Y0
Y1
Y-(n-1)
Y_{DQS}
CKO
WDQS
RDQS
DS
330
I.D. Control
CKM
310
230
312
CK
Module Ctrl

FIG. 3

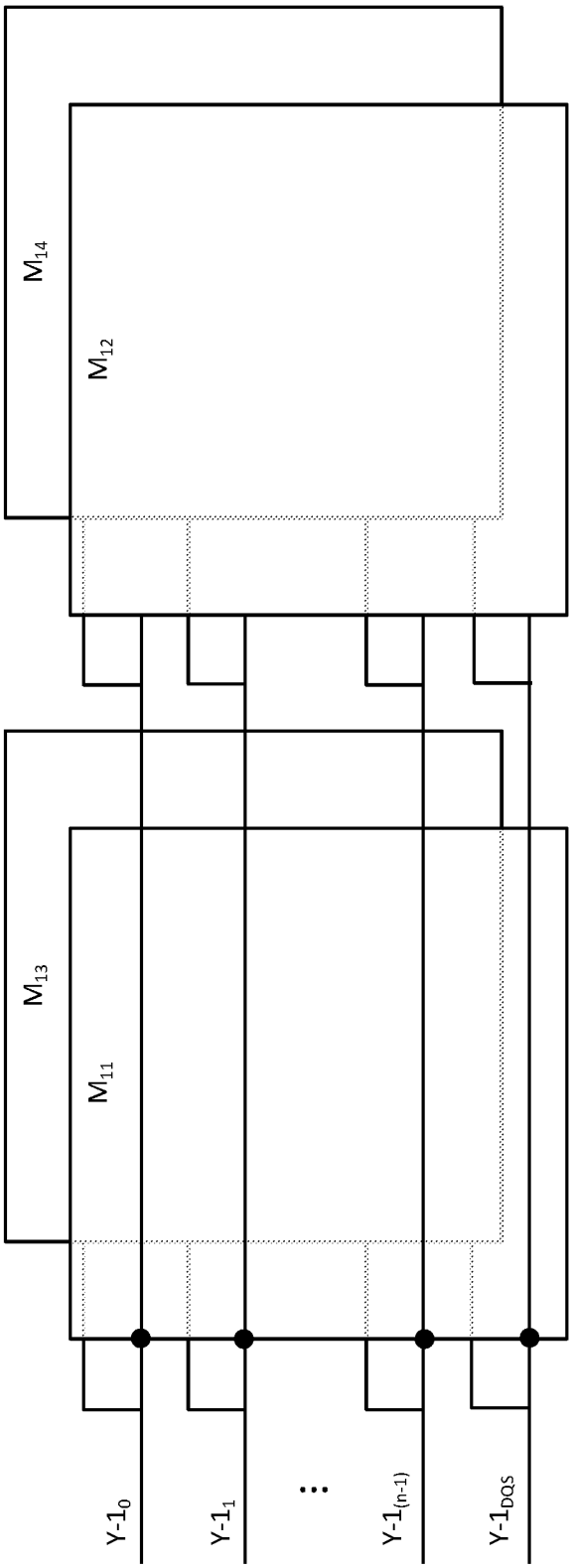


FIG. 4A

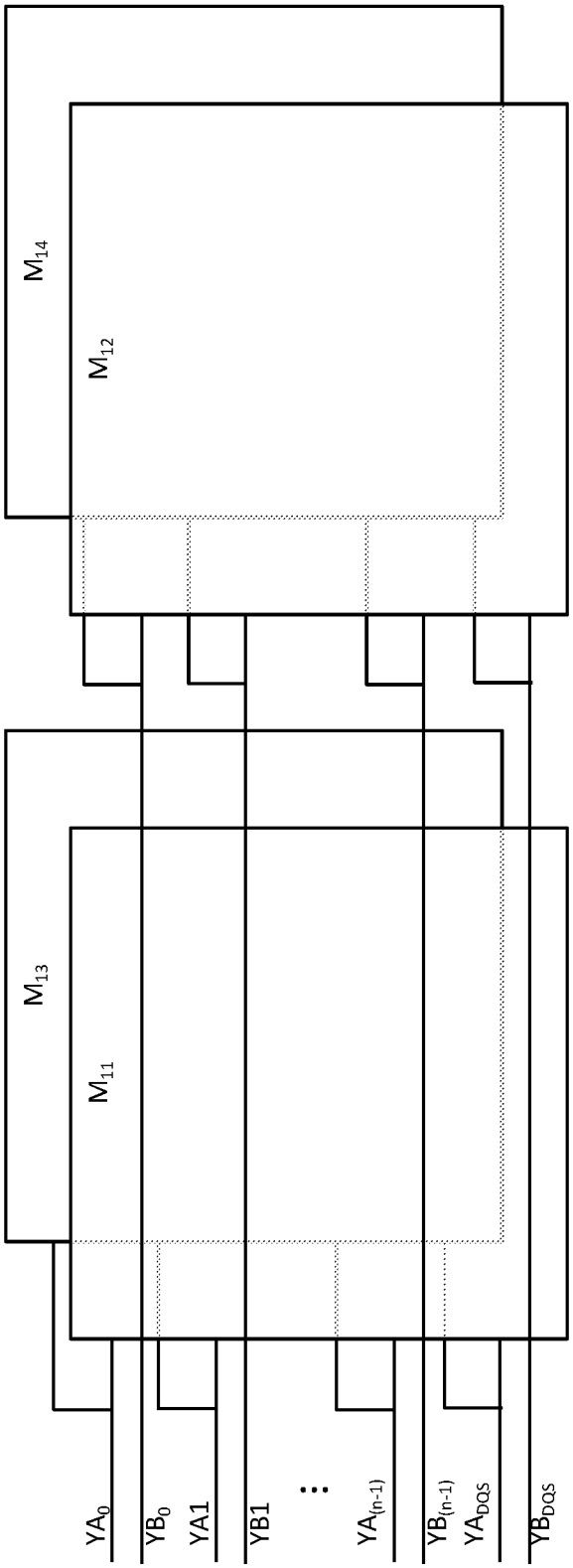


FIG. 4B

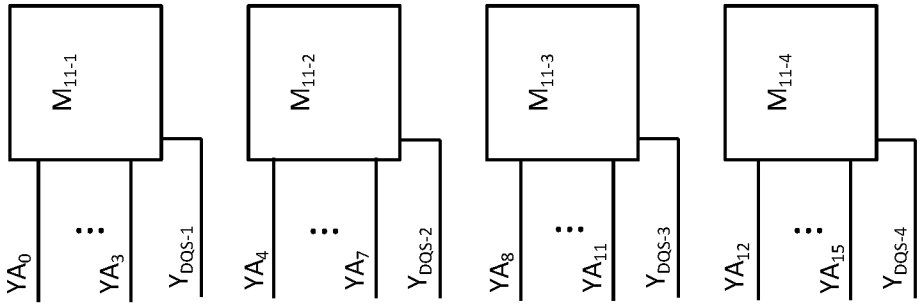

M_{11-1}
YA_0
YA_3
Y_{DQS-1}
M_{11-2}
YA_4
YA_7
Y_{DQS-2}
M_{11-3}
YA_8
YA_{11}
Y_{DQS-3}
M_{11-4}
YA_{12}
YA_{15}
Y_{DQS-4}

FIG. 5B

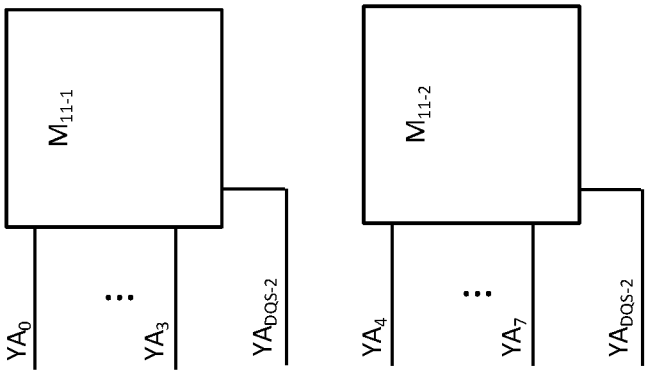

M_{11-1}
YA_0
YA_3
YA_{DQS-2}
M_{11-2}
YA_4
YA_7
YA_{DQS-2}

FIG. 5A

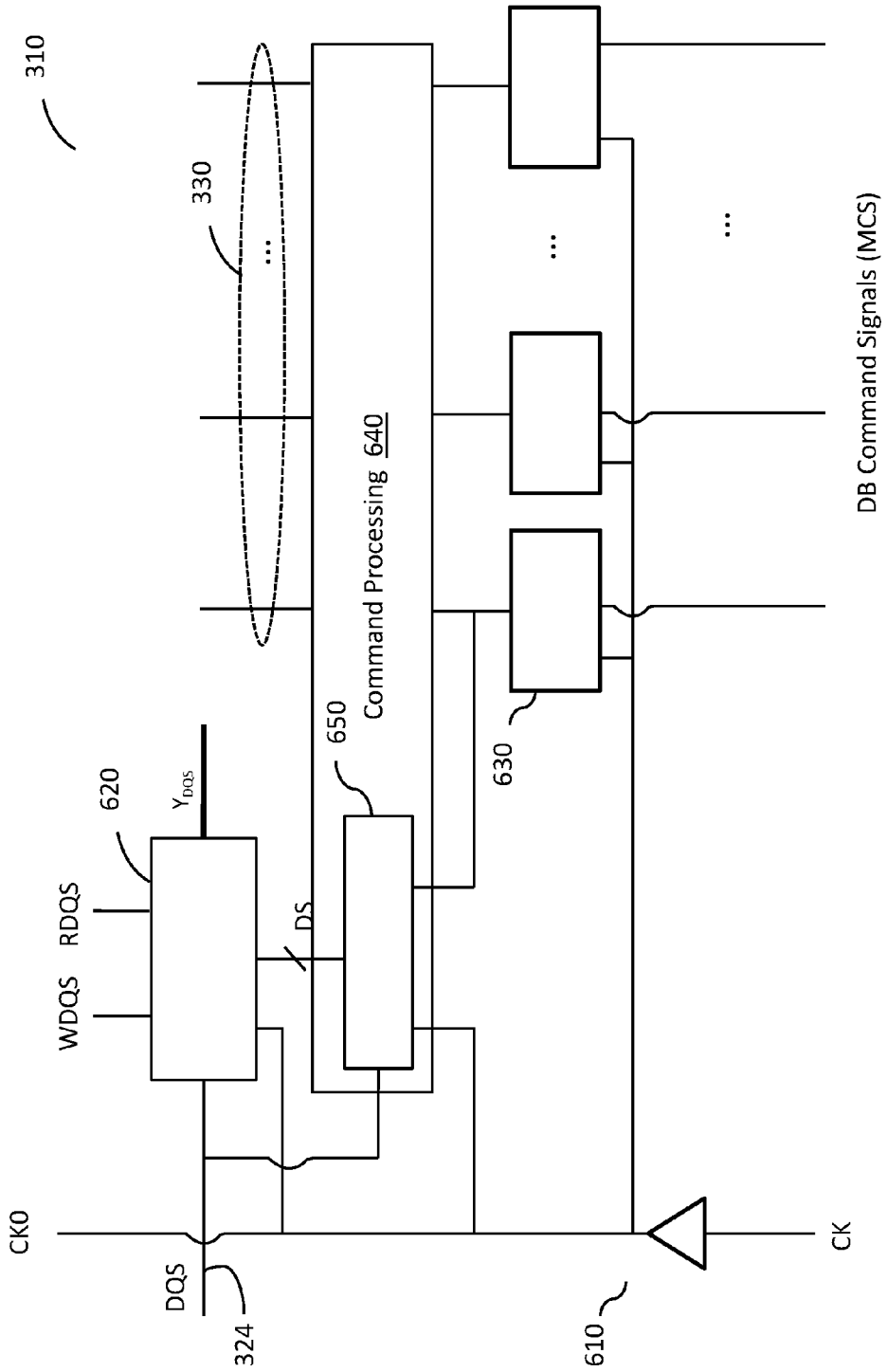

310
330
620
Y_{DQS}
RDQS
WDQS
DS
650
Command Processing 640
630
CK0
DQS
324
610
CK
DB Command Signals (MCS)

FIG. 6

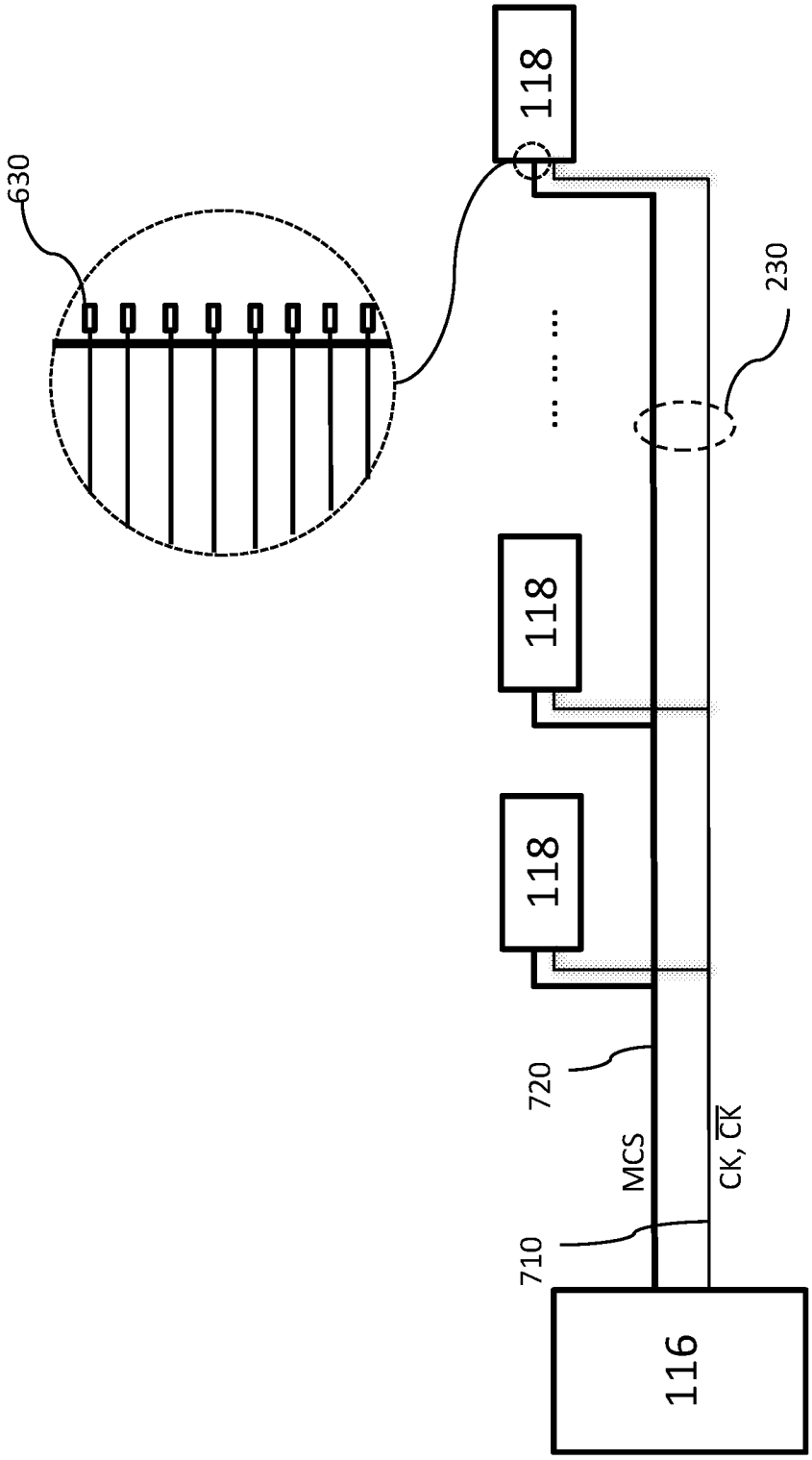


FIG. 7

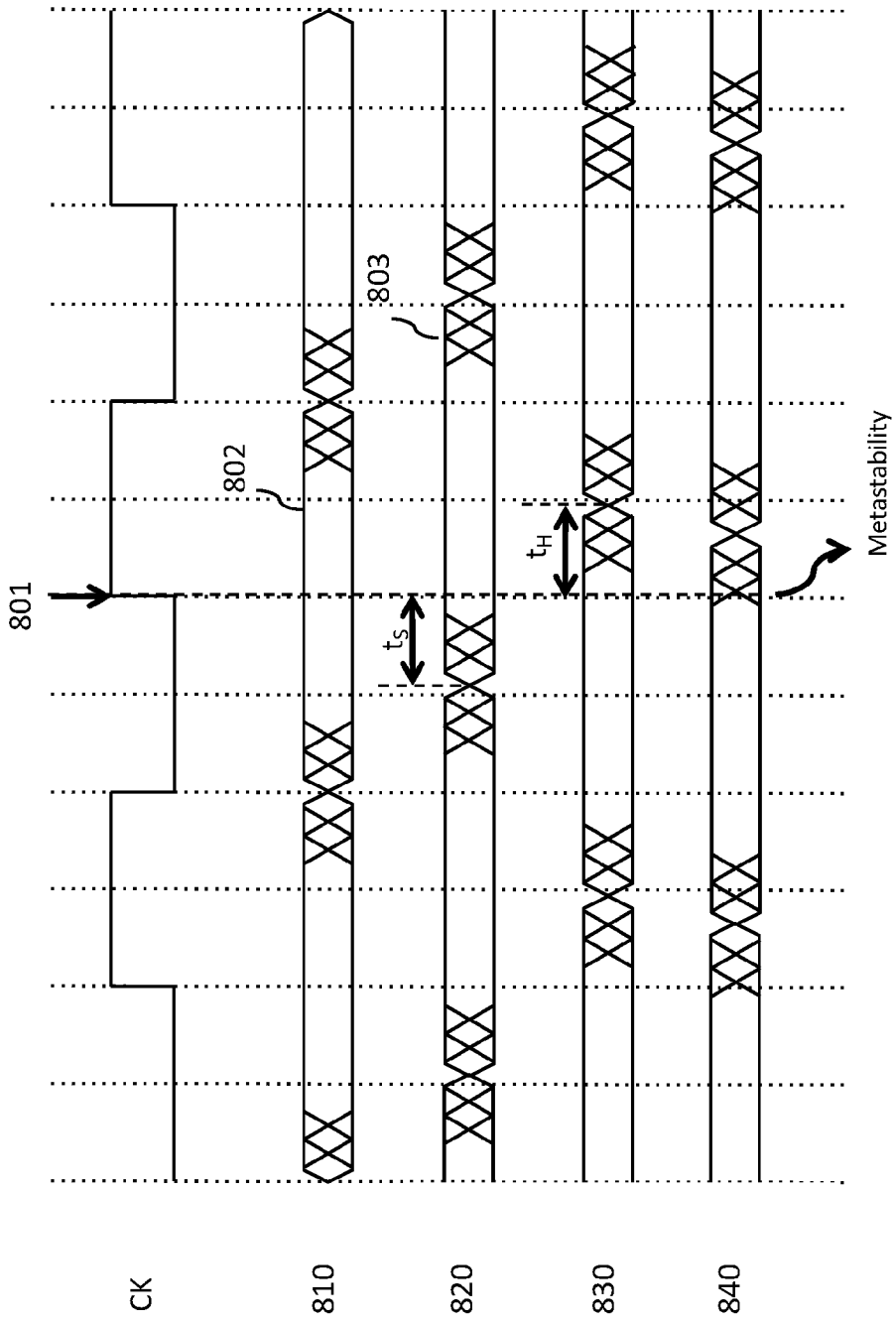


FIG. 8

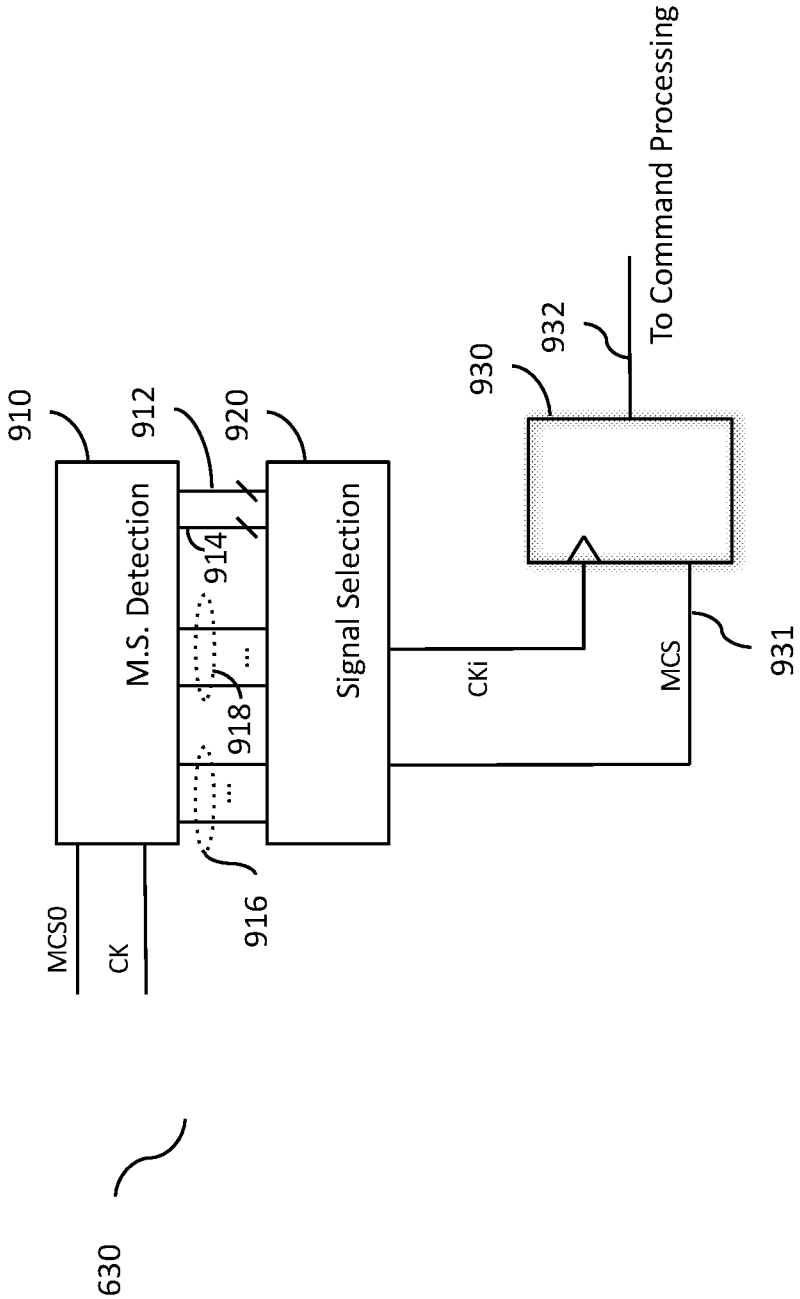

910
912
920
930
932
To Command Processing
M.S. Detection
914
918
916
Signal Selection
CKi
MCS
931
MCS0
CK
630

FIG. 9

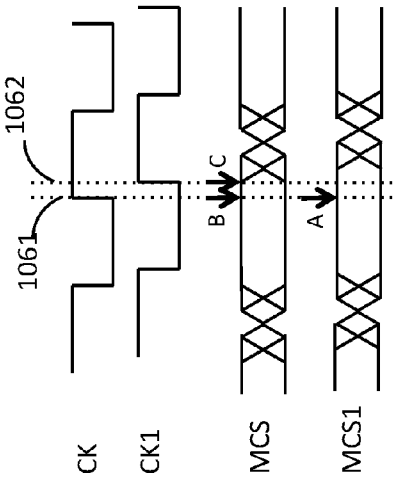


FIG. 10B

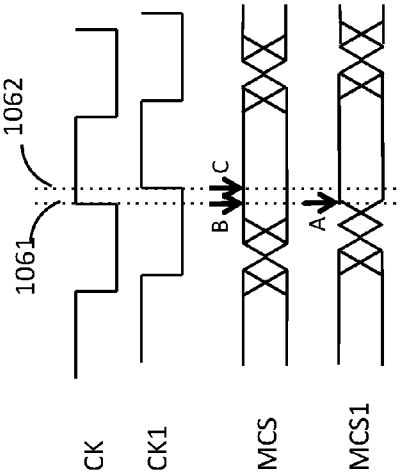


FIG. 10C

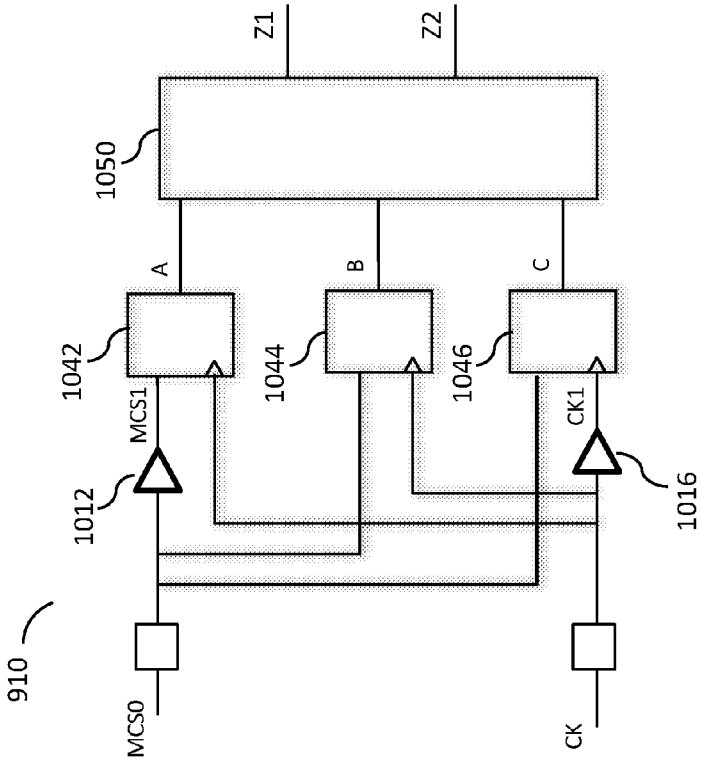


FIG. 10A

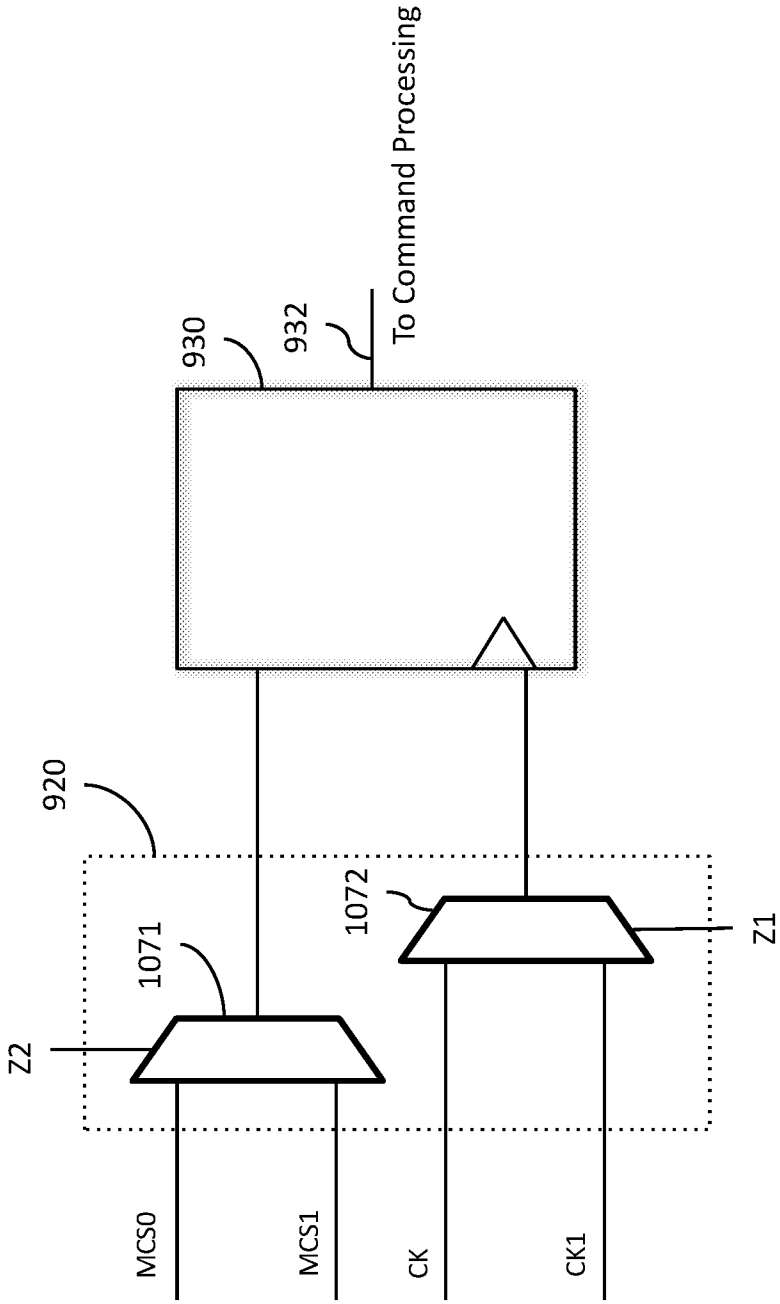

920
930
932
To Command Processing
1071
1072
Z2
Z1
MCS0
MCS1
CK
CK1

FIG. 10D

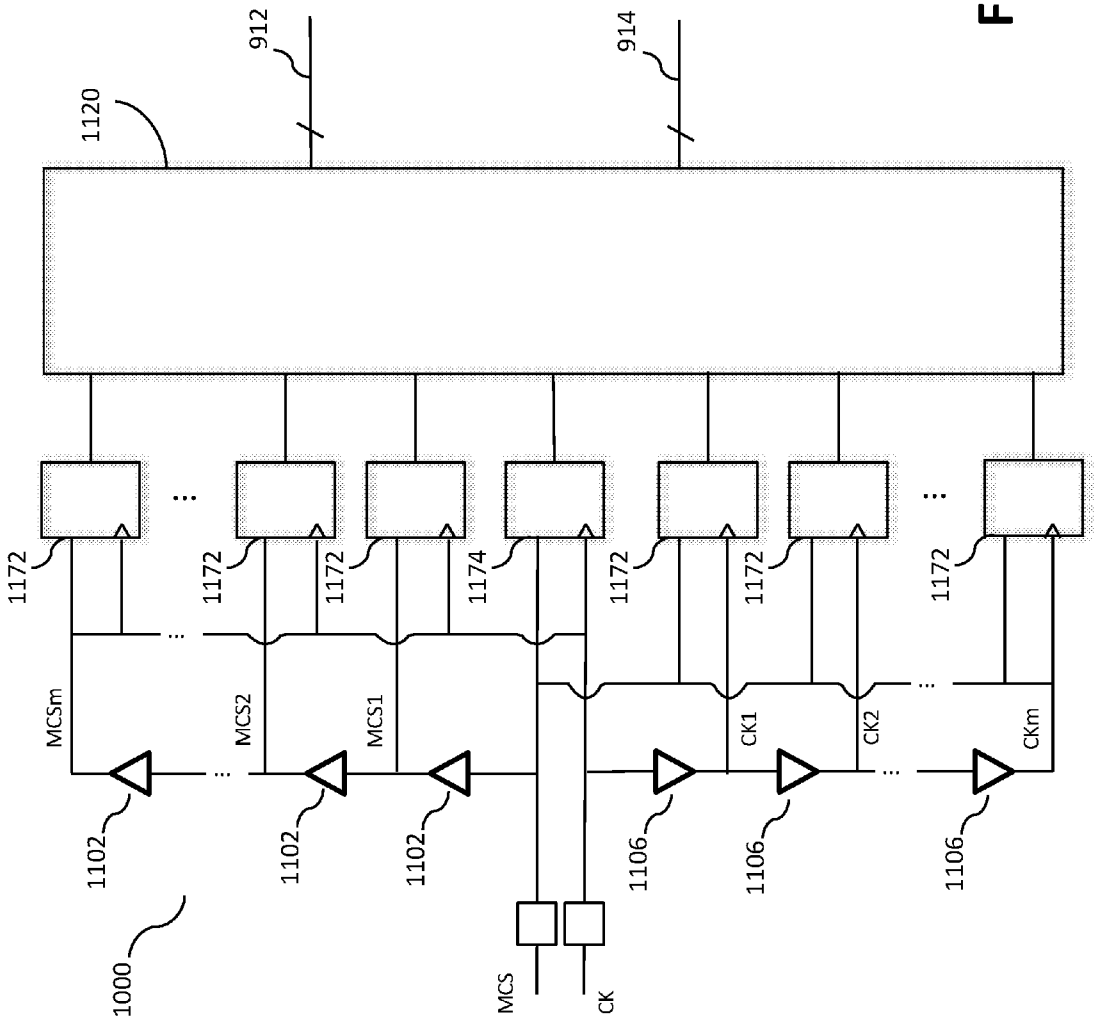

1000
1120
912
914
1172
1174
1102
1106
MCSm
MCS2
MCS1
CK1
CK2
CKm
MCS
CK

FIG. 11A

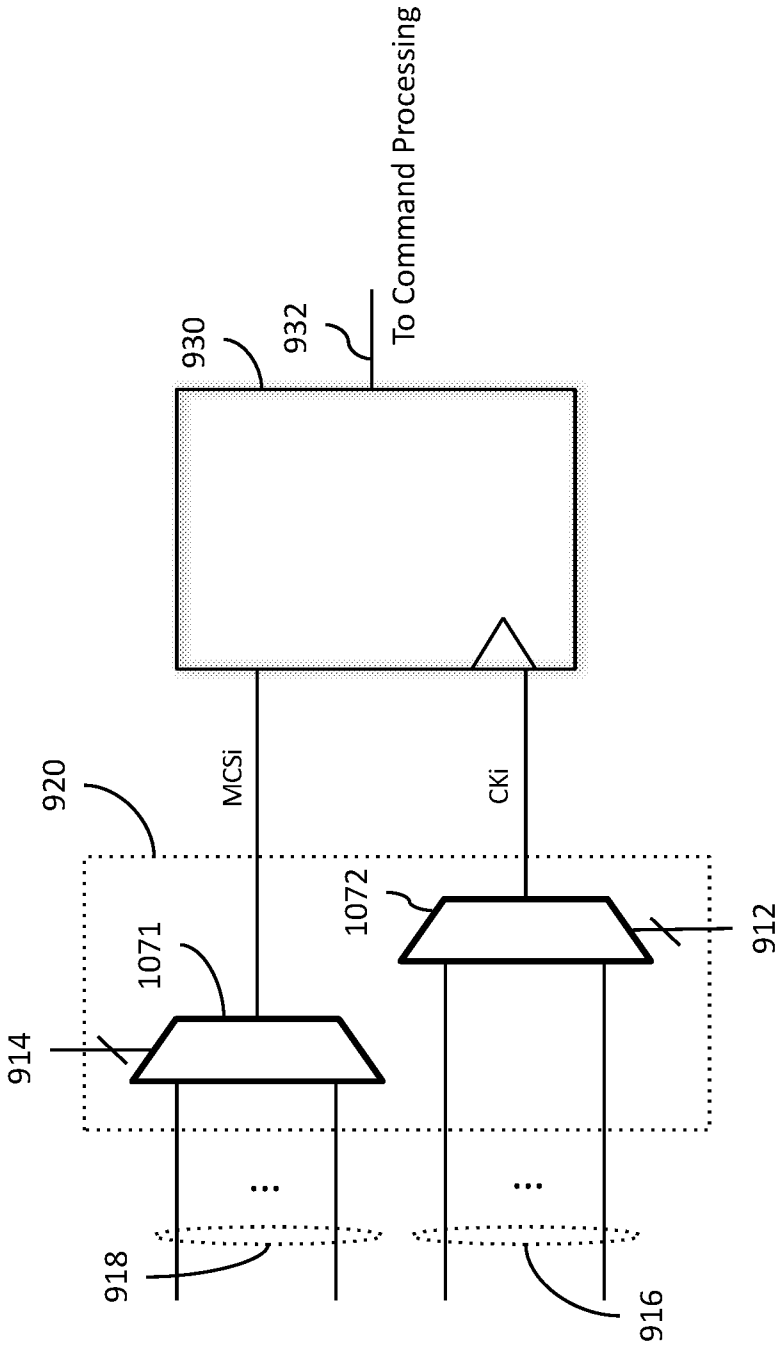

To Command Processing
930
932
920
MCSi
CKi
1071
1072
914
912
918
916

FIG. 11B

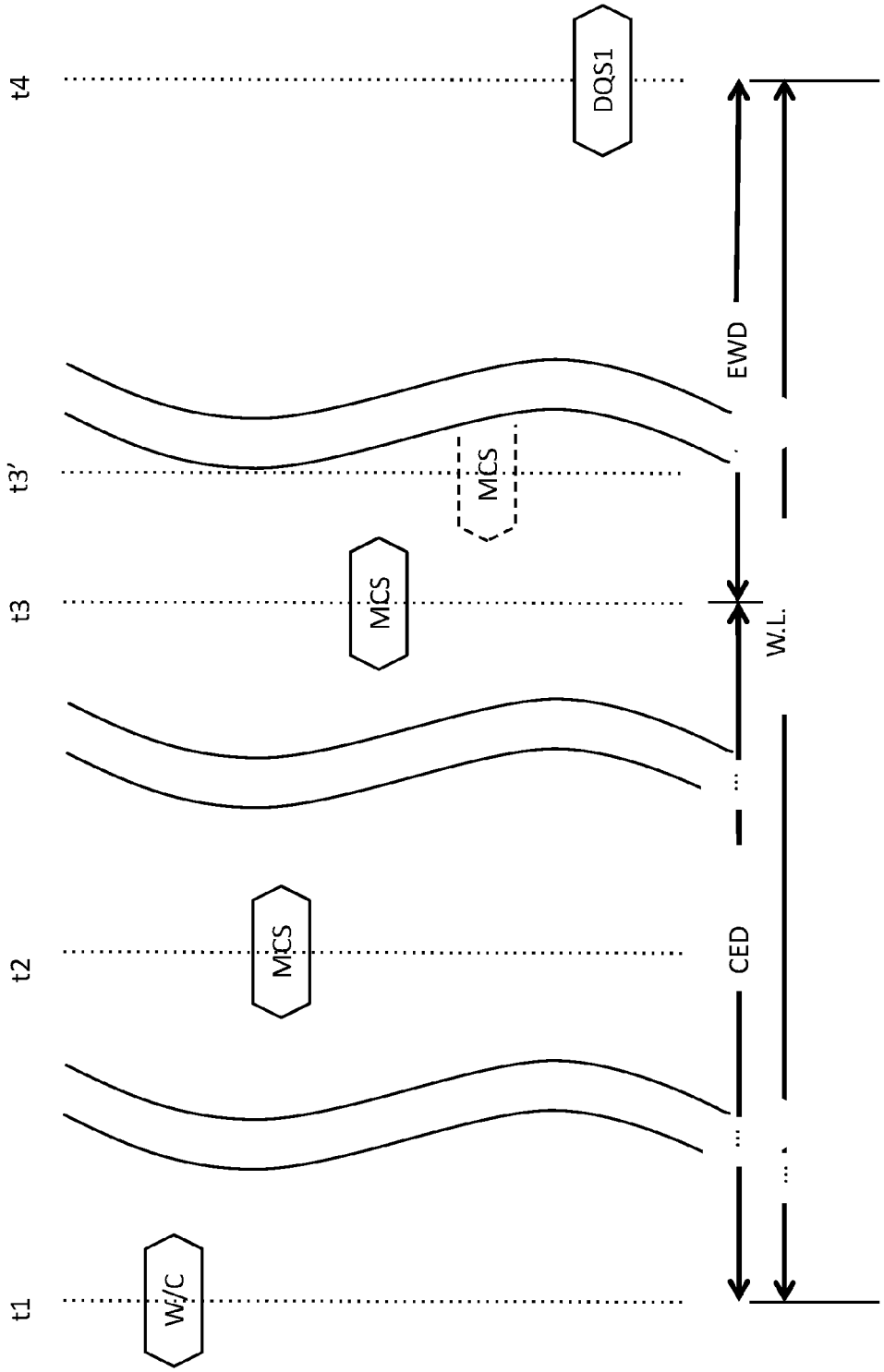


FIG. 12A

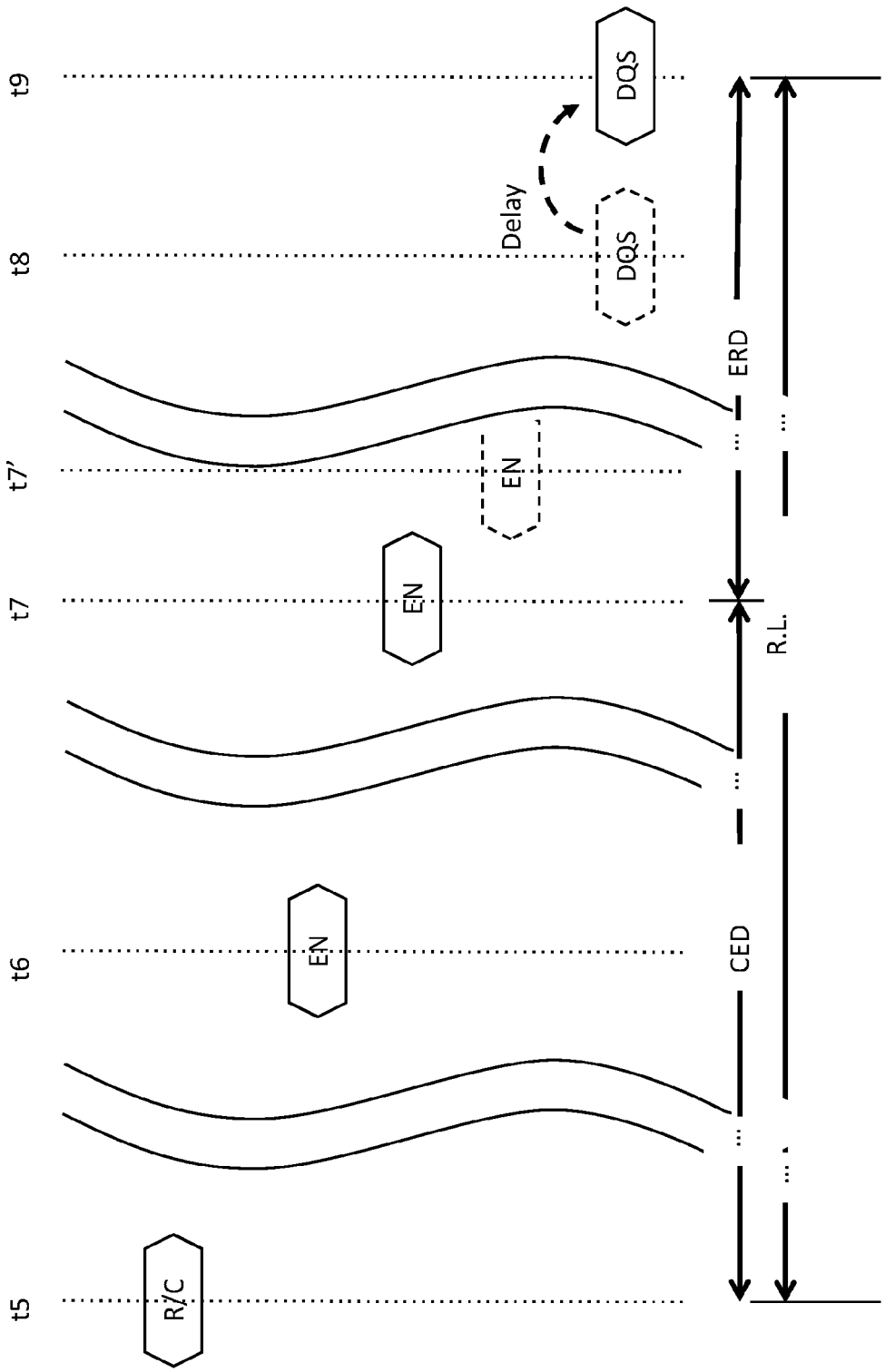


FIG. 12B

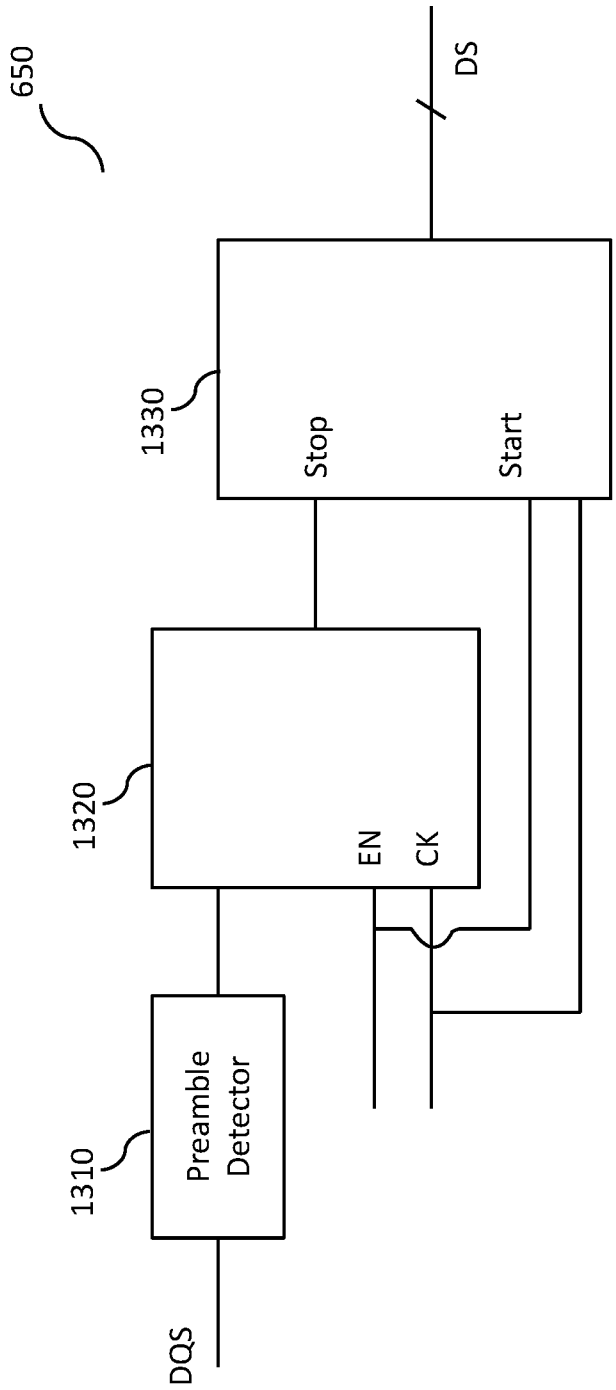


FIG. 13

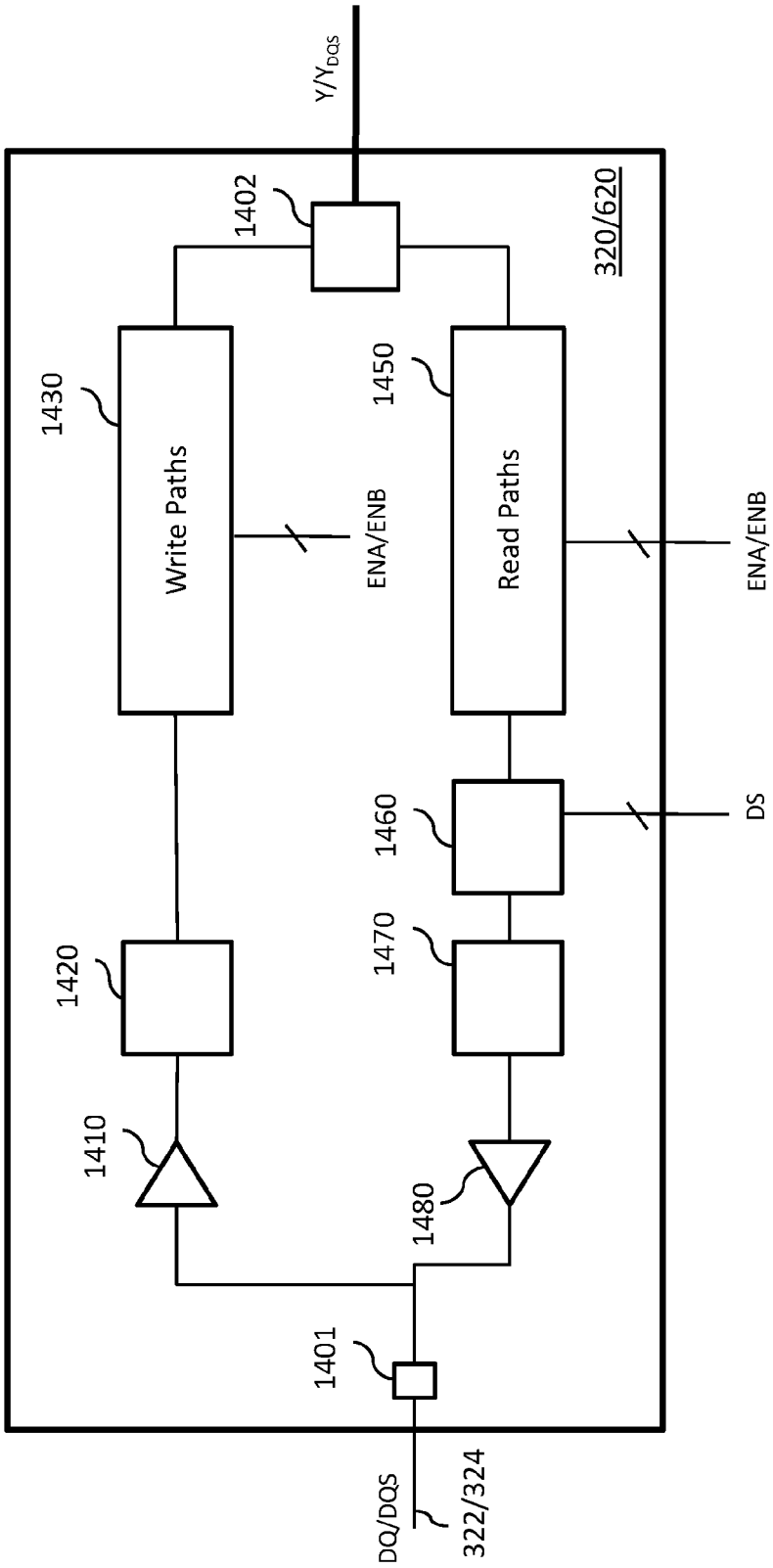

Y/Y_DQS
1402
320/620
1430
Write Paths
ENA/ENB
1450
Read Paths
ENA/ENB
1420
1460
DS
1410
1470
1480
1401
DQ/DQS
322/324

FIG. 14

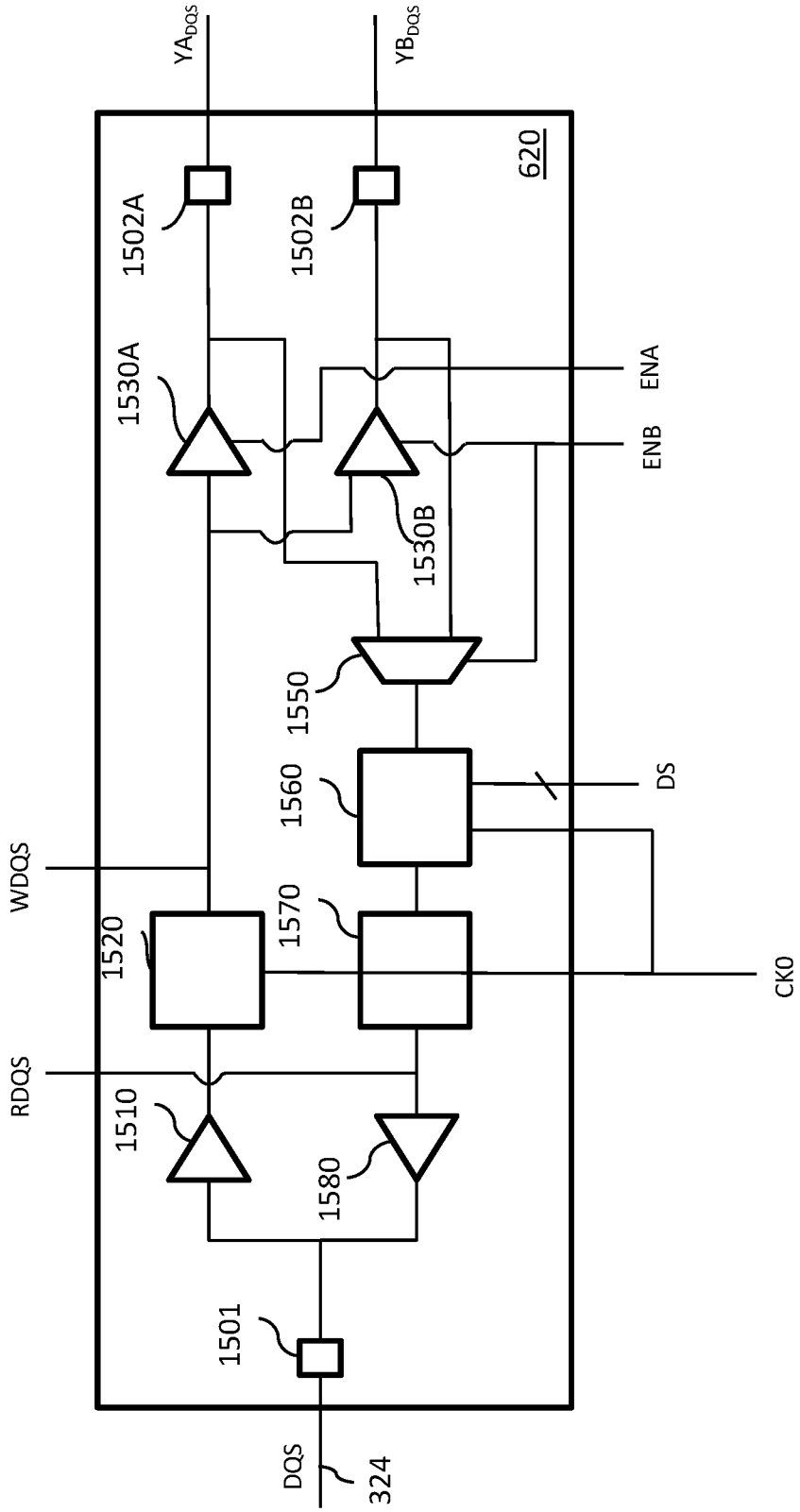

YA_DQS
YB_DQS
620
1502A
1502B
1530A
1530B
ENA
ENB
1550
1560
DS
WDQS
1520
1570
CK0
RDQS
1510
1580
1501
DQS
324

FIG. 15

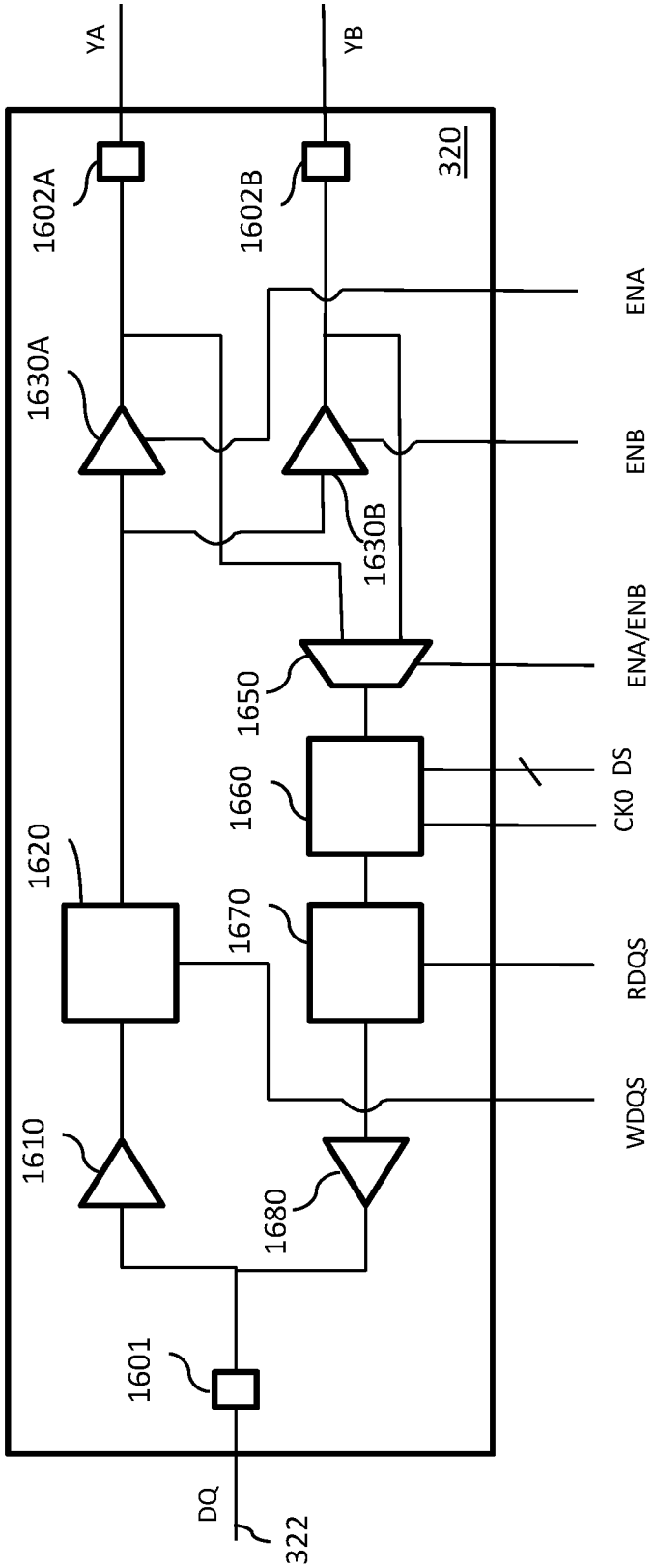

YA
YB
1602A
1602B
320
1630A
1630B
ENA
ENB
ENA/ENB
1650
1660
CK0 DS
1620
1670
RDQS
WDQS
1610
1680
1601
DQ
322

FIG. 16

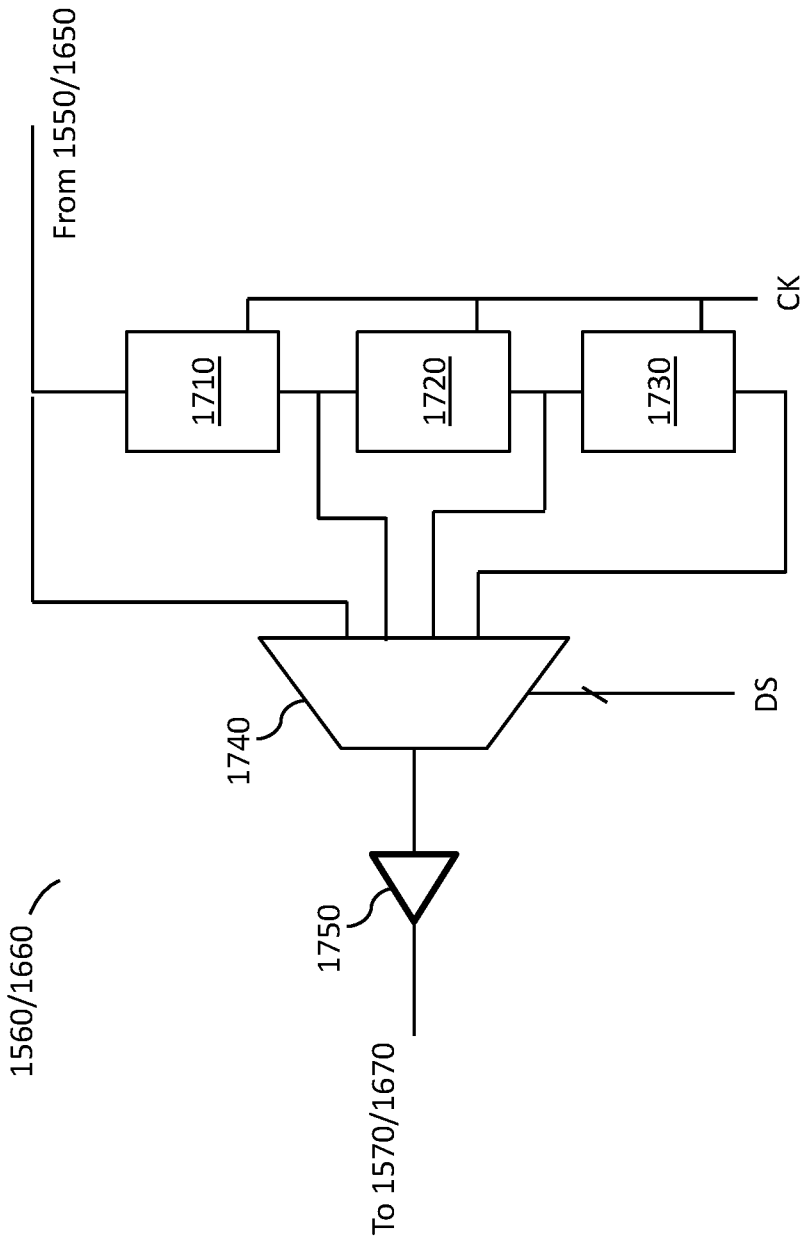

1560/1660
From 1550/1650
1710
1720
1730
CK
1740
DS
1750
To 1570/1670

FIG. 17

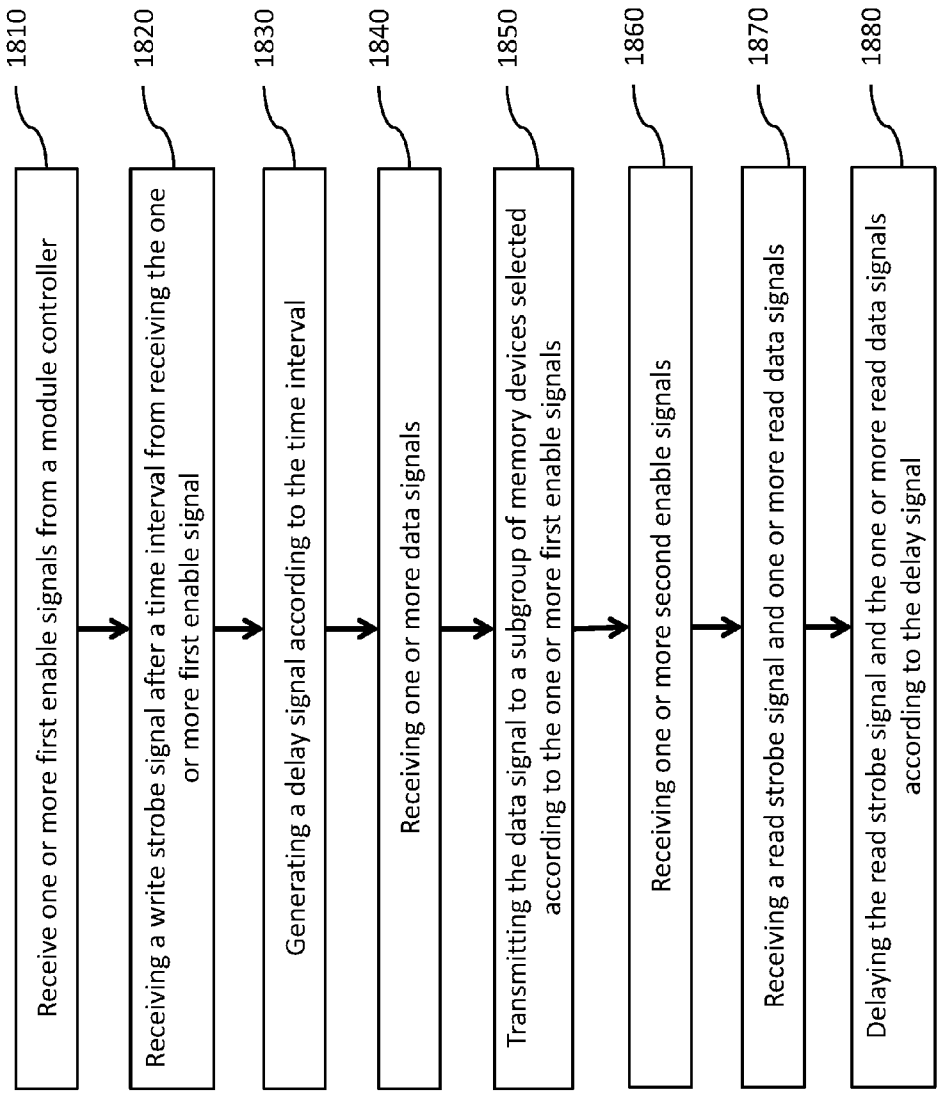

1810
Receive one or more first enable signals from a module controller
1820
Receiving a write strobe signal after a time interval from receiving the one or more first enable signal
1830
Generating a delay signal according to the time interval
1840
Receiving one or more data signals
1850
Transmitting the data signal to a subgroup of memory devices selected according to the one or more first enable signals
1860
Receiving one or more second enable signals
1870
Receiving a read strobe signal and one or more read data signals
1880
Delaying the read strobe signal and the one or more read data signals according to the delay signal

FIG. 18

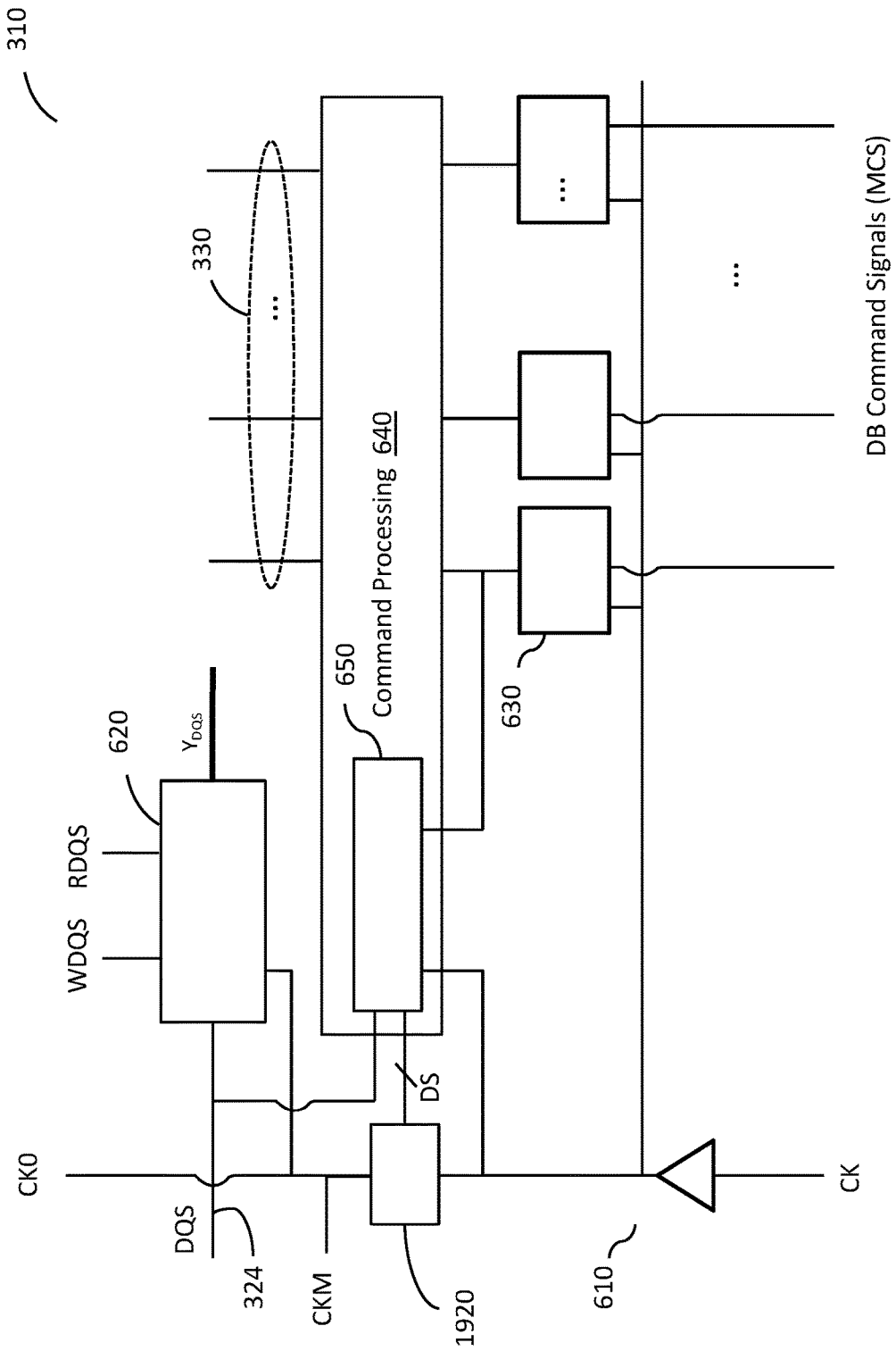

310
330
620
Y_{DQS}
RDQS
WDQS
650
Command Processing 640
630
DB Command Signals (MCS)
CK0
DQS
324
CKM
DS
1920
610
CK

FIG. 19

MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS

CLAIM OF PRIORITY

The present application is a continuation of U.S. patent application Ser. No. 14/846,993, to be issued as U.S. Pat. No. 9,563,587, which is a continuation of U.S. patent application Ser. No. 13/952,599, filed Jul. 27, 2013, issued as U.S. Pat. No. 9,128,632, which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on Jul. 27, 2012. Each of the above applications is incorporated by reference herein in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to commonly-owned U.S. patent application Ser. No. 14/715,486, filed on May 18, 2015; U.S. patent application Ser. No. 13/970,606, filed on Aug. 20, 2013; U.S. patent application Ser. No. 12/504,131, filed on Jul. 16, 2009, now U.S. Pat. No. 8,417,870; U.S. patent application Ser. No. 12/761,179, filed on Apr. 15, 2010, now U.S. Pat. No. 8,516,185; U.S. patent application Ser. No. 13/287,042, filed on Nov. 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. patent application Ser. No. 13/287,081, filed on Nov. 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

FIELD

The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

BACKGROUND

With recent advancement of information technology and widespread use of the Internet to store and process information, more and more demands are placed on the acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a

memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

For memory devices in such as a memory module to be properly accessed, distribution of control signals and a control clock signal in the memory module is subject to strict constraints. In some conventional memory modules, control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram illustrating a memory system including at least one memory module according to one embodiment.

FIGS. **2**A-**2**D are each a diagrams illustrating interactions among components in a a memory module according to certain embodiments.

FIG. **3** is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

FIGS. **4**A-**4**B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

FIGS. **5**A-**5**B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

FIG. **6** is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

FIG. **7** is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

FIG. **8** is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

FIG. **9** is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

FIGS. **10**A-**10**C are diagrams illustrating a metastability detection circuit according to certain embodiments.

FIG. **10**D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

FIGS. **11**A-**11**B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

FIGS. **12**A-**12**B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

FIG. **13** is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

FIG. **14** is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

FIG. **15** a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

FIG. **16** a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

FIG. **17** is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.

FIG. **18** is a flowchart illustrating a method for data edge alignment according to embodiments.

FIG. **19** is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

DESCRIPTION OF EMBODIMENTS

A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

FIG. **1** shows a system **100** including a memory controller (MCH) **101** and one or more memory modules **110** coupled to the MCH by a memory bus **105**, according to one embodiment. As shown, the memory bus includes C/A signal lines **120** and groups of system data/strobe signal lines **130**. Also as shown, each memory module **110** has a plurality of memory devices **112** organized in a plurality of ranks **114**. Each memory module **110** further includes a module control circuit (module controller or module control device) **116** coupled to the MCH **101** via the C/A signal lines **120**, and a plurality of buffer circuits or isolation devices **118** coupled to the MCH **101** via respective groups of system data/strobe signal lines **130**. In one embodiment, the memory devices **112**, the module control circuit **116** and the isolation devices **118** can be mounted on a same side or different sides of a printed circuit board (module board) **119**.

In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module **110** may vary. For example, as shown, each memory module **110** may include four ranks of memory devices **112**. In another embodiment, the memory module **110** may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices **112**.

In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices **112**. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus **105** may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

Furthermore, the memory devices **112** may include any type of memory devices. For example, in one embodiment, the memory devices **112** may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module **110** may include a dual in-line memory module (DIMM).

Referring to FIG. **2**A, which illustrates one memory module **110** according to an embodiment, the module control device **116** receives system memory commands represented by a set of system control/address (C/A) signals from the MCH **101** via signal lines **120** and generates module

command signals and module control signals based on memory commands from the system. The module control device **116** also received a system clock MCK and generates a module clock signal CK in response to the system clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{MCK}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{CK}$.

Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices **118**; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices **118** via respective module control signal lines **230**. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices **118** via the module control signal lines and decoded/processed at the isolation devices.

Module control device **116** transmits the module command signals to the memory devices **112** via module C/A signal lines **220**. The memory devices **112** operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices **118** via module control signal lines **230**. As shown in FIG. **2**, at least some of the memory devices in a same rank share a same set of module C/A signal lines **220**, and at least some of the isolation devices **118** share a same set of module control signal lines **230**.

As shown n FIGS. **2**A and **2**B, each rank **114** includes N memory devices, where N is an integer larger than one. For example, a first rank includes memory devices $M_{11}, \ldots, M_{i1}, M_{i+1,1}, \ldots, M_N$, a second rank includes memory devices $M_{12}, \ldots, M_{i2}, \ldots, M_{i+1,2}, \ldots, M_{N,2}$, and so on. In one embodiment, the memory devices **112** are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines **130** and including at least one memory device from each rank. For example, memory devices M_{11}, M_{12}, M_{13}, and M_{14} form a first group of memory devices, memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} form an ith group of memory devices, and so on.

As shown, the isolation devices **118** are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines **130** and the respective groups of memory devices. For example, isolation device ID-**1** among the isolation devices **118** is associated with the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14} and is coupled between the group of system data/strobe signal lines **130-1** and the first group of memory devices, isolation devices ID-i among the isolation devices **118** is associated with the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} and is coupled between the group of system data/strobe signal lines **130**-i and the ith group of memory devices, and so on.

In one embodiment, each group or sets of memory devices are coupled to the associated isolation device **118** via a set of module data/strobe lines **210**. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device **118** via a same set of module data/strobe lines **210** (as shown in FIG. **2**A) or via respective subsets of module data/strobe lines **210** (as shown in FIG. **2**B). For example, as shown in FIG. **2**B, in the first group of memory devices, memory devices M_{11} and/or M_{13} form a first subgroup, and memory devices M_{12} and/or M_{14} form a second subgroup; in the ith group of memory devices, memory devices M_{i1} and/or M_{i3} form a first subgroup, and memory devices M_{i2} and/or M_{i4} form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device **118** via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices M_{11} and/or M_{13} form the first subgroup are/is coupled to the isolation device ID-**1** via the corresponding first subset of module data/strobe lines YA-**1**, and memory devices M_{12} and/or M_{14} form the second subgroup are/is coupled to the isolation device ID-**1** via the corresponding second subset of module data/strobe lines YA-**2**.

In one embodiment, the isolation devices **118** are in the data paths between the MCH **101** and the memory module **110** and include data buffers between the MCH **101** and the respective groups of memory devices. In one embodiment, each isolation device **118** is configured to select a subgroup in the respective group of memory devices to communicate data with the MCH **101** in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH **101**. Further, each isolation devices **118** is configured to isolate unselected subgroup(s) of memory devices from the MCH **101** during write operations, so that the MCH sees a load on each data

line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

In one embodiment, the isolation devices **118** are distributed across the memory module **110** or the module board **119** in positions corresponding to the respective groups of memory devices. For example, isolation device ID-**1** is disposed in a first position corresponding to the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and isolation device ID-i is disposed in an ith position separate from the first position and corresponding to the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4}. In one embodiment, the first position is between the first group of memory devices and an edge **201** of the module board **119** where connections (not shown) to the data/strobe signal lines **130** are placed, and i^{th} position is between the ith group of memory devices and the edge **201** of the module board **119**. In one embodiment, the isolation devices **118** are distributed along the edge **201** of the memory module **110**. In one embodiment, each isolation device **118** is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines **210**, the module C/A signal lines **220**, and the module control signal lines **230** include signal traces formed on and/or in the module board **119**.

As an option, memory module **110** may further include a serial-presence detect (SPD) device **240**, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module **110**. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory module **110**, a memory density per rank, a number of memory device on the memory module **110**, and a memory density per memory device, etc. A basic input/output system (BIOS) of system **100** can be informed of these attributes of the memory module **110** by reading from the SPD **240** and can use such data to configure the MCH **101** properly for maximum reliability and performance.

In certain embodiments, the SPD **240** and/or the control circuit **116** store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit **116**, input and output signals electrical and logical level control information for the control circuit **116**, etc. In certain embodiments, the SPD **240** contains a system view of the module **110** which can be different from an actual physical construction of the module **110**. For example, the SPD **240** stores at least one memory operation parameter that is different from a corresponding memory operation parameter in a system memory controller setting. The SPD **240** may also store at least on data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

Thus, in certain embodiment, in the memory module **110**, C/A signals representing a memory command are received and buffered by the module control circuit **116**, so that the MCH sees only the module control circuit **116** as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices **118** before being transmitted to the memory devices **112** by the isolation devices **118**. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines **130**. Thus, MCH **101** does not directly operate or control the memory devices **112**. As far as data/strobe signals are concerned, the MCH **101** mainly sees the isolation devices **118**, and the system **100** depends on the isolation devices **118** to properly time the transmission of the read data and strobe signals to the MCH **101**.

In certain embodiments, the memory module **110** is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM). In certain embodiments, the control circuit **116** includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.

As shown in FIG. **2**C, in certain embodiments, the control circuit **116** transmits registered C/A and clock signals to the memory devices **112**, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices **118**, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

For example, load reduction mechanism in the isolation devices **118** would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller **101**. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller **101** over the interface between the memory devices **112** and the associated isolation devices **118**. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller **101**, which may cause silent system failure.

Moreover, clock skew amongst the memory devices **112** and the associated isolation devices **118** due to the distributed architecture of the memory module **110** can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

To address at least some of the above issues, in certain embodiments, as shown in FIG. **2**D, the control circuit **116** transmits registered C/A signals to the memory devices **112**, and transmits the module control signals and the module clock signal to the data buffers **118**, in a fly-by arrangement. The memory devices **112** do not receive the module clock signal from the control circuit **116**. Instead, each data buffer **118** regenerates the clock that is used by the respective set of memory devices **112**. Each Data buffer **118** is thus responsible for providing a correct data timing interface between the respective set of memory devices **112** and the system memory controller **101**. Each data buffer **118** is also responsible for providing the correct control signal timing between the control circuit **116** and the respective set of memory devices **112**.

Thus, the memory module **110** in FIG. **2**D allows a locally synchronized operation for each respective set of memory

devices **112**, which can correspond to a nibble or a byte of a DDR data bus between the memory module **110** and the system memory controller **101**. Also, signal interface between each data buffer **118** and the respective set of memory devices **112** can be synchronized. In one embodiment, each data buffer **118** has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices **112**, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller **101**, programmable phase adjustment related to at least one control signal that is coupled to the control circuit **116**. The locally synchronized operation also makes it easier for each data buffer **118** to perform self-testing of the associated set of memory devices **112**, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Pat. No. 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

In certain embodiments, operations of the isolation devices **118** are controlled by the module control signals from the module control circuit **116**, which generates the module control signals according to the C/A signals received from the MCH. Thus, the module control signals need to be properly received by the isolation devices **118** to insure their proper operation. In one embodiment, the module control signals are transmitted together with the module clock signal CK, which is also generated by the module control circuit **116** based on the system clock signal MCK. The isolation circuits **118** buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices **118** are distributed across the memory module, the module control signal lines **230** can stretch across the memory module **110**, over a distance of several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits **118** includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

Because the isolation devices **118** are distributed across the memory module **110**, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines **230** from the module control device **116** to the farthest positioned isolation devices **118**, such as isolation device ID-**1** and isolation device ID-(n-1) in the exemplary configuration shown in FIG. **2**. In other words, a same set of module control signals may reach different isolation devices **118** at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70 ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

With the isolation devices **118** receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to time the transmission of read data signals to the MCH **101** from the isolation devices **118**. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit **116** and a time when a write strobe or write data signal is received from the MCH **101**. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH **101**, such that the read data follows a read command by a read latency value associated with the system **100**, as explained in more detail below.

More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

In one embodiment, as shown in FIG. **3**, each group of signal lines **130** include a set of n data (DQ) signal lines **322** each for transmitting one of a set of data signals DQ_0, DQ_1, . . . , DQ_{n-1}, and at least one strobe (DQS) signal line **324** for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of n module data signal lines Y_0, Y_1, . . . , Y_{n-1} and at least one module strobe signal line Y_{DQS}. When the subsets of memory devices are coupled to the associated isolation device **118** via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. **2**B. Each subset of module data/strobe lines YA include a set of n first module data lines YA_0, YA_1, . . . , YA_n and at least one first module strobe signal line YA_{DQS}; and each subset of module data/strobe lines YB include a set of n second module data lines YB_0, YB_1, . . . , YB_n and at least one second module strobe signal line YB_{DQS}.

Each isolation device **118** includes a set of DQ routing circuits **320** coupled on one side to respective ones of the set of n DQ signal lines **322**, and on another side to respective ones of the respective set of n module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines YA_0, YA_1, . . . , YA_n and the second module data lines YB_0, YB_1, . . . , YB_n. Each isolation device **118** further includes an ID control circuit **310** coupled on one side to the at least one DQS signal line **324**, on another side to the one or more module strobe signal lines Y_{DQS}, or the first module strobe signal line YA_{DQS} and second module strobe signal line YB_{DQS}. The ID control circuit **310** also receives the module clock signal CK and the module control signals via the module control signal lines **230**, and outputs ID control signals **330** to the DQ routing circuits **320**, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module control signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK**0**. Each DQ routing circuit **320** is configured to enable data

communication between the respective DQ signal line **322** with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

In certain embodiments, the ID control circuit **310** also provides a delay signal DS, which is used by the DQ routing circuits **320** to align read data output by the isolation device **118** with read data output by the other isolation devices **118**, as explained in further detail below. In certain embodiments, the ID control circuit **310** regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK**0** and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

The memory devices **112** are coupled to the isolation devices **118** via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. **4**A, memory devices M_{11}, M_{12}, M_{13}, and M_{14} in the first group of memory devices can be coupled to the isolation device ID-**1** via a same set of module data lines Y-$\mathbf{1}_0$, Y-$\mathbf{1}_1$, . . . , Y-$\mathbf{1}_{n-1}$ and module strobe line Y-$\mathbf{1}_{DQS}$. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which can be different with respect to different subgroups of memory devices.

Alternatively, as shown in FIG. **4**B, memory devices M_{11} and M_{13}, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-**1** via the module data lines YA-$\mathbf{1}_0$, YA-$\mathbf{1}_1$, . . . , YA-$\mathbf{1}_n$ and module strobe line YA-$\mathbf{1}_{DQS}$ and memory devices M_{12} and M_{14}, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-**1** via the module data lines YB-$\mathbf{1}_0$, YB-$\mathbf{1}_1$, . . . , YB-$\mathbf{1}_n$ and module strobe line YB-$\mathbf{1}_{DQS}$. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board **119**. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards **119**, or stacked over each other, and/or over the associated isolation device.

Multiple memory devices having a data width that is less than a data width of the isolation devices **118** may be used in place of one of the memory devices **112**, which has the same data width as that of the isolation devices. For example, as shown in FIG. **5**A, two memory devices M_{11-1} and M_{11-2} may be used in place of the memory device M_{11}. Each of the two memory devices M_{11-1} and M_{11-2} has a data width of 4, and together they act like a memory device M_{11} of a data width of 8. Thus, memory device M_{11-1} is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_0$, . . . , YA-$\mathbf{1}_3$ and module strobe line YA-$\mathbf{1}_{DQS-1}$ while memory circuit M_{11-2} is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_4$, YA-$\mathbf{1}_7$ and module strobe line YA-$\mathbf{1}_{DQS-2}$.

In another embodiment, as shown in FIG. **5**B, four memory devices M_{11-1} to M_{11-4} may be used as the memory device M_{11}. Each of the four memory devices M_{11-1} to M_{11-4} has a data width of 4, and together they act like a memory device M_{11} of a data width of 16. Thus, memory device M_{11-1} is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_0$, . . . , YA-$\mathbf{1}_3$ and module strobe line YA-$\mathbf{1}_{DQS-1}$ while memory device M_{11-2} is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_4$, . . . , YA-$\mathbf{1}_7$ and module strobe line YA-$\mathbf{1}_{DQS-2}$, and so on.

FIG. **6** illustrates the ID control circuit **310** in an isolation device **118**. As shown, the ID control circuit **310** includes a clock buffer **610** to receive the module clock signal CK from the module control device **116**, and to output a module clock signal CK**0**. The ID control circuit **310** further includes a strobe routing circuit **620** that are coupled on one side to the corresponding system DQS signal line **324** and on another side to the corresponding module DQS signal lines YA_{DQS} and YB_{DQS}. The ID control circuit **310** further includes a receiver circuit **630** with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit **310** further includes a command processing circuit **640** that provides the received, decoded, and/or otherwise processed module control signals **330** to the DQ routing circuits **320** and the strobe routing circuit **620** either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits **320** and the strobe routing circuit **620** to selectively enabling data communication between the MCH **101** and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

The strobe routing circuit **620** also buffers strobe signals received from either the MCH **101** or the memory devices **112**, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits **320**. In one embodiment, the ID control circuit **310** further includes a delay control circuit **650** that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit **320** and the strobe routing circuit **620**. The delay amount is provided to the DQ routing circuit **320** and the strobe routing circuit in a delay signal DS.

In a receiver circuit **630**, the respective MCS is received in accordance with the module clock signal CK**0**. In one embodiment, receiver circuit **630** samples the respective MCS using rising (or falling) edges of the module clock CK**0**. Since the isolation devices **118** are distributed across the memory module **110** at positions corresponding to the respective groups of memory devices, the module control signal lines **230** that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as shown in FIG. **7**. As the MCS and CK**0** travel along their respective module control signal lines **710** and **720**, they can become misaligned with each other when they reach the input pins **730** of an isolation device **118**.

For example, a module control signal, like the MCS **810** shown in FIG. **8**, can be perfectly aligned with the module clock signal CK, with a rising edge **801** of the module clock signal CK being at a center of a data eye **802**, when the MCS signal and the clock signal leave the module control circuit **116**. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS **820** with respect to the CK signal, i.e., the rising edge **801** of the clock signal is near a left edge of a data eye of the MCS **820**, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS **830**, can be shifted with respect to the module clock signal such that a rising edge **801** of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS **840**, can be so shifted with respect to the module clock signal such that a rising edge **801** of the clock signal falls in the glitches **803** at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

In one embodiment, as shown in FIG. **9**, a receiver circuit **630** includes a metastability detection circuit (MDC) **910** to determine a metastability condition in a corresponding module control signal MCS**0**. In one embodiment, the MDC **910** generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS**0**. The MDC **910** also generates one or more metastability indicators and outputs the one or more metastability indicators via lines **912** and/or **914**.

The receiver circuit **630** further includes a signal selection circuit **920** that receives the module clock CK and the at least one delayed version of the module clock via signal lines **916**. The signal selection circuit **920** also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines **918**. The signal selection circuit **920** selects a clock signal CK from among the module clock CK and the at least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit **920** may also select an MCS signal MCS_i from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.

The receiver circuit **630** further includes a sampler or register circuit **930** that samples the selected module control signal MCS_i according to the selected clock signal CK_i and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit **640** for further processing (if needed) before being provided to the DQ routing circuits **320** and DQS routing circuit **620**.

FIG. **10**A illustrates an MDC **910** according to one embodiment. As shown, the MDC **910** includes a delay circuit **1012** that generates a delayed version MCS**1** of the corresponding MCS**0** by adding a predetermined amount of delay (e.g., 10 ps) to MCS**0**. MDC **910** also includes a delay circuit **1016** that generates a delayed version CK**1** of the clock signal CK**0** by adding a predetermined amount of delay to CK**0**. In one embodiment, CK**1** is delayed from CK**0** by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC **910** further includes a sampler circuit **1042** that samples MCS**1** according to CK**0** and outputs a sampled result A, a sampler circuit **1044** that samples MCS**0** according to CK**0** and outputs a sampled result B, and a sampler circuit **1046** that samples MCS**0** according to CK**1** and outputs a sampled result C. The MDC **910** further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z**1** and Z**2** based on the sampled results A, B, and C.

In one embodiment, Z**1** is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., Z**1**= $\overline{A \oplus B}$, and Z**2** is the result of another logic operation on the sampled results, e.g., Z**2**=$\overline{B \oplus C}$. Thus, as shown in FIG. **10**B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge **1061** of CK**0** is close to the right side of a data eye where gliches at the edges of the data eyes can make C unpredicatable, A and B can be in agreement (i.e., Z**1** is true) while B and C are likely not in agreement (i.e., Z**2** is false). FIG. **10**C illustrates a metastability condition when there is insufficient set-up time. As shown in FIG. **10**C and Table 1 below, a rising clock edge **1061** of CK**0** is close to the left side of a data eye where gliches at the edges of the data eyes can make A unpredicatable. Thus, A and B can be in disagreement so Z**1** is false while B and C can be in agreement so Z**2** is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge **1061** of CK**0** and the rising clock edge **1062** of CK**1** are near the middle of an MCS**0** data eye so there is no metastability issues and both Z**1** and Z**2** are true, as shown in Table 1.

FIG. **10**D illustrates a signal selection circuit **920** according to an embodiment. As shown, in one embodiment, the signal selection circuit **920** includes a first multiplexor **1071** that selects between CK**0** and CK**1** based on the metastability indicator Z**1**, and a second multiplexor **1072** that selects between MCS**0** and MCS**1** based on the metastability indicator Z**2**. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, Z**1**=1 and Z**2**=0, and MCS**1** is output from multiplexor **1071** while CK**0** is output from multiplexor **1072**. Sampler **930** thus samples MCS**1** according to the rising edges of CK**0**. Thus, more hold time is provided to mitigate the metastability condition since MCS**1** is shifted from MCS**0** toward the right.

On the other hand, where a metastability condition of insufficient set-up time occurs, Z**1**=0 and Z**2**=1, and CK**1** is output from multiplexor **1071** while MCS**0** is output from multiplexor **1072**. Sampler **930** thus samples MCS**0** according to the rising edges of CK**1**. Since CK**1** is shifted from CK**0** toward the right, more set-up time is provided to mitigate the metastability condition.

In the case when no metastability is detected, Z**1**=1 and Z**2**=1, and CK**0** is output from multiplexor **1071** while MCS**0** is output from multiplexor **1072**. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

TABLE 1

Metastability Detection and Signal Selection

Sampler Output			MS Indicators			Signal Selection	
A	B	C	Z1	Z2	MS Condition	CK	MCS
D1	D1	D2	1	0	insufficient hold time	CK0	MCS1
D1	D2	D2	0	1	insufficient set-up time	CK1	MCS0
D1	D1	D1	1	1	no metastability	CK0	MCS0

FIGS. **10**A-**10**D illustrate a relatively simple implementation of the metastability detection circuit (MDC) **910** where only three different sample points are provided to detect metastability condition in the module control signal. In general, the MDC **910** may generate more delayed versions of the module clock signal CK**0** and/or the corresponding module control signal MCS**0**, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. **11**A, the MDC **910** can include a plurality of delay circuits **1102** that generate m delayed versions of MCS**0**, e.g., MCS**1**, MCS**2**, . . . MCSm, and m delayed versions of CK**0**, e.g., CK**1**, CK**2**, . . . CKm. The MDC **910** can include sampler circuits **1104** that sample MCS**0** according to CK**0**, CK**1**, . . . CKm, respectively, and sampler circuits **1104** that sample MCS**0**, MCS**1**, MCS**2**, . . . MCSm according to CK**0**, respectively. The outputs of the samplers **1104** are provided to a logic circuit **1120**, which determines a metastability condition in MCK**0** based on the sampler outputs using, for example, a majority decision logic. The logic circuit **1120** outputs a first metastability indicator on line(s) **912** and a second metastability indicator on line(s) **914**.

FIG. **11**B illustrates a signal selection circuit **920** according to an embodiment. As shown, in one embodiment, the

signal selection circuit **920** includes a first multiplexor **1171** that selects between CK**0**, CK**1**, . . . , CKm based on the metastability indicator provided on line(s) **912**, and a second multiplexor **1172** that selects between MCS**0**, MCS**1**, . . . , MCSm based on the metastability indicator provided on line(s) **914**, such that the rising edges of the selected clock signal, e.g., Cki, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCSi. The selected signals MCSi and Cki are provided to the sampler **930**, which samples MCSi according to the rising edges of CKi.

As stated above, in certain embodiments, since the isolation devices **118** are in the data paths between the MCH **101** and the respective groups of memory devices **112**, the MCH **101** does not have direct control of the memory devices **112**. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices **118** includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation, as discussed further below.

FIG. **12**A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit **116** at time t**1**, the module control circuit **116** outputs one or more enable signals EN at time t**2** in response to the write commands. The one or more enable signals are received by an isolation device **118** at time t**3**, which afterwards receives one or more strobe signal DQS from the MCH **101** at time t**4**. Note that the same enable signal may be received by another isolation device **118** at time t**3'**, which can be in a different cycle of the system clock MCK from the cycle which t**3** is in. The time interval between t**4** and t**1** is consistent with a write latency W.L. associated with the system **100**, and is controllable by the MCH **101** and knowable to the isolation device **118**. The time interval between t**4** and t**3**, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device **118** since both these signals are received by the isolation device. Based on such determination, the isolation device **118** can have knowledge of the time interval between t**3** and t**1**, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device **118** to properly time transmission of read data to the MCH, as explained further below.

FIG. **12**B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit **116** at time t**5**, the module control circuit **116** outputs one or more enable signals EN at time t**6** in response to the read commands. The one or more enable signals are received by an isolation device **118** at time t**7**, which afterwards receives at time t**8** read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. Note that the same enable signal may be received by another isolation device **118** at time t**3'**, which can be in a different cycle of the system clock MCK from the cycle which t**3** is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices **118**.

With knowledge of the time interval between t**7** and t**5**, which should be about the same as the time interval between t**3** and t**1**, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t**9** by the isolation device to the MCH **101** via the respective group of data/strobe signal lines **130**, with the time interval between t**9** and t**5** being consistent with a read latency R.L. associated with the system **100**.

The time interval between t**4** and t**3**, i.e., the enable to write data delay EWD, is determined by the delay control circuit **650** in the ID control circuit **310**, as shown in FIG. **6**. According to one embodiment, as shown in FIG. **13**, the delay control circuit **650** includes a peramble detector **1310** to detect a write preamble in the DQS, a flip-flop circuit **1320** having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK**0**, and a counter circuit **1330** having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit **1320**. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

FIG. **14** illustrates a DQ or DQS routing circuit **320** or **620** according to an embodiment. As shown, the DQ/DQS routing circuit **320**/**620** includes a DQ/DQS pin **1401** that is coupled to the corresponding DQ/DQS signal line **322**/**324**, a set of one or more DQS pins **1402** that is coupled to a corresponding module DQ/DQS line(s) Y/Y_{DQS}, or YA/YA_{DQS} and YB/YB_{DQS}. The DQ/DQS routing circuit **320**/**620** further includes a write strobe buffer **1410** that buffers write data/strobe, and a write data/strobe receiver **1420** that samples the write data/strobe. The DQ/DQS routing circuit **320**/**620** further includes a plurality of write paths **1430** that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

The DQS routing circuit further includes a plurality of read paths **1450** that are selectable by the one or more of the module control signals. Output from the selected read path is delayed in a delay circuit **1460** by an amount controlled by the delay signal DS, and sampled by a sampler circuit **1470**. The sampled read data/strobe is transmitted by transmitter **1480** onto the corresponding data/strobe signal line **322**/**324** via the DQ/DQS pin **1401**.

FIG. **15** illustrates a DQS routing circuit **620** according to an embodiment. As shown, the DQS routing circuit **620** includes a first DQS pin **1501** that is coupled to a corresponding DQS signal line **324**, a second DQS pin **1502**A that is coupled to a corresponding module DQS line YA_{DQS}, a third DQS pin **1502**B that is coupled to a corresponding module DQS line YB_{DQS}. The DQS routing circuit **620** further includes a first write strobe path coupled between the first DQS pin **1501** and the second DQS pin **1502**A and a second write strobe path coupled between the first DQS pin **1501** and the third DQS pin **1502**B. The first write strobe path includes a write strobe buffer **1510** that buffers a write strobe, a write strobe receiver **1520** that samples the write strobe according to the buffered module signal CK**0**. The sampled write strobe is provided to the DQ routing circuits **320** as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter **1530**A that transmits the write strobe to one or more memory devices **112** coupled to the module strobe line YA_{DQS}. The second write strobe path includes the write strobe buffer **1510**, the write strobe receiver **1520**, and a second write strobe transmitter **1530**B that transmits the write strobe to one or more memory devices **112** coupled to the module strobe line YB_{DQS}. The first and second write strobe transmitters, **1530**A and **1530**B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe

path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

The DQS routing circuit further includes a read strobe path coupled between the first DQS pin **1501** and a selected one of the second and third DQS pins **1502**A and **1502**B. In the read strobe path, a select circuit **1550** (e.g., a multiplexor) selects either a read strobe signal received via DQS pin **1502**A or a read strobe signal received via DQS pin **1502**B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit **1560** by an amount controlled by the delay signal DS, and sampled by a sampler circuit **1570** according to the buffered module clock signal CK**0**. The sampled read strobe is provided to the DQ routing circuits **320** as the read strobe RDQS and is transmitted by transmitter **1580** onto the corresponding strobe signal line **324** via the first DQS pin **1501**.

FIG. **16** illustrates a DQ routing circuit **320** according to an embodiment. As shown, the DQ routing circuit **320** includes a first DQ pin **1601** that is coupled to a corresponding DQ signal line **130**, a second DQ pin **1602**A that is coupled to a corresponding module DQ line YA_{DQ}, a third DQ pin **1602**B that is coupled to a corresponding module DQ line YB_{DQ}. The DQ routing circuit **320** further includes a first write data path coupled between the first DQ pin **1601** and the second DQ pin **1602**A and a second write data path coupled between the first DQ pin **1601** and the third DQ pin **1602**B. The first write data path includes a write data buffer **1610**, a write data receiver **1620** that samples write data according to the write strobe WDQS from the DQS routing circuit **620**, and a first write data transmitter **1630**A that transmits the write data to one or more memory devices **112** coupled to the module data line YA_{DQ}. The second write data path includes the write data buffer **1610**, the write data receiver **1620**, and a second write data transmitter **1630**B that transmits the write data to one or more memory devices **112** coupled to the module data line YB_{DQ}. The first and second write data transmitters, **1530**A and **1530**B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

The DQ routing circuit further includes a read data path coupled between the first DQ pin **1601** and a selected one of the second and third DQ pins **1602**A and **1602**B. In the read data path, a select circuit **1650** (e.g., a multiplexor) selects either a read data signal received via DQ pin **1602**A or a read data signal received via DQ pin **1602**B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit **1660** by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit **1670** according to the read strobe RDQS from the DQS routing circuit **620**, and transmitted by transmitter **1680** onto the corresponding data signal line **130** via the first DQ pin **1601**.

FIG. **17** illustrate a delay circuit **1560** or **1660** according to an embodiment. As shown, the delay circuit **1560** or **1660** includes a plurality of delay stages, such as delay stages **1710**, **1720**, and **1730**, each delaying a read data or read strobe signal from the select circuit **1550**/**1650** by a predetermined amount. The delay circuit **1560** or **1660** further includes a select circuit **1740** (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit **1740**, is provided to the sampler circuit **1570** or **1670**, either directly or after being buffered by a buffer circuit **1750**.

Thus, as shown in FIG. **18**, in one embodiment, a memory module **110** operates in the memory system **100** according to a method **1800**. In the method, during a write operation, one or more module control signals are received by an isolation device **118** from a module control circuit or module controller **116** (**1810**). The module controller **116** generates the one or more module control signals in response to C/A signals representing a write command from the MCH **101**. The one or more module control signals are used to control the isolation device **118**. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device **118**. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device **118** from the MCH **101** (**1820**). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

Since the time interval between the arrival of the command signals from the MCH **101** and the arrival of the write data/strobe signal DQ/DQS from the MCH **101** is a set according to a write latency parameter associated with the system **100**, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module **110** and the time when the one or more enable signals are received by the isolation device **118**. The time interval CED can be used by the isolation device **118** to properly time the transmission of read data to the MCH **101**, as described above and explained further below.

As shown in FIG. **18**, a delay signal DS is generated according to the time interval EWD (**1830**). Concurrent to receiving the write strobe signal DQS, the isolation device **118** also receives a set of write data signals DQ (**1840**). The received write data signals are transmitted to the subgroup of memory devices (**1850**), which are selected from the group of memory devices coupled to the isolation device **118** by the one or more first enable signals.

During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device **118** from the module controller **116** (**1860**). The one or more second enable signals are generated by the module controller **116** in response to read command signals received from the MCH **101**, and are used by the isolation device **118** to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (**1870**). To properly time the transmission of the DQS and DQ signals to the MCH **101**, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system **100**.

In certain embodiments, especially the embodiments shown in FIG. **2**D, the delay circuits **1560** and **1660** shown in FIGS. **15** and **16** are not needed to provide alignment of the read data. As shown in FIG. **19**, the ID control circuit **310** includes a clock regeneration circuit **1920** that regenerates the clock signal CK received from the control circuit **116**, according to the delay signal DS. The regenerated clock signals CK**0** and CKM each includes a proper amount of

delay as compared to the clock signal CK. The clock CK**0** is provided to the strobe routing circuit **620** so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer **118** and the respective set of memory devices are locally synchronized.

We claim:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and

memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

2. The memory module of claim **1**, wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation.

3. The memory module of claim **2**, wherein the each respective buffer circuit includes a delay control circuit configured to determine, during the memory write operation, a time interval between receiving a first signal from the module control device and receiving a second signal from the memory controller, and wherein the timing information includes the time interval.

4. The memory module of claim **3**, wherein the each respective buffer circuit is further configured to receive a module clock signal and further includes a clock regeneration circuit configure to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

5. The memory module of claim **3**, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

6. The memory module of claim **2**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output the respective data and strobe signals.

7. The memory module of claim **3**, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

8. The memory module of claim **7**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output the respective data and strobe signals, the two memory devices being in a same rank.

9. The memory module of claim **1**, wherein the each respective buffer circuit is further configured to receive a module clock signal from the module control device and further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal.

10. The memory module of claim **1**, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

11. The memory module of claim **10**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals.

12. The memory module of claim **1**, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

13. The memory module of claim **12**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to receive or output the respective data and strobe signals, the two memory devices being in a same rank.

14. The memory module of claim **1**, wherein the each respective buffer circuit is further configured to receives a module clock signal and further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is configured to output the local clock signal to the respective set of memory devices.

15. The memory module of claim **14**, wherein the data paths include a first data path for transmitting a strobe signal among the respective data and strobe signals, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal.

16. The memory module of claim **15**, wherein the data paths include a second data path for transmitting a first data signal among the data and strobe signals, the second data

path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

17. The memory module of claim **14**, wherein each of the plurality of buffer circuits has a data width of 1 byte , and wherein each of the memory devices has a data width of 1 byte.

18. The memory module of claim **17**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal.

19. The memory module of claim **14**, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

20. The memory module of claim **19**, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal, the two memory devices being in a same rank.

21. The memory module of claim **1**, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device.

22. The memory module of claim **1**, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the memory controller.

* * * * *

EXHIBIT 2

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21T

(Revision of JM21S, November 2017)

SEPTEMBER 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

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JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

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JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

(From JEDEC Board Ballot JCB-02-31A, JCB-04-75, JCB-04-89, JCB-05-60, JCB-05-103, JCB-05-124, JCB-05-99C, JCB-06-02, JCB-06-36, JCB-08-11, JCB-09-65, JCB-09-73, JCB-09-82, JCB-09-86, JCB-10-15, JCB-10-21, JCB-10-88, JCB-12-38, JCB-13-46, JCB-13-47, JCB-15-14, JCB-17-24, JCB-19-04, JCB-19-27, JCB-20-14, and JCB-20-15, formulated under the cognizance of the JEDEC Board of Directors.)

1 JEDEC

JEDEC is an independent incorporated Association governed by a Board of Directors (Board). The Association facilitates standardization within the solid-state, microelectronics, and associated industries, and other related activities through special purpose committees.

The Association and its members are committed to foster open competition in the development of products and services.

1.1 Mission

The mission of JEDEC is to serve the solid state industry by creating, publishing, and promoting global acceptance of standards, and by providing a forum for technical exchange on leading industry topics.

1.2 Scope

The scope of JEDEC includes but is not necessarily limited to areas relating to (1) solid state devices, (2) integrated circuits, (3) electronic modules and associated electronic components, and (4) various manufacturing functions/processes.

1.3 Membership

Any company, organization, consumer, or individual conducting business that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall[1] be eligible for membership in JEDEC. Membership on a given committee shall be open to any JEDEC member company in good standing dependent solely on the dues structure defined by the Board[2]. Government representatives may also participate as described in 2.4.

Each member company, organization, or individual shall be entitled to appoint one member and multiple alternates for each committee it joins. The member and alternates should be capable of making a technical contribution to the standards-setting process of the committee. To preserve the “one-company one-vote” concept within JEDEC, wholly-owned or majority-owned subsidiaries shall not be granted separate voting privileges within any single committee or subcommittee. The JEDEC Office shall maintain a list of all member companies and representatives for each committee.

[1] Special word usage. The word "shall" indicates a requirement; see JM7, Annex J.
[2] JEDEC membership is not a prerequisite to committee participation. Non-member participation fees will be charged. Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual. Further details are available from the JEDEC Office. See 3.4.

1.3 Membership (cont'd)

All changes in committee membership shall be the responsibility of the member company, who shall so advise the JEDEC Office and the committee chairperson in writing or by electronic means.

NOTE Government regulations restrict the participation of non-U.S. Nationals at certain meetings. Every effort shall be made to notify member companies, well in advance, when a meeting will cover restricted topics.

1.4 Board of Directors

The governing body of JEDEC is the JEDEC Board of Directors (Board) which is comprised of individual Directors (or their alternates) representing JEDEC member companies.

1.4.1 Eligibility

Any maximum dues paying Member Company of JEDEC, having an identified representative in two or more committees for at least the past two consecutive years, may nominate one candidate for Board membership. The nomination consists of the nominee's resume accompanied by a letter from a company executive to the Board chairperson (in care of the JEDEC Office). The support letter is to request that the nominee be considered for Board membership and committing that if elected the member company will support the nominee's active attendance and participation in JEDEC Board meetings and affairs. If the application meets the above requirements, the JEDEC Office will hold the application on file with other (qualified) nominees. The JEDEC Office will maintain an official list of nominations to the Board. A list of the current Board Committees with a brief description and the membership of each will be sent to the nominee with an invitation for the nominee to participate where he/she has interest.

Seats on the Board are occupied by Directors representing individual JEDEC Member Companies. Once elected to a Seat on the Board, the Member Company maintains its position until the seat is voluntarily relinquished or forfeited due to other events as outlined in 1.4.4. Mergers, divestitures, acquisitions and other corporate changes that do not substantially alter the nature of a member company will not be grounds to forfeit a seat on the Board so long as the new entity continues to meet all Board Eligibility Requirements, see 1.4.3.

The total number of Directors shall not exceed thirty (30).

1.4.2 Election of Directors

The Membership Committee (chaired by appointment of the Chairman of the Board with membership open to any Board Member) shall review with the Board circumstances of a vacated seat and recommend qualified nominees from the official nominations list. In order to choose an appropriate nominee to fulfill objectives of the Board, the Membership Committee will review activities that are being conducted in active Board Committees with their respective Chairs.

1.4.2 Election of Directors (cont'd)

The following process will occur:

- Board Committee Chairs will be informed of the vacant seat by the Membership Committee.
- It will be the responsibility of the Membership Committee to qualify the level of support required to achieve ongoing Board Committee objectives.
- The Membership Committee will compile inputs and prepare a review to the Board at the next Board meeting including a recommendation on how to fill any vacated seats.

The following procedures and guidelines will be employed by the Membership Committee during the preparation of its Director recommendations:

- Gathering of Board Committee Chair inputs on current activities and resource requirements. Chairs will have an opportunity to review with the Membership Committee special requirements, shortcomings, etc. that should be made evident during the election process.
- Identification of the nominee's JEDEC experience and previous contributions. Tenure and amount of activity within a Committee or Task group will be identified.
- Identification of Board demographics in regards to representation of committees.
- Identification of the leadership qualities the candidate will bring to the Board.
- Identification of the unique value of the individual and the member company. (Value based on Committee Objectives identified to properly support JEDEC.)
- Identification of the individual's education and professional background (Engineering, Management, Finance, Marketing, Business development, etc.) and the balance the candidate will bring to the Board.

The Board will act on the recommendations of the Membership Committee. New Directors are elected to the Board by a 75% majority of the Board members voting at the meeting. There is no requirement that the maximum of 30 Seats be filled. The Membership Committee will send a response letter to the elected candidate/company and inform them of their responsibilities as outlined in this section. The elected Director's qualifications will be presented in regards to support as an active member on one or more of the Board Committees. The Board may stipulate a contingency period during which the newly-elected Director is required to serve on one or more Board Committees.

1.4.3 Board Representation Changes

The following outlines events that may occur that affect Board Representation.

1.4.3.1 Merger

Two companies on the Board merge or consolidate:

- It is up to the new surviving company (or the new parent company) to decide which Board representative remains on the Board to comply with the "one vote per company" rule.

1.4.3 Board Representation Changes (cont'd)

1.4.3.2 Acquisition

One Board company acquires another Board company:

- It is up to the acquiring company to decide which Board representative remains on the Board to comply with the "one vote per company" rule.

A Board company acquires a non-Board company:

- The Board company can elect to nominate a different Board representative if it wishes, but final approval is still required by the Board.

1.4.3.3 Merger or Acquisition by Non-Board Company

A non-Board company merges with or acquires a Board company:

- If the non-Board company is eligible for Board membership (ref. 1.4.1), it can assume the Board seat of the acquired company subject to Board approval.

- If the non-Board company is not eligible for Board membership, it cannot assume the Board seat of the acquired company and the Board seat is considered open.

1.4.3.4 Split

A Board company splits into two or more companies:

- If the Board representative associated with the split (or spun-off subsidiary) is still employed by the member company then his/her status is unchanged.
- If the Board representative associated with the split is now a member of the new (or non-member) company then representative in question loses his/her seat.
  - Exceptions: Board decides that the Board representative in question is vital to the Board and the new member company complies with all JEDEC requirements to be on the Board.
- The member company that still has a seat on the Board can nominate a new representative to the Board who is then subject to Board approval.

1.4.4 Member company and Director resignation

The Director will relinquish a position on the Board in the instance of any of the following events:

1) The Member Company formally resigns the position. This includes a statement from the Member Company that confirms the Director and Member Company resignation.
2) The Member Company which the Director represents is no longer eligible as defined in 1.4.1.
3) The Member Company is removed by a majority vote of the Board for gross violation of JEDEC policy.
4) The Director is absent from and not represented by a Member Company's approved alternate at two consecutive Board meetings. It is the expectation that Directors attend all Board meetings, at minimum Directors must attend at least one face-to-face Board meeting, in person, each calendar year.

1.4.4 Member company and Director resignation (cont'd)

In the event that a Director no longer represents the Member Company for which the individual was elected (including but not limited to retirement or change of employment) or should the Director be removed due to gross violation of JEDEC policy outside of the control of the Member Company, then the Board seat shall not be considered vacated and the Member Company shall have the right to maintain its position on the Board by nominating a replacement Director. The replacement Director must meet all nomination requirements as set forth in 1.4.1 and be elected by the full Board by a 75% majority of the Board members voting at the meeting. Should the replacement Director fail to be elected, the Member Company may submit a second candidate and repeat the process.

1.4.5 Officers of the Board of Directors

The officers of the Board shall follow the same guidelines as the officers of a committee with the following exceptions: There shall be at least one Vice Chairperson on the Board. The number of Vice Chairpersons on the Board shall be determined by regular vote at any regularly scheduled Board meeting.

1.4.6 Board of Directors meetings

All meetings of the Board shall follow the same procedures and guidelines as outlined for regular committee meetings, with exceptions per 1.4.6.1, 1.4.6.2, and 1.4.6.3.

1.4.6.1 Board of Directors executive session

The needs of the Association occasionally require the Board to meet in executive session. Such executive sessions are to be defined as closed meetings of Board member company representatives and guests invited for specific purposes only.

1.4.6.2 Board of Directors voting

All actions within the Board require an affirmative vote of at least 75%; members abstaining shall not be considered for determination of the 75% criterion. When defined and agreed to by a duly recorded vote of the Board, specific action may require polling of all members whether present or not and/or may require a higher percentage affirmative vote.

1.4.6.3 Emergency action by the Board of Directors

If action normally requiring Board consideration must be taken, and a meeting cannot be reasonably convened, then the following modifications apply to the approval process: 1) A reasonable attempt must be made to notify 100% of Board members, and 2) The decision shall become binding only upon receipt by the JEDEC Office of affirmative votes from 75% of the members of the Board.

1.4.7 Board of Directors guest policy

All guests must be approved by the chairman and must have a purpose related to the topics of discussions at the Board meeting. The guest must be introduced to the Board at the meeting and the purpose of the guest's visit should be stated in the agenda for that meeting.

At the discretion of the Board, a guest may be allowed to stay beyond the allotted time slot if the Board feels there is a need for that guest's continued attendance. Otherwise, all guests may only attend the portion of the Board meeting that is directly related to their purpose in the meeting. At no time may a guest speak to the Board beyond the intended purpose of his/her invitation without the explicit approval of the Board.

At anytime, any member of the Board may request that the chairman, at his discretion, ask a guest to leave the meeting.

1.5 Governance/Interpretation

The Board shall have the sole authority to interpret, in whole or in part, these operating procedures. In any case where conflict arises from ambiguity, or lack of specificity, or misunderstanding within or related to this document, the officers of the Board of the Association may make temporary rulings to be confirmed or modified at or before the next regularly scheduled Board meeting by vote of the Directors. In any case where there is not agreement between 100% of the officers of the Board concerning an interpretation, then the matter must be referred to the entire Board for resolution.

1.6 Scope of participation

The standards development process shall not be dominated by any single interest category, individual, or organization. Dominance means a position or exercise of dominate authority, leadership, or influence by reason of superior leverage, strength, or representation to the exclusion of fair and equitable consideration of other viewpoints.

The standards development process should have a balance of interests. Participants from diverse interest categories shall be sought with the objective of achieving balance.

NOTE In the case of an ANSI American National Standard, JEDEC shall comply with the criteria for balance as contained in ANSI Essential Requirements.

1.6.1 Interest categories

For a formulating group to work effectively, all interest categories should be represented, and no interest category shall be intentionally excluded. Because standards development depends on consensus rather than the will of a majority, participation in the consensus-building process is of far greater significance than the final act of voting in a formulating group. Unless it is claimed by a directly and materially affected interest that a single interest category dominated the standards development process, no test for dominance is required.

Interest categories are defined relative to each standards activity: producer; user; and general interest. See ANSI Essential Requirements for further information.

1.6.1 Interest categories (cont'd)

1.6.1.1 Producer

Producers are formulating group members that manufacture electronic equipment or electronics-related products covered by the standard.

1.6.1.2 User

Users are members that utilize electronic equipment or electronics-related products covered by the standard to provide services to an end user.

1.6.1.3 General interest

General Interest members are neither producers nor users. This category includes, but is not limited to, regulatory agencies (state and federal), researchers, other organizations and associations, end users and consumers.

1.7 Limits and restrictions

The Members (particularly where they are direct competitors in certain lines of business, and including their employees and representatives), shall, when engaged in the activities and affairs of the Association, act in a manner that does not violate any state, federal or international laws or regulations.

Member companies must abide by all applicable export control regulations of their respective countries while attending a JEDEC meeting, irrespective of where the meeting is actually held. It is recommended that the member seek guidance from his or her company if involved in "state of the art" engineering work, as significant changes are made to the export control regulations from time to time.

The Association prohibits any discussion on specific costs, prices, quantity or yield of production levels, methods or channels of distribution, markets, customers or any other topic, or any conduct that may be construed as a violation of antitrust laws. Each respective member company shall advise its respective participant representatives and employees on the importance of compliance with applicable state, federal or international antitrust laws or regulations and require the scope of any discussions or exchanges amongst representatives of Members and/or the Association, be limited to the mission and scope of the Association stated above.

1.8 Modifications to the Manual of Organization and Procedure

Modifications to this manual may be made in whole or in part, upon approval by the Board by the normal ballot process. Any changes to this Manual shall be distributed to the JEDEC membership at the earliest possible time upon adoption.

2 Committees

The Board shall have the authority to establish committees to perform any task(s) for the association. JEDEC committees (main and sub) shall be authorized only by the Board, and the Board shall approve the scope of each[3]. A main committee shall be designated by the prefix JC- plus a two-digit designator, such as committee JC-11. Main committees are separated into two types: (1) service committees, whose scope is limited to a specific subject that may impact several product types, and (2) product committees, whose scope is limited to a specific type product. For service committees, the first digit of the two-digit designator shall be the number 1, and for product committees, the first digit shall be the number 2 or higher.

When the main committee finds it necessary to divide its work into parts, subcommittees may be formed under the scope of the main committee and such subcommittees shall be designated by adding a period to the main committee number followed by a number or a number-and-letter designator (e.g., JC-42.3 or JC-42.3B).

Subcommittees shall have all the same authority and responsibilities as committees herein defined, except that a subcommittee scope shall be a subset of a committee scope, to be authorized, reviewed, and approved by the Board.

NOTE Participation shall be open to all persons who are directly and materially affected by the activity in question.

2.1 Committee responsibilities

Each committee shall have the authority to consider all matters within its approved scope, including but not limited to the following actions:

a) Develop proposed standards, guidelines, registrations, and related technical publications for committee ballot.

b) Authorize committee ballots on all matters within the committee's defined scope.

c) Initiate proposals for Board ballots of previously approved committee ballots.

d) Evaluate the results of all committee ballots, as well as comments on related Board ballots.

e) Request approval of the Board to convert standards or publications into ANSI or IEC standards.

f) Maintain liaison with other national and international organizations.

g) Initiate press releases to announce a significant advancement in the work of solid state technology covered within the committee scope such as: registrations, standardization, or publication. All press releases are to be issued by the JEDEC Office after review and concurrence by the JEDEC Legal Counsel.

[3] The committee scope shall go through the standard balloting process and must be completed within a reasonable timeframe and prior to any publication of a JEDEC document authored by the committee.

2.2 Executive committee

A JEDEC committee or subcommittee may form an executive committee to manage its administrative work. The executive committee shall meet the following criteria:

a) The executive committee should be chaired by the committee or subcommittee chairperson and shall include as a minimum all chairpersons and vice chairpersons of that committee and its subcommittees.

b) Meetings of the executive committee shall be open to any committee member who gives reasonable advance notice to the executive committee chairperson or secretary.

c) Actions of the executive committee shall be limited to handling administrative matters dealing with such items as meeting schedule, meeting agenda, future meeting dates and locations, personnel requirements, proposed work priorities, and the like. Any decision made by the executive committee is subject to review and modification by the full committee at the request of any committee member or alternate. Decisions on the final disposition of all technical matters shall be made only by the overseeing committee. Recommendations concerning future meeting dates and locations should be presented to the overseeing committee.

2.3 Election of officers

All JEDEC committee officers shall be members or alternates of their respective committees. All JEDEC committees shall have a chairperson and may also have a vice chairperson as officer(s) of the committee. All officers shall be directly elected either by secret vote of the committee members present during a regular meeting or by ballot as determined by vote of the committee. Committee officers shall serve a term of two (2) years. The JEDEC staff shall count the secret ballot and announce the result at the meeting.

At least two meetings prior to the end of a chairperson's term, he/she shall appoint a nominating committee to propose candidates to fill the next term of office(s) for the committee. The committee's candidates must be presented to the full committee at the next meeting and nominations from the floor shall also be accepted. All nominees must agree to accept the additional responsibilities before they can be considered.

If any of the officers cannot fulfill his/her term then elections shall be held at the earliest opportunity of the committee members. Similarly, if a new committee is formed, then the chairperson shall be selected by vote of the members attending the first meeting as a first order of business of the committee. These special case elections shall become effective immediately.

2.4 Government entities

JEDEC desires and encourages the active participation in its standards-developing activities of all parties having a direct and material interest in the standards, including U.S. federal, state, and local government entities when they have such a direct and material interest via the JC-13 Committee, Government Liaison.

Contribution to the standards development process may take the form of liaison with appropriate formulating groups, participation in the ANSI public review process, and active participation in formulating groups.

3 Meetings

Communication between JEDEC member companies is essential for the work within the Association. All committees shall hold regular meetings for the purpose of conducting JEDEC business.

The use of teleconference or other electronic conferencing equipment is permitted for any type of JEDEC meeting.

3.1 General requirements

Every JEDEC meeting, regardless of type, shall be held in accordance with the directives contained within this manual and in accordance with all applicable laws.

All meeting notices, agendas, ballots, and minutes shall be distributed only by the JEDEC Office. All correspondence from the JEDEC Office shall only be by electronic means unless otherwise required by law. If a company requests distribution by other means, the JEDEC Office will charge a fee for such additional service as directed by the JEDEC Board. The JEDEC website, www.jedec.org, shall be the primary method of electronic communication.

3.2 Notices

Notices of regular meetings shall be distributed solely by the JEDEC Office no less than 28 calendar days prior to the start of such meeting, unless a “special” meeting is authorized by committee vote and the date and agenda for such meeting is fixed at a regularly scheduled meeting. Notices of such special meetings shall be distributed as soon as possible after said regular meeting and in no case less than 10 calendar days prior to the start of such special meeting.

3.3 Agendas

All meetings shall have prepared agendas distributed as soon as possible, but in no case less than 10 days prior to a meeting and should be included with the meeting notice if possible. All special meeting notices shall include the agenda at time of distribution of such notice.

3.4 Meeting attendance

All JEDEC committee and subcommittee meetings are open to members, their designated alternates, and guests invited by the committee or subcommittee chairperson.

A JEDEC staff member or a designated alternate must participate in every committee meeting, either in person or by electronic means. The duties of the staff person shall include but not be limited to taking minutes, advising the chairperson regarding the content of this manual and JEDEC legal policies and guidelines, and distributing the minutes. JEDEC staff attendance is not required at every subcommittee meeting.

A potential new member company may be a guest for one meeting with prior approval of the chairperson. A timely submission of such a request stating the purpose of attendance shall be given so that appropriate accommodations can be made. If there are any issues to be raised by a guest, those issues must be specified in the purpose statement.

Nonmembers may participate in committee meetings if they pay a nonmember participation fee, the fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available. Nonmembers do not have the right to vote. Nonmembers should contact the JEDEC Office prior to the meeting date for further details.

Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual.

An individual representative may represent only one company at any committee, subcommittee or task group meeting, and may vote on behalf of only one company on any ballot placed on the electronic voting machine. It is the responsibility of the committee chairman to enforce this rule during a committee or subcommittee meeting. For the electronic voting machine, it is the responsibility of the ballot sponsor to enforce this rule when the ballot tally is reported.

3.5 Quorum

The JEDEC Office shall maintain a list of active members for the sole purpose of determining the quorum requirements for a committee meeting. An active member is defined as a member company that has been represented at either or both of the previous two consecutive regular meetings of the committee. Special meetings shall not be considered for the purpose of determining “active” member status. The quorum requirements shall be 50% by count of a committee’s active member list, but in no case shall the quorum requirement be greater than 12 member companies regardless of committee size. All committee member companies present at a meeting are counted toward quorum requirement.

3.6 Recording devices

Voice or video recording devices of any kind are forbidden at any type of JEDEC meeting.

3.7 Minutes

The principal activities and attendees at all JEDEC meetings shall be duly recorded in meeting minutes. Meeting minutes shall be taken by the assigned JEDEC staff for that committee or by a substitute designated by the JEDEC staff. In the absence of a JEDEC staff person at a committee meeting, a temporary secretary may be assigned by the committee chairperson.

Minutes shall be termed "unconfirmed" until reviewed and confirmed by the committee chairperson and JEDEC Legal Counsel. In the interest of member company needs, minutes should be distributed to members and alternates within 14 calendar days after a meeting. If the chairperson is unable to review and confirm the minutes within that time, the JEDEC Office should distribute the unconfirmed minutes clearly labeled as unconfirmed minutes. Unconfirmed minutes shall be approved by JEDEC Legal Counsel prior to distribution. Confirmed meeting minutes from regular meetings shall be distributed no later than 28 days prior to the next regular meeting. Confirmed minutes from "special" meetings should be distributed as soon as possible after such special meeting and in no case less than 10 days prior to the next regular meeting.

At the end of each set of minutes the following statements shall appear:

"Reviewed/corrected and authorized for release" followed by the Chairperson's and Secretary's name and date.

_____
Chairperson, Name / date

_____
Secretary, Name / date

_____
Confirmed Legal Approval Date

"This meeting was conducted in accordance with JEDEC Legal Guides and the JEDEC Manual of Organization and Procedure."

For those situations where a report from an independent group is included in the minutes, for information purposes, then the following disclaimer may be added to the minutes:

"Disclaimer: All liaison, government, technical, and task group reports contained herein are believed to be accurate but the accuracy or completeness thereof is not guaranteed."

Minutes of a task group meeting shall include a list of the attendees, the meeting agenda, a status review of the agenda items, and any final proposals including discussion related to the proposals. The time, the place, and any required follow-up should be included. Task group minutes are reported and approved as part of the minutes for the next meeting of the sponsoring committee.

3.7.1 Policy statement on JEDEC sign-in/attendance rosters

The policy statements reproduced on the reverse side of the JEDEC sign-in/attendance rosters shall become an integral part of the minutes of all committee, subcommittee, and task group meetings; and a statement shall be included in the minutes indicating compliance with the foregoing policy.

3.8 Regular meetings

Every JEDEC committee shall set up an annual calendar for regular meetings at which any item covered under the scope of the committee may be discussed. Under the JEDEC guidelines, committees must hold at least one (1) regular meeting each year to retain status as an active committee.

3.9 Special (Limited Scope)

All JEDEC committees shall have the authority to approve meetings of limited scope. Schedule for the meeting and specific agenda items must be approved by formal vote during a regular committee meeting. During a limited scope meeting, no other committee business shall be conducted outside of the specific items on the previously agreed to agenda. Items shall not be added to the agenda of a special meeting.

3.10 Joint meetings

3.10.1 Between JEDEC committees

Joint meetings between two or more JEDEC committees may be authorized by agreement of the committees by vote. Selection of the joint meeting chairperson shall occur by vote of the committees' attendees. The joint chairperson shall ensure that all meeting notices, agendas, and minutes are distributed to the relevant JEDEC committees.

3.10.2 Between JEDEC and any non-JEDEC organization

Joint meetings between a JEDEC committee and any non-JEDEC organization are subject to the same requirements as 3.10.1. In addition, JEDEC Legal Counsel shall establish a Memorandum of Understanding (MoU), see 3.10.3, between the organizations and review all release of information from the meetings to any outside person or organization.

JEDEC committees may meet jointly with other organizations or agencies for the purpose of permanent or ongoing liaison. In these cases, those nonmembers attending the committee meeting are expected to pay their proportionate part of the total meeting costs. Apportionment of the meeting costs shall be agreed upon between the committee chair and the representatives of those groups participating in the meeting(s), subject to the approval of the JEDEC Board.

3.10.3 Memorandum of Understanding (MoU) with any non-JEDEC organization

Prior to the formation of a joint meeting/task group with a non-JEDEC committee, a Memorandum of Understanding (MoU) must be in effect between JEDEC and the other organization covering the following items:

a) Balloting procedure (acceptance criteria, resolution of comments, and disapprovals),

b) Patents procedure (including joint ownership),

c) Distribution rights (copyright, use of association logos, available on JEDEC website without charge),

d) Procedures for future revisions of the document(s),

e) Selection of chairperson(s) and appointment of task group membership, and

f) Meetings and related legal requirements (notices, agendas, motions, minutes, costs, etc.).

3.11 Task groups

A task group may be authorized by any committee chairperson for a specific non-continuing objective. The task group chairperson, appointed by the committee chairperson, shall be a member or alternate of the overseeing committee. Membership within a task group is open to any member or alternate of the committee within which the task group is formed. In addition, members of the task group may also be appointed by the task group chairperson from nonmember JEDEC companies with approval of the overseeing committee chairperson; appointment shall be based solely on ability to contribute to the work; however, all members of a task group shall conduct their work in accordance with this manual.

A task group is not permitted to hold any formal votes or establish any final results relative to standards, publications, or ballots. All task group activities shall be presented to the overseeing committee for review, modification, and approval in the form of reports generated from every task meeting. By duly recorded committee vote, committees may authorize a task group to issue ballots or other specific tasks as required, the specific exception being that committees cannot authorize a task group to conduct a formal vote. A task group must be dissolved upon completion of its objectives.

Scheduling of task group meetings is subject to approval of the sponsoring committee's chairperson, in order to avoid conflict with regularly scheduled meetings.

3.11.1 Joint task groups between JEDEC committees

Joint task groups between two or more JEDEC committees may be authorized by agreement of the committee chairpersons. Selection of the task group chairperson shall be part of this agreement and that chairperson must be a member or alternate of one or more committees involved in the task group. The task group chairperson shall keep all sponsoring committees on the distribution list for all meeting notices, agendas, and reports. Joint task groups between JEDEC committees shall comply with all other requirements for task groups.

3.11.2 Joint task groups between a JEDEC committee and other organizations

Joint task groups between a JEDEC committee and other non-JEDEC organizations are subject to the same requirements as task groups per 3.11. Unless otherwise authorized by the Board and approved by JEDEC Legal Counsel, such joint task groups shall establish a Memorandum of Understanding (MoU), see 3.10.3, in the same manner as joint committees covered in 3.10.2.

4 Document development procedure

The development of all JEDEC documents shall follow the minimum sequential procedure outlined herein.

1) Presentation – initial showing or distribution of material proposed for publication. Presentations may occur at any regular meeting or special meeting if the limited scope and agenda include such information. Presentations may also occur entirely electronically without being at a meeting. An additional showing of material proposed for publication may be required.
2) Motion for ballot – may occur at any time after a presentation. The motion must have a second before being considered for vote. The company agreeing to second the motion for ballot should be willing to accept responsibility for sponsoring the material should the original sponsor be unable or unwilling to do so. The motion for ballot should be discussed after receiving a second and then a formal vote shall be taken.
3) All committee ballots shall be subjected to the committee's editorial process prior to being posted on the JEDEC voting machine.
4) Committee ballot – if approved, material shall be sent out to ballot through the JEDEC voting machine. Details of balloting procedure are covered in section 6.
5) Motion to Board ballot – if a ballot passes and all comments are addressed then a motion may be made to send the material on to the Board for further consideration and approval. Alternatively, the motion to forward the ballot to the Board is unnecessary if the ballot passes by acclamation, see 5.2.
6) Board ballot – when approved, the committee material shall be sent out to ballot through the JEDEC voting machine. Board ballots follow the same procedures as committee ballots, see 6.6.1(c). When reviewing material passed by committee, the Board primarily considers whether due process has been followed.
7) Publication – once proposed material has successfully completed all the above steps and obtained approval through the appropriate balloting processes, it is approved for publication.
8) All JEDEC documents shall be published by the JEDEC Office.

NOTE 1 Steps may be repeated as many times as required to satisfy the wishes of the member companies participating in the process.

NOTE 2 JEDEC Registrations are special-case publications that do not have to be reviewed by the JEDEC Board of Directors, and the registration procedure ends upon the completion of step 4 above.

4.1 Copyrights

JEDEC owns the copyright to all documents created through JEDEC, and use of that copyrighted material is at the sole discretion of the JEDEC Board.

For the protection of member companies, all JEDEC publications and standards shall be copyrighted. As a precaution, draft proposals circulated for comment and/or vote shall display the symbol ©, followed by the year and "JEDEC". Stapled or bound documents require this designation only on the first page or title page; short documents that may be distributed unstapled shall be so labeled on every page. When final documents are ready for publication, the JEDEC Office shall register the copyright and maintain all appropriate records.

JEDEC member companies may reproduce any JEDEC document for internal use, without restriction. Use of JEDEC material outside of member companies is at the discretion of the Board. Generally, all JEDEC documents are available on the JEDEC website: www.jedec.org.

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, the committee shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

5 Voting

JEDEC shall formally operate under the rule of "One company, one vote" wherein all formal, binding votes will be restricted to one vote per company. Nonbinding fact-finding "straw" or survey votes are not considered formal votes. Unless specifically authorized by the Board, all approval vote counts within JEDEC shall be a minimum of 2/3 of votes cast. All Board approval vote counts shall be a minimum of 3/4 of votes cast. Abstention votes shall not be considered in the calculation.

Votes taken during committee meetings shall be duly recorded in the meeting minutes, and, except for unanimous votes, the vote count shall be included in those same meeting minutes.

In order to maintain fairness within every committee, the committee chairperson shall refrain from voting during a meeting for all but secret votes. If a chairperson has a specific company position on a topic being discussed, then control of the meeting should be turned over to the vice chairperson or other less biased member. Chairpersons may vote on any ballot to represent his/her company position.

5.1 Ballot voting

The period for voting on committee ballots shall be at least 21 calendar days from the date of issuance, and shall not exceed 90 days. In any case, the ballot closes at midnight, Eastern Time, on the final day of the voting period. All committee ballots shall be processed through the JEDEC electronic voting machine, and shall include the following vote options:

a) approve, comments are optional with approval

b) disapprove, comment is required and shall include a full explanation of the reason(s) for the disapproval

c) abstain, comments are optional with abstain

NOTE All committee ballots shall contain the following patent statement:

"If anyone receiving this ballot is aware of any patents (granted or pending) involving in this ballot, check here and notify the committee, citing the applicable patent numbers."

No one can have access to the ballot results before the voting period ends. As part of the deliberative, consensus-building process, commenters may send questions to the ballot sponsor independent of their votes via email, telephone, etc.

5.2 Ballot approval by acclamation

A committee ballot is considered approved by acclamation in either of the following two cases:

a) The ballot is approved unanimously with no comment at the close of the voting period.

b) The ballot is approved by count at the end of the voting period, and all comments whether from approve, disapprove, or abstain votes are resolved to the satisfaction of the sponsor and the commenting company. If any company is not satisfied with the proposed resolution of a comment, then resolution of the ballot must await committee action.

Any ballot approved by acclamation shall automatically advance to the next level in the publication process (i.e., committee ballots are automatically submitted to the Board, or Board ballots automatically become approved for publication). At the discretion of the committee chairperson, ballots that otherwise meet the requirement for approval by acclamation may be referred back to committee for further action if special conditions exist (e.g., uncharacteristically low vote count for the committee).

6 Ballots

All committee ballots shall be distributed ONLY by the JEDEC Office with Board-approved electronic distribution methods to all committee members and alternates for vote and to all related committees for information and comment. A submission for ballot shall be made through the JEDEC Office ONLY by Board approved editable and non-editable "soft copy" format of the complete ballot content.

Reference to any individual(s) and/or member company name(s) is prohibited from appearing on any committee ballot unless it is part of a return address.

In order to facilitate document identification and retrieval, keywords shall be submitted with all ballots. A keyword is defined as a word, term, or acronym that is descriptive of the essential contents of the ballot or a major portion thereof.

6.1 Editorial changes

During a committee meeting, provided there is no disagreement within the committee that the changes are editorial, these changes may be incorporated into committee-approved balloted material without reballoting.

6.2 Ballot lobbying

Member companies should not lobby or coerce other member companies to approve or disapprove ballots. Open discussion of balloted material is permitted and encouraged, but such discussions should focus on the technical aspects of balloted material.

The use of verbal, physical or business threats, intimidation, harassment or coercion is unprofessional behavior and unacceptable conduct at or in connection with any activity sponsored by JEDEC, including committee and task group meetings.

6.3 Copyrights

See 4.1

6.4 Regular committee ballot

A "regular" ballot is one in which the entire standard, publication, registration, guideline, or specification is open for comment.

Prompt consideration shall be given to the written comments and objections of all participants during the committee balloting process. An effort to resolve all expressed objections accompanied by comments related to the proposal under consideration shall be made, and the disposition of each such comment or objection and the reasons therefore shall be documented in writing (including electronic minutes and ballot material).

6.5 Limited committee ballot

If a limited number of revisions to an existing document are being proposed, a "limited" ballot may be issued. Limited ballots may be restricted to considering only the proposed areas for modification, addition, or deletion. In the cases of limited ballots both the original material and the proposed revisions thereto shall be clearly shown in the ballot material. Examples of appropriate occasions for using limited ballots are (1) a proposal to add a new definition to a long list of definitions or (2) a new package outline to JEDEC Publication No. 95.

On occasion, after a committee ballot has been approved, the committee may wish to propose minor technical changes to the ballot before forwarding the approved material on to the Board for final consideration. In such cases, a motion may be made for a limited ballot in which only these technical changes may be addressed. If the limited ballot is passed, these changes shall be incorporated. If it fails, the original material stands as approved.

NOTE This process is not intended for use in the development of an ANS.

6.6 Board of Directors ballot

In general, all ballots originating at the Board level shall follow the same guidelines outlined in 6.4. Board ballots are restricted in scope to non-technical Association business and specifically may not include new technical for publication creation as such material must first be submitted by the appropriate technical committee.

6.6.1 Committee ballots sent to the Board of Directors

All passed committee ballots relating to proposed JEDEC standards, guidelines, or specifications must be reviewed and approved by the JEDEC Board before becoming official JEDEC publications. Upon approval by acclamation or by committee vote[4], the originating committee shall submit such passed committee ballot[5] to the JEDEC Office for distribution as a Board ballot.

All ballots submitted to the JEDEC Board must include the committee ballot material, and:

a) a brief description of the recent committee background regarding the material.
b) the complete voting report including the names and votes of the member companies voting and all comments on the material.
c) a description of the resolution of all of the comments on the material. Negative votes must be addressed, however if they cannot be resolved, the ballot can be submitted to the Board with the approval of the committee.

The Board may make only editorial modifications to any material proposed by committee for further action. Any technical modifications of committee material must be referred back to the originating committee for possible action.

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[4] Unless the committee ballot passes by acclamation, a formal committee vote must be taken and recorded in the minutes to send the committee ballot to the Board for further action.

[5] Ballot material submitted for a Board ballot must be identical to the ballot material approved by the committee. The committee may authorize an editorial committee to review the document for editorial corrections only prior to issuing the Board ballot. In this situation, the Board ballot must be a marked up version of the committee-approved ballot material, such that all edits are clearly noted.

6.7 Survey ballots

Surveys may be issued to determine whether a proposal warrants further action. A survey may ask for information or for a support/nonsupport position. No committee vote is required for the distribution of a survey ballot; however, every survey must be approved by the committee chairperson and issued by the JEDEC Office following legal approval. The JEDEC Office shall monitor every survey to ensure adherence to JEDEC legal guidelines. Surveys that contain company-sensitive material that must remain confidential shall be stripped of any reference to a company by the JEDEC Office prior to use of the material. In all cases, survey results shall be presented to the full committee at the first meeting following the voting period expiration date.

Survey ballots are for gathering information or further clarifying member positions and survey votes are strictly nonbinding. All surveys should contain the following background statement:

"Companies are under no obligation to respond to this survey."

The committee shall determine the method of data collection to ensure company confidentiality if required. In the case of anonymous surveys, the names of respondents shall be deleted by the JEDEC Office. The survey shall specify the method of data-collection.

7 JEDEC documents

JEDEC documents are available from the JEDEC website: www.jedec.org. JEDEC documents may not be sold without written authorization from JEDEC.

7.1 Interpretation

Official interpretations involving technical matters pertaining to JEDEC and/or ANSI/JEDEC standards and publications shall be made by the formulating committee of the document in question.

7.2 Document Maintenance

JEDEC documents shall be reviewed by the formulating committee within five years of the last publication date, after which the committee shall take one of the following actions with respect to the standards material:

a) Reaffirm it as a JEDEC document

b) Recommend its revision and reissuance as a JEDEC document

c) Recommend its rescission

d) Recommend its consideration as an ANSI or IEC document proposal.

7.3 Document Types

7.3.1 Standards (JESD)

Documents that are intended to represent a sound approach to product specification and application.

7.3.2 Publications (JEP)

Documents containing general engineering information on products, procedures, or services, that are not necessarily appropriate for standardization.

7.3.3 Specifications (JES)[6]

Documents prepared specifically to facilitate procurement, that clearly and accurately describes the essential technical requirements for purchased material or services.

7.3.4 Registered Outlines/Standards (CO, DO, GS, MO, MS, etc.)

Mechanical package outline drawings that have been registered and assigned a JEDEC registration number.

7.3.5 Registration Data Formats (RDF)

Engineering information in the form of a list of specific electrical and mechanical parameters necessary for the characterization of a particular class of solid state devices.

7.3.6 Manuals (JM)

Documents that describe internal JEDEC policies and procedures.

7.3.7 Joint Documents (J-STD, JP, and JS)

Documents created in cooperation between JEDEC and another organization.

7.3.8 ANSI/JEDEC Standards

At the request of the sponsoring committee and after approval by Board ballot, JEDEC standards and publications may be submitted to ANSI through the JEDEC Office for processing as an ANSI National Standard. The JEDEC Office will be responsible for providing appropriate documentation to ANSI. All policies and procedures set forth by ANSI per the "ANSI Essential Requirements: Due Process Requirements for American National Standards" shall be followed. See Annex D for more details.

[6] This document type has not been in use by JEDEC since early 1990's but is maintained here for historical purposes only.

8 Legal guidelines

All meetings of the JEDEC Board and its associated committees, subcommittees, task groups, and other units shall comply with JEDEC Legal Guidelines incorporated herein by reference. JEDEC Legal Counsel may advise the Board and committees from time to time concerning interpretation of Legal Guidelines.

8.1 JEDEC documents and publications

Prior to publication, the following documents including, but not limited to, all JEDEC standards, publications, manuals, minutes, surveys, questionnaires, press releases, registration data formats, and workshop proceedings, formulated by the Board, committees, and subcommittees, must be approved by JEDEC Legal Counsel.

8.2 Patent Policy

8.2.1 Terms and definitions

Affiliate: An entity owned or controlled by a Committee Member, or which controls or is under common control with a Committee Member for so long as such control exists.

NOTE For purposes of this definition, control means the ownership of greater than 50% of the voting securities of that Committee Member.

Approval by the Committee: An approval by vote of the committee to send a proposed Standard to the Board of Directors for review and approval. Some committees approve proposed Standards in parts, for example, by a "pass-hold" process. In those instances, “Approval by the Committee” means preliminary or final approval of the relevant part of a proposed Standard by a committee vote.

Committee Member: An entity that participates in a JEDEC committee and its Affiliates.

Contribution: Any submitted material, proposal or other submission offered by a Committee Member in the process of developing a Standard for the purpose of incorporating such submitted material, proposal, or other submission into a Standard, provided that such submitted material, proposal, or other submission either, a) exists in a tangible form of expression (including in electronic media); or b) is a verbal statement that is memorialized in written documentation (such as a proposed Standard or submitted material) and is either confirmed or not objected to by such Committee Member within thirty (30) calendar days after its receipt of or access to such memorialization, including without limitation, via posting on the JEDEC website.

8.2.1 Terms and definitions (cont'd)

Disclosure of Potentially Essential Patents (to Disclose Potentially Essential Patents)**:** Disclosure to JEDEC, in writing, in the following form:

a) for issued patents, disclose the patent owner, assignee (if available at time of disclosure) name, address and intellectual property rights ("IPR") contact person; name or title of the patent; the patent number; the country or countries of issuance, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read,

b) for published applications, disclose the patent application owner, assignee (if available at time of disclosure) name, address and IPR contact person; name or title of the patent; the patent application number; the country or countries of filing, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read, and

c) for unpublished pending applications, disclose the name or title of the patent application, the patent application owner or assignee (if available at time of disclosure) name, address and the IPR contact person; the patent application number; the general subject matter of such unpublished application(s) and the Standard(s) on which the submitter of the disclosure believes an Essential Patent claim may read. Nothing herein precludes broader disclosure of unpublished patent applications on a voluntary basis or pursuant to a non-disclosure agreement.

Disclosure of a patent is deemed to include all patents claiming priority of a single filing. The listing of foreign equivalents is optional and at the discretion of the patent holder.

NOTE If any of a Committee Member's disclosed patent or patent application contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, the Committee Member must also note this fact in its disclosure statement.

Essential Patent: A Patent containing one or more Essential Patent Claims.

Essential Patent Claims: Those Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard.

NOTE Essential Patent Claims do not include Patent claims covering aspects that are not required to comply with a JEDEC Standard, or are required only for compliance with sections that are marked "example," "non-normative," or otherwise indicated as not being required for compliance, or related to underlying enabling technologies or manufacturing techniques not specified in the standard.

Participate (Participated, Participation): (a) joining a JEDEC committee or task group involved in the development of or amendments to a Standard; or (b) attending more than one meeting of such committee or task group (in person or by telephone) within a one-year period. "Participate" includes being present at any point in a meeting of a committee or task group even if the individual or entity has not formally joined the committee or task group.

Patents: All classes or types of patents other than design patents (including, without limitation, originals, divisions, continuations, continuations-in-part, extensions or reissues), and applications for these classes or types of patents throughout the world.

Potentially Essential Patent: A Patent that is reasonably believed by a subject person to contain one or more Essential Patent Claims.

8.2.1 Terms and definitions (cont'd)

Potential Licensees: All JEDEC Committee Members and non-members.

RAND: Reasonable and non-discriminatory licensing terms and conditions.

Representative: An individual who represents a Committee Member. The term includes entities that have not formally joined the committee or task group, if they participate.

Standard: Standards include publications and package outlines, provided that they are adopted (or intended to be adopted) by the JEDEC Board of Directors and have the effect of Standards. Standards work includes activities in JEDEC committees and task groups.

NOTE Standards include both proposed and adopted JEDEC technical specifications.

8.2.2 General Provisions

8.2.2.1 Committee Members

All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy ("Patent Policy"). This commitment also applies to entities that Participate in JEDEC Committees or task groups, whether or not they have formally joined as JEDEC members.

All Committee Members, as a condition of committee membership and participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.

The disclosure and licensing obligations of Committee Members and Participants are limited to Standards developed in the particular JEDEC committees in which and while they Participate.

As JEDEC members, Committee Members and Representatives are encouraged, but not required, both to disclose their Potentially Essential Patents and to license their Essential Patent Claims on RAND terms and conditions for Standards developed in all other JEDEC committees in which they are not Committee Members. Such disclosure shall be in the format described in 8.2.3 and be made to the JEDEC Legal Department.

Committee Members and Representatives are encouraged, but not required, to disclose the Potentially Essential Patents of other entities, including other Committee Members and third-parties.

Committee Members and Representatives are encouraged, but not required, to bring Patent Policy issues or concerns with respect to the Disclosure of Potentially Essential Patents and the licensing of Essential Patent Claims to the attention of the JEDEC Board of Directors for resolution, see 9.2.

8.2.2 General Provisions (cont'd)

8.2.2.2 Committees

JEDEC committees and task groups shall not consider any matters or proposals that are outside the approved scope of such committees or task groups. Furthermore, JEDEC committees and task groups are encouraged to use best efforts to avoid proposals for Standards that are within the approved scope of such committees and task groups and that would be likely to cause Committee Members to terminate their membership in the committee or task group for the purpose of discontinuing their disclosure or RAND licensing obligations.

JEDEC committees and task groups shall keep track of all notices, disclosures and licensing assurances with respect to Potentially Essential Patents and to review, on a periodic basis, the list of prior disclosures of Potentially Essential Patent Claims.

JEDEC committees and task groups shall consider reasonable workarounds and technical alternatives (but are not required to implement such workarounds or alternatives) within the earlier of: a) balloting, or b) one-hundred twenty (120) calendar days of receiving Notice of Refusal to offer Licenses on RAND Terms.

JEDEC committees and task groups are encouraged, but not required, to resolve patent policy issues before balloting. Unresolved issues relating to Potentially Essential Patents may be submitted to the JEDEC Board of Directors for resolution, see 9.2. The sole remedy for any issues or concerns about deviations from approved scope shall be an appeal to the JEDEC Board of Directors made prior to Approval by the Committee, see 9.2.

8.2.3 Disclosure of Potentially Essential Patents

At each committee meeting, the chairperson should call to the attention of all those present the requirements contained in the JEDEC Legal Guides and the obligation of all Representatives to inform the committee of any personal knowledge they have of any Potentially Essential Patents that are owned or controlled by that Committee Member and to call for the Disclosure of Potentially Essential Patents by Representatives. Annex A provides information to be displayed at the beginning of the committee meeting to satisfy the requirement. Additionally, all Representatives should be asked to read the statement attached to each JEDEC sign-in/attendance roster; see Annex A for patent policy application guidelines.

All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member to the personal knowledge of the Representatives. However, neither Committee Members nor Representatives shall have any obligation to conduct a search for Potentially Essential Patents.

Disclosure of Potentially Essential Patents by a Representative or the Committee Member being represented shall be made as early as reasonably possible. The Disclosure of Potentially Essential Patents shall be in accordance with the definition of Disclosure of Potentially Essential Patents, see 8.2.1. Initial disclosure by a Committee Member or Representative may be made in a meeting of the committee or task group. The Representative is responsible for ensuring that such disclosure is properly recorded in the meeting minutes.

8.2.3 Disclosure of Potentially Essential Patents (cont'd)

The Representative or Committee Member shall document all known Potentially Essential Patents in either: a) License Assurance/Disclosure Forms, see Annex A.3, or b) Notice of Refusal to offer Licenses on RAND Terms forms, see Annex A.4. Such disclosures or notices of known Potentially Essential Patents shall be delivered to the JEDEC Legal Department within thirty (30) calendar days of Approval by the Committee in order to be effective.

8.2.3.1 Disclosure of unwillingness to license work of a committee

If a Committee Member knows that it would not be willing to offer to license Essential Patent Claims arising from the Contributions of another Committee Member on RAND terms to all Potential Licensees consistent with 8.2.4, the Committee Member shall notify the committee chair in writing as early as reasonably possible but no later than thirty (30) calendar days after Approval by the Committee in the form of a Notice of Refusal to offer Licenses on RAND Terms, see Annex A.4.

The committee shall consider working around the material or other technical alternatives with a goal of resolving the concern if at all possible. The Committee Member may (at its own discretion) withdraw its notification of Refusal to License at any time. However, if the Committee Member wishes to maintain its position that it would refuse to License the work of the committee, the Committee Member must withdraw from the committee no later than one-hundred twenty (120) calendar days after providing notice of its unwillingness to license.

8.2.4 RAND Patent Licensing Commitment

Subject to the terms and conditions of section 8.2.4, each Committee Member, as a condition of Participation, agrees to offer to license on RAND terms, to all Potential Licensees, such Committee Member's Essential Patent Claims for the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard issued during the period of membership in that committee. The licensing commitment does not apply to Essential Patents of a Committee Member where notice of a Refusal to License has been given by the Committee Member in accordance with 8.2.3.1.

This commitment applies to any Standard that was pending in the committee or task group while the Committee Member Participated in that committee or task group. If a Committee Member terminates its committee membership, the commitment does not apply with respect to any new proposal or Standard introduced in the committee or task group after the Committee Member provided notice to the JEDEC Legal Department terminating its committee membership. If and as necessary, questions whether or not a particular proposal is a new Standard or merely a continuation of a prior Standard will be addressed in the first instance by the JEDEC Legal Department in accordance with 8.2.10.

Certain exceptions apply to the licensing requirement. A Committee Member will not be required to license or continue to license its Essential Patent Claims to a Potential Licensee for a particular Standard if: (i) such Potential Licensee does not agree to grant a license to all other Potential Licensees under such Potential Licensee's Essential Patent Claims of that Standard on RAND terms and conditions for the approved Standard and/or (ii) such Potential Licensee has commenced or has threatened to commence patent litigation targeting such Committee Member's products that are meant to comply with that Standard.

8.2.5 Licensing Assurance/Disclosure Form

A Committee Member or Representative agrees to offer the following licensing options for an Essential Patent Claim:

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:

(i) A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; *or*

(ii) A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[7], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form (see Annex A.3) at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.

8.2.6 Reference to patented products in JEDEC standards and publications

The following notice shall be included inside the front cover of all JEDEC Standards in which Essential Patent Claims are or may be involved:

> "The user's attention is called to the possibility that compliance with this document may implicate the use of an invention covered by patent rights."

> "By publication of this document, no position is taken with respect to the infringement or validity of any patents. However, JEDEC has received statements of a willingness to offer to license certain rights on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from JEDEC."

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[7] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

8.2.7 Special legal disclaimer

The Board has the discretion to approve the issuance of a standard for which a patent owner or applicant has not provided written assurance that the Essential Patent Claims will be licensed, subject to special legal disclaimers.

When determining whether to approve the issuance of such a standard, the Board shall consider whether the committee used diligent efforts, if appropriate under the circumstances, to develop a standard that does not require the use of the Essential Patent Claim(s).

A special legal disclaimer might include the following language:

> "Notice: JEDEC has received information that certain patents or patent applications may be essential to this standard. However, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided. JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Anyone making use of the standard assumes all liability resulting from such use. JEDEC and its members disclaim any representation or warranty, express or implied, relating to the standard and its use."

If the Board determines that:

(1) the claim by the patent owner or applicant that an identified patent or patent application may be essential to implement a Standard is a reasonable claim, and

(2) there is a credible indication that the patent owner or applicant is unwilling or unable to grant licenses, with or without compensation, on RAND terms,

then the Board *shall not* approve the issuance of the standard except as provided in 8.2.7. In its discretion, the Board may seek the advice of an independent outside patent attorney or consultant in making the determinations in subsections (1) and/or (2) of 8.2.7.

8.2.8 Miscellaneous

The Patent Policy applies equally to situations involving the Essential Patent Claims that are discovered after adoption of the Standard.

JEDEC makes no representation as to the reasonableness of any terms or conditions of the license agreements offered by such patent rights holders, and all negotiations regarding such terms and conditions must take place between the individual parties outside the context of JEDEC.

To the extent that Potentially Essential Patent Claims are disclosed with respect to a JEDEC Standard, information regarding the parties who have asserted patent rights in the Standard may be obtained from the JEDEC Corporate Office.

It is possible that other patent rights that have not been disclosed to JEDEC may be implicated by implementation of or compliance with a JEDEC Standard. JEDEC is not responsible for identifying patent claims for which a license may be required in order to implement a JEDEC Standard, and takes no position and conducts no inquiries with respect to the legal validity or scope of those patents or patent claims that are brought to its attention.

8.2.9 Violations

If a Committee Member or Representative materially violates this Patent Policy and the violation is not cured within thirty (30) days following notification of the violation by the JEDEC Corporate Office, the JEDEC Board of Directors may in its discretion suspend the Committee Member or Representative's right to participate in JEDEC. If the Committee Member is allowed to continue participation and engages in another material violation of this Policy, the JEDEC Board of Directors may in its discretion revoke the Committee Member or Representative's right to participate in JEDEC.

8.2.10 Interpretation and Governing Law

The obligations and rights of parties to this agreement in the conduct of committee meetings and the approval of standards as set forth in this Patent Policy will be interpreted in the first instance by the JEDEC Legal Department. When specifically requested by a Committee Member or Representative, interpretations by the Legal Department will be in writing.

Written interpretations by the Legal Department can be appealed by a Committee Member or Representative to the JEDEC Board of Directors. The Board of Directors will make a final decision on appeal, as determined in their reasonable and good faith judgment. The final decision will be in writing.

In no event will JEDEC or the JEDEC Board make a determination that a Patent is or is not a Potentially Essential Patent or that a Patent Claim is or is not an Essential Patent Claim.

The Patent Policy will be interpreted and governed under the laws of the State of New York.

9 Appeals

All appeals related to standard or publication development are initially directed to the JEDEC Office. The provision for appeals is important for the protection of all parties involved within the JEDEC standards development process. An appeals mechanism safeguards both those who are directly and or materially affected by the process and the standards developing organization.

9.1 Appeals related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process for the development of ANSI/JEDEC standards and publications.

9.1.1 Right of appeal

Persons who have directly and or materially affected interests and who have been or will be adversely affected by a standard or publication within ANSI jurisdiction have the right to appeal substantive or procedural actions or inactions of JEDEC formulating groups.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

9.1.2 Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

a) Appeals shall be addressed promptly and a decision made expeditiously;
b) The right of the involved parties to present their cases shall not be denied;
c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;
d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and
e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials. The fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available.

9.1.3 Appeals procedures

The following subsections outline the JEDEC Appeals Procedures. In the case of an appeal to ANSI of a JEDEC action or inaction on an ANSI/JEDEC standard, the appellant may waive the right of the JEDEC appeals process, see 9.1.4.

9.1.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.1.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent (formulating group chairman or JEDEC representative) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge. Complaints that are technical in nature shall be referred to the appropriate JEDEC formulating committee having jurisdiction over the material for review and possible action. Complaints that are procedural in nature shall be referred to the JEDEC Board for review and possible action.

9.1.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 15 calendar days, the JEDEC Office shall schedule a hearing with an appeals panel* on a date agreeable to all participants but within 30 calendar days, giving at least 10 calendar days' notice. Hearing on the complaint will take place at the next regular meeting of the JEDEC formulating committee or the JEDEC Board depending on the nature of the complaint.

NOTE In the case of an ANSI appeal, see Annex D.10 for clarification of an appeals panel.

9.1.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.1.3.5 Decision

The appeal disposition shall be documented by the formulating committee for technical matters and by the JEDEC Board for procedural matters. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

NOTE In the case of an ANSI appeal, the appeals panel shall render its decision in writing within 30 days of the hearing, based upon a preponderance of the evidence, stating its findings of fact and conclusions, with reasons therefore and citing the evidence. The Committee Secretary shall notify the appellant and the Committee of the decision of the appeals panel, which shall be binding and final on all concerned.

If, for whatever reason(s), the appellant chooses to forego the process detailed above, the JEDEC Office shall maintain all documents pertaining to JEDEC attempts to resolve the matter at hand. These documents may be used in any further appeals proceedings.

9.1.4 Further appeal

If the matter under appeal relates to a JEDEC Standard that has been or is expected to be recognized as an American National Standard, subsequent further appeal may be made directly to ANSI. If the appellant gives notice to the JEDEC Office that further appeal to ANSI is intended, a full record of the complaint, response and decision shall be submitted by the JEDEC Office to ANSI.

NOTE ANSI will not normally hear an appeal of an action or inaction by JEDEC until the appeals process has been completed. Such appeals shall be directed to ANSI in accordance with the procedures of the appropriate ANSI entity (e.g., Board of Standards Review, Executive Standards Council, etc.).

9.2 Appeals not related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process that are not related to the development of ANSI/JEDEC standards and publications.

9.2.1 Right of appeal

Committee Members or Participants who have directly and or materially affected interests and who have been or will be adversely affected by the activities of another Committee Member or Representative, a JEDEC committee, or a JEDEC standard or publication have the right to appeal technical or procedural actions or inactions.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

9.2.2 Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

a) Appeals shall be addressed promptly and a decision made expeditiously;

b) The right of the involved parties to present their cases shall not be denied;

c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;

d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and

e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials.

9.2.3 Appeals procedures

The following subsections outline the JEDEC Appeals Procedures for appeals that are not related to ANSI/JEDEC standards and publications.

9.2.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the Standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.2.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent(s) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge.

Complaints that are technical in nature shall be referred to the appropriate JEDEC committee having jurisdiction over the material for review and possible action. Complaints that are non-technical or procedural in nature shall be referred to the JEDEC Board for review and possible action. Complaints that relate to the patent policy shall be referred to the JEDEC Board for review and possible action.

9.2.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 30 calendar days, the JEDEC Office shall schedule a hearing with an impartial appeals panel consisting of three individuals appointed by the committee or the JEDEC Board, as appropriate, on a date agreeable to all parties, giving at least 10 calendar days' notice. Hearing on the complaint will take place in person or by telephone.

9.2.3 Appeals procedures (cont'd)

9.2.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.2.3.5 Decision

The appeal disposition shall be documented by the JEDEC appeals panel. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

Appeal dispositions on complaints that are technical in nature may be further appealed to the appropriate JEDEC committee. Appeal dispositions on complaints that are non-technical or procedural in nature may be further appealed to the JEDEC Board of Directors.

10 External publicity

All articles, presentations, news releases, or other publicity must be approved by JEDEC Legal Counsel prior to release.

Articles, speeches, and other presentations for publication or delivery by members of the Board, its committees, or JEDEC staff that cover specific JEDEC work or JEDEC policy or purports to speak on behalf of JEDEC must be approved by the Board, if time permits; otherwise by the Board chairperson who shall be responsible for ensuring that the content is accurate and reflects current JEDEC policy. Any publicity that speaks for the Board shall require similar approval.

The committee chairperson may talk to the press and approve technical and tradeshow presentations about ongoing committee work when it is appropriate to promote a particular standard or the work of the committee. This public disclosure should be limited to the goal of the standard under development and any details of the standard that have been approved by committee ballot(s).

Companies may not advertise or give press releases stating that their products comply with a JEDEC standard, publication, or registration prior to Board approval of the documents.

11 JEDEC ethics rules for electronic communications

No JEDEC member or alternate shall post to an e-mail reflector, bulletin board, or Web site owned or sponsored by JEDEC, any of the following:

a) any advertising or marketing information,

b) any cost or pricing information,

c) any proprietary information,

d) any non-JEDEC copyright information or material that is in excess of that allowed under current USA copyright laws,

e) any technical information that requires a USA government export license before it is transferred outside of the United States,

f) information covered by USA secrecy laws,

g) solicitations, or requests for contributions to “for profit” or “non-profit” (charitable) organizations,

h) chain letters,

i) job search or hiring information,

j) computer games or other software products,

k) files with known software viruses,

l) offensive material covering:

   1) libel (i.e., false or malicious statements),

   2) threats, retaliation, or intimidation,

   3) use of language that is obscene or in poor taste, including jokes,

   4) sexual harassment or inappropriate sexual content, such as pictures, images, messages, or cartoons,

   5) discriminatory communication relating to race, color, national origin, sex, marital status, sexual orientation, age, veteran’s status, disability, religious or political beliefs.

All electronic communications and posting must comply with this JEDEC Manual and the JEDEC Legal Guides.

Annex A (normative) Legal guidelines summary

A.1 JEDEC patent policy summary

- All JEDEC Member Companies and their Representatives agree to abide by the JEDEC patent policy.
- The commitment applies to all entities, including non-committee members, that have a Representative present at any point in a meeting of a JEDEC Committee or Task Group.
- The commitment continues as long as the Committee Member or Representative is a member of or a participant in a particular JEDEC Committee.
- For the purposes of the patent policy, "Committee" refers to the full committee, except for those committees that have subcommittees. In that context, “committee” refers to any group that has a separate scope.
- All companies and their representatives are required to disclose all known Potentially Essential Patent Claims owned or controlled by the company.
- No company has a duty to conduct a search for Potentially Essential Patent Claims.
- All companies, as a condition of committee membership or participation, agree to license their Essential Patent Claims on RAND terms and conditions.
- The licensing assurance must indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee, and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.
- If a Member Company knows it would be unwilling to license its Essential Patent Claims on RAND terms, the member must notify the committee chair and withdraw from the committee within 120 days after giving the notice. This option is not available to a Member Company with respect to its own Contribution.
- Companies and their representatives are required to use a standard form for the disclosures and assurances.
- The disclosure and licensing obligations of companies and their representatives are limited to Standards developed in the particular JEDEC committees in which they are members or in which they participate.
- The obligations apply to all entities, including non-committee members, that have a representative present at any point in a meeting of a JEDEC Committee or Task Group.
- Member Companies and their Representatives are strongly encouraged to review their current committee and subcommittee assignments, and ensure they are prepared to accept the commitments defined by the patent policy.

See, 8.2 for additional information.

A.2 Copyright material

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, it shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

A.3 License Assurance/Disclosure Form (See 8.2.3 and 8.2.5 of the JEDEC Patent Policy)

For the electronic version of the License Assurance/Disclosure Form go to: http://www.jedec.org/sites/default/files/License_Assurance-Disclosure_Form_20150710.pdf

Part 1

Date: _____

Entity Name: _____

Address: _____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

Part 2

Identify the relevant JEDEC Standard:

_____

_____

Part 3

For Issued Patents:

Patent No: _____

Patent Name or Title: _____

Country of Issuance: _____

For Published Patent Applications:

Published Patent Application No. :_____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

_____

_____

A.3 License Assurance/Disclosure Form (cont'd)

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

Part 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

___ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

___ (ii) A license will be offered, with compensation, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[8], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

[8] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 of the JEDEC Patent Policy are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

A.3 License Assurance/Disclosure Form (cont'd)

Part 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

_____
(Signature)

_____
(Name printed)

_____
(Date)

NOTE The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

A.4 Notice of Refusal to Offer Licenses on RAND Terms

Part 1

Date: _____

Committee Member: _____

Entity Mailing Address: _____

IPR Contact Name: _____

IPR Contact Telephone Number: _____

IPR Contact E-Mail Address: _____

Part 2

Identify the relevant JEDEC Standard:

_____

Part 3

Pursuant to 8.2.3.1 of the JEDEC Patent Policy, the Committee Member hereby provides notice that the Committee Member is not willing to offer a license on RAND terms to the Potentially Essential Patents identified in A.4, Part 4.

Part 4

For Issued Patents (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Patent Name or Title: _____
3. Patent Number: _____
4. Country of Issuance: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

   _____

For Published Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Published Patent Application Number: _____
3. Patent Application Name or Title: _____
4. Country of Filing: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

   _____

   _____

A.4 Notice of Refusal to Offer Licenses on RAND Terms (cont'd)

For Unpublished Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. General Subject Matter of Patent Application: _____
   _____
   _____
3. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:
   _____

Part 5

By signing this Notice, the IPR Contact represents that they are authorized to complete and submit this Notice on behalf of the Committee Member. Pursuant to Section 8.2.3.1 of the JEDEC Patent Policy, the IPR Representative represents that the information provided in this Notice does not include a contribution that was contributed by the Committee Member. If the Committee Member becomes aware of any other Potentially Essential Patent not already covered by a Notice and the ballot period is open, then the Committee Member may submit additional Notices.

_____
Signature of IPR Contact

Accepted and Agreed to:

_____
JEDEC

_____

Date Accepted: _____

RETURN THE COMPLETED NOTICE BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

Annex B (informative) Patent policy application guidelines

The following points describe the application of the JEDEC patent policy:

B.1 Committee discussion of pending or existing patents is a permissible activity and is encouraged when the committee feels that the patented item or process represents the best technical basis for a standard.

B.2 Discussion of a pending or existing patent does not constitute an acknowledgment of the validity of the patent, because validity is based on prior art and determination of the company/individual that first made the invention or applied for the patent. The committee's concern is only with the technical merits of the patent and whether the technical proposal is a sound basis for standardization.

B.3 By its terms, the JEDEC patent policy applies with equal force to situations involving:

a) the discovery of patents that may be required for use of a standard subsequent to its adoption, and

b) the initial issuance of a patent after the adoption of a standard.

Once disclosure is made, the holder is obligated to provide the same assurances to JEDEC as are required in situations where patents exist or are known prior to approval of a proposed standard.

Thus, if notice is given of a patent that may be required for use of an already approved JEDEC standard, a standards developer may wish to make it clear to other standards-making participants that the JEDEC procedures require the patent holder to provide the assurances contained in the patent policy or suffer the withdrawal of JEDEC's approval of the document as a JEDEC standard.

Annex C (normative) ANSI Standardization Procedures

For those documents that are intended for publication as an American National Standard (ANS), the provisions set forth in this annex apply.

C.1 Notification of American National Standards (ANS) development

Notification of American National Standards activity shall be announced in suitable media as appropriate to demonstrate provision of opportunity for participation by all directly and materially affected persons. At the initiation of a project to develop or revise a Standard, notification shall be transmitted to ANSI using the Project Initiation Notification System (PINS) form, or its equivalent, for listing in Standards Action. A PINS form may be submitted, but is not required, at the initiation of a project to reaffirm or withdraw a Standard. Prompt consideration shall be given to the written views and objections of all participants, including those commenting on the PINS announcement. Comments resulting from the filing of PINS will be handled in accordance with the ANSI Essential Requirements, 2.5.

C.2 Submission to ANSI for public review

Following approval of the standard, responsible JEDEC Standards staff shall submit the proposed ANS to ANSI to initiate public review. JEDEC Standards staff shall provide appropriate documentation to ANSI. Responsible JEDEC Standards staff shall receive, collect and acknowledge receipt of public review comments. In addition, responsible JEDEC Standards staff shall forward all public review comments to the formulating group for review and response. The response to each commenter shall include a notation of the JEDEC and ANSI appeals process.

NOTE A proposed ANS is subject to comment only (not for vote) during public review and by any and all materially or directly affected parties.

C.3 Public review comments

JEDEC Standards staff shall acknowledge receipt of a public review comment, regardless of its nature. The only comments normally addressed by a working group or formulating group are editorial or technical in nature. Technical comments should be accompanied with wording that would aid the formulating group in addressing the comments.

Other comments may be handled in the following manner on behalf of the formulating group:

- The JEDEC Legal Counsel shall respond to comments relating to legal concerns;
- JEDEC Standards staff shall respond to comments relating to concerns regarding the standards development process;
- The formulating group with input from JEDEC staff shall address scope concerns;
- The reason for non-acceptance shall be sent regarding editorial or technical concerns;
- Vague comments shall be returned to the respondent requesting expeditious clarification.

JEDEC Standards staff shall retain copies of response to comments.

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.4 Public review commenter response

The commenter shall have 14 calendar days after response to acknowledge the acceptance or rejection of that reply. If no response is received, the responsible JEDEC Standards staff shall send a reminder notice to the commenter requesting response. If no response is received within an additional 5 calendar days, the responsible JEDEC Standards staff will send a registered letter to the commenter noting the lack of response. The commenter's comments are then recorded as unresolved and circulated to the formulating group per the provisions of C.3.

All correspondence showing the formulating group's effort to address the comments, noting a lack of response when appropriate, shall be included in any package of materials provided to ANSI.

C.5 Results scenarios

Results scenario #1: If no comments are received after the close of public review, the document shall be forwarded to ANSI with a request for approval.

Results scenario #2: If editorial comments are received by the close of public review, the document editor, editing group, or chair shall address the comments. The document, with edits, if any, shall be forwarded to ANSI for approval.

Results scenario #3: If substantive comments are received from public review, the working group or formulating group shall review these comments, and attempt to resolve them, and notify each commenter of said action (see C.4), along with a notification of the JEDEC and ANSI appeals process.

a) If no substantive changes are made, the document is forwarded to ANSI for approval.

b) If substantive changes are made, the formulating group shall conduct a recirculation vote/ballot and "second" public review (see C.4).

c) If negative, substantive comments remain unresolved from public review, the formulating group shall conduct a recirculation vote/ballot, and, if necessary, a "second" public review (see C.4).

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.6 Voting on an American National Standard

When a vote in a formulating group is for the purpose of approving a document for publication as an American National Standard, a Ballot Summary (Tally of votes) shall be prepared and included in the minutes. The Interest Category is normally self-selected by the voting member.

Action Required	Method (all calendar days)	Approval Criteria
Meeting Vote*	At the meeting	Two-thirds voting
Ballot	30 day ballot	Two-thirds voting
ANSI BSR8 (Public review)	Initial 60 day comment period [30 or 60 day subsequent comment period(s)] (or other ANSI designated time period where applicable)	Comments addressed by formulating group

* Voting members not present at the time of the vote shall be given the opportunity to vote on the standard after the meeting. The JEDEC staff shall notify the absent voting members via e-mail of any substantive changes made to the standard subsequent to the 21 day ballot period and advise that they have 7 days to cast their vote via the JEDEC Voting Machine. Any absent voting members that fail to respond shall be listed as No Response on the final submittal for approval to ANSI. Response to this opportunity to vote shall not be considered as attendance at the meeting for purposes of voting maintenance.

C.7 Legal approval

All ANSI/JEDEC standards shall receive JEDEC legal approval before publication.

C.8 ANSI approval

If ANSI/BSR is approved, responsible JEDEC Standards staff is notified and in turn publishes the document.

If ANSI/BSR does not approve, comment resolution issues will be dealt with by the formulating group and process-related issues will be dealt with by JEDEC Standards staff. If the ANSI/BSR comments are resolved and the document is approved, responsible JEDEC Standards staff publishes the document.

If the comments cannot be resolved, the document is returned to the formulating group for further resolution or cancellation. The formulating group may appeal the actions of the ANSI/BSR.

C.9 ANSI patent policy

If a JEDEC standard is intended for an American National Standard, then the standard must comply with the current ANSI patent policy.

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.10 Appeals panel (for an appeal of an ANS)

In the case of an ANSI appeal, the appeals panel shall consist of three individuals who have not been directly involved in the matter in dispute, and who (knowingly in good faith) will not be materially or directly affected by any decision made or to be made in the dispute. At least two members shall be acceptable to the appellant and at least two members shall be acceptable to JEDEC. In the event the appellant does not wish to select a panelist or a third panelist cannot be agreed upon, JEDEC shall appoint this individual to the panel in order to hold a hearing.

C.11 ANSI Commercial Terms and Conditions

Provisions involving business relations between buyer and seller such as guarantees, warranties, and other commercial terms and conditions shall not be included in an ANS.

Annex D (informative) Differences between revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JM21T, compared to its predecessor, JM21S (November 2015). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	**Description of Change**
1.4.4	4), Removed "within a calendar year" from 1st sentence, removed "Participation via teleconference is allowed only once per calendar year" and replaced with ". It is the expectation that Directors attend all Board meetings, at minimum Directors must attend at least one face-to-face Board meeting, in person, each calendar year." (JCB-19-27)
3.5	Quorum: Changed "20" to "12". (JCB-19-04)
1.4.3.3	Changed to 1.4.3.4. (JCB-20-14)
1.4.3.3	New subclause added. (JCB-20-14)
8.2.1	New term and definition added for "Approval by the Committee". (JCB-20-15)
8.2.2.2	4th paragraph, last sentence, modified as follows: The sole remedy for any issues or concerns about deviations from approved scope shall be an appeal to the JEDEC Board of Directors made prior to ~~approval of the subject draft specification for resolution~~ Approval by the Committee, see 9.2. (JCB-20-15)
8.2.3	4th paragraph, last sentence, modified as follows: Such disclosures or notices of known Potentially Essential Patents shall be delivered to the JEDEC Legal Department within thirty (30) calendar days of ~~draft specification completion~~ Approval by the Committee in order to be effective. (JCB-20-15)
8.2.3.1	1st paragraph, modified as follows: … reasonably possible but no later than thirty (30) calendar days after ~~completion of the draft specification~~ Approval by the Committee in the form of a Notice of Refusal to offer Licenses on RAND Terms, see Annex A.4. (JCB-20-15)

D.1 Differences between JM21S and JM21R (July 2015)

Clause	**Description of Change**
3.4	2nd para., 1st sentence modified as follows: A JEDEC staff member or a designated alternate must ~~be in attendance at~~ participate in every committee meeting, either in person or by electronic means.

JEDEC®

JS 44 (Rev. 06/17)

CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. *(SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)*

I. (a) PLAINTIFFS

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG SEMICONDUCTOR, INC. and SAMSUNG ELECTRONICS AMERICA, INC.

(b) County of Residence of First Listed Plaintiff _____
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorneys *(Firm Name, Address, and Telephone Number)*
Rodger D. Smith, II, Esquire; Morris, Nichols, Arsht & Tunnell LLP
1201 North Market Street, Wilmington, DE 19801
(302) 658-9200

DEFENDANTS

NETLIST, INC.

County of Residence of First Listed Defendant _____
(IN U.S. PLAINTIFF CASES ONLY)

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

Attorneys *(If Known)*

II. BASIS OF JURISDICTION *(Place an "X" in One Box Only)*

- ❒ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question *(U.S. Government Not a Party)*
- ❒ 2 U.S. Government Defendant
- ❒ 4 Diversity *(Indicate Citizenship of Parties in Item III)*

III. CITIZENSHIP OF PRINCIPAL PARTIES *(Place an "X" in One Box for Plaintiff and One Box for Defendant)*
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	❒ 1	❒ 1	Incorporated *or* Principal Place of Business In This State	❒ 4	❒ 4
Citizen of Another State	❒ 2	❒ 2	Incorporated *and* Principal Place of Business In Another State	❒ 5	❒ 5
Citizen or Subject of a Foreign Country	❒ 3	❒ 3	Foreign Nation	❒ 6	❒ 6

IV. NATURE OF SUIT *(Place an "X" in One Box Only)*

Click here for: Nature of Suit Code Descriptions.

CONTRACT
- ❒ 110 Insurance
- ❒ 120 Marine
- ❒ 130 Miller Act
- ❒ 140 Negotiable Instrument
- ❒ 150 Recovery of Overpayment & Enforcement of Judgment
- ❒ 151 Medicare Act
- ❒ 152 Recovery of Defaulted Student Loans (Excludes Veterans)
- ❒ 153 Recovery of Overpayment of Veteran's Benefits
- ❒ 160 Stockholders' Suits
- ❒ 190 Other Contract
- ❒ 195 Contract Product Liability
- ❒ 196 Franchise

REAL PROPERTY
- ❒ 210 Land Condemnation
- ❒ 220 Foreclosure
- ❒ 230 Rent Lease & Ejectment
- ❒ 240 Torts to Land
- ❒ 245 Tort Product Liability
- ❒ 290 All Other Real Property

TORTS

PERSONAL INJURY
- ❒ 310 Airplane
- ❒ 315 Airplane Product Liability
- ❒ 320 Assault, Libel & Slander
- ❒ 330 Federal Employers' Liability
- ❒ 340 Marine
- ❒ 345 Marine Product Liability
- ❒ 350 Motor Vehicle
- ❒ 355 Motor Vehicle Product Liability
- ❒ 360 Other Personal Injury
- ❒ 362 Personal Injury - Medical Malpractice

PERSONAL INJURY
- ❒ 365 Personal Injury - Product Liability
- ❒ 367 Health Care/ Pharmaceutical Personal Injury Product Liability
- ❒ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ❒ 370 Other Fraud
- ❒ 371 Truth in Lending
- ❒ 380 Other Personal Property Damage
- ❒ 385 Property Damage Product Liability

CIVIL RIGHTS
- ❒ 440 Other Civil Rights
- ❒ 441 Voting
- ❒ 442 Employment
- ❒ 443 Housing/ Accommodations
- ❒ 445 Amer. w/Disabilities - Employment
- ❒ 446 Amer. w/Disabilities - Other
- ❒ 448 Education

PRISONER PETITIONS

Habeas Corpus:
- ❒ 463 Alien Detainee
- ❒ 510 Motions to Vacate Sentence
- ❒ 530 General
- ❒ 535 Death Penalty

Other:
- ❒ 540 Mandamus & Other
- ❒ 550 Civil Rights
- ❒ 555 Prison Condition
- ❒ 560 Civil Detainee - Conditions of Confinement

FORFEITURE/PENALTY
- ❒ 625 Drug Related Seizure of Property 21 USC 881
- ❒ 690 Other

LABOR
- ❒ 710 Fair Labor Standards Act
- ❒ 720 Labor/Management Relations
- ❒ 740 Railway Labor Act
- ❒ 751 Family and Medical Leave Act
- ❒ 790 Other Labor Litigation
- ❒ 791 Employee Retirement Income Security Act

IMMIGRATION
- ❒ 462 Naturalization Application
- ❒ 465 Other Immigration Actions

BANKRUPTCY
- ❒ 422 Appeal 28 USC 158
- ❒ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- ❒ 820 Copyrights
- ☒ 830 Patent
- ❒ 835 Patent - Abbreviated New Drug Application
- ❒ 840 Trademark

SOCIAL SECURITY
- ❒ 861 HIA (1395ff)
- ❒ 862 Black Lung (923)
- ❒ 863 DIWC/DIWW (405(g))
- ❒ 864 SSID Title XVI
- ❒ 865 RSI (405(g))

FEDERAL TAX SUITS
- ❒ 870 Taxes (U.S. Plaintiff or Defendant)
- ❒ 871 IRS—Third Party 26 USC 7609

OTHER STATUTES
- ❒ 375 False Claims Act
- ❒ 376 Qui Tam (31 USC 3729(a))
- ❒ 400 State Reapportionment
- ❒ 410 Antitrust
- ❒ 430 Banks and Banking
- ❒ 450 Commerce
- ❒ 460 Deportation
- ❒ 470 Racketeer Influenced and Corrupt Organizations
- ❒ 480 Consumer Credit
- ❒ 490 Cable/Sat TV
- ❒ 850 Securities/Commodities/ Exchange
- ❒ 890 Other Statutory Actions
- ❒ 891 Agricultural Acts
- ❒ 893 Environmental Matters
- ❒ 895 Freedom of Information Act
- ❒ 896 Arbitration
- ❒ 899 Administrative Procedure Act/Review or Appeal of Agency Decision
- ❒ 950 Constitutionality of State Statutes

V. ORIGIN *(Place an "X" in One Box Only)*

- ☒ 1 Original Proceeding
- ❒ 2 Removed from State Court
- ❒ 3 Remanded from Appellate Court
- ❒ 4 Reinstated or Reopened
- ❒ 5 Transferred from Another District *(specify)*
- ❒ 6 Multidistrict Litigation - Transfer
- ❒ 8 Multidistrict Litigation - Direct File

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing ***(Do not cite jurisdictional statutes unless diversity)***:
28 U.S.C. § 2201 et seq., 35 U.S.C. § 271 and 35 U.S.C. § 285

Brief description of cause:
Declaratory Judgment for Patent Non-Infringement

VII. REQUESTED IN COMPLAINT:

❒ CHECK IF THIS IS A **CLASS ACTION** UNDER RULE 23, F.R.Cv.P.

DEMAND $

CHECK YES only if demanded in complaint:
JURY DEMAND: ☒ Yes ❒ No

VIII. RELATED CASE(S) IF ANY

(See instructions): JUDGE Jennifer L. Hall DOCKET NUMBER 21-1453, 23-1122, 24-614, 25-626,

DATE 11/11/2025

SIGNATURE OF ATTORNEY OF RECORD /s/ Rodger D. Smith II

FOR OFFICE USE ONLY

RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____