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Application Number	Unassigned
Filing Date	August 19, 2015
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Title	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
Art Unit	
Examiner Name	
Attorney Docket Number	3304.001B

SIGNATURE of Applicant or Patent Practitioner

Signature	/Kevin P. Radigan, Esq./	Date (Optional)	August 19, 2015
Name	Kevin P. Radigan, Esq.	Registration Number	31,789
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	TETRASUN, INC.		

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☑ *Total of one (1) forms are submitted.

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

TETRASUN, INC.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

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SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Mark Widmar	Date (Optional)	4/20/15
Name	Mark Widmar		
Title	Director		

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	Application Number	
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

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	1	6194763	B1	2001-02-27	Hisamoto et al.	
	2	6924179	B2	2005-08-02	Oh et al.	
	3	7202143	B1	2007-04-10	Naseem et al.	
	4	6210991	B1	2001-04-03	Wenham et al.	
	5	5665607	A	1997-09-09	Kawama et al.	
	6	6821875	B1	2004-11-23	Wenham et al.	

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	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

	1	20080001169	A1	2008-01-03	Lochtefeld	
	2	20060213548	A1	2006-09-28	Bachrach et al.	
	3	20080072959	A1	2008-03-27	Chen et al.	
	4	20030136440	A1	2003-07-24	Machida et al.	
	5	20070295399	A1	2007-12-27	Carlson, David E.	
	6	20080311697	A1	2008-12-18	Reber, Stefan	
	7	20100105190	A1	2010-04-29	Ferre i Tomas, Rafel	
	8	20090178711	A1	2009-07-16	Joo et al.	
	9	20100136768	A1	2010-06-03	Biro et al.	
	10	20100227431	A1	2010-09-09	Rana, Virendra V.	
	11	20120055547	A1	2012-03-08	Schultz-Wittmann et al.	

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	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

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	1	JP2003-298078	JP	A	2003-10-17	EBARA Corp.	English Abstract Only	☒
	2	JP2006-128630	JP	A	2006-05-18	Sanyo Electric Co., Ltd.	English Abstract Only	☒
	3	WO2007/125903	WO	A1	2007-11-08	Fukushima et al.	English Abstract Only	☒
	4	WO2008/028625	WO	A2	2008-03-13	Biro et al.	English Abstract Only	☒
	5	WO2008115814	WO	A2	2008-09-25	Carlson et al.	English Document	☒

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	SCHULTZ, O. et al., "Deielctric Rear Surface Passivation for Industrial Multicrystalline Silicon Solar Cells", 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, Vol. 1, May 7-12, 2006 (pages 885-889).	☐
	2	DeWOLF, S. et al., "Surface Passivation Properties of Boron-Doped Plasma-Enhanced Chemical Vapor Deposited Hydrogenated Amorphous Silicon Films on P-Type Crystalline Si Substrates", Applied Physics Letters, Vol. 88, Issue 2, January 2006 (1 page; Abstract Only).	☐

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	Application Number	
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

	3	TUCCI, M. et al., "Laser Fired Back Contact for Silicon Solar Cells", Thin Solid Films, Vol. 516, Issue 20, Auugst 30, 2008 (1 page; Abstract Only).	☐
	4	BAU et al, "Application of PECVD-SiC as Intermediate Layer in Crystalline Silicon Thin-Film Solar Cells", 3rd World Conference on Photovoltaic Energy Conversion (2003).	☐
	5	SCHULTZ-WITTMANN et al., International Search Report for PCT/US2010/031869, dated August 18, 2010 (4 pages).	☐
	6	SCHUTLZ-WITTMANN et al., Patent Examination Report No. 1, for Australian Patent Application No. AU2010-239265, dated August 19, 2013 (4 pages).	☐
	7	SCHULTZ-WITTMANN et al., Examination Report No. 2 for Australian Application No. AU2010-239265, dated January 22, 2014 (3 pages).	☐
	8	SCHULTZ-WITTMANN et al., Patent Examination Report No. 3 for Australian Patent Application No. AU2010-239265, dated March 6, 2014 (3 pages).	☐

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2015-08-19
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

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The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-298078
(43)Date of publication of application : 17.10.2003

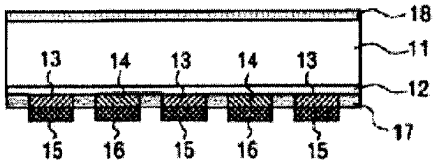
(51)Int.Cl. H01L 31/04

(21)Application number : 2002-096229
(22)Date of filing : 29.03.2002

(71)Applicant : EBARA CORP
(72)Inventor : MISHIMA TAKAHIRO
ISHIKAWA NAOKI

(54) PHOTOELECTROMOTIVE ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a photoelectromotive element such as a solar cell or the like that is superior in electric characteristics such as power generation efficiency or the like, by adopting a low-temperature process to keep a semiconductor substrate with a long carrier life time and high quality.
SOLUTION: A rear-side joint type solar cell is provided with a PN joint and an electrode on the opposite surface to the light incident surface of a semiconductor substrate 11, and it is also provided with an intrinsic semiconductor film 12 of ≥0.1 nm and ≤50 nm in thickness, P- an N-type conductive semiconductor layers 13 and 14 thereon, and electrodes 15 and 16 thereon, on the entire surface with the PN joint.



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Page 9

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2003－298078
（P2003－298078A）
(43)公開日　平成15年10月17日(2003.10.17)

(51)Int.Cl.[7]	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　31/04		Ｈ０１Ｌ　31/04	Ａ　５Ｆ０５１

審査請求　未請求　請求項の数９　ＯＬ　（全 6 頁）

(21)出願番号　特願2002－96229(P2002－96229)

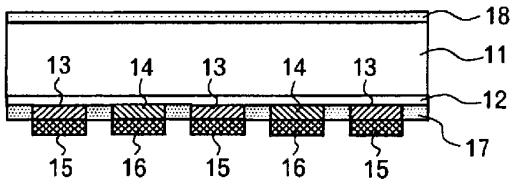
(22)出願日　平成14年３月29日(2002.3.29)

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(74)代理人　100091498
弁理士　渡邉　勇　（外３名）

Ｆターム(参考)　5F051 AA02 AA03 AA04 AA05 CA05
CA14 DA03 DA07 DA20 HA03

(54)【発明の名称】　光起電力素子

(57)【要約】
【課題】　低温処理プロセスを用いることで、大きなキャリアライフタイムを有する高品質な半導体基板の状態を維持し、これにより発電効率等の電気的特性に優れた太陽電池等の光起電力素子を提供する。
【解決手段】　半導体基板１１の光入射面と反対の面にＰＮ接合と電極を形成した裏面接合型太陽電池において、前記ＰＮ接合を形成する面全体に、０．１ｎｍ以上５０ｎｍ以下の膜厚の真性半導体膜１２と、該膜上にＰ型およびＮ型の導電性半導体層１３，１４と、該半導体層上に設けた電極１５，１６とを備えた。



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1

【特許請求の範囲】

【請求項１】　半導体基板の光入射面と反対の面にＰＮ接合と電極を形成した裏面接合型太陽電池において、前記ＰＮ接合を形成する面全体に、０．１ｎｍ以上５０ｎｍ以下の膜厚の真性半導体膜と、該膜上にＰ型およびＮ型の導電性半導体層と、該半導体層上に設けた電極とを備えたことを特徴とする裏面接合型光起電力素子。

【請求項２】　前記Ｐ型およびＮ型の導電性半導体層上に設けた電極は、櫛の歯状に交互に並べて配置したことを特徴とする請求項１記載の光起電力素子。

【請求項３】　前記基板が単結晶半導体基板または多結晶半導体基板であることを特徴とする請求項１記載の光起電力素子。

【請求項４】　前記真性半導体膜として、非結晶Ｓｉ膜、または非結晶Ｓｉ／微結晶Ｓｉヘテロ構造膜、または非結晶ＳｉＣ膜、または非結晶ＳｉＣ／微結晶Ｓｉヘテロ構造膜を用いたことを特徴とする請求項１記載の光起電力素子。

【請求項５】　前記真性半導体膜は、触媒ＣＶＤを用いて形成したことを特徴とする請求項１記載の光起電力素子。

【請求項６】　前記半導体基板の光入射面に反射防止膜を備えたことを特徴とする請求項１記載の光起電力素子。

【請求項７】　前記半導体基板の光入射面に前記半導体基板と反対導電型の層を備えたことを特徴とする請求項１記載の光起電力素子。

【請求項８】　前記半導体基板の光入射面に真性半導体膜を備えたことを特徴とする請求項１記載の光起電力素子。

【請求項９】　一導電型の半導体結晶基板を準備し、前記基板の少なくとも一面に真性非結晶半導体膜を被着し、該膜上にＰ型およびＮ型に不純物ドープした導電性半導体層を互いに離隔して配置することを特徴とする光起電力素子の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、光入射面と反対の面にＰＮ接合と正負の電極を配置した裏面接合型太陽電池等の光起電力素子に関するものである。

【０００２】

【従来の技術】工業的に大量に生産されている太陽電池は、非結晶（アモルファス）シリコン材料を用いたものが多い。しかしながら、このような太陽電池は生産コストは低いが発電効率が低いという問題がある。そこでこの改良のため、シリコン単結晶または多結晶基板に、該基板とは反対導電型の非結晶シリコン膜を被着してＰＮ接合を形成し、これにより光起電力の変換効率を向上させる努力がなされている。

【０００３】このような結晶系シリコン基板と、非結晶

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シリコン膜との組合せで接合を形成した場合に、異なる種類の半導体層の界面で、界面順位の存在により光生成キャリアの再結合が生じて、期待される性能を実現することが困難であるという問題があった。このような問題点を解決するため、結晶性シリコン基板と非結晶シリコン膜との界面に真性非結晶半導体膜を形成し、界面順位を低減する試みがなされている。

【０００４】また、一般に太陽電池は、光入射面側に透明電極を備え、光入射面と反対面に設けた電極との間で光起電力を取り出している。このため、光入射面側に設けた透明電極による光の遮蔽損が存在し、このため発電効率に限界が生じるという問題があった。このような問題点を避けるため、光入射面側に透明電極を配置せず、基板の光入射面と反対面側の近傍にＰＮ接合を形成し、Ｐ層およびＮ層に接続する電極をそれぞれ配置し、Ｐ層とＮ層とを交互に櫛の歯状に並べた裏面接合型太陽電池が知られている。

【０００５】ところが、裏面接合型太陽電池では、半導体基板の表面付近で生成したキャリアが基板の裏面近傍に配置されたＰＮ接合まで到達するために、大きなキャリアライフタイムを有する高品質な結晶性半導体基板が必要である。しかしながら、裏面接合型太陽電池の製造工程では、熱酸化および熱拡散等の高温プロセスが必要であるため、キャリアライフタイムが劣化し、期待した発電効率等の性能が得られ難いという問題がある。

【０００６】

【発明が解決しようとする課題】本発明は上述した事情に鑑みてなされたもので、低温処理プロセスを用いることで、大きなキャリアライフタイムを有する高品質な半導体基板の状態を維持し、これにより発電効率の高い太陽電池等の光起電力素子を提供することを目的とする。

【０００７】

【課題を解決するための手段】本発明の光起電力素子は、半導体基板の光入射面と反対の面にＰＮ接合と電極を形成した裏面接合型太陽電池において、前記ＰＮ接合を形成する面全体に、０．１ｎｍ以上５０ｎｍ以下の膜厚の真性半導体膜と、該膜上にＰ型およびＮ型の導電性半導体層と、該半導体層上に設けた電極とを備えたことを特徴とする。ここで、前記Ｐ型およびＮ型の導電性半導体層上に設けた電極は、櫛の歯状に交互に並べて配置することが好ましい。

【０００８】また、真性半導体膜は、プラズマＣＶＤまたは触媒ＣＶＤを用いて形成することが好ましく、特に触媒ＣＶＤを用いることが好ましい。また、半導体基板の光入射面側に基板と反対導電型の層を設けるようにしてもよい。

【０００９】真性半導体膜をプラズマＣＶＤまたは触媒ＣＶＤを用いて形成し、その真性半導体膜上にＰ型およびＮ型の櫛の歯状に交互に並べた接合および電極を同様に低温処理プロセスで形成することで、半導体基板のキ

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ャリアライフタイムを高い状態で維持することが可能となる。これにより、裏面接合型光起電力素子としての高い発電効率等の良好な光電変換効率が得られる。特に、触媒ＣＶＤを用いることで、高品位な状態に基板を維持できると共に、膜生成の生産性を比較的高くすることができる。

【００１０】

【発明の実施の形態】以下、本発明の実施形態について添付図面を参照しながら説明する。

【００１１】図１は、本発明の一実施形態の光起電力素子を示す。この光起電力素子は太陽電池であり、例えばＮ型の結晶性半導体基板１１の裏面側にＰＮ接合と電極を配置した裏面接合型の太陽電池である。結晶性半導体基板１１は、例えば厚さが１００μｍ程度のデンドリックウェブからなるＮ型に不純物ドープしたシリコン単結晶基板であり、この裏面側に真性半導体膜１２を備えている。また、結晶性半導体基板１１として、リボン多結晶を用いてもよい。

【００１２】係る単結晶または多結晶シリコン基板は、所定温度に調整されたシリコン原料を溶融したるつぼから、所定方位の結晶軸に沿って種結晶を引上げることで、薄い帯状（シート状）の結晶を成長させて生産することができる。即ち、この結晶をエンドレスベルトに挟んで引上げることで、長尺の結晶を連続的に引上げることができる。そして、薄い帯状の結晶を適当な寸法で裁断することにより、厚さ１５０μｍ以下の矩形シート形状の単結晶または多結晶シリコン基板が得られる。この詳細については、本出願人の特願２０００－２７５３１５号を参照されたい。

【００１３】真性半導体膜１２は、厚さが０．１ｎｍ以上、５０ｎｍ以下の極めて薄い非結晶性（アモルファス）層である。そして、この真性半導体膜は、非結晶シリコン膜、または非結晶シリコンと微結晶シリコン膜とのヘテロ構造膜、または非結晶炭化シリコン膜、または非結晶炭化シリコン膜と微結晶シリコン膜とのヘテロ構造膜等である。この真性半導体膜は、電気的に中性な膜であり、この膜をＰＮ接合間に挟むことで、水素パッシベーション効果があり、開放電圧が上昇する等の電気的特性の改良が可能である。

【００１４】この真性半導体膜１２は、触媒ＣＶＤまたはプラズマＣＶＤで形成することが好ましい。触媒ＣＶＤ法は、図２（ａ）に示すように、減圧可能な真空容器内にガス供給系装置２１、高温触媒２２、成膜対象の基板２３、基板ホルダ２４等を備える。ここで、高温触媒２２は、タングステンまたはモリブデン等の線材を１５００～２４００℃に加熱して、対象ガスを活性化して基板２３の表面に気相成長被膜を形成するものである。これに対して、図３（ｂ）に示すプラズマＣＶＤ装置は、電極２５，２６間に高周波電源２７より高周波電圧を供給することで、成膜対象のガス分子２８をプラズマ化して図中の矢印方向に振動させ、これにより成膜対象の基板２３の表面上に気相成長被膜を形成するものである。この図３（ａ）に示す触媒ＣＶＤ法は、図３（ｂ）に示すプラズマＣＶＤ法と比較すると、成膜対象基板へのプラズマダメージがほとんど存在しない、装置の構造が簡単でかつ低コストとなる、スケールアップが容易である等の特徴がある。特に、成膜速度が、例えば５～１０ｎｍ／秒程度と比較的高く、アモルファスシリコン膜や微結晶シリコン膜等の形成で品質が高い膜が比較的短時間で得られる。

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【００１５】この真性半導体膜１２の表面には、Ｐ型に不純物ドープした導電性半導体層１３と、Ｎ型に不純物ドープした導電性半導体層１４とが交互に並べて配置されている。この半導体層１３，１４は、例えばメタルマスクを用いて触媒ＣＶＤまたはプラズマＣＶＤにより形成された非結晶導電性シリコン層である。半導体層１３，１４上にはそれぞれ電極１５，１６が配置されている。これらの電極１５，１６は、例えば銀等の導電性ペーストをスクリーン印刷によりパターン形成し、これを加温硬化して形成される。Ｐ型およびＮ型にそれぞれ不純物ドープした半導体層１３，１４間は、例えばポリイミド樹脂膜等の絶縁膜１７により絶縁されている。半導体基板１１の光入射面側にはＳｉＮからなる反射防止膜１８が配置されている。

【００１６】図３は、この太陽電池の裏面側を模式的に示した図であり、Ｐ型半導体層１３に接続する電極１５と、Ｎ型半導体層１４に接続する電極１６とが、櫛の歯状に交互に並べて互いに平行に配置されている。多数の櫛の歯状の電極１５はその基部である母線部１５ａに接続し、多数の櫛の歯状の電極１６はその基部である母線部１６ａにそれぞれ接続されている。従って、この太陽電池の起電力は母線部の電極１５ａ，１６ａ間で取り出される。

【００１７】次に、この太陽電池の構造上の特徴について説明する。この太陽電池は、基板１１の裏面側に触媒ＣＶＤまたはプラズマＣＶＤで形成された薄い非結晶真性シリコン層（半導体膜）１２を備え、その表面に触媒ＣＶＤまたはプラズマＣＶＤで形成されたＰ型およびＮ型に不純物ドープした半導体層１３，１４を備えている。従って、真性半導体膜１２と導電性半導体層１３，１４は共に触媒ＣＶＤまたはプラズマＣＶＤ等の低温プロセスにより形成された膜を用いている。そして、絶縁膜１７の形成、および電極１５，１６の形成も、それぞれスクリーン印刷等により被膜のパターンを形成し、これを比較的低温の４００℃未満の加温硬化処理により形成している。従って、すべてのプロセスが４００℃未満の低温処理により被膜が形成されるので、半導体基板１１において大きなキャリアライフタイムを有する高品質な状態をそのまま維持することができる。そして、その表面側には透明電極が存在しないので、これによる遮蔽

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損が発生せず、高い発電効率等の良好な光電変換特性が得られる。

【００１８】真性半導体膜１２、およびＰ型およびＮ型の導電性半導体層１３，１４は、それぞれ触媒ＣＶＤを用いて形成することが好ましい。触媒ＣＶＤにおいては、基板温度が１００～４００℃程度であり、低温プロセスであるため、半導体基板１１がダメージを受けない。また、高濃度の水素ラジカルの存在により結晶内部の欠陥を補修して欠陥順位密度を低減できる等の特徴がある。また、プラズマＣＶＤと異なり、プラズマによるダメージを受けないので、これにより半導体基板１１のキャリアライフタイムの維持に寄与することができる。

【００１９】図４は、本発明の他の実施形態の光起電力素子を示す。この実施形態においては、基板１１の光入射面側にも真性半導体膜２０を備えている。その他の構成は、図１に示す第１の実施形態と同様である。ここで、真性半導体膜２０は、基板裏面側の真性半導体膜１２と同時に基板１１の表裏両面および側面に形成することが好ましい。これにより、結晶性シリコン基板１１の光入射面側および側面もその表面が真性半導体膜で覆われることにより、界面順位を低減して、電気的特性を向上させることができる。

【００２０】図５は、本発明の更に他の実施形態の光起電力素子を示す。この実施形態においては、基板１１の光入射面側に基板１１と反対導電型の層２１を備えている。この層２１は、Ｎ型の半導体基板１１に対して反対導電型のＰ型層であり、反対導電型電荷により基板の内部電界を利用してキャリア再結合を防止する機能を有している。これにより、光電変換効率等の電気的特性を向上することが可能である。

【００２１】次に、図６を参照して本発明の光起電力素子の製造方法について説明する。まず、図６（ａ）に示すように、Ｎ型の単結晶または多結晶シリコン基板１１を準備する。これは、上述したようにデンドリックウェブ結晶またはリボン多結晶を用いることができる。そして、次に洗浄を行い表面に付着した酸化膜等を除去し、表面を清浄な状態にする。次に、図６（ｂ）に示すように、触媒ＣＶＤにより非結晶真性シリコン膜１２，２０を基板１１の表裏両面に形成する。この厚さは、０．１ｎｍ以上５０ｎｍ以下が好ましいが、一例として１０ｎｍ程度に形成する。この非結晶真性シリコン膜の形成条件の一例は、次のとおりである。

ガス流量：SiH_4＝２０ｓｃｃｍ
ガス比：SiH_4／H_2＝１：１０
成膜圧力：１Ｐａ
基板温度：２５０℃
フィラメント温度：１８００℃

【００２２】次に、図６（ｃ）に示すように、触媒ＣＶＤにより非結晶導電性シリコン層１３を形成する。ここで導電性シリコン層１３はＰ型であり、例えば膜厚を３

０ｎｍ程度とする。このＰ型非結晶シリコン層は、

ガス流量：SiH_4＝２０ｓｃｃｍ、B_2H_6＝１ｓｃｃｍ（１％、H_2希釈）、
ガス比：SiH_4／H_2＝１：１０、
成膜圧力：１Ｐａ、
基板温度：２５０℃、
フィラメント温度：１８００℃、

により形成している。

【００２３】次に、図６（ｄ）に示すようにＮ型の非結晶導電性シリコン層１４を形成する。これも同様にメタルマスクを用いて導電性シリコン層１３の間に櫛の歯状に間挿するように多数の平行パターンを形成する。膜厚は例えば３０ｎｍ程度である。この条件は、

ガス流量：SiH_4＝２０ｓｃｃｍ、PH_3＝１ｓｃｃｍ（１％、H_2希釈）、
ガス比：SiH_4／H_2＝１：１０、
成膜圧力：１Ｐａ、
基板温度：２５０℃、
フィラメント温度：１８００℃、

により形成している。

【００２４】次に、図６（ｅ）に示すように、保護膜１７を形成する。これは、例えばポリイミド樹脂ペーストをスクリーン印刷法等により、導電性シリコン層１３，１４の間に埋め込んで、２５０℃以下の温度で加温硬化することにより形成する。この保護膜１７の形成により、耐候性および耐はんだ付け性が向上する。そして、図６（ｆ）に示すように、例えば銀ペーストをスクリーン印刷により塗布し、これを同様に２５０℃以下の比較的低温で加温硬化することにより、図３に示す櫛の歯状の交互に間挿した電極パターン１５，１６，１５ａ，１６ａを形成する。

【００２５】なお、上記工程において、図示はしないが基板１１の表面に反射防止膜を形成することが好ましい。反射防止膜は、例えば高周波スパッタ法によるSi_3N_4膜等が好適であり、例えば膜厚６０ｎｍ程度に形成する。また、図５に示すように、半導体基板１１の光入射面側に基板と反対導電型の拡散層を設けるようにしてもよい。これは、半導体基板１１にあらかじめ熱拡散またはイオン注入等の方法により形成しておくことが好ましい。

【００２６】なお、上記実施形態は本発明の実施例の一態様を述べたもので、本発明の趣旨を逸脱することなく種々の変形実施例が可能なことは勿論である。

【００２７】

【発明の効果】以上説明したように本発明によれば、半導体基板のキャリアライフタイムが大きく、発電効率等の電気的特性に優れた裏面接合型太陽電池等の光起電力素子を提供できる。

【図面の簡単な説明】

【図１】本発明の一実施形態の光起電力素子の概略構成

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を示す断面図である。

【図２】（ａ）は触媒ＣＶＤ法を示す図であり、（ｂ）はプラズマＣＶＤ法を示す図である。

【図３】図１の光起電力素子の底面の電極構成を示す図である。

【図４】本発明の他の実施形態の光起電力素子の概略構成を示す断面図である。

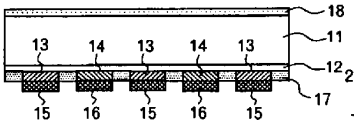
【図５】本発明の他の実施形態の光起電力素子の概略構成を示す断面図である。

【図６】本発明の光起電力素子の製造工程を示す図である。

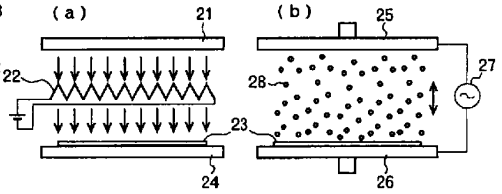
【符号の説明】

１１　結晶性半導体基板
１２，２０　真性半導体膜
１３　Ｐ型導電性シリコン層
１４　Ｎ型導電性シリコン層
１５，１６　電極
１７　絶縁層
１８　反射防止膜
２１　反対導電型層

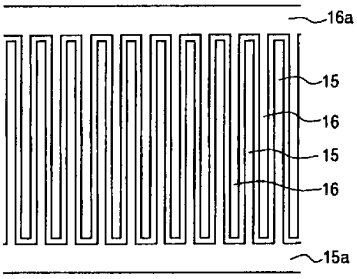
【図１】



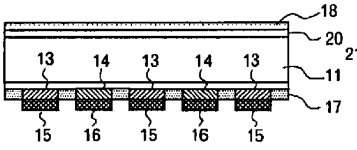
【図２】



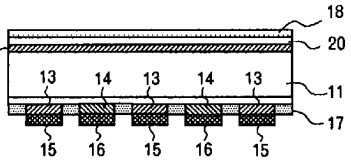
【図３】



【図４】

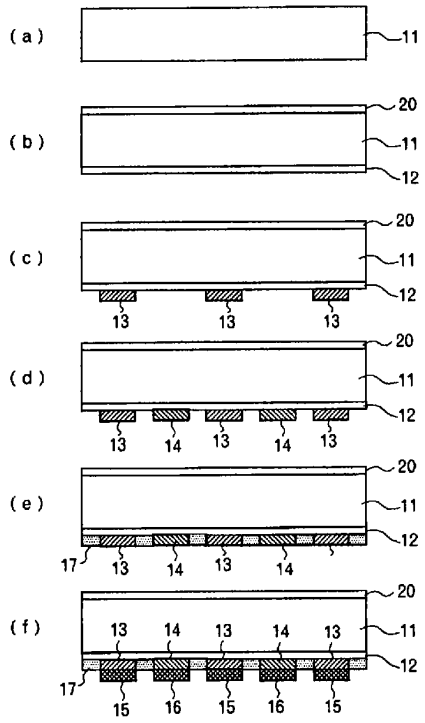


【図５】



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【図６】



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PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2006-128630**
(43)Date of publication of application : **18.05.2006**

(51)Int.Cl. *H01L 31/04 (2006.01)*

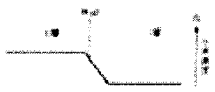
(21)Application number : **2005-257818**
(22)Date of filing : **06.09.2005**

(71)Applicant : **SANYO ELECTRIC CO LTD**
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(30)Priority
Priority number : **2004284569** Priority date : **29.09.2004** Priority country : **JP**

(54) PHOTOVOLTAIC DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the deterioration of output characteristics of a solar battery in a heating process after forming an amorphous semiconductor thin film layer by a plasma CVD method.
SOLUTION: A photovoltaic device is formed with a substantially intrinsic amorphous silicon layer containing hydrogen between an n-type single crystal silicon substrate and a p-type amorphous silicon layer containing hydrogen. A trap layer whose hydrogen concentration is lower than that of the intrinsic amorphous silicon layer is formed between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer. By this trap layer, hydrogen diffusion from the intrinsic amorphous layer to the p-type amorphous silicon layer is prevented.



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(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2006-128630
(P2006-128630A)
(43)公開日　平成18年5月18日(2006.5.18)

(51)Int.Cl.		F1		テーマコード（参考）
H01L 31/04	(2006.01)	H01L 31/04	N	5F051

審査請求 未請求　請求項の数 16　OL　（全 18 頁）

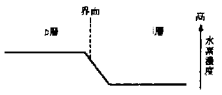
(21)出願番号　特願2005-257818 (P2005-257818)
(22)出願日　平成17年9月6日 (2005.9.6)
(31)優先権主張番号　特願2004-284569 (P2004-284569)
(32)優先日　平成16年9月29日 (2004.9.29)
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Fターム(参考)　5F051 AA05 CA02 CA03 CA13 CA15
DA04 FA04 GA04 GA14 HA20

(54)【発明の名称】光起電力装置

(57)【要約】
【課題】　この発明は、プラズマＣＶＤ法による非晶質系半導体薄膜層を形成した以降の加熱工程で太陽電池の出力特性の低下を抑制することを課題とする。
【解決手段】　この発明は、ｎ型単結晶シリコン基板と水素を含有するｐ型非晶質シリコン層との間に、水素を含有する実質的に真性な非晶質シリコン層を設けた光起電力装置において、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との間に、前記真性な非晶質シリコン層の水素濃度より水素濃度が低いトラップ層を設ける。このトラップ層により、真性な非晶質シリコン層からｐ型非晶質シリコン層への水素拡散を抑制する。
【選択図】　図３



【特許請求の範囲】
【請求項１】
結晶系半導体基板と、この結晶系基板上に設けられる水素を含有する実質的に真性な非晶質系半導体薄膜層と、この真性な非晶質系半導体薄膜上に設けられる水素を含有する荷電子制御された非晶質系半導体薄膜層と、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との間に設けられ、前記真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制する水素拡散抑制領域と、を備えたことを特徴とする光起電力装置。
【請求項２】
前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が高濃度な領域で形成されることを特徴とする請求項１に記載の光起電力装置。
【請求項３】
前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が高濃度で且つ前記荷電子制御された非晶質系半導体薄膜層と同型の荷電子制御用の不純物がドープされた領域で形成されることを特徴とする請求項１に記載の光起電力装置。
【請求項４】
前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が低いトラップ層で形成されることを特徴とする請求項１に記載の光起電力装置。
【請求項５】
前記トラップ層は、実質的に真性な非晶質系半導体薄膜層で形成されることを特徴とする請求項４に記載の光起電力装置。
【請求項６】
前記トラップ層は前記荷電子制御された非晶質系半導体薄膜層と同型の荷電子制御用の不純物がドープされていることを特徴とする請求項４に記載の光起電力装置。
【請求項７】
ｎ型単結晶シリコン基板と、この単結晶シリコン基板上に設けられる水素を含有する実質的に真性な非晶質シリコン層と、この真性な非晶質シリコン層上に設けられる水素を含有するｐ型非晶質シリコン層と、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との間に設けられ、前記真性な非晶質シリコン層から前記ｐ型非晶質シリコン層への水素拡散を抑制する水素拡散抑制領域と、を備えたことを特徴とする光起電力装置。
【請求項８】
前記水素拡散抑制領域は、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が高濃度な領域で形成されることを特徴とする請求項７に記載の光起電力装置。
【請求項９】
前記水素拡散抑制領域は、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が高濃度で且つ前記ｐ型の不純物がドープされた領域で形成されることを特徴とする請求項７に記載の光起電力装置。
【請求項１０】
前記水素拡散抑制領域は、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が低いトラップ層で形成されることを特徴とする請求項７に記載の光起電力装置。
【請求項１１】

前記トラップ層は、実質的に真性な非晶質シリコン層で形成されることを特徴とする請求項１０に記載の光起電力装置。
【請求項１２】
前記トラップ層の膜厚は１ｎｍ以上５ｎｍ以下であることを特徴とする請求項１１に記載の光起電力装置。
【請求項１３】
前記トラップ層の膜厚は１ｎｍ以上２ｎｍ以下であることを特徴とする請求項１１に記載の光起電力装置。
【請求項１４】
前記トラップ層はｐ型の不純物がドープされている非晶質シリコン層であることを特徴とする請求項１０に記載の光起電力装置。
【請求項１５】
前記トラップ層の膜厚は０．１ｎｍ以上３ｎｍ未満であることを特徴とする請求項１４に記載の光起電力装置。
【請求項１６】
前記トラップ層の膜厚は０．３ｎｍ以上２ｎｍ以下であることを特徴とする請求項１４に記載の光起電力装置。
【発明の詳細な説明】
【技術分野】
【０００１】
この発明は、ヘテロ半導体接合を有する光起電力装置に関する。
【背景技術】
【０００２】
近年、光起電力装置として、単結晶シリコンや多結晶シリコン等の結晶系半導体を用いた太陽電池の研究および実用化が盛んに行なわれている。中でも、非晶質シリコンと結晶系シリコンとを組合せることにより構成されたヘテロ半導体接合を有する太陽電池は、その接合を２００℃以下のプラズマＣＶＤ法などの低温プロセスで形成することができ、かつ、高い変換効率が得られることから、注目を集めている。このような光起電力素子において、光電変換効率を向上させるためには、高い短絡電流（Ｉｓｃ）および開放電圧（Ｖｏｃ）を維持しつつ曲線因子（Ｆ．Ｆ．）を向上させる必要がある。
【０００３】
そこで、ｎ型単結晶シリコン基板と水素を含有したｐ型非晶質シリコン層との間に、水素を含有した実質的に真性な非晶質シリコン層（ｉ型非晶質シリコン層）が挿入された所謂Ｈ．Ｉ．Ｔ．（Ｈｅｔｅｒｏｊｕｎｃｔｉｏｎ ｗｉｔｈ Ｉｎｔｒｉｎｓｉｃ Ｔｈｉｎ－ｌａｙｅｒ）構造を有する太陽電池が開発されている。Ｈ.Ｉ.Ｔ. 構造を有する太陽電池装置において、光生成キャリアの再結合を更に低減し、光電変換効率を向上させるために、ｉ型非晶質シリコン層の光学的バンドギャップをｐ型非晶質シリコン層と接する側において広く構成したものが提案されている（例えば、特許文献１参照）。
【０００４】
上記したＨ．Ｉ．Ｔ．構造を有する太陽電池装置においては、光入射側に位置するｐ型非晶質シリコン層は導電性と光透過性の両方を考慮して水素濃度やボロン（Ｂ）などのｐ型不純物のドープ量等の組成が最適化された層に構成されている。また、ｉ型非晶質シリコン層も界面特性を向上すべく水素濃度などの組成が最適化された層に構成されている。このように、単にｐ型非晶質シリコン層、ｉ型非晶質シリコン層をそれぞれを最適化した従来のＨ.Ｉ.Ｔ. 構造の太陽電池においては、水素濃度がｐ型非晶質シリコン層よりｉ型非晶質シリコン層の方が高くなっている。
【特許文献１】特開２００２－７６４０９号公報
【発明の開示】
【発明が解決しようとする課題】
【０００５】

ところで、プラズマＣＶＤ法で形成した非晶質シリコン層を有する各種太陽電池は２００℃以上の高温で長時間加熱すると出力特性が低下してしまう。このため、非晶質シリコン層形成後の電極形成やラミネート工程はなるべくＣＶＤ工程の温度を超えないように管理されている。

【０００６】

高温加熱による特性低下の原因としては、（１）水素を含有した荷電子制御された非晶質系半導体薄膜への電極材料の拡散、（２）水素を含有した実質的に真性な非晶質系半導体薄膜層へのドーパントの拡散、（３）水素の拡散、等が考えられる。このうち（３）が最も低温でその影響が現れる。

【０００７】

特に、ｉ型非晶質シリコン層からｐ型非晶質シリコン層への水素拡散により、ドーパントであるボロン（Ｂ）の活性化率が低下して内蔵電界が低下して太陽電池の出力特性が低下してしまうという問題があった。

【０００８】

この発明は、上記した問題点に鑑み、プラズマＣＶＤ法による非晶質系半導体薄膜層を形成した以降の加熱工程で太陽電池の出力特性の低下を抑制することを課題とするものである。

【課題を解決するための手段】

【０００９】

この発明は、結晶系半導体基板と、この結晶系基板上に設けられる水素を含有する実質的に真性な非晶質系半導体薄膜層と、この真性な非晶質系半導体薄膜上に設けられる水素を含有する荷電子制御された非晶質系半導体薄膜層と、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との間に設けられ、前記真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制する水素拡散抑制領域と、を備えてなる。

【００１０】

上記のように、この発明は、水素拡散抑制領域により、真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制することができる。この結果、非晶質系半導体薄膜層の形成以降の加熱工程で太陽電池の出力特性の低下を抑制することができる。

【００１１】

前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が高濃度な領域で形成することができる。

【００１２】

上記のように、前記真性な非晶質系半導体薄膜層より水素濃度が高濃度な領域を設けることで、水素拡散抑制領域を構成することができる。そして、水素濃度が高濃度な領域により、真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制することができる。

【００１３】

また、前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が高濃度で且つ前記荷電子制御された非晶質系半導体薄膜層と同型の荷電子制御用の不純物がドープされた領域で形成することができる。

【００１４】

上記のように、前記真性な非晶質系半導体薄膜層より水素濃度が高濃度で且つ前記荷電子制御された非晶質系半導体薄膜層と同型の荷電子制御用の不純物がドープされた領域を設けることで、水素拡散抑制領域を構成することができる。そして、前記領域により、真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制することができる。

【００１５】
また、前記水素拡散抑制領域は、前記荷電子制御された非晶質系半導体薄膜層と前記真性な非晶質系半導体薄膜層との界面近傍において、前記真性な非晶質系半導体薄膜層の水素濃度より水素濃度が低いトラップ層で形成することができる。
【００１６】
上記のように、前記真性な非晶質系半導体薄膜層より水素濃度より水素濃度が低いトラップ層を設けることで、水素拡散抑制領域を構成することができる。そして、前記トラップ層により、真性な非晶質系半導体薄膜層から前記荷電子制御された非晶質系半導体薄膜層への水素拡散を抑制することができる。
【００１７】
前記トラップ層は、実質的に真性な非晶質系半導体薄膜層で構成することができる。
【００１８】
前記トラップ層は、前記荷電子制御された非晶質系半導体薄膜層と同型の荷電子制御用の不純物がドープされていてもよい。
【００１９】
また、この発明は、ｎ型単結晶シリコン基板と、この単結晶シリコン基板上に設けられる水素を含有する実質的に真性な非晶質シリコン層と、この真性な非晶質シリコン層上に設けられる水素を含有するｐ型非晶質シリコン層と、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との間に設けられ、前記真性な非晶質シリコン層から前記ｐ型非晶質シリコン層への水素拡散を抑制する水素拡散抑制領域と、を備えたことを特徴とする。
【００２０】
上記のように、この発明は、水素拡散抑制領域により、真性な非晶質シリコン層から前記ｐ型非晶質シリコン層への水素拡散を抑制することができる。この結果、非晶質シリコン層の形成以降の加熱工程で太陽電池の出力特性の低下を抑制することができる。
【００２１】
前記水素拡散抑制領域は、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が高濃度な領域で形成することができる。
【００２２】
上記のように、前記真性な非晶質シリコン層より水素濃度が高濃度な領域を設けることで、水素拡散抑制領域を構成することができる。そして、水素濃度が高濃度な領域により、真性な非晶質シリコン層から前記ｐ型非晶シリコン層への水素拡散を抑制することができる。
【００２３】
また、前記水素拡散抑制領域は、前記ｐ型非晶質シリコン層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が高濃度で且つ前記ｐ型の不純物がドープされた領域で形成することができる。
【００２４】
上記のように、前記真性な非晶質シリコン層より水素濃度が高濃度且つ前記ｐ型の不純物がドープされた領域を設けることで、水素拡散抑制領域を構成することができる。そして、前記領域により、真性な非晶質シリコン層から前記ｐ型非晶質シリコン層への水素拡散を抑制することができる。
【００２５】
前記水素拡散抑制領域は、前記ｐ型非晶質シリコン半導体薄膜層と前記真性な非晶質シリコン層との界面近傍において、前記真性な非晶質シリコン層の水素濃度より水素濃度が低いトラップ層で形成してもよい。
【００２６】
上記のように、前記真性な非晶質シリコン層の水素濃度より水素濃度が低いトラップ層を設けることで、水素拡散抑制領域を構成することができる。そして、前記トラップ層により、真性な非晶質シリコン層から前記ｐ型非晶質シリコン層への水素拡散を抑制するこ

とができる。

【００２７】

前記トラップ層は、実質的に真性な非晶質シリコン層で形成することができる。そして、この場合、トラップ層の膜厚は１ｎｍ以上５ｎｍ以下、好ましくは１ｎｍ以上２ｎｍ以下にするとよい。

【００２８】

前記トラップ層はｐ型の不純物がドープされた非晶質シリコン層で構成することができる。そして、この場合、トラップ層の膜厚は０．１ｎｍ以上３ｎｍ未満、好ましくは０．３ｎｍ以上２ｎｍ以下にするとよい。

【発明を実施するための最良の形態】

【００２９】

以下、この発明の実施形態につき、図面を参照して説明する。まず、この発明が適用されるH.I.T.構造の光起電力装置につき図１に従い説明する。図１は、この発明が適用されるH.I.T. 構造の光起電力装置を示す概略断面図である。

【００３０】

この光電変換装置は、図１に示すように、結晶系半導体基板として、約１Ω・ｃｍの抵抗率と約３００μｍの厚みとを有するとともに、（１００）面を有するｎ型単結晶シリコン（Ｃ－Ｓｉ）基板１（以下、ｎ型単結晶シリコン基板１という）を備えている。ｎ型単結晶シリコン基板１の表面には、数μｍから数十μｍの高さを有する光閉じ込めのためのピラミッド状凹凸が形成されている。このｎ型単結晶シリコン基板１上には、ＲＦプラズマＣＶＤ法により水素を含有する実質的に真性な非晶質半導体薄膜層として、３ｎｍ～２５０ｎｍの厚みを有する実質的に真性のｉ型非晶質シリコン（ａ－Ｓｉ：Ｈ）層２が形成されている。また、ｉ型非晶質シリコン層２上には、水素を含有する荷電子制御された非晶質半導体薄膜層として、約５ｎｍの厚みを有するｐ型非晶質シリコン層３が形成されている。

【００３１】

そして、ｐ型非晶質シリコン層３上には、約１００ｎｍの厚みを有する酸化物透明導電膜として、この実施形態では、ＩＴＯ（Ｉｎｄｉｕｍｅ　ｔｈｉｎ　Ｏｘｉｃｉｄｅ）膜４がマグネトロンスパッタ法により形成されている。このＩＴＯ膜４は、SnO_2（酸化錫）を添加したIn_2O_3（インジウム酸化物）によって形成されている。

【００３２】

このＩＴＯ膜４の上面の所定領域には銀ペーストからなる櫛形状の集電極５が形成されている。

【００３３】

また、ｎ型単結晶シリコン基板１の下面上には、約５ｎｍの厚みを有する実質的に真性のｉ型非晶質シリコン層６が形成されている。ｉ型非晶質シリコン層６上には、約２０ｎｍの厚みを有するｎ型非晶質シリコン層７が形成されている。このようにｎ型単結晶シリコン基板１の下面上に、ｉ型非晶質シリコン層６およびｎ型非晶質シリコン層７が順番に形成されることにより、いわゆるＢＳＦ（Ｂａｃｋ　Ｓｕｒｆａｃｅ　Ｆｉｅｌｄ）構造が形成されている。更に、ｎ型非晶質シリコン層７上には、約１００ｎｍの厚みを有する酸化物透明導電膜として、この実施形態ではＩＴＯ膜８がマグネトロンスパッタ法により形成されている。このＩＴＯ膜８は、SnO_2を添加したIn_2O_3によって形成されている。

【００３４】

このＩＴＯ膜８の上面の所定領域には銀ペーストからなる櫛形状の集電極９が形成されている。

【００３５】

上記した光起電力装置の製造例について以下に述べる。洗浄したｎ型の単結晶シリコン基板１を真空チャンバーに導入し、適度な温度（２００℃以下）に加熱し、基板表面に付着する水分を極力除去する。次に、水素ガスを導入し、プラズマ放電により基板表面のク

リーニングを行う。

【００３６】

その後、シラン（SiH_4）ガス及び水素ガスを導入してノンドープのｉ型非晶質シリコン層２を形成する。続いて、SiH_4ガス、水素ガス、およびドーピングガスとしてジボラン（B_2H_6）ガスを導入してｐ型の非晶質シリコン層３を形成してｐｎ接合が完成される。さらに、表面電極４として酸化インジウム錫層をスパッタ法による、集電極５として銀電極をスクリーン印刷法にて形成し、この銀電極を焼成して集電極５が形成される。

【００３７】

なお、基板１の反対側にノンドープのｉ型非晶質シリコン層６、ｎ型の非晶質シリコン層７、および裏面電極層８，９を形成していわゆるＢＳＦ構造を形成してもよい。このとき、ｐ型層を作成する順序については裏面側（ｎ型側）から作成してもよいし、表側（ｐ側）から作成してもよい。

【００３８】

また、基板をｐ型とし、表側にノンドープの非晶質シリコン層、ｎ型の非晶質シリコン層、および酸化インジウム錫層、銀集電極を、裏側にノンドープの非晶質シリコン層、ｐ型の非晶質シリコン層および裏面電極層を作成する場合も全く同様に取り扱える。表１に光起電力装置としての太陽電池作成時の各非晶質シリコン層の形成条件を示す。

【００３９】

【表１】

処理		形成条件等			
		基板温度 (℃)	使用ガス	圧力 (Pa)	パワー密度 (mW/cm^2)
表側	水素処理	150~180	H_2 : 100sccm	30~100	3~30
	i-type a-Si	150~180	H_2 : 0~100sccm SiH_4 : 40sccm	40~120	5~15
	p-type a-Si	150~180	H_2 : 0~100sccm SiH_4 : 40sccm B_2H_6(2%) : 20sccm	40~120	5~15
裏側	水素処理	170	H_2 : 100sccm	50	3~30
	i-type a-Si	170	SiH_4 : 40sccm	40	8.33
	n-type a-Si	170	H_2 : 0~100sccm SiH_4 : 40sccm PH_3(1%) : 40sccm (PH_3/SiH_4 : 1%)	40	8.33

【００４０】

上述したように、ｐ型非晶質シリコン層３、ｉ型非晶質シリコン層２をそれぞれを最適化した従来のＨ．Ｉ．Ｔ．構造の太陽電池においては、水素濃度がｐ型非晶質シリコン層３よりｉ型非晶質シリコン層２の方が高くなっている。

【００４１】

図２は、従来のＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面近傍の水素濃度プロファイルを模式的に示したものである。ｐ型非晶質シリコン層３よりもｉ型非晶質シリコン層２の方が水素濃度が高く、ｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面近傍には、ｉ型非晶質シリコン層（ｉ層）２か

らｐ型非晶質シリコン層（ｐ層）３に向かって負の水素濃度勾配が形成されている。このため、ｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面も形成後に行われる集電極形成のための焼成やモジュール化の際のラミネート工程などの高温加熱によって、膜中の水素はｉ型非晶質シリコン層２からｐ型非晶質シリコン層３へ拡散し易くなっている。

【００４２】

図３は、この発明の第１の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを模式的に示したものである。この図３に示すように、この発明の第１の実施形態においては、従来とは逆に、ｉ型非晶質シリコン層２からｐ型非晶質シリコン層３に向かって水素濃度が高くなるように、正の水素濃度勾配を持たせている。すなわち、ｉ型非晶質シリコン層２の水素濃度よりｐ型非晶質シリコン層３の水素濃度を高くして水素拡散抑制領域を形成している。このように構成することで、ｐ型非晶質シリコン層３中への水素拡散を防止するように構成している。

【００４３】

ｐ型非晶質シリコン層３中の水素濃度をｉ型非晶質シリコン層２よりも高くするには、以下の方法を用いて形成すればよい。

（１）ｐ型非晶質シリコン層３の形成時の基板温度をｉ型非晶質シリコン層２の形成時よりも低くする。（２）ｐ型非晶質シリコン層３の形成時の水素希釈量をｉ型非晶質シリコン層２の形成時よりも高くする。（３）ｐ型非晶質シリコン層３の形成時の成膜圧力をｉ型非晶質シリコン層２の形成時よりも高くする。（４）ｐ型非晶質シリコン層３の形成時のＲＦ投入電力をｉ型非晶質シリコン層２の形成時よりも高くする。

【００４４】

ｐ型非晶質シリコン層３の形成時の水素希釈量をｉ型非晶質シリコン層２の形成時よりも高くして形成してこの発明の第１の実施形態を作成した。表２に表側のｐ型非晶質シリコン層３とｉ型非晶質シリコン層２の具体的形成条件を示す。裏面側の条件は表１に示す条件により作成した。また、ｉ型非晶質シリコン層２は膜厚１０ｎｍ、ｐ型非晶質シリコン層３は膜厚５ｎｍにしてそれぞれの膜を形成した。

【００４５】

【表２】

処理		形成条件等			
		基板温度 (℃)	使用ガス	圧力 (Pa)	パワー密度 (mW/cm^2)
表側	水素処理	170	H_2 : 100sccm	50	15
	i-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm	50	15
	p-type a-Si	170	H_2 : 400sccm SiH_4 : 40sccm B_2H_6(2%) : 20sccm	50	15

【００４６】

表２に従いこの発明の第１の実施形態をｐ型非晶質シリコン層の形成時の水素希釈量をｉ型非晶質シリコン層の形成時よりも高くして形成した。図４に、この発明の第１の実施形態と従来装置とを用意し、ＳＩＭＳにより、膜中の水素濃度プロファイル測定した結果を示す。従来装置は同じ水素の希釈量で形成した以外は第１の実施形態と同じ条件で形成

した。図４は、第１の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面部分の水素濃度プロファイルを示す図である。

【００４７】

測定に用いたＳＩＭＳ装置と、水素（Ｈ）とフッ素（Ｆ）の測定条件を以下に記載する。測定はサンプルにセシウムプラスイオン（Ｃｓ$^{+}$）を照射してたたき出された水素マイナスイオン（Ｈ$^{-}$）、フッ素マイナスイオン（Ｆ$^{-}$）、シリコンマイナスイオン（Ｓｉ$^{-}$）の２次イオン数をカウントし、水素濃度は［Ｈ$^{-}$］／［Ｓｉ$^{-}$］、フッ素濃度は［Ｆ$^{-}$］／［Ｓｉ$^{-}$］として定量している。ただし、シリコン濃度は５．０×１０^{22}／ｃｍ^{3}である。また、測定装置は、ＵＬＶＡＣ－ＰＨＩ（Ｐｈｙｓｉｃａｌ ｅｌｅｃｔｒｏｎｉｃ Ｉｎｃｏｒｐｏｒａｔｉｏｎ）社製のＡＤＥＰＴ１０１０を用い、イオン照射エネルギ１ｋｅＶで行った。

【００４８】

図４に示すＳＩＭＳで測定した水素濃度プロファイルから、図２と図３の模式図と同様の水素濃度プロファイルを確認でき、この発明の第１の実施形態においては、ｉ型非晶質シリコン層２からｐ型非晶質シリコン層３に向かって正の水素濃度勾配を持ち、ｐ型非晶質シリコン層３がｉ型非晶質シリコン層２より水素濃度が高くなっていることが分かる。

【００４９】

なお、第１の実施形態は、光入射側の窓層にあたるｐ型非晶質シリコン層３の水素濃度が高いために水素拡散を防止する効果に加えて、ｐ型非晶質シリコン層３での光吸収損失が小さくなり発電電流が増加する効果もある。

【００５０】

次に、この発明の第２の実施形態につき図５及び図６を参照して説明する。図５は、この発明の第２の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを模式的に示したものである。

【００５１】

図５に示すように、第２の実施形態は、ｐ型非晶質シリコン層３の構成を変更している。第１の実施形態では、ｐ型非晶質シリコン層３全体の水素濃度を高めたのに対して、この第２の実施形態では、ｐ型非晶質シリコン層３のｉ型非晶質シリコン２に近い側の前半部３１のみ高水素濃度として、後半部３２は従来装置と同等の水素濃度に戻している。

【００５２】

この第２の実施形態の構造は、前半部のｐ型非晶質シリコン層３１のボロン（Ｂ）ドープ濃度が比較的低く（＜１．０ａｔ．％）、後半部３２のボロン（Ｂ）ドープ濃度が比較的高い（＞２．０ａｔ．％）場合に有効である。なぜなら、この第２の実施形態の構造は第１の実施形態と同様にｉ型非晶質シリコン層からｐ型非晶質シリコン層への水素拡散を防止できるが、前半部のｐ型非晶質シリコン層３１から後半部の非晶質シリコン層３２への水素の拡散が生じてしまう。しかし、後半部の非晶質シリコン層３２はボロン（Ｂ）濃度が高いので、微量の拡散水素によるボロン（Ｂ）の一部が不活性化してもデバイス特性への影響は比較的小さくできる。

【００５３】

第２の実施形態の形成条件を表３に示す。この表から分かるように、ｐ型シリコン層３１と、ｐ型シリコン層３２のB_2H_6流量を異ならして膜を形成している。B_2H_6流量をｐ型非晶質シリコン層３1よりｐ型非晶質シリコン層３２の方が多くし、更に、水素希釈量はｐ型非晶質シリコン層３１の方を高くした。裏面側の条件は表１に示す条件により作成した。また、ｉ型非晶質シリコン層２は膜厚１０ｎｍ、ｐ型非晶質シリコン層３１、３２はそれぞれ膜厚４ｎｍにして膜を形成した。

【００５４】

【表３】

処理		形成条件等			
		基板温度 (℃)	使用ガス	圧力 (Pa)	パワー密度 (mW/cm^2)
表側	水素処理	170	H_2 : 100sccm	50	15
	i-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm	50	15
	p-type a-Si (31)	170	H_2 : 400sccm SiH_4 : 20sccm B_2H_6: 10sccm	50	15
	p-type a-Si (32)	170	H_2 : 100sccm SiH_4 : 40sccm B_2H_6(2%) : 40sccm	50	15

【００５５】

そして、第２の実施形態と従来装置とを用意し、ＳＩＭＳにより、膜中の水素濃度プロファイル測定した。その結果を図６に示す。図６は、第２の実施形態におけるH.I.T. 構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層３１、３２とｉ型非晶質シリコン層２との界面部分の水素濃度プロファイルを示す図である。測定等の条件は第１の実施形態と同じである。

【００５６】

図６のＳＩＭＳで測定した水素濃度プロファイルから、図２と図５の模式図と同様の濃度プロファイルを確認でき、ｐ型非晶質シリコン層のｉ型非晶質シリコン層に近い側の前半部３１のみ高水素濃度として、後半部３２は従来装置と同等の水素濃度の勾配を持たせていることが分かる。

【００５７】

次に、この発明の第３の実施形態につき、図７及び図８を参照して説明する。図７は、この発明の第３の実施形態におけるH.I.T.構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを模式的に示したものである。

【００５８】

第３の実施形態は、ｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面近傍に、水素拡散抑制領域として、膜厚２ｎｍ程度の低水素濃度のｉ型トラップ層３３を設置したものである。この第３の実施形態では、ｉ型非晶質シリコン層２からｉ型トラップ層３３への水素拡散は生じるが、その影響はｐ型非晶質シリコン層までは及ばない。

【００５９】

第３の実施形態の形成条件を表４に示す。裏面側の条件は表１に示す条件と同じである。また、ｉ型トラップ層３３を含めたｉ型非晶質シリコン層２は膜厚１０ｎｍ、ｉ型トラップ層３３は２ｎｍ、ｐ型非晶質シリコン層３は膜厚８ｎｍにして膜を形成した。

【００６０】

【表４】

処理		形成条件等			
		基板温度 (℃)	使用ガス	圧力 (Pa)	パワー密度 (mW/cm^2)
表側	水素処理	170	H_2 : 100sccm	50	15
	i-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm	50	15
	i-type a-Si トラップ層(33)	170	SiH_4 : 40sccm	50	15
	p-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm B_2H_6(2%) : 40sccm	50	15

【００６１】

ｉ型トラップ層３３中の水素濃度をｉ型非晶質シリコン層よりも低くするため、この第３の実施形態では、ｉ型トラップ層３３の水素希釈を無くしたが、そのほかにも以下の方法がある。

【００６２】

（１）ｐ型非晶質シリコン層の形成時の基板温度をｉ型非晶質シリコン層の形成時よりも高くする。（２）ｐ型非晶質シリコン層の形成時の水素希釈量をｉ型非晶質シリコン層の形成時よりも低くする。（３）ｐ型非晶質シリコン層の形成時の成膜圧力をｉ型非晶質シリコン層の形成時よりも低くする。（４）ｐ型非晶質シリコン層の形成時のＲＦ投入電力をｉ型非晶質シリコン層の形成時よりも低くする。

【００６３】

第３の実施形態と従来装置とを用意し、ＳＩＭＳにより、膜中の水素濃度プロファイル測定した。その結果を図８に示す。図８は、第３の実施形態におけるII．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層３、ｉ型トラップ層３３とｉ型非晶質シリコン層２との界面部分の水素濃度プロファイルを示す図である。測定等の条件は第１の実施形態と同じである。測定等の条件は第１の実施形態と同じである。

【００６４】

図８のＳＩＭＳで測定した水素濃度プロファイルから、図２と図７の模式図と同様の濃度プロファイルを確認でき、ｉ型非晶質シリコン層２からの水素拡散はトラップ層３３で捕獲できることがわかる。

【００６５】

次に、この発明の第４の実施形態につき、図９及び図１０を参照して説明する。図９は、この発明の第４の実施形態におけるH.I.T.構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを模式的に示したものである。

【００６６】

ｐ型非晶質シリコン層３とｉ型非晶質シリコン層２との界面近傍のｉ型非晶質シリコン層２の水素濃度はH.I.T.太陽電池の発電電圧に影響を及ぼす。ｉ型非晶質シリコン層２の後半部（ｐ型非晶質シリコン層３側）の水素濃度を高くすることで出力電圧を向上できることが分かっている。上記した第３の実施形態はこれとは逆の方向であり、ｐ型非晶質シリコン層３への水素拡散を防止することができるが、出力電圧はやや低下してしまう。そこで、この第４の実施形態では、膜厚２ｎｍ程度のトラップ層３４にボロン（Ｂ）をドープした。これにより、出力電圧を低下させることなくｐ型非晶質シリコン層３への水素拡散を防止することができる。

【００６７】
第４の実施形態の形成条件を表５に示す。裏面側の条件は表１に示す条件と同じである。また、ｉ型非晶質シリコン層２は膜厚１０ｎｍ、トラップ層３４は０．５ｎｍ、ｐ型非晶質シリコン層３は膜厚６ｎｍにして膜を形成した。
【００６８】
【表５】

処理		形成条件等			
		基板温度 (℃)	使用ガス	圧力 (Pa)	パワー密度 (mW/cm²)
表側	水素処理	170	H_2 : 100sccm	50	15
	i-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm	50	15
	トラップ層(34)	170	SiH_4 : 40sccm B_2H_6(2%) : 10sccm	50	15
	p-type a-Si	170	H_2 : 100sccm SiH_4 : 40sccm B_2H_6(2%) : 40sccm	50	15

【００６９】
第４の実施形態と従来装置とを用意し、ＳＩＭＳにより、膜中の水素濃度プロファイル測定した。その結果を図１０に示す。図１０は、第４の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層３、トラップ層３４とｉ型非晶質シリコン層２との界面部分の水素濃度プロファイルを示す図である。測定等の条件は第１の実施形態と同じである。測定等の条件は第１の実施形態と同じである。
【００７０】
図１０のＳＩＭＳで測定した水素濃度プロファイルから、図２と図９の模式図と同様の濃度プロファイルを確認でき、ｉ型非晶質シリコン層２からの水素拡散はトラップ層３４で捕獲できることがわかる。
【００７１】
次に、上記したこの発明の第１から第４の実施形態によるＨ．Ｉ．Ｔ．構造の太陽電池装置と従来の太陽電池装置を用意し、大気中で２５０℃、３時間の熱アニールを行い、その特性変化を測定した結果を表６に示す。
【００７２】

【表６】

		Voc (V)	Isc (A/cm²)	F.F.	Pmax (W)
従来技術	初期特性	0.706	3.820	0.772	2.082
	アニール後特性	0.684	3.811	0.753	1.963
	変化率	-3.12%	-0.24%	-2.46%	-5.72%
第１実施形態	初期特性	0.709	3.880	0.762	2.096
	アニール後特性	0.700	3.869	0.752	2.037
	変化率	-1.27%	-0.28%	-1.31%	-2.84%
第２実施形態	初期特性	0.707	3.850	0.769	2.090
	アニール後特性	0.699	3.835	0.758	2.032
	変化率	-1.13%	-0.39%	-1.43%	-2.78%
第３実施形態	初期特性	0.698	3.810	0.760	2.020
	アニール後特性	0.691	3.796	0.751	1.970
	変化率	-1.00%	-0.37%	-1.18%	-2.48%
第４実施形態	初期特性	0.707	3.790	0.775	2.080
	アニール後特性	0.701	3.783	0.767	2.034
	変化率	-0.85%	-0.18%	-1.03%	-2.21%

【００７３】

表６から分かるように、この発明の第１から第４の実施形態のように、ｐ型非晶質シリコン層とｉ型非晶質シリコン層との間に水素拡散抑制領域を設けることで、高温加熱による出力特性の低下を大幅に抑制できたことが確認できた。また、高温加熱を行っても出力特性の低下が抑制できることから、集電極として高温焼成の材料を使用することが可能となり、電極抵抗が低減できる。

【００７４】

次に、トラップ層３３、トラップ層４４の膜厚を変化させ、特性の変化を調べた。まず、第３の実施形態におけるｉ型トラップ層３３の膜厚を種々変化させてサンプルとなる太陽電池装置を形成した。ｉ型トラップ層３３の膜厚を変化させた以外は上記した形成条件でサンプルを作成した。そして、各サンプルを大気中で２５０℃、３時間の熱アニールを行い、その初期特性、変化率、アニール後特性を調べた。その結果を表７及び図１１ないし図１３に示す。特性はトラップ層３３を設けていない従来例の出力を１としてそれぞれ規格化した。図１１は、膜厚と初期特性との関係を示す特性図、図１２は、変化率として熱処理後の特性と初期特性の相対出力を求め、その膜厚との関係で示した特性図、図１３は、熱処理後の相対出力をその膜厚との関係で示した特性図である。

【００７５】

【表７】

膜厚(nm)	初期	変化率	アニール後特性
0	1	0.93	0.930
0.5	0.99	0.93	0.921
1.0	0.99	0.97	0.960
2.0	0.99	0.97	0.960
3.0	0.98	0.97	0.951
4.0	0.96	0.98	0.941
5.0	0.95	0.98	0.931
6.0	0.93	0.99	0.921
7.0	0.92	0.99	0.911

【００７６】

表６及び図１１ないし図１３より、ｉ型トラップ層３３を設ける場合、その膜厚を１ｎｍ以上５ｎｍ以下にすると、アニール後特性が従来例より向上していることが分かる。よって、ｉ型トラップ層３３の膜厚は、１ｎｍ以上５ｎｍ以下にすると良く、更に好ましくは１ｎｍ以上２ｎｍ以下である。なお、この膜厚は、所定の膜厚を有する膜を成膜した形成時間で求め、各サンプルを形成時間に基づいて算出した値である。

【００７７】

次に、第４の実施形態におけるボロン（Ｂ）をドープしたトラップ層３４の膜厚を種々変化させてサンプルとなる太陽電池装置を形成した。トラップ層３４の膜厚を変化させた以外は上記した形成条件でサンプルを作成した。そして、各サンプルを大気中で２５０℃、３時間の熱アニールを行い、その初期特性、変化率、アニール後特性を調べた。その結果を表８及び図１４ないし図１６に示す。特性はトラップ層３４を設けていない従来例の出力を１としてそれぞれ規格化した。図１４は、膜厚と初期特性との関係を示す特性図、図１５は、変化率として熱処理後の特性と初期特性の相対出力を求め、その膜厚との関係で示した特性図、図１６は、熱処理後の相対出力をその膜厚との関係で示した特性図である。

【００７８】

【表８】

膜厚(nm)	初期	変化率	アニール後特性
0	1	0.93	0.930
0.1	0.995	0.93	0.925
0.3	0.990	0.98	0.970
0.5	0.990	0.98	0.970
1.0	0.980	0.98	0.960
2.0	0.960	0.98	0.941
3.0	0.940	0.98	0.921
4.0	0.910	0.985	0.896
5.0	0.880	0.99	0.871

【００７９】

表８及び図１４ないし図１６より、トラップ層３４を設ける場合、その膜厚を０．１ｎｍ以上３ｎｍ未満にすると、アニール後特性が向上していることが分かり、更に０．３ｎｍ以上２ｎｍ以下になるとより特性が向上することが分かる。よって、トラップ層３４の膜厚は、０．１ｎｍ以上３ｎｍ未満にすると良く、更に好ましくは０．３ｎｍ以上２ｎｍ以下である。なお、この膜厚は、所定の膜厚を有する膜を成膜した形成時間で求め、各サンプルを形成時間に基づいて算出した値である。

【００８０】

なお、上記した実施形態においては、結晶系半導体基板として、単結晶シリコン基板を用いたが、多結晶シリコン基板などの多結晶半導体基板を用いても同様の効果が得られる。また、上記した実施形態においては、水素を含有する非晶質系半導体膜として、非晶質シリコン層を用いたが、これに限られず、非晶質シリコンカーバイト、非晶質シリコンゲルマニウム非晶質シリコン系合金や膜中に微少な結晶粒を含む半導体薄膜を用いても同様の効果が得られる。

【００８１】

今回開示された実施の形態はすべての点で例示であって制限的なものではないと考えられるべきである。本発明の範囲は、上記した実施の形態の説明ではなくて特許請求の範囲によって示され、特許請求の範囲と均等の意味および範囲内でのすべての変更が含まれることが意図される。

【図面の簡単な説明】

【００８２】

【図１】この発明が適用されるＨ．Ｉ．Ｔ．構造の光起電力装置を示す概略断面図である。

【図２】従来のＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを示す模式図である。

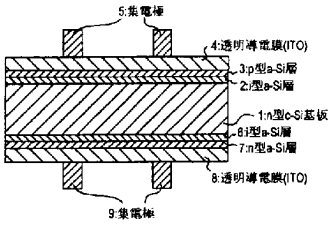
【図３】この発明の第１の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを示す模式図である。

【図４】この発明の第１の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面部分の水素濃度プロファイルを示す図である。

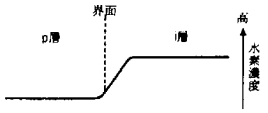
【図５】この発明の第２の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを示す模式図であ

る。
【図６】この発明の第２の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面部分の水素濃度プロファイルを示す図である。
【図７】この発明の第３の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを示す模式図である。
【図８】この発明の第３の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面部分の水素濃度プロファイルを示す図である。
【図９】この発明の第４の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池のｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面近傍の水素濃度プロファイルを示す模式図である。
【図１０】この発明の第４の実施形態におけるＨ．Ｉ．Ｔ．構造の太陽電池をＳＩＭＳで測定したｐ型非晶質シリコン層とｉ型非晶質シリコン層との界面部分の水素濃度プロファイルを示す図である。
【図１１】この発明の第３の実施形態におけるトラップ層の膜厚と初期特性との関係を示す特性図である。
【図１２】この発明の第３の実施形態における変化率として熱処理後の特性と初期特性の相対出力を求め、トラップ層の膜厚との関係で示した特性図である。
【図１３】この発明の第３の実施形態における熱処理後の相対出力をトラップ層の膜厚との関係で示した特性図である。
【図１４】この発明の第４の実施形態におけるトラップ層の膜厚と初期特性との関係を示す特性図である。
【図１５】この発明の第４の実施形態における変化率として熱処理後の特性と初期特性の相対出力を求め、トラップ層の膜厚との関係で示した特性図である。
【図１６】この発明の第４の実施形態における熱処理後の相対出力をトラップ層の膜厚との関係で示した特性図である。
【符号の説明】
【００８３】
１　ｎ型単結晶シリコン基板
２　ｉ型非晶質シリコン層
３　ｐ型非晶質シリコン層
４　ＩＴＯ膜
５　集電極
６　ｉ型非晶質シリコン層
７　ｎ型非晶質シリコン層
８　ＩＴＯ膜
９　集電極

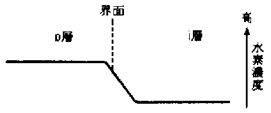
【図１】



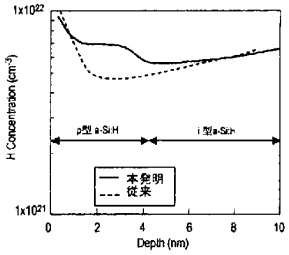
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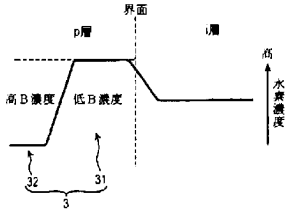
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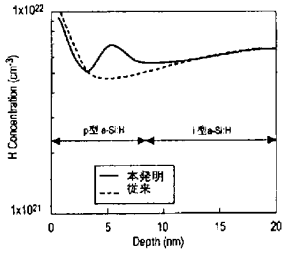
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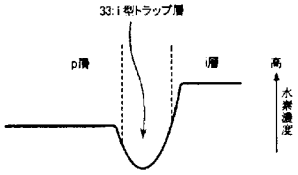
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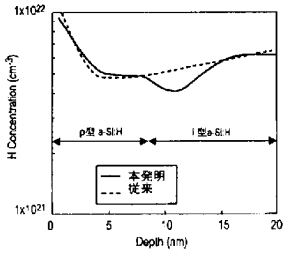
【図６】



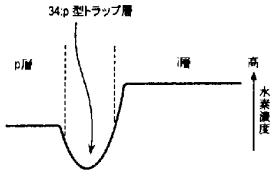
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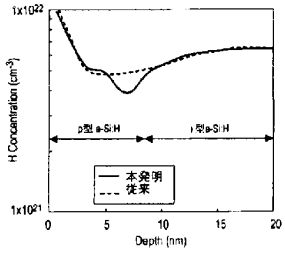
【図８】



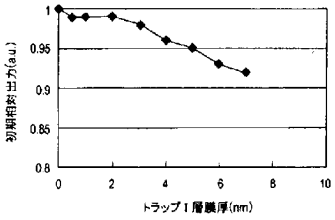
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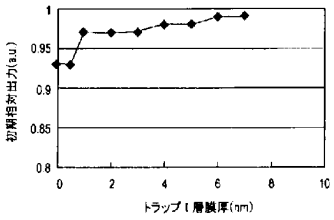
【図１０】



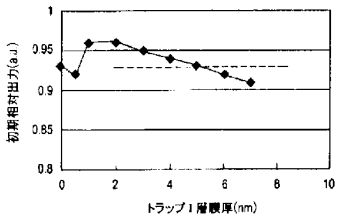
【図１１】



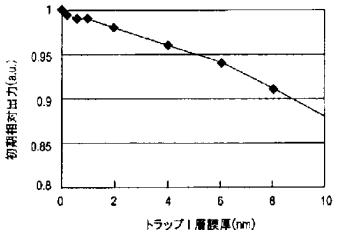
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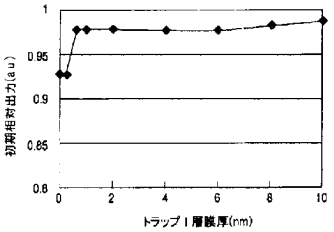
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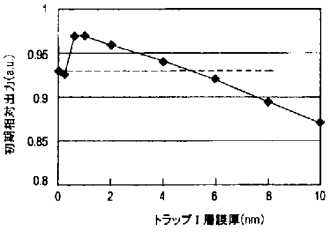
【図１４】



【図１５】



【図１６】



(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2007 年11 月8 日 (08.11.2007)

PCT

(10) 国際公開番号
WO 2007/125903 A1

(51) 国際特許分類:
H01L 31/042 (2006.01) *H01L 31/05* (2006.01)
H01L 31/04 (2006.01)

(21) 国際出願番号: PCT/JP2007/058818

(22) 国際出願日: 2007 年4 月24 日 (24.04.2007)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願2006-121930 2006 年4 月26 日 (26.04.2006) JP

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(81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

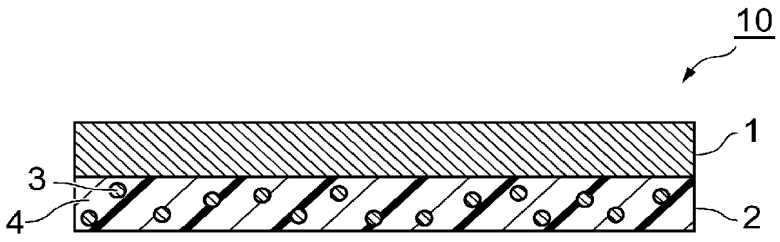
(84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書

２文字コード及び他の略語については、定期発行される各*PCT*ガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(54) **Title:** ADHESIVE TAPE AND SOLAR CELL MODULE USING THE SAME

(54) 発明の名称: 接着テープ及びそれを用いた太陽電池モジュール



(57) **Abstract:** An adhesive tape (10) and a solar cell module using the adhesive tape. The adhesive tape (10) electrically connects solar cells and has metal foil (1) and an adhesive agent layer (2) provided on at least one side of the metal foil (1) and made of an adhesive agent. The adhesive tape (10) can suppress a reduction in yielding of products and increase workability of connection of the solar cells.

(57) 要約: 本発明は、複数の太陽電池セルを電気的に接続するための接着テープであって、金属箔１と、金属箔１の少なくとも一方面上に設けられた、接着剤からなる接着剤層２とを備える接着テープ１０及びそれを用いた太陽電池モジュールを提供する。本発明の接着テープによれば、製品の歩留り低下を抑制でき、且つ太陽電池セルの接続作業性を向上させることができる。

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明 細 書

接着テープ及びそれを用いた太陽電池モジュール

技術分野

[0001] 本発明は、複数の太陽電池セルを電気的に接続するための接着テープ及びそれを用いた太陽電池モジュールに関する。

背景技術

[0002] 太陽電池モジュールは、光エネルギーを直接電気エネルギーに変換する太陽光発電装置である。太陽電池モジュールは、近年、クリーンエネルギーとして注目を集めており、今後その市場は急激に拡大すると予想されている。このような太陽電池モジュールは、一般的に、複数の太陽電池セルが電気的に接続された構造を有する。

[0003] 太陽電池セルを電気的に接続する方法として、従来、はんだを用いる方法が知られている(例えば特許文献1及び2参照)。はんだは、導通性や固着強度等の接続信頼性に優れ、安価で汎用性があることから広く用いられている。

[0004] 一方、はんだを使用せずに太陽電池セルを電気的に接続する方法として、導電性接着剤を使用する方法も開示されている(例えば特許文献3, 4, 5及び6参照)。

[0005] 特許文献1:特開2004－204256号公報
特許文献2:特開2005－050780号公報
特許文献3:特開2000－286436号公報
特許文献4:特開2001－357897号公報
特許文献5:特開平7－147424号公報
特許文献6:特開2005－101519号公報

発明の開示

発明が解決しようとする課題

[0006] しかしながら、はんだを用いる接続方法では、接続の際に高温(通常、はんだの溶融温度は230～260℃)を伴うため、被着体(太陽電池セル)に体積収縮等が生じ、太陽電池の特性劣化が生じることがあった。そのため、製品の歩留りが低下するという問題があった。

[0007] 特に、太陽電池モジュールにおいては、太陽電池セルの価格が太陽電池モジュールの価格の約40%を占め、また太陽電池市場の急速な拡大が予想されるため、将来、太陽電池セルの薄型化が求められることは必死である。そして、太陽電池セルの薄型化が進むと、接続の際に伴う高温により太陽電池セルの反り及び割れが生じ、さらに製品の歩留まり低下が顕著になるという問題もある。

[0008] さらに、はんだを用いる接続方法においては、はんだの特性上、被着体との接続界面の厚みをコントロールすることが難しく、パッケージ化する際の寸法精度を十分に得ることが難しかった。そして、十分な寸法精度が得られない場合にはパッケージングプロセスの際、製品の歩留まりの低下につながる。

[0009] 一方、導電性接着剤を使用する方法は、はんだを用いる方法よりも低温での接続が可能となるため、薄型化された太陽電池セルの電気的接続に適している。しかし、従来の導電性接着剤を使用する方法では、導電性接着剤を被着体に転写する工程が必要となり、太陽電池セルの接続作業性が低いという問題があった。

[0010] そこで、本発明は上記事情に鑑みてなされたものであり、製品の歩留り低下を抑制でき、且つ太陽電池セルの接続作業性を向上させることができる接着テープ及びそれを用いた太陽電池モジュールを提供することを目的とする。

課題を解決するための手段

[0011] 本発明は、複数の太陽電池セルを電気的に接続するための接着テープであって、金属箔と、金属箔の少なくとも一方面上に設けられた、接着剤からなる接着剤層とを備える接着テープを提供する。

[0012] 本発明の接着テープによれば、金属箔の少なくとも一方面上に接着剤層が設けられているため、太陽電池セル同士を接続するに際して、絶縁性基材上の接着剤層を基材から各太陽電池セルに転写する作業を省略することができる。また、はんだを用いて太陽電池セルを接続する場合よりも十分に低い温度で接続することが可能である。このため、接続の際における太陽電池セルの反り及び割れを十分に防止することができ、ひいては太陽電池モジュールの歩留りを十分に高くすることができる。

[0013] 上記接着剤は導電性粒子を含有することが好ましい。これにより、複数の太陽電池セルの電気的接続を容易に行うことができる。

[0014] 接着剤は、接続後の接続信頼性をより向上させるために、さらに熱硬化性樹脂を含有することが好ましい。

[0015] 金属箔は、導電性に優れることから、銅箔又はアルミニウム箔であることが好ましい。

[0016] 本発明の接着テープにおいては、接着剤層が金属箔の両面に設けられていることが好ましい。これによれば、接着テープの両面に太陽電池セルを接着できるため、太陽電池セルの直列接続及び並列接続のいずれも容易に行うことができる。

[0017] 本発明はまた、複数の太陽電池セルを有し、複数の太陽電池セルが接続部材によって電気的に接続され、接続部材が上述の接着テープを用いて形成されるものである太陽電池モジュールを提供する。このような太陽電池モジュールは、本発明の接着テープを用いているため、製品の歩留りを高くできるとともに、太陽電池セル同士の接続作業性を向上させることができる。このため、太陽電池モジュール作製の際のコストの低減が可能となる。

発明の効果

[0018] 本発明によれば、製品の歩留り低下を抑制でき、且つ太陽電池セルの接続作業性を向上させることができる接着テープ及びそれを用いた太陽電池モジュールが提供される。

図面の簡単な説明

[0019] [図1]本発明に係る接着テープの一実施形態を示す模式断面図である。

[図2]本発明に係る接着テープの他の実施形態を示す模式断面図である。

[図3]本発明に係る太陽電池モジュールの一実施形態を示す部分平面図である。

[図4]図3の太陽電池モジュールの底面図である。

[図5]図3のV－V線断面図である。

符号の説明

[0020] 1…金属箔、2，2a，2b…接着剤層、3…導電性粒子、4…絶縁性接着剤組成物、5a，5b…バス電極、6…発電部、7…フィンガー電極、8…裏面電極、10，20…接着テープ、100…太陽電池モジュール、101…太陽電池セル、102a，102b…接続層、120…接続部材。

発明を実施するための最良の形態

[0021] 以下、本発明の好適な実施形態について図面を用いて詳細に説明するが、本発明は以下の実施形態に限定されるものではない。なお、図面中、同一要素には同一符号を付すこととし、重複する説明は省略する。また、上下左右等の位置関係は、特に断らない限り、図面に示す位置関係に基づくものとする。さらに、図面の寸法比率は図示の比率に限られるものではない。

[0022] 図1は、本発明に係る接着テープの第1実施形態を示す模式断面図である。図1に示す接着テープ10は、金属箔1の片面に、接着剤層2が設けられた構造を有する。

[0023] 図2は、本発明に係る接着テープの第2実施形態を示す模式断面図である。図2に示す接着テープ20は、金属箔1の両面に接着剤層2a及び2bが設けられた構造を有する。

[0024] 接着剤層2，2a及び2bは、それぞれ導電性粒子3及び絶縁性接着剤組成物4を含む接着剤からなる。なお、第1及び第2実施形態では接着剤層2，2a及び2bが導電性粒子3を含む実施形態を示したが、接着剤層2，2a及び2bは導電性粒子3を含有していなくともよい。すなわち、金属箔1を、接着剤層を介して、後述する太陽電池セルの電極に押し付けることによって金属箔1と太陽電池セルの電極とを直接接触させることができる場合には、接着剤層2，2a及び2bは導電性粒子を含有していなくともよい。ただし、接着剤層2，2a及び2bが導電性粒子3を含有することにより、太陽電池セル同士の電気的接続をより安定して行うことが可能となる。

[0025] 金属箔1としては、例えば、銅、アルミニウム、鉄、金、銀、ニッケルパラジウム、クロム、モリブデン又はそれらの合金の箔が挙げられる。この中で、導電性に優れることから、銅箔及びアルミニウム箔が好ましい。このような金属箔1の厚みは、接続信頼性等の観点から、10～200μmであることが好ましい。

[0026] 導電性粒子3としては、例えば、金粒子、銀粒子、銅粒子、ニッケル(Ni)粒子、金めっきニッケル粒子、金／ニッケルめっきプラスチック粒子、銅めっき粒子、ニッケルめっき粒子が挙げられる。これらの導電性粒子は、接続時の被着体表面の凹凸に対する導電性粒子の埋め込み性の観点から、毬栗状又は球状であることが好ましい。すなわち、毬栗状又は球状の導電性粒子は、被着体表面の複雑な凹凸形状に対し

ても埋め込み性が高く、接続後の振動や膨張等の変動に対して追随性が高いことから好ましい。

[0027] このような導電性粒子は、導電性を確保する点から、平均粒子径2～20μmであることが好ましい。また、導電性粒子の含有量は、接着剤全体の体積に対して0．1～20体積％であることが好ましい。導電性粒子の含有量が0．1体積％未満であると、導電性粒子による接続安定性効果が十分に発揮されない傾向にある。また、導電性粒子の含有量が20体積％を超えると、接着剤層の成形性が低下する傾向にある。

[0028] 絶縁性接着剤組成物4としては、熱可塑性材料や、熱や光に対して硬化性を示す材料を用いることができる。この絶縁性接着剤組成物4は、接続後の高温高湿下における接続信頼性を向上させる観点から、熱硬化性樹脂を含有することが好ましい。熱硬化性樹脂としては、例えば、エポキシ樹脂、ポリイミド樹脂、不飽和ポリエステル樹脂、ポリウレタン樹脂、ビスマレイミド樹脂、トリアジンービスマレイミド樹脂及びフェノール樹脂が挙げられる。これらの中では耐熱性を向上させる観点から、エポキシ樹脂が好ましい。エポキシ樹脂としては、エピクロルヒドリンと、ビスフェノールA、ビスフェノールF、ビスフェノールAD及び／又はビスフェノールAF等とから誘導されるビスフェノール型エポキシ樹脂；エピクロルヒドリンと、フェノールノボラック及び／又はクレゾールノボラックとから誘導されるエポキシノボラック樹脂；ナフタレン環を含んだ骨格を有するナフタレン系エポキシ樹脂；グリシジルアミン、グリシジルエーテル、ビフェニル、脂環式等の1分子内に2個以上のグリシジル基を有する各種のエポキシ化合物が挙げられる。これらは1種を単独で又は2種以上を混合して用いられる。

[0029] このような熱硬化性樹脂の含有量は、絶縁性接着剤組成物4の全量に対して、10～80質量％であることが好ましく、15～70質量％であることがより好ましい。この含有量が10質量％未満であると、上記範囲内にある場合と比較して、接着剤の流動性及び作業性が低下する傾向にある。この含有量が80質量％を超えると、上記範囲内にある場合と比較して、接着テープの接着性が低下する傾向にある。

[0030] 絶縁性接着剤組成物4は、熱硬化性樹脂とともに熱硬化性樹脂用硬化剤をさらに含んでいてもよい。

[0031] 熱硬化性樹脂用硬化剤とは、熱硬化性樹脂とともに加熱した場合に、熱硬化性樹

脂の硬化を促進する硬化剤を示す。その具体例としては、イミダゾール系硬化剤、ヒドラジド系硬化剤、アミン系硬化剤、フェノール系硬化剤、酸無水物系硬化剤、三フッ化ホウ素－アミン錯体、スルホニウム塩、ヨードニウム塩、ポリアミンの塩、アミンイミド及びジシアンジアミドが挙げられる。これらの中で、熱硬化性樹脂としてエポキシ樹脂が用いられる場合には、イミダゾール系硬化剤、ヒドラジド系硬化剤、三フッ化ホウ素アミン錯体、スルホニウム塩、アミンイミド、ポリアミンの塩又はジシアンジアミドが好適に用いられる。

[0032] このような熱硬化性樹脂用硬化剤の含有量は、絶縁性接着剤組成物4の全量に対して、2～10質量％であることが好ましく、4～8質量％であることがより好ましい。この含有量が2質量％未満であると、上記範囲内にある場合と比較して、接着テープの接着性が低下する傾向にある。この含有量が10質量％を超えると、上記範囲内にある場合と比較して、接着テープの保存の際の安定性が低下する傾向にある。

[0033] また、接着剤層2，2a及び2bは、膜厚寸法精度や圧着時の圧力配分の観点から、フィルム状であることが好ましい。この場合、接着剤層2，2a及び2bを構成する絶縁性接着剤組成物4は、上述の熱硬化性樹脂及び熱硬化性樹脂用硬化剤のほか、フィルム形成材をさらに含有する。

[0034] フィルム形成材としては、より良好にフィルムを形成できるという観点から、フェノキシ樹脂、ポリエステル樹脂及びポリアミド樹脂等の熱可塑性の高分子が好ましく、フェノキシ樹脂がより好ましい。これらのフィルム形成性高分子の重量平均分子量は、接着フィルムの流動性の観点から、10000～10000000であることが好ましい。このフィルム形成性高分子の重量平均分子量が10000未満であると、上記範囲内にある場合と比較して、接着剤層2の成形性の形成性が低下する傾向にある。このフィルム形成性高分子の重量平均分子量が10000000を超えると、上記範囲内にある場合と比較して、接着剤層の硬化時の応力緩和効果及び作業性が低下する傾向にある。

[0035] このようなフィルム形成性高分子の含有量は、絶縁性接着剤組成物4の全量に対して、2～80質量％であることが好ましく、5～70質量％であることがより好ましい。フィルム形成性高分子の含有量が2質量％未満であると、上記数値範囲にある場合と比較して、硬化時の応力緩和効果及び接着性向上効果が低下する傾向にあり、80質

量%を超えると接着剤層の流動性及び作業性が低下する傾向にある。

[0036] 絶縁性接着剤組成物4は、必要に応じて、カップリング剤、分散剤及びキレート材料等の添加剤をさらに含有していてもよい。

[0037] カップリング剤は、被着体との接着性や濡れ性を改善するために用いられる。その具体例としては、シラン系カップリング剤、チタネート系カップリング剤が挙げられる。分散剤は、導電性粒子3の分散性を向上させるために用いられる。その具体例としては、リン酸カルシウム及び炭酸カルシウムが挙げられる。キレート材料は、銀や銅等の金属マイグレーション等を抑制するために用いられる。その具体例としては、無機イオン交換体が挙げられる。

[0038] これらの添加剤を用いる場合、その含有量は、絶縁性接着剤組成物4の全量に対して、0.1～10質量%であることが好ましく、0.2～8質量%であることがより好ましい。この含有量が0.1質量%未満であると、上記範囲にある場合と比較して、添加剤を含有することによる効果が小さい。この含有量が10質量%を超えると、上記範囲内にある場合と比較して、接着テープの保存の際の安定性が低下する傾向にある。

[0039] また、絶縁性接着剤組成物4は、熱可塑性樹脂、ラジカル重合性化合物及びラジカル重合開始剤を含有するものであってもよい。

[0040] 熱可塑性樹脂としては、ポリアミド類、フェノキシ樹脂類、ポリ(メタ)アクリレート類、ポリイミド類、ポリウレタン類、ポリエステル類、ポリビニルブチラール類等を用いることができる。これらの樹脂は、必要に応じて単独あるいは2種以上混合して用いてもよい。なお、これらの熱可塑性樹脂の一般的な重量平均分子量は5000～150000である。

[0041] ラジカル重合性化合物としては、(メタ)アクリル基、(メタ)アクリロイル基やビニル基等、分子内にオレフィンを有する化合物であれば、特に制限なく公知のものを使用することができる。この中でも(メタ)アクリロイル基を有するラジカル重合性化合物であることが好ましい。

[0042] ラジカル重合性化合物の具体例としては、例えば、エポキシ(メタ)アクリレートオリゴマー、ウレタン(メタ)アクリレートオリゴマー、ポリエーテル(メタ)アクリレートオリゴマー、ポリエステル(メタ)アクリレートオリゴマー等のオリゴマー、トリメチロールプロパントリ

(メタ)アクリレート、ポリエチレングリコールジ(メタ)アクリレート、ポリアルキレングリコールジ(メタ)アクリレート、ジシクロペンテニル(メタ)アクリレート、ジシクロペンテニロキシエチル(メタ)アクリレート、ネオペンチルグリコールジ(メタ)アクリレート、ジペンタエリスリトールヘキサ(メタ)アクリレート、イソシアヌル酸変性2官能(メタ)アクリレート、イソシアヌル酸変性3官能(メタ)アクリレート、2，2'－ジ(メタ)アクリロイロキシジエチルホスフェート、2－(メタ)アクリロイロキシエチルアシッドホスフェート等の多官能(メタ)アクリレート化合物が挙げられる。これらの化合物は、必要に応じて単独あるいは2種以上混合して用いてもよい。

[0043] ラジカル重合開始剤としては、従来から知られている過酸化物やアゾ化合物等公知の化合物を用いることができる。具体的には、クミルパーオキシネオデカノエート、1，1，3，3－テトラメチルブチルパーオキシネオデカノエート、1－シクロヘキシル－1－メチルエチルパーオキシネオデカノエート、t－ヘキシルパーオキシネオデカノエート、t－ブチルパーオキシネオデカノエート、t－ブチルパーオキシピバレート、1，1，3，3－テトラメチルブチルパーオキシ－2－エチルヘキサノエート、2，5－ジメチル－2，5－ジ(2－エチルヘキサノイルパーオキシ)ヘキサン、t－ヘキシルパーオキシ－2－エチルヘキサノエート、t－ブチルパーオキシ－2－エチルヘキサノエート、t－ブチルパーオキシネオヘプタノエート、t－アミルパーオキシ－2－エチルヘキサノエート、ジ－t－ブチルパーオキシヘキサヒドロテレフタレート、t－アミルパーオキシ－3，5，5－トリメチルヘキサノエート、3－ヒドロキシ－1，1－ジメチルブチルパーオキシネオデカノエート、1，1，3，3－テトラメチルブチルパーオキシ－2－エチルヘキサノエート、t－アミルパーオキシネオデカノエート、t－アミルパーオキシ－2－エチルヘキサノエート、2，2'－アゾビス－2，4－ジメチルバレロニトリル、1，1'－アゾビス(1－アセトキシ－1－フェニルエタン)、2，2'－アゾビスイソブチロニトリル、2，2'－アゾビス(2－メチルブチロニトリル)、ジメチル－2，2'－アゾビスイソブチロニトリル、4，4'－アゾビス(4－シアノバレリン酸)、1，1'－アゾビス(1－シクロヘキサンカルボニトリル)、t－ヘキシルパーオキシイソプロピルモノカーボネート、t－ブチルパーオキシマレイン酸、t－ブチルパーオキシ－3，5，5－トリメチルヘキサノエート、t－ブチルパーオキシラウレート、2，5－ジメチル－2，5－ジ(3－メチルベンゾイルパーオキシ

)ヘキサン、t－ブチルパーオキシ－2－エチルヘキシルモノカーボネート、t－ヘキシルパーオキシベンゾエート、2，5－ジメチル－2，5－ジ(ベンゾイルパーオキシ)ヘキサン、t－ブチルパーオキシベンゾエート、ジブチルパーオキシトリメチルアジペート、t－アミルパーオキシノルマルオクトエート、t－アミルパーオキシイソノナノエート、t－アミルパーオキシベンゾエート等が挙げられる。これらの化合物は、単独で用いても、2種以上を混合して用いてもよい。

[0044] なお、熱可塑性樹脂、ラジカル重合性化合物及びラジカル重合開始剤を含有する絶縁性接着剤組成物4においても、必要に応じて添加剤をさらに含有することができる。

[0045] 上述の接着剤層2，2a及び2bの厚みは、接着性及び導電性を考慮すると、5～50μmであることが好ましい。さらに、接着剤層2，2a及び2bの厚みは、接続信頼性を考慮すると、8～40μmであることがより好ましい。接着剤層2，2a及び2bの厚みは、接着剤の不揮発性成分の量の調整や、アプリケータやリップコータのギャップの調整により制御することができる。

[0046] 上述の接着テープによれば、製品の歩留り低下を抑制でき、且つ太陽電池セルの接続作業性を向上させることができる。

[0047] このような接着テープは、従来公知の方法により作製することができ、例えば次のような方法で作製することができる。

[0048] まず、上述の絶縁性接着剤組成物4の構成成分を含む接着剤組成物を有機溶剤に溶解あるいは分散することで液状化して塗布液を調製する。この塗布液を金属箔の片面又は両面上に塗布した後、溶剤を除去することにより、接着剤層を形成することができる。このとき、絶縁性接着剤組成物4の構成成分に熱硬化性樹脂及び熱硬化性樹脂用硬化剤が含まれている場合には、塗布液の乾燥は熱硬化樹脂用硬化剤の活性温度未満で行う。このようにして得られる片面又は両面に接着剤層が形成された金属箔を適当な幅にスリットすることにより、上述の接着テープが得られる。

[0049] このときの有機溶剤としては、例えば酢酸エチル等のエステル系溶剤を用いることができる。また、塗布液は、ロールコーター、スリットダイコーター、ディップコーター、スピンコーター、アプリケータ及びリップコータ等の塗布装置を用いて塗布することが

できる。なお、金属箔の両面に接着剤層が形成された接着テープを作製する場合には、片面に接着剤層を形成した後にもう一方の面に接着剤層を形成してもよく、ディップコーター等を用いて金属箔の両面に塗布液を塗布した後にこれを乾燥してもよい。

[0050] 本発明の接着テープは、太陽電池セルの接続に好適に用いることができる。太陽電池モジュールでは、一般的に、表面電極を備えた太陽電池セルが複数個、直列及び／又は並列に接続されている。接続された太陽電池セルは、耐環境性のために、強化ガラス等で挟み込まれ、太陽電池セルと強化ガラスとの間隙が透明性のある樹脂によって埋められている。本発明の接着テープは、複数の太陽電池セルを直列及び／又は並列に接続する用途に特に好適に用いられる。

[0051] 本発明の太陽電池モジュールは、複数の太陽電池セルを有し、複数の太陽電池セルが上述の接着テープを用いて電気的に接続されたものである。

[0052] ここで、図3，4及び5は、本発明の一実施形態である太陽電池モジュールの要部を示す図であり、複数の太陽電池セルが相互に接続された構造の概略を示している。図3は本実施形態における太陽電池モジュールの一部切欠き部分平面図であり、図4は図3の太陽電池モジュールの一部切欠き底面図であり、図5は、図3におけるV－V線断面図を示す。なお、図3及び図4においては後述する接続部材120の一部を切欠いて示してある。

[0053] 図3，4及び5に示すように、本実施形態の太陽電池モジュール100は、複数の太陽電池セル101を有する。各太陽電池セル101は板状の発電部6を有している。発電部6は、太陽光によって起電力を生じさせるものであり、例えば半導体ウエハを用いて形成されているものである。発電部6の表面側には、複数本（図3～5では6本）のフィンガー電極7が並設されている。そして、フィンガー電極7の上には、フィンガー電極7と交差するように複数本（図3～5では2本）のバス電極5aが設けられている。ここで、フィンガー電極7とバス電極5aとは接触している。

[0054] 一方、発電部6の裏面側には、裏面電極8が設けられ、裏面電極8の上には、複数本（図3～5では2本）のバス電極5bが設けられている。ここで、裏面電極8とバス電極5bとは接触している。

[0055] そして、2つの太陽電池セル101同士は、接続部材120によって接続されている。具体的には、接続部材120の一端は、一方の太陽電池セル101におけるバス電極5aに接続され、接続部材120の他端は、他方の太陽電池セル101におけるバス電極5bに接続されている。すなわち、太陽電池セル101同士は直列に接続されている。接続部材120は、金属箔1と、その両面にそれぞれ設けられる接続層102a，102bとで構成されている。バス電極5bに接触しているのは接続層102aであり、バス電極5aに接触しているのは接続層102bである。

[0056] ここで、接続部材120は、接着テープ20を用いて形成されるものである。接続層102a，102bは、接着テープ20における接着剤層2a，2bにそれぞれ対応する。このとき、絶縁性接着剤組成物4の構成成分に熱硬化性樹脂及び熱硬化性樹脂用硬化剤が含まれている場合には、少なくともバス電極5a及び5bに対応する部分の接続層102a，102bは、後述する方法等により硬化処理されている。従って、少なくともバス電極5a及び5bに対応する部分の接続層102a，102bは、それぞれ導電粒子3と、絶縁性接着剤組成物4の硬化体とで構成されている。

[0057] そして、太陽電池モジュール100では、上述の接続部材120により接続された太陽電池セル101が強化ガラス（図示せず）等で挟みこまれ、太陽電池セル101と強化ガラスとの間隙が透明性のある樹脂（図示せず）によって埋められる。

[0058] 半導体ウエハの材料としては、例えば、シリコンの単結晶、多結晶及び非結晶等の半導体が挙げられる。

[0059] フィンガー電極7、バス電極5a及び5b、並びに裏面電極8の材料としては、導電性を有する公知の材料として一般的なもの、例えば、銀を含有したガラスペーストや接着剤樹脂に各種の導電粒子を分散した銀ペースト、金ペースト、カーボンペースト、ニッケルペースト、アルミペースト及び焼成や蒸着によって形成されるITOが挙げられる。この中で、耐熱性、導電性、安定性及びコストの観点から、銀を含有したガラスペーストからなる電極が好適に用いられる。フィンガー電極7、バス電極5a及び5b、並びに裏面電極8は、半導体ウエハ6上に、例えば、スクリーン印刷等によって形成することができる。

[0060] 絶縁性接着剤組成物4の構成成分に熱硬化性樹脂及び熱硬化性樹脂用硬化剤

が含まれている場合における上述の接着テープ20の硬化処理は、例えば、140～200℃、0．5～4MPaで、5～20秒間加熱加圧することにより行うことができる。また、絶縁性接着剤組成物4の構成成分に熱可塑性樹脂、ラジカル重合性化合物及びラジカル重合開始剤が含まれている場合における上述の接着テープ20の硬化処理は、例えば、140～200℃、0．1～10MPaで、0．5～120秒間加熱加圧することにより行うことができる。この硬化処理により、バス電極5a及び5bに対して接着テープ20を圧着することができ、接着テープ20における接着剤層2a及び2bの少なくともバス電極5a及び5bに対応する部分が硬化して、接着テープ20は接続部材120となる。

[0061] かかる構成を有する太陽電池モジュール100は、上述した接着テープを用いているため、製品の歩留りを高くできるとともに、太陽電池セル同士の接続作業性を向上させることができる。このため、太陽電池モジュール作製の際のコストの低減が可能となる。

実施例

[0062] 次に実施例により本発明を詳細に説明するが、本発明はこれに限定されるものではない。

[0063] （実施例1）

（1）接着テープの作製

フェノキシ樹脂（高分子量エポキシ樹脂）（ユニオンカーバイト社製、商品名「PKHC」）50gとエポキシ樹脂（ジャパンエポキシレジン社製、商品名「YL－980」）20g及びイミダゾール5gを酢酸エチル中に添加し、30質量％の酢酸エチル溶液を調製し、これに平均粒径2．5μmの毬栗状のNi粒子を、固形成分全体の体積に対して5体積％添加した。得られた混合液を厚み75μmの銅箔の片面にロールコーターを用いて塗布した。これを、110℃で5分間乾燥し、片面に厚み30μmの接着剤層が形成された金属箔を得た。これを幅2．0mmにスリットし、接着テープを得た。なお、接着剤層の厚みは、マイクロメータ（Mtutoyo Corp社製、ID－C112）を用いて測定した。

[0064] （2）接着テープを用いた太陽電池セルの接続

この接着テープを太陽電池セル（厚み150μm，15cm×15cm）上に形成されて

いる電極配線(材質:銀ガラスペースト、2mm×15cm、Rz=10μm、Ry=14μm)の幅方向に合わせ、圧着ツール(装置名AC-S300、日化設備エンジニアリング社製)を用いて170℃, 2MPaで, 20秒間加熱加圧して、実施例1の接着テープ付き太陽電池セルを得た。

[0065] (実施例2)

接着剤層の厚みを40μmとしたこと以外は実施例1と同様として、実施例2の接着テープ付き太陽電池セルを得た。

[0066] (実施例3)

平均粒径2.5μmの毬栗状のNi粒子に代えて、平均粒子径5μmの金めっきNi粒子を用いたこと以外は実施例1と同様として、実施例3の接着テープ付き太陽電池セルを得た。

[0067] (実施例4)

平均粒径2.5μmの毬栗状のNi粒子に代えて、平均粒子径が10μmの金/Niめっきプラスチック(スチレン-ブタジエン共重合体)粒子を、固形成分全体の体積に対して0.5体積%を用いたこと以外は実施例1と同様として、実施例4の接着テープ付き太陽電池セルを得た。

[0068] (実施例5)

銅箔に代えてアルミニウム箔を用いたこと以外は実施例1と同様として、実施例5の接着テープ付き太陽電池セルを得た。

[0069] (実施例6)

厚み75μmの銅箔に代えて、厚み175μmの銅箔を用いたこと以外は実施例1と同様として、実施例6の接着テープ付き太陽電池セルを得た。

[0070] (実施例7)

Ni粒子を添加しなかったこと以外は実施例1と同様として、実施例7の接着テープ付き太陽電池セルを得た。

[0071] (比較例1)

接着テープに代えてTAB線を用い、TAB線と電極配線とをはんだを用いて接続することにより、比較例1の接着テープ付き太陽電池セルを得た。

[0072] (太陽電池の評価)

実施例1～7及び比較例1で得られた接着テープ付き太陽電池セルについて太陽電池のF．F．(曲線因子)を測定した(初期値)。F．F．については、初期測定の終わったセルを85℃，85%RH下に暴露し、1500時間経過後の値も測定した(終値)。ワコム電創社製ソーラシミュレータ(WXS－155S－10，AM1．5G)を用いてIVカーブを測定し、初期値から終値を減じた値をDelta(F．F．)とした。なお、Delta(F．F．)が0．2以上の場合には、接続信頼性が十分でない。

[0073] さらに、セル歩留り、接着剤層成形性及び接着テープ成形性についても評価した。セル歩留りは、太陽電池セル10枚中、接着テープを圧着した後のセルの状態を観察し、割れや剥離のあるものを除いた割合(%)を示す。また、接着剤層成形性については、φ50μm以上の欠点が無い場合をA、φ50μm以上の欠点がある場合をBとして評価した。接着テープ成形性については金属箔において接着剤層の浮きや剥離が無い場合をA、金属箔において接着剤層の浮きや剥離が有る場合をBとして評価した。以上の実施例1～7についての、接着テープの材料の構成等を表1に、実施例1～7及び比較例1についての評価結果を表2に示す。

[0074] [表1]

		実施例1	実施例2	実施例3	実施例4	実施例5	実施例6	実施例7
絶縁性接着剤	フェノキシ樹脂(g)	50	50	50	50	50	50	50
	エポキシ樹脂(g)	20	20	20	20	20	20	20
	イミダゾール(g)	5	5	5	5	5	5	5
	厚み(μm)	30	40	30	30	30	30	30
導電性粒子	種類	毬栗状Ni粒子	毬栗状Ni粒子	金めっきNi粒子	金／Niめっきプラスチック粒子	毬栗状Ni粒子	毬栗状Ni粒子	無
	平均粒子径(μm)	2.5	2.5	5	10	2.5	2.5	−
	含有量(体積%)	5	5	5	0.5	5	5	0
金属箔	種類	銅箔	銅箔	銅箔	銅箔	アルミニウム箔	銅箔	銅箔
	厚み(μm)	75	75	75	75	75	175	75

[0075] [表2]

	実施例1	実施例2	実施例3	実施例4	実施例5	実施例6	実施例7	比較例1
Delta (F. F.)	0. 03	0. 03	0. 02	0. 04	0. 04	0. 02	0. 05	0. 03
セル歩留まり(%)	100	100	100	100	100	100	100	60
接着剤層成形性	A	A	A	A	A	A	A	−
テープ成形性	A	A	A	A	A	A	A	−

請求の範囲

[1] 複数の太陽電池セルを電気的に接続するための接着テープであって、

金属箔と、該金属箔の少なくとも一方面上に設けられた、接着剤からなる接着剤層と、を備える、接着テープ。

[2] 前記接着剤が導電性粒子を含有する、請求項1記載の接着テープ。

[3] 前記接着剤がさらに熱硬化性樹脂を含有する、請求項1又は2記載の接着テープ。

[4] 前記金属箔が銅箔又はアルミニウム箔である、請求項1～3のいずれか一項に記載の接着テープ。

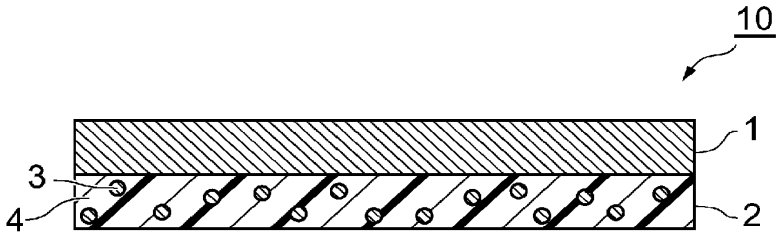
[5] 前記接着剤層が前記金属箔の両面に設けられた、請求項1～4のいずれか一項に記載の接着テープ。

[6] 複数の太陽電池セルを有し、

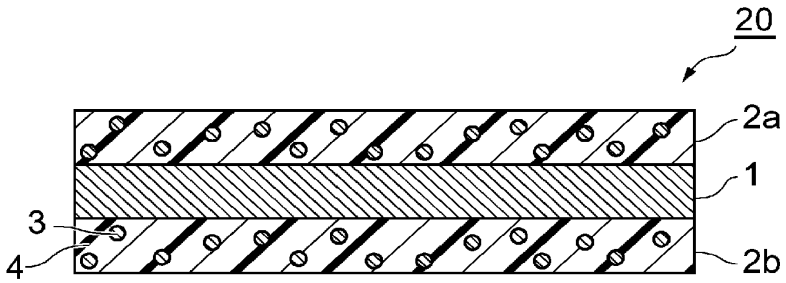
前記複数の太陽電池セルが接続部材によって電気的に接続され、

前記接続部材が請求項1～5のいずれか一項に記載の接着テープを用いて形成されるものである、太陽電池モジュール。

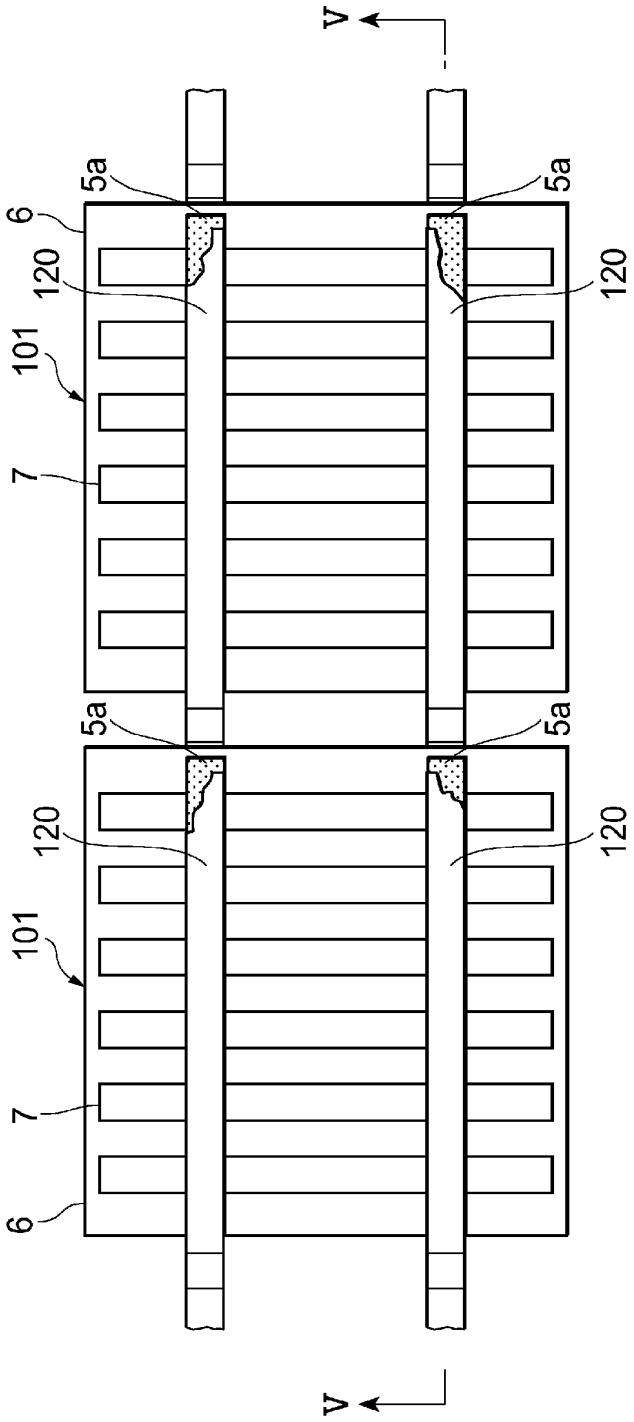
[図1]



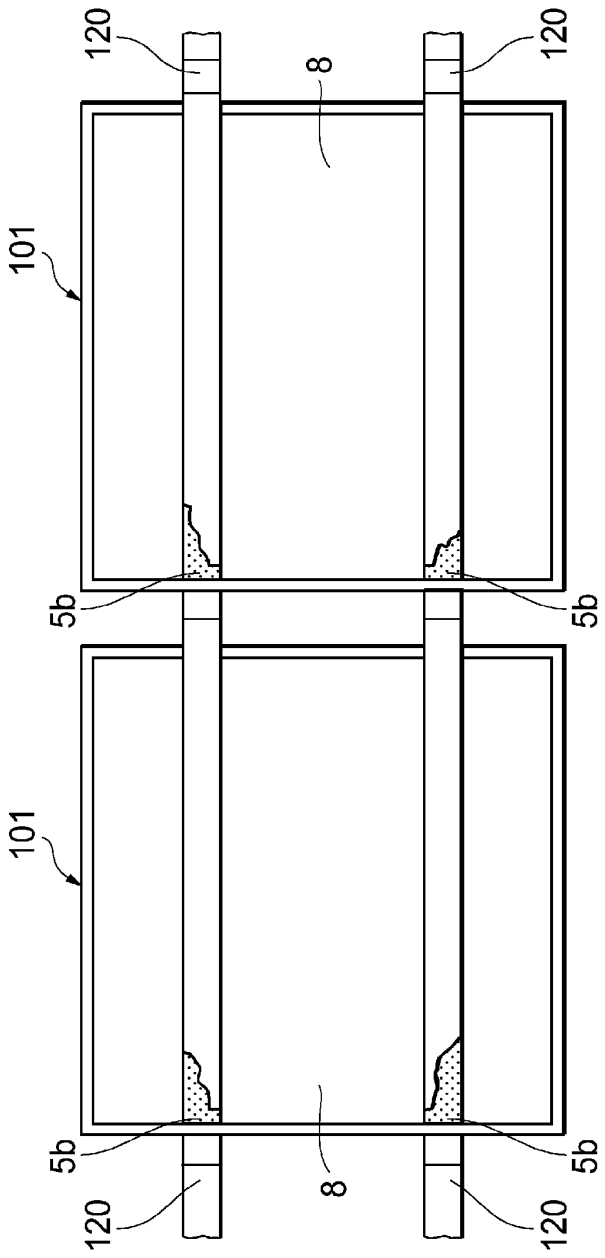
[図2]



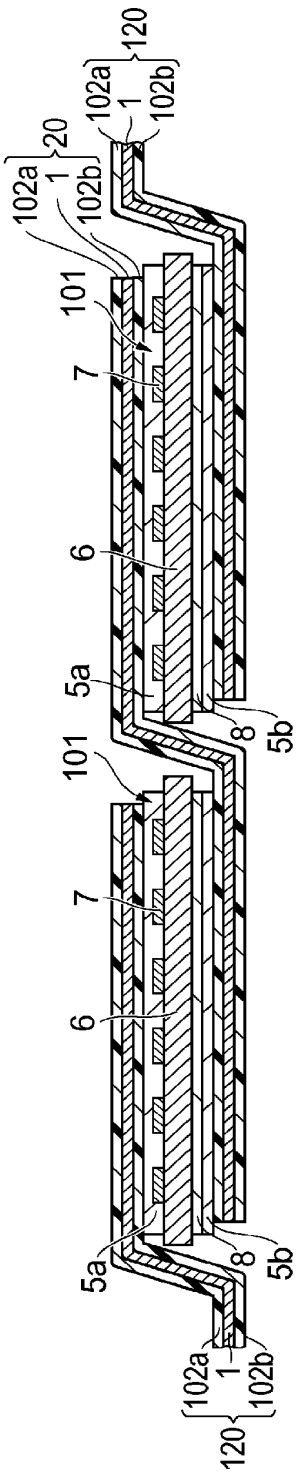
[図3]



[図4]



[図5]


120
102a
1
102b
20
102a
1
102b
101
7
6
5a
8
5b
101
7
6
5a
8
5b
102a
1
102b
120

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/058818

A. CLASSIFICATION OF SUBJECT MATTER
H01L31/042(2006.01)i, *H01L31/04*(2006.01)i, *H01L31/05*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L31/04(2006.01)i-*H01L31/078*(2006.01)i,
C09J7/00(2006.01)i-*C09J7/04*(2006.01)i

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2007
Kokai Jitsuyo Shinan Koho	1971-2007	Toroku Jitsuyo Shinan Koho	1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 6-196743 A (Canon Inc.), 15 July, 1994 (15.07.94), Par. No. [0039] (Family: none)	1-2,4,6
Y	JP 11-80682 A (Bridgestone Corp.), 26 March, 1999 (26.03.99), Par. Nos. [0002], [0003], [0031], [0034] (Family: none)	1-6
Y	JP 10-326904 A (Fuji Electric Co., Ltd.), 08 December, 1998 (08.12.98), Par. No. [0012] (Family: none)	1-6

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 May, 2007 (10.05.07)	22 May, 2007 (22.05.07)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2007/058818

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 4-152679 A (Showa Shell Sekiyu Kabushiki Kaisha), 26 May, 1992 (26.05.92), Page 2, upper left column & US 5248345 A & EP 0482511 A1	1-6
A	JP 2000-323739 A (Kaneka Corp.), 24 November, 2000 (24.11.00), Par. No. [0022] (Family: none)	1-6
A	WO 2005/086557 A1 (Bridgestone Corp.), 15 September, 2005 (15.09.05), Par. Nos. [0010], [0011] (Family: none)	1-6
A	JP 10-93125 A (Sanyo Electric Co., Ltd.), 10 April, 1998 (10.04.98), Fig. 1 (Family: none)	1-6

国際調査報告

国際出願番号　ＰＣＴ／ＪＰ２００７／０５８８１８

Ａ．　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Int.Cl.　H01L31/042(2006.01)i, H01L31/04(2006.01)i, H01L31/05(2006.01)i

Ｂ．　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Int.Cl.　H01L31/04(2006.01)i - H01L31/078(2006.01)i, C09J7/00(2006.01)i - C09J 7/04(2006.01)i

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	１９２２－１９９６年
日本国公開実用新案公報	１９７１－２００７年
日本国実用新案登録公報	１９９６　２００７年
日本国登録実用新案公報	１９９４－２００７年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

Ｃ．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Ｘ	ＪＰ　６－１９６７４３　Ａ（キヤノン株式会社） １９９４．０７．１５，段落【００３９】（ファミリーなし）	1-2, 4, 6
Ｙ	ＪＰ　１１－８０６８２　Ａ（株式会社ブリヂストン） １９９９．０３．２６，段落【０００２】，【０００３】，【００３１】，【００３４】（ファミリーなし）	1-6

☑ Ｃ欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
１０．０５．２００７	２２．０５．２００７

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	
日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００－８９１５ 東京都千代田区霞が関三丁目４番３号	加藤　昌伸	２Ｋ　３７００
	電話番号　０３－３５８１－１１０１　内線　３２５５	

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（２００５年４月）

Ｃ（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Ｙ	ＪＰ　１０－３２６９０４　Ａ（富士電機株式会社） １９９８．１２．０８，段落【００１２】（ファミリーなし）	1-6
Ａ	ＪＰ　４－１５２６７９　Ａ（昭和シェル石油株式会社） １９９２．０５．２６，第２頁左上欄 ＆　ＵＳ　５２４８３４５　Ａ ＆　ＥＰ　０４８２５１１　Ａ１	1-6
Ａ	ＪＰ　２０００－３２３７３９　Ａ（鐘淵化学工業株式会社） ２０００．１１．２４，段落【００２２】（ファミリーなし）	1-6
Ａ	ＷＯ　２００５／０８６５５７　Ａ１（株式会社ブリヂストン） ２００５．０９．１５，段落［００１０］，［００１１］ （ファミリーなし）	1-6
Ａ	ＪＰ　１０－９３１２５　Ａ（三洋電機株式会社） １９９８．０４．１０，図１（ファミリーなし）	1-6

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
13. März 2008 (13.03.2008)

PCT

(10) Internationale Veröffentlichungsnummer
WO 2008/028625 A2

(51) Internationale Patentklassifikation:
H01L 31/18 (2006.01)

(21) Internationales Aktenzeichen: PCT/EP2007/007703

(22) Internationales Anmeldedatum:
4. September 2007 (04.09.2007)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
10 2006 041 424.1
4. September 2006 (04.09.2006) DE

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Veröffentlicht:
— *ohne internationalen Recherchenbericht und erneut zu veröffentlichen nach Erhalt des Berichts*

WO 2008/028625 A2

(54) **Title:** METHOD FOR SIMULTANEOUSLY DOPING AND OXIDIZING SEMICONDUCTOR SUBSTRATES, AND ITS USE

(54) **Bezeichnung:** VERFAHREN ZUR SIMULTANEN DOTIERUNG UND OXIDATION VON HALBLEITERSUBSTRATEN UND DESSEN VERWENDUNG

(57) **Abstract:** The invention relates to a method for simultaneously doping and oxidizing semiconductor substrates and to doped and oxidized semiconductor substrates which have been produced in this manner. The invention also relates to the use of this method for producing solar cells.

(57) **Zusammenfassung:** Die Erfindung betrifft ein Verfahren zur simultanen Dotierung und Oxidation von Halbleitersubstraten sowie derart hergestellte dotierte und oxidierte Halbleitersubstrate. Weiterhin betrifft die Erfindung die Verwendung dieses Verfahrens zur Herstellung von Solarzellen.

Verfahren zur simultanen Dotierung und Oxidation von Halbleitersubstraten und dessen Verwendung

Die Erfindung betrifft ein Verfahren zur simultanen Dotierung und Oxidation von Halbleitersubstraten sowie derart hergestellte dotierte und oxidierte Halbleitersubstrate. Weiterhin betrifft die Erfindung die Verwendung dieses Verfahrens zur Herstellung von Solarzellen.

Moderne Solarzellenkonzepte enthalten zum einen oberflächennah dotierte Bereiche beispielsweise zur Erzeugung des pn-Übergangs oder sog. Front- oder Backsurfacefields. Hier kann beispielsweise eine Phosphoreindiffusion in p-dotiertes Silicium zur Emittererzeugung angewendet werden. Des Weiteren weisen exzellente Solarzellen dielektrisch passivierte Oberflächenbereiche auf, die die Rekombination der erzeugten Ladungsträgerpaare unterdrücken und auch die optischen Eigenschaften des Halbleiterbauelemen-

tes vorteilhaft beeinflussen. Derartige Schichten können mit PVD-Verfahren oder durch thermische Prozesse erzeugt werden. Im Falle von Siliciumdioxid auf Silicium wird eine thermische Oxidation unter Beisein von Sauerstoff und für eine feuchte Oxidation unter zusätzlichem Beisein von Wasserdampf durchgeführt. Gegenwärtig werden diese Prozessschritte sequentiell durchgeführt, wodurch der Herstellungsprozess beispielsweise von Solarzellen verkompliziert wird, da er mindestens einen thermischen Diffusionsprozess und einen Oxidationsprozess enthält. Werden diese Schritte sequentiell ausgeführt, ist mit weiteren zusätzlichen Schritten zu rechnen, die gewährleisten, dass in den Prozessschritten nur die dafür vorgesehenen Bereiche der Wafer bearbeitet werden, z.B. Maskierungs- oder Ätzschritte.

Im Folgenden sollen die einzelnen Verfahrensschritte, die für die die Solarzellenherstellung von Bedeutung sind, kurz erläutert werden.

Eine Diffusion von Dotieratomen kann auf unterschiedliche Weise erfolgen. Gemeinsam ist allen aus dem Stand der Technik bekannten Prozessen, dass eine Dotierstoffquelle vorliegt, aus der der Dotierstoff unter geeigneten Bedingungen in das Silicium übertritt. Diese Dotierquelle kann in der gasförmigen Atmosphäre vorliegen, z.B. $POCl_3$, oder kann durch geeignete Verfahren abgeschieden werden, z.B. kann Phosphorsäure aufgesprüht werden. Des Weiteren können CVD-Prozesse eingesetzt werden um dotierte Schichten zu erzeugen.

Beim Vorgang der Ionenimplantation werden die Dotieratome in den Wafer implantiert. Der Wafer wird dazu hochenergetischen, Dotieratome enthaltenden, Teilchenstrahlen ausgesetzt. Die Atome dringen dann in

den Wafer ein und es wird die Dotierung in einem nachfolgenden Annealingschritt bei erhöhter Temperatur aktiviert und nach Wunsch umverteilt. Bei der Aktivierung bewegen sich die in das Kristallgitter eingetriebenen Atome auf freie Gitterplätze und können dann als Dotierstoff dienen. Bei der Umverteilung verändert sich durch Diffusion der Dotieratome das Konzentrationsprofil der Dotieratome durch Diffusion innerhalb des Halbleiters. In beiden Fällen liegt während der thermischen Behandlung keine äußere Dotieratomquelle mehr vor und der Teilchenstrahl ist abgeschaltet.

Die thermische Oxidation von Silicium ist in der Halbleitertechnologie weit verbreitet. Im Wesentlichen wird in sauerstoffhaltiger Atmosphäre an der Oberfläche des Si-Kristalls befindliches Silicium bei erhöhten Temperaturen oxidiert. Dieses Oxid bildet mit dem darunter liegenden Siliciumsubstrat eine SiO_2/Si Grenzfläche. Während des Oxidwachstums wird Silicium in Oxid umgesetzt und die Grenzfläche verschiebt sich so, dass die SiO_2-Schichtdicke wächst. Dabei nimmt die Wachstumsrate ab, da die oxidierenden Atmosphärenbestandteile durch immer dicker werdende Oxidschichten an die SiO_2/Si Grenzfläche diffundieren müssen. Die Kinetik dieser Reaktion hängt von der Kristallorientierung, Dotierung und von den oxidierenden Atmosphärenbestandteilen ab. Beispielsweise kann durch Hinzugabe von Wasserdampf (Feuchtoxidation) die Oxidation beschleunigt werden. Auch DCE (trans-1,2-dichloroethylene) kann die Reaktionsgeschwindigkeit beeinflussen (O. Schultz, High-Efficiency Multicrystalline Silicon Solar Cells, Dissertation an der Universität Konstanz, Fakultät für Physik (2005), S. 103). Weiterhin ist die Kinetik sehr stark von der Temperatur, die bei der Oxidation vor-

herrscht, bestimmt.

Die SiO_2/Si Grenzfläche kann bei geeigneter Prozessführung so ausgebildet werden, dass sie passiviert ist. Das bedeutet, dass die Rekombinationsrate der Minoritätsladungsträger gegenüber einer unpassivierten Oberfläche reduziert ist (O. Schultz, High-Efficiency Multicrystalline Silicon Solar Cells, Dissertation an der Universität Konstanz, Fakultät für Physik (2005), S. 104 ff.).

Als Gettern bezeichnet man einen Prozess, bei dem gezielt Verunreinigungen von einem Bereich des Halbleiters in einen anderen überführt werden können (A.A. Istratov et al., Advanced Gettering Techniques in ULSI Technology, MRS Bulletin (2000), S. 33-38). Dieser Vorgang kann durch unterschiedliche Verfahren realisiert werden. Eines ist das Phosphorgettern. Während einer Phosphordiffusion entstehen Siliciumzwischengitteratome, die die Beweglichkeit von vielen Verunreinigungstypen erhöhen. Durch die höhere Löslichkeit dieser Komponenten in hochdotierten Siliciumbereichen, sammeln sich diese während des Hochtemperaturschrittes folglich in diesen Arealen und das Volumen des Halbleiters wird gereinigt.

Da während der reinen Oxidation kein Gettern beobachtet wird, ist dieser Prozess besonders anfällig für Verunreinigungen, die sich entweder auf oder in dem Substrat befinden, in verunreinigten Prozess- und Handlingsgeräten bzw. in verunreinigten Prozessgasen oder Prozesshilfsmitteln.

Ausgehend hiervon war es Aufgabe der vorliegenden Erfindung, die bekannten Verfahren zur Herstellung von Solarzellen hinsichtlich der einzelnen Verfahrens-

schritte zu optimieren und eine einfachere Herstellung zu ermöglichen.

Diese Aufgabe wird durch das Verfahren mit den Merkmalen des Anspruchs 1 und das hiernach hergestellte dotierte und oxidierte Halbleitersubstrat mit den Merkmalen des Anspruchs 29 gelöst. Weiterhin wird die Verwendung mit den Merkmalen des Anspruchs 30 bereitgestellt. Die weiteren abhängigen Ansprüche zeigen vorteilhafte Weiterbildungen auf.

Erfindungsgemäß wird ein Verfahren zur simultanen Dotierung und Oxidation von Halbleitersubstraten bereitgestellt, bei dem zumindest eine Oberfläche des Halbleitersubstrats zumindest bereichsweise mit mindestens einer einen Dotierstoff enthaltenen Schicht beschichtet wird. Es können auch mehrere Dotierstoffe in der mindestens einen Dotierstoff-Schicht enthalten sein. Im Anschluss erfolgt dann eine thermische Behandlung in einer Atmosphäre, die ein Oxidationsmittel für das Halbleitermaterial enthält, wodurch eine Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrats ermöglicht wird. Bei der thermischen Behandlung erfolgt ebenso eine partielle Oxidation der nicht mit der Dotierstoff-Schicht beschichteten Oberflächenbereiche des Halbleitersubstrats. Es können so auf einfache Weise zwei Prozessschritte verbunden werden, was zur Vereinfachung des Gesamtprozesses führt.

Vorzugsweise besteht die den Dotierstoff enthaltende Schicht aus einem Material oder enthält ein Material, das ausgewählt ist aus der Gruppe bestehend aus amorphem Silicium, Siliciumdioxid, Siliciumcarbid, Siliciumnitrid, Aluminiumoxid, Titandioxid, Tantaloxid, dielektrischen Materialien, keramischen Materialien,

Materialien enthaltend organische Verbindungen, die im Diffusionsprozess chemisch veränderbar sind, nicht-stöchiometrischen Abwandlungen dieser Materialien und Mischungen dieser Materialien. Unter nicht-stöchiometrischen Abwandlungen sind beispielsweise im Hinblick auf Siliciumnitrid Zusammensetzungen zu verstehen, die von dem stöchiometrischen Verhältnis Si_3N_4 abweichen.

Ebenso ist es möglich, wie aus der Halbleitertechnologie bekannt, Substanzen einzusetzen, die beispielsweise zunächst in flüssiger oder pastöser Form vorliegen. Diese werden dann auf dem Halbleiter deponiert, beispielsweise durch Aufschleudern, Sprühen, Tauchbeschichten, Drucken oder CVD. Im Anschluss kann dann ein Trockenschritt folgen, in dem ein Teil der organischen Bestandteile austritt. In einem weiteren Schritt kann dann die Substanz in eine glasartige Konsistenz überführt werden, die dann im nachfolgenden Hochtemperaturprozess als Diffusionsquelle oder auch als Barriere dient. Derartige Substanzen können nach dem bekannten Sol-Gel-Verfahren hergestellt und verarbeitet werden.

Der Dotierstoff wird vorzugsweise ausgewählt aus der Gruppe bestehend aus Phosphor, Bor, Arsen, Aluminium und Gallium.

Vorzugsweise weist die den Dotierstoff enthaltende Schicht einen Konzentrationsgradienten hinsichtlich des Dotierstoffs auf, wobei in dem dem Halbleitersubstrat zugewandten Bereich eine höhere Dotierstoff-Konzentration herrscht.

Hinsichtlich der Beschichtung des Halbleitersubstrats bestehen verschiedene Alternativen. So sieht eine

erste bevorzugte Variante vor, dass das Halbleitersubstrat auf einer Oberfläche mit einer einen Dotierstoff enthaltenden Schicht durchgängig beschichtet wird und anschließend durch thermische Behandlung mit einer ein Oxidationsmittel enthaltenden Atmosphäre eine partielle Oxidation der nicht-beschichteten Oberflächen, z.B. der Rückseite des Halbleitersubstrats, erfolgt. Eine andere Variante sieht vor, dass eine oder mehrere Oberflächen des Halbleitersubstrats lediglich bereichsweise mit einer einen Dotierstoff enthaltenden Schicht beschichtet werden, wodurch auch unbeschichtete Bereiche zurückbleiben. Im anschließenden Oxidationsschritt erfolgt dann eine partielle Oxidation der nicht-beschichteten Oberflächen des Halbleitersubstrats.

Grundsätzlich ist es so, dass das erfindungsgemäße Verfahren mit beliebigen Prozessschritten, die für die Bearbeitung von Halbleitersubstraten und insbesondere bei der Herstellung von Solarzellen bekannt sind, zu beliebigen Zeitpunkten kombiniert werden können. So ist es z.B. möglich, dass das Halbleitersubstrat vor der Beschichtung mit der den Dotierstoff enthaltenden Schicht zumindest bereichsweise behandelt wurde. Ebenso ist es aber auch möglich, dass eine Behandlung nach der Beschichtung mit der den Dotierstoff enthaltenden Schicht und vor der thermischen Behandlung durchgeführt wird. Die Behandlungsschritte sind hierbei vorzugsweise ausgewählt aus der Gruppe bestehend aus einer nasschemischen oder trockenchemischen Bearbeitung, einer thermischen Bearbeitung, einer Beschichtung, einer mechanischen Bearbeitung, einer lasertechnischen Bearbeitung, einer Metallisierung, einer Siliciumbearbeitung, einer Reinigung, einer nass- oder trockenchemischen Texturierung, einer Beseitigung der Texturierung sowie Kombi-

nationen aus den genannten Behandlungsschritten. Es gibt hier eine Vielzahl von Kombinationen zwischen den genannten Behandlungsschritten. Beispielsweise können die Halbleitersubstrate nach der Beschichtung mit dem Dotierstoff mit dem Ziel bearbeitet werden, die unbeschichteten Bereiche für die thermische Behandlung vorzubereiten. Dies kann beispielsweise umfassen, dass bestehende Texturen ganz oder teilweise eingeebnet werden oder dass verschiedene Reinigungsvorgänge durchgeführt werden. Die Reinigung kann dabei sowohl nasschemischer wie trockenchemischer Natur sein. Ein anderes Beispiel betrifft die zumindest bereichsweise Entfernung von bestehenden Beschichtungen mit dem Ziel, eine Strukturierung der Beschichtung zu erreichen oder aber auch, um parasitäre Beschichtungen auf beispielsweise der Rückseite zu entfernen.

Eine weitere bevorzugte Variante sieht vor, dass vor der thermischen Behandlung das beschichtete Halbleitersubstrat nass- oder trockenchemisch behandelt wird. Ebenso besteht die Möglichkeit, die unbeschichteten Teile des Halbleiters zu ätzen, während die Beschichtung den restlichen Halbleiter maskiert. Auf diese Weise können geeignete Ausgangsbedingungen für die thermische Oxidation geschaffen werden, insbesondere kann so eine sehr hohe Passivierungsqualität erzielt werden.

Eine bevorzugte Variante sieht vor, dass auf dem Halbleitersubstrat mindestens eine weitere Beschichtung aufgebracht ist. So kann z.B. die den Dotierstoff enthaltende Schicht auf der vom Halbleitersubstrat abgewandten Seite mit einer Deckschicht als Diffusionsbarriere für den Dotierstoff versehen sein, um ein Austreten des Dotierstoffs zu verhindern. Diese Deckschicht besteht vorzugsweise aus einem Materi-

al, das ausgewählt ist aus der Gruppe bestehend aus amorphem Silicium, Siliciumdioxid, Siliciumcarbid, Siliciumnitrid, Aluminiumoxid, Titandioxid, Tantaloxid, dielektrischen Materialien, keramischen Materialien, Materialien enthaltend organische Verbindungen, die im Diffusionsprozess chemisch veränderbar sind, nicht-stöchiometrischen Abwandlungen dieser Materialien und Mischungen dieser Materialien. In einer weiteren bevorzugten Variante kann die Deckschicht auch mehrlagig aufgebaut sein, wobei die unterschiedlichen Lagen aus verschiedenen Materialien bestehen.

In einer bevorzugten Variante kann die mindestens eine Beschichtung in der Weise erfolgen, dass das Beschichtungsmaterial in flüssiger oder pastöser Form auf dem Halbleitersubstrat oder den bereits auf dem Halbleitersubstrat aufgebrachten Beschichtungen abgeschieden wird. Dies kann vorzugsweise durch Aufschleudern, Sprühen, Tauchbeschichten, Drucken oder CVD-Verfahren erfolgen. Im Anschluss kann dann ein Trockenschritt erfolgen, in dem ein Teil der organischen Bestandteile entfernt wird. In einem weiteren Schritt kann dann das Beschichtungsmaterial in eine glasartige Konsistenz überführt werden und dient bei dem nachfolgenden Hochtemperaturprozess als Diffusionsquelle oder auch als Barriere. Derartige Beschichtungsmaterialien können ebenso nach dem Sol-Gel-Verfahren hergestellt und verarbeitet werden. Ebenso können aber auch Beschichtungsverfahren und Dotierungsverfahren, wie sie aus dem Stand der Technik bekannt sind, angewendet werden. Hierzu wird auf S.K. Ghandhi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, 2. Auflage (1994), Kapitel 8. S. 510-586, verwiesen.

Eine weitere erfindungsgemäße Variante sieht vor, dass zwischen Halbleitersubstrat und der mindestens einen Dotierstoff-Schicht mindestens eine weitere Schicht aufgebracht ist, durch die die Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrates nicht vollständig unterdrückt bzw. behindert wird. Beispielsweise bildet sich auf Silicium üblicherweise eine native Siliciumdioxidschicht, die so dünn ist, dass eine Dotierung des Silicium dadurch nicht maskiert wird. Ebenso ist es möglich, dass andere Schichten aus vorherigen Prozessen oder Prozessschritten noch vorhanden sind, durch die die Diffusion aber nicht unterdrückt wird.

Die thermische Behandlung bei dem erfindungsgemäßen Verfahren erfolgt vorzugsweise in einem Rohrofen oder einem Durchlaufofen. Grundsätzlich ist es aber auch denkbar, dass die thermische Behandlung direkt in einem PECVD-Reaktor durchgeführt wird. Die thermische Behandlung erfolgt dabei vorzugsweise bei Temperaturen im Bereich von 600 bis 1150 °C.

Hinsichtlich des Oxidationsschrittes bestehen verschiedene Verfahrensvarianten. So kann eine trockene Oxidation unter Verwendung von Sauerstoff als Oxidationsmittel durchgeführt werden. Eine weitere bevorzugte Variante sieht vor, dass eine feuchte Oxidation durchgeführt wird, d.h. es wird Sauerstoff als Oxidationsmittel in Gegenwart von Wasserdampf eingesetzt. Die für die Oxidation eingesetzte Atmosphäre kann darüber hinaus weitere Verbindungen zur Steuerung des Oxidationsprozesses enthalten. Ebenso können der Atmosphäre Verbindungen zur Reinhaltung derselben zugesetzt werden. Hierzu zählt insbesondere trans-1,2-Dichlorethan.

Das Halbleitersubstrat besteht vorzugsweise aus Silicium, Germanium oder Galliumarsenid. Ebenso können auch bereits dotierte Halbleitersubstrate, die z.B. mit Phosphor, Bor, Arsen, Aluminium und/oder Gallium dotiert sind, eingesetzt werden. Es ist aber insbesondere bevorzugt, dass das Halbleitersubstrat in den oberflächennahen Bereichen neben bereits vorhandenen Dotierungen höchstens eine geringfügige Dotierung aufweist, die aus der zuvor abgeschiedenen Dotierstoffquelle stammt und durch eine zusätzliche thermische Behandlung vor der simultanen Diffusion und Oxidation gebildet worden ist. Bei der abschließenden thermischen Behandlung wird dann die Diffusion dieser Dotierstoffe verstärkt.

Es ist ebenso möglich, dass das Halbleitersubstrat bereits vor Durchführung des erfindungsgemäßen Verfahrens zumindest bereichsweise Strukturen, z.B. in Form einer Maskierung, aufweist, die eine thermische Oxidation des Halbleitersubstrats in diesen Bereichen unterdrücken oder behindern.

Eine weitere erfindungsgemäße Variante sieht vor, dass bei dem Verfahren durch Anreicherung von Verunreinigungen in dotierten Bereichen im Halbleitersubstrat ein Getterprozess durchgeführt wird. Dies ist insbesondere bei der Dotierung mit Phosphor im thermischen Prozess möglich. Gettern findet bei der Phosphordiffusion als Nebeneffekt statt. Die Verunreinigungen diffundieren in die Bereiche hoher Phosphorkonzentrationen, da sie dort besser löslich sind als im übrigen Volumen. Dort nehmen sie weniger Einfluss auf das Halbleiterbauelement. Bei einem reinen Oxidationsprozess, wie es aus dem Stand der Technik bekannt ist, kommt es dagegen nicht zu einem Gettervorgang, sodass hier sehr hohe Reinheitsanforderungen

eingehalten werden müssen. Somit weist das erfindungsgemäße Verfahren gegenüber dem Stand der Technik auch den Vorteil auf, dass hinsichtlich der Reinheitsbedingungen nicht derartig hohe Anforderungen einzuhalten sind, was auf den parallel ablaufenden Gettervorgang zurückzuführen ist.

Erfindungsgemäß wird ebenso ein dotiertes und oxidiertes Halbleitersubstrat bereitgestellt, das nach dem zuvor beschriebenen Verfahren herstellbar ist.

Verwendung findet das zuvor beschriebene Verfahren insbesondere bei der Herstellung von Solarzellen.

Die Erfindung soll im Folgenden an dem konkreten Beispiel von einem Bor-dotierten Siliciumsubstrat als Halbleitersubstrat und einem phosphorhaltigen Siliciumdioxid als Dotierstoffquelle dargestellt werden.

Der Siliciumwafer 1 wird beispielsweise in einer sog. PECVD-Beschichtungsanlage mit einem Phosphorhaltigen Siliciumoxid 2 einseitig beschichtet (Fig. 1).

Das Siliciumoxid 2 dient als Phosphorquelle und Schicht 3 als Barriere gegen austretenden Phosphor. Die andere Seite der Scheibe verbleibt unbeschichtet. Die so beschichtete Scheibe kann nun noch gereinigt werden, um die unbeschichtete Seite für den nachfolgenden thermischen Prozess vorzubehandeln. Diese Reinigung kann nass- oder trockentechnisch durchgeführt werden. Sind in dieser Reinigung Schritte enthalten, die die Schicht 3 angreifen, sind diese Schritte so kurz zu wählen, dass die Eigenschaft der Schicht 3 als Diffusionsbarriere zu dienen nicht verloren geht. Entsprechend kann auch die Schicht geeignet dick ausgebildet werden.

Anschließend erfolgt nun ein Hochtemperaturschritt. Dieser Schritt ist im Wesentlichen dadurch gekennzeichnet, dass auf der mit Schicht 2 beschichteten Seite der Phosphor aus Schicht 2 in das Silicium eindringt und eine geeignete Dotierkonzentration 4 in dem Wafer erreicht wird. Simultan bildet sich auf den nicht beschichteten Bereichen des Wafers ein thermisch gewachsenes Siliciumdioxid 5 aus (Fig. 2). Dieses Siliciumdioxid entsteht, wenn die Atmosphäre in dem Ofen, in welchem der Hochtemperaturprozess durchgeführt wird, Sauerstoff enthält. Zusätzlich zum Sauerstoff können auch Wasserdampf oder andere geeignete Substanzen in der Atmosphäre enthalten sein, die den Oxidationsprozess ermöglichen oder vorteilhaft beeinflussen, beispielsweise beschleunigen. Die oben genannten Schichten 2 und 3 können auch zu einer Schicht zusammengefasst werden, die einen geeigneten Verlauf der Konzentration des Dotierstoffes aufweist, so dass verhindert wird, dass dieser in unerwünschtem Maße aus der Schicht in die Prozessatmosphäre austritt. Im Wesentlichen muss die Schicht lediglich auf geeignete Weise gewährleisten, dass die zu oxidierende Seite nicht durch austretenden Dotierstoff unvorteilhaft beeinflusst wird.

Wie bereits zuvor beschrieben, ist auch die bereichsweise Beschichtung möglich. Dies kann durch Verwendung entsprechender Masken oder auch durch gezieltes Rückätzen erfolgen. In Fig. 3 ist ein Siliciumwafer 1 vor der thermischen Behandlung zur simultanen Diffusion und Oxidation dargestellt. Eine erste Oberfläche weist hier Bereiche mit einer phosphorhaltigen Siliciumoxidschicht 2 auf. Das Siliciumoxid 2 dient dabei als Phosphorquelle. Gleichzeitig sind auf diesen Bereichen Deckschichten aus Siliciumdioxid 3 abgeschie-

den. Durch die thermische Behandlung zur Diffusion und Oxidation erhält man dann einen Aufbau, wie er in Fig. 4 dargestellt ist. Dieser Hochtemperaturschritt bewirkt, dass auf der mit Schicht 2 beschichteten Seite der Phosphor aus Schicht 2 in den Siliciumwafer 1 eindringt und eine geeignete Dotierkonzentration 4 in dem Wafer erreicht wird. Simultan bildet sich auf den nicht beschichteten Bereichen des Wafers ein thermisch gewachsenes Siliciumdioxid 5 aus.

Die oben beschriebene Erfindung kann auf vielfältige Weise, beispielsweise für die Herstellung von Solarzellen, eingesetzt werden. Zwei mögliche Prozessvarianten sind im Folgenden dargestellt:

Prozessvariante A

Es wird zunächst eine rückseitige geeignete Deckschicht aufgebracht und danach ein Ätzschritt durchgeführt, bei dem die Schichten 2 und 3 entfernt werden. Die Deckschicht schützt dabei die darunter liegende Schicht 5. Die Materialwahl für diese Schicht ist sehr frei. Die Schicht kann beispielsweise aus einem Dielektrikum, einem Metall, einer Keramik oder einem Schichtsystem bestehen. Anschließend wird auf der Vorderseite des Wafers eine Antireflexionsschicht 7 abgeschieden (Fig. 5).

Danach wird mit einem geeigneten Verfahren, z.B. mit einem Laser, das rückseitige Schichtsystem lokal geöffnet (Fig. 6).

Anschließend wird mit einem geeigneten Verfahren auf der Vorderseite und auf der Rückseite in frei wählbarer Reihenfolge eine geeignete Kontaktpaste angeordnet, z.B. mittels Siebdruck. Es können auf der Rück-

seite auch Pasten kombiniert werden, die eine einfache spätere Verschaltung der Solarzellen in Modulen erlauben (Fig. 7).

Im darauf folgenden Schritt werden die Kontakte ausgebildet, indem die Siliciumscheibe einem geeigneten thermischen Prozess ausgesetzt wird. Dieses sog. Kontaktsintern kann beispielsweise in einem Sinterofen durchgeführt werden, wie er bereits jetzt in der Solarzellenproduktionstechnologie bekannt ist (Fig. 8).

Der Herstellungsprozess der Solarzelle ist nun im Wesentlichen abgeschlossen. Auch hier können weitere Prozessschritte ein- oder angefügt werden, mit denen das Bauelement veredelt wird. Beispielsweise können eingangs nasschemische Oberflächenvorbehandlungen stattfinden, um die Reflexion der Siliciumscheibe durch eine sog. Texturierung zu reduzieren. Darüber hinaus können thermische Ausheilschritte oder Laserprozesse zur Kantenisolation angewendet werden.

Prozessvariante B

Nach Abscheidung der Antireflexionsschicht gemäß Fig. 3 in Variante A, wird hier die Kontaktpaste auf der Vorderseite angeordnet. Die Scheibe wird anschließend in einem geeigneten thermischen Prozess behandelt, wobei sich der Vorderseitenkontakt ausbildet (Fig. 9).

Anschließend wird auf der Rückseite der Solarzelle eine geeignete Metallschicht angeordnet. Dieser Schritt kann auch mit dem vorherigen kombiniert werden. Es ist allerdings hier wesentlich, dass die Metallschicht die darunter liegende Schichtfolge nicht bis zum Silicium durchdringt (Fig. 10).

Abschließend wird die rückseitige Metallschicht mit einem Laser derart bearbeitet, dass sie an dafür vorgesehenen Bereichen die darunter liegende Schichtfolge durchdringt und einen elektrischen Kontakt zum Silicium herstellt. Ist die Metallschicht beispielsweise aluminiumhaltig, so kann sie auch eine lokale p++ Dotierung an den Stellen der Laserbearbeitung ausbilden (Fig. 11).

Der Herstellungsprozess der Solarzelle ist nun im Wesentlichen abgeschlossen. Auch hier können weitere Prozessschritte ein- oder angefügt werden, mit denen das Bauelement veredelt wird. Beispielsweise können eingangs nasschemische Oberflächenvorbehandlungen stattfinden, um die Reflexion der Siliciumscheibe durch eine sog. Texturierung zu reduzieren. Darüber hinaus können thermische Ausheilschritte oder Laserprozesse zur Kantenisolation angewendet werden.

Patentansprüche

1. Verfahren zur simultanen Dotierung und Oxidation von Halbleitersubstraten, bei dem zumindest eine Oberfläche des Halbleitersubstrats zumindest bereichsweise mit mindestens einer mindestens einen Dotierstoff enthaltenden Schicht beschichtet wird und anschließend durch eine thermische Behandlung in einer ein Oxidationsmittel für das Halbleitermaterial enthaltenden Atmosphäre eine Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrats ermöglicht und eine Oxidation der nicht mit der Dotierstoff-Schicht beschichteten Oberflächenbereiche des Halbleitersubstrats erfolgt.

2. Verfahren nach Anspruch 1,
dadurch gekennzeichnet, dass die den Dotierstoff enthaltende Schicht aus einem Material besteht oder ein Material enthält, das ausgewählt ist aus der Gruppe bestehend aus amorphem Silicium, Siliciumdioxid, Siliciumcarbid, Siliciumnitrid, Aluminiumoxid, Titandioxid, Tantaloxid, dielektrische Materialien, keramische Materialien, Materialien enthaltend organischen Verbindungen, die im Diffusionsprozess chemisch veränderbar sind, nicht-stöchiometrischen Abwandlungen dieser Materialien und Mischungen dieser Materialien.

3. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass der Dotierstoff ausgewählt ist aus der Gruppe bestehend aus Phosphor, Bor, Arsen, Aluminium und Gallium.

4. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die den Dotierstoff enthaltende Schicht einen Konzentrationsgradienten hinsichtlich des Dotierstoffs aufweist, wobei in dem dem Halbleitersubstrat zugewandten Bereich eine höhere Dotierstoff-Konzentration herrscht.

5. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat auf einer Oberfläche des Halbleitersubstrats mit mindestens einer mindestens einen Dotierstoff enthaltenden Schicht beschichtet wird und anschließend durch eine thermische Behandlung in einer ein Oxidationsmittel für das Halbleitermaterial enthaltenden Atmosphäre eine Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrats ermöglicht und eine Oxidation der nicht mit der Dotierstoff-Schicht beschichteten Oberflächen des Halbleitersubstrats erfolgt.

6. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass mindestens eine Oberfläche des Halbleitersubstrats bereichsweise

mit mindestens einer mindestens einen Dotierstoff enthaltenden Schicht beschichtet wird und anschließend durch eine thermische Behandlung in einer ein Oxidationsmittel für das Halbleitermaterial enthaltenden Atmosphäre eine Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrats ermöglicht und eine Oxidation der nicht-beschichteten Oberflächenbereiche des Halbleitersubstrats erfolgt.

7. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat vor der Beschichtung mit der den Dotierstoff enthaltenden Schicht zumindest bereichsweise behandelt wurde.

8. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass nach der Beschichtung mit der den Dotierstoff enthaltenden Schicht und vor der thermischen Behandlung mindestens ein weiterer Behandlungsschritt des Halbleitersubstrats erfolgt.

9. Verfahren nach einem der beiden vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die Behandlungsschritte ausgewählt sind aus der Gruppe bestehend aus einer nasschemischen oder trockenchemischen Bearbeitung, einer thermischen Bearbeitung, einer Beschichtung, einer mechanischen Bearbeitung, einer lasertechnischen Bearbeitung, einer Metallisierung, einer Siliciumbearbeitung,

einer Reinigung, einer nass- oder trockenchemischen Texturierung, einer Beseitigung der Texturierung sowie Kombinationen aus den genannten Behandlungsschritten.

10. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass auf dem Halbleitersubstrat mindestens eine weitere Beschichtung aufgebracht ist.

11. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die den Dotierstoff enthaltende Schicht auf der vom Halbleitersubstrat abgewandten Seite mit einer Deckschicht als Diffusionsbarriere für den Dotierstoff versehen ist.

12. Verfahren nach dem vorhergehenden Anspruch,
dadurch gekennzeichnet, dass die Deckschicht aus einem Material besteht oder ein Material enthält, das ausgewählt ist aus der Gruppe bestehend aus amorphem Silicium, Siliciumdioxid, Siliciumcarbid, Siliciumnitrid, Aluminiumoxid, Titandioxid, Tantaloxid, dielektrische Materialien, keramische Materialien, Materialien enthaltend organischen Verbindungen, die im Diffusionsprozess chemisch veränderbar sind, nichtstöchiometrischen Abwandlungen dieser Materialien und Mischungen dieser Materialien.

13. Verfahren nach einem der beiden vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die Deckschicht mehrlagig aufgebaut ist.

14. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die mindestens eine Beschichtung in der Weise erfolgt, dass das Beschichtungsmaterial in flüssiger oder pastöser Form auf dem Halbleitersubstrat oder bereits vorliegenden Beschichtungen abgeschieden wird.

15. Verfahren nach dem vorhergehenden Anspruch,
dadurch gekennzeichnet, dass die abgeschiedene Schicht getrocknet sowie anschließend in eine glasartige Konsistenz überführt wird.

16. Verfahren nach dem vorhergehenden Anspruch,
dadurch gekennzeichnet, dass die Abscheidung des Beschichtungsmaterials durch Aufschleudern, Sprühen, Tauchbeschichten, Drucken und/oder CVD erfolgt.

17. Verfahren nach einem der beiden vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass mindestens ein Beschichtungsmaterial aus einem Sol-Gel besteht.

18. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass zwischen Halbleitersubstrat und der mindestens einen Dotier-

stoff-Schicht mindestens eine weitere Schicht aufgebracht ist, durch die die Diffusion des Dotierstoffs in das Volumen des Halbleitersubstrats nicht vollständig unterdrückt wird.

19. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die thermische Behandlung in einem Rohrofen oder einem Durchlaufofen erfolgt.

20. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die thermische Behandlung bei einer Temperatur im Bereich von 600 bis 1150 °C durchgeführt wird.

21. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass eine trockene Oxidation unter Verwendung von Sauerstoff als Oxidationsmittel durchgeführt wird.

22. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass eine feuchte Oxidation unter Verwendung von Sauerstoff als Oxidationsmittel in Gegenwart von Wasserdampf durchgeführt wird.

23. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass die für die Oxida-

tion eingesetzte Atmosphäre weitere Verbindungen zur Steuerung der Oxidation oder zur Reinhaltung der Atmosphäre, insbesondere trans-1,2-Dichlorethen enthält.

24. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat aus Silicium, Germanium oder Galliumarsenid besteht.

25. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat mit Phosphor, Bor, Arsen, Aluminium und/oder Gallium dotiert ist.

26. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat in den oberflächennahen Bereichen neben bereits vorhandenen Dotierungen höchstens eine geringfügige Dotierung aufweist, die aus der zuvor abgeschiedenen Dotierstoffquelle stammt und durch eine zusätzliche thermische Behandlung vor der simultanen Diffusion und Oxidation gebildet worden ist.

27. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass das Halbleitersubstrat zumindest bereichsweise Strukturen aufweist, die eine thermische Oxidation des Halb-

leitersubstrats in diesen Bereichen unterdrücken oder behindern.

28. Verfahren nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, dass bei dem Verfahren ein Getterprozess durch Anreicherung von Verunreinigungen in den dotierten Bereichen im Halbleitersubstrat erfolgt.

29. Dotiertes und oxidiertes Halbleitersubstrat herstellbar nach einem der vorhergehenden Ansprüche.

30. Verwendung des Verfahrens nach einem der Ansprüche 1 bis 28 zur Herstellung von Solarzellen.

Fig. 1

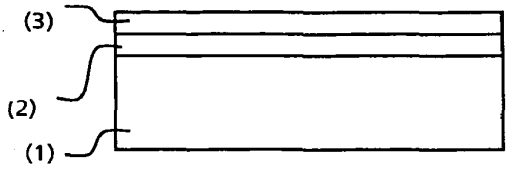


Fig. 2

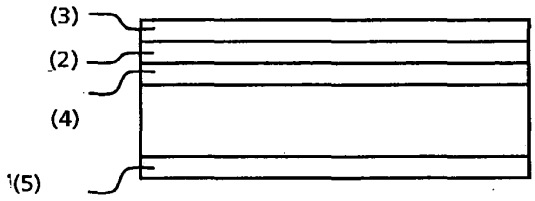


Fig. 3

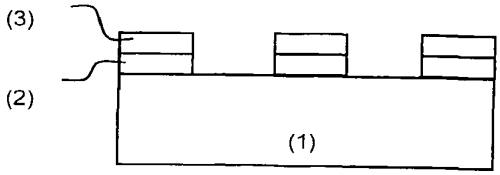


Fig. 4

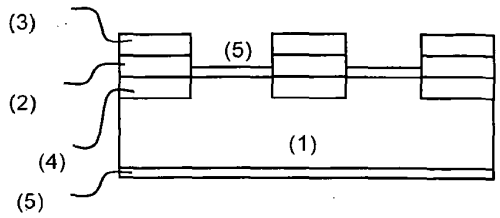


Fig. 5

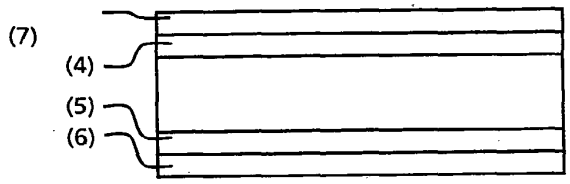


Fig. 6

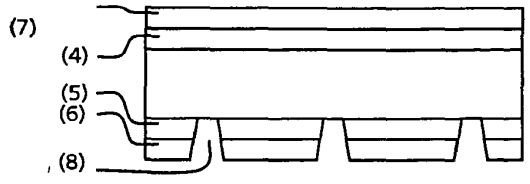


Fig. 7

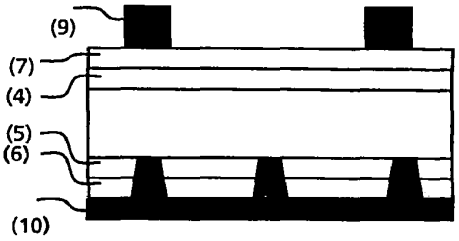


Fig. 8

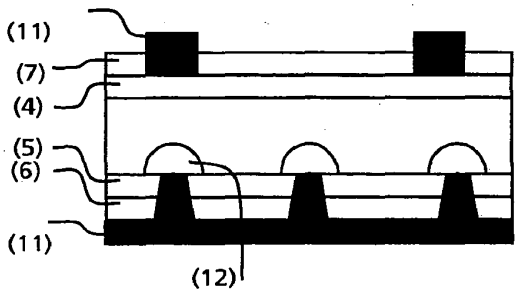


Fig. 9

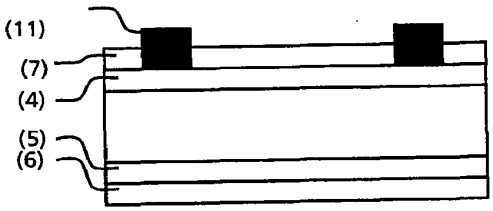


Fig. 10

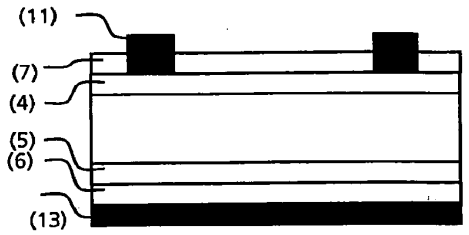
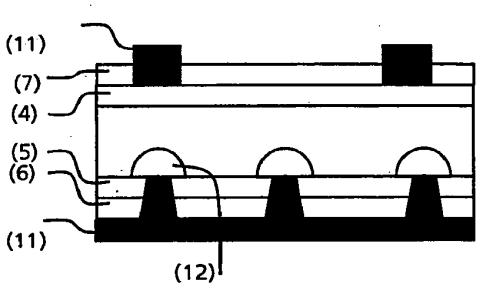


Fig. 11



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 September 2008 (25.09.2008)

PCT

(10) International Publication Number
WO 2008/115814 A2

(51) International Patent Classification:
H01L 31/0224 (2006.01)

(21) International Application Number:
PCT/US2008/057068

(22) International Filing Date: 14 March 2008 (14.03.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/895,217 16 March 2007 (16.03.2007) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *without international search report and to be republished upon receipt of that report*

(54) Title: SOLAR CELLS

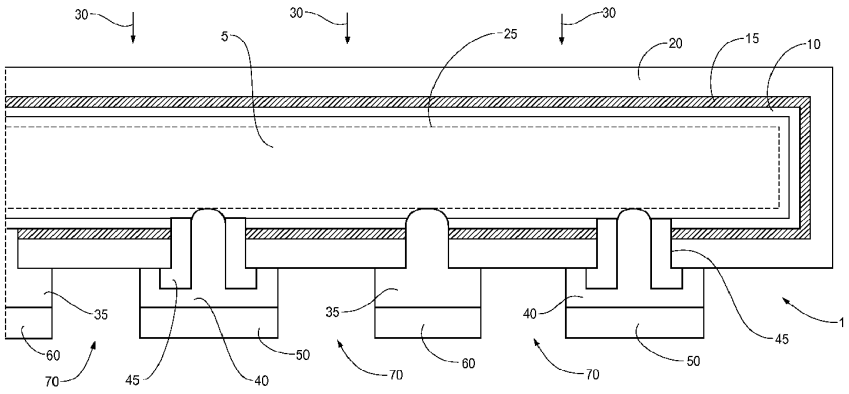


Fig. 2

(57) Abstract: A photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a passivation layer on at least the back surface, a doped layer opposite in conductivity type to the wafer over the passivation layer, an induced inversion layer, a dielectric layer over the doped layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer; and a neutral surface photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, neutral passivation layer on at least the back surface, a dielectric layer over the passivation layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer.

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Solar Cells

This application claims the benefit of U.S. Provisional Patent Application 60/895,217, filed on March 16, 2007.

Background of the Invention

This invention relates to new photovoltaic cells, also sometimes referred to herein as solar cells. More particularly, this invention relates to new photovoltaic cells that are highly efficient in converting light energy, and particularly solar energy, to electrical energy, and where such cells have electrical contacts on the back surface. This invention is also methods for making such cells.

One of the most important aspects of a photovoltaic cell is its efficiency in converting sunlight into electrical current. The art is in need of photovoltaic or solar cells that are highly efficient, and that are also easy to manufacture. The present invention provides for such solar cells and a method for their manufacture.

Although photovoltaic cells can be fabricated from a variety of semiconductor materials, silicon is generally used because it is readily available at reasonable cost and because it has the proper balance of electrical, physical and chemical properties for use in fabricating photovoltaic cells. In a typical procedure for the manufacture of photovoltaic cells using silicon as the selected semiconductor material, the silicon is doped with a dopant of either positive or negative conductivity type, formed into either ingots of monocrystalline silicon, or cast into blocks or "bricks" of what the art refers to as a multicrystalline silicon, and these ingots or blocks are cut into thin substrates, also referred to as wafers, by various slicing or sawing methods known in the art. These wafers are used to manufacture photovoltaic cells. However, these are not the only methods used to obtain suitable semiconductor wafers for the manufacture of photovoltaic cells.

By convention, and as used herein, positive conductivity type is commonly designated as "p" or "p-type" and negative conductivity type is designated as "n" or "n-type". Therefore, "p" and "n" are opposing conductivity types.

The surface of the wafer intended to face incident light when the wafer is formed into a photovoltaic cell is referred to herein as the front face or front surface, and the surface of the wafer opposite the front face is referred to herein as the back face or back surface.

In a typical and general process for preparing a photovoltaic cell using, for example, a p-type silicon wafer, the wafer is exposed to a suitable n-dopant to form an emitter layer and a p-n junction on the front, or light-receiving surface of the wafer. Typically, the n-type layer or emitter layer is formed by first depositing the n-dopant onto the front surface of the p-type wafer using techniques commonly employed in the art such as chemical or physical deposition and, after such deposition, the n-dopant, for example, phosphorus, is driven into the front surface of the silicon wafer to further diffuse the n-dopant into the wafer surface. This "drive-in" step is commonly accomplished by exposing the wafer to high temperatures. A p-n junction is thereby formed at the boundary region between the n-type layer and the p-type silicon wafer substrate. The wafer surface, prior to the phosphorus or other doping to form the emitter layer, can be textured.

In order to utilize the electrical potential generated by exposing the p-n junction to light energy, the photovoltaic cell is typically provided with a conductive front electrical contact on the front face of the wafer and a conductive back electrical contact on the back face of the wafer. Such contacts are typically made of one or more highly electrically conducting metals and are, therefore, typically opaque. Since the front contact is on the side of the photovoltaic cell facing the sun or other source of light energy, it is generally desirable for the front contact to take up the least amount of area of the front surface of the cell as possible yet still capture the electrical charges generated by the incident light interacting with the cell. Even though the front contacts are applied to minimize the area of the front surface of the cell covered or shaded by the contact, front contacts nevertheless reduce the amount of surface area of the photovoltaic cell that could otherwise be used for generating electrical energy.

The art therefore needs photovoltaic cells that have high efficiency, can be manufactured using large scale production methods, and, preferably, in order to increase efficiency, do not have electrical contacts on the front side or surface of the wafer, thereby maximizing the available area of the front surface of the cell for converting light into electrical current. The present invention provides such a photovoltaic cell. The photovoltaic cells of this invention can be used to efficiently generate electrical energy by exposing the photovoltaic cell to the sun.

Summary of the Invention

In one aspect this invention is a photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a passivation layer on at least the back surface, a doped layer opposite in conductivity type to the wafer over the passivation layer, an induced inversion layer, a dielectric layer over the doped layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer. Preferably, the localized emitter contact or contacts and localized base contact or contacts are all on the back surface of the photovoltaic cell. The localized emitter contact and localized base contacts are suitably laser fired contacts.

In another aspect this invention is a neutral surface photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a neutral passivation layer on at least the back surface, a dielectric layer over the passivation layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer. Preferably, the localized emitter contacts and localized base contact or contacts are all on the back surface of the photovoltaic cell. The localized emitter contacts and localized base contacts are suitably laser fired contacts. By neutral surface we mean that the cell does not have a purposely induced inversion layer and, preferably, does not have an inversion layer.

This invention is also a method for making such photovoltaic cells.

Brief Description of the Drawings

Figure 1 is an energy band diagram showing how an induced inversion layer in a silicon wafer "bends" the conduction and valance bands near the wafer surface so the Fermi level is closer to the conduction band.

Figure 2 is a cross-section view of a portion of a photovoltaic cell in accordance with an embodiment of this invention having an induced inversion layer.

Figure 3 is a cross-section view of a portion of a photovoltaic cell in accordance with an embodiment of this invention having a neutral surface.

Figure 4 is view of the back surface of a photovoltaic cell in accordance with an embodiment of this invention showing a back contact having interdigitated fingers.

Detailed Description of the Invention

The following is a description of embodiments of the present invention but such embodiments are not to be construed as limiting the scope of this invention.

A semiconductor wafer useful in the method of this invention for preparing photovoltaic cells preferably comprises silicon and is typically in the form of a thin, flat shape. The silicon may comprise one or more additional materials, such as one or more semiconductor materials, for example germanium, if desired. For a p-type wafer, boron is widely used as the p-type dopant, although other p-type dopants, for example, aluminum, gallium or indium, will also suffice. Boron is the preferred p-type dopant. Combinations of such dopants are also suitable. Thus, the dopant for a p-type wafer can comprise, for example, one or more of boron, aluminum, gallium or indium, and preferably it comprises boron. If an n-type silicon wafer is used, the n-type dopants can be, for example, one or more of phosphorus, arsenic, antimony, or bismuth. Suitable wafers are typically obtained by slicing or sawing silicon ingots, such as ingots of monocrystalline silicon, to form monocrystalline wafers, such as the so-called Czochralski (C_z) silicon wafers. Suitable wafers can be obtained by slicing or sawing ingots of silicon as described in U.S. Patent Applications Publication Nos. 2007/0169684 A1 and 2007/0169685 A1, for example, silicon referred to therein as monocrystalline silicon, cast monocrystalline silicon, near-monocrystalline silicon, and geometric multi-crystalline silicon. Suitable wafers can also be made by slicing or sawing blocks of cast, multi-crystalline silicon. Silicon wafers can also be pulled straight from molten silicon using processes such as Edge-defined Film-fed Growth technology (EFG) or similar techniques. Although the wafers can be any shape, wafers are typically circular, square or pseudo-square in shape. "Pseudo-square" means a predominantly square shaped wafer usually with rounded corners. The wafers used in the photovoltaic cells of this invention are suitably thin. For example, wafers useful in this invention can be about 10 microns thick to about 300 microns thick. For example, they can be about 10 microns up to about 200 microns thick. They can be about 10 microns up to about 30 microns thick. If circular, the wafers can have a diameter of about 100 to about 180 millimeters, for example 102 to 178 millimeters. If square or pseudo-square, they can have a width of about 100 millimeters to about 150 millimeters with rounded corners having a diameter of about 127 to about 178 millimeters. The wafers useful in the process of this invention, and consequently the photovoltaic cells made by the process of this invention can, for

example, have a surface area of about 100 to about 250 square centimeters. The doped wafers that are useful in the process of this invention can have a resistivity of about 0.1 to about 20 ohm.cm, typically of about 0.5 to about 5.0 ohm.cm.

The wafers used in the photovoltaic cells of this invention preferably have a diffusion length (L) that is greater than the wafer thickness (t). For example, the ratio of L to t is suitably greater than 1. It can, for example be greater than about 1.1, or greater than about 2. The ratio can be up to about 3 or more. The diffusion length is the average distance that minority carriers (such as electrons in p-type material) can diffuse before recombining with the majority carriers (holes in p-type material). The L is related to the minority carrier lifetime τ through the relationship $L = (D\tau)^{1/2}$ where D is the diffusion constant. The diffusion length can be measured by a number of techniques such as the Photon-Beam-Induced Current technique or the Surface Photovoltage technique. See for example, "Fundamentals of Solar Cells", by A. Fahrenbruch and R. Bube, Academic Press, 1983, pp. 90-102, which is incorporated by reference herein, for a description of how the diffusion length can be measured.

Although the term wafer, as used herein, includes the wafers obtained by the methods described, particularly by sawing or cutting ingots or blocks of single crystal or multi-crystalline silicon, it is to be understood that the term wafer can also include any other suitable semiconductor substrate or layer useful for preparing photovoltaic cells by the process of this invention. Any damage created by sawing or cutting wafers from ingots can be removed by etching the wafers in sodium hydroxide (NaOH) at an elevated temperature; for example, a solution of 40 wt % NaOH in water at about 80°C. The wafers can be cleaned by, for example, using a standard RCA clean followed by a dip in dilute hydrofluoric acid (HF) for example, about 5% wt% HF in water.

The front surface of the wafer is preferably textured. Texturing generally increases the efficiency of the resulting photovoltaic cell by increasing light absorption. For example, the wafer can be suitably textured using chemical etching, plasma etching, laser or mechanical scribing. If a monocrystalline wafer is used, the wafer can be etched to form an anisotropically textured surface by treating the wafer in an aqueous solution of a base, such as sodium hydroxide, at an elevated temperature, for example about 70°C to about 90°C for about 10 to about 120 minutes. The aqueous solution may contain an alcohol, such as isopropanol. A multicrystalline wafer can be textured by mechanical dicing using beveled dicing blades or profiled texturing wheels. In a

preferred process a multicrystalline wafer is textured using a solution of hydrofluoric acid, nitric acid (HNO_3) and water. Such a texturing process is described by Hauser, Melnyk, Fath, Narayanan, Roberts and Bruton in their paper "A Simplified Process for Isotropic Texturing of MC-Si", Hauser, et al., from the conference "3rd World Conference on Photovoltaic Energy Conversion", May 11-18, Osaka, Japan, which is incorporated by reference herein in its entirety. The textured wafer is typically subsequently cleaned, for example, by immersion in hydrofluoric and then hydrochloric acid with intermediate and final rinsing in de-ionized water, followed by drying. The back surface of the wafer may or may not be textured depending on the thickness of the wafer and the light-trapping geometry employed.

Prior to texturing a wafer, the wafer can be subjected to phosphorus and/or aluminum gettering. For example, gettering can be accomplished by forming a heavily doped n-type layer (n^+ layer) by, for example, phosphorus diffusion on one or both sides of the wafer. This can be accomplished, for example, by exposing the wafer to a gas such as $POCl_3$, for 30 minutes at 900°C to 1000°C. Such gettering will increase the diffusion length of the wafer. After formation of the heavily doped n-type layer or layers, they can be removed by, for example, etching using acids such as HF and HNO_3 or a mixture thereof, or strong bases such as NaOH. One embodiment of this invention would involve forming a heavily doped n-type layer on the front of the wafer to getter impurities and then subsequently removing it during the texture etching of the front surface as described above.

I. The Induced-Inversion-Layer Back-Contact Photovoltaic Cell

In one aspect, this invention is a back contact photovoltaic cell comprising an induced inversion layer. This cell comprises passivated, more suitably, well-passivated silicon wafer surfaces and also preferably comprises an induced emitter, also referred to herein as an induced inversion layer, in conjunction with localized contacts that are, preferably, fired through a dielectric layer. By localized we mean that the contacts do not occupy the total back surface of the photovoltaic cell and, preferably, the total area of all the localized contacts is only a small percentage of the total area of the back surface of the photovoltaic cell, such as no more than about 5 percent, or no more than about 3 or 2 percent of the total area of the back surface of the photovoltaic cell.

The silicon wafers, which can be either p-type or n-type, are preferably cleaned and the front surface may be textured. Then, at least the back surface of the wafer, or the front and back surfaces of the wafer, or all surfaces of the wafer, are coated with one or more, preferably thin, passivating layers, for example, a layer of amorphous silicon (a-Si:H) that is up to about 30 nanometers (nm) thick, for example, about 4 to about 30 nm thick. The passivation layer can be about 10 nm thick. This passivation layer may also be an undoped, or so-called intrinsic layer of an a-Si:H alloy such as a-$SiN_xC_yO_z$:H comprising varying amounts of carbon, nitrogen and oxygen. There may be one or more of such layers to form the passivation layer where the total thickness of the single layer or all the layers is about 4 to about 30 nm. The values of x, y and z can be such that they each vary from about 0 to less than about 0.66. However, in the case of nitrogen and oxygen, the composition may be close to stoichiometric, so that instead of it being a-Si:H it is more nearly the composition of silicon nitride in the case of adding N, or silicon dioxide in the case of adding O . Layers of a-Si:H with or without added C, N or O that are deposited by plasma enhanced chemical vapor deposition (PECVD), also typically contain 5 – 20 at.% of hydrogen. Ammonia can be used as a suitable source of nitrogen. Low molecular weight hydrocarbons, most suitably methane, are suitable sources of carbon. Oxygen gas is a suitable source of oxygen, but other oxygen containing gases such as CO_2 or N_2O may also be used as a source of oxygen. Such a-Si:H layer can be applied by any suitable method such as, for example, by PECVD in an atmosphere of silane. Most suitably, it is applied by PECVD in an atmosphere containing about 10% silane in hydrogen, and most suitably it is applied at low temperatures such as, for example, about 100°C to about 250°C.

Without intending to be bound by a theory of operation, this passivation layer is added to passivate defects near the surface of the silicon wafer. After such passivation layer or layers are applied, the wafer silicon surface recombination velocity should be $\leq$ 100 cm/s for the coated silicon wafer surfaces, for example, $\leq$ 40 cm/s, and preferably $\leq$ 10 cm/s. The surface recombination velocity (S) at the surface of a silicon wafer is determined by measuring the effective lifetime of a wafer (τ_{eff}) using techniques such as photoconductive decay (the effective lifetime can be measured using the microwave photoconductive decay technique with the WT-2000 Wafer Tester made by Semilab) and by also determining the bulk lifetime (τ_b) of the silicon used to make the wafer, and then using the expression $1/\tau_{eff} = 1/\tau_b + 2S/W$ where W is the sample thickness to

determine S. The bulk lifetime can be determined by measuring the effective lifetime of a similar silicon wafer having extremely well passivated surfaces so that $\tau_{eff} = \tau_b$. The silicon surfaces can be extremely well passivated by, for example, by immersing the wafer in a solution of 10% hydrogen fluoride (HF) in water for a few minutes at room temperature before measuring the lifetime. For silicon surfaces with aluminum back-surface field contacts, S is usually > 1,000 cm/s.

After adding the one or more passivating layers, one or more, preferably, thin layers of a doped layer having a conductivity type or doping opposite to that of the wafer is applied to at least the back surface of the wafer. The doped layer or layers can be applied to both the back and front surfaces of the wafer, and can be applied to all surfaces of the wafer. Such doped layer, preferably, heavily doped a-Si:H , is for example, about 10 to about 30 nm thick, of a conductivity type opposite to the wafer. If the wafer is p-type, the doped layer such as an a-Si:H layer can be doped with, for example, one or more of phosphorus, arsenic, antimony or bismuth. If the wafer is n-type, the layer can be doped with, for example, one or more of boron, aluminum, gallium or indium. The doped layer may also be an alloy such as phosphorus-doped a-SiC_y:H for generating an inversion layer in a p-type wafer, and boron-doped a-SiC_y:H for generating an inversion layer in an n-type wafer. The concentration of dopant, such as, for example, phosphorus, can be about 0.1 to about 1.0 atomic % (at.%). The doped layer can also be a doped alloy a-$SiN_xC_yO_z$:H, where x can be in the range of about 0 to about 0.2 and y and z can be in the range of about 0 to about 0.05. The doped layer can be applied in any suitable manner such as, for example, by PECVD. Without intending to be bound by a theory of operation, the passivation layer capped by a doped layer induces an inversion layer or induced emitter in the silicon wafer. The passivation and doped layers can be deposited on all surfaces of the wafer, that is the front, back, and edges of the wafer. Preferably, the inversion layer is adjacent to all surfaces of the wafer. Again, without intending to be bound by a theory of operation, such inversion layer generated over the entire surface of the wafer would minimize any polarization or charging effects that might occur in operating photovoltaic modules having photovoltaic cells made in accordance with this embodiment of the invention. An inversion layer is created in silicon when sufficient charge is induced near the surface so that the minority carriers in the bulk become the majority carriers near the surface. In the case of p-type silicon, where holes are the majority carriers and the Fermi level is close to the valence

band, one can induce an inversion layer by locating a layer containing fixed positive charge near the silicon surface or by locating an n^+, for example, phosphorus-doped, silicon layer near the surface of the silicon wafer. Figure 1 shows an energy band diagram for the case where an intrinsic layer of undoped a-Si:H is deposited on p-type crystalline silicon and then a phosphorus doped (n^+) layer of a-Si:H is deposited on the intrinsic a-Si:H layer. In this case, the phosphorus-doped a-Si:H layer will induce an inversion layer containing negative charge (excess electrons) near the surface of the p-type crystalline silicon. Thus, as shown in Figure 1, the conduction and valence bands (E_C and E_V, respectively) will bend such that the Fermi level (E_F), in equilibrium, will be closer to the conduction band near the surface. In another example, the fixed positive charge in silicon nitride deposited by PECVD, which typically has a charge density of about 2×10^{12} cm^{-2}, will induce a negatively charged or inversion layer near the surface of a p-type wafer, which causes the conduction band near the surface to move closer to the Fermi level. However, it is desirable to induce a strong inversion layer, so the preferred embodiment would employ a heavily doped layer, such as a heavily doped layer of a-Si:H or an a-Si:H alloy containing, for example, carbon. For example, in the case of a p-type wafer, the doped layer can be an a-Si:H layer or a a-SiC_y:H layer (y is > 0) that can be 30 nm thick and containing about 0.5 to about 2.0 at.% n-type dopant, such as 1.0 at.% of an n-type dopant such as phosphorus, and in the case of an n-type wafer the doped layer can be an a-Si:H layer or a a-SiC_y:H layer (y is > 0) that can be 30 nm thick and containing 0.5 to about 2.0 at.% p-type dopant, such as about 1.0 at.% a of p-type dopant such as boron. By a "strong" inversion layer, we mean, preferably, an inversion layer where the amount of induced charge causes the wafer surface to become degenerate or very conductive, such as an electrical conductivity that is close to metallic.

In another embodiment, the passivation layer and doped layer can be replaced by one or more lightly doped layers. For example, a lightly doped layer of a-Si:H. In the case of a p-type wafer, the layer can be a-Si:H, and the layer can be about 10 to about 50 nm thick, and the layer can contain about 0.01 to about 0.3 at.% n-type dopant, such as one or more of phosphorus, arsenic, antimony, or bismuth. For example, a layer of a-Si:H that is 30 nm thick and containing about 0.1 at.% of phosphorus. In the case of an n-type wafer, the layer can be a-Si:H, and the layer can be about 10 to about 50 nm thick, and the layer can contain about 0.01 to about 0.3 at.% p-type dopant, such as one

or more of boron, aluminum, gallium, or indium. For example, a layer of a-Si:H that is 30 nm thick and containing about 0.1 at.% of boron. In this case, the lightly doped a-Si:H layer forms a heterojunction with silicon, and as before, the doped layer induces an inversion layer in the silicon wafer.

One or more layers of dielectric material, such as a layer silicon nitride, for example is then deposited on the front of the wafer, more preferably on the front and back of the wafer, and most preferably, all surfaces of the wafer. If deposited by PECVD, the silicon nitride can be a-SiN_x:H where x is suitably about 0.4 to about 0.57. The dielectric layer can be up to about 90 nm thick, for example, about 70 to about 90 nm thick. The dielectric may also be other materials such as a-$SiN_xC_yO_z$:H deposited by, for example, PECVD, and comprising varying amounts of carbon, nitrogen and oxygen. The values of x, y and z can be such that they each vary from about 0 to less than about 0.66. The relative amounts of carbon, nitrogen and oxygen in the a-$SiN_xC_yO_z$:H may be selected to minimize light absorption in the dielectric layer and to optimize light coupling into the silicon wafer. In the preferred case, the dielectric layer on the front and its thickness are selected to minimize light absorption in the dielectric and to optimize the light coupling into the silicon wafer, and the type of dielectric layer on the back and its thickness are selected to enhance reflection of weakly absorbed radiation back into the silicon wafer. In both cases, the composition of the dielectric layer on the front surface may be graded to optimize the light trapping. Grading means that the composition of the dielectric, for example the concentration of carbon and/or nitrogen in the dielectric on the front surface of the wafer, changes by decreasing from the part of the dielectric layer closest to the front to the part of the dielectric layer closest to the doped layer. Thus, the dielectric constant of the graded layer on the front surface would decrease from the outer surface to the doped layer of the sample so as to reduce reflection at the front surface. At the back surface alternating layers of dielectric materials with different dielectric constants can be deposited to optimize reflection of weakly absorbed radiation back into the silicon wafer. For example, a layer of SiN_x:H, where x is about 0.4 to about 0.57, might be deposited on the doped layer and then overcoated with a layer of a-SiO_z:H, where z is about 0.5 to about 0.66, with the thicknesses of the layers selected to minimize reflection. In most cases, the dielectrics and thicknesses of the dielectric layers on the front of the cells would be selected to minimize light absorption in the

layers and to minimize reflection from the cells when encapsulated in a photovoltaic module.

The photovoltaic cells in accordance with embodiments of this invention have localized electrical contacts, preferably only on the back surface of the wafer. These localized contacts extend through at least the dielectric layer, and preferably through the doped layer and the passivation layer (or the lightly doped, thicker layer if that layer is used to replace the combination of the passivation and doped layers) and into the silicon wafer. In one embodiment of the invention, materials, such as a metal or non-metal, that can form localized n^+ contacts, or pastes or inks that contain n-type dopants, such as one or more of As, Bi, P or Sb; and materials, such as a metal or non-metal, that can form localized p^+ contacts, or pastes or inks that contain p-type dopants, such as one or more of Al, B, Ga or In, are applied in a pre-selected pattern on the wafer to form the localized contacts. One of the advantages of this invention is that the these localized base and emitter contacts can, as will be described in more detail below, be readily formed on the wafer by treating the back surface of the wafer after the passivation layer, doped layer (or the lightly doped, thicker layer if that layer is used to replace the combination of the passivation and doped layers), and dielectric layer have been applied. The pattern is preferably formed by applying the materials locally, that is, in a manner so that the material is applied only where it needs to be rather than in, for example, a manner that covers the entire surface of the wafer. The pattern is preferably selected so that, ultimately, the localized contacts can be easily electrically connected, as described in more detail below, to form two separate photovoltaic cell electrical contacts, one that is the positive electrical contact for the photovoltaic cell and the other the negative electrical contact. The material can be applied onto the dielectric layer on the back surface of the wafer in a series of separated dots or short lines, or in some other pattern such as a continuous line. A series of separated dots is preferred. One such preferred pre-selected pattern is an interdigitated finger pattern on, preferably, only the back dielectric layer, where the first part of the interdigitated finger pattern is the material comprising the p-type material for the p^+ localized contacts and the other, second part of the interdigitated finger pattern is material comprising the n-type material for the n^+ localized contacts. By interdigitated finger pattern we mean a pattern where a first set of, preferably parallel, rows or "fingers" of the material are applied between a second set of such "fingers". The material can be applied in a series of isolated "dots" or

short lines, or in some other pattern, to form each finger. As series of separated dots is preferred. Such interdigitated finger pattern can be visualized by placing the fingers of a hand between, but separated from, the fingers of another hand, in an alternating manner. One hand and its fingers would form one contact and the other hand, the other contact. The interdigitated finger patterns of dots or lines will be overcoated with an interdigitated pattern of conductive fingers to collect the photogenerated current.

A laser, other source of radiation, or a source of heat, or other suitable method, can be used to fire the p-type and n-type materials through the dielectric, through the doped and through the passivation layers forming both p^+ and n^+ localized contacts to the silicon wafer. Laser firing can be accomplished using, for example, a Nd-YAG laser. For example, the laser can be a Q-switched, Nd-YAG laser having a pulse duration of, for example, about 10 to about 200 nanoseconds. If the p-type and n-type materials are deposited as separated dots, or separated short lines and then fired as described above, the localized emitter and base contacts so formed will also be separated from each other on the wafer.

In another embodiment, the localized p^+ and n^+ contacts are formed by thermal treatment, such as a rapid thermal processing, but in this case the passivation, doping and dielectric layers should be able to withstand the thermal processing, for example, where the passivation and doping layer might comprise a-SiC_y:H alloy where y can be in the range from about 0 to about 0.2. For example, a composition might be 75 at.% Si, 15 at.% C and 10 at.% H. In this case, the layers on the surface of the wafer could be first opened, for example by etching, through the dielectric, doped and passivation layers (or the lightly doped, thicker layer if that layer is used to replace the combination of the passivation and doped layers) in a pre-selected pattern as described above so that the p-type and n-type material being used to form the contacts can be placed in contact with the silicon wafer in those opened regions. The opened regions, such as in the shape of separated round holes, or short lines or other suitable shape, could also be formed using laser ablation. Alternatively, the dopant-containing material can be applied locally on top of the dielectric layer in a pre-selected pattern as described above if it can be thermally fired through the dielectric, doped and passivation layers (or the lightly doped, thicker layer if that layer is used to replace the combination of the passivation and doped layers) and on or into the silicon layer beneath the dielectric, doped and passivation layers. A rapid thermal processing can be accomplished by heating the

silicon at least in the region where the desired p^+ or n^+ localized contact is to be formed for a short time period, such as about 5 seconds to about 2 minutes at a temperature of, for example, about 700°C to about 1000°C.

The dopant-containing materials used to form the localized contacts can be metals, such Al, Ga or In, for p^+ contacts, and Sb, As or Bi, for n^+ contacts, deposited by or more methods such as vapor deposition, or they can be alloys such as, for example Sn-Sb, Sn-Bi for the n^+ contacts, or Sn-In, Al-Si for the p^+ contacts. The dopant-containing materials used to form the localized contacts can be inks or pastes comprising compounds, such as one or more of SbN or AsP, that can form n^+ contacts or one or more of B_2Si or AlB_2 , that can form p^+ contacts, or organometallic compounds containing, for example, one or more of B, Al, Ga or In, that can form p^+ contacts or one or more of P, As, Sb, Bi that can form n^+ contacts. The number of such localized contacts and the spacing and shape of the localized contacts will, preferably, be selected to achieve optimal photovoltaic cell performance.

Minority carriers that may collect in the inversion layer during the operation of the photovoltaic cell may leak to the base contacts, that is, the p^+ localized contacts in a p-type wafer and the n^+ localized contacts in an n-type wafer. Such leakage would decrease the efficiency of the photovoltaic cell in converting light energy into electrical energy. These base contacts are ohmic contacts to the wafer that allow the collection of majority carriers. This leakage or shunting can be prevented or minimized by, for example, electrically isolating the base contact from the inversion layer. This electrical isolation can be accomplished by, for example, adding an insulation layer between at least part of and preferably all of the base contact and the inversion layer. The insulation layer is preferably a dielectric material, such as one or more of SiO_2, intrinsic a-Si:H, or $SiN_xC_yO_z$:H, where the values of x, y and z can be such that they each vary from about 0 to less than about 0.66. If the base contacts are "point" contacts, such as, for example, a contact made by laser or thermally firing a dot or short line of the material used to form the contact through the dielectric, doped and passivation layers, the electrical isolation can be accomplished by forming a ring or collar of electrically insulating material, such as one or more dielectric materials mentioned above, around the base contacts. Such an isolation ring or collar can be made by depositing a layer or region of the selected dielectric material in the form of, for example, an ink or paste over the dielectric layer in the areas where the base contacts will be formed. Then, using, for example, a laser, the

dielectric material can be fired or fused through at least the dielectric layer and the doped layer. The dielectric material could be fired or fused through the dielectric layer, for example, silicon nitride, the doped layer, and the passivation layer all the way to the wafer and even into the silicon wafer to some extent. The material used to form the base contacts can then be deposited over the same area and then, as describe above, fired through the dielectric material using a laser and thereby forming the base contact having a ring or collar of dielectric material surrounding the material used to form the base contact so there is no significant inversion layer induced in the silicon wafer in the vicinity of the isolation ring or collar. Such isolation ring can also be formed by a rapid thermal processing step where the dielectric material use to form the isolation ring is, for example, a glass frit paste or ink that fuses through at least the dielectric layer and the doped layer so that no significant inversion layer is formed in the silicon in the vicinity of the isolation ring. At least a portion, and preferably all of the base contacts have an insulation layer electrically isolating the base contact from the inversion layer.

A pre-selected pattern, such as an interdigitated finger pattern described above, comprising an electrically conductive material, or a material that will become electrically conductive after subsequent thermal or other treatment, is deposited over the localized emitter contacts and over the localized base contacts to separately electrically connect each set of contacts so that electric current can be collected from the operating photovoltaic cell.

For example, the pre-selected, electrically conductive pattern can comprise silver, aluminum or other suitable metal, and the silver, aluminum or other suitable metal can be applied to the wafer by one or more deposition methods. For example the pattern can be applied by applying an aluminum containing paste or inkjet printing a silver containing ink. Firing or otherwise thermally treating such pastes would convert it into a stable, electrically conducting contact.

In one embodiment, using a p-type wafer, for example, the base and emitter localized contacts, the isolating rings and the electrically conductive pattern, for example, an interdigitated finger pattern, that electrically connects the localized contacts can be formed using a multi-headed, inkjet printer. In such embodiment, one head prints, for example, dots or other suitable shapes of an ink containing an n-type contact material such as antimony, another head prints an interdispersed array of dots containing a p-type contact material such as aluminum, another head prints a ring of

material to be used to form the isolation ring around the p-type dots (for a p-type wafer), and another head prints the pattern of electrically conductive material, such as interdigitated fingers of silver containing paste or ink, with a first pattern, such as a finger pattern, over the p-type dots (or other suitable shapes) and the associated isolation rings, and a second pattern over the n-type dots (or other suitable shapes), such as a finger pattern, electrically separated from the first pattern. Then a laser is used to fire the n^+ contacts and to simultaneously fire both the p^+ contacts and the material for forming the isolation rings to form the localized emitter contacts and localized base contacts having the isolation ring, respectively. In another embodiment, again using a p-type wafer as an example, one print head of a multi-headed inkjet printer would first print the isolation ring material onto the dielectric layer, another head prints a first pattern, for example, finger pattern, of p-type material such as an Al-containing ink over the isolation ring material, another head prints a second pattern, for example, finger pattern, of an n-type material, such as an Sb-containing ink, separated from the first pattern, and then another head prints a electrically conductive material such as a Ag-containing ink in an interdigitated finger pattern over both the patterns of p-type and n-type materials. Then a laser is used to form n^+ localized contacts in selected regions of the patterns containing the n-type materials and another laser beam is used to both form p^+ localized contacts in the central regions of the isolation ring material as well as fusing the isolation ring material at least into the dielectric and doped layers as mentioned above. Alternatively, as also mentioned above, the localized contacts might be formed by rapid thermal processing, but, preferably, in this case conditions for the rapid thermal processing should be selected so that the material used to form the electrically conducting patterns that electrically connect the localized contacts does not fire through the dielectric layer.

In the case of laser-fired contacts, a thermal annealing step may be used to optimize the performance of the photovoltaic cell. Such annealing can be accomplished, for example, by heating the cell to a temperature of about 300°C to about 450°C, for about 5 to about 60 minutes, for example, at about 350°C for 30 minutes. It can be annealed by rapid thermal processing, for example, at about 700°C to about 1000°C, for about 5 seconds to about 2 minutes, for example, at about 700°C for about 1 minute. In both cases, the passivation and dielectric layers selected must be able to tolerate such annealing step.

II. The Neutral Surface Back-Contact Photovoltaic Cell

In another aspect, this invention is a photovoltaic cell referred to herein as a neutral surface back-contact photovoltaic cell. That is, there is no purposely induced charge or band bending near the surface of the wafer that could induce shunting or current leakage near the localized contacts.

To form the neutral surface back-contact photovoltaic cell, a passivation layer that contains no or no significant fixed charges is applied to the wafer, such as a layer of a-Si:H. It can be one or more such layers. The passivation layer or layers can be applied on the back surface of the wafer, on the back and the front surfaces of the wafer, or to all surfaces of the wafer. The wafer can be p-type or n-type. Such neutral passivation layer or layers can be as described above for the passivation layers for the induced inversion layer cell; however, for this aspect of the invention, the passivation layer or combination of passivation layers, such as a layer of a-Si:H, may be thicker than the passivation layer or layers for the induced inversion layer cell. For example, such neutral passivation layer or combination of such layers can be up to about 100 nm thick; for example about 4 to 100 nm thick. The neutral passivation layer on the back surface of the wafer should be thick enough to provide dielectric isolation of the pattern of electrically conductive material on the back of the wafer from the silicon wafer outside those regions where localized contacts are formed. Also, the neutral passivation layer should be thick enough to greatly reduce or eliminate the formation of an inversion layer or an accumulation layer at the surface of the wafer. Without intending to be bound by a theory of operation, it is believed an a-Si:H passivation layer, if made thick enough, can provide enough charge of the opposite polarity to compensate the charge in any dielectric layer that is deposited over the a-Si:H layer. The deposition of such dielectric layer is described in more detail below. For example, SiN_x:H deposited by PECVD typically has a positive charge density of about 2×10^{12} cm^{-2} while SiO_2 typically has a positive charge density of about 10^{11} cm^{-2}. Thus, a thin a-Si:H passivation layer, for example, a layer about 5 to about 50 nm thick, can be used in conjunction with an SiO_2 dielectric layer to prevent a significant inversion layer from forming in the p-type silicon wafer, while a much thicker passivation a-Si:H layer, for example about 30 to about 100 nm thick, would need to be used with a SiN_x:H dielectric layer to prevent a significant inversion layer from forming in the p-type silicon wafer. The thickness of the a-Si:H layer will depend on the conductivity of the a-Si:H, which is determined by the deposition

conditions such as substrate temperature, residual impurities, and other variables. In another embodiment of the neutral surface back-contact photovoltaic cell, a layer of intrinsic a-Si:H could be used as both a passivation layer and as a dielectric layer, and in this case the thickness of the a-Si:H might be about 40 to about 100 nm thick.

A thin, doped layer can also be used over the passivation layer or layers in the neutral surface back-contact photovoltaic cell, such as, preferably, a layer of doped a-Si:H, to assure a neutral surface condition in the silicon wafer so that there is no significant inversion or accumulation layer. The dopant can be one or more of a p-type dopant such as boron, aluminum, gallium, indium or one or more of an n-type dopant such as phosphorus, arsenic, antimony and indium. The amount of dopant can be experimentally determined by determining the zero band bending condition using, for example, surface photovoltage measurements. The magnitude of photovoltage will depend on the amount of band bending and the polarity of the photovoltage will depend on the direction of the band bending. The photovoltage will be close to zero when the band bending is close to zero. An inversion layer can occur, for example, when a layer containing fixed positive charge, such as a layer of SiN_x:H, is located near the surface of a p-type wafer so that minority carriers, that is, electrons in a p-type wafer or holes for an n-type wafer, dominate near the surface and the conduction and valence bands bend so that the Fermi level is brought close to the conduction band. One or more thin layers, for example, about 4 to about 20 nm thick, lightly doped with one or more of a p-type dopant, for example, boron, aluminum, gallium or indium, can be used to compensate or negate the fixed positive charge that might exist in the dielectric layer. The layer can be a-Si:H. For example, for a dielectric layer of SiN_x:H with a fixed positive charge density of about 2×10^{12} cm^{-2}, a thin layer of a-Si:H doped with boron can be used to assure that no inversion layer or accumulation layer occurs in the silicon wafer. The thin doped layer might contain, for example, about 0.001 at.% p-type dopant, such as boron, to about 0.1 at.% p-type dopant, depending on the thickness of the doped layer and the amount of fixed positive charge in the dielectric layer. Such a doped layer or layers, if used, is preferably optimized in terms of thickness, dopant type and dopant concentration to assure that the conduction and valence band bending near the surface of the silicon wafer is at or essentially zero. Conversely, if the dielectric layer should contain fixed negative charge, then one or more thin layers, for example, about 4 to about 20 nm thick lightly n-doped an n-type dopant, such as one or more of phosphorus,

arsenic, antimony or bismuth, at a doping level of about 0.001 at.% n-type dopant to about 0.1 at.% n-type dopant, is preferably applied over the passivation layer or layers. Preferably, the thickness of the n-doped layer would depend on the doping level and on the fixed negative charge in the dielectric layer, and is, preferably selected to assure that no or substantially no charge is induced at the silicon wafer surface.

One or more layers of dielectric material are applied to the wafer over the passivation layer and, if present, over the thin doped layer in the neutral surface back-contact photovoltaic cell. The one or more dielectric layers can be applied to the back surface of the wafer, to the back and front surfaces of the wafer, or to all surfaces of the wafer. Such dielectric layer or layers can be as described above for the dielectric layer for the induced inversion layer cell, but may be optimized, for example, by depositing the dielectric under conditions so that there is no or essentially no fixed charge in the dielectric, so that no significant conduction or valence band bending or induced charge occurs in the silicon. A neutral surface with no significant band bending can usually be achieved with the deposition of intrinsic a-Si:H on a well-cleaned silicon wafer. As mentioned above, SiN_x:H typically has a positive charge density of about 2 x 10^{12} $cm^{-2,}$ while SiO_2 typically has a positive charge density of about 10^{11} cm^{-2}. As also mentioned above, any charge in the dielectric layer could be negated or compensated by using an appropriate doped layer.

The localized contacts for this neutral surface, back-contact photovoltaic cell can be applied in a manner as described above for the induced inversion layer cell. As described above for the induced inversion layer cell, such localized contacts are preferably formed on the wafer for the neutral surface back-contact photovoltaic cell after the deposition of the layers described above on the back face of the wafer. Thus, the base and emitter contacts for the neutral surface back-contact photovoltaic cell extend through the dielectric layer and preferably through the passivation layer (and thin doped layer if used.)

Isolation rings, as described above for the induced inversion layer cell, are optional for this neutral surface, back-contact photovoltaic cell. However, if used, they can be formed as described above for the induced inversion layer cell.

The electrical contacts formed from electrically conductive material that electrically connects the emitter localized contacts on neutral surface back-contact photovoltaic cell, and electrically connects the localized base contacts on neutral

surface back-contact photovoltaic cell, can be applied to the back surface of the photovoltaic cell as described above for the induced inversion layer cell. The pattern can be, for example, in the form of interdigitated fingers, or some other suitable pattern. If laser firing is used to form the localized contacts, a thermal annealing step as described above for the induced inversion layer cell might be required to optimize the performance of the photovoltaic cell.

Certain embodiments of the photovoltaic cells of this invention will now be described with respect to Figures 2 and 3. However, it is to be understood that these are not the only embodiments of this invention.

Figure 2 shows a cross section view of a section of an induced inversion layer, back-contact photovoltaic cell 1 in accordance with an embodiment of this invention. Figure 2 shows a p-type silicon wafer 5 of the type suitable for manufacturing solar cells. Such wafers are known to those of skill in the art. However, it is to be understood that such wafer can also be n-type.

Figure 2 shows an intrinsic passivation layer 10 made from amorphous silicon (a-Si:H) deposited on wafer 5. This layer can be deposited on the wafer 5 by any suitable means such as, for example, plasma enhanced chemical vapor deposition (PECVD). It can be about 4 to about 30 nm thick and, as shown in Figure 2, can be applied on all surfaces of the wafer 5.

After depositing the intrinsic passivation layer, a doped layer 15 is applied having a doping opposite to that of the wafer. Since the silicon wafer 5 in Figure 2 is p-type, the doped layer 15 as shown in Figure 2 is n-type. In this example, the doped layer 15 can be doped a-Si:H, for example, a-Si:H doped with phosphorus. The doped layer 15 can be about 10 to about 30 nm in thickness and the concentration of dopant, such as, for example, phosphorus, can be about 0.1 to about 1.0 at.%. The doped layer 15 can also be an alloy of a-Si:H with carbon, nitrogen and /or oxygen. The doped layer 15 can be deposited by any convenient method such as, for example, by PECVD. As shown in Figure 2, such doped layer can be deposited on all surfaces of the wafer.

After depositing the doped layer 15, a layer of dielectric material 20 is deposited. Such layer can be, for example, a layer of SiN_x:H, for example, a layer about 70 to about 90 nm thick and where the value x can be about 0.4 to about 0.57 at.%. Such layer can be deposited by PECVD.

Figure 2 shows an inversion layer 25 depicted as a dashed line around the inside perimeter of the silicon wafer. As discussed above, the inversion layer contains a high concentration of induced charge; for example, in the case of a p-type wafer, the induced charge in the inversion layer consists of electrons. This excess of electrons near the surface can be described by a local bending of the conduction and valence bands so that the Fermi level is brought close to the conduction band, thus creating an induced junction.

In the case of an n-type wafer, an inversion layer can be generated by depositing a thin passivating layer of, for example, a-Si:H and then a layer of a-Si:H doped with a p-type dopant such as , for example, boron. This doped layer can be about 10 to about 30 nm in thickness and the concentration of dopants, such as, for example, boron, can be about 0.1 to about 1.0 at.%. The doped layer can also be an alloy of Si:H with carbon, nitrogen and/or oxygen. This doped layer can be deposited by any convenient method such as, for example, by PECVD.

In the next steps, localized emitter contacts 35 and localized base contacts 40 are formed on the back side of the wafer, that is, the side of the wafer opposite to the side that will be the front, light receiving side of the completed photovoltaic cell. Arrows 30 depict light impinging on the light receiving side of induced-inversion-layer, back-contact photovoltaic cell 1.

The localized contacts can be formed, for example, by first depositing a metal by, for example, one or more deposition or plating methods, or by depositing a conductive material containing a dopant, for example aluminum, for forming local p^+ contacts. The conductive material may be a paste or, more preferably, an ink. The metal or conductive material is preferably applied as separated dots, separated short lines, or in other suitable shapes such as continuous lines. The deposited metal or conductive material is subsequently treated so that the metal or conductive material containing the dopant reaches through the dielectric layer, the doped layer, the passivation layer and into the silicon wafer in localized regions. This can be accomplished by, for example, firing the metal or conductive material containing the dopant with a laser or other suitable source of heat such as an ion beam or electron beam. If a laser is used, it can be a Q-switched, Nd-YAG laser having a pulse duration of, for example, about 10 to about 200 nanoseconds. In this process, the metal or conductive material containing the dopant is locally heated by, for example, the laser beam and the heated, preferably molten, metal

or conductive material with dopant penetrates through the layers below and forms the base 40 and emitter 35 contacts with the silicon wafer. For a p-type wafer the metal or conductive material used to form the base contacts can be as described above and is suitably aluminum or an aluminum–containing material. If the wafer is p-type the emitter contacts can be made using a metal such as antimony or bismuth, or a metal such as tin containing a dopant such as phosphorus, antimony or bismuth. In Figure 2, the base contacts 40 can be made of aluminum and the emitter contacts 35 can be made of antimony.

In the case of localized emitter contacts 35, a contact can also be made by firing a metal through the dielectric layer into the doped layer, but in this case the intrinsic a-Si:H layer is preferably thin, for example, about 4 to 10 nm thick, so that minority carriers can move from the silicon wafer into the doped layer.

Contacts made in such manner are referred to as point contacts. However, they need not be in the shape of a point or dot. They can be any shape such as an oval or have a linear shape, such as a line shape.

In one preferred method, the localized base and emitter contacts are made by depositing a metal-containing material in the form of an ink in a desired pattern on the surface of the wafer. The pattern can be separated lines, dots, or some other suitable shape or pattern. The ink can be dried by, for example, heating prior to being fired to form the contacts.

In one such method the ink is deposited in the form of a pattern of separated dots on the back surface of the wafer. One set of separated dots comprises a material for forming the emitter contacts and the other set of dots comprises a material for forming the base contacts. The dots are then treated with a laser beam to fire the metal through the layers beneath the dots and into the silicon wafer to form the contacts.

It is preferable to electrically insulate or isolate the outer portions of the base contact 40 from the inversion layer 25. Such insulation can be achieved by including an isolation ring 45 around the outer portion of the base contacts 40. Such isolation ring 45 is shown in Figure 2. Such isolation ring can be formed by opening holes in the passivation , doped and dielectric layers with , for example, a laser, by mechanical means, or by masking and etching the layers , and then filing the holes with a suitable dielectric material such as silicon dioxide. The metal or conductive material containing a

dopant used to form the base contact 40 can be deposited over the hole having the dielectric material contained therein, and the metal or conductive material containing a dopant is then, for example, fired through the dielectric by using a laser or other suitable method, and the dielectric material will form a ring or collar 45 around the contact thereby isolating it from the inversion layer 25. Alternatively, the isolation ring can be formed by first depositing dielectric material for forming the isolation ring, and then depositing the material used to form the base contact. Then, in one firing step using, for example, a laser, the base contact material is fired through the dielectric material and through the passivation layer, the doped layer and the dielectric layer to form the base contact with the silicon wafer, and having a ring or collar of insulating dielectric material 45 surrounding the contact as shown, for example, in Figure 2.

In the preferred method of making the photovoltaic cells of this invention, the metal containing materials used to form the contacts are deposited on the wafer in the form of an ink, and where the deposition is accomplished using a printer, and preferably an ink jet printer or an aerosol jet printer, and more preferably an ink jet printer that is controlled by a computer so that the specific pattern of printing the inks can be programmed and controlled by the computer.

The collection of localized base contacts are electrically connected to each other and the collection of localized emitter contacts are electrically connected to each other so that the electrical current generated by exposing the photovoltaic cell to light can be collected. This can be done by, for example, applying a layer of an electrically conducting metal, such as silver, in a first pattern over and in electrical contact with the base contacts, and a second pattern over and in electrical contact with the emitter contacts, where the first pattern and the second pattern are not electrically connected. Such a pattern can be applied by one or more deposition methods such as the deposition of the metal as a vapor, or electrochemically using appropriate masks, or screen-printed using appropriate masks. Preferably, the patterns are deposited as an ink, preferably using an inkjet or aerosol jet printer as described above. Figure 2 shows a cross-section of such pattern 60 over emitter contacts 35 and a cross-section of such pattern 50 over base contacts 40. One preferable pattern is an interdigitated finger pattern as shown in Figure 4, where back surface of photovoltaic cell 1 has one set of fingers 50 that contact the base contacts 40, and the another set of interdigitated fingers 60 that contact the emitter contacts 35, and a space 70 that electrically separates

fingers 50 and 60. In another embodiment, dopant-containing inks for forming the base and the emitter contact are deposited in a desired pattern such as a pre-selected pattern of separated dots. As described above, in the regions where the base contacts will be formed, a dielectric material can be deposited first to provide for the formation of an isolation ring. Thereafter, a layer of electrically conducting material, such as an ink containing silver, can be applied by, for example, ink jet printing a suitable pattern, such as an interdigitated pattern of fingers, over the areas where the pattern for the emitter and base contacts were printed, one set of fingers covering and connecting the dots for the base contacts, and one set of fingers covering and connecting the dots for the emitter contacts. The contacts are then formed by laser firing, as described above, the area of the fingers where the dots are printed to form the base and emitter contacts with the wafer.

As a final step, the wafer can be annealed by, for example, heating the wafer to a temperature of about 350°C for 15 to 60 minutes or by rapid thermal processing, for example, about 700°C for 1 minute.

Figure 3 shows a cross section of a neutral-surface back-contact photovoltaic cell 1 in accordance with an embodiment of this invention. Figure 3 shows a p-type silicon wafer 5. Such wafer can also be n-type. As in Figure 2, arrows 30 in Figure 3 depict light impinging on the front, light receiving side of the neutral-surface, back-contact photovoltaic cell 1.

Figure 3 shows also intrinsic passivation layer 15 made from a-Si:H. This passivation layer can be deposited as described above with respect to Figure 2 for the induced-inversion-layer back-contact photovoltaic cell. It can be about 4 to about 100 nm thick and, as shown in Figure 3, can be applied only on the back surface of the wafer but can be on the front surface of the wafer as well.

As shown in Figure 3, a layer of dielectric material 20 is deposited on the wafer. Such layer can be, for example, a layer of SiN_x:H, for example, a layer about 70 to about 90 nm thick. The value x can be in the range of about 0.4 to about 0.57. Such layer can be applied as described above with respect to Figure 2 for the induced-inversion-layer back-contact photovoltaic cell. Such layer can function as an anti-reflective coating on the front surface of the layer and as a dielectric layer on the back surface of the layer. The layer 20 on the front surface and the layer 20 on the back surface of the wafer 5 as

shown in Figure 3 can be deposited separately or at the same time. If the dielectric layers are deposited separately, then it is preferable to deposit SiN_x:H., where the value x can be about 0.4 to about 0.57, on the front surface to act as an antireflection layer and to deposit a-SiO_z:H on the back surface, where the value z can be about 0.5 to about 0.66, to optimize the reflection of weakly absorbed infrared light back into the cell.

In the next steps, the emitter contacts 35 and base contacts 40 are formed on the back side of the wafer. These contacts can be formed as described for the induced inversion layer, back-contact photovoltaic cell.

The collection of localized emitter contacts are electrically connected to each other and the collection of localized base contacts are electrically connected to each other so that the electrical current generated by exposing the photovoltaic cell to light can be collected. This can be done by, for example, the methods described above for applying the interdigitated pattern of conducting material using patterns 50 and 60 as shown in Figures 3 and 4.

As a final step, the wafer can be annealed by, for example, heating the wafer to a temperature of about 350°C for 15 to 60 minutes or by rapid thermal processing, for example, at about 700°C for about 1 minute.

Only certain embodiments of the invention have been set forth and alternative embodiments and various modifications will be apparent from the above description to those of skill in the art. These and other alternatives are considered equivalents and within the spirit and scope of the invention.

U.S. Provisional Patent Application 60/895,217, filed on March 16, 2007, is incorporated by reference herein in its entirety.

That which is claimed is:

1. A photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a passivation layer on at least the back surface, a doped layer opposite in conductivity type to the wafer over the passivation layer, an induced inversion layer, a dielectric layer over the doped layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer.

2. The photovoltaic cell of Claim 1 wherein the one or more localized emitter contacts and the one or more localized base contacts are all on the back side of the photovoltaic cell.

3. The photovoltaic cell of Claim 1 wherein the one or more localized emitter contacts and the one or more localized base contact are laser fired contacts.

4. The photovoltaic cell of Claim 1 wherein at least a portion of the base contacts comprise an insulation layer electrically isolating the base contact from the inversion layer.

5. The photovoltaic cell of Claim 1 wherein the semiconductor wafer comprises p-type silicon.

6. The photovoltaic cell of Claim 1 wherein the semiconductor wafer comprises n-type silicon.

7. The photovoltaic cell of Claim 1 wherein at least a portion of the localized base contacts extend through the dielectric layer, the doped layer and the passivation layer.

8. A photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a passivation layer on at least the back surface, a doped layer opposite in conductivity type to the wafer over the passivation layer, a dielectric layer over the doped layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer.

9. A neutral surface photovoltaic cell comprising a semiconductor wafer comprising a front, light receiving surface and an opposite back surface, a neutral passivation layer on at least the back surface, a dielectric layer over the passivation

layer, and one or more localized emitter contacts and one or more localized base contacts on at least the back surface extending at least through the dielectric layer.

10. The photovoltaic cell of Claim 9 wherein the localized emitter contact and localized base contacts are all on the back surface of the photovoltaic cell.

11. The photovoltaic cell of Claim 9 wherein the wherein the one or more localized emitter contacts and one or more localized base contacts are laser fired contacts.

12. The photovoltaic cell of Claim 9 wherein the neutral passivation layer is a-Si:H and is up to about 100 nm thick.

13. The photovoltaic cell of Claim 12 wherein the a-Si:H is at least about 40 nm thick.

14. A method for manufacturing a photovoltaic cell comprising a semiconductor wafer comprising silicon, a front surface and a back surface, the method comprising:

a) depositing a passivation layer on the front and back surfaces of the wafer:

b) depositing a doped layer opposite in conductivity type to the wafer on at least the back surface of the wafer and over the passivation layer;

c) depositing a dielectric layer over at least the doped layer; and

d) forming localized base and emitter contacts on at least the back surface of the wafer and extending at least through the dielectric layer.

15. The method of Claim 14 wherein the base contacts further comprise a layer of insulating material around at least a portion of the base contact.

16. The method of Claim 14 wherein the photovoltaic cell comprises an induced inversion layer and the insulating material electrically insulates the base contact from the inversion layer.

17. The method of Claim 14 wherein the localized base contacts and the localized emitter contacts are formed on the back surface of the photovoltaic cell in an interdigitated finger pattern.

18. The method of Claim 14 wherein a first pattern of electrically conducting material is deposited on the back surface of the electrically connecting the base contacts, and a second pattern of electrically conducting material is deposited on the back surface electrically connecting the emitter contacts.

19. The method of Claim 14 wherein the base and emitter contacts are laser fired contacts.

20. A method for manufacturing a photovoltaic cell comprising a semiconductor wafer comprising silicon, a front surface and a back surface, the method comprising:

a) depositing a passivation layer on at least the back surface of the wafer;

b) depositing a dielectric layer on at least the back surface of the wafer and over the passivation layer; and

c) forming localized base and emitter contacts on at least the back surface of the wafer extending at least through the dielectric layer.

21. The method of Claim 20 wherein the dielectric layer is on the front and the back surface of the wafer.

22. The method of Claim 20 wherein the passivation layer comprises a-Si:H and is about 4 to about 100 nm thick.

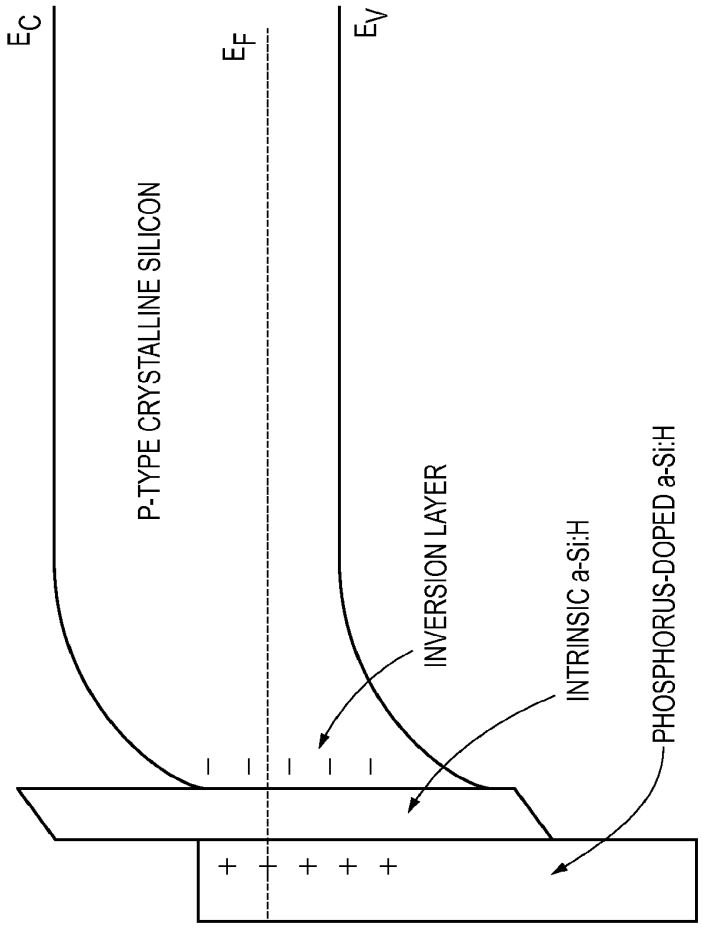
23. The method of Claim 20 wherein the passivation layer and the dielectric layer is combined as one layer that is at least about 40 nm thick.

24. The method of Claim 20 wherein the passivation layer and dielectric layer comprise a-Si:H.

25. The method of Claim 20 wherein a thin doped layer is deposited over the passivation layer and is between the passivation layer and the dielectric layer.

26. The method of Claim 25 wherein the thin doped layer comprises doped a-Si:H and is about 4 to about 20 nm thick.

Fig. 1


E_C
E_F
E_V
P-TYPE CRYSTALLINE SILICON
INVERSION LAYER
INTRINSIC a-Si:H
PHOSPHORUS-DOPED a-Si:H

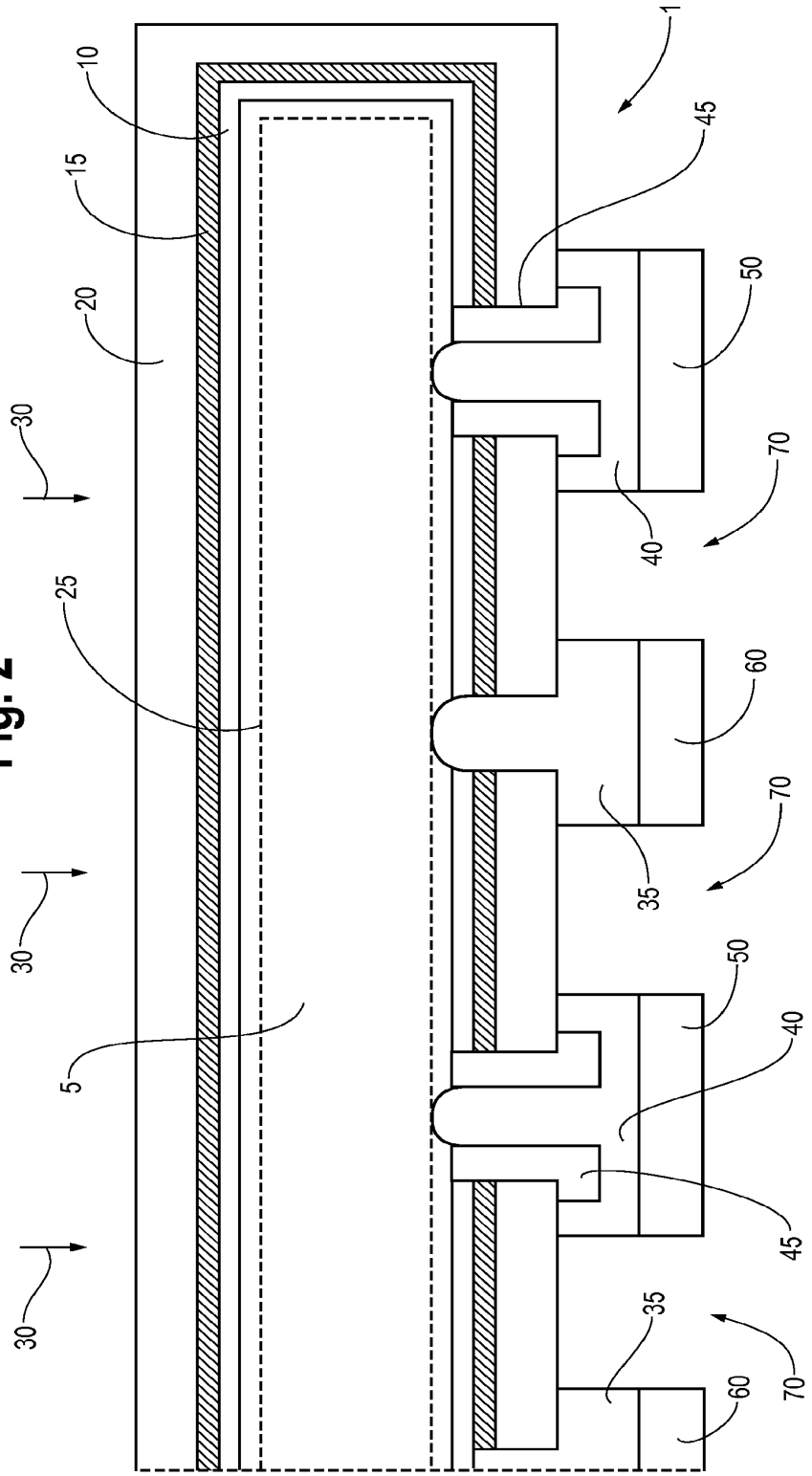


Fig. 2

Fig. 3

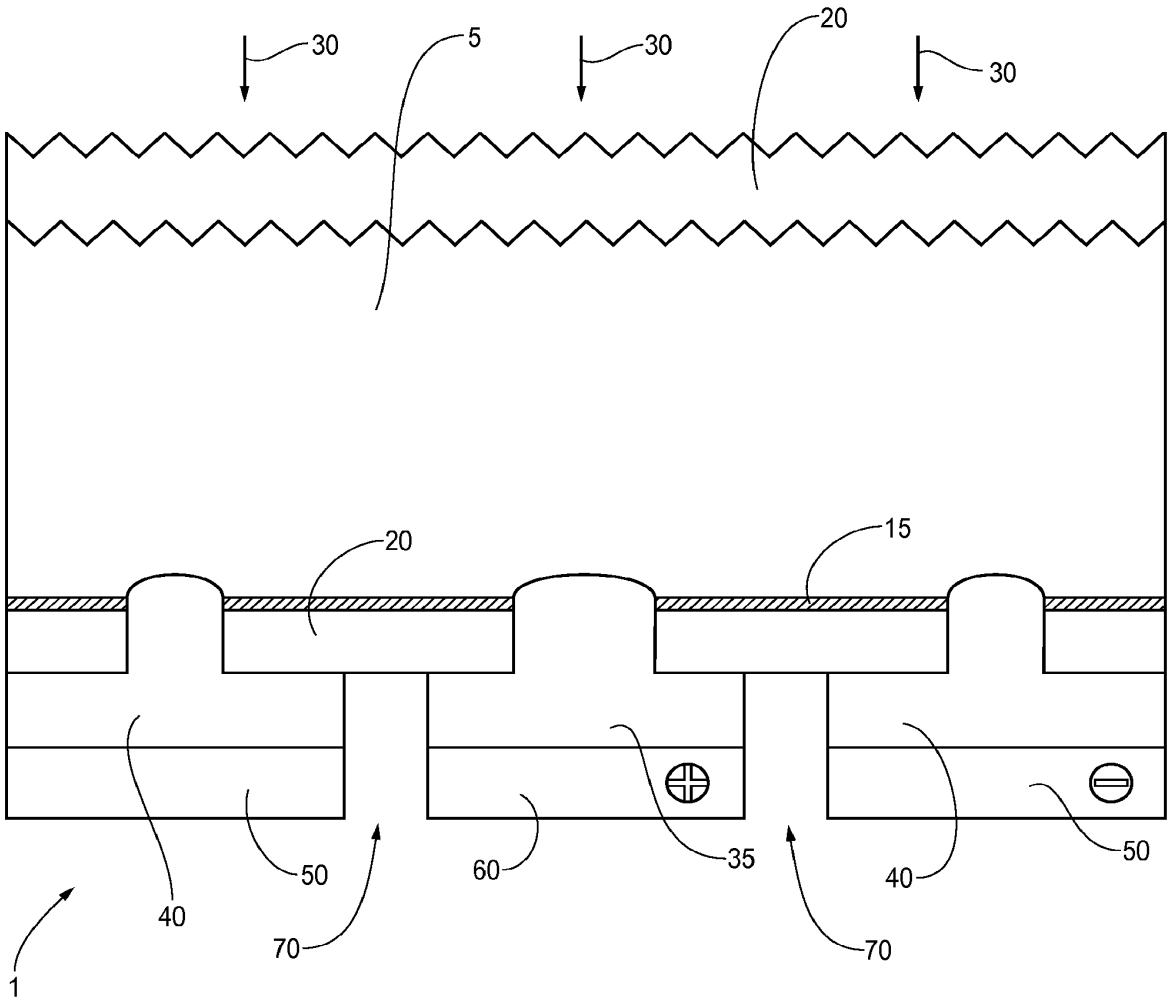
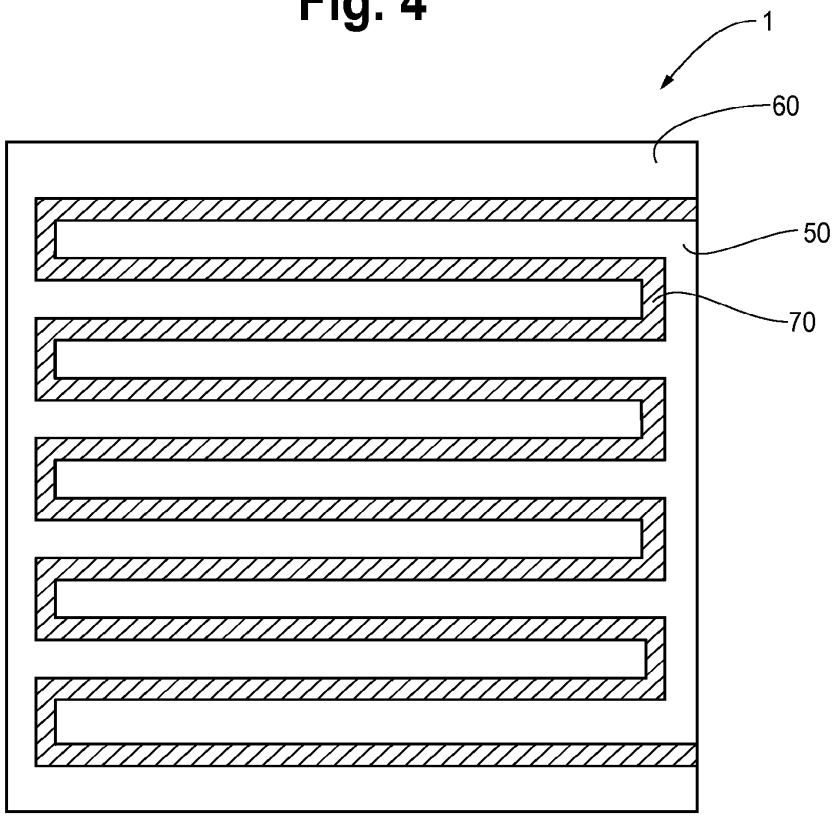


Fig. 4



PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 3304-001AWO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2010/031869	International filing date *(day/month/year)* 21 April 2010	(Earliest) Priority Date *(day/month/year)* 21 April 2009
Applicant TETRASUN, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☒ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the **drawings** to be published with the abstract is Figure No. 6

   ☒ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/031869

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-2

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/031869

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/00 (2010.01)
USPC - 136/261
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/00 (2010.01)
USPC - 136/256, 258, 261; 257/414, 431,439; 438/57, 96, 97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO EAST System (US, USPG-PUB, EPO, DERWENT)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,194,763 B1 (HISAMOTO et al) 27 February 2001 (27.02.2001) entire document	1-2, 9
Y	US 2008/0001169 A1 (LOCHTEFELD) 03 January 2008 (03.01.2008) entire document	1-2, 9
Y	US 2006/0213548 A1 (BACHRACH et al) 28 September 2006 (28.09.2006) entire document	2
A	US 6,924,179 B2 (OH et al) 02 August 2005 (02.08.2005) column 14, lines 30-67	1-2

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 August 2010	18 AUG 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

Continuation of Box III.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-2, 9, drawn to a method of fabricating a solar cell, comprising depositing a passivation layer on a substrate, depositing a conductive layer on the passivation layer; providing thermal treatment; and providing metallization as electrodes.
Group II, claims 3-4, 5-6,9, drawn to a method of forming a solar cell, comprising applying a heat treatment to produce a multifunctional film which separates into a surface passivating interface layer and a highly doped polycrystalline layer with high transparency.
Group III, claims 7-8,9, drawn to a method of forming a solar cell, comprising depositing an amorphous, silicon containing compound and using a heat treatment to activate doping atoms in the compound.

The inventions listed as Groups I, II or III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: depositing a conductive layer on a passivation layer and providing metallization as electrodes as claimed therein is not present in the invention of Groups II or III. The special technical feature of the Group II invention: crystallization of the passivation layer as claimed therein is not present in the invention of Groups I or III. The special technical feature of the Group III invention: using a heat treatment to activate doping atoms in an amorphous, silicon containing compound as claimed therein is not present in the invention of Groups I or II.

Groups II, II and III lack unity of invention because even though the inventions of these groups require the technical feature of forming a solar cell including a passivation layer and heat treating the layers of the solar cell, this technical feature is not a special technical feature as it does not make a contribution over the prior art in view of US 6,924,179 B2 (OH et al) 02 August 2005 (02.08.2005) column 14, lines 30-67.

Since none of the special technical features of the Group I, II or III inventions are found in more than one of the inventions, unity of invention is lacking.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Filer:	Kevin P. Radigan/Staci Medlock
Attorney Docket Number:	3304.001B

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	23249460
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Staci Medlock
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	19-AUG-2015
Filing Date:	
Time Stamp:	14:09:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1600
RAM confirmation Number	385
Deposit Account	081935
Authorized User	RADIGAN, KEVIN P.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	H0367248.pdf	1561437 fc80019f3694b722bcaea27c00266546c80e09b9	no	7
Warnings:					
Information:					
2		H0363482.pdf	224265 2f4ebd735fb7ce64f4b161d485dd84d07bba81b1	yes	42

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	36
Claims	37	41
Abstract	42	42

Warnings:					
Information:					
3	Drawings-only black and white line drawings	H0363211.pdf	1703860 60b24afb0367a4615789c4bfeb9e6697327d4b80	no	12
Warnings:					
Information:					
4	Oath or Declaration filed	H0367018.pdf	809982 427f8ee387a9f317eb5c8d75cad48b52da15b0e2	no	3
Warnings:					
Information:					
5	Power of Attorney	H0367218.pdf	250656 9190146ca5a318c0bb3258232021a3a139d82b2d	no	2
Warnings:					

The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing

Information:

6	Information Disclosure Statement (IDS) Form (SB08)	H0367267.pdf	613853 f5c1c023e94501c798fe304364b403b87d447700	no	6
Warnings:					
Information:					
7	Foreign Reference	H0367225.pdf	495336 8702d68198224e994b8cc9f4eea8e305eb570501	no	7
Warnings:					
Information:					
8	Foreign Reference	H0367224.pdf	1138006 47aded3e5b7aa4143898c1ea2ea7c47306249fb0	no	19
Warnings:					
Information:					
9	Foreign Reference	H0367291.pdf	1074316 13b4005f1c85da38cdb002bed6dfebc46f64d8e9	no	27
Warnings:					
Information:					
10	Foreign Reference	H0367300.pdf	986811 fa31ca13c0a47216f4c98d0fd8b3727f47693200	no	29
Warnings:					
Information:					
11	Foreign Reference	H0367298.pdf	1707826 de8769b767e61159ed709a64f26a35ffcd2bda0f	no	32
Warnings:					
Information:					
12	Non Patent Literature	H0367232.pdf	364540 fbee36546d709e297d989cc72e918d912f465b32	no	5
Warnings:					
Information:					
13	Non Patent Literature	H0367230.pdf	119883 db7c09287b741b1d220b330a75dac9f8aefc2725	no	1
Warnings:					
Information:					
14	Non Patent Literature	H0367233.pdf	136773 0920a0ae662ca7ea1b2981e0dd075d8963b5183a	no	1
Warnings:					
Information:					

15	Non Patent Literature	H0258293.pdf	577296 b628a351c733e6c3861a31410e466c3aea14ce99	no	4
Warnings:					
Information:					
16	Non Patent Literature	H0367280.pdf	487515 3aaecc3430ad744ebb697e5a1dc4d6523dec8fd6	no	4
Warnings:					
Information:					
17	Non Patent Literature	H0367226.pdf	464873 7cd9899e430ad9d6626b86d9a45d465e3c6df03c	no	4
Warnings:					
Information:					
18	Non Patent Literature	H0367227.pdf	341594 33698911f2dee6ba8a56ca81a55f38db3fcf2212	no	3
Warnings:					
Information:					
19	Non Patent Literature	H0367228.pdf	221883 5df944c293364ea388c850c70443aeb535d24063	no	3
Warnings:					
Information:					
20	Fee Worksheet (SB06)	fee-info.pdf	35358 47ab4ed5c4e4a25888d6556c66985217f5aee1d8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	13316063		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (12-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Oliver		SCHULTZ-WITTMANN	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	970 Corte Madera Avenue		
Address 2	Apt. #401		
City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Denis		DeCEUSTER	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Woodside	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	12 SkyLonda Drive		
Address 2			
City	Woodside	State/Province	CA
Postal Code	94062	Country i	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (12-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

☐ **An Address is being provided for the correspondence Information of this application.**			
Customer Number	23405		
Email Address	kpr@hrfmlaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE		
Attorney Docket Number	3304.001B	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	12	**Suggested Figure for Publication (if any)**	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23405		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13265462	2011-10-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13265462	a 371 of international	PCT/US2010/031869	2010-04-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US2010/031869	Claims benefit of provisional	61171194	2009-04-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

PTO/AIA/14 (12-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	TETRASUN, INC.

Mailing Address Information:

Address 1	2161 O-Toole Avenue		
Address 2	Suite 10		
City	San Jose	**State/Province**	CA
Country [i]	US	Postal Code	95131
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3304.001B
	Application Number	
Title of Invention	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE	

Organization Name	TETRASUN, INC.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	2161 O'Toole Avenue		
Address 2	Suite 10		
City	San Jose	**State/Province**	CA
Country i	US	Postal Code	95131
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Kevin P. Radigan, Esq../			Date (YYYY-MM-DD)	2015-08-19
First Name	Kevin P.	Last Name	Radigan, Esq.	Registration Number	31789

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HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

Related Application Information

[0001] This application is a divisional of U.S. Serial No. 13/265,462, filed October 20, 2011, entitled "High-Efficiency Solar Cell Structures and Methods of Manufacture", which claims the benefit of previously filed U.S. Provisional Application entitled "High-Efficiency Solar Cell Structures and Methods of Manufacture," filed April 21, 2009, and assigned application number 61/171,194, both of which are hereby incorporated herein by reference in their entirety.

Technical Field

[0002] The present invention relates to solar cells. More particularly, the present invention relates to improved solar cell structures and methods of their manufacture for increased cell efficiency.

Background of the Invention

[0003] Solar cells are providing widespread benefits to society by converting essentially unlimited amounts of solar energy into useable electrical power. As their use increases, certain economic factors become important, such as high-volume manufacturing and efficiency.

[0004] High volume manufacturing is generally considered to attain a high degree of cost-effectiveness and efficiency if the number of manufacturing steps, and the complexity of each step, can be minimized.

[0005] Finished solar cell efficiencies of 20% or more are highly desired in the industry, however, known embodiments of such efficient cells often suffer from cell structure complexity and/or manufacturing complexity.

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[0006] What is required therefore, are solar cells which attain high operational efficiency, and which can be manufactured in a cost effective manner.

Summary of the Invention

[0007] The shortcomings of the prior art are overcome and additional advantages are provided by the present invention which in one aspect extends to any one or a combination of the solar cell structures disclosed below, including generally a central substrate, conductive layer(s), antireflection layers(s), passivation layer(s) and/or electrode(s). Multifunctional layers provide combined functions of passivation, transparency, sufficient conductivity for vertical carrier flow, the junction, and/or varying degrees of anti-reflectivity. Improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion are also disclosed.

[0008] In one aspect the present invention includes methods of fabricating any of these structures, including: providing a wafer as a central substrate; deposition or growth of interface passivation layers over the substrate; deposition of conductive layers over the passivation layers; providing thermal treatment; optional deposition of antireflective layers (possibly including back side mirrors); and providing metallization as electrodes.

[0009] In one embodiment the present invention comprises applying a heat treatment to produce a multifunctional film which separates into a surface passivating interface layer and a highly doped polycrystalline passivation layer with high transparency.

[0010] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment to initiate crystallization into a polycrystalline film.

[0011] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment which leads to a crystallization of the film and increases the optical transmissivity.

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[0012] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment in order to activate doping atoms in the compound.

[0013] In one embodiment, the present invention comprises depositing an amorphous, silicon containing compound and using a thermal treatment greater than 500°C in order to activate doping atoms in the compound and result in diffusion of dopant atoms into a substrate wafer to provide a high-low junction or a p-n junction.

[0014] Systems and computer program products corresponding to the above-summarized methods are also described and claimed herein.

[0015] Further, additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention.

Brief Description of the Drawings

[0016] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0017] Fig. 1 is an energy band diagram for an n-type crystalline silicon solar cell with doped polysilicon layers and a passivated interface;

[0018] Fig. 2 is a partial cross-sectional view of a solar cell depicting one type of minority and majority carrier flow for a front junction, p-type wafer;

[0019] Fig. 3 is a partial cross-sectional view of a solar cell depicting one type of minority and majority carrier flow for a back junction, p-type wafer;

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[0020] Fig. 4 is a partial cross-sectional view of a solar cell depicting one type of minority and majority carrier flow for a front junction, n-type wafer;

[0021] Fig. 5 is a partial cross-sectional view of a solar cell depicting one type of minority and majority carrier flow for a back junction, n-type wafer;

[0022] Fig. 6 is a partial cross-sectional view of a solar cell having n-type front, n- or p-type wafer, and p-type back;

[0023] Fig. 7 is a partial cross-sectional view of a solar cell having n-type front, n- or p-type wafer, p-type back, in a bifacial configuration;

[0024] Fig. 8 is a partial cross-sectional view of a solar cell having n-type front, n-type wafer, p-type back, and includes isolating the antireflection coating;

[0025] Fig. 9 is a partial cross-sectional view of a solar cell having n-type front, n-type wafer, p-type back, and includes a multifunctional transparent, conductive, highly doped silicon compound layer;

[0026] Fig. 10 is a partial cross-sectional view of a solar cell having n- or p-type wafer, n-type front, including certain front layer improvements, and p-type back;

[0027] Fig. 11 is a partial cross-sectional view of a solar cell having a p-type front, n- or p-type wafer, and n-type back;

[0028] Fig. 12 is a partial cross-sectional view of a solar cell having p-type front, n- or p-type wafer, n-type back, in a bifacial configuration;

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[0029] Fig. 13 is a partial cross-sectional view of a solar cell having p-type front, p-type wafer, n-type back, and includes isolating the antireflection coating;

[0030] Fig. 14 is a partial cross-sectional view of a solar cell having p-type front, p-type wafer, n-type back, and including a multifunctional transparent, conductive, highly doped silicon compound layer;

[0031] Fig. 15 is a partial cross-sectional view of a solar cell having n- or p-type wafer, p-type front, including certain front layer improvements, and n-type back;

[0032] Fig. 16 is a partial cross-sectional view of a solar cell having glass or other transparent film with embedded electrodes, compressed or bonded to the cell;

[0033] Fig. 17 is a partial cross-sectional view of a solar cell having glass or other transparent film with embedded electrodes, compressed or bonded to the cell, including a localized electrode on the back; and

[0034] Fig. 18 is a partial cross-sectional view of a solar cell having additional silicon buffer layers formed therein, all in accordance with the present invention.

Description of the Invention

[0035] With reference to the energy band diagram and partial cross-sectional views of exemplary solar cells of Figs. 1-5, solar radiation is assumed to preferentially illuminate one surface of a solar cell, usually referred to as the front side. To achieve high energy conversion efficiency of incident photons into electric energy, an efficient absorption of photons within the silicon substrate material forming the cell is important. This can be achieved by a low parasitic optical absorption of photons within all layers except the substrate itself.

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[0036] For the sake of simplicity, the geometrical surface shape of layer surfaces (e.g., surface texture such as pyramids, or other surface texture, can be formed on layer surfaces) is not portrayed in these drawings, however, it is understood that the geometrical shape and/or surfaces may be textured in any shape beneficial for improved solar cell efficiency, and falls within the scope of the invention.

[0037] One important parameter for high solar cell efficiency is surface passivation. Surface passivation provides suppression of recombination of electrons and holes at or in the vicinity of certain physical surfaces within the solar cell. Surface recombination can be reduced by the application of dielectric layers. These layers reduce the interface density of states and therefore reduce the number of recombination centers. Two examples are thermally grown silicon oxide and PECVD deposited silicon nitride. Another example of a surface passivating layer is intrinsic amorphous silicon. These layers can also provide an electrical charge which reduces the number of carriers of the opposite polarity and reduces recombination rates via this mechanism. Two examples are silicon nitride and aluminum oxide.

[0038] Another method of reducing the amount of carriers of one type close to a surface is the diffusion of doping atoms either of the same or the opposite doping of the layer doping type. In this case doping levels in excess of the layer doping are necessary to obtain a high-low junction (also commonly called back surface field or front surface field) or a p-n junction. This can be combined with other methods of surface passivation mentioned above.

[0039] Surface passivation can play an important role in achieving highly efficient solar cells. In most of the solar cell structures described below in accordance with the present invention, multiple layers or multifunctional layers can provide excellent surface passivation. This can be achieved via a very steep doping profile and an additional passivation of the interface using a layer with low interface state density and a high band gap resulting in a tunneling barrier for substrate minority carriers to pass. A corresponding energy band diagram is shown in Fig. 1. The solid lines depict the case of an n-type crystalline silicon wafer with a passivated interface and doped polycrystalline

silicon passivation layers. The dotted lines represent the case of an n-type crystalline silicon wafer and a double layer structure of intrinsic amorphous silicon followed by doped amorphous silicon layer, sometimes referred to as a heterojunction cell.

[0040] These structures provide another benefit for a highly efficient solar cell: the recombination in areas underneath the contacts can be as low as in areas without contacts. The contacts can be shielded by the passivation. As a result, the contact area can be optimized for optical properties, thus minimizing resistive losses, but carrier recombination is decoupled.

[0041] Depending on the choice of materials, and doping types and concentrations, the disclosed cell structures may be categorized as front-junction or back-junction cells. In a front-junction cell the minority carriers (in the case of a p-type wafer these are electrons) are collected on the side of illumination. In a back junction cell the minority carriers are collected at the side opposed to the illumination. Current flow patterns are shown generally in the partial cross-sectional solar cell views of Figs. 2-5 for p-type and n-type wafers.

[0042] Fig. 2 shows carrier flow for a solar cell 20, in which minority carriers (solid lines) flow to front electrodes 21 from a p-type wafer 25 having a front junction. The electrons need to use lateral flow within the thin n-type emitter 22 to reach the electrodes 21, and the lateral sheet resistance of the emitter 22 increases resistive losses. The majority carriers (dashed lines) can use the shortest geometrical path to the full area back electrode 29.

[0043] Fig. 3 shows carrier flow for a solar cell 30 from p-type wafer 35 having a back junction. The majority carriers (dashed lines) can use the entire wafer conductivity to reach the front electrodes 31. The minority carriers (solid lines) can use the shortest geometrical path to reach the rear n-type emitter 38, and their transport within the emitter is vertical instead of mainly lateral. This back junction structure reduces the requirements for lateral conductivity of the emitter layer.

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[0044] Fig. 4 shows carrier flow for a solar cell 40, in which minority carriers (solid lines) flow to front electrodes 41 from an n-type wafer 45 having a front junction. The holes need to use lateral flow within the thin p-type emitter 42 to reach the electrodes 41, and the lateral conductivity of the emitter determines the resistive losses. The majority carriers (dashed lines) can use the shortest geometrical path to the full area back electrode 49.

[0045] Fig. 5 shows carrier flow for a solar cell 50 from an n-type wafer 55 having a back junction. The majority carriers (dashed lines) can use the entire wafer conductivity to reach the front electrodes 51. The minority carriers (solid lines) can use the shortest geometrical path to reach the rear p-type emitter 58, and their transport within the emitter is vertical instead of mainly lateral. This back junction structure reduces the requirements for lateral conductivity of the emitter layer.

[0046] A back junction cell with a full area back contact has the advantage that the minority carriers do not have to flow laterally through the emitter to reach the contacts, their transport within the emitter is mainly vertical. This reduces the losses associated with the lateral transport of the minority carriers within the emitter. Since the full contact area coverage is a requirement to benefit from this property of the structure, a shielded contact is important, e.g., since the metal contacts the layer everywhere ("full area contact coverage"), there is no need for the minority carriers to flow laterally toward the nearest contact, like they do within the emitter in, e.g., Fig. 4.

Exemplary Cell Structures: n-type front, n- or p-type wafer, p-type back:

[0047] Fig. 6 is a partial cross-sectional view of a solar cell 60 having an n-type front, n- or p-type wafer, and p-type back.

[0048] The metal electrodes 61 and 69 are positioned on the outer layers 62 and 68, respectively. This has the benefit that the metal does not need to penetrate underlying layers before it contacts the wafer. Furthermore the silicon bulk wafer 65 is shielded from the contact interfaces and hence the contact interface carrier recombination is minimized. This structure has an n-type front surface, which for a p-type wafer 65

collects the minority carriers (electrons) on the front. Therefore a maximum lateral sheet resistance of, for example, 500 Ohm/sq of the combined layers 62, 63 and 64 is required. For an n-type wafer this structure collects the minority carriers (holes) on the back. Therefore the current flow pattern in the solar cell is different and the requirements of lateral conductivity of layer 62 are less critical. Exemplary layers of cell 60 include the following:

[0049] 61: Front metal electrode.

[0050] 62: Transparent and conductive film, refractive index in the range of $1.4 < n < 3$; thickness in the range of 20 nm <thickness<110 nm; sheet resistance of less than 500 Ohm/sq for a p-type wafer (front junction solar cell), specific resistivity in the range of rho < 1000 Ohm cm for an n-type wafer (back junction solar cell). Examples include transparent conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[0051] 63: Electrically passivating and conductive film, highly n-doped $1e18\ cm^{-3} < N_D < 5e21\ cm^{-3}$; thickness in the range of 2 nm <thickness<50 nm ; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[0052] Any of the above listed examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

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[0053] 64: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0054] 65: n-type or p-type crystalline silicon wafer; thickness is the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[0055] 66: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness**.** Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0056] 67: Electrically passivating and conductive film, highly p-doped 1E18-5E21/cm^3; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;
- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-cystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[0057] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[0058] 68: transparent and conductive film, refractive index in the range of $1.4 < n < 3$; specific resistivity in the range of rho < 1000 Ohm cm. Examples include conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[0059] 69: back metal electrode.

[0060] Fig. 7 is a partial cross-sectional view of a solar cell 70 having n-type front, n- or p-type wafer, p-type back, in a bifacial configuration. Cell 70 is similar to cell 60 but includes localized electrodes 79 on the back. Because of the localized structure on the back, photons impinging from the rear of the solar cell can be absorbed within the wafer 75 and produce electron-hole pairs. This can increase the power output generated by the solar cell under outdoor operating conditions where albedo can be used at low additional module manufacturing and installation cost.

[0061] Fig. 8 is a partial cross-sectional view of a solar cell 80 having n-type front, n-type wafer, p-type back, and includes isolating the antireflection coating. This structure is especially beneficial for material combinations where the conductive layers on the front surface of cell structures 60 and 70 have a high absorption. By placing the electrode 81 directly on the contacting layer 83 the conductivity requirements of layer 82 are waived and traditional antireflection coating films (which are insulators) can be used. Exemplary layers of cell 80 include the following:

[0062] 81: Front metal electrode.

[0063] 82: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness in the range of 20 nm <thickness<110 nm. Examples include silicon nitride, silicon carbide, silicon oxide, transparent conductive oxides.

[0064] 83: Electrically passivating and conductive film; thickness <110 nm ; highly n-doped $1e18\ cm^{-3}<N_D<5e21\ cm^{-3}$, specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[0065] Any of the above examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[0066] 84: Electrically passivating interface layer; thickness thickness<10 nm ; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0067] 85: n-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm.

[0068] 86: Electrically passivating interface layer; thickness<10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0069] 87: Electrically passivating and conductive film, highly doped p-doped 1e18 $cm^{-3}<N_A<5e21\ cm^{-3}$; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;

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- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-cystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[0070] Any of the above examples may contain oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[0071] 88: Transparent and conductive film, refractive index in the range of $1.4 < n < 3$; specific resistivity in the range of rho < 1000 Ohm cm. Examples include transparent conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[0072] 89: back metal electrode.

[0073] Fig. 9 is a partial cross-sectional view of a solar cell 90 having n-type front, n-type wafer, p-type back, and including a multifunctional transparent, conductive, highly doped silicon compound layer. This aspect of the invention is an improvement to the other disclosures above, because the functions of layers 62 and 63 of, e.g., solar cell 60 of Fig. 6 (and any other similar layers in any other embodiments disclosed herein) are combined into a multifunctional layer 93a depicted in Fig. 9. This layer can be electrically passivating, transparent, and sufficiently conductive for a vertical carrier flow to the electrodes (back junction solar cell), provides the junction with the wafer 95 and/or reduces the reflectance of the incoming light (e.g., antireflection coating). On the rear, layer 97a can combine the functions of layers 67 and 68 of, e.g., solar cell 60 of Fig. 6 (and any other similar layers in any other embodiments disclosed herein). Layer 97a provides the junction with the wafer 95, has a refractive index which results in a high reflectivity for photons of more than 900 nm wavelength and is sufficiently conductive for vertical carrier flow from the wafer 95 to the metal electrode 99. Exemplary layers of cell 90 include the following:

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[0074] 91: Front metal electrode.

[0075] 93a: Electrically passivating, transparent and conductive film, refractive index in the range of $1.4 < n < 3$; thickness in the range of 20 nm <thickness<110 nm ; specific resistivity in the range of rho < 1000 Ohm cm for an n-type wafer; highly doped n-doped 1e18 cm^{-3}<N_D<5e21 cm^{-3}. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[0076] Any of the above examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[0077] 94: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0078] 95: n-type or p-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[0079] 96: Electrically passivating interface layer; thickness <10 nm ; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0080] 97a: Electrically passivating and transparent and conductive film; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;
- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-crystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[0081] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[0082] 99: back metal electrode.

[0083] Fig. 10 is a partial cross-sectional view of a solar cell 100 having n- or p-type wafer, n-type front, including certain front layer improvements, and p-type back. The rear surface structures (omitted for convenience) can be implemented according to any of the other structures described herein.

[0084] This structure is especially beneficial for material combinations where the layers x3 and x4 on, e.g., the front surface of structures disclosed above, have unacceptably high absorption. (The x3 and x4 notation is further explained below and represents any of the above layers with reference numerals ending in 3,3a, 4, 4a, respectively). In cell 100, by placing layers 103 and 104 under the contacts only, their optical properties (refractive index, absorption) are not important for cell efficiency. Resistance losses only occur through vertical carrier flow to the contacts 101. Layers 102, 104b and 105b also do not have to shield the contact, so they can be optimized for transmissivity and surface passivation. If they do provide lateral conductivity, this will facilitate the current flow towards the contacts and the contact structures can be placed

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further apart from each other. This reduces optical shading losses. This structure works best with a back junction since the lateral conductivity requirements of layer 102, 104b and 105b are waived. Exemplary layers of cell 100 include the following:

[0085] 101: Front metal electrode.

[0086] 102: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness <150 nm. Examples include silicon nitride, silicon carbide, silicon oxide, titanium oxide, transparent conductive oxides.

[0087] 103: Electrically passivating conductive film, e.g., thickness <50 nm ; e.g., specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[0088] Any of the above examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[0089] 104: Electrically passivating interface layer; thickness <10 nm ; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[0090] 104b: Electrically passivating interface layer; thickness <110 nm. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride, silicon carbide or stacks of two or more of these materials.

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[0091] 105: n-type or p-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[0092] 105b: phosphorus diffused silicon layer (optional), sheet resistance >70 Ohm/sq.

[0093] The structures above are not mutually exclusive, and any feature of one structure, can apply to any other structure herein, in accordance with the present invention.

Exemplary Cell Structures: p-type front, n- or p-type wafer, n-type back:

[0094] Fig. 11 is a partial cross-sectional view of a solar cell 110 having a p-type front, n- or p-type wafer, and n-type back.

[0095] In this cell, the metal electrodes 111and 119 are placed on the outer layers 112 and 118, respectively. This provides the benefit that the metal does not need to penetrate underlying layers before it contacts the wafer. Furthermore the silicon bulk wafer 115 is shielded from the contact interfaces and hence the contact interface carrier recombination is minimized. This structure has a p-type front surface, for an n-type wafer this structure collects the minority carriers (holes) on the front. Therefore a maximum lateral sheet resistance of 500 Ohm/sq of the combined layers 112, 113 and 114 is allowed. For a p-type wafer this structure collects the minority carriers (electrons) on the back. Therefore the current flow pattern in the solar cell is different and the requirements on the lateral conductivity of layer 112 are less critical. Exemplary layers of cell 110 include the following:

[0096] 111: Front metal electrodes.

[0097] 112: Transparent and conductive film, refractive index in the range of 1.4 < n < 3; thickness<110 nm ; sheet resistance of less than 500 Ohm/sq for an n-type wafer, specific resistivity in the range of rho < 1000 Ohm cm for a p-type wafer. Examples

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include transparent conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[0098] 113: Electrically passivating and conductive film, highly doped p-doped 1e18 $cm^{-3}<N_A<5e21\ cm^{-3}$; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;
- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-crystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[0099] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[00100] 114: Electrically passivating interface layer; <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00101] 115: n-type or p-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho <20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

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[00102] 116: Electrically passivating interface layer; thickness <10 nm ; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00103] 117: Electrically passivating, transparent and conductive film, highly doped n-doped 1e18 cm^{-3}<N_D<5e21 cm^{-3}; e.g., thickness in the range of 2 nm <thickness<50 nm or more; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[00104] Any of the above examples may contain oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[00105] 118: Transparent and conductive film, refractive index in the range of 1.4 < n < 3; specific resistivity in the range of rho < 1000 Ohm cm. Examples include transparent conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[00106] 119: back metal electrode.

[00107] Fig. 12 is a partial cross-sectional view of a solar cell 120 having p-type front, n- or p-type wafer, n-type back, in a bifacial configuration. Cell 120 is similar to cell 110 but includes localized electrodes 129 on the back. Because of the localized structure on the back, photons impinging from the rear of the solar cell can be absorbed within the

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wafer 125 and produce electron-hole pairs. This can improve the efficiency of the solar cell under outdoor operating conditions where albedo can be used at low additional module manufacturing and installation cost.

[00108] Fig. 13 is a partial cross-sectional view of a solar cell 130 having p-type front, p-type wafer, n-type back, and includes isolating the antireflection coating. This structure is especially beneficial for material combinations where the conductive layers on the front surface of cell structures 110 and 120 have a high absorption. By placing the electrodes 131 directly on the contacting layer 133 the conductivity requirements of layer 132 are waived and traditional antireflection coating films (which are insulators) can be used. This structure works best with a back junction since the lateral conductivity requirements of layer 133 and 134 are not critical. Exemplary layers of cell 130 include the following:

[00109] 131: Front metal electrodes.

[00110] 132: Antireflection film, refractive index in the range of $1.4 < n < 3$; <150 nm. Examples include silicon nitride, silicon carbide, silicon oxide, aluminum oxide, titanium oxide, transparent conductive oxides.

[00111] 133: Electrically passivating, transparent and conductive film; thickness <110 nm; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;
- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-cystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[00112] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[00113] 134: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00114] 135: p-type crystalline silicon wafer; thickness is the range of w<300 um, base resistivity for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[00115] 136: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00116] 137: Electrically passivating, transparent and conductive film, highly doped n-doped 1e18 $cm^{-3}<N_D<5e21$ cm^{-3} ; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;
- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[00117] Any of the above examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[00118] 138: transparent and conductive film, refractive index in the range of $1.4 < n < 3$; specific resistivity in the range of rho < 1000 Ohm cm. Examples include transparent conductive oxides like indium tin oxide, aluminum doped zinc oxide, fluorine doped tin oxide, tantalum oxide, antimony tin oxide, germanium oxide, zirconium oxide, titanium oxide, gallium oxide, cadmium antimony oxide.

[00119] 139: back metal electrode.

[00120] Fig. 14 is a partial cross-sectional view of a solar cell 140 having p-type front, p-type wafer, n-type back, and including a multifunctional transparent, conductive, highly doped silicon compound layer. This aspect of the invention is an improvement to the other disclosures above, because the functions of layers 112 and 113 of, e.g., solar cell 110 of Fig. 11 (and any other similar layers in any other embodiments disclosed herein) are combined into a multifunctional layer 143a depicted in Fig. 14. This layer can be electrically passivating, transparent, and sufficiently conductive for a vertical carrier flow to the electrodes (back junction solar cell), provides the junction with the wafer 145 and/or reduces the reflectance of the incoming light (e.g., antireflection coating). On the rear, layer 147a can combine the functions of layers 117 and 118 of, e.g., solar cell 110 of Fig. 11 (and any other similar layers in any other embodiments disclosed herein). Layer 147a provides the junction with the wafer 145, has a refractive index which results in a high reflectivity for photons of more than 900 nm wavelength and is sufficiently conductive for vertical carrier flow from the wafer 145 to the metal electrode 149. Exemplary layers of cell 140 include the following:

[00121] 141: Front metal electrode.

[00122] 143a: Electrically passivating and transparent and conductive film, refractive index in the range of $1.4 < n < 3$; thickness <150 nm ; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;

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- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-cystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[00123] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[00124] 144: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00125] 145: n-type or p-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[00126] 146: Electrically passivating interface layer; thickness <10 nm ; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00127] 147a: Electrically passivating and transparent and conductive film; specific resistivity in the range of rho < 1000 Ohm cm for a highly doped n-doped 1E18 cm^{-3} $<N_D<$5E21 cm^{-3}. Examples include:

- n-type amorphous or polycrystalline silicon carbides: phosphorus doped silicon carbide, nitrogen doped silicon carbide;

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- n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon, nitrogen doped amorphous silicon;
- n-type amorphous or poly-crystalline diamond-like-carbon: nitrogen doped diamond-like carbon.

[00128] Any of the above examples may include oxygen and hydrogen (n-doped $SiC_xO_yH_z$; n-doped $SiN_xO_yH_z$).

[00129] 149: back metal.

[00130] Fig. 15 is a partial cross-sectional view of a solar cell 150 having n- or p-type wafer, p-type front, including certain front layer improvements, and n-type back. The rear surface structures (omitted for convenience) can be implemented according to any of the other structures described herein.

[00131] This structure is especially beneficial for material combinations where the layers xx3 and xx4 on, e.g., the front surface of structures disclosed above, have unacceptably high absorption. In cell 150, by placing layers 153 and 154 under the contacts only, their optical properties (refractive index, absorption) are not important for cell efficiency. Resistance losses only occur through vertical carrier flow to the contacts 151. Layers 152, 154b and 155b also do not have to shield the contact, so they can be optimized for transmissivity and surface passivation. If they do provide lateral conductivity, this will facilitate the current flow towards the contacts and the contact structures can be placed further apart from each other. This reduces optical shading losses. This structure works best with a back junction since the lateral conductivity requirements of layer 152, 154b and 155b are waived. Exemplary layers of cell 150 include the following:

[00132] 151: Front metal electrode.

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[00133] 152: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness thickness<110 nm. Examples include silicon nitride, silicon carbide, silicon oxide, titanium oxide.

[00134] 153: Electrically passivating conductive film, thickness <110 nm ; specific resistivity in the range of rho < 1000 Ohm cm. Examples include:

- p-type amorphous or polycrystalline silicon carbides: boron doped silicon carbide, aluminum doped silicon carbide, gallium doped silicon carbide;
- p-type amorphous or polycrystalline silicon: boron doped silicon, aluminum doped silicon, gallium doped silicon;
- p-type amorphous or poly-cystalline diamond-like-carbon: boron doped diamond-like carbon, aluminum doped diamond-like carbon.

[00135] Any of the above examples may include oxygen and hydrogen (p-doped $SiC_xO_yH_z$; p-doped $SiN_xO_yH_z$).

[00136] 154: Electrically passivating interface layer; thickness <10 nm; no conductivity requirements because of small thickness; no absorption restrictions due to small thickness. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.

[00137] 154b: Electrically passivating interface layer; thickness <10 nm. Examples include silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride, silicon carbide.

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[00138] 155: n-type or p-type crystalline silicon wafer; thickness is in the range of w<300 um, base resistivity for n-type wafers 0.5 Ohm cm < rho < 20 Ohm cm, for p-type wafers 0.1 Ohm cm < rho < 100 Ohm cm.

[00139] 155b: phosphorus diffused silicon layer (optional), sheet resistance >70 Ohm/sq.

[00140] The structures above are not mutually exclusive, and any feature of one structure, can apply to any other structure herein, in accordance with the present invention.

Exemplary Cell Structures – Alternative Electrode Configurations:

[00141] Fig. 16 is a partial cross-sectional view of a solar cell 160 having glass or other transparent film with embedded electrodes, compressed or bonded to the cell. This alternative applies to any of the structures above, and can include an n- or p-type front, n- or p-type wafer, and p- or n-type back. As an alternative to the metal electrodes being deposited directly on the cell, the metal electrodes 161 and 169 are embedded in a glass or other laminating films 161a and 169a. When the glass or laminating film is compressed or laminated under pressure, the embedded electrodes make contact on top of the outer layers 162 and 168, respectively. This has the benefit that the metal does not need to be deposited directly onto the cell itself, thereby eliminating a typical source of film stress which can cause cell bowing. This is particularly useful when dealing with very large area wafers, such as thin-film silicon sheets and/or very thin wafers. In many of the embodiments above, the metal electrodes do no need to penetrate underlying layers before they contact the cell. Moreover, various conducing materials can be used to enhance the electrical conductivity between the metal electrodes 161 and 169 and the surface of the outer layers 162 and 168. These conducting materials could include but are not limited to anisotropic conducting films (ACF), conductive epoxies, or spring-like contact probes. Exemplary layers of cell 160 include the following (which can be formed of any of the materials above, omitted here for simplicity):

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161a: Glass plate or transparent film carrying embedded metal electrodes.

161: Front metal electrode.

162: Transparent and conductive film.

163: Electrically passivating and conductive film.

164: Electrically passivating interface layer.

165: n-type or p-type crystalline silicon wafer; thickness is the range of w<300 um.

166: Electrically passivating interface layer.

167: Electrically passivating and conductive film.

168: Transparent and conductive film.

169: Back metal electrode.

169a: Glass plate or transparent film carrying embedded metal electrode.

[00142] Fig. 17 is a partial cross-sectional view of a solar cell 170 having glass or other transparent film with embedded electrodes, compressed or bonded to the cell, having localized electrodes 179 on the back. Because of the localized electrode structure on the back, photons impinging the rear of the solar cell can be absorbed within the wafer 175 and produce electron-hole pairs in this bifacial configuration. This can improve the efficiency of the solar cell under outdoor operating conditions where albedo can be used at low additional module manufacturing and installation cost.

[00143] This alternative applies to any of the structures above, and can include an n- or p-type front, n- or p-type wafer, and p- or n-type back. As an alternative to the metal electrodes being deposited directly on the cell, the metal electrodes 171 and 179 are embedded in a glass or other laminating films 171a and 179a. When the glass or laminating film is compressed or laminated under pressure, the embedded electrodes make contact on top of the outer layers 172 and 178, respectively. This has the benefit that the metal does not need to be deposited directly onto the cell itself, thereby

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eliminating a typical source of film stress which can cause cell bowing. This is particularly useful when dealing with very large area wafers, such as thin-film silicon sheets and/or very thin wafers. In many of the embodiments above, the metal electrodes do no need to penetrate underlying layers before they contact the cell. Moreover, various conducing materials can be used to enhance the electrical conductivity between the metal electrodes 171 and 179 and the surface of the outer layers 172 and 178. These conducting materials could include but are not limited to anisotropic conducting films (ACF), conductive epoxies, or spring-like contact probes. Exemplary layers of cell 170 include the following (which can be formed of any of the materials above, omitted here for simplicity):

171a: Glass plate or transparent film carrying embedded metal electrodes.

171: Front metal electrode.

172: Transparent and conductive film.

173: Electrically passivating and conductive film.

174: Electrically passivating interface layer.

175: n-type or p-type crystalline silicon wafer; thickness is the range of w<300 um.

176: Electrically passivating interface layer.

177: Electrically passivating and conductive film.

178: Transparent and conductive film.

179: Back metal electrode.

179a: Glass plate or transparent film carrying embedded metal electrode.

[00144] The structures above are not mutually exclusive, and any feature of one structure, can apply to any other structure herein, in accordance with the present invention.

Fabrication Methods:

[00145] The following process flows are examples of methods to produce the structures disclosed above; but other methods are possible without departing from the scope of the present invention. Initially, the incoming wafer is obtained free of surface damage, may be textured or otherwise modified in its geometrical shape, and has a clean surface. As discussed above, and for the sake of simplicity, the geometrical surface shape of layer surfaces (e.g., surface texture such as pyramids, or other surface texture, can be formed on layer surfaces) is not portrayed in these drawings, however, it is understood that the geometrical shape and/or surfaces may be textured in any shape beneficial for improved solar cell efficiency, and falls within the scope of the invention.

[00146] Subsequent processing steps can be as follows (the use of the designation such as "xx4" or any other similarly designated number connotes the analogous layers of any of the above structures of Figs. 1-18 ending in "4" or "4a" such as 4, 14, 134, 4a, 14a, 134a, etc):

- Deposition or growth of the interface passivation layers xx4 and xx6;
- Deposition of layers xx3 and xx7;
- Thermal treatment;
- Optional deposition of layers xx2 and xx8 (including possibly a low reflective index layer for a good internal mirror on the back - refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5); and
- Metallization.

[00147] In any of the structures above, the layers (e.g., xx2, xx3, xx4, xx6, xx7 and xx8) are electrically conductive are electrically conductive, i.e., the metallization can be placed directly on the outer layer. (In typical high-efficiency solar cells this is not the case since surface passivation is usually done by materials that are also electrical

insulators.) This allows for innovative metallization schemes, for example, the solar cells can be laminated into a module which has the electrodes embedded in the glass or in the lamination sheets. Furthermore, conductive sheets can be applied to mechanically strengthen the cells. Another way of metallization could involve the deposition of thin lines of metals. Due to the conductivity of the surfaces, the requirements on the metal paste are reduced because they directly contact the outer layers and do not need to etch through an insulating layer in order to contact the solar cell. Another example would be the direct evaporation or sputtering of metal onto the conductive surfaces.

[00148] Most layers within the solar cell structures described above can be deposited or grown with methods such as PECVD, APCVD, LPCVD, PVD, plating etc. For some layers and combinations of layers, innovative methods of producing the layers and structures may be useful. For example, thermal oxidation or plasma deposition or plasma assisted oxidation can be used to form the interface passivating layer(s).

[00149] For example, in order to achieve a highly efficient solar cell with a cost-effective production method, it is advantageous to deposit films of different characteristics only on one side. While this can be difficult to do, (e.g., for a standard tube furnace deposition of e.g. LPCVD deposited polycrystalline silicon), a PECVD deposition can be done on one side of a wafer without deposition on the other side. PECVD tools are available on an industrial scale but may only operate in temperature regimes where amorphous or microcrystalline silicon layers can be deposited. In the described cell structures, amorphous silicon layers can be turned into polycrystalline silicon layers by thermal treatment. This also holds true for doped amorphous silicon layers or compounds of amorphous silicon carbides, etc. This crystallization negatively affects the passivation quality of the silicon/amorphous silicon interface layer (if it exists in the cell structure). However, layers xx4 and xx6 buffer the wafer surface from the crystallized polysilicon layer. Therefore, the interface is still passivated after the thermal treatment and the layer systems are stable at the thermal-treatment temperature.

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[00150] In accordance with the present invention, during the crystallization process many properties of the layer change: Donors or acceptors get activated, the optical transmission increases, hydrogen effuses from the layer. The thermal treatment may activate doping atoms in the compound and result in diffusion of dopant atoms into a substrate wafer to provide a high-low junction or a p-n junction.

[00151] In accordance with the present invention, good passivation of layers xx4 and xx6 persists and/or improves after high temperature thermal treatment. Passivation may be adequate after deposition, but the high temperature thermal treatment can improve its character. The passivation is temperature-stable (from 500°C, or 600°C, or 700°C, to 1100°C or more) because of the composition of the layers. Thermal treatment at 500°C or more therefore comprises an aspect of the present invention. Other potential benefits of the structure may include: thermal treatment may not modify the crystallinity of the silicon substrate, at least at the interface, because the first interface layer is amorphous SiO_2, and/or because the conductive layer is SiC. Therefore another aspect of the present invention contemplates providing a thermal treatment without modifying the crystallinity of the silicon substrate, and/or that the interface passivation layer acts as a buffer for re-crystallization during thermal treatment.

[00152] If the layer composition is chosen correctly, a layer deposited in a single process can split into two (or more) layers. The incorporated oxygen in the amorphous deposited layer migrates toward the silicon interface and a thin oxide can be grown. If this mechanism is exploited by the use of oxide containing films xx3 and xx7, the passivating interface layers xx4 and xx6 do not need to be produced prior to layers xx3 and xx7, therefore all described structures can also work without layers xx4 and xx6. At the same time the film crystallizes and dopants may be activated. This effect can be employed to create structures such as cells 90 and 140 disclosed above, in a very short process flow, but it is not restricted to this application. For that reason layers xx3 and xx7 in all structures can be used to employ this mechanism if they contain a low amount of oxygen and the list of examples is expanded by the same layers containing oxygen.

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[00153] In case the passivating interface layers xx4 and xx6 and the highly doped layers xx3 and xx7 were deposited or grown with built-in stress, or the thermal treatment for crystallization described above creates stress, this can negatively affect the passivation properties of the wafer surface xx5. In order to prevent this negative effect, and with reference to the partial cross sectional view of solar cell 180 of Fig. 18 a thin silicon film 1831 and 1871 can be deposited on top of the passivation films 184 and 186, to act as a buffer layer. Fig. 18 illustrates this concept of a silicon buffer layers 1831 and 1871 between the passivation layers 184 and 186 and the highly doped layers 183a, and 187a, respectively. This concept is particularly beneficial for cells 90 and 140 disclosed above, but its application is not limited to these structures.

[00154] This silicon buffer layer can be, for example, undoped polysilicon. In this case, since the film can be deposited on both sides, a standard tube furnace can be used. In a process sequence where the passivation layers 184 and 186 are a thin thermal oxide, the process of oxidation can directly be followed by the deposition of polycrystalline silicon, in the same furnace but a different tube (saving handling of wafers) or even in the same tube. The doping needed for passivation can be produced by driving dopants incorporated in films 183a and 187a, with the temperature treatment used for crystallization at the same time drives the dopants from layers 183a and 187a into layers 1831 and 1871 respectively, making them passivating and conductive. The allowed thickness of the buffer layer depends on the doping level of the doped layers which are deposited on top as well as on the time/temperature profile that is used for crystallization of this doped top layer. The undoped layer is doped during this thermal treatment by the doped layers 183a and 187a. The buffer layers 1831 and 1871can also be composed of multiple silicon layers.

[00155] Another effect of the thermal treatment is the re-organization of the passivating interface layers 184 and 186. Depending on their thickness, the thermal treatment and the layers over them, these layers shrink and via-holes open (e.g., perforation occurs) such that the adjacent layers 1831 and 1871 can make contact to the wafer 185 directly. A very small fraction of the interface allows the carriers to bypass the

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layers 184 and 186. If the thermal treatment is chosen in a way that no or insufficient via-holes open up, the layers 184 and 186 need to be thin enough to allow for tunneling of the carriers.

[00156] Other aspects of the present invention include improved methods of metallization fabrication. In one example, metallization for any of the above structures can be formed in accordance with previously filed U.S. Provisional Application entitled "Method for Forming Structures in a Solar Cell," filed 21 April 2009 and assigned application number 61/171,187; and to commonly-assigned, co-filed International Patent Application entitled "Method for Forming Structures in a Solar Cell," filed as Attorney Docket No. 3304.002AWO and assigned application number PCT/US2010/123976. Each of these Applications is hereby incorporated by reference herein in its entirety. According to these Applications, metallization may be formed according to a method of forming a conductive contact/heterocontact pattern on a surface of solar cell, including forming a thin conductive layer over at least one lower layer of the solar cell, and ablating a majority of the thin conductive layer using a laser beam, thereby leaving behind the conductive contact/heterocontact pattern. A self-aligned metallization may be formed on the conductive contact pattern. The lower layer may include a passivation and/or antireflective layer beneath the thin conductive layer, wherein the conductive contact pattern forms an electrical contact through the at least one lower layer to a semiconductor layer of the solar cell.

[00157] In another example, metallization for any of the above structures can be formed in accordance with previously filed U.S. Provisional Application entitled "Localized Metal Contacts By Localized Laser Assisted Reduction Of Metal-Ions In Functional Films, And Solar Cell Applications Thereof," filed 22 April 2009 and assigned application number 61/171,491; and to commonly-assigned, co-filed International Patent Application entitled "Localized Metal Contacts By Localized Laser Assisted Conversion Of Functional Films In Solar Cells," filed as Attorney Docket No. 3304.003AWO and assigned application number PCT/US2010/031881. Each of these Applications is hereby incorporated by reference herein in its entirety. According to

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these Applications, metallization may be formed according to a method of forming at least one electrical contact in a layer of a solar cell, including forming a layer in the solar cell comprising a material which can be selectively modified to electrical contacts upon laser irradiation; and applying selective laser irradiation to at least one area of the layer to thereby form at least one electrical contact in the area of the layer. A remaining region of the layer may comprise a functional layer of the solar cell and need not be removed; e.g., a transparent, conductive film, and anti-reflective film, and/or passivation as disclosed above.

[00158] The present invention extends to any one or a combination of the solar cell structures disclosed above, including generally a central substrate, conductive layer(s), antireflection layers(s), passivation layer(s) and/or electrode(s). The structures above are not mutually exclusive, and any feature of one structure, can apply to any other structure herein, in accordance with the present invention.

[00159] The present invention includes methods of fabricating any of these structures, including: providing a wafer as a central substrate; deposition or growth of interface passivation layers xx4 and xx6 over the substrate; deposition of conductive layers xx3 and xx7 over the passivation layers; providing thermal treatment; optional deposition of antireflective layers xx2 and xx8 (including possibly a low reflective index layer for a good internal mirror on the back); and providing metallization as electrodes.

[00160] In one embodiment the present invention comprises applying a heat treatment to produce a multifunctional film which separates into a surface passivating interface layer and a highly doped polycrystalline passivation layer with high transparency.

[00161] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment in order to initiate crystallization into a polycrystalline film.

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[00162] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment which leads to a crystallization of the film and increases the optical transmissivity.

[00163] In one embodiment the present invention comprises depositing an amorphous, silicon containing compound and using a heat treatment in order to activate doping atoms in the compound.

[00164] In one embodiment, the present invention comprises depositing an amorphous, silicon containing compound and using a thermal treatment greater than 500°C in order to activate doping atoms in the compound and result in diffusion of dopant atoms into a substrate wafer to provide a high-low junction or a p-n junction.

[00165] One or more of the process control aspects of the present invention can be included in an article of manufacture (e.g., one or more computer program products) having, for instance, computer usable media. The media has embodied therein, for instance, computer readable program code means for providing and facilitating the capabilities of the present invention. The article of manufacture can be included as a part of a computer system or sold separately.

[00166] Additionally, at least one program storage device readable by a machine embodying at least one program of instructions executable by the machine to perform the capabilities of the present invention can be provided.

[00167] The flow diagrams and steps depicted herein are just examples. There may be many variations to these diagrams or the steps (or operations) described therein without departing from the spirit of the invention. For instance, the steps may be performed in a differing order, or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

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[00168] Although preferred embodiments have been depicted and described in detail herein, it will be apparent to those skilled in the relevant art that various modifications, additions, substitutions and the like can be made without departing from the spirit of the invention and these are therefore considered to be within the scope of the invention as defined in the following claims.

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Claims

What is claimed is:

1. A solar cell comprising:

a substrate;

an interface passivation layer over the substrate, the interface passivation layer comprising a conductive dopant diffused throughout;

a passivating film over the interface passivation layer, the passivating film comprising a passivating material and the conductive dopant, wherein the passivating film is at least partially crystallized; and

at least one electrode over the passivating film, the conductive dopant within the passivating film and throughout the interface passivation layer providing direct electrical connection between the at least one electrode and the substrate.

2. The solar cell of claim 1, wherein the interface passivation layer has a thickness that permits tunneling of electrical carriers through the interface passivation layer.

3. The solar cell of claim 1, wherein the conductive dopant of the passivating film is diffused into at least a portion of the substrate.

4. The solar cell of claim 1, further comprising an antireflective layer over the passivating film.

5. The solar cell of claim 1, further comprising at least one conductive film over the passivating film, wherein the at least one electrode contacts the at least one conductive film.

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6. The solar cell of claim 5, wherein the at least one conductive film is a transparent conductive film.

7. The solar cell of claim 1, wherein the at least one electrode does not penetrate through the passivating film.

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8. A method of fabricating a solar cell, comprising:

providing a substrate;

providing an interface passivation layer over the substrate;

providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant;

thermally treating the passivating film, the thermally treating diffusing at least a portion of the conductive dopant from the passivating film throughout the interface passivation layer to facilitate electrical connection to the substrate; and

providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate.

9. The method of claim 8, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

10. The method of claim 9, wherein the crystallized passivating film is a transparent film.

11. The method of claim 9, wherein the crystallization of the passivating film improves a passivation of the passivating film.

12. The method of claim 9, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.

13. The method of claim 8, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.

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14. The method of claim 8, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.

15. The method of claim 8, wherein providing the interface passivation layer and providing the passivating film comprise:

providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;

diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.

16. The method of claim 15, wherein the diffusing of the oxygen comprises thermally treating the amorphous silicon-containing compound, the thermally treating diffusing the conductive dopant from the passivating film throughout the interface passivation layer.

17. The method of claim 8, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.

18. The method of claim 8, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

19. The method of claim 8, further comprising providing at least one conductive film over the passivating film, wherein providing the at least one electrode comprises providing the at least one electrode on the at least one conductive film.

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20. The method of claim 12, wherein the at least one conductive film is a transparent conductive film.

* * * * *

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Abstract of the Disclosure

Solar cells of varying composition are disclosed, generally including a central substrate, conductive layer(s), antireflection layers(s), passivation layer(s) and/or electrode(s). Multifunctional layers provide combined functions of passivation, transparency, sufficient conductivity for vertical carrier flow, the junction, and/or varying degrees of anti-reflectivity. Improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion are also disclosed.

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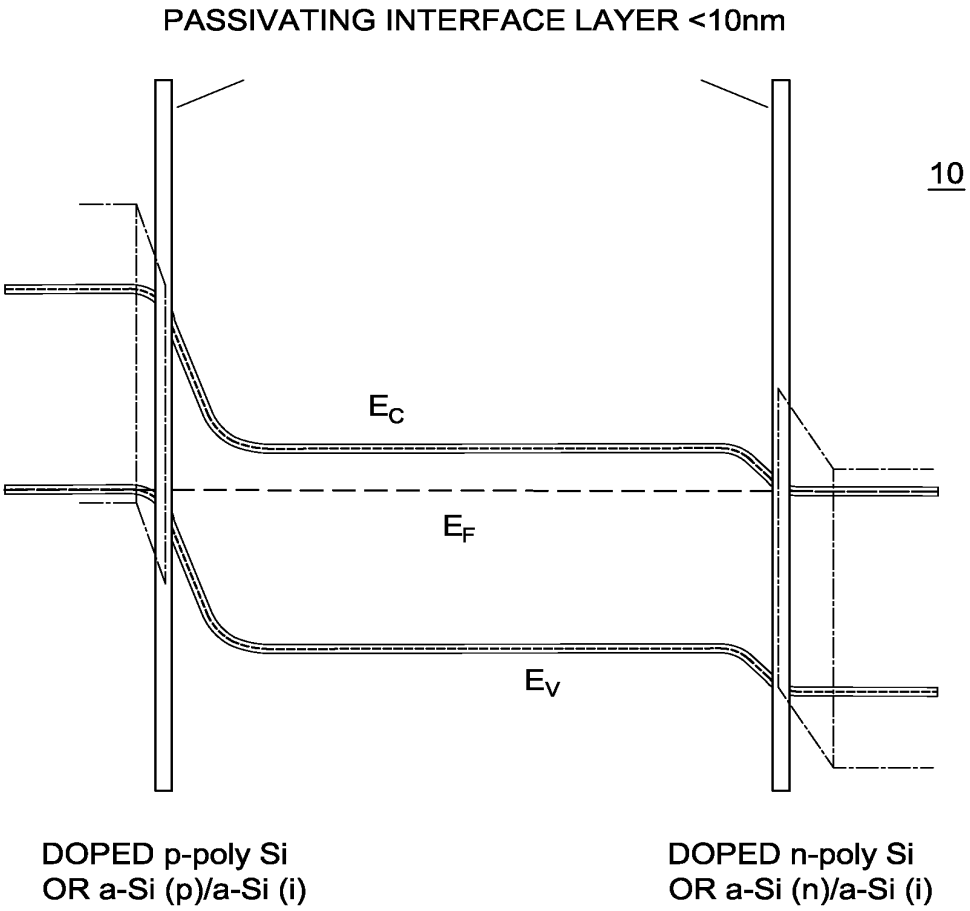

PASSIVATING INTERFACE LAYER <10nm
10
E_C
E_F
E_V
DOPED p-poly Si
OR a-Si (p)/a-Si (i)
DOPED n-poly Si
OR a-Si (n)/a-Si (i)

FIG. 1

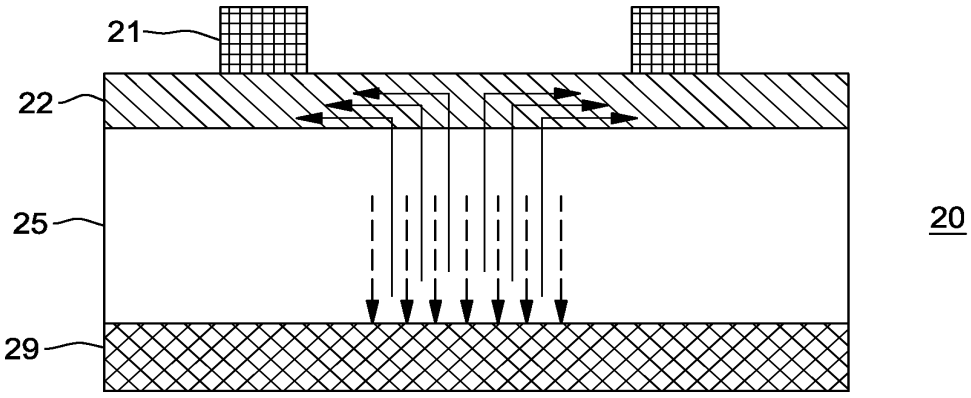


FIG. 2

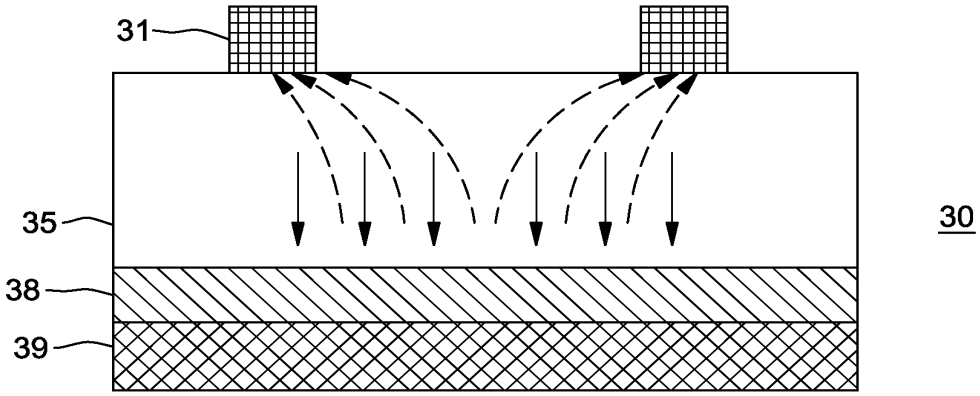


FIG. 3

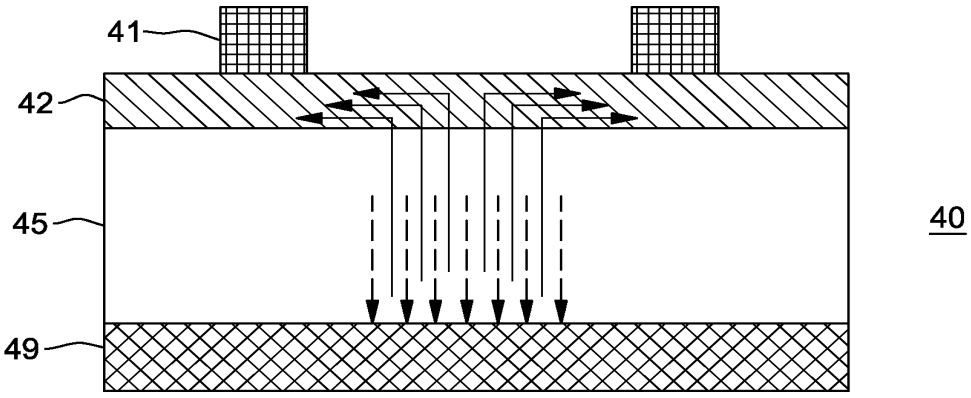


FIG. 4

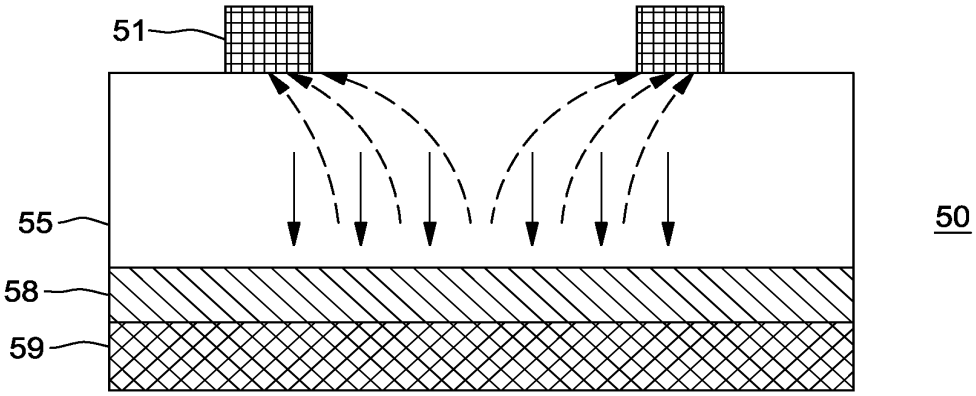


FIG. 5

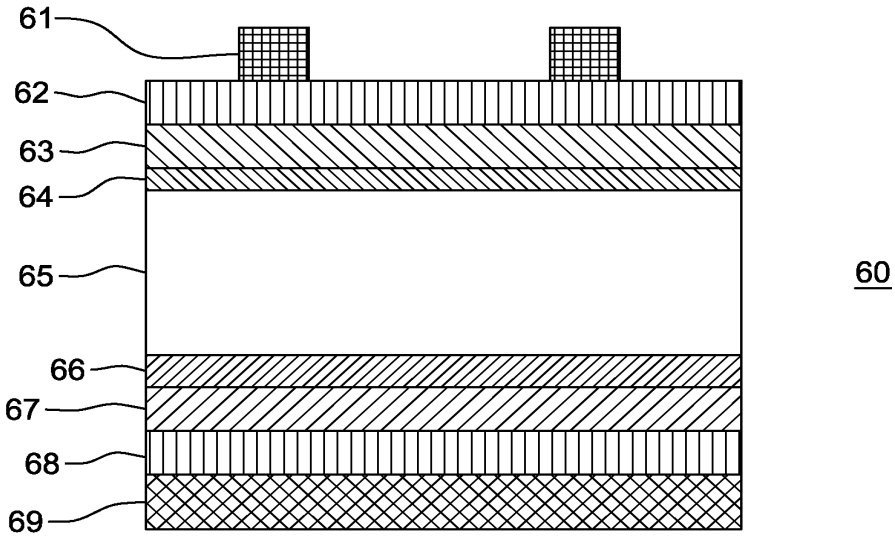


FIG. 6

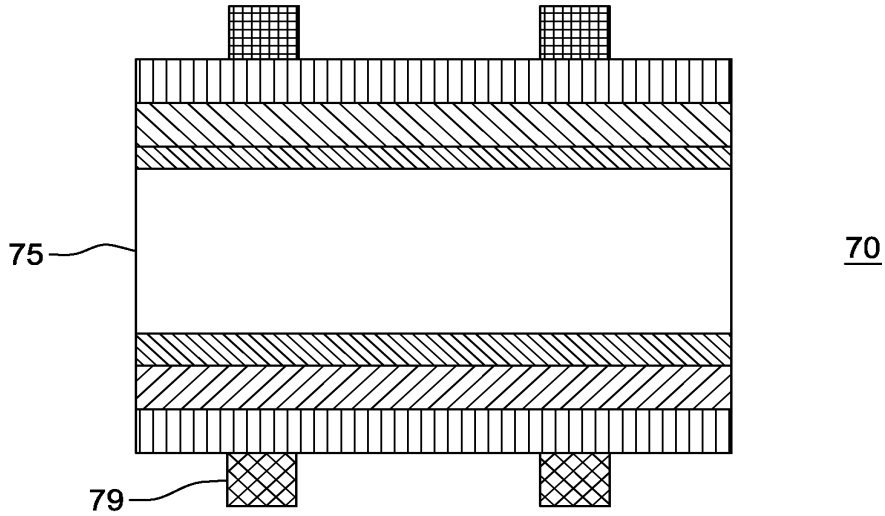


FIG. 7

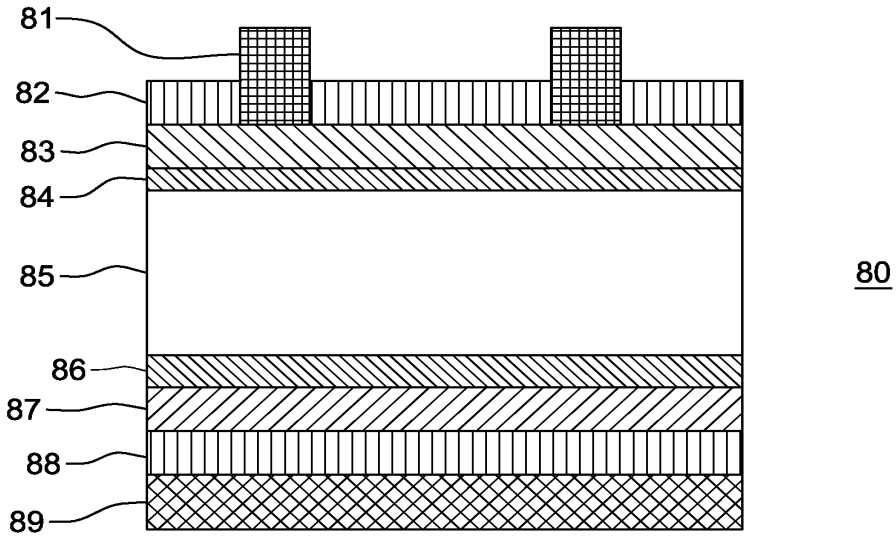


FIG. 8

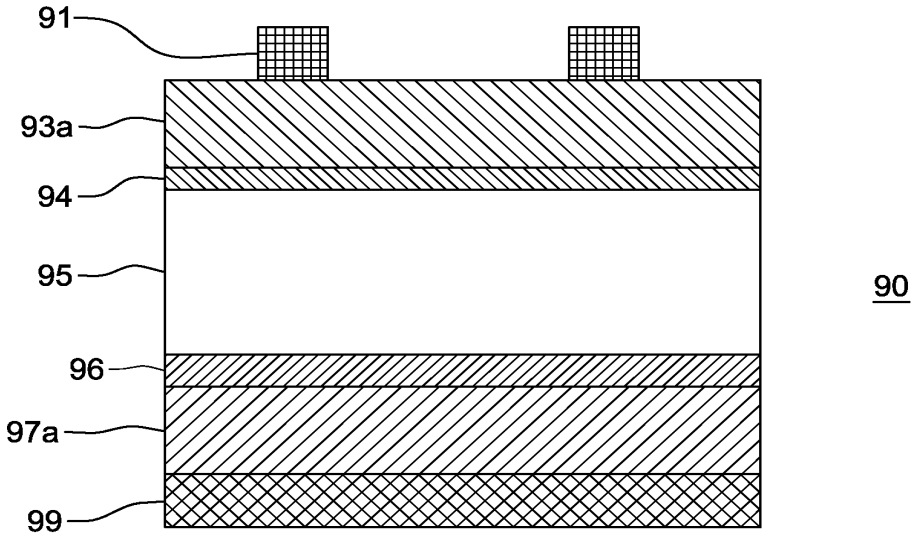


FIG. 9

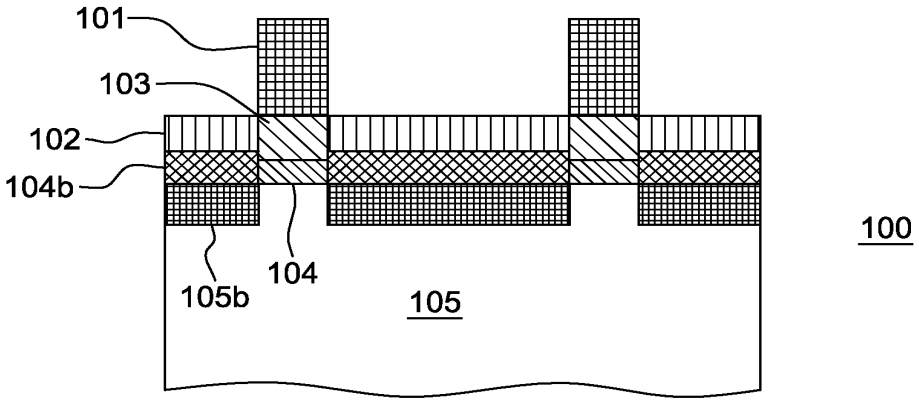


FIG. 10

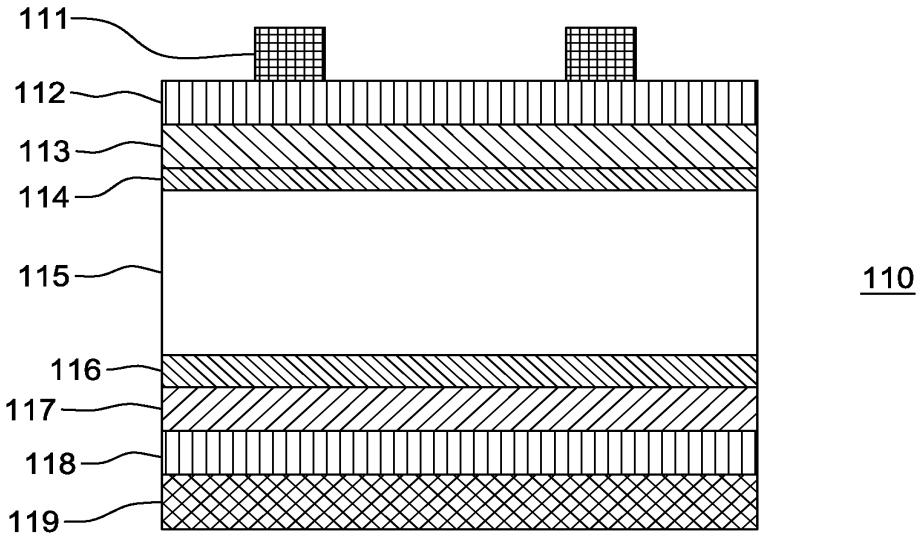


FIG. 11

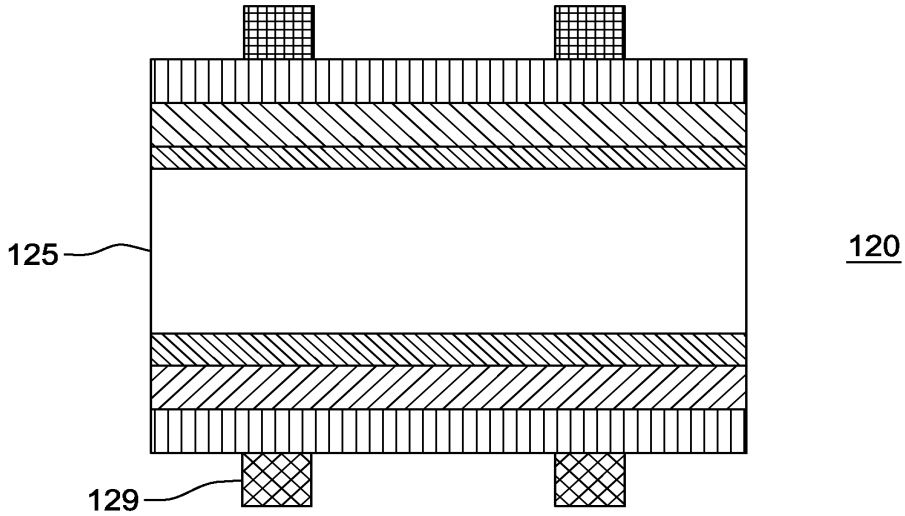


FIG. 12

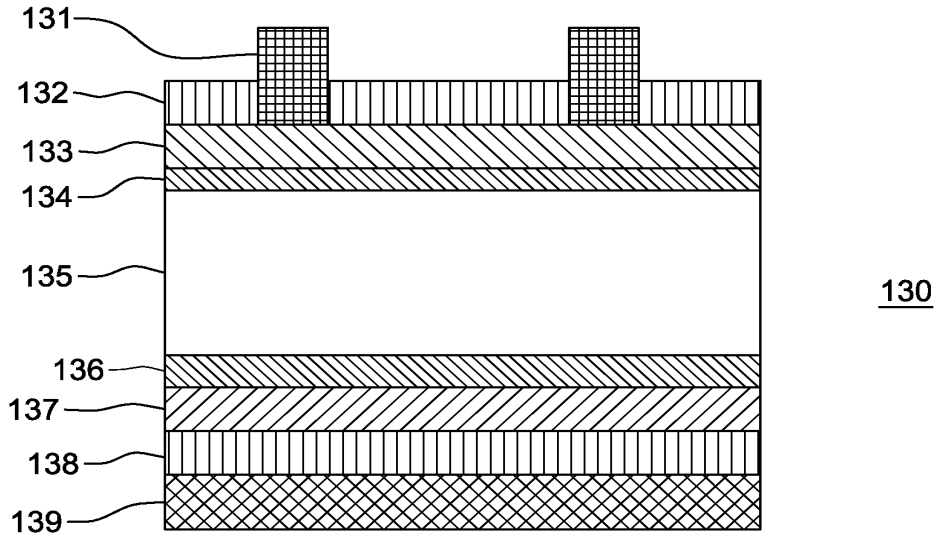

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FIG. 13

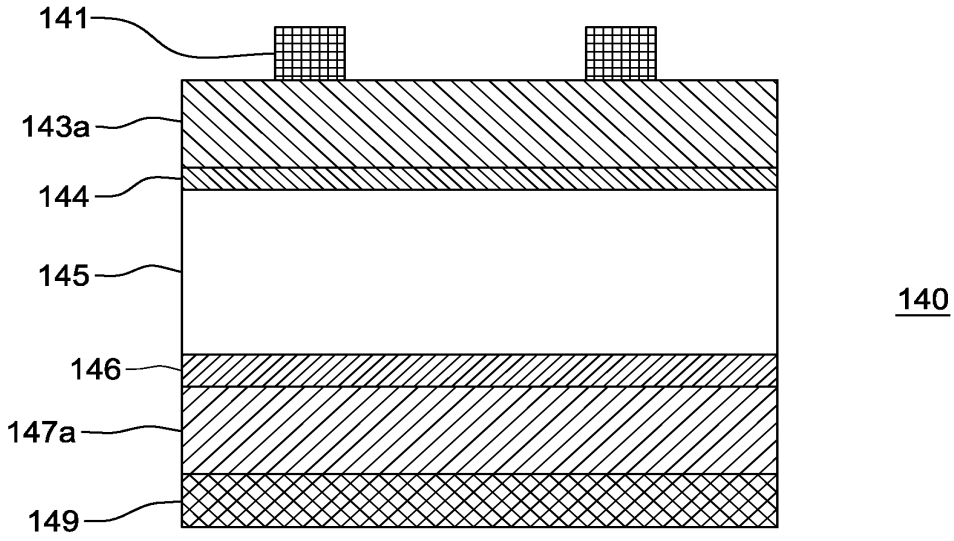

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FIG. 14

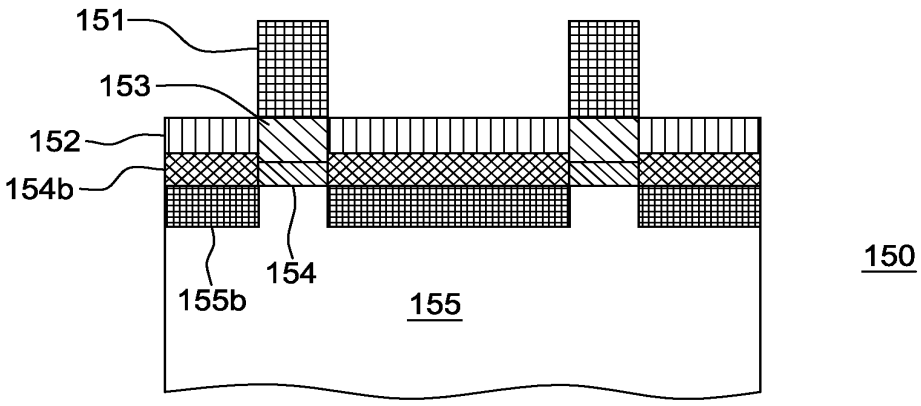


FIG. 15

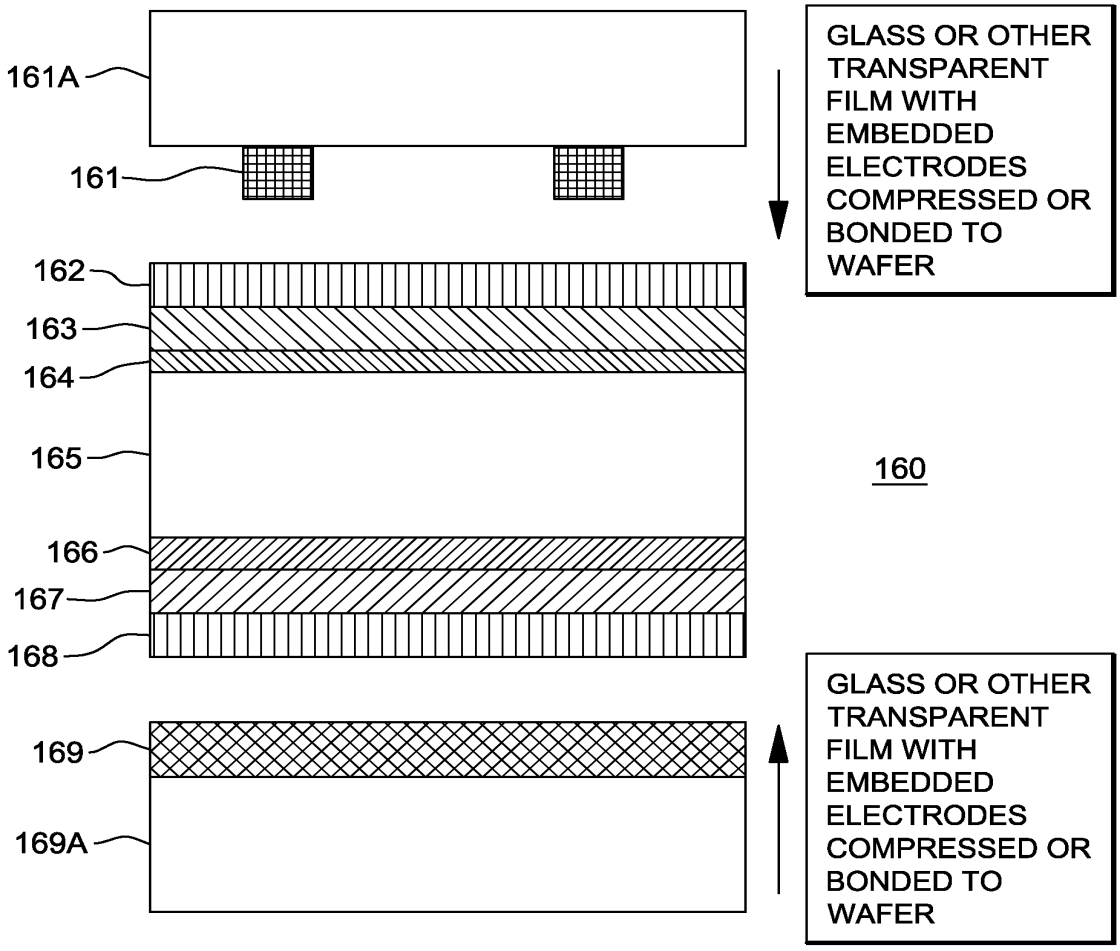

161A
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169A
GLASS OR OTHER TRANSPARENT FILM WITH EMBEDDED ELECTRODES COMPRESSED OR BONDED TO WAFER
160
GLASS OR OTHER TRANSPARENT FILM WITH EMBEDDED ELECTRODES COMPRESSED OR BONDED TO WAFER

FIG. 16

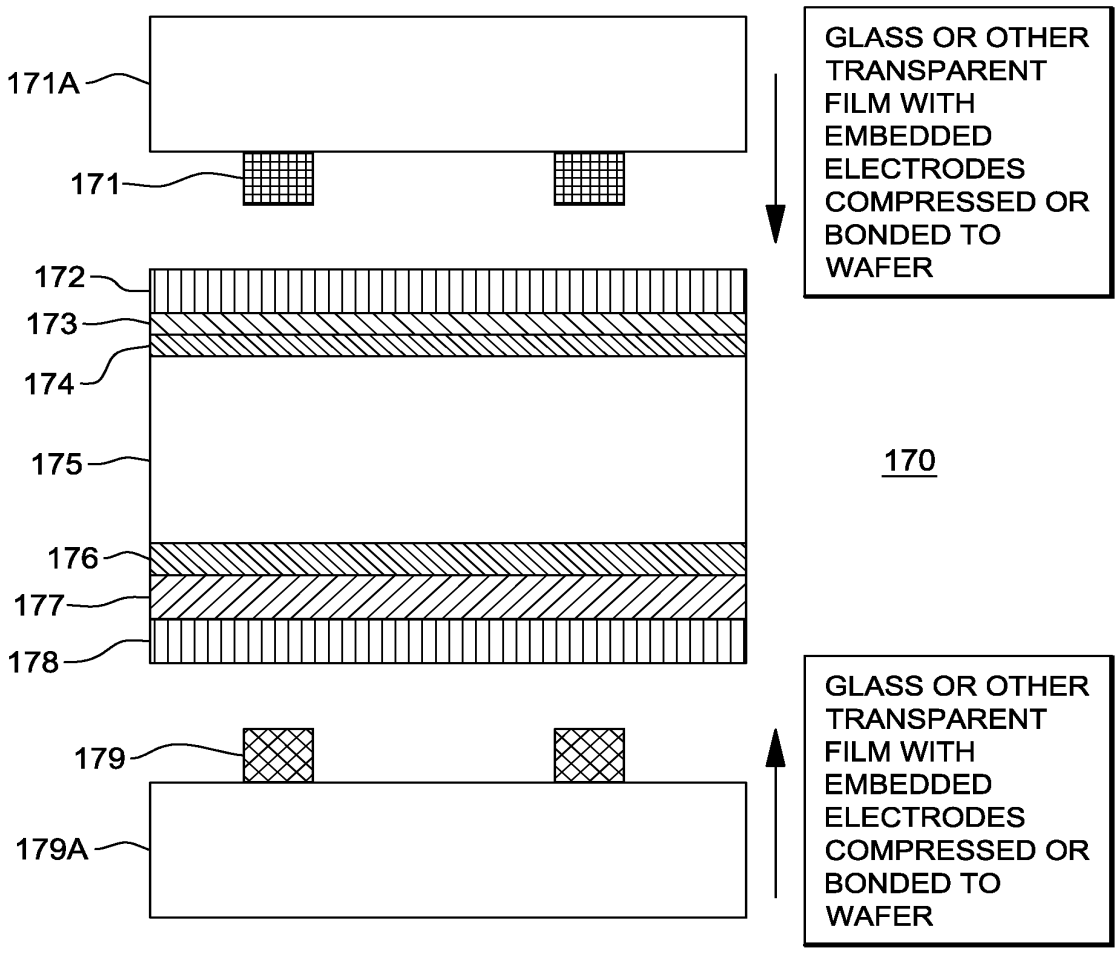

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GLASS OR OTHER TRANSPARENT FILM WITH EMBEDDED ELECTRODES COMPRESSED OR BONDED TO WAFER
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GLASS OR OTHER TRANSPARENT FILM WITH EMBEDDED ELECTRODES COMPRESSED OR BONDED TO WAFER

FIG. 17

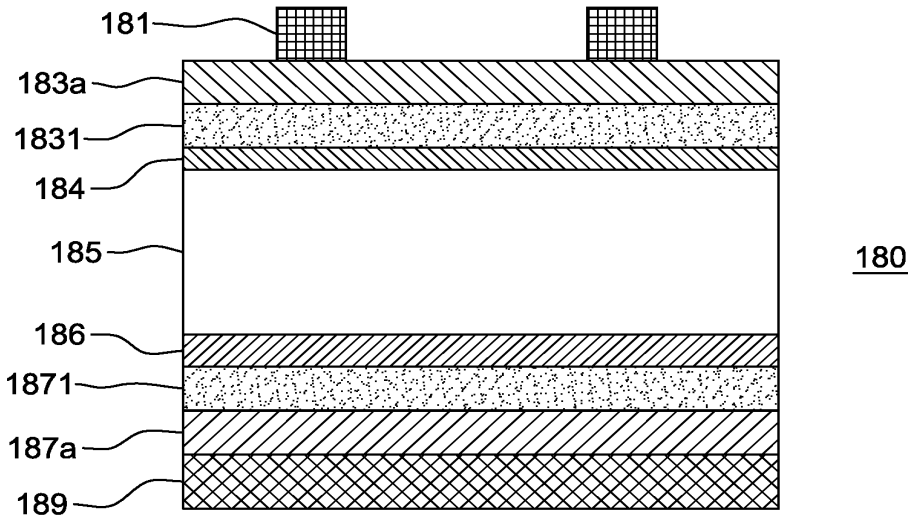


FIG. 18

ASSIGNMENT & DECLARATION

WHEREAS, WE,

Oliver SCHULTZ-WITTMANN, a citizen of the Federal Republic of Germany, residing at 970 Corte Madera Avenue, Apt. #401, Sunnyvale, California 94085 (USA); and

Denis DeCEUSTER, a citizen of Belgium, residing at 12 SkyLonda Drive, Woodside, California 94062 (USA);

have invented certain new and useful improvements in

HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

which is the subject of United States Patent Application Serial Number _____ filed on _____, which is a divisional of U.S. patent application Serial Number 13/265,462, filed October 20, 2011, and for which we have filed an International application pursuant to the Patent Cooperation Treaty on April 21, 2010, which was assigned International Application Number PCT/US2010/031869, which claims priority to United States Provisional Application No. 61/171,194, filed April 21, 2009; and

WHEREAS, **TetraSun, Inc.,** having offices at 2161 O'Toole Avenue, Suite 10, San Jose, California 95131, is desirous of obtaining the entire right, title and interest in, to and under said improvements and said application; and

NOW, THEREFORE, in exchange for good and valuable consideration, the receipt of which I hereby acknowledge, We, **Oliver SCHULTZ-WITTMANN** and **Denis DeCEUSTER**, do hereby assign, transfer and set over to TetraSun, Inc., its successors, legal representatives and assigns, the entire right title and interest in, to and under said improvements, of above-identified application - including the right to claim priority to said application – and all divisions, renewals and continuations thereof, and all Letters Patent which may be granted thereon and all reissues and extensions thereof, and all applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and We hereby authorize and request the

Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to TetraSun, Inc., its successors, legal representatives and assigns, in accordance with the terms of this instrument;

AND WE HEREBY covenant that We have full right to convey the entire interest herein assigned, and that I have not executed, and will not execute, any agreement in conflict herewith;

AND WE HEREBY further covenant and agree that We will communicate to TetraSun, Inc., its successors, legal representatives and assigns, any facts known to me respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid TetraSun, Inc., its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries;

AND WE HEREBY grant Heslin Rothenberg Farley & Mesiti, P.C. the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document;

AND WE HEREBY, as the above named inventors, declare that the above-identified application was made or authorized to be made by us;

AND WE HEREBY, as the above named inventors, declare that We believe that We are the original inventors of a claimed invention in the above-identified application;

AND WE HEREBY state that We have reviewed and understand the contents of the above-identified specification, including the claims;

AND WE HEREBY acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56;

AND WE HEREBY declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that any willful false statements and the like so made in this declaration are punishable by fine or imprisonment of not more than five (5) years, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 18th day of August, 2015.

Oliver SCHULTZ-WITTMANN

Witness

Witness

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this _____ day of Aug 18, 2015.

Denis DeCEUSTER

Witness

Witness

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3489547

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
OLIVER SCHULTZ-WITTMANN	08/18/2015
DENIS DECEUSTER	08/18/2015

RECEIVING PARTY DATA

Name:	TETRASUN, INC.
Street Address:	2161 O'TOOLE AVENUE
Internal Address:	SUITE 10
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95131

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14829999

CORRESPONDENCE DATA

Fax Number: (518)452-5579

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 518-452-5600
Email: sdm@hrfmlaw.com
Correspondent Name: KEVIN P. RADIGAN, ESQ.
Address Line 1: HESLIN ROTHENBERG FARLEY & MESITI P.C.
Address Line 2: 5 COLUMBIA CIRCLE
Address Line 4: ALBANY, NEW YORK 12203

ATTORNEY DOCKET NUMBER:	3304.001B
NAME OF SUBMITTER:	KEVIN P. RADIGAN, ESQ.
SIGNATURE:	/Kevin P. Radigan, Esq./
DATE SIGNED:	08/19/2015
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
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source=H0367018#page3.tif

ASSIGNMENT & DECLARATION

WHEREAS, WE,

Oliver SCHULTZ-WITTMANN, a citizen of the Federal Republic of Germany, residing at 970 Corte Madera Avenue, Apt. #401, Sunnyvale, California 94085 (USA); and

Denis DeCEUSTER, a citizen of Belgium, residing at 12 SkyLonda Drive, Woodside, California 94062 (USA);

have invented certain new and useful improvements in

HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

which is the subject of United States Patent Application Serial Number _____ filed on _____, which is a divisional of U.S. patent application Serial Number 13/265,462, filed October 20, 2011, and for which we have filed an International application pursuant to the Patent Cooperation Treaty on April 21, 2010, which was assigned International Application Number PCT/US2010/031869, which claims priority to United States Provisional Application No. 61/171,194, filed April 21, 2009; and

WHEREAS, **TetraSun, Inc.,** having offices at 2161 O'Toole Avenue, Suite 10, San Jose, California 95131, is desirous of obtaining the entire right, title and interest in, to and under said improvements and said application; and

NOW, THEREFORE, in exchange for good and valuable consideration, the receipt of which I hereby acknowledge, We, **Oliver SCHULTZ-WITTMANN** and **Denis DeCEUSTER**, do hereby assign, transfer and set over to TetraSun, Inc., its successors, legal representatives and assigns, the entire right title and interest in, to and under said improvements, of above-identified application - including the right to claim priority to said application – and all divisions, renewals and continuations thereof, and all Letters Patent which may be granted thereon and all reissues and extensions thereof, and all applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and We hereby authorize and request the

Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to TetraSun, Inc., its successors, legal representatives and assigns, in accordance with the terms of this instrument;

AND WE HEREBY covenant that We have full right to convey the entire interest herein assigned, and that I have not executed, and will not execute, any agreement in conflict herewith;

AND WE HEREBY further covenant and agree that We will communicate to TetraSun, Inc., its successors, legal representatives and assigns, any facts known to me respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid TetraSun, Inc., its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries;

AND WE HEREBY grant Heslin Rothenberg Farley & Mesiti, P.C. the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document;

AND WE HEREBY, as the above named inventors, declare that the above-identified application was made or authorized to be made by us;

AND WE HEREBY, as the above named inventors, declare that We believe that We are the original inventors of a claimed invention in the above-identified application;

AND WE HEREBY state that We have reviewed and understand the contents of the above-identified specification, including the claims;

AND WE HEREBY acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56;

AND WE HEREBY declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that any willful false statements and the like so made in this declaration are punishable by fine or imprisonment of not more than five (5) years, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 6th day of August, 2015.

Oliver SCHULTZ-WITTMANN

Witness

Witness

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this _____day of Aug 18, 2015.

Denis DeCEUSTER

Witness

Witness

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/829,999

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/829,999	08/19/2015	2812	1600	3304.001B	20	2

CONFIRMATION NO. 1023

23405
HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

FILING RECEIPT

OC000000077208786

Date Mailed: 09/02/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

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Assignment For Published Patent Application

TETRASUN, INC., San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 23405

Domestic Priority data as claimed by applicant

This application is a DIV of 13/265,462 11/15/2011 PAT 9130074 *
which is a 371 of PCT/US2010/031869 04/21/2010
which claims benefit of 61/171,194 04/21/2009
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/829,999**

Projected Publication Date: 12/10/2015

Non-Publication Request: No

Early Publication Request: No

Title

HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B

CONFIRMATION NO. 1023

23405
HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

PUBLICATION NOTICE

OC000000079262454

Title:HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

Publication No.US-2015-0357487-A1
Publication Date:12/10/2015

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	2812
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4481046		1984-09-29	Bouldin et al.	
	2	6649956	B2	2003-11-18	Yoshida et al.	

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	1	20080251119	A1	2007-04-13	Forehand et al.	
	2	20090014056	A1	2007-07-09	Hockaday et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	JP-SHO-57-071188	JP	A	1982-01-05	Mitsubishi Electric Corp.	English Abstract Only	X

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	2812
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

	2	JP-H06-111877	JP	A	1994-04-22	Toshiba Lighting & Technology Corp.	English Abstract Only	☒

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	2812
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2016-01-08
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

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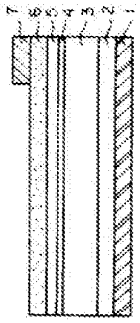
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Lega

(11)Publication number 57-071188
(43)Date of publication of application 01.05.1982
(51)Int.Cl. H01L 31/04

(21)Application number 55-147846
(22)Date of filing 21.10.1980
(71)Applicant MITSUBISHI ELECTRIC CORP
(72)Inventor HIGAKI YUKIO
YUKIMOTO YOSHINORI



(54)AMORPHOUS SOLAR CELL

(57)Abstract

PURPOSE: T obtain P-i-N type cell, of small electric resistance, by constituting most of poly-crystal and a part of amorphous layer in a P type layer, as for a solar cell which consists of a P type semiconductor layer and an i type amorphous semiconductor layer, accumulated subsequently on a substrate, and an N type amorphous semiconductor layer.

CONSTITUTION: An N type layer 2 and an i type layer 3, composed of amorphous layer, and a P type layer 4 are accumulated on a metal substrate 1 of stainless steel or the like. A P type polycrystalline layer 5 is accumulated thereon. A transparent electrode 6 of In-Sn composite is accumulated thereon. An Al metal electrode 7 is attached to an end thereon. In this constitution, the layers 2~4 are formed subsequently by glow discharge or the like. THe layer 5 is formed temporarily as a P type amosphous layer, and mostly converted into poly-crystal, while partly remaining as unification with the P type amorphous layer 4, by applying a laser beam. This allows poly-crystallization so as to decrease the electric resistace as well as reduce absorption coefficient, thereby to make it possible to increase the thickness correspondingly and further lowes the resistance.

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Page 212

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭57—71188

⑤1Int. Cl.³	識別記号	庁内整理番号	⑬公開　昭和57年(1982)5月1日
H 01 L 31/04		7021—5F	

発明の数　1
審査請求　未請求

（全 3 頁）

⑤4アモルファス太陽電池

⑳特　　願　昭55—147846
㉒出　　願　昭55(1980)10月21日
㉜発 明 者　檜垣幸夫
伊丹市瑞原4丁目1番地三菱電機株式会社エル・エス・アイ研究所内
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㉔代 理 人　弁理士　葛野信一　　外1名

明　細　書

1. 発明の名称

アモルファス太陽電池

2. 特許請求の範囲

(1) 基板上に順次積層されたp型半導体層，i型アモルファス半導体層，n型アモルファス半導体層を有するアモルファス太陽電池において、前記p型半導体層は大部分がp型多結晶層半導体層によつて形成されかつ一部がp型アモルファス半導体層によつて形成されていることを特徴とするアモルファス太陽電池。

(2) p型多結晶半導体層は、p型アモルファス半導体層にレーザ光を照射することによつて形成されていることを特徴とする特許請求の範囲第1項記載のアモルファス太陽電池。

3. 発明の詳細な説明

この発明はアモルファス半導体を用いたpin型構造を有する太陽電池に関するものである。

この種の太陽電池においては一般に、光エネルギを受けて電子と正孔のキャリアを発生する部分は主としてi型半導体部に集中しており、p型およびn型層はキャリアの発生には殆んど寄与しない。従つて、光が照射される側にあるp型層については、特に、光の無駄な吸収を防ぐためにできる限り薄く形成する必要がある。

しかしながら、このようにp型アモルファス半導体層を薄くすると、他方で電気抵抗が増大するという問題が生じて来る。

この発明は、このような従来技術における問題を解決するためになされたもので、その目的は、電気抵抗の小さいpin型のアモルファス太陽電池を提供することにある。

このような目的を達成するために、この発明によるアモルファス太陽電池は、p型アモルファス半導体層の大部分を多結晶半導体層によつて置換したものである。以下、実施例によつて、この発明によるアモルファス太陽電池を詳細に説明する。

第1図は、この発明によるアモルファス太陽電池の一実施例を示す断面図である。同図において、ステンレス鋼等の金属基板(1)の上にn型アモルファス

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層(2)，i型アモルファス層(3)，p型アモルファス層(4)，p型多結晶層(5)が積層され、その上に、例えばインジウムとすずの混合物を蒸着することによつて透明電極(6)が形成されている。この透明電極(6)の上に更に、アルミニウム等によつて金属電極(7)が形成されている。該n型アモルファス層(2)，i型アモルファス層(3)，p型アモルファス層(4)は、例えばグロー放電法によつて順次形成される。またp型多結晶層(5)は、一旦p型アモルファス層を形成してこれにレーザ光を照射し、一部をp型アモルファス層(4)として残して大部分を多結晶層に変換することによつて形成される。

このように一旦形成したp型アモルファス層の大部分を多結晶化することにより、電気抵抗を低減することができる。また、多結晶化によつて光の吸収係数が小さくなるために、アモルファス層のみの場合に比べて厚くすることができ、電気抵抗が更に低減される。またこの場合には、はじめから薄いp型アモルファス層を形成しなければならない従来のものに比べ、膜厚の成長条件を緩和することができる利点がある。また、多結晶化する部分の厚さは、照射されるレーザ光の出力を調整することによつて高精度で制御することができる。

第2図は、この発明によるアモルファス太陽電池の他の実施例を示す断面図であり、第1図と同一部分は同一記号を用いてその詳細説明を省略する。同図において、ガラス基板(8)の上に、透明電極(6)が形成され、その上に、ボロンを大量にドーピングしたp型多結晶層(5)が形成されている。このp型多結晶層(5)を形成するには、先ず例えば化学的気相成長法によつてノンドーピングの多結晶層を形成した後にボロンをドーピングしてもよいし、予めドーピングしたガスを用いて化学的気相成長を行なつてもよい。また、グロー放電法により、ガス中にドーピングしながら高温で形成してもよいし、低温でアモルファス状態のものを形成した後に、レーザ光を照射して多結晶化する方法によつてもよい。このp型多結晶層(5)の上に、周辺の一部を残してp型アモルファス層(4)，i型アモルファス層(3)，n型アモルファス層(2)が順次積層されている。これらのアモルファス層は、該周辺の一部を金属マスクで蔽つた状態で、例えばグロー放電法によつて形成することができる。該n型アモルファス層(2)および露出したp型多結晶層(5)の表面上に、金属電極(7a)，(7b)が設けられている。この金属電極は、所定のパターンを有する金属マスクを用い、アルミニウム等の金属を蒸着することによつて形成される。

この場合も、p型半導体層のうちアモルファス層は極く薄く形成し、大部分を多結晶層によつて構成したことにより、電気抵抗を低減することができる。

以上説明したように、この発明によるアモルファス太陽電池によれば、光が照射される側のp型半導体層を、アモルファス層と該アモルファス層よりも小さい比抵抗を有する多結晶層とによつて形成したことにより、アモルファス層のみを用いた場合に比べて電気抵抗を低減することができる。また、該多結晶層はアモルファス層に比べて光の吸収係数が小さいため、キャリア発生部としてのi型半導体部に到達する前にp型半導体層において無駄に吸収される光を減少させることができる。従つて、p型半導体層で吸収される光を一定とした場合には、従来のものに比べて厚く形成することができ、電気抵抗を更に減少させることが可能になると共に、製造が容易になる等の種々優れた効果を有する。

4. 図面の簡単な説明

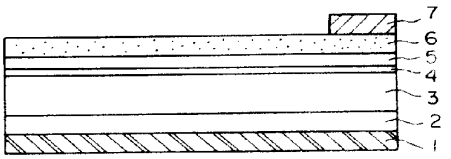
第1図はこの発明によるアモルファス太陽電池の一実施例を示す断面図、第2図はこの発明によるアモルファス太陽電池の他の実施例を示す断面図である。

(1)・・・・金属基板、(2・・・・n型アモルファス層、(3)・・・・i型アモルファス層、(4)・・・・p型アモルファス層、(5)・・・・p型多結晶層、(8)・・・・ガラス基板。

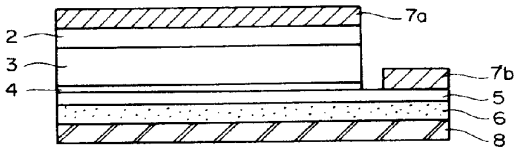
代理人　葛野信一（外1名）

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第1図



第2図



手 続 補 正 書 （自発）

昭和[illegible]年[illegible]月16日

特許庁長官殿

1. 事件の表示　　特願昭 55－147846号 ✓

2. 発明の名称

アモルファス太陽電池

3. 補正をする者

事件との関係　特許出願人
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名 称（601）　三菱電機株式会社
代表者　進　藤　貞　和
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三菱電機株式会社内
氏 名(6699)　弁理士　鈴　野　信　一

(1)

5. 補正の対象

明細書の発明の詳細な説明の欄

6. 補正の内容

(1) 明細書第3頁第3行の「インジウムとすず」を「酸化インジウムと酸化すず」と補正する。

以　上

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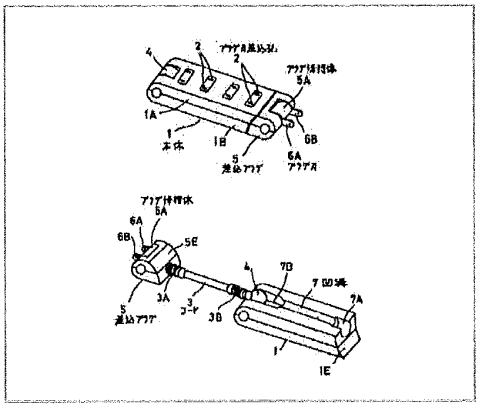
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JP,06-111877,A

PAJ Detail Image

Legal Status

(11)Publication number	06-111877
(43)Date of publication of application	22.04.1994
(51)Int.Cl.	H01R 13/46 H01R 25/00
(21)Application number	04-261069
(22)Date of filing	30.09.1992
(71)Applicant	TOSHIBA LIGHTING & TECHNOL CORP
(72)Inventor	YASUMOTO HIROMI TORII HIRONARI USAMI MAYUMI



(54)MULTIPLE RECEPTACLE

(57)Abstract

PURPOSE: To obtain a combined cord tap device which is simple in constitution and in use and can be used over a wide range with and without a cord attached by providing an accommodating part for an attachment plug and a cord in the main top body.

CONSTITUTION: This tap device includes plug-blade attachment holes 2 in a main body made of electric insulating materials and an attachment plug 5 connected with a cord 3 extending from the main body 1. Accommodating parts 7A, 7B for the attachment plug 5 and the cord 3 and a recessed groove 7 are provided in the main body 1, and when a cord is accommodated, the cord 3 substantially is not protruded from the surface of the main body 1. The attachment plug 5 is an attachment plug form of the same material as that of the main body 1 and is provided with a rotatable plug holder 5A having a pair of plug blades 6A, 6B at its one end, and the cord 3 extending from a cord holder 4 is introduced and electrically connected with the plug blades 6A, 6B.

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(19)日本国特許庁（ＪＰ） (12) **公開特許公報（Ａ）** (11)特許出願公開番号

特開平6－111877

(43)公開日 平成６年(1994)４月22日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｒ 13/46		Ｅ 7161－5Ｅ		
25/00		Ｃ 7354－5Ｅ		

審査請求 未請求 請求項の数３(全 ４ 頁)

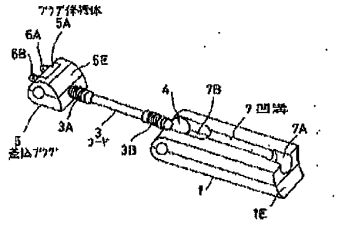
(21)出願番号 特願平4－261039

(22)出願日 平成４年(1992)９月30日

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(74)代理人 弁理士 大胡 典夫

(54)【発明の名称】 テーブルタップ

(57)【要約】
【目的】 構成および使用が簡単でかつ広い範囲でコード類しとしても，コード付きとしても使用できる兼用のコードタップを提供することを目的とする。
【構成】 電気絶縁体からなる本体１にプラグ刃差込孔２およびこの本体１から延出したコード３に差込プラグ５を接続してなり、上記本体１には差込プラグ５およびコード３の収納部１Ｆ、７．７Ａ、７Ｂが設けられコード３収納時に本体１面から実質的にコード３が突出していないことを特徴とするタップである。



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1

【特許請求の範囲】

【請求項１】　電気絶縁体からなる本体にプラグ刃差込孔およびこの本体から延出したコードに差込プラグを接続してなるタップにおいて，上記本体には差込プラグおよびコードの収納部が設けられコード収納時に本体面から実質的にコードが突出していないことを特徴とするテーブルタップ。

【請求項２】　コードは本体の非プラグ刃差込孔側の側面に形成された凹溝内に収容されることを特徴とする上記請求項１に記載のテーブルタップ。

【請求項３】　コードは本体内に収容されることを特徴とする上記請求項１に記載のテーブルタップ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はコンセントから受電して電気機械器具などへ配電するテーブルタップに関する。

【０００２】

【従来の技術】一つのコンセントで複数個の電気機械器具を併用する場合やコンセントと電気機械器具とが離れている場合などにはコンセントにタップやテーブルタップを接続して，このタップに電気機械器具を接続して使用の便宜を図ることが行われている。

【０００３】このタップは２本の突出した受電用の差込プラグを有していて，このプラグをコンセントに差し込み，電気絶縁体で形成した本体の裏面に形成した給電端子用のプラグ刃差込孔に照明用スタンド，炊飯器，テレビ，ビデオ，掃除機，洗濯機などの家庭用電気機器類あるいはコンピュータ，ワードプロセッサー，ファクシミリなどＯＡ用電気機器類のプラグを差し込み使用している。また，テーブルタップは受電用のプラグと給電端子用のプラグ刃差込孔を備えた本体とがコードで接続されたものでコンセントと離れた所で使用される電気機械器具の接続に用いられている。

【０００４】このように従来のタップはそれぞれの用途に応じて使用はできるが，たとえば壁面にあるコンセントにコードなしのタップを差込み使用したいがテーブルタップしかない場合は，テーブルタップを床に置くか，テーブルタップを紐など他の部材で吊るすしかないがコードが邪魔になり，見掛け上も悪い。また，コードが床上配線の場合は歩行者が引掛かかる虞があり安全上も問題がある。

【０００５】

【発明が解決しようとする課題】この発明が解決しようとする問題点は，コンセントへ取付けるタップがコード無しか，コード付きのそれぞれ専用品であって，両者を兼ね備えたものがないということである。

【０００６】本発明はこの点に鑑みなされたもので，構成および使用が簡単でかつ広い範囲で使用できるテーブルタップを提供することを目的とする。

【０００７】

2

【課題を解決するための手段】本発明の請求項１に記載のテーブルタップは，電気絶縁体からなる本体にプラグ刃差込孔およびこの本体から延出したコードに差込プラグを接続してなり，上記本体には差込プラグおよびコードの収納部が設けられコード収納時に本体面から実質的にコードが突出していないことを特徴としている。

【０００８】本発明の請求項２に記載のテーブルタップは，コードが本体の非プラグ刃差込孔側の側面に形成された凹溝内に収納されることを特徴としている。

【０００９】本発明の請求項３に記載のテーブルタップは，コードが本体内に収納されることを特徴としている。

【００１０】

【作用】タップをコード付きとしてもコード無しとしても自在に使用できる。

【００１１】

【実施例】以下，本発明の第一の実施例を図１および図２を参照して説明する。図１はタップＴをコード無しとして使用する場合の態様を上面から示し，図２はコード付きとして使用する場合の態様を裏面から示す。

【００１２】図において１は電気絶縁性の合成樹脂で成型した一対の偏平部材１Ａ，１Ｂを接合して構成した長方形をなす本体で，一方の部材１Ａ面（表面側）には複数個のプラグ刃差込孔２，２，…が設けられている。また，本体１内には上記プラグ刃差込孔２，２，…から挿入されたプラグ刃が接続される受刃端子片（図示しない。）が設けられている。３はコードでこの本体１の一端に回動可能なコード保持体４から延出している。

【００１３】５は本体１と同材質で形成された差込プラグで，一端には一対のプラグ刃６Ａ，６Ｂを有する回動可能なプラグ保持体５Ａが設けられている。また，プラグ保持体５Ａの反対側には上記コード保持体４から延出したコード３が導入されプラグ刃６Ａ，６Ｂと電気的接続をしている。この差込プラグ５は容易に本体１から脱落しないように，それぞれの接合面は円弧面１Ｅ，５Ｅが形成されている。

【００１４】また，他方の部材１Ｂ面（裏面側）にはプラグ刃差込孔が設けてなく長手方向に沿ってコード３収納用の凹溝７が形成してある。なお，この凹溝７の両端は両保持体４，５の接続部に当たる部分でその被覆を太く補強したコード３Ａ，３Ｂに合わせ溝７Ａ，７Ｂを大きくしてある。なお，これらの凹溝７，７Ａ，７Ｂはコード３の径より細い幅であったり途中に突起などが形成してあってコード３が簡単には抜け出ないよう工夫されているとともに実質的にコード３が本体１の表面から突出しないよう収納されている。

【００１５】このような構造のタップＴを図３に示す壁面Ｗのコンセント Ｃに差込み使用する場合は，図１に示すように差込プラグ５が本体１に装着され，コード３もコード収納用の凹溝７内に収められた状態で，約１８０

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度の範囲で回動可能なプラグ保持体５Ａに取付けられたプラグ刃６Ａはコンセント Ｃのプラグ刃差込孔内に挿入され電気的接続をなすとともにタップＴ全体の機械的な保持をもしている。そして．このタップＴのプラグ刃差込孔２、２、…に電気器具（図示しない）のプラグ刃を差込めば電気器具に所定の給電が行える。

【００１６】なお、上記でいう実質的にコード３が本体１の表面から突出しないとは、コンセントＣにタップＴを差込んだときにコード３の表面が少々はみでていても．タップＴの下面がコンセントＣの表面に安定して当接していればよいことを表す。また．このタップＴを床Ｆ上に置いて使用する場合は、図４に示すように本体１から差込プラグ５が外されるとともに．非プラグ刃差込孔側（裏面側）のコード収納用の凹溝７からコード３も取り出され延ばした状態でプラグ刃６Ａをコンセント Ｃのプラグ刃差込孔内に挿入され電気的接続をなさしめるようになっている。

【００１７】このように本発明に係わるタップＴは、コンセントＣに直付けあるいはコード３を介し接続することが可能でその使用範囲を拡大できる。

【００１８】また、図５は本発明の第二の実施例を示し．図中図１および図２と同一部分には同一の符号を付してその説明は省略する。この第二実施例のものはコード３を本体１の側面の孔１Ｆから出入自在としたものである。差込プラグ５は本体１を延長して形成した延長側壁１Ｃ、１Ｃのガイド溝１Ｄ内に収容されている。その使用は、差込プラグ５を持って引っ張ればコード３も引っ張られ本体１内から出て図示のような状態になる。また．逆に差込プラグ５を本体１側に押して行くとコード３は本体１内に入り、差込プラグ５の両側面の突起５Ｆ（一側のみしか見えない）が本体１のガイド溝１Ｄ内の両凹所１Ｆ（一側のみしか見えない）と係合すればコード３なしの利用ができ第一の実施例と同様の作用効果を表する。

【００１９】なお、本発明は上記の実施例に限るものではなく、その趣旨を逸脱しない範囲で種々変形して実施することができる。たとえば、本体の形状は長方形のも＊

＊のに限らず、正四角形や最近流行のキャラクターを模した形など他の形状であってもよい。

【００２０】また、差込プラグの本体への装着係合手段や形状も実施例のものに限らず、差込プラグの刃がコード軸に対して直交しているものであってもよい。

【００２１】さらに、コードはぜんまいなどを用い本体内に巻き取られ収納されたり、全コードが引き出されず中間部までででクリップされるものでもよく、コード自体も螺旋状に巻かれ弾性により伸長するものなどであっても差支えない。

【００２２】

【発明の効果】以上詳述したように本発明によれば，コンセントの取付け位置や電気機器類の種類、配置状況に応じてタップをコード無しあるいはコード付きとして適宜安定使用することができる。このタップはコード付きにも拘らずタップを小形化して、かつ．タップの種類を減らすことができ生産性のうえからも好ましい。

【図面の簡単な説明】

【図１】本発明の第一の実施例を示すテーブルタップの斜視図である。

【図２】図１のテーブルタップの他の態様を示す斜視図である。

【図３】本発明のテーブルタップの使用状態を示す斜視図である。

【図４】本発明のテーブルタップの他の使用状態を示す斜視図である。

【図５】本発明の第二の実施例を示すテーブルタップの斜視図である。

【符号の説明】

Ｔ：タップ

１：本体

２：プラグ刃差込孔

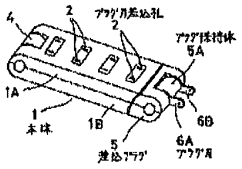
３：コード

５：差込プラグ

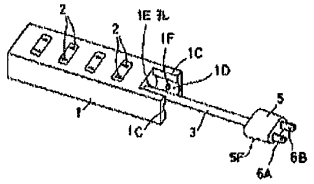
１Ｆ：コード収納部（孔）

７．７Ａ、７Ｂ：コード収納部（凹溝）

【図１】



【図５】



Previous Page | Next Page

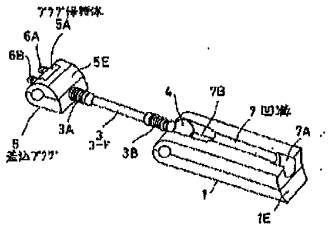
Previous Document 1/1 Next Document

To return to the top of this page

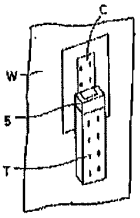
Notice on Usage Privacy Policy Questionnaire

Mundra Solar PV Ltd., Ex. 1002
Page 219

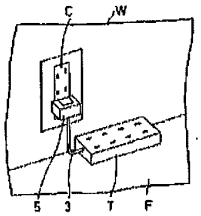
【図2】



【図3】



【図4】



Previous Page | Next Page

Previous Document 1/1 Next Document

To return to the top of this page

Notice on Usage Privacy Policy Questionnaire

Mundra Solar PV Ltd., Ex. 1002
Page 220

Electronic Acknowledgement Receipt

EFS ID:	24572487
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Annette Altheiser
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	11-JAN-2016
Filing Date:	19-AUG-2015
Time Stamp:	11:50:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	H0480527.pdf	612542 5d0d9c4ea2a40110eec96fd2bfc868a8008eb8ad	no	4

Warnings:	
Information:	

2	Foreign Reference	H0478405.pdf	402942 1a50612d4994c9a054b668d4b21cff717f1d2962	no	4
Warnings:					
Information:					
3	Foreign Reference	H0480565.pdf	229722 9c850fbae09a69bfcdd821f8d346c264397d252c	no	5
Warnings:					
Information:					
			Total Files Size (in bytes):	1245206	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

23405 7590 02/08/2016
HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER
SMITH, ERIC R

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
02/08/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/829,999	Applicant(s) SCHULTZ-WITTMANN ET AL.	
	Examiner ERIC R. SMITH	Art Unit 1757	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/19/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-7, drawn to a solar cell, classified in H01L31/068.

II. Claims 8-20, drawn to a method of fabricating a solar cell, classified in H01L31/186.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. The dopant may be diffused throughout the interface passivation layer prior to providing the passivating film, by a process such as ion implantation that does not require thermal treatment.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35

U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process

invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC R. SMITH whose telephone number is (571)270-7186. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Barton can be reached on 571 272 1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERIC R SMITH/
Examiner, Art Unit 1757

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Oliver SCHULTZ-WITTMANN et al. Confirmation No.: 1023

Serial No.: 14/829,999 Group Art Unit: 1757

Filed: August 19, 2015 Examiner: Eric R. Smith

Title: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF FABRICATION

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Response to Office Action

Dear Commissioner:

This paper is filed responsive to the Restriction Requirement contained in the Office Action mailed February 8, 2016, in connection with the above-identified U.S. patent application.

Remarks with election of claims appear on page 2 of this paper.

Mundra Solar PV Ltd., Ex. 1002
Page 229

Remarks

In the Office Action, restriction to one of the following inventions is required under 35 U.S.C. §121:

Group I: Claims 1-7, drawn to a solar cell, classified in H01L31/068.

Group II: Claims 8-20, drawn to a method of fabricating a solar cell, classified in H01L31/186.

In response to this Restriction Requirement, Applicant hereby provisionally elects Group II, claims 8-20, for prosecution on the merits at this time.

If a telephone conference would be of assistance in advancing prosecution of this application, the Examiner is invited to telephone Applicant's undersigned representative.

An Action on the merits of all claims, and a Notice of Allowance therefore, are respectfully requested.

Respectfully submitted,

Kevin P. Radigan

Kevin P. Radigan, Esq.
Attorney for Applicant
Registration No.: 31,789

Dated: March 30, 2016

HESLIN ROTHENBERG FARLEY & MESITI P.C.
5 Columbia Circle
Albany, New York 12203-5160
Telephone: (518) 452-5600
Facsimile: (518) 452-5579

Electronic Acknowledgement Receipt

EFS ID:	25344406
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Annette Altheiser
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	30-MAR-2016
Filing Date:	19-AUG-2015
Time Stamp:	13:22:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	H0551067.pdf	54116 a3cd206ab59eb6208e5421d53c900936b712b857	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	54116

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New Applications Under 35 U.S.C. 111
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/829,999	Filing Date 08/19/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/30/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DORIS BURNS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

23405 7590 04/13/2016

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER
SMITH, ERIC R

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
04/13/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/829,999	Applicant(s) SCHULTZ-WITTMANN ET AL.	
	Examiner ERIC R. SMITH	Art Unit 1757	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/19/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *8-14 and 17-20* is/are rejected.

8)☒ Claim(s) *15 and 16* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *8/19/2015,1/11/2016*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group II, claims 8-20 in the reply filed on 3/30/2016 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.01(a)).

Claim Rejections - 35 USC § 112

> The following is a quotation of 35 U.S.C. 112(b):
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19 and 20 rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 19 recites that the method further comprises providing at least one conductive film over the passivating film, and that providing at least one electrode comprises providing at least one electrode on the at least one conductive film. This claim is indefinite, as a person having ordinary skill in the art could not ascertain the metes and bounds of the claim from the instant disclosure. Claim 8, upon which claim 19 directly depends, requires that an interface passivation layer be provided over a substrate, and a passivating film comprising a passivating material and a conductive dopant be provided over the interface passivation layer. Claim 8 requires that the conductive dopant "provides direct electrical connection between the at least one electrode and the substrate". A special technical definition of what constitutes a "direct electrical connection" is not provided.

Paragraphs [00153]-[00155] of the instant specification recite an embodiment of the invention which claim 8 reads upon. In this embodiment, a buffer layer (1831) is formed on a passivation film (184).

A highly doped layer (183a) is formed on the buffer layer. In that embodiment, layer (1831) does not comprise conductive dopant throughout until after it is diffused from layer (183a), and the layer (184) does not comprise conductive dopant throughout (if at all) until pinholes open in that layer. The examiner interprets the layer (1831) therefore to read on the claimed interface passivation layer, as it is not recited as comprising conductive dopant until after the thermally treating step. The examiner interprets the highly doped layer (183a) as reading on the passivating film, as it comprises conductive dopant and, in some embodiments, a passivating material (presumably amorphous silicon, as discussed in paragraph [00152]). Further, an analogous at least one electrode (181) is provided over (and contacting) the passivating film. In that way, the conductive dopant of the passivating film and post-thermally treating interface passivation layer can be reasonably assumed to provide direct electrical connection between the at least one electrode and the substrate.

Although the highly doped layer (183a) may read on the conductive film in an interpretation, the layer (1831) cannot read on the passivation film, as it does not comprise conductive dopant until after thermal treatment. Therefore, that embodiment does not seem to comprise at least one conductive film in addition to the at least one electrode (181).

Other embodiments do comprise conductive films xx2, which are generally recited as transparent conductive films which may comprise, *inter alia*, aluminum doped zinc oxide (paragraph [0050] and the like). However, the disclosure does not provide sufficient context for a person having ordinary skill in the art to assume an alternative embodiment in which a conductive layer comprising aluminum doped zinc oxide is also formed over a layer such as the highly doped layer (183a) which fulfills "wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate".

The examiner also notes that claim 20, which claims dependence from claim 12, recites that the at least one conductive film is a transparent conductive film. **Claim 20** is indefinite because the limitation “the at least one conductive film” lacks antecedent basis.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).

Claims 8, 9, 11, and 12 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US PGPub 6,821,875 to Wenham (included in Applicant's IDS filed 8/19/2015), and further in view of WO2007/125903A1 to Fukushima (included in Applicant's IDS filed 8/19/2015, US PGPub 2009/0235972 relied upon as a translation).

Regarding claims 8, 9, 11, and 12, Wenham teaches a method of fabricating a solar cell comprising

- Providing a substrate 11 (Fig. 11, C11/L11-18)
- Providing an interface passivation layer 14 over the substrate (amorphous silicon layer 14 is formed at interface 18 of substrate 11, C11/L43-46)
- Providing a passivating film 12/13 over the interface passivation layer 14, the passivating film comprising a passivating material (passivation properties of oxide in sublayer 12 described in C1/L12-20, C8/L24-39, C9/L4-11) and a conductive dopant (aluminum, C7/L14-36)
- Thermally treating the passivating film 12/13, the thermally treating diffusing at least a portion of the conductive dopant from the passivating film throughout the interface passivation layer 14 to facilitate electrical connection to the substrate (Figs. 12-14, C11/L19-42; Wenham is clear that more than one region of diffused dopant 26 is formed to extend through the interface passivation layer, therefore the combination of such a plurality of regions results in at least a portion of the conductive dopant being diffused throughout the interface passivation layer).

The thermal treatment of the passivating film results in a metal layer 13 and a region of diffused conductive dopant 26 providing a direct electrical connection to the substrate 11 (Fig. 14). Wenham does not teach a step of providing at least one electrode over the passivating film. Fukushima teaches that it is known in the art to form an electrode (element 5a in Figs. 3-5, referred to as "bus electrodes" in the text) over similar passivating films (layer 8 analogous to metal layer 13 of Wenham) in order to provide a stable electrical contact that extracts current from a solar cell (¶0010-0016, 0055-0062). Therefore it would have

been obvious at the time of invention for a person having ordinary skill in the art to provide an electrode over the passivating film in order to extract current from the solar cell.

As the conductive dopant within the passivating film and throughout the interface passivation layer provide an connection which extends from the interface 18 of the substrate 11 to the conductive metal layer 13 formed entirely of conductive dopant, the conductive dopant necessarily provides a direct electrical connection between the at least one electrode, formed in the way of Fukushima on the conductive metal layer, and the substrate.

Per claim 9, modified-Wenham teaches the limitations of claim 8. The thermally treating replaces at least a portion of the passivating film 12/13 with a crystallized passivating film 26 coincident with a region of diffused dopant (Fig. 14, previously cited passages). Therefore the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

Per claim 11, modified-Wenham teaches the limitations of claim 9. Wenham teaches that the passivating film 12/13 converts in part to a crystallized passivating film 26 (Fig. 14, previously cited passages). Wenham teaches that such crystallized films shields the high surface recombination velocity associated with a metal silicon interface (C7/L26-31). Therefore the crystallization necessarily improves a passivation of the passivating film because it provides an electrical contact which has better surface recombination properties than the previous passivating film 12/13, which provided no electrical contact.

Per claim 12, modified-Wenham teaches the limitations of claim 9. The interface passivation layer 14 of the embodiment of Figs. 11-14 intercedes between a metal portion 13 of the passivating film 12/13 and the substrate 11. During the thermal treating process, the material of the interface passivation layer 14 diffuses away from the crystalline interface 18 of the substrate into the metal portion 13 to form a crystallized passivating film 26, using the crystalline interface as a template (C5/L26-44, C10/L55-C11/L2, C11/L18-46). Wenham elsewhere discusses how the availability of such a material as in the interface passivation layer protects a crystalline interface from reaction with a metal portion (C7/L42-62). Further, the direct alloying of an interface with a metal portion is not desirable (Fig. 7, C8/L5-12). Therefore a person having ordinary skill in the art would appreciate that the interface passivation layer chemically interacts with the metal portion of the passivating film to enable crystallization during the thermally

treating, and the substrate does not undergo such crystallization or recrystallization. The examiner therefore interprets modified-Wenham to teach "wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.

Claim 20 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomas and Schmidt as applied to claim 8 above, and further in view of US Patent 4,577,393 to Schmidt.

Regarding claim 20, modified-Wenham teaches the limitations of claim 12. Claim 20, as noted above, is indefinite, as there is no antecedent basis for the at least one conductive film in claims 8, 9, or 12. Claim 20 will therefore be interpreted to require that at least one conductive film in the form of a transparent conductive film is required to be present in or on the solar cell.

Wenham teaches electrodes 23 formed on a light receiving surface of the solar cell in some embodiments (Fig. 10). Wenham does not teach at least one transparent conductive film. Schmidt teaches that a transparent conductive film may be present on a light receiving surface of a solar cell, to allow for collection of current and to provide antireflection properties (Figs. 1-5, C3/L15-C4/L30). It would have been obvious at the time of invention for a person having ordinary skill in the art to include at least one transparent conductive film in order to collect current from the solar cell and to provide antireflection properties.

Claims 8, 9, 11, and 19 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wenham, and further in view of Fukushima. This rejection relies upon a different interpretation of Wenham than relied upon directly above.

Regarding claims 8, 9, 11, and 19, Wenham teaches a method of fabricating a solar cell comprising

- Providing a substrate 11 (Fig. 11, C11/L11-18)
- Providing an interface passivation layer 14 over the substrate (amorphous silicon layer 14 is formed at interface 18 of substrate 11, C11/L43-46)

- Providing a passivating film 12/25 over the interface passivation layer 14, the passivating film comprising a passivating material (passivation properties of oxide in sublayer 12 described in C1/L12-20, C8/L24-39, C9/L4-11) and a conductive dopant (aluminum found in alloyed region 25 of Fig. 13, C7/L14-36)
- Thermally treating the passivating film 12/25, the thermally treating diffusing at least a portion of the conductive dopant from the passivating film throughout the interface passivation layer 14 to facilitate electrical connection to the substrate (Figs. 12-14, C11/L19-42; Wenham is clear that more than one region of diffused dopant 26 is formed to extend through the interface passivation layer, therefore the combination of such a plurality of regions results in at least a portion of the conductive dopant being diffused throughout the interface passivation layer).

Per claim 19, the method further comprises providing at least one conductive film 13 over the passivating film 12/25 formed of the conductive dopant. The thermal treatment of the passivating film results in a region of diffused conductive dopant 26 providing a direct electrical connection to the substrate 11 through the conductive film 13 (Fig. 14). Wenham does not teach a step of providing at least one electrode over the passivating film, or that the provision of the at least one electrode comprises providing the at least one electrode on the at least one conductive film. Fukushima teaches that it is known in the art to form an electrode (element 5a in Figs. 3-5, referred to as "bus electrodes" in the text) over similar conductive films (layer 8 analogous to film 13 of Wenham) in order to provide a stable electrical contact that extracts current from a solar cell (¶0010-0016, 0055-0062). Therefore it would have been obvious at the time of invention for a person having ordinary skill in the art to provide an electrode over the at least one conductive film in order to extract current from the solar cell. As such, the electrode of modified-Wenham would also necessarily be provided over the passivating film.

As the conductive dopant within the passivating film and throughout the interface passivation layer provide an connection which extends from the interface 18 of the substrate 11 to the conductive layer 13 formed entirely of conductive dopant, the conductive dopant necessarily provides a direct

electrical connection between the at least one electrode, formed in the way of Fukushima on the conductive metal layer, and the substrate.

Per claim 9, modified-Wenham teaches the limitations of claim 8. The thermally treating replaces at least a portion of the passivating film 12/25 with a crystallized passivating film 26 coincident with a region of diffused dopant (Fig. 14, previously cited passages). Therefore the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

Per claim 11, modified-Wenham teaches the limitations of claim 9. Wenham teaches that the passivating film 12/25 converts in part to a crystallized passivating film 26 (Fig. 14, previously cited passages). Wenham teaches that such crystallized films shields the high surface recombination velocity associated with a metal silicon interface (C7/L26-31). Therefore the crystallization necessarily improves a passivation of the passivating film because it provides an electrical contact which has better surface recombination properties than the previous passivating film 12/25.

Claim 10 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wenham and Fukushima as applied to claim 9 directly above. Supporting information is provided by US PGPub 2003/0136440 to Machida (included in Applicant's IDS filed 8/19/2015).

Regarding claim 10, modified-Wenham teaches the limitations of claim 9. The examiner interprets the claimed method to read on the embodiment of paragraph [00150] of the instant specification. In that passage, a crystallization process due to a thermally treating step is described as increasing the optical transmission**.** Paragraph [00153]-[00155], also reading on the claimed method, describes a doped layer (183a) being converted to a more crystalline version by a thermal treatment (also see paragraph [00160]-[00162]. The examiner interprets "wherein the crystallized passivating film is a transparent film" to encompass a film which has increased in transparency due to its crystallization. Other embodiments discuss conductive films xx2 which are transparent; however, those layers are not disclosed as undergoing crystallization, and are not interpreted as reading on the passivating film.

As such, Wenham clearly teaches that the passivating film portion 25 undergoes crystallization during the thermally treating step from an amorphous silicon-aluminum alloy to a crystallized passivating film 26 comprising doped crystalline silicon (Figs. 11-14, previously cited passages). Machida teaches

that crystalline silicon materials are more optically transmissive than amorphous silicon materials (¶0013, 0014, 0028, 0076). Therefore the thermally-treating step of modified-Wenham results in a crystallized passivating film that is a transparent film.

Claims 8, 14, and 18, rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US PGPub 2010/0105190 to Tomas (included in Applicant's IDS filed 8/19/2015), and further in view of US Patent 4,577,393 to Schmidt.

Regarding claims 8, 14, and 18, Tomas teaches a method of fabricating a solar cell comprising

- Providing a substrate 10 (Figs. 3, ¶0023, 0033, 0036, 0037)
- Providing an interface passivation layer 20 over the substrate (¶0024, 0025, 0035)
- Providing a passivating film 24 over the interface passivation layer 20, the passivating film comprising a passivating material and a conductive dopant 22 (¶0031)
- Thermally treating the passivating film 24, the thermally treating diffusing at least a portion of the conductive dopant 22 from the passivating film throughout the interface passivation layer 20 (¶0027, 0028, 0038).

Tomas teaches that the degree of dopant loading in the interface passivation layer 20 and passivating film 24 may be changed relative to each other to achieve the desired behavior from those elements (¶0033), and that the parameters of the thermal treating step can be tuned to arrive at a desired conductive dopant profile (¶0038). Although Tomas refers to providing an electrode over the substrate in regards to prior art methods (¶0005), Tomas does not specifically teach that the thermally treating facilitates electrical connection to the substrate nor explicitly teach the step of providing at least one electrode over the passivating film, such that the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate.

Schmidt teaches a similar method of fabricating a solar cell, in which a step of thermally treating a film (elements 2, 3 of Figs. 1-5) comprising conductive dopants causes diffusion of those dopants into a similar substrate (1) (C3/L15-C4/L20), and further teaches performing the thermal treating step to

facilitate direct electrical connection between the substrate and at least one electrode (7) provided over the film via the conductive dopant in order to provide an electrical connection to the substrate (C4/L21-30). It would have been obvious at the time of invention for a person having ordinary skill in the art to perform the thermal treating step to facilitate direct electrical connection to the substrate by the provision of at least one electrode over the passivating film via conductive dopant throughout the passivating film and interface passivation layer in order to extract electricity from the solar cell.

Per claim 14, modified-Tomas teaches the limitations of claim 8. Tomas's invention allows for the thermally treating step to diffuse a portion of the conductive dopant 22 through the interface passivation layer 20 into the substrate 10 (Figs. 3, ¶0027, 0028, 0033, 0038).

Per claim 18, modified-Tomas teaches the limitations of claim 8. A person having ordinary skill in the art, informed of the teachings of Tomas and Schmidt, would form the at least one electrode to only electrically connect to the substrate through the passivating film via the conductive dopant because the combination of references only teaches that connection. In other words, it would have been obvious at the time of invention for a person having ordinary skill in the art to electrically connect the at least one electrode to the substrate through the passivating film through the conductive dopant because the combination of references teaches that manner of connection alone.

Claim 13 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomas and Schmidt as applied to claim 8 above, and further in view of US Patent 4,694,117 to Friedrich.

Regarding claim 13, modified-Tomas teaches the limitations of claim 8. Tomas teaches that the interface passivation layer and passivating film can be formed to a thickness between 30 and 120 nm, and in an embodiment, 80 nm (¶0035, 0041), in order to optimize anti-reflection properties of the combination of layers. Neither Tomas nor Schmidt specifically teach that the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate. Friedrich teaches a similar sequence of layers as the interface passivation layer and passivating film of modified-Tomas (element 3 of Fig. 3), upon which is formed at least one electrode (5), and teaches that such a sequence of layers can be formed with an aggregate thickness that is selected to

permit tunneling of electrical carriers through the sequence of layers into the substrate, wherein a thickness of 70 nm is suggested (C1/L34-45, C1/L53-61, C2/L41-57, C3/L27-38). The use of a known technique to improve similar devices (methods or products) in the same way is likely to be obvious. See *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421, USPQ2d 1385, 1395 – 97 (2007) (see MPEP § 2143, C.). Therefore it would have been obvious at the time of invention for a person having ordinary skill in the art to provide the interface passivation layer and passivating film of an aggregate thickness to permit tunneling of electrical carriers through the layers into the substrate because forming such layers of that thickness is a known improvement in the art. As such, the thickness of the interface passivation layer would necessarily permit tunneling of electrical carriers.

Claim 17 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomas and Schmidt as applied to claim 8 above, and further in view of US Patent 5,131,933 to Flödl.

Regarding claim 17, modified-Tomas teaches the limitations of claim 8. Tomas does not teach an additional step of providing an anti-reflective film over the conductive upper surface of the passivating film. Flödl teaches a step of providing an anti-reflective film (element 9 of Figs. 1, 3E, 4F) after the provision of at least one electrode (6) (C2/L42-45, C3/L6-31, C4/L2-4). The combination of familiar elements is likely to be obvious when it does no more than yield predictable results. See *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421, 82 USPQ2d 1385, 1395 – 97 (2007) (see MPEP § 2143, A.). Therefore it would have been obvious at the time of invention for a person having ordinary skill in the art to provide an anti-reflective film over the at least one electrode because the provision of such a film is known in the art. As the at least one electrode is necessarily also over the conductive upper surface of the passivation film of modified-Tomas, the anti-reflective film would also be over the conductive upper surface of the passivating film.

Allowable Subject Matter

Claims 15 and 16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any

intervening claims. Claim 15 recites that the step of providing the interface passivation layer and providing the passivating film comprises providing an amorphous silicon-containing compound with both an oxygen dopant and a conductive dopant, followed by the step of diffusing the oxygen dopant into the upper surface of the substrate to form an oxide layer. US PGPub 2010/0075485 to Rana is the closest prior art. Rana teaches providing an amorphous silicon containing compound (element 260 of Fig. 3) over an upper surface (244) of a substrate (226), and the diffusion of an oxygen dopant through the amorphous silicon-containing compound to form an oxide layer and diffusion of conductive dopant into the substrate by a thermally treating step (¶0020-0030, 0030-0036). Rana does not teach that the oxygen dopant diffuses into the upper surface of the substrate, but rather forms over the remaining amorphous-silicon containing compound away from the substrate. Therefore the subject matter of claims 15 and 16 are allowable over the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC R. SMITH whose telephone number is (571)270-7186. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Barton can be reached on 571 272 1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERIC R SMITH/
Examiner, Art Unit 1757

Notice of References Cited	Application/Control No. 14/829,999	Applicant(s)/Patent Under Reexamination SCHULTZ-WITTMAN ET AL.	
	Examiner ERIC SMITH	Art Unit 1757	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0235972 A1	09-2009	Fukushima; Naoki	H01L31/0512	136/244
*	B	US-5,131,933 A	07-1992	Flodl; Helmut	H01L31/02168	136/256
*	C	US-4,577,393 A	03-1986	Schmidt; Wilfried	H01L21/2255	136/255
*	D	US-4,694,117 A	09-1987	Friedrich; Gerda	H01L31/02168	136/256
*	E	US-2010/0075485 A1	03-2010	Rana; Virendra V.	H01L21/02532	438/482
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	
Examiner Name	
Attorney Docket Number	3304.001B

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/E.R.S/	1	6194763	B1	2001-02-27	Hisamoto et al.	
/E.R.S/	2	6924179	B2	2005-08-02	Oh et al.	
/E.R.S/	3	7202143	B1	2007-04-10	Naseem et al.	
/E.R.S/	4	6210991	B1	2001-04-03	Wenham et al.	
/E.R.S/	5	5665607	A	1997-09-09	Kawama et al.	
/E.R.S/	6	6821875	B1	2004-11-23	Wenham et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999 - GAU: 1757
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

/E.R.S/	1	20080001169	A1	2008-01-03	Lochtefeld	
/E.R.S/	2	20060213548	A1	2006-09-28	Bachrach et al.	
/E.R.S/	3	20080072959	A1	2008-03-27	Chen et al.	
/E.R.S/	4	20030136440	A1	2003-07-24	Machida et al.	
/E.R.S/	5	20070295399	A1	2007-12-27	Carlson, David E.	
/E.R.S/	6	20080311697	A1	2008-12-18	Reber, Stefan	
/E.R.S/	7	20100105190	A1	2010-04-29	Ferre i Tomas, Rafel	
/E.R.S/	8	20090178711	A1	2009-07-16	Joo et al.	
/E.R.S/	9	20100136768	A1	2010-06-03	Biro et al.	
/E.R.S/	10	20100227431	A1	2010-09-09	Rana, Virendra V.	
/E.R.S/	11	20120055547	A1	2012-03-08	Schultz-Wittmann et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2015-08-19
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	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/E.R.S/	1	JP2003-298078	JP	A	2003-10-17	EBARA Corp.	English Abstract Only	☒
/E.R.S/	2	JP2006-128630	JP	A	2006-05-18	Sanyo Electric Co., Ltd.	English Abstract Only	☒
/E.R.S/	3	WO2007/125903	WO	A1	2007-11-08	Fukushima et al.	English Abstract Only	☒
/E.R.S/	4	WO2008/028625	WO	A2	2008-03-13	Biro et al.	English Abstract Only	☒
/E.R.S/	5	WO2008115814	WO	A2	2008-09-25	Carlson et al.	English Document	☒

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/E.R.S/	1	SCHULTZ, O. et al., "Deielctric Rear Surface Passivation for Industrial Multicrystalline Silicon Solar Cells", 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, Vol. 1, May 7-12, 2006 (pages 885-889).	☐
/E.R.S/	2	DeWOLF, S. et al., "Surface Passivation Properties of Boron-Doped Plasma-Enhanced Chemical Vapor Deposited Hydrogenated Amorphous Silicon Films on P-Type Crystalline Si Substrates", Applied Physics Letters, Vol. 88, Issue 2, January 2006 (1 page; Abstract Only).	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999 ~ GAU: 1757
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

/E.R.S/	3	TUCCI, M. et al., "Laser Fired Back Contact for Silicon Solar Cells", Thin Solid Films, Vol. 516, Issue 20, Auugst 30, 2008 (1 page; Abstract Only).	☐
/E.R.S/	4	BAU et al, "Application of PECVD-SiC as Intermediate Layer in Crystalline Silicon Thin-Film Solar Cells", 3rd World Conference on Photovoltaic Energy Conversion (2003).	☐
/E.R.S/	5	SCHULTZ-WITTMANN et al., International Search Report for PCT/US2010/031869, dated August 18, 2010 (4 pages).	☐
/E.R.S/	6	SCHUTLZ-WITTMANN et al., Patent Examination Report No. 1, for Australian Patent Application No. AU2010-239265, dated August 19, 2013 (4 pages).	☐
/E.R.S/	7	SCHULTZ-WITTMANN et al., Examination Report No. 2 for Australian Application No. AU2010-239265, dated January 22, 2014 (3 pages).	☐
/E.R.S/	8	SCHULTZ-WITTMANN et al., Patent Examination Report No. 3 for Australian Patent Application No. AU2010-239265, dated March 6, 2014 (3 pages).	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999 ~ GAU: 1757
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3304.001B

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2015-08-19
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	2812
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/E.R.S/	1	4481046		1984-09-29	Bouldin et al.	
/E.R.S/	2	6649956	B2	2003-11-18	Yoshida et al.	

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/E.R.S/	1	20080251119	A1	2007-04-13	Forehand et al.	
/E.R.S/	2	20090014056	A1	2007-07-09	Hockaday et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/E.R.S/	1	JP-SHO-57-071188	JP	A	1982-01-05	Mitsubishi Electric Corp.	English Abstract Only	X

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14829999
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	2812
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

/E.R.S/	2	JP-H06-111877	JP	A	1994-04-22	Toshiba Lighting & Technology Corp.	English Abstract Only	☒

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Examiner Signature	/ERIC R SMITH/	Date Considered	04/04/2016

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5787	h01l31/186-1872.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	AND	ON	2016/04/06 10:11
L2	4982	h01l31/186-1872.cpc.	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 10:11
L3	136	l2 and (oxygen with dop$3)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 10:11
L4	144	l2 and ((oxygen or "o.sub.2") with dop$3)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 10:12
L5	575	l2 and ((oxygen or "o.sub.2" or oxide) with dop$3)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 10:12
L33	2606	h01l21/02667,02694.cpc.	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 16:20
L34	115	l33 and ((amorphous or "a-si") and ((oxygen or "o.sub.2") with (dop$3 or diffus$4)))	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 16:21
L35	115	l34 and (thermal or anneal$3 or temperature or heat)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 16:22
L36	115	l34 and (thermal or anneal$3 or temperature or heat$3)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/06 16:22
S367	663	h01l31/02168.cpc.	DERWENT	AND	ON	2016/04/05 10:44
S368	53	S367 and (dop$3 with (passivat$3 or antireflect$3 or anti adj reflect$3))	DERWENT	AND	ON	2016/04/05 10:45
S369	4619	h01l31/02168.cpc.	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/05 10:46
S370	454	S369 and (dop$3 with (passivat$3 or antireflect$3 or anti adj reflect$3))	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/04/05 10:46

4/6/2016 5:20:02 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	Art Unit
	ERIC R SMITH	1757

CPC- SEARCHED		
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CPC COMBINATION SETS - SEARCHED		
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US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
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SEARCH NOTES		
Search Notes	Date	Examiner
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "oxygen diffusion")	4/6/2016	ERS
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "codiffusion")	4/6/2016	ERS
Keyword search in H01L31/186-1872, 02168 (see EAST history for search strategy)	4/6/2016	ERS
Keyword search in H01L21/02667,02694	4/6/2016	ERS

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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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CONFIRMATION NO. 1023

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/829,999	08/19/2015 RULE	136	1757	3304.001B

APPLICANTS

TETRASUN, INC., San Jose, CA;

INVENTORS

Oliver SCHULTZ-WITTMANN, Sunnyvale, CA;
Denis DeCEUSTER, Woodside, CA;

**** CONTINUING DATA ***********************

This application is a DIV of 13/265,462 11/15/2011 PAT 9130074 *
which is a 371 of PCT/US2010/031869 04/21/2010
which claims benefit of 61/171,194 04/21/2009
(*)Data provided by applicant is not consistent with PTO records.

**** FOREIGN APPLICATIONS ***********************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

09/01/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ERIC R SMITH/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	12	20	2

ADDRESS

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203
UNITED STATES

TITLE

HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Oliver SCHULTZ-WITTMANN, et al. Confirmation No.: 1023

Serial No.: 14/829,999 Group Art Unit: 1757

Filed: August 19, 2015 Examiner: Eric R. Smith

Title: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Response to Office Action

Dear Commissioner:

This paper is filed responsive to the Office Action mailed April 13, 2016, in connection with the above-designated U.S. patent application. Allowance of the application is respectfully requested in view of the Amendments and Remarks below.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 4 of this paper.

Mundra Solar PV Ltd., Ex. 1002
Page 263

Amendments to the Claims

Kindly amend claims 8 & 16, and cancel claims 1-7, 15, 19 & 20 (without prejudice), as set forth below. All pending claims are reproduced below, with changes in the amended claims shown by underlining for added matter, and strikethrough or double brackets for deleted matter.

1-7. (Canceled).

8. (Currently Amended) A method of fabricating a solar cell, comprising:

providing a substrate;

providing an interface passivation layer over the substrate;

providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant;

thermally treating the passivating film, the thermally treating diffusing at least a portion of the conductive dopant from the passivating film throughout the interface passivation layer to facilitate electrical connection to the substrate; [[and]]

providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate[[.]]; and

wherein providing the interface passivation layer and providing the passivating film comprise:

providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;

diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.

9. (Original) The method of claim 8, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

10. (Original) The method of claim 9, wherein the crystallized passivating film is a transparent film.

11. (Original) The method of claim 9, wherein the crystallization of the passivating film improves a passivation of the passivating film.

12. (Original) The method of claim 9, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.

13. (Original) The method of claim 8, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.

14. (Original) The method of claim 8, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.

15. (Canceled).

16. (Currently Amended) The method of claim 8 [[15]], wherein the diffusing of the oxygen comprises thermally treating the amorphous silicon-containing compound, the thermally treating diffusing the conductive dopant from the passivating film throughout the interface passivation layer.

17. (Original) The method of claim 8, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.

18. (Original) The method of claim 8, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

19-20. (Canceled).

* * * * *

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Remarks

Favorable consideration and allowance of the application are respectfully requested. Claims 8-14 & 16-18 remain pending.

Applicant thanks the Examiner for the indication of allowability of claims 15 & 16 if rewritten in independent form including all the limitations of the base claim and any intervening claims. Pursuant to this indication, claim 15 is rewritten into independent claim 8, and as such, claim 8, as well as dependent claims 9-14 & 16-18 are believed to be in condition for allowance.

To facilitate the issuance of the allowable subject matter, withdrawn claims 1-7 are canceled herein without prejudice to the refiling thereof in a divisional application, and rejected claims 19 & 20 are also canceled without prejudice. Based on the amendments submitted herewith, the 35 U.S.C. §112 and 35 U.S.C. §103 rejections noted in the Office Action are believed moot.

All pending claims are believed to be in condition for allowance, and such actions are respectfully requested.

In this amendment, Applicant has amended claims 8 & 16, and cancelled claims 1-7, 15, 19 & 20 (without prejudice) to facilitate expeditious prosecution of the application. Applicant is not conceding that the subject matter encompassed by the claims prior to this amendment is unpatentable over the art cited in the Office Action. Rather, Applicant respectfully reserves the right to pursue claims in one or more continuing applications, including claims capturing the subject matter encompassed by the claims prior to this amendment, and additional claims.

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Should any issue remain unresolved by this paper, Applicant's undersigned attorney invites the Examiner to telephone him at the time that the Examiner is considering this Response, in order to discuss the matter in the hope of facilitating prosecution of this application.

Respectfully submitted,

/Kevin P. Radigan, Esq./

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PTO/SB/08a (01-10)
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(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	2812
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

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	Attorney Docket Number	3304.001B

	1	SCHULTZ-WITTMANN et al., Search Report for EP Application No. 10767689.2, dated April 14, 2016 (7 pages).	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	2812
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2016-07-13
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 643 564 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
05.04.2006 Bulletin 2006/14

(51) Int Cl.:
H01L 31/068 *(2006.01)*

(21) Application number: **05021035.0**

(22) Date of filing: **27.09.2005**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **29.09.2004 JP 2004284569**

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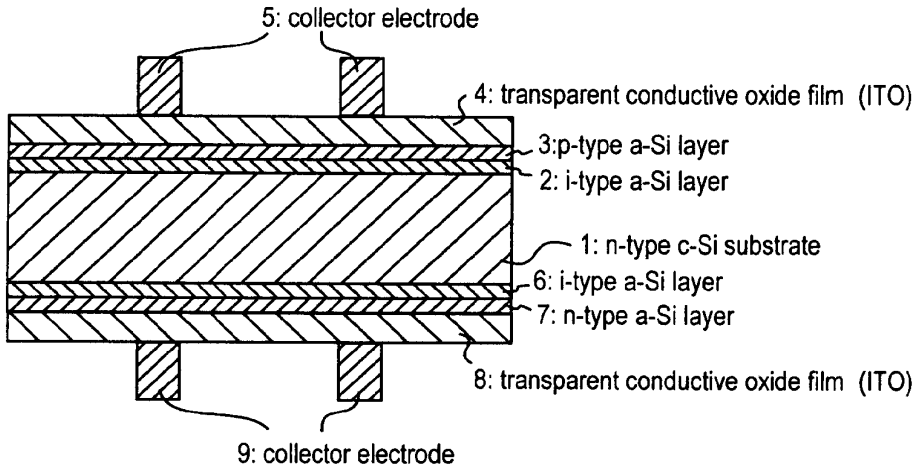
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(54) Photovoltaic device

(57) In the photovoltaic devices comprising a substantially intrinsic amorphous silicon layer containing hydrogen (2) between an n-type single-crystal silicon substrate (1) and a p-type amorphous silicon layer containing hydrogen (3), the photovoltaic device according to the present invention comprises a trap layer (33) that contains less hydrogen than the intrinsic amorphous silicon layer (2) between the p-type amorphous silicon layer (3) and the intrinsic amorphous silicon layer (2). The trap layer (33) reduces hydrogen diffusion from the intrinsic amorphous silicon layer (2) to the p-type amorphous silicon layer (3).

Fig.1



EP 1 643 564 A2

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The priority application Number JP2004-284569 upon which this patent application is based is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a photovoltaic device having semiconductor heterojunctions.

[0003] Recently, considerable research has been done on solar cells, or photovoltaic devices, using crystalline semiconductors such as single-crystal silicon and multicrystalline silicon, and many photovoltaic devices have been put in practical use. In particular, solar cells having semiconductor heterojunctions formed by combining amorphous silicon and crystalline silicon receive attention for the junction that can be formed through a low-temperature process, at 200 degrees centigrade or lower, by a plasma CVD method and others, and for their high conversion efficiency. In order to further improve the photoelectric conversion efficiency, the photovoltaic device needs to improve fill factor (F.F.) as maintaining short-circuit current (Isc) and open-circuit voltage (Voc) high.

[0004] There have been developed solar cells having the so-called H.I.T. (Heterojunction with Intrinsic Thin-layer) structure in which a substantially intrinsic amorphous silicon layer (i-type amorphous silicon layer) containing hydrogen is interposed between an n-type single-crystal silicon substrate and a p-type amorphous silicon layer containing hydrogen. Some proposed solar cell devices having the H.I.T. structure include an i-type amorphous silicon layer with an optical band gap expanded on a side in contact with the p-type amorphous silicon layer in order to reduce the recombination of photo-generated carries and improve the photoelectric conversion efficiency (e.g. Japanese unexamined patent publication No. 2002-76409, U.S. patent application No. 09/947,317).

[0005] In a solar cell device having the H.I.T. structure, the p-type amorphous silicon layer disposed on a light incident side has an optimal composition of hydrogen concentration and p-type impurity dopant, such as boron (B), in consideration of conductivity and light-transmissivity. The i-type amorphous silicon layer also has an optimal composition of hydrogen concentration and others for the purpose of improvement of interfacial quality. In the conventional H.I.T. solar cell having the merely optimized p-type amorphous silicon layer and i-type amorphous silicon layer, the hydrogen concentration of the i-type amorphous silicon layer is higher than that of the p-type amorphous silicon layer.

[0006] By the way, any solar cells having amorphous silicon layers formed by a plasma CVD method deteriorate their output characteristics by a long application of heat at high temperatures of 200 degrees centigrade or more. For this reason, the formation of electrodes and lamination coating after the amorphous silicon layer is formed are performed while controlling temperature so as not to exceed the temperature in the CVD process.

SUMMARY OF THE INVENTION

[0007] The possible causes of the deterioration in output characteristics by heating at high temperatures are: (1) diffusion of electrode materials into doped amorphous semiconductor thin films containing hydrogen; (2) diffusion of the dopant into substantially intrinsic amorphous semiconductor thin-film layers; (3) diffusion of hydrogen; and others. Among these causes, the cause (3) affects the output characteristics the most at low temperatures.

[0008] Especially, the diffusion of hydrogen from an i-type amorphous silicon layer to a p-type amorphous silicon layer reduces activation rate of boron (B), which is a dopant, thereby decreasing a built-in electric field. As a result, the output characteristics of the solar cell are deteriorated, which is a problem.

[0009] The present invention was made in view of the above problem, and has an object to reduce the deterioration of the output characteristics of the solar cells suffered during the heating processes after the amorphous semiconductor thin-film layer is formed by the plasma CVD method.

[0010] A photovoltaic device according to the present invention includes a crystalline semiconductor substrate, a substantially intrinsic amorphous semiconductor thin-film layer containing hydrogen and provided on the crystalline semiconductor substrate, a doped amorphous semiconductor thin-film layer containing hydrogen and provided on the intrinsic amorphous semiconductor thin-film layer, and a hydrogen-diffusion reducing area provided between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer and reducing hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer.

[0011] As described above, the present invention can reduce the hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer by the use of the hydrogen-diffusion reducing area. Consequently, the deterioration in the output characteristics of the solar cell suffered during the heating processes after the formation of the amorphous semiconductor thin-film layer can be reduced.

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[0012] The hydrogen-diffusion reducing area is an area formed in the vicinity of an interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer, and containing higher concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does.

[0013] As described above, the hydrogen-diffusion reducing area can be formed by containing more hydrogen than the intrinsic amorphous semiconductor thin-film layer does. The area with the high concentrations of hydrogen can reduce the hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer.

[0014] In addition, the hydrogen-diffusion reducing area is an area formed in the vicinity of the interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer, containing higher concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does, and doped with the same type of impurity as that for the doped amorphous semiconductor thin-film layer.

[0015] As described above, the hydrogen-diffusion reducing area can be formed by containing more hydrogen than the intrinsic amorphous semiconductor thin-film layer does and doping the same type of impurity as that for the doped amorphous semiconductor thin-film layer. The area can reduce the hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer.

[0016] Furthermore, the hydrogen-diffusion reducing area is a trap layer formed in the vicinity of the interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer and containing lower concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does.

[0017] As described above, the hydrogen-diffusion reducing area can be formed by providing the trap layer containing less hydrogen than the intrinsic amorphous semiconductor thin-film layer does. The trap layer can reduce the hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer.

[0018] The trap layer may be a substantially intrinsic amorphous semiconductor thin-film layer.

[0019] The trap layer may be doped with the same type of impurity as that for the doped amorphous semiconductor thin-film layer.

[0020] A photovoltaic device according to the present invention is characterized by including an n-type single-crystal silicon substrate, a substantially intrinsic amorphous silicon layer containing hydrogen and provided on the single-crystal silicon substrate, a p-type amorphous silicon layer containing hydrogen and provided on the intrinsic amorphous silicon layer, and a hydrogen-diffusion reducing area provided between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and reducing hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer.

[0021] As described above, the present invention can reduce the hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer by the use of the hydrogen-diffusion reducing area. Consequently, the deterioration in the output characteristics of the solar cell suffered during the heating processes after the formation of the amorphous semiconductor thin-film layer can be reduced.

[0022] The hydrogen-diffusion reducing area is an area formed in the vicinity of an interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and containing higher concentrations of hydrogen than the intrinsic amorphous silicon layer does.

[0023] As described above, the hydrogen-diffusion reducing area can be formed by containing more hydrogen than the intrinsic amorphous silicon layer does.
The area with the high concentrations of hydrogen can reduce hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer.

[0024] In addition, the hydrogen-diffusion reducing area is an area formed in the vicinity of the interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer, containing higher concentrations of hydrogen than the intrinsic amorphous silicon layer does, and doped with a p-type impurity.

[0025] As described above, the hydrogen-diffusion reducing area can be formed by containing more hydrogen than the intrinsic amorphous silicon layer does and doping the p-type impurity. The area can reduce hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer.

[0026] Furthermore, the hydrogen-diffusion reducing area is a trap layer formed in the vicinity of the interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and containing lower concentrations of hydrogen than the intrinsic amorphous silicon layer does.

[0027] As described above, the hydrogen-diffusion reducing area can be formed by providing the trap layer containing less hydrogen than the intrinsic amorphous silicon layer does. The trap layer can reduce hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer.

[0028] The trap layer may be a substantially intrinsic amorphous silicon layer. In this case, the thickness of the trap layer should be from 1 nm to 5 nm, more preferably 1 nm to 2 nm.

[0029] The trap layer may be an amorphous silicon layer doped with the p-type impurity. In this case, the thickness of the trap layer should be 0.1 nm or more but less than 3 nm, more preferably 0.3 nm to 2 nm.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. 1 is a schematic cross-sectional view showing a photovoltaic device with a H.I.T. structure to which the present invention is applied.

[0031] FIG. 2 is a schematic view showing a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a conventional solar cell with the H.I.T. structure.

[0032] FIG. 3 is a schematic view showing a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell with the H.I.T. structure according to the first embodiment of the present invention.

[0033] FIG. 4 shows a profile of hydrogen concentration, measured by a SIMS, at the interface between a p-type amorphous silicon layer and the i-type amorphous silicon layer of the solar cell with the H.I.T. structure according to the first embodiment.

[0034] FIG. 5 is a schematic view showing a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layers and an i-type amorphous silicon layer of a solar cell with the H.I.T. structure according to the second embodiment of the present invention.

[0035] FIG. 6 shows a profile of hydrogen concentration, measured by the SIMS, at the interface between the p-type amorphous silicon layers and the i-type amorphous silicon layer of the solar cell with the H.I.T. structure according to the second embodiment.

[0036] FIG. 7 is a schematic view showing a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell with the H.I.T. structure according to the third embodiment of the present invention.

[0037] FIG. 8 shows a profile of hydrogen concentration, measured by the SIMS, at the interface between the p-type amorphous silicon layer and the i-type amorphous silicon layer of the solar cell with the H.I.T. structure according to the third embodiment.

[0038] FIG. 9 is a schematic view showing a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell with the H.I.T. structure according to the fourth embodiment of the present invention.

[0039] FIG. 10 shows a profile of hydrogen concentration, measured by the SIMS, at the interface between the p-type amorphous silicon layer and the i-type amorphous silicon layer of the solar cell with the H.I.T. structure according to the fourth embodiment.

[0040] FIG. 11 is a characteristic diagram showing the relationship between film thicknesses and initial characteristics of a trap layer according to the third embodiment of the present invention.

[0041] FIG. 12 is a characteristic diagram showing the relationship between relative outputs and film thicknesses of the trap layer according to the third embodiment of the present invention. The relative outputs, which are expressed as rate of change, are obtained from post-annealing characteristics and the initial characteristics.

[0042] FIG. 13 is a characteristic diagram showing the relationship between the post-annealing characteristics and the thicknesses of the trap layer according to the third embodiment of the present invention.

[0043] FIG. 14 is a characteristic diagram showing the relationship between film thicknesses and initial characteristics of a trap layer according to the fourth embodiment of the present invention.

[0044] FIG. 15 is a characteristic diagram showing the relationship between relative outputs and film thicknesses of the trap layer according to the fourth embodiment of the present invention. The relative outputs, which are expressed as rate of change, are obtained from post-annealing characteristics and the initial characteristics.

[0045] FIG. 16 is a characteristic diagram showing the relationship between the post-annealing characteristics and the thicknesses of the trap layer according to the fourth embodiment of the present invention.

[0046] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when reviewed in conjunction with the accompanying drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0047] Descriptions will be made on embodiments according to the present invention with reference to drawings. Firstly, a photovoltaic device with the H.I.T. structure to which the present invention is applied will be described with reference to FIG. 1. FIG. 1 is a schematic cross-sectional view of a photovoltaic device with the H.I.T. structure to which the present invention is applied.

[0048] This photoelectric conversion device, as shown in FIG. 1, includes a crystalline semiconductor substrate, or an n-type single-crystal silicon (C-Si) substrate 1 (hereinafter referred to as n-type single-crystal silicon substrate 1) that has resistivity of approximately 1 Ω·cm, a thickness of approximately 300 μm, and (100) faces. On a surface of the n-type single-crystal silicon substrate 1, formed are pyramidal projections and depressions having a few micro meters

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to a few tens of micro meters in height in order to confine light. As a substantially intrinsic amorphous semiconductor thin-film layer containing hydrogen, a substantially intrinsic i-type amorphous silicon (a-Si:H) layer 2 having a thickness of 3 nm to 250 nm is formed on the n-type single-crystal silicon substrate 1 by an RF plasma CVD method. On the i-type amorphous silicon layer 2 formed is a p-type amorphous silicon layer 3 having a thickness of approximately 5 nm as a doped amorphous semiconductor thin-film layer containing hydrogen.

[0049] In this embodiment, an ITO (Indium Tin Oxide) film 4, as a transparent conductive oxide film having a thickness of approximately 100 nm, is formed on the p-type amorphous silicon layer 3 by a magnetron sputtering method. The ITO film 4 is made of In_2O_3 (indium oxides) with the addition of SnO_2 (tin oxides).

[0050] Comb-shaped collector electrodes 5, which are silver paste electrodes, are formed at predetermined regions on an upper surface of the ITO film 4.

[0051] In addition, a substantially intrinsic i-type amorphous silicon layer 6 having a thickness of approximately 5 nm is formed on a lower surface of the n-type single-crystal silicon substrate 1. On the i-type amorphous silicon layer 6 formed is an n-type amorphous silicon layer 7 having a thickness of approximately 20 nm. By thus forming the i-type amorphous silicon layer 6 and the n-type amorphous silicon layer 7 on the lower surface of the n-type single-crystal silicon substrate 1 in sequence, the so-called BSF (Back Surface Field) structure is formed. Furthermore, in this embodiment, an ITO film 8 is formed on the n-type amorphous silicon layer 7 by a magnetron sputtering method, as a transparent conductive oxide film having a thickness of approximately 100 nm. The ITO film 8 is made of In_2O_3 with the addition of SnO_2

[0052] Comb-shaped collector electrodes 9, which are silver paste electrodes, are formed at predetermined regions on an upper surface of the ITO film 8.

[0053] An example of manufacturing the aforementioned photovoltaic device will be described below. A cleaned n-type single-crystal silicon substrate 1 is installed in a vacuum chamber which heats up the substrate 1 at appropriate temperatures (200 degrees centigrade or lower) to remove water adhered on the surface of the substrate as much as possible. Hydrogen gas is then supplied and plasma is discharged to clean the surface of the substrate.

[0054] A non-doped i-type amorphous silicon layer 2 is formed by supplying silane (SiH_4) gas and hydrogen gas. Subsequently, a p-type amorphous silicon layer 3 is formed by supplying SiH_4 gas, hydrogen gas and diborane (B_2H_6) gas functioning as a doping gas, resulting in completion of a p-n junction. In addition, an indium tin oxide layer functioning as a surface electrode 4 is formed by a sputtering method. Silver electrodes functioning as collector electrodes 5 are formed by a screen printing method. The collector electrodes 5 are completed by burning the silver electrodes.

[0055] The BSF structure may be formed by providing the non-doped i-type amorphous silicon layer 6, the n-type amorphous silicon layer 7, and the rear surface electrode layers 8 and 9 on the other surface of the substrate 1. These layers can be formed from either the rear surface side (n-type side) or the front surface side (p-type side) of the substrate.

[0056] Alternatively, a p-type substrate is also available. As in the case of the n-type substrate, a non-doped amorphous silicon layer, an n-type amorphous silicon layer, an indium tin oxide layer, and silver collector electrodes are formed on a front surface of the substrate, whereas a non-doped amorphous silicon layer, a p-type amorphous silicon layer and rear surface electrode layers are formed on a rear surface of the substrate in the same manner. Table 1 shows formation conditions of each amorphous silicon layer to form a solar cell working in a photovoltaic device.

[Table 1]

process		conditions			
		Substrate temperature (degrees centigrade)	gas	pressure (Pa)	power density (mW/cm^2)
front	hydrogenation	150 - 180	H_2 : 100 sccm	30-100	3-30
	i-type a-Si	150 - 180	H_2 : 0 - 100 sccm SiH_4 40 sccm	40-120	5-15
	p-type a-Si	150 - 180	H_2:0-100 sccm SiH_4 : 40 sccm 2%B_2H_6/H_2 : 20 sccm	40-120	5-15

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Table continued

process		conditions			
		Substrate temperature (degrees centigrade)	gas	pressure (Pa)	power density (mW/cm^2)
rear	hydrogenation	170	H_2: 100 sccm	50	3-30
	i-type a-Si	170	SiH_4 : 40 sccm	40	8.33
	p-type a-Si	170	H_2: 0 - 100 sccm SiH_4: 40 sccm $1\%PH_3/H_2$: 40 sccm	40	8.33

[0057] As described above, in the conventional solar cell with the H.I.T. structure including an optimized p-type amorphous silicon layer 3 and i-type amorphous silicon layer 2, the i-type amorphous silicon layer 2 contains higher concentrations of hydrogen than the p-type amorphous silicon layer 3 does.

[0058] FIG. 2 schematically shows a profile of hydrogen concentration in the vicinity of an interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2 of the conventional solar cell with the H.I.T. structure. The hydrogen concentration of the i-type amorphous silicon layer 2 is higher than that of the p-type amorphous silicon layer 3. In the vicinity of the interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2, a negative gradient of hydrogen concentration is formed from the i-type amorphous silicon layer (i-layer) 2 toward the p-type amorphous silicon layer (p-layer) 3. Because of this, at the interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2, hydrogen in the films is prone to diffuse from the i-type amorphous silicon layer 2 to the p-type amorphous silicon layer 3 by being heated at high temperatures in the process of burning to form the collector electrodes and the process of lamination coating to modularize the solar cells.

[0059] FIG. 3 schematically shows a profile of hydrogen concentration in the vicinity of the interface between the p-type amorphous silicon layer and the i-type amorphous silicon layer of the solar cell with the H.I.T. structure according to the first embodiment of the present invention. As shown in FIG. 3, contrary to the conventional solar cell, a positive gradient of hydrogen concentration is formed so as to increase the hydrogen concentration from the i-type amorphous silicon layer 2 toward the p-type amorphous silicon layer 3 in the first embodiment of the present invention. In other words, an area where hydrogen diffusion is reduced (hereinafter referred to as "hydrogen-diffusion reducing area") is formed by allowing the p-type amorphous silicon layer 3 to contain higher concentrations of hydrogen than the i-type amorphous silicon layer 2 does. Such a structure prevents hydrogen from diffusing into the p-type amorphous silicon layer 3 at some level.

[0060] In order to form the p-type amorphous silicon layer 3 containing higher concentrations of hydrogen than the i-type amorphous silicon layer 2 does, a method described below may be available.

(1) The temperature of the substrate during the formation of the p-type amorphous silicon layer 3 is set to be lower than that during the formation of the i-type amorphous silicon layer 2.
(2) The amount of hydrogen dilution during the formation of the p-type amorphous silicon layer 3 is set to be higher than that during the formation of the i-type amorphous silicon layer 2.
(3) The pressure for forming films during the formation of the p-type amorphous silicon layer 3 is set to be higher than that during the formation of the i-type amorphous silicon layer 2.
(4) The RF power applied during the formation of the p-type amorphous silicon layer 3 is set to be higher than that applied during the formation of the i-type amorphous silicon layer 2.

[0061] A solar cell according to the first embodiment was prepared with the p-type amorphous silicon layer 3 formed with more hydrogen dilution than that for the i-type amorphous silicon layer. Table 2 shows specific conditions to form the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2 on the front surface of the substrate. Layers on the rear surface of the substrate are formed under conditions shown in Table 1. In addition, the i-type amorphous silicon layer 2 and the p-type amorphous silicon layer 3 were formed so as to have thicknesses of 10 nm and 5 nm, respectively.

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[Table 2]

process		conditions			
		Substrate temperature (degrees centigrade)	gas	pressure (Pa)	power density (mW/cm^2)
front	hydrogenation	170	H_2: 100 sccm	50	15
	i-type a-Si	170	H_2: 100 sccm SiH_4 : 40 sccm	50	15
	p-type a-Si	170	H_2: 400 sccm SiH_4 : 40 sccm 2%B_2H_6/H_2:20 sccm	50	15

[0062] In compliance with Table 2, the p-type amorphous silicon layer 3 was formed with more hydrogen dilution than that used to form the i-type amorphous silicon layer in order to form a solar cell of the first embodiment. The solar cell of the first embodiment according to the present invention and a conventional solar cell were prepared. FIG. 4 shows profiles of hydrogen concentrations in films measured by a Secondary Ionization Mass Spectrometer (SIMS). The conventional solar cell was manufactured under the same conditions as those of the first embodiment except for that the p-type amorphous silicon layer and the i-type amorphous silicon layer were formed with same amounts of hydrogen dilution. FIG. 4 shows profiles of hydrogen concentration, measured by the SIMS, at an interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2 of the solar cell with the H.I.T. structure according to the first embodiment.

[0063] Descriptions will be made on the SIMS in use and the measurement conditions of hydrogen (H). In the measurement, cesium positive ions (Cs^+) were irradiated at the samples to sputter off hydrogen negative ions (H^-) and silicon negative ions (Si-). The number of secondary ions of each of the negative ions was counted. The hydrogen concentration was quantified by [H-]/[Si-]. However, the silicon concentration was $5.0 \times 10^{22}/cm^3$. The measuring device in use was ADEPT 1010 by ULVAC-PHI, Inc in Japan. Ion beam energy was 1 keV.

[0064] The profile of the hydrogen concentration measured by the SIMS shown in FIG. 4 indicates the same profile of the hydrogen concentration as those shown in the schematic views in FIG. 2 and FIG. 3. Specifically, the solar cell of the first embodiment has a positive gradient of hydrogen concentration from the i-type amorphous silicon layer 2 toward the p-type amorphous silicon layer 3. It is apparent that the p-type amorphous silicon layer 3 contains more hydrogen than the i-type amorphous silicon layer 2 does.

[0065] Since the p-type amorphous silicon layer 3 functioning as a window layer on the light incident side has a high concentration of hydrogen, the first embodiment has, in addition to an effect of preventing hydrogen diffusion, an effect of generating more electric current due to less light absorption loss at the p-type amorphous silicon layer 3.

[0066] Next description will be made on the second embodiment of the present invention with reference to FIGs. 5 and 6. FIG. 5 schematically shows a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell having the H.I.T. structure according to the second embodiment of the present invention.

[0067] As shown in FIG. 5, the p-type amorphous silicon layer 3 of the second embodiment has a different composition. While the hydrogen concentration is set to be high throughout the entire p-type amorphous silicon layer 3 in the first embodiment, only a front half 31, which is closer to the i-type amorphous silicon layer 2, of the p-type amorphous silicon layer 3 in the second embodiment contains hydrogen in high concentrations. The hydrogen concentration of a rear half 32 is set to the same hydrogen concentration as that of the conventional device.

[0068] The structure of the second embodiment will be more effective when the front half of the p-type amorphous silicon layer 31 is doped with boron (B) in relatively small concentrations (< 1.0 at.%) and the rear half 32 is doped with boron (B) in relatively large concentrations (>2.0 at.%). The structure of the second embodiment, similar to the first embodiment, can reduce hydrogen diffusion from the i-type amorphous silicon layer to the p-type amorphous silicon layer, but hydrogen still diffuses from the front half of the p-type amorphous silicon layer 31 to the rear half of the amorphous silicon layer 32. However, since the rear half of the amorphous silicon layer 32 contains high concentrations of boron (B), even if boron partially becomes inactive by a trace amount of hydrogen diffusion, the device characteristics will not be affected so much.

[0069] Table 3 shows formation conditions of the second embodiment. As appreciated from Table 3, the p-type amorphous silicon layer 31 and the p-type amorphous silicon layer 32 were formed with different flow rates of B_2H_6. More amount of B_2H_6 flow was used for the p-type amorphous silicon layer 32 than that for the p-type amorphous silicon layer 31, while more amount of the hydrogen dilution was used for the p-type amorphous silicon layer 31. Layers on the rear

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surface of the substrate were formed under the conditions shown in Table 1. The i-type amorphous silicon layer 2 was formed to have a thickness of 10 nm, while the p-type amorphous silicon layers 31 and 32 have a thickness of 4 nm each.

[Table 3]

process		conditions			
		Substrate temperature (degrees centigrade)	gas	pressure (Pa)	Power Density (mW/cm^2)
front	hydrogenation	170	H_2 : 100 sccm	50	15
	i-type a-Si	170	H_2 100 sccm SiH_4 : 40 sccm	50	15
	p-type a-Si (31)	170	H_2 : 400 sccm SiH_4 : 20 sccm B_2H_6: 10 sccm	50	15
	p-type a-Si (32)	170	H_2: 100 sccm SiH_4 : 40 sccm $2\%B_2H_6/H_2$:40 sccm	50	15

[0070] After the preparation of the solar cell according to the second embodiment and a conventional solar cell, their profiles of hydrogen concentrations in films were measured by the SIMS. FIG. 6 shows the results. FIG. 6 shows profiles of hydrogen concentrations, measured by the SIMS, at interfaces of p-type amorphous silicon layers 31 and 32 and an i-type amorphous silicon layer 2 of a solar cell with the H.I.T. structure according to the second embodiment. Measurement conditions are the same as those for the first embodiment.

[0071] It is recognized that the profile of the hydrogen concentration measured by the SIMS shown in FIG. 6 is similar to the profiles of the hydrogen concentrations shown in FIG. 2 and FIG. 5. It is therefore found that only front half 31, which is closer to the i-type amorphous silicon layer, of the p-type amorphous silicon layer contains high hydrogen concentration, whereas the rear half 32 is controlled so as to have a gradient of hydrogen concentration equivalent to that of the conventional photovoltaic device.

[0072] Next description will be made on the third embodiment of the present invention with reference to FIGs 7 and 8. FIG. 7 schematically shows a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell with the HIT structure according to the third embodiment of the present invention.

[0073] In the third embodiment, an i-type trap layer 33, which has a thickness of approximately 2 nm and low hydrogen concentrations, is disposed in the vicinity of the interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2. The i-type trap layer 33 functions as a hydrogen-diffusion reducing area. In the third embodiment, hydrogen diffuses from the i-type amorphous silicon layer 2 to the i-type trap layer 33, but has no influence on the p-type amorphous silicon layer.

[0074] The formation conditions of the third embodiment are shown in Table 4. Layers on the rear surface of the substrate were formed under the conditions shown in Table 1. The thickness of the i-type amorphous silicon layer 2 including the i-type trap layer 33 is 10 nm, (i-type trap layer 33 has a thickness of 2 nm alone). The p-type amorphous silicon layer 3 has a thickness of 8 nm.

[Table 4]

process		conditions			
		Substrate temperature (degrees (degrees centigrade)	gas	pressure (Pa) (Pa)	Power density (mW/cm^2)
front	hydrogenation	170	H_2: 100 sccm	50	15
	i-type a-Si	170	H_2: 100 sccm SiH_4 : 40 sccm	50	15

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Table continued

process		conditions			
		Substrate temperature (degrees (degrees centigrade)	gas	pressure (Pa) (Pa)	Power density (mW/cm^2)
	i-type a-Si trap layer (33)	170	SiH_4 : 40 sccm	50	15
	p-type a-Si	170	H_2 100 sccm SiH_4: 40 sccm 2%B_2H_6/H_2: 40 sccm	50	15

[0075] In the third embodiment, no hydrogen dilution was used to form the i-type trap layer 33 in order to make the hydrogen concentration in the i-type trap layer 33 lower than that in the i-type amorphous silicon layer. There are some other ways as indicated below.

[0076] (1) The temperature of the substrate during the formation of the p-type amorphous silicon layer is set to be higher than that during the formation of the i-type amorphous silicon layer.

(2) The amount of hydrogen dilution during the formation of the p-type amorphous silicon layer is set to be lower than that during the formation of the i-type amorphous silicon layer.

(3) The pressure during the formation of the p-type amorphous silicon layer is set to be lower than that during the formation of the i-type amorphous silicon layer.

(4) The RF power applied during the formation of the p-type amorphous silicon layer is set to be lower than that applied during the formation of the i-type amorphous silicon layer.

[0077] FIG. 8 shows profiles of hydrogen concentrations, measured by the SIMS, in films of a solar cell according to the third embodiment and a conventional solar cell. FIG. 8 shows profiles of hydrogen concentration, measured by the SIMS, at interfaces of the p-type amorphous silicon layer 3, the i-type trap layer 33 and the i-type amorphous silicon layer 2 of the solar cell with the H.I.T. structure according to the third embodiment. Measurement conditions are the same as those for the first embodiment.

[0078] It is recognized that the profile of the hydrogen concentration measured by the SIMS shown in FIG. 8 is similar to the profiles of the hydrogen concentrations shown in FIGs. 2 and 7. It is therefore found that the trap layer 33 can capture hydrogen diffused from the i-type amorphous silicon layer 2.

[0079] Next description will be made on the fourth embodiment of the present invention with reference to FIGs 9 and 10. FIG. 9 shows a profile of hydrogen concentration in the vicinity of an interface between a p-type amorphous silicon layer and an i-type amorphous silicon layer of a solar cell with the H.I.T. structure according to the fourth embodiment of the present invention.

[0080] Hydrogen concentration of the i-type amorphous silicon layer 2 in the vicinity of the interface between the p-type amorphous silicon layer 3 and the i-type amorphous silicon layer 2 have an influence on the voltage generated in the H.I.T. solar cell. It has been known that output voltage can be improved by making hydrogen concentration in the rear half (near the p-type amorphous silicon layer) of the i-type amorphous silicon layer 2 high. The solar cell according to the aforementioned third embodiment, which is structured in the opposite manner, reduces hydrogen diffusion toward the p-type amorphous silicon layer 3, but decreases its output voltage to some extent. Thus, in the fourth embodiment, boron (B) is doped into the trap layer 34 having a thickness of approximately 2 nm. This can reduce hydrogen diffusion toward the p-type amorphous silicon layer 3 without reduction of output voltages.

[0081] The formation conditions of the fourth embodiment are shown in Table 5. Layers on the rear surface of the substrate were formed under the conditions shown in Table 1. The thickness of the i-type amorphous silicon layer 2 is 10 nm, while the trap layer 34 has a thickness of 0.5 nm. The p-type amorphous silicon layer 3 is formed to have a thickness of 6 nm.

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[Table 5]

process		conditions			
		Substrate temperature(degrees centigrade)	gas	pressure (Pa)	Power density (mW/cm^2)
front	hydrogenation	170	H_2 100 sccm	50	15
	i-type a-Si	170	H_2: 100 sccm SiH_4 : 40 sccm	50	15
	trap layer (34)	170	SiH_4 : 40 sccm 2%B_2H_6/H_2: 10 sccm	50	15
	p-type a-Si	170	H_2 100 sccm SiH_4 : 40 sccm 2%B_2H_6/H_2:40 sccm	50	15

[0082] After the preparation of a solar cell according to the fourth embodiment and a conventional solar cell, their profiles of hydrogen concentrations in films were measured by the SIMS. FIG. 10 shows the results. FIG. 10 shows the profiles of hydrogen concentrations, measured by the SIMS, at interfaces of the p-type amorphous silicon layers 3, the trap layer 34 and the i-type amorphous silicon layer 2 of the solar cell with the H.I.T. structure according to the fourth embodiment. Measurement conditions are the same as those for the first embodiment.

[0083] It is recognized that the profile of the hydrogen concentration, measured by the SIMS shown in FIG. 10, is similar to the profiles of the hydrogen concentrations shown in FIGs. 2 and 9. It is therefore found that the trap layer 34 can capture hydrogen diffused from the i-type amorphous silicon layer 2.

[0084] Then solar cell device having the H.I.T. structure according to the first to fourth embodiments of the present invention and a conventional solar cell device were prepared and thermal-annealed at 250 degrees centigrade in the atmosphere for three hours. Table 6 shows measurement results of the characteristics changes.

[Table 6]

		Voc (V)	Isc (A/cm^2)	F.F.	Pmax (W)
Conventional technology	Initial characteristics	0.706	3.820	0.772	2.082
	Post-annealing characteristics	0.684	3.811	0.753	1.963
	Rate of change	-3.12%	-0.24%	-2.46%	-5.72%
First embodiment	Initial characteristics	0.709	3.880	0.762	2.096
	Post-annealing characteristics	0.700	3.869	0.752	2.037
	Rate of change	-1.27%	-0.28%	-1.31%	-2.84%
Second embodiment	Initial characteristics	0.707	3.850	0.769	2.090
	Post-annealing characteristics	0.699	3.835	0.758	2.032
	Rate of change	-1.13%	-0.39%	-1.43%	-2.78%
Third embodiment	Initial characteristics	0.698	3.810	0.760	2.020
	Post-annealing characteristics	0.691	3.796	0.751	1.970
	Rate of change	-1.00%	-0.37%	-1.18%	-2.48%
Fourth embodiment	Initial characteristics	0.707	3.790	0.775	2.080
	Post-annealing characteristics	0.701	3.783	0.767	2.034
	Rate of change	-0.85%	-0.18%	-1.03%	-2.21%

[0085] As appreciated from Table 6, it is confirmed that deterioration in output characteristics caused by being heated at high temperatures can be significantly reduced by providing the hydrogen-diffusion reducing area between the p-type amorphous silicon layer and the i-type amorphous silicon layer as in the first to fourth embodiments of the present

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invention. Because of this, the collector electrodes can be made of materials requiring to be burned at high-temperatures, thereby reducing electrode resistance.

[0086] Next, an examination was done on variation in characteristics when the thicknesses of the trap layer 33 and the trap layer 34 were changed. Firstly solar cell devices having i-type trap layers 33, according to the third embodiment, with different thicknesses were prepared as samples. The samples were made under the aforementioned conditions except for that the thicknesses of the i-type trap layers 33 were changed. Then, each sample was thermal-annealed in the atmosphere at 250 degrees centigrade for 3 hours, and examined for its initial characteristics, rate of change, post-annealing characteristics. The results are shown in Table 7 and FIGs. 11 to 13. The characteristics are standardized with respect to the output of the conventional solar cell device without the trap layer 33, that is, the output of the conventional solar device is defined as 1. FIG. 11 is a characteristic diagram showing the relationship between film thicknesses and initial characteristics. FIG. 12 is a characteristic diagram showing the relationship between relative outputs and film thicknesses. The relative outputs, which are expressed as rate of change, are obtained from post-annealing characteristics and the initial characteristics. FIG. 13 is a characteristic diagram showing the relationship between the post-annealing characteristics and the film thicknesses.

[Table 7]

Film thickness (nm)	Initial characteristics	Rate of change	Post-annealing characteristics
0	1	0.93	0.930
0.5	0.99	0.93	0.921
1.0	0.99	0.97	0.960
2.0	0.99	0.97	0.960
3.0	0.98	0.97	0.951
4.0	0.96	0.98	0.941
5.0	0.95	0.98	0.931
6.0	0.93	0.99	0.921
7.0	0.92	0.99	0.911

[0087] From Table 6 and FIGs. 11 to 13, it is found that in the case of providing the i-type trap layer 33, the solar cell devices having the i-type trap layers 33 with thicknesses ranging from 1 nm to 5nm improved their output characteristics after annealing. Thus, the thickness of the i-type trap layer 33 should be 1 nm to 5 nm, more preferably 1 nm to 2 nm. For your information, film-forming time was obtained in advance by calculating from a film with a certain thickness and time elapsed to form the film. The i-type trap layer of each sample was formed based on the film-forming time.

[0088] Next, solar cell devices having trap layers 34 doped with boron (B), according to the fourth embodiment, with different thicknesses were prepared as samples. The samples were made under the aforementioned conditions except for that the thicknesses of the trap layers 34 were changed. Then, each sample was thermal-annealed in the atmosphere at 250 degrees centigrade for 3 hours, and examined for its initial characteristics, rate of change, post-annealing characteristics. The results are shown in Table 8 and FIGs. 14 to 16. The characteristics are standardized with respect to the output of the conventional solar cell device without the trap layer 34, that is, the output of the conventional solar device is defined as 1. FIG. 14 is a characteristic diagram showing the relationship between film thicknesses and initial characteristics. FIG. 15 is a characteristic diagram showing the relationship between relative outputs and film thicknesses. The relative outputs, which are expressed as rate of change, are obtained from post-annealing characteristics and the initial characteristics. FIG. 16 is a characteristic diagram showing the relationship between the post-annealing characteristics and the film thicknesses.

[Table 8]

Film thickness (nm)	Initial characteristics	rate of change	Post-annealing characteristics
0	1	0.93	0.930
0.1	0.995	0.93	0.925
0.3	0.990	0.98	0.970
0.5	0.990	0.98	0.970

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Table continued

Film thickness (nm)	Initial characteristics	rate of change	Post-annealing characteristics
1.0	0.980	0.98	0.960
2.0	0.960	0.98	0.941
3.0	0.940	0.98	0.921
4.0	0.910	0.985	0.896
5.0	0.880	0.99	0.871

[0089] From Table 8 and FIGs. 14 to 16, it is found that in the case of providing the trap layer 34, the solar cell devices having the trap layers 34 with thicknesses of 0.1 nm or more but less than 3 nm improved their output characteristics after annealing. Furthermore, the trap layers 34 with thicknesses ranging from 0.3 nm to 2 nm further improved their output characteristics. Thus, the thickness of the trap layer 34 should be 0.1 nm or more but less than 3 nm, more preferably 0.3 nm to 2 nm. For your information, film-forming time was obtained by calculating from a film with a certain thickness and time elapsed to form the film. The i-type trap layer of each sample was formed based on the film-forming time.

[0090] In the above-mentioned embodiments, although a single-crystal silicon substrate was used as a crystalline semiconductor substrate, multicrystalline semiconductor substrates such as a multicrystalline silicon substrate can obtain same effect. In the above-mentioned embodiments, although an amorphous silicon layer was used as an amorphous semiconductor film containing hydrogen, the present invention is not limited to this. Same effect can be obtained by using amorphous silicon carbide, amorphous silicon germanium, amorphous silicon base alloy, and semiconductor films including minute crystal grains.

[0091] It should be understood that the embodiments disclosed herein are to be taken as examples and not limited. The scope of the present invention is defined not by the above described embodiments but by the following claims. All changes that fall within meets and bounds of the claims, or equivalence of such meets and bounds are intended to embraced by the claims.

Claims

1. A photovoltaic device comprising:

   a crystalline semiconductor substrate;
   a substantially intrinsic amorphous semiconductor thin-film layer containing hydrogen and provided on the crystalline semiconductor substrate;
   a doped amorphous semiconductor thin-film layer containing hydrogen and provided on the intrinsic amorphous semiconductor thin-film layer; and
   a hydrogen-diffusion reducing area provided between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer and reducing hydrogen diffusion from the intrinsic amorphous semiconductor thin-film layer to the doped amorphous semiconductor thin-film layer.

2. The photovoltaic device according to claim 1, wherein the hydrogen-diffusion reducing area is an area formed in the vicinity of an interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer, and containing higher concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does.

3. The photovoltaic device according to claim 1, wherein the hydrogen-diffusion reducing area is an area formed in the vicinity of the interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer, containing higher concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does, and doped with the same type of impurity as that for the doped amorphous semiconductor thin-film layer.

4. The photovoltaic device according to claim 1, wherein the hydrogen-diffusion reducing area is a trap layer formed in the vicinity of the interface between the doped amorphous semiconductor thin-film layer and the intrinsic amorphous semiconductor thin-film layer and containing lower concentrations of hydrogen than the intrinsic amorphous semiconductor thin-film layer does.

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5. The photovoltaic device according to claim 4, wherein the trap layer is a substantially intrinsic amorphous semiconductor thin-film layer.

6. The photovoltaic device according to claim 4, wherein the trap layer is doped with the same type of impurity as that for the doped amorphous semiconductor thin-film layer.

7. A photovoltaic device comprising:

an n-type single-crystal silicon substrate;
a substantially intrinsic amorphous silicon layer containing hydrogen and provided on the single-crystal silicon substrate;
a p-type amorphous silicon layer containing hydrogen and provided on the intrinsic amorphous silicon layer; and
a hydrogen-diffusion reducing area provided between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and reducing hydrogen diffusion from the intrinsic amorphous silicon layer to the p-type amorphous silicon layer.

8. The photovoltaic device according to claim 7, wherein the hydrogen-diffusion reducing area is an area formed in the vicinity of an interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and containing higher concentrations of hydrogen than the intrinsic amorphous silicon layer does.

9. The photovoltaic device according to claim 7, wherein the hydrogen-diffusion reducing area is an area formed in the vicinity of the interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer, containing higher concentrations of hydrogen than the intrinsic amorphous silicon layer does, and doped with a p-type impurity.

10. The photovoltaic device according to claim 7, wherein the hydrogen-diffusion reducing area is a trap layer formed in the vicinity of the interface between the p-type amorphous silicon layer and the intrinsic amorphous silicon layer and containing lower concentrations of hydrogen than the intrinsic amorphous silicon layer does.

11. The photovoltaic device according to claim 10, wherein the trap layer is a substantially intrinsic amorphous silicon layer.

12. The photovoltaic device according to claim 11, wherein the thickness of the trap layer is from 1 nm to 5 nm.

13. The photovoltaic device according to claim 11, wherein the thickness of the trap layer is from 1 nm to 2 nm.

14. The photovoltaic device according to claim 10, wherein the trap layer is an amorphous silicon layer doped with the p-type impurity.

15. The photovoltaic device according to claim 14, wherein the thickness of the trap layer is 0.1 nm or more but less than 3 nm.

16. The photovoltaic device according to claim 14, wherein the thickness of the trap layer is 0.3 nm to 2 nm.

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Fig.1

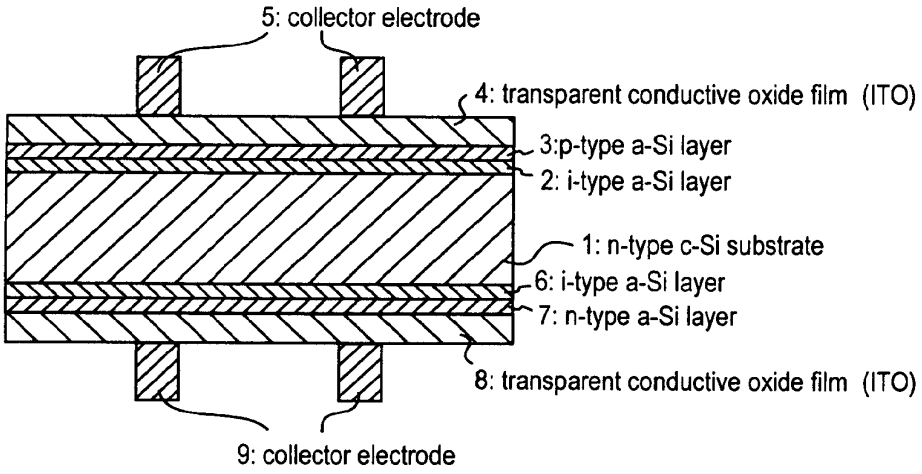
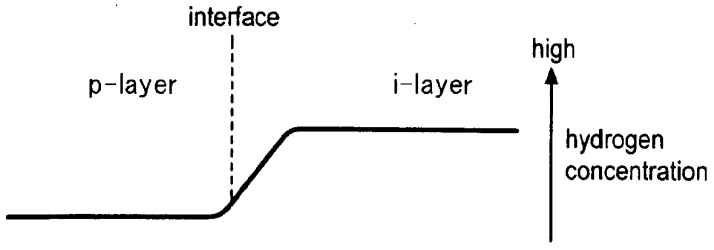


Fig.2



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Fig.3

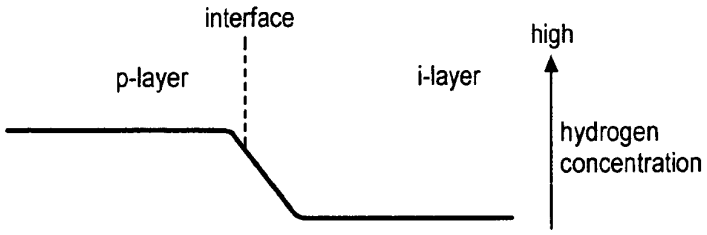
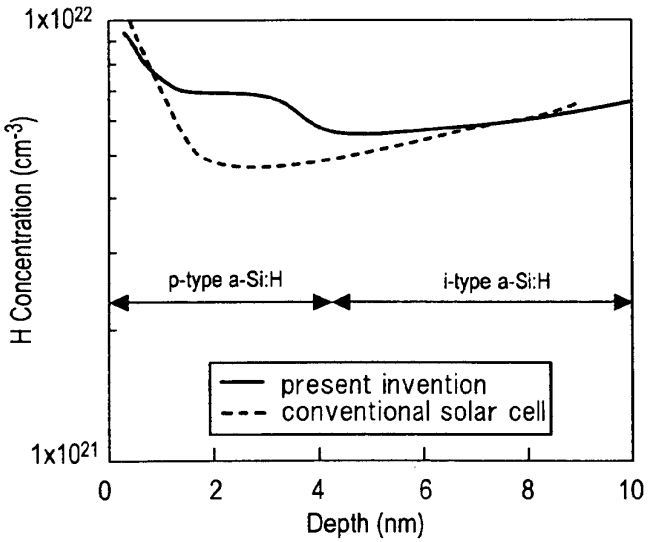


Fig.4



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Fig.5

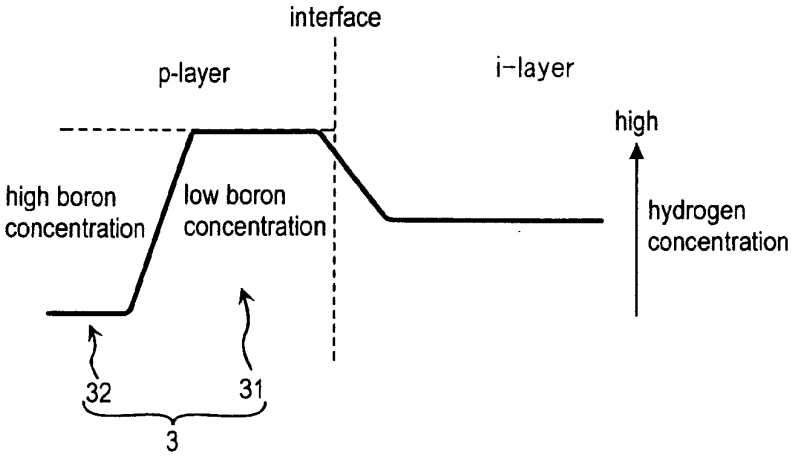
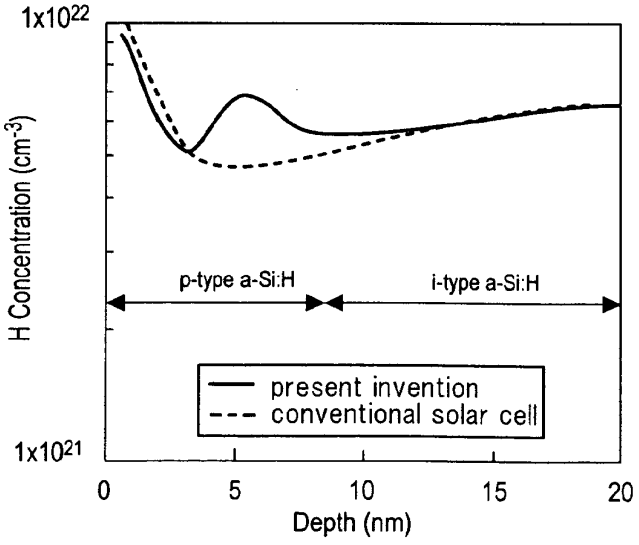


Fig.6



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Page 287

Fig.7

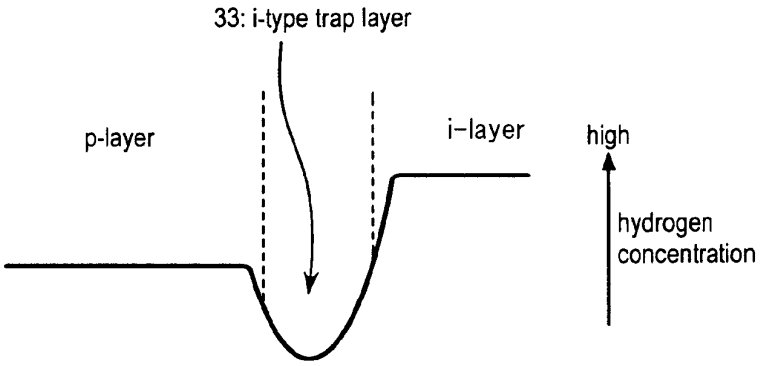
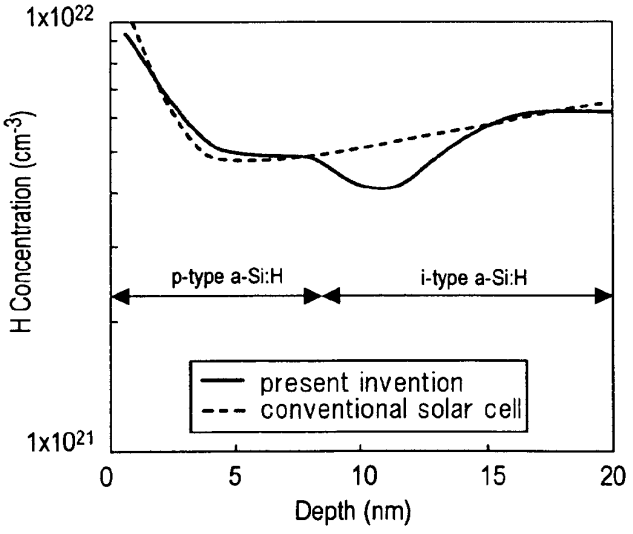


Fig.8



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Fig.9

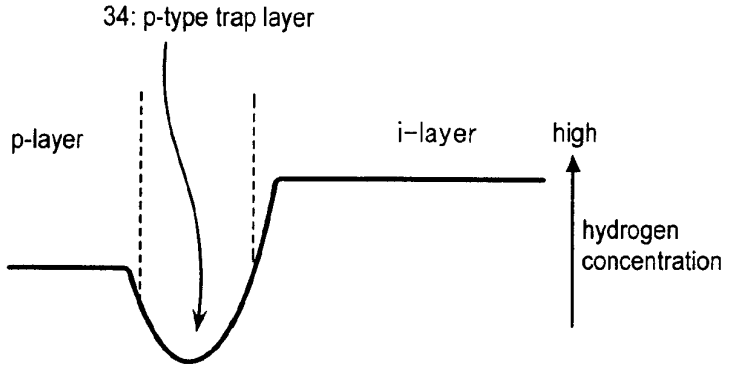
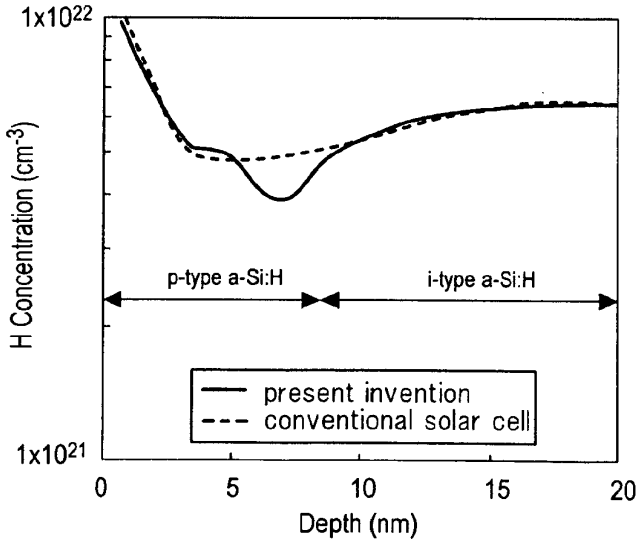


Fig.10



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Fig.11

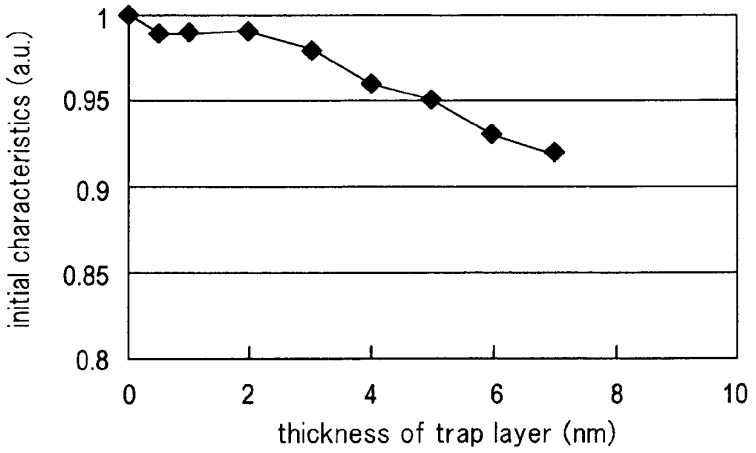
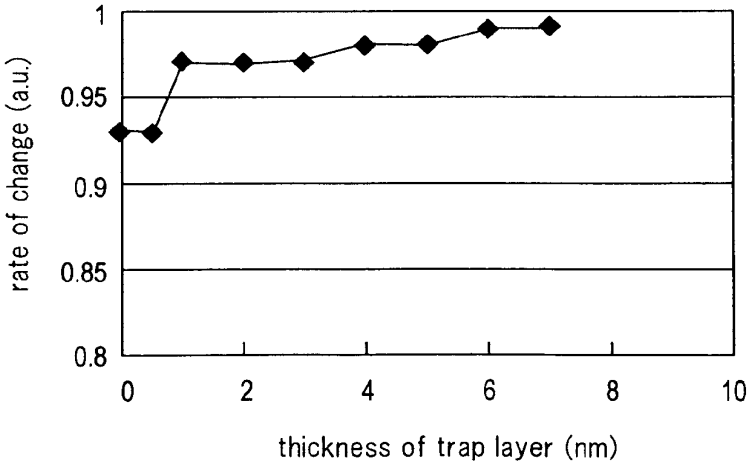


Fig.12



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Fig.13

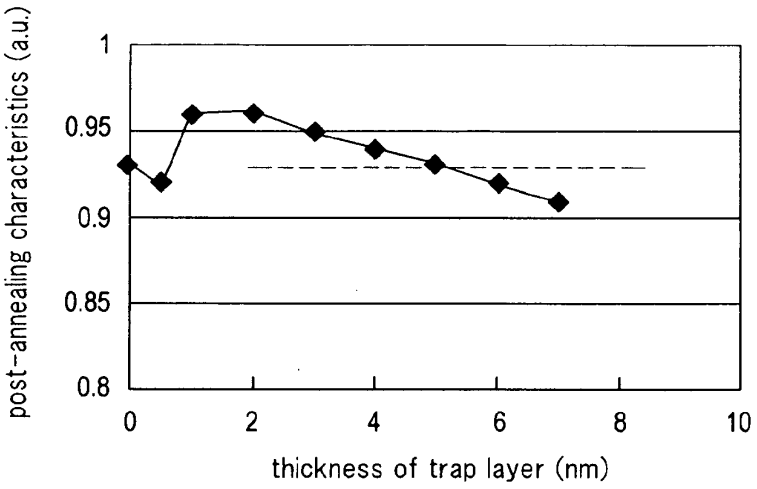
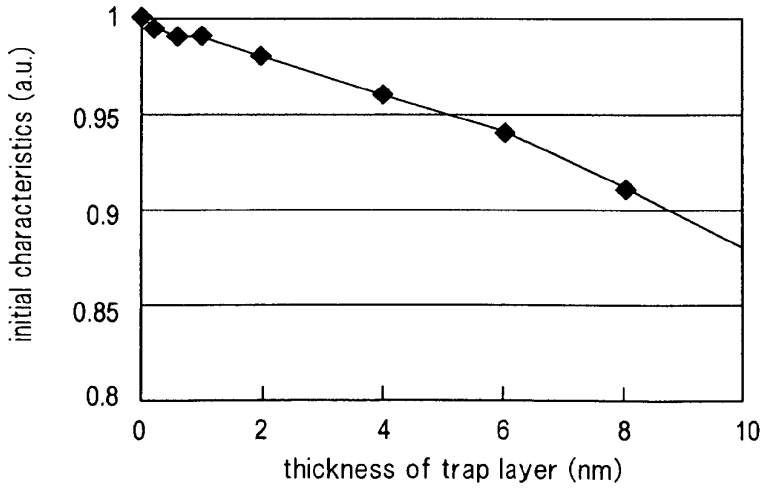


Fig.14



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Fig.15

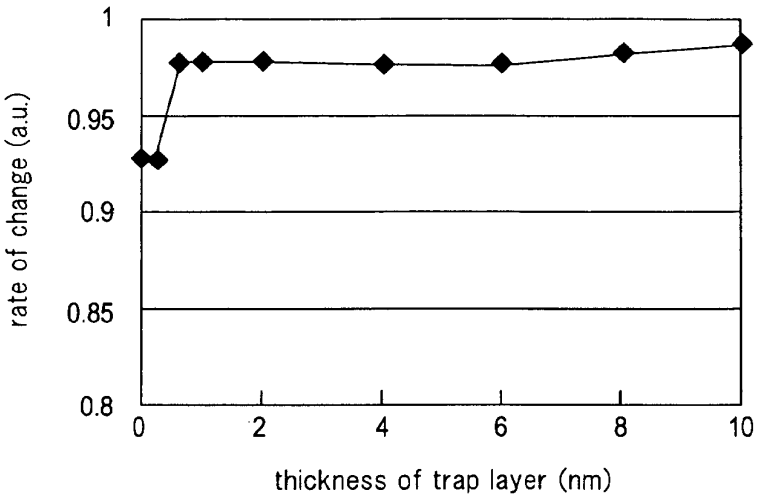
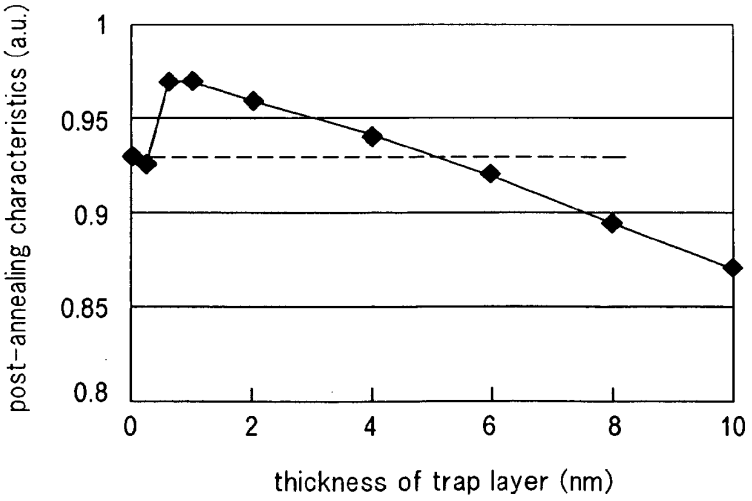


Fig.16



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Electronic Patent Application Fee Transmittal

Application Number:	14829999
Filing Date:	19-Aug-2015
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Filer:	Kevin P. Radigan/Staci Medlock
Attorney Docket Number:	3304.001B

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	26332101
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Staci Medlock
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	13-JUL-2016
Filing Date:	19-AUG-2015
Time Stamp:	12:26:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$180
RAM confirmation Number	071316INTEFSW00009694081935
Deposit Account	081935
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Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	H0573143.pdf	612391 ab226011b73020b35e41287a5cbb749aa7b14ab8	no	4
Warnings:					
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3	Foreign Reference	H0573148.pdf	963553 15902c56e5a7069391acf945ee1afb4f362062e7	no	21
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/13/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
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(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	1757
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

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	Application Number	14829999
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	1757
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

	1	SCHULTZ-WITTMANN et al., Extended European Search Report (EESR) for EP Application NO. 10767689.2, dated July 11, 2016 (12 pages).	

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	Application Number	14829999
	Filing Date	2015-08-19
	First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
	Art Unit	1757
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

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Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2016-08-17
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

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EFS ID:	26662338
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Staci Medlock
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	17-AUG-2016
Filing Date:	19-AUG-2015
Time Stamp:	10:50:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	H0674506.pdf	1035133 51c33d6d6e6d84882d20a4901bdc629724d6881a	no	4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

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The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/829,999	Applicant(s) SCHULTZ-WITTMANN ET AL.	
	Examiner ERIC R. SMITH	Art Unit 1757	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/13/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *8-14 and 16-18* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *8-14 and 16-18* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *8/17/2016,7/13/2016*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Amendment

This is a non-final office action.

The amendment filed 7/13/2016 does not place the application in condition for allowance.

The rejections over Wenham et al. and Tomas et al. are withdrawn due to Applicant's amendment.

New rejections follow.

Specification

The disclosure is objected to because of the following informalities: Line 2 of paragraph [00147] on page 29 of the instant specification recites "are electrically conductive are electrically conductive".

Claim Rejections - 35 USC § 112

> The following is a quotation of 35 U.S.C. 112(b):
> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-14 and 16-18 rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 8 recites that the method comprises the steps of providing an interface passivation layer over the substrate and providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant. The method also comprises thermally treating the passivating film, the thermally treating diffusing at least a portion of the conductive dopant

from the passivating film throughout the interface passivation layer. Further, the claim recites that the steps of providing the interface passivation layer and providing the passivating film comprise

- Providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant
- Diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer
- Wherein remaining amorphous-silicon containing compound above the oxide layer defines the passivating film.

Logically, the interface passivation layer and passivating film must exist before or at least during the step of thermally treating. Therefore the passivating film that is being thermally treated and the interface passivation layer that the conductive dopant from the passivating film is diffusing through must have the following characteristics: the interface passivation layer is an oxide layer formed by diffusion of the oxygen dopant from an amorphous silicon-containing compound and the passivating film comprises amorphous silicon-containing compound.

Paragraph [00152] of the instant specification seems to describe this embodiment of the invention. That paragraph describes a layer xx3/xx7 comprising oxygen dopant and conductive dopant, reading on the claimed amorphous silicon-containing compound, provided over the substrate. The interface passivation layer xx4/xx6 is produced by thermally treating the layer xx3/xx7. However, the thermally treating of the layer xx3/xx7 simultaneously causes crystallization (at least in part) of the compound and diffusion of dopant from the compound (paragraph [00150] connects the activation and diffusion of dopants). Therefore it is unclear, when the claims are read in light of instant disclosure, that the interface passivation layer, which must be an oxide layer over the substrate, can exist before the step of thermally treating the passivating film. In other words, it is unclear how the thermally treating results in the conductive dopant diffusing from the passivating film throughout the interface passivation layer when the interface passivation layer is created only after the thermally treating step begins.

Only one thermal treatment step is recited; a person having ordinary skill in the art would not be apprised of how to form the interface passivation layer that is an oxide layer using steps that are distinct from the thermally treating step. While the scope of the claim may allow for the thermally treating step to be occurring during both the steps of providing the interface passivation layer and providing the passivating film as well as the step of diffusing at least a portion of the conductive dopant from the passivation film throughout the interface passivation layer, the disclosure only recites that those physical processes happen simultaneously. Therefore, at best, a skilled artisan would interpret the disclosure to allow for the oxygen atoms and the conductive dopant to be diffusing from the amorphous silicon-containing compound at the same time. There is not sufficient detail to conclude that the oxide layer forms prior to the diffusion of the conductive dopant, and therefore that the conductive dopant can diffuse throughout the interface passivation layer. **Claims 9-14 and 16-18** are also rejected based on their dependence from claim 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC R. SMITH whose telephone number is (571)270-7186. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Barton can be reached on 571 272 1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative

or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERIC R SMITH/
Examiner, Art Unit 1757

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	2812
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/E.R.S/	1	20080000521	A1	2008-01-03	Sivoththaman et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/E.R.S/	1	EP 1 643 564	EP	A2	2006-04-05	Sanyo Electric Co.	English Document	X

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	2812
	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

/E.R.S/	1	SCHULTZ-WITTMANN et al., Search Report for EP Application No. 10767689.2, dated April 14, 2016 (7 pages).	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/ERIC R SMITH/	Date Considered	08/23/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Examiner Name	Eric R. Smith
	Attorney Docket Number	3304.001B

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kevin P. Radigan, Esq./	Date (YYYY-MM-DD)	2016-07-13
Name/Print	Kevin P. Radigan, Esq.	Registration Number	31789

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Art Unit	1757
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/E.R.S/	1	5972784		1999-10-26	Rohatgi et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/E.R.S/	1	20030092226	A1	2003-05-15	Nagashima et al.	

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/E.R.S/	SCHULTZ-WITTMANN et al., Extended European Search Report (EESR) for EP Application NO. 10767689.2, dated July 11, 2016 (12 pages).	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	Art Unit
	ERIC R SMITH	1757

CPC- SEARCHED		
Symbol	Date	Examiner
H01L21/2022,2026,02356	8/24/2016	ERS
C30B1/023	8/24/2016	ERS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
kEY			

SEARCH NOTES		
Search Notes	Date	Examiner
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "oxygen diffusion")	4/6/2016	ERS
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "codiffusion")	4/6/2016	ERS
Keyword search in H01L31/186-1872, 02168 (see EAST history for search strategy)	4/6/2016	ERS
Keyword search in H01L21/02667,02694	4/6/2016	ERS
Keyword search in CPC subclasses (See EAst history for search strategy)	8/24/2016	ERS
Updated inventor search in PALM/DAV	8/24/2016	ERS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	6636	h01l21/2022,2026,02356.cpc.	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:24
L7	4192	l6 and (thermal$3 or heat$3 or temperature$1)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:24
L8	1552	l6 and ((oxygen or "o.sub.2") and (dop$3 or diffus$3))	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:25
L9	1549	l7 and l8	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:25
L10	1324	l9 and ("a-si" or amorphous near silicon)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:25
L11	361	l6 and (((oxygen or "o.sub.2") and (dop$3 or diffus$3)) same ("a-si" or amorphous near silicon))	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:26
L12	359	l11 and l7	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:26
L13	95	l12 and (passivat$3)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 10:27
L14	603	c30b1/023.cpc.	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 11:00
L15	93	l14 and ((oxygen or "o.sub.2") and (dop$3 or diffus$3))	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 11:01
L16	281	l14 and ("a-si" or amorphous near silicon)	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 11:01
L17	64	l15 and l16	US-PGPUB; USPAT; USOCR; FPRS	AND	ON	2016/08/24 11:01

8/24/2016 3:02:48 PM
C:\Users\esmith3\Documents\EAST\Workspaces\Cells_thin_films_\14829999_xtalline_passivation_interface_con.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Oliver SCHULTZ-WITTMANN, et al. Confirmation No.: 1023

Serial No.: 14/829,999 Group Art Unit: 1757

Filed: August 19, 2015 Examiner: Eric R. Smith

Title: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Response to Office Action

Dear Commissioner:

This paper is filed responsive to the Office Action mailed August 26, 2016, in connection with the above-designated U.S. patent application, and is in accordance with the November 28, 2016, Interview between the Examiner and Applicant's undersigned representative. Allowance of the application is respectfully requested in view of the Amendments and Remarks below.

Amendments to the Specification appear on page 2, of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 5 of this paper.

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Page 321

Amendments to the Specification

Kindly amend paragraph [00147] as follows:

[00147] In any of the structures above, the layers (e.g., xx2, xx3, xx4, xx6, xx7 and xx8) are electrically conductive ~~are electrically conductive~~, i.e., the metallization can be placed directly on the outer layer. (In typical high-efficiency solar cells this is not the case since surface passivation is usually done by materials that are also electrical insulators.) This allows for innovative metallization schemes, for example, the solar cells can be laminated into a module which has the electrodes embedded in the glass or in the lamination sheets. Furthermore, conductive sheets can be applied to mechanically strengthen the cells. Another way of metallization could involve the deposition of thin lines of metals. Due to the conductivity of the surfaces, the requirements on the metal paste are reduced because they directly contact the outer layers and do not need to etch through an insulating layer in order to contact the solar cell. Another example would be the direct evaporation or sputtering of metal onto the conductive surfaces.

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Page 322

Amendments to the Claims

Kindly amend claim 8, and cancel claim 16 (without prejudice), as set forth below. All pending claims are reproduced below, with changes in the amended claims shown by underlining for added matter, and strikethrough or double brackets for deleted matter.

1-7. (Previously Canceled).

8. (Currently Amended) A method of fabricating a solar cell, comprising:

providing a substrate;

providing an interface passivation layer over the substrate;

providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant;

wherein providing the interface passivation layer and providing the passivating film comprise:

providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;

thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film; and

wherein the thermally treating ~~the passivating film, the thermally treating diffusing~~ also diffuses at least a portion of the conductive dopant ~~from the passivating film~~ throughout the interface passivation layer to facilitate electrical connection to the substrate; and

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providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate[[; and]].

~~wherein providing the interface passivation layer and providing the passivating film comprise:~~

~~providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;~~

~~diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and~~

~~wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.~~

9. (Original) The method of claim 8, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

10. (Original) The method of claim 9, wherein the crystallized passivating film is a transparent film.

11. (Original) The method of claim 9, wherein the crystallization of the passivating film improves a passivation of the passivating film.

12. (Original) The method of claim 9, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.

13. (Original) The method of claim 8, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.

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14. (Original) The method of claim 8, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.

15. (Previously Canceled).

16. (Canceled).

17. (Original) The method of claim 8, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.

18. (Original) The method of claim 8, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

19-20. (Previously Canceled).

* * * * *

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Remarks

Favorable consideration and allowance of the application are respectfully requested. Claims 8-14 & 17 & 18 remain pending.

Initially, Applicant thanks the Examiner for the time afforded Applicant's undersigned representative on November 28, 2016, regarding amended claim 8 presented herewith. Based on the Interview, it is Applicant's understanding that amended claim 8 addresses the 35 U.S.C. §112(b), second paragraph, indefiniteness rejection stated in the Office Action. Should any issue remain unresolved by this paper, Applicant requests the Examiner to telephone Applicant's undersigned representative in order to discuss the matter in the hope of facilitating prosecution of the application.

By this paper, specification paragraph [00147] is amended to address the typographical error noted in the Office Action at line 2 of the paragraph. Based on this amendment, withdrawal of the specification objection is respectfully requested.

Claims 8-14 & 16-18 were rejected under 35 U.S.C. §112(b), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventors regard as the invention. Responsive to this rejection, claim 8 is amended (and claim 16 is canceled without prejudice), to recite, in part, that providing the interface passivation layer and providing the passivating film includes thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer. Additionally, the claim is amended to specify that the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate. Based on this amendment, claim 16 is canceled without prejudice, with the language thereof being included in amended claim 8. Further support for amended claim 8 can further be found, for instance, in specification paragraph [00152]. No new matter is believed added to the application by any amendment presented. Based upon the amended language, reconsideration and withdrawal of the 35 U.S.C. §112(b), second paragraph, rejection to claims 8-14, 17 & 18, are respectfully requested.

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All pending claims are believed to be in condition for allowance, and such action is respectfully requested.

In this amendment, Applicant has amended claim 8, and canceled claim 16 (without prejudice), to facilitate expeditious prosecution of the application. Applicant is not conceding that the subject matter encompassed by the claims prior to this amendment is unpatentable over the art cited in the Office Action. Rather, Applicant respectfully reserves the right to pursue claims in one or more continuing applications, including claims capturing the subject matter encompassed by the claims prior to this amendment, and additional claims.

Should any issue remain unresolved by this paper, Applicant's undersigned attorney invites the Examiner to telephone him at the time that the Examiner is considering this Response, in order to discuss the matter in the hope of facilitating prosecution of this application.

Respectfully submitted,

/Kevin P. Radigan, Esq./

Kevin P. Radigan, Esq.
Attorney for Applicant
Registration No.: 31,789

Dated: November 28, 2016

HESLIN ROTHENBERG FARLEY & MESITI P.C.
5 Columbia Circle
Albany, New York 12203-5160
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Facsimile: (518) 452-5579

Electronic Acknowledgement Receipt

EFS ID:	27618039
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Staci Medlock
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	28-NOV-2016
Filing Date:	19-AUG-2015
Time Stamp:	14:19:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	H0754240.pdf	130469 3bb1a3a94537015490d5edac2bd066b198df25ca	no	7

Warnings:

Information:	
Total Files Size (in bytes):	130469

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/829,999	Filing Date 08/19/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/28/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 9	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
ERIC V. BURNS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

23405 7590 11/30/2016

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER
SMITH, ERIC R

ART UNIT	PAPER NUMBER
1757	

MAIL DATE	DELIVERY MODE
11/30/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	14/829,999	SCHULTZ-WITTMANN ET AL.	
	Examiner	Art Unit	
	ERIC R. SMITH	1757	

All participants (applicant, applicant's representative, PTO personnel):

(1) *ERIC R. SMITH*. (3)_____.

(2) *Kevin Radigan*. (4)_____.

Date of Interview: *28 November 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☒112 ☐102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *8*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Mr. Radigan sent Examiner Smith a proposed claim amendment (attached) which was intended to address the 112(b) rejection in the Office Action of 8/26/2016. Examiner Smith agreed that the language would overcome the rejection if properly submitted into the record. Examiner Smith also discussed how claim 16 may not have a different scope than claim 8 and how line 12 of the proposed amendment recites "define the oxygen dopant", which may have been intended to be "diffuse the oxygen dopant".

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☒ Attachment

/ERIC R SMITH/
Primary Examiner, Art Unit 1757

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Proposed Claim Amendments – 11/28/2016

8. (Currently Amended) A method of fabricating a solar cell, comprising:

providing a substrate;

providing an interface passivation layer over the substrate;

providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant;

wherein providing the interface passivation layer and providing the passivating film comprise:

providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;

thermally treating the amorphous silicon-containing compound to define the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film;

wherein the thermally treating ~~the passivating film, the thermally treating diffusing~~ also diffuses at least a portion of the conductive dopant ~~from the passivating film~~ throughout the interface passivation layer to facilitate electrical connection to the substrate; and

providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate[[; and]].

~~wherein providing the interface passivation layer and providing the passivating film comprise:~~

~~providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;~~

~~diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and~~

~~wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.~~

* * * * *

Smith, Eric (Ryan)

From: Kevin P. Radigan <KPR@hrfmlaw.com>
Sent: Monday, November 28, 2016 8:31 AM
To: Smith, Eric (Ryan)
Subject: Serial No. 14/829.999
Attachments: 14829999_ProposedClaimAmendments_11-28-16 (H0754058xD16FB).pdf

Dear Examiner,

Attached is a proposed amended claim 8 to facilitate our discussion at 11:30 am EST today.

Thank you for your assistance,

Kevin P. Radigan, Esq.
Heslin Rothenberg Farley & Mesiti P.C.
5 Columbia Circle
Albany, New York 12203
ph (518) 452-5600
fax (518) 452-5579
email kpr@hrfmlaw.com

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NOTICE OF ALLOWANCE AND FEE(S) DUE

23405 7590 01/30/2017

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER
SMITH, ERIC R

ART UNIT	PAPER NUMBER
1757	

DATE MAILED: 01/30/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

TITLE OF INVENTION: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/01/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23405 7590 01/30/2017
HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

TITLE OF INVENTION: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/01/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
SMITH, ERIC R	1757	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

23405 7590 01/30/2017

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER	
SMITH, ERIC R	

ART UNIT	PAPER NUMBER
1757	

DATE MAILED: 01/30/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/829,999	Applicant(s) SCHULTZ-WITTMANN ET AL.	
	Examiner ERIC R. SMITH	Art Unit 1757	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 11/28/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *8-14,17 and 18*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ERIC R SMITH/
Primary Examiner, Art Unit 1757

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

US PGPub 2010/0075485 to Rana (of record) is the closest prior art. Rana teaches providing an amorphous silicon-containing compound (element 260 of Fig. 3) over an upper surface (244) of a substrate (226), and the diffusion of an oxygen dopant through the amorphous silicon-containing compound to form an oxide layer and diffusion of conductive dopant into the substrate by a thermally treating step (¶0020-0030, 0030-0036). Rana does not teach that the oxygen dopant diffuses into the upper surface of the substrate, as is claimed, but rather forms over the remaining amorphous silicon containing compound away from the substrate. Therefore the claims are allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC R. SMITH whose telephone number is (571)270-7186. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Barton can be reached on 571 272 1307. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERIC R SMITH/
Primary Examiner, Art Unit 1757

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14841	h01l31/18-1896.cpc.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:06
L2	5051	h01l31/028,0368-03685,0376-03762,068,072,074,0747.cpc.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:11
L3	16893	l1 or l2	US-PGPUB; USPAT	AND	ON	2017/01/20 14:11
L4	2507	l3 and (amorphous).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:12
L5	24	l4 and (oxygen or "o.sub.2").clm. with (doping or dopant).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:12
L6	369	l4 and (passivat$3).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:13
L7	69	l6 and (thermal or heat).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:13
L8	41	l7 and (doping or dopant).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:13
L9	65	l8 or l5	US-PGPUB; USPAT	AND	ON	2017/01/20 14:13
L10	64	l9 and (method or process or step).clm.	US-PGPUB; USPAT	AND	ON	2017/01/20 14:15

1/20/2017 2:34:47 PM
C:\Users\esmith3\Documents\EAST\Workspaces\Cells_thin_films_\14829999_xtalline_passivation_interface_con.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	**Art Unit**
	ERIC R SMITH	1757

CPC						
Symbol					**Type**	**Version**
H01L		31	/	022425	F	2013-01-01
H01L		31	/	1872	I	2013-01-01
H01L		31	/	1864	I	2013-01-01
H01L		31	/	1884	I	2013-01-01
H01L		31	/	022466	I	2013-01-01
H01L		31	/	02167	I	2013-01-01
H01L		31	/	02168	I	2013-01-01
H01L		31	/	1868	I	2013-01-01
Y02E		10	/	50	A	2013-01-01
Y02P		70	/	521	A	2015-11-01
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 8	
/E.R.S./ Primary Examiner.Art Unit 1757 (Primary Examiner)	01/20/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	**Art Unit**
	ERIC R SMITH	1757

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	31 / 0224 (2006.01.01)						
CROSS REFERENCE(S)		H	0	1	L	31 / 0216 (2014.01.01)						
		H	0	1	L	31 / 18 (2006.01.01)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 8	
/E.R.S./ Primary Examiner.Art Unit 1757 01/20/2017 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	**Art Unit**
	ERIC R SMITH	1757

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 8	
/E.R.S./ Primary Examiner.Art Unit 1757 01/20/2017 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 18

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14829999	SCHULTZ-WITTMANN ET AL.
	Examiner	**Art Unit**
	ERIC R SMITH	1757

CPC- SEARCHED		
Symbol	**Date**	**Examiner**
H01L21/2022,2026,02356	8/24/2016	ERS
C30B1/023	8/24/2016	ERS

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
kEY			

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "oxygen diffusion")	4/6/2016	ERS
Keyword search in Google Scholar (amorphous + silicon + passivat$ + (thermal or anneal$) + "codiffusion")	4/6/2016	ERS
Keyword search in H01L31/186-1872, 02168 (see EAST history for search strategy)	4/6/2016	ERS
Keyword search in H01L21/02667,02694	4/6/2016	ERS
Keyword search in CPC subclasses (See EAst history for search strategy)	8/24/2016	ERS
Updated inventor search in PALM/DAV	8/24/2016	ERS
Updated inventor search in DAV	1/20/2017	ERS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
H01L31	18-1896,028,0368-03685,0376-03762,068,07,074,0747	1/20/2017	ERS

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23405 7590 01/30/2017
HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	08/19/2015	Oliver SCHULTZ-WITTMANN	3304.001B	1023

TITLE OF INVENTION: HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	05/01/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
SMITH, ERIC R	1757	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Kevin P. Radigan, Esq.
2 HESLIN ROTHENBERG
3 FARLEY & MESITI P.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: TETRASUN, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Jose, CA (USA)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
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5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature Kevin P. Radigan Date April 21, 2017

Typed or printed name Kevin P. Radigan, Esq. Registration No. 31,789

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	14829999
Filing Date:	19-Aug-2015
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Filer:	Kevin P. Radigan/Staci Medlock
Attorney Docket Number:	3304.001B

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt	
EFS ID:	28991879
Application Number:	14829999
International Application Number:	
Confirmation Number:	1023
Title of Invention:	HIGH-EFFICIENCY SOLAR CELL STRUCTURES AND METHODS OF MANUFACTURE
First Named Inventor/Applicant Name:	Oliver SCHULTZ-WITTMANN
Customer Number:	23405
Filer:	Kevin P. Radigan/Staci Medlock
Filer Authorized By:	Kevin P. Radigan
Attorney Docket Number:	3304.001B
Receipt Date:	21-APR-2017
Filing Date:	19-AUG-2015
Time Stamp:	14:16:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$960
RAM confirmation Number	042417INTEFSW00000533081935
Deposit Account	081935
Authorized User	Staci Medlock
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees)	

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30769 8dd526c742478806c5bf03dee0842cbc3ede194b	no	2
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14829999
Filing Date	2015-08-19
First Named Inventor	Oliver SCHULTZ-WITTMANN et al.
Art Unit	2812
Examiner Name	Eric R. Smith
Attorney Docket Number	3304.001B

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, /E.R.S/ 2/13/2017	1	4481046		11/1984 ~~1984-09-29~~	Bouldin et al.	
/E.R.S/	2	6649956	B2	2003-11-18	Yoshida et al.	

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/E.R.S/	1	JP-SHO-57-071188	JP	A	1982-01-05	Mitsubishi Electric Corp.	English Abstract Only	X

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/829,999	05/30/2017	9666732	3304.001B	1023

23405 7590 05/10/2017

HESLIN ROTHENBERG FARLEY & MESITI PC
5 COLUMBIA CIRCLE
ALBANY, NY 12203

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Oliver SCHULTZ-WITTMANN, Sunnyvale, CA;
TETRASUN, INC., San Jose, CA;
Denis DeCEUSTER, Woodside, CA;

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