

ELECTRICAL CHARACTERIZATION OF POLYSILICON-TO-SILICON INTERFACES

E.F. Crabbé, J.L. Hoyt, R.F.W. Pease, and J.F. Gibbons
Stanford Electronics Laboratories, Stanford, CA 94305

ABSTRACT

The structural properties of the polysilicon-to-silicon interface affect the electrical characteristics of devices with polysilicon contacts. The current characteristics of advanced bipolar transistors with polysilicon base and emitter contacts are very sensitive to the presence of interfacial oxides and segregated dopants. Hence, bipolar transistors provide an excellent tool for studying the effects of different interfaces on minority carrier transport. The transport of majority carriers through polysilicon-to-silicon interfaces is best investigated with contact resistance structures. In this paper, we review the correlation between interface morphology and the electrical properties of a variety of interfacial layers, ranging from native oxides to chemical oxides or thermal nitrides. Measurements on both *npn* transistors and contact resistance structures provide quantitative information on the trade-off between base current (i.e. current gain) and emitter resistance. Within this constraint, a variety of electrical characteristics can be obtained by tailoring the nature of the polysilicon-to-silicon interface to the device application of interest.

INTRODUCTION

Polysilicon-to-silicon interfaces play an important role in the operation of scaled transistors. The use of polysilicon base and emitter contacts is largely responsible for the lateral scaling and high speed performance of advanced bipolar transistors [1]. As the vertical profiles of these devices are scaled down, the transistor characteristics become extremely sensitive to the nature of these contacts. In particular, the polysilicon-to-silicon interface affects the transport of both majority and minority carriers. Because it is a three terminal, minority carrier device, the bipolar transistor is an excellent test structure for studying minority carrier transport across the polysilicon-to-silicon interface. The effect of the interface on majority carriers is best studied with contact resistance structures such as the Kelvin resistor [2].

Several different types of interfacial layers are investigated in this work. The chemical and structural nature of these interfaces are sensitive to several processing variables, particularly the anneal conditions following deposition. In the following section we briefly review the electrical characterization techniques used in this work. The annealing behavior of emitter contacts with various interfacial layers is then discussed. We begin with n^+ polysilicon emitter contacts with 'clean' (i.e. native oxide) interfaces. The effect of the interface on carrier transport varies widely with the type of anneal chosen (either conventional furnace annealing or rapid thermal annealing). Emitter contacts with modified interfaces will then be considered. Finally, the effects of different interfacial layers on the behavior of boron doped polysilicon base contacts will be discussed.

ELECTRICAL CHARACTERIZATION TOOLS

The transport of both majority and minority carriers should be considered for polysilicon emitter contacts. In this work, we concentrate on electron and hole transport in n^+ (arsenic doped) polysilicon *emitter* contacts for *npn* devices. For the polysilicon *base* contacts, only the transport of majority carriers (holes) is important. Electrons do not reach the p^+ base contacts because they are repelled by the potential barrier set up by the lateral doping gradient. Fig. 1 is a simplified cross-section of an *npn* transistor with a polysilicon emitter contact. In a well designed device, the base current I_b is equal to the hole current injected from the base into the emitter. The maximum transistor current gain is inversely proportional to I_b , which is generally of the form $I_b = I_{b0} \exp(qV_{be}/kT)$. The base saturation current density, I_{b0} (A/cm^2) is used as a figure of merit for polysilicon emitter contacts, and should be minimized for maximum current gain. In this work, I_{b0} is extracted by extrapolating the ideal component of I_b to zero bias and normalizing the data to a temperature of 300 K, using the method of Kwark [3].

Figure 1: Simplified cross-section of an npn bipolar transistor with a polysilicon emitter contact. The base current, I_B is determined by recombination of holes (1) in the n^+ single-crystal emitter, (2) at the polysilicon-to-silicon interface, and (3) in the polysilicon itself.

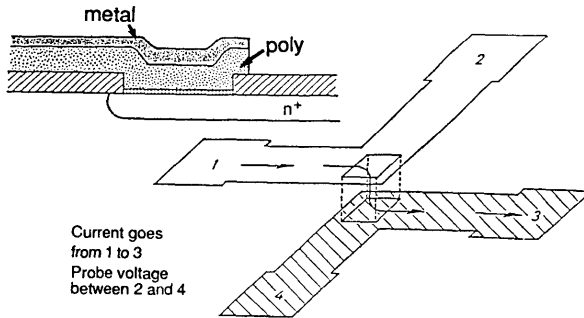
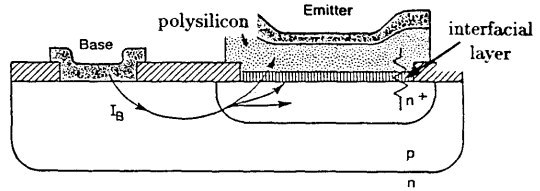


Figure 2: Cross-section and top view of a Kelvin resistor structure used to measure the emitter resistance. The emitter specific contact resistivity, ρ_e has units of $\Omega - \mu\text{m}^2$.

The electron or majority carrier transport in polysilicon-to-silicon contacts is characterized by R_e , the emitter resistance. R_e can be measured accurately with a Kelvin resistor structure as illustrated in Fig. 2. The emitter resistance has four components: (1) the single-crystal component, which is negligible in all cases, (2) the contact resistance of the polysilicon-to-silicon interface, (3) the polysilicon resistance, which is generally small and (4) the metal-to-polysilicon resistance. By independently measuring the metal-to-polysilicon resistance, we can isolate the interfacial component of R_e , which is the one of interest here. As a figure of merit for majority carrier transport, we use the emitter specific contact resistivity, ρ_e which should be minimized for VLSI applications.

EMITTER CONTACTS WITH A 'CLEAN' POLYSILICON-TO-SILICON INTERFACE

Polysilicon contacts with 'clean' polysilicon-to-silicon interfaces were fabricated in the following manner. After opening the contact windows by wet oxide etching, the wafers received a standard RCA clean followed by a 50:1 HF dip etch. Cleaning of the wafers was performed immediately prior to loading in a conventional LPCVD polysilicon reactor. Polysilicon was then deposited at 620 °C to achieve thicknesses in the range of 300 to 500 nm. It is known that this procedure produces a thin, amorphous interfacial layer, which is several monolayers thick [4]. This layer, often referred to as a 'native oxide', consists of carbon atoms as well as a thin oxide which probably grows as the wafers enter the hot reactor in the presence of oxygen from the atmosphere. The structure and continuity of the native oxide interface is very sensitive to the concentration of arsenic in the polysilicon and the emitter anneal temperature.

Continuous Native Oxide Interfaces

After deposition, the polysilicon is implanted with arsenic and capped with LPCVD oxide. The emitter anneal then redistributes the arsenic uniformly in the polysilicon, and

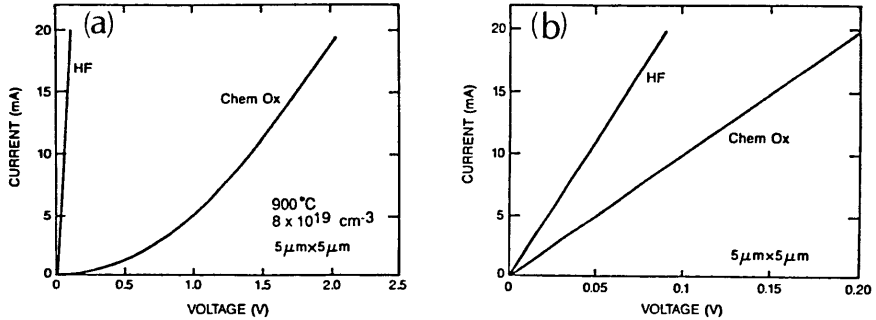


Figure 3: Current-voltage characteristics for HF etched and Chem-Ox interfaces annealed at (a) 900 and (b) 1000 °C for 30 min. The arsenic concentration in the polysilicon is $8 \times 10^{19} \text{ cm}^{-3}$ in these samples.

some arsenic outdiffuses into the underlying substrate to form the emitter-base junction. If the average arsenic concentration in the polysilicon is less than or equal to $2 \times 10^{20} \text{ cm}^{-3}$, and if the anneal temperature does not exceed 900°C , Bravman *et al.* have shown that the native oxide interface remains essentially continuous during the emitter anneal [4]. Evidence that the interfacial layer is degraded (i.e. the presence of oxide inclusions and epitaxial realignment structures) is absent in this case.

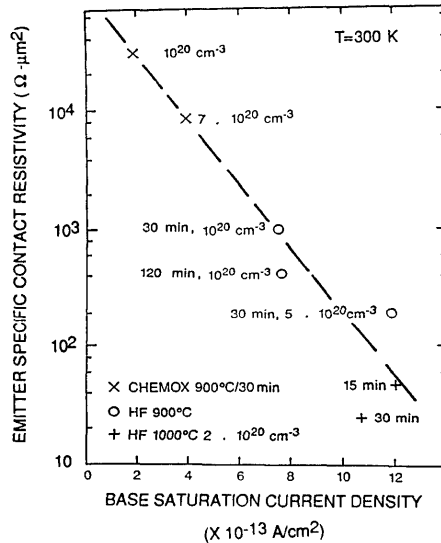
Under these conditions, the emitter resistance is dominated by the interfacial layer, and is on the order of $1000 \text{ } \Omega - \mu\text{m}^2$. The current-voltage characteristics of these contacts are only slightly non-linear, and have little if any temperature dependence. This is a strong indication that electron transport across the continuous native oxide is dominated by a tunnelling mechanism. Fig. 3 (a) compares the I-V characteristics for HF etched and Chem-Ox interfaces. As discussed below, the contacts with Chem-Ox interfaces exhibit highly non-linear characteristics for low emitter annealing temperatures.

For a continuous interfacial layer, the transport of minority carriers (holes) is strongly dependent upon the arsenic concentration in the polysilicon. For doping levels below 10^{20} cm^{-3} , Patton *et al.* [5] have shown that most of the holes reaching the interface recombine there at interface states. This effective recombination leads to rather large base saturation current densities ($\geq 5 \times 10^{-12} \text{ A/cm}^2$). As the arsenic concentration is increased to 1 or $2 \times 10^{20} \text{ cm}^{-3}$, a non-negligible fraction of the arsenic segregates at grain boundaries in the polysilicon and at the polysilicon-to-silicon interface[6]. The segregated arsenic atoms passivate the interface states, greatly reducing hole recombination. They also impede hole transport through the interface by setting up a potential barrier of approximately 100 meV [7]. When the native oxide is not degraded and few holes recombine at the interface, the base current is minimized. Minimum base saturation current densities of $3 \times 10^{-13} \text{ A/cm}^2$ have been obtained for an arsenic concentration of $2 \times 10^{20} \text{ cm}^{-3}$ [5].

Discontinuous Interfaces

For arsenic concentrations above $2 \times 10^{20} \text{ cm}^{-3}$, or for annealing temperatures above 900°C , the native oxide interface is no longer continuous. This break-up and agglomeration of the interfacial layer substantially modifies the electrical characteristics of the interface. The I-V characteristics of the contacts are linear, even in the case of Chem-Ox interfaces (see Fig. 3 (b)). The emitter resistance is dominated by the metal-to-polysilicon contact resistance and ρ_e is below $100 \text{ } \Omega - \mu\text{m}^2$. The electrons flow preferentially through the openings in the native oxide interface, which are paths of least resistance. The minority carriers (holes) are not effectively blocked by the interface either. As a result, the base saturation current is increased ($I_{bo} \approx 10^{-12} \text{ A/cm}^2$). Because of enhanced hole recombination at these high emitter doping levels, there is no significant dependence of I_{bo} on polysilicon thickness for the range examined in this work (300 - 500 nm).

Figure 4: Data from *npn* bipolar transistors and Kelvin resistors which quantitatively illustrates the trade-off between emitter resistance and base current for n^+ polysilicon emitter contacts. The interfacial layer is thick and continuous in the upper left region of the plot, and essentially completely broken-up in the lower right region.



By choosing the arsenic concentration and the anneal temperature, the device designer can choose either a transparent or reflective polysilicon-to-silicon interface. However, the majority and minority transport parameters can not be optimized independently. As illustrated in Fig. 4, there is a trade-off between the emitter resistance and the base current [7]. The reason for this trade-off is intuitively clear: if the native oxide layer is continuous and blocks hole transport, it also impedes the transport of electrons. Consequently, an emitter characterized by a low base current also has a high emitter resistance, and vice versa.

Complete Interface Break-up

The polysilicon-to-silicon interface can be completely eliminated by rapid thermal annealing the emitters at high temperatures. In this case, the polysilicon is epitaxially aligned to the silicon substrate [8]. To maximize epitaxial alignment while minimizing arsenic diffusion, the arsenic doping level should be at least 5×10^{20} cm $^{-3}$, and the RTA temperature should be greater than 1100 °C[9].

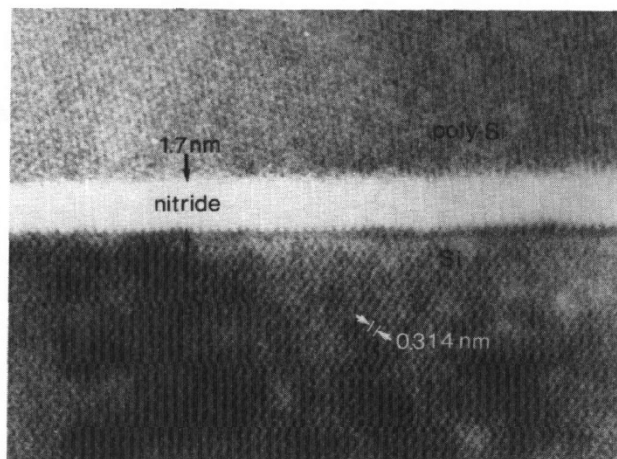
The minority hole current is rather insensitive to the processing conditions ($I_{b0} \approx 10^{-12}$ A/cm ^{2} at 300 K), even if the interface is not completely broken-up [10]. The hole current is determined primarily by the transport parameters in the heavily-doped aligned polysilicon. The emitter resistance has a very small interface component and is dominated by the metal-to-polysilicon contact resistance. If an adequate metallization technology is used, the emitter specific contact resistivities below $50 \Omega - \mu\text{m}^2$ should be achievable. The high anneal temperatures induce high dopant activation, leading to a very low metal-to-polysilicon contact resistance. The low emitter resistance comes at the expense of a relatively high base current. Hence, these types of contacts are best suited to applications where the emitter resistance places the largest constraint on device design.

EMITTER CONTACTS WITH MODIFIED INTERFACES

Chemically Oxidized Interfaces

The polysilicon-to-silicon interface can be altered chemically prior to polysilicon deposition in order to form a thicker interfacial 'oxide' layer. The fabrication sequence is almost identical to the one described above. After the conventional RCA clean followed by an HF dip, the wafers are chemically oxidized for 10 min. in a 70 °C solution of

Figure 5: Cross-sectional TEM micrograph of an interfacial nitride layer grown by rapid thermal nitridation.



5:1:1 $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HNO}_3$. After a DI water rinse and spin-dry, the wafers are loaded into the polysilicon reactor. The resulting chemical oxide thickness is on the order of 1.6 nm and is continuous across the wafer [4].

For low anneal temperatures ($T \leq 900^\circ\text{C}$), the polysilicon-to-silicon interface remains continuous. The chemical oxide blocks the injection of holes in the polysilicon and very low base currents can be obtained. The oxide layer also affects the emitter resistance. R_e is dominated by the polysilicon-to-silicon interface component and is rather high ($6000 \Omega - \mu\text{m}^2$ for $J = 1.1 \times 10^4 \text{ A/cm}^2$) and non-linear as shown in Fig. 3 (a). At higher anneal temperatures, (1000°C) approximately 15 % of the contact area has a broken-up interface: the base current increases as expected and the emitter resistance is linear and lower ($\rho_e \approx 100 \Omega - \mu\text{m}^2$) as shown in Fig. 3 (b). In either case, the base current/emitter resistance trade-off is still valid, but the data points are displaced towards lower base currents and higher emitter resistances (see Fig. 4).

Thermally Stable Layers: Nitrided Interfaces

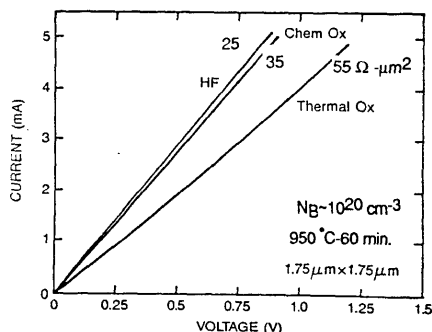
A different approach to altering the polysilicon-to-silicon interface is to grow an extremely thin insulating layer which does not break-up during the emitter anneal. A thermal nitride film satisfies this requirement, and can be grown by rapid nitridation in a very reproducible manner. To this end, some wafers were nitrided at either 750 or 900°C for 30 sec. in a pure ammonia ambient after an RCA clean followed by an HF dip etch. They were then immediately loaded into a reactor for polysilicon deposition. The thickness of the resulting interfacial nitride layers was 1.7 or $2.1 \pm 0.2 \text{ nm}$ for the two nitridation temperatures respectively, as determined by high resolution transmission electron microscopy. Fig. 5 is a cross-sectional TEM micrograph of the nitride layer following a 1000°C , 15 min. anneal. The average arsenic concentration in the polysilicon is $2 \times 10^{20} \text{ cm}^{-3}$.

The nitrided interface is undegraded by either high anneal temperatures (up to 1000°C) or high arsenic concentrations (up to $5 \times 10^{20} \text{ cm}^{-3}$). The holes either recombine at the interface or are repelled, but very few tunnel through the nitride layer. As a result, the base current of bipolar transistors with nitrided emitters can be as low as $5 \times 10^{-14} \text{ A/cm}^2$ at 300 K [10]. However, the emitter resistance is very high and non-linear (about $2 \times 10^4 \Omega - \mu\text{m}^2$ for $J = 1.3 \times 10^3 \text{ A/cm}^2$). These types of contacts are useful for applications in which the series resistance is not a critical concern.

BASE CONTACTS

For boron doped polysilicon base contacts, the primary concern is the effect of the polysilicon-to-silicon interface on majority carrier (hole) transport. Kelvin resistor structures with both native oxide and chemical oxide interfaces were investigated. In addition,

Figure 6: Current-voltage characteristics of p^+ (boron-doped) polysilicon contacts.



a third set of contacts with thermally oxidized interfaces was fabricated (600 °C oxidation for 10 min. in dry oxygen). The average chemical concentration of boron in the polysilicon was 10^{20} cm^{-3} . The contacts were annealed at 950 °C for 1 hr. The I-V characteristics of these contacts are shown in Fig. 6 and are linear in all three cases. The emitter resistances are 25, 35, and $55 \Omega \cdot \mu\text{m}^2$ for the native oxides, chemical oxides, and thermally oxidized contacts respectively. Unlike the case of n^+ polysilicon contacts, there is little difference in the majority carrier transport properties for the different interfacial layers. The most probable reason for this surprising result is that boron tends to segregate in the 'oxide' layer at the interface, altering its physical properties, thereby making it fairly transparent to hole transport.

CONCLUSIONS

The structure of the interfacial layer at the polysilicon-to-silicon interface can dominate the carrier transport properties of polysilicon contacts. For arsenic-doped emitter contacts, there is a fundamental trade-off between base current (i.e. gain) and emitter resistance. This trade-off simply implies that a barrier to hole injection at the interface will also impede the flow of electrons. Within the base current/emitter resistance constraint, the interface can be tailored for specific applications depending on the device requirements. In the case of boron-doped polysilicon base contacts, the interface has only a minor effect on majority carrier (hole) transport.

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