

IMPACT OF PROCESSING PARAMETERS ON BASE CURRENT IN POLYSILICON CONTACTED BIPOLAR TRANSISTORS

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ABSTRACT

A number of models have been presented to explain the lower base current in bipolar transistors with polysilicon emitter contacts: the effects of oxides (native and chemically grown) at the polysilicon-silicon interface; dopant segregation at this interface; and minority carrier transport in the polysilicon. To differentiate between these models and to determine the process sensitivity of polysilicon contacted BJT's, a series of controlled experiments correlating physical structures with electrical characteristics have been performed.

We find that for anneals at low temperatures and times (e.g., 900°C/1hr) the unintentional native oxide at the polysilicon-silicon interface dominates the electrical characteristics, resulting in extremely low base currents. For higher temperature anneals or doping levels above $2 \times 10^{20}/\text{cm}^3$, the native oxide layer breaks up and epitaxial regrowth of the polysilicon layer occurs. This reduces the blocking action of the interface and allows more carriers to enter the polysilicon, increasing the base current by as much as a factor of four.

INTRODUCTION

The use of polysilicon as an emitter contact to bipolar transistors has received widespread attention because of the reduced device parasitics and improved process control that can be obtained. These advantages stem from the self-aligned structure and from the lower base current, compared to metal contacted devices. With the reduced base current, a higher device gain or a lower intrinsic base resistance (for the same gain) can be realized.

Controversy exists regarding the mechanisms that contribute to the lower base current with polysilicon emitter contacts. Ning and Isaac [1] explained the improvement in terms of minority carrier transport in the polysilicon layer itself: the polysilicon merely acts as an extension of the emitter. However, de Graaff and de Groot [2] suggested that an unavoidable consequence of the processing involved in making these devices is the formation of a native oxide layer on the single crystal silicon substrate prior to polysilicon deposition. This native oxide layer acts as a tunneling barrier to hole injection into the polysilicon. More recently, Neugroschel, et al. [3], have shown that if arsenic is not segregated to the polysilicon-silicon interface, there is no reduction in base current, compared to devices with metal contacts.

The use of intentional chemically grown interface oxides as a tunneling barrier to hole injection has been shown to give the lowest base currents. However, their use significantly degrades the high performance capability of the devices by increasing the emitter resistance an order of magnitude, reducing control of the emitter profile, and increasing low current leakage [4,5]. Therefore, this work concentrates on devices with "clean" interfaces, i.e., interfaces

with only an unavoidable native oxide. The relative importance of this interface and of the bulk properties of the polysilicon in influencing J_{oe} , the emitter saturation current density, has been examined by studying the effects of dopant segregation and hydrogen passivation at the polysilicon grain boundaries, polysilicon deposition and annealing temperature, doping level, and polysilicon thickness. High resolution cross-section transmission electron microscopy (XTEM) has been used to correlate the electrical and structural characteristics of these devices.

EXPERIMENTAL PROCEDURES

Three types of emitter contacts were formed on each wafer: Type A, metal reference with implanted emitter (Al-Si with a Ti barrier layer); Type B, polysilicon as the diffusion source for the emitter; and Type C, polysilicon with Type A implanted emitter (Fig. 1). This paper will focus on the Type B devices, the structure used for high performance bipolar circuits. Type A and C are used to monitor the process and for modeling purposes, respectively.

Following a standard pre-deposition treatment, consisting of an RCA clean followed by an HF dip etch, 4000Å of LPCVD polysilicon was deposited at 620°C (unless otherwise specified). Damage from the arsenic implantation is confined to the top 1000Å of the polysilicon layer, away from the interface. All anneals were performed in argon with a capping oxide layer.

Devices with a large area/perimeter ratio were chosen so that the area component of base current would dominate. This allows J_{oe} , the emitter saturation current density, to be extracted directly from the ideal component of the base current (Fig. 2). All data reported is for a temperature of 300°K (J_{oe} at a room temperature of 21°C will be lower by a factor of approximately 2.7). A consistent temperature is used in making comparisons between different devices because a variation of only 0.5-1.0°K adds an additional 10-20% uncertainty in the values of J_{oe} . The emitters in these devices were profiled using RBS and spreading resistance and modeled using procedures outlined elsewhere [6,7] to verify that the changes observed in J_{oe} were due to changes in S_p , the effective recombination velocity of the contact, and not due to an increase in the recombination rate in the single crystal portion of the emitter.

EXPERIMENTAL RESULTS AND DISCUSSION

Figures 3 and 4 show the dependence of J_{oe} on the average arsenic concentration in the polysilicon for a variety of anneals from 900°C to 1000°C. Three distinct regions of behavior can be observed and are described below.

As previously mentioned, Neugroschel [3] showed that segregation of arsenic to the polysilicon-silicon interface is essential in obtaining low values of base current. Similarly, we observed a dramatic reduction in J_{oe} as the arsenic concentration increased from 3.3×10^{19} to $1 \times 10^{20}/\text{cm}^3$. However, above $1 \times 10^{20}/\text{cm}^3$ the dependence is weak. The high base current observed at the lower

doping level can be explained by a high recombination rate at grain boundaries in the polysilicon, especially the polysilicon-silicon interface (a pseudo-grain boundary), due to interface states. The increase in doping level will decrease the barrier height at the grain boundaries and, consequently, decrease the recombination velocity there [8]. In addition, as the doping level in the polysilicon increases, more arsenic will be segregated to the grain boundaries thereby reducing the interface state density.

The effect of arsenic segregation on this recombination was examined by first annealing samples at 1000°C, to set the grain size and the structure of the interface. A subsequent anneal at 800°C will cause arsenic to segregate to the grain boundaries, drastically increasing the concentration of arsenic there. Figure 5 shows that such an anneal produces a 20% reduction in J_{oe} at $3.3 \times 10^{19}/\text{cm}^3$; however, there is little effect on J_{oe} at doping levels above $1 \times 10^{20}/\text{cm}^3$: the remaining interface states cannot be passivated by arsenic segregation.

To verify that recombination at the polysilicon-silicon interface and at grain boundaries in the polysilicon is appreciable, hydrogen was introduced by implantation as outlined elsewhere [9]. Kazmerski [10] found a correlation between the segregation of hydrogen to the grain boundaries and a reduction of the barrier height and recombination velocity of these boundaries. Similarly, we found that hydrogen reduced J_{oe} for the devices doped at $3.3 \times 10^{19}/\text{cm}^3$ by 65% to a value near that of the devices doped at $1 \times 10^{20}/\text{cm}^3$ (Fig. 6). Even the samples doped at $1 \times 10^{20}/\text{cm}^3$ show an appreciable drop of 38%, indicating that even at high arsenic concentrations there is appreciable carrier recombination at the grain boundaries.

As the arsenic concentration in the polysilicon increases from 1×10^{20} to $2 \times 10^{20}/\text{cm}^3$, J_{oe} decreases only slightly. In this region, J_{oe} increases strongly with the time and temperature of the anneal. J_{oe} values as low as $3.2 \times 10^{-13} \text{ A/cm}^2$ ($1.2 \times 10^{-13} \text{ A/cm}^2$ at 21°C) for a 900°C/1hr anneal were obtained. This represents a reduction in the value of J_{oe} by a factor of 35 from the value that would be obtained with the same arsenic profile in the single crystal silicon, but with a metal contact. For the 1000°C/30min anneal, J_{oe} increased to $1.2 \times 10^{-12} \text{ A/cm}^2$, representing a reduction of only a factor of 2.6 over that of a metal contact with the same profile. We have previously shown [11,12] that high temperature annealing degrades the integrity of the native oxide layer. With a 900°C anneal, good structural integrity is maintained at the interface, little epitaxial realignment occurs, and therefore carriers should still be blocked (Fig. 7). However, after a 1000°C anneal, the interfacial oxide agglomerates and epitaxial realignment of the polysilicon occurs (Fig. 8). Thus, the interface no longer acts as a blocking layer.

If carriers are not being adequately blocked by the interface, a reduction in the thickness of the polysilicon layer would be expected to increase the base current in the device. To examine this effect, three different polysilicon thicknesses were obtained on the same wafer by etching back regions to 450Å and 900Å after all thermal processing was complete. A laser signal was used to determine when to stop etching and XTEM was used to verify the thickness and uniformity of the etched-back regions. For a 900°C/3hr anneal, reducing the polysilicon thickness to 450Å has no effect on J_{oe} (Fig. 9). In addition, a substantial reduction in J_{oe} is obtained by using polysilicon instead of metal (zero polysilicon thickness). This anneal maintains an interfacial structure which allows few carriers to be injected into the polysilicon. In contrast, for a 1000°C/30min anneal, J_{oe} is increased by 20-50% for a thickness of 450Å and a much smaller reduction in J_{oe} is obtained by using polysilicon instead of metal. The integrity of the interface is reduced and a larger number of carriers recombine in the polysilicon layer. However, since no increase was observed for a thickness of 900Å, we can conclude that

only the first 450-900Å of the polysilicon layer was influencing the base current. It is not surprising that the carriers have such a short diffusion length in the polysilicon since it was shown above that recombination at the grain boundary interface states is appreciable even at doping levels of $1 \times 10^{20}/\text{cm}^3$.

As the arsenic concentration rises above $2 \times 10^{20}/\text{cm}^3$, J_{oe} increases. Part of this increase is due to a higher recombination rate in the single-crystal portion of the emitter, due to the higher doping level there. However, preliminary results suggest that the increase is actually dominated by an increase in the recombination velocity of the contact. This would be due to an enhancement, due to doping, in the rate at which the interface degrades and epitaxial realignment occurs.

To maintain the blocking action of the native oxide and obtain low values of base current, the polysilicon anneal should be minimized. For thick polysilicon layers, as in this work, the minimum anneal is limited by the time it takes to diffuse the implanted arsenic down through the polysilicon layer to form the emitter and to uniformly dope the grains of the polysilicon, for minimum series resistance. For thin polysilicon layers, there is the risk that the implantation could damage the interface, resulting in much larger values of J_{oe} . The best alternative for avoiding these problems is the use of in-situ doped polysilicon. The minimum anneal in this case will be limited by the time it takes to obtain a base-emitter junction deep enough so that the depletion region is confined in the single crystal silicon substrate and, also, to obtain the desired polysilicon resistivity.

CONCLUSION

In this work, we have presented the results of a detailed study correlating the physical structure and the electrical characteristics of devices contacted with polysilicon. In summary, extremely low values of base current can be obtained without resorting to the use of chemical oxides. The previously reported dependence of base current on the presence of arsenic at the polysilicon-silicon interface can be explained by a high recombination rate at the grain boundaries in the polysilicon. At doping levels above $1 \times 10^{20}/\text{cm}^3$, no further improvement can be offered by arsenic segregation. The most dominant effect is the degradation of the unintentional native oxide layer at the polysilicon-silicon interface produced by high temperature annealing or doping levels above $2 \times 10^{20}/\text{cm}^3$. This reduces the blocking action of the interface and allows more carriers to enter the polysilicon layer. Base current is increased substantially because of the high recombination rate that exists at grain boundaries in the polysilicon.

ACKNOWLEDGMENTS

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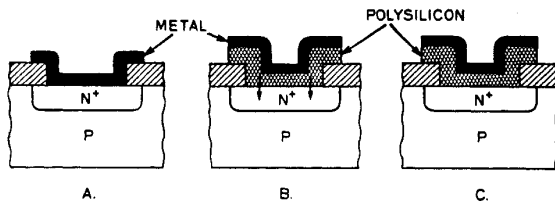


Fig. 1. Cross-section of the three types of emitter contacts used: Type A, metal reference with implanted emitter (Al-Si with a Ti barrier layer); Type B, polysilicon as the diffusion source for the emitter; and Type C, polysilicon with Type A implanted emitter.

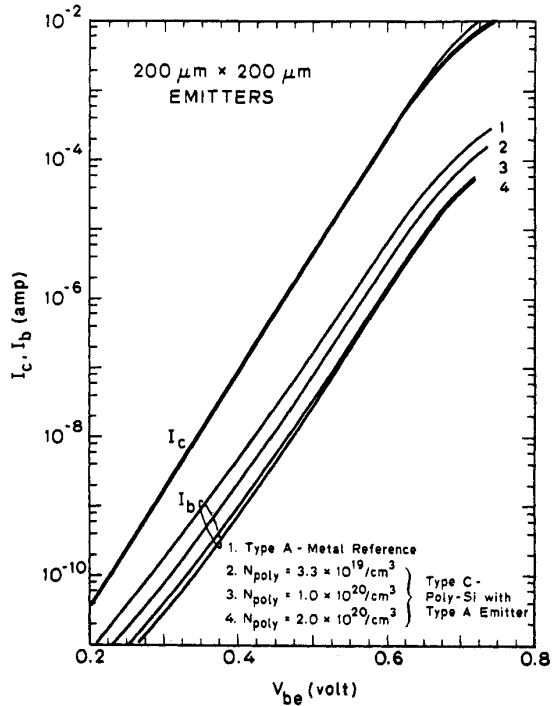


Fig. 2. Substantial gain enhancements can be obtained with polysilicon emitter contacts without the use of intentional chemical oxides.

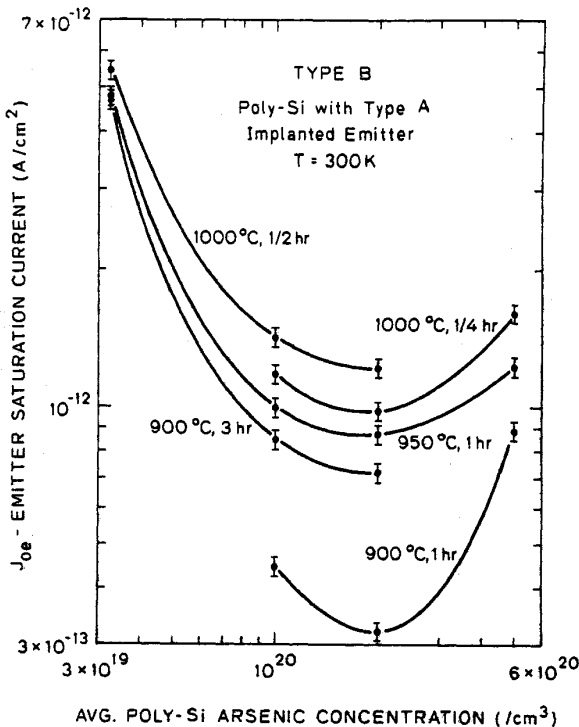


Fig. 3. Type B: J_{oe} dependence on the average arsenic concentration in the polysilicon.

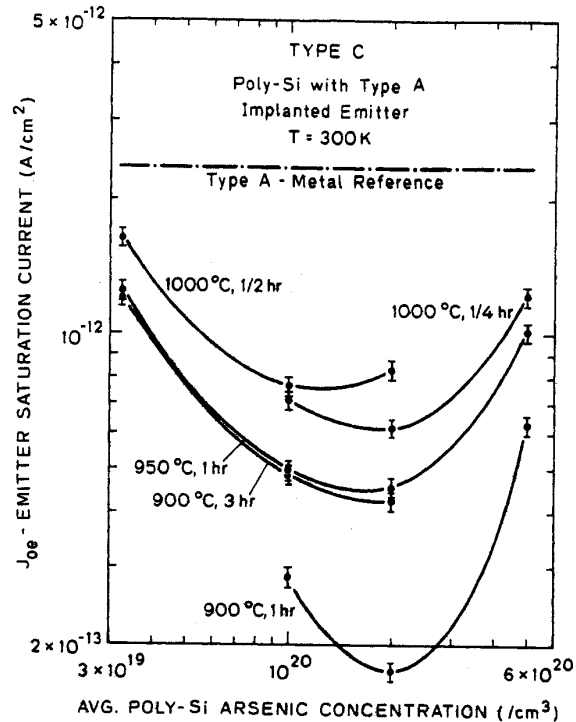


Fig. 4. Type C: J_{oe} dependence on the average arsenic concentration in the polysilicon.

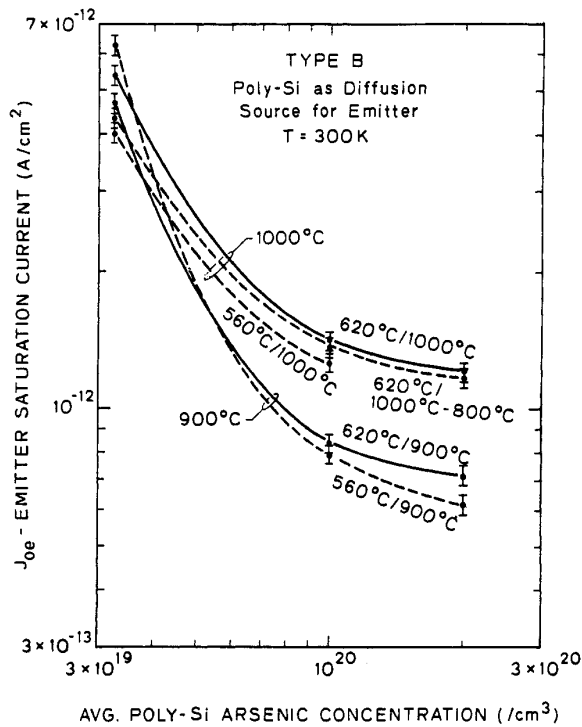


Fig. 5. Type B: J_{oe} dependence on the average arsenic concentration in the polysilicon. (Poly-Si deposition temperature/anneal temperature)

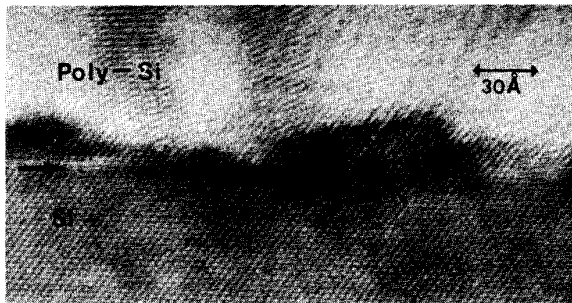


Fig. 8. XTEM micrograph of device given a 1000°C/30min anneal; substantial epitaxial regrowth has occurred (original interface is marked with arrow).

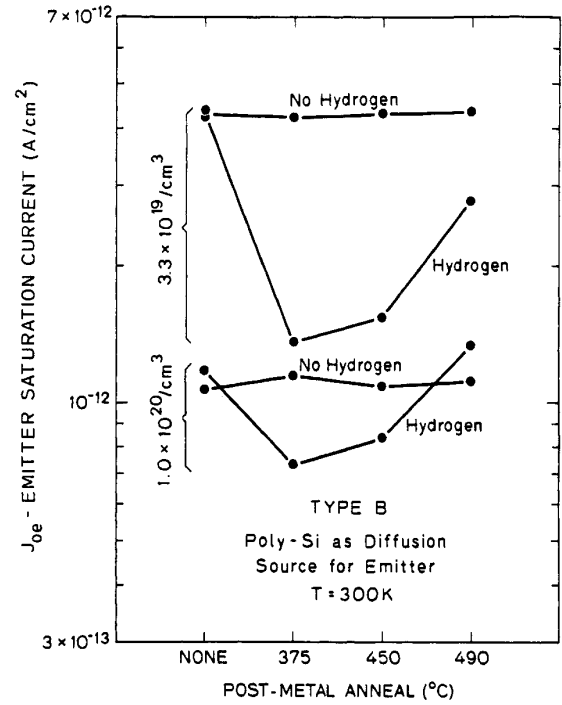


Fig. 6. Type B: Effect of hydrogen passivation on J_{oe} .

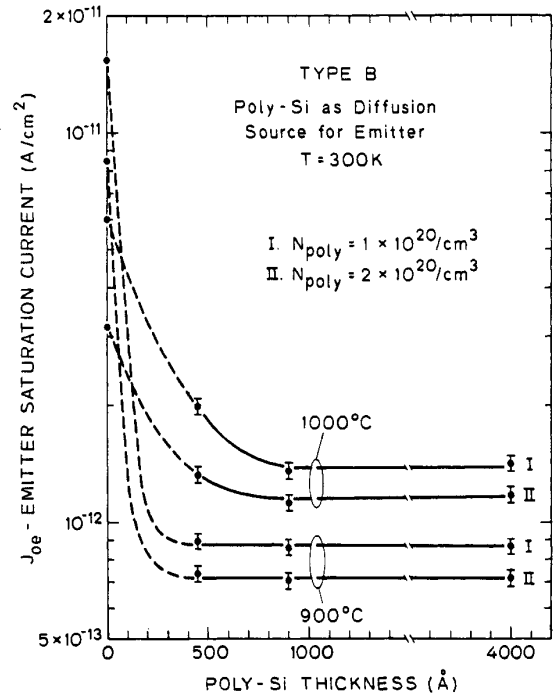


Fig. 9. Type B: J_{oe} dependence on polysilicon thickness (extrapolated to zero polysilicon thickness, i.e., device with metal contact).

