

ELECTRICAL AND MICROSTRUCTURAL INVESTIGATION INTO THE
EFFECT OF ARSENIC EMITTER CONCENTRATION ON THE ENHANCED
GAIN POLYSILICON EMITTER BIPOLAR TRANSISTOR

M C Wilson¹, N Jorgensen², G R Booker² and P C Hunt¹

¹ Plessey Research(Caswell)Ltd., Caswell,
Towcester, Northants, England, NN12 8EQ

² Dept. of Metallurgy & Science of Materials,
University of Oxford, Parks Road, Oxford,
England, OX1 3PH

Introduction

Polysilicon is now widely used in advanced bipolar integrated circuit technology. In these processes polysilicon is deposited directly onto the single crystal and serves as a diffusion source and contacting layer for the emitter region. An advantage of using polysilicon in this way is that transistors exhibit a higher current gain than equivalent conventional transistors. Depending on the surface treatment prior to polysilicon deposition, different interfaces can be formed which control the electrical parameters.

A number of studies have been performed on such structures. This paper forms part of a comprehensive investigation into a proven VLSI, oxide isolated bipolar process with potential high speed applications.

For this study polysilicon emitters were fabricated with the polysilicon/silicon substrate interface as clean as possible and with an intentionally grown very thin interface oxide. For transistors with identical base Gummel numbers, both classes of polysilicon emitter produce a higher current gain than conventional emitters. The gain enhancement is a result of increased emitter efficiency arising, for the former class of device, from the retarded transport of injected minority carriers due to their lower mobility in the polysilicon region. The latter class of device is dominated by the interfacial oxide. The oxide acts as a tunnel barrier to electrical carriers with a low tunnelling probability for holes(1). The collector current critically depends on the barrier height, itself a function of interface oxide thickness(2,3). Furthermore, an interface oxide thicker than 20Å introduces an unacceptably high majority-carrier emitter series resistance(3). Therefore control of the thickness and uniformity of the oxide layer is critical for the success of the device.

Our previous studies(4,5), have determined the thickness of the interface oxide for various methods of preparation and examined the integrity of the oxide during subsequent processing. It was shown that after the polysilicon layer had been given an implantation of $5 \times 10^{15} \text{ cm}^{-2} \text{ As}^+$ ions and an oxidation anneal at 1000°C , the oxide layer became increasingly non-uniform and eventually "balled-up". As this occurred, the underlying single crystal silicon progressively 'penetrated' the oxide layer and grew into the polysilicon layer.

Our more recent studies(6) investigated the effects of anneals at 900, 950 and 1000°C .

The results showed that increasing the anneal temperature caused the oxide layer to be 'penetrated' more rapidly. This structural change was accompanied by a drop of one order of magnitude in the corresponding transistor gains.

In the present study, polysilicon emitter devices have been fabricated with an intentionally grown thin interface oxide and various polysilicon doping levels. The aim was to establish the effect of arsenic concentration on the gain enhancement and device microstructure. The polysilicon was implanted with 5×10^{15} , 1×10^{16} and $2 \times 10^{16} \text{ cm}^{-2} \text{ As}^+$ ions and given an oxidation drive-in at 900°C . The corresponding transistor gains were measured and compared to the detailed microstructure of the polysilicon and interface region.

Microstructural studies were performed by lattice-image TEM of plan view and cross-section specimens in a JEOL 200 CX 200keV TEM after polysilicon deposition and after implantation and drive-in. Emitter series resistance measurements were also made for Si/Cu/Al and PtSi metallisations.

Results

The transistor current gains, h_{FE} , for the devices with and without an interface oxide (i.e. SP and HF) are shown in Fig.1. At a dose of $5 \times 10^{15} \text{ cm}^{-2}$, the gains were 22x and 2x respectively. At a dose of $2 \times 10^{16} \text{ cm}^{-2}$, devices with and without an interface oxide had gains approximately equal at 5x.

Lattice-image cross-section TEM results are shown in Figs.2-4. The interface oxide formed after sulphuric-peroxide immersion and polysilicon deposition was determined to be $10 \pm 1.5 \text{ Å}$. The oxide was uniform and continuous. The polysilicon comprised columnar grains of average diameter, $\sim 500 \text{ Å}$. After $5 \times 10^{15} \text{ cm}^{-2} \text{ As}^+$ ion implantation and 900°C drive-in (Fig.2), the oxide remained continuous though the silicon substrate surface roughened. There was no evidence of break-up of the interface oxide. The average polysilicon grain size, measured at the specimen surface, increased to $500\text{--}1000 \text{ Å}$.

Following $2 \times 10^{16} \text{ cm}^{-2} \text{ As}^+$ ion implantation and drive-in, there was clear evidence of corresponding penetration of the underlying single crystal. An example of one such region is shown in Fig.3. The average polysilicon grain size, at the surface, was $\sim 2000 \text{ Å}$. For comparison the specimen HF dipped prior to polysilicon deposition and implanted with $5 \times 10^{15} \text{ cm}^{-2} \text{ As}^+$ ions is shown in Fig.4. Complete break-up of the interface oxide is evident with

the oxide remaining as spherical particles $\sim 40\text{\AA}$ diameter.

Conclusions

The results indicate that the integrity of an interfacial oxide layer is affected by high arsenic concentrations. An increase in arsenic implant dose from 5×10^{15} to 2×10^{16} caused a break-up in the oxide layer and penetration of the underlying single crystal. Commensurate with the oxide break-up was the decrease in current gain enhancements. The results indicate the gain to be extremely sensitive to the integrity of the thin oxide. The emitter series resistance of such devices was unacceptably high but it has been demonstrated that a significant portion of the series resistance is a result of the contact metallisation. It is concluded that the sensitivity of the gain enhancement to the integrity of the oxide barrier layer and hence to processing conditions, and the high contact resistance to polysilicon will greatly limit enhanced gain polysilicon emitter transistors as a viable VLSI process.

References

- (1) De Graff H.C. and De Groot J.D., (1979) IEEE Trans. Electron. Devices ED-26 No.11 p.1771.
- (2) Yu Z., Ricco B. and Dutton R.W. (1984) IEEE Trans. Electron. Devices ED-31 No.6 p.773.
- (3) Schrabner H., Benna B., Treitinger L and Wieder A.W., (1984) IEDM San Francisco, USA Dec. p.738.
- (4) Duffill J. (1982) 12th ESSDERC (Munich)
- (5) Wilson M.C., Ashburn P., Soerwirdjo B., Booker G.R. and Ward P. (1982) J. de Physique 43 (10) C1-253
- (6) Jorgensen N., Barry J.C., Booker G.R., Ashburn P., and Wilson M.C., (1985) Microsc. Semicond. Materials Conf., Oxford (To be published).

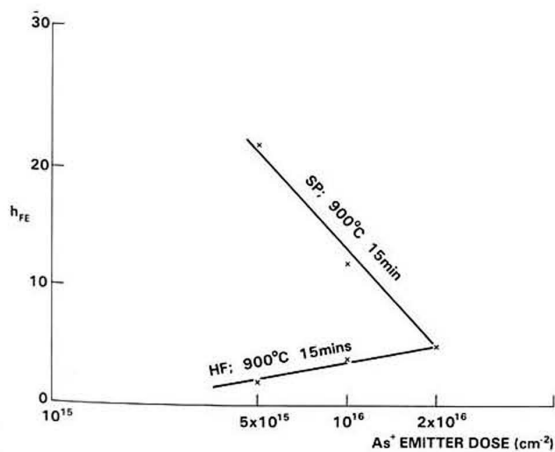


Fig. 1 h_{FE} versus As^+ emitter dose for devices with (SP) and without (HF) an interface oxide layer

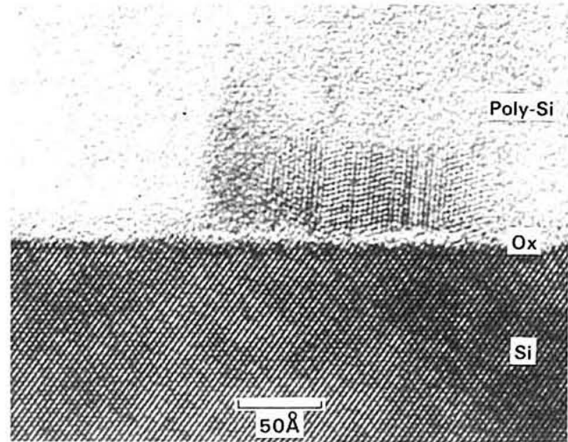


Fig. 2 SP specimen after $5 \times 10^{15} \text{cm}^{-2} As^+$, 900°C 15min

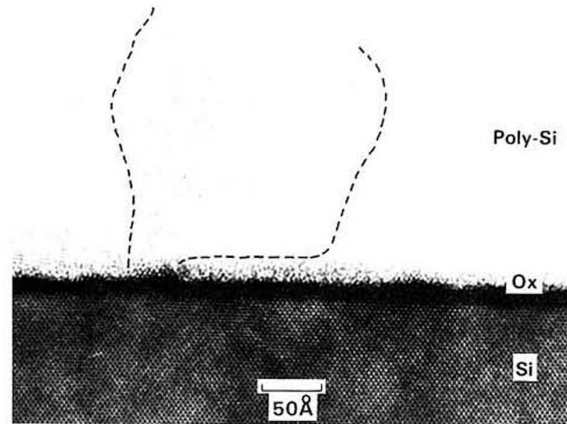


Fig. 3 SP specimen after $2 \times 10^{16} \text{cm}^{-2} As^+$, 900°C 15min
Note oxide break-up and epitaxial re-alignment



Fig. 4 HF specimen after $5 \times 10^{15} \text{cm}^{-2} As^+$, 900°C 15min
Note complete oxide break-up and extensive epitaxial re-alignment