

STUDY OF LATERAL NON-UNIFORMITY AS A FUNCTION OF JUNCTION DEPTH IN ULTRA-SHALLOW JUNCTIONS AND ITS EFFECT ON LEAKAGE BEHAVIOR IN AS-DEPOSITED POLYCRYSTALLINE Si AND AMORPHOUS Si DIODES

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Abstract—Heavily implanted polycrystalline Si films are finding increasing applications as solid diffusion sources, for example, in the formation of ultra-shallow junctions in elevated source/drain metal-oxide-semiconductor field effect transistors and polycrystalline Si emitter bipolar junction transistors. For these applications the dopants are implanted into the polycrystalline Si layer and subsequently diffused into the underlying Si substrate. The diffusion behavior, is however, determined by the evolution of the polycrystalline Si grain microstructure. A large final grain size could lead to laterally more non-uniform and hence leakier junctions. These non-uniformities are lesser for high thermal budget anneals (1100–1150°C, 30 s) than for lower thermal budget anneals (950°C, 30 s) because any doping inhomogeneities in the Si substrate get smeared out as the junction becomes deeper. The junction depth, however, cannot be increased indefinitely from a device viewpoint and a trade-off between leakage current and junction depth has to be made. In this paper, we will study the effect of grain microstructure of ion-implanted as-deposited amorphous Si and as-deposited polycrystalline Si diffusion sources on the diffusion of As and B in the Si substrate, correlate it to the electrical properties of the ultra-shallow junctions formed using this technique.

NOTATION

J_R leakage current density (A/cm²)
 I_R leakage current (A)
 V_R reverse bias voltage (V)
 η ideality factor
 V_{BR} breakdown voltage (V)
 E_A activation energy of leakage current (eV)

INTRODUCTION

Polycrystalline Si has recently been finding application as a solid diffusion source in Very Large Scale Integration (VLSI) to form ultra-shallow junctions in polycrystalline Si emitter Bipolar Junction Transistors (BJTs) and elevated source/drain Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) [1,2]. In these applications, the dopants are implanted into the polycrystalline Si layer at very high doses and subsequently diffused into the underlying silicon substrate to form ultra-shallow junctions. During this step the dopant atoms in polycrystalline Si undergo extremely rapid diffusion in the polycrystalline Si film due to segregation of dopant atoms at grain boundaries which act as “diffusion pipelines” due to a much higher dopant diffusivity in the grain boundaries. The dopant atoms next undergo rapid lateral diffusion along the polycrystalline Si-single crystal Si interface, followed by a much slower

diffusion into the single crystal Si substrate. In polycrystalline-on-single crystal Si systems, the diffusion behavior is therefore influenced by the polycrystalline Si grain microstructure. In particular, the diffusion fronts in the substrate could differ in terms of junction depth and lateral uniformity for as-deposited polycrystalline Si and as-deposited amorphous Si films because the final grain size after annealing is much larger for the as-deposited amorphous Si films. The native interfacial oxide at the polycrystalline Si-single crystal Si interface can also affect the diffusion behavior because of dopant segregation, blockage and pile-up at the interface which is furthermore dependent upon the dopant species. This interfacial oxide can also break up into clusters upon very high thermal budget annealing causing the polycrystalline Si layer to realign with respect to the underlying silicon substrate. The prevalent models [3,4] treat this interfacial oxide as a grain boundary along which rapid lateral diffusion occurs at the interface. This is an over-simplified view, however, and it will be shown later in this paper that it is necessary to consider the lateral spacing between the polycrystalline Si grain boundaries intersecting the interface, in addition to the interfacial oxide, when studying the lateral uniformity of these diffused junctions.

In this paper, the effect of the grain microstructure on the lateral uniformity of the diffusion fronts will be studied by looking at diffusion from as-deposited amorphous Si and as-deposited polycrystalline Si diffusion sources. We will also correlate the diffusion behavior with the leakage properties of these shallow junctions for various rapid thermal and furnace annealing conditions. This is very important to determine the feasibility of using polycrystalline Si as a solid diffusion source to form ultra-shallow junctions. The electrical characterization was performed using diodes fabricated on these heavily-doped polycrystalline Si-on-single crystal Si films following a dopant drive-in anneal.

EXPERIMENTAL PROCEDURE

300 nm thick amorphous Si and polycrystalline Si films were deposited at 580 and 620°C, respectively, on lightly B-doped (100) silicon substrates (10 Ω -cm) in a conventional Low Pressure Chemical Vapor Deposition (LPCVD) reactor after a standard RCA clean. For the diode part of the study, these films were deposited on patterned 300 nm wet oxidized (950°C) Si substrates with window areas ranging from 10⁻⁴ to 10⁻² cm². The films were then implanted with 5 $\times$ 10¹⁵ cm⁻² As or BF₂ at energies of 110 and 70 keV, respectively. After capping the samples with a 50 nm Low Temperature Oxide (LTO) cap to prevent outdiffusion of dopants, the samples were annealed using Rapid Thermal Annealing (RTA) or Furnace Annealing (FA). FA was carried out between 800 and 950°C for various times ranging from 15 to 60 min, and RTA was performed between 950 and 1150°C for various times ranging from 5 to 120 s. For the diodes, Al was sputtered on the front and back, followed by a forming gas sinter at 450°C for 30 min. A cross-sectional schematic of the completed diode structure is shown in Fig. 1. The diffusion behavior was studied using Secondary Ion Mass Spectroscopy (SIMS). The microstructure of the polycrystalline Si films, lateral non-uniformity of the diffused junctions and the morphology of the interfacial oxide were studied using plan-view and Cross-Sectional Transmission Electron Microscopy (XTEM). A concentration-dependent etch of 0.3% HF: 99.7% HNO₃ was used to delineate the lateral non-uniformity of the diffusion front. Reverse bias leakage, breakdown voltage, forward resistance and

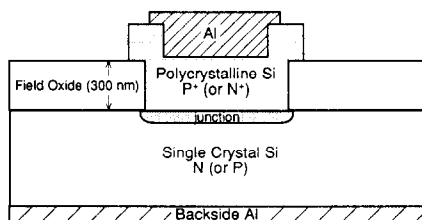


Fig. 1. Schematic diagram showing the cross-section of a polycrystalline Si-on-single crystal Si diode.

ideality factor measurements were performed to electrically characterize the diodes. Temperature-dependent current–voltage (I – V) measurements were also carried out to study the defect injection behavior into the single crystal silicon substrate.

RESULTS AND DISCUSSION

The reverse and forward bias characteristics of arsenic-implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes (diode area = 7.3 $\times$ 10⁻⁴ cm²) after a 30 s anneal at 1100°C are shown in Fig. 2. The reverse bias characteristics show that the leakage current for the as-deposited amorphous Si diodes is approximately 3–5 orders of magnitude larger than the leakage current for the as-deposited polycrystalline Si diodes. In fact, the as-deposited amorphous Si diodes have a leakage current density, J_R = 17 mA/cm² at 10 V reverse bias, whereas the as-deposited polycrystalline Si diodes have a leakage current density J_R = 34 nA/cm² at the same reverse bias. Similar results were obtained for arsenic-implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes subjected to a 30 min FA at 900°C. It is important to note that the leakage current densities for the as-deposited amorphous Si diodes are much higher than state-of-the-art industry leakage current density values of 1–10 nA/cm². However, the breakdown voltages, V_{BR} , for the as-deposited amorphous Si and as-deposited polycrystalline Si diodes are 170 and 200 V, respectively, which agree reasonably well with the theoretical value for our substrate doping, obtained from capacitance–voltage analyses. The forward bias

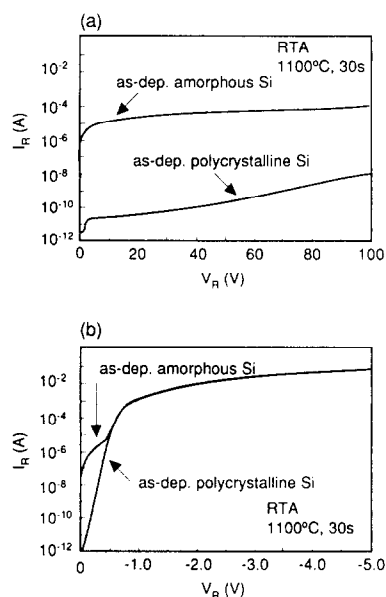


Fig. 2. (a) Reverse bias characteristics; and (b) forward bias characteristics of arsenic-implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes after a 30 s, 1100°C RTA. The diode area is 7.3 $\times$ 10⁻⁴ cm².

characteristics of the as-deposited polycrystalline Si diodes, as shown in Fig. 2(b), are much closer to the ideal diode characteristics than the characteristics for the as-deposited amorphous Si diodes. In fact, the ideality factors, η , for the as-deposited polycrystalline Si and as-deposited amorphous Si diodes have values of 1.04 and 1.86, respectively. This suggests that diffusion current is the dominant conduction mechanism in the as-deposited polycrystalline Si diode whereas generation-recombination in the depletion region dominates the conduction in as-deposited amorphous Si diodes.

The difference in leakage characteristics can be explained by examining the evolution of the polycrystalline Si grain microstructure and its effect on the lateral uniformity of the diffused junctions. It is necessary to study the grain microstructure because As segregates at the grain boundaries where the diffusivity is 3–4 orders of magnitude higher than in the intra-grain regions[5], causing the grain boundaries to act as “diffusion pipelines” transporting dopant atoms to the polycrystalline Si-single crystal Si interface. Therefore, As diffusion depends upon the evolution of the grain microstructure and a larger final grain size would result in less indiffusion from polycrystalline Si into single crystal Si. Figure 3 shows XTEM pictures of arsenic-implanted, as-deposited amorphous Si and as-deposited polycrystalline Si films after a 950°C, 60 s RTA. A lower thermal budget was chosen (950°C, 60 s rather than 1100°C, 30 s as for the diodes) in order to better delineate the lateral non-uniformity of the junction with XTEM. The lateral non-uniformities get smeared out for long diffusion times near the polycrystalline-single crystal Si interface. The lateral uniformity of the diffusion fronts was delineated using a concentration-dependent etch of 0.3%HF:99.7% HNO₃. This etch has a much higher etching rate for n -type doping concentrations above $2 \times 10^{17} \text{cm}^{-3}$, and consequently, the highly doped regions appear brighter in the XTEM picture [6]. From the XTEM pictures, the diffusion front is seen to be very non-uniform laterally for the as-deposited amorphous Si films [Fig. 3(a)], whereas it is quite uniform laterally for the as-deposited polycrystalline Si films [Fig. 3(b)]. The greater lateral non-uniformity of the diffusion front for the as-deposited amorphous Si films results from a larger final grain size in the amorphous films which causes the grain boundaries to be spaced much farther apart along the interface. The reason for this is two-fold. For as-deposited amorphous Si, the density of nuclei for grain growth is less than that for as-deposited polycrystalline Si. Secondly, heavy n -type doping increases the singly and double negatively-charged Si vacancies, and hence, the grain boundary mobility, leading to a higher grain growth rate. This higher grain growth rate in conjunction with a lower density of nuclei results in a larger final grain size after annealing in n -type, as-deposited amorphous Si films [7]. Since the

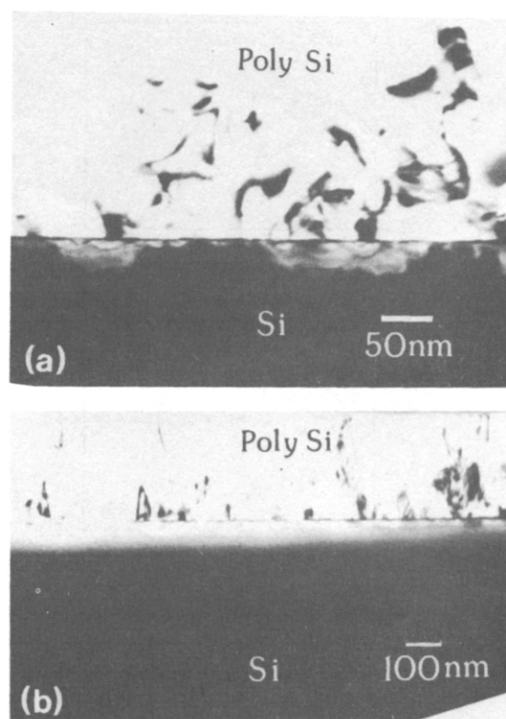


Fig. 3. XTEM micrographs of arsenic-implanted, (a) as-deposited amorphous Si; and (b) as-deposited polycrystalline Si films after at 60 s, 950°C RTA. A concentration-dependent etch was used to delineate the diffusion fronts.

grain boundaries inject point defects into the substrate directly beneath them and can also act as diffusion pipelines, for the high concentration of arsenic segregated at the grain boundaries, to the polycrystalline Si-single crystal Si interface, localized enhanced diffusion occurs beneath the grain boundaries. This localized enhanced diffusion gives rise to doping inhomogeneities in the substrate. The greater spatial separation of the grain boundaries along the interface for the as-deposited amorphous Si films prevents the averaging out of these lateral inhomogeneities. For the as-deposited polycrystalline Si films the final grain size after annealing is much smaller and the grain boundaries are consequently very closely spaced along the interface. This allows any lateral doping inhomogeneities in the substrate to average out.

Unlike for arsenic-implanted diodes, relatively little difference of leakage current is seen between the BF₂-implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes. For example, as shown in Fig. 4(a), after a 1100°C, 30 s RTA the leakage current for as-deposited polycrystalline Si diodes is about 115 nA/cm² at a reverse bias of 10 V, while for as-deposited amorphous Si diodes it is approximately 94 nA/cm² at the same reverse bias. The breakdown voltages are comparable with $V_{BR} = 165 \text{ V}$ for as-deposited polycrystalline Si diodes and $V_{BR} = 145 \text{ V}$ for as-deposited amorphous Si diodes. Under forward bias, for BF₂-implanted

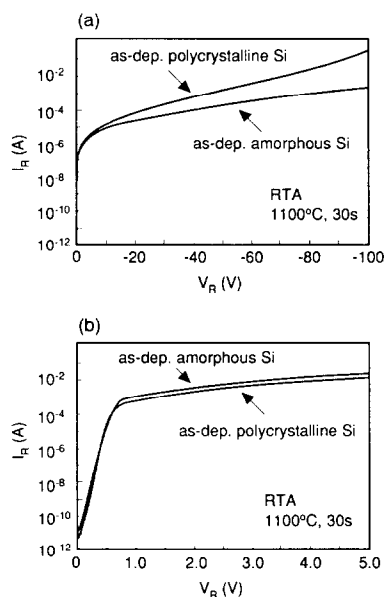


Fig. 4. (a) Reverse bias characteristics; and (b) forward bias characteristics of BF_2 -implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes after a 30 s, 1100°C RTA. The diode area is $7.3 \times 10^{-4} \text{ cm}^2$.

diodes, the characteristics for both as-deposited amorphous Si and as-deposited polycrystalline Si diodes approach ideal diode characteristics [Fig. 4(b)], the ideality factors being 1.1 and 1.2 for the as-deposited amorphous Si and as-deposited polycrystalline Si diodes, respectively.

The relatively small difference between the leakage currents of BF_2 -implanted, as-deposited amorphous Si and as-deposited polycrystalline Si diodes can again be explained by examining the grain microstructure. A comparison of the grain microstructure of BF_2 -implanted, as-deposited amorphous Si and as-deposited polycrystalline Si films after a 950°C, 60 s RTA is shown in Fig. 5. It can be seen that for the case of BF_2 -implanted films both the as-deposited amorphous Si and the as-deposited polycrystalline Si films have a similar final columnar grain microstructure after annealing. This is mainly due to two factors influencing grain growth. The high concentration of F increases the nucleation rate and decreases the primary grain growth rate. Secondly, B doping does not increase the grain boundary mobility significantly because the increase of positively charged vacancies with p -type doping is much less pronounced than the increase of negatively charged vacancies for comparable n -type doping. This is because the energy level of the positively charged vacancy in Si is very close to the valence band edge ($E_v + 0.06$) eV, while the singly and doubly charged vacancies are closer to midgap at ($E_c - 0.44$) eV and ($E_c - 0.11$) eV, respectively. Furthermore, B does not segregate appreciably at the grain boundaries resulting in less impact of the grain microstructure on B diffusion. Consequently, its diffusivity in polycrystalline Si is only 10–50 times

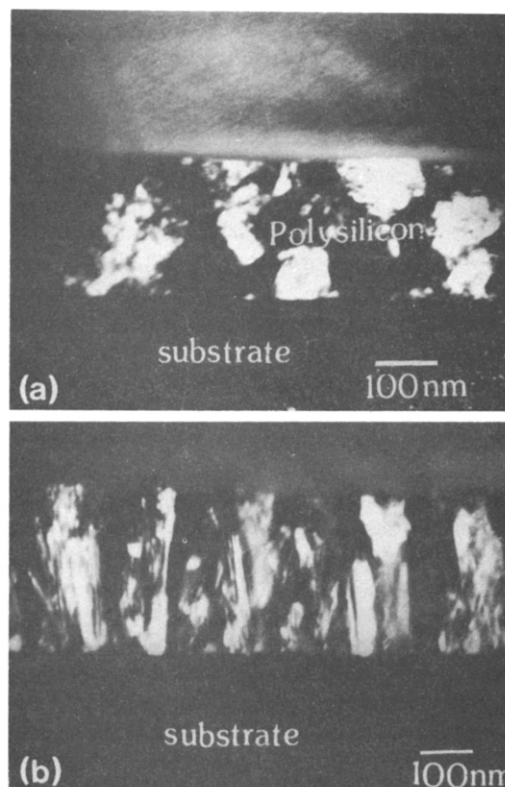


Fig. 5. XTEM micrographs of BF_2 -implanted, (a) as-deposited amorphous Si, and (b) as-deposited polycrystalline Si films after a 60 s, 950°C RTA.

greater than the single crystal Si diffusivity [8]. The small grain size in BF_2 -implanted films, along with the fact that B does not segregate at grain boundaries, results in diffusion fronts that are laterally more uniform than for As. Also, any potential doping inhomogeneities in the silicon substrate that could arise where the grain boundaries intersect the polycrystalline Si–single crystal Si interface, would tend to be laterally averaged out due to the higher diffusivity of B in the Si substrate.

A comparison of the leakage currents of As and BF_2 -implanted, as-deposited polycrystalline Si diodes at a reverse bias of 10 V, after isochronal 30 s RTA is shown in Fig. 6. From the figure, it is seen that for low thermal budget anneals the leakage current for arsenic-implanted diodes is much greater than that for BF_2 -implanted diodes. This difference can again be explained by studying the impact of grain microstructure on the diffusion of these dopants. For low thermal budget anneals the final grain size after annealing is limited, by thermal grooving effects, to the thickness of the polycrystalline Si film [9]. Since As segregates to a greater extent than B at the grain boundaries, especially at low temperatures, the polycrystalline Si film acts as a more efficient diffusion source for As than for B. Therefore, the junction is deeper for arsenic-implanted films, as can be seen in the SIMS profiles shown in Fig. 7. A deeper junction would normally be less leaky because under reverse

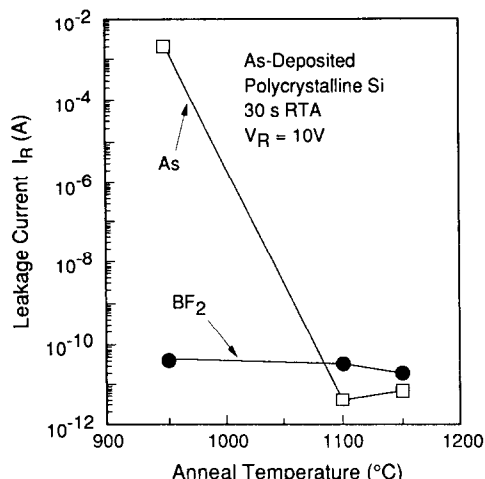


Fig. 6. Comparison of the leakage currents at a reverse bias of 10 V in As and BF_2 -implanted, as-deposited polycrystalline Si diodes after 30 s isochronal RTA. The diode area is $7.3 \times 10^{-4} \text{ cm}^2$.

bias the depletion region at the junction would not be able to probe the high concentration of defects near the polycrystalline Si-single crystal Si interface. However, as seen in Fig. 6 the leakage current for the arsenic-implanted diodes is actually higher even though the junction depth is greater than for BF_2 -implants. We believe the greater lateral non-uniformity of the junctions in the arsenic-implanted diodes is responsible for the higher leakage current since the electric field is enhanced locally in the regions of doping inhomogeneities. Thus, the lateral non-uniformity of the diffused junctions plays a more dominant role in determining leakage current than the depth of the junction. For higher thermal budget anneals the leakage current decreases for both the As and BF_2 -implanted diodes, not only because the junctions become deeper, but also because they be-

come more uniform laterally as any doping inhomogeneities in the substrate get averaged out as the dopants diffuse in further. The decrease is not as significant for BF_2 -implanted diodes because the p^+ junction depth is much greater than the n^+ junction depth (Fig. 6), and this gives rise to increased sidewall leakage current. This was confirmed by looking at longer duration furnace anneals at 900°C . After a 900°C , 30 min anneal $J_R = 10 \text{ nA/cm}^2$ for arsenic-implanted diodes while $J_R = 30 \text{ nA/cm}^2$ for BF_2 -implanted diodes at reverse bias of 10V.

Activation energy measurements were carried out to study the leakage mechanisms in these diodes and to characterize the defect injection behavior from the polycrystalline Si layer. The activation energies of leakage currents as a function of annealing temperature were studied for As and BF_2 -implanted, as-deposited polycrystalline Si diodes in order to study the leakage mechanisms. In an ideal diode, leakage is due to diffusion current which is proportional to the square of intrinsic carrier concentration and, thus, has an activation energy of 1.1 eV. However, if traps are present which give rise to generation-recombination in the depletion region, the leakage current is proportional to the intrinsic carrier concentration, and hence has an activation energy of 0.55 eV. If the depletion region in these diodes formed using the shallow junctions extends to the polycrystalline Si-single crystal Si interface, then the activation energy can be much less than 0.55 eV due to field emission through the grain boundary trap sites. Low activation energies may also be due to impact ionization or tunneling breakdown. Figure 8 shows the activation energies of leakage currents of As and BF_2 -implanted, as-deposited polycrystalline Si diodes as a function of 30 s RTA temperature, at a reverse bias of 10 V. For low temperature anneals, the activation energy is considerably less than 0.55 eV for both As and BF_2 -implanted diodes. Since these measurements were taken at a reverse bias of 10 V, the low activation energy cannot be attributed to avalanche because impact ionization is a breakdown phenomena and should therefore only become important close to the breakdown voltage of $\sim 150 \text{ V}$. Tunneling across the depletion region can also be disregarded because of the low substrate doping. We believe that the low activation energy is due to the fact that the depletion region extends to the polycrystalline Si-single crystal Si interface and field emission through the trap states is occurring. At higher annealing temperatures, the activation energy is around 0.55 eV. This is because the junction depth increases and the depletion region is no longer able to probe the polycrystalline Si-single crystal Si interface. The leakage current in this case is mainly due to generation-recombination current in the depletion region. This explanation is further supported by temperature-dependent ideality factor measurements carried out for arsenic-implanted polycrystalline Si diodes annealed at two different conditions, 950°C for 120 s

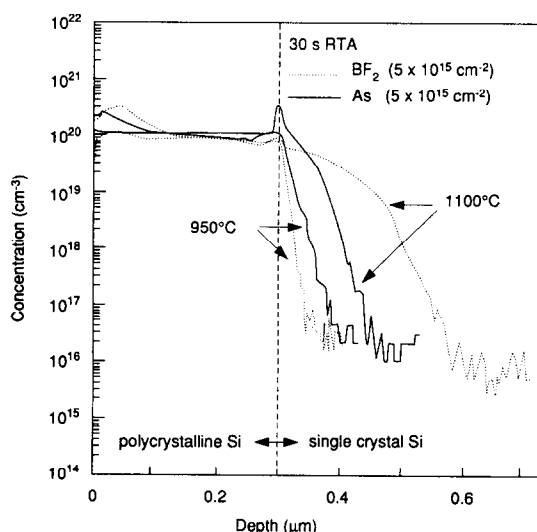


Fig. 7. SIMS profiles of As and B showing the diffusion profiles after a 950°C , 30 s and 1100°C , 30 s RTA.

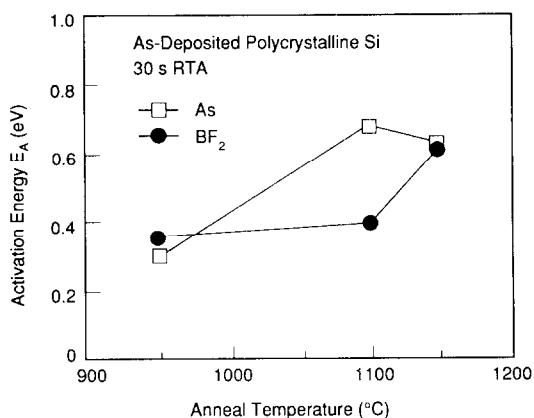


Fig. 8. Activation energy of leakage current at a reverse bias of 10 V in As and BF_2 -implanted, as-deposited polycrystalline Si diodes after 30 s isochronal RTA.

and 1150°C for 30 s, respectively (Fig. 9). The ideality factor for diodes annealed at the lower temperature (950°C , 120 s) is approximately 2 because in this case the depletion region is close to the polycrystalline Si-single crystal Si interface. The interface has a lot of traps and, hence, a lot of recombination takes place in the depletion region. For the diodes annealed at 1150°C for 30 s, the junction is much deeper and far from the polycrystalline Si-single crystal Si interface. For this anneal condition, the ideality factor is ~ 1 , indicating that diffusion current is the dominant transport mechanism. The ideality factor decreases with increasing measurement temperature because the diffusion current component increases more drastically with temperature due to a higher activation energy of 1.1 eV than the generation-recombination current component, which has a lower activation energy of 0.55 eV.

CONCLUSION

In this paper, it has been shown that the lateral non-uniformity of ultra-shallow junctions formed using a heavily-implanted polycrystalline Si solid diffusion source is strongly dependent upon the evolution of the grain microstructure during annealing. This lateral non-uniformity, in turn, determines the leakage behavior of these ultra-shallow junctions. Although, as-deposited amorphous Si is more desirable than as-deposited polycrystalline Si in terms of surface smoothness and sheet resistivity [10], arsenic-implanted, as-deposited polycrystalline Si is a better diffusion source since it gives more laterally uniform junctions which exhibit lower leakage currents. Higher-thermal-budget anneals result in lower leakage currents for both types of diffusion sources because any doping inhomogeneities in the substrate get smeared out, and also because the depletion region cannot probe the polycrystalline Si-single crystal Si interface as the junction gets deeper. No significant difference is observed in the leakage

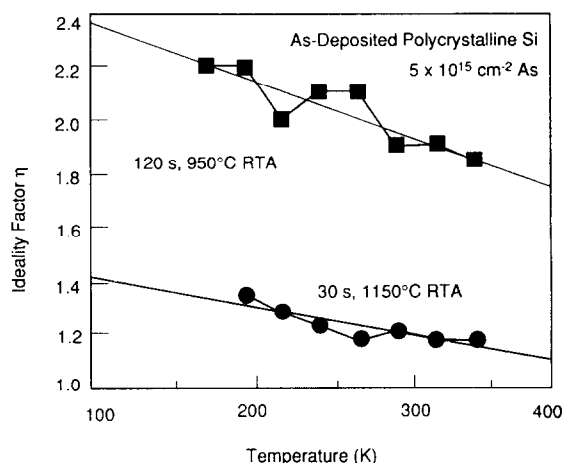


Fig. 9. Plot of temperature-dependent ideality factors in arsenic-implanted, as-deposited polycrystalline Si diodes for two different RTA conditions: 950°C , 120 s and 1150°C , 30 s.

characteristics of BF_2 -implanted, as-deposited amorphous Si or as-deposited polycrystalline Si diodes. This is because of negligible grain growth in BF_2 -implanted polycrystalline Si films, and also due to the higher diffusivity of B in single crystal Si which smears out any lateral doping non-uniformities. The leakage current decreases as the junction becomes deeper not only because of more uniform junctions but also because the depletion region is no longer able to probe the polycrystalline Si-single crystal Si interface. However, from a device viewpoint there is a limit to how deep the junctions can be made, and a trade-off between leakage current and junction depth has to be considered.

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