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Filed on behalf of Mundra Solar PV Limited

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MUNDRA SOLAR PV LIMITED
Petitioners

v.

FIRST SOLAR, INC.
Patent Owner

Case No. IPR2025-01411

**Petition for *Inter Partes* Review of
U.S. Patent No. 9,666,732**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	MANDATORY NOTICES.....	1
	A. Real Parties-in-Interest	1
	B. Related Matters.....	1
	C. Notice of Counsel and Service Information.....	1
	D. Fee for <i>Inter Partes</i> Review	2
III.	 GROUNDS FOR STANDING	3
IV.	 IDENTIFICATION OF CHALLENGES	3
V.	 BACKGROUND	3
	A. Overview of the Technology	3
	1. Solar Cells, PN Junctions, and Doping.....	3
	2. Recombination	6
	3. Passivation by Polysilicon and Thin Oxides.....	7
	B. '732 Patent.....	8
	C. Prosecution History	10
VI.	 THE PRIOR ART	11
	A. Yablonovitch (EX1005)	11
	B. Kwark (EX1017)	16
VII.	 LEVEL OF ORDINARY SKILL	20
VIII.	 CLAIM CONSTRUCTION	21

**IX. GROUND 1: YABLONOVITCH VIEW OF KWARK RENDERS
OBVIOUS CLAIMS 1-4, 6-9 21**

A.	Motivation to Combine	21
B.	Reasonable Expectation of Success	26
C.	Independent Claim 1	30
1.	Element [1.pre] A method of fabricating a solar cell, comprising;.....	30
2.	Element [1.a] providing a substrate, ...	31
3.	Element [1.b] providing an interface passivation layer over the substrate, ...	34
4.	Element [1.c] providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant,.....	41
5.	Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: [1d.1] providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant,.....	47
6.	Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.2] thermally treating the amorphous silicon- containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and, ...	50
7.	Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.3] wherein remaining amorphous silicon-containing	

	compound above the oxide layer defines the passivating film; and, ...	53
8.	Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.4] wherein the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate; and,.....	54
9.	Element [1.e] providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate,.....	62
D.	Dependent Claim 2: The method of claim 1, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.	65
E.	Dependent Claim 3: The method of claim 2, wherein the crystallized passivating film is a transparent film.....	68
F.	Dependent Claim 4: The method of claim 2, wherein the crystallization of the passivating film improves a passivation of the passivating film.	69
G.	Dependent Claim 6: The method of claim 1, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.....	70
H.	Dependent Claim 7: The method of claim 1, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.....	70
I.	Dependent Claim 8: The method of claim 1, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.	71

- J. Dependent Claim 9: The method of claim 1, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant. 73

**IX. GROUND 2: YABLONOVITCH IN VIEW OF KWARK AND BATRA
RENDER OBVIOUS CLAIM 5 73**

- A. Motivation to Combine 73
- B. Reasonable Expectation of Success 76
- C. Dependent Claim 5 77
1. The method of claim 2, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film. 77

X. SECONDARY CONSIDERATIONS.....79

XI. CONCLUSION 80

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	30
<i>Mundra Solar PV Limited v. First Solar, Inc.</i> , C.A. No. 25-462-UNA (D. Del.)	1, 54, 64
Statutes	
35 U.S.C. 102 § 102(a) and (b).....	12
35 U.S.C. § 102(a) and (b).....	16, 18
35 U.S.C. § 103	3, 5
35 U.S.C. § 103(a)	10
35 U.S.C. § 112	11
35 U.S.C. § 312(a)(3).....	1
Other Authorities	
37 C.F.R. § 42.8(b)(1).....	1
37 C.F.R. § 42.10(b)	2
37 C.F.R. § 42.15(a).....	3
37 C.F.R. §42.24(a).....	84
37 C.F.R. § 42.24(d)	84
37 C.F.R. § 42.100(b)	21
37 C.F.R. § 42.104(a).....	3

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 9,666,732 to Schultz-Wittmann (“the ’732 Patent”)
1002	File History of U.S. Patent No. 9,666,732
1003	Declaration of Dr. Sanjay Banerjee, Ph.D.
1004	Curriculum Vitae of Dr. Sanjay Banerjee, Ph.D.
1005	Yablonovitch, E., T. Gmitter, R. M. Swanson, and Y. H. Kwark. "A 720 mV open circuit voltage $\text{SiO}_x:\text{cSi}:\text{SiO}_x$ double heterostructure solar cell." <i>Applied Physics Letters</i> , vol. 47, no. 9 (1 November 1985): 1211-1213. (“Yablonovitch”)
1006	Thomas, J. H., & Feigl, F. J. (1972). <i>Electron trapping levels in silicon dioxide thermally grown on silicon</i> . Journal of Physics and Chemistry of Solids, 33(12), 2197–2216 (“Thomas”)
1007	Kragler, G., Bender, H., Willeke, G., Bucher, E., & Vanhellemont, J. (1994). <i>Characterization of SIPOS films by spectroscopic ellipsometry and transmission electron microscopy</i> . Applied Physics A, 58(1) (“Kragler”)
1008	Crabbé, E. F., Hoyt, J. L., Pease, R. F. W., & Gibbons, J. F. (1988). <i>Electrical characterization of polysilicon-to-silicon interfaces</i> . Materials Research Society Symposium Proceedings, 106, pp. 247-52. © Materials Research Society
1009	Ghoshtagore, R. N. (1975). <i>Silicon dioxide masking of phosphorus diffusion in silicon</i> . Solid-State Electronics, 18(5), 399–406. https://doi.org/10.1016/0038-1101(75)90041-6 (“Ghoshtagore”)
1010	Shimakura, K., Suzuki, T., & Yadoiwa, Y. (1975). <i>Boron and phosphorus diffusion through an SiO_2 layer from a doped polycrystalline Si source under various drive-in ambients</i> Solid-State Electronics, 18(11), 991–997. https://doi.org/10.1016/0038-1101(75)90117-3 (“Shimakura”)

Exhibit No.	Description
1011	RESERVED
1012	RESERVED
1013	May, Gary S., and Simon M. Sze. <i>Fundamentals of Semiconductor Fabrication</i> . John Wiley & Sons, 2004 (“May”)
1014	Hamasaki M., Adachi T., Wakayama S., & Kikuchi M. (1978). <i>Crystallographic study of semi-insulating polycrystalline silicon (SIPOS) doped with oxygen atoms</i> . <i>Journal of Applied Physics</i> , 49(7), 3987–3992 (“Hamasaki”)
1015	Yablonovitch, E., Swanson, R. M., Eades, W. D., & Weinberger, B. R. (1986). Electron-hole recombination at the Si-SiO ₂ interface. <i>Applied Physics Letters</i> , 48(3), 245–247. https://doi.org/10.1063/1.96570 (“Yablonovitch III”).
1016	Gan, J. Y., & Swanson, R. M. (1990, May). <i>Polysilicon emitters for silicon concentrator solar cells</i> . In <i>Conference Record of the Twenty-First IEEE Photovoltaic Specialists Conference</i> (pp. 245–250). Kissimmee, FL, USA: IEEE. https://doi.org/10.1109/PVSC.1990.111625 (“Gan”).
1017	Kwark, Young Hoon. <i>Sipos Heterojunction Contacts to Silicon</i> . Dissertation. Department of Electrical Engineering, Stanford University. Stanford, CA: Stanford University, 1984. (“Kwark”)
1018	Kwark, Y. H., Sinton, R. A., & Swanson, R. M. (1984, December). <i>SIPOS heterojunction contacts to silicon</i> . In <i>Proceedings of the 1984 International Electron Devices Meeting (IEDM)</i> (pp. 742–745). IEEE. https://doi.org/10.1109/IEDM.1984.190832 (“Kwark II”)
1019	Kwark, Y. H., & Swanson, R. M. (1987). <i>N-type SIPOS and poly-silicon emitters</i> . <i>Solid-State Electronics</i> , 30(11), 1121–1125. https://doi.org/10.1016/0038-1101(87)90076-1 (“Kwark III”)

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1022	Green, M. A. (1982). <i>Solar cells: Operating principles, technology, and system applications</i> . Prentice-Hall.
1023	Cook, G., Billman, L., & Adcock, R. (1991). <i>Photovoltaic fundamentals</i> (SERI/TP-220-3957). Solar Energy Research Institute
1024	Neudeck, G. W.; Pak, J. H.; and Bagri, R., “ <i>Poly silicon Contacted Emitter Bipolar Transistors: Fabrication Development</i> ” (1988). Department of Electrical and Computer Engineering Technical Reports. Paper 597.
1025	Wolstenholme, G. R., Jorgensen, N., Ashburn, P., & Booker, G. R. (1987). <i>An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations</i> . <i>Journal of Applied Physics</i> , 61(1), 225-233. https://doi.org/10.1063/1.338861
1026	Patton et. al., “Impact of processing parameters on base current in polysilicon contacted bipolar transistors” (1985). Stanford University Department of Materials Science and Engineering.
1027	Jorgensen, N., Barry, J. C., Booker, G. R., Ashburn, P., Wolstenholme, G. R., Wilson, M. C., & Hunt, P. C. (1985). <i>TEM investigation of the effect of anneal temperature and arsenic concentration on the polysilicon/thin oxide/single-crystal-silicon emitter of a new high-performance bipolar transistor</i> . In A. G. Cullis & D. B. Holt (Eds.), <i>Microscopy of Semiconducting Materials</i> , 1985 (<i>Institute of Physics Conference Series</i> , Vol. 76, pp. 471). Adam Hilger Ltd.

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1028	Wilson, M.C., et. al., <i>Electrical and Microstructural Investigation into the Effect of Arsenic Emitter Concentration on the Enhanced Gain Polysilicon Emitter Bipolar Transistor</i> , (1985) Plessey Research (Caswell), Ltd.
1029	Sah, C. T., Sello, H., & Tremere, D. A. (1959). Diffusion of phosphorus in silicon oxide film. <i>Journal of Physics and Chemistry of Solids</i> , 11(3-4), 288-298. https://doi.org/10.1016/0022-3697(59)90159-8
1030	Tsubo, Y., Komatsu, Y., Saito, K., Matsumoto, S., Sato, Y., Yamamoto, I., & Yamashita, Y. (2000). Phosphorus diffusion from doped polysilicon through ultra-thin SiO ₂ films into Si substrates. <i>Japanese Journal of Applied Physics</i> , 39(10A), L955-L957.
1031	Ni, J., & Arnold, E. (1981). Electrical conductivity of semi-insulating polycrystalline silicon and its dependence upon oxygen content. <i>Applied Physics Letters</i> , 39(7), 554-556.
1032	Thurston, M.O., et. al., “ <i>Diffusion of impurities into Silicon through an Oxide Layer</i> ”, Ohio State University Research Foundation, AD 261201, Contract No. DA-36-039-SC-83874, Final Report, Columbus, Ohio, March 1961.
1033	Wesoff, E. (2011, June 29). <i>SunPower’s Dick Swanson Still Very Much Alive</i> . Greentech Media. https://www.greentechmedia.com/articles/read/sunpowers-dick-swanson-still-very-much-alive
1034	Batra, Shubneesh, Kyle Picone, Keun Hyung Park, Suryanarayana Chattacharya, Sanjay Banerjee, Jack Lee, Monte Manning, and Chuck Dennison. “Study of Lateral Non-Uniformity as a Function of Junction Depth in Ultra-Shallow Junctions and Its Effect on Leakage Behavior in As-Deposited Polycrystalline Si and Amorphous Si Diodes.” <i>Solid-State Electronics</i> , vol. 36, no. 7 (July 1993): 955-960. (“ Batra ”)
1035	Declaration of Sylvia Hall-Ellis, Ph.D.

I. INTRODUCTION

Mundra Solar PV Limited (“Petitioner”) respectfully requests *inter partes* review of claims 1-9 of U.S. Patent No. 9,666,732 (EX1001, “’732 Patent”) and a finding that all challenged claims of the ’732 Patent are unpatentable. The ’732 Patent is directed to a method of manufacturing a solar cell. For each challenged claim, this Petition presents grounds of unpatentability based on references that were not considered by the Office during prosecution of the application that issued as the ’732 Patent. As such, the grounds are at least reasonably likely to prevail, and this Petition should be granted.

II. MANDATORY NOTICES

A. Real Parties-in-Interest

The real party-in-interest under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.8(b)(1) is Petitioner, Mundra Solar PV Limited.

B. Related Matters

The ’732 Patent is currently being litigated in *Mundra Solar PV Limited v. First Solar, Inc.*, C.A. No. 25-462-UNA (D. Del.).

C. Notice of Counsel and Service Information

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Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this petition. Petitioner consents to electronic service by e-mail at the email addresses above and at PH-Mundra-FirstSolarIPR@paulhastings.com.

D. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 50-2613.

III. GROUNDS FOR STANDING

Petitioner certifies pursuant to 37 C.F.R. § 42.104(a) that the '732 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

IV. IDENTIFICATION OF CHALLENGES

Petitioner requests *inter partes* review of claims 1-9 of the '732 Patent under 35 U.S.C. § 103 based on the following grounds:

Ground	Claims	Statute	Prior Art
1	1-4, 6-9	35 U.S.C. § 103	Yablonovitch, Kwark
2	5		Yablonovitch, Kwark, Batra

V. BACKGROUND

A. Overview of the Technology

1. Solar Cells, PN Junctions, and Doping

Solar cells fundamentally operate based on the photovoltaic (“PV”) effect, which describes how when photons of light strike a photovoltaic cell, the energy of a given photon is transferred to an electron in an atom of a semiconductor, allowing the atom to escape from its normal position within the atom and become part of electrical current. To collect this electric current as electricity, PV cells use a built-in electric field to provide the voltage needed to drive the current through an external load. This is done using a p-n junction formed by a p-type semiconductor region

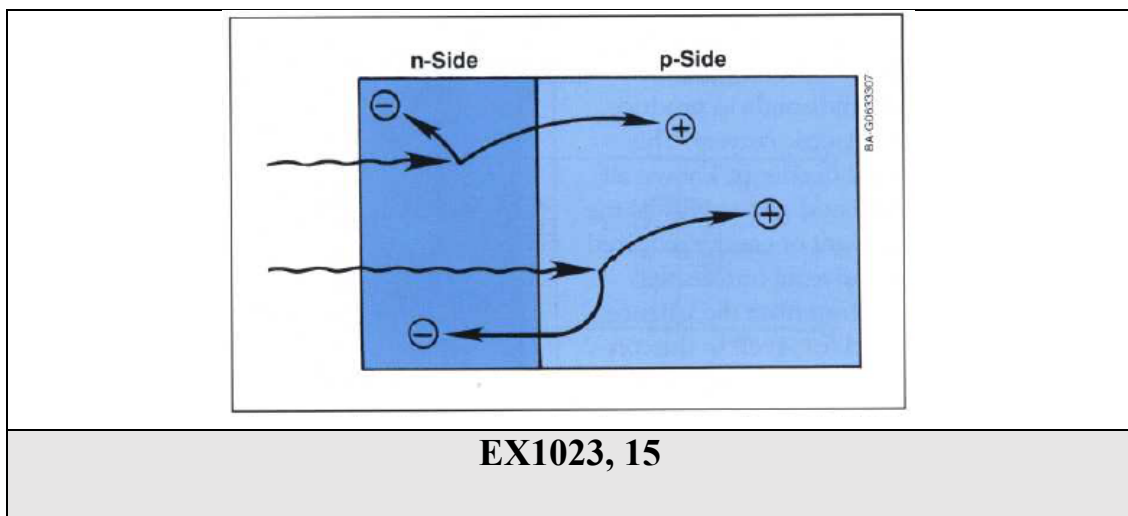
and an n-type semiconductor region, which pushes electrons toward the n-side contact and the holes toward the p-side contact, which drives current through an external load. EX1003, ¶43 (citing EX1023, 14 (describing p-n junction photovoltaic fundamentals)).

In silicon solar cells, the electric field is often created by doping silicon. Doping involves intentionally introducing impurity atoms into the semiconductor crystal lattice to alter its electrical properties. While undoped silicon has no net electric field, adding p-type and n-type dopants create an electric field through the formation of a p-n junction. For instance, adding Group V elements like phosphorus to silicon creates an excess of free electrons, resulting in an n-type semiconductor. Conversely, introducing Group III elements like boron leads to an excess of “holes” (vacant electron states), forming a p-type semiconductor. The interface formed when p-type and n-type semiconductor regions are joined is known as a p-n junction. EX1003, ¶44 (citing EX1023, 12-13 (describing p-n junction photovoltaic fundamentals)). As a result, the electric field drives positive and negative charges in opposite directions, and the movement of charge carriers (through an external circuit) is what defines electricity. *Id.*

Specifically, a p-n junction formed by a p-type semiconductor region and an n-type semiconductor region forms an intrinsic electric field because the electrons in the n-region diffuse are attracted to the p-region, while holes from the p-region

diffuse to the n-region. The electrons and holes recombine, thereby exposing immobile positively charged donors on the n-side and negatively charged acceptors on the p-side in a depletion region. This causes a build-up of opposite charges at the interface of the p-n junction (see forming of “+” and “-” at the junction images below). EX1003, ¶45 (citing EX1023, 14-15 (describing p-n junction photovoltaic fundamentals)). At equilibrium, when all the charge carriers have settled down, a net charge concentration exists on each side of the junction. *Id.* This overpopulation of opposite charges creates an electric field across the interface. *Id.*

As a result of the electric field, as shown below, when sunlight strikes a cell creating charge carriers, the electric field will push new electrons to one side of the junction and new holes to the other side. EX1003, ¶46 (citing EX1023, 15 (describing photovoltaic fundamentals)). This process drives charge carriers in an electric circuit. *Id.*



Thus, the PV cell's foundational operation generates electrons and holes from photons and collect the electrons at the n-type semiconductor region and the holes at the p-type semiconductor region, which generates electricity. EX1003, ¶47.

2. Recombination

If a generated electron and hole recombine before they are collected as current, they contribute nothing to an electrical current. EX1003, ¶48 (citing EX1023, 15 (describing photovoltaic fundamentals)). As a result, the solar cell is less efficient. EX1003, ¶48.

A known way to increase solar cell efficiency is to increase the number of electrons and holes exiting through the electrodes by preventing them from “recombining” before exiting. “Recombination” happens when an electron freed by a photon collides with (and fills) a hole before reaching an electrode, preventing both the electron and hole from contributing to the output current and reducing efficiency. One well-known mechanism of recombination is “surface recombination,” whereby electrons or holes recombine at surfaces or interfaces between different materials, though other recombination mechanisms exist. EX1003, ¶49 (citing EX1023, 55 (describing photovoltaic fundamentals)). In surface recombination, broken bonds at the surface of the silicon substrate or its interface with other materials (e.g., metals) introduce defect states for recombination.

3. Passivation by Polysilicon and Thin Oxides

Passivation refers to the treatment of a material's surface to make it chemically stable and to reduce unwanted reactions or defects. By sweeping electrons and holes away from the device surfaces, the field increases the likelihood that carriers contribute rather than being lost. Polycrystalline silicon (polysilicon) is a semiconductor material composed of numerous small crystalline grains. Its electrical properties are highly dependent on its grain structure, size, and dopant concentration. A specific variant, Semi-Insulating Polycrystalline Silicon (SIPOS), is essentially polysilicon, but additionally incorporates oxygen. SIPOS and polysilicon were widely utilized as passivation films in silicon solar cells due to their unique microstructure and semi-insulating properties. EX1003, ¶50.

A high-temperature treatment or “anneal” is essential for activating dopants by incorporating them into substitutional lattice sites, and for crystallizing SIPOS and polysilicon films. During annealing, amorphous or fine-grained silicon within the deposited SIPOS/polysilicon layer undergoes crystallization and grain growth, leading to the precipitation and enlargement of silicon microcrystalline grains. Also during annealing, a thin interfacial oxide layer can be formed by diffusion of oxygen from the SIPOS film to the SIPOS-Si interface, where they react with Si atoms at the surface leading to the formation of passivating interfacial SiO₂. EX1003, ¶51.

Interfacial oxides were well-known for their advantageous passivation qualities, including their ability to significantly reduce surface recombination at the surface of silicon. The impact of this interfacial oxide on both majority and minority carrier transport was well documented before the relevant time. EX1003, ¶52.

B. '732 Patent

The '732 Patent, entitled “High-efficiency Solar Cell Structures and Methods of Manufacture,” has nine method claims: independent claim 1 and dependent claims 2–9. The '732 Patent is generally directed to a well-known processes for manufacturing a solar cell having a substrate, conductive layer(s), antireflection layer(s), passivation layer(s), and electrode(s). EX1001, Abstract, 1:46-2:31; EX1003, ¶54.

The '732 Patent purports that these layers “provide combined functions of passivation, transparency, sufficient conductivity for vertical carrier flow, the junction, and/or varying degrees of anti-reflectivity.” EX1001, Abstract, 1:46-57. The '732 Patent also describes “improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion.” EX1001, 1:54-57; EX1003, ¶55.

The '732 patent states that “[t]he present invention includes methods of fabricating” several examples of various structures that generally include: “providing a wafer as a central substrate; deposition or growth of interface

passivation layers xx4 and xx6 over the substrate; deposition of conductive layers xx3 and xx7 over the passivation layers: providing thermal treatment; optional deposition of antireflective layers xx2 and xx8 (including possibly a low reflective index layer for a good internal mirror on the back); and providing metallization as electrodes.” EX1001, 18:46-54; EX1003, ¶56

For example, Figure 6 shows a solar cell structure that has been fabricated with a “n- or p-type wafer 65”, “electrically passivating interface layer” 64 and 66, “electrically passivating and conductive film” layers 63 and 67, “transparent and conductive film” layers 62 and 68, “front metal electrode” 61 and “back metal electrode” 69. EX1001, 5:14-6:25, FIG. 6; EX1003, ¶57.

For the fabrication method, the ’732 Patent describes that “a heat treatment” may cause a film to “separate[] into a surface passivating interface layer and a highly doped polycrystalline passivation layer with high transparency.” EX1001, 1:66-2:3, 16:53-17:11 (“a layer deposited in a single process can split into two (or more) layers” when “incorporated oxygen in the amorphous deposited layer migrates toward the silicon interface and a thin oxide can be grown”); EX1003, ¶58.

Specifically, claim 1 recites, *inter alia*, a method of “thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and wherein remaining

amorphous silicon-containing compound above the oxide layer defines the passivating film.” EX1001, 20:5-12 (claim 1, in part).

C. Prosecution History

On April 13, 2016, the Examiner issued a Non-Final Rejection of the pending independent claim under pre-AIA 35 U.S.C. § 103(a) based on U.S. Patent No. 6,821,875 (“Wenham”) in view of WO2007/125903A1 (“Fukushima”), which were both included in Applicant’s IDS filed August 19, 2015. EX1002, 239. The Examiner relied on Fukushima as teaching “providing at least one electrode over the passivating film.” *Id.*, 240.

On July 13, 2016, the Applicant responded to the Non-Final Rejection by amending the pending independent claim to include the following limitations:

wherein providing the interface passivation layer and providing the passivating film comprise:

providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;

diffusing the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and

wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film.

EX1002, 264.

On August 26, 2016, the Examiner issued a second Non-Final Rejection under pre-AIA 35 U.S.C. § 112. EX1002, 306. According to the Examiner, the temporal relationship between the interface passivation layer and the thermal treating step was unclear in light of the specification. *Id.*, 308.

On November 28, 2016, the Applicant responded to the Non-Final Rejection by amending the pending independent claim primarily to recite that it is the “thermally treating” that diffuses the oxygen dopant. *Id.*, 323.

On January 30, 2017, a Notice of Allowance was issued by the Examiner. *Id.*, 337. The patent issued on May 30, 2017. *Id.*, 355.

VI. THE PRIOR ART

The '732 Patent's earliest possible priority date is April 21, 2009, which is the filing date of Provisional Application No. 61/171,194. EX1001, Cover. All prior art in the grounds predates this date.

A. Yablonovitch (EX1005)

Yablonovitch, entitled “A 720 mV open circuit voltage SiO_x:c-Si:SiO_x double heterostructure solar cell”, is a scientific article published in 1985 in *Applied Physics Letters*, a peer-reviewed scientific journal, and was publicly available as of December 1, 1985. See EX1005 at 1; EX1035¹ ¶¶46-53 (in ¶53, concluding that

¹ Dr. Hall-Ellis's declaration (EX1035) refers to the same EX1005 as this Petition.

Yablonovitch was publicly available as of December 1, 1985); EX1003, ¶70. Yablonovitch thus qualifies as prior art under at least 35 U.S.C. 102 § 102(a) and (b).

Yablonovitch is in the field of solar cell design, which is the same field as the '732 Patent. EX1003, ¶71; *see, supra*, Section V.B (Overview of '732 Patent). As shown below in Table II, Yablonovitch discloses a processing sequence (i.e., method of fabrication) for a double heterostructure solar cell. *See* EX1005, Table II; EX1003, ¶71.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

EX1005, Table II

Yablonovitch discloses that a double heterostructure configuration may result a maximal performance of solar cells. EX1005, 1211. Though wide band-gap heterocontact layers may be single crystal and lattice matched to assure high

performance, Yablonovitch notes that such layers are needed only to “be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer.” *Id.*, 1211. Further, due to the larger band gap, there may be quality and disorder issues in the active layer. *Id.*, 1211. Additionally, defect states at the heterocontacts interface states must be passivated. *Id.*, 1211. EX1003, ¶72.

Figure 3 below shows the substrate wafer as the base for other layers during fabrication of the solar cell. EX1005, Fig. 3; EX1003, ¶73.

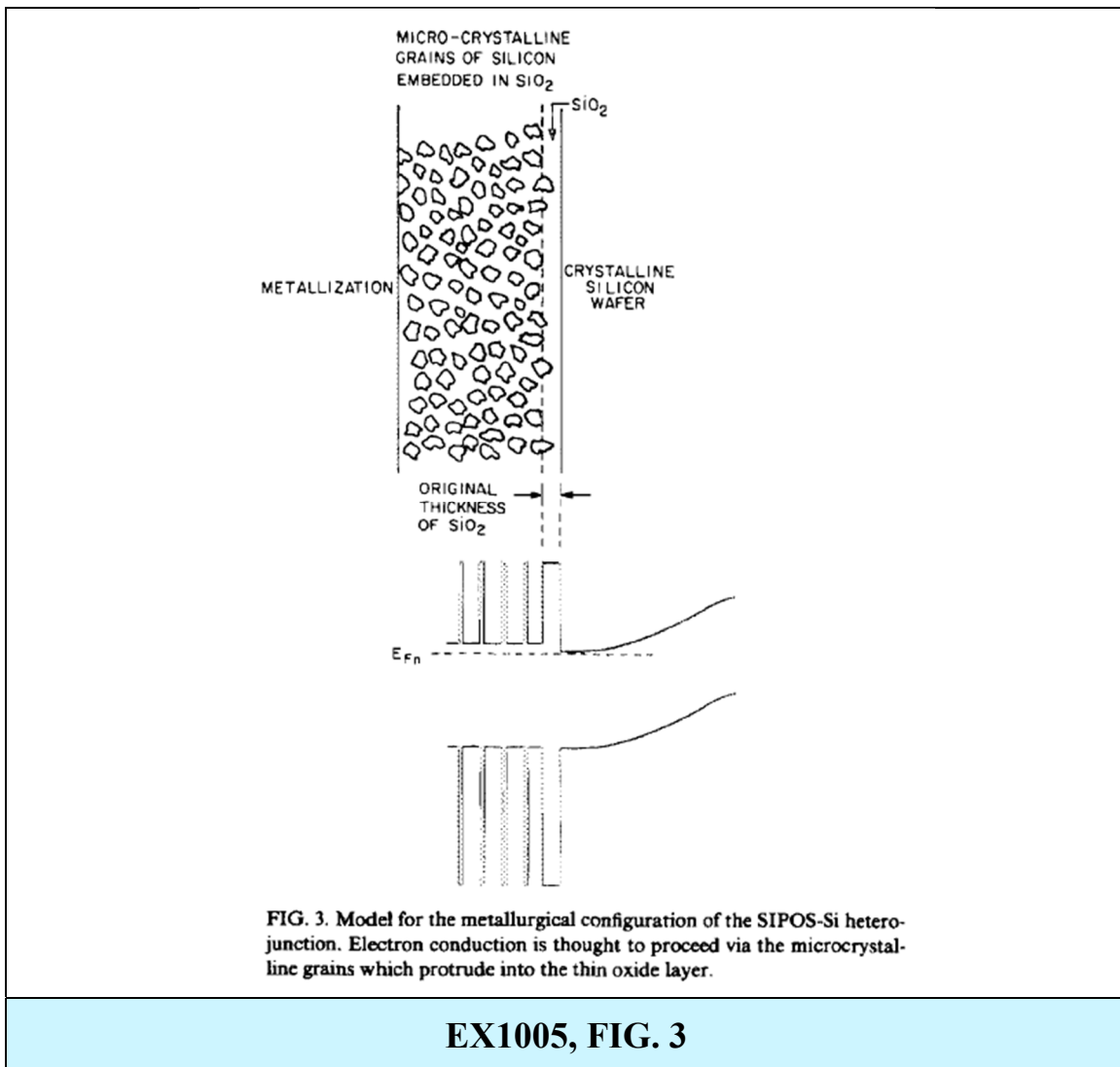
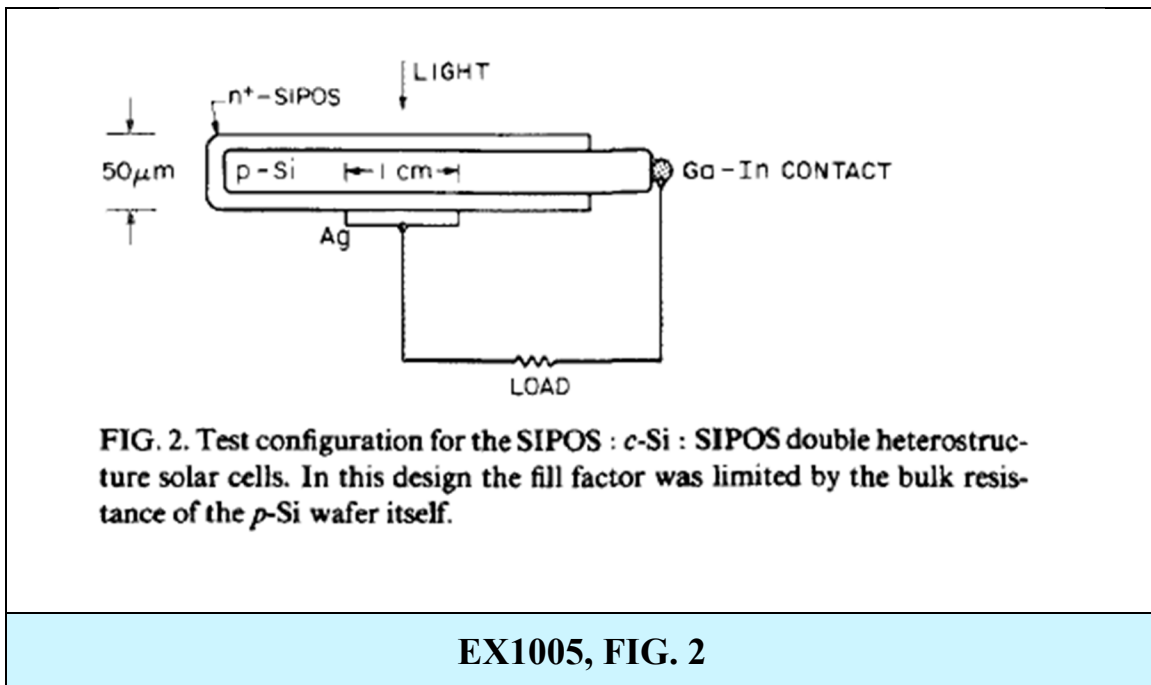


Figure 2 below shows the test configuration of the semiconductor structure for the solar cell. EX1005, Fig. 2; EX1003, ¶74.



According to Yablonovitch, SIPOS (semi-insulating polycrystalline silicon) provides “superior” passivation, preventing electrons and holes from recombining, while allowing current to flow where needed. EX1005, 1211. As such, Yablonovitch provides a solar cell design with better light trapping with 24-25% efficiency. EX1005, 1213; EX1003, ¶75.

In addition, Yablonovitch recognizes that the use of thin interfacial SiO₂ layers further passivates the interface of SIPOS and crystalline silicon, minimizing the recombination and improving overall device performance. EX1005, 1213. These teachings, understood and disclosed decades before the filing of the '732 Patent, highlight the extent to which interface passivation and dopant diffusion techniques were well-known long before the filing of the '732 Patent. EX1003, ¶76.

B. Kwark (EX1017)

Kwark, entitled “SIPOS heterojunction contacts to silicon”, is a doctoral dissertation published in 1984, in Stanford University’s Department of Electrical Engineering and was publicly accessible as of November 20, 1984. *See* EX1017, Cover; EX1035², ¶54-59 (in ¶59, concluding that Kwark was publicly available and accessible as of November 20, 1984); EX1003, ¶77. Kwark qualifies as prior art under at least 35 U.S.C. § 102(a) and (b).

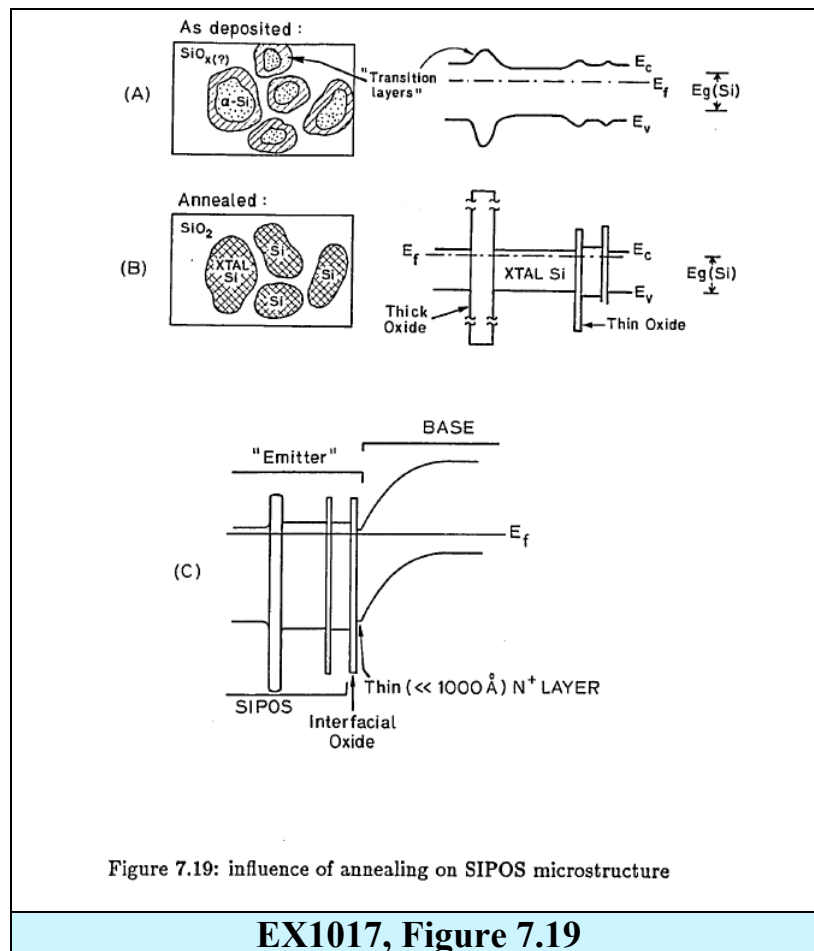
Kwark is in the field of solar cell design, which is the same field as the ’732 Patent. *See* EX1017, Abstract; EX1003, ¶78; *see, supra*, Section V.B (Overview of ’732 Patent).

Kwark explains many of the physical properties of Yablonovitch’s solar cell design in greater detail. For example, Kwark explains how the presence or absence of an interfacial chemical oxide, as well as the thermal treatment, impact the reverse saturation current, J_{oe} , and this impacts cell efficiency. EX1017, 95. Furthermore, Kwark explains the physical properties and phenomenon that result in carrier transport properties in relation to oxide thickness. EX1017, 171. As such, Kwark discloses how SIPOS with an interfacial oxide can yield solar cells with high open circuit voltage and efficiency, as well as insights for implementing complex interface

² Dr. Hall-Ellis’s declaration (EX1035) refers to the same EX1017 as this Petition.

design considerations to better optimize the thin oxide used in solar cells. EX1017, 178; EX1003, ¶79.

More specifically, Kwarck discloses “an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{oe} reduction.” EX1017, 121. Kwarck Figure 7.19 further discloses the SIPOS crystallizes during subsequent annealing instead of being crystallized as-deposited. EX1017, FIG. 7.19; EX1003, ¶80.



Many of the teachings of Kwark regarding SIPOS and interfacial oxides were published in peer-reviewed journals, including Kwark II – *SIPOS heterojunction contacts to silicon* (see EX1018) – in 1984, and Kwark III – N-type SIPOS and poly-silicon emitters (see EX1019) – in 1987. EX1003, ¶81.

C. Batra (EX1034)

Batra, entitled “Study of lateral non-uniformity and function of junction depth in ultra-shallow junctions and its effect on leakage behavior in as-deposited polycrystalline Si and Amorphous Si Diodes,” is a scientific article published in the July 1993 issue of *Solid-State Electronics*, a peer-reviewed scientific journal and was publicly available and accessible as of July 14, 1993. See EX1034, 955; EX1035³ ¶60-67 (in ¶67, concluding that Batra was publicly available as of July 14, 1993); EX1003, ¶82. Batra thus qualifies as prior art under at least 35 U.S.C. §§ 102(a) and (b).

Batra is in the field of polycrystalline Si films, which are present in solar cells and addresses the same problems as the is the '732 Patent. EX1034, 955; EX1003, ¶83; see, *supra*, Section V.B.

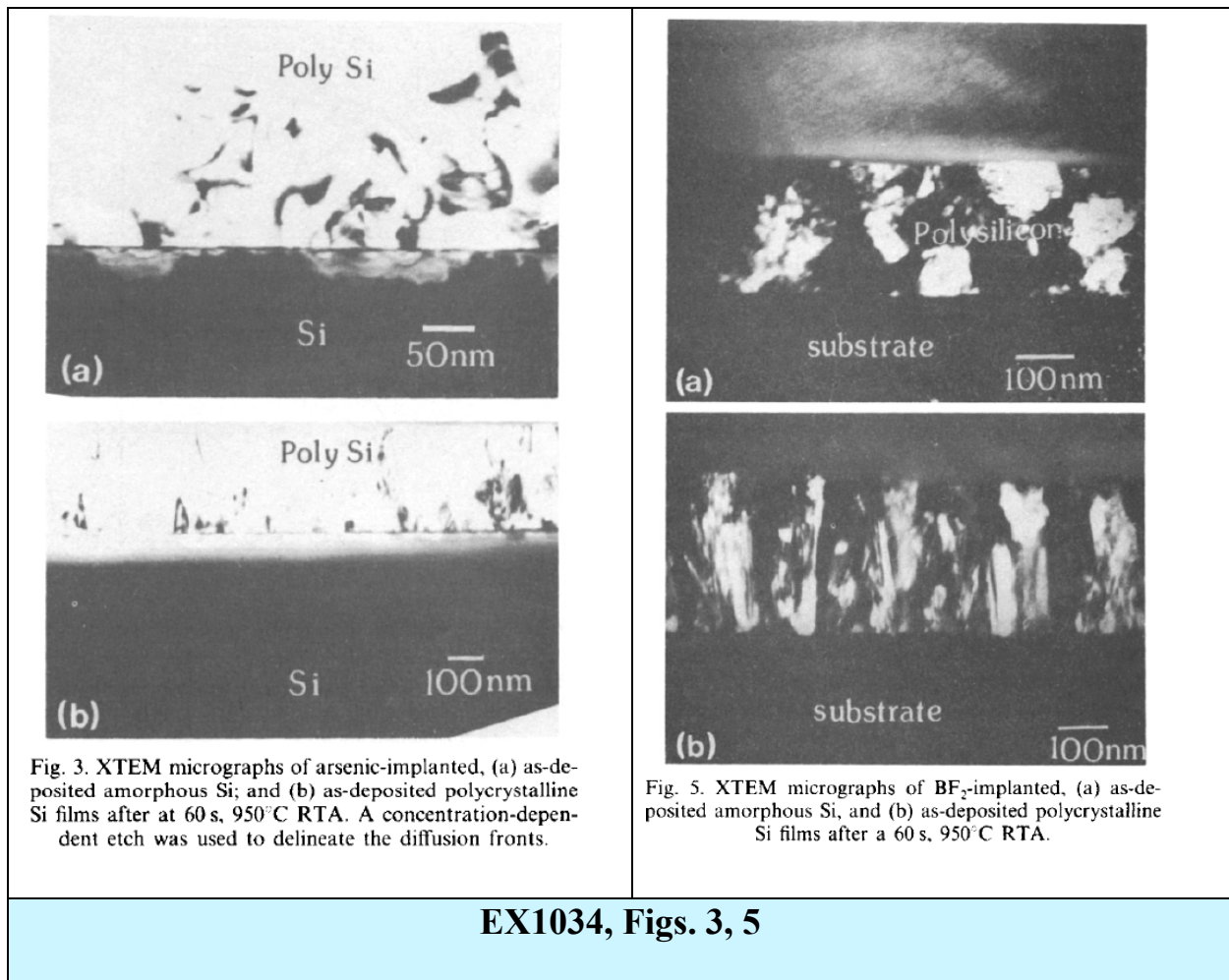
Batra recognizes that “heavily implanted polycrystalline Si films are finding increasing applications as solid diffusion sources.” EX1034, 955. As such, Batra

³ Dr. Hall-Ellis’s declaration (EX1035) refers to the same EX1034 as this Petition.

explains the importance of determining the effect of the interface passivation layer (“SiO₂”) on the substrate (“crystalline silicon wafer”) during anneal. EX1034, 955; EX1003 ¶84.

Batra’s findings about nonuniformity in junctions apply to interface passivation layers given that Batra teaches how annealing changes the crystal structure and dopant distribution such that higher-temperature or longer anneals lead to a more uniform junction, which resolves the underlying problem crystallization or re-crystallization of the passivating film since the even dopant distribution reduces p-n junction lateral non-uniformity. EX1034, 955; EX1003 ¶85.

Batra’s Figures 3 and 5 reproduced below illustrate that the crystallization of the polysilicon layer does not to create damage in the substrate and vice versa. EX1034, Figs. 3, 5; EX1003, ¶86



VII. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art in the '732 Patent's field of solar cell design or manufacture by 2009 ("POSITA") would have been someone with a bachelor's degree involving the disciplines of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field. Alternatively, a person with less

formal education but additional relevant practical experience, or vice versa, would also qualify as a person of ordinary skill in the art. EX1003, ¶67.

VIII. CLAIM CONSTRUCTION

The Board construes the claims “using the claim construction standard that would be used” in district courts. 37 C.F.R. § 42.100(b). This Petition establishes the prior art meets each claim limitation under any reasonable construction.⁴ Therefore, no express construction is necessary.

IX. GROUND 1: YABLONOVITCH VIEW OF KWARK RENDERS OBVIOUS CLAIMS 1-4, 6-9

A. Motivation to Combine

A POSITA would have found it obvious to apply the teachings of Kwark to Yablonovitch. Yablonovitch and Kwark are analogous art because each is in the same field of endeavor as the '732 Patent —solar cell design. *See* EX1005, Abstract, 1211; EX1017, 1-5; EX1001, Abstract; EX1003, ¶88; *see, supra*, Sections VI.A. and VI.B. (Overview of Yablonovitch and Kwark). Each is reasonably pertinent to the problems of efficiencies of solar cell designs. *Id.*

⁴ Petitioner reserves the right to argue alternative constructions in other proceedings, including that the claims are indefinite where such a defense is available.

Yablonovitch and Kwark address the critical role of polysilicon/SIPOS interface with silicon substrates and thin interfacial oxides in controlling carrier transport and device efficiency. EX1003, ¶88.

The combination of Yablonovitch and Kwark requires no modification to Yablonovitch – Kwark’s teachings supply details about the physical phenomenon occurring during Yablonovitch’s process that, while understood by a POSITA, Yablonovitch omitted. As such, Kwark provides context to Yablonovitch’s process. A POSITA would have been motivated to look to Kwark to understand the physical phenomenon occurring during Yablonovitch’s process, particularly in its formation of the critical interfacial region of the SIPOS layer and the silicon substrate, which would be necessary to determine implementation details and design considerations omitted from Yablonovitch. These considerations would have been important to a POSITA looking to implement and optimize Yablonovitch’s process because others taught and understood that there were important design considerations for forming interfacial oxides that affected the performance of the solar cell. EX1003, ¶89.

Yablonovitch discloses a SIPOS-Si heterojunction solar cell design and provides important explanation on the basic mechanism for interface passivation, explaining that “the interface states at the heterocontacts *must be passivated*.” EX1005, 1211. In order to do so, Yablonovitch teaches that for its solar cell design, “[t]he interface states between SIPOS and crystalline silicon (c-Si) seem to be

passivated as well as the high quality interface between thermally grown SiO₂ and c-Si.” EX1005, 1211. In other words, Yablonovitch recognizes that thin interfacial SiO₂ oxides passivate the interface of SIPOS and crystalline silicon. EX1003, ¶90.

Yablonovitch also recognizes that interfacial oxides “frequently occurs inadvertently,” but does not analyze in detail the ways in which interfacial oxides may form. EX1005, 1212. Yablonovitch further recognizes that the functioning of the interfacial oxide structures is “complex,” but omits a complete analysis of the physical phenomenon underlying formation of interfacial oxides. Knowledge of such physical phenomenon would have been sought after by a POSITA in order to implement Yablonovitch, particularly in order to implement Yablonovitch and its SIPOS emitter according to any given design considerations, such as desired electrical and optical characteristics of the solar cell. EX1003, ¶91. Kwark provides such knowledge of physical phenomenon. For example, Kwark explains how the presence or absence of an interfacial chemical oxide, as well as the thermal treatment impact the reverse saturation current, J_{oe} , which impacts cell efficiency. EX1003, ¶91.

For example, “[d]ifferential tunneling probability between electrons and holes... [is] very sensitive to oxide thickness.” EX1005, 1213 (emphasis added). It is therefore important to know the physical nature of an interfacial oxide in a solar cell to optimize its properties for particular design considerations. EX1003, ¶92.

While Yablonovitch generally acknowledges that oxide thickness plays a crucial role in carrier transport properties, Kwark explains further the physical properties and phenomenon that result in such properties in relation to the oxide's thickness. In particular, Kwark provides explanation and experimentation data that describe and quantify the trade-off between current density (J_o) and contact resistivity. EX1017, 141-84. These properties represent a known design consideration that a POSITA would optimize for a given application by tailoring the interfacial oxide thickness. EX1003, ¶93 (citing EX1008, 250 (“there is a trade-off between the emitter resistances and the base current... [t]he reason for this trade-off is intuitively clear: if the native oxide layer is continuous and blocks hole transport, it also impedes the transport of electrons”)). A thicker interfacial oxide will provide better passivation qualities but suffer from higher resistance, while a thinner interfacial oxide will provide worse passivation qualities but will benefit from lower resistance. EX1003, ¶93.

As Kwark explains, SIPOS with an interfacial oxide can yield solar cells with high open circuit voltage and efficiency. EX1017, 178; EX1003, ¶94.

A POSITA would understand that optimizing these parameters are crucial for achieving the desired balance between low contact resistance and high open circuit voltage, which has concomitant benefits for efficiency. EX1003, ¶95.

Yablonovitch and Kwark are highly complementary, as Kwark provides insights regarding complex interface design considerations as disclosed by Yablonovitch. The combined teachings of Yablonovitch and Kwark would provide a POSITA a comprehensive understanding of the interface engineering at work in Yablonovitch's process, moving beyond Yablonovitch's general disclosure of the "complex" processes affecting the structure. EX1005, 1213; EX1003, ¶96. With knowledge of such design considerations, as taught by Kwark, a POSITA would have been able to optimize the thin oxide to the design constraints of any given application. EX1003, ¶96.

A POSITA would have had the skills, knowledge and rationale to design and implement Kwark's teachings in Yablonovitch's process that would have predictably resulted in optimized parameters to form the interfacial oxide. EX1003, ¶97. A POSITA would have considered fabrication parameters, such as anneal time, anneal temperature, and dopant concentration to facilitate such an optimization. EX1017, 3; EX1003, ¶97. As one example, the resulting optimization, would have resulted in tailored contact resistivity (ρ_c) and emitter saturation current density (J_o) to meet the design constraints of a particular application for the solar cell. EX1017, 3; EX1003, ¶97.

It would have been well within the skill of a POSITA in 2009 to consider the design benefit/tradeoffs in designing/implementing such modification. EX1003,

¶98. Here, guided by Kwark, a POSITA would have balanced tradeoffs between contact resistivity (ρ_c) and emitter saturation current density (J_o) to warrant consideration and implementation of the above modification. EX1017, 3; EX1003, ¶98. Moreover, a POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (*e.g.*, Kwark's implementation details) and thus would have had the motivation and reasonable expectation of success in implementing them in Yablonovitch's process. EX1017, 3; EX1003, ¶98. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable result of optimized contact resistivity (ρ_c) and emitter saturation current density (J_o). (*Id.*). See EX1017; EX1003, ¶98.

B. Reasonable Expectation of Success

A POSITA would have had a reasonable expectation of success in implementing the combination of Yablonovitch and Kwark. EX1003, ¶99.

The art was mature and predictable. Fabrication of polysilicon/SIPOS emitters and silicon oxide layers for semiconductor devices (including solar cells), including techniques for dopant diffusion, thermal annealing, and interface engineering, was a mature and well-understood discipline well before the relevant timeframe (2009). The behavior of thin oxide layers under high-temperature processing, especially in the presence of dopants, was an area of extensive research and optimization. EX1003, ¶100 (citing EX1006 (recognizing in 1971 the "intense

interest” in “thin films of silicon dioxide due to their extensive use as passivating and insulating layers in the silicon planar technology,” specifically due to the “interface states” formed between silicon dioxide and silicon); EX1020, 892 (noting Kwark’s SIPOS structure findings as Ph.D. student to be a promising direction for the solar industry)). The keen interest and research activity in the subject matter more than 20 years before the effective filing date of the ’732 Patent highlights the degree to which the subject matter had been researched and characterized decades before 2009. EX1003, ¶100.

There was a comprehensive and mature understanding of the complex polysilicon/SIPOS interface with silicon and the role of interfacial oxides, which indicates a predictable art where combining known phenomena would yield anticipated results. *See, e.g.*, EX1007-10, 1014-19, 1024-32; EX1003, ¶101. The concentration of research on polysilicon/SIPOS emitters, evidenced by these publications, further supports the robustness and predictability of these phenomena. Kwark’s findings, which for example, explain the effects of oxygen dopant on interfacial oxide formation demonstrates a systematic and predictable understanding of these phenomena. *See generally* EX1017. This strong corroborating evidence from the above multiple independent studies reinforces the predictability and reliability of the phenomenon. EX1003, ¶101.

A POSITA would have considered the Yablonovitch / Kwark combination to be simply an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). EX1003, ¶102.

The understanding of the trade-offs, such as between contact resistivity (ρ_c) and emitter saturation current density (J_o) further support a high expectation of success. EX1003, ¶103 (citing EX1016, 245; EX1017, 166; EX1024, 23 (studies showing that resistivity and emitter saturation current density influence oxide thickness and oxide break-up)). A POSITA would understand that by controlling dopant concentration and other conditions (such as annealing), one could predictably influence the oxide thickness and degree of oxide break-up, and thus optimize the balance between achieving low contact resistance (for efficient carrier flow) and maintaining high emitter efficiency by providing interface passivation and reducing J_o). EX1003, ¶103. Such routine experimentation would have been a matter of engineering optimization within known parameters, not discovery of new phenomena. EX1003, ¶103.

Applying the teachings of Kwark to Yablonovitch's SIPOS emitter structure would not be unworkable, lead to undesirable results, or otherwise discourage the proposed combination. Instead, these references build on each other's teachings of

interface engineering for improved device performance. The results are presented as a beneficial outcome for achieving low-resistance contacts and efficient carrier transport, which indicates that a POSITA would actively pursue conditions that optimize this oxide thickness and break-up, to achieve desired device characteristics. EX1005, 1211 (discussing “good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells”); *see also* EX1017, 62 (disclosing use of lower oxygen content SIPOS films whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices); EX1003, ¶104. Identifying negatives (in addition to positives) in trade-offs (*e.g.*, between contact resistivity (ρ_c) and emitter saturation current density (J_o)) are design considerations for optimization, not teachings away from fundamental concepts such as oxide thickness and break-up. A POSITA would understand that essentially any design decision in engineering comes with costs and benefits (*i.e.*, positives and negatives), and that weighing those costs and benefits is part of the design process. EX1003, ¶104.

Combining Yablonovitch and Kwark as described herein would have been well within the level of ordinary skill in the art. EX1003, ¶105. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply have been the combination of well-known prior art steps

in solar cell and semiconductor fabrication to yield predictable results. Likewise, implementing Yablonovitch's interfacial oxide according to the design considerations of Kwark would have been a simple use of a known technique to improve similar devices (Yablonovitch's process) in the same way. It is nothing more than applying a known technique to a known device ready for improvement to yield predictable results. EX1003, ¶105; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

C. Independent Claim 1

1. Element [1.pre] A method of fabricating a solar cell, comprising;

To the extent limiting, Yablonovitch discloses the preamble of claim 1.⁵ EX1003, ¶107-108.

As shown in the following limitations of claim 1, Yablonovitch teaches **[a] method of fabricating a solar cell**. EX1003, ¶107.

Yablonovitch teaches a fabrication method for “[a] 720 mV open circuit voltage SiO_x:c-Si:SiO_x double heterostructure **solar cell**.” EX1005, Cover. As shown below in Table II, Yablonovitch discloses the processing sequence (i.e.,

⁵ Petitioner does not acquiesce that the preambles are limiting.

method of fabrication) for the double heterostructure solar cell. *See generally* EX1005, Table II; EX1003, ¶108.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^\circ\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^\circ\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^\circ\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

EX1005, Table II

2. Element [1.a] providing a substrate,

Yablonovitch discloses this limitation. EX1003, ¶109-113.

Yablonovitch teaches a “crystalline silicon wafer” as **a substrate** for the **solar cell**. EX1005, 1211 (discussing the “silicon wafer”), 1212 (discussing properties of the silicon wafer and showing the p-Si silicon wafer in Figure 2), 1213 (showing the “crystalline silicon wafer” in Figure 3). A crystalline silicon wafer is the foundation layer, or **a substrate** on which the rest of the solar cell is built. Table I below summarizes the material properties of the wafer. EX1003, ¶110.

TABLE I. Properties of silicon wafer material.

Orientation	$\langle 100 \rangle$
Resistivity	$0.5 \Omega \text{ cm } p\text{-type}$
Doping concentration	$2.5 \times 10^{16} / \text{cm}^3$
Bulk minority-carrier lifetime	$450 \mu\text{s}$
Minority-carrier mobility	$700 \text{ cm}^2 / \text{Vs}$
Diffusion length	0.9 mm
Thickness	$50 \mu\text{m}$
J_0 of n^+ -SIPOS heterocontact	10^{-14} A/cm^2 at 27°C
Emitter Gummel number	$3.3 \times 10^{15} \text{ s/cm}^4$

EX1005, Table I

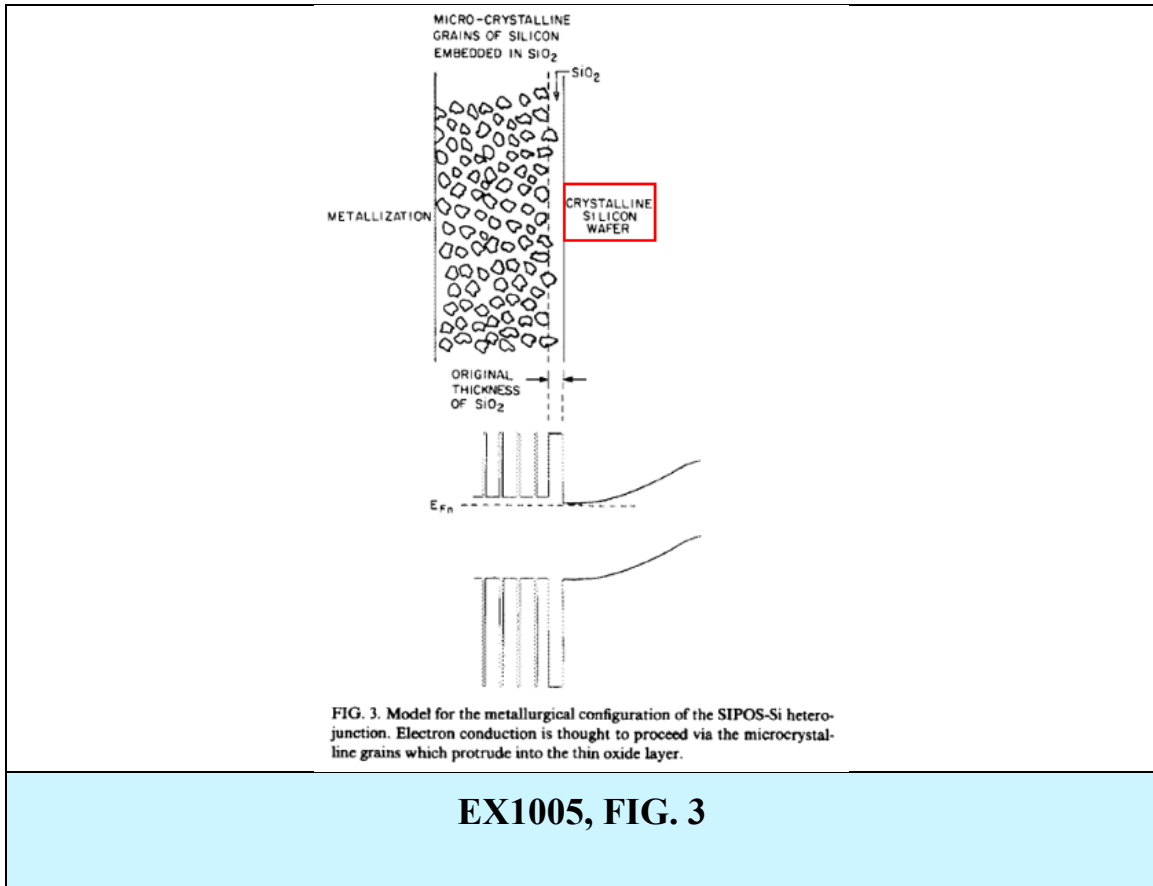
According to the process sequence such as in Table II, Yablonovitch uses a “float-zone p-type silicon wafers of $0.5 \Omega \text{ cm}$ resistivity... [which] were chemically thinned to $50 \mu\text{m}$ ” as a **substrate** for fabricating the solar cell, as shown in Table II. EX1005, 1212; EX1003, ¶111.

TABLE II. Processing sequence.

- 1. Thin silicon wafers to $50 \mu\text{m}$ in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650°C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900°C .
9. Anneal for 15 min.
10. Ramp furnace down to 450°C .
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

EX1005, Table II

Figure 3 below shows the wafer as the base for other layers during fabrication of the solar cell, meaning that the wafer is **a substrate**. EX1005, Fig. 3; EX1003, ¶112.



Further, Figure 2 shows the test configuration of the semiconductor structure for the solar cell. EX1005, Fig. 2. Here, the wafer is **a substrate** that acts as a foundation layer. EX1003, ¶113.

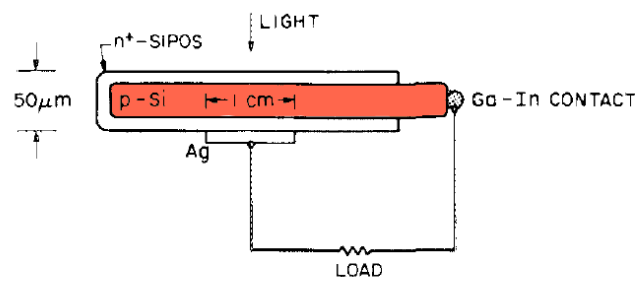


FIG. 2. Test configuration for the SIPOS : c-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the p-Si wafer itself.

EX1005, FIG. 2

3. Element [1.b] providing an interface passivation layer over the substrate,

Yablonovitch discloses this limitation. EX1003, ¶114-126.

Yablonovitch deposits n^+ SIPOS layer that is oxygenated poly-Si (polysilicon), which is a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1005, 1211-13; EX1003, ¶115.

As shown in Step (7), the n^+ SIPOS layer is formed with 10 ppm O_2 , which results in a “5% oxygen concentration.” EX1005, 1213. As shown in Step (9), the n^+ SIPOS layer is then annealed at 900 °C for 15 minutes. EX1005, Table II; EX1003, ¶116.

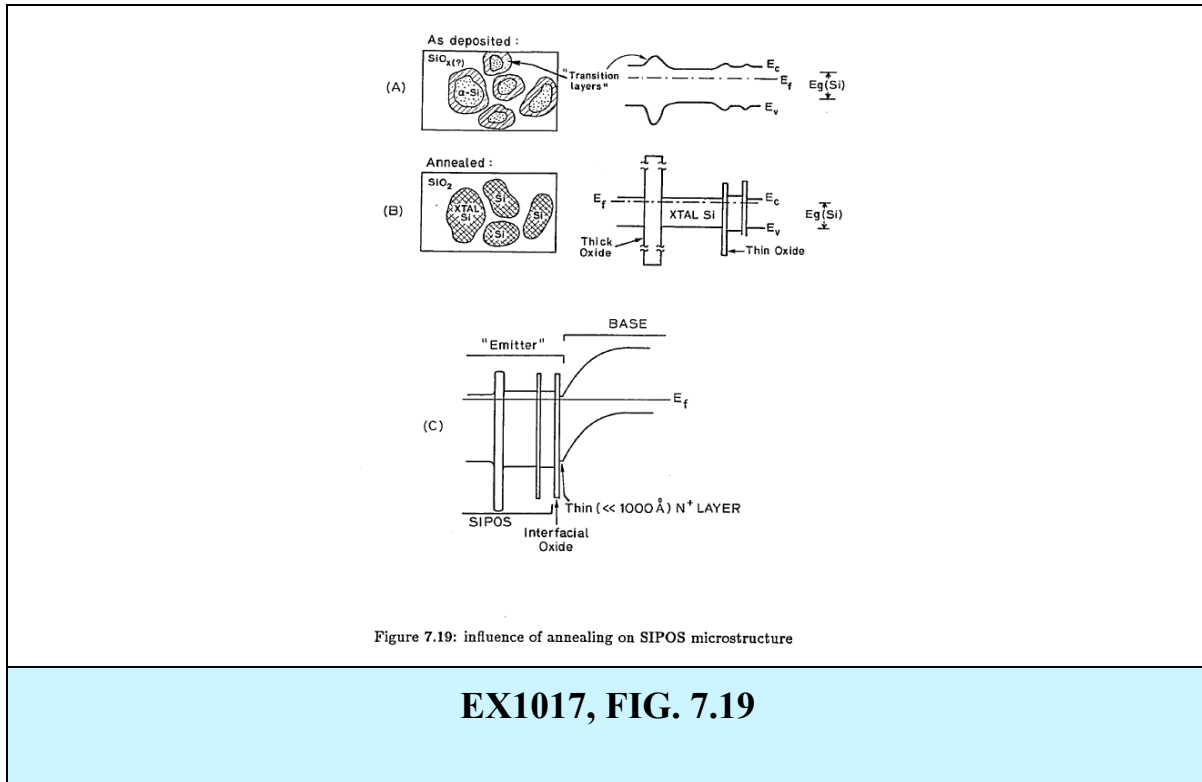
TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^\circ\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^\circ\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^\circ\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

EX1005, Table II

Kwark notes that while “SIPOS in the as deposited form consists of amorphous silicon islands embedded in a silicon rich matrix,” “[a]nnealing promotes the crystallization of the α -Si islands with accompanying rejection of oxygen from the crystals to the surrounding matrix.” EX1017, 178. Kwark further explains, “[t]he expulsion of oxygen outside the grains also *causes the formation of an oxide layer at the Si-SIPOS interface*” that “acts much like the intentionally introduced chem oxide in blocking hole injection into the SIPOS.” EX1017, 178. Thus, this “oxide layer at the Si-SIPOS interface” (**an interface passivation layer over the substrate**) is indicated as an “interfacial oxide” in Kwark’s Figure 7.19 below. *See*

also EX1017, 180 (referring to the interfacial oxide as a “thin tunnelable oxide at the Si-SIPOS interface”); EX1003, ¶117.

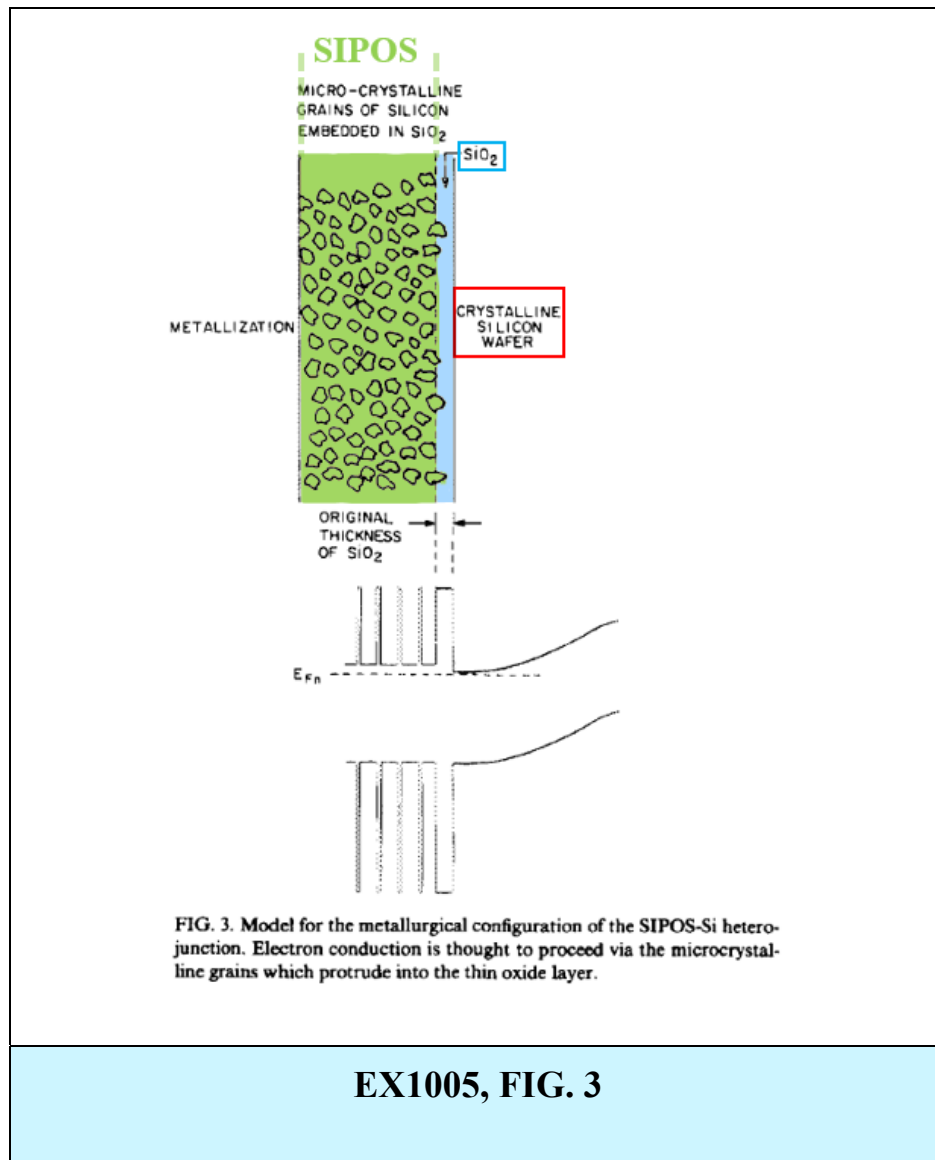


This interfacial oxide-forming property of SIPOS has been well understood for many years. Indeed, as of 1981, SIPOS was known to contain far more oxygen than can dissolve in silicon, such that during annealing, as crystal forms, the surplus oxygen is forced out of the crystal grains and into the surrounding regions. EX1003, ¶118 (citing EX1031, 554 (“[t]he oxygen concentration in SIPOS greatly exceeds its solubility in silicon, so that when silicon crystallites begin to form during annealing the excess oxygen must segregate outside the grains.”)).

Yablonovitch also discloses thermally growing a very thin silicon oxide, SiO₂, on the silicon wafer. *See* EX1005, 1211 (describing “thermally grown SiO₂”), 1213 (showing “thin oxide layer” of SiO₂ in Figure 3). In particular, step (6) describes growing the thin silicon oxide. EX1005, 1212; EX1003, ¶119.

TABLE II. Processing sequence.	
	1. Thin silicon wafers to 50 μm in aqueous KOH.
	2. Getter in an oxidation furnace containing substantial chlorine.
	3. Strip gettering oxide in HF acid.
	4. Immediately load into cold APCVD furnace while purging with N ₂ .
	5. Ramp up to 650 °C while maintaining N ₂ purge.
→	6. Oxidize for 5 min with 100 ppm O ₂ .
	7. Deposit SIPOS from 1000 ppm SiH ₄ , 50 ppm PH ₃ , and 10 ppm O ₂ .
	8. Ramp furnace to 900 °C.
	9. Anneal for 15 min.
	10. Ramp furnace down to 450 °C.
	11. Anneal in forming gas for 2 h.
	12. Pull wafers from cold furnace.
EX1005, Table II	

Step (6) grows a thin oxide layer for interface passivation by purging the chamber with N₂, then exposing the silicon wafer to oxygen for approximately five minutes. EX1005, Table II. This forms a very thin (25–40 Å, or 2.5-4 nm) amorphous layer of SiO₂ (silicon dioxide) (**an interface passivation layer**), which forms on the silicon wafer (**over the substrate**), as depicted in Figure 3 below. EX1005, 1212-13; EX1003, ¶120.



Kwark explains that if an oxide layer is formed on the Si/SIPOS interface before annealing, the anneal will create a separate interfacial oxide, where the two oxides together form a thicker composite oxide. EX1017, 180 (“adding the chem oxide layer to the SIPOS contact is therefore seen to result in two layers of interfacial oxide, one deliberately grown, the other, a by-product of the SIPOS annealing

process,” resulting in a “thicker composite oxide”). This “thicker composite oxide” is also **an interface passivation layer over the substrate**. EX1003, ¶121 (citing EX1017, 180).

A POSITA would have understood that the expelled oxygen from the SIPOS layer would also aid in the formation of the thermal thin oxide formed in Step (6). EX1003, ¶122 (citing EX1018 (explaining that “a thin tunnelable interfacial oxide” formed from the out-diffusion of oxygen from SIPOS during an anneal will “simply add[] an additional thickness” with a pre-formed thin oxide layer)). This thicker thermal thin oxide formed in Step (6) is also **an interface passivation layer over the substrate**. EX1003, ¶122.

Yablonovitch teaches that thin oxides at the interface between SIPOS and silicon substrates provide **interface passivation**. Yablonovitch teaches that when fabricating the solar cell, “the **interface** states at the heterocontacts *must be passivated*.” EX1005, 1211. In order to do so, Yablonovitch teaches that in its solar cell, “[t]he **interface** states between SIPOS and crystalline silicon (c-Si) seem to be **passivated as well as the high quality interface between thermally grown SiO₂ and c-Si**.” EX1005, 1211. In other words, thin interfacial SiO₂ oxides passivate the interface of SIPOS and crystalline silicon. EX1003, ¶123.

Further, Yablonovitch notes that the “outstanding voltage performance” of a fabricated solar cell according to its method “is made possible” in part by “the

excellent surface passivation of the n⁺ -SIPOS heterocontact.” EX1005, 1212 (emphasis added). Yablonovitch attributes the cell’s strong performance partly to excellent interface passivation from thermally grown SiO₂, while Kwark adds that this oxide partly came from oxygen released during the step (9) anneal, where the anneal also forms a separate interfacial oxide that improves passivation. EX1005, 1212; EX1003, ¶125.

Further, a POSITA would recognize that interfacial SiO₂ on silicon is well known to provide excellent surface passivation, which is consistent with the ’732 Patent. EX1003, ¶126 (also citing EX1006, 2197 (recognizing in 1971 the “intense interest” in “thin films of silicon dioxide due to their extensive use as passivating and insulating layers in the silicon planar technology,” specifically due to the “interface states” formed between silicon dioxide and silicon)).

The ’732 Patent’s descriptions of the **interface passivation layer** align with Yablonovitch and Kwark’s teachings. All of the ’732 Patent’s embodiments of the “passivating interface layer” describe it as having “<10 nm” thickness and identifies “silicon oxide” as a primary example. *See* EX1001, 5:61-64, 6:5-6:8, 7:5-8, 7:15-18, 8:15-18, 8:26-29, 9:22-25, 10:20-23, 10:30-33, 11:33-36, 11:43-46, 12:43-46, 12:54-57, 12:54-57, 13:50-53, FIG. 1. As such, the ’732 Patent does not purport to teach any invention or novelty regarding these properties, such that the omitted teachings are within the knowledge of a POSITA. EX1003, ¶126.

4. **Element [1.c] providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant,**

Yablonovitch discloses this limitation. EX1003, ¶127-137.

Yablonovitch **provid[es]** an n^+ SIPOS (“semi-insulating polycrystalline silicon”) layer over the thermal oxide and diffused oxide (**providing a passivating film over the interface passivation layer**). EX1005, 1211-13. It was well-known to a POSITA that SIPOS is oxygenated poly-Si (polysilicon), which can also be thought of as a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1005, 1211; EX1003, ¶127.

Steps (7-9) disclose the deposition the n^+ SIPOS layer: “*Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 and 10 ppm O_2 ,*” and then anneal, as shown below. EX1003, ¶128 (citing EX1005, 1211).

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^\circ\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^\circ\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^\circ\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

EX1005, Table II

The n⁺ SIPOS (**passivating film**) **compris[es]** phosphorus (**a conductive dopant**). EX1005, 1213. As shown in step (7), the n⁺ SIPOS deposition includes phosphine (PH₃), which produces phosphorus in the SIPOS layer. EX1005, 1213; EX1003, ¶129.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N₂.
5. Ramp up to 650 °C while maintaining N₂ purge.
6. Oxidize for 5 min with 100 ppm O₂.
- 7. Deposit SIPOS from 1000 ppm SiH₄, 50 ppm PH₃, and 10 ppm O₂.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

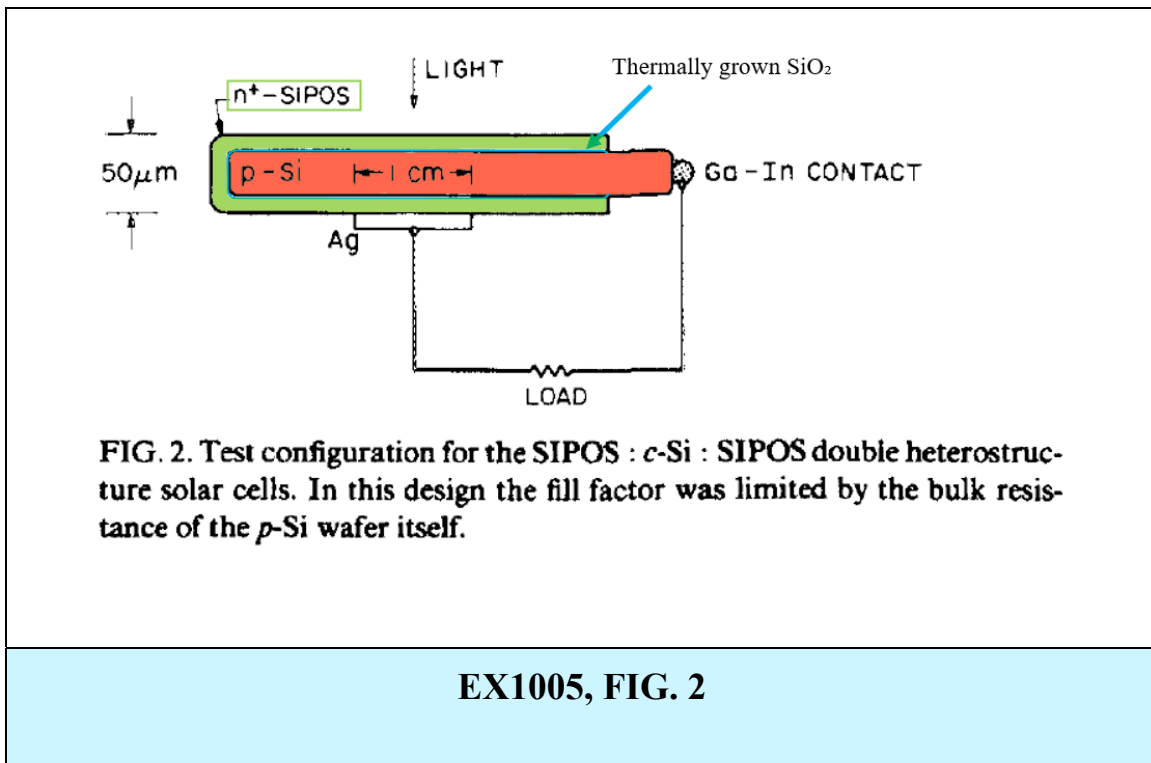
EX1005, Table II

Yablonovitch explicitly discloses that the SIPOS includes a “phosphorus **dopant**.” EX1005, 1213. The “phosphorus **dopant**” is an n-type dopant, which dopes the SIPOS layer to be n-doped, hence why it is an “n⁺ SIPOS” layer. EX1005, 1211. Phosphorus is a very well-known n-type dopant of silicon to a POSITA, if not the most commonly known n-type dopant of silicon. EX1003, ¶130 (citing

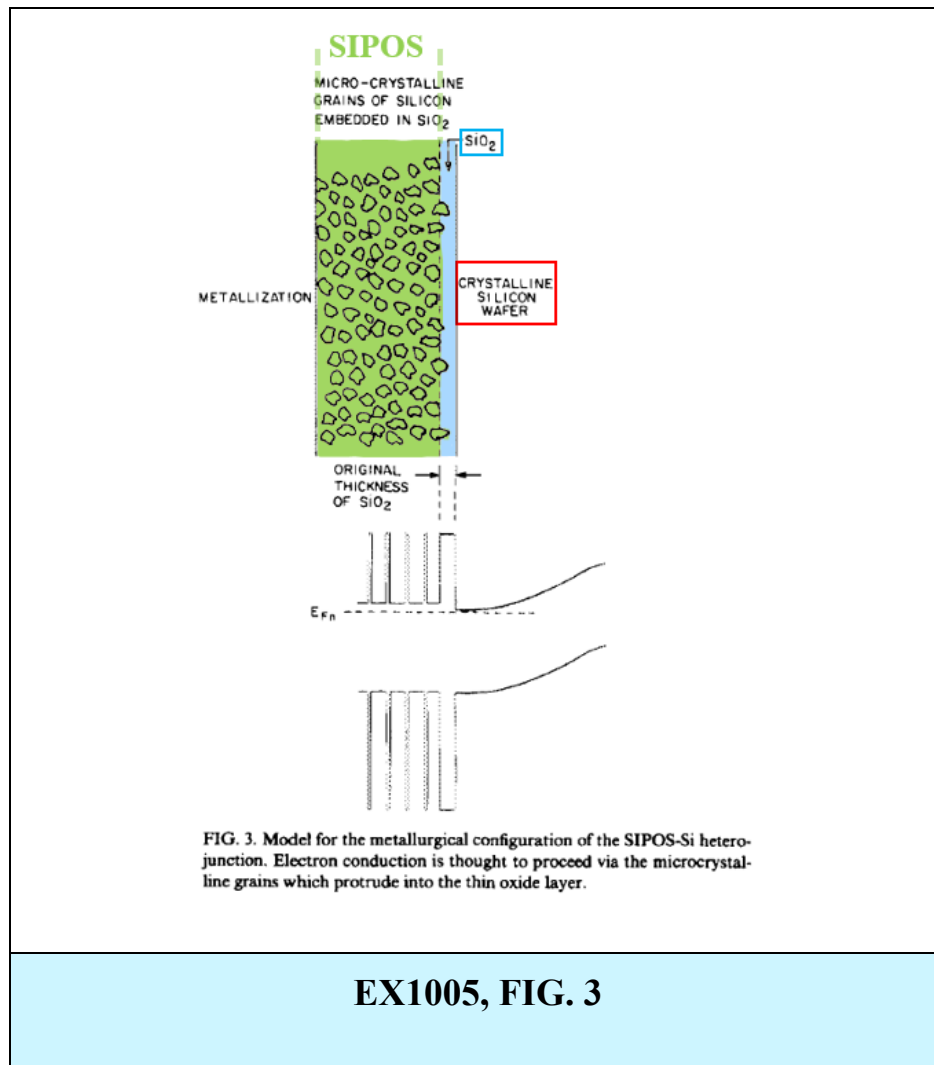
EX1022, 28 (“[p]hosphorus [was] the impurity generally used” to as the n-type dopant in “standard solar cell technology”)).

The anneal (step 9) serves to “activate the phosphorous **dopant**,” which causes the n^+ SIPOS to be more **conductive**. EX1005, 1212. When the phosphorous is “activated,” the phosphorous dopant is incorporated into the lattice structure of the n^+ SIPOS, making it more conductive because the incorporated phosphorous donates free electrons to the material, increasing the number of charge carriers and thus boosting conductivity. EX1005, 1212. Anneals “activate” dopants by incorporating them into the material’s lattice structure, which changes its electrical properties. *Id.* When annealed, phosphorus atoms replace silicon atoms in the lattice, subsequently bonding with four neighbors while leaving one loosely bonded electron that can move freely, thus increasing conductivity. EX1003, ¶131.

As a result of the phosphorous dopant and annealing, the n^+ SIPOS layer becomes conductive, forming a “SIPOS emitter structure,” as shown in Figures 2 and 3. EX1005, 1211-12. EX1003, ¶132. A POSITA would have understood that emitters in solar cells are **conductive** because carriers (i.e., electrons and holes) are generated in the emitter, and must be swept to a contact to generate current. *See* Section V.A. (Overview of the Technology); EX1003, ¶132. Accordingly, if an emitter is not conductive, carriers cannot be conducted through it, rendering solar cells unable to generate any currents. EX1003, ¶132.



The n⁺ SIPOS layer is also explicitly taught by Yablonovitch to be **conductive** after the phosphorous dopant and annealing. As shown in Figure 3, in the SIPOS-Si heterojunction, “[e]lectron **conduction** is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.” EX1005, 1213. As Yablonovitch further explains, such contact “provide[s] **more than enough conductivity** for majority-carrier electrons.” EX1005, 1213; EX1003, ¶133.



The '732 Patent states that its “[e]lectrically passivating and conductive film” may be an “amorphous or polycrystalline silicon.” EX1001, 5:47-51. SIPOS is simply oxygenated poly-Si (polysilicon). EX1005, 1211. In other words, SIPOS is a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1005, 1211. Further, Yablonovitch explains that the “electrical” properties of the n^+ SIPOS emitter are generally the same as a polysilicon emitter, to which a POSITA would

recognize as conductive. EX1005, 1213; EX1003, ¶134. For example, Yablonovitch explains that the resistivity of the n^+ SIPOS of $10^{-3} \Omega \cdot \text{cm}$ is “similar to that of doped polysilicon.” EX1005, 1213. Yablonovitch notes that rather than an electrical difference, the relevant difference provided by the 5% additional oxygen concentration in n^+ SIPOS as compared to poly-Si is that the oxygen content increases the density of grains protruding into the thin oxide layer, increasing conduction. EX1005, 1213. As discussed above, n^+ SIPOS is essentially oxygenated poly-Si (polysilicon), such that its “[e]lectrically passivating and conductive film” may be an “amorphous or polycrystalline silicon.” EX1005, 1211. Polysilicon was a well-known conductor used to form conductive emitters in solar cells. *See* ’732 Patent, 17:26-46 (describing how polysilicon is an exemplary material used for used to form conductive emitters); *see also* Section V.A (Overview of the Technology); EX1003, ¶134.

The n^+ SIPOS layer is a **passivating** film that **compris[es] a passivating material**. EX1003, ¶135. Yablonovitch notes that the “outstanding voltage performance” of the solar cell fabricated according to its method “is made possible” in part by “the **excellent surface passivation** of the n^+ -SIPOS heterocontact.” EX1005, 1212. Yablonovitch teaches that “the interface states at the heterocontacts *must be passivated*” and that in order to do so, Yablonovitch teaches that in the solar cell fabricated according to its method, “[t]he interface states between **SIPOS** and

crystalline silicon (c-Si) seem to be **passivated** as well as the high quality interface between thermally grown SiO₂ and c-Si.” EX1005, 1211; EX1003, ¶135.

Thus, the n⁺ SIPOS layer acts as a **passivating** heterojunction emitter with “excellent surface passivation” that enables an outstanding open-circuit voltage of 720 mV. EX1005, 1212. The SIPOS/c-Si junction yields an extremely low saturation current ($J_0 \sim 1 \times 10^{-14}$ A/cm²) due to this passivation. EX1005, 1212; EX1003, ¶136.

It was also well-known to a POSITA that SIPOS emitters were **passivating**. EX1003, ¶137. Further, a POSITA would have also recognized Yablonovitch’s SIPOS emitter as a **passivating layer** because it reduces surface defects and minimizes carrier recombination at the silicon interface, thus improving solar cell efficiency. EX1003, ¶137 (citing EX1007, 77 (an “application [of SIPOS] is the incorporation of a SIPOS emitter as a passivating layer in conventional silicon solar cell structures”); EX1014, Abstract (SIPOS is “used as passivation films on silicon devices”)).

5. **Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: [1d.1] providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant,**

Yablonovitch discloses this limitation. EX1003, ¶138.143

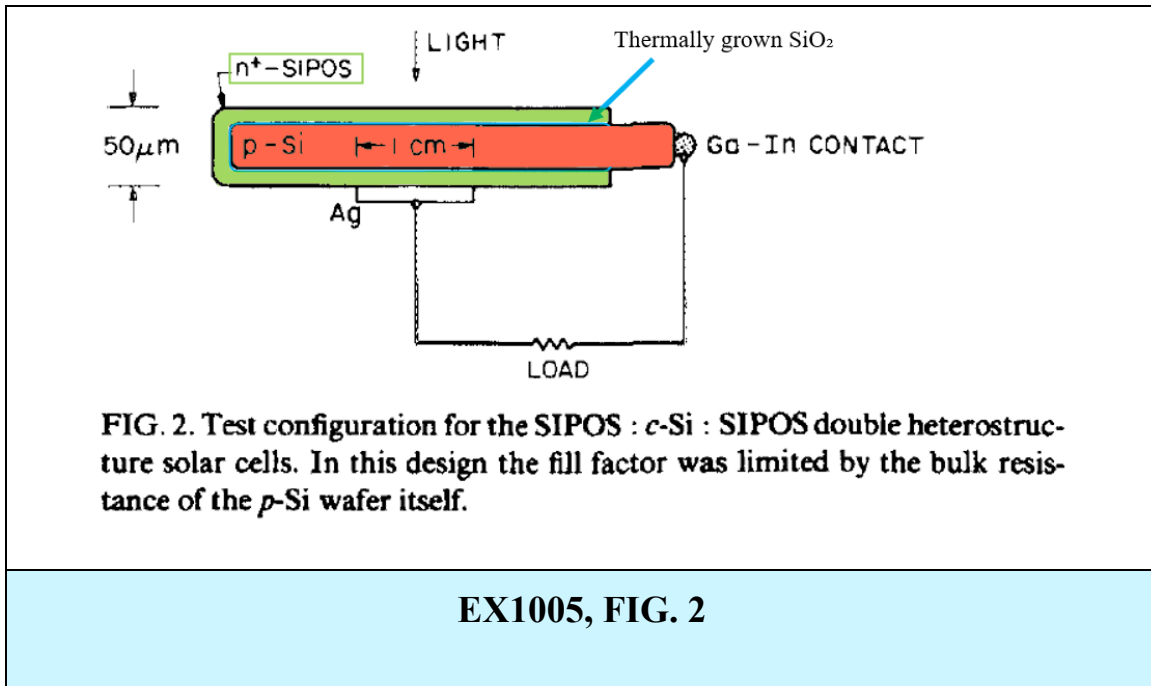
Before annealing, the n⁺ SIPOS layer is **an amorphous silicon-containing compound**. EX1005, 1211-13. As discussed, SIPOS stands for “semi-insulating polycrystalline **silicon**,” meaning that it is a **silicon-containing compound**. EX1005, 1211; EX1003, ¶139.

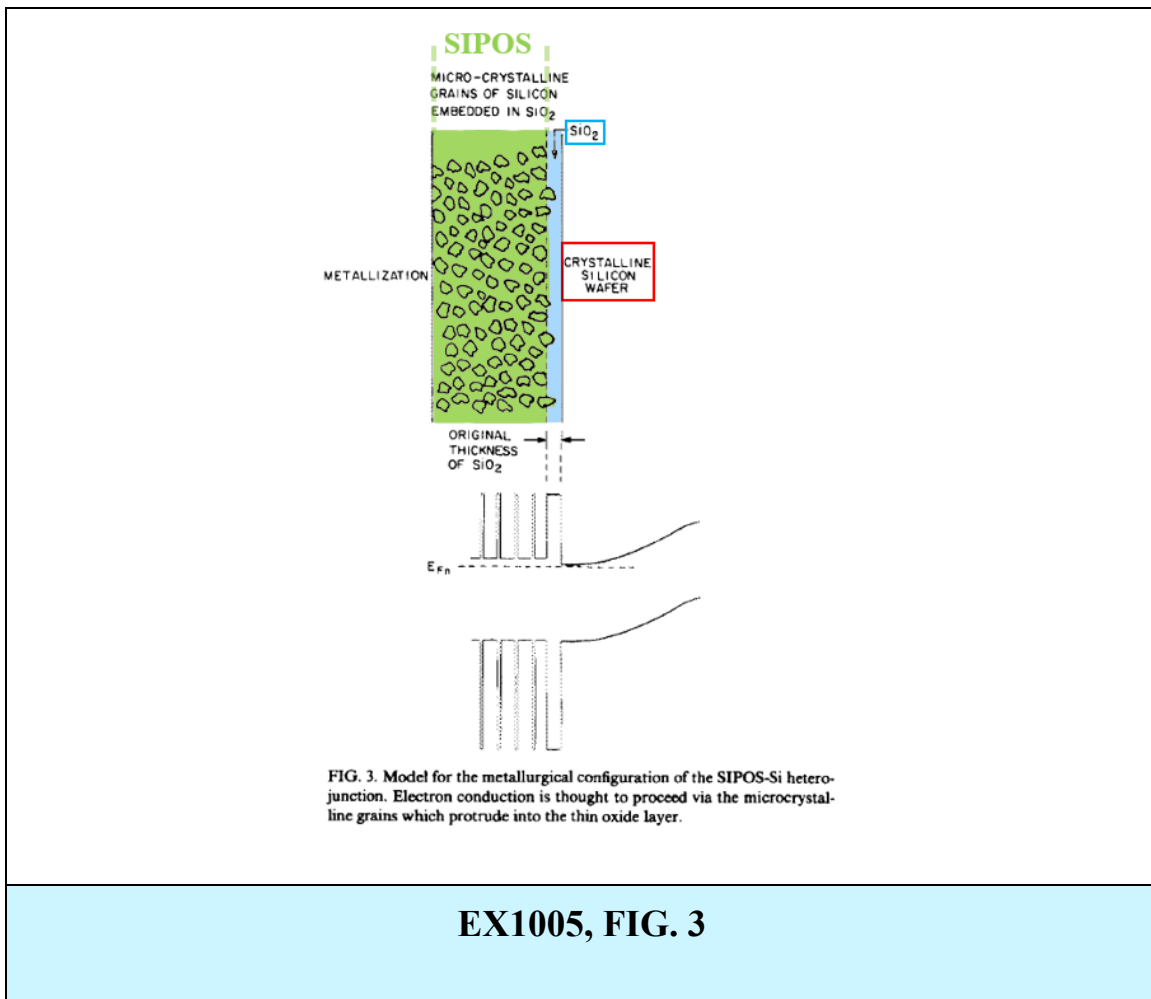
Prior to annealing, the n⁺ SIPOS layer is **amorphous**. Yablonovitch explains that the anneal is “necessary to precipitate microcrystalline silicon grains.” EX1005, 1211. Here, a POSITA would recognize that the term “precipitate” is referring to crystal precipitation, which is the process of transitioning from amorphous silicon to polycrystalline silicon. EX1003, ¶140 (citing EX1019, 1021 (“As deposited, SIPOS is usually amorphous... During annealing it has been found that the film morphology changes. *Si precipitates into small grains of crystalline Si and the oxygen segregates as SiO₂ on the grain boundaries*”)) (emphases added)). It was conventional and well-known to a POSITA that a silicon compound formed from a deposition of SiH₄ at 650 C is amorphous until it is annealed at a higher temperature because 650 C is not hot enough for silicon atoms to form an ordered crystal, thus **amorphous** (see step 7). EX1003, ¶140 (citing EX1019, 1021 (“As deposited, SIPOS is usually amorphous”)).

While it was well-known before the relevant time, Kwark explicitly recognizes that while “SIPOS in the as deposited form consists of **amorphous silicon** islands embedded in a silicon rich matrix,” “[a]nnealing promotes the

crystallization of the α -Si islands with accompanying rejection of oxygen from the crystals to the surrounding matrix.” EX1017, 178; EX1003, ¶141.

As shown in Figures 2 and 3, the n^+ SIPOS is provided **over an upper surface of the substrate**. EX1005, Fig. 2-3; EX1003, ¶142.





The n^+ SIPOS comprises **oxygen dopant** and the **conductive dopant**. A POSITA would recognize that SIPOS by definition is polycrystalline silicon doped with oxygen. EX1003, ¶143. Here, in the case of Yablonovitch, a “5% oxygen concentration” of **oxygen dopant** is used. EX1005, 1213. As discussed in element [1c], Yablonovitch discloses that the SIPOS includes a “phosphorus dopant” (**the conductive dopant**). EX1005, 1213; *see also* Section IX.C.4 ([1.c]); EX1003, ¶143.

6. Element [1.d] wherein providing the interface passivation

layer and providing the passivating film comprise: ... [1d.2] thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and,

Yablonovitch in view of Kwark discloses this limitation. EX1003, ¶144-146.

After depositing the SIPOS in step (7), Yablonovitch teaches anneals at high temperature. EX1005, 1212. As shown in steps 8-9 of Table II, after deposition at 650 °C, the furnace is ramped up to 900 °C, such that the wafer is annealed for 15 minutes, which is **thermally treating the amorphous silicon-containing compound**. EX1005, 1212; EX1003, ¶145.

TABLE II. Processing sequence.	
	1. Thin silicon wafers to 50 μm in aqueous KOH.
	2. Getter in an oxidation furnace containing substantial chlorine.
	3. Strip gettering oxide in HF acid.
	4. Immediately load into cold APCVD furnace while purging with N_2 .
	5. Ramp up to 650 °C while maintaining N_2 purge.
	6. Oxidize for 5 min with 100 ppm O_2 .
	7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
	8. Ramp furnace to 900 °C.
	9. Anneal for 15 min.
	10. Ramp furnace down to 450 °C.
	11. Anneal in forming gas for 2 h.
	12. Pull wafers from cold furnace.
EX1005, Table II	

As discussed in element [1.b] (*see* Section IX.C.3), Kwark recognizes that while “SIPOS in the as deposited form consists of amorphous silicon islands

embedded in a silicon rich matrix,” (corresponding to **the amorphous silicon-containing compound**), annealing (**thermally treating**) causes “rejection of oxygen from the crystals to the surrounding matrix” (i.e., **to diffuse the oxygen dopant**). EX1017, 178. As Kwark further explains, “[t]he expulsion of oxygen outside the grains also *causes the formation of an oxide layer at the Si-SIPOS interface.*” *Id.* Indeed, the anneal causes the SIPOS layer **to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate.** As further discussed in element [1.b] (*see* Section IX.C.3), this SIPOS-formed oxide is an **oxide layer defining the interface passivation layer** both alone and in combination with the “composite oxide” formed with the thermally grown oxide from Step (6). EX1017, 178-80; EX1003, ¶146.

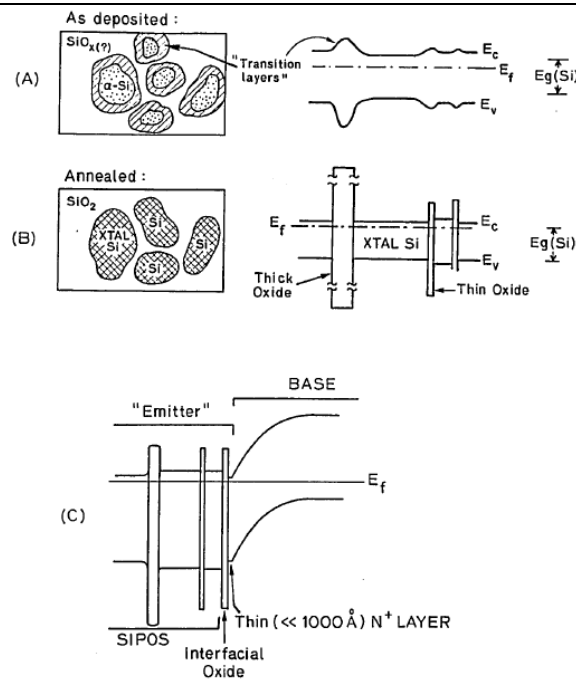


Figure 7.19: influence of annealing on SIPOS microstructure

EX1017, FIG. 7.19

7. Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.3] wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film; and,

Yablonovitch discloses this limitation. EX1003, ¶147.

As discussed in element [1c] (*see* Section IX.C.4), Yablonovitch teaches that after annealing (thermally treating the amorphous silicon-containing compound) into the amorphous SIPOS layer (remaining amorphous silicon-containing compound above the oxide layer), the result annealed SIPOS becomes

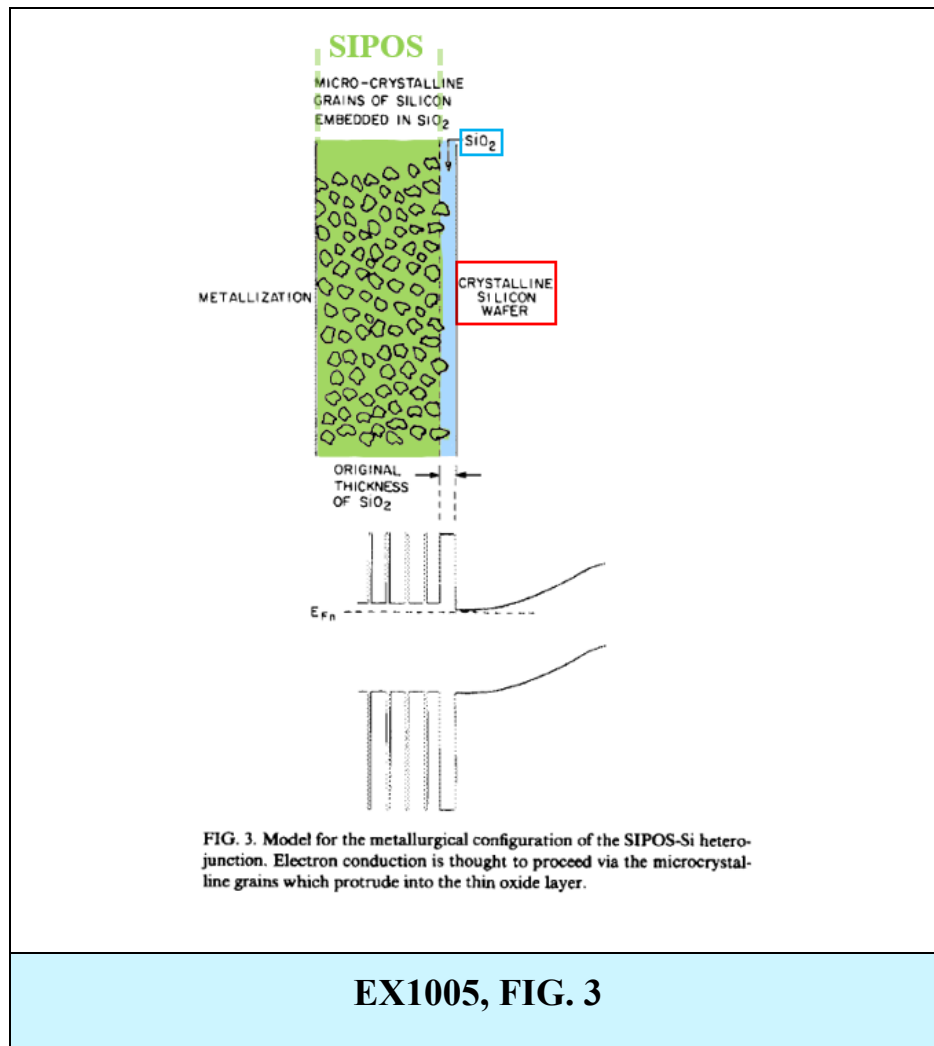
the passivating film (**defines the passivating film**). EX1003, ¶147.

8. **Element [1.d] wherein providing the interface passivation layer and providing the passivating film comprise: ... [1d.4] wherein the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate; and,**

Yablonovitch in view of Kwark discloses this limitation. EX1003, ¶148-166.

First, Yablonovitch explains that “during [the annealing] step the phosphorus **diffuses** about 20-50 Å into the silicon wafer as measured by secondary ion mass spectrometry.” EX1005, 1212. Yablonovitch’s anneal step (9) (**the thermally treating**) **diffuses at least a portion of the** phosphorus dopant (**conductive dopant**) **throughout the interface passivation layer** and into the c-Si substrate by roughly 2–5 nm, which is on the other side of the SIPOS layer. EX1005, 1212. Yablonovitch teaches that the result is a “shallow n⁺ accumulation layer” at the wafer surface, which essentially forms an n⁺ region (cause by the presence of phosphorus dopant) in the wafer directly beneath/through the interface oxide. EX1005, 1212; EX1003, ¶149.

Because the silicon wafer is on the opposite side of the interfacial oxide as the SIPOS layer, the phosphorous must diffuse **throughout the interface passivation layer** that sits between the SIPOS layer (**green**) and silicon wafer (**red**), as shown in Figure 3. EX1005, 1212; EX1003, ¶150.



The anneal causing the phosphorous dopant diffused through the interfacial oxide and “*n* + accumulation layer” at the wafer surface (i.e., the surface interfacing the interfacial oxide) serves **to facilitate electrical connection to the substrate**. Such a diffusion makes the wafer surface more strongly *n*-type, thus better matching the SIPOS layer so that the wafer surface will have higher conductivity, and particularly a higher conductivity path (i.e., **electrical connection**) **to the substrate**. The anneal further aids in such diffusion by breaking up the oxide(s), which allows

the phosphorous dopant to diffuse more freely. EX1003, ¶151 (citing EX1024, 36-37 (“Annealing at high temperatures can reduce the emitter resistance and the leakage by breaking up the chemical oxide and diffusing the junction deeper into the substrate.”)).

Second, for very thin oxides, such as under 5nm, dopant can pass and enter throughout and pass through the oxide easily. EX1003, ¶152 (citing EX1030, 956-7 (describing the “diffusion of phosphorous in ultra-thin oxides from a doped polysilicon” into a silicon substrate, finding “very high” concentrations of dopants in the silicon substrate “[e]ven with a short diffusion time.”); EX1029, 292 (describing “increasing amounts of phosphorus pass through the silicon oxide/silicon interface as the oxide layer gets thinner.”)).

Yablonovitch uses a phosphorus dopant in the interfacial oxide and substrate to form low resistance pathways through those layers, making it easier for electrons to travel across. Specifically, the diffusion of dopant into these layers increases the conductivity of the solar cell near the surface of the silicon substrate, i.e., through the interfacial oxide, since its conductivity is more similar to the conductivity of the n^+ SIPOS. Indeed, because it is an interfacial oxide, the charges take a more direct route from the substrate toward the electrodes than they otherwise would without the diffusion of the dopant. EX1003, ¶153.

The diffusion of phosphorus from the n+ SIPOS layer through the interfacial oxide (**interface passivation layer**) creates such conductive paths. It has been well-known to a POSITA that diffusion of phosphorous through an SiO₂ layer and through its interface with a silicon substrate **facilitate[s] electrical connection to the substrate**. EX1003, ¶154.

For example, in 1961, experiments showed that the distribution of phosphorus across the oxide-silicon interface was continuous. EX1003, ¶155 (citing EX1032, 5 (“the distribution of phosphorus across the oxide-silicon interface is continuous”) (describing results demonstrating phosphorus atoms more without interruption across the oxide-silicon interface)).

As another example, in 1975, another experiment demonstrated that there is phosphorus distribution through the interface across SiO₂ and silicon. EX1003, ¶156, (citing EX1009, 399 (there is a “continuity of impurity [phosphorous] distribution through th[e] interface” of SiO₂ and silicon) (describing results from using doped oxide condition suggesting continuous distribution at the oxide-silicon interface)).

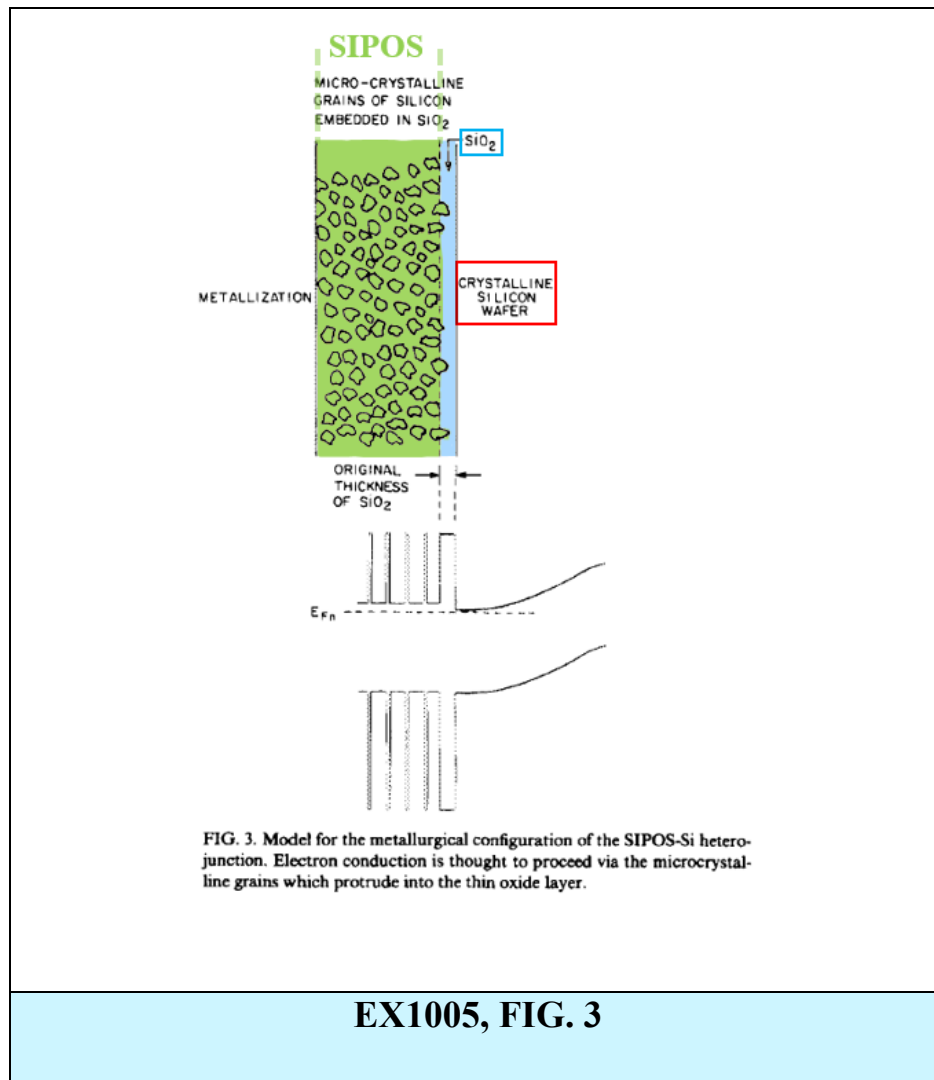
In another example, in 1985, a study found that annealing drives dopants along polysilicon grain boundaries, through the oxide, and into the underlying single-crystal silico to form the emitter-base junction. EX1003, ¶157 (quoting from EX1027, 471 (explaining that an anneal causes dopants “to diffuse rapidly down the

grain boundaries of the polysilicon, through the oxide film and into the underlying single-crystal Si to form the e/b junction”) (describing results showing how oxide needs to be continuous to fabricate a bipolar transistor)).

Further, the anneal (**the thermally treating**) also diffuses at least a portion of the conductive dopant throughout the interface passivation layer by embedding phosphorous and phosphorous-containing microcrystals into the interfacial oxide. Thus, the annealing perforates the interfacial oxide **to facilitate electrical connection to the substrate**; EX1003, ¶158.

Yablonovitch explains that the anneal (**the thermally treating**) causes phosphorus (**the conductive dopant**) in the microcrystalline grains to **diffuse[]** from the SIPOS layer to be “embedded in”/ “protrude into” the thin oxide (**throughout the interface passivation layer**). EX1005, 1212. The phosphorous-containing microcrystalline grains are embedded into and **throughout** the thin oxide, as they form a “thin spots and pinholes in the SiO₂.” EX1005, 1213; EX1003, ¶159.

Yablonovitch explains that the incorporation of oxygen means that the SIPOS grains are smaller but have a “significant surface density,” in contrast to the “much larger” polysilicon grains that are fewer in number. EX1005, 1213. A POSITA would understand that to have “significant surface density of individual” phosphorous-containing microcrystalline grains, they must be **throughout** the thin oxide to form such a “significant surface density”. EX1003, ¶160.



Due to the anneal, the interface is not a uniform insulating barrier. Instead, the interface contains pinholes of doped material that let carriers through locally. Figure 3 of Yablonovitch illustrates this feature, explaining that “[e]lectron **conduction** is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer,” which means that it is **to facilitate electrical connection to the substrate** since the [e]lectron **conduction** protrude into the thin oxide layer.

EX1005, 1213 (“the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO₂.”); EX1003, ¶161.

Further, those n⁺ SIPOS microcrystalline grains include the phosphorous dopant in their lattice. The phosphorous dopant makes the lattice more conductive because the anneal serves to “activate the phosphorous dopant”. EX1005, 1212; *see also* Section IX.C.4 (discussion of “activating the phosphorous dopant” in [1.c]). Here, anneals “activate” dopants by incorporating them into the material’s lattice structure, changing its electrical properties. This is because when dopants like phosphorus are introduced into a semiconductor, they might not immediately settle into the correct, “substitutional” positions within the crystal lattice where they can donate their extra electron. Annealing causes phosphorous atoms to substitute silicon atoms in the crystal lattice. More specifically, four of the silicon atom’s valence electrons form covalent bonds with the surrounding silicon atoms, such that the fifth valence electron is then loosely bound to the phosphorus atom. This extra electron can easily become a free electron, contributing to the material’s conductivity by acting as a charge carrier since it has not been bonded to a silicon atom. EX1003, ¶162.

High-temperature annealing causes phosphorous-doped microcrystalline Si grains in the SIPOS to poke through the interfacial SiO₂. As such, electrical contact

between the n^+ layer and the wafer occur at these numerous microscopic points. Yablonovitch explicitly notes that “*electrical contact is via thin spots and pinholes in the SiO_2* ” at the interface. EX1005, 1213. As such, the highly conductive phosphorous-doped microcrystalline Si grains **facilitate electrical connection to the substrate** for majority carriers (electrons, in the n^+/p junction) to flow from the silicon substrate through the thin oxide and SIPOS layer and to the metal electrode. Thus, for majority carriers, the electrical connection to the substrate is facilitated and low-resistance in comparison to if the microcrystalline grains did not form the pinhole “contacting points” from high-temperature annealing. EX1003, ¶163.

It was well-known to a POSITA that anneals caused thermally grown interfacial oxides to perforate or “break-up.” EX1003, ¶164. The perforations allow current paths through the oxide. After the native oxide interface break-up from annealing, electrons will flow preferentially through openings in the native oxide interface. EX1003, ¶164 (citing to EX1008, 249 (explaining that after “native oxide interface” break-up from annealing, “[t]he electrons flow preferentially through the openings in the native oxide interface, which are **paths of least resistance.**”)). This flow is the path of least resistance. *Id.*

Furthermore, as the oxide begins to break up because of annealing, additional highly conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions. EX1003, ¶165 (citing to

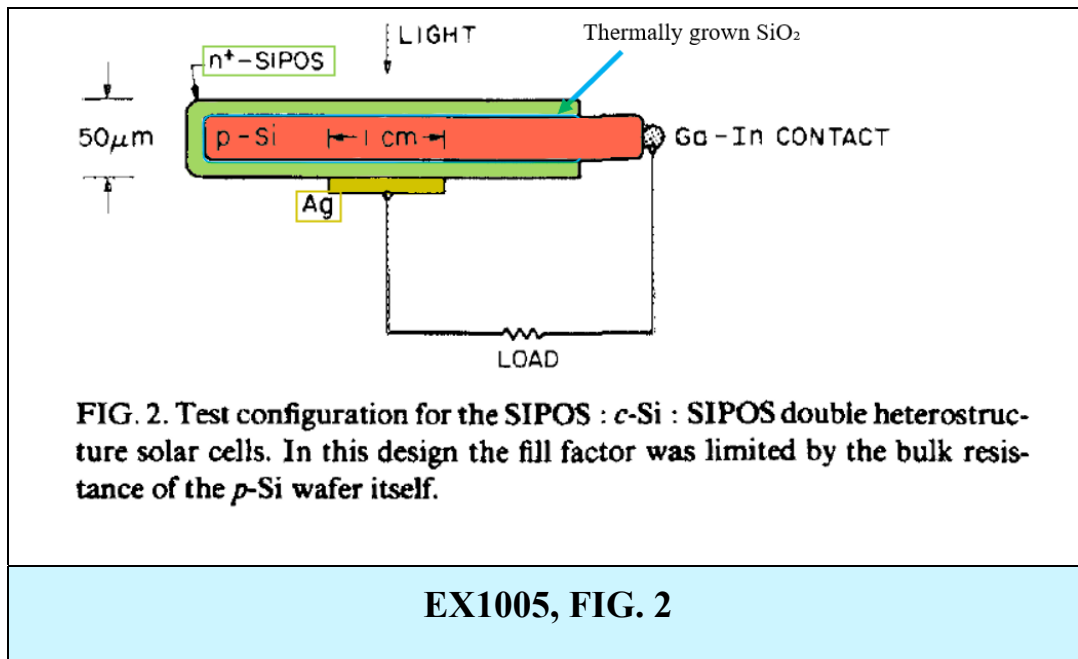
EX1016, 249 (explaining that explained that “[a]s the oxide starts to break up [due to the anneal]” additional **highly conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions**)).

Yablonovitch teaches annealing at 900 °C for oxide break-up at a portion of the interface oxide **resulting in a low emitter resistance**. EX1005, 1211. A POSITA would understand that the oxide break-up occurs at 900 °C. EX1003, ¶166 (citing to EX1025, 228 (finding that a “significant breakup of the oxide layer” occurs “during the 900°C drive-in”)).

9. Element [1.e] providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate,

Yablonovitch discloses this limitation. EX1003, ¶167-175.

Yablonovitch discloses that “[t]he n⁺ -SIPOS was contacted with a 0.5 cm x 1 cm evaporated silver electrode” (**providing at least one electrode over the passivating film**), as shown in Figure 2. EX1005, 1212. Indeed, Yablonovitch teaches that the **provid[ed] silver electrode is over the n⁺ -SIPOS (the passivating film)**. EX1005, 1212; EX1003, ¶168.



Yablonovitch's teaches that by diffusing phosphorus into the wafer and crystallizing the SIPOS, the diffusion creates an n^+/p "high-low" junction at the interface, increasing conductivity in the interface region and aligning the Fermi levels. EX1005, 1212. As a result, carriers can take a direct route using these phosphorous dopant-created conductive pathways from the silicon wafer to the electrode through the composite layers. As discussed above in element [1.d.3] (*see* Section IX.C.7), phosphorous diffusion from the n^+ SIPOS throughout the interfacial oxide and into the surface of the silicon wafer occurs **to facilitate electrical connection to the substrate**, by diffusion of phosphorous atoms and diffusion of phosphorous-containing micro crystallites that perforate the interfacial oxide. Accordingly, this phosphorous (**conductive dopant**) **within the** n^+ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation**

layer) provides direct electrical connection between the at least one electrode and the substrate. EX1003, ¶169.

Yablonovitch's device produces electric current from sunlight by a resulting direct electrical path that electrons travel from the crystalline silicon wafer to the silver electrode. Thus, the path of electrons in Yablonovitch's device travels along a direct electrical connection between the at least one electrode and the substrate. EX1003, ¶170.

First, electrons originate in the crystalline silicon wafer. Electrons, as minority carriers in the p-Si, are generated within the p-type crystalline silicon wafer by photon absorption. Indeed, the fundamental operation of a solar cell involves the generation of electron-hole pairs in the semiconductor material when exposed to light. *See* Section V.A.1 (Overview of Solar Cells, PN Junctions, and Doping). For the p-n junction of n⁺-SIPOS and p-Si, holes are the majority carriers in the p-Si substrate (or base) that need to be collected from the p-Si base. EX1003, ¶171.

Second, electrons are swept from the silicon wafer through an electrical connection across the interfacial oxide and thermal oxide to the n⁺ SIPOS layer as discussed in element [1.d.3]. *See* Section IX.C.7; EX1003, ¶172. Phosphorous diffusion from the n⁺ SIPOS throughout the interfacial oxide and thermal oxide and into the surface of the silicon wafer serves to facilitate electrical connection to the substrate. This is because of both the diffusion of phosphorous atoms and because

of diffusion of phosphorous-containing micro crystallites perforate the interfacial oxide. Accordingly, this phosphorous (**conductive dopant**) **within the** n⁺ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation layer**) **provides direct electrical connection between the** silicon wafer and silicon wafer-facing surface of the n⁺ SIPOS layer. EX1003, ¶172.

Third, electrons pass into and through the n⁺-SIPOS layer. EX1003, ¶173. As discussed in element [1.c] (*see* Section IX.C.4), the n⁺-SIPOS layer is highly conductive after annealing. EX1003, ¶173.

Fourth, electrons reach other side of the n⁺-SIPOS layer and are collected by the silver electrode (described above herein in [1.e]). EX1003, ¶174.

Accordingly, phosphorous dopant-created conductive pathways **within the** n⁺ SIPOS (**passivating film**) and **throughout the** interfacial oxide (**interface passivation layer**) **provide[s] direct electrical connection between the at least one electrode and the substrate.** EX1003, ¶175.

D. Dependent Claim 2: The method of claim 1, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.

Yablonovitch discloses this claim. EX1003, ¶176-181.

Yablonovitch explains that “[t]he annealing step (9)... is necessary to precipitate microcrystalline silicon grains within the material” (**the thermally treating crystallizes, at least in part, the passivating film to establish a**

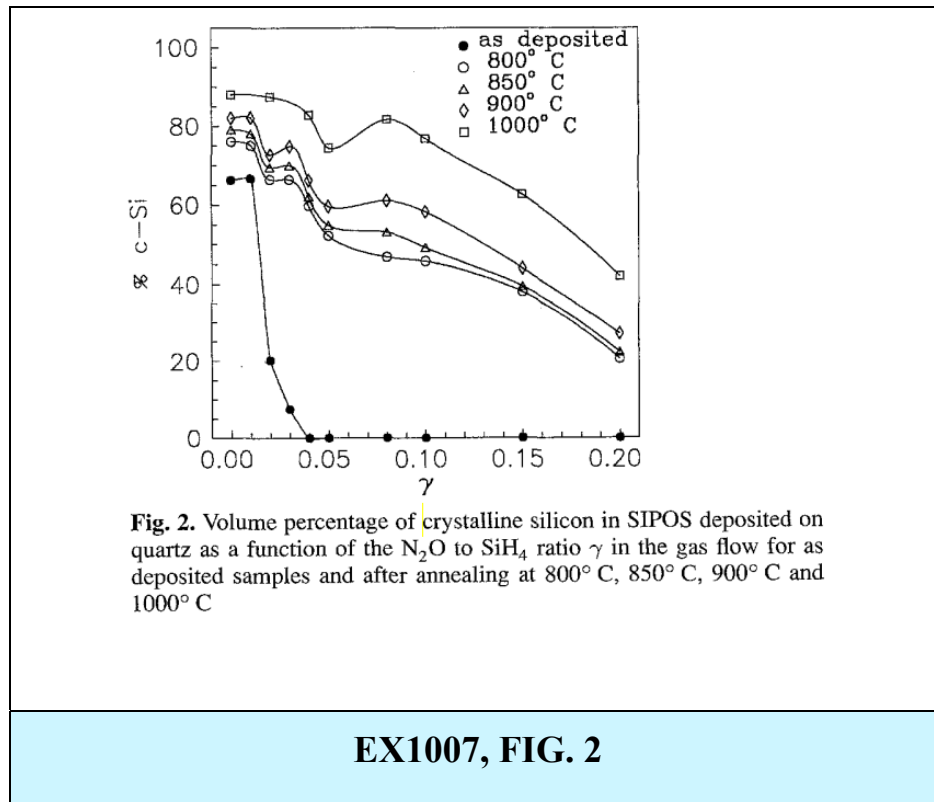
crystallized passivating film). EX1005, 1212. The high-temperature anneal at 900 °C causes the initially deposited (amorphous) SIPOS to become **a crystallized passivating film**, i.e., polycrystalline (with embedded microcrystals). EX1005, 1212-13, FIG. 3 (showing the “microcrystalline silicon grains”); EX1003, ¶176.

A POSITA would have understood that “precipitate microcrystalline silicon grains” means the SIPOS **crystallizes, at least in part** because “precipitate” refers to crystal precipitation. EX1005, 1211. Crystal precipitation is one way to perform crystallization. EX1005, 1211; EX1003, ¶177.

SIPOS and polysilicon were well known to crystallize at an anneal temperature 900 °C, such that a POSITA would have recognized that Yablonovitch’s SIPOS layer would have crystallized during the 900 °C anneal. EX1003, ¶178 (citing to EX1013, 166 (“When phosphorous is diffused at 950 °C, the structure changes to crystallite, and grain size increases to a size between 0.5 and 1.0 μm.”)).

Furthermore, after annealing, the amorphous film turns polycrystalline, with the amount of crystalline silicon increasing as the annealing temperature rises. EX1003, ¶179 (citing from EX1003, 79 (“After annealing the amorphous films become polycrystalline whereby the volume fraction of c-Si increases with annealing temperature.”)). This is shown in Figure 2, which shows the percent crystallization of silicon in SIPOS as deposited, and after subsequent anneal steps at various anneal temperatures. EX1003, ¶179 (citing to EX1007, Fig. 2). As shown,

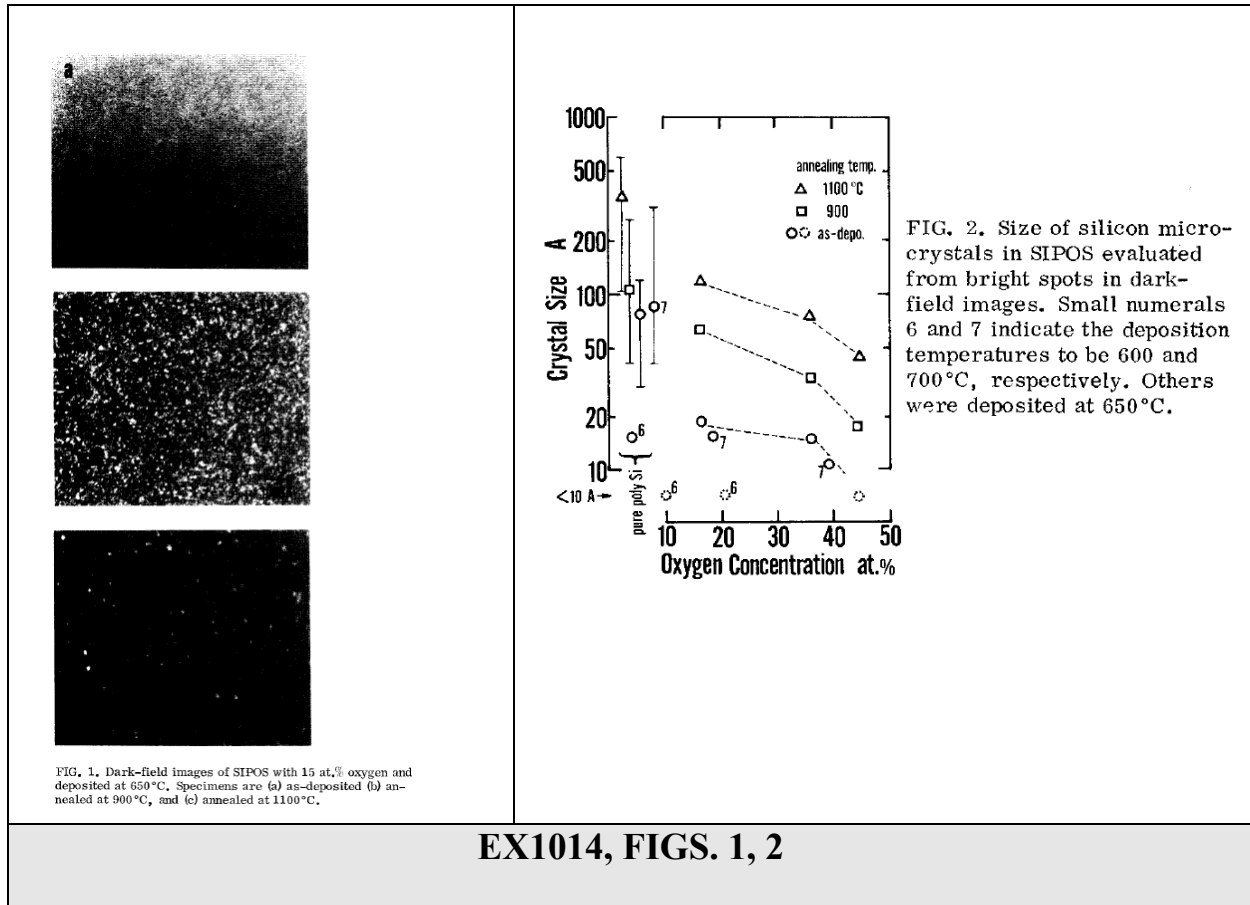
Yablonovitch's high-temperature anneal of 900 °C would result in significantly increased percent crystallization of silicon in SIPOS, and therefore the SIPOS **crystallizes, at least in part** as a result of the anneal. EX1005, 1212; EX1003, ¶179.



“SIPOS can be regarded as a three component mixed phase consisting of crystalline and amorphous silicon as well as voids or SiO_2 ,” where the anneal step results in a phase separation of amorphous silicon into crystalline Si grains. EX1003, ¶180 (quoting from EX1007, 77-79).

As shown in Figures 1 and 2 in Yablonovitch, under identical thermal conditions as (650 °C deposition and 900 °C anneal, annealing crystallizes SIPOS. See EX1014, Figs. 1-2; EX1003, ¶181 (citing EX1005, 1212 (describing micro

crystals in SIPOS layers how annealing crystallizes SIPOS at 650 °C deposition and 900 °C anneal)

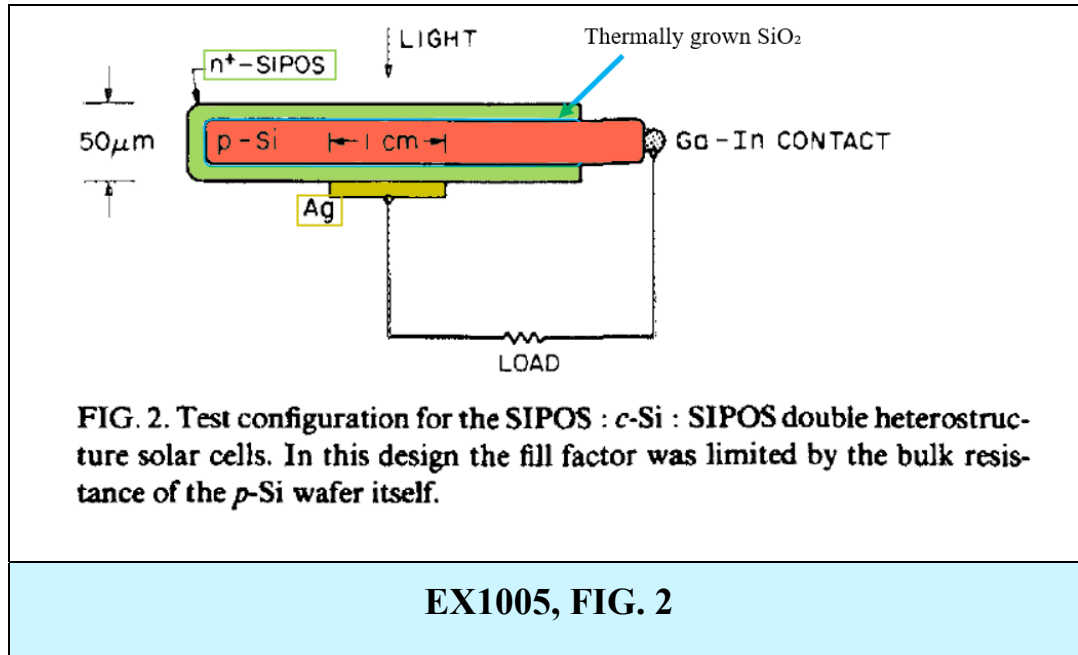


E. Dependent Claim 3: The method of claim 2, wherein the crystallized passivating film is a transparent film.

Yablonovitch discloses this claim. EX1003, ¶182-184.

The annealed n+ SIPOS layer (**the crystallized passivating film**) is a **transparent film**. This is because the SIPOS can cover the light-facing side of the silicon substrate, while light is able to enter the silicon substrate to generate

electrons, meaning that it is a **crystallized passivating film** that allows light through because it is a **transparent film**. EX1003, ¶183.



It was further known to a POSITA before the relevant time that SIPOS was transparent. EX1003, ¶184 (citing EX1005, 1212 (noting that the SIPOS layer is transparent to minority carriers)).

F. Dependent Claim 4: The method of claim 2, wherein the crystallization of the passivating film improves a passivation of the passivating film.

Yablonovitch discloses this claim. EX1003, ¶185.

As incorporated by reference for claim limitations [1.b] and [1.d.2] (see Sections IX.C.3, IX.C.6), which explain that **the crystallization of the SIPOS layer (the passivating film)** expels oxygen to form an interfacial oxide. By expelling

oxygen, a thicker composite interfacial oxide is formed with the existing thermal oxide, which **improves a passivation of the passivating film**. EX1003, ¶185.

G. Dependent Claim 6: The method of claim 1, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.

Yablonovitch in view of Kwark discloses this claim. EX1003, ¶186-187.

First, as discussed above in [1.b], Yablonovitch discloses a “thin” (**thickness selected**) **interface passivation layer**. *See* Section IX.C.3; EX1003, ¶186.

Further, it would have been obvious to a POSITA how the interface passivation layer **permits tunneling of electrical carriers through the interface passivation layer into the substrate** because it is a known phenomenon. Kwark further explains that the interfacial oxide (**the interface passivation layer**) is a “thin tunnelable oxide at the Si-SIPOS interface” (**has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate**). EX1017, 180. More specifically, Kwark explains that the physical properties and phenomenon that result in carrier transport properties are in relation to oxide thickness. EX1017, 181 (noting that oxide thickness is crucial to achieve a proper balance between low majority carrier series resistance and low hole tunnelling probabilities to avoid bulk resistivity); EX1003, ¶187.

H. Dependent Claim 7: The method of claim 1, wherein the thermally treating diffuses a portion of the conductive dopant

through the interface passivation layer into the substrate.

Yablonovitch in view of Kwark discloses this claim. EX1003, ¶188-190.

First, Yablonovitch in view of Kwark renders obvious claim 1, on which claim 7 depends. *See* Section IX.C (claim 1); EX1003, ¶189. Next, **thermally treating diffuses the conductive dopant through the interface passivation layer** corresponds to element [1.d.4]. *See* Section IX.C.8. As discussed above, Yablonovitch's discloses "a portion" of said conductive dopant that diffuses "into the substrate." *See* Section IX.C.8 (analysis of [1.d.4]); EX1003, ¶189.

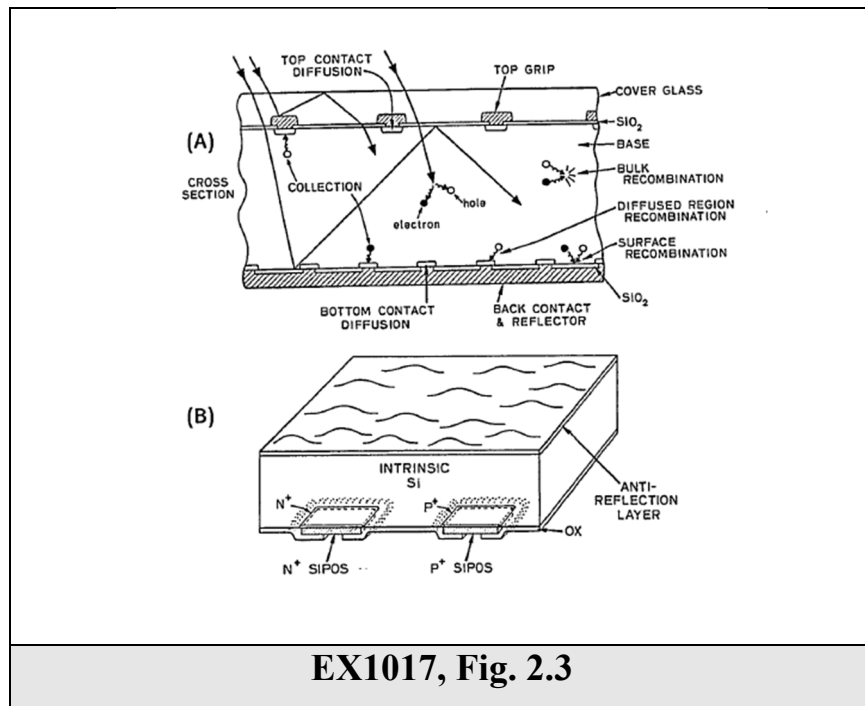
Specifically, during Yablonovitch's anneal step (9), the phosphorus dopant (**conductive dopant**) diffuses throughout the interface passivation layer and also into the c-Si substrate by roughly 2–5 nm (**diffuses a portion of the conductive dopant through the interface passivation layer into the substrate**). EX1005, 1212. The result is a "shallow n⁺ accumulation layer" at the wafer surface, essentially forming an n⁺ region caused by the presence of phosphorus dopant in the wafer directly beneath or through the interface oxide. EX1005, 1212; EX1003, ¶190.

I. Dependent Claim 8: The method of claim 1, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.

Yablonovitch in view of Kwark discloses this limitation. EX1003, ¶191-193.

Yablonovitch teaches that “[t]he open circuit voltage was measured under a simulator at 1.3 suns... An intensity slightly above one sun was chosen in order to partially compensate for the absence of **an antireflection coating on the silicon wafer.**” EX1005, 1211. A POSITA would understand this to mean that an anti-reflection film is present in Yablonovitch’s solar cell design because Yablonovitch assumes that it would be present and adjusts the sun intensity during simulation to account for the anti-reflection film in the solar cell design. EX1003, ¶192.

Moreover, a POSITA would understand that providing an anti-reflection field would provide more accurate results and the actual sun intensity can be applied, instead of adjusting for it numerically. EX1003, ¶193. Kwark explains, “the use of anti-reflection coatings (**an anti-reflective film**) and surface texturizing techniques [1] are common techniques employed to ensure that the incident light is tightly coupled to the bulk of the cell where generation takes place.” EX1017, 10. A POSITA would understand that such teachings provide **an anti-reflective film over the conductive upper surface of the passivating film** because doing so minimizes the light coupled into the cell while maintaining the passivating layer and results in more accurate simulation in Yablonovitch. EX1003, ¶193. Kwark depicts an anti-reflection layer below in Fig. 2.3 below.



J. Dependent Claim 9: The method of claim 1, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

Yablonovitch discloses this claim. EX1003, ¶194.

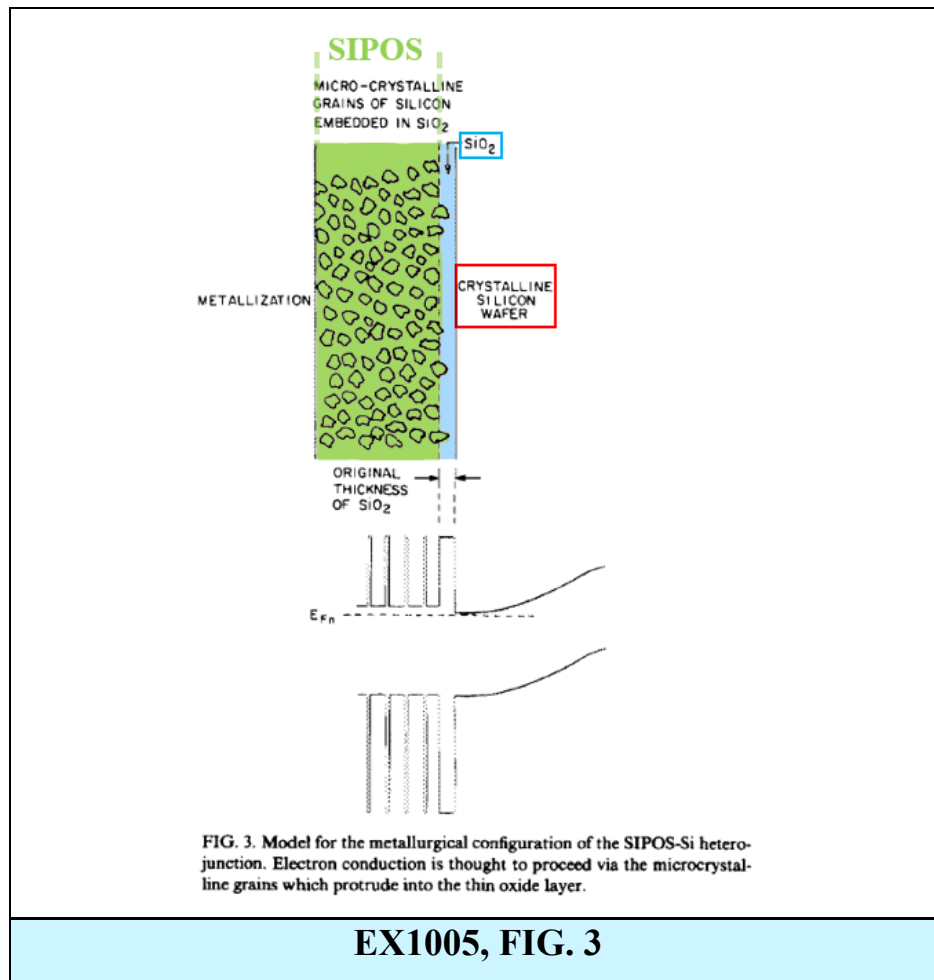
To the extent [1.e] is limiting, the dopant conductive pathways provide direct electrical connection between the electrode and the substrate. *See, supra*, Section IX.C.9 ([1.3]); EX1003, ¶194. Here, the electrode only electrically connects to the substrate due to the phosphorous dopant since there are no other electrical connections. Further, the electrical connection would not occur without the phosphorous dopant. EX1003, ¶194.

IX. GROUND 2: YABLONOVITCH IN VIEW OF KWARK AND BATRA RENDER OBVIOUS CLAIM 5

A. Motivation to Combine

A POSITA would have been motivated to apply the teachings of Batra to Yablonovitch in view of Kwarik. *See* Section IX.A (motivation to combine Yablonovitch and Kwarik); EX1003, ¶195.

A POSITA would have been motivated to look to Batra to understand details about Yablonovitch's solar cell design. EX1003, ¶196. Specifically, Yablonovitch provides an interface passivation layer over the substrate with Step (6) of Yablonovitch's processing sequence. *See, supra*, Section IX.C.3. Yablonovitch provides a passivating film over the interface passivating layer with Steps (7)-(9). *See, supra*, Section IX.C.4. Yablonovitch illustrates the resulting structure in Figure 3, reproduced below. EX1005, Fig. 3; EX1003, ¶196.



In addition, the thermal anneal of steps (8) and (9) “crystallizes, at least in part, the passivating film to establish a crystallized passivating film,” which is seen in Yablonovitch’s Figure 3 above. *See also, supra*, Section IX.D (claim 2). In its Figure 3 and description, Yablonovitch omits details of the effect of the passivating layer formed on the substrate. Indeed, Figure 3 of Yablonovitch does not depict the substrate (“crystalline silicon wafer”) layer and interface passivation layer (“SiO₂”). A POSITA would understand such information is necessary to understand whether

the interface passivation layer **protects the substrate from crystallization or re-crystallization** during thermal annealing. EX1003, ¶197.

A POSITA reviewing Yablonovitch would therefore understand the importance of determining the effect of the interface passivation layer (“SiO₂”) on the substrate (“crystalline silicon wafer”) during anneal and would look to Batra for those details. EX1003, ¶198. A POSITA would look to Batra to understand the details missing from Yablonovitch because Batra taught and understood those details. EX1003, ¶198. A POSITA would have understood Batra’s teachings to be beneficial to Yablonovitch since it teaches methods applicable to the passivation layer that enhance efficiency and uniformity of dopant diffusion. EX1003, ¶198.

B. Reasonable Expectation of Success

A POSITA would have a reasonable expectation of success combining the teachings Batra with Yablonovitch, as discussed above in Section IX.B (reasonable expectation of success to combine Yablonovitch and Kwark). EX1003, ¶199.

Batra is in a same field to Yablonovitch and Kwark, dopant diffusion in semiconductor structures. *See* Section VI (overview of the prior art); EX1003, ¶200. Batra’s teachings on nonuniformity in junctions would have been obvious to a POSITA to rely on these teachings for Yablonovitch’s interface passivation layer. *See* Section VI.C (overview of Batra); EX1003, ¶200. A POSITA would have also had the skill to implement and reasonable expectation of success in achieving such

a modification because would naturally be a consideration in implementing Yablonovitch to ensure efficiency. EX1003, ¶200.

C. Dependent Claim 5

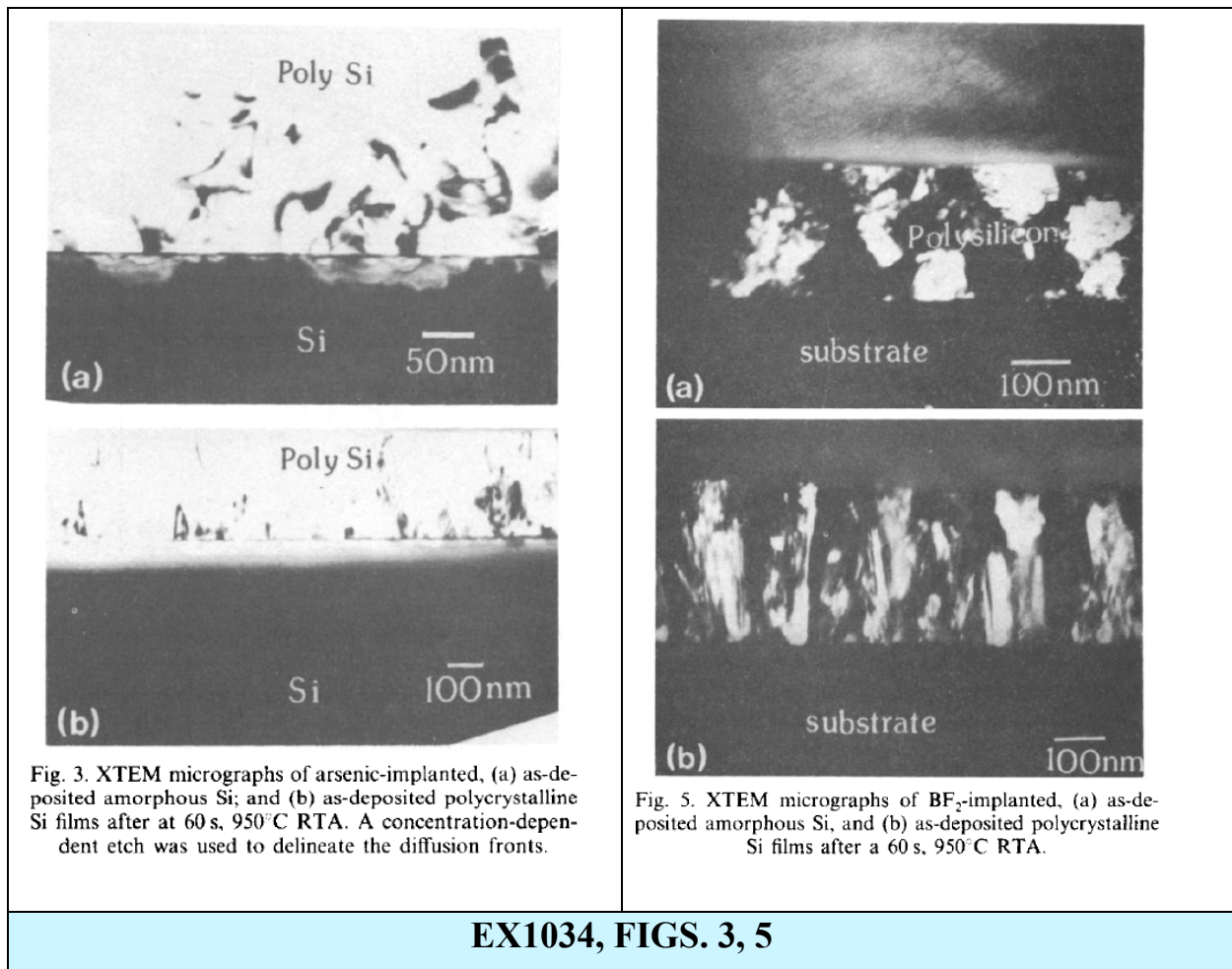
- 1. The method of claim 2, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.**

Yablonovitch in view of Kwark and further in view of Batra renders obvious this limitation. EX1003, ¶201-204.

First, Yablonovitch in view of Kwark renders obvious claim 2, on which claim 5 depends. *See* Section IX.D (explaining how thermally treating the substrate crystallizes the passivating film establishes a crystallized passivating film); EX1003, ¶202.

A POSITA would have found it obvious to refer to the teachings of Batra to Yablonovitch for the properties of an interface passivation layer formed over the substrate in Yablonovitch after annealing has completed. EX1003, ¶203. Specifically, Yablonovitch discloses that an interface passivation layer is formed over the substrate and a passivating film is formed over the interface passivation layer, and a thermal treatment (i.e., anneal) is performed to crystalize the passivating film. *See, supra*, Sections IX.C.3 ([1.b]), IX.C.4 ([1.c]), IX.D (claim 2). Batra teaches how thermal annealing affects the substrate's crystal structure and dopant

diffusion. EX1034, 955 (describing how higher-temperature or longer anneals cause dopants to diffuse deeper in the substrate making the junctions more uniform). Batra's Figures 3 and 5 (below) illustrate that the crystallization of the Poly-Si does not create damage in the substrate and vice versa. EX1034, Figs. 3, 5. A POSITA would understand that the lack of damage thereof is due to an interfacial oxide. EX1034, Figs. 3, 5; EX1003, ¶203. Therefore, the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film. EX1003, ¶203.



Batra explains that annealing alters the crystal structure and dopant distribution, and that high-temperature or longer anneals produce a more uniform junction, which fixes pn junction lateral non-uniformity by evening out dopant distribution in the passivating film. EX1034, 959-60. Lateral uniformities of the junction or other structural defects in the substrate can lead to an increase of the leakage current (i.e. J_0). *Id.*, 959-960 (“for higher thermal budget anneals the leakage current decreases... not only because the junctions become deeper, but also because they become more uniform laterally as any doping inhomogeneities in the substrate get averaged out as the dopants diffuse in further”, “higher-thermal-budget anneals result in lower leakage currents... because any doping inhomogeneities get smeared out, and also because the depletion region cannot probe the polycrystalline Si-single crystal Si interface as the junction gets deeper”). A POSITA would have recognized that the junctions are affected by the crystallization or re-crystallization structural changes occurring to the substrate. EX1003, ¶204.

X. SECONDARY CONSIDERATIONS

There are no secondary considerations known to Petitioner that affect, let alone overcome, this strong case of obviousness. Should Patent Owner proffer any relevant evidence of secondary considerations, Petitioner reserves the right to address.

XI. CONCLUSION

For these reasons, Petitioner respectfully requests institution.

Dated: August 15, 2025

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CLAIM LISTING APPENDIX

1-9

- [1.pre] A method of fabricating a solar cell, comprising:
 - [1.a] providing a substrate;
 - [1.b] providing an interface passivation layer over the substrate;
 - [1.c] providing a passivating film over the interface passivation layer, the passivating film comprising a passivating material and a conductive dopant;
 - [1.d] wherein providing the interface passivation layer and providing the passivating film comprise:
 - [1.d.1] providing an amorphous silicon-containing compound over an upper surface of the substrate, the compound comprising oxygen dopant and the conductive dopant;
 - [1.d.2] thermally treating the amorphous silicon-containing compound to diffuse the oxygen dopant, at least in part, into the upper surface of the substrate to form an oxide layer over the substrate, the oxide layer defining the interface passivation layer; and
 - [1.d.3] wherein remaining amorphous silicon-containing compound above the oxide layer defines the passivating film; and
 - [1.d.4] wherein the thermally treating also diffuses at least a portion of the conductive dopant throughout the interface passivation layer to facilitate electrical connection to the substrate; and
 - [1.e] providing at least one electrode over the passivating film, wherein the conductive dopant within the passivating film and throughout the interface passivation layer provides direct electrical connection between the at least one electrode and the substrate.
- [2] The method of claim 1, wherein the thermally treating crystallizes, at least in part, the passivating film to establish a crystallized passivating film.
- [3] The method of claim 2, wherein the crystallized passivating film is a transparent film.
- [4] The method of claim 2, wherein the crystallization of the passivating film improves a passivation of the passivating film.

- [5] The method of claim 2, wherein the interface passivation layer protects the substrate from crystallization or re-crystallization during the thermally treating and crystallization of the passivating film.
- [6] The method of claim 1, wherein the interface passivation layer has a thickness selected to permit tunneling of electrical carriers through the interface passivation layer into the substrate.
- [7] The method of claim 1, wherein the thermally treating diffuses a portion of the conductive dopant through the interface passivation layer into the substrate.
- [8] The method of claim 1, further comprising providing an anti-reflective film over the conductive upper surface of the passivating film.
- [9] The method of claim 1, wherein the at least one electrode only electrically connects to the substrate through the passivating film via the conductive dopant.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing
PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 9,666,732
exclusive of the parts exempted as provided in 37 C.F.R. §42.24(a), contains 12,264
words and therefore complies with the type-volume limitations of 37 C.F.R.
§42.24(a).

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,666,732 AND EXHIBITS EX1001-1035** are being served on August 15, 2025, via FedEx overnight mail on counsel of record for U.S. Patent No. 9,666,732 as addressed below:

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