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Silicon-based passivating contacts: The TOPCon route

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Abstract

Passivating contacts based on poly-Si/SiO_x structures also known as TOPCon (tunnel oxide passivated contacts) have a great potential to improve the efficiency of crystalline silicon solar cells, resulting in more than 26% and 24% for laboratory and industrial cells, respectively. This publication gives an overview of the historical development of such contact structures which have started already in the 1980s and describes the current state-of-the-art in laboratory and industry. In order to demonstrate the great variety of scientific and technological research, four different research topics are addressed in more detail: (i) the superior passivation quality of TOPCon structures made it necessary to re-parametrize intrinsic recombination in silicon, (ii) the control of diffusion of dopants through the intermediate SiO_x layer is essential to optimize passivation and transport properties, (iii) single-sided deposition of the poly-Si layer would reduce process complexity for industrial TOPCon cells, and (iv) silicon-based tunnel junctions for perovskite–silicon tandem cells can be fabricated using the TOPCon technology.

KEYWORDS
high-efficiency silicon solar cells, passivating contacts, polysilicon

1 | INTRODUCTION

1.1 | Fundamentals of passivating contacts

The basic working principle of a solar cell can be distinguished in two fundamental processes. First, light is absorbed in the absorber region of the cell and each photon generates an electron and hole. In order to describe the electron and hole concentration, n and p, two quasi-Fermi levels, E_{Fn} and E_{Fp}, are required, respectively. The splitting of the quasi-Fermi levels (QFL) becomes larger with increased photogeneration and reduced carrier recombination. Often, this splitting of the QFLs is related to an internal voltage of the solar cell, iV_{oc}.[1]

$$iV_{OC} = (E_{F,n} - E_{F,p})/q \tag{1-1}$$

where q is the elementary charge.

In the second step, the two carrier types have to be separated and transferred to the n- and p-electrode of the cell. This is accomplished by a layer or layer system with a high carrier selectivity placed under the p- and n-electrode. The important parameter to describe the selectivity is the asymmetry of conductivity, σ_n and σ_p, for

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electrons and holes, respectively.[2] For an electron-selective layer the following relationship should be satisfied:

$$\sigma_n = q\mu_n n \gg \sigma_p = q\mu_p p \tag{1-2}$$

where μ_n and μ_p are the carrier mobility for electrons and holes, respectively.

If the carrier selectivity is not sufficient, the external voltage at the electrodes, V_{oc}, is lower than iV_{oc}.[3,4] A selective contact of high quality should allow for an effective carrier transport of the majority carriers to the electrodes and also reduce the recombination of minority carriers. A practical metrics was suggested by Brendel et al.[5] The contact resistance, ρ_c, is used to quantify the carrier transport and the recombination parameter, J_c, to describe the carrier recombination. They showed that the following expression is a very good metrics to predict the efficiency potential of a solar cell:

$$S_{10} = log\left(\frac{V_{th}}{J_c \rho_c}\right) \tag{1-3}$$

where V_{th} is the thermal voltage. S_{10} can be used to determine the efficiency potential of the contact structure.

To emphasize the low recombination activity at a high-quality selective contact, often the attribute "passivating" is added, although such characteristic is already included in a high selectivity. In this article we will also use the term "passivating contacts" since it is now the acronym as used by the silicon PV community for a contact system beyond the classical diffused pn-junction.

1.2 | Types of passivating contacts

In classical silicon solar cells, the selective layers are created by near-surface n- or p-type doping of the silicon absorber, resulting in a diffused pn- and high-low-junctions. Silicon solar cells using this approach have achieved a maximum efficiency of 25%.[6] A major limitation of such cells is the increased Auger-recombination due to the high doping concentration in the diffused regions. The principal idea to overcome this limitation is to *decouple* the contact layer system from the absorber. For other types of solar cells this idea is not new at all. In fact, decoupled selective contacts are required for many PV technologies since the formation of diffused pn-junctions is technically not possible. Typical examples for such decoupled selective contacts are PEDOT:PSS layers in organic solar cells[7] or TiO_2 electrodes in perovskite solar cells.[8] For crystalline silicon solar cells, however, it took more than 50 years since the first diffused pn-junctions in the Bell labs[9] that this approach gained significant importance. In the following four prominent passivating contact technologies are shortly introduced:

i. *a-Si/c-Si heterojunctions*: The layer system consists of a very thin intrinsic hydrogenated amorphous silicon layer (a-Si:H(i)) to reduce the recombination at the crystalline silicon interface and a second amorphous highly doped (either a-Si:H(n) or a-Si:H(p)) to achieve carrier selectivity. This a-Si:H(i) intermediate layer was introduced by Sanyo in the 1990s and also led to the trade name (HIT = heterojunction with intrinsic thin-layer).[10] It is important to note that the carrier selectivity is achieved by an induced junction in the c-Si absorber.[3] Therefore, the idealized image of a total decoupling of the contact layer system and the absorber is limited. There is no chemical interaction between contact layer system and c-Si but still an electronical manipulation of the absorber. The passivation quality of a-Si/c-Si heterojunction is excellent which allowed to achieve the actual world record efficiency of 26.7% for silicon solar cells.[11] However, the significant parasitic absorption of light in the a-Si layers made it necessary to use an interdigitated back contact (IBC) cell structure. Both-sides contacted heterojunction cells were commercialized by Sanyo and then later by Panasonic. After a longer time of stagnation in production, strong industrial activities to ramp up production could be observed in the last years.[12]

ii. *Transparent layers with high or low work functions*: In this case the carrier selectivity is achieved by a band bending in the c-Si absorber which is induced by a metal oxide or an organic layer with either high or low work function.[13] Due to the high recombination at the interface metal oxide/c-Si, it is necessary to insert an intermediate passivation layer such as a-Si:H(i). Solar cells with MoO_x/a-Si:H(i) as hole contact system show a high efficiency potential.[14,15] Using additionally a layer system, a-Si:H(i)/TiO_x/LiF/Al made it possible to fabricate "dopant-free" heterojunction solar cells.[16] However, it was shown that the stability of some of the used metal oxide layers is not sufficient[15] which limits the applicability of this technology somehow.

iii. *Metal–insulator silicon solar cells (MIS)*: The idea to use a MIS structures in silicon solar cells was already suggested in 1970s.[17,18] The metal front contacts were separated by a thin tunnel oxide in order to reduce the recombination at the contact system significantly. The work function difference between metal and semiconductor led to an induced junction. The junction between the front metal contacts could be established either by an inversion layer (IL) enhanced by charges incorporated in a SiN_x layer[19] or by an additional phosphorus diffusion resulting in the so-called MIS-n^+p (MINP) cell structure.[20] Such MINP cells showed a high open-circuit voltage of 678 mV[21] and a very good blue response. MIS-IL cells were later produced by the German company Nukem.[22]

iv. *Doped polycrystalline silicon on SiO_2 (SIS)*: Similar to MIS, in this approach a thin oxide layer is used to passivate the c-Si interface. However, instead of a metal, a highly doped polycrystalline silicon (poly-Si hereafter) layer is responsible for achieving the carrier selectivity. SIS structures were used for microelectronic devices as high-speed bipolar junction transistors.[23] After the deposition of the layer system (SiO_x + poly-Si), an anneal at temperatures between 800°C and 1100°C is applied. It was shown that at very high temperatures the interfacial oxide breaks up and the recombination characteristics of the bipolar devices deteriorate. The

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importance of an intermediate oxide was also pointed out for bipolar emitters by Graaf et al.[24] The introduction of the technology to silicon photovoltaics is described in the following section in more detail.

1.3 | Technology and historical development of polysilicon-based passivating contacts

Already in the 1980s, Overstraeten suggested to use polysilicon layers under the contacts to reduce recombination in silicon solar cells.[25] Green et al. extended their work on MIS and MINP solar cells by using SIS structures ("We have also used degenerately doped polycrystalline silicon as the "metal" layer in our devices").[26] Promising open-circuit voltages in the range of 660–665 mV showed the potential of this approach. Another approach using SIPOS (semi-insulating poly-Si) followed at the Stanford University[27,28] led to excellent open-circuit voltages of 720 mV on solar cell test structures.[29] Gan and Swanson[30] followed an approach with rather thick thermally grown oxides (≈ 2 nm) which cannot act as tunnel oxides anymore. Therefore, a high-temperature step was used to generate pinholes in the oxide and thus enable a direct current flow.

After these strong activities in the 1980s, research on poly-Si/SiO_x contacts sank into a deep slumber in the coming decade. However, the excellent potential of such structures was not forgotten. In his visionary paper "Approaching the 29% limit efficiency of silicon solar cells" in 2005[31] Richard Swanson pointed out the need for new contacts with low J_0 ("What is needed is a new contact that has J_0 less than 5 fA/cm^2 and makes good majority carrier contact") and reminded the community of the old activities ("On another front, the author supervised a PhD student in 1985 who developed oxygen doped poly silicon emitters (SIPOS) with J_0 less than 10 fA/cm^2."). This can be regarded as a starting point for the renaissance of poly-Si-based passivating contacts for silicon solar cells.

SunPower used passivating contacts for their third generation (Gen III) of high-efficiency IBC solar cells.[32,33] A comparison of power losses of Gen III (passivating emitters) with Gen II (diffused emitters) showed a strong reduction of carrier losses at the contacts from 2.4% to 0.8%. Excellent open-circuit voltages of 727 mV were reported. No details of the fabrication process of these passivating contacts have been published. Given the respective expertise of SunPower demonstrated by their patent portfolio, it appears likely that poly-Si/SiO_x contacts were used.

TetraSun developed an advanced cell technology ("TetraCell") for both-sides contacted solar cells[34] resulting in very high open-circuit voltages of 718 mV. The excellent recombination characteristics were attributed to a "shielding of the contacts" indeed a nice synonym for passivating contacts. The TetraCell architecture featured passivating contacts on front and rear. TetraSun's patent portfolio suggests that their passivating contact technology is based on poly-Si/SiO_2 structures.

Borden et al.[35] fabricated poly-Si/SiO_2 with hyper-abrupt junctions using microelectronic equipment. The tunnel oxides were fabricated using RTO or chemical oxidation. The final solar cell showed promising contact passivating quality; however, the open-circuit voltage was limited by the rather thick silicon wafers (770 μm).

The first hybrid cell structure with a diffused front emitter (p^+ boron) and poly-Si/SiO_2 rear contact was published by Feldmann et al.[36,37] in 2013. In the same publication the term TOPCon (tunnel oxide passivated contacts) was coined. Using the TOPCon technology, Feldmann et al. were able to demonstrate a high efficiency of 23% with a high open-circuit voltage of 698 mV. As notable as the high voltage was the high fill factor demonstrating the excellent majority transport over the tunnel oxide. The n-TOPCon structure of these first cells was realized by growing a thin interfacial oxide in HNO_3, depositing a phosphorus-doped Si-rich SiC_x layer by plasma-enhanced chemical vapor deposition (PECVD), thermal annealing at 800–900°C, and a hydrogen passivation step. The thermal annealing leads to a diffusion of dopant into the crystalline silicon absorber. In simulation it was shown that a slight doping profile in the bulk facilitates the majority carrier transport over the tunnel oxide.[38] Therefore, it should be noted that poly-Si/SiO_2 contact systems cannot be regarded as "decoupled" from the c-Si absorber. There is a strong electronical and chemical interaction, that is, band bending and in-diffusion, respectively.

The recombination properties of the first n-type TOPCon cells were mainly limited by the recombination at the front contacts. In fact, the introduction of a local p^{++} boron diffusion under the front contacts and other improvements led to a record efficiency of 25.8% ($V_{oc} = 724$ mV) on *n*-type TOPCon cells.[39,40] A deep analysis of the recombination and transport characteristics within TOPCon cells led to the conclusion that a rear emitter configuration on *p*-type silicon might be attractive as well. Indeed, TOPCon back junction cells (TOPCore) on *p*-type silicon led to a record efficiency for both-sides contacted solar cells ($\eta = 26\%$, $V_{oc} = 732$ mV; see Table 1).[41]

Also in 2013, Römer et al. published first results on ISFH's work on the POLO technology.[42,43] They were able to demonstrate low J_0 of less than 10 fA/cm^2. A major difference to the TOPCon approach of Fraunhofer ISE was the use of a rather thick intermediate oxide in the range of 2.4 to 3.6 nm which cannot act a direct tunnel oxide anymore (similar to the approach of Gan and Swanson.[30]) This makes it necessary to apply a high-temperature anneal at $T > 1000$°C to break up the oxide. The POLO approach was mainly used for IBC solar cells and led to a record efficiency of 26.1% ($V_{oc} = 727$ mV).[44,45]

The early publications of Fraunhofer ISE and ISFH triggered a vivid renaissance of research on poly-Si/SiO_2 based passivating contacts. This led to many interesting technological and scientific results.* Good overviews about recent developments can be found in previous studies.[40,46–49]

1.4 | Majority transport in TOPCon structures

In the last years, there was a lively scientific discussion whether the majority carrier transport in poly-Si/SiO_x structures has to be

*... and to even more synonyms for the technology.

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Configuration	V_{oc} (mV)	J_{sc} (mA cm^{-2})	*FF* (%)	*η* (%)
Front junction, 1 Ω cm, *n*-type	724.1	42.87	83.1	25.8
Rear junction, 1 Ω cm, *p*-type	732.3	42.05	84.3	26.0

Abbreviation: TOPcon, tunnel oxide passivated contacts.

TABLE 1 Calibrated IV parameters of record laboratory TOPCon cells (A = 4 cm^2) with front or rear junction on n-type and p-type silicon[50]

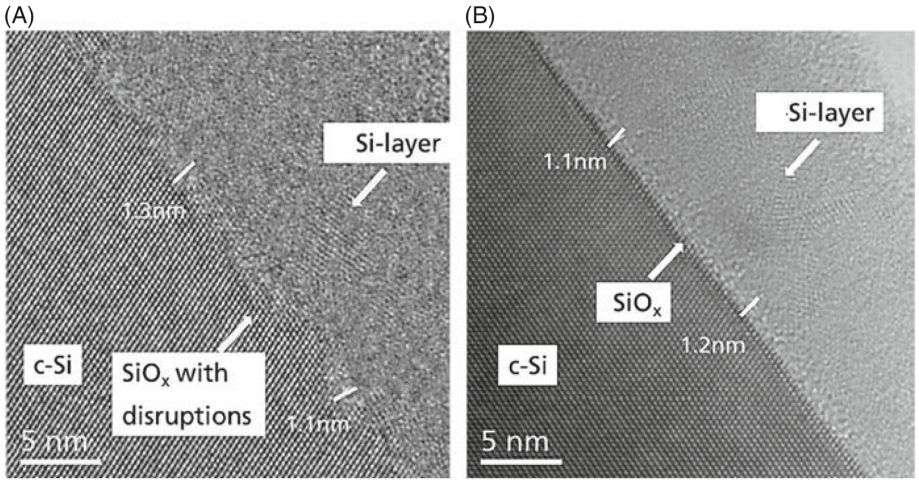

FIGURE 1 TEM cross-sections of tunnel oxide passivated contacts (TOPCon) samples (A) with and (B) without local disruptions of the tunnel oxide. Adapted from Moldovan et al.[56]

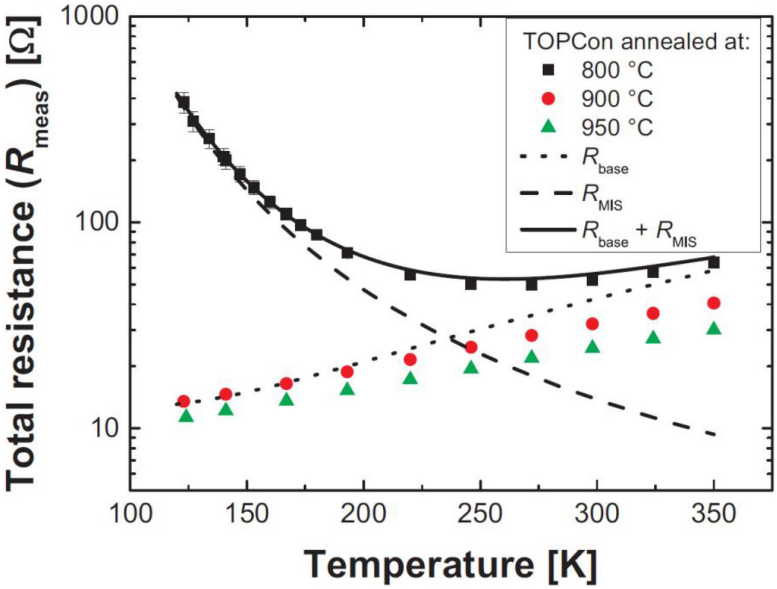

FIGURE 2 Measured temperature-dependent resistance of poly-Si/SiO_2 structures annealed at different temperatures. For lower anneal temperatures (800°C) a tunnel component R_{MIS} is needed to model the measured date. For higher anneal temperatures (900°C and 950°C) the total resistance is dominated by an ohmic behavior, due to creation pinholes in the tunneling oxide. Taken from Feldmann et al.[51]

described by a tunnel mechanisms or is more due to a direct current flow via pinholes in the thin oxide.[51–55] The dominating mechanism is determined by the type of oxide and annealing temperatures during processing. Figure 1 shows TEM cross-section of two samples both annealed at 900°C but with HNO_3-grown oxide (a) and UV/O_3 oxide (b).[56] While for the HNO_3 sample pinholes are observed and thus a direct current flow is possible, the UV/O_3 oxide seems to be intact and thus a tunneling mechanism. It has to be kept in mind that a transmission electron microscopy (TEM) cross-section covers only a very small region of the sample and therefore does not allow for general conclusions. A method to determine of pinhole density by etching was suggested by Tetzlaff et al.[57] The current flow through pinholes was visualized by Kale et al. using electron beam-induced current (EBIC).[58]

Feldmann et al. have conducted temperature-dependent measurement of the resistance of TOPCon structure (Figure 2).[51] The temperature dependence allows for a separation of tunnel currents and direct current flow. While for samples with low annealing temperature (800°C) and intact SiO_2 layer, tunnel currents have to be considered to describe the measurement; for samples annealed at higher

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temperatures (900°C) pinholes are created and the carrier transport is dominated by a direct current flow.

For the POLO technology which uses rather thick oxides and high annealing temperatures as used by Gan and Swanson, a direct current flow through pinholes describes the characteristics of the samples very well.[52,53]

1.5 | Industrial process routes for TOPCon cells (i-TOPCon)

The efficiency potential of TOPCon cells and its compatibility with the passivated emitter and rear cell (PERC) process flow make this technology very interesting for a transfer to industrial production. However, it is well known that mass production of solar cells has a lot of strict requirements.[59,60] Therefore, for mass production of industrial TOPCon (i-TOPCon) cells[61] the evaluation of reliable and high-throughput technologies for the cell fabrication is essential. i-TOPCon cells feature an *n*-type base with the rear side passivated by *n*-type TOPCon. The front side boron emitter is passivated by an Al_2O_3/SiN_x stack. The rear TOPCon structure is covered by a SiN_x layer which also serves as hydrogen source and improves the optical properties of the solar cell. Excellent efficiencies of 24% and more have been already demonstrated[62–65] for the i-TOPCon cell structure. Some announcements for TOPCon cells even claim efficiencies of more than 25%.[66,67] However, for these cells the exact cell structure (especially the front side configuration) is not known.

The best industrial process route to fabricate i-TOPCon cells is still under investigation. As pointed out by Chen et al.,[68] this is a situation similar to the industrial introduction of the PERC technology in 2014. Figure 3 gives an overview of different aspects and research topics in the fabrication of i-TOPCon solar cells. Out of these, there are two topics we want to discuss further in the following, that is, the polysilicon (TOPCon) deposition and the metallization of the solar cells.

For the deposition of the TOPCon layer, two technologies are mainly investigated, low-pressure chemical vapor deposition (LPCVD) as well as PECVD. Here, LPCVD is a widespread technology and industrial-size tools are often used for the industrial fabrication of i-TOPCon cells. However, since industrial-scale PECVD of TOPCon was demonstrated[71,72] the market share of PECVD is expected to increase significantly.[73] Among others, the advantage of PECVD here is that it is easier to achieve in situ doping and the deposition is usually only applied to one side. However, this is only partially true, as a certain amount of wrap-around is expected, as will be discussed in one of the following sections.

Another important topic is the metallization of the cells. Based on the experience with PERC production, the technology of choice here would be screen-printing of silver or aluminum-silver pastes. However, due to the silver consumption and thus the influence of the silver price on the fabrication costs, alternative metallization concepts are investigated for this not yet fully established cell concept. One additional problem with the current screen-printing pastes is that rather thick poly-Si layers are required to prevent increased recombination.[74,75] An interesting alternative to screen-printing could be plating of contacts on TOPCon structures. In fact, a process sequence using laser ablation of the SiN_x and subsequent electroplating of nickel, copper, and an electroless silver capping, has

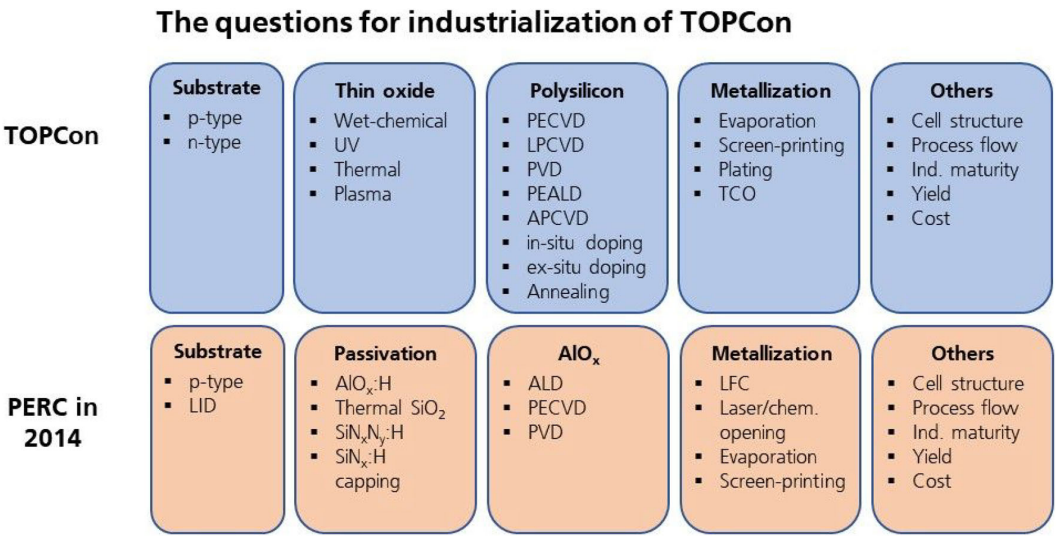

FIGURE 3 Overview of the technologies to be investigated for the fabrication of i-tunnel oxide passivated contacts (TOPCon) solar cells in comparison to the similar situation for passivated emitter and rear cell (PERC) in 2014. This graph was adapted from a conference presentation by Chen et al.[68] in 2019 and updated by additional technological options such as sputtered polysilicon layers[69] or plated contacts on TOPCon[70]

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shown encouraging results since a very low passivation damage was demonstrated for poly-Si thicknesses of below 100 nm.[75–77] Furthermore, as most of the silver is substituted by copper, the material costs can be decreased resulting in a significant reduction in total cost of ownership compared with screen-printing.[78] This approach was further applied to industrial precursors to investigate the feasibility of laser ablation and plating in direct comparison to reference solar cells metallized by screen-printing.[79] The results for either champion cell can be found in Table 2. The plated cells feature a small increase in V_{oc} from 708 to 709 mV and FF from 82.0% to 82.2% as well as a significant increase in J_{sc} from 40.4 to 40.9 mA/cm^2 resulting in a gain of almost 0.4%$_{abs}$ in the efficiency. This gain in the efficiency is attributed mostly to the reduced shading of the metal fingers as well as a decrease in the contact opening width.[79]

1.6 | The spectrum of TOPCon research: From surface passivation to tandem photovoltaics

In this article, we would like to discuss some recent investigations aiming to achieve both, a deeper scientific understanding and significant technological progress in the field of the TOPCon technology. The publication highlights the wide variety of fascinating scientific questions and technological challenges that TOPCon technology presents to the PV community.

The first part is dedicated to the excellent surface passivation quality which can be achieved with TOPCon structures. Indeed, amazingly high effective lifetimes up to 0.5 s (half a second!) have been measured, values which have not been achieved with pure dielectric surface passivation layers so far.

Subsequently, we discuss approaches to control the in-diffusion of dopants through the intermediate oxide. A new plasma-based oxidation technology is introduced.

Section 4 focuses on the deposition of the poly-Si using PECVD. As discussed before a major challenge is to restrict the layer only on one side of the wafer.

The last part describes the use of the TOPCon technology for the next generation of solar cells. Poly-Si(p$^+$)/poly-Si(n$^+$) layer systems with hyper-abrupt junction are used as tunnel diodes for the interconnection of perovskite/silicon tandem solar cells.

TABLE 2 IV results of full area (268 cm^2) bifacial i-TOPCon solar cells according to the metallization type measured by Fraunhofer ISE CalLab

Metallization	V_{oc} (mV)	J_{sc} (mA·cm^{-2})	*FF* (%)	η (%)
Plating	709	40.9	82.2	23.84
Screen-printing	708	40.4	82.0	23.46

Note: The screen-printed solar cell features the grid with 9 BB 106 fingers whereas the plated solar cell features 9 BB and 163 fingers with an LCO width of 5.5 μm on the front side. These values were taken from.[79]
Abbreviation: TOPcon, tunnel oxide passivated contacts.

2 | PASSIVATION QUALITY AND CARRIER LIFETIME

2.1 | Surface recombination velocity of TOPCon structures

TOPCon—and poly-Si/SiO_2 contacts in general—have demonstrated excellent surface passivation properties.[36,42,71,80] This led to the necessity to update the models for the intrinsic bulk recombination in silicon since the measured effective minority charge carrier lifetime was often found to be higher than the predicted intrinsic minority charge carrier lifetime.[81–83] In a recent study by Niewelt et al.[82] nine sets of crystalline silicon materials were passivated by TOPCon and the effective lifetime was determined. For more detail on the sample preparation and measurement setup, see previous research.[82,84] Since the thickness of the samples was varied in each set of samples, it was possible to separate between bulk and surface recombination.[85] Figure 4 shows the data relevant for the surface passivation from these data sets. In the left panel the injection-dependent surface recombination velocity S is shown for two of the materials including the fitted J_{0s} curves. The right panel shows the J_{0s} evaluated for eight data sets. Additionally, the panel gives the mean J_{0s} and the standard deviation. The injection-dependent evaluation shows that a large portion of the determined S values can be described using a J_{0s} model according to Kane and Swanson.[86] At low excess carrier densities Δn, deviations are possible if the effective lifetime of one or more samples is affected by bulk defect recombination or—in case of opposite bulk and surface polarities—an inversion layer at the surface.[87] At high $\Delta n \geq 1 \times 10^{16}$ cm^{-3}, a systematic deviation between the acquired values and the model was found. The origin of this deviation is currently unknown. For the range in-between, the J_{0s} could be evaluated very well using the model by Kane and Swanson and applying the method to multiple datasets yielded very similar values for J_{0s} across all datasets resulting $J_{0s,mean} = 0.64 \pm 0.09$ fA/cm^2 at 25°C.[†] It should be kept in mind that the low uncertainty here represents mostly statistical uncertainties in the evaluation of J_{0s}. However, for the lifetime evaluation, the systematic uncertainties are usually dominant; thus, the actual uncertainty is expected to be higher, approximately in the range of 30%–40% relative. Nevertheless, the low $J_{0s,mean}$ underlines the excellent surface passivation quality of TOPCon structures and the low standard deviation from the mean value demonstrates the excellent reproducibility of this surface passivation across a wide spread of doping concentrations on both *n*- and *p*-type crystalline silicon.

2.2 | Record lifetimes

The excellent surface passivation combined with the best-known pretreatment of the material led to extraordinarily high values for the

[†]It should be noted that the J_{0s} values resulting from the thickness variation experiment are independent of the chosen Auger model.

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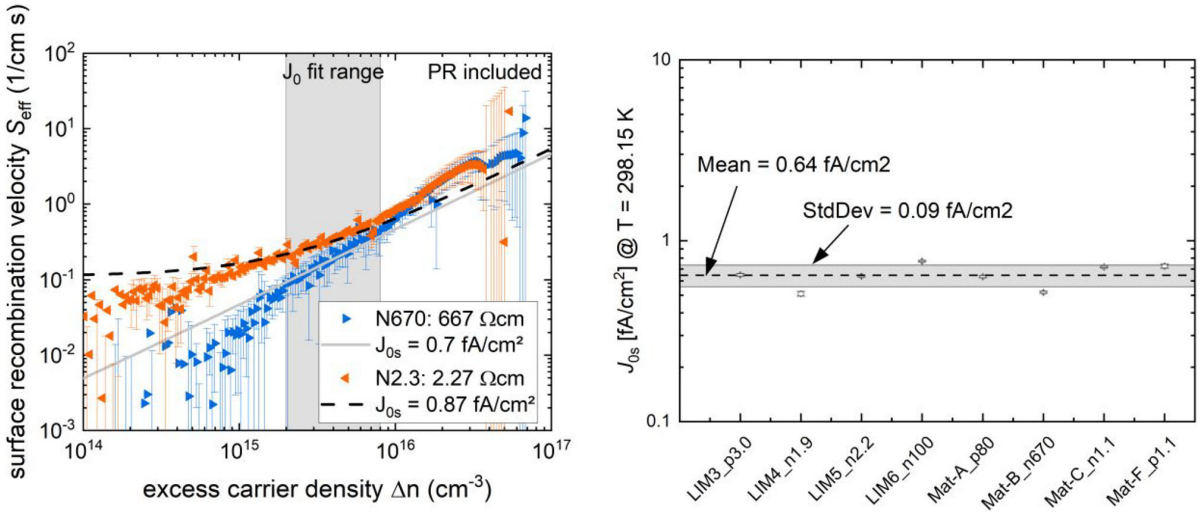

FIGURE 4 Left: values for surface recombination velocity for each evaluated Δn for two of the materials investigated in Niewelt et al.[82] (graph taken from Niewelt et al.[82]) The lines give the J_{0s} curve fitted to these datasets based on the model by Kane and Swanson.[86] The gray area indicates the fit range. The graph was taken from Niewelt et al.[82] Right: J_{0s} values extracted for all eight materials including the mean value for J_{0s} and the standard deviation from the mean value. For more information on the experiment, please refer to Niewelt et al.[82]

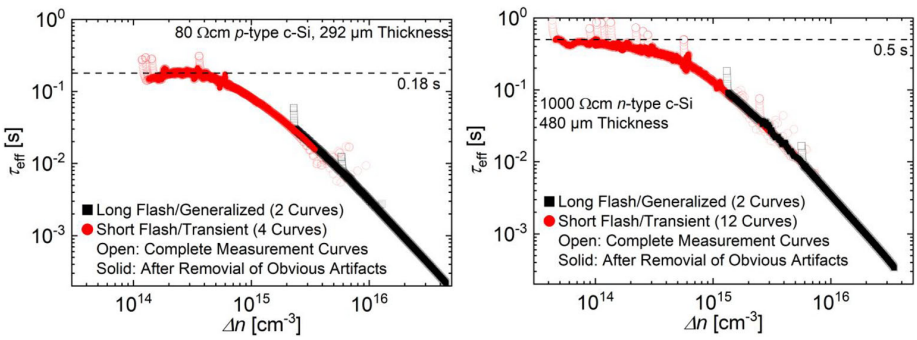

FIGURE 5 Effective minority charge carrier lifetime on lowly doped p-type (left) and n-type (right) crystalline silicon. The open symbols show the measured data fully, while the solid symbols highlight the more credible part of the curves removing some obvious measurement artifacts. Reproduced from,[84] reproduced under the terms of the creatives commons license CC-BY-NC 3.0

determined effective lifetime as recently reported by Steinhauser et al.[84] Figure 5 reproduces the highest lifetime curves from this publication. On *p*-type material, a maximum lifetime of 0.18 s was reached, while on *n*-type, the lifetime was even higher than 0.5 s. These values represent—to our knowledge—the highest lifetimes reported on each base doping type for crystalline silicon yet. At the maximum, both lifetime curves correspond to a minority charge carrier diffusion length of approximately 2.5 cm. To be able to achieve such high effective lifetimes, it is therefore essential to achieve a homogeneous surface passivation and to avoid surface defects (e.g. scratches), since even very few of such imperfections across the wafer can significantly impact the measured lifetime.

3 | CONTROLLING THE IN-DIFFUSION OF DOPANTS USING SIO_XN_Y TUNNEL OXIDES

3.1 | In-diffusion of dopants through the tunnel oxide

As discussed before, the annealing step at temperatures between 800°C and 1000°C leads to diffusion of dopants from the poly-Si layer into the c-Si bulk.[88] The resulting doping profile enhances the majority transport via the tunnel oxide[54] and also increases Auger recombination. Therefore, the doping profile has to be controlled properly to find a good compromise between these two constraints. It

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was shown that the type of tunnel oxide plays a decisive role for the thermal stability of the TOPCon system[56] and also for the in-diffusion and the resulting doping profiles.[89,90]

An interesting option for the control of the resulting doping profiles might be the use of SiO_xN_y layers. Recent publications have shown their successful application in *n*-type poly-Si/SiO_2 passivating contacts with very low J_0 values of 2–3 fA/cm^2.[91,92] Moreover, structures featuring SiO_xN_y revealed an increased firing stability presumably originating from increased Si–H bond energies due to incorporation of N which reduces H effusion from the interface during firing.[93] In this investigation we compare the performance of SiO_xN_y layers using plasma oxidation with thermally grown oxides.

3.2 | Sample preparation

Poly-Si/SiO_2-based passivating contacts were prepared using an industry-scale inline PECVD tool for oxidation as well as subsequent a-SiC_x deposition. To this end, plasma oxidation was carried out by employing a 2.45-GHz microwave source and N_2O precursor gas at a process temperature of 400°C. While other process parameters remained constant, the microwave peak plasma power and the velocity of the wafer carrier passing underneath was varied. Table 3 lists the process parameters of selected SiO_x layers and its resulting thickness t_{oxide} accessed by spectroscopic ellipsometry. Thermal oxide "TO" grown in a O_2/N_2 gas atmosphere serves as a reference.

The resulting plasma oxides PO1–PO3 reached a thickness of 1.1 to 1.6 nm which was in the same order of magnitude as the 1.2 nm thermally grown SiO_x. At a constant carrier velocity of 75 cm/min, SiO_x grew significantly thicker when increasing the plasma power from 1 to 1.6 kW_{peak} (compare PO1 and PO2). An increased microwave plasma power was reported to induce a higher atomic oxygen concentration in the plasma and thereby enhance oxidation of the substrate surface.[94] Furthermore, we found a decrease in the oxide thickness for higher carrier velocities at a constant plasma power of 1.6 kW_{peak}. This can be ascribed to a reduced exposure of the Si wafers to the oxidizing plasma at 150 cm/min.

The stoichiometry of ultra-thin SiO_x for TOPCon was extensively studied by means of X-ray photoelectron spectroscopy (XPS).[90,95]

TABLE 3 Selected plasma oxidation processes and thermal oxidation reference for interfacial SiO_x in TOPCon

Oxide	Temperature (°C)	Plasma power (kW_{peak})	Carrier velocity (cm/min)	t_{oxide} (nm)
TO	600	-	-	1.2
PO1	400	1	75	1.1
PO2	400	1.6	75	1.6
PO3	400	1.6	150	1.4

Note: t_{oxide} represents the mean value of three measurements on 10 samples each, standard deviation was < 0.1 nm and therefore neglectable small.
Abbreviation: TOPcon, tunnel oxide passivated contacts.

Figure 6 shows the molar fractions of N 1s and the detailed binding states of Si 2p, that is, Si elemental, substoichiometric SiO_x as well as SiO_2, for a native oxide, the thermally grown oxide TO and plasma oxide PO1. Both TO and PO1 revealed a significantly higher amount of SiO_2 compared with a native oxide grown at ambient air. However, plasma oxide PO1 is not only thinner but also less stoichiometric than 1.2-nm thermal oxide TO. Notably, XPS analysis further confirmed the incorporation of nitrogen into the oxide solely during plasma oxidation. The molar fraction of N 1 s binding states is approximately 1%. The amount of incorporated nitrogen is expected to increase with increasing oxidation time[95–97] due to lower carrier velocities.

The SiO_x layers listed in Table 3 were further implemented into symmetric *n*- and *p*-type TOPCon test structures with planar surface morphology. After oxidation, the wafers were either coated with P-doped a-SiC_x (n) or a stack of a-Si(i) and B-doped a-SiC_x (p) (without breaking the vacuum after plasma oxidation in the same tool). For process details of a-SiC_x depositions, please see Harter et al.[98] Subsequently, the samples were annealed at T_{anneal} in the range of 800°C to 1000°C for 10 min under N_2 atmosphere and exposed to a remote plasma hydrogenation step (RPHP) afterwards.

3.3 | Passivation quality

Figure 6 compares the recombination current density J_{0s} plotted over the annealing temperature T_{anneal} of *n*-type and *p*-type TOPCon with TO and the three selected plasma oxides PO1–PO3 after hydrogenation.

n-type TOPCon samples reached an excellent passivation quality with $J_{0s} \leq 1$ fA/cm^2 with all plasma oxides—although at different T_{anneal}—which was a similar level compared with the TO reference process. However, the structures exhibited a different thermal stability upon high-temperature annealing. With the thinnest 1.1-nm

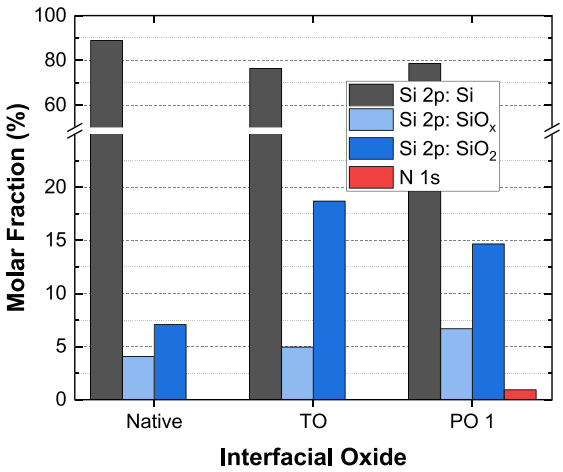

FIGURE 6 Molar fraction of N 1s and Si 2p binding states of a native oxide, thermally grown oxide (TO) and nitrous plasma oxide (PO1)

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plasma oxide PO1, J_{0s} was stable up to $T_{anneal} = 875°C$ but strongly degraded when annealed at higher temperatures. Structures with a slightly thicker and more stoichiometric 1.2 nm TO behaved similarly, but they took their lowest J_{0s} value at a higher T_{anneal} of 900°C. The thicker oxides PO2 and PO3 which were fabricated with an increased plasma power were more stable up to 950°C annealing.

However, *p*-type TOPCon structures exhibited a different behavior. Similar to TOPCon samples with the thermal oxide,[90] the passivation quality increased with increasing T_{anneal} of maximum 950°C with the two plasma oxides PO1 and PO3. Data at higher T_{anneal} and for PO2 are not available. Noteworthy, the thinner PO1 even outperformed PO3 at $T_{anneal} = 950°C$ ($J_{0s} = 9$ fA/cm^2 compared with 12 fA/cm^2).

The corresponding dopant diffusion profiles for *n*- and *p*-type TOPCon samples are shown in Figure 7A and B), respectively.

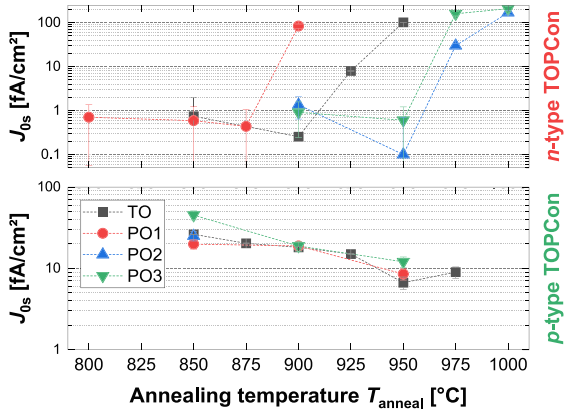

FIGURE 7 Recombination current density J_{0s} after hydrogenation over T_{anneal} for n-type (top) and p-type (bottom) TOPCon structures with thermally (TO) or different plasma oxides (PO1-3). Error bars represent J_{0s} uncertainties calculated by error propagation from uncertainties of input parameters and models

After annealing *n*-type TOPCon at 900°C, the P dopant diffusion from poly-Si into the c-Si substrate was significantly enhanced with a thin 1.1-nm PO1 compared with the thermal oxide (Figure 8A). Moreover, a high dopant concentration at the Si/SiO_x interface of $N_{D,\ surf} = 3.6 \times 10^{19}$ cm^{-3} (PO1) compared with 6.4×10^{18} cm^{-3} (TO) was measured. The thicker, 1.4-nm-thick PO3, however, effectively blocked P diffusion resulting in a very shallow doping profile. Excessive dopant diffusion can lead to increased recombination rates due to the high Auger recombination in the heavily doped c-Si region[99,100] and thereby can result in a significant limitation in the cell efficiency.

The B diffusion through TO and PO3 depicted in Figure 8B also showed a Gaussian-shape but slightly deeper profile and higher $N_{D,\ surf}$ after 950°C annealing. Noteworthy, B diffusion through nitrous PO1 was clearly reduced and revealed a similar shape to pure TO.

The contact resistivity ρ_c of *n*-type TOPCon featuring plasma oxides PO1 and thermal oxide was ≤ 2 mΩ cm^2 after annealing at 900°C. With PO3, a higher annealing temperature of at least 950°C for both *n*- and *p*-type TOPCon was necessary to enable efficient carrier transport.

3.4 | Effect of nitrogen incorporation in SiO_xN_y on dopant diffusion

Studies on MOS devices revealed that P diffusion is effectively suppressed by a 2-nm gate oxide while B readily segregates into the oxide.[88,101] In poly-Si/SiO_x passivating contacts this can adversely affect the passivation quality. The incorporation of N into the interfacial oxide during N_2O plasma oxidation or subsequent nitridation suppresses B penetration.[102,103] In more detail, a nitrogen-rich layer near the Si/SiO_2 interface was reported to potentially lower the B segregation coefficient compared with pure SiO_2 layers.[104] Other studies suggested the formation of B^+-N bonds acting as deep trapped sited,

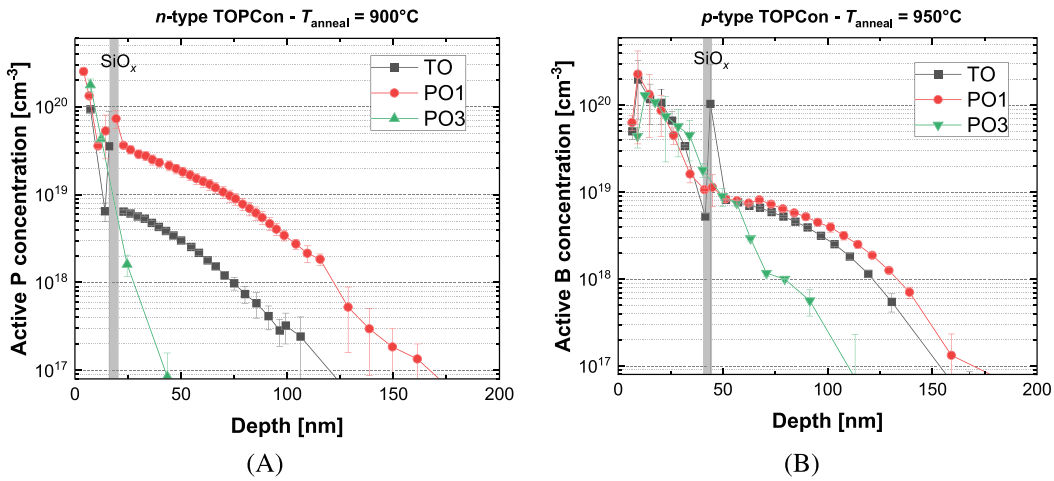

FIGURE 8 Electrically active dopant diffusion profiles for (A) n-type or (B) p-type tunnel oxide passivated contacts (TOPCon) with thermal (TO) or plasma oxides (PO1, PO3) capped with doped poly-Si obtained by ECV

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rather than B^+-O pairs, that effectively suppress the transport of boron through SiO_2 gate oxides.[105] However, this does not influence P diffusion through the nitrous interfacial oxide. Therefore, this presumably explains the reduced B diffusion from poly-Si into the c-Si in our experiment. This trend was less pronounced in PO3 compared with PO1 most likely due to shorter plasma exposure time (higher carrier velocity) resulting in a lower amount of N incorporated into the interfacial oxide.

In summary, the preparation of ultra-thin interfacial oxides by plasma oxidation appeared to be an appealing low-temperature alternative to thermal oxidation as a comparable degree of surface passivation could be achieved for *n*- as well as *p*-type TOPCon. The incorporation of nitrogen into the interfacial oxide during plasma oxidation is presumed to effectively block boron diffusion thus retaining a high level of surface passivation. With regards to fabrication of both-sided TOPCon solar cells featuring a lean process flow, plasma oxidation offers the advantage of a single-sided layer fabrication. This allows to individually adjust the oxide properties according to the requirements of the dopant species for a single high-temperature annealing step while preventing potential degradation of one side (no need for etch-back and two-step annealing).

4 | DEPOSITION OF POLY-SI USING PECVD

4.1 | Reduction of wrap-around during deposition of the poly-Si layer

For poly-Si deposition by LPCVD it is known that a major amount of wrap-around will take place and might have to be removed before finishing the cell. One advantage of PECVD is thought to be the single-sided character of the deposition. However, even for PECVD, it is expected that a certain amount of wrap-around will occur. This amount of wrap-around depends on the layout and design of the PECVD system. At Fraunhofer ISE, this was investigated using a centrotherm cPLASMA tube direct-plasma PECVD system with a parallel plate electrode design.[71] The deposition takes place on a horizontal carrier that features 24 pockets for wafers.[71] To characterize the wrap-around of the tube PECVD system at Fraunhofer ISE, we prepared wafers that were first coated with SiN_x and then flipped upside down before then being coated by 150 nm of TOPCon. Here, the SiN_x has two advantages: (i) on top of c-Si/SiN_x the (local) deposition of poly-Si can be visually inspected and (ii) the thickness of the deposition can be more precisely measured using ellipsometry. For the ellipsometry measurement we used a Sentech 400 laser ellipsometer operating at 632 nm.

Figure 9 shows the result of this wrap-around measurement for two M2-sized samples (pseudo-square shape with 156.75-mm length and 210-mm diameter). Both were deposited in a horizontal sample carrier with lowered pockets (1-mm depth). The sample on the left was placed in a square pocket that featured three pins holding and contacting the wafer. The height of these pins was 0.5 mm. A significant amount of wrap-around was measured in this case. The wrap-around is pronounced at the edges due to a shape mismatch between the pocket and the wafer with up to 60-nm TOPCon thickness. To reduce this amount of wrap-around, new pockets were designed that feature a pseudo-square shape. Furthermore, the pins were removed to allow the sample to be placed directly onto the carrier. These contact pins are important in case of deposition with isolating layers like SiN_x to ensure a reproducible contact of carrier and samples. However, for the deposition of highly doped—and therefore conductive—Si layers the pins are not necessary. The sample on the right was placed in such a pocket. Consequently, the wrap-around was significantly reduced all-around, but especially at the pseudo-square edges.

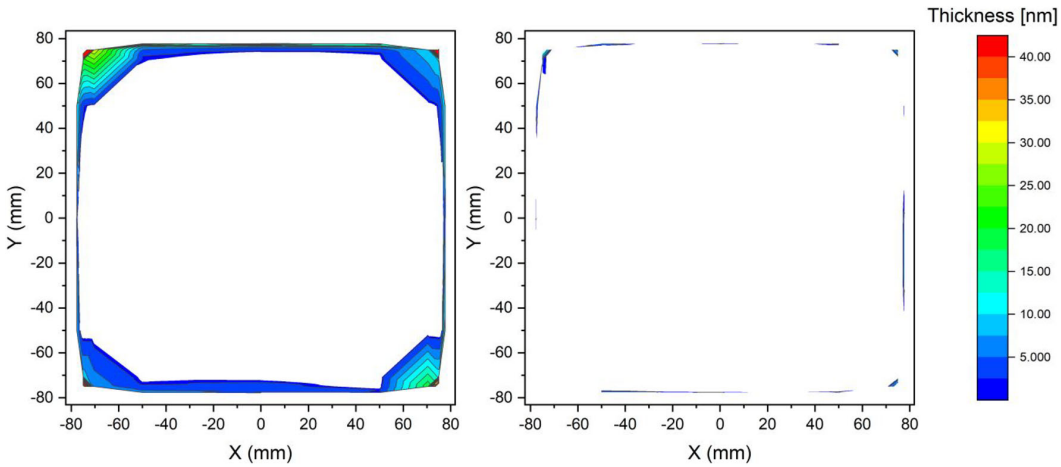

FIGURE 9 Measurement of the wrap-around of the tunnel oxide passivated contacts (TOPCon) deposition on a horizontal carrier in the tube PECVD. Left: square pocket, wafer contact by 3 pins of 0.5-mm height. Right: pseudo-square pocket, no contact pins. Note that the shape does not correspond exactly to the shape of the wafer due to systematic uncertainties in the position of the measurement spot relative to the wafer edge

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These investigations demonstrate the strong influence which the carrier design can have on the effective amount of wrap-around. However, for the industrial usage a vertical layout of the carrier is desirable since the throughput per deposition doubles. Unfortunately, it is harder to ensure a tight fit between the holding plates of the carrier and the samples in a vertical layout. Furthermore, the investigations show that even with the adapted layout, wrap-around was not fully avoided. While the parasitic TOPCon deposition seems minor, it can affect the final performance at the module level and thus a wrap-around removal step might still be required. However, since the wrap-around is strongly reduced, such a removal step can be designed with lower requirements since less parasitic deposition has to be removed. Due to the large asymmetry in the thickness between desired and undesired deposition (approximately a ratio of 15:1), even an unprotected batch etch might be an option when the wrap-around is well controlled. It should be mentioned that these investigations were done using a carrier with a horizontal layout. However, in industrial productions typically vertical layouts are used to double the throughput. While the findings in this work cannot be directly applied to vertical carriers, they can still be used to derive design optimizations even for industrial-type carriers.

4.2 | Removal of poly-Si wrap-around

Figure 10 shows a schematic illustration of a typical i-TOPCon cell processing sequence from emitter diffusion to wrap-around removal. It includes two single-side etches, first the removal of the emitter on the backside after boron diffusion and the poly-Si wrap-around removal. These process steps are necessary to prevent a shunt formation at the solar cell edge.

Various dry and wet processes are known for single-sided etching of solar cells. Recently, Kafle et al. have demonstrated that dry etching using an inline-plasma tool results in high parallel resistance and excellent device performance.[106] In this article we are focusing on one-sided wet-chemical etching since it is successfully used to remove the parasitic emitter on the back side in large-scale production. Regarding a later gentle removal of the poly-Si wrap-around, it is very useful to leave the borosilicate glass (BSG) on the front emitter in this process step. This means that the poly-Si wrap-around is deposited onto the BSG and the p^+-diffused emitter is protected against the wrap-around etchant. A diluted mixture of HNO_3 and HF—as commonly used for single-sided emitter etching—is not well suited because of its very high etch rates for c-Si. Such a solution would quickly etch the BSG and finally the emitter on the front side. In contrast, BSG is an efficient etching stop for alkaline solutions. We investigated the etch rate of phosphorus-doped TOPCon before polysilicon anneal in potassium hydroxide (KOH) solution as a function of temperature and KOH concentration after a dip in HF 1% for 1 min. The HF removes any SiO_2 that may have unintentionally formed on the TOPCon structure. We used the same SiN_x/TOPCon coated samples for which the wrap-around was measured in the last section. Figure 11 shows that the etch rate nicely resembles the Arrhenius equation $R = R_0 \exp(-E_A/kT)$ with the pre-exponential factor R_0, the activation energy E_a, the Boltzmann constant k, and the absolute temperature T. E_A is about 0.61 eV for every considered KOH concentration. Therefore, the etch rate goes up by a factor of approximately 1.76 every 10°C. R_0 and thus the etch rate increase in the range of 5 to 10 wt% KOH and then saturate.

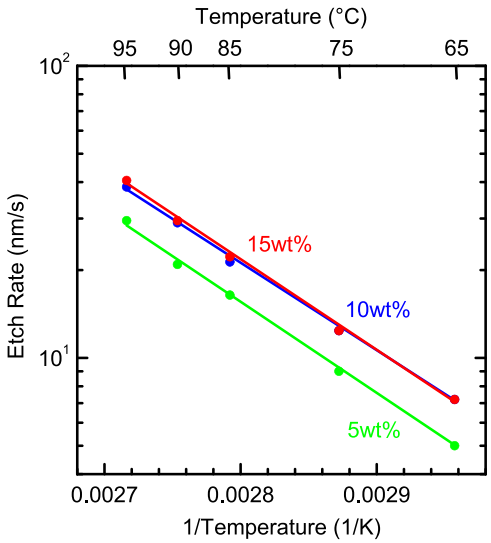

FIGURE 11 Measured etch rate of nonannealed P-doped plasma-enhanced chemical vapor deposition (PECVD) tunnel oxide passivated contacts (TOPCon) in potassium hydroxide solution as a function of temperature and KOH concentration

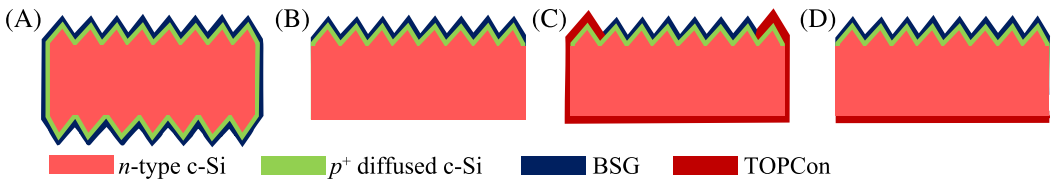

FIGURE 10 Schematic illustration of the cross-sectional structure of tunnel oxide passivated contacts (TOPCon) cells showing a process sequence including two single-side etches: (A) after double-side boron diffusion, (B) single-side emitter etching, (C) tunnel oxide formation and TOPCon deposition, (D) TOPCon wrap-around removal

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The effect of alkaline wrap-around removal on M2-sized large bifacial i-TOPCon cells prepared by the process sequence shown in Figure 10 was investigated. The base doping of the used *n*-type CZ Si wafers was 1.5 Ωcm. The emitter sheet resistance was 113 Ω/sq. The 160-nm-thick TOPCon layer was deposited using the older, square-shaped design of the pockets (meaning that the wrap-around corresponds to Figure 9 (left)). The subsequent process steps were BSG etching and cleaning, TOPCon anneal, AlO_x/SiN_x passivation on the front side, SiN_x deposition on the back side, and screen-printing of Ag grids on both sides and contact firing. For the horizontal wrap-around etching, we used a KOH concentration of 15 wt% at a temperature of 65°C. As a reference, other cells without wrap-around etch were fabricated in the same batch. The electrical performance parameters of the cells measured under standard test conditions using a flasher provided by Halm are listed in Table 4. It is obvious that the wrap-around etch significantly increased the parallel resistance by 30 kΩ cm^2 and therefore reduced the FF_0–*pFF* loss by 1.2% absolute. At the same time, J_{rev} decreased (not shown) which is important for the production of reliable modules. Furthermore, V_{oc} is clearly increased by 5 mV. This is due to inferior surface passivation at the areas where the TOPCon wrap-around covers the boron emitter. While an effect of parasitic absorption by the TOPCon wrap-around could be expected in J_{sc}, this was not observed due to the small area of the wrap-around. Overall, we achieved an absolute efficiency gain of 0.6% by TOPCon wrap-around etching. While the impact of the wrap-around could be reduced by adjusted carrier designs (see above), this shows the importance of this additional process step if any significant amount of wrap-around is deposited within the process sequence.

5 | TOPCON TUNNEL JUNCTIONS FOR TANDEM SOLAR CELLS

In search of higher efficiencies beyond the fundamental limits of single-junction devices and to further reduce the levelized cost of electricity (LCOE), more and more research is dedicated to tandem solar cells. The combination of a perovskite top and a Si bottom cell promises highly efficient devices at affordable cost. Regarding the Si

TABLE 4 Measured electrical performance parameters of i-TOPCon solar cells manufactured with and without wrap-around etch, respectively

	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	FF_0-*pFF* (%)	R_p (kΩ cm^2)	*η* (%)
w/etch	698	40.3	80.5	1.1	31.3	22.7
w/o etch	693	40.3	78.8	2.3	1.3	22.1
w/ - w/o	**5**	**0**	**1.7**	**−1.2**	**30.0**	**0.6**

Note: The last row (in bold emphasis) is the difference between row 1 and row 2.
Abbreviation: TOPcon, tunnel oxide passivated contacts.

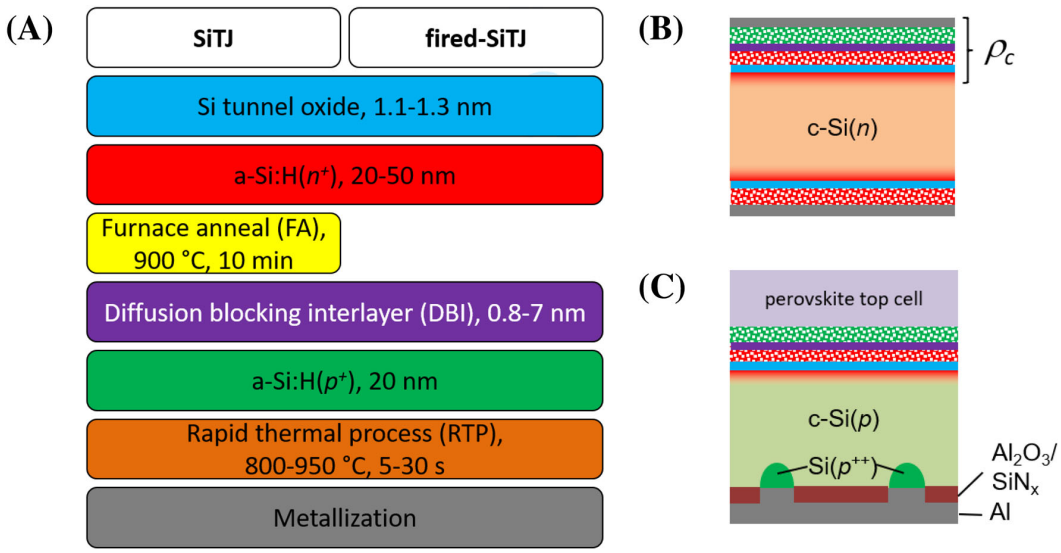

FIGURE 12 (A) Process sequences to fabricate a Si-based tunneling junction (SiTJ) based on tunnel oxide passivated contacts (TOPCon) with furnace anneal ("SiTJ") and without furnace anneal using only a single rapid thermal process ("fired-SiTJ"). The deposition of a diffusion blocking interlayer (DBI) directly before a-Si:H(p+) deposition is only mandatory for high $T_{RTP} \geq 900$°C. (B) Sketch of the sample structure for dark J–V measurements to determine the contact resistivity of the full poly-Si(p$^+$)/poly-Si(n$^+$)/SiO_x/c-Si stack. (C) Proposed bottom cell structure with passivated emitter and rear cell (PERC) rear side, a front side poly-Si passivating contact, and a p$^+$/n$^+$ poly-SiTJ as subcell interconnection in monolithic perovskite/Si tandem solar cells. This figure is adapted from Luderer et al.[114]

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bottom cell, it is highly desirable to adapt the mainstream PERC technology for tandem application.[107] The so-called "TOPerc" approach combines the well-established rear side of the PERC technology with a TOPCon front contact[107,108] as shown in Figure 12C.

A monolithic two-terminal tandem configuration requires a transparent and low-resistive recombination junction between both subcells to allow efficient recombination of the different majority carriers from each cell. While usually transparent conductive oxides (TCOs) are used to serve that purpose (e.g., in previous studies,[109–111]) n^+/p^+ Si-based tunneling junction (SiTJ) could reduce optical losses by better refractive index matching.[112]

5.1 | Fundamental concepts

In a recent publication, we presented a low-resistive and passivating SiTJ based on TOPCon.[113] With respect to the electrical properties, the process flow and layers must allow (i) excellent passivation of the c-Si surface, (ii) low contact resistance at the poly-Si/c-Si contact, (iii) low resistance at the poly-Si(p^+)/poly-Si(n^+) tunneling junction, and (iv) low contact resistance between the tunneling junction and the first layer of the top cell. The structure to determine the contact resistances is shown in Figure 12B.

Two process routes have been evaluated to form the SiTJ as shown in Figure 12A. In the standard SiTJ route, the SiTJ is formed by depositing a-Si:H(p^+) on n-TOPCon, followed by a rapid thermal process step (RTP) to crystallize the Si(p^+) layer to activate boron dopants. With the furnace anneal (FA) after a-Si(n^+) deposition and prior to the a-Si(p^+) deposition, the formation of a low-resistive passivating contact to the c-Si absorber can be assured prior to the formation of the SiTJ. Alternatively, in the fired-SiTJ route, the prolonged FA after a-Si:H(n^+) deposition is omitted and both the contact formation to the Si wafer and the SiTJ are realized solely by the RTP.

Especially for the fired-SiTJ approach, the thermal budget of the RTP must be carefully considered for optimal performance. A dopant diffusion trade-off exists, as illustrated in Figure 13A. It shows the phosphorus (P) depth profile across the different layers, as measured with time-of-flight secondary ion mass spectroscopy (ToF-SIMS), as a function of the applied thermal budget. For the highly doped a-Si(n^+), a rectangle-shaped P depth profile with high P concentration within Si(n^+) and negligibly low P concentration elsewhere was obtained in the as deposited state. Thermal processing leads to P diffusion in both directions, into the c-Si absorber and into the Si(p^+) region. Diffusion into the c-Si substrate (right) is necessary to some extent for contact formation. It is controlled by the interfacial oxide, which acts as a diffusion barrier for P as pointed out in section 3. P is known to pile-up at Si/SiO_x interfaces.[88,90]

As a sharp/abrupt transition between p^+ and n^+ necessary to form a SiTF with a narrow depletion width is desirable (Figure 13B), dopant exchange of the n^+ and p^+ regions should be prevented as much as possible. If significant dopant interdiffusion occurs, as observed for temperatures $T_{RTP} > 850°C$, the charge carrier

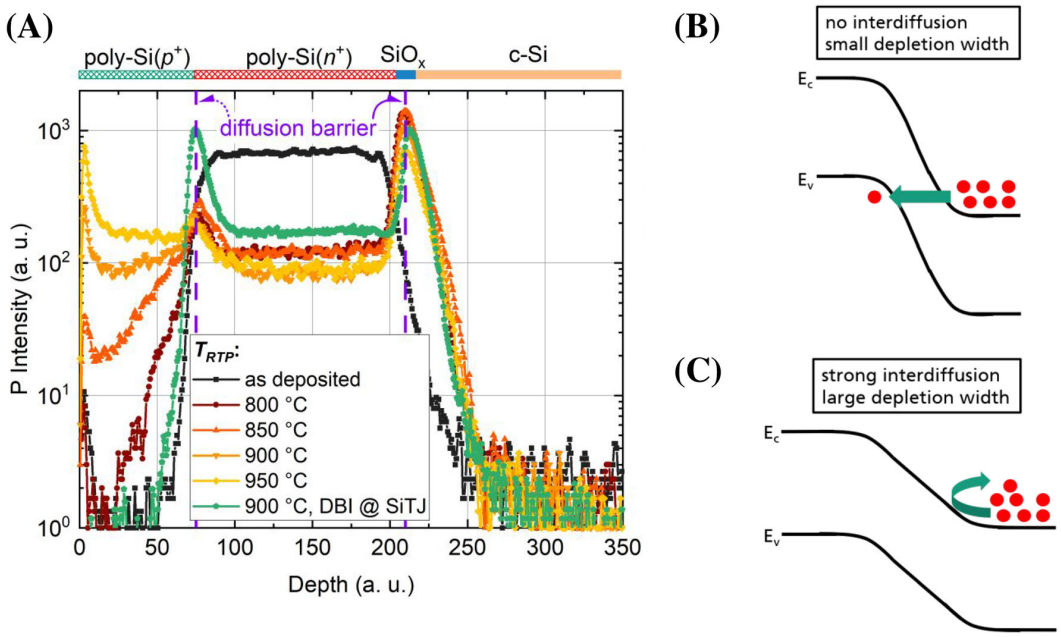

FIGURE 13 (A) Dopant depth profiles, as measured with time-of-flight secondary ion mass spectroscopy (ToF-SIMS), for different postdeposition thermal treatments. The influence of T_{RTP} on the P depth profile is shown. (B, C) Sketch of the Si-based tunneling junction (SiTJ) band diagram. With minor dopant interdiffusion at lower temperatures (B), the bands are crossed, and the depletion region width is sufficiently small to allow tunneling transport. With strong interdiffusion at higher temperatures (C), the bands are no longer crossed, and the large depletion width prevents tunneling transport

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concentration is reduced on both sides of the SiTJ leading to reduced band bending and a wider depletion width. If the bands are no longer crossed, no direct tunneling transport can occur Figure 13C). Therefore, dopant interdiffusion results in very high ρ_c or can even cause complete overcompensation of one dopant species and yield an isotype junction.[113]

Thus, the RTP thermal budget, mandatory for dopant activation in the poly-Si and to form both the TOPCon front contact and the aluminum back-surface-field at the PERC rear side in the TOPerc approach, must be as low as possible to achieve appropriate properties at the SiTJ.

Two solutions for this trade-off problem have been presented in Luderer et al.[114]:

- Altering the Si tunnel oxide to ease contact formation between Si(n^+) and the substrate, that is, choose a less stoichiometric, more permeable wet-chemically (HNO_3) grown Si oxide instead of a thermally grown Si oxide.[90]
- Applying a diffusion blocking interlayer at the SiTJ interface. Especially SiC_x and SiN_x have been shown to successfully block dopant diffusion Figure 13A, green data) and therefore increase the thermal stability of the SiTJ.

For appropriate processing conditions, the additional heavily boron-doped Si(p^+) layer, which is expected to ease the formation of a low-resistive contact to the hole transport layer of the top cell, does not significantly increase the resistance of the poly-Si(n^+)/SiO_x passivating contact (TOPCon). As a result, for the SiTJ route with FA, very low $\rho_c \approx 10$ mΩ cm^2 were obtained at $T_{RTP} = 800°C$,[113] and ρ_c < 100 mΩ cm^2 were achieved over a wide range of T_{RTP}.[114] This is a very promising result, since it leaves some room for optimizing the combination of poly-Si/SiO_x passivating contacts (TOPCon) and the PERC technology to form an efficient but low-cost, industrial-feasible Si bottom cell for tandem application (TOPerc). Similarly, Haug et al. used ex situ (oxidation) and in situ (carbon alloying) treatments at the SiTJ interface to prevent dopant interdiffusion and achieved ρ_c values as low as 7 mΩ cm^2.[115]

Further, by using a wet-chemically (HNO_3) grown Si tunneling oxide, a SiTJ with good surface passivation ($iV_{oc} = 711$ mV) and very low ρ_c down to ≈30 mΩcm^2 was achieved with the highly desirable "fired-SiTJ" process route comprising only a single rapid post-deposition thermal treatment at $T_{RTP} = 850°C$.[114]

In the next section, the poly-SiTJ is integrated into a Si single-junction solar cell to test its performance on cell level.

5.2 | Cell results

The cell design comprised a planar 200-μm-thick 1 Ω cm *n*-type FZ c-Si absorber and poly-Si/SiO_x passivating contacts (TOPCon) on both sides with the full area poly-Si(p^+) emitter at the front side. The SiTJ was formed with an additional poly-Si(p^+) layer on top of the rear side poly-Si(n^+)/SiO_x contact (Figure 14A). Solar cells without this additional poly-Si(p^+) at the rear side served as references (Figure 14B). The two most promising SiTJ processes mentioned in the previous section were tested. Namely, a SiTJ utilizing both the FA and an RTP at $T_{RTP} = 800°C$ and a fired-SiTJ with a wet-chemically (HNO_3) grown passivating Si tunnel oxide and $T_{RTP} = 850°C$.

The poly-Si(p^+)/SiO_x emitter was the same for all cells and comprised a SiO_x thermally grown at 600°C for 10 min in pure oxygen atmosphere (thickness ≈1.3 nm, TO2) and a FA at 950°C for 10 min. The emitter was completed before the rear side contact and the SiTJ, which were formed with lower thermal budget. For group "SiTJ", the thermally grown rear side SiO_x (600°C for 10 min under N_2/O_2 atmosphere, TO1) and the Si(n^+) received the FA at 900°C for 10 min before Si(p^+) deposition, followed by an RTP at $T_{RTP} = 800°C$. For group "fired-SiTJ", Si(n^+), and Si(p^+) were deposited on a wet-chemically (HNO_3) grown Si oxide at the rear, followed by an RTP at $T_{RTP} = 850°C$. For hydrogenation, all samples were exposed to a remote plasma hydrogen passivation (RPHP) step at 400°C for 30 min. Then, for lateral transport between the metal finger grid and for better light coupling, 75 nm of ITO was sputtered on the front side using a shadow mask with 2.1 × 2.1-cm^2 openings. To reduce sputter damage, a low power/high power stack was used in combination with a subsequent hotplate annealing at 350°C for 3 min.[116] The metallization was realized with full-area thermal evaporation of a Ti/Pd/Ag stack at the rear side and Ti/Pd/Ag evaporation and the photolithography lift-off technique for the front side grid with a pitch of 800 mm. The illuminated *J*–*V* characteristics were measured with the active cell area set to 2.0 × 2.0 cm^2 using a shadow mask.

Figure 15 depicts the solar cell parameters of the different groups. Overall, very similar results were obtained for both SiTJs groups compared with the reference without SiTJ. Thus, the additional poly-Si(p^+) layer at the rear side did neither increase the cell's

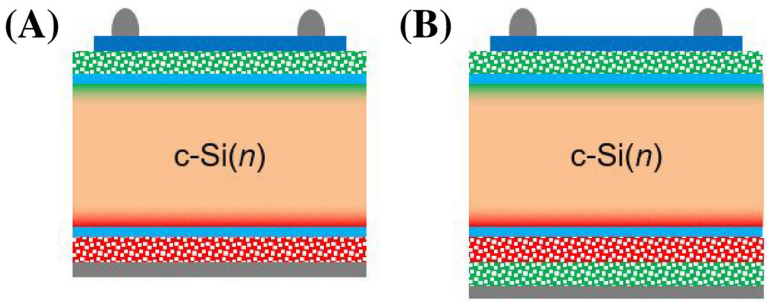

FIGURE 14 Sketch of Si single-junction solar cell structures used (A) with and (B) without Si-based tunneling junction (SiTJ). For the fired-SiTJ solar cells, a wet-chemically grown Si tunnel oxide was used at the rear side to ease contact formation during thermal process step (RTP)

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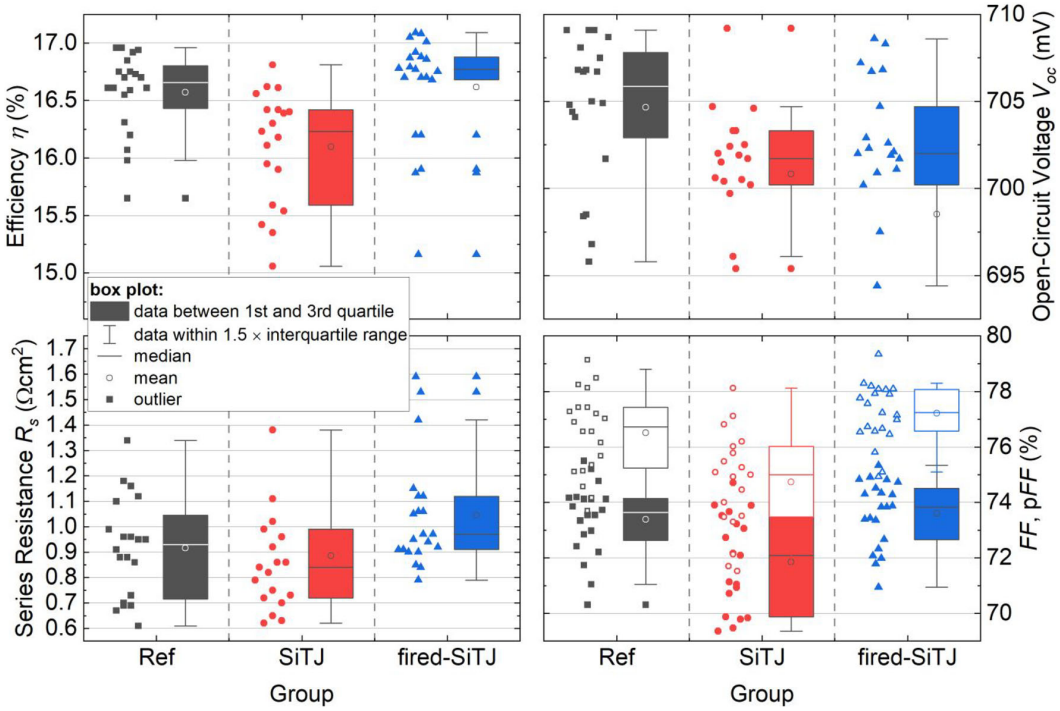

FIGURE 15 Solar cell parameters of poly-Si single-junction solar cells without Si-based tunneling junction (SiTJ) ("Ref"), with a SiTJ formed by both furnace anneal (FA) and thermal process step (RTP) ("SiTJ"), and with a "fired-SiTJ" formed by a single RTP

series resistance nor harm the surface passivation significantly, proving the suitability of the developed SiTJ for solar cell application. This is especially remarkable for group "fired-SiTJ", where the electron selective poly-Si(n^+)/SiO_x passivating rear contact and the SiTJ were formed with a single rapid thermal treatment.

The cell efficiency η in this test batch is limited by three aspects, which are not related to the SiTJ: the planar surface of the c-Si absorber, limiting the short-circuit current density J_{sc} to ≈32.0 mA cm^{-2} (not shown), the TCO/poly-Si(p^+) contact resistance [116], and the low pseudo fill factor p*FF* < 80%. The latter is mainly caused by the so-called dark emitter effect, since the poly-Si(p^+) area—and thus the emitter—was larger than the illuminated area. Due to nonnegligible lateral conductivity in the 35-nm-thick poly-Si(p^+) layer, the cells are connected to nonilluminated emitter areas (pn-junctions) acting as a sink for charge carriers, that is, a highly recombination-active region. This effect was quantified measuring the p*FF* of the solar cells using the SunsVoc method.[117] Measuring with and without a 2.0 × 2.0-cm^2 mask resulted in a difference in p*FF* of ≈ $4\%_{abs}$. For comparison, the SunsVoc method was also performed on silicon heterojunction (SHJ) front emitter cells with and without mask. There, only a minor difference of ≈ $0.2\%_{abs}$ was measured, which was most likely due to the small offset between ITO (2.1 × 2.1 cm^2) and mask area (2.0 × 2.0 cm^2). The significant difference of the dark emitter effect for both cell technologies can be ascribed to the difference in lateral conductivity of a-Si:H and poly-Si. The sheet resistance of a-Si:H is too high to support lateral transport and to contribute to the dark emitter effect. This emphasizes that for application in perovskite/Si tandem solar cells, care must be taken to control the lateral conductivity of heavily doped poly-Si layers to avoid efficient connection of shunt paths. Options for higher sheet resistance are, for example, thinner layers or carbon alloying of the poly-Si. On the other hand, for large-area tandem cells, this effect will be strongly reduced due to the more favorable area to edge ratio.

In conclusion, a SiTJ based on TOPCon with good surface passivation and low transport losses could be transferred from test structures to a Si single-junction solar cell. Therefore, the passivating p^+/n^+ poly-SiTJ is ready to be tested in an industrial-feasible tandem solar cell featuring a perovskite top cell and a TOPerc Si bottom cell.

6 | CONCLUSION

Passivating contacts based on poly-Si/SiO_x structures were already investigated in the early days of silicon photovoltaics. In the last decade there has been a lively renaissance of this technology, also known as TOPCon. In this article, we could present only some aspects of the broad research on TOPCon technology. Indeed, there are many more activities to gain a better scientific understanding of such poly-Si/SiO_x structures and to find process routes suitable for mass production of TOPCon cells. We are confident that TOPCon, similar to

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PERC technology, will play an important role in the next generation of silicon solar cells and may even be a key technology for exciting future options such as tandem solar cells.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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