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(54) DISPLAY PANEL, LIQUID CRYSTAL DISPLAY DEVICE AND DRIVE-CIRCUIT-MOUNTED BOARD

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(57) **ABSTRACT**

A display panel is connected to a wiring-mounted board on which a signal supply wiring that supplies wiring supplies signals for driving the display panel is mounted. The wiring-mounted board has (i) first and second wires extending toward the display panel, and (ii) first and second terminals that are connected to the first and second wires, respectively. The display panel has a first short-circuit wire that is connected to the first and second wires at a connecting part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires.

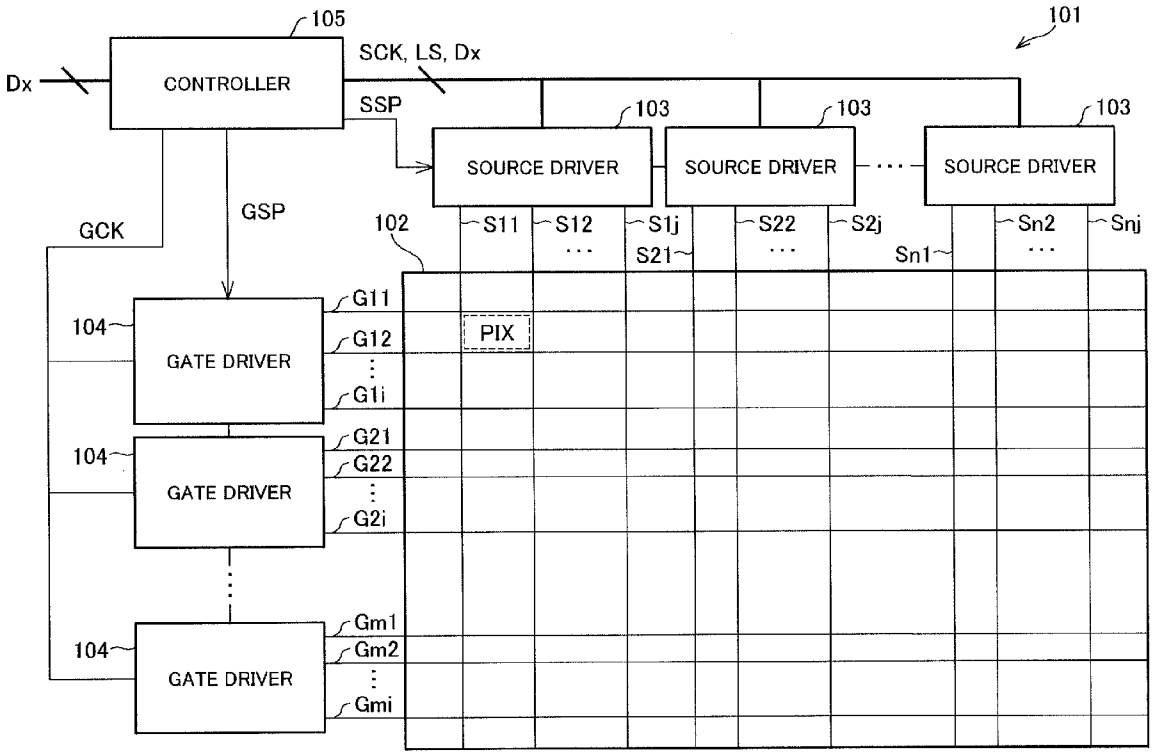


FIG. 1

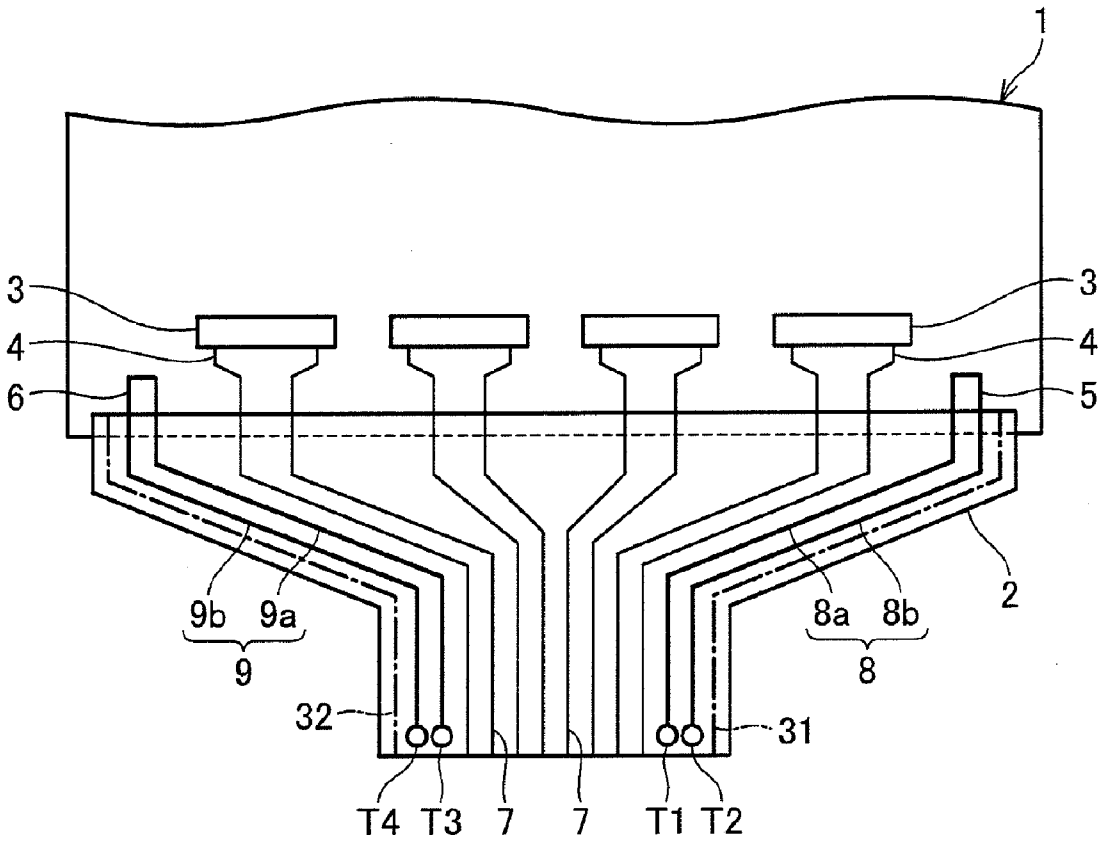


FIG. 2 (a)

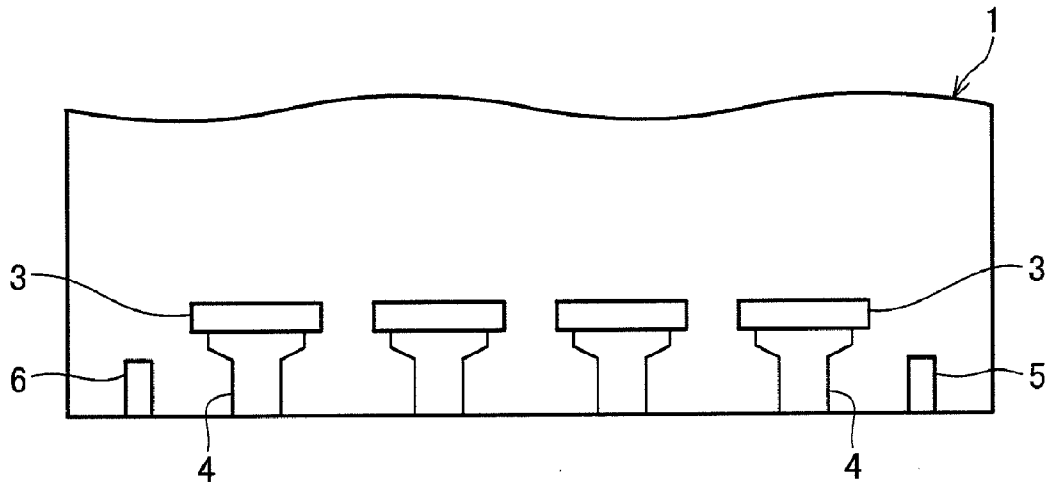
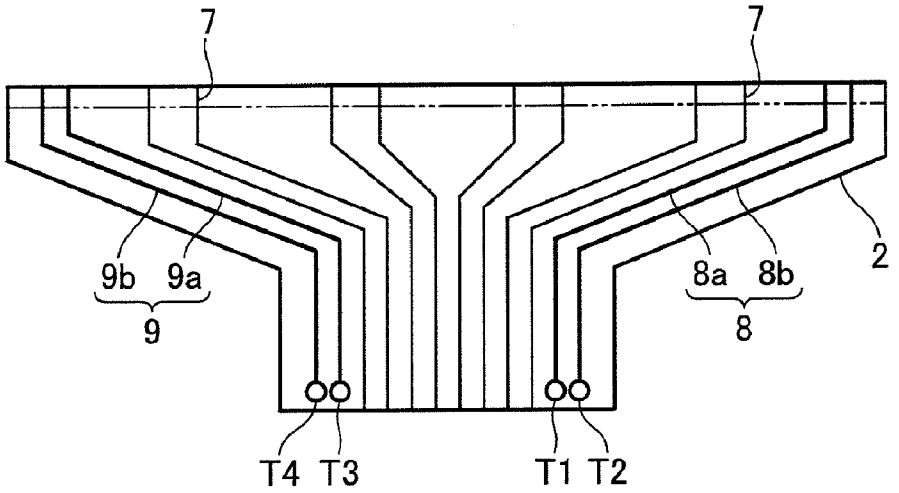
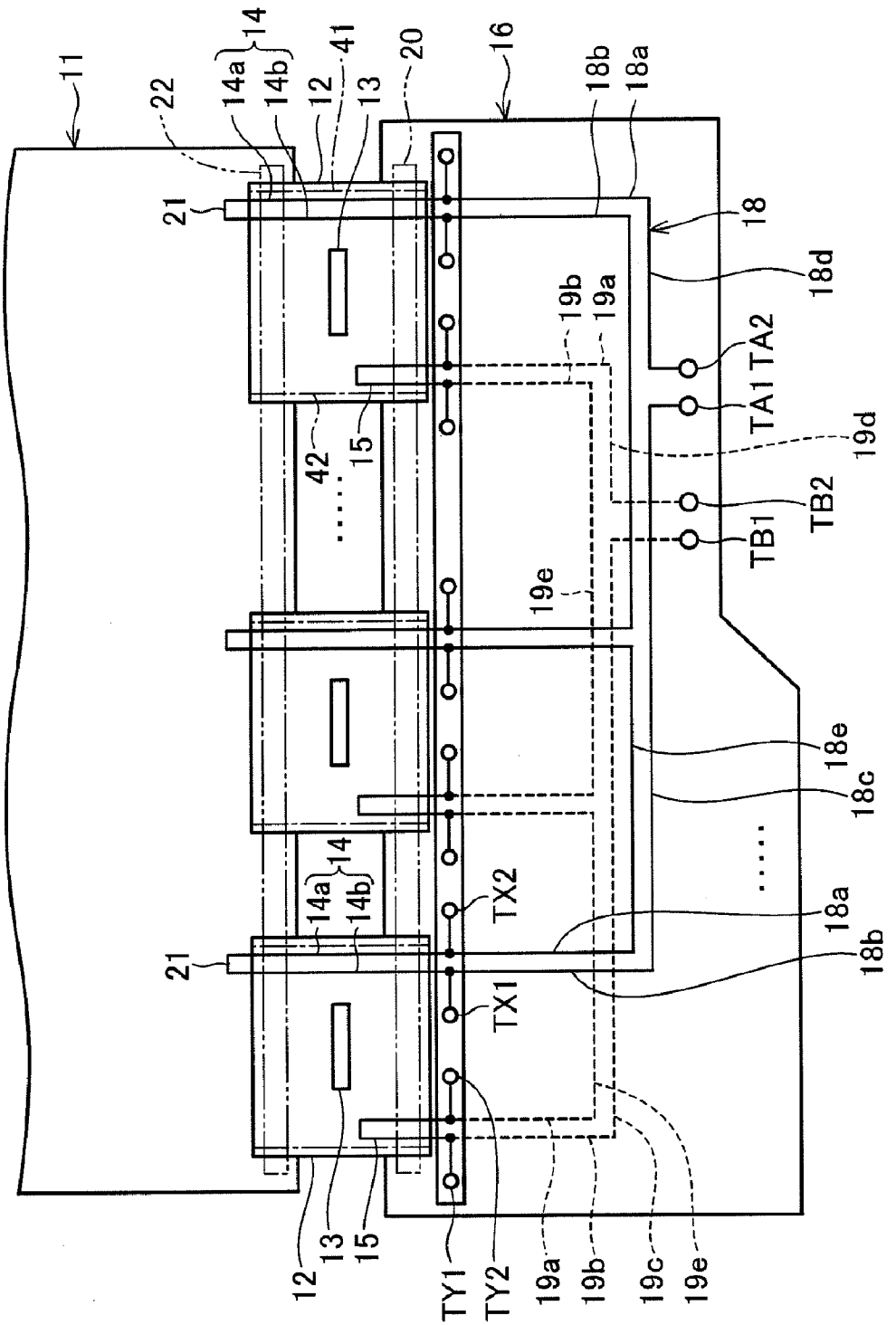


FIG. 2 (b)

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14b
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18d
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19d
42
15
TB2
TB1
19e
18e
18c
14a
14b
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TX2
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18b
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TX1
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TY1
TY2
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FIG. 3

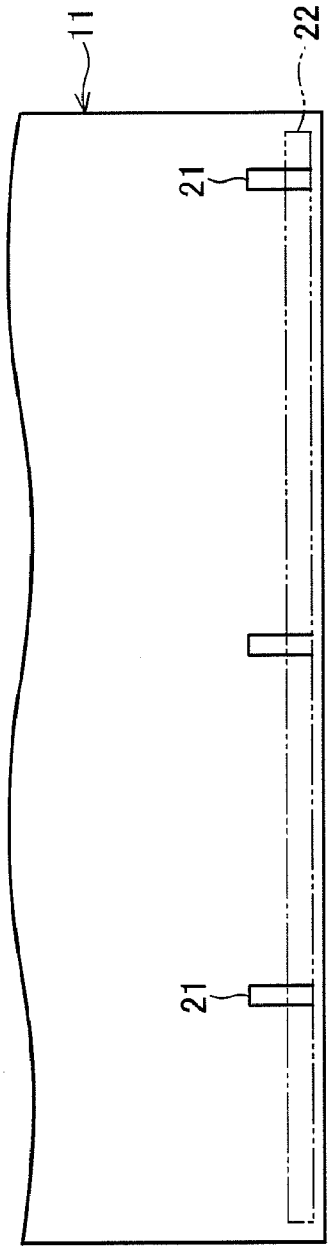
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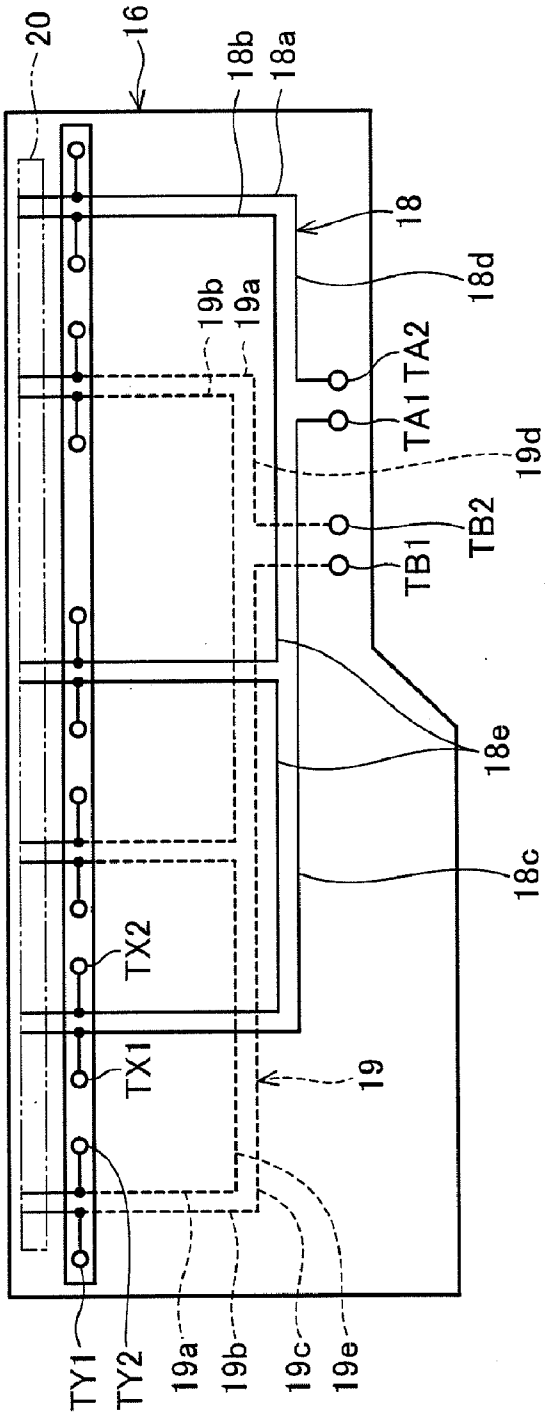
FIG. 4 (a)


20
16
18b
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18
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19a
TA1 TA2
19d
TB1
TB2
18e
18c
TX2
TX1
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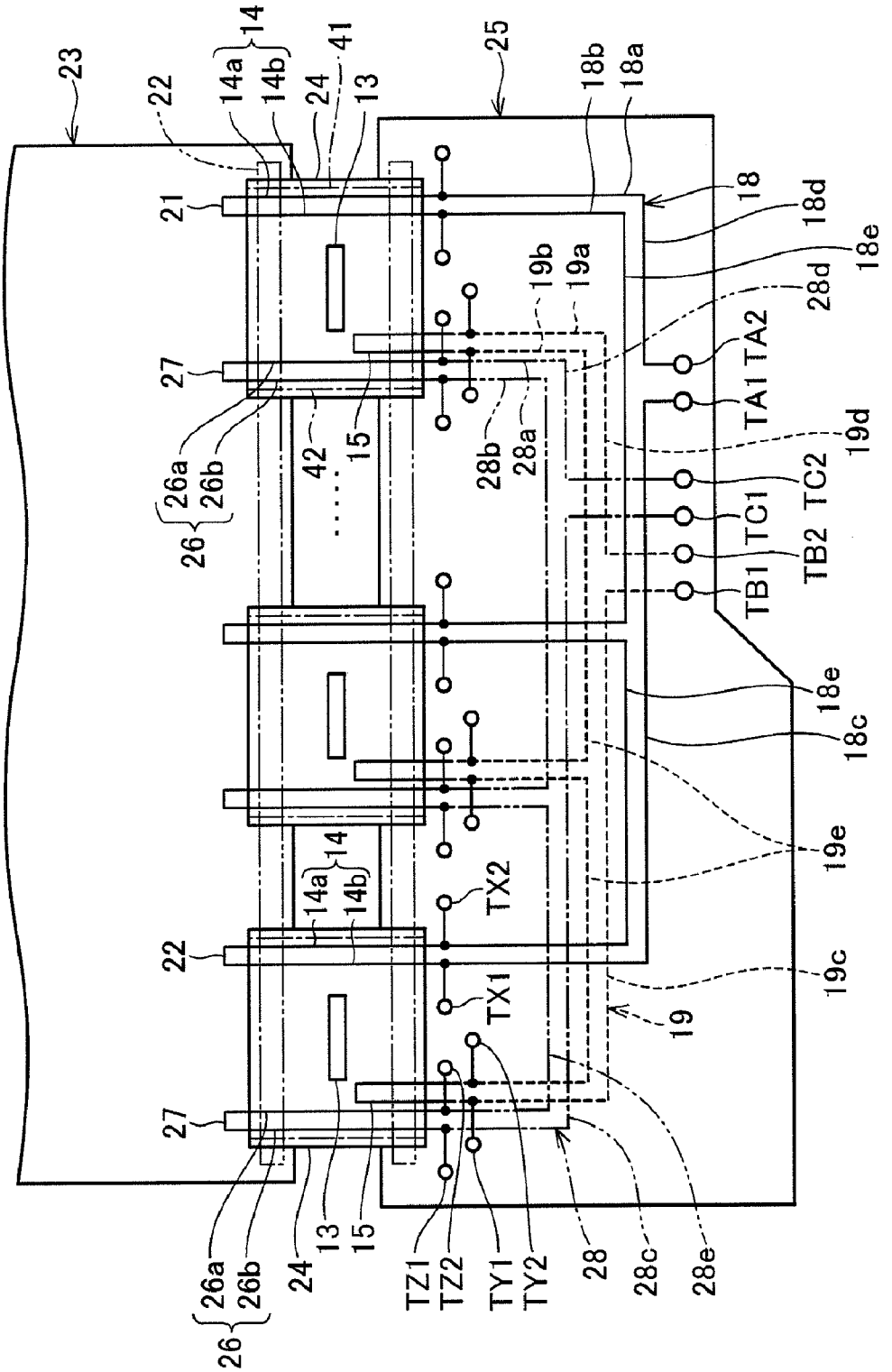
TY1
TY2
19a
19b
19c
19e

FIG. 4 (b)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TA2
TA1
26a
26b
26
42
15
28b
28a
19d
TC2
TC1
TB2
TB1
18e
18c
19e
14
14a
14b
TX2
22
TX1
19c
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26b
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TZ1
TZ2
TY1
TY2
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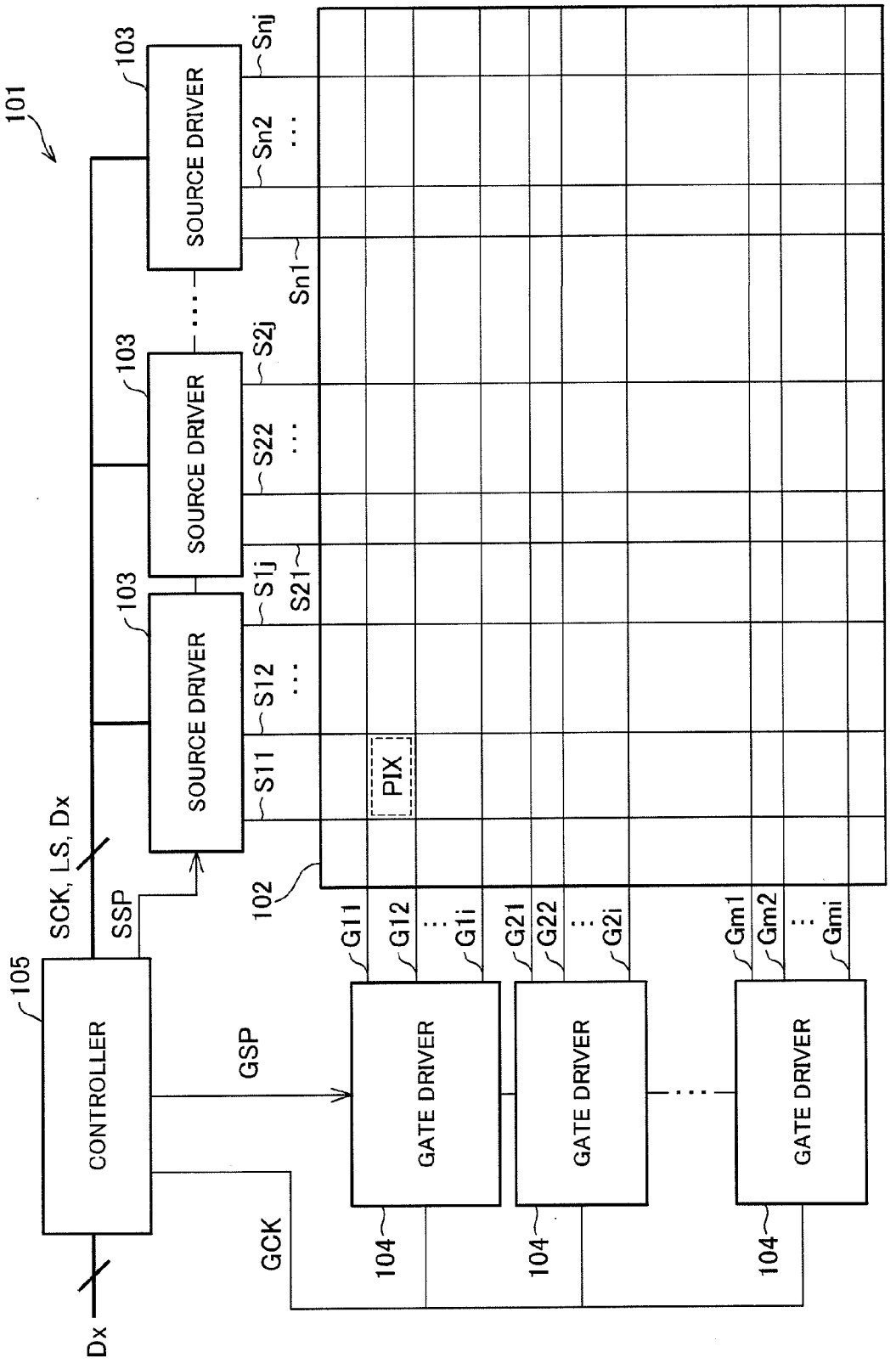
28c
28e

FIG. 5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SOURCE DRIVER
Snj
Sn2
Sn1
S2j
S22
S21
S1j
S12
S11
PIX
102
SCK, LS, Dx
SSP
105
CONTROLLER
GSP
GCK
Dx
G11
G12
G1i
G21
G22
G2i
Gm1
Gm2
Gmi
GATE DRIVER
104

FIG. 6

DISPLAY PANEL, LIQUID CRYSTAL DISPLAY DEVICE AND DRIVE-CIRCUIT-MOUNTED BOARD

[0001] This Nonprovisional application hereby incorporate by reference the entire contents of Patent Application No. 2007-077769 filed in Japan on Mar. 23, 2007.

TECHNICAL FIELD

[0002] The present invention relates to a display panel connected to a wiring-mounted board on which wiring that supplies a signal for driving the display panel is mounted, a liquid crystal display device including such a display panel, and a drive-circuit-mounted board on which a semiconductor integrated circuit for driving the display panel is mounted.

BACKGROUND ART

[0003] A flat type display apparatus such as a liquid crystal display device has become widespread due to its easiness in achievement of reduction in thickness. Such a display apparatus includes a display panel containing a large number of pixels. The display panel receives, from a drive circuit, signals for driving the pixels. This drive circuit is integrated, and is provided as a packaged arrangement such as a COF (Chip On Film). Such drive circuit is provided externally to the display panel. Alternatively, the drive circuit is directly mounted on a glass substrate of the display panel, as a COG (Chip On Glass) form. The signals for driving the pixels are provided to the drive circuit thus mounted on the glass substrate via wiring mounted on an FPC (Flexible Printed Circuit) connected to the display panel.

[0004] In order to ensure reliability of signal communication to the display panel, it is required for the COF and the FPC to be securely connected to the display panel. As a technique for improving reliability of such a connection, a technique for structurally reinforcing the FPC is disclosed in Japanese Unexamined Patent Publication No. 183247/1993 (Tokukaihei 5-183247; published on Jul. 23, 1993), for example. In this technique, the FPC is reinforced at both outer side end sections which receive stress, by providing a reinforcement member that has no electrical connection.

[0005] Verification of the reliability of the connection is also carried out by a test conducted after the COF or the FPC is connected to the display panel. A mainstream of such a test is an impression test carried out at a connecting part. The impression test examines, through an image, a state of a thermally compressed impression part, by an automated machine incorporating a microscope. More specifically, a state of the impression part such as a depth and a width are analyzed by use of a photographed image.

[0006] The flat type display apparatus are becoming used as a display section for various machines, due to its advantage that the display apparatus can be arranged so as to be thin in thickness. For example, use of the flat type display apparatus in machines such as an onboard display apparatus and a display apparatus of a controlling apparatus have been promoted. In such fields of use, the machines which include the flat type display apparatus are often placed under a harsh environment. In a case of a passenger car, the display apparatus is subject to vibration, high and low temperatures, and the like. The controlling apparatus that is used in factories and the like are also often placed in a similar environment as with the passenger car.

[0007] Use of the flat type display apparatus under such a harsh environment causes film base material used in the COF and FPC to receive stress. Therefore, as compared to a case where the flat type display apparatus is used under a normal usage environment, there is a high possibility that the film base material (particularly at a connecting part with the display panel) is to break.

[0008] As described above, structural reinforcement of the FPC can reduce the occurrence of breakage of the FPC that is caused by stress. However, it can also be fully considered that, under the harsh usage environment, the reinforcement may still not prevent damage to the FPC given due to stress that has been received for a long term. As a result, in a case where the FPC actually breaks, there is a possibility that the display panel cannot be able to carry out a display due to a disconnection thus occurred to the FPC. Such a situation hinders operation of the passenger car and the controlling apparatus.

[0009] Moreover, although the impression test can verify the reliability of the connection during a manufacturing step of the display apparatus, verification cannot be made once the display apparatus is marketed as a product. Therefore, even if the COF and the FPC are close to breakage as a result of continuous use of the display apparatus under the foregoing harsh environment, this state cannot be verified. Consequently, further continuous use of the display apparatus in such state results in breakage of the COF and the FPC. As a result, display can no longer be carried out by the display panel.

SUMMARY OF INVENTION

[0010] An object of the present invention is to provide an arrangement capable of checking a connection state between a display panel and a flexible mounting board (e.g. COF and FPC), not only during manufacture but also during use thereof.

[0011] In order to attain the object, a display panel of the present invention is a display panel connected to a wiring-mounted board on which signal supply wiring that supplies signals for driving the display panel is mounted, the wiring-mounted board having (i) first and second wires which extend toward the display panel, and (ii) first and second terminals which are connected to the first and second wires, respectively, and the display panel having a first short-circuit wire which is connected to the first and second wires, at a connecting part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires.

[0012] In the arrangement, first and second wires are connected so as to form one wire, via a first short-circuit wire. In such a state, assumption of (i) a breakage state of the wiring-mounted substrate and (ii) a connection state between the display panel and the wiring-mounting substrate are possible, by inputting a signal from a first terminal and checking a state of the signal that appears at a second terminal. The assumption can similarly be made by carrying out the following comparison: (i) a normal resistance of the first and second wires connected so as to form one wire is measured between the first and second terminals in advance; and (ii) a resistance of the wiring that is similarly measured at a state in which the wiring has changed over time is compared to the normal resistance.

[0013] For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0014] FIG. **1**

[0015] FIG. **1** is plan view illustrating a display panel according to First Embodiment of the present invention and an FPC which is connected to the display panel.

[0016] FIG. **2**(*a*)

[0017] FIG. **2**(*a*) is a plan view illustrating an arrangement of the display panel.

[0018] FIG. **2**(*b*)

[0019] FIG. **2**(*b*) is a plan view illustrating an arrangement of the FPC.

[0020] FIG. **3**

[0021] FIG. **3** is a plan view illustrating a display panel according to Second Embodiment of the present invention and a PWB which is connected to the display panel.

[0022] FIG. **4**(*a*)

[0023] FIG. **4**(*a*) is a plan view illustrating an arrangement of the display panel illustrated in FIG. **3**.

[0024] FIG. **4** (*b*)

[0025] FIG. **4**(*b*) is a plan view illustrating an arrangement of the PWB illustrated in FIG. **3**.

[0026] FIG. **5**

[0027] FIG. **5** is a plan view illustrating an arrangement of a modification of Second Embodiment.

[0028] FIG. **6**

[0029] FIG. **6** is a block diagram illustrating an arrangement of a liquid crystal display device according to Third Embodiment.

DESCRIPTION OF EMBODIMENTS

[0030] One embodiment of the present invention is described below with reference to FIGS. **1** through **6**.

First Embodiment

[0031] FIG. **1** illustrates a state (display panel module) of a display panel **1** according to the present embodiment. The display panel **1** is connected to an FPC **2**. FIGS. **2**(*a*) and **2**(*b*) illustrate the display panel **1** and the FPC **2** in unconnected states, respectively.

[0032] As illustrated in FIG. **1**, a plurality of driver chips **3** are mounted along one side of the display panel **1** by a COG technique. The driver chips **3** are integrated drive circuits, which provide drive signals to a plurality of pixels included in the display panel **1** for driving the pixels. Selection signals for selecting display data and a scanning line, and other signals are provided as the drive signals.

[0033] Various signals in accordance with driving methods of the driver chips **3** are inputted to the driver chips **3**, such as a clock for controlling timing for outputting display data or controlling timing of the selection signal, and the like. In order to receive such signals, wiring patterns **4** are provided on the display panel **1** on a side on which the driver chips **3** are mounted. The wiring patterns **4** include a plurality of wires (not illustrated) for supplying a plurality of signals to the driver chips **3** from the FPC **2**.

[0034] Moreover, on the surface of the display panel **1** on which the driver chips **3** are mounted, short-circuit wires **5** and **6** are respectively provided on both end sections of a part on which the driver chips **3** are provided. The short-circuit wires **5** and **6** are later described in detail.

[0035] The FPC **2** is made of film base material such as polyimide or the like, and wiring patterns **7** are formed on this film base material. The wiring patterns **7** are provided so as to correspond to the driver chips **3**, so that the signals are provided to the driver chips **3**. As with the wiring patterns **4**, the wiring patterns **7** include a plurality of wires (not illustrated).

[0036] The FPC **2** is connected to the display panel **1** via an ACF (Anisotropic Conductive Film), in a state in which a connecting end section of the FPC **2** is placed on a connecting end section of the display panel **1**. This causes the wiring patterns **4** and **7** to be electrically connected to each other.

[0037] As illustrated in FIG. **2**(*b*), the FPC **2** has test wiring sections **8** and **9**. The test wiring sections **8** and **9** are provided in the vicinity of both side edges of the FPC **2**, respectively, so as to sandwich all of the wiring patterns **7**. The test wiring section **8** is made of two wires **8***a* and **8***b* provided parallel to each other. The test wiring section **9** is made of two wires **9***a* and **9***b* provided parallel to each other. One end of each of the wires **8***a*, **8***b*, **9***a*, and **9***b* extend toward the connecting end section of the FPC **2**. The other end of each of the wires **8***a*, **8***b*, **9***a* and **9***b* are connected to terminals T**1** to T**4**, respectively, which terminals T**1** to T**4** are provided at an input side end section of the FPC **2**.

[0038] As illustrated in FIG. **2**(*a*), the short-circuit wires **5** and **6** are provided in a U-shape so as to form a rectangular shape. Both ends of the short-circuit wires **5** and **6** extend up to the connecting end section of the display panel **1**. Accordingly, as illustrated in FIG. **1**, one end of the short-circuit wire **5** is connected to the wire **8***a*, and the other end of the short-circuit wire **5** is connected to the wire **8***b*. Moreover, one end of the short-circuit wire **6** is connected to the wire **9***a*, and the other end of the short-circuit wire **6** is connected to the wire **9***b*. At this state, the wires **8***a* and **8***b* are connected so as to form one wire via the short-circuit wire **5**, and the wires **9***a* and **9***b* are connected so as to form one wire via the short-circuit wire **6**.

[0039] In this state, a test signal having an arbitrary waveform is inputted from the terminals T**1** and T**3**, so as to monitor a signal that appears at the terminals T**2** and T**4**. This allows assumption of (i) a breakage state of the FPC **2** and (ii) a connection state between the display panel **1** and the FPC **2**.

[0040] For example, if the signal that appears at the terminals T**2** and T**4** has a substantially same waveform as the signal thus inputted, the test wiring sections **8** and **9** properly transmit the signal. Hence, the connection of the display panel **1** and the FPC **2** is normal, and is thus considered that breakage has not occurred to the FPC **2**, at least in a part on which the test wiring sections **8** and **9** are provided.

[0041] If a signal does not appear at one or both of the terminals T**2** and T**4**, there is a high possibility that the test wiring section **8** and/or **9** at which the signal does not appear is disconnected, or that connection states between the test wiring sections **8** and **9** and the short-circuit wires **5** and **6** have degraded. Consequently, in this case, there may be a case of a breakage occurring at an edge section (side end section) of the FPC **2**, or occurrence of a poor connection between the display panel **1** and the FPC **2**.

[0042] Further, if the waveform of the signal that appears at one or both of the terminals T**2** and T**4** is blunter as compared to the signal thus inputted, there is a possibility that a resistance of the test wiring sections **8** and **9** has increased due to a breakage of the test wiring sections **8** and **9**, or the like.

[0043] Moreover, the following comparisons may be carried out: (i) comparing between a resistance of a wiring path including the test wiring section **8** and the short-circuit wire **5** and a normal resistance of such wiring path measured in advance; and (ii) comparing between a resistance of a wiring path including the test wiring section **9** and the short-circuit wire **6** and a normal resistance of that wiring path measured in advance. Carrying out these comparisons also allow the assumption of (i) the breakage state of the FPC **2** and (ii) the connection state between the display panel **1** and the FPC **2**. A remarkably larger resistance of the wiring path as compared to a normal value gives an assumption that a state of the wiring path is close to disconnection. The terminals T**1** to T**4** are usable for measurement of the resistance.

[0044] As such, in the present embodiment, the display panel **1** has the short-circuit wires **5** and **6**, and the FPC **2** has the test wiring sections **8** and **9**; the short-circuit wire **5** is connected to the test wiring section **8**, and the short-circuit wire **6** is connected to the test wiring section **9**. Moreover, the ends of the test wiring section **8** are connected to the terminals T**1** and T**2**, respectively, and the ends of the test wiring section **9** are connected to the terminals T**3** and T**4**, respectively. This thus allows easy assumption of (i) the breakage state of the FPC **2**, particularly on both end parts which readily receive stress, and (ii) the connection state between the display panel **1** and the FPC **2**, by checking a state of an output signal from the terminals T**2** and T**4** with respect to input signals from the terminals T**1** and T**3**, during use of a display apparatus which includes the display panel **1**. Moreover, a similar assumption can be made by carrying out the following comparisons: (i) comparing between a resistance between the terminals T**1** and T**2** and its normal resistance; and (ii) comparing between a resistance between the terminals T**3** and T**4** and its normal resistance.

[0045] The present embodiment explains an arrangement which provides the test wiring sections **8** and **9** in a vicinity of both side edges of the FPC **2**, respectively. However, if there is a limitation to a layout of a pin in the FPC **2**, just one of the test wiring sections **8** and **9** may be provided.

[0046] The present embodiment may further have dummy wires **31** and **32** on the FPC **2**, as illustrated by alternate long and short dash lines in FIG. **1**. The dummy wire **31** is provided between the test wiring section **8** and one side edge of the FPC **2**. The dummy wire **32** is provided between the test wiring section **9** and the other side edge of the FPC **2**.

[0047] The dummy wires **31** and **32** are usually provided as independent wires that are not electrically connected to any wires of the display panel **1** or any external wires. Such dummy wires **31** and **32** have a function of reinforcing the FPC **2**. Hence, it is possible to further improve strength of both side edges of the FPC **2**.

[0048] Moreover, the dummy wires **31** and **32** may be electrically connected to a wire of the display panel **1** or an external wire, if necessary.

Second Embodiment

[0049] FIG. **3** illustrates a state (display panel module) of a PWB (Printed Wiring Board) **16** connected to a display panel **11** according to the present embodiment, via COFs **12**. FIGS. **4**(*a*) and **4**(*b*) illustrate the display panel **11** and the PWB **16** in an unconnected state, respectively.

[0050] As illustrated in FIG. **3**, a plurality of COFs **12** provided side by side are connected to the display panel **11** along one side of the display panel **11**. Short-circuit wires **21** are provided at sections on which the COFs **12** are connected on the display panel **11**. The short-circuit wires **21** are later explained in details.

[0051] Each of the COFs **12** has film base material made of polyimide or the like, on which a driver chip **13** and input and output wires (not illustrated) are mounted. The input wire is provided for transmitting an input signal from the PWB **16** to the driver chip **13**. The output wire is provided for transmitting an input signal from the driver chip **13** to the display panel **11**. The driver chip **13** is arranged as similar to the foregoing driver chips **3**, and provides drive signals to a plurality of pixels included in the display panel **11**, for driving the pixels.

[0052] The COFs **12** take a form of an SOF (System On Chip), a TCP (Tape Carrier Package), or the like. The SOF is arranged such that a chip is mounted on film base material made of polyimide or the like. Recently, the SOF is becoming widely spread as an integrated circuit component for driving, such as a liquid crystal driver. Such arrangement of the SOF allows providing wiring to a part on which the chip is to be mounted, different to the TCP on which a chip is mounted on an opening section of the film base material. Moreover, different to the TCP, the SOF does not have a slit that specifies a bending position. Thus, it is possible to bend the SOF at a desired position.

[0053] Each of the COFs **12** include a test wiring section **14** and a short-circuit wire **15**. The test wiring section **14** includes two wires **14***a* and **14***b* provided parallel to each other. The wires **14***a* and **14***b* are provided on one side of the film base material of the COF **12** with respect to the driver chip **13**, so as to connect the display panel **11** and the PWB **16**. The short-circuit wire **15** is provided in a U-shape on the other side of the driver chip **13** that is provided on the film base material of each of the COF **12**, so as to form a rectangular shape. Both ends of the short-circuit wire **15** extend toward the PWB **16**, to connecting end sections of the COFs **12**.

[0054] The display panel **11** is connected to the COFs **12** at a connecting section **22** via the ACF, in a state such that a connecting end section of the display panel **11** overlaps with connecting end sections of the COFs **12**. Thus, the output wires of the COFs **12** and input wires (not illustrated) of the display panel **11** are electrically connected to each other.

[0055] As illustrated in FIG. **4**(*a*), the short-circuit wires **21** are U-shaped so as to form a rectangular shape. Both ends of the short-circuit wires **21** extend toward the connecting end section of the display panel **11**. One end of the short-circuit wires **21** are connected to respective wires **14***a*, and the other end of the short-circuit wires **21** are connected to respective wires **14***b*, as illustrated in FIG. **3**. At this state, the wires **14***a* and **14***b* connect so as to form one wire via respective short-circuit wires **21**.

[0056] The PWB **16** generates a timing signal required for driving the display panel **11**, by use of a controller (not illustrated) installed in the PWB **16**. Moreover, the PWB **16** has a wiring pattern (not illustrated) provided so as to correspond to each of the COF **12**. The wiring pattern includes a plurality of wires (not illustrated) for transmitting timing signals to be supplied to the driver chips **13** of the COFs **12**. The timing signals are prepared in accordance with driving methods, such as a clock for controlling a timing for outputting display data or for controlling a timing of a selection signal, and such timing signal is supplied from the controller (not illustrated)

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mounted on the PWB **16**. The controller generates the timing signals based on externally supplied clock and various pulse signals.

[0057] Note that the controller may be provided externally to the PWB **16**.

[0058] Moreover, as illustrated in FIG. **4**(*b*), the PWB **16** includes: test wiring sections **18** and **19**; terminals TA**1**, TA**2**, TB**1** and TB**2**; and intermediate terminals TX**1**, TX**2**, TY**1**, and TY**2**. The test wiring section **18** includes a plurality of wires **18***a* and **18***b*, an input wire **18***c*, an output wire **18***d*, and common wires **18***e*. The test wiring section **19** includes a plurality of wires **19***a* and **19***b*, an input wire **19***c*, an output wire **19***d*, and common wires **19***e*.

[0059] One pair of the wires **18***a* and **18***b* is provided for each of the COFs **12**. One end of the wires **18***a* is connected to respective wires **14***a*, and one end of the wires **18***b* is connected to respective wires **14***b*. The input wire **18***c* causes the terminal TA**1** to be connected to one end of the wire **18***b* that is connected to a wire **14***b* of a COF **12** provided on one end (left end in Figure) of the PWB **16**. The output wire **18***d* causes the terminal TA**2** to be connected to the other end of a wire **18***a* that is connected to the wire **14***a* of a COF **12** provided on the other end (right end in Figure) of the PWB **16**. Moreover, the common wires **18***e* cause adjacent wires **18***a* and **18**b of adjacent pairs of the wires **18***a* and **18***b* to be connected to each other.

[0060] Similarly, one pair of wires **19***a* and **19***b* is provided for each of the COFs **12**. One end of the wires **19***a* is connected to one end of respective short-circuit wires **15**, and one end of the wires **19***b* is connected to the other end of the respective short-circuit wires **15**. The input wire **19***c* causes the terminal TB**1** to be connected to the other end of a wire **19***b* that is connected to one end of a short-circuit wire **15** of the COF **12** provided on one end (left end in Figure) of the PWB **16**. The output wire **19***d* causes the terminal TB**2** to be connected to the other end of the wire **19***a* that is connected to the other end of a short-circuit wire **15** in the COF **12** provided on the other end (right end in Figure) of the PWB **16**. Moreover, the common wires **19***e* cause adjacent wires **19***a* and **19***b* of adjacent pairs of the wires **19***a* and **19***b* to be connected to each other.

[0061] The terminals TX**1** and TX**2** are connected to ends of the wires **18***a* and **18***b* on the COF **12** side, respectively. Similarly, the terminals TY**1** and TY**2** are connected to ends of the wires **19***a* and **19***b* on the COF **12** side, respectively.

[0062] The PWB **16** is connected to the COF **12** at a connection section **20** via the ACF, in such a manner that a connecting end section of the PWB **16** overlaps with a connecting end section of each of the COFs **12**. Thus, the aforementioned input wires of each of the COFs **12** and the wiring pattern are electrically connected to each other.

[0063] Moreover, the test wiring sections **14** of the COFs **12** and the test wiring section **18** of the PWB **16** become electrically connected to each other. More specifically, the wires **18***a* and **18***b* of the PWB **16** are connected to respective wires **14***a* and **14***b* of corresponding COFs **12**. Thus, the test wiring section **18**, the test wiring sections **14** and the short-circuit wires **21** are connected so as to form one wire between the terminals TA**1** and TA**2**.

[0064] Further, the short-circuit wires **15** of the COFs **12** and the test wiring section **19** of the PWB **16** are electrically connected to each other. More specifically, the wires **19***a* and **19***b* of the PWB **16** are connected to the ends of the short-circuit wires **15** of the corresponding COF **12**s, respectively. Thus, the test wiring section **19** and the short-circuit wires **15** are connected so as to form one wire between the terminals TB**1** and TB**2**.

[0065] In such a state, a test signal which has an arbitrary waveform is inputted from the terminals TA**1** and TB**1**, and a signal that appears at the terminals TA**2** and TB**2** are monitored. This allows assumption of (i) a breakage state of the COF **12** and/or the PWB **16**, (ii) a connection state between the display panel **11** and the COFs **12**, and (iii) a connection state between the COFs **12** and the PWB **16**.

[0066] For example, if the signal that appears at the terminals TA**2** and TB**2** are of a substantially same waveform as the signal thus inputted, the test wiring sections **14**, **18**, and **19** are properly transmitting the signal. Therefore, the connection between the display panel **11** and the COFs **12** and the connection between the COFs **12** and the PWB **16** are normal. As a result, it is possible to consider that no breakage has occurred to the COFs **12** and the PWB **16** in at least parts in which the test wiring sections **14**, **18** and **19** are provided on the COFs **12** and the PWB **16**.

[0067] If a signal does not appear at just the terminal TA**2**, there is a high possibility that the test wiring sections **14** and **18** itself are disconnected, or that the connection state between the test wiring sections **18** and **14** and/or the connection state between the test wiring sections **14** and the short-circuit wires **21** have degraded. Hence, in this case, there is a possibility of (i) a breakage in an edge section (end section in which the test wiring section **14** is provided) of the COFs **12**, or (ii) occurrence of a poor connection between the COFs **12** and the PWB **16** and/or a poor connection between the display panel **11** and the COFs **12**.

[0068] Moreover, if a signal does not appear at just the terminal TB**2**, there is a high possibility that the test wiring section **19** is disconnected, or that the connection state between the test wiring section **19** and the short-circuit wires **15** has degraded. Thus, in this case, there is a possibility of a breakage in an edge section (end section in which the short circuit wires **15** is provided) of the COFs **12**, or occurrence of a poor connection between the COFs **12** and the PWB **16**.

[0069] If the waveform of the signal that appears at just the terminal TA**2** is blunter as compared to that of the signal thus inputted, there is a possibility that resistances of the test wiring sections **14** and **18** have increased due to the breakage of the test wiring sections **14** and **18**, or the like. Moreover, if the waveform of the signal that appears at just the terminal TB**2** is blunter as compared to that of the signal thus inputted, there is a possibility that a resistance of the test wiring section **19** has increased due to the breakage of the test wiring section **19**.

[0070] Moreover, the following comparisons may be carried out: (i) comparing between a resistance of a wiring path including the test wiring sections **14** and **18** and the short-circuit wires **21** and a normal resistance of such wiring path measured in advance; and (ii) comparing between a resistance of a wiring path including the test wiring section **19** and the short-circuit wires **15** and a normal resistance of that wiring path measured in advance. Carrying out these comparisons also allow the assumption of (i) the breakage state of the COFs **12** and (ii) the connection state between the display panel **11** and the COFs **12**. A remarkably larger resistance of the wiring path as compared to a normal value gives an assumption that a state of the wiring path is close to disconnection. The terminals TA**1**, TA**2**, TB**1** and TB**2** are usable for measurement of the resistance.

[0071] Moreover, measurement of the resistance between the terminal TX**1** and the TX**2** and the resistance between the terminal TY**1** and TY**2** allows verification of whether the aforementioned sections are broken or have poor connection at the connecting sections, in each of the COFs **12**.

[0072] As such, in the present embodiment, the display panel **11** has the short-circuit wires **21**, and the COFs **12** have the test wiring sections **14** and the short-circuit wires **15**. The test wiring sections **14** cause the test wiring section **18** to be connected the short-circuit wires **21**, and the short-circuit wires **15** are connected to the test wiring section **19**. The terminals TA**1** and TA**2** are connected to the ends of the test wiring section **18**, respectively, and the terminals TB**1** and TB**2** are connected to the ends of the test wiring section **19**, respectively. This arrangement allows easy assumption of (i) a breakage state of the COFs **12**, (ii) the connection state between the display panel **11** and the COFs **12** and (iii) the connection state between the COFs **12** and the PWB **16**, by checking a state of outputted signals from the terminals TA**2** and TB**2** with respect to inputted signals from the terminals TA**1** and TB**1**, during use of the display apparatus including the display panel **11**. Moreover, a similar assumption can be made by carrying out the following comparisons: (i) comparing between a resistance between the terminals TA**1** and TA**2** and its normal resistance; and (ii) comparing between a resistance between the terminals TB**1** and TB**2** and its normal resistance.

[0073] The following description explains a modification of the present embodiment. FIG. **5** is a plan view illustrating the modification.

[0074] As illustrated in FIG. **5**, the present modification includes a display panel **23**, COFs **24** and a PWB **25**.

[0075] The COFs **24** have a same arrangement as the COFs **12** except that the COFs **24** further include test wiring sections **26**. The test wiring sections **26** are provided further closer to the side end than the short-circuit wires **15** of the aforementioned COFs **12**. The test wiring sections **26** are made of two wires **26***a* and **26***b* provided parallel to each other.

[0076] The display panel **23** has a same arrangement as the display panel **11** except that the display panel **23** further has short-circuit wires **27**. The short-circuit wires **27** are provided as similar to the short-circuit wires **21**, so as to short-circuit the wires **26***a* and **26***b*.

[0077] The PWB **25** has a same arrangement as the PWB **16** expect that the PWB **25** further has a test wiring section **28**. The test wiring section **28** includes wires **28***a* and **28***b* and a wiring group **28***c*, **28***d*, and **28***e*, and is connected to the test wiring sections **26** such that a similar relationship as the connection between the test wiring section **18** and the test wiring sections **14** is established. In addition, the test wiring sections **26** has terminals TZ**1** and TZ**2** provided for each of the COFs **24**, which terminals TZ**1** and TZ**2** function as similar to the foregoing terminals TX**1** and TX**2**.

[0078] In the arrangement, use of a wiring path including the test wirings **26** and **28** and the short-circuit wires **27** allows conducting a similar test to the aforementioned electrical test and resistance measurement test, which electrical test and resistance measurement test passes a signal through the wiring path made of the test wiring sections **14** and **18** and the short-circuit wires **21**. Thus, it is possible to assume (i) a breakage on both of side ends of the COFs **24** on which stress is readily applied and (ii) a connection state between the display panel **23** and the COFs **24** and/or a connection state between the COFs **24** and the PWB **25**, during use of a display apparatus including the arrangement of the present modification.

[0079] The present embodiment explains an arrangement in which the test wiring sections **14** and the short-circuit wires **15** are provided in a vicinity of both side edges of the COFs **12** and **24**, respectively. However, if there is a limitation to a layout of a pin in the COFs **12** and **24**, just either one of the test wiring sections **14** or the short-circuit wires **15** may be provided.

[0080] Moreover, in the present embodiment, further dummy wires **41** and **42** may be provided to the COFs **12** and **24**, as illustrated by alternate long and short dash lines in FIGS. **3** and **5**. The dummy wires **41** are provided between the test wiring sections **14** and one side edge of the COFs **12** and **24**. Each of the dummy wires **42** are provided between the short-circuit wires **15** and the other side edge of the COFs **12** and **24**.

[0081] The dummy wires **41** and **42** are usually provided as independent wires that are not electrically connected to any wires of the display panels **11** and **23** or to any external wires. Such dummy wires **41** and **42** function so as to reinforce the COFs **12** and **24**. Thus, it is possible to reinforce strength of both side edges of the COFs **12** and **24**.

[0082] The dummy wires **41** and **42** can be electrically connected to the display panels **11** and **23** or the PWB **16** and **25**, if necessary.

Third Embodiment

[0083] FIG. **6** illustrates an arrangement of a liquid crystal display device **101** according to the present embodiment.

[0084] As illustrated in FIG. **6**, the liquid crystal display device **101** includes a liquid crystal display panel **102**, a plurality of source drivers **103**, a plurality of gate drivers **104**, and a controller **105**.

[0085] The liquid crystal display panel **102** includes a plurality (m×i lines) of gate bus lines G**11** to Gmi, a plurality (n×j lines) of source bus lines S**11** to Snj, and a plurality of pixels PIX.

[0086] In explanations that follow, "gate bus lines G" denotes all of the gate bus lines G**11** to Gmi as appropriate, when an explanation is made with respect to all of the gate bus lines G**11** to Gmi. Similarly, "source bus lines S" denotes all of the source bus lines S**11** to Snj as appropriate, when an explanation is made with respect to all of the source bus lines S**11** to Snj.

[0087] The pixels PIX are provided in the vicinity of intersecting parts of the gate bus lines G and the source bus lines S. The pixels PIX has a thin film transistor (hereinafter referred simply as transistor) and a display element provided on a glass substrate of the liquid crystal display panel **102**.

[0088] Gates of the transistors are connected to the gate bus lines G. Sources of the transistors are connected to the source bus lines S. Further, drains of the transistors are connected to pixel electrodes (not illustrated). A common electrode (not illustrated) is provided so as to face the pixel electrodes. A common voltage is applied to this common electrode. The display element is made of the pixel electrodes, the common electrode, and liquid crystal provided between the electrodes.

[0089] The gate bus lines G**11** to Gmi, the source bus lines S**11** to Snj, the transistors and the pixel electrodes are formed on the glass substrate. The common electrode is provided on another glass substrate provided so as to face the glass substrate on which the gate bus lines G, the source bus lines S, the

transistors and the pixel electrodes are formed. Accordingly, liquid crystal is injected between the two glass substrates (between the pixel electrodes and the common electrode) so as to fill a space therebetween.

[0090] An n number of source drivers **103** are provided in the liquid crystal display device **101**. The source drivers **103** cause a start pulse SSP to be transferred by use of a shift register, at a timing of a source clock signal SCK. Thereafter, the source drivers **103** hold display data Dx at a position of corresponding source bus lines S, at a timing of a timing pulse outputted from output stages of the shift register. Moreover, the source drivers **103** read the display data Dx thus held into a latch, at a timing of a latch signal LS, and outputs this display data Dx thus read to a j number of source bus lines S.

[0091] An m number of gate drivers **104** are provided in the liquid crystal display device **101**. The gate drivers **104** cause a start pulse GSP to be transferred by use of a shift register, at a timing of a gate clock signal GCK, and generates a gate pulse by use of a timing pulse outputted from the output stages of the shift register, so as to output to an i number of gate bus lines G.

[0092] The controller **105** generates control signals such as the start pulse SSP, the source clock signal SCK, and the latch signal LS, which are provided to the source drivers **103**, and also outputs received display data Dx to the source drivers **103**. The controller **105** generates control signals such as the start pulse GSP and the gate clock signal GCK, which are provided to the gate drivers **104**.

[0093] In the liquid crystal display device **101**, the liquid crystal display panel **102** is arranged as the display panel **1**, **11**, or **23**. Moreover, the source drivers **103** and the gate drivers **104** are the driver chips **3** in the arrangement of the display panel **1**, the COFs **12** in the arrangement of the display panel **11**, or the COFs **24** in the arrangement of the display panel **23**. Hence, in a case where the liquid crystal display panel **102** is arranged as the display panel **1**, the liquid crystal display panel **102** is to be connected to the FPC **2**. Moreover, in a case where the liquid crystal display panel **102** is arranged as the display panel **11**, the liquid crystal display panel **102** is to be connected to the PWB **16**. Further, in a case where the liquid crystal display panel **102** is arranged as the display panel **23**, the liquid crystal display panel **102** is to be connected to the PWB **25**.

[0094] As such, incorporation of the display panel **1**, **11** or **23** in the liquid crystal display device **101** makes it possible to easily assume, during use of the liquid crystal display device **101**, (i) a breakage state of the FPC **2** or the PWB **16** or **25**, particularly on both end sections of the FPC **2** or the PWB **16** or **25** on which stress is readily applied, and (ii) a connection state between the liquid crystal display panel **102** and the FPC **2** or the PWB **16** or **25**.

[0095] The present embodiment explains that the display panel **1** of First Embodiment or the display panel **11** or **23** of Second Embodiment are incorporated in the liquid crystal display device **101**. However, the display panel **1**, **11**, and **23** may be incorporated in other display apparatuses such as an organic LE display or a plasma display as long as the display panel **1**, **11**, and **23** can be driven by use of a driver chip.

Summary of Embodiment

[0096] A display panel according to the present embodiment, which is connected to a wiring-mounted board on which signal supply wiring that supplies signals for driving the display panel is mounted, is arranged such that the wiring-mounted board has (i) first and second wires which extend toward the display panel, and (ii) first and second terminals which are connected to the first and second wires, respectively, and the display panel has a first short-circuit wire, which is connected to the first and second wires, at a connecting part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires.

[0097] In the arrangement, first and second wires are connected so as to form one wire via a first short-circuit wire. In such state, it is possible to assume (i) a breakage state of the wiring-mounted board and (ii) a connection state between the display panel and the wiring-mounted board, by inputting a signal from a first terminal and checking a state of the signal that appears at a second terminal. A same assumption can be made by carrying out the following comparison: (i) a normal resistance of the first and second wires connected so as to form one wire is measured between the first and second terminals in advance; and (ii) a resistance of the wiring that is similarly measured at a state in which the wiring has changed over time is compared to the normal resistance.

[0098] It is preferable for the display panel to be arranged such that the first and second wires are provided on at least one side end section of the wiring-mounted board. This allows easy assumption of (i) the breakage state of the wiring-mounted board, particularly on both end sections of the wiring-mounted board which easily receive stress, and (ii) a connection state between the wiring-mounted board and the display panel.

[0099] Alternatively, it is preferable for the display panel to be arranged such that the display panel is connected to the wiring-mounted board, via an intermediate substrate on which wiring for communicating signals between the wiring-mounted board and the display panel is mounted, and the intermediate substrate has third and fourth wires that cause the respective first and second wires to be connected to the first short-circuit wire. An intermediate substrate is made of, for example, the aforementioned COF. The first and second wires and the first short-circuit wire are caused to be connected via the third and fourth wires; even if the intermediate substrate is present between the wiring-mounted board and the display panel, the first and second wires are connected so as to form one wire. Hence, it is possible to check a state of a signal inputted from the first terminal at the second terminal.

[0100] It is preferable for the display panel to be arranged such that the wiring-mounted board has (i) fifth and sixth wires, which extend toward the intermediate substrate, and (ii) third and fourth terminals, which are connected to the fifth and sixth wires, respectively, and the intermediate substrate has a second short-circuit wire which is connected to the fifth and sixth wires, at a connecting part of the intermediate substrate and the wiring-mounted board, so as to short-circuit the fifth and sixth wires. In this arrangement, fifth and sixth wires are connected so as to form one wire, via a second short-circuit wire. In this state, it is possible to easily assume, during use of a display apparatus including the display panel, (i) the breakage state of the wiring-mounted board and (ii) a connection state between the wiring-mounted board and the intermediate substrate. A similar assumption can also be made by the following comparison: (i) a normal resistance of the fifth and sixth wires connected so as to form one wire is measured between the third and fourth terminals in advance; and (ii) a resistance similarly measured in a state in which the wire has changed over time is compared to the normal resistance.

[0101] It is preferable for the display panel having the intermediate substrate to be arranged such that the intermediate substrate is made up of a plurality of intermediate substrates, and the display panel is connected to the wiring-mounted board via the plurality of intermediate substrates. Hence, even if there are the plurality of intermediate substrates, it is possible to assume connection states between the wiring-mounted board and the intermediate substrate and between the display panel and the intermediate substrate, for each of the intermediate substrates.

[0102] It is preferable for the display panel to be arranged such that the intermediate substrate has a pair of the fifth and sixth wires on both of side end sections of the intermediate substrate.

[0103] It is preferable for the display panel to be arranged such that the wiring-mounted board is a printed wiring board, and the intermediate substrate is a mounting substrate on which an integrated circuit for driving the display panel is mounted on a film. This allows assumption of a connection state between a printed wiring board and a mounting substrate that easily receives damage due to stress caused by vibration or the like received for a long term.

[0104] A liquid crystal display device according to the present embodiment includes any one of the foregoing display panels.

[0105] This thus allows, during use of the liquid crystal display device as a product after the liquid crystal display device has been marketed, assumption of a connection state between the wiring-mounted board and the display panel, and other states, as described above.

[0106] A drive-circuit-mounted board according to the present embodiment mounts (i) a semiconductor-integrated circuit that outputs drive signals for driving the display panel (ii) wiring that is connected to the semiconductor-integrated circuit, which drive-circuit-mounted board is connected between the display panel and a wiring-mounted board on which signal supply wiring for supplying, to the semiconductor-integrated circuit, signals causing the semiconductor-integrated circuit to output the drive signals is mounted, the drive-circuit-mounted board further including third and fourth wires causing first and second wires provided on the wiring-mounted board to be connected to a first short-circuit wire provided on the display panel for short-circuiting the first and second wires.

[0107] This drive-circuit-mounted board is equivalent to the foregoing intermediate substrates. Thus, the first and second wires and the first short-circuit wire are respectively connected to the third and fourth wires. Hence, as described above, the first and second wires are connected so as to form one wire.

[0108] It is preferable for the drive-circuit-mounted board to further include a second short-circuit wire, connected to corresponding fifth and sixth wires provided on the wiring-mounted board, for short-circuiting the fifth and sixth wires. The fifth and sixth wires are caused to connect via a second short-circuit wire; hence, the fifth and sixth wires are connected so as to form one wire as aforementioned.

[0109] As described above, a display panel according to the present embodiment is connected to a wiring-mounted board, which wiring-mounted board has (i) first and second wires which extend toward the display panel, and (ii) first and second terminals which are connected to the first and second wires, respectively. In addition, the display panel has a first short-circuit wire which is connected to the first and second wires, at a connection part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires. Thus, it is possible to electrically check states (whether or not the wires are disconnected, or the like) of the first and second wires that are connected via the first short-circuit wire. Hence, (i) a breakage state of the wiring-mounted board and (ii) a connection state between the display panel and the wiring-mounted board are easily assumed during use of a display apparatus that includes the display panel.

[0110] A display panel of the present embodiment allows, by checking a conductivity state of signal wiring to a drive circuit even while the display panel is in use, assumption of a breakage state of a flexible substrate on which such signal wiring is mounted. Hence, the display panel is suitably used for an onboard display apparatus.

[0111] The embodiments and concrete examples of implementation discussed in the foregoing detailed explanation serve solely to illustrate the technical details of the present invention, which should not be narrowly interpreted within the limits of such embodiments and concrete examples, but rather may be applied in many variations within the spirit of the present invention, provided such variations do not exceed the scope of the patent claims set forth below.

1.
A display panel connected to a wiring-mounted board on which signal supply wiring that supplies signals for driving the display panel is mounted,
the wiring-mounted board having (i) first and second wires which extend toward the display panel, and (ii) first and second terminals, which are connected to the first and second wires, respectively and
the display panel having a first short-circuit wire, which is connected to the first and second wires, at a connecting part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires.

2.
The display panel as set forth in claim **1**, wherein the first and second wires are provided on at least one side end section of the wiring-mounted board.

3.
The display panel as set forth in claim **1**, wherein
the display panel is connected to the wiring-mounted board, via an intermediate substrate on which wiring for communicating signals between the wiring-mounted board and the display panel is mounted, and
the intermediate substrate has third and fourth wires that cause the respective first and second wires to be connected to the first short-circuit wire.

4.
The display panel as set forth in claim **3**, wherein
the wiring-mounted board has (i) fifth and sixth wires, which extend toward the intermediate substrate, and (ii) third and fourth terminals, which are connected to the fifth and sixth wires, respectively, and
the intermediate substrate has a second short-circuit wire, which is connected to the fifth and sixth wires, at a connecting part of the intermediate substrate and the wiring-mounted board, so as to short-circuit the fifth and sixth wires.

5.
The display panel as set forth in claim **3**, wherein the intermediate substrate is made up of a plurality of inter-

mediate substrates, and the display panel is connected to the wiring-mounted board via the plurality of the intermediate substrates.

6.

The display panel as set forth in claim **4**, wherein the intermediate substrate has a pair of the fifth and sixth wires on both of side end sections of the intermediate substrate.

7.

The display panel as set forth in claim **3**, wherein

the wiring-mounted board is a printed wiring board, and

the intermediate substrate is a mounting substrate on which an integrated circuit for driving the display panel is mounted on a film.

8.

A liquid crystal display device comprising:

a display panel; and

a wiring-mounted board connected to the display panel on which signal supply wiring that supplies signals for driving the display panel is mounted,

the wiring-mounted board having (i) first and second wires which extend toward the display panel, and (ii) first and second terminals which are connected to the first and second wires, respectively, and

the display panel having a first short-circuit wire, which is connected to the first and second wires, at a connecting part of the display panel and the wiring-mounted board, so as to short-circuit the first and second wires.

9.

The liquid crystal display device as set forth in claim **8**, wherein the first and second wires are provided on at least one side end section of the wiring-mounted board.

10.

The liquid crystal display device as set forth in claim **8**, wherein

the display panel is connected to the wiring-mounted board via an intermediate substrate on which wiring for communicating signals between the wiring-mounted board and the display panel is mounted, and

the intermediate substrate has third and fourth wires that cause the respective first and second wires to be connected to the first short-circuit wires.

11.

The liquid crystal display device as set forth in claim **10**, wherein

the wiring-mounted board has (i) fifth and sixth wires, which extend toward the intermediate substrate, and (ii) third and fourth terminals, which are connected to the fifth and sixth wires, respectively, and

the intermediate substrate has a second short-circuit wire which is connected to the fifth and sixth wires, at a connecting part of the intermediate substrates and the wiring-mounted board, so as to short-circuit the fifth and sixth wires.

12.

The liquid crystal display device as set forth in claim **10**, wherein the intermediate substrate is made up of a plurality of intermediate substrates, and the display panel is connected to the wiring-mounted board via the plurality of the one or more intermediate substrates.

13.

The liquid crystal display device as set forth in claim **11**, wherein the intermediate substrate has a pair of the fifth and sixth wires on both of side end sections of the intermediate substrates.

14.

The liquid crystal display device as set forth in claim **10**, wherein

the wiring-mounted board is a printed wiring board, and

the intermediate substrate is a mounting substrate on which an integrated circuit for driving a display panel is mounted on a film.

15.

A drive-circuit-mounted board comprising:

a semiconductor-integrated circuit that outputs drive signals for driving a display panel; and

wiring that is connected to the semiconductor-integrated circuit;

wherein the drive-circuit-mounted board is connected between the display panel and a wiring-mounted board on which signal supply wiring for supplying, to the semiconductor-integrated circuit, signals causing the semiconductor-integrated circuit to output the drive signals,

the drive-circuit-mounted board further comprising the third and fourth wires causing first and second wires provided on the wiring-mounted board to be connected to a first short-circuit wire provided on the display panel for short-circuiting the first and second wires.

16. The drive-circuit-mounted board as set forth in claim **15**, further comprising:

a second short-circuit wire, connected to the fifth and sixth wires that are provided on the wiring-mounted board, for short-circuiting the fifth and sixth wires.

* * * * *