

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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BOE TECHNOLOGY GROUP CO., LTD.

Petitioner v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

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PTAB Case No. IPR 2025-01412

Patent No. 8,391,020

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**DECLARATION OF DR. PATRICK MURPHY IN SUPPORT OF  
PETITION FOR *INTER PARTES* REVIEW  
OF PATENT NO. 8,391,020**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code.

Executed on September 5, 2025 in New York, NY.

Signed by:  
  
329EB749D3704D6...

Patrick F. Murphy, Ph.D., P.E.

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## **EXHIBIT LIST**

| Exhibit No. | Document                                                                                                                                                                                                                                    |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ex. 1001    | U.S. Patent No. 8,391,020 (“ <b>’020 Patent</b> ”)                                                                                                                                                                                          |
| Ex. 1002    | Declaration and Curriculum Vitae of Dr. Patrick Murphy (“ <b>Murphy</b> ”)                                                                                                                                                                  |
| Ex. 1003    | File history of the ’020 Patent                                                                                                                                                                                                             |
| Ex. 1004    | U.S. Patent Application Publication No. 2008/0291379 (“ <b>Takenaka</b> ”)                                                                                                                                                                  |
| Ex. 1005    | Japanese Patent Application Publication No. 2009168877A & Certified Translation (“ <b>Ito</b> ”)                                                                                                                                            |
| Ex. 1006    | Japanese Patent Application Publication No. H0643473A & Certified Translation (“ <b>Takemura</b> ”)                                                                                                                                         |
| Ex. 1007    | den Boer, W., Active Matrix Liquid Crystal Displays (2005) (“ <b>den Boer</b> ”)                                                                                                                                                            |
| Ex. 1008    | Chen, C.-I. et al., “Bondability Study of Chip-on-Film (COF) Inner Lead Bonding (ILB) Using Conventional Gang Bonder,” IEEE Transactions on Electronics Packaging Manufacturing, Vol. 31, No. 4, p. 285-90 (October 2008) (“ <b>Chen</b> ”) |
| Ex. 1009    | Watanabe, I. et al., “19.1: Invited Paper: Driver IC Packaging Technologies Using Anisotropic Conductive Films in Flat Panel Display,” SID Symposium Digest of Technical Papers, Vol. 39, p. 240-43 (2008) (“ <b>Watanabe</b> ”)            |
| Ex. 1010    | Govaerts, J. et al., “Interconnecting drivers to flexible displays,” Journal of the Society for Information Display, Vol. 16, No. 7, p. 765-775 (2008) (“ <b>Govaerts</b> ”)                                                                |
| Ex. 1011    | U.S. Patent Application Publication No. 2010/0321623 (“ <b>Wakita</b> ”)                                                                                                                                                                    |
| Ex. 1012    | U.S. Patent Application Publication No. 2011/0175800 (“ <b>Mizumaki</b> ”)                                                                                                                                                                  |

| Exhibit No. | Document                                                                                                                                                                                       |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ex. 1013    | Minami, H. et al., “Prospects of LCD Panel Fabrication and Inspection Equipment Amid Growing Demand for Increased Size,” Hitachi Review, Vol. 56, No. 3, p. 63-69 (2007) (“ <b>Minami</b> ”)   |
| Ex. 1014    | Souk, J. et al., Flat Panel Display Manufacturing (2018) (“ <b>Souk</b> ”)                                                                                                                     |
| Ex. 1015    | Ni, G. et al., “Automated optical inspection of liquid crystal display anisotropic conductive film bonding,” Optical Engineering, Vol. 55, No. 10, 103109-1 - 8 (October 2016) (“ <b>Ni</b> ”) |
| Ex. 1016    | Li, T. et al., “A Novel Method for LCD Module Alignment and Particle Detection in Anisotropic Conductive Film Bonding,” Machines, Vol. 11, No. 49, p. 1-19 (2023) (“ <b>Li</b> ”)              |
| Ex. 1017    | Murakami, T. et al., “Electrostatic problems and ionization solutions in TFT-LCD production,” Solid State Technology, Vol. 40, No. 1 (January 1997) (“ <b>Murakami</b> ”)                      |
| Ex. 1018    | U.S. Patent No. 5,737,272 (“ <b>Uchiyama</b> ”)                                                                                                                                                |

### **CHALLENGED CLAIM LISTING**

| <b>Claim</b> | <b>Limitation No.</b> | <b>Limitation</b>                                                                                                                                                                                                                           |
|--------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1            | [1pre]                | An electro-optical device comprising:                                                                                                                                                                                                       |
|              | [1a]                  | an electro-optical panel including:                                                                                                                                                                                                         |
|              | [1b]                  | a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and                                                          |
|              | [1c]                  | a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal |
|              | [1d]                  | the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,                                                                                            |
|              | [1e]                  | the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;                                                                                           |
|              | [1f]                  | a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;                                                           |
|              | [1g]                  | a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion; and                 |
|              | [1h]                  | a second circuit substrate including: a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion;                                                       |

| Claim | Limitation No. | Limitation                                                                                                                                                                                                                                                                         |
|-------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | [1i]           | a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.                                |
| 2     |                | The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.                                                                       |
| 3     | [3a]           | The electro-optical device according to claim 1, wherein: each of the first and second group of terminals configures a terminal group arranged in a predetermined direction, and                                                                                                   |
|       | [3b]           | the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.                                                                                                    |
| 4     |                | The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.                            |
| 5     | [5a]           | The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a fourth terminal portion having a fourth group of terminals arranged so as to be adjacent to the third terminal portion, |
|       | [5b]           | a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on which a fourth connection terminal portion having a  |

| Claim | Limitation No. | Limitation                                                                                                                                                                                                                                                                                            |
|-------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                | fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,                                                                                                                                                                                         |
|       | [5c]           | the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel, |
|       | [5d]           | the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and                                                                                                                   |
|       | [5e]           | the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,                                                          |
|       | [5f]           | the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and                                                                  |
|       | [5g]           | the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.                                                             |
| 6     |                | The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.                                                                                                                                                      |
| 7     | [7a]           | The electro-optical device according to claim 5, wherein: each of the third and fourth group of terminals configures                                                                                                                                                                                  |

| Claim | Limitation No. | Limitation                                                                                                                                                                                                                                                                                          |
|-------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                | a terminal group arranged in a predetermined direction, and                                                                                                                                                                                                                                         |
|       | [7b]           | the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.                                                                                                                    |
| 8     | [8pre]         | An electro-optical device comprising:                                                                                                                                                                                                                                                               |
|       | [8a]           | an electro-optical panel including:                                                                                                                                                                                                                                                                 |
|       | [8b]           | a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and                                                                                                                  |
|       | [8c]           | a third terminal portion arranged on a side opposed to a display region with respect to the first terminal portion, the third terminal portion having a third group of terminals, the third group of terminals including: a fifth terminal; and a sixth terminal separated from the fifth terminal, |
|       | [8d]           | the first terminal and the fifth terminal being electrically connected through a fifth connection wiring provided on the electro-optical panel,                                                                                                                                                     |
|       | [8e]           | the second terminal and the sixth terminal being electrically connected through a sixth connection wiring provided on the electro-optical panel;                                                                                                                                                    |
|       | [8f]           | a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;                                                                                                                   |
|       | [8g]           | a first external terminal connected to the first terminal through the first connection terminal portion; and a                                                                                                                                                                                      |

| Claim | Limitation No. | Limitation                                                                                                                                                                                                                                      |
|-------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                | second external terminal connected to the second terminal through the first connection terminal portion respectively; and                                                                                                                       |
|       | [8h]           | a third circuit substrate including: a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion;                                                               |
|       | [8i]           | a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion; and a sixth external terminal electrically connected to the sixth terminal through the third connection terminal portion. |
| 9     |                | The electro-optical device according to claim 8, wherein the fifth connection wiring and the sixth connection wiring are provided at an end side of the electro-optical panel rather than the display region.                                   |
| 10    | [10a]          | The electro-optical device according to claim 8, wherein: each of the first and third group of terminals configures a terminal group arranged in a predetermined direction, and                                                                 |
|       | [10b]          | the first terminal and the second terminal, and the fifth terminal and the sixth terminal are provided at both end sides of the predetermined direction of the terminal group.                                                                  |
| 11    | [11pre]        | An electro-optical panel comprising:                                                                                                                                                                                                            |
|       | [11a]          | a substrate;                                                                                                                                                                                                                                    |
|       | [11b]          | a first terminal portion including a first group of terminals having a first terminal and a second terminal separated from each other;                                                                                                          |

| Claim | Limitation No. | Limitation                                                                                                                                                                                                                                         |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | [11c]          | a second terminal portion arranged adjacent to the first terminal portion, the second terminal portion including a second group of terminals having a third terminal and a fourth terminal separated from each other;                              |
|       | [11d]          | a third terminal portion arranged between one side of the substrate and the first terminal portion, the third terminal portion including a third group of terminals having a fifth terminal and a sixth terminal separated from each other;        |
|       | [11e]          | a fourth terminal portion arranged between one side of the substrate and the second terminal portion, the fourth terminal portion including a fourth group of terminals having a seventh terminal and a eighth terminal separated from each other; |
|       | [11f]          | a first connection wiring configured to electrically connect the first terminal and the fourth terminal;                                                                                                                                           |
|       | [11g]          | a fifth connection wiring configured to electrically connect the first terminal and the fifth terminal;                                                                                                                                            |
|       | [11h]          | a sixth connection wiring configured to electrically connect the second terminal and the sixth terminal;                                                                                                                                           |
|       | [11i]          | a seventh connection wiring configured to electrically connect the third terminal and the seventh terminal;                                                                                                                                        |
|       | [11j]          | an eighth connection wiring configured to electrically connect the fourth terminal and the eighth terminal; and                                                                                                                                    |
|       | [11k]          | a ninth connection wiring configured to electrically connect the sixth connection wiring and the seventh connection wiring so as to electrically connect the second terminal, the third terminal, the sixth terminal and the seventh terminal.     |

| Claim | Limitation No. | Limitation                                                                                                                                                                                         |
|-------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12    | [12a]          | An electro-optical device comprising: the electro-optical panel according to claim 11;                                                                                                             |
|       | [12b]          | a first circuit substrate on which a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion is provided and     |
|       | [12c]          | which has a first external terminal connected to the first terminal through the first connection terminal portion and a second external terminal connected to the second terminal;                 |
|       | [12d]          | a second circuit substrate on which a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion is provided and |
|       | [12e]          | which has a third external terminal connected to the third terminal through the second connection terminal portion and a fourth external terminal connected to the fourth terminal;                |
|       | [12f]          | a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided and     |
|       | [12g]          | which has a fifth external terminal connected to the fifth terminal through the third connection terminal portion and a sixth external terminal connected to the sixth terminal; and               |
|       | [12h]          | a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided and |

| Claim | Limitation No. | Limitation                                                                                                                                                                               |
|-------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | [12i]          | which has a seventh external terminal connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal connected to the eighth terminal. |
| 13    |                | An electronic apparatus comprising the electro-optical device according to claim 1.                                                                                                      |

I, Dr. Patrick Murphy, declare as follows:

1. I have been retained by Holland & Knight LLP on behalf of BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”) to provide certain opinions regarding the patentability of claims 1-13 of U.S. Patent No. 8,391,020 (“’020 Patent”).

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

3. I am a salaried employee of Exponent. Exponent charges \$575 per hour for my time plus expenses for work performed in connection with this project, and I am being paid my regular salary for time spent on this project. I have received no additional compensation for work in this case. My compensation does not depend upon the contents of this declaration, any testimony I may provide, or the ultimate outcome of the case. I have no other interest in this proceeding.

## **I. INTRODUCTION AND QUALIFICATIONS**

4. My technical background and experience for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my curriculum vitae, which is attached as Appendix 1.

5. I received my B.S. degree in Electrical Engineering (magna cum laude) in 2002 from Boston University; my M.A. degree in Electrical Engineering in 2004 from Princeton University; and my Ph.D. degree in Electrical Engineering, also from

Princeton University in 2009. This education included advanced coursework, project work, and laboratory work in design and manufacturing of electronic circuits, integrated circuits, and optoelectronic devices, including liquid crystal displays (“LCDs”). Specifically, my undergraduate and Master’s coursework included study of methods and apparatus for testing of electrical circuits and semiconductor devices such as LCDs, as well as optics of liquid crystal materials used in LCDs, the effects of electrical overstress and electrostatic discharge on CMOS devices and circuits, techniques such as surge limiting devices for protecting against electrostatic discharge when designing electronic circuits and systems, and fabrication techniques for manufacturing integrated circuits including thin-film transistors for LCD backplanes and multilayer conductive paths on flexible and rigid substrates.

6. My training and research for my academic degrees at Princeton was generally in the area of semiconductor integrated circuit design and fabrication technologies, including liquid crystal optoelectronic devices. I fabricated and tested integrated circuits and optoelectronic devices on various substrates. I taught university-level topics in electronic devices, integrated circuit testing and fabrication, and optics. I am author of several publications in these areas, including on liquid crystal-based optoelectronic devices as well as on electronic and optoelectronic devices for displays and other applications.

7. I am licensed as a professional engineer in the State of New York and licensed as a professional engineer in electrical engineering in the State of California. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE). I have over 20 years of experience in electrical engineering including over 20 years of experience in the areas of design and manufacturing of electronic circuits and optoelectronic devices.

8. I am currently a Principal Engineer in Exponent's Electrical Engineering and Computer Science Practice and I am based in Exponent's New York office. Exponent is an engineering and science consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025.

9. Since joining Exponent in 2009, my duties and responsibilities have included leading investigations into the performance, design, and condition, of electrical and electronic systems and devices, including projects relating to the design, structure, function, and failures of electronic circuits and optoelectronic devices, such as LCDs.

10. As part of my work at Exponent, I have analyzed the materials, manufacturing processes, components, designs, and applications of LCD panels. I also have experience with the technology of connectors, flat panel displays, TFTs and backplanes for displays, as well as design, layout, and manufacturing of

electronic circuits on printed circuit boards, and signal routing on semiconductor devices for LCDs.

11. As part of my work at Exponent, I have analyzed the design, manufacturing, and performance of such semiconductor devices and integrated circuits as microprocessors, flash memory, 3D integrated circuits, bipolar power transistors, insulated-gate bipolar transistors, photodetectors, photovoltaic cells, light-emitting diodes, and thin-film transistors for displays.

12. I have authored or co-authored eighteen articles, and presented at fourteen conferences and webinars on various topics in electrical engineering, including numerous papers and presentations concerning electrical wiring patterns and/or electrical testing. My CV lists these articles and presentations.

13. In summary, I have over two decades of experience in the field of electronic circuits, including those for LCDs.

14. I have been an expert witness in two patent cases, have provided expert consulting services for over 50 patent cases, have written dozens of expert reports and declarations, and have testified in district court once.

## **II. LEGAL PRINCIPLES**

15. I am not a lawyer and I do not provide any legal opinions in this Declaration. Although I am not a lawyer, I have been advised certain legal standards

are to be applied by technical experts in forming opinions regarding the meaning and patentability / validity of patent claims.

16. In forming my analysis, opinions and conclusions expressed in this Declaration, I have applied the legal principles set forth below which were provided to me by counsel for BOE.

**A. Independent and Dependent Claims**

17. I understand that there are two types of patent claims: “independent” and “dependent claims.” I understand that independent claims include only the aspects stated in the independent claim. I further understand that a claim in dependent form shall contain a reference to a claim previously set forth (which previously set forth claim can be an independent or a dependent claim) and then specify a further limitation of the subject matter claimed. I understand that a claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

**B. Prior Art**

18. I understand that the Patent Act defines various categories of prior art.

19. For example, I understand that pre-AIA 35 U.S.C. §102(b) states that a “person shall be entitled to a patent unless . . . the invention was patented or described in a printed publication in this or a foreign country ... more than one year prior to the date of the application for patent in the United States.” I also understand

that pre-AIA 35 U.S.C. §119(a) states that “no patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country.” I understand that the actual filing date of the United States application leading to the ’146 patent (Application Serial No. 10/914,044) was August 6, 2004.

20. As another category of prior art, I understand that pre-AIA 35 U.S.C. §102(a) states that a “person shall be entitled to a patent unless . . . the invention was . . . patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.”

21. I further understand that pre-AIA 35 U.S.C. §102(e)(1) states that a “person shall be entitled to a patent unless . . . the invention was described in . . . an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent.”

22. For purposes of this Declaration, I have been instructed to assume that the invention date of all claims of the ’020 Patent was December 3, 2009 (based on the date of an alleged “priority” application that the original owner of the ’020 Patent filed in Japan).

23. I also understand that there can be applicant admitted prior art (“AAPA”) based on statements in the specification (*e.g.*, describing technology as

“known”) or based on the applicant’s similar statements made during prosecution. I understand that the United States Court of Appeals for the Federal Circuit (“Federal Circuit”) has held that such admissions are binding on the applicant and patentee for determinations of anticipation and obviousness. I also understand that the Federal Circuit has held that AAPA can be important evidence of general background knowledge, and general knowledge can be used to supply a missing claim limitation. I further understand that the Federal Circuit has held that permissible uses for general background knowledge in an IPR include, for example, furnishing a motivation to combine prior art references, or supplying a missing claim limitation.

**C. Anticipation and Obviousness**

24. I understand that a claim is not patentable if it is anticipated or obvious. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in a single prior art reference. In this Declaration I am not setting forth any opinions that any claims of the ’020 Patent are unpatentable due to anticipation.

25. I further understand that obviousness of a claim requires that the claim be obvious from the perspective of a person of ordinary skill in the art (“POSITA”) at the time the invention of the challenged patent claim was made. Again, I have been instructed to assume that the invention date of all claims of the ’020 Patent was December 3, 2009.

26. I understand that to prove that prior art or a combination of prior art renders a patent claim obvious, it is necessary to: identify the particular reference that, alone or in combination with others, renders the claim obvious; specifically identify which elements of the claim are disclosed by one or more of the asserted references; and explain why a POSITA would have combined the teachings of the references, and how they would have done so, to create the inventions in the challenged patent claim.

27. I understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try”—choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and
- some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

28. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second prior art reference can be explicit or implicit, and may provide further evidence of obviousness.

29. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective)

considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant to the obviousness or non-obviousness of the claim. I am not currently aware of any such evidence for the claims of the '020 Patent and reserve my right to review and respond to such evidence if any is presented.

**D. Claim Construction**

30. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms. I also understand that the words of the claims should be interpreted as they would have

been interpreted by a POSITA at the time the alleged invention was made (not today). I have used the date of December 3, 2009 for reasons explained above.

### **III. BASIS FOR MY OPINIONS**

31. In forming my opinions, I have considered the '020 Patent (including the specification's written description of the invention, all of the figures, and all of claims) along with the prosecution history. I understand that the prosecution history is the written record with the U.S. Patent Office. I have also considered the exhibits to BOE's Petition, as well as any additional materials identified in this Declaration, plus my own experience and expertise as a skilled artisan in the relevant art at the time of the invention.

### **IV. SUMMARY OF MY OPINIONS**

32. I have been asked to consider whether claims 1-13 of the '020 Patent are rendered obvious by certain prior art references. Based on the analysis set forth herein, including my experience and knowledge in the field, my understanding of the claims, the prior art, the applicable law, and the level of skill in art in the relevant timeframe, it is my opinion that claims 1-13 are obvious for the reasons set forth herein.

### **V. LEVEL OF ORDINARY SKILL IN THE ART AT THE TIME OF THE ALLEGED INVENTION**

33. The relevant time for assessing the level of skill of the hypothetical person of ordinary skill in the art ("POSITA") is the December 3, 2009 filing date

of the earliest alleged priority Japanese application. To assess the level of ordinary skill in the art at that time, I understand that one should consider factors such as the educational level of the inventor; the type of problems encountered in the art; prior art solutions to those problems; the rapidity with which innovations are made; the sophistication of the technology; and the educational level of active workers in the field.

34. Considering these factors, it is my opinion that, as of December 3, 2009, a POSITA had at least: i) a B.S. in electrical engineering, physics, or a related subject and two plus years of experience working in the field of LCD displays; ii) an M.S. degree in the aforementioned subjects, and at least 1 year of experience in the design/development of LCD displays; or iii) a Ph.D. in the aforementioned subjects, and at least some experience in the area of LCD displays. Additional education may substitute for professional experience, and significant work experience may substitute for formal education.

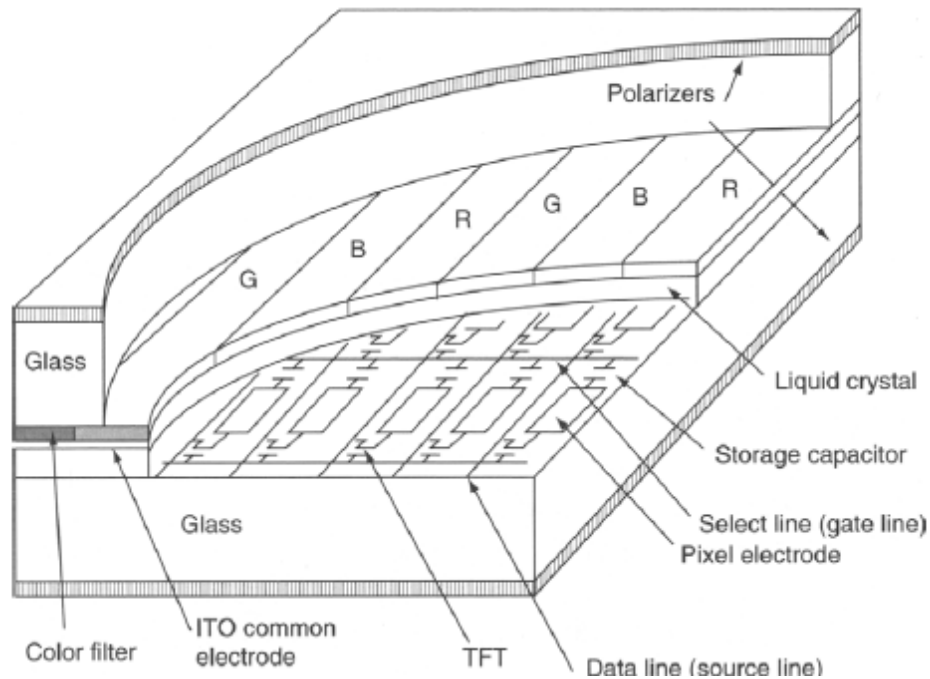
35. I met the definition of a POSITA in the relevant time frame. I render my opinions concerning the '020 Patent and the prior art from the perspective of a POSITA, based on my knowledge and research experience.

## **VI. TECHNOLOGY OVERVIEW**

36. Below, I provide a brief summary of the background technology as context for understanding the disclosure and claims of the '020 Patent.

## A. LCDs

37. A diagram of a typical liquid crystal panel is shown below:



(den Boer, Fig. 3.1.) A liquid crystal panel is generally comprised of multiple layers including two glass panels with liquid crystal disposed between them. The liquid crystal is confined to a display region, which is divided into pixels or subpixels, in the case of a color LCD.

38. A liquid crystal panel functions by the excitation of the liquid crystal. The liquid crystal molecules rotate when an electric field is applied to each pixel by transparent pixel electrodes formed on the bottom glass panel. The state of rotation of the liquid crystal molecules affects the polarization of light passing through the liquid crystal layer and, therefore, the amount of light passing through polarizers

placed on either side of the glass panels. Collectively, the light passed through the pixels forms an image.

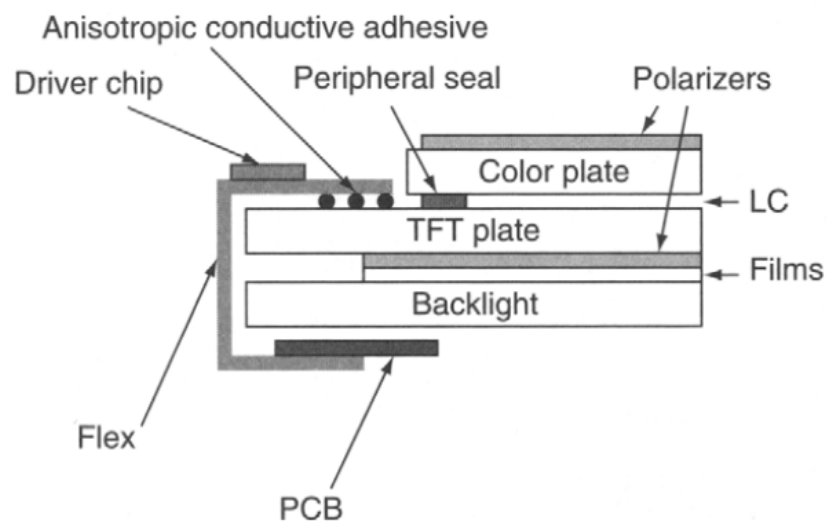
39. The transmission of light is controlled by signals from driver circuitry. In an active-matrix LCD, driver signals control pixel circuits formed on the bottom glass panel. The pixel circuits typically include thin film transistors (“TFT”), storage capacitors, and the pixel electrodes.

40. There are generally two types of driver signals: one that sequentially activates rows of pixels, and another that carries image information for each pixel within a row. Specifically, scanning signals activate pixel circuit TFTs one row at a time and typically flow along horizontal lines called select lines, gate lines, scan lines or scanning lines. Data or video signals carry color and brightness information for each pixel and typically flow along vertical lines called data lines, image lines, or drain lines.

41. Other names for these wiring lines include lines, wirings, conductors, traces or circuit traces. They are electrically conductive circuit paths formed on the glass panel. The wiring lines are connected to driving circuitry that may be provided either on the glass panel or externally. In the former case, the driving circuitry is located on the glass panels but outside of the display region.

42. In the latter case, the wiring lines are connected to terminals, also called electrodes or pads, provided on the glass panel. These terminals, in turn, are

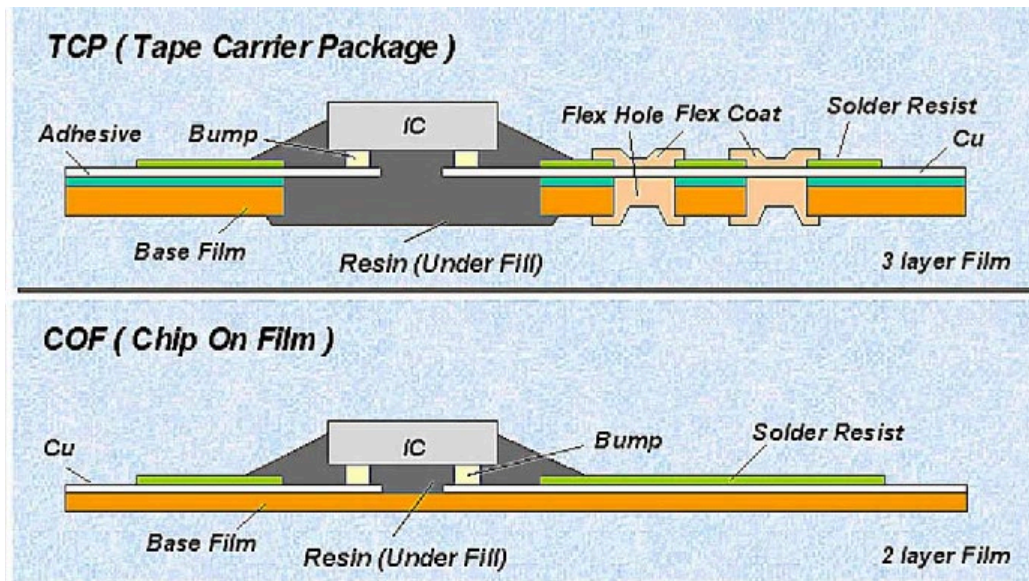
electrically connected to corresponding terminals on an external element carrying the driving circuitry. For example, the external element carrying driving circuitry could be a substrate mounting an integrated circuit (“IC”) or chip. As shown in the cross-sectional diagram of a liquid crystal device below, a driver chip is mounted on a flex, also known as a flexible substrate, flexible printed circuit (“FPC”), base film or tape, and the flex is connected to an LCD glass panel (“TFT plate”) and a printed circuit board (“PCB”):



(den Boer, Fig. 3.2.)

43. The assembly of a chip mounted on a type of flexible substrate is commonly known as a chip on flex (“COF”), chip on film, chip on FPC, or, in earlier forms, a tape carrier package (“TCP”). (Watanabe, 240-241). The process of attaching the flexible substrate to the panel glass is often called tape automated bonding (“TAB”), however, the substrate itself is sometimes referred to as a TAB.

(See den Boer, 49-50; Takemura, [0002]-[0004]). As shown below, for both TCP and COF, the driver IC is mounted on the flexible substrate and the electrical leads of the IC are connected via solder bumps to electrically conductive paths, i.e., wiring lines, depicted as a copper layer on the flexible substrate:

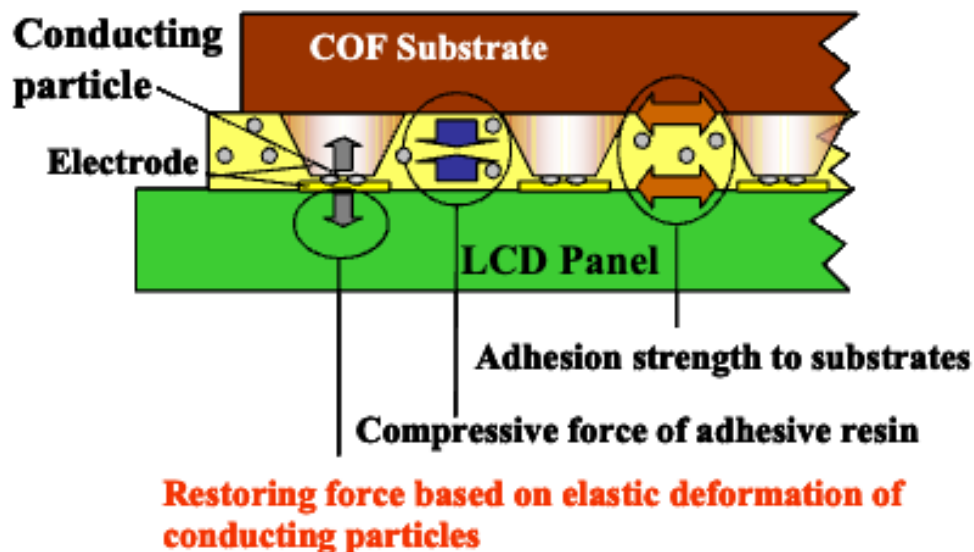


(Chen 2008, Fig. 1.)

44. Referring again to the cross-sectional diagram of a liquid crystal device, anisotropic conductive adhesive material (“anisotropic conductive film” or “ACF”) is disposed between the flexible substrate and glass panel, outside the display region. The ACF enables driver signals to pass from the driver IC to the wiring lines on the glass panel. (den Boer, 49-50, 77-78.)

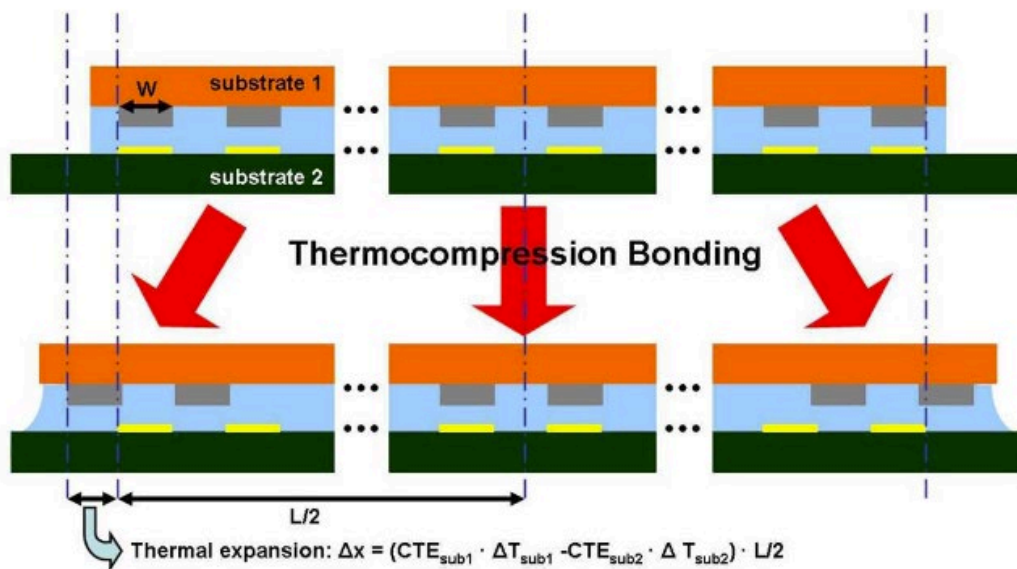
45. The process of forming the electro-mechanical connection between the glass panel and flexible substrate is called bonding. During bonding, the ACF is applied between the terminals of the glass panel and the corresponding terminals of

the flexible substrate. The groups of terminals then are aligned with each other before heat and pressure is applied. As shown below, conductive particles suspended within the ACF are compressed during bonding, creating an electrical connection between corresponding terminals of the glass panel and flexible substrate. (den Boer, 77-78.; Watanabe, 240, Fig. 1.) At the same time, the ACF electrically insulates adjacent pairs of terminals:



(den Boer, 77-78.; Watanabe, Fig. 1.)

46. The heat applied during bonding can cause thermal expansion of both the glass panel and flexible substrate. Because they have different coefficients of thermal expansion, this can lead to misalignment of the glass panel terminals with the flexible substrate terminals. As shown below, terminal misalignment will tend to be greatest at the terminals furthest from the center of the terminal group, such that this effect is more pronounced for smaller terminal group widths.



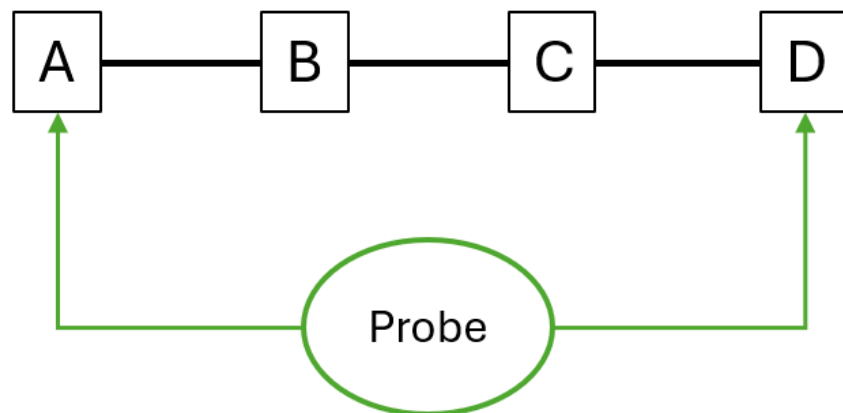
(Govaerts, Fig. 2.) Misalignment of terminals during bonding, inadequate temperature, pressure, or processing duration, or issues with the ACF material can lead to excessive electrical resistance or a failure to make an electrical connection at the affected terminals.

## B. Electrical Connectivity Testing

47. A method for identifying whether two components are electrically connected is to measure the resistance of the connection with a tool such as a multimeter. If the components are electrically connected, current will flow between them along a circuit path with a stable and typically low resistance value as determined by the properties of the conductor and connection. If there is no electrical connection between the components, no current will flow between them and the measured resistance will be, for practical purposes, infinite. In some cases, an electrical connection will be present but not as sound as is required or expected,

such as in the case of a faulty solder joint. This is indicated by a fluctuating measured resistance, or by a resistance that is much higher than would be expected based on the material properties of the conductor.

48. Two components may be separated by multiple points, as illustrated below. If a low resistance is measured, for instance, between component A and D, one can reasonably assume that the connection points between the two components (i.e., from A to B, B to C, and C to D) are low resistance. However, if the measured resistance indicates a faulty connection, more testing would be required to determine which connection point has failed.



### **C. Test and Inspection of ACF Bonding**

49. Bonding the flexible substrate terminals to the glass panel terminals is part of the back-end processes of LCD manufacturing. Bonding is performed after the pixel circuits and other circuitry have been created, and the liquid crystal cells have been filled with liquid crystal material between the LCD panels. (Minami, 64; Souk, 5.1.)

50. The quality of the electrical connection between the flexible substrate and glass panel may be assessed through in-line optical or electrical tests. Optical inspections are known to have several limitations, including the inability of imaging equipment to capture the ACF's conductive particles at a sufficiently high resolution for a human or image processing algorithm to determine the quantity and degree of deformation of the particles. (See Ni, 103109-6 - 7; Lin, 294.) Another factor that one must account for with optical inspections is the difference between ACFs that use rigid or soft particles because they deform differently during bonding. (See Ni, 103109-2.) Furthermore, optical inspections may not be feasible if the terminal materials are not transparent.

51. These limitations do not apply to electrical connectivity tests in determining the viability of an ACF bond, however, electrical tests come with their own limitations. It is generally preferable to avoid contacting electrical probes to the LCD panel itself in order to limit introduction of foreign particles and to avoid physical and electrical damage to the circuitry on the glass panel, for example, by electrostatic discharge. (See Murakami, 99-100; Li, 3.) Moreover, the bonded terminals are often not directly accessible by a probe because they face each other and are surrounded by residual ACF. (Watanabe, Fig. 1.) Any electrical probing of the bonded terminals should instead be performed through electrical traces. It is

52. Indeed, these motivating factors led to the creation of several strategies – prior to the '020 Patent's invention date – for testing the state of electrical connectivity between a liquid crystal panel and an FPC using external terminals. For example, as shown below, parallel leads on the FPC may be short-circuited where the panel and FPC meet such that current may flow through the leads as a circuit path when the connection is sound:

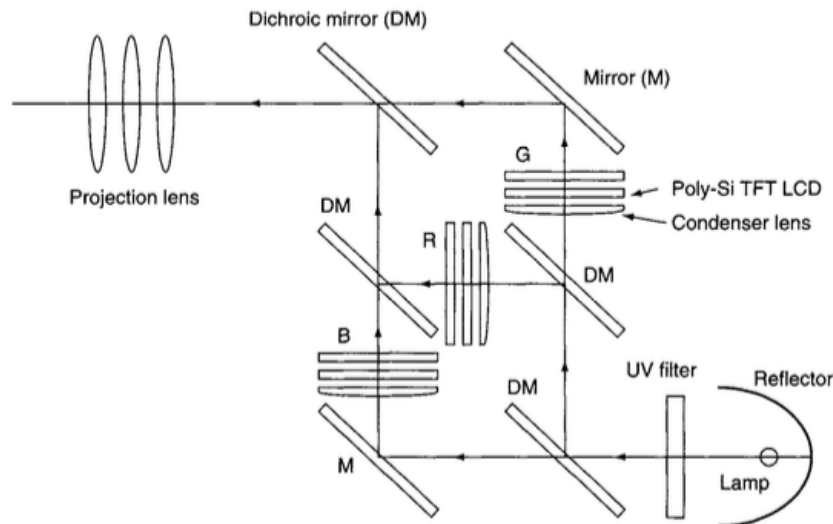
(Wakita, [0038]-[0043], Figs 1-3.)

53. As detailed in Sections IX.A and IX.C, Takenaka and Takemura disclose similar methods of applying a voltage across external terminals connected to circuit paths that traverse an FPC and LCD display.

**D. LCD Panel Implementations**

54. LCD panels can be implemented in a number of ways, depending on their display configuration. A common configuration is a transmissive LCD display that uses a backlight as the light source. (den Boer, 105.) In contrast, reflective LCD displays rely on reflected ambient light rather than a backlight, and transfective LCD displays operate in a reflective mode under high ambient lighting conditions and operate in transmissive mode in low ambient lighting conditions. (den Boer, 182-84.)

55. LCD panels can also be used in projection displays. One common configuration, shown below, is to use dichroic mirrors to separate white light from a projection lamp into the three primary colors and use three transmissive TFT LCD panels to create the image for each color:



(den Boer, Fig 8.16, 214-20.) The combined image is then projected onto a screen.

## VII. THE '020 PATENT

56. The '020 Patent is titled, “Electro-optical device, electro-optical panel, and electronic apparatus,” and issued on March 5, 2013 to Seiko Epson Corporation. (Ex. 1001 at Cover).

### A. Specification

57. The '020 Patent relates to LCD panels and electro-optical devices comprising such panels, i.e., LCD devices. (Ex. 1001 at 1:7-15.) Additionally, the '020 Patent relates to electronic apparatuses comprising such electro-optical devices, e.g., liquid crystal projectors. (Ex. 1001 at 21:6-9, Fig. 17.)

### B. Alleged Problem

58. The '020 Patent identifies a change in the manufacturing process for LCD devices that creates a problem with quality control checks. (Ex. 1001 at 1:24-42.)

59. The specification discloses that LCD devices typically comprise three elements: an external driving circuit, an LCD panel and a plurality of flexible substrates used as a bridge between the external driving circuit and the LCD panel. (Ex. 1001 at 1:11-14.) These elements are connected via terminals provided on the LCD panel and corresponding terminals on the flexible substrates. (Ex. 1001 at 1:14-19.) The terminals are pressed together with ACF between them. (Ex. 1001 at 1:16-23.) Some of these electrically connected terminals are used to provide a constant potential (“LCCOM”), a reference voltage signal, to the pixels of the panel. (Ex. 1001 at 19:32-37.)

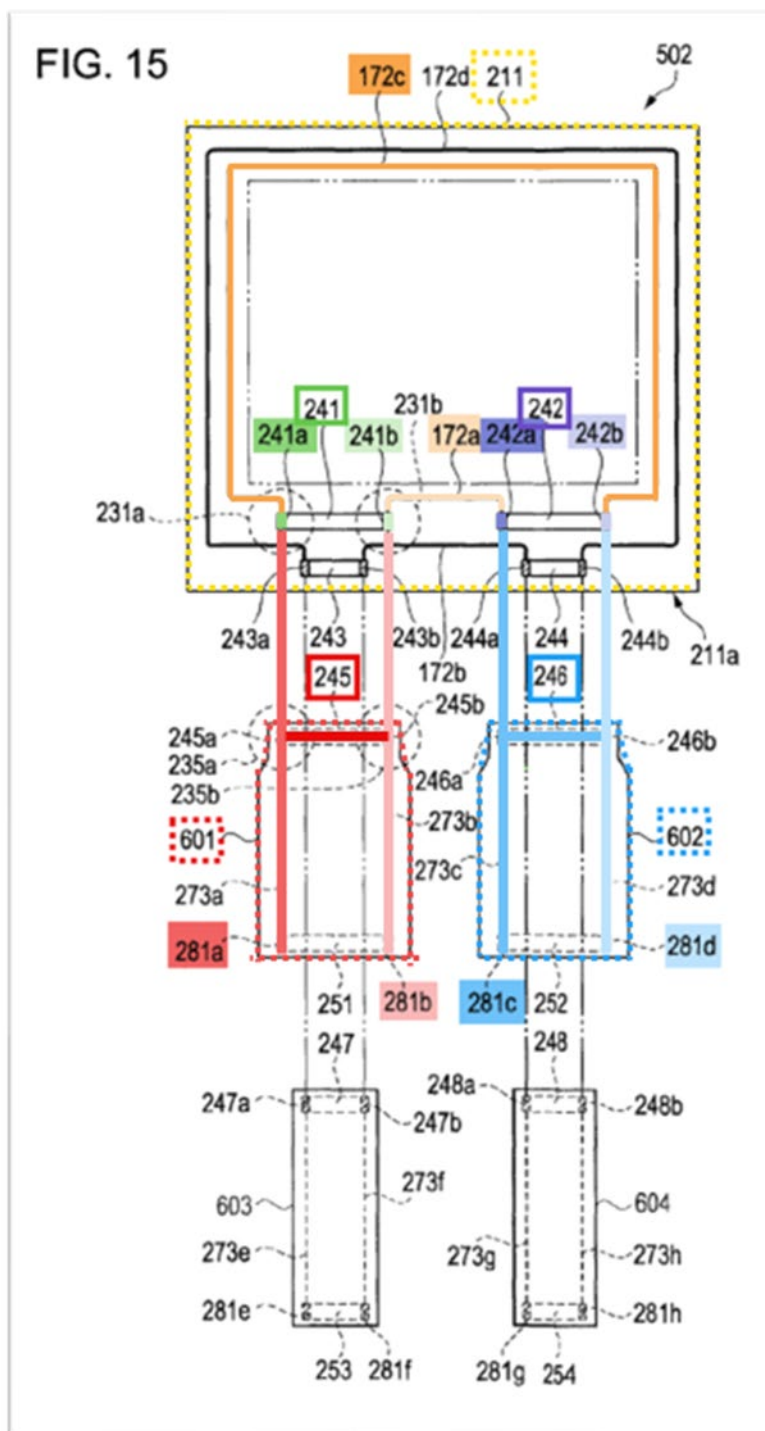
60. One type of conductive particle used in the ACF is a ball of nickel. (Ex. 1001 at 1:27-28.) When the balls of nickel are compressed during the connection process, they leave “particle marks” that one may observe when inspecting the quality of the electrical connection. (Ex. 1001 at 1:24-28.)

61. Plastic balls plated with metal replaced solid balls of nickel as the conductive particles used in the ACF. (Ex. 1001 at 1:27-31.) However, the ’020 Patent states that when the plastic balls are compressed during the connection process, they do not leave “particle marks” required for visual inspection purposes. (Ex. 1001 at 1:32-35.) Thus, there is allegedly no method of checking the connection between the LCD panel and flexible substrates beside turning on the LCD device. (Ex. 1001 at 1:35-42.)

### **C. Alleged Invention**

62. The '020 Patent's solution to the above-identified problem is to electrically connect the LCD panel's terminals together. (Ex. 1001 at 1:46-2:6.) The connection between the LCD panel and the flexible substrates may then be performed by measuring the resistance value between external terminals: if "electricity flows" between the terminals then the liquid crystal panel and the flexible substrate are connected. (Ex. 1001 at 2:7-19, 13:5-17.)

63. For example, Figure 15 shows one embodiment of the claimed LCD device:



(Ex. 1001 at 1:46-2:6, 16:15-26, Fig. 15 (annotated).) LCD device (502) comprises a panel (211) and flexible substrates (601) and (602). (Ex. 1001 at 16:27-31, 16:34-38.) The external driving circuit is not shown. Terminal portions (241) and (242)

are provided on LCD panel (211), corresponding terminal portions (245) and (246) are provided on flexible substrates (601) and (602), and the groups of terminals of those terminal portions are connected together through an anisotropic conductive film. (Ex. 1001 at 16:52-58, 17:5-10.) Flexible substrates (601) and (602) also have external terminals (281a) and (281b), and (281c) and (281d), respectively, on the ends that would be connected to the external driving circuit. (Ex. 1001 at 17:48-61.) Several connection wirings (172a) and (172c) are provided on LCD panel (211), connecting panel terminals (241a) and (242b), and (241b) and (242a) of terminal portions (241) and (242).

64. The connection between these elements is tested by measuring the resistance value between external terminals, e.g., (281a) and (281d) via constant potential LCD panel terminals (241a) and (242b): if “electricity flows” between the terminals then the liquid crystal panel and the flexible substrate are connected. (Ex. 1001 at 2:7-19, 13:5-17, 19:32-37.) If the circuit paths are confirmed, it is determined that LCD panel (211) and flexible substrates (601) and (602) are electrically connected. (Ex. 1001 at 18:20-23.)

#### **D. Prosecution History**

65. On December 1, 2010, Seiko Epson Corporation filed U.S. Application No. 12/958,154 (the “’154 Application”). (Ex. 1003 at 2.) The ’154 Application claims priority to Japanese Patent Application No. 2009-275218, filed on December

3, 2009, and Japanese Patent Application No. 2010-214838, filed on September 27, 2010. (*Id.* at 4.) In the same filing, Seiko Epson Corporation filed an Information Disclosure Statement citing a single Japanese patent. (*Id.* at 106.)

66. On October 31, 2012, without issuing any substantive Office Actions, the Examiner mailed a Notice of Allowance for the '154 Application. (*Id.* at 233-246.) The Examiner did not cite any additional prior art or analyze the single Japanese patent that Seiko Epson Corporation cited. (*Id.*) On March 5, 2013, the '154 Application issued as the '020 Patent. (*Id.* at 253.)

## VIII. CLAIM CONSTRUCTION

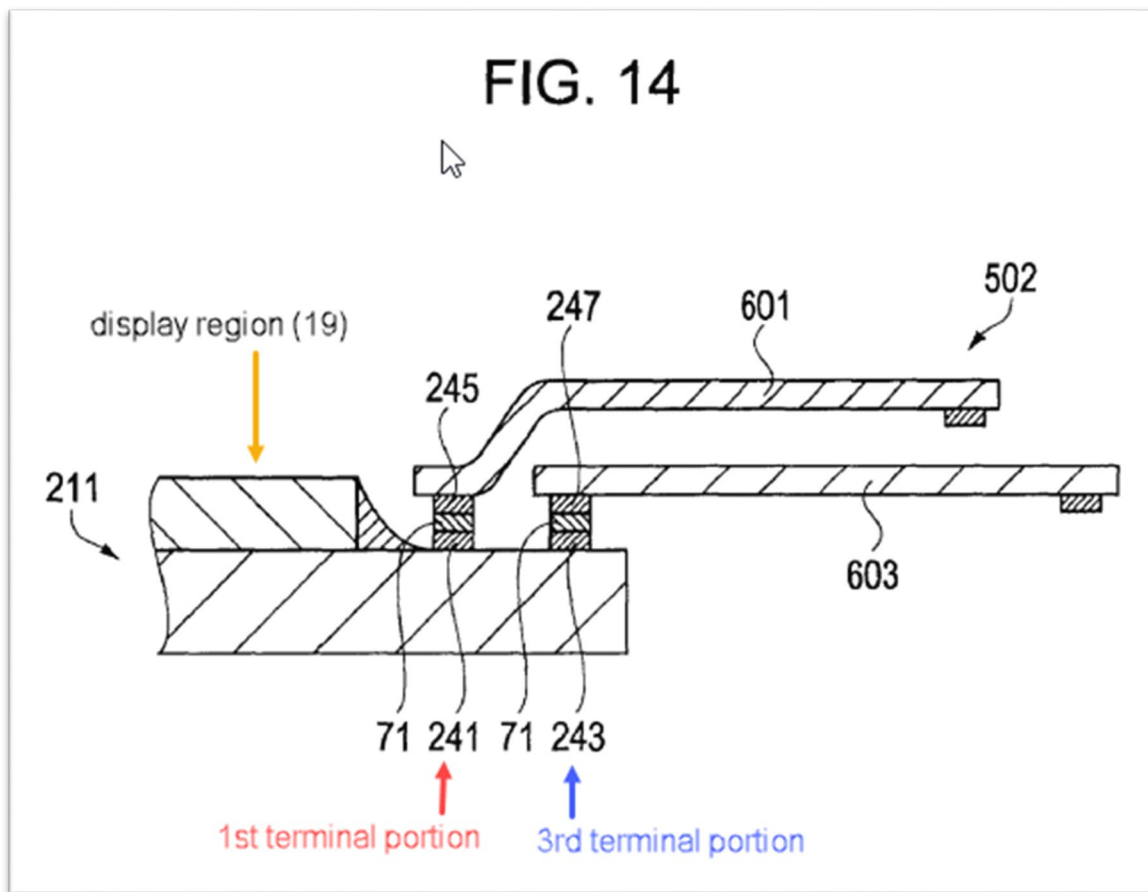
67. I have been asked to use the plain-and-ordinary meaning of each of the claim terms for purposes of my analysis. Below, I address the plain-and-ordinary meaning of two terms to aid the Board's review. However, I reserve the right to respond to any constructions that Patent Owner may offer or that may be adopted by the Board.

### A. **“arranged on a side opposed to a display region with respect to the first terminal portion” (Claim 8)**

68. In my opinion, a POSITA at the time of the '020 Patent's filing would have understood the term “arranged on a side opposed to a display region with respect to the first terminal portion” to mean “arranged on an opposite side of the first terminal portion from the display region.”

69. First, Claim 8 makes clear that the third terminal portion and display region are arranged relative to the first terminal portion. ('020 Patent, cl. 8.) Specifically, they are arranged on opposing sides of the first terminal portion or, in other words, one on one side and one on an opposite side. ('020 Patent, cl. 8.)

70. Second, the specification confirms that the third terminal portion is arranged on the other side of the first terminal portion as the display region. ('020 Patent, 16:34-42, Figs. 13-15.) Figure 13 and Figure 14 (a cross-sectional view of the liquid crystal device shown in Figure 13) shows an embodiment with the claimed arrangement, where the display region (19) is on one side of the first terminal portion (241), and the third terminal portion (243) is arranged on the other side as the display region:



(’020 Patent, Fig. 14 (annotated).)

**B. “connection wiring” (Claims 1, 2, 5, 6, 8, 9 and 11)**

71. In my opinion, a POSITA at the time of the ’020 Patent’s filing would have understood the term “connection wiring” to mean “circuit path”.

72. The ’020 Patent explains that the connection between the LCD panel and flexible substrates is checked by measuring the resistance value between external terminals: if “electricity flows” between the terminals then the liquid crystal panel and the flexible substrate are connected. (’020 Patent, 13:5-17, 19:32-34.) This is only possible if there is a circuit path that links the terminals.

73. Furthermore, the '020 Patent suggests that a “wiring” is not limited to a physical wire, a single wire, multiple wires tied together, or a wire on a single layer. First, the structure of a flexible substrate carrying an integrated circuit chip is described as a “*wiring substrate*” that has a “*wiring patterned and formed* on the base.” ('020 Patent, 7:31-39.) Another name synonymous with flexible substrates carrying integrated circuit chips is “flexible printed *circuits*.” (See, e.g., Wakita, [0003].) Such devices do not generally have loose physical wires but rather circuit paths fixed on the surfaces or within the flexible substrate. (See, e.g., Uchiyama, 3:47-50.) Moreover, the circuits paths of these flexible substrates may pass between different layers. (See Uchiyama, Fig. 1)

74. Second, connection wirings are described as being able to “creep between the layers [of the LCD panel] using contact holes so as to connect different panel terminals.” ('020 Patent, 23:39-40.) Connection wirings are also described as being in some cases “connected over the layers laminated on the device substrate 12 without obstruction of the other wirings (for example, the data lines and the like).” ('020 Patent, 19:50-53.) Contact holes and laminated layers are characteristic of circuit paths, not of physical wires. This confirms that a “wiring” is not limited to a physical wire, a single wire, multiple wires tied together or a wire on a single layer.

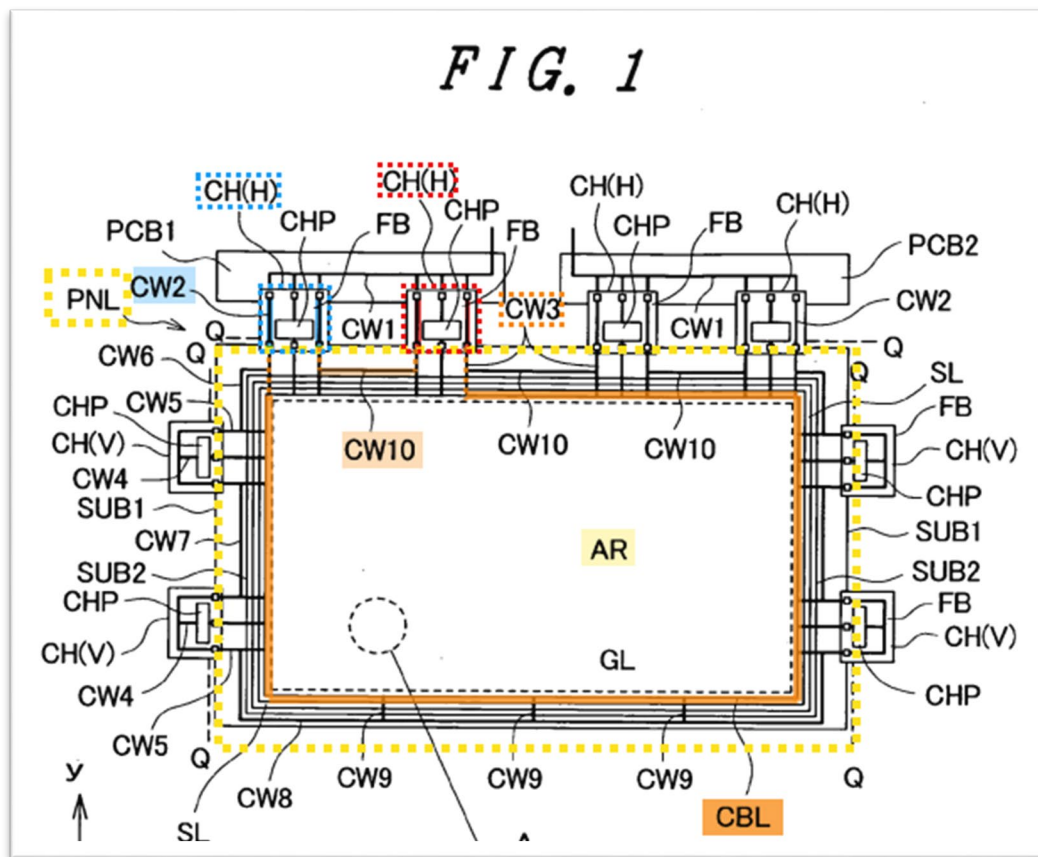
## **IX. STATE OF THE ART**

75. The '020 Patent discloses only conventional features that were well known in the industry long before the alleged December 3, 2009 invention date.

**A. Takenaka**

76. Takenaka relates to a liquid-crystal display device where a reference voltage signal is provided to the display panel through a “multiplicity of distributed supply paths.” (Takenaka at Abstract, [0014].) Specifically, the multiplicity of distributed supply paths comprise common lines that are provided on tape-carrier-schemed semiconductor devices connected to the panel, as well as a common bus line formed around the circumference of the panel. (Takenaka at Abstract, Fig. 1.) Takenaka discloses that this arrangement of wirings stabilizes the reference voltage signal provided to the panel’s pixels such that the size of the panel can be increased and picture quality is improved. (Takenaka at [0011] - [0013].)

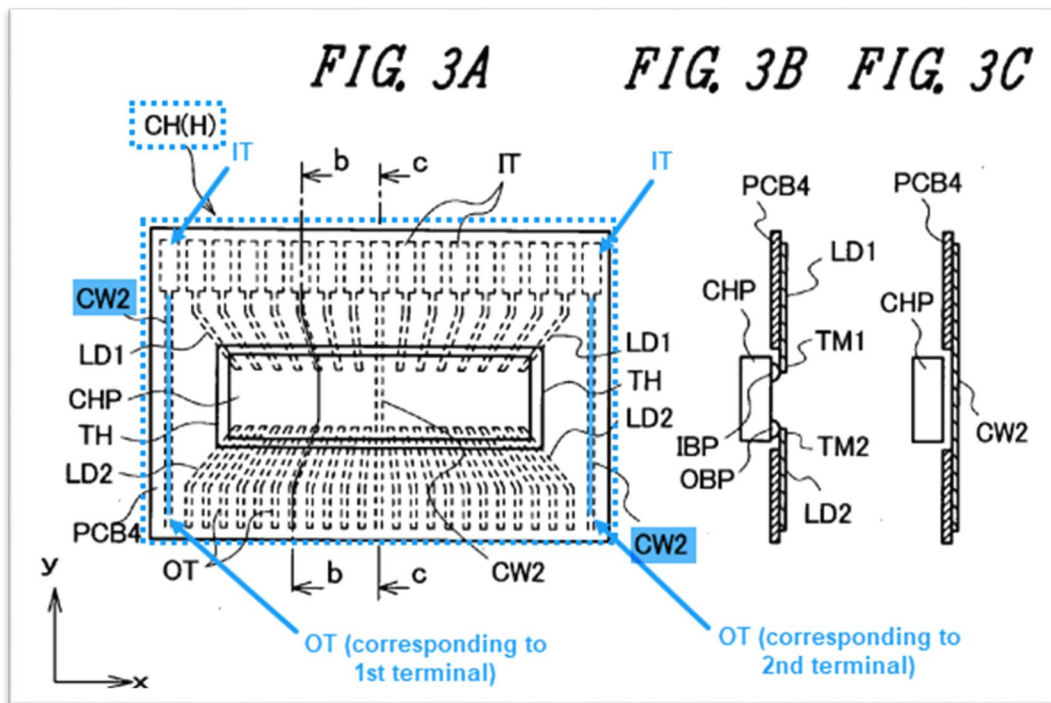
77. Figure 1 illustrates a preferred embodiment for the liquid-crystal display device of the claimed invention:



(Takenaka at [0025], Fig. 1 (annotated).) The liquid-crystal display panel (PNL) is connected on three sides to semiconductor devices (CH(H) and CH(V)) that respectively supply video signals and scanning signals to the panel's pixels. (Takenaka at [0026], [0027], [0040].) The semiconductor devices also pass the reference voltage signal through common wires (CW2). (Takenaka at [0056].) These common wires are connected to common wires (CW3) formed on the panel at terminals that are illustrated as small square boxes. (Takenaka at [0056].) In turn, these common wires (CW3) are connected to other common wires (CW10) and the

common bus line (CBL), which surrounds the panel's display area (AR). (Takenaka at [0037], [0058], [0070].)

78. Figures 3A-C show a detailed view of a semiconductor device of the preferred invention:

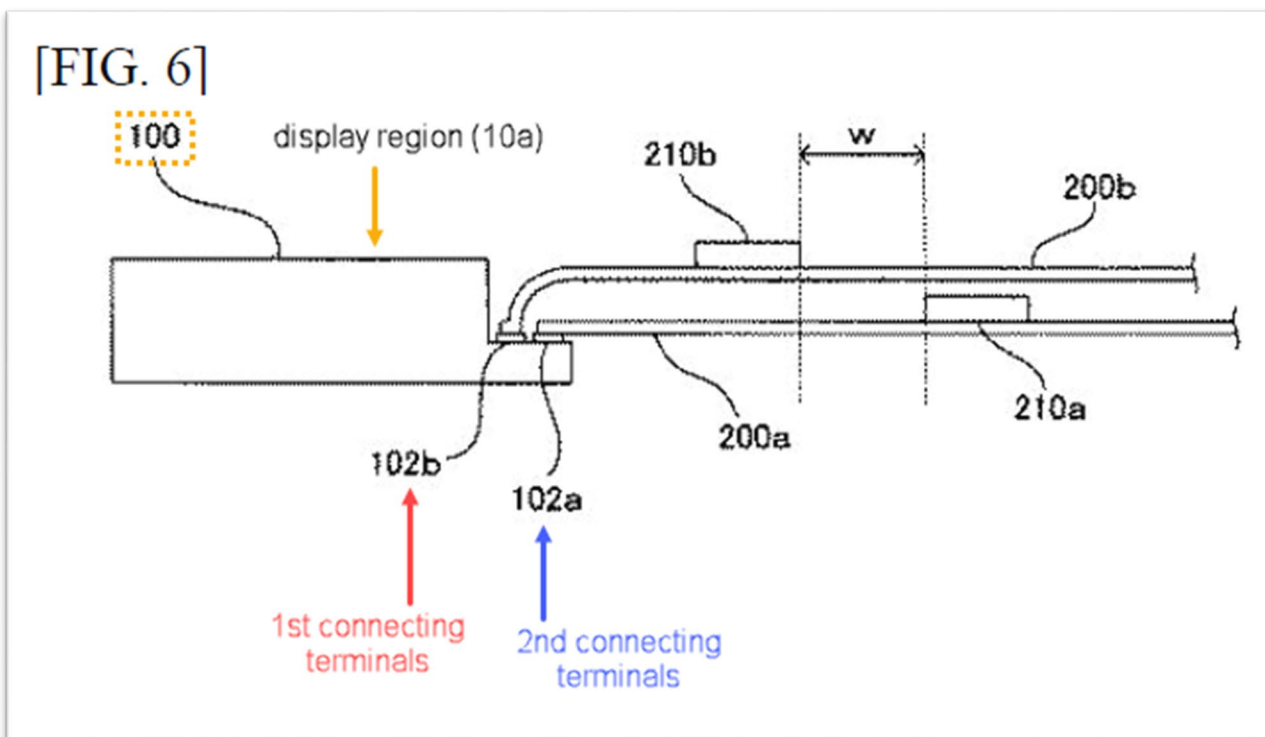


79. (Takenaka at [0075], Figs. 3A-C (annotated).) The semiconductor device (CH(H)) comprises a chip mounted on a flexible circuit board (FB), with common wires (CW2) formed at the sides of the board. (Takenaka at [0076], [0081].) The ends of the common wires (CW2) are connected to an input terminal (IT) and an output terminal (OT), the latter of which are connected to corresponding terminals on the panel. (Takenaka at [0076], [0081], [0085].)

**B. Ito**

80. Ito relates to a liquid-crystal display device having flexible substrates that overlap with one another. (Ito at [0008].) Each of the substrates carry an integrated circuit for driving the liquid-crystal panel, but when the circuits are positioned close together in the substrates' overlapping configuration, this can concentrate heat and negatively affect reliability. (Ito at [0005].) Ito solves this problem by having offset integrated circuits. (Ito at [0007].)

81. Figure 6 shows the overlapping configuration of Ito's substrates (200a, 200b):

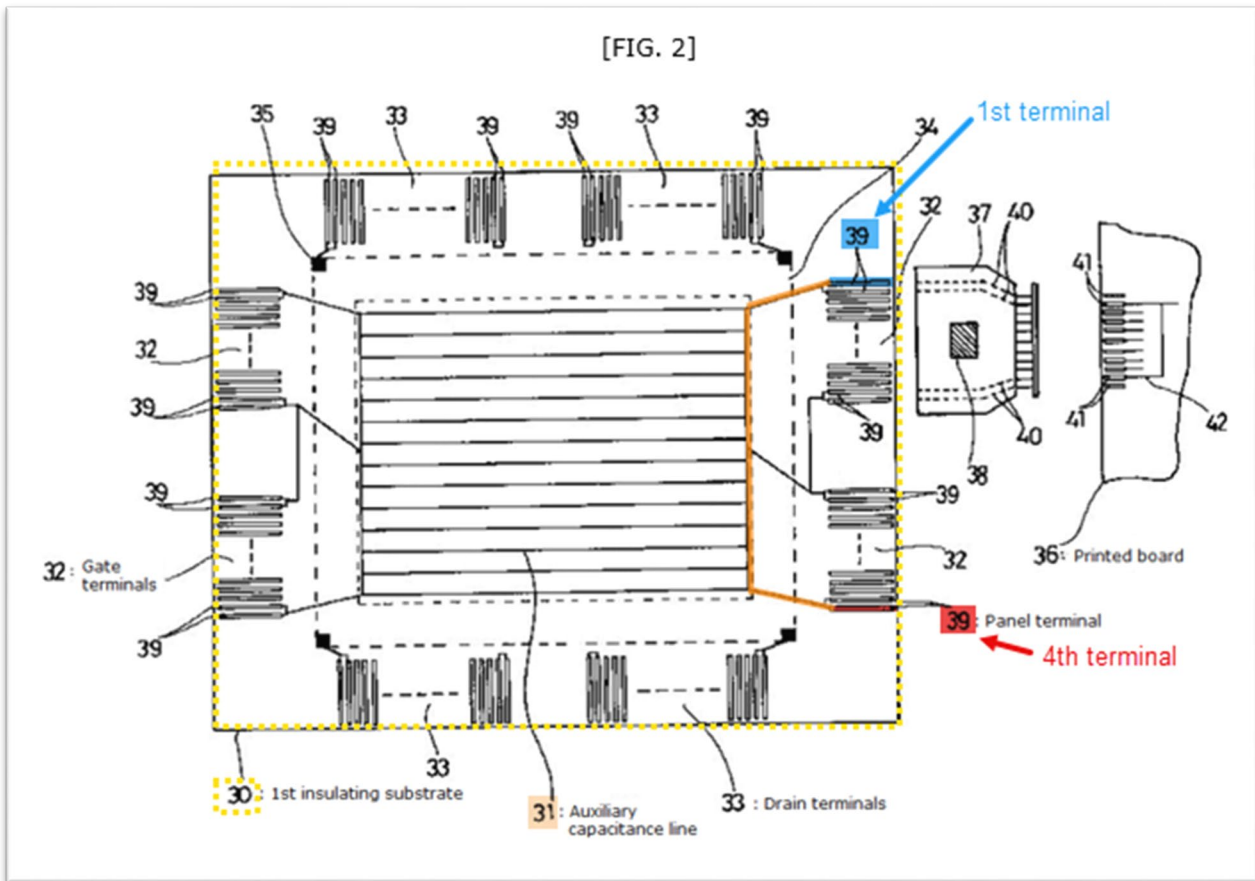


(Ito at [0036], Fig. 6 (annotated).) This configuration is achieved by electrically connecting the substrates (200a, 200b) to the two rows of panel terminals (102a, 102b). (Ito at [0036], Fig. 4.)

### **C. Takemura**

82. Takemura relates to a liquid-crystal display device configured such that terminal connection quality can be checked. (Takemura at [0001].) Takemura teaches that these quality checks are necessary because connections between an LCD panel and flexible substrates may be compromised during manufacturing. (Takemura at [0003], [0004].) For example, conductive metal balls in the ACF used for the connections may be insufficient when pressed, or the film may expand due to heat, causing the terminals to shift. (Takemura at [0004].)

83. To solve this problem, as shown in Figure 2 below, Takemura teaches a configuration where terminal groups (32) on the LCD panel have two short-circuited terminals (39) on each end, and these terminals are electrically connected to corresponding terminals on flexible substrates (37):



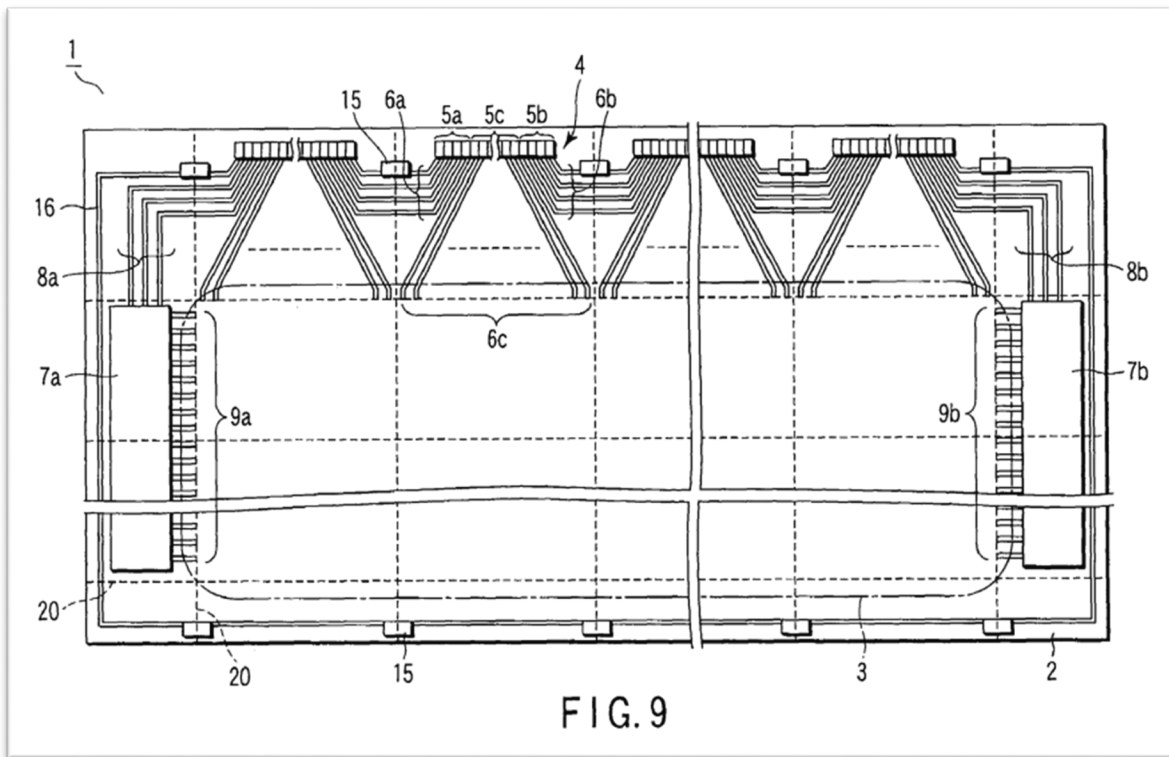
(Takemura at [0005], [0010], Fig. 2.) Terminals on the other ends of the flexible substrates are electrically connected to measurement terminals (41), whereby the resistance between the short-circuited terminals connections may be tested. (Takemura at [0005], [0011], Fig. 2.)

84. Additionally, Takemura teaches that the short-circuited panel terminals are connected to auxiliary capacitance lines (31). (Takemura at [0030], Fig. 2.) The lines may be used for further terminal connection measurements, or they can be used to provide a stable voltage. (Takemura at [0011], [0031].)

**D. Aoki**

85. Aoki is another patent that relates to electrically connected LCD panel terminals. Aoki discloses a liquid-crystal display device that is structured and segmented in such a way to reduce the number of unique patterns that must be formed during manufacturing in order to make the process simpler, quicker and result in a higher display quality. (Aoki at 1:36-51, 2:16-25.) Aoki teaches that if the structures in, for example, the connection portions along one side of the display are the same as one another, a fewer number of mask patterns are needed during the photolithography steps of the manufacturing process. (Aoki at 5:32-35, 5:54-6:18.)

86. Figure 9 illustrates a preferred embodiment for the liquid-crystal display device of the claimed invention:



(Aoki at 7:5-18, Fig. 9.) A plurality of connection portions (4) are arranged on the side of the display (1), with each comprising terminal groups (5a-c) and wiring line groups (6a-c). (Aoki at 4:1-4.) A terminal group (5a or 5b) of one connection portion (4) is connected to the corresponding terminal group (5b or 5a, respectively) of an adjacent connection portions (4) via a wiring line group (6a or 6b). (Aoki at 4:5-16, 7:5-9.) The terminal groups (5a-c) are also connected to wiring line groups formed on tape-carrier flexible substrates (not shown). (Aoki at 4:42, 47.) In this embodiment, there also exists a wiring line (16) surrounding the display region that acts as a common wiring line. (Aoki at 7:11-22.)

#### **E. Uchiyama**

87. Uchiyama relates to structures for electrically connecting multiple substrates of different types in various configurations to LCD panel terminals (Uchiyama at 3:32-37, 3:50-55, 1:12-2:37, 3:4-14).

88. Uchiyama discloses as related art Figure 91, Figure 92, and Figure 95 wherein the terminals (18) of an LCD panel (16) are electrically connected to the connection terminals (50046) of flexible TCP substrate (50042) by an ACF (50049) comprised of conductive particles (50050) and an adhesive agent (50051). Figure 91 of Uchiyama also shows output (50044) and input (50045) wiring lines on the flexible substrate electrically connected to the panel terminals via the flexible substrate terminals, including at least one wiring line on one side of the flexible substrate that is part of an electrical connection between the LCD panel and a third “bus” substrate (50043) (Uchiyama at 1:25-40, 1:55-58, Fig. 91, Fig. 92, Fig. 95).

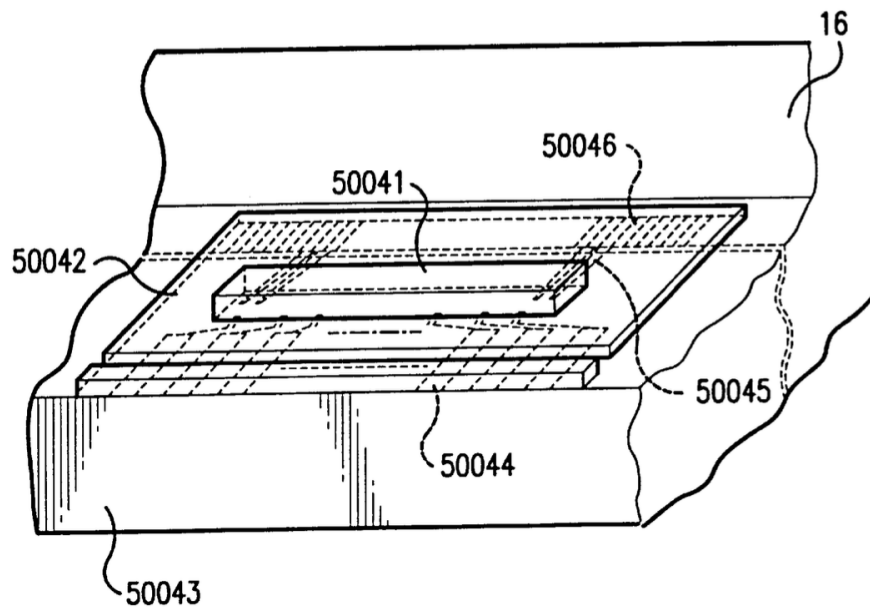


FIG. 91  
PRIOR ART

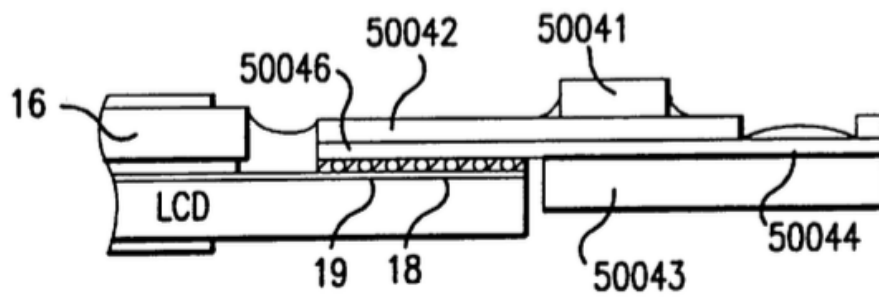


FIG. 92  
PRIOR ART

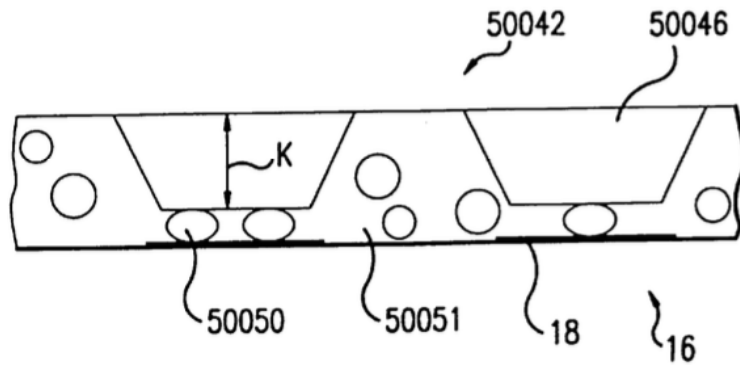


**FIG. 95**  
PRIOR ART

89. Uchiyama further discloses as related art Figure 99 which shows three TCPs “formed into three layers” and electrically connected to the LCD panel (110) and a “drive control substrate” (50155). (Uchiyama at 3:25-40, 2:23-37, Fig. 97, Fig. 98, Fig. 99).

## **X. GROUNDS**

90. I am informed by Counsel that claims 1-13 of the '020 Patent are challenged. As explained below, an element-by-element analysis demonstrates that these claims are taught or rendered obvious by the prior art.

### **A. Ground 1: Claims 1-7, 11 and 12 are Obvious over Takenaka**

91. In my opinion, claims 1-7, 11 and 12 would have been obvious in view of Takenaka to a person of ordinary skill at the time of the '020 Patent's filing. Specifically, and as explained in greater detail below, claims 1-7, 11 and 12 recite LCD devices and LCD panels having various configurations of connection wirings,

and it would have been obvious for a POSITA to arrive at the claimed configurations in view of Takenaka.

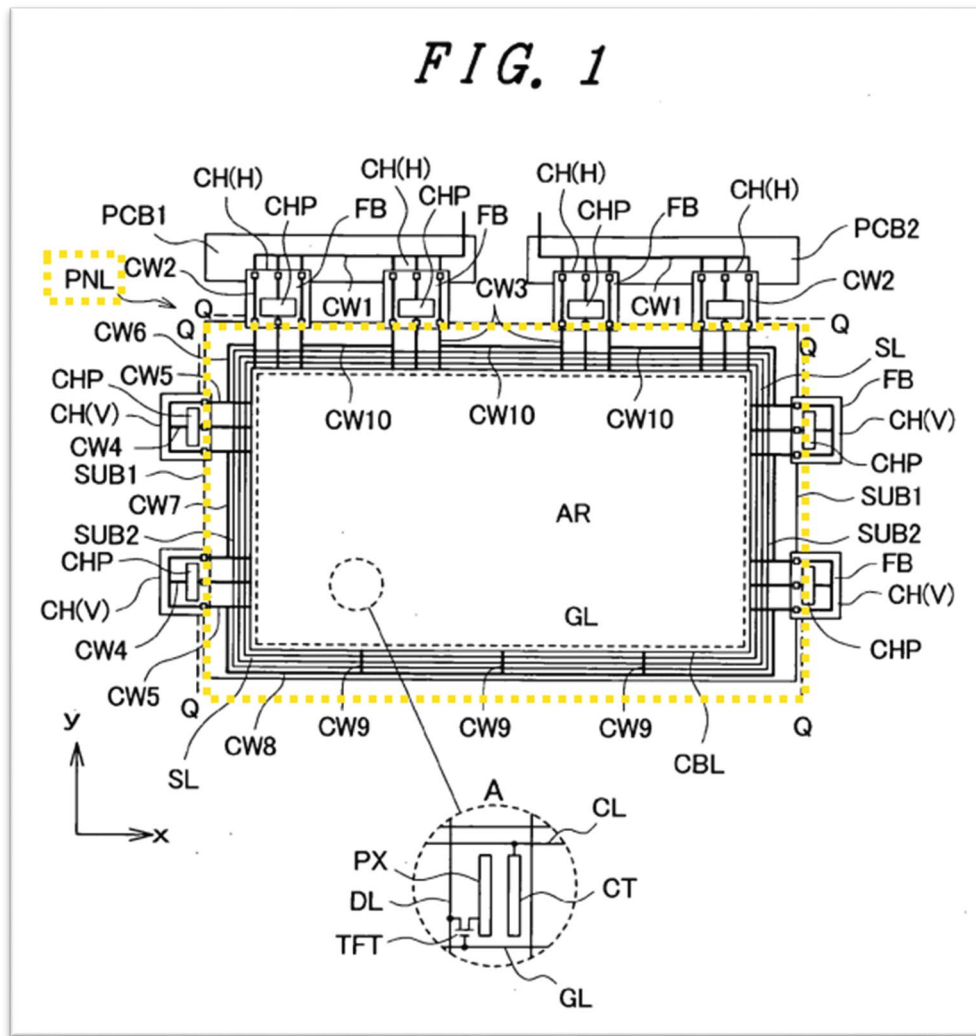
**1. Independent Claim 1**

*[1pre] “An electro-optical device comprising:”*

92. In my opinion, to the extent the preamble is limiting, it is taught by Takenaka. Takenaka discloses a “***liquid-crystal display device***[.]” (Takenaka at Abstract.) In my opinion, this limitation is met.

*[1a] “an electro-optical panel including:”*

93. In my opinion, Takenaka teaches this limitation. Takenaka discloses a “liquid-crystal display device [that] includes a ***liquid-crystal display panel***[.]” (Takenaka at Abstract.) The LCD panel (PNL) is shown in Figure 1 below:



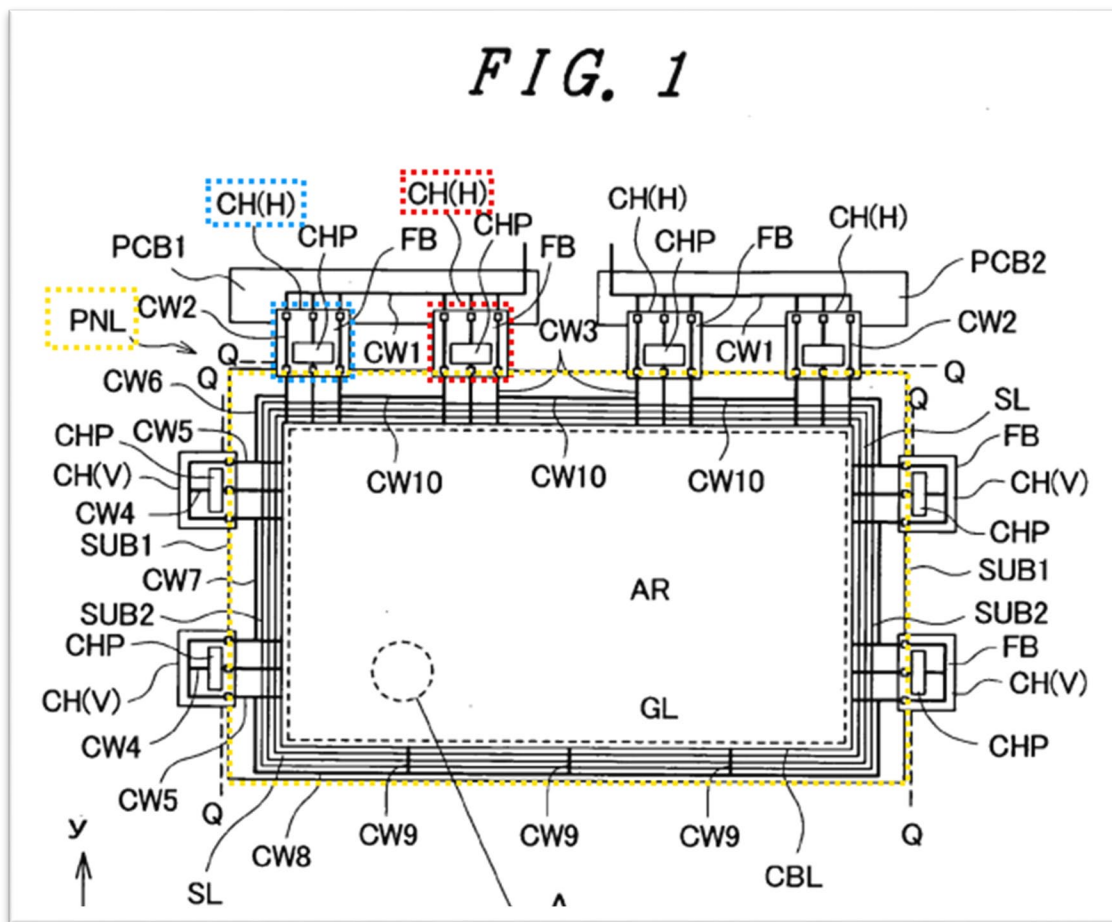
(Takenaka at [0026], Fig. 1 (annotated).) In my opinion, this limitation is met.

*[1b] “a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and”*

94. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka’s LCD panel is connected to semiconductor devices at the periphery of the panel. (Takenaka at Abstract (“The liquid-crystal display device includes a liquid-crystal display panel and *a*

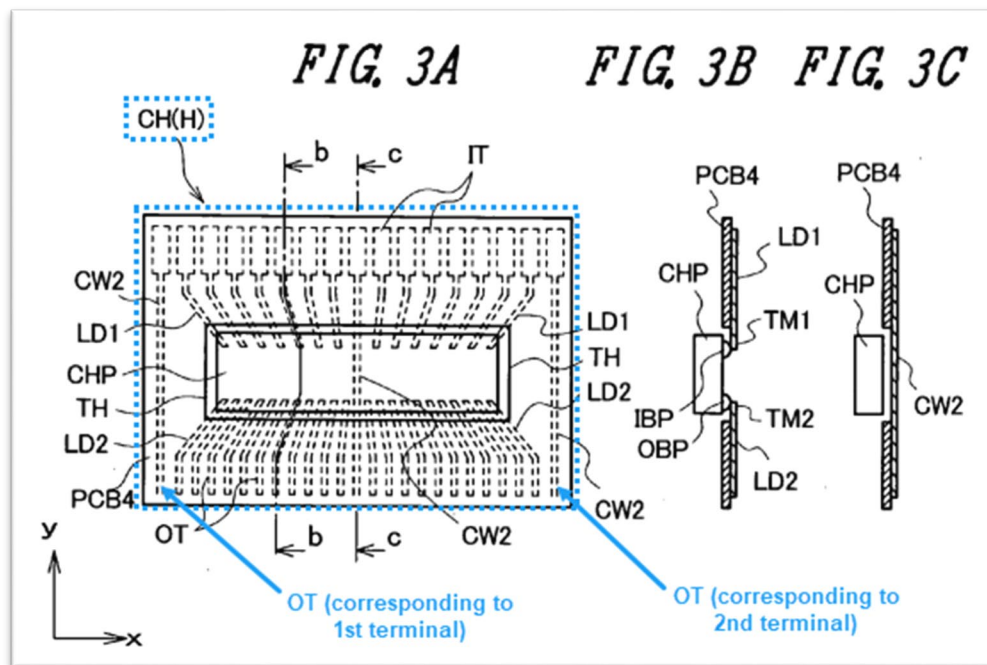
*semiconductor device connected to a part of a periphery of the liquid-crystal display panel.”*), [0028], Fig. 1.) A semiconductor device comprises a chip mounted on a flexible board with lines leading from the terminals of the chip to the periphery of the board. (Takenaka at [0007.]) These lines are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0008] (“Such a semiconductor device can be electrically connected to the *corresponding terminals* . . . [on] a part of the periphery of the liquid crystal display panel.”), [0053] – [0054] (“[Drain signal lines DL] further extend across the seal member SL and reach the *terminals (not shown) on the substrate SUB1. Those terminals are electrically connected to the output terminals of the semiconductor device CH(H)* through a not-shown anisotropic conductive film”), Figs. 1, 2.) Thus, a POSITA would have understood that Takenaka’s LCD panel has a terminal portion and a terminal group.

95. Moreover, a POSITA would understand the necessity for any terminals provided on the semiconductor device to have corresponding terminals on the LCD panel. As shown in Figure 1 below, semiconductor devices (CH(H)) bridge between the panel (PNL) and printed-circuit boards (PCB1) and (PCB2):



(Takenaka at [0042], Fig. 1 (annotated).) For signals to move across the bridges created by the semiconductor devices to reach the LCD panel, the terminals on the semiconductor devices are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0076] (“The flexible board FB is structured with . . . *a plurality of output terminals OT connected to the terminals (not shown) on the liquid-crystal display panel PNL*”), Fig. 1.)

96. Figure 3A is a detailed view of Takenaka’s semiconductor device:



(Takenaka at [0076], Fig. 3A (annotated.)) In addition to the output terminals connected via leads (LD1) to the semiconductor chip, there are two output terminals positioned on either side of the semiconductor device that are not connected to the semiconductor chip. (Takenaka at [0076], [0081] (“Each of these common lines CW2 has one . . . end connected to another *output terminal OT provided parallel with the output terminals OT connected to the leads LD2*”), Fig. 3A.) For the same reasons noted above, a POSITA would understand that these two output terminals are connected to corresponding first and second terminals on the LCD panel, and the first connected pair of terminals is separated from the second pair of connected terminals as shown in Fig. 1. (Takenaka at [0076], [0081], Fig. 1.) In my opinion, this limitation is met.

*[1c] “a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal”*

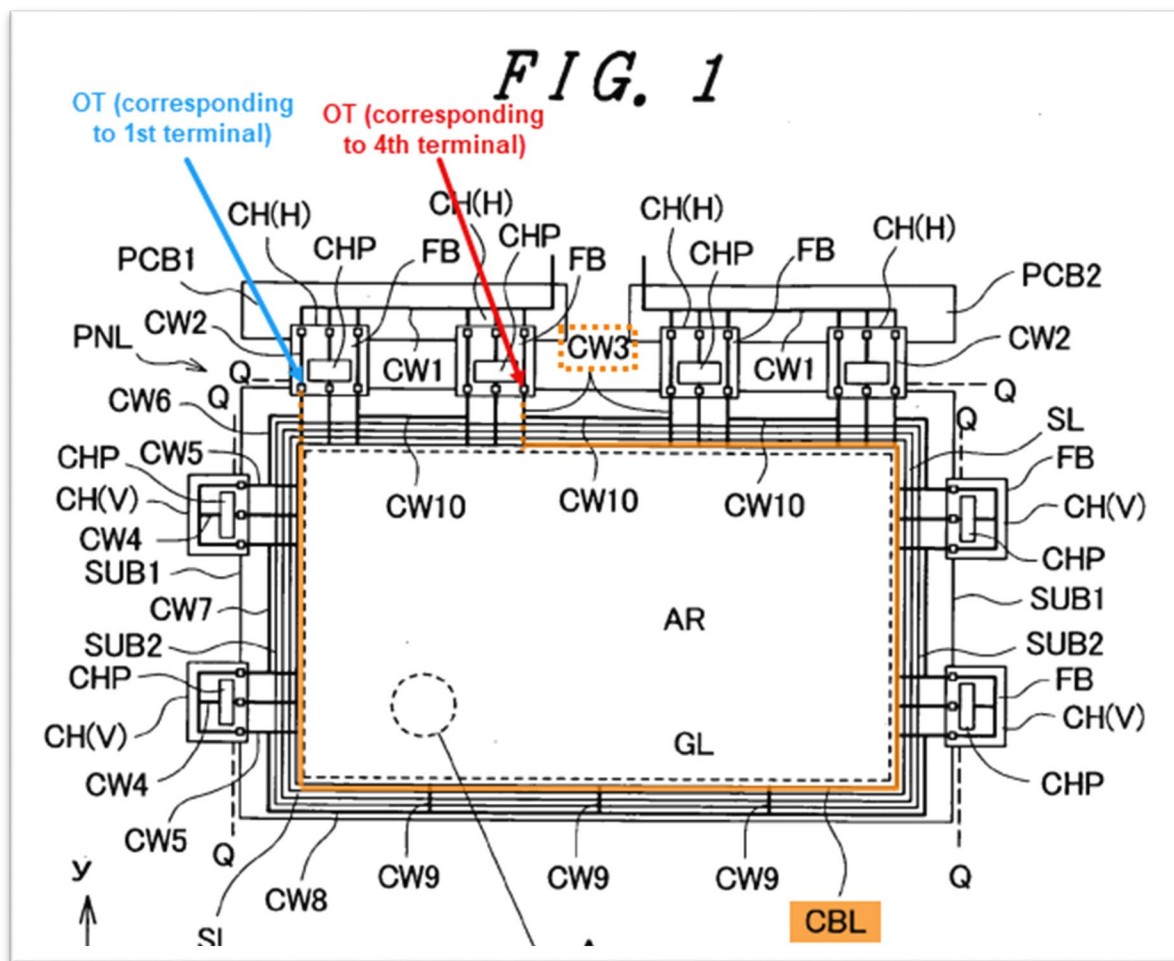
97. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka discloses that the LCD panel is connected to multiple semiconductor devices including, for example, two adjacent CH(H) semiconductor devices. (Takenaka at [0028], [0042], Fig. 1. *See also* Claim [1b] *supra*.) Thus, a POSITA would understand that the LCD panel has a second corresponding terminal portion and group of terminals including third and fourth terminals separated from each other in such a second semiconductor device. (*See* Claim [1b], *supra*.) In my opinion, this limitation is met.

*[1d] “the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,”*

98. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka discloses that there is a need to supply LCD panels with a reference signal having a reference potential relative to the scanning and video signals. (Takenaka at [0009].) Takenaka provides that reference voltage signal through a common bus line (CBL) as well as common lines (CW1), (CW2) and (CW3). (Takenaka at [0037], [0056] (“[T]he reference voltage

signal . . . is led to the common bus line CBL through, in order, the common line CW1 . . . , the common lines CW2 . . . and the common line[s] CW3[.]”, [0058].)

99. As shown in Figure 1 below, common bus line (CBL) is electrically connected to common lines (CW3), both of which are formed on the LCD panel (PNL):



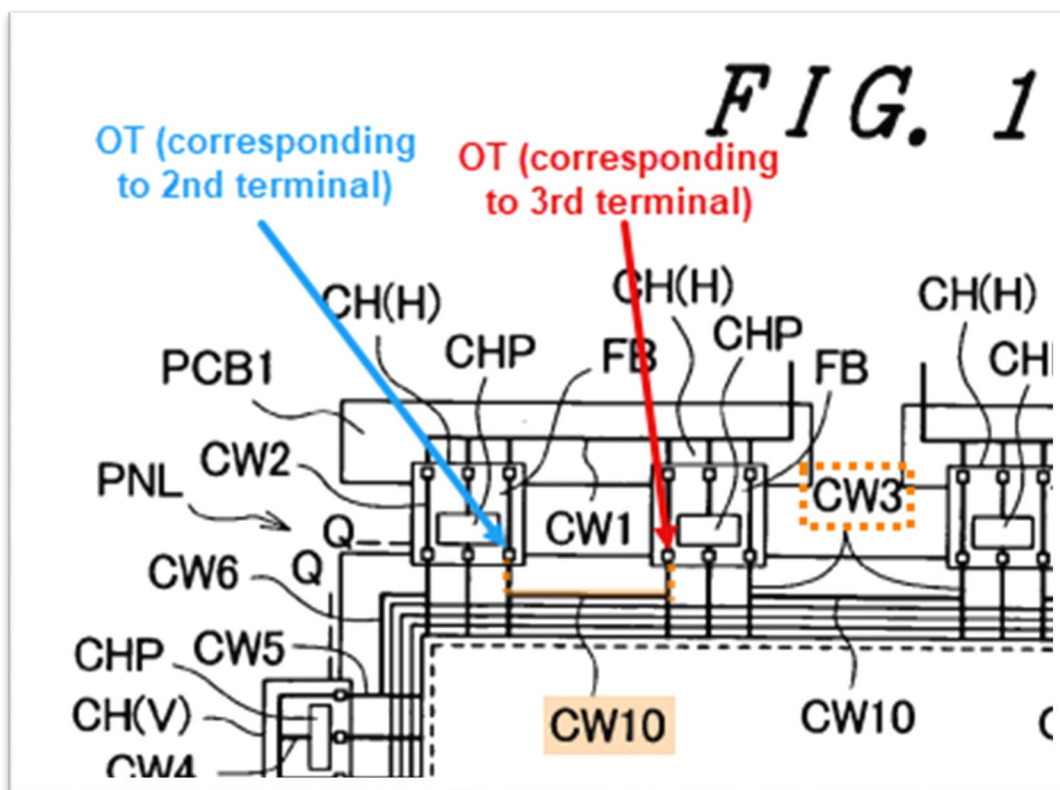
(Takenaka at [0058], Fig. 1 (annotated).) Common lines (CW3) in turn are connected common lines (CW2) to terminals (not shown) on the LCD panel that correspond to output terminals (OT) of semiconductor devices (CH(H)) (small

square boxes). (Takenaka at [0056] (“[C]ommon lines CW1, CW2, CW3 are to be electrically connected together through the terminals (illustrated with square boxes in the figure, corresponding to the references IT and OT in FIG. 3) of the semiconductor device CH(H)[.]”)) Thus, a POSITA would understand that the first and fourth terminals are electrically connected through two common lines (CW3) and common bus line (CBL). (Takenaka at Fig. 1. *See also* Claim [1c], *supra*.) In my opinion, this limitation is met.

*[1e] “the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;”*

100. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka further discloses that additional common lines are provided on the LCD panel, such as common line (CW10), for stabilizing the reference voltage signal throughout the common bus line. (Takenaka at [0070], [0073].)

101. As shown in Figure 1 below, common line (CW10) provides an electrical connection between common lines (CW3):

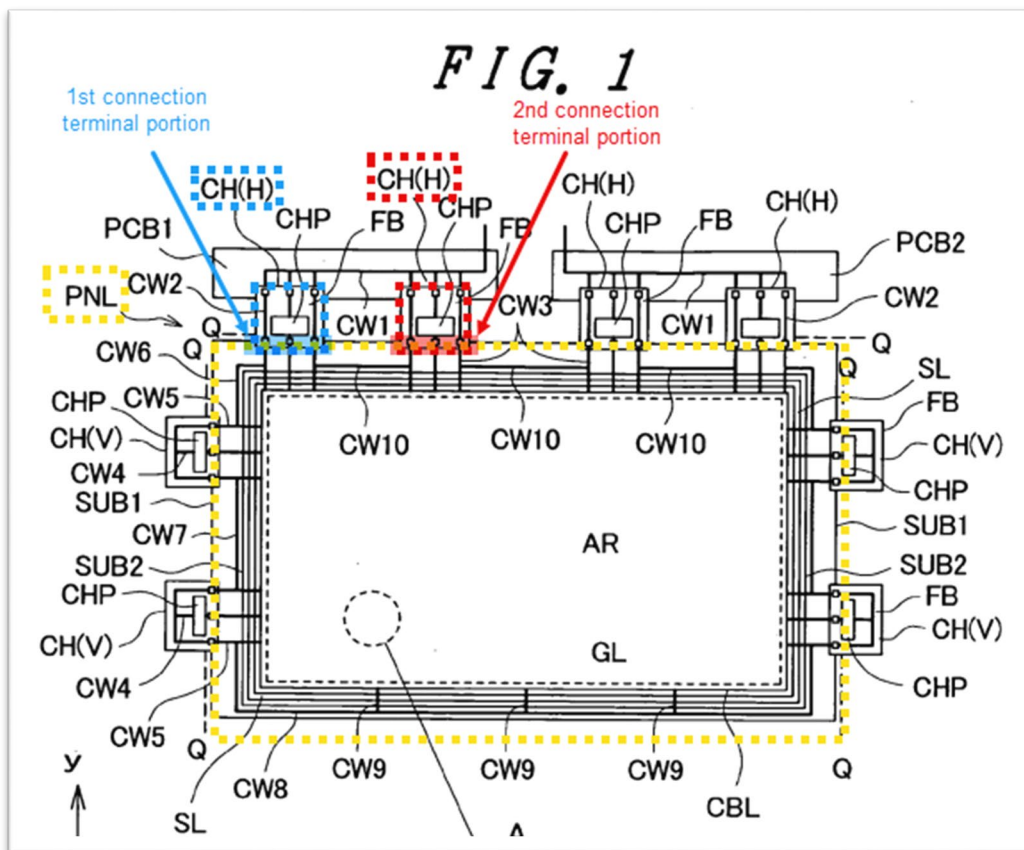


(Takenaka at [0070] (“The common line CW10 is connected between the semiconductor devices CH(H) at their common lines CW3.”), Fig. 1 (annotated).) Accordingly, a POSITA would understand that the LCD panel’s second and third terminals are electrically connected through two common lines (CW3) and common line (CW10). (Takenaka at Fig. 1 (annotated).) In my opinion, this limitation is met.

*[1f] “a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;”*

102. In my opinion, Takenaka teaches this limitation. As shown below, Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each

comprising a flexible board with output terminals that are electrically connected to corresponding terminals on the LCD panel:

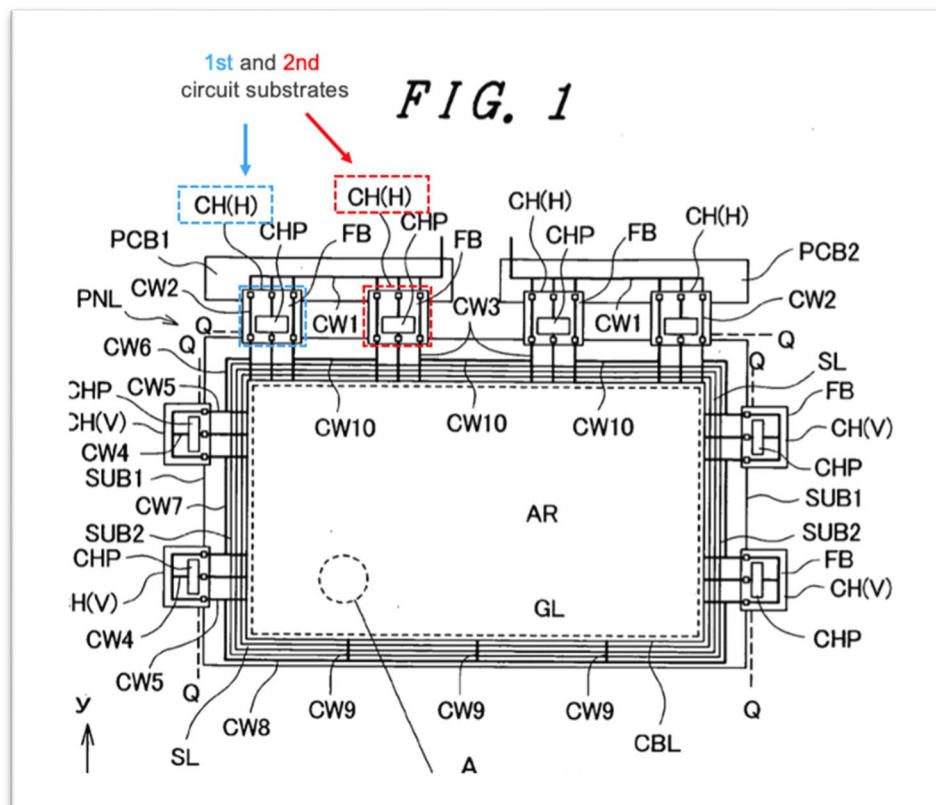


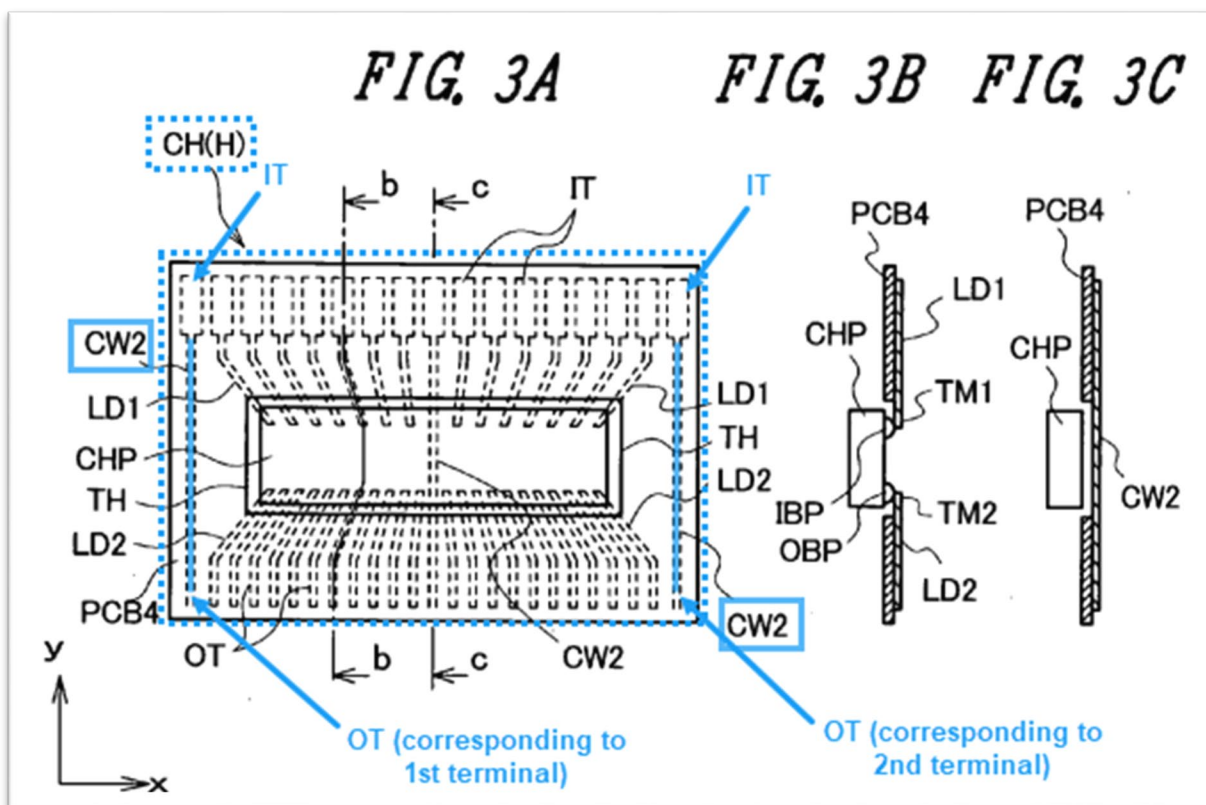
(Takenaka at [0007], [0041], [0076], [0081], Figs. 1, 3A. *See also* Claim [1b], *supra*.) In my opinion, this limitation is met.

*[1g] “a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion; and”*

103. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. As shown in Figures 1 and 3A below,

Takenaka's semiconductor device (CH(H)) further comprises input terminals (IT) at the ends of the two common lines (CW2):



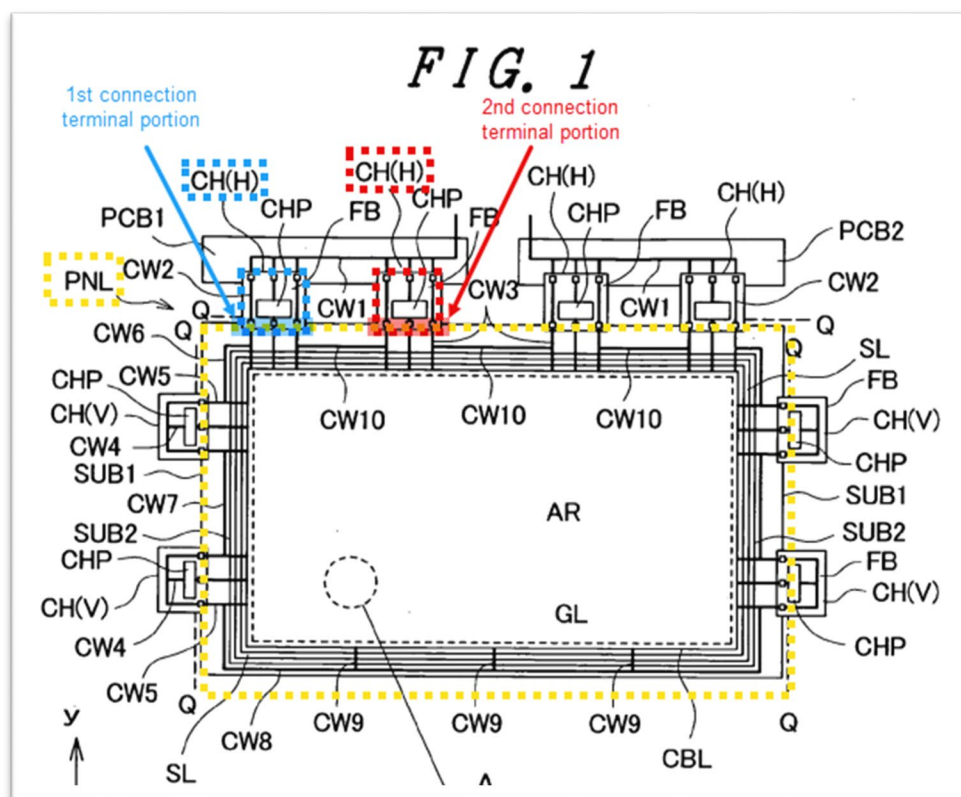


(Takenaka at [0081] (“*Each of these common lines CW2 has one end connected to another input terminal IT[.]*”), Figs. 1 (annotated), 3A (annotated).) These input terminals are electrically connected to the respective output terminals at the other end of each common line (CW2). (Takenaka at [0081], Fig. 3A.) In turn, these output terminals are electrically connected to the corresponding terminals on the LCD panel, as discussed above. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A. *See also* Claims [1b], [1f], *supra*.) Accordingly, a POSITA would understand that Takenaka discloses first and second external terminals on a semiconductor device that are respectively connected to the first and second terminals on the LCD panel

through the first connection terminal portion on the flexible board of Takenaka's semiconductor device. In my opinion, this limitation is met.

*[1h] "a second circuit substrate including: a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion;"*

104. In my opinion, Takenaka teaches this limitation. As shown below, Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each comprising a flexible board with output terminals that are electrically connected to corresponding terminals on the LCD panel:



(Takenaka at [0007], [0041], [0076], [0081], Figs. 1 (annotated), 3A. *See also* Claims [1b], [1f], *supra*.) In my opinion, this limitation is met.

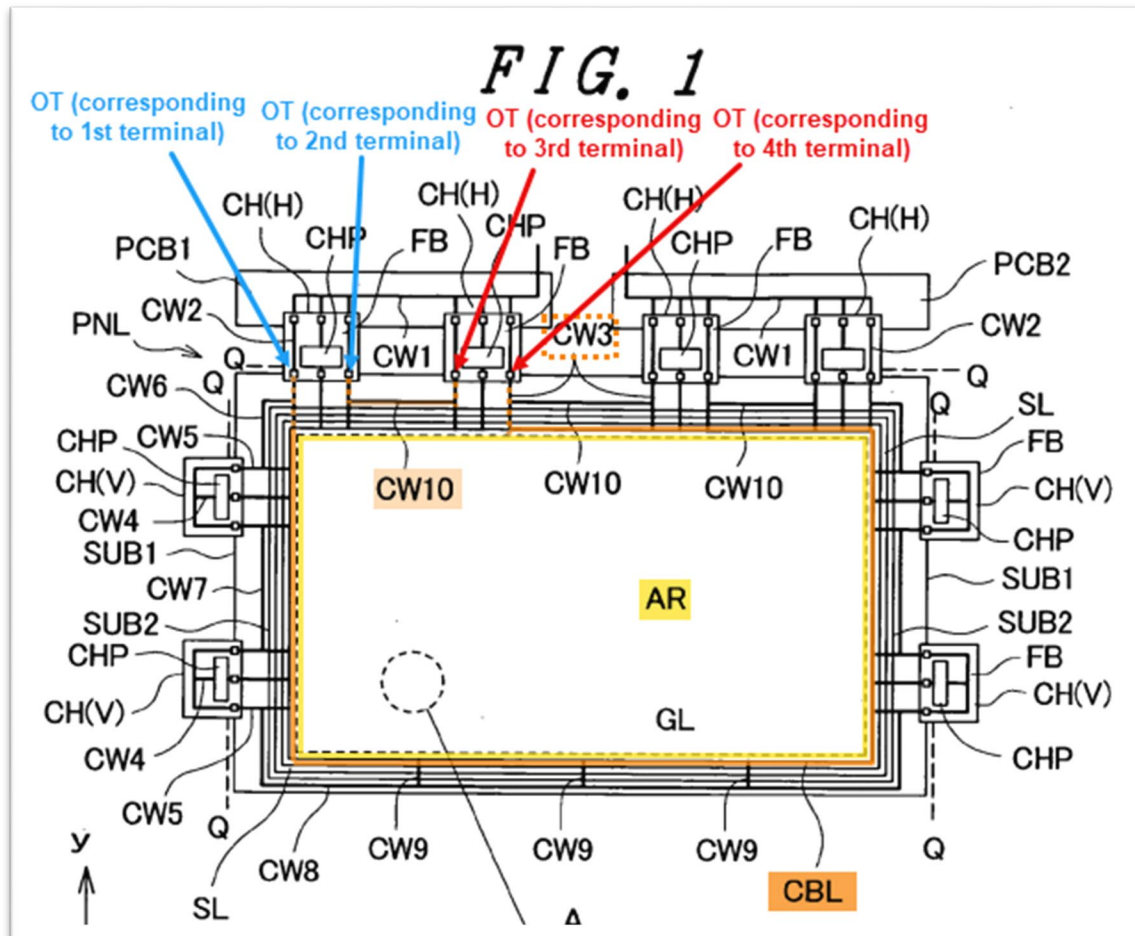
*[1i] “a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.”*

105. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each with input terminals electrically connected to output terminals, which in turn are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A. *See also* Claims [1b], [1g].) Thus, a POSITA would understand that Takenaka discloses third and fourth external terminals on a semiconductor device that are respectively connected to the third and fourth terminals on the LCD panel through the second connection terminal portion on the flexible board of Takenaka’s semiconductor device. In my opinion, this limitation is met.

## **2. Dependent Claim 2**

*The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.*

106. In my opinion, Takenaka teaches this limitation. As shown in Figure 1 below, Takenaka discloses that some of common bus line (CBL) and common line (CW10) extend around the circumference of display region (AR):



(Takenaka at [0030], [0037], [0070], Fig. 1 (annotated).) In my opinion, this limitation is met.

### 3. Dependent Claim 3

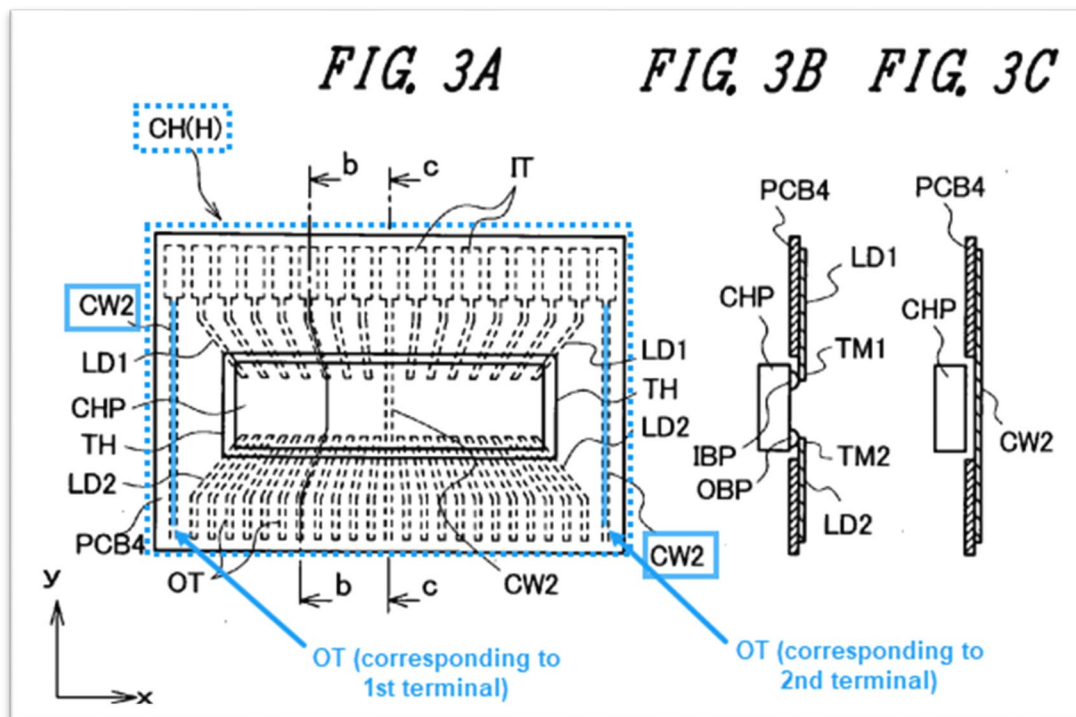
*[3a] The electro-optical device according to claim 1, wherein: each of the first and second group of terminals*

*configures a terminal group arranged in a predetermined direction, and*

107. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. Takenaka discloses that the first and second groups of terminals are fixed on the LCD panel. (See Claims [1b], [1c].) As such, the order of the terminals within a group of terminals does not change, e.g., the first terminal is always on the left of the second terminal. Accordingly, a POSITA would understand that the terminals within a terminal group are arranged in a predetermined direction, for example, the horizontal direction. In my opinion, this limitation is met.

*[3b] the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.*

108. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. As shown in Figure 3A below, Takenaka discloses that common lines (CW2) are positioned on the sides of semiconductor device (CH(H)):

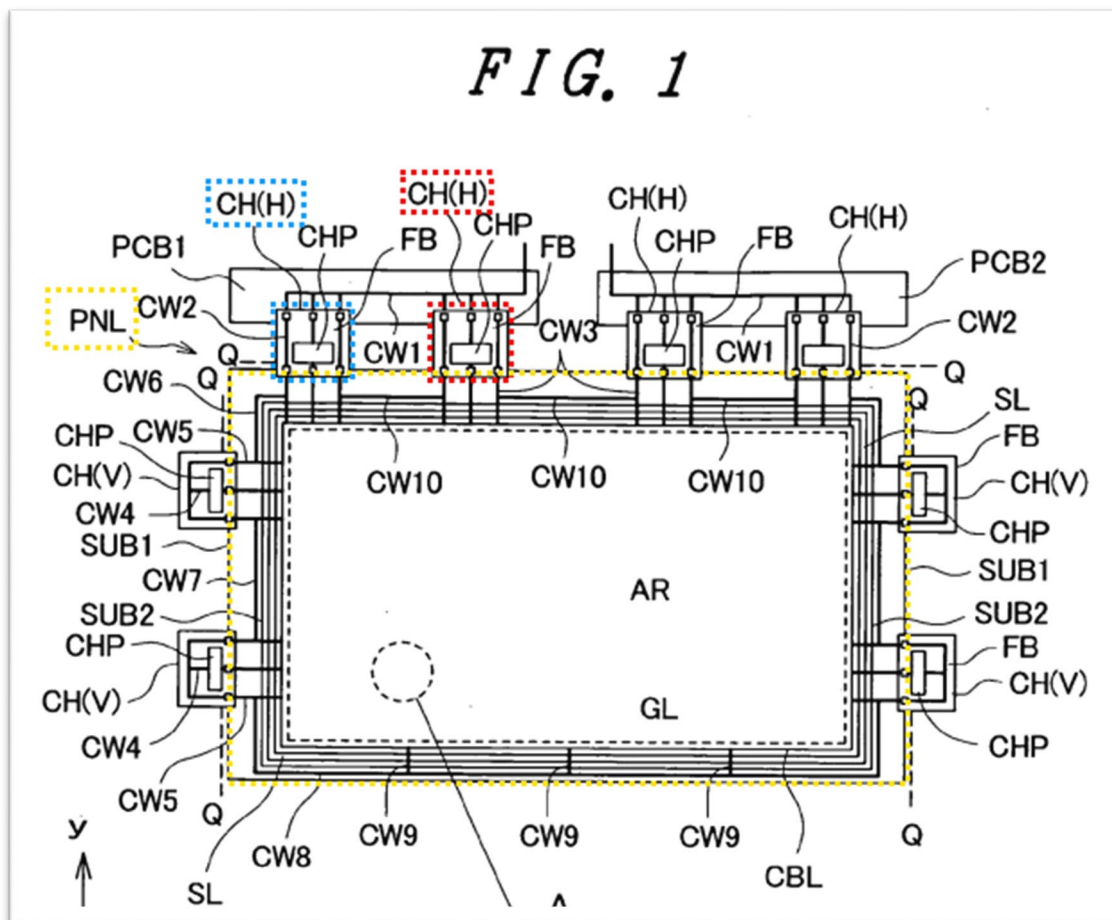


(Takenaka at [0081], Fig. 3A (annotated).) The two output terminals at the ends of common lines (CW2) are also positioned at the sides of the semiconductor device, at the ends of the row of output terminals in the horizontal direction. (Takenaka at [0081], Fig. 3A.) Accordingly, a POSITA would understand that the LCD panel's first and second terminals, and third and fourth terminals corresponding to these output terminals are at the ends of the first and second groups of terminals, respectively, in the predetermined direction. In my opinion, this limitation is met.

#### 4. Dependent Claim 4

*[4] The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.*

109. In my opinion, Takenaka teaches this limitation. As shown in Figure 1 below, Takenaka discloses multiple semiconductor devices (CH(H)) connected to the LCD panel (PNL) along its top side:



(Takenaka at [0028], Fig. 1 (annotated).) The bottom side of the panel is a second side of a direction crossing the top side of the panel. In my opinion, this limitation is met.

## 5. Dependent Claim 5

*[5a] The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a*



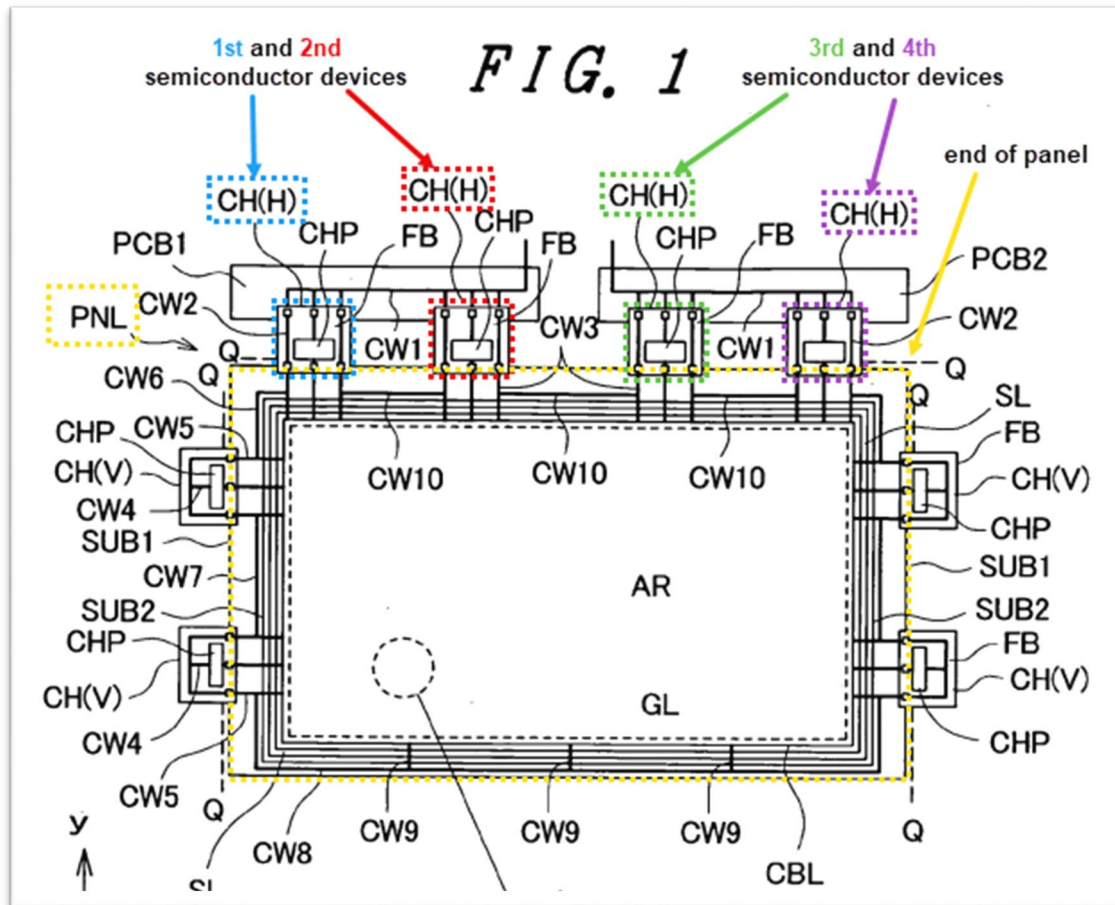
adjacent third and fourth terminal portions with third and fourth groups of terminals, respectively. In my opinion, this limitation is met.

*[5b] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,*

111. In my opinion, Takenaka teaches this limitation. Takenaka discloses two pairs of semiconductor devices, each comprising a flexible board having output terminals that are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0041], [0076], [0081], Figs. 1, 3A. *See also* Claims [1b], [1c], [1f], [1h], [5a] *supra*.) In my opinion, this limitation is met.

*[5c] the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel,*

112. In my opinion, Takenaka teaches this limitation. As shown in Figure 1 below, Takenaka discloses that the third and fourth semiconductor devices are respectively positioned between the first and second semiconductor devices and an end of the LCD panel:



(Takenaka at [0028], Fig. 1 (annotated). *See also* Claims [1b], [1c], [5a], *supra.*) In my opinion, this limitation is met.

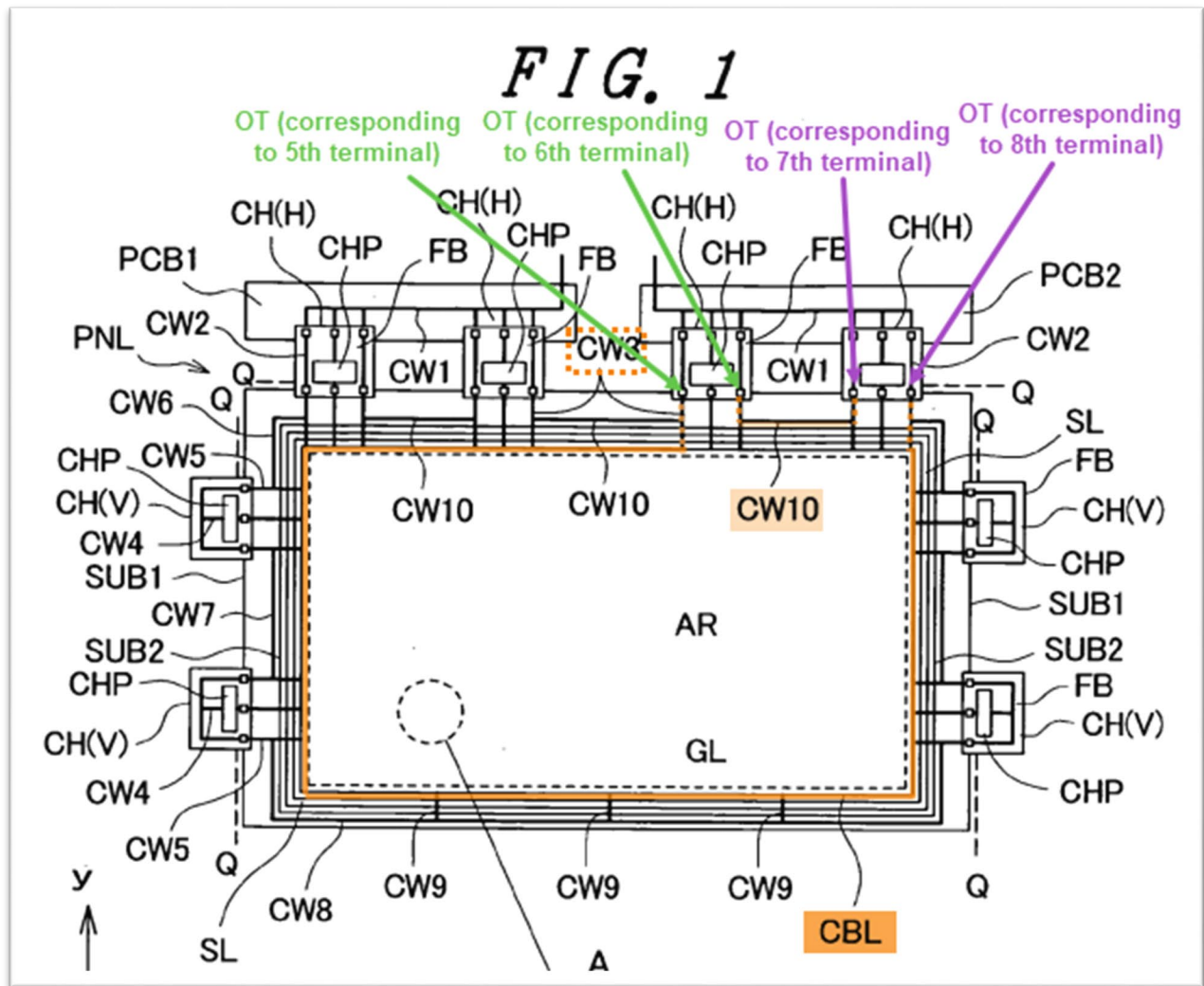
*[5d] the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and*

113. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in structure and are similarly electrically connected to corresponding

terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A. *See also* Claims [1b], [1c], *supra*.) Accordingly, a POSITA would understand that the third and fourth groups of terminals on the LCD panel have fifth and sixth, and seventh and eighth terminals, respectively, that are each separated from one another. (Takenaka at [0076], [0081]. *See also* Claims 1[b], 1[c], *supra*.) In my opinion, this limitation is met.

*[5e] the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,*

114. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to provide a reference voltage signal to the LCD Panel. (Takenaka at [0037], [0056], [0058], [0070] Figs. 1, 3A. *See also* Claims [1d], [1e], *supra*.) As shown in Figure 1 below, the fifth and eighth terminals are electrically connected, and the sixth and seventh terminals are electrically connected:



(Takenaka at [0007], [0076], [0081], Figs. 1 (annotated), 3A. *See also* Claims [1d], [1e], *supra*.) Accordingly, a POSITA would understand that the fifth and eighth terminals are electrically connected through two common lines (CW3) and common bus line (CBL), whereas the sixth and seventh terminals are electrically connected through two common lines (CW3) and common line (CW10). In my opinion, this limitation is met.

*[5f] the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and*

115. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in structure and are similarly electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A. *See also* Claims [1b], [1c], [1g], [1i] *supra*.) Accordingly, a POSITA would understand that Takenaka discloses fifth and sixth external terminals on a semiconductor device that are respectively connected to the fifth and sixth terminals on the LCD panel through the panel's third connection terminal portion. In my opinion, this limitation is met.

*[5g] the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.*

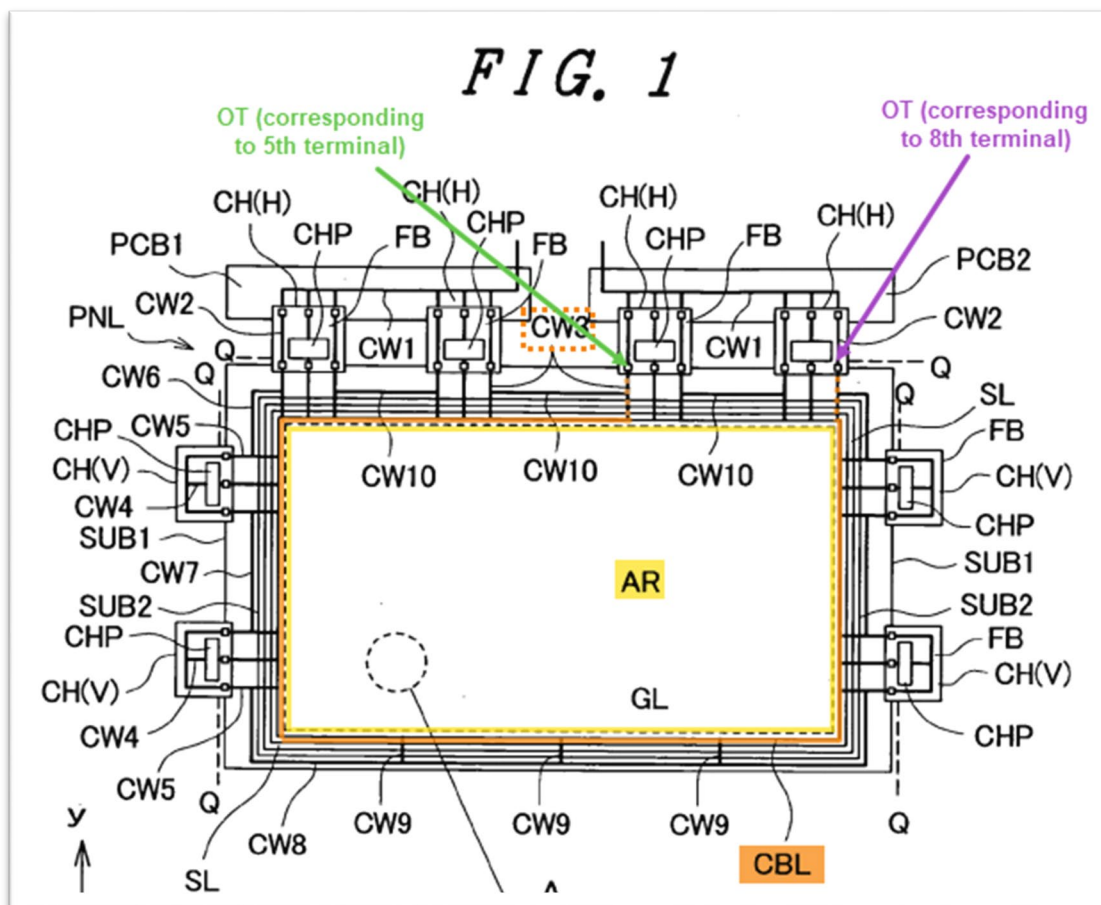
116. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in structure and are similarly electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A. *See also* Claims [1b], [1c], [1g], [1i] *supra*.) Accordingly, a POSITA would understand that Takenaka discloses seventh and eighth external terminals on a semiconductor

device that are respectively connected to the seventh and eighth terminals on the LCD panel through the panel's fourth connection terminal portion. In my opinion, this limitation is met.

## 6. Dependent Claim 6

*[6] The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.*

117. In my opinion, Takenaka teaches this limitation. As shown in Figure 1 below, the third connection wiring, comprising two common lines (CW3) and common bus line (CBL), extends around the circumference of display region (AR):



(Takenaka at [0030], [0037], [0073], Fig. 1 (annotated). *See also* Claims [2], [5e], *supra.*) In my opinion, this limitation is met.

## **7. Dependent Claim 7**

*[7a] The electro-optical device according to claim 5, wherein: each of the third and fourth group of terminals configures a terminal group arranged in a predetermined direction, and*

118. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A. *See also* Claims 3[a], [5a], [5b], [5d], *supra.*) Accordingly, a POSITA would understand that the third and fourth group of terminals are each arranged in a predetermined direction. In my opinion, this limitation is met.

*[7b] the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.*

119. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A. *See also* Claims 3[b], [5a], [5b], [5d], *supra.*) Accordingly, a POSITA

would understand that the LCD panel's fifth and sixth terminals, and seventh and eighth terminals are at the ends of the third and fourth groups of terminals, respectively, in the predetermined direction. In my opinion, this limitation is met.

## **11. Independent Claim 11**

*[11pre] An electro-optical panel comprising:*

120. In my opinion, to the extent the preamble is limiting, it is taught by Takenaka. Takenaka discloses a “liquid-crystal display device [that] includes a *liquid-crystal display panel*[.]” (Takenaka at Abstract. *See also* Claim [1a].) In my opinion, this limitation is met.

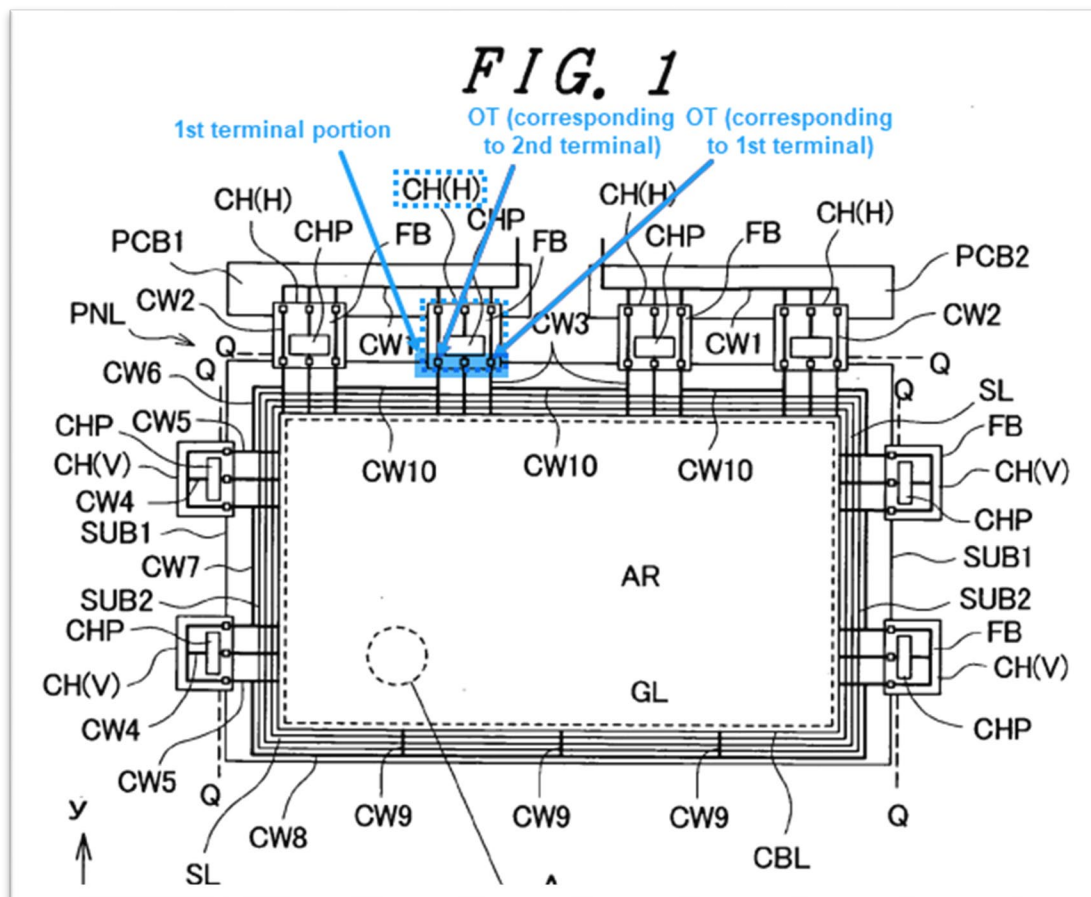
*[11a] a substrate;*

121. In my opinion, Takenaka teaches this limitation. Takenaka discloses that the LCD panel “is structured with an envelope including a *substrate SUB1* (lower substrate in the figure) and a substrate SUB2 (upper substrate in the figure)[.]” (Takenaka at [0026].) In my opinion, this limitation is met.

*[11b] a first terminal portion including a first group of terminals having a first terminal and a second terminal separated from each other;*

122. In my opinion, Claim [11b] is substantially similar to Claim [1b], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious.

123. Here, however, the first terminal portion, first group of terminals, and first and second terminals are designated in relation to the middle, left semiconductor device, as shown in Figure 1 below:

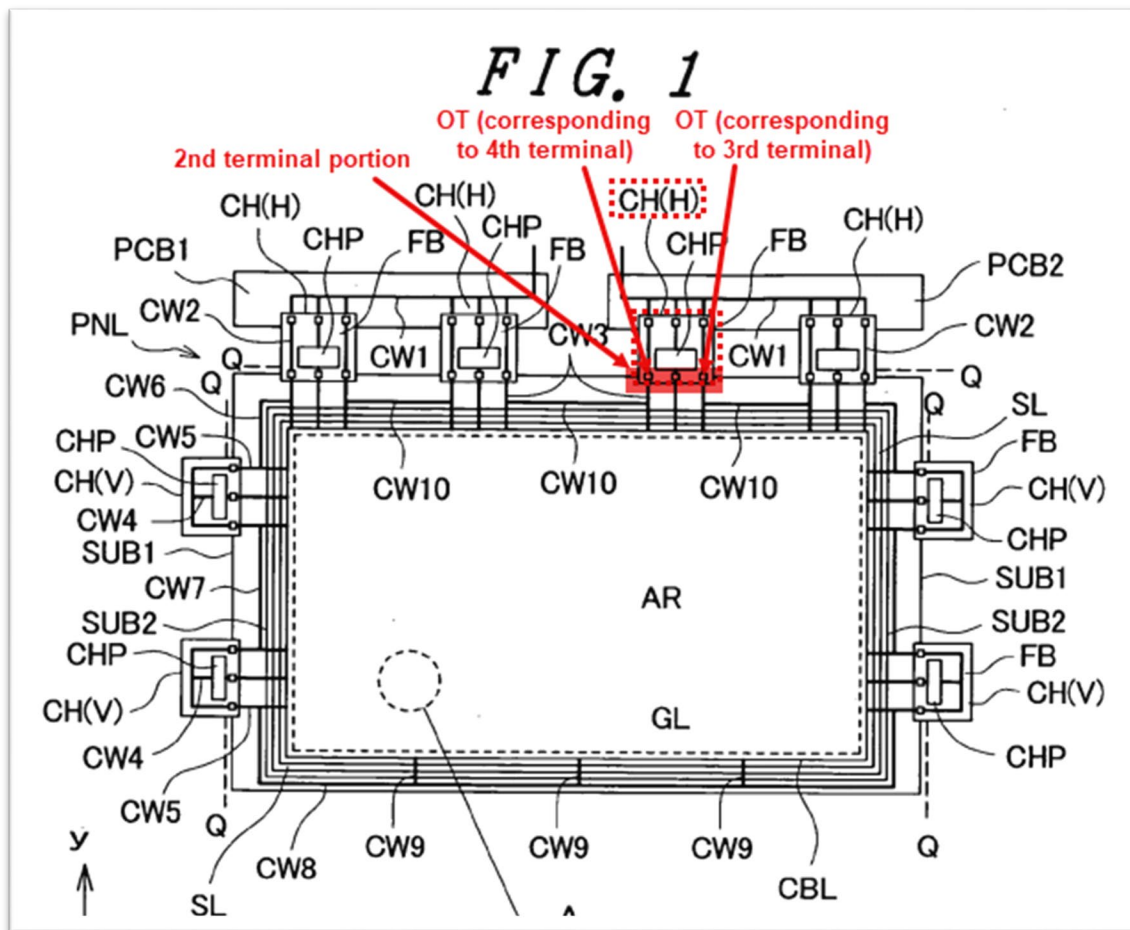


(Takenaka at Fig. 1 (annotated). See also Claim [1b].) In my opinion, this limitation is met.

*[11c] a second terminal portion arranged adjacent to the first terminal portion, the second terminal portion including a second group of terminals having a third terminal and a fourth terminal separated from each other;*

124. In my opinion, Claim [11c] is substantially similar to Claim [1c], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious.

125. Here, however, the second terminal portion, second group of terminals, and third and fourth terminals are designated in relation to the middle, right semiconductor device, as shown in Figure 1 below:

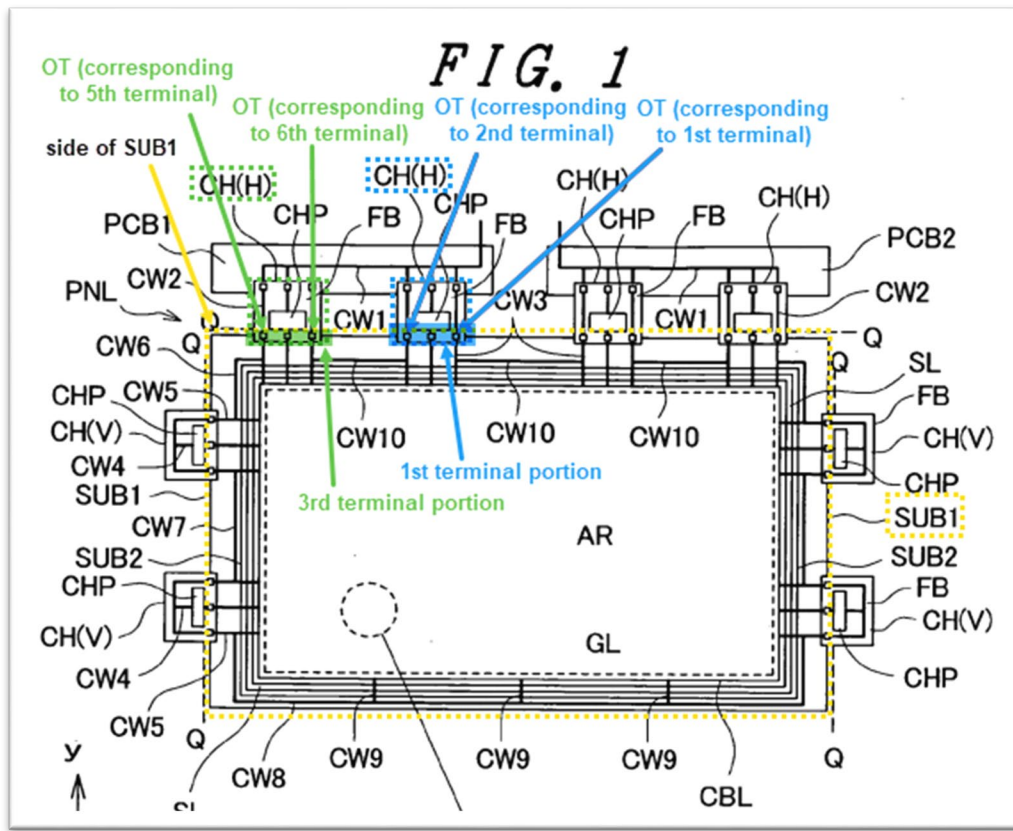


(Takenaka at Fig. 1 (annotated). See also Claim [1c].) In my opinion, this limitation is met.

*[11d] a third terminal portion arranged between one side of the substrate and the first terminal portion, the third terminal portion including a third group of terminals having a fifth terminal and a sixth terminal separated from each other;*

126. In my opinion, Claim [11d] is substantially similar to the combination of Claims [5a], [5c] and [5d], discussed in Section X.A.5. However, they differ in that the third terminal portion is not required to be adjacent to the fourth terminal portion. (*Compare* Claim [11d] *with* Claims [5a], [5c] and [5d].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious.

127. Here, because the third terminal portion is not required to be adjacent to the fourth terminal portion, the third terminal portion, third group of terminals, and fifth and sixth terminals are designated in relation to the outer, left semiconductor device, as shown in Figure 1 below:



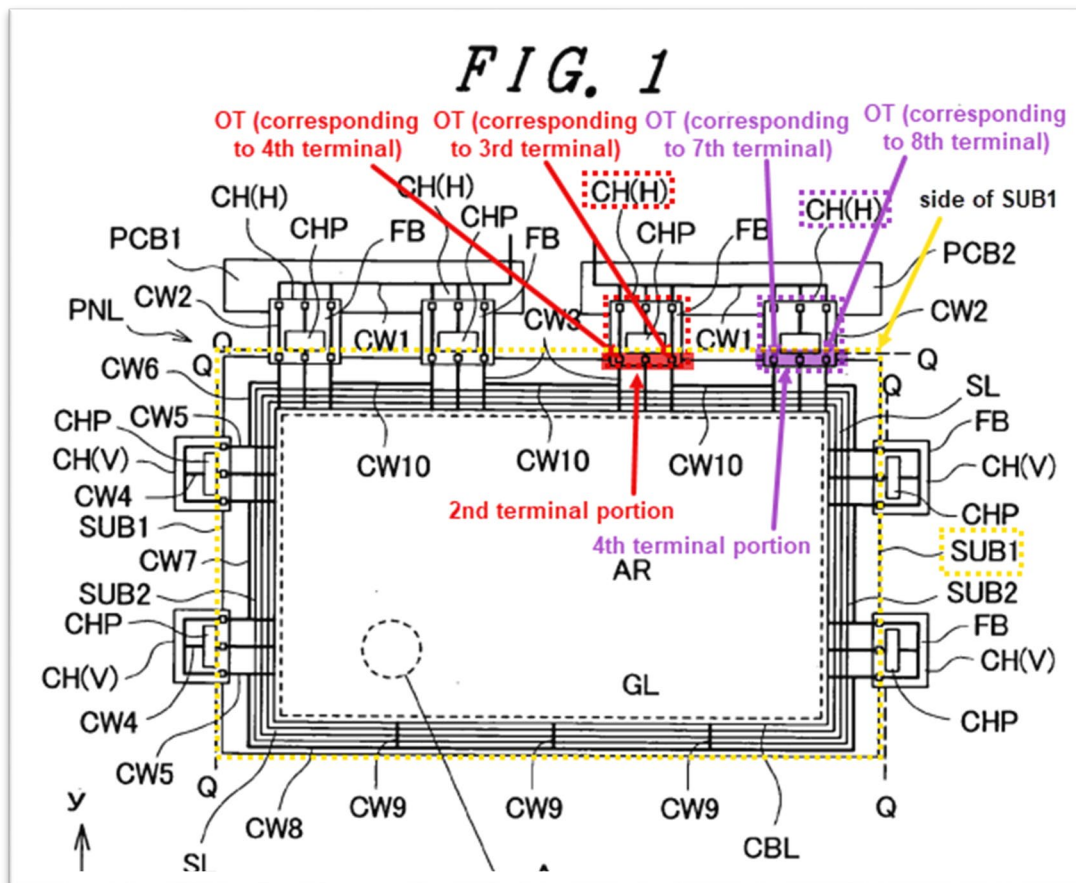
(Takenaka at Fig. 1 (annotated). *See also* Claims [5a], [5c] and [5d].) In this arrangement, a POSITA would understand that the third terminal portion is between the first terminal portion and one side of the substrate (SUB1). In my opinion, this limitation is met.

[11e] a fourth terminal portion arranged between one side of the substrate and the second terminal portion, the fourth terminal portion including a fourth group of terminals having a seventh terminal and a eighth terminal separated from each other;

128. In my opinion, Claim [11e] is substantially similar to the combination of Claims [5a], [5c] and [5d], discussed in Section X.A.5. However, they differ in that the fourth terminal portion is not required to be adjacent to the third terminal

portion. (Compare Claim [11e] with Claims [5a], [5c] and [5d].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious.

129. Here, because the fourth terminal portion is not required to be adjacent to the third terminal portion, the fourth terminal portion, fourth group of terminals, and seventh and eighth terminals are designated in relation to the outer, right semiconductor device, as shown in Figure 1 below:



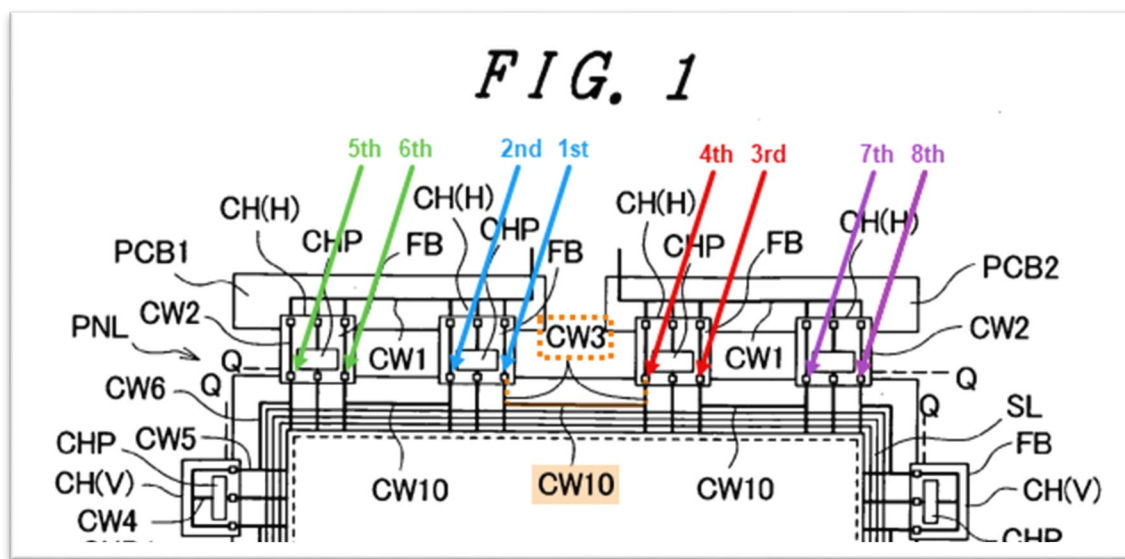
(Takenaka at Fig. 1 (annotated). See also Claims [5a], [5c] and [5d].) In this arrangement, a POSITA would understand that the third terminal portion is between

the first terminal portion and one side of the substrate (SUB1). In my opinion, this limitation is met.

*[11f] a first connection wiring configured to electrically connect the first terminal and the fourth terminal;*

130. In my opinion, Claim [11f] is substantially similar to Claim [1d], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious.

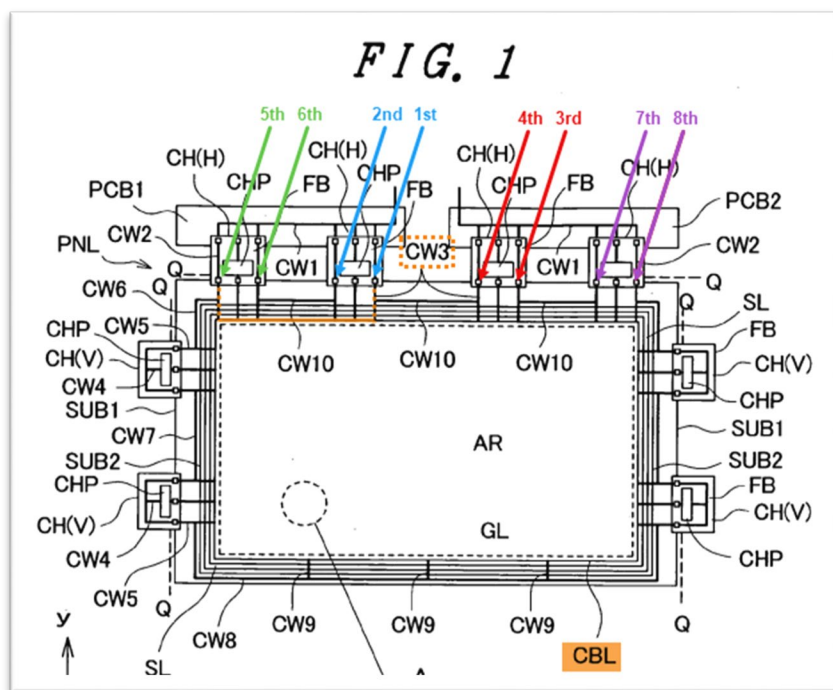
131. Here, however, the first and fourth terminals are electrically connected through two common lines (CW3) and common line (CW10), as shown in Figure 1 below:



(Takenaka at Fig. 1 (annotated). See also Claim [1d].) In my opinion, this limitation is met.

*[11g] a fifth connection wiring configured to electrically connect the first terminal and the fifth terminal;*

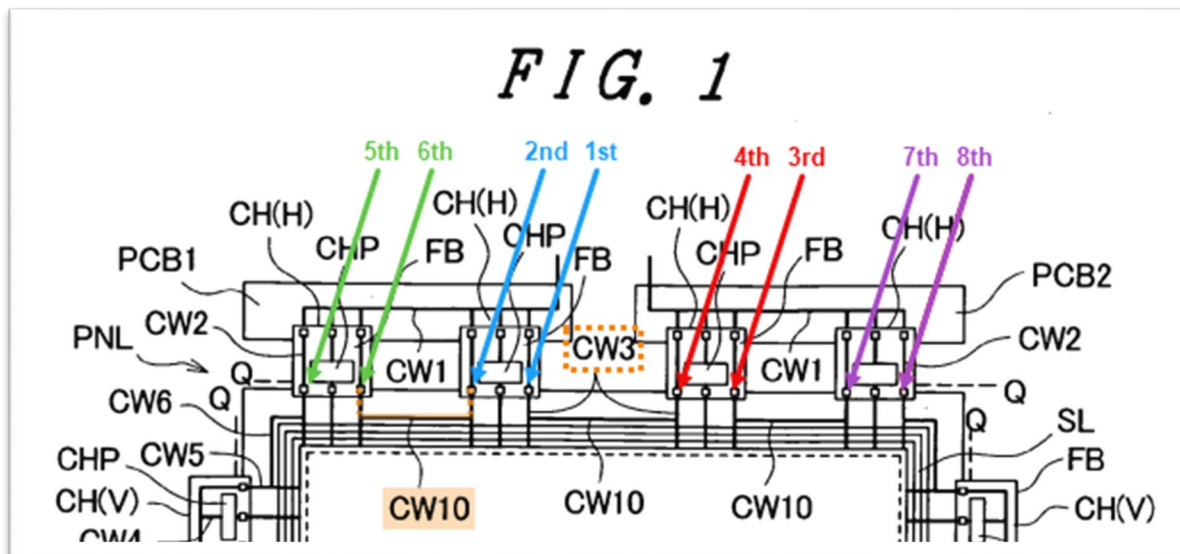
132. In my opinion, Claim [11d] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections X.A.1 and X.A.5. However, they differ in that the first and fifth terminals are electrically connected. (*Compare* Claim [11g] *with* Claims [1d], [1e] and [5e].) As shown in Figure 1 below, the first and fifth terminals are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated). *See also* Claims [1d], [1e] and [5e].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[11h] a sixth connection wiring configured to electrically connect the second terminal and the sixth terminal;*

133. In my opinion, Claim [11h] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections X.A.1 and X.A.5. However, they differ in that the second and sixth terminals are electrically connected. (*Compare Claim [11h] with Claims [1d], [1e] and [5e].*) As shown in Figure 1 below, the second and sixth terminals are electrically connected through two common lines (CW3) and common line (CW10):

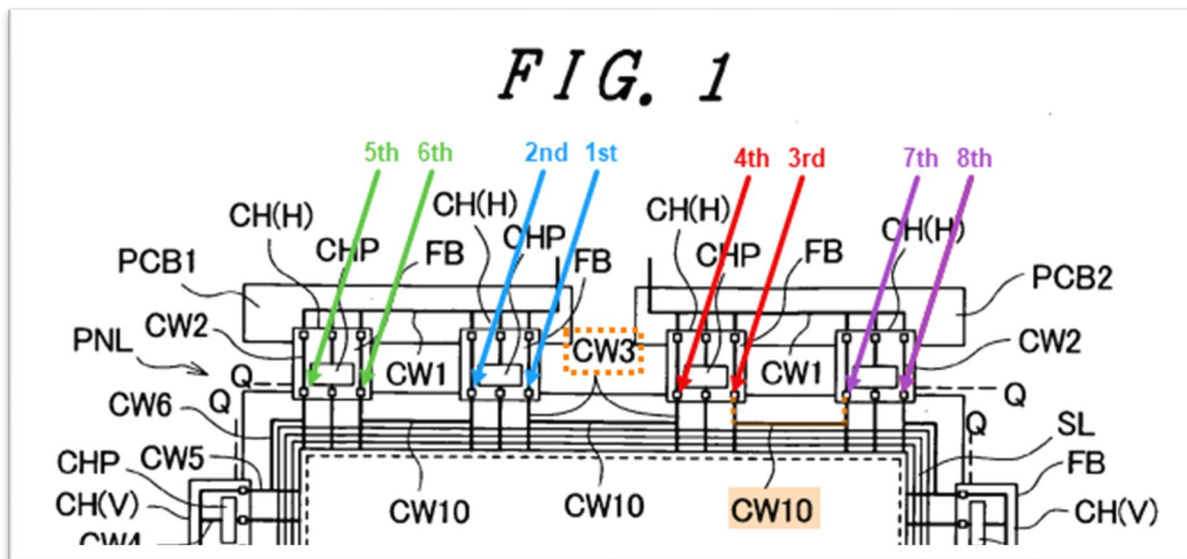


(Takenaka at Fig. 1 (annotated). *See also* Claims [1d], [1e] and [5e].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[11i] a seventh connection wiring configured to electrically connect the third terminal and the seventh terminal;*

134. In my opinion, Claim [11i] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections X.A.1 and X.A.5. However, they differ in that

the third and seventh terminals are electrically connected. (*Compare Claim [11i] with Claims [1d], [1e] and [5e].*) As shown in Figure 1 below, the third and seventh terminals are electrically connected through two common lines (CW3) and common line (CW10):

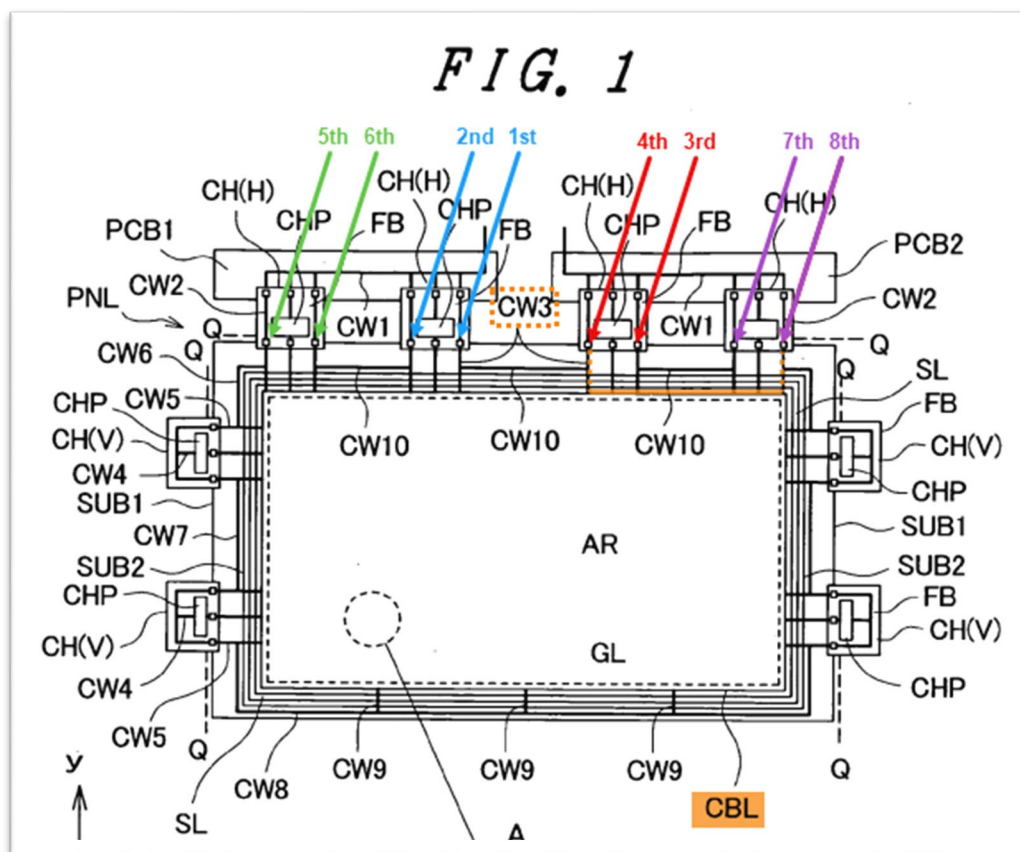


(Takenaka at Fig. 1 (annotated). *See also Claims [1d], [1e] and [5e].*) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[11j] an eighth connection wiring configured to electrically connect the fourth terminal and the eighth terminal; and*

135. In my opinion, Claim [11j] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections X.A.1 and X.A.5. However, they differ in that the fourth and eighth terminals are electrically connected. (*Compare Claim [11j] with Claims [1d], [1e] and [5e].*) As shown in Figure 1 below, the fourth and eighth

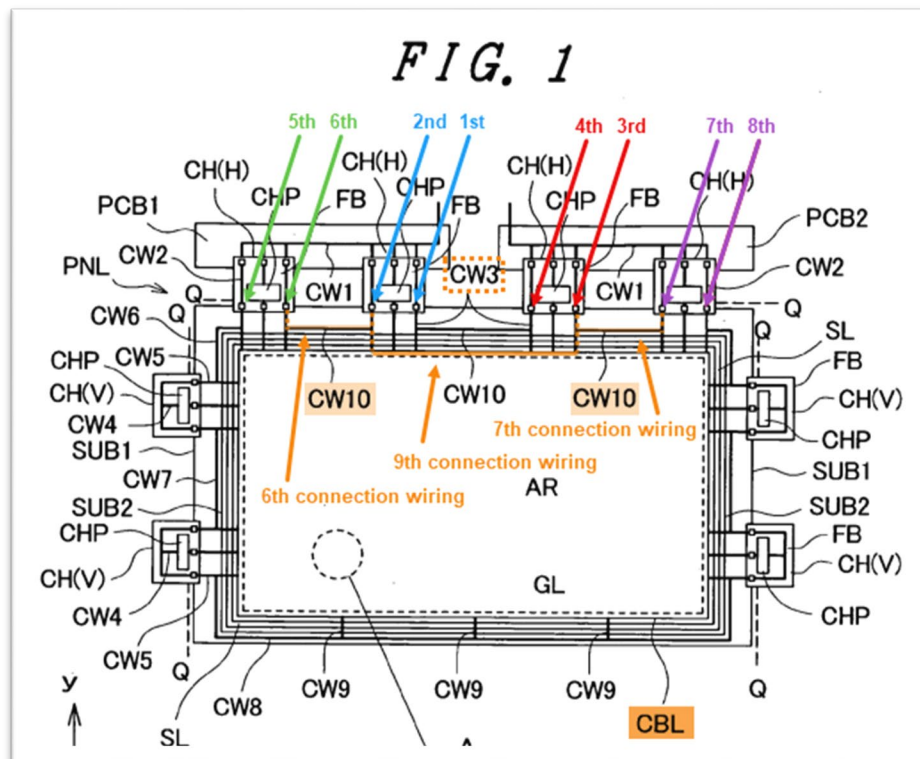
terminals are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated). See also Claims [1d], [1e] and [5e].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[11k] a ninth connection wiring configured to electrically connect the sixth connection wiring and the seventh connection wiring so as to electrically connect the second terminal, the third terminal, the sixth terminal and the seventh terminal.*

136. In my opinion, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. As shown in Figure 1 below, Takenaka discloses that the sixth and seventh connection wirings are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated). *See also* Claims [1d], [1e] and [5e].) Accordingly, a POSITA would understand that this ninth connection wiring electrically connects the second, third, sixth and seventh terminals. In my opinion, this limitation is met.

## 12. Dependent Claim 12

[12a] *An electro-optical device comprising: the electro-optical panel according to claim 11;*

137. In my opinion, Claim [12a] is substantially similar to the combination of Claims [1pre] and [1a], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12b] a first circuit substrate on which a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion is provided and*

138. In my opinion, Claim [12b] is substantially similar to Claim [1f], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12c] which has a first external terminal connected to the first terminal through the first connection terminal portion and a second external terminal connected to the second terminal;*

139. In my opinion, Claim [12c] is substantially similar to Claim [1g], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12d] a second circuit substrate on which a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion is provided and*

140. In my opinion, Claim [12d] is substantially similar to Claim [1h], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12e] which has a third external terminal connected to the third terminal through the second connection terminal portion and a fourth external terminal connected to the fourth terminal;*

141. In my opinion, Claim [12e] is substantially similar to Claim [1i], discussed in Section X.A.1. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12f] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided and*

142. In my opinion, Claim [12f] is substantially similar to Claim [5b], discussed in Section X.A.5. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12g] which has a fifth external terminal connected to the fifth terminal through the third connection terminal portion and a sixth external terminal connected to the sixth terminal; and*

143. In my opinion, Claim [12g] is substantially similar to Claim [5f], discussed in Section X.A.5. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12h] a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided and*

144. In my opinion, Claim [12h] is substantially similar to Claim [5b], discussed in Section X.A.5. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[12i] which has a seventh external terminal connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal connected to the eighth terminal.*

145. In my opinion, Claim [12i] is substantially similar to Claim [5g], discussed in Section X.A.5. Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

**B. Ground 2: Claims 8-10 are Obvious over Takenaka and Ito**

146. Claims 8-10 are directed to an electro-optical device wherein a third terminal portion is “arranged on a side opposed to a display region with respect to

the first terminal portion.” (’020 Patent, cl. 8.) Takenaka does not disclose an LCD device with terminal portions in this arrangement as it would be understood by a POSITA at the time of the ’020 Patent’s filing. However, as discussed below, it is my opinion that it would have been obvious to a POSITA to configure Takenaka’s terminal portions in Ito’s arrangement.

### **Motivation to Combine**

147. In my opinion, a POSITA would have been motivated to combine the teachings of Takenaka with Ito.

148. Both references were driven by the same design incentives: increasing the number of terminals on the LCD panel to improve display quality. (Takenaka at [0011] (“[B]y reason of the increasing number of pixels with the addressability improvement of the liquid-crystal display panel, the number of terminals must be increased[.]”); Ito at [0041] (“[H]aving two ranks of external circuit connecting terminals . . . enables an increase in resolution while accommodating the need for mini[a]turaization”).)

149. Moreover, both references offer solutions to reliability issues that arise from increasing the number of pixels, albeit in slightly different ways. Takenaka proposes supplying a stable reference voltage signal to the pixels through a multiplicity of wirings, including some provided on the flexible boards of the semiconductor devices. (Takenaka at [0011]- [0015], [0018].) Ito proposes

offsetting the integrated circuits provided on the flexible substrates such that they do not overheat when driven. (Ito at [0005], [0007], [0010], [0013] - [0014], [0041], [0045].)

150. Neither reference teaches away from the other. While Ito describes its arrangement of the panel terminals being motivated by the miniaturization of panels, it expressly acknowledges the possibility of fitting three or more flexible substrates. (Ito at [0041], [0047].) As such, a POSITA would not be discouraged from combining the references.

151. Modifying Takenaka to configure the terminal portions in Ito's arrangement would also be simple and obvious to try. Takenaka teaches or renders obvious two terminal portions aligned parallel to the side of the panel. (Takenaka at Fig. 1.) Ito teaches that terminal portions may be aligned perpendicular to the side of the panel: the one other possible arrangement given the shape and alignment of terminals on each terminal portion shown in both Takenaka and Ito. (Ito at Fig. 4.) As a result, configuring Takenaka's terminal portions in Ito's arrangement would have been achieved with a reasonable expectation of success and involved simply repositioning the terminal portions.

## **8. Independent Claim 8**

*[8pre] An electro-optical device comprising:*

152. In my opinion, Claim [8pre] is identical to Claim [1pre]. For the reasons discussed in Section X.A.1, Takenaka teaches this limitation. In my opinion, this limitation is met.

*[8a] an electro-optical panel including:*

153. In my opinion, Claim [8a] is identical to Claim [1a]. For the reasons discussed in Section X.A.1, Takenaka teaches this limitation. In my opinion, this limitation is met.

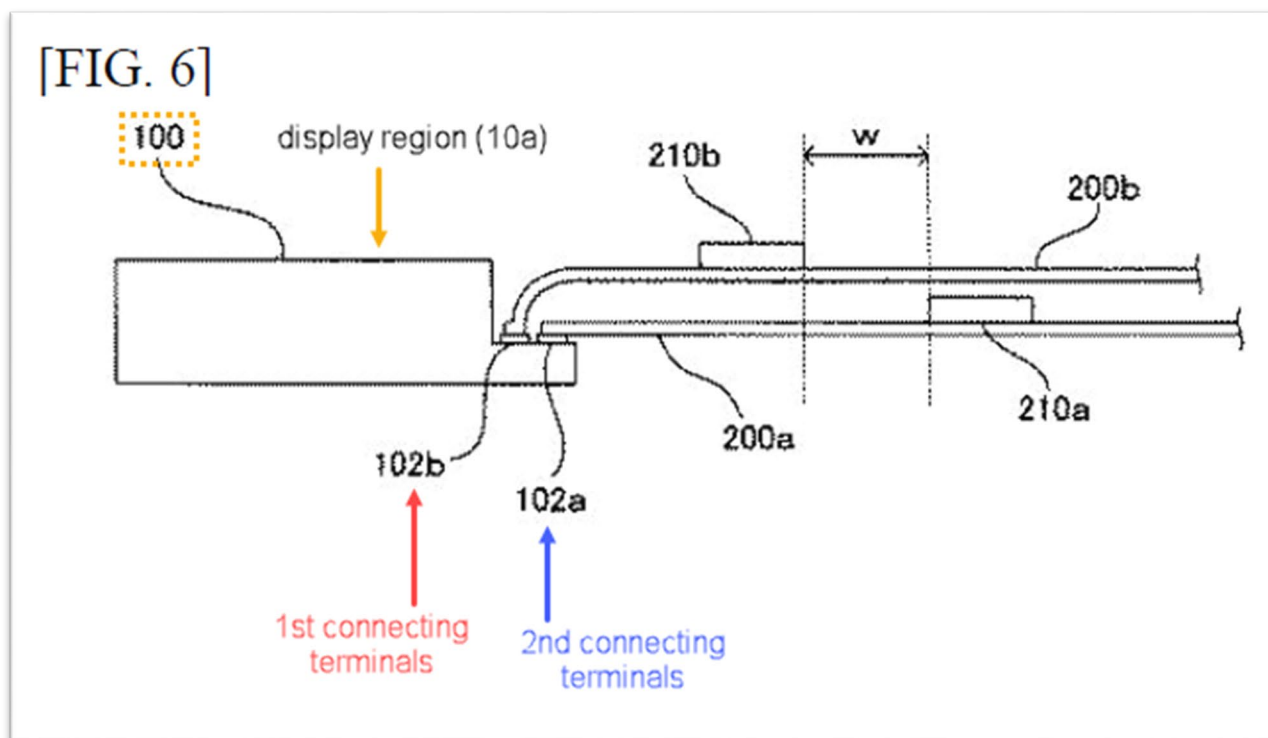
*[8b] a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and*

154. In my opinion, Claim [8b] is identical to Claim [1b]. For the reasons discussed in Section X.A.1, Takenaka teaches this limitation, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[8c] a third terminal portion arranged on a side opposed to a display region with respect to the first terminal portion, the third terminal portion having a third group of terminals, the third group of terminals including: a fifth terminal; and a sixth terminal separated from the fifth terminal,*

155. In my opinion, Claim [8c] is similar to Claim [1c], discussed in Section X.A.1. Here, however, a third terminal portion is arranged on a side opposed to a display region with respect to the first terminal portion.

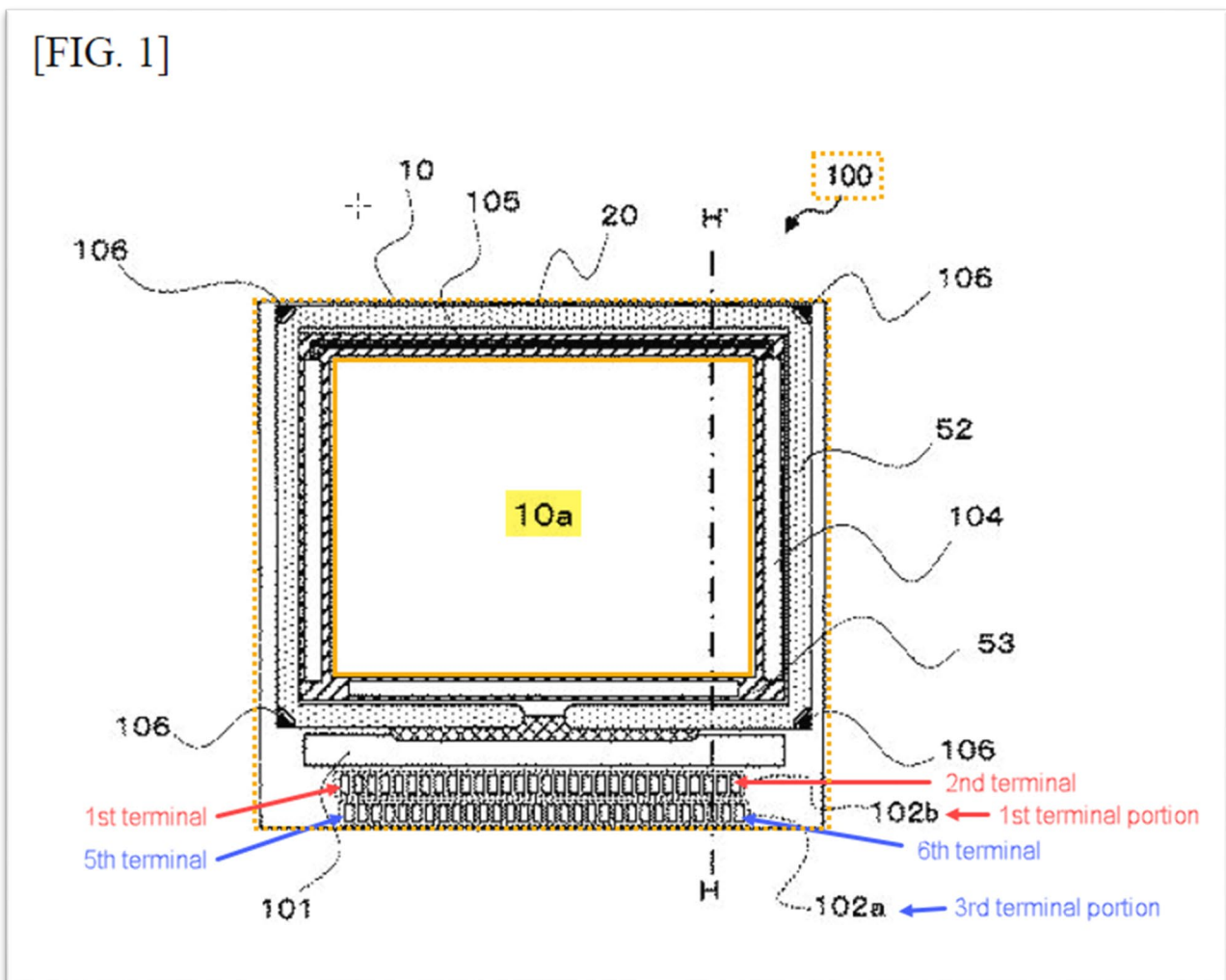
156. A POSITA would understand that Takenaka in view of Ito renders this limitation obvious. As shown in Figure 6, Ito discloses two rows of terminals (102a, 102b) on an electrical-optical panel (100) that has a display region (10a):



(Ito at [0021], [0036], Fig. 6 (annotated).) The display region (10a) is positioned on one side of the first connecting terminals (102b), and the second connecting terminals (102a) are positioned on the other side as the display region. (Ito at [0025], Figs. 1, 4-6.) In other words, the second connecting terminals are arranged on a side opposed to a display region with respect to the first terminal connecting terminals.

157. An additional difference here from Claim [1c] is that the second terminal portion, second group of terminals, third terminal and fourth terminal are

re-labeled as Claim [8c]’s third terminal portion, third terminal group, fifth terminal and sixth terminal, respectively. (*Compare* Claim [8c] *with* Claim [1c].) These limitations are arranged as shown in Figure 1 below:

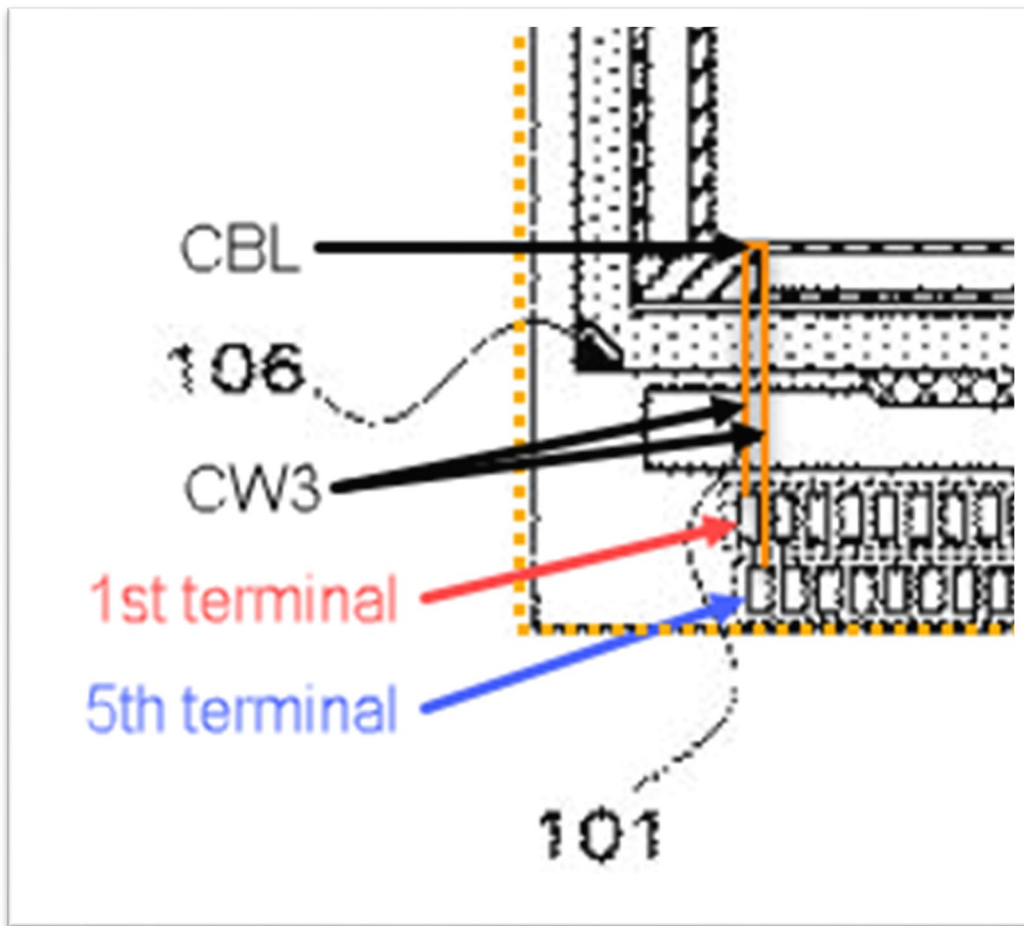


(Ito at Fig. 1 (annotated).) Thus, a POSITA would understand that Takenaka's terminal portions may be configured in Ito's arrangement, each having a group of terminals with two terminals separated from each other. In my opinion, this limitation is met.

*[8d] the first terminal and the fifth terminal being electrically connected through a fifth connection wiring provided on the electro-optical panel,*

158. In my opinion, Claim [8d] is similar to Claim [1d], discussed in Section X.A.1. Here, however, the first terminal is connected to the fifth terminal by a fifth connection wiring.

159. A POSITA would understand that Takenaka in view of Ito renders this limitation obvious. As demonstrated in Sections X.A.1, X.A.5 and X.A.11, Takenaka's LCD panel terminals are electrically connected by connection wiring comprised of some combination of common lines (CW3), and common line (CW10) or common bus line (CBL), for a given arrangement. (Takenaka at Fig. 1. *See also* Claims [1d], [1e], [5e], and [11f]-[11j], *supra*.) The same holds true for the first and fifth terminals, here. As shown in Figure 1 below, the first and fifth terminals, configured in Ito's arrangement, are electrically connected by Takenaka's two common lines (CW3) and a portion of common bus line (CBL):

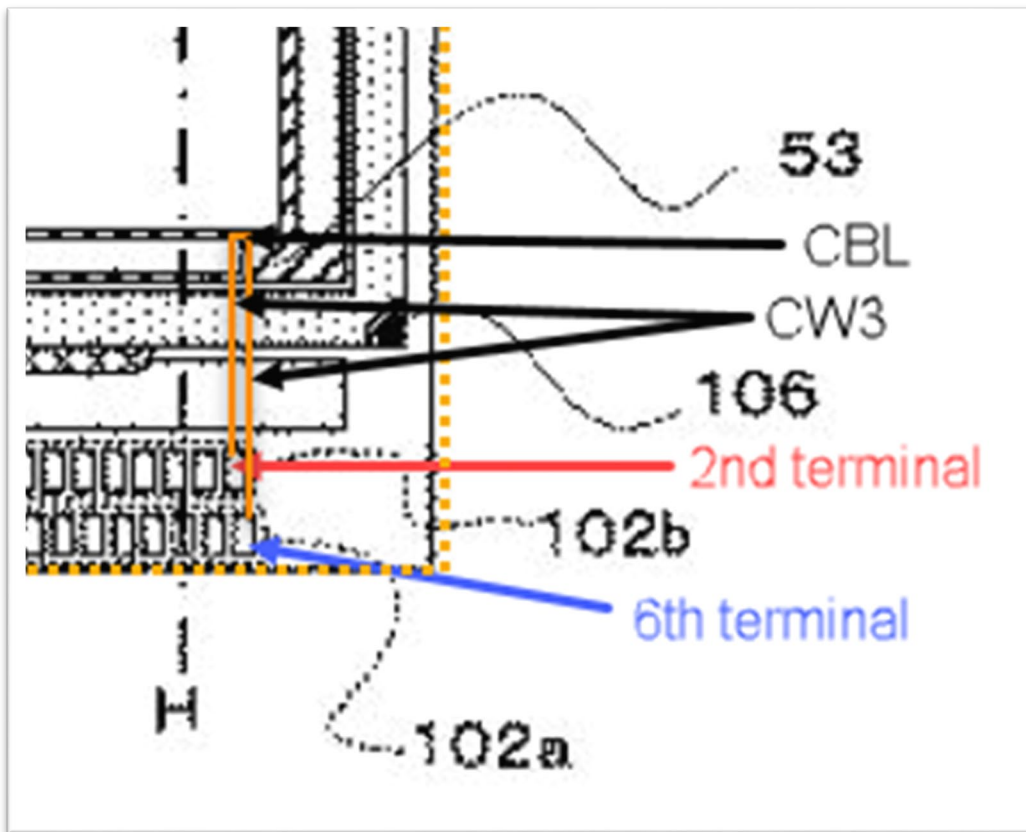


(Ito at Fig. 1 (annotated).) Thus, a POSITA would understand that the first and fifth terminals are electrically connected by a fifth connection wiring provided on the electro-optical panel. In my opinion, this limitation is met.

*[8e] the second terminal and the sixth terminal being electrically connected through a sixth connection wiring provided on the electro-optical panel;*

160. In my opinion, Claim [8e] is similar to Claim [1e], discussed in Section X.A.1. Here, however, the second terminal is connected to the sixth terminal by a sixth connection wiring.

161. A POSITA would understand that Takenaka in view of Ito renders this limitation obvious. As demonstrated in Sections X.A.1, X.A.5 and X.A.11, Takenaka's LCD panel terminals are electrically connected by connection wiring comprised of some combination of common lines (CW3), and common line (CW10) or common bus line (CBL), for a given arrangement. (Takenaka at Fig. 1. *See also* Claims [1d], [1e], [5e], [8d] and [11f]-[11j], *supra.*) The same holds true for the second and sixth terminals, here. As shown in Figure 1 below, the second and sixth terminals, configured in Ito's arrangement, are electrically connected by Takenaka's two common lines (CW3) and a portion of common bus line (CBL):



(Ito at Fig. 1 (annotated).) Thus, a POSITA would understand that the second and sixth terminals are electrically connected by a sixth connection wiring provided on the electro-optical panel. In my opinion, this limitation is met.

*[8f] a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;*

162. In my opinion, Claim [8f] is identical to Claim [1f]. For the reasons discussed in Section X.A.1, Takenaka teaches this limitation. In my opinion, this limitation is met.

*[8g] a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion respectively; and*

163. In my opinion, Claim [8g] is identical to Claim [1g]. For the reasons discussed in Section X.A.1, Takenaka teaches this limitation, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[8h] a third circuit substrate including: a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion;*

164. In my opinion, Claim [8h] is substantially similar to Claim [1h], discussed in Section X.A.1. They differ in that Claim [1h]'s second circuit substrate, second connection terminal portion and second group of connection terminals are relabeled as Claim [8h]'s third circuit substrate, third connection terminal portion and third group of connection terminals, respectively. (*Compare Claim [8h] with Claim [1h].*) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[8i] a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion; and a sixth external terminal electrically connected to the sixth terminal through the third connection terminal portion.*

165. In my opinion, Claim [8i] is substantially similar to Claim [1i], discussed in Section X.A.1. They differ in that Claim [1i]'s third and fourth external

terminals are relabeled as Claim [8i]'s fifth and sixth external terminals, respectively. (*Compare* Claim [8i] *with* Claim [1i].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

#### **9. Dependent Claim 9**

*[9] The electro-optical device according to claim 8, wherein the fifth connection wiring and the sixth connection wiring are provided at an end side of the electro-optical panel rather than the display region.*

166. In my opinion, a POSITA would understand that Takenaka in view of Ito renders this limitation obvious. As shown in Figure 1 below, the fifth and sixth connection wiring are provided at an end side of the LCD panel rather than the display region (10a):

[illegible]

(Ito at Fig. 1 (annotated).) In my opinion, this limitation is met.

## 10. Dependent Claim 10

[10a] The electro-optical device according to claim 8, wherein: each of the first and third group of terminals configures a terminal group arranged in a predetermined direction, and

167. In my opinion, Claim [10a] is substantially similar to Claim [3a], discussed in Section X.A.3. (*Compare* Claim [10a] *with* Claim [3a].) Thus, a

POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

*[10b] the first terminal and the second terminal, and the fifth terminal and the sixth terminal are provided at both end sides of the predetermined direction of the terminal group.*

168. In my opinion, Claim [10b] is substantially similar to Claim [3b], discussed in Section X.A.3. (*Compare* Claim [10b] *with* Claim [3b].) Thus, a POSITA would understand that Takenaka teaches, or at minimum renders this limitation obvious. In my opinion, this limitation is met.

### **C. Ground 3: Claims 1-7 and 13 are Obvious over Takemura**

169. In my opinion, Claims 1-7 and 13 would have been obvious in view of Takemura to a person of ordinary skill at the time of the '020 Patent's filing. Specifically, and as explained in greater detail below, claims 1-7 and 13 recite LCD devices and LCD panels having various configurations of connection wirings, and it would have been obvious for a POSITA to arrive at the claimed configurations in view of Takemura.

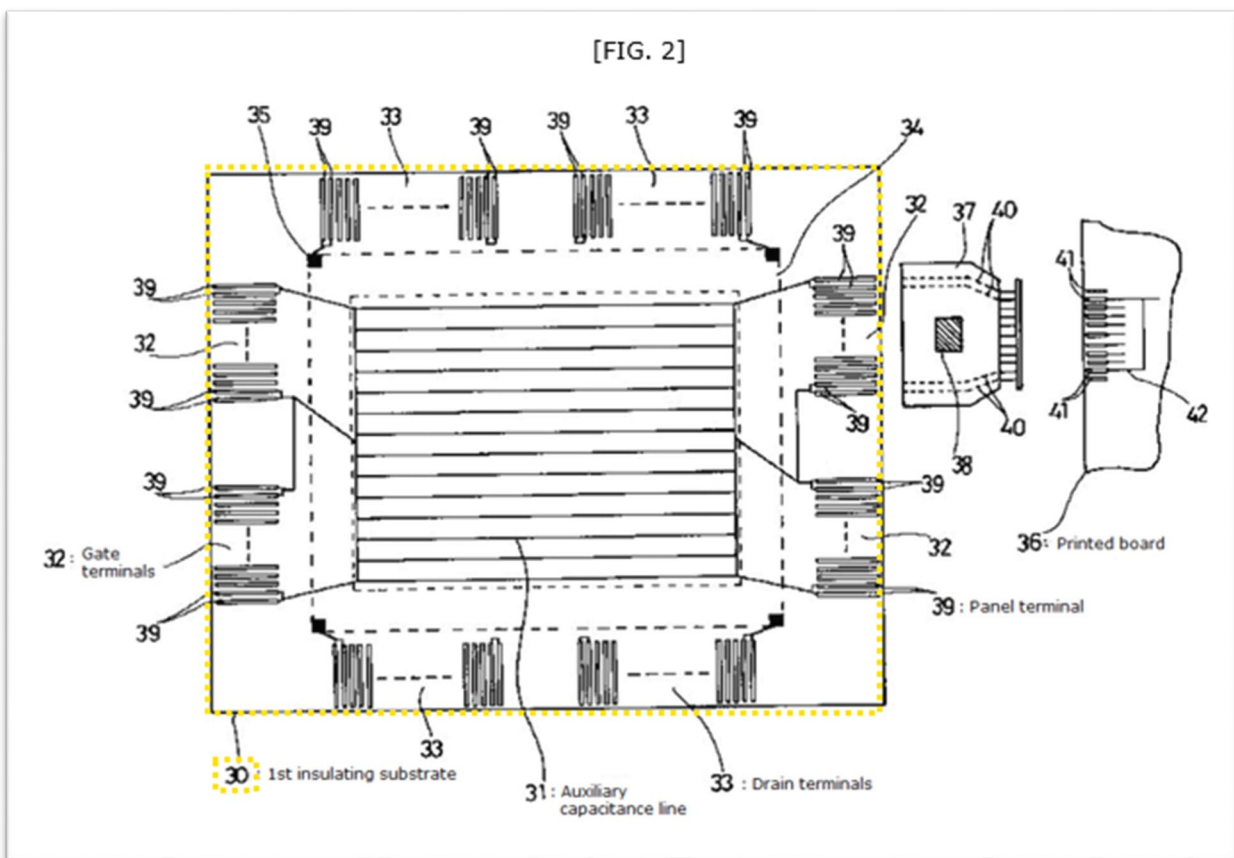
#### **1. Independent Claim 1**

*[1pre] "An electro-optical device comprising:"*

170. In my opinion, to the extent the preamble is limiting, it is taught by Takemura. Takemura discloses a "*liquid crystal display device.*" (Takemura at [0001].) In my opinion, this limitation is met.

[1a] “an electro-optical panel including:”

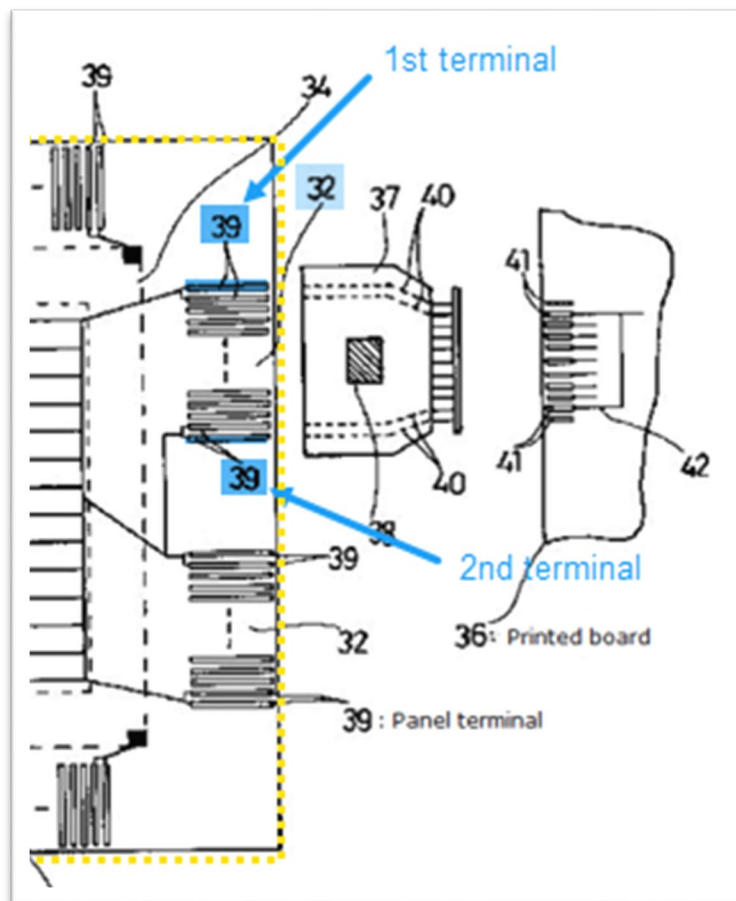
171. In my opinion, Takemura teaches this limitation. Takemura discloses a liquid crystal display device configured with a “*liquid crystal panel.*” (Takemura at [0001].) As shown in Figure 2 below, the LCD panel “is composed of a transparent first insulating substrate (30) and a transparent opposing substrate facing each other, with liquid crystals injected between them.”:



(Takemura at [0021], Fig. 2 (annotated).) In my opinion, this limitation is met.

*[1b] “a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and”*

172. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that a first portion of the LCD panel has “*panel terminals (39) [] provided at both ends of a gate terminal group (32)*”:

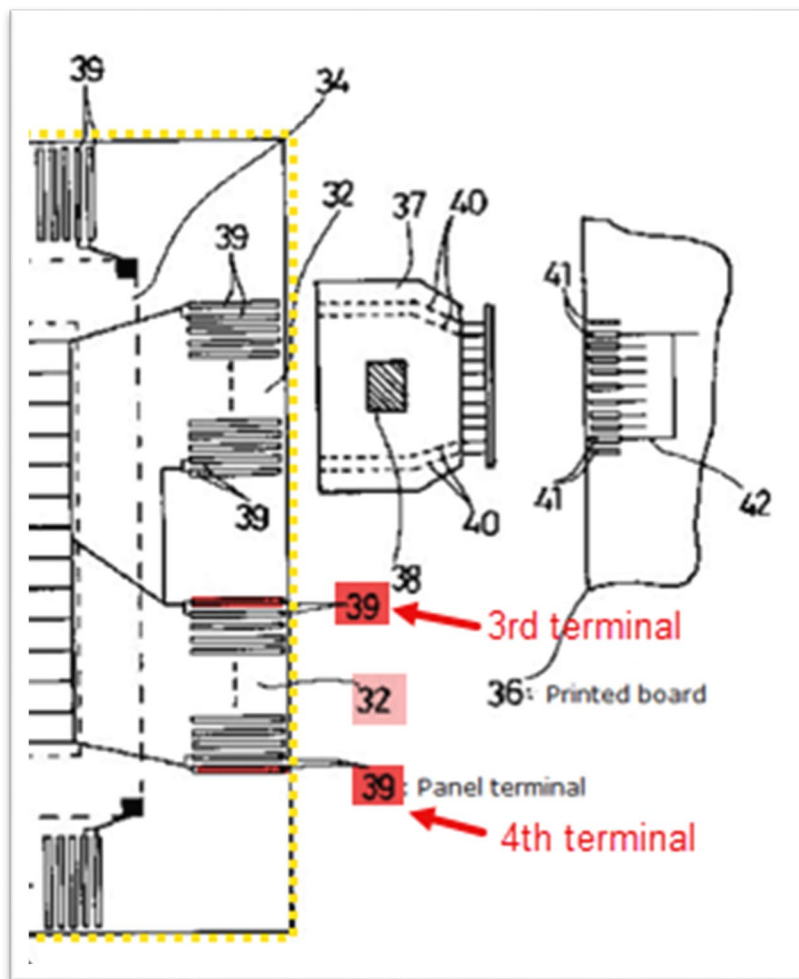


(Takemura at [0029], Fig. 2 (annotated).) In my opinion, this limitation is met.

*[1c] “a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal”*

173. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that a second portion of the LCD panel, adjacent to the

first portion, has “*panel terminals (39) [] provided at both ends of a gate terminal group (32)*”:

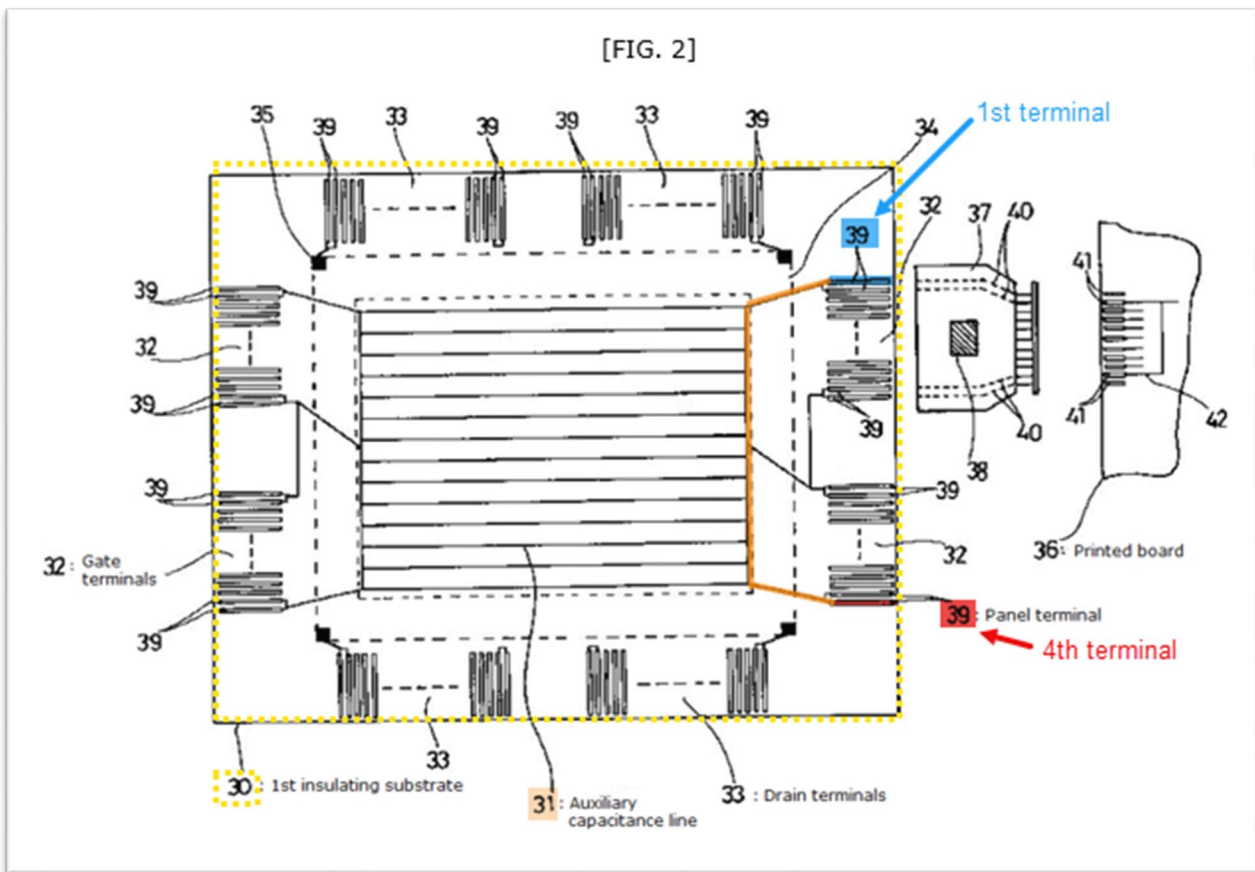


(Takemura at [0029], Fig. 2 (annotated).) In my opinion, this limitation is met.

*[1d] “the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,”*

174. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that the panel terminals may be used to supply a stable voltage to the LCD panel. (Takemura at

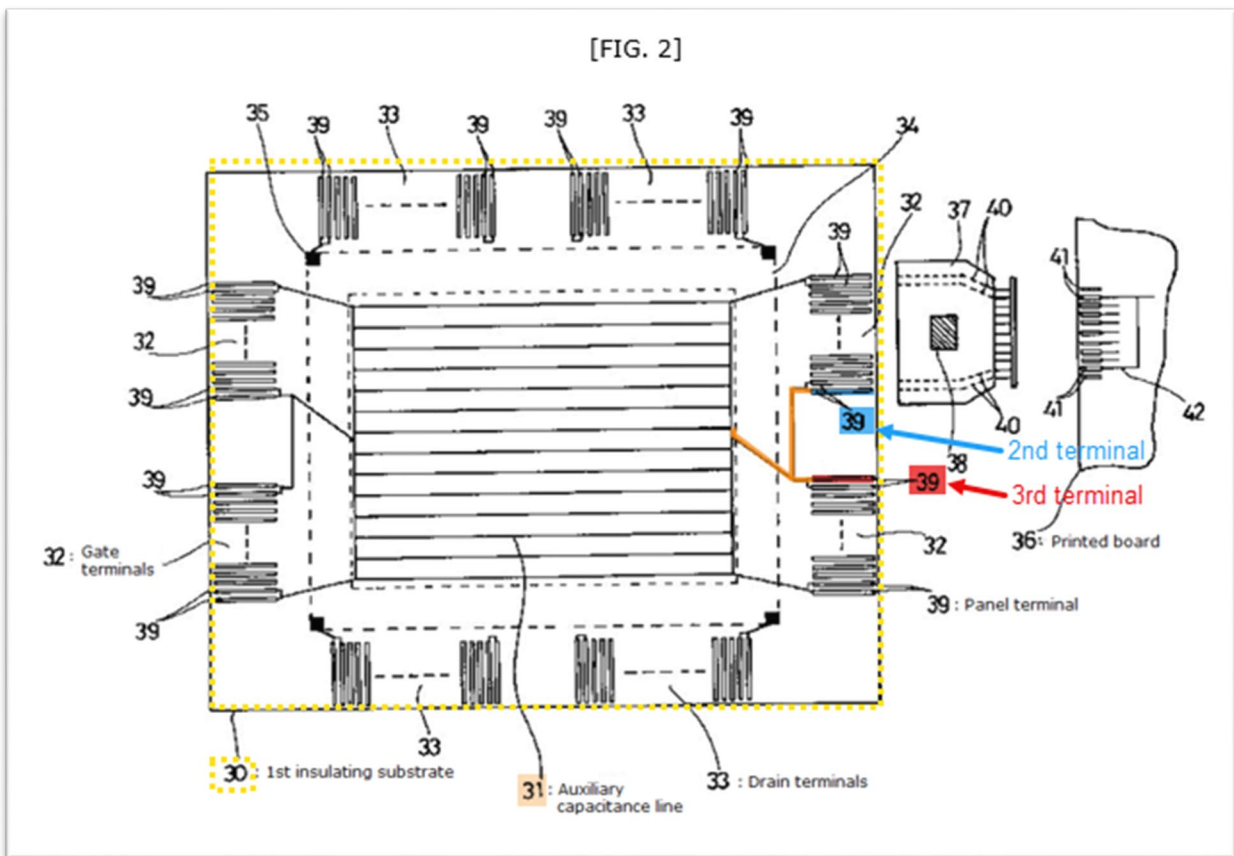
[0031] (“The second aspect of the present invention uses the panel terminals as terminals for auxiliary capacitance[.]”), [0033].) As shown in Figure 2 below, this is accomplished by “contact[ing]” the panel terminals (39), such as the first and fourth terminals to auxiliary capacitance lines (31) on the insulating substrate (30):



(Takemura at [0030] (“[T]he panel terminal on the gate terminal side is in contact with an auxiliary capacitance line[.]”), Fig. 2 (annotated).) A POSITA would understand that the contact with the auxiliary capacitance line is an electrical connection because an auxiliary capacitance signal is supplied. (Takemura at [0029] – [0031], [0033], Fig. 2.) In my opinion, this limitation is met.

[1e] “the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;”

175. Similarly, in my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. As shown in Figure 2 below, second and third panel terminals (39) “contact” auxiliary capacitance lines (31) on the insulating substrate (30):



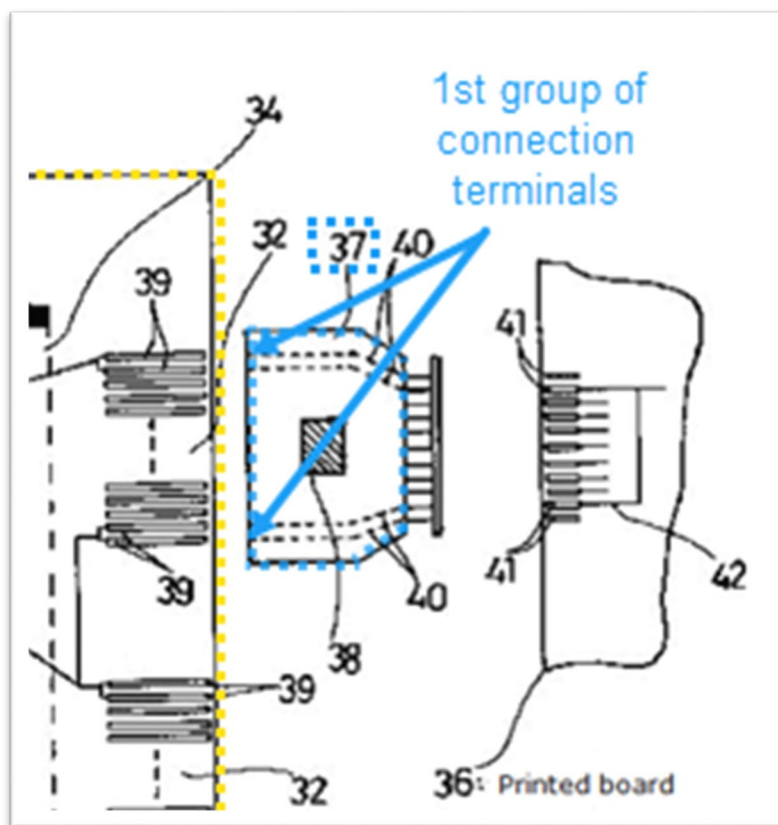
(Takemura at [0030], Fig. 2 (annotated).) A POSITA would understand that the contact with the auxiliary capacitance line is an electrical connection because an

auxiliary capacitance signal is supplied. (Takemura at [0029] – [0031], [0033], Fig.

2.) In my opinion, this limitation is met.

*[1f] “a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;”*

176. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that tape automated bonding (“TAB”) (37) is a flexible substrate between the LCD panel and printed circuit board (36):

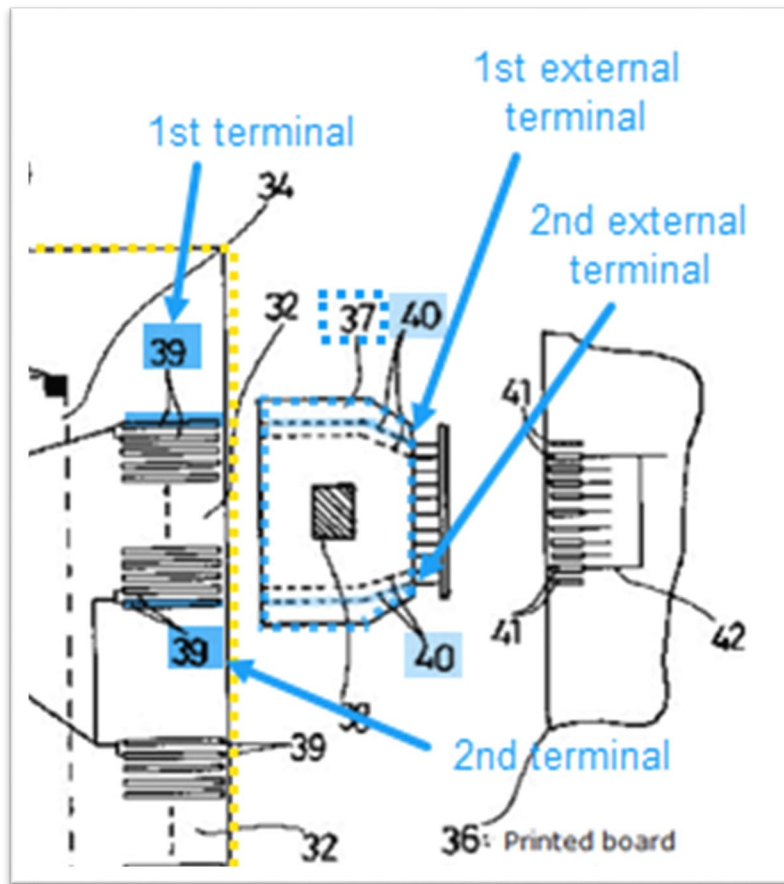


(Takemura at [0013] (“The connecting means is a *flexible substrate*, generally TAB[.]”), [Reference Numbers], Fig. 2 (annotated).) Takemura further discloses

that a group of “terminals (or wiring serving as terminals) are provided on the left . . . side[] of the TAB” and that “panel terminals [(39)] are connected to wiring via left-side terminals of the TAB[.]” (Takemura at [0030], [0017], [0013], [0015], [0029].) In other words, the left side terminals of TAB (37) are a first group of connection terminals in a first connection terminal portion to be electrically connected to the first terminal portion of the LCD panel. In my opinion, this limitation is met.

*[1g] “a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion; and”*

177. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that “terminals (or wiring serving as terminals) are [also] provided on the . . . right side[] of the TAB” and that “panel terminals [(39)] are connected to wiring via left-side terminals of the TAB [(37)], and the right ends of the wiring extend to the right edge of the TAB and are connected to the [right-side] terminals” of TAB (37):



(Takemura at [0013], [0015], [0017], [0029], [0030], Fig. 2 (annotated).) A POSITA would understand that wiring (40) between the left and right-side terminals of the substrate of the TAB (37) may comprise a metal film such as copper. (Takemura at [0029].) In other words, the right-side terminals of the TAB include first and second external terminals which are connected to the first and second panel terminals, respectively, through the first connection terminal portion. In my opinion, this limitation is met.

*[1h] “a second circuit substrate including: a second connection terminal portion having a second group of*

*connection terminals to be electrically connected to the second terminal portion;”*

178. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that “**two TABs (37)** like the one shown in FIG. 2 ***may be provided on each side edge***” of the LCD panel (Takemura at [0028].) Thus, a POSITA would understand that the second TAB is structured similarly to the first TAB such that a second circuit substrate includes a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion. (See Claim [1f], *supra*.) In my opinion, this limitation is met.

*[1i] “a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.”*

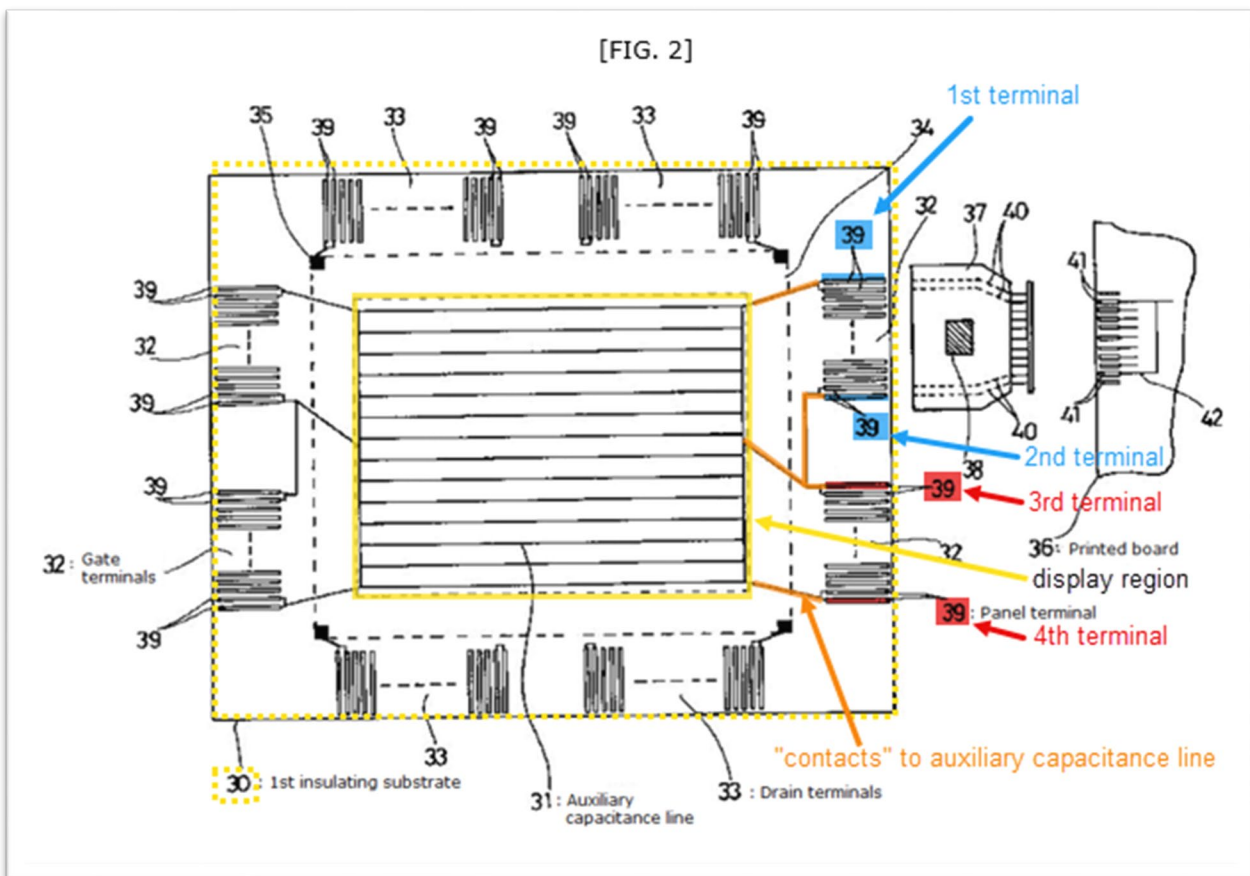
179. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that the LCD panel is connected to two TABs. (Takemura at [0028].) Thus, a POSITA would understand that the second TAB is structured similarly to the first TAB such that the second circuit substrate includes a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second

connection terminal portion. (See Claim [1g], *supra*.) In my opinion, this limitation is met.

## 2. Dependent Claim 2

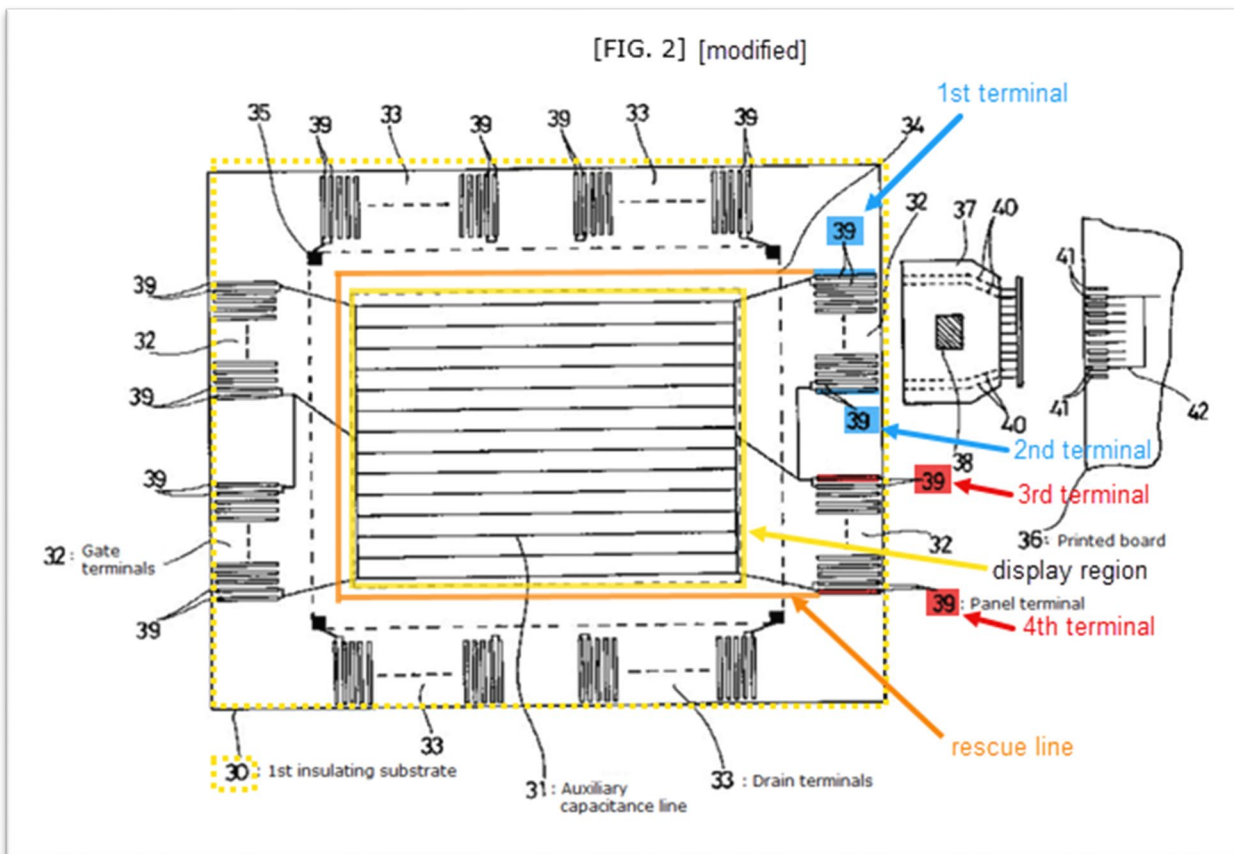
*The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.*

180. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. As shown in Figure 2 below, Takemura discloses that a portion of the panel terminals' (39) "contacts" to auxiliary capacitance line (31) extends around the circumference of the display region:



(Takemura at [0014], [0029] – [0031], [0033], Fig. 2 (annotated). *See also* Claim 1[e], *supra*.)

181. Alternatively, Takemura discloses that the panel terminals may be used as rescue terminals that are “in contact with *a rescue line extending around the display region.*” (Takemura at [0033].) In this case, the rescue line takes the place of the “contacts” to auxiliary capacitance line (31), as shown in modified Figure 2 below:



(Takemura at [0033], Fig. 2 (modified) (annotated).) Thus, Takemura teaches, or at minimum renders obvious the electro-optical device according to claim 1, wherein

some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region. In my opinion, this limitation is met.

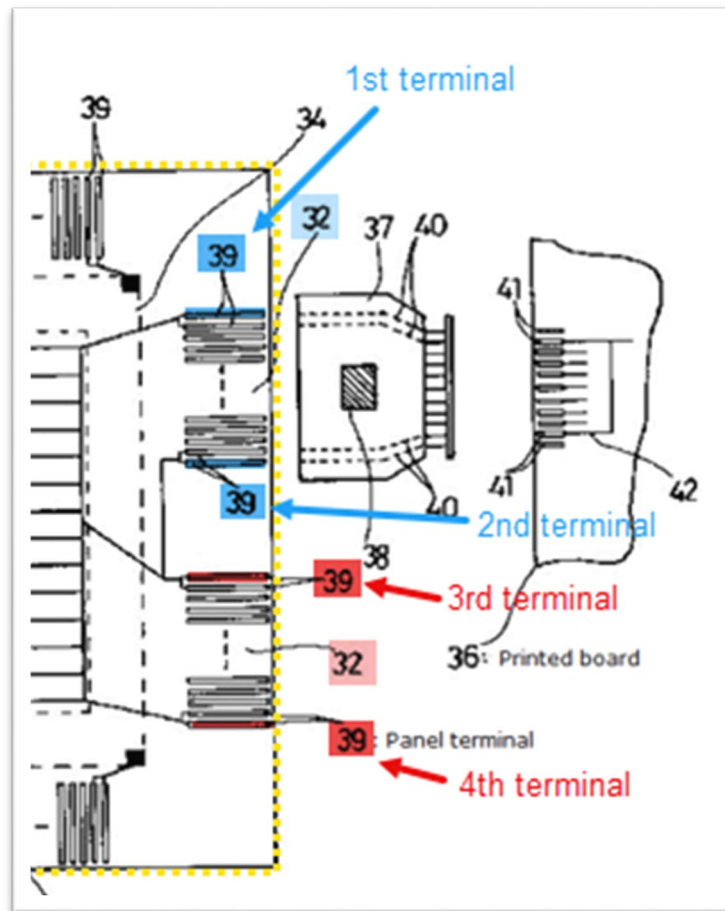
### 3. Dependent Claim 3

*[3a] The electro-optical device according to claim 1, wherein: each of the first and second group of terminals configures a terminal group arranged in a predetermined direction, and*

182. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that the first and second groups of terminals are fixed on the LCD panel. (Takemura at [0028], Fig. 2. *See also* Claims [1b], [1c].) As such, the order of the terminals within a terminal group does not change, e.g., the first terminal is always above the second terminal. Accordingly, a POSITA would understand that the terminal groups are arranged in a predetermined direction. In my opinion, this limitation is met.

*[3b] the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.*

183. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that the “*panel terminals (39) are provided at both ends of a gate terminal group (32)*”:

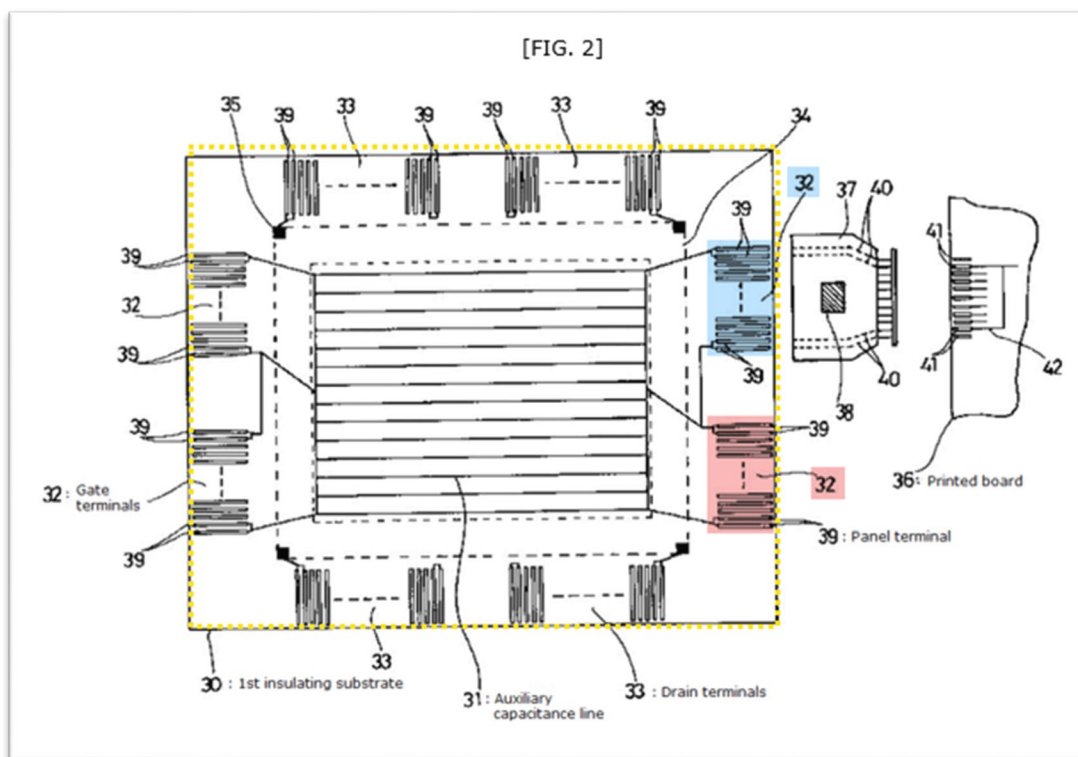


(Takemura at [0029], Fig. 2 (annotated).) In my opinion, this limitation is met.

#### 4. Dependent Claim 4

*[4] The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.*

184. In my opinion, Takemura teaches this limitation. As shown in Figure 2 below, Takemura discloses that the first and second terminal portions, indicated by the first and second terminal groups, respectively, are provided along the right side of the LCD panel:

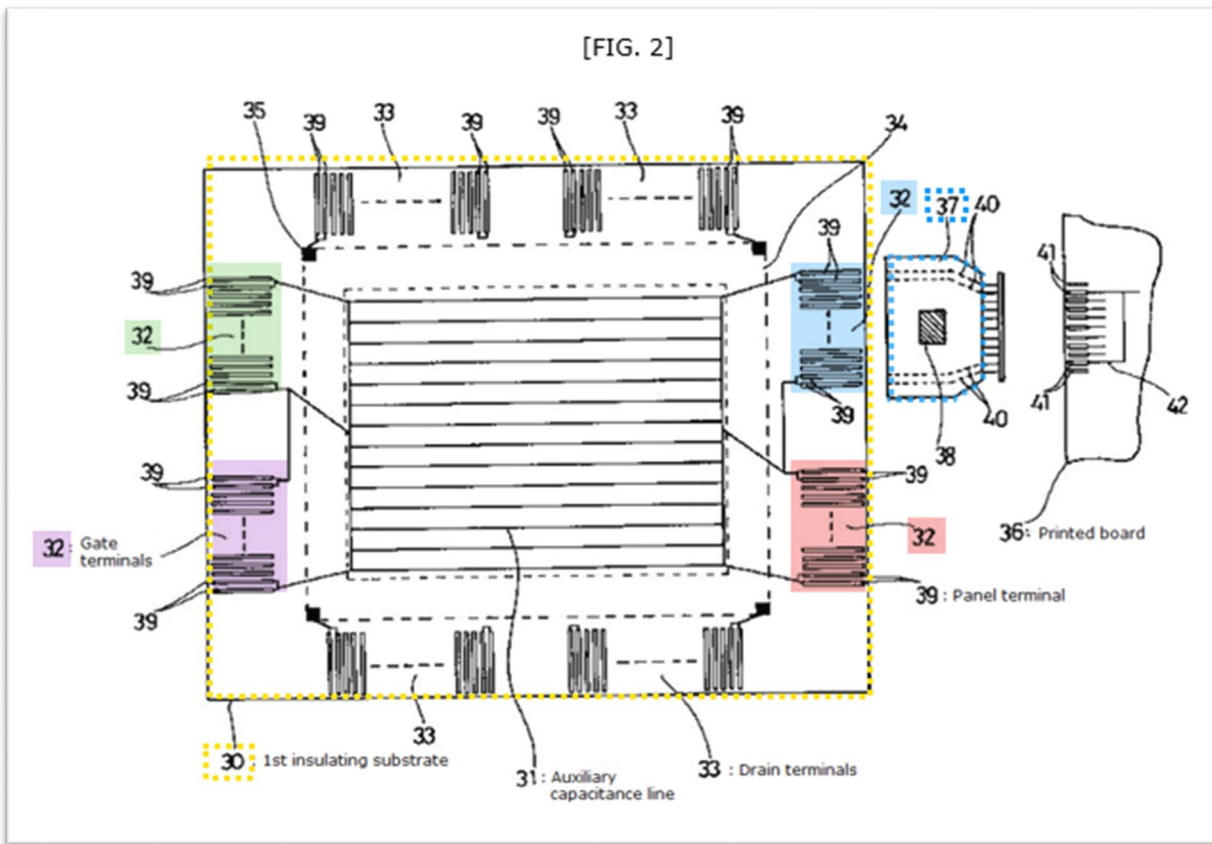


(Takemura at Fig. 2 (annotated).) The left side of the panel is a second side of a direction crossing the right side of the panel. In my opinion, this limitation is met.

## 5. Dependent Claim 5

[5a] The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a fourth terminal portion having a fourth group of terminals arranged so as to be adjacent to the third terminal portion,

185. In my opinion, Takemura teaches this limitation. As shown in Figure 2, Takemura discloses four portions of the LCD panel, each with a terminal group (32):



(Takemura at [0014], [0021], Fig. 2 (annotated).) The third and fourth terminal portions with third and fourth groups of terminals, respectively, are adjacent to each other on the left side of the LCD panel. In my opinion, this limitation is met.

*[5b] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,*

186. In my opinion, Takemura teaches this limitation. Takemura discloses that “*two TABs (37) like the one shown in FIG. 2 may be provided on each side*

*edge.*” (Takemura at [0028].) The TABs are similar in structure and are similarly electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0028]. *See also* Claim [1f], [1h], *supra.*) Thus, Takemura discloses third and fourth flexible substrates, provided on the left side of the LCD panel, the third substrate including a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion, and the fourth substrate including a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion. In my opinion, this limitation is met.

*[5c] the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel,*

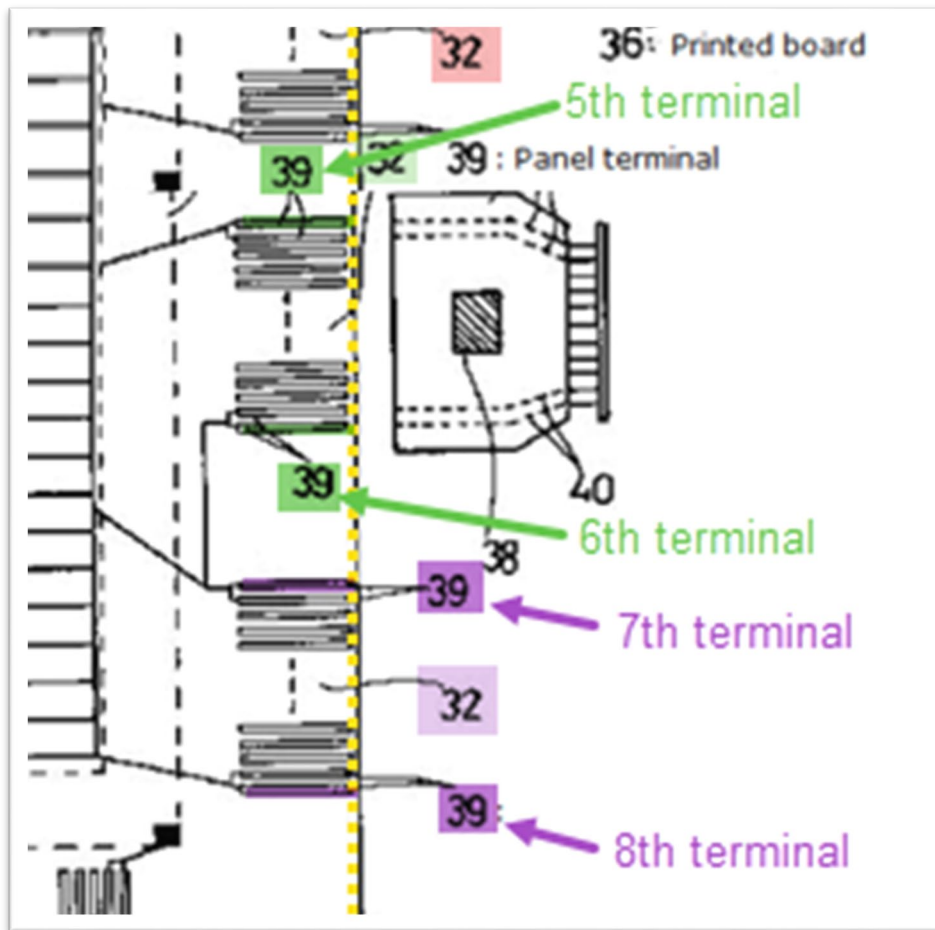
187. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that the number of TABs provided on any side of the LCD panel “is not limited, and one [TAB] may be provided on each side edge, *or three or more may be provided on each side edge.*” (Takemura at [0028].) In the case where four TABs are provided on the right side of the LCD panel, a POSITA would understand that there are also four corresponding terminal portions and groups of terminals that are electrically



(Takemura at Fig. 2 (modified) (annotated).) The third and fourth terminal portions and third and fourth groups of terminals remain adjacent to each. Moreover, the TABs are similar in structure and are similarly electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0028].) Thus, a POSITA would understand that, in this arrangement, the third terminal portion is provided between the first terminal portion and an end of the LCD panel, and the fourth terminal portion is provided between the second terminal portion and an end of the electro-optical panel. In my opinion, this limitation is met.

*[5d] the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and*

189. In my opinion, Takemura teaches this limitation. Each of the terminal groups are structurally similar. (Takemura at [0014], [0021], [0029], Fig. 2. *See also* Claim 1[b], 1[c], [5a], *supra*.) Thus, Takenaka discloses that the third group of terminals has fifth and sixth terminals separated from each other, and the fourth group of terminals has seventh and eighth terminals separated from each other, as shown in modified Figure 2 below:

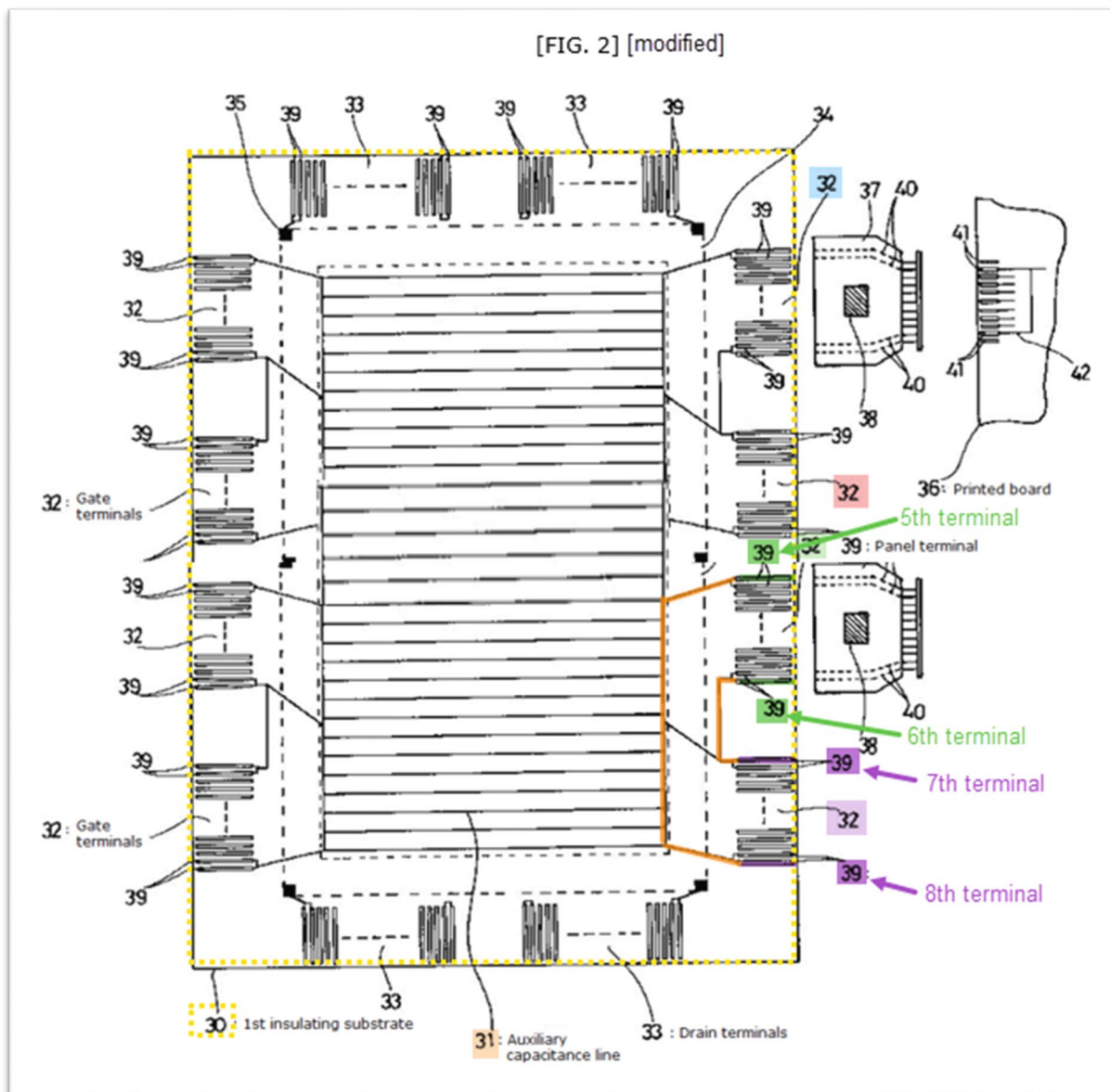


(Takemura at [0029], Fig. 2 (modified) (annotated).) In my opinion, this limitation is met.

*[5e] the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,*

190. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. The first and second, and third and fourth terminal groups, are similar in how their respective panel terminals “contact”

the auxiliary capacitance lines on the LCD panel, as shown in modified Figure 2 below:

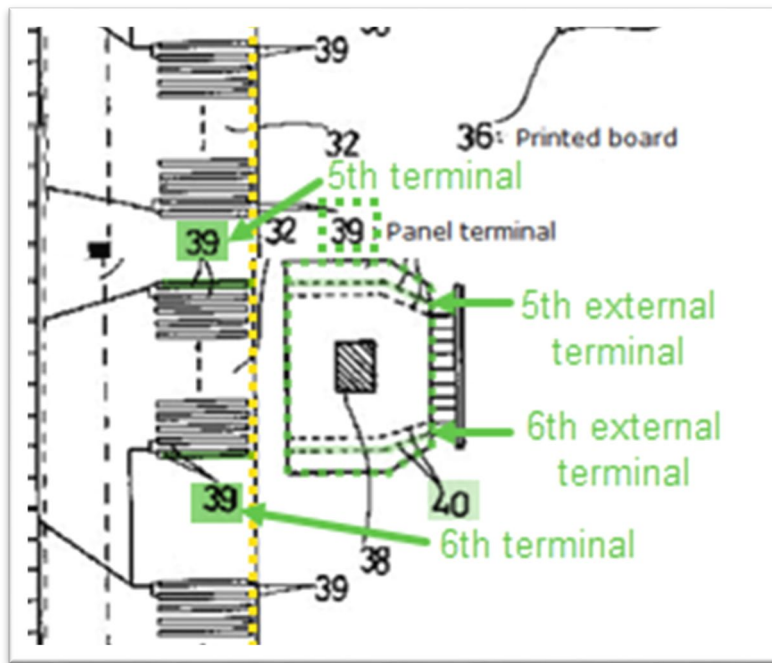


(Takemura at [0014], [0021], [0029]–[0031], [0033], Fig. 2 (modified) (annotated).  
*See also* Claim [1d], [1e], *supra*.) Accordingly, a POSITA would understand that  
the fifth terminal and the eighth terminal, and the sixth terminal and the seventh

terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively. In my opinion, this limitation is met.

*[5f] the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and*

191. In my opinion, Takemura teaches this limitation. The TABs are similar in structure and are similarly electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0013], [0015], [0017], [0028]-[0030]. *See also* Claims [1g], [1i], [5b], [5d], *supra*.) Thus, Takemura discloses that the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, as shown in modified Figure 2 below:



(Takemura at Figure 2 (modified) (annotated).) In my opinion, this limitation is met.

*[5g] the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.*

192. Similarly, in my opinion, Takemura teaches this limitation. The TABs are similar in structure and are similarly electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0013], [0015], [0017], [0028]-[0030]. *See also* Claims [1g], [1i], [5b], [5d], *supra*.) Thus, Takemura discloses that the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and

an eighth external terminal electrically connected to the eighth terminal. In my opinion, this limitation is met.

## 6. Dependent Claim 6

*[6] The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.*

193. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Takemura discloses that panel terminals may be used as “rescue terminals,” as an alternative to being used to supply signals to the auxiliary capacitance line. (Takemura at [0033].) In this case, Takemura discloses that “rescue terminals will be in contact with a ***rescue line extending around the display region.***” (Takemura at [0033].) Accordingly, a POSITA would find obvious that the third connection wiring electrically connecting the fifth and eighth terminals may comprise a rescue line extended around the circumference of the display region, as shown in modified Figure 2 below:

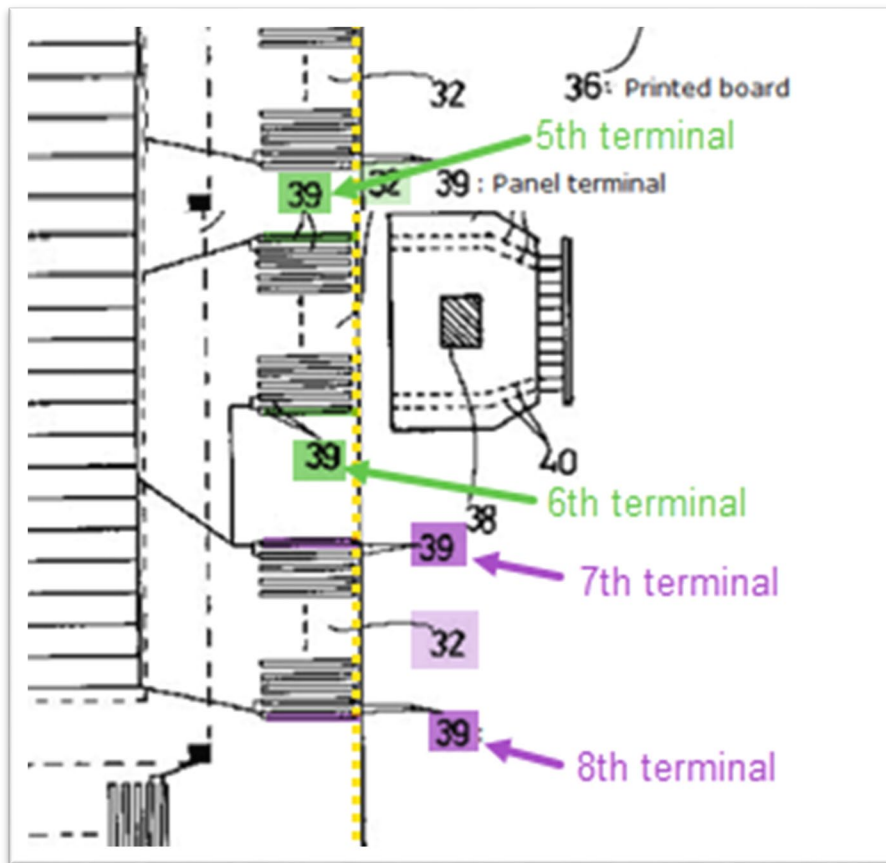


*configures a terminal group arranged in a predetermined direction, and*

194. In my opinion, a POSITA would understand that Takemura teaches, or at minimum renders this limitation obvious. Similarly to the first and second groups of terminals, Takemura discloses that the third and fourth groups of terminals are fixed on the LCD panel. (Takemura at [0028]. *See also* Claims [1b], [1c], [3a], *supra*.) As such, the order of the terminals within a terminal group does not change, e.g., the fifth and seventh terminals are always above the sixth and eighth terminals, respectively. Accordingly, a POSITA would understand that the terminal groups are arranged in a predetermined direction. In my opinion, this limitation is met.

*[7b] the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.*

195. In my opinion, Takemura teaches this limitation. As shown in modified Figure 2 below, similarly to the first through fourth terminals, Takemura discloses that the fifth and sixth, and seventh and eighth “***panel terminals (39) are provided at both ends of a gate terminal group (32)***”:



(Takemura at [0029], Fig. 2 (modified) (annotated).) In my opinion, this limitation is met.

### 13. Dependent Claim 13

*[13] An electronic apparatus comprising the electro-optical device according to claim 1.*

196. In my opinion, Takemura teaches this limitation. Takemura discloses that the LCD device may be incorporated into an LCD projector. (Takemura at [0027] (“[P]rinted circuit board (36) is hollow in the center for use in an LCD projector.”).) In my opinion, this limitation is met.

## **XI. CONCLUSION**

197. For the reasons discussed in detail above, it is my opinion that claims 1-13 of the '020 Patent are invalid in view of the prior art.

198. The findings and opinions set forth in this Declaration are based on my work and analysis to date. I may continue my analysis. I may also receive additional documentation and other factual evidence over the course of this proceeding that will allow me to supplement and/or refine my opinions. I reserve the right to add to, alter, or delete my opinions and my Declaration upon discovery of any additional information. I also reserve the right to make such changes as may be deemed necessary.

199. In signing this Declaration, I recognize that it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

# **Appendix 1**

## **(Curriculum Vitae)**



**Exponent<sup>®</sup>**  
Engineering & Scientific Consulting

**Patrick Murphy, Ph.D., P.E., CFEI**

Principal Engineer | Electrical Engineering and Computer Science  
New York  
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## Professional Profile

Dr. Murphy applies his expertise in electrical engineering to lead investigations into the performance, design, and condition of electrical and electronic systems and devices. He has experience with range of technologies found in consumer electronics and appliances, medical devices, and electric power systems.

Dr. Murphy has inspected and tested smart home products and smart building installations, and has published and presented on issues in networked building controls and the safety and security of Internet-of-Things products. He has investigated a number of property losses related to fires and water damage in electrical and electronic equipment including losses related to extreme weather events. Dr. Murphy is a licensed electrical engineer and has over 10 years of experience preparing technical reports to inform clients engaged in risk analysis, regulatory matters, and dispute resolution proceedings.

Dr. Murphy has experience in design and manufacture of semiconductor devices and optoelectronic technologies for lighting, displays, and sensing at the component level and as part of systems for professional audio, automated building management, and consumer electronics and appliances. As part of technical investigations, Dr. Murphy has instrumented and measured per relevant standards electrical power quality, utility-frequency and radio-frequency electromagnetic fields, and optical and acoustic energy.

Dr. Murphy has experience analyzing failures and damage to equipment, cables, insulators, and systems for electric power distribution, rail transportation systems, and solar energy. As part of this work he has measured power quality and electrical equipment performance in the field, examined and tested electrical cables, insulators, and equipment in the laboratory, and reviewed system designs for compliance with industry standards.

Dr. Murphy's research experience focused on semiconductor integrated circuit fabrication technologies including nanoimprint, optical lithography and pulsed laser processing, as well as design, fabrication, and characterization of optical filters, waveguides, photodetectors, nanowires and solar cells. Dr. Murphy has university-level experience teaching topics in electrical and computer engineering, applied physics, semiconductor devices, and optics.

## Academic Credentials & Professional Honors

Ph.D., Electrical Engineering, Princeton University, 2009

M.A., Electrical Engineering, Princeton University, 2004

B.S., Electrical Engineering, Boston University, 2002

Richard Ralston Hough Award for Distinguished Teaching, Princeton University Department of Electrical Engineering

Graduate Student Teaching Award, Association of Princeton Graduate Alumni

Commendation for Outstanding Teaching, Princeton University School of Engineering and Applied Science

McGraw Graduate Fellow, Princeton University

## Licenses and Certifications

Professional Engineer Electrical, California, #20317

Professional Engineer, New York, #104358

Certified Fire and Explosion Investigator (CFEI)

## Prior Experience

Research Assistant, Nanostructures Laboratory, Princeton University, 2003-2009

Research Assistant, Optical Characterization and Nanophotonics Laboratory, Boston University, 2001-2002

Research Assistant, Spire Corporation, 1999-2001

## Professional Affiliations

Institute of Electronics and Electrical Engineers (IEEE, Senior Member)

National Association of Fire Investigators

## Publications

D'Andrade B, Lenox K, Murphy, PF. "Internet of Things Risks." In Software Engineering: Artificial Intelligence, Compliance, and Security. D'Andrade B (ed), Nova Science Publishers, 2021.

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