

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

PTAB Case No. IPR 2025-01412

Patent No. 8,391,020

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,391,020
CHALLENGING CLAIMS 1-13**

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EXHIBIT LIST

Exhibit No	Document
Ex. 1001	U.S. Patent No. 8,391,020 (“ ’020 Patent ”)
Ex. 1002	Declaration and Curriculum Vitae of Dr. Patrick Murphy (“ Murphy ”)
Ex. 1003	File history of the ’020 Patent
Ex. 1004	U.S. Patent Application Publication No. 2008/0291379 (“ Takenaka ”)
Ex. 1005	Japanese Patent Application Publication No. 2009168877A & Certified Translation (“ Ito ”)
Ex. 1006	Japanese Patent Application Publication No. H0643473A & Certified Translation (“ Takemura ”)
Ex. 1007	den Boer, W., Active Matrix Liquid Crystal Displays (2005) (“ den Boer ”)
Ex. 1008	Chen, C.-I. et al., “Bondability Study of Chip-on-Film (COF) Inner Lead Bonding (ILB) Using Conventional Gang Bonder,” IEEE Transactions on Electronics Packaging Manufacturing, Vol. 31, No. 4, p. 285-90 (October 2008) (“ Chen ”)
Ex. 1009	Watanabe, I. et al., “19.1: Invited Paper: Driver IC Packaging Technologies Using Anisotropic Conductive Films in Flat Panel Display,” SID Symposium Digest of Technical Papers, Vol. 39, p. 240-43 (2008) (“ Watanabe ”)
Ex. 1010	Govaerts, J. et al., “Interconnecting drivers to flexible displays,” Journal of the Society for Information Display, Vol. 16, No. 7, p. 765-775 (2008) (“ Govaerts ”)
Ex. 1011	U.S. Patent Application Publication No. 2010/0321623 (“ Wakita ”)
Ex. 1012	U.S. Patent Application Publication No. 2011/0175800 (“ Mizumaki ”)

Exhibit No	Document
Ex. 1013	Minami, H. et al., “Prospects of LCD Panel Fabrication and Inspection Equipment Amid Growing Demand for Increased Size,” Hitachi Review, Vol. 56, No. 3, p. 63-69 (2007) (“ Minami ”)
Ex. 1014	Souk, J. et al., Flat Panel Display Manufacturing (2018) (“ Souk ”)
Ex. 1015	Ni, G. et al., “Automated optical inspection of liquid crystal display anisotropic conductive film bonding,” Optical Engineering, Vol. 55, No. 10, 103109-1 - 8 (October 2016) (“ Ni ”)
Ex. 1016	Li, T. et al., “A Novel Method for LCD Module Alignment and Particle Detection in Anisotropic Conductive Film Bonding,” Machines, Vol. 11, No. 49, p. 1-19 (2023) (“ Li ”)
Ex. 1017	Murakami, T. et al., “Electrostatic problems and ionization solutions in TFT-LCD production,” Solid State Technology, Vol. 40, No. 1 (January 1997) (“ Murakami ”)
Ex. 1018	U.S. Patent No. 5,737,272 (“ Uchiyama ”)

CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1pre]	An electro-optical device comprising:
	[1a]	an electro-optical panel including:
	[1b]	a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and
	[1c]	a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal
	[1d]	the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,
	[1e]	the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;
	[1f]	a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;
	[1g]	a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion; and
	[1h]	a second circuit substrate including: a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion;

Claim	Limitation No.	Limitation
	[1i]	a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.
2		The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.
3	[3a]	The electro-optical device according to claim 1, wherein: each of the first and second group of terminals configures a terminal group arranged in a predetermined direction, and
	[3b]	the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.
4		The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.
5	[5a]	The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a fourth terminal portion having a fourth group of terminals arranged so as to be adjacent to the third terminal portion,
	[5b]	a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on

Claim	Limitation No.	Limitation
		which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,
	[5c]	the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel,
	[5d]	the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and
	[5e]	the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,
	[5f]	the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and
	[5g]	the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.
6		The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.
7	[7a]	The electro-optical device according to claim 5, wherein: each of the third and fourth group of terminals configures

Claim	Limitation No.	Limitation
		a terminal group arranged in a predetermined direction, and
	[7b]	the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.
8	[8pre]	An electro-optical device comprising:
	[8a]	an electro-optical panel including:
	[8b]	a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and
	[8c]	a third terminal portion arranged on a side opposed to a display region with respect to the first terminal portion, the third terminal portion having a third group of terminals, the third group of terminals including: a fifth terminal; and a sixth terminal separated from the fifth terminal,
	[8d]	the first terminal and the fifth terminal being electrically connected through a fifth connection wiring provided on the electro-optical panel,
	[8e]	the second terminal and the sixth terminal being electrically connected through a sixth connection wiring provided on the electro-optical panel;
	[8f]	a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;
	[8g]	a first external terminal connected to the first terminal through the first connection terminal portion; and a

Claim	Limitation No.	Limitation
		second external terminal connected to the second terminal through the first connection terminal portion respectively; and
	[8h]	a third circuit substrate including: a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion;
	[8i]	a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion; and a sixth external terminal electrically connected to the sixth terminal through the third connection terminal portion.
9		The electro-optical device according to claim 8, wherein the fifth connection wiring and the sixth connection wiring are provided at an end side of the electro-optical panel rather than the display region.
10	[10a]	The electro-optical device according to claim 8, wherein: each of the first and third group of terminals configures a terminal group arranged in a predetermined direction, and
	[10b]	the first terminal and the second terminal, and the fifth terminal and the sixth terminal are provided at both end sides of the predetermined direction of the terminal group.
11	[11pre]	An electro-optical panel comprising:
	[11a]	a substrate;
	[11b]	a first terminal portion including a first group of terminals having a first terminal and a second terminal separated from each other;

Claim	Limitation No.	Limitation
	[11c]	a second terminal portion arranged adjacent to the first terminal portion, the second terminal portion including a second group of terminals having a third terminal and a fourth terminal separated from each other;
	[11d]	a third terminal portion arranged between one side of the substrate and the first terminal portion, the third terminal portion including a third group of terminals having a fifth terminal and a sixth terminal separated from each other;
	[11e]	a fourth terminal portion arranged between one side of the substrate and the second terminal portion, the fourth terminal portion including a fourth group of terminals having a seventh terminal and a eighth terminal separated from each other;
	[11f]	a first connection wiring configured to electrically connect the first terminal and the fourth terminal;
	[11g]	a fifth connection wiring configured to electrically connect the first terminal and the fifth terminal;
	[11h]	a sixth connection wiring configured to electrically connect the second terminal and the sixth terminal;
	[11i]	a seventh connection wiring configured to electrically connect the third terminal and the seventh terminal;
	[11j]	an eighth connection wiring configured to electrically connect the fourth terminal and the eighth terminal; and
	[11k]	a ninth connection wiring configured to electrically connect the sixth connection wiring and the seventh connection wiring so as to electrically connect the second terminal, the third terminal, the sixth terminal and the seventh terminal.

Claim	Limitation No.	Limitation
12	[12a]	An electro-optical device comprising: the electro-optical panel according to claim 11;
	[12b]	a first circuit substrate on which a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion is provided and
	[12c]	which has a first external terminal connected to the first terminal through the first connection terminal portion and a second external terminal connected to the second terminal;
	[12d]	a second circuit substrate on which a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion is provided and
	[12e]	which has a third external terminal connected to the third terminal through the second connection terminal portion and a fourth external terminal connected to the fourth terminal;
	[12f]	a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided and
	[12g]	which has a fifth external terminal connected to the fifth terminal through the third connection terminal portion and a sixth external terminal connected to the sixth terminal; and
	[12h]	a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided and

Claim	Limitation No.	Limitation
	[12i]	which has a seventh external terminal connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal connected to the eighth terminal.
13		An electronic apparatus comprising the electro-optical device according to claim 1.

Petitioner BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”) respectfully requests *inter partes* review of claims 1-13 (the “Challenged Claims”) of U.S. Patent No. 8,391,020 (“’020 Patent”) in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’020 Patent’s alleged invention is simple—it is a means to check the electrical connections between a liquid-crystal display (“LCD”) panel and flexible substrates. Specifically, an LCD device typically comprises an LCD panel, a driving circuitry that can be external to the LCD panel to drive the pixels of an LCD panel, and flexible substrates to bridge between the LCD panel and external circuitry. Terminals on the flexible substrates must thus be electrically connected to corresponding terminals on the LCD panel and electrical driving circuit. The ’020 Patent describes a way to check the electrical connections between the LCD panel and the flexible substrates from the terminals on the external driving circuit-end of the flexible substrate. This is simply achieved by providing wirings in various configurations on the LCD panel that interconnect the LCD panel’s terminals. However, by the time the ’020 Patent’s priority applications were filed, wirings in these specific configurations were already well-known.

Not only were these wirings well-known, they were publicly disclosed more than one year before the earliest priority date of the ’020 Patent. These disclosures

should have been cited during the prosecution of the '020 Patent, but the Examiner did not cite any prior art or issue any Office Actions. The '020 Patent received a first action allowance.

This Petition and the associated exhibits establish that the Challenged Claims are invalid under 35 U.S.C. § 103(a) (pre-AIA) that the '020 Patent should have never issued.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner BOE is the sole real party-in-interest for this Petition.

B. Related Matters

Patent Owner 138 East LCD Advancements Limited and its purported exclusive licensee Longitude Licensing Limited (collectively, “Patent Owner” or “138 East LCD”) asserted, in two separate district court cases, that BOE infringes at least claims 1, 2 and 11-13 of the '020 Patent and infringes certain claims of U.S. Patent Nos. 8,319,512 and 7,636,146: *Longitude Licensing Limited v. BOE Technology Group Co. Ltd.*, No. 2:25-cv-440 (E.D. Tex.) and *Longitude Licensing Limited v. BOE Technology Group Co. Ltd.*, No 2:25-cv-358 (E.D. Tex.). In Case No. 2:25-cv-440, 138 East LCD also sued LG Electronics, Inc., which allegedly sells TVs incorporating BOE LCD panels. In Case No. 2:25-cv-358, 138 East LCD also sued Hisense Group Holdings Co. Ltd. and Hisense Visual Technology Co., Ltd. (collectively, “Hisense”), which allegedly sell TVs incorporating BOE LCD panels.

Finally, Petitioner is also filing petitions for *inter partes* review challenging two other patents also asserted in the above-listed litigations, U.S. Patent No. 7,636,146 (in IPR 2025-01396) and U.S. Patent No. 8,319,512 (in IPR 2025-01413).

C. Counsel and Service Information

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Petitioner consents to electronic service. All services and communications to the attorneys listed above may be sent to BOEIPRService@hklaw.com. A Power of Attorney is concurrently filed with this Petition.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds For Standing

Petitioner certifies that the '020 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review challenging the claims of the '020 Patent on the grounds presented here. This

Petition is filed less than one year after the earliest date on which 138 East LCD filed BOE's waiver of service in the underlying district court litigation.

B. Overview of Challenges and Requested Relief

Petitioner requests cancellation of claims 1-13 of the '020 Patent under pre-AIA 35 U.S.C. § 103.

1. Identification of Prior Art

Petitioner relies on the patents and publications listed in the Table of the Exhibits, including:

Exhibit No.	Prior Art Basis
Ex. 1004: ("Takenaka") U.S. Patent Application Publication No. 2008/0291379	Takenaka published on November 27, 2008 and is prior art at least under pre-AIA 35 U.S.C. §102(b).
Ex. 1005: ("Ito") Japanese Patent Application Publication No. 2009168877A	Ito published on July 30, 2009 and is prior art at least under pre-AIA 35 U.S.C. §102(b).
Ex. 1006: ("Takemura") Japanese Patent Application Publication No. H0643473A	Takemura published on February 18, 1994 and is prior art at least under pre-AIA 35 U.S.C. §102(b).

The Examiner did not cite to or discuss any of the prior art used as grounds in this Petition during the prosecution of the '020 Patent.

2. Grounds for Challenge

The table below summarizes the grounds challenging the independent and dependent claims directed to electrically connected LCD panel terminals.

Ground	Claims	Basis
1	1-7, 11 and 12	Obvious over Takenaka
2	8-10	Obvious over Takenaka in view of Ito
3	1-7 and 13	Obvious over Takemura

Dr. Patrick Murphy’s expert declaration (Ex. 1002, “Murphy”) supports this Petition and demonstrates a reasonable likelihood that Petitioner will prevail with respect to the cancellation of at least one challenged claim.

IV. OVERVIEW OF THE ’020 PATENT

The ’020 Patent is titled, “Electro-optical device, electro-optical panel, and electronic apparatus,” and issued on March 5, 2013 to Seiko Epson Corporation. (Ex. 1001 at Cover).

A. Specification

The ’020 Patent relates to electrical connectivity testing of LCD panels and electro-optical devices comprising such panels, i.e., LCD devices, by applying a voltage signal to the panel through connection wirings that electrically connect panel terminals. (Ex. 1001 at Abstract, 1:7-15, 19:32-34.)

1. Alleged Problem

The ’020 Patent identifies a change in the manufacturing process for LCD devices that creates a problem with quality control checks. (Ex. 1001 at 1:24-42.)

LCD devices typically comprise three elements: an external driving circuit, an LCD panel and a plurality of flexible substrates used as a bridge between the

external driving circuit and the LCD panel. (Ex. 1001 at 1:11-14.) These elements are connected via terminals provided on the LCD panel and corresponding terminals on the flexible substrates. (Ex. 1001 at 1:14-19.) The terminals are pressed together with Anisotropic Conductive Film (“ACF”) between them, which is an adhesive film with conductive particles dispersed in a thermosetting resin. (Ex. 1001 at 1:16-23.) Some of these electrically connected terminals are used to provide a constant potential (“LCCOM”), a reference voltage signal, to the pixels of the panel. (Ex. 1001 at 19:32-37.)

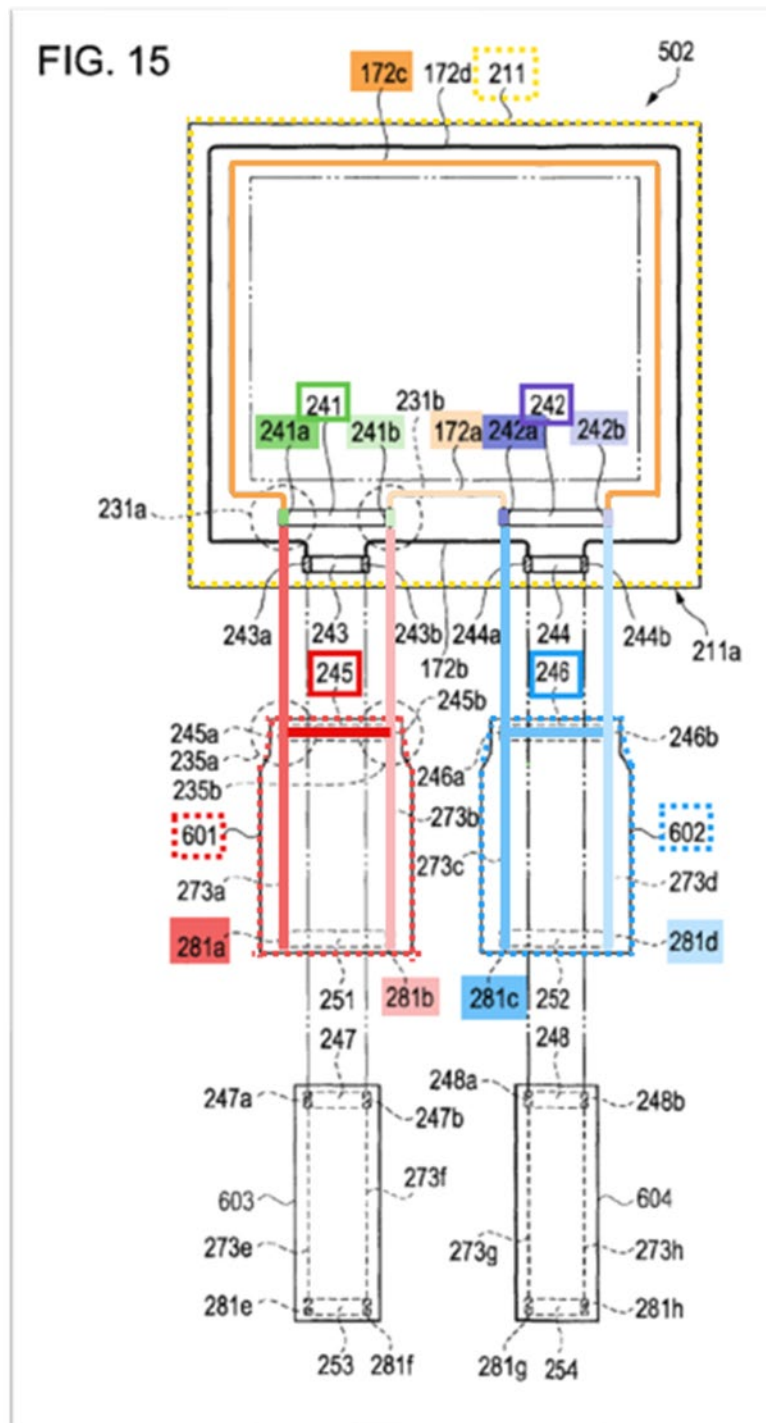
Plastic balls plated with metal replaced solid balls of nickel as the conductive particles used in the ACF. (Ex. 1001 at 1:27-31.) However, the ’020 Patent states that when the plastic balls are compressed during the connection process, they do not leave “particle marks” required for visual inspection purposes. (Ex. 1001 at 1:32-35.) Thus, there is allegedly no method of checking the connection between the LCD panel and flexible substrates beside turning on the LCD device. (Ex. 1001 at 1:35-42.)

2. Alleged Invention

The ’020 Patent’s solution to the above-identified problem is to electrically connect the LCD panel’s terminals together. (Ex. 1001 at 1:46-2:6.) The connection between the LCD panel and the flexible substrates may then be performed by measuring the resistance value between external terminals: if “electricity flows”

between the terminals then the liquid crystal panel and the flexible substrate are connected. (Ex. 1001 at 2:7-19, 13:5-17.)

For example, Figure 15 shows one embodiment of the claimed LCD device:



(Ex. 1001 at 1:46-2:6, 16:15-26, Fig. 15 (annotated).) LCD device (502) comprises a panel (211) and flexible substrates (601) and (602). (Ex. 1001 at 16:27-31, 16:34-38.) The connection between these elements is tested by measuring the resistance value between external terminals, e.g., flexible substrate terminals (281a) and (281d) via constant potential LCD panel terminals (241a) and (242b): if “electricity flows” between the terminals then the liquid crystal panel and the flexible substrate are connected. (Ex. 1001 at 2:7-19, 13:5-17, 19:32-37.) If the circuit path is confirmed, it is determined that LCD panel (211) and flexible substrates (601) and (602) are electrically connected. (Ex. 1001 at 18:20-23.)

B. Prosecution History

On December 1, 2010, Seiko Epson Corporation filed U.S. Application No. 12/958,154 (the “’154 Application”). (Ex. 1003 at 2.) The ’154 Application claims priority to Japanese Patent Application No. 2009-275218, filed on December 3, 2009, and Japanese Patent Application No. 2010-214838, filed on September 27, 2010. (*Id.* at 4.) In the same filing, Seiko Epson Corporation filed an Information Disclosure Statement citing a single Japanese patent. (*Id.* at 106.)

On October 31, 2012, without issuing any substantive Office Actions, the Examiner mailed a Notice of Allowance for the ’154 Application. (*Id.* at 233-246.) The Examiner did not cite any additional prior art or analyze the single Japanese

patent that Seiko Epson Corporation cited. (*Id.*) On March 5, 2013, the '154 Application issued as the '020 Patent. (*Id.* at 253.)

As discussed in Section VIII, it was material error that the Examiner did not address the Challenged Claims at least in view of the technical disclosures and teachings of Takenaka, Ito and Takemura, which render those claims invalid.

C. Alleged Priority Date

For present purposes only, Petitioner assumes the priority date is December 3, 2009. But the critical date for purposes of pre-AIA §102(b) is December 1, 2009—one year before the “actual filing of the application in this country” of December 1, 2010. Pre-AIA 35 U.S.C. §119(a) (“... no patent shall be granted on any application for patent for an invention which had been patented or described in a printed publication in any country more than one year before the date of the actual filing of the application in this country . . .”); MPEP 2133.II (“The 1-year time bar is measured from the U.S. filing date.”).

V. CLAIM CONSTRUCTION

In an *inter partes* review, claims are “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” (37 C.F.R. § 42.100(b).) Claims must be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the invention in light of the specification and the prosecution history pertaining

to the patent. *Id.* See also *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-1313 (Fed. Cir. 2005) (*en banc*); 83 Fed. Reg. 51,340. For the purposes of this Petition, Petitioner proposes several constructions below to aid the Board’s review; however, these constructions simply articulate the plain-and-ordinary meanings of phrases that were well-understood to a person of ordinary skill. All other claim terms should be given their plain and ordinary meaning as would be understood in the context of the ’020 Patent’s disclosure.

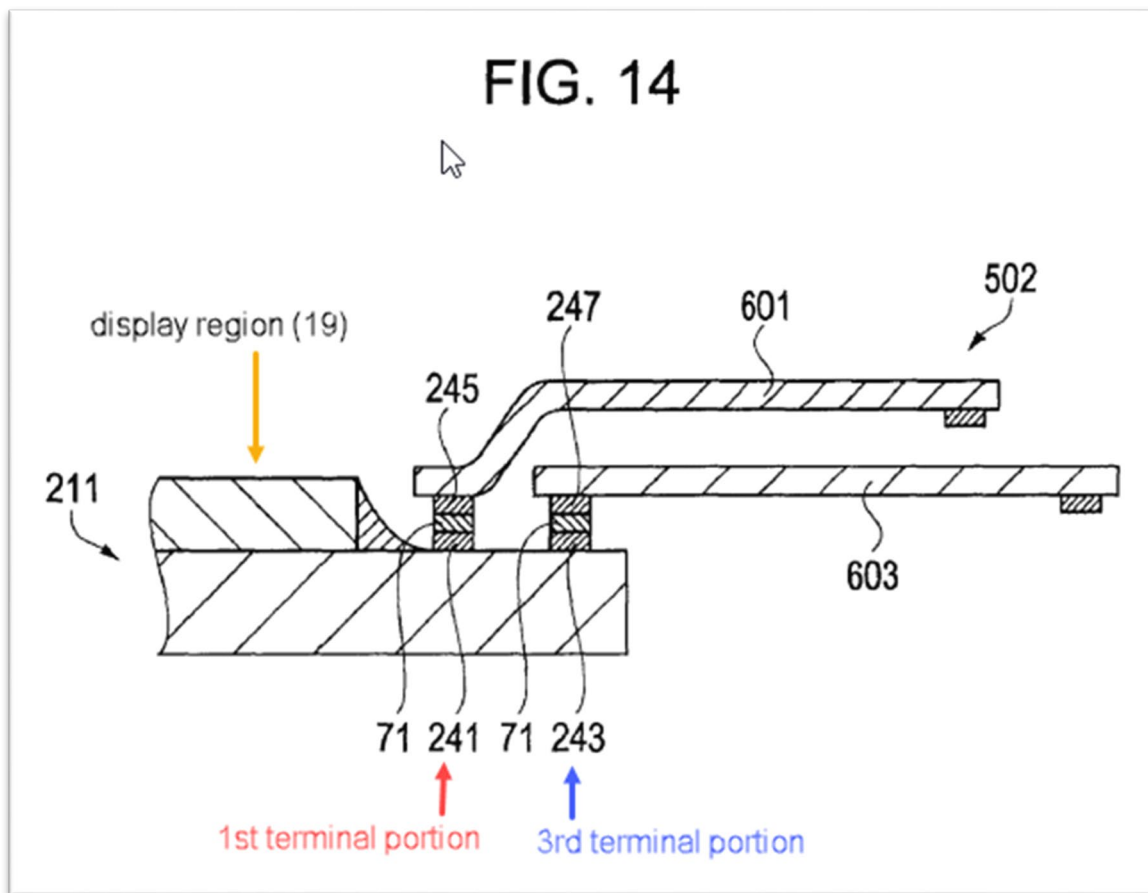
A. “arranged on a side opposed to a display region with respect to the first terminal portion” (Claim 8)

A POSITA at the time of the ’020 Patent’s filing would have understood the plain and ordinary meaning of “arranged on a side opposed to a display region with respect to the first terminal portion” to mean “arranged on an opposite side of the first terminal portion from the display region.” (Murphy ¶68.)

First, Claim 8 makes clear that the third terminal portion and display region are arranged relative to the first terminal portion. (’020 Patent, cl. 8; Murphy ¶69.) Specifically, they are arranged on opposing sides of the first terminal portion or, in other words, one on one side and one on an opposite side. (’020 Patent, cl. 8; Murphy ¶69.)

Second, the specification confirms that the third terminal portion is arranged on the other side of the first terminal portion as the display region. (’020 Patent, 16:34-42, Figs. 13-15; Murphy ¶70.) Figure 13 and Figure 14 (a cross-sectional

view of the liquid crystal device shown in Figure 13) show an arrangement where the display region (19) is on one side of the first terminal portion (241), and the third terminal portion (243) is arranged on the other side as the display region:



(’020 Patent, Fig. 14 (annotated); Murphy ¶70.)

B. “connection wiring” (Claims 1, 2, 5, 6, 8, 9 and 11)

A POSITA at the time of the ’020 Patent’s filing would have understood the plain and ordinary meaning of “connection wiring” to mean “circuit path”. (Murphy ¶71.)

The '020 Patent explains that the connection between the LCD panel and flexible substrates is checked by measuring the resistance value between external terminals: if “electricity flows” between the terminals then the liquid crystal panel and the flexible substrate are connected. ('020 Patent, 13:5-17, 19:32-34; Murphy ¶72.) This is only possible if there is a circuit path that links the terminals. (Murphy ¶72.)

Furthermore, the '020 Patent suggests that a “wiring” is not limited to a physical wire, a single wire, multiple wires tied together or a wire on a single layer. (Murphy ¶73.) First, the structure of a flexible substrate carrying an integrated circuit chip is described as a “*wiring substrate*” that has a “*wiring patterned and formed* on the base.” ('020 Patent, 7:31-39; Murphy ¶73.) As Dr. Murphy explains, another name synonymous with flexible substrates carrying integrated circuit chips is “flexible printed *circuits*.” (Murphy ¶73.) Such devices do not generally have physical wires but rather circuit paths fixed on the surfaces or within the flexible substrate. (Murphy ¶73.) Moreover, the circuits paths of these flexible substrates pass may between different layers. (Murphy ¶73.)

Second, connection wirings are described as being able to “creep between the layers [of the LCD panel] using contact holes so as to connect different panel terminals.” ('020 Patent, 23:39-40; Murphy ¶74.) Connection wirings are also described as being in some cases “connected over the layers laminated on the device

substrate 12 without obstruction of the other wirings (for example, the data lines and the like).” (’020 Patent, 19:50-53; Murphy ¶74.) Contact holes and laminated layers are characteristic circuit paths, not physical wires. (Murphy ¶74.) This confirms that a “wiring” is not limited to a physical wire, a single wire, multiple wires tied together or a wire on a single layer. (Murphy ¶74.)

VI. LEVEL OF ORDINARY SKILL

As of December 3, 2009, a POSITA had at least: i) a bachelor-level degree in electrical engineering, physics, or a related subject and two or more years of experience working in the field of LCD displays; ii) a Master’s-level degree in electrical engineering, physics, or a related field, and at least 1 year of experience in the design/development of LCD displays; or iii) a Ph.D.-level degree in electrical engineering, physics, or a related field, and at least some experience in the area of LCD displays. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. (Murphy ¶34.)

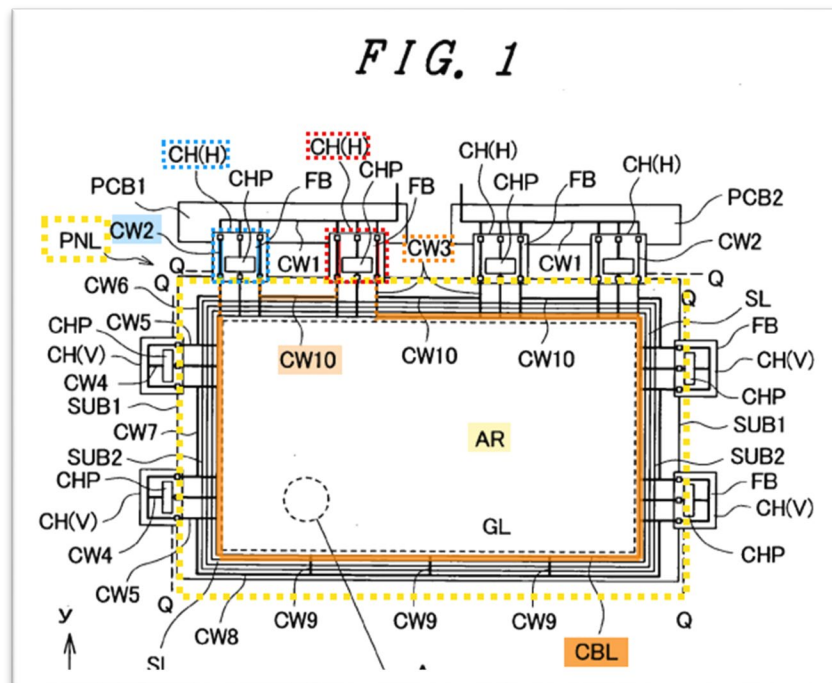
VII. DESCRIPTION OF THE PRIOR ART

A. Takenaka

Like the ’020 Patent, Takenaka relates to a liquid-crystal display device where a voltage signal is provided to the display panel through a “multiplicity of distributed supply paths” that electrically connect panel terminals. (Takenaka at Abstract, [0014].) Specifically, the multiplicity of distributed supply paths comprise common lines that are provided on tape-carrier-schemed semiconductor devices connected to

the panel, as well as a common bus line formed around the circumference of the panel. (Takenaka at Abstract, Fig. 1.) Takenaka discloses that this arrangement of wirings stabilizes the reference voltage signal provided to the panel's pixels such that the size of the panel can be increased and picture quality is improved. (Takenaka at [0011] - [0013].)

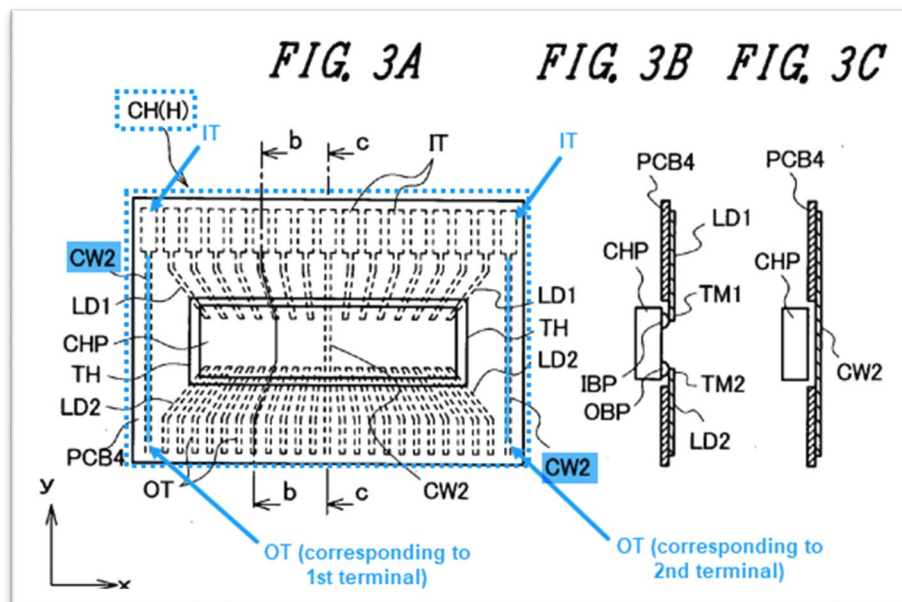
Figure 1 illustrates a preferred embodiment for the liquid-crystal display device of the claimed invention:



(Takenaka at [0025], Fig. 1 (annotated).) The liquid-crystal display panel (PNL) is connected on three sides to semiconductor devices (CH(H) and CH(V)) that respectively supply video signals and scanning signals to the panel's pixels. (Takenaka at [0026], [0027], [0040].) The semiconductor devices also pass the

reference voltage signal through common wires (CW2). (Takenaka at [0056].) These common wires are connected to common wires (CW3) formed on the panel at terminals that are illustrated as small square boxes. (Takenaka at [0056].) In turn, these common wires (CW3) are connected to other common wires (CW10) and the common bus line (CBL), which surrounds the panel's display area (AR). (Takenaka at [0037], [0058], [0070].)

Figures 3A-C show a detailed view of a semiconductor device of the preferred invention:



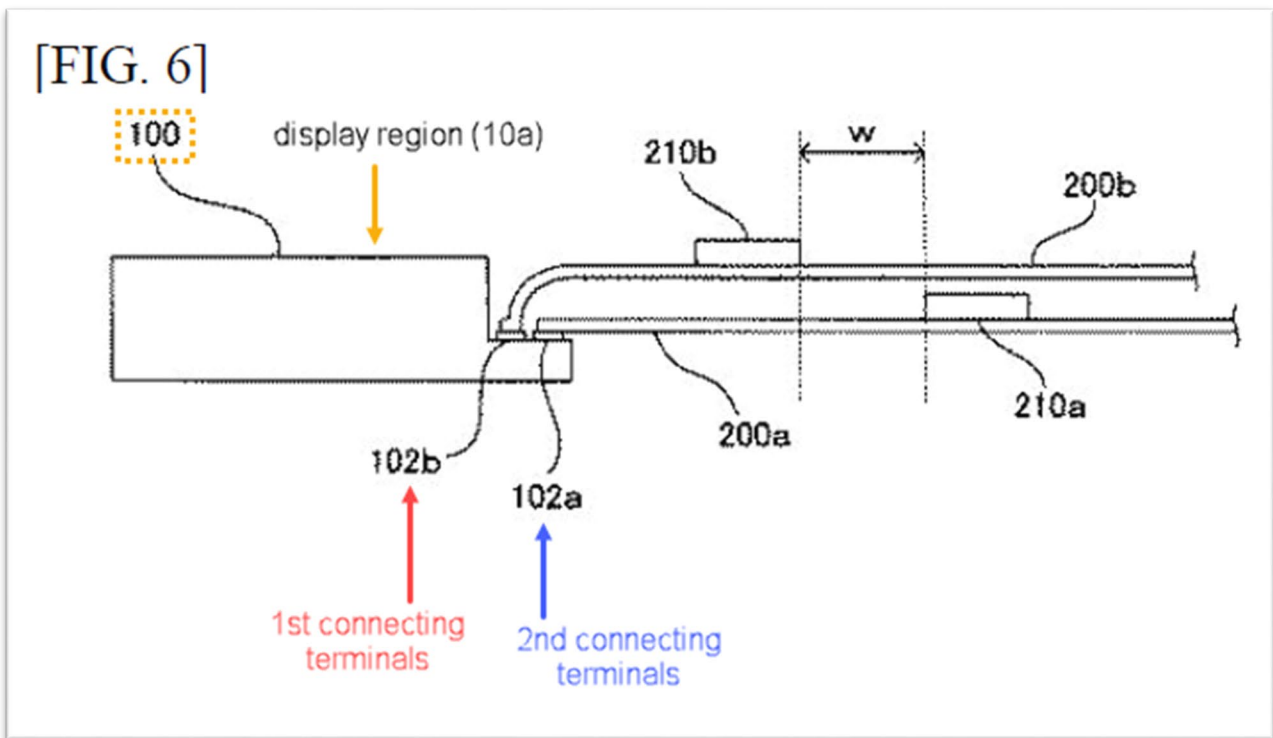
(Takenaka at [0075], Figs. 3A-C (annotated).) The semiconductor device (CH(H)) comprises a chip mounted on a flexible circuit board (FB), with common wires (CW2) formed at the sides of the board. (Takenaka at [0076], [0081].) The ends of the common wires (CW2) are connected to an input terminal (IT) and an output

terminal (OT), the latter of which are connected to corresponding terminals on the panel. (Takenaka at [0076], [0085].)

B. Ito

Ito relates to a liquid-crystal display device having flexible substrates that overlap with one another, similarly to the '020 Patent. (Ito at [0008].) Each of the substrates carry an integrated circuit for driving the liquid-crystal panel, but the circuits are positioned close together in the substrates' overlapping configuration, which concentrates heat and negatively affects reliability. (Ito at [0005].) Ito solves this problem by having offset integrated circuits. (Ito at [0007].)

Figure 6 shows the overlapping configuration of Ito's substrates (200a, 200b):

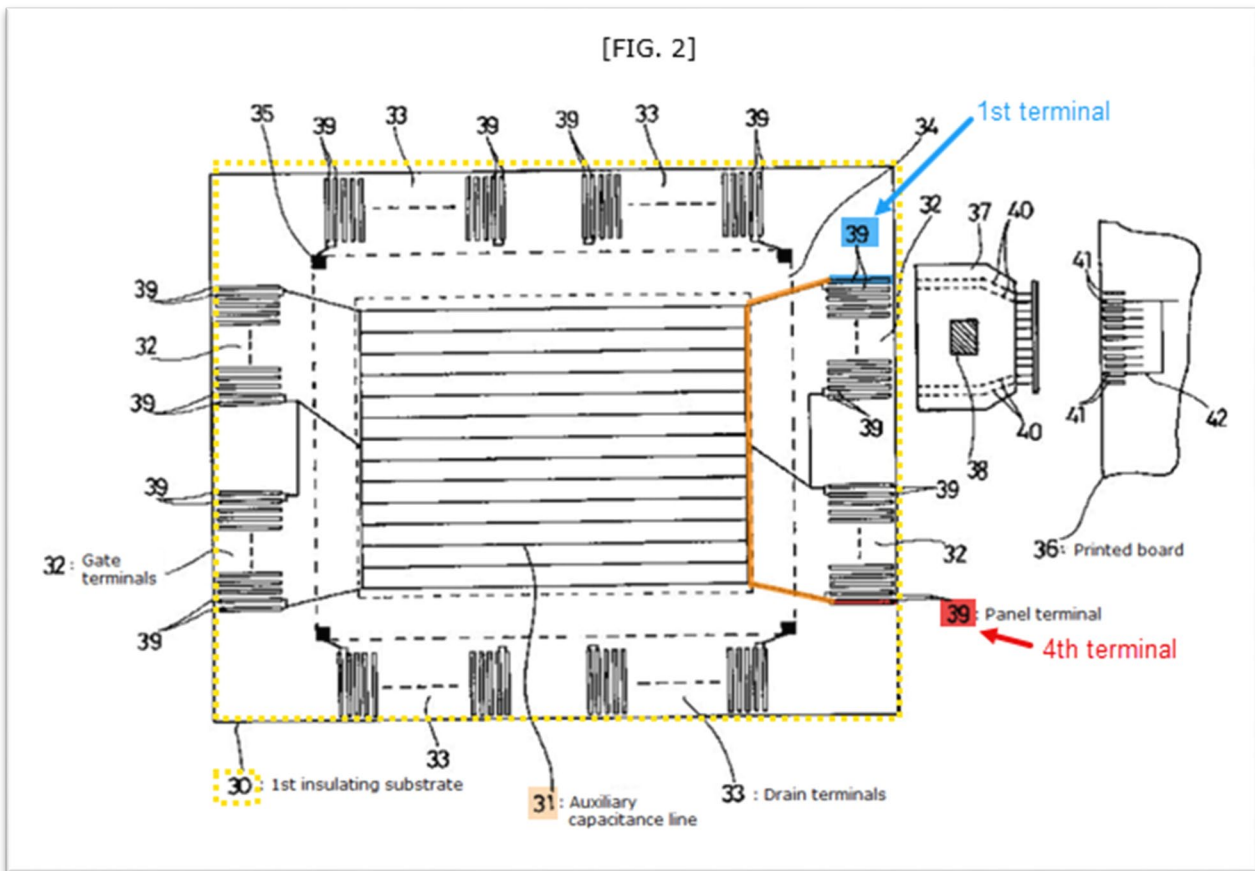


(Ito at [0036], Fig. 4 (annotated).) This configuration is achieved by electrically connecting the substrates (200a, 200b) to the two rows of panel terminals (102a, 102b). (Ito at [0036], Fig. 4.)

C. Takemura

Takemura solves the same problem as the '020 Patent – checking the quality of terminal connections used by a liquid crystal display device. (Takemura at [0001].) Like the '020 Patent, Takemura teaches that quality checks are necessary because connections between an LCD panel and flexible substrates are compromised during manufacturing. (Takemura at [0003], [0004].) For example, conductive metal balls in the ACF used for the connections may be insufficient when pressed, or the film may expand due to heat, causing the terminals to shift. (Takemura at [0004].)

To solve this problem, as shown in Figure 2 below, Takemura teaches a configuration where terminal groups (32) on the LCD panel have two short-circuited terminals (39) on each end, and these terminals are electrically connected to corresponding terminals on flexible substrates (37):



(Takemura at [0005], [0010], Fig. 2 (annotated).) Terminals on the other ends of the flexible substrates are electrically connected to measurement terminals (41), whereby the resistance between the short-circuited terminals connections may be tested. (Takemura at [0005], [0011], Fig. 2.)

Additionally, Takemura teaches that the short-circuited panel terminals are connected to auxiliary capacitance lines (31). (Takemura at [0030], Fig. 2.) The lines may be used for further terminal connection measurements, or they can be used to provide a stable voltage. (Takemura at [0011], [0031].)

VIII. GROUNDS

As evidenced by the references cited below, before December 3, 2009, a POSITA would have known to provide connection wirings between the terminals of an LCD panel so the LCD panel's electrical connection with flexible substrates could be checked through the external terminals of the flexible substrates. (Murphy Section X.) Under the Grounds below, when reading Takenaka, Ito and Takemura, a POSITA would understand that each of these references have the same structure as the '020 Patent. (*Id.*) Thus, there is a reasonable likelihood that Petitioner will show that Claims 1-13 of the '020 Patent are invalid.

A. Ground 1: Claims 1-7, 11 and 12 are Obvious over Takenaka

Claims 1-7, 11 and 12 would have been obvious in view of Takenaka to a person of ordinary skill at the time of the '020 Patent's filing. (Murphy ¶91.) *Game & Tech Co. v. Activision Blizzard Inc.*, 926 F.3d 1370, 1381 (Fed. Cir. 2019) (“[A] patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention.”); *SIBIA Neurosciences, Inc. v. Cadus Pharmaceutical Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000) (“In appropriate circumstances, a single prior art reference can render a claim obvious.”). Specifically, and as explained in greater detail below, claims 1-13 recite LCD devices and LCD panels having various configurations of connection wirings, and it would have been obvious for a POSITA to arrive at the claimed configurations in view of Takenaka.

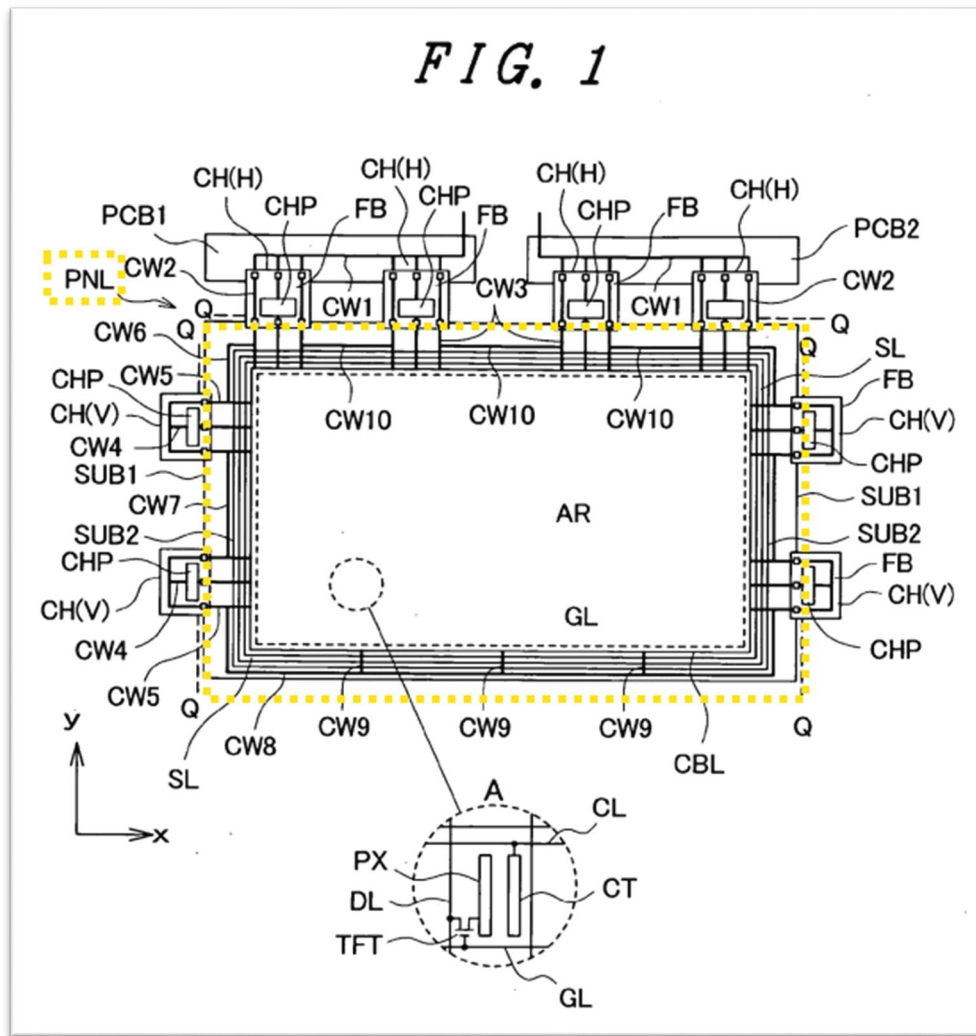
1. Independent Claim 1

[1pre] “An electro-optical device comprising:”

To the extent the preamble is limiting, it is taught by Takenaka. (Murphy ¶92.) Takenaka discloses a “***liquid-crystal display device***[.]” (Takenaka at Abstract; Murphy ¶92.)

[1a] “an electro-optical panel including:”

Takenaka discloses a “liquid-crystal display device [that] includes a ***liquid-crystal display panel***[.]” (Takenaka at Abstract; Murphy ¶93.) The LCD panel (PNL) is shown in Figure 1 below:



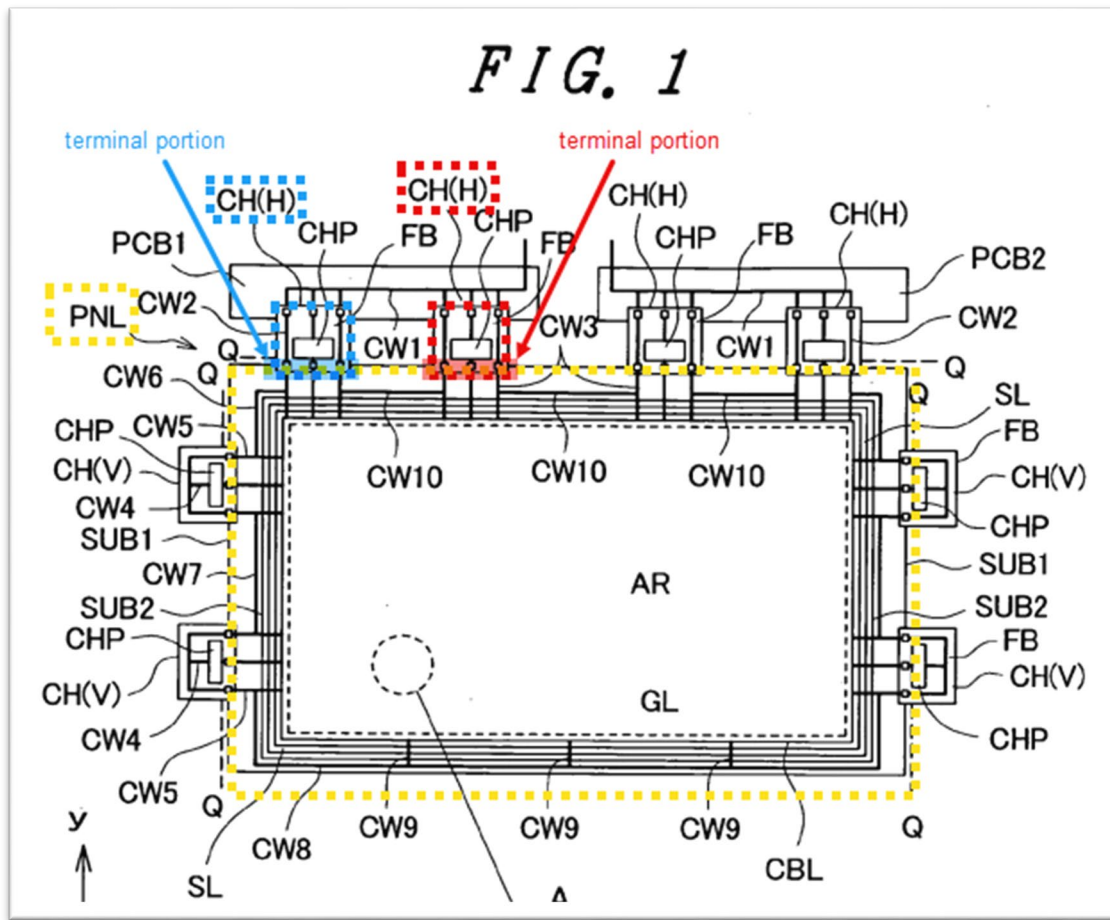
(Takenaka at [0026], Fig. 1 (annotated); Murphy ¶93.) A POSITA reading Takenaka would understand that Takenaka teaches this Claim [1a]. (Murphy ¶93.)

[1b] “a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and”

Takenaka’s LCD panel is connected to semiconductor devices at the periphery of the panel. (Takenaka at Abstract (“The liquid-crystal display device includes a liquid-crystal display panel and *a semiconductor device connected to a part of a*

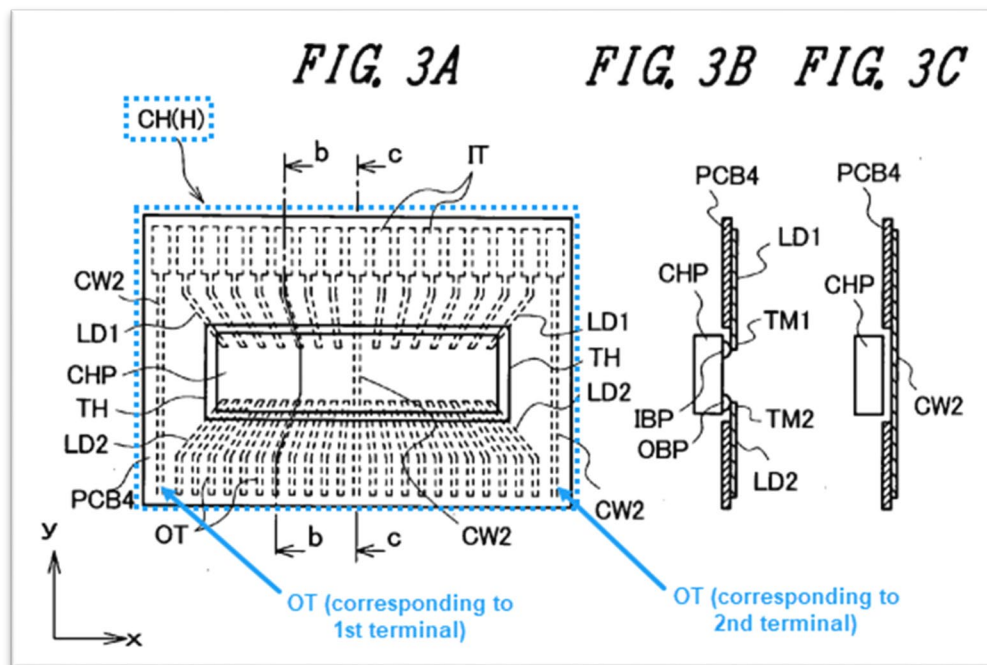
*periphery of the liquid-crystal display panel.”), [0028], Fig. 1; Murphy ¶94) A semiconductor device comprises a chip mounted on a flexible board with lines leading from the terminals of the chip to the periphery of the board. (Takenaka at [0007]; Murphy ¶94.) These lines are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0008] (“Such a semiconductor device can be electrically connected to the **corresponding terminals** . . . [on] a part of the periphery of the liquid crystal display panel.”), [0053] – [0054] (“[Drain signal lines DL] further extend across the seal member SL and reach the **terminals (not shown) on the substrate SUB1. Those terminals are electrically connected to the output terminals of the semiconductor device CH(H)** through a not-shown anisotropic conductive film”), Figs. 1, 2; Murphy ¶94.) Thus, a POSITA would have understood that Takenaka’s LCD panel has a terminal portion, i.e., an area, and a terminal group, i.e., terminals within the area. (Murphy ¶94.)*

Moreover, a POSITA would understand the necessity for any terminals provided on the semiconductor device to have corresponding terminals on the LCD panel. (Murphy ¶95.) As shown in Figure 1 below, semiconductor devices (CH(H)) bridge between the panel (PNL) and printed-circuit boards (PCB1) and (PCB2):



(Takenaka at [0042], Fig. 1 (annotated); Murphy ¶95.) For signals to move across the bridges created by the semiconductor devices to reach the LCD panel, the terminals on the semiconductor devices must be electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0076] (“The flexible board FB is structured with . . . a plurality of output terminals OT connected to the terminals (not shown) on the liquid-crystal display panel PNL”), Fig. 1; Murphy ¶95.)

Figure 3A is a detailed view of Takenaka’s semiconductor device:

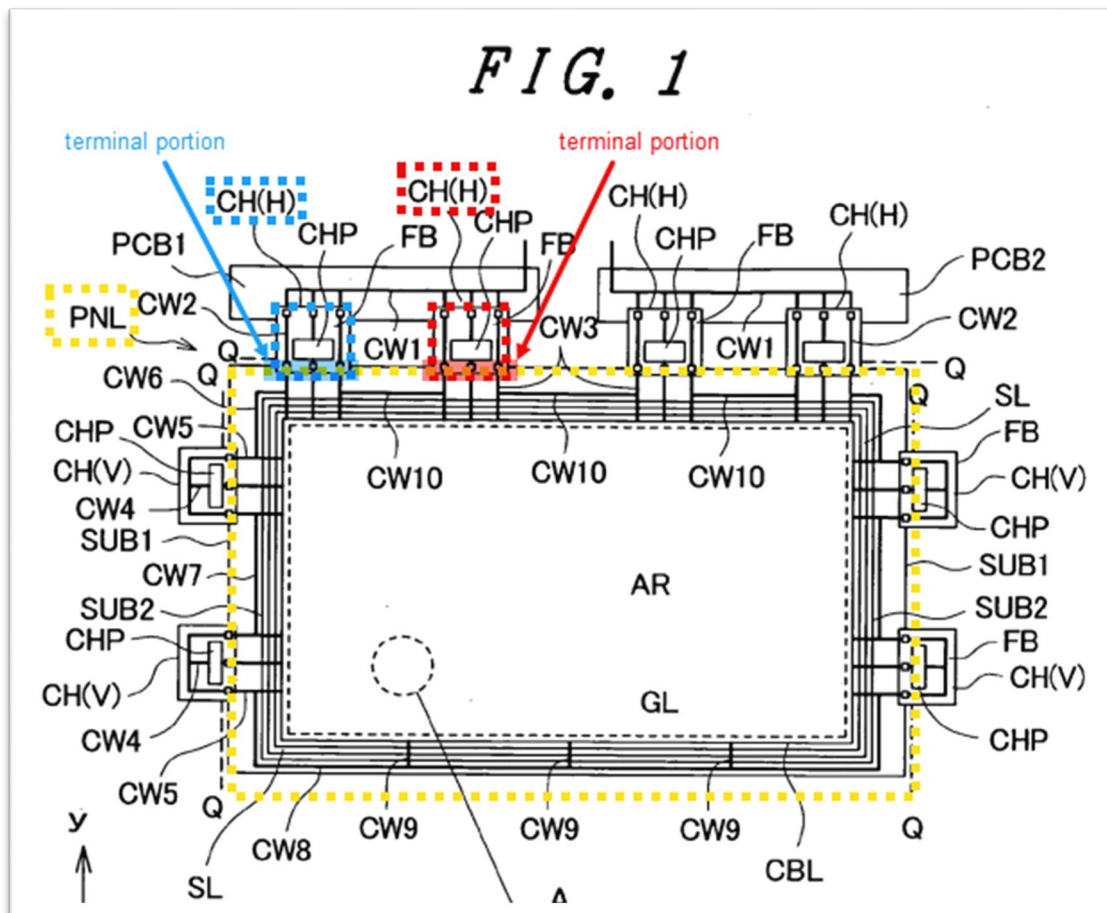


(Takenaka at [0076], Fig. 3A (annotated); Murphy ¶96.) In addition to the output terminals connected via leads (LD1) to the semiconductor chip, there are two output terminals positioned on either side of the semiconductor device that are not connected to the semiconductor chip. (Takenaka at [0076], [0081] (“Each of these common lines CW2 has one . . . end connected to another *output terminal OT provided parallel with the output terminals OT connected to the leads LD2*”), Fig. 3A; Murphy ¶96.) For the same reasons noted above, a POSITA would understand that these two output terminals are connected to corresponding first and second terminals on the LCD panel, and the first connected pair of terminals is separated from the second pair of connected terminals as shown in Fig. 1. (Takenaka at [0071],

Takenaka teaches Claim [1b]. (Murphy ¶96.)

[1c] “a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal”

semiconductor devices, as shown below:

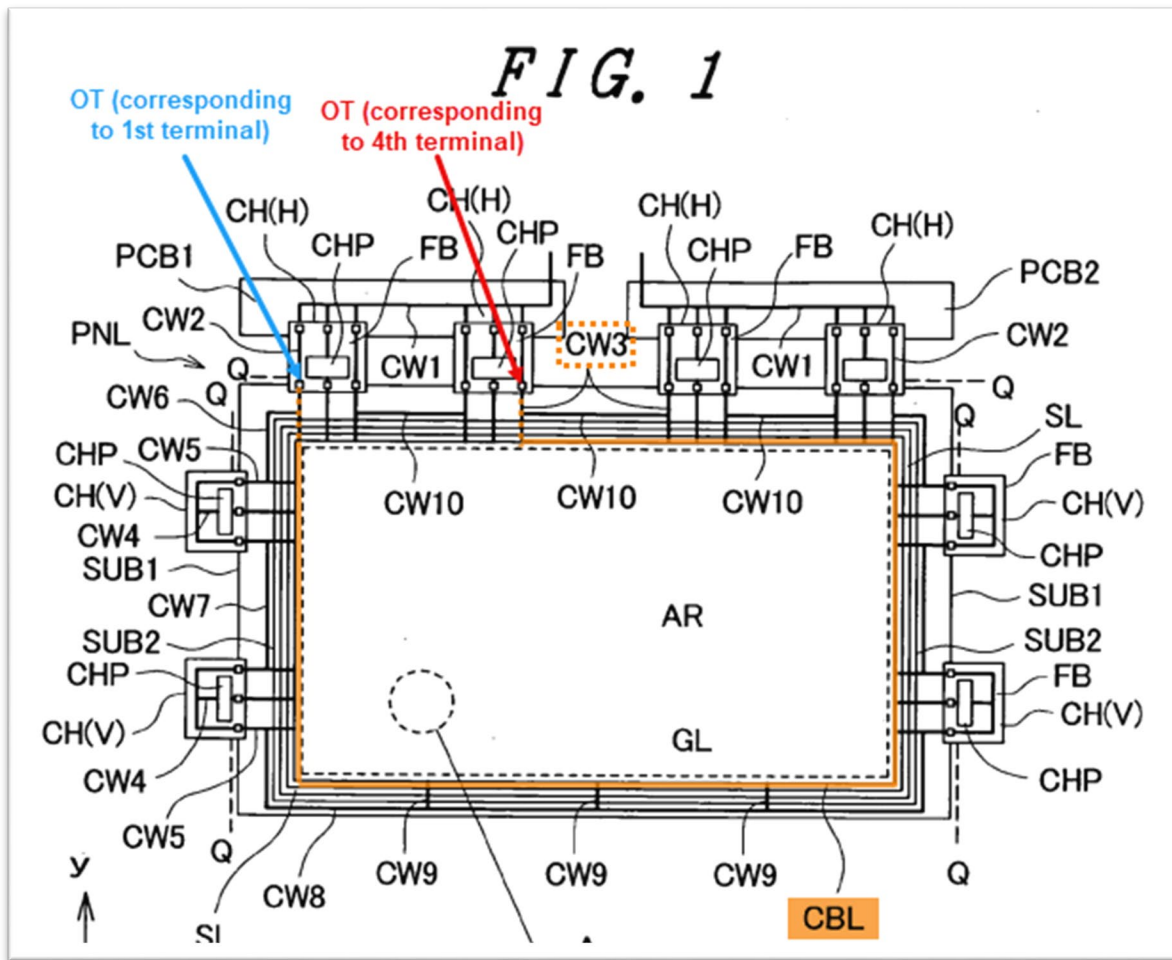


(Takenaka at [0028], [0042], Fig. 1; Murphy ¶97. *See also* Claim [1b] *supra*.) Thus, a POSITA would understand that the LCD panel has a second corresponding terminal portion and group of terminals including third and fourth terminals separated from each other. (Murphy ¶97. *See also* Claim [1b], *supra*.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1c]. (Murphy ¶97.)

[1d] “the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,”

Takenaka discloses that there is a need to supply LCD panels with a reference signal having a reference potential relative to the scanning and video signals. (Takenaka at [0009]; Murphy ¶98.) Takenaka provides that reference voltage signal through a common bus line (CBL) as well as common lines (CW1), (CW2) and (CW3). (Takenaka at [0037], [0056] (“[T]he reference voltage signal . . . is led to the common bus line CBL through, in order, the common line CW1 . . . , the common lines CW2 . . . and the common line[s] CW3[.]”), [0058]; Murphy ¶98.)

As shown in Figure 1 below, common bus line (CBL) is electrically connected to common lines (CW3), both of which are formed on the LCD panel (PNL):



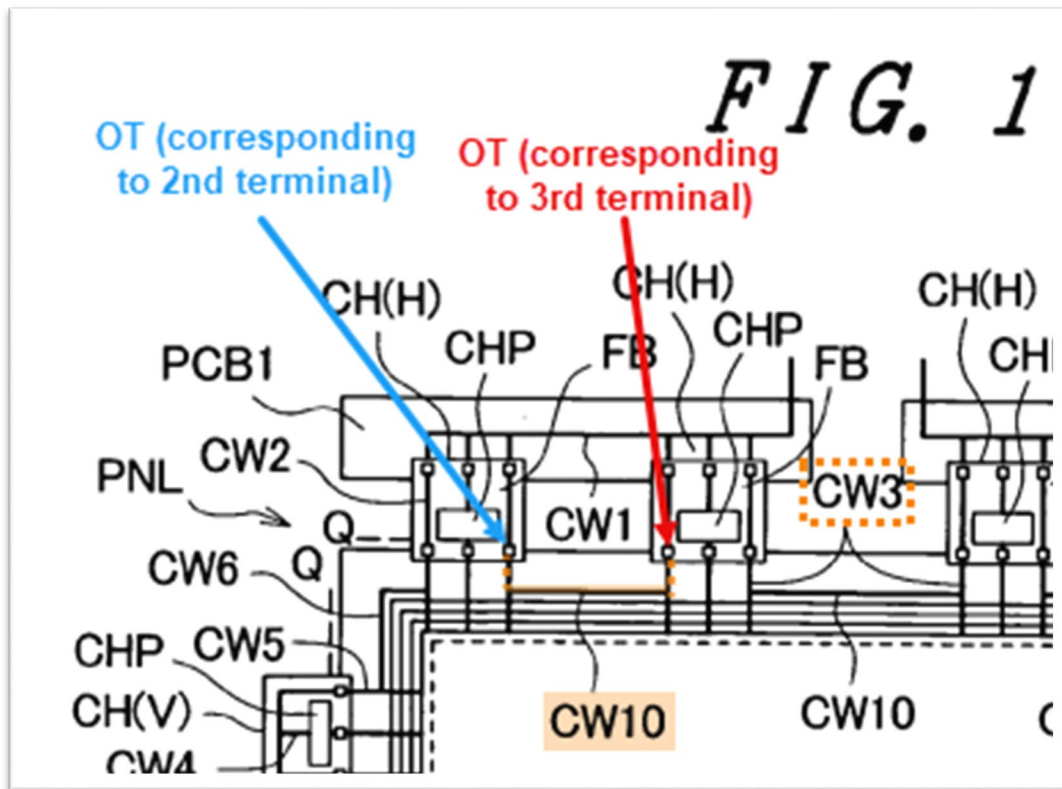
(Takenaka at [0058], Fig. 1 (annotated); Murphy ¶99.) Common lines (CW3) in turn are connected common lines (CW2) to terminals (not shown) on the LCD panel that correspond to output terminals (OT) of semiconductor devices (CH(H)) (small square boxes). (Takenaka at [0056] (“[C]ommon lines CW1, CW2, CW3 are to be electrically connected together through the terminals (illustrated with square boxes in the figure, corresponding to the references IT and OT in FIG. 3) of the semiconductor device CH(H)[.]”)) Thus, a POSITA would understand that the first and fourth terminals are electrically connected through two common lines (CW3)

and common bus line (CBL). (Takenaka at Fig. 1; Murphy ¶99. *See also* Claim [1c], *supra*.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1d]. (Murphy ¶99.)

[1e] “the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;”

Takenaka further discloses that additional common lines are provided on the LCD panel, such as common line (CW10), for stabilizing the reference voltage signal throughout the common bus line. (Takenaka at [0070], [0073]; Murphy ¶100.)

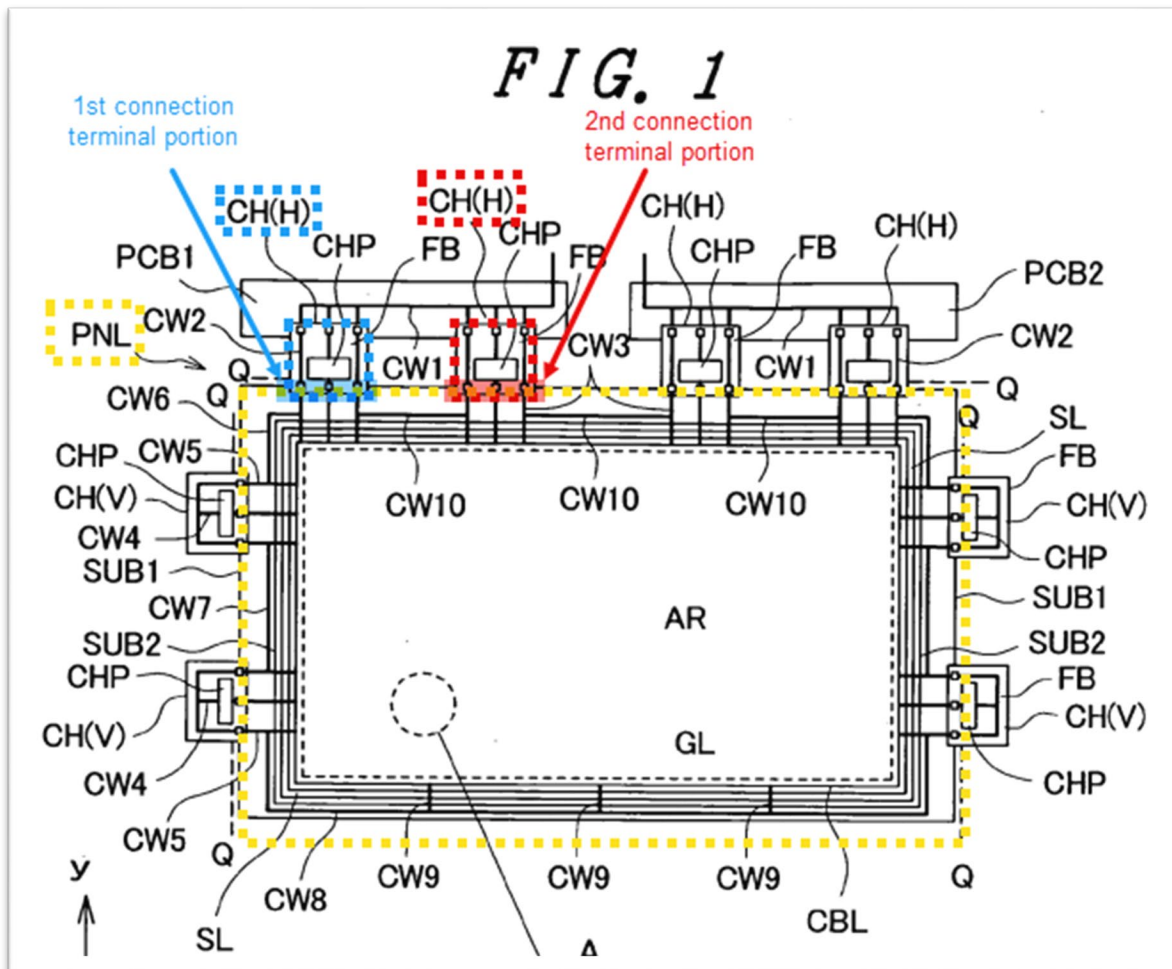
As shown in Figure 1 below, common line (CW10) provides an electrical connection between common lines (CW3):



(Takenaka at [0070] (“The common line CW10 is connected between the semiconductor devices CH(H) at their common lines CW3.”), Fig. 1 (annotated); Murphy ¶101.) Accordingly, a POSITA would understand that the LCD panel’s second and third terminals are electrically connected through two common lines (CW3) and common line (CW10). (Takenaka at Fig. 1 (annotated); Murphy ¶101.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1e]. (Murphy ¶101.)

[1f] “a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;”

As shown below, Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each comprising a flexible board with output terminals in an area that are electrically connected to corresponding terminals on the LCD panel:

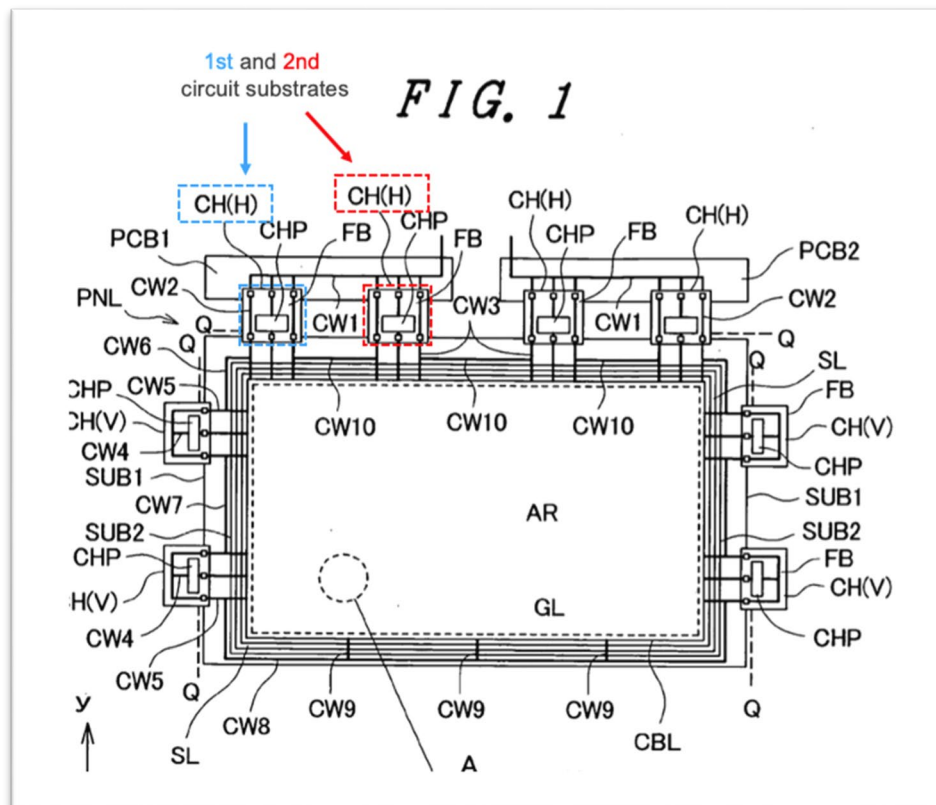


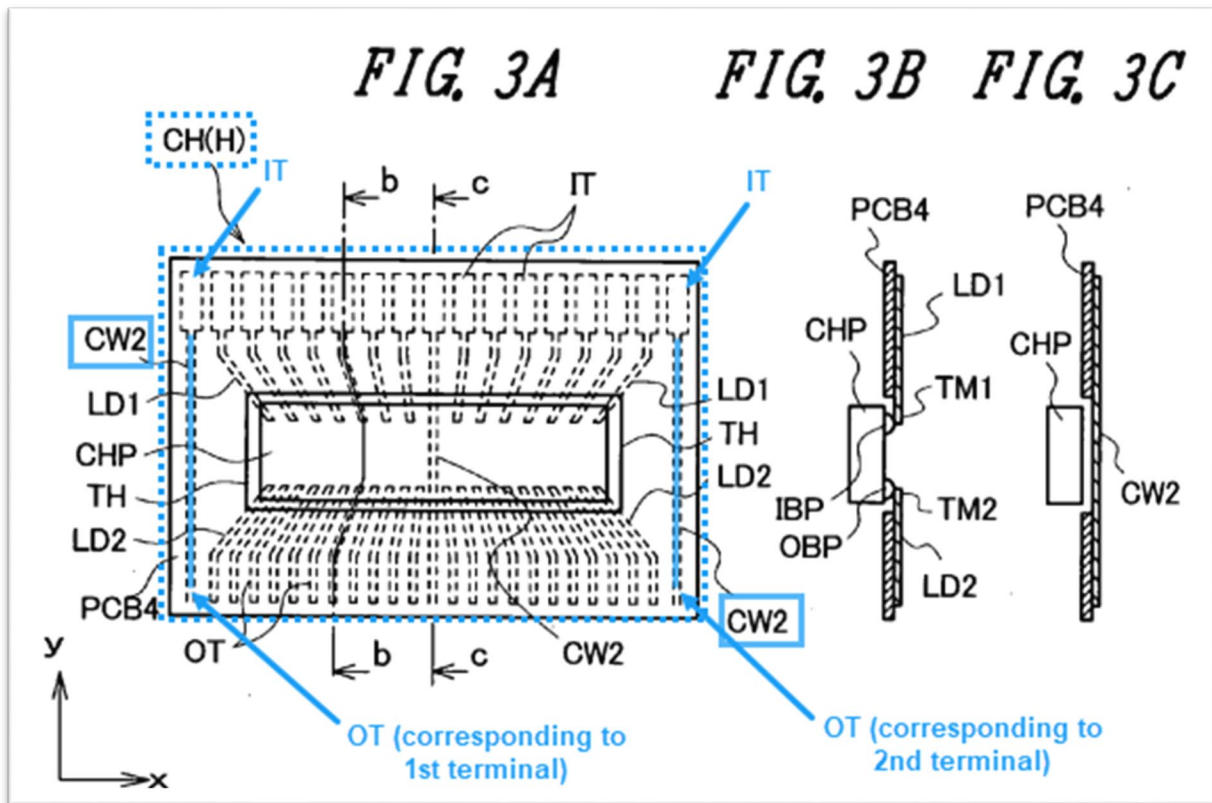
(Takenaka at [0007], [0041], [0076], [0081] Figs. 1, 3A; Murphy ¶102. *See also* Claim [1b], *supra*.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1f]. (Murphy ¶102.)

[1g] “a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second

*terminal through the first connection terminal portion;
and”*

As shown in Figures 1 and 3A below, Takenaka's semiconductor device (CH(H)) further comprises input terminals (IT) at the ends of the two common lines (CW2):





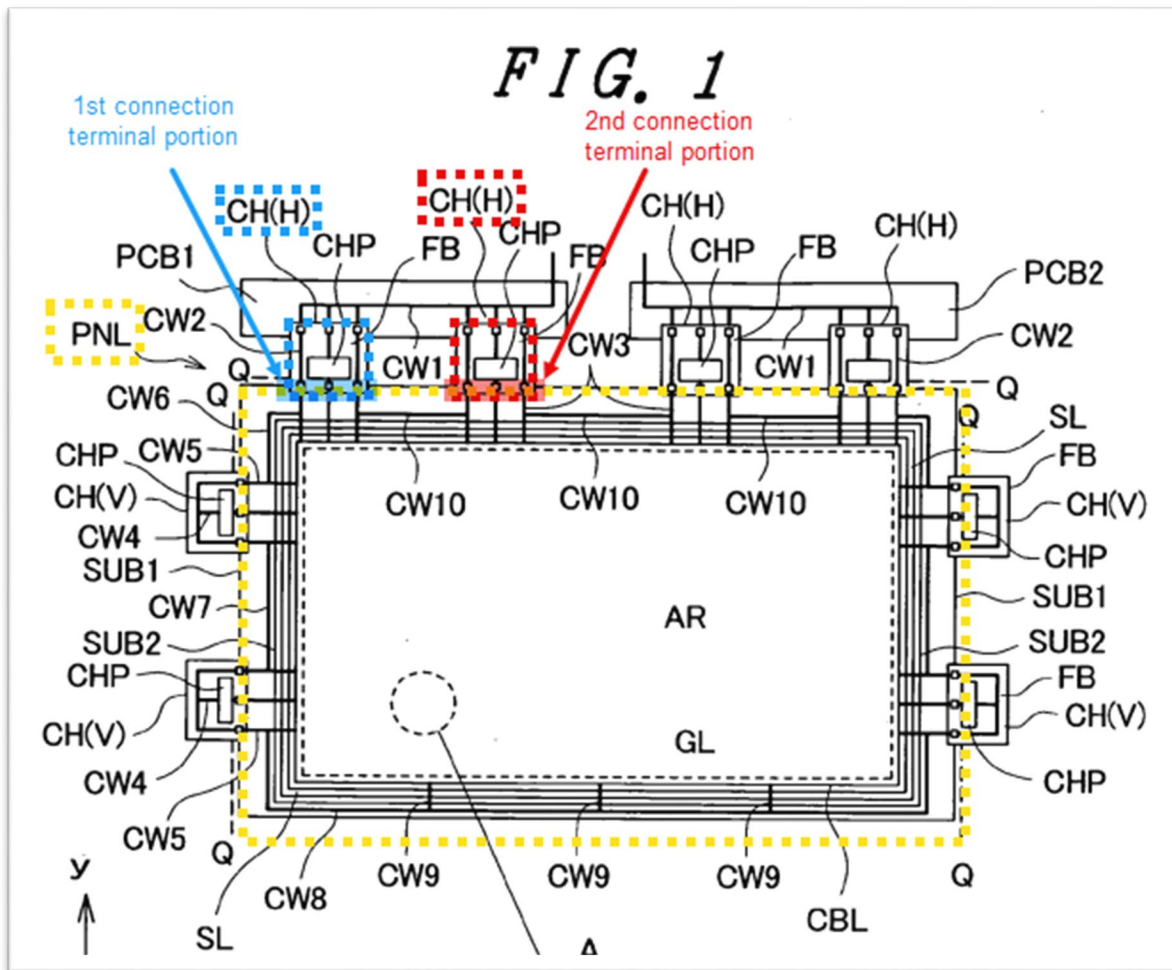
(Takenaka at [0081] (“*Each of these common lines CW2 has one end connected to another input terminal IT[.]*”), Figs. 1 (annotated), 3A (annotated); Murphy ¶103.)

These input terminals are electrically connected to the respective output terminals at the other end of each common line (CW2). (Takenaka at [0081], Fig. 3A; Murphy ¶103.) In turn, these output terminals are electrically connected to the corresponding terminals on the LCD panel, as discussed above. (Takenaka at [0007], [0076], [0081], Figs. 1, 3A; Murphy ¶103. *See also* Claims [1b], [1f], *supra*.) Accordingly, a POSITA would understand that Takenaka discloses first and second external terminals on a semiconductor device that are respectively connected to the first and second terminals on the LCD panel through the first connection terminal portion on

the flexible board of Takenaka's semiconductor device. (Murphy ¶103.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1g]. (Murphy ¶103.)

[1h] “a second circuit substrate including: a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion;”

As shown below, Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each comprising a flexible board with output terminals that are electrically connected to corresponding terminals on the LCD panel:



(Takenaka at [0007], [0041], [0076], [0081] Figs. 1 (annotated), 3A; Murphy ¶104.

See also Claims [1b], [1f], *supra*.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1h]. (Murphy ¶104.)

[1i] “a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.”

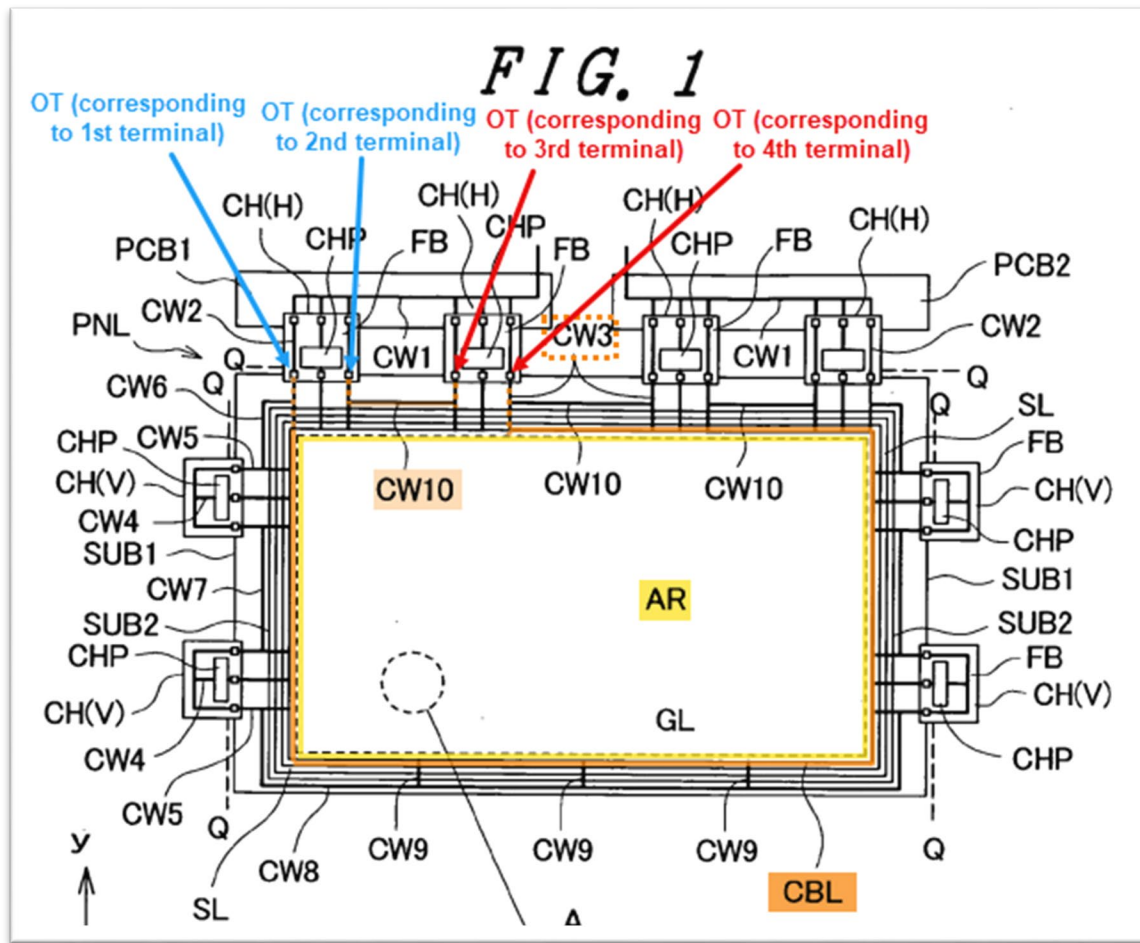
Takenaka discloses multiple tape-carrier-schemed semiconductor devices, each with input terminals electrically connected to output terminals, which in turn

are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶105. *See also* Claims [1b], [1g].) Thus, a POSITA would understand that Takenaka discloses third and fourth external terminals on a semiconductor device that are respectively connected to the third and fourth terminals on the LCD panel through the second connection terminal portion on the flexible board of Takenaka's semiconductor device. (Murphy ¶105.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [1i]. (Murphy ¶105.)

2. Dependent Claim 2

The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.

As shown in Figure 1 below, Takenaka discloses that some of common bus line (CBL) and common line (CW10) extend around the circumference of display region (AR):



(Takenaka at [0030], [0037], [0070], Fig. 1 (annotated); Murphy ¶106.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [2]. (Murphy ¶106.)

3. Dependent Claim 3

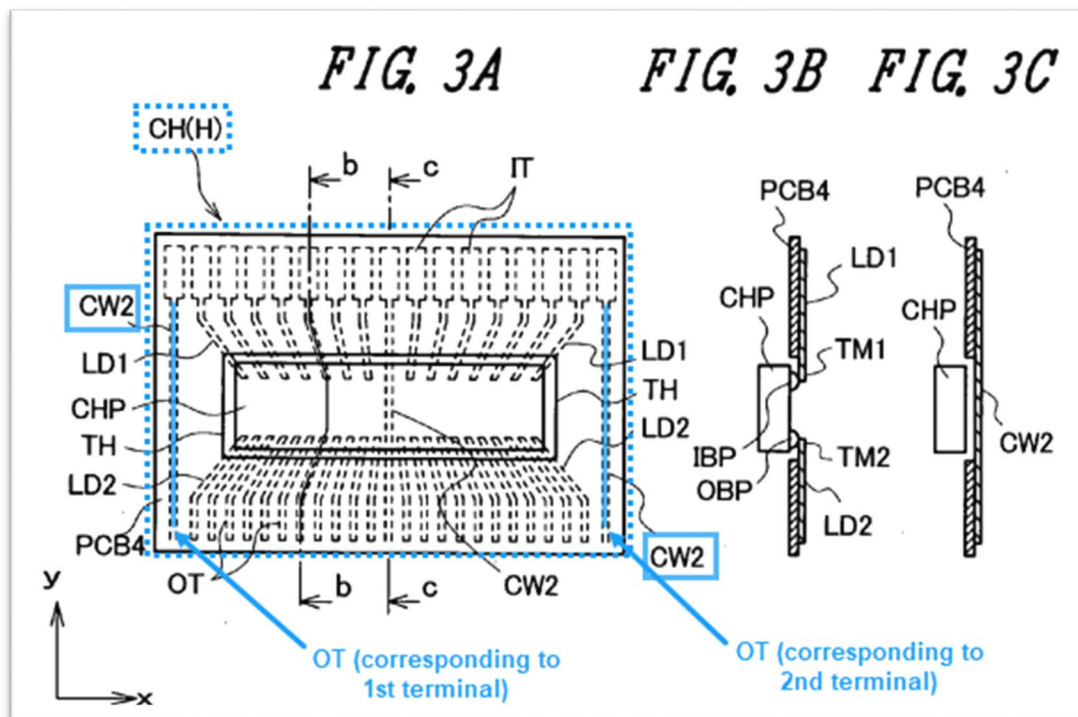
[3a] The electro-optical device according to claim 1, wherein: each of the first and second group of terminals configures a terminal group arranged in a predetermined direction, and

Takenaka discloses that the first and second groups of terminals are fixed on the LCD panel. (Murphy ¶107. *See also* Claims [1b], [1c].) As such, the order of

the terminals does not change, e.g., the first terminal is always on the left of the second terminal. (Murphy ¶107.) Accordingly, a POSITA would understand that the terminal groups are arranged in a predetermined direction. (Murphy ¶107.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [3a]. (Murphy ¶107.)

[3b] the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.

As shown in Figure 3A below, Takenaka discloses that common lines (CW2) are positioned on the sides of semiconductor device (CH(H)):

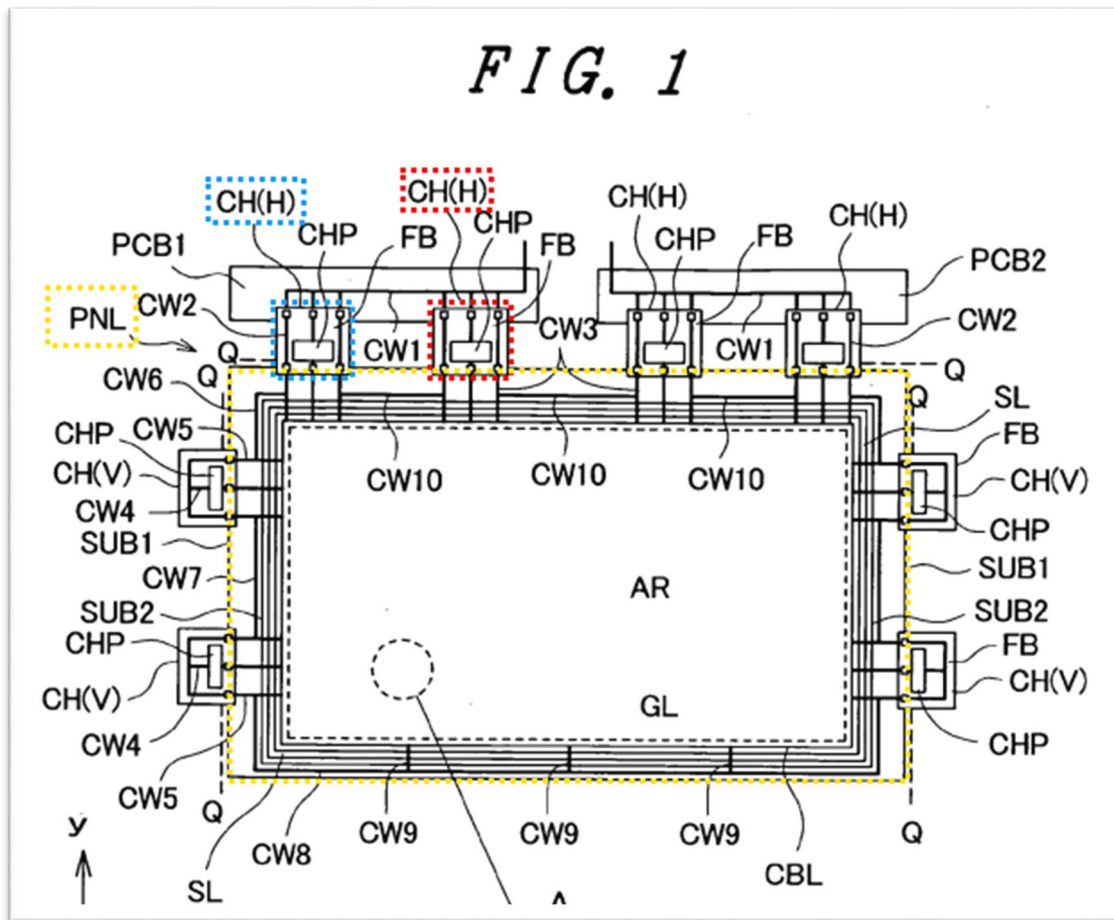


(Takenaka at [0081], Fig. 3A (annotated); Murphy ¶108.) The two output terminals at the ends of common lines (CW2) are also positioned at the sides of the semiconductor device, at the ends of the row of output terminals. (Takenaka at [0081], Fig. 3A; Murphy ¶108.) Accordingly, a POSITA would understand that the LCD panel's first and second terminals, and third and fourth terminals corresponding to these output terminals are at the ends of the first and second groups of terminals, respectively, in the predetermined direction. (Murphy ¶108.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [3b]. (Murphy ¶108.)

4. Dependent Claim 4

[4] The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.

As shown in Figure 1 below, Takenaka discloses multiple semiconductor devices (CH(H)) connected to the LCD panel (PNL) along its top side:

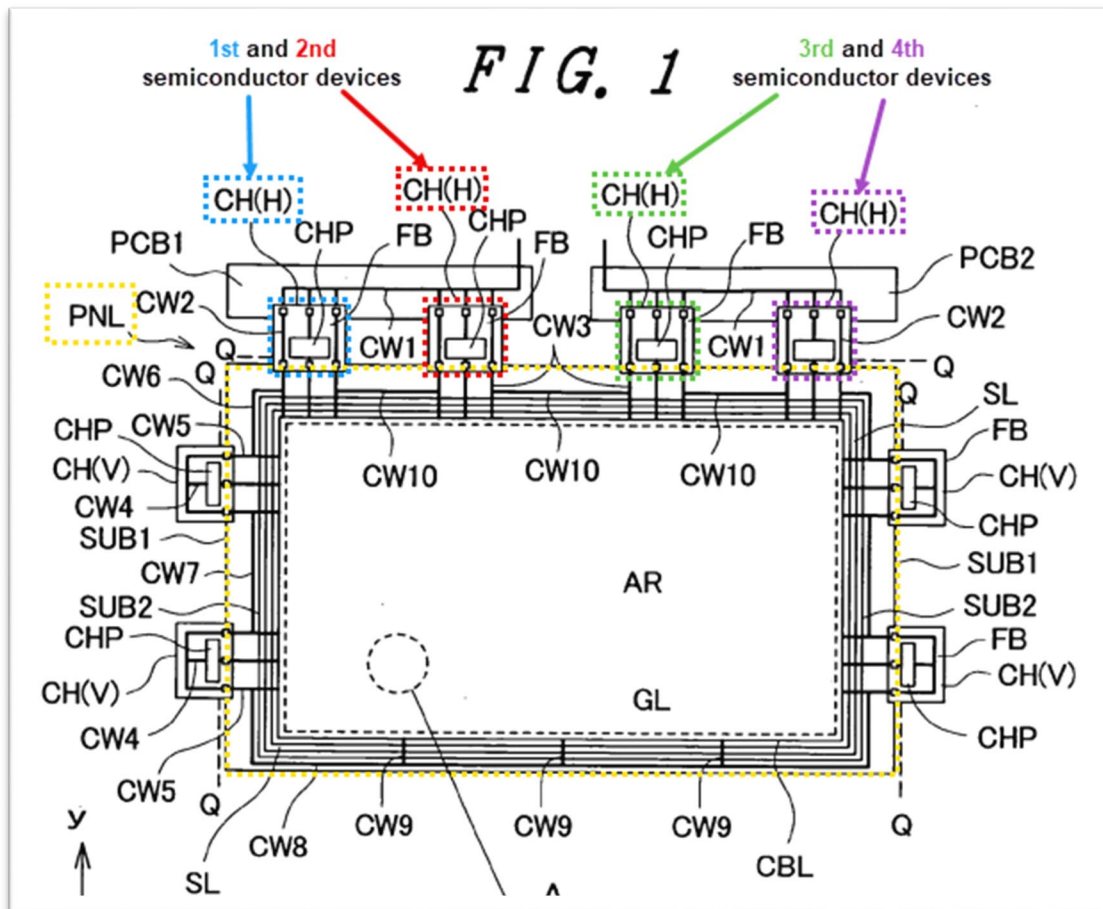


(Takenaka at [0028], Fig. 1 (annotated); Murphy ¶109.) The bottom side of the panel is a second side of a direction crossing the top side of the panel. (Murphy ¶109.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [4]. (Murphy ¶109.)

5. Dependent Claim 5

[5a] The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a fourth terminal portion having a fourth group of terminals arranged so as to be adjacent to the third terminal portion,

As shown in Figure 1 below, Takenaka discloses that the LCD panel is connected to two pairs of adjacent semiconductor devices (CH(H)):



(Takenaka at [0028], Fig. 1 (annotated); Murphy ¶110. *See also* Claims [1b], [1c], *supra*.) The two pairs of semiconductor devices are similar in structure and are similarly electrically connected to the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶110. *See also* Claims [1b], [1c], *supra*.) Thus, Takenaka discloses that the LCD panel has adjacent third and fourth terminal portions with third and fourth groups of terminals, respectively. (Murphy ¶110.) A

POSITA reading Takenaka would understand that Takenaka teaches Claim [5a].

(Murphy ¶110.)

[5b] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,

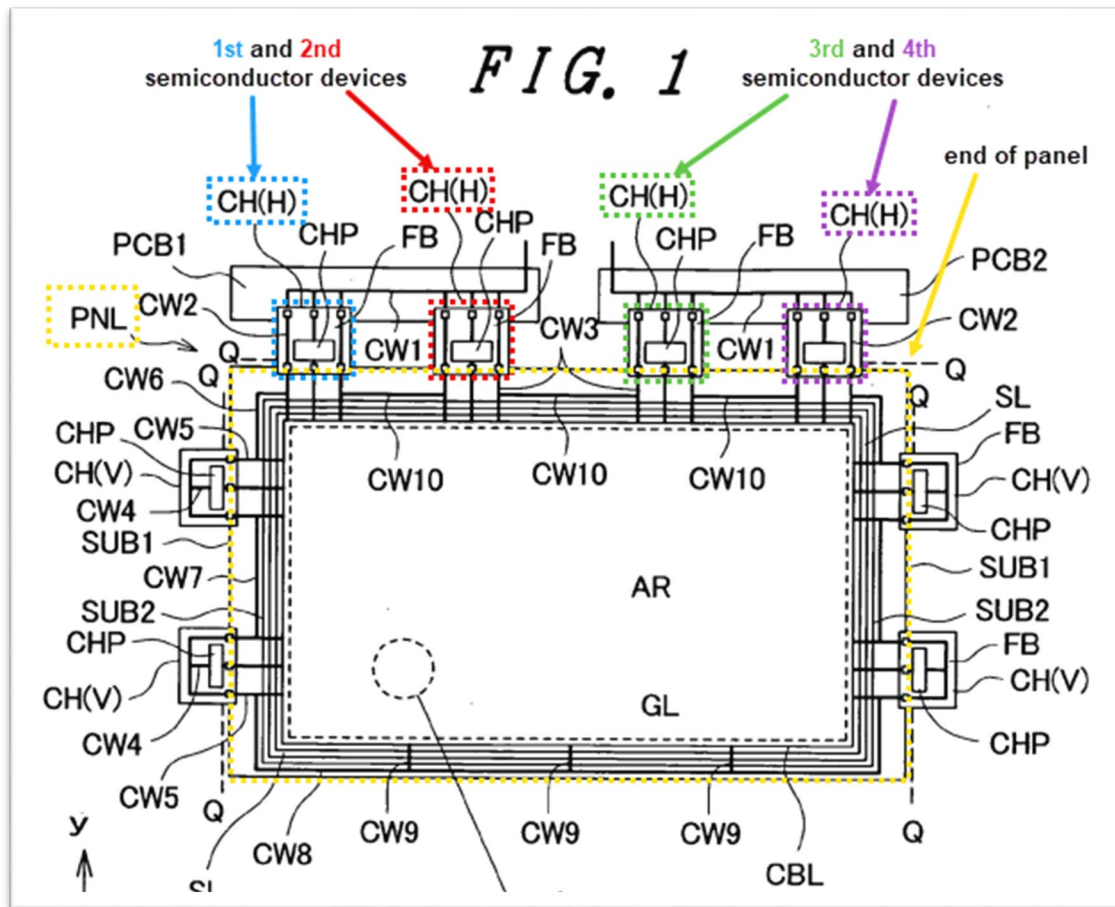
Takenaka discloses two pairs of semiconductor devices, each comprising a flexible board having output terminals that are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0041], [0076], [0081] Figs. 1, 3A; Murphy ¶111. *See also* Claims [1b], [1c], [1f], [1h], [5a] *supra*.)

A POSITA reading Takenaka would understand that Takenaka teaches Claim [5b].

(Murphy ¶111.)

[5c] the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel,

As shown in Figure 1 below, Takenaka discloses that the third and fourth semiconductor devices are respectively positioned between the first and second semiconductor devices and an end of the LCD panel:



(Takenaka at [0028], Fig. 1 (annotated); Murphy ¶112. *See also* Claims [1b], [1c], [5a], *supra*.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [5c]. (Murphy ¶112.)

[5d] the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and

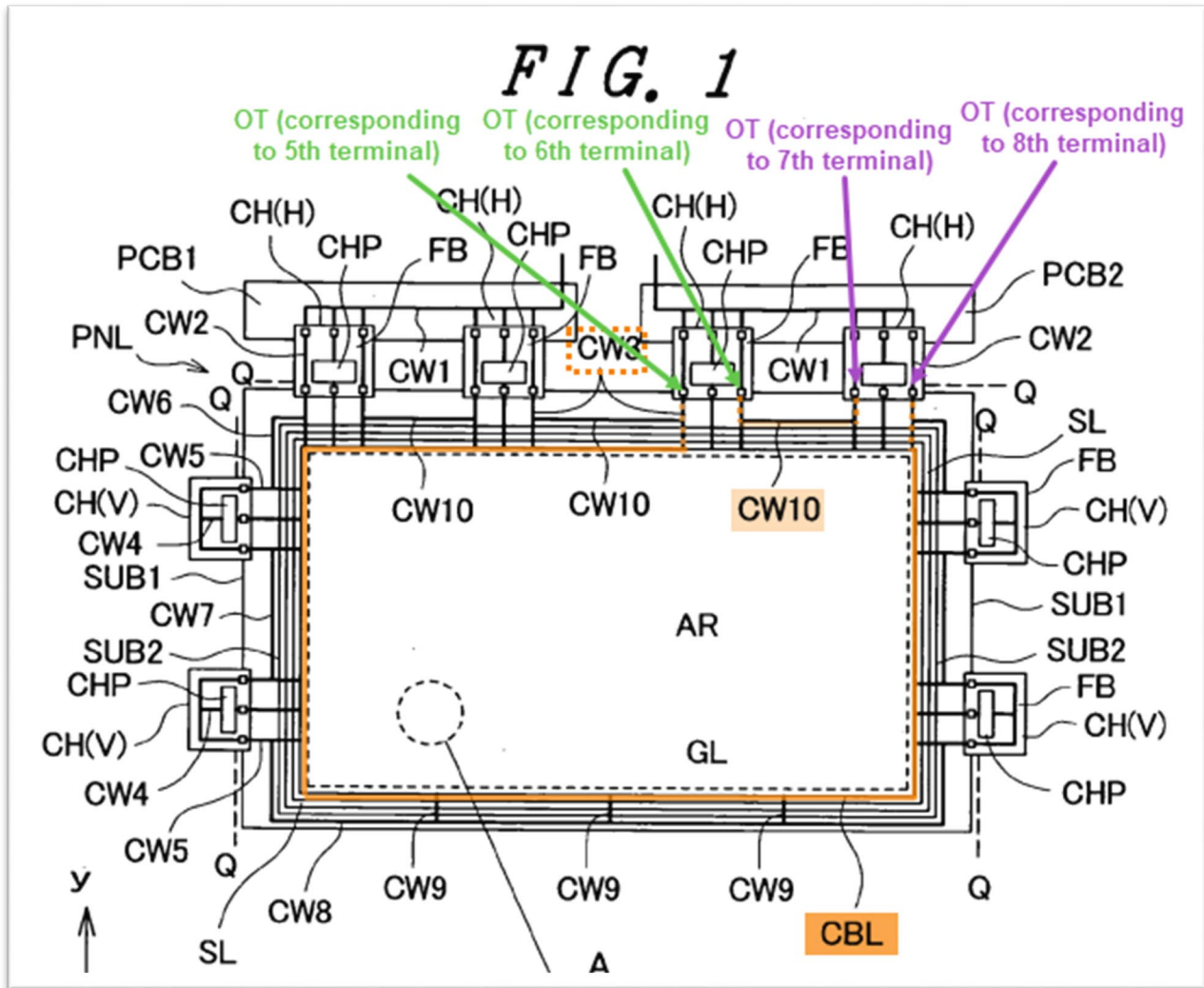
The two pairs of semiconductor devices are similar in structure and are similarly electrically connected to corresponding terminals on the LCD panel.

(Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶113. *See also* Claims

[1b], [1c], *supra.*) Accordingly, a POSITA would understand that the third and fourth groups of terminals on the LCD panel have fifth and sixth, and seventh and eighth terminals, respectively, that are each separated from one another. (Takenaka at [0071], [0076], [0081]; Murphy ¶113. *See also* Claims 1[b], 1[c], *supra.*) A POSITA reading Takenaka would understand that Takenaka teaches Claim [5d]. (Murphy ¶113.)

[5e] the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,

The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to provide a reference voltage signal to the LCD Panel. (Takenaka at [0037], [0056], [0058], [0070] Figs. 1, 3A; Murphy ¶114. *See also* Claims [1d], [1e], *supra.*) As shown in Figure 1 below, the fifth and eighth terminals are electrically connected, and the sixth and seventh terminals are electrically connected:



(Takenaka at [0007], [0076], [0081] Figs. 1 (annotated), 3A; Murphy ¶114. *See also* Claims [1d], [1e], *supra*.) Accordingly, a POSITA would understand that the fifth and eighth terminals are electrically connected through two common lines (CW3) and common bus line (CBL), whereas the sixth and seventh terminals are electrically connected through two common lines (CW3) and common line (CW10). (Murphy ¶114.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [5e]. (Murphy ¶114.)

[5f] the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and

The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶115. *See also* Claims [1b], [1c], [1g], [1i] *supra*.) Accordingly, a POSITA would understand that Takenaka discloses fifth and sixth external terminals on a semiconductor device that are respectively connected to the fifth and sixth terminals on the LCD panel through the panel's third connection terminal portion. (Murphy ¶115.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [5f]. (Murphy ¶115.)

[5g] the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.

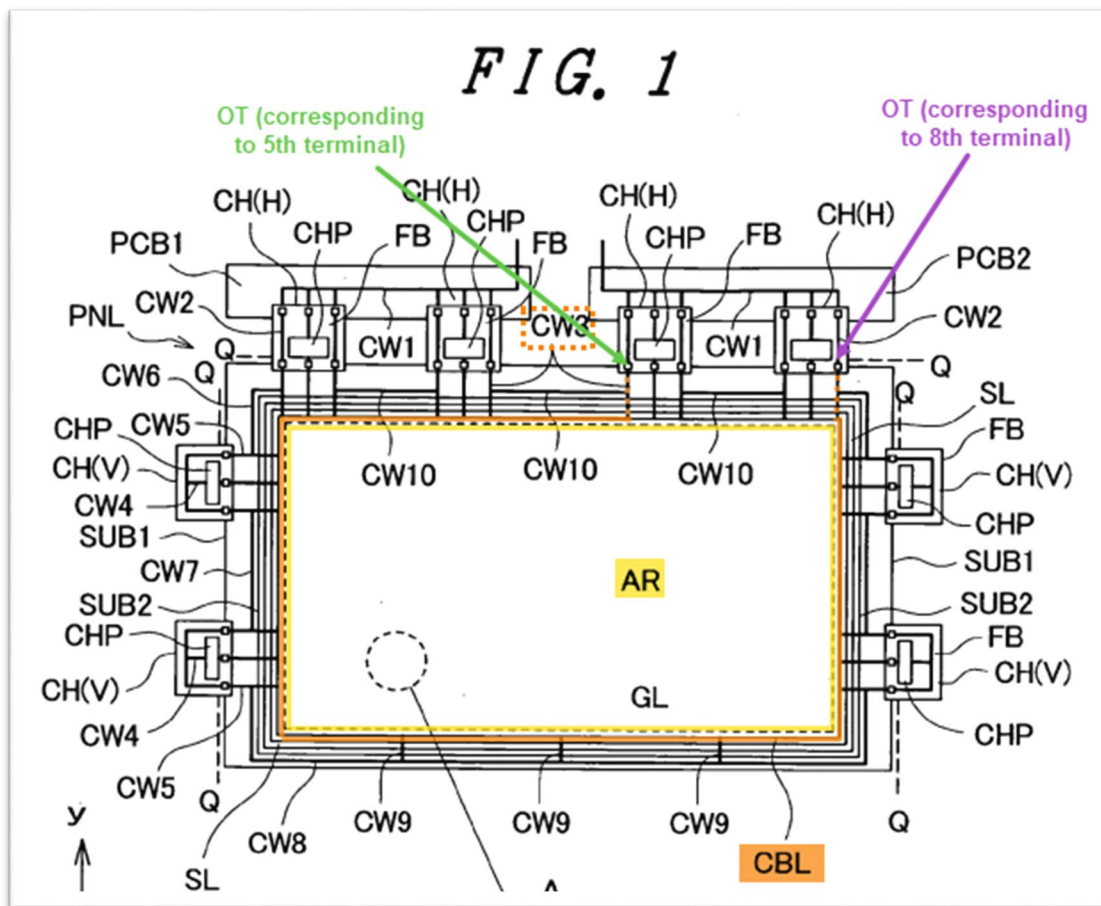
The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶116. *See also* Claims [1b], [1c], [1g], [1i] *supra*.) Accordingly, a POSITA would understand that Takenaka discloses seventh and eighth external terminals on a semiconductor device that are respectively connected to the seventh and eighth terminals on the LCD panel through the panel's fourth connection terminal portion. (Murphy ¶116.) A POSITA

reading Takenaka would understand that Takenaka teaches Claim [5g]. (Murphy ¶116.)

6. Dependent Claim 6

[6] *The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.*

As shown in Figure 1 below, the third connection wiring, comprising two common lines (CW3) and common bus line (CBL), extends around the circumference of display region (AR):



(Takenaka at [0030], [0037], [0073], Fig. 1 (annotated); Murphy ¶117. *See also* Claims [2], [5e], *supra.*) A POSITA reading Takenaka would understand that Takenaka teaches Claim [6]. (Murphy ¶117.)

7. Dependent Claim 7

[7a] The electro-optical device according to claim 5, wherein: each of the third and fourth group of terminals configures a terminal group arranged in a predetermined direction, and

The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶118. *See also* Claims 3[a], [5a], [5b], [5d], *supra.*) Accordingly, a POSITA would understand that the third and fourth group of terminals are each arranged in a predetermined direction. (Murphy ¶118.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [7a]. (Murphy ¶118.)

[7b] the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.

The two pairs of semiconductor devices are similar in terms of structure and how they are electrically connected to corresponding terminals on the LCD panel. (Takenaka at [0007], [0076], [0081] Figs. 1, 3A; Murphy ¶119. *See also* Claims 3[b], [5a], [5b], [5d], *supra.*) Accordingly, a POSITA would understand that the

LCD panel's fifth and sixth terminals, and seventh and eighth terminals are at the ends of the third and fourth groups of terminals, respectively, in the predetermined direction. (Murphy ¶119.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [7b]. (Murphy ¶119.)

11. Independent Claim 11

[11pre] An electro-optical panel comprising:

To the extent the preamble is limiting, it is taught by Takenaka. (Murphy ¶120.) Takenaka discloses a “liquid-crystal display device [that] includes a **liquid-crystal display panel**[.]” (Takenaka at Abstract; Murphy ¶120. *See also* Claim [1a].)

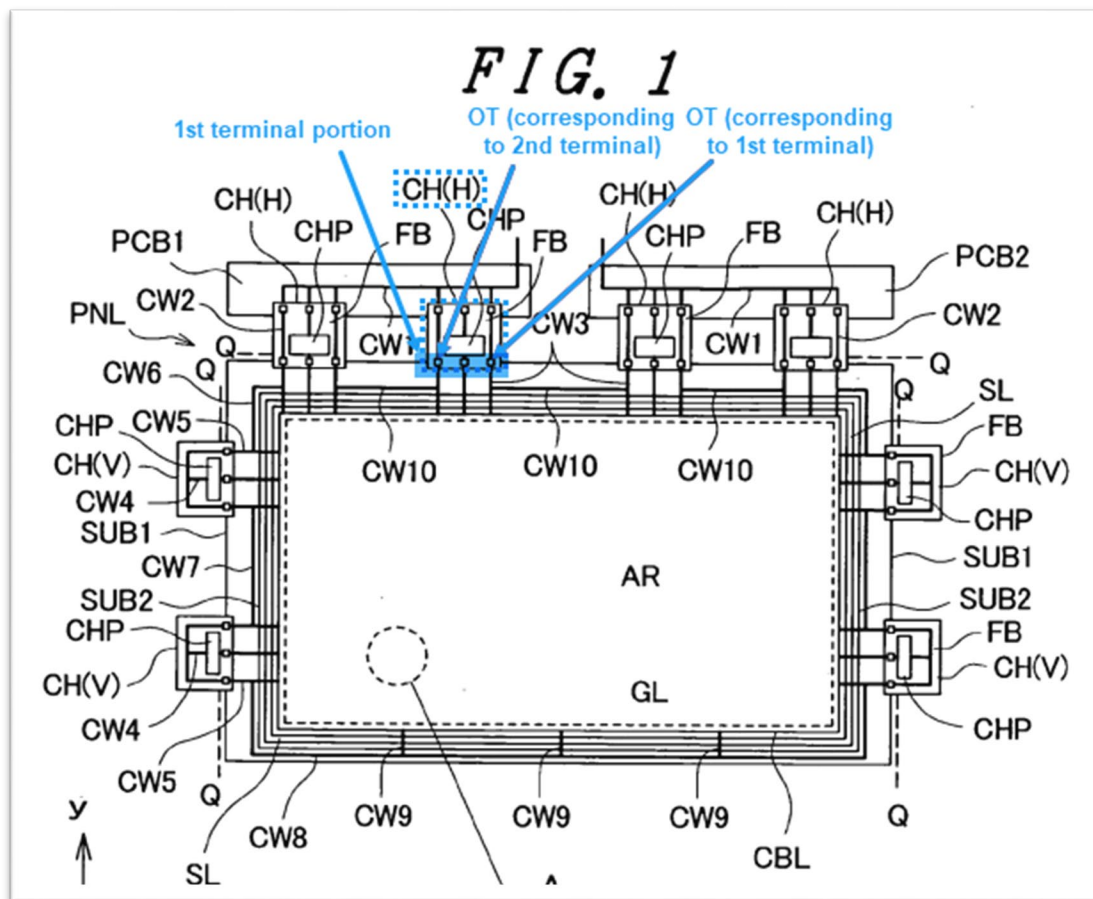
[11a] a substrate;

Takenaka discloses that the LCD panel “is structured with an envelope including a **substrate SUB1** (lower substrate in the figure) and a substrate SUB2 (upper substrate in the figure)[.]” (Takenaka at [0026]; Murphy ¶121.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11a]. (Murphy ¶121.)

[11b] a first terminal portion including a first group of terminals having a first terminal and a second terminal separated from each other;

Claim [11b] is substantially similar to Claim [1b], discussed in Section VIII.A.1. (Murphy ¶122.)

Here, however, the first terminal portion, first group of terminals, and first and second terminals are designated in relation to the middle, left semiconductor device, as shown in Figure 1 below:

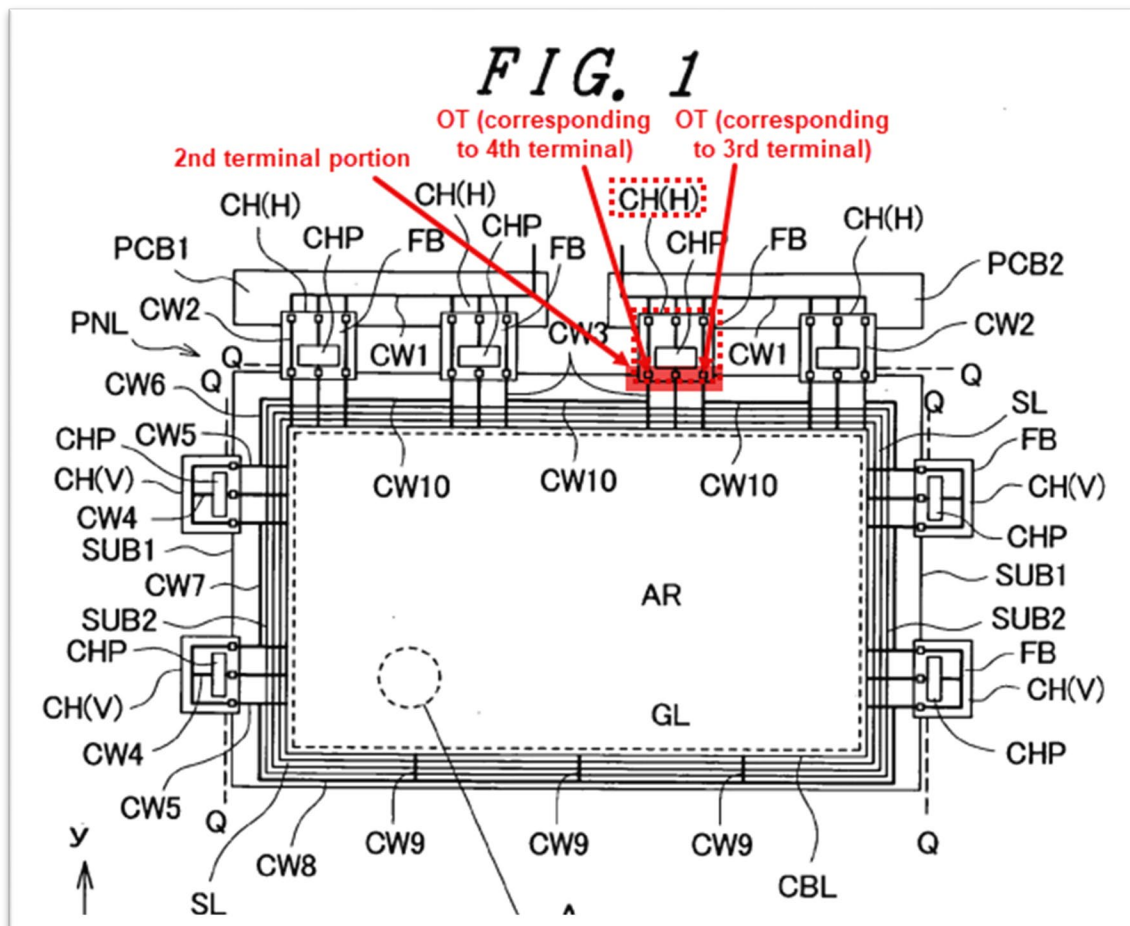


(Takenaka at Fig. 1 (annotated); Murphy ¶123. *See also* Claim [1b].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11b]. (Murphy ¶123.)

[11c] a second terminal portion arranged adjacent to the first terminal portion, the second terminal portion including a second group of terminals having a third terminal and a fourth terminal separated from each other;

Claim [11c] is substantially similar to Claim [1c], discussed in Section VIII.A.1. (Murphy ¶124.)

Here, however, the second terminal portion, second group of terminals, and third and fourth terminals are designated in relation to the middle, right semiconductor device, as shown in Figure 1 below:

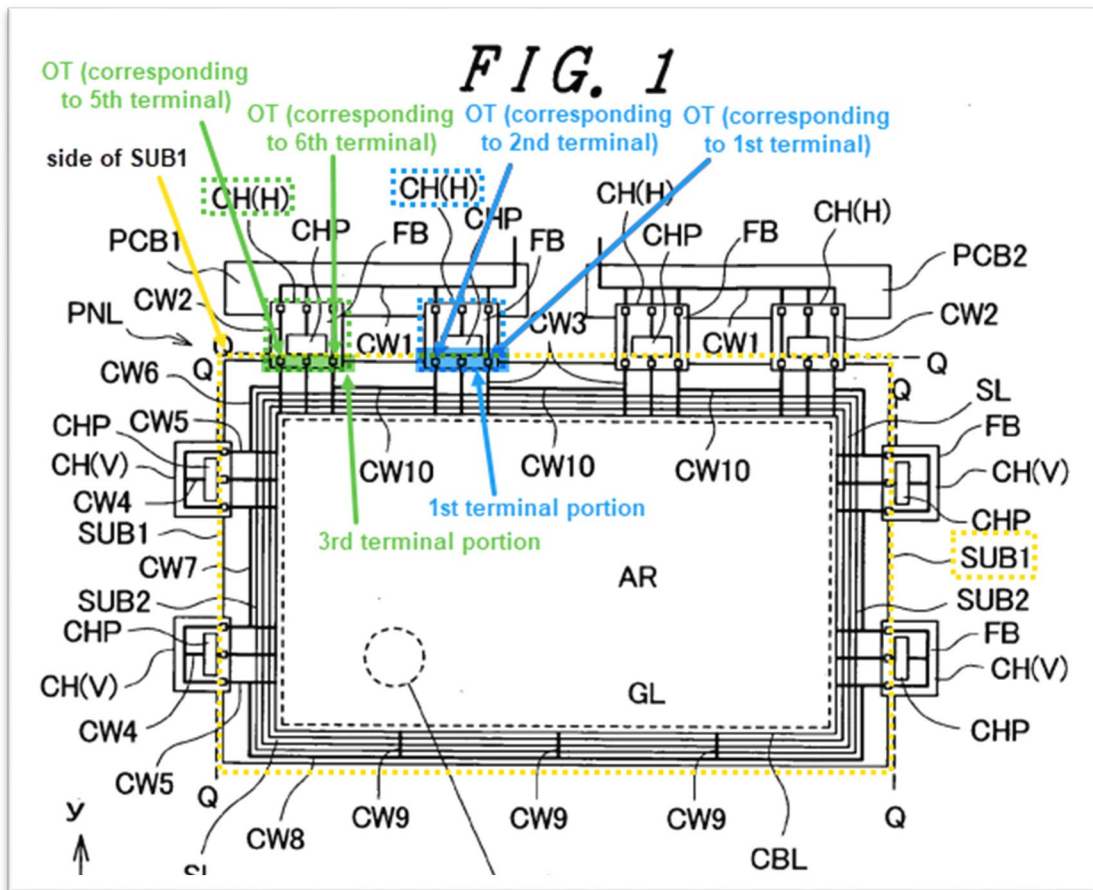


(Takenaka at Fig. 1 (annotated); Murphy ¶125. *See also* Claim [1c].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11c]. (Murphy ¶125.)

[11d] a third terminal portion arranged between one side of the substrate and the first terminal portion, the third terminal portion including a third group of terminals having a fifth terminal and a sixth terminal separated from each other;

Claim [11d] is substantially similar to the combination of Claims [5a], [5c] and [5d], discussed in Section VIII.A.5. (Murphy ¶126.) The only difference is that the third terminal portion is not required to be adjacent to the fourth terminal portion. (*Compare* Claim [11d] *with* Claims [5a], [5c] and [5d]; Murphy ¶126.)

Here, because the third terminal portion is not required to be adjacent to the fourth terminal portion, the third terminal portion, third group of terminals, and fifth and sixth terminals are designated in relation to the outer, left semiconductor device, as shown in Figure 1 below:

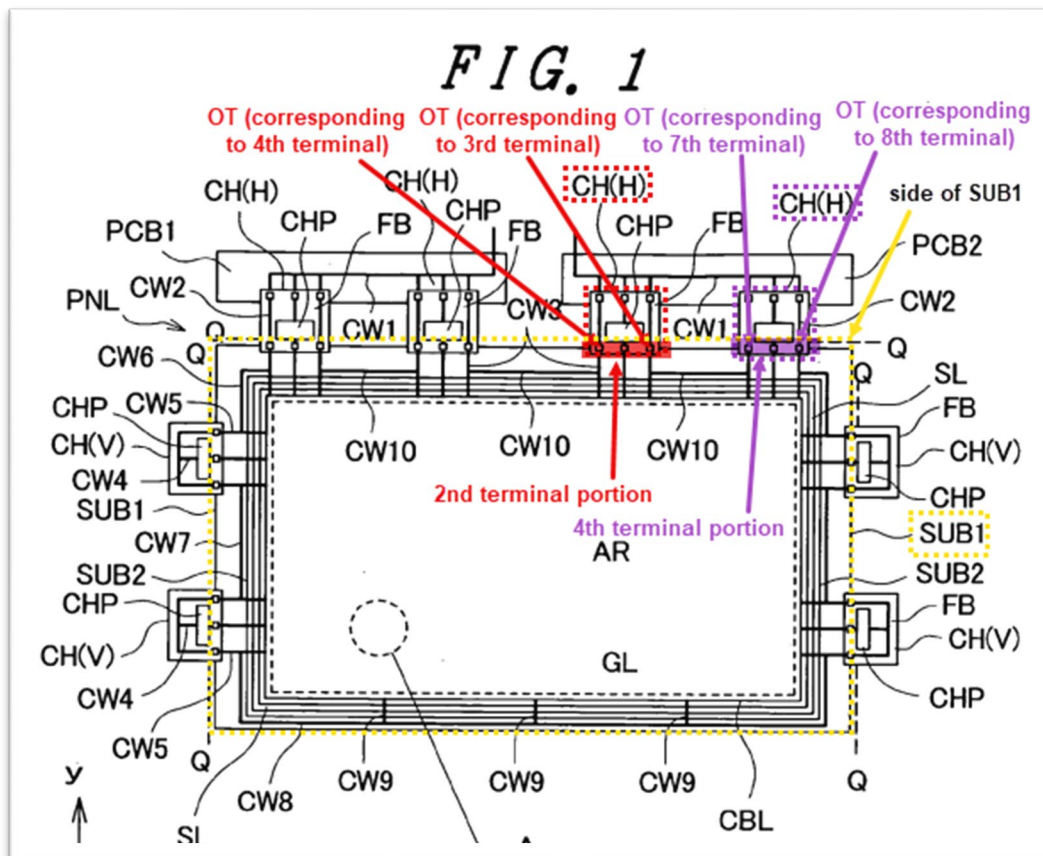


(Takenaka at Fig. 1 (annotated); Murphy ¶127. *See also* Claims [5a], [5c] and [5d].) In this arrangement, a POSITA would understand that the third terminal portion is between the first terminal portion and one side of the substrate (SUB1). (Murphy ¶127.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11d]. (Murphy ¶127.)

[11e] a fourth terminal portion arranged between one side of the substrate and the second terminal portion, the fourth terminal portion including a fourth group of terminals having a seventh terminal and a eighth terminal separated from each other;

Claim [11e] is substantially similar to the combination of Claims [5a], [5c] and [5d], discussed in Section VIII.A.5. (Murphy ¶128.) The only difference is that the fourth terminal portion is not required to be adjacent to the third terminal portion. (*Compare* Claim [11e] *with* Claims [5a], [5c] and [5d]; Murphy ¶128.)

Here, because the fourth terminal portion is not required to be adjacent to the third terminal portion, the fourth terminal portion, fourth group of terminals, and seventh and eighth terminals are designated in relation to the outer, right semiconductor device, as shown in Figure 1 below:

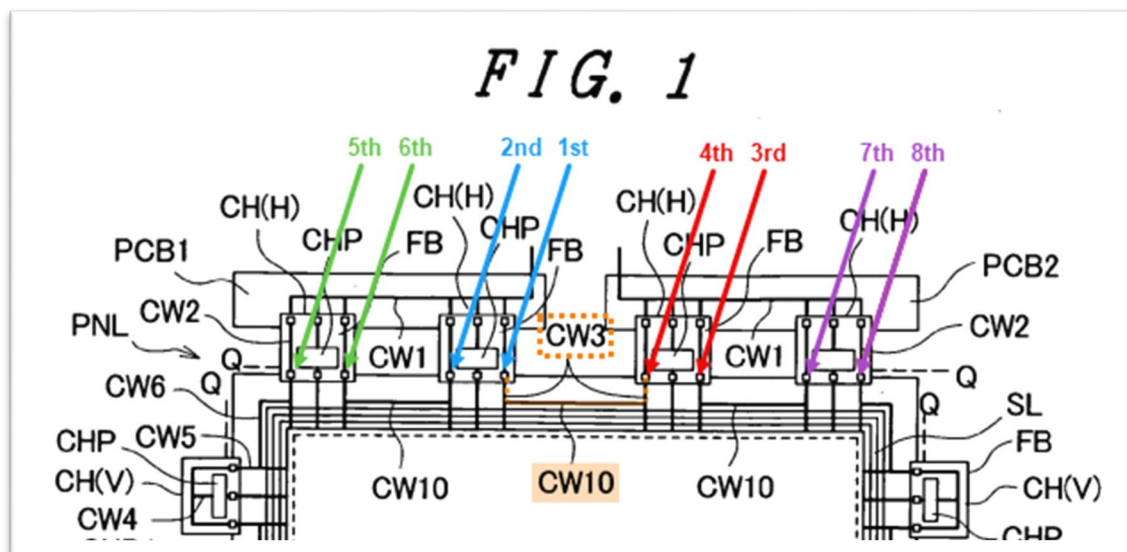


(Takenaka at Fig. 1 (annotated); Murphy ¶129. *See also* Claims [5a], [5c] and [5d].) In this arrangement, a POSITA would understand that the third terminal portion is between the first terminal portion and one side of the substrate (SUB1). (Murphy ¶129.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11e]. (Murphy ¶129.)

[11f] a first connection wiring configured to electrically connect the first terminal and the fourth terminal;

Claim [11f] is substantially similar to Claim [1d], discussed in Section VIII.A.1. (Murphy ¶130.)

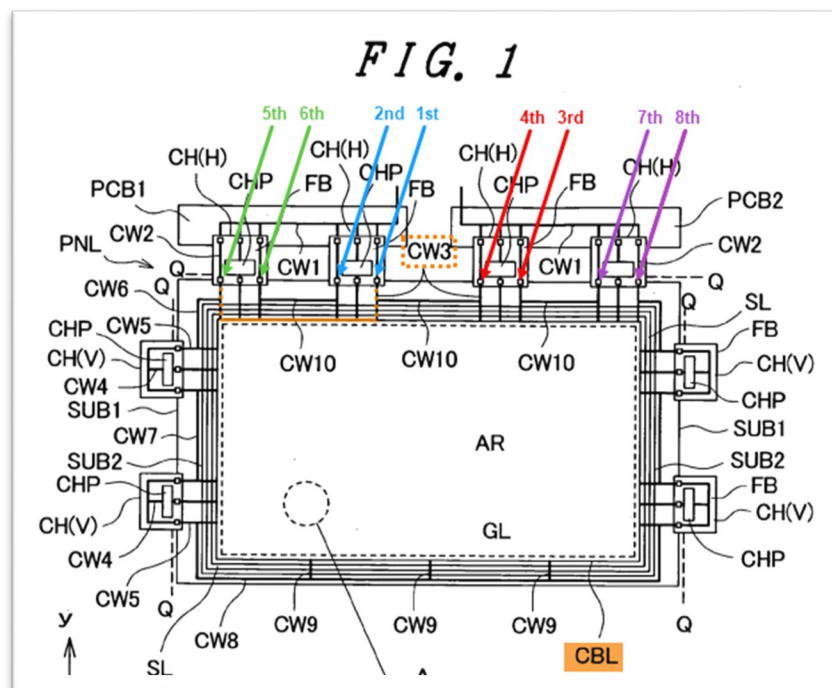
Here, however, the first and fourth terminals are electrically connected through two common lines (CW3) and common line (CW10), as shown in Figure 1 below:



(Takenaka at Fig. 1 (annotated); Murphy ¶131. *See also* Claim [1d].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11f]. (Murphy ¶131.)

[11g] a fifth connection wiring configured to electrically connect the first terminal and the fifth terminal;

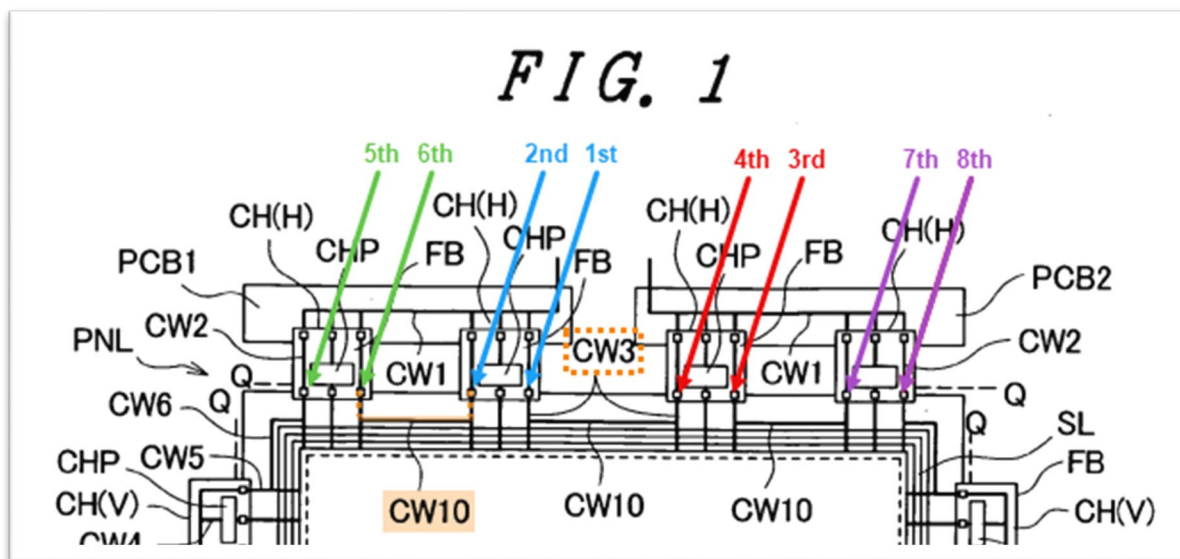
Claim [11d] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections VIII.A.1 and VIII.A.5. (Murphy ¶132.) The only difference, here, is that the first and fifth terminals are electrically connected. (*Compare* Claim [11g] *with* Claims [1d], [1e] and [5e]; Murphy ¶132.) As shown in Figure 1 below, the first and fifth terminals are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated); Murphy ¶132. *See also* Claims [1d], [1e] and [5e].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11g]. (Murphy ¶132.)

[11h] a sixth connection wiring configured to electrically connect the second terminal and the sixth terminal;

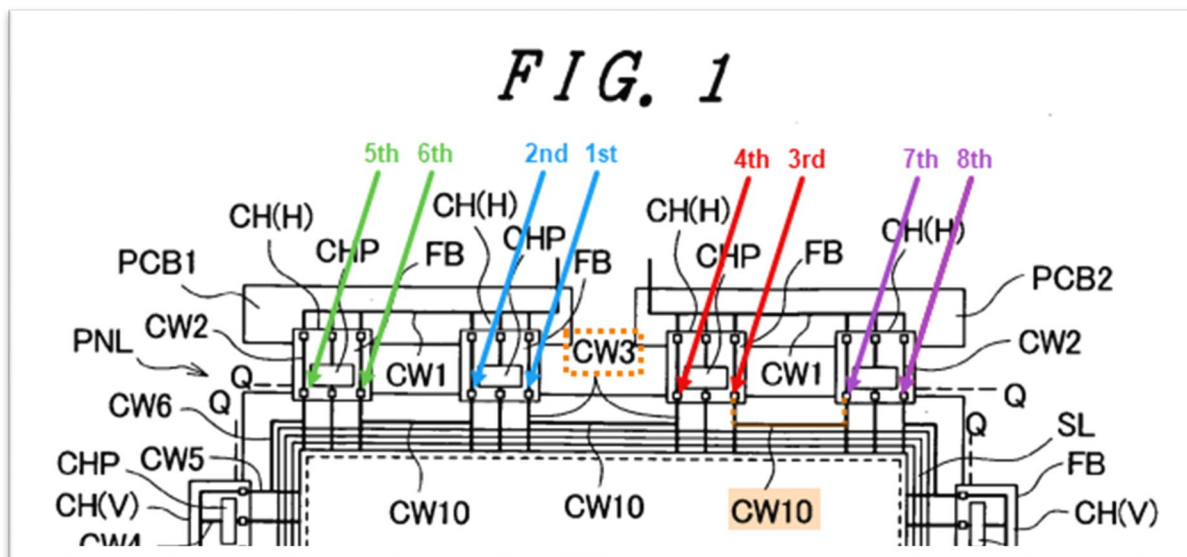
Claim [11h] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections VIII.A.1 and VIII.A.5. (Murphy ¶133.) The only difference, here, is that the second and sixth terminals are electrically connected. (*Compare* Claim [11h] *with* Claims [1d], [1e] and [5e]; Murphy ¶133.) As shown in Figure 1 below, the second and sixth terminals are electrically connected through two common lines (CW3) and common line (CW10):



(Takenaka at Fig. 1 (annotated); Murphy ¶133. *See also* Claims [1d], [1e] and [5e].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11h]. (Murphy ¶133.)

[11i] a seventh connection wiring configured to electrically connect the third terminal and the seventh terminal;

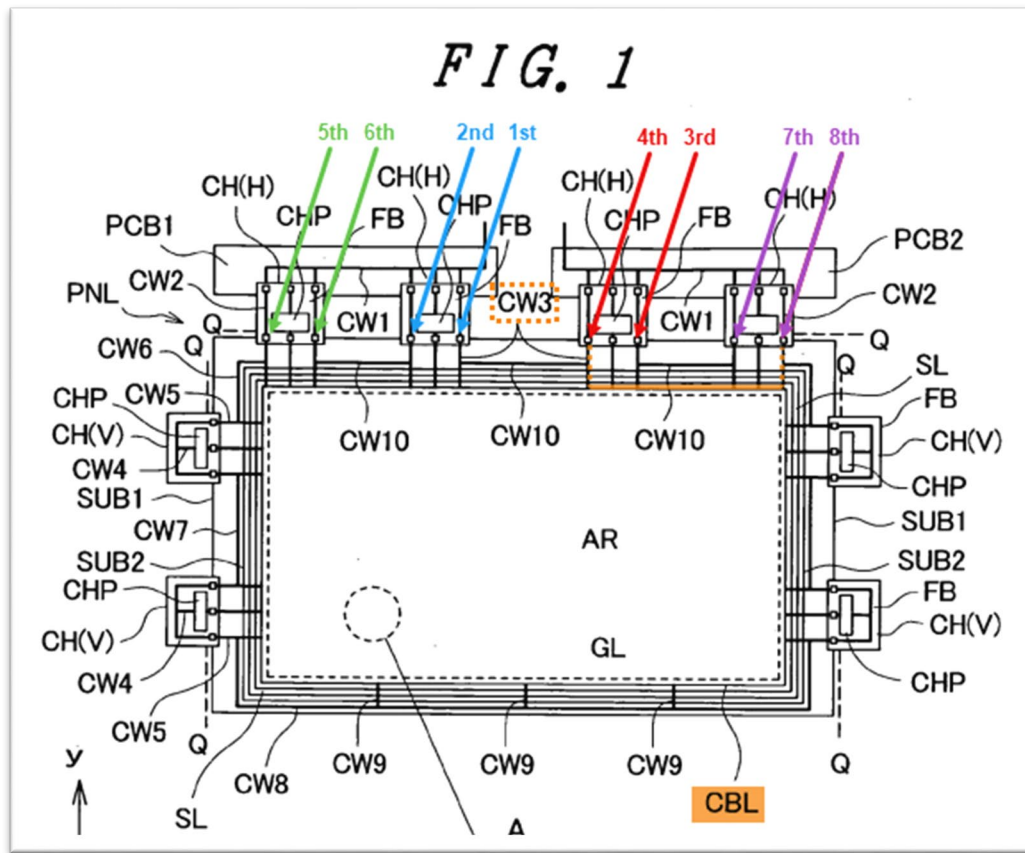
Claim [11i] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections VIII.A.1 and VIII.A.5. (Murphy ¶134.) The only difference, here, is that the third and seventh terminals are electrically connected. (*Compare* Claim [11i] *with* Claims [1d], [1e] and [5e]; Murphy ¶134.) As shown in Figure 1 below, the third and seventh terminals are electrically connected through two common lines (CW3) and common line (CW10):



(Takenaka at Fig. 1 (annotated); Murphy ¶134. *See also* Claims [1d], [1e] and [5e].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11i]. (Murphy ¶134.)

[11j] an eighth connection wiring configured to electrically connect the fourth terminal and the eighth terminal; and

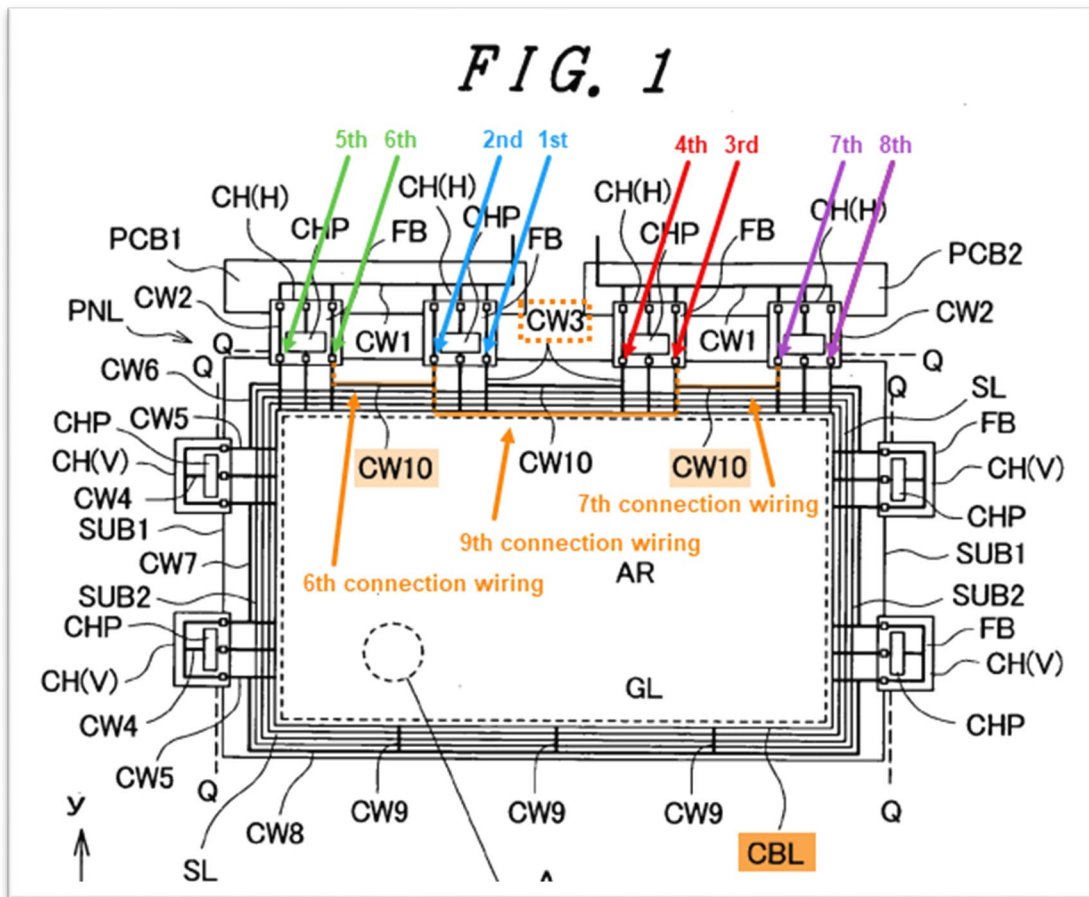
Claim [11j] is similar to the combination of Claims [1d], [1e] and [5e], discussed in Sections VIII.A.1 and VIII.A.5. (Murphy ¶135.) The only difference, here, is that the fourth and eighth terminals are electrically connected. (*Compare* Claim [11j] *with* Claims [1d], [1e] and [5e]; Murphy ¶135.) As shown in Figure 1 below, the fourth and eighth terminals are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated); Murphy ¶135. *See also* Claims [1d], [1e] and [5e].) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11j]. (Murphy ¶135.)

[11k] a ninth connection wiring configured to electrically connect the sixth connection wiring and the seventh connection wiring so as to electrically connect the second terminal, the third terminal, the sixth terminal and the seventh terminal.

As shown in Figure 1 below, Takenaka discloses that the sixth and seventh connection wirings are electrically connected through two common lines (CW3) and common bus line (CBL):



(Takenaka at Fig. 1 (annotated); Murphy ¶136. *See also* Claims [1d], [1e] and [5e].) Accordingly, a POSITA would understand that this ninth connection wiring electrically connects the second, third, sixth and seventh terminals. (Murphy ¶136.) A POSITA reading Takenaka would understand that Takenaka teaches Claim [11k]. (Murphy ¶136.)

12. Dependent Claim 12

[12a] *An electro-optical device comprising: the electro-optical panel according to claim 11;*

Claim [12a] is substantially similar to the combination of Claims [1pre] and [1a], discussed in Section VIII.A.1. (Murphy ¶137.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12a]. (Murphy ¶137.)

[12b] a first circuit substrate on which a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion is provided and

Claim [12b] is substantially similar to Claim [1f], discussed in Section VIII.A.1. (Murphy ¶138.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12b]. (Murphy ¶138.)

[12c] which has a first external terminal connected to the first terminal through the first connection terminal portion and a second external terminal connected to the second terminal;

Claim [12c] is substantially similar to Claim [1g], discussed in Section VIII.A.1. (Murphy ¶139.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12c]. (Murphy ¶139.)

[12d] a second circuit substrate on which a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion is provided and

Claim [12d] is substantially similar to Claim [1h], discussed in Section VIII.A.1. (Murphy ¶140.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12d]. (Murphy ¶140.)

[12e] which has a third external terminal connected to the third terminal through the second connection terminal portion and a fourth external terminal connected to the fourth terminal;

Claim [12e] is substantially similar to Claim [1i], discussed in Section VIII.A.1. (Murphy ¶141.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12e]. (Murphy ¶141.)

[12f] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided and

Claim [12f] is substantially similar to Claim [5b], discussed in Section VIII.A.5. (Murphy ¶142.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12f]. (Murphy ¶142.)

[12g] which has a fifth external terminal connected to the fifth terminal through the third connection terminal portion and a sixth external terminal connected to the sixth terminal; and

Claim [12g] is substantially similar to Claim [5f], discussed in Section VIII.A.5. (Murphy ¶143.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12g]. (Murphy ¶143.)

[12h] a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided and

Claim [12h] is substantially similar to Claim [5b], discussed in Section VIII.A.5. (Murphy ¶144.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12h]. (Murphy ¶144.)

[12i] which has a seventh external terminal connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal connected to the eighth terminal.

Claim [12i] is substantially similar to Claim [5g], discussed in Section VIII.A.5. (Murphy ¶145.) Thus, a POSITA reading Takenaka would understand that Takenaka teaches Claim [12j]. (Murphy ¶145.)

B. Ground 2: Claims 8-10 are Obvious over Takenaka and Ito and in further view of the Knowledge of a Skilled Artisan

Claims 8-10 are directed to an electro-optical device wherein a third terminal portion is “arranged on a side opposed to a display region with respect to the first terminal portion.” (’020 Patent, cl. 8; Murphy ¶146.) Takenaka does not disclose an LCD device with terminal portions in this arrangement as it would be understood by a POSITA at the time of the ’020 Patent’s filing. (Murphy ¶146.) However, as discussed below, it would have been obvious to a POSITA to configure Takenaka’s terminal portions in Ito’s arrangement.

Motivation to Combine

A POSITA would have been motivated to combine the teachings of Takenaka with Ito. (Murphy ¶147.)

Both references were driven by the same market force: increasing the number of terminals on the LCD panel to improve display quality. (Takenaka at [0011] (“[B]y reason of the increasing number of pixels . . . the number of terminals must be increased[.]”); Ito at [0041] (“[H]aving two ranks of external circuit connecting terminals . . . enables an increase in resolution while accommodating the need for minituraization”); Murphy ¶148.)

Moreover, both references offer solutions to reliability issues that arise from increasing the number of pixels, albeit in slightly different ways. (Murphy ¶149.) Takenaka proposes supplying a stable reference voltage signal to the pixels through a multiplicity of wirings, including some provided on the flexible boards of the semiconductor devices. (Takenaka at [0014], [0015], [0018], [0011], [0012], [0013]; Murphy ¶149.) Ito proposes offsetting the integrated circuits provided on the flexible substrates such that they do not overheat when driven. (Ito at [0005], [0008], [0011], [0014], [0042], [0046]; Murphy ¶149.)

Neither reference teaches away from the other. (Murphy ¶150.) While Ito describes its arrangement of the panel terminals being motivated by the miniaturization of panels, it expressly acknowledges the possibility of fitting three or more flexible substrates. (Ito at [0041], [0047]; Murphy ¶150.) This matches the number of Takenaka’s flexible substrates and, as such, a POSITA would not be discouraged from combining the references. (Murphy ¶150.)

Modifying Takenaka to configure the terminal portions in Ito’s arrangement would also be simple and obvious to try. (Murphy ¶151.) Takenaka teaches or renders obvious two terminal portions aligned parallel to the side of the panel. (Takenaka at Fig. 1; Murphy ¶151.) Ito teaches that terminal portions may be aligned perpendicular to the side of the panel: the one other possible arrangement given the shape and alignment of terminals on each terminal portion shown in both Takenaka and Ito. (Ito at Fig. 4; Murphy ¶151.) As a result, configuring Takenaka’s terminal portions in Ito’s arrangement would have been achieved with a reasonable expectation of success and involved simply repositioning the terminal portions. (Murphy ¶151.) *See Skedco, Inc. v. Strategic Operations, Inc.*, 287 F. Supp. 3d 1100, 1138 (D. Or. 2018) (when there is “market pressure to solve a problem, ***and there are a finite number of identified, predictable solutions***, a POSITA has motivation to ‘pursue the known options within his or her technical grasp’ and if this leads to anticipated success, it is likely not the product of innovation but of ordinary skill and common sense[.]”) (quoting *KSR*, 550 U.S. at 421).

8. Independent Claim 8

[8pre] An electro-optical device comprising:

Claim [8pre] is identical to Claim [1pre]. (Murphy ¶152.) For the reasons discussed in Section VIII.A.1, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8pre]. (Murphy ¶152.)

[8a] an electro-optical panel including:

Claim [8a] is identical to Claim [1a]. (Murphy ¶153.) For the reasons discussed in Section VIII.A.1, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8a]. (Murphy ¶153.)

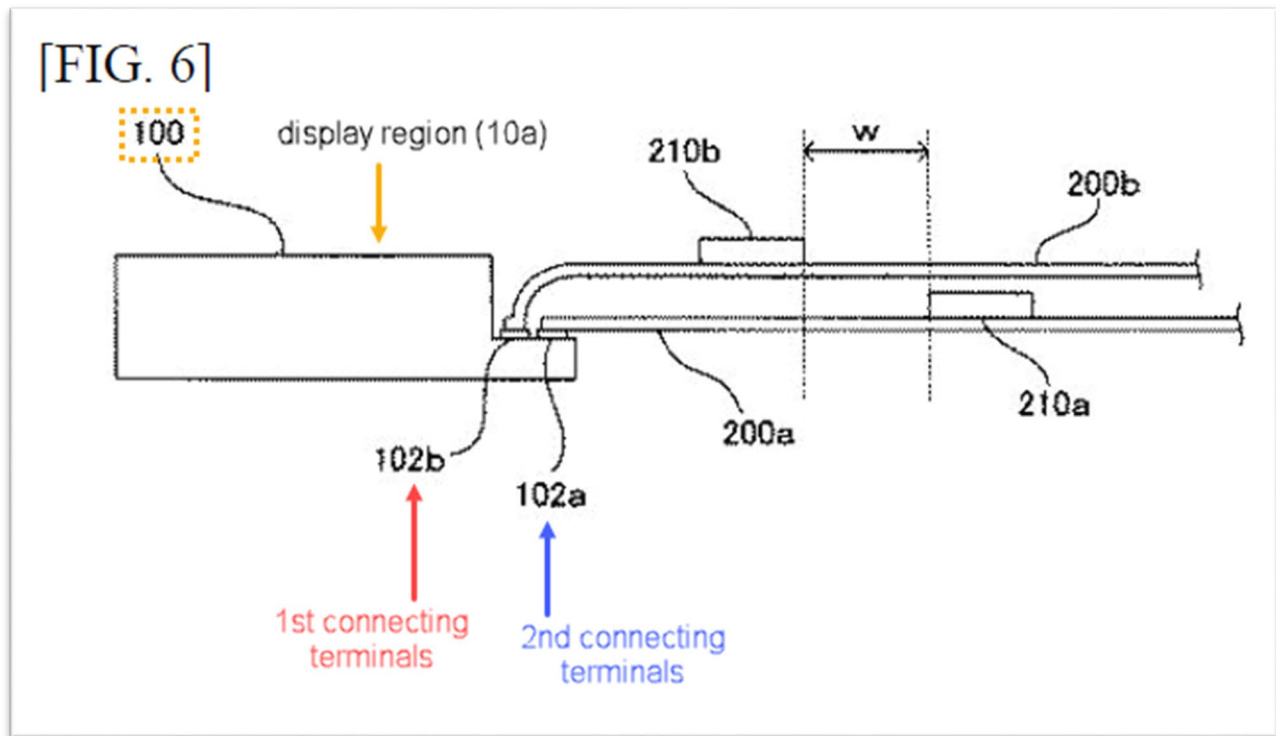
[8b] a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and

Claim [8b] is identical to Claim [1b]. (Murphy ¶154.) For the reasons discussed in Section VIII.A.1, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8b]. (Murphy ¶154.)

[8c] a third terminal portion arranged on a side opposed to a display region with respect to the first terminal portion, the third terminal portion having a third group of terminals, the third group of terminals including: a fifth terminal; and a sixth terminal separated from the fifth terminal,

Claim [8c] is similar to Claim [1c], discussed in Section VIII.A.1. (Murphy ¶155.) Here, however, a third terminal portion is arranged on a side opposed to a display region with respect to the first terminal portion. (Murphy ¶155.)

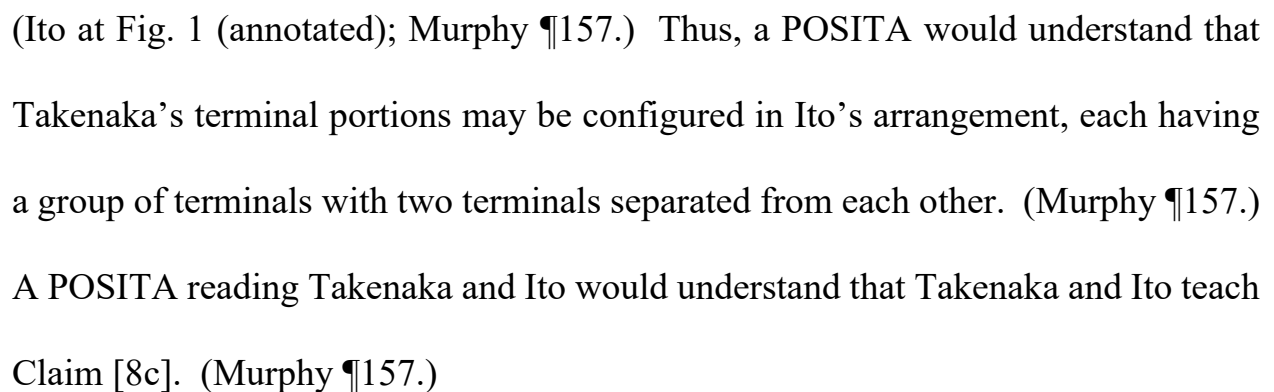
As shown in Figure 6, Ito discloses two rows of terminals (102a, 102b) on an electrical-optical panel (100) that has a display region (10a):



(Ito at [0036], Fig. 6 (annotated); Murphy ¶156.) The display region (10a) is positioned on one side of the first connecting terminals (102b), and the second connecting terminals (102a) are positioned on the other side as the display region. (Ito at [0025], Figs. 1, 4-6; Murphy ¶156.) In other words, the second connecting terminals are arranged on a side opposed to a display region with respect to the first terminal connecting terminals. (Murphy ¶156.)

An additional difference, here, is that Claim [1c]’s second terminal portion, second group of terminals, third terminal and fourth terminal are relabeled as Claim [8c]’s third terminal portion, third terminal group, fifth terminal and sixth terminal,

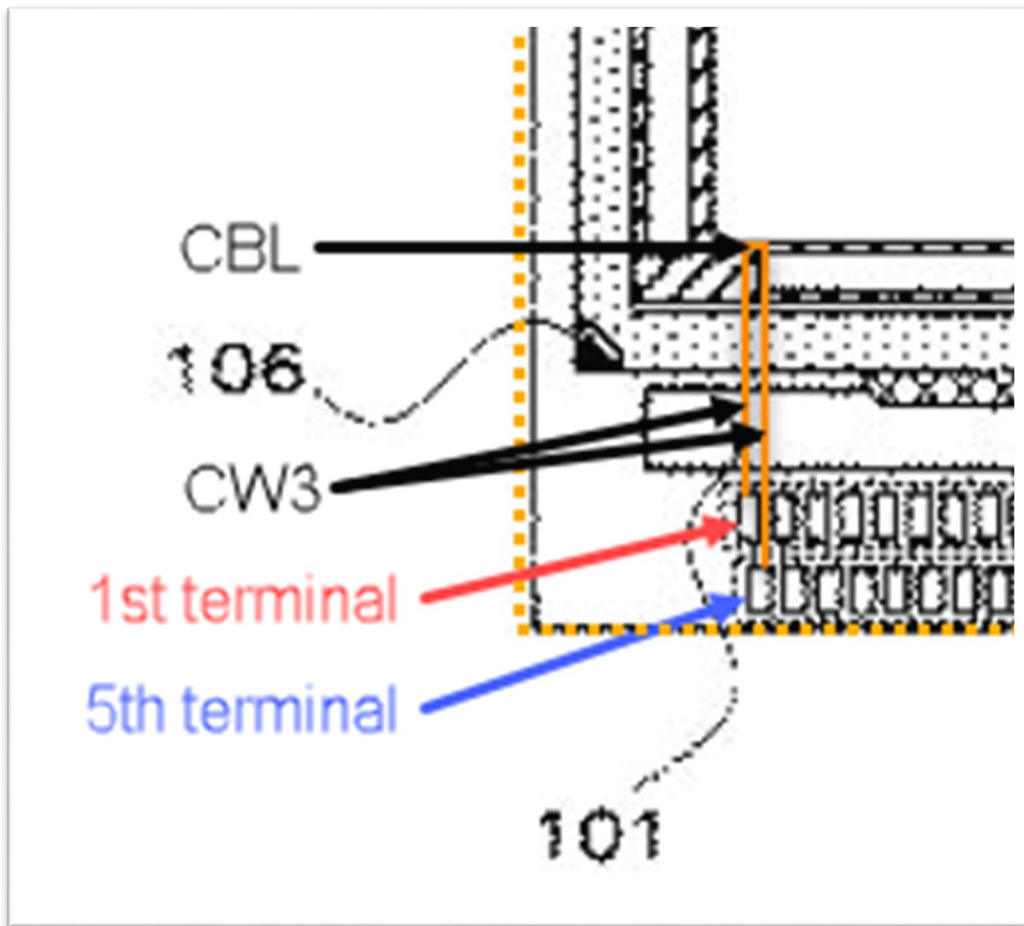
[FIG. 1]



[8d] the first terminal and the fifth terminal being electrically connected through a fifth connection wiring provided on the electro-optical panel,

Claim [8d] is similar to Claim [1d], discussed in Section VIII.A.1. (Murphy ¶158.) Here, however, the first terminal is connected to the fifth terminal by a fifth connection wiring. (Murphy ¶158.)

As demonstrated in Sections VIII.A.1, VIII.A.5 and VIII.A.11, Takenaka's LCD panel terminals are electrically connected by connection wiring comprised of some combination of common lines (CW3), and common line (CW10) or common bus line (CBL), no matter their arrangement. (Takenaka at Fig. 1; Murphy ¶159. *See also* Claims [1d], [1e], [5e], and [11f]-[11j], *supra*.) The same holds true for the first and fifth terminals, here. (Murphy ¶159.) As shown in Figure 1 below, the first and fifth terminals, configured in Ito's arrangement, are electrically connected by Takenaka's two common lines (CW3) and a portion of common bus line (CBL):

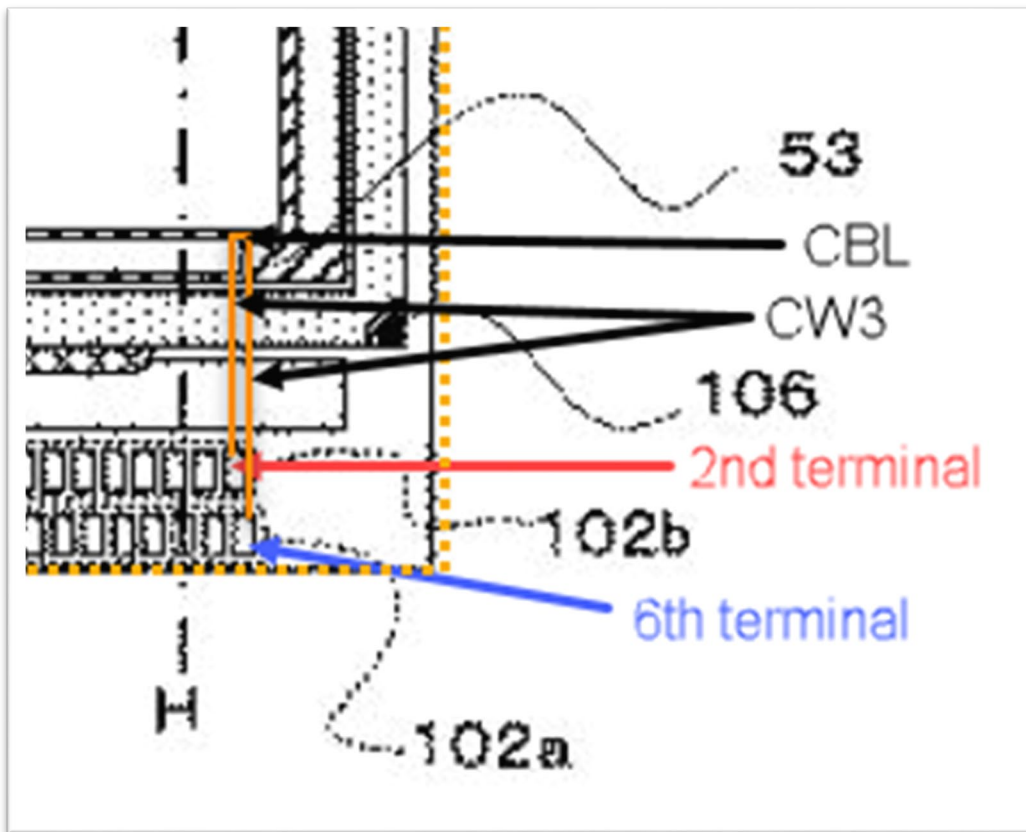


(Ito at Fig. 1 (annotated); Murphy ¶159.) Thus, a POSITA would understand that the first and fifth terminals are electrically connected by a fifth connection wiring provided on the electro-optical panel. (Murphy ¶159.) A POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8d]. (Murphy ¶159.)

[8e] the second terminal and the sixth terminal being electrically connected through a sixth connection wiring provided on the electro-optical panel;

Claim [8e] is similar to Claim [1e], discussed in Section VIII.A.1. (Murphy ¶160.) Here, however, the second terminal is connected to the sixth terminal by a sixth connection wiring. (Murphy ¶160.)

As demonstrated in Sections VIII.A.1, VIII.A.5 and VIII.A.11, Takenaka's LCD panel terminals are electrically connected by connection wiring comprised of some combination of common lines (CW3), and common line (CW10) or common bus line (CBL), no matter their arrangement. (Takenaka at Fig. 1; Murphy ¶161. *See also* Claims [1d], [1e], [5e], [8d] and [11f]-[11j], *supra*.) The same holds true for the second and sixth terminals, here. (Murphy ¶161.) As shown in Figure 1 below, the second and sixth terminals, configured in Ito's arrangement, are electrically connected by Takenaka's two common lines (CW3) and common bus line (CBL):



(Ito at Fig. 1 (annotated); Murphy ¶161.) Thus, a POSITA would understand that the second and sixth terminals are electrically connected by a sixth connection wiring provided on the electro-optical panel. (Murphy ¶161.) A POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8e]. (Murphy ¶161.)

[8f] a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;

Claim [8f] is identical to Claim [1f]. (Murphy ¶162.) For the reasons discussed in Section VIII.A.1, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8f]. (Murphy ¶162.)

[8g] a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion respectively; and

Claim [8g] is identical to Claim [1g]. (Murphy ¶163.) For the reasons discussed in Section VIII.A.1, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8g]. (Murphy ¶163.)

[8h] a third circuit substrate including: a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion;

Claim [8h] is substantially similar to Claim [1h], discussed in Section VIII.A.1. (Murphy ¶164.) The only differences, here, are that Claim [1h]’s second circuit substrate, second connection terminal portion and second group of connection terminals are relabeled as Claim [8h]’s third circuit substrate, third connection terminal portion and third group of connection terminals, respectively. (*Compare Claim [8h] with Claim [1h];* Murphy ¶164.) Thus, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8h]. (Murphy ¶164.)

[8i] a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion; and a sixth external terminal electrically

connected to the sixth terminal through the third connection terminal portion.

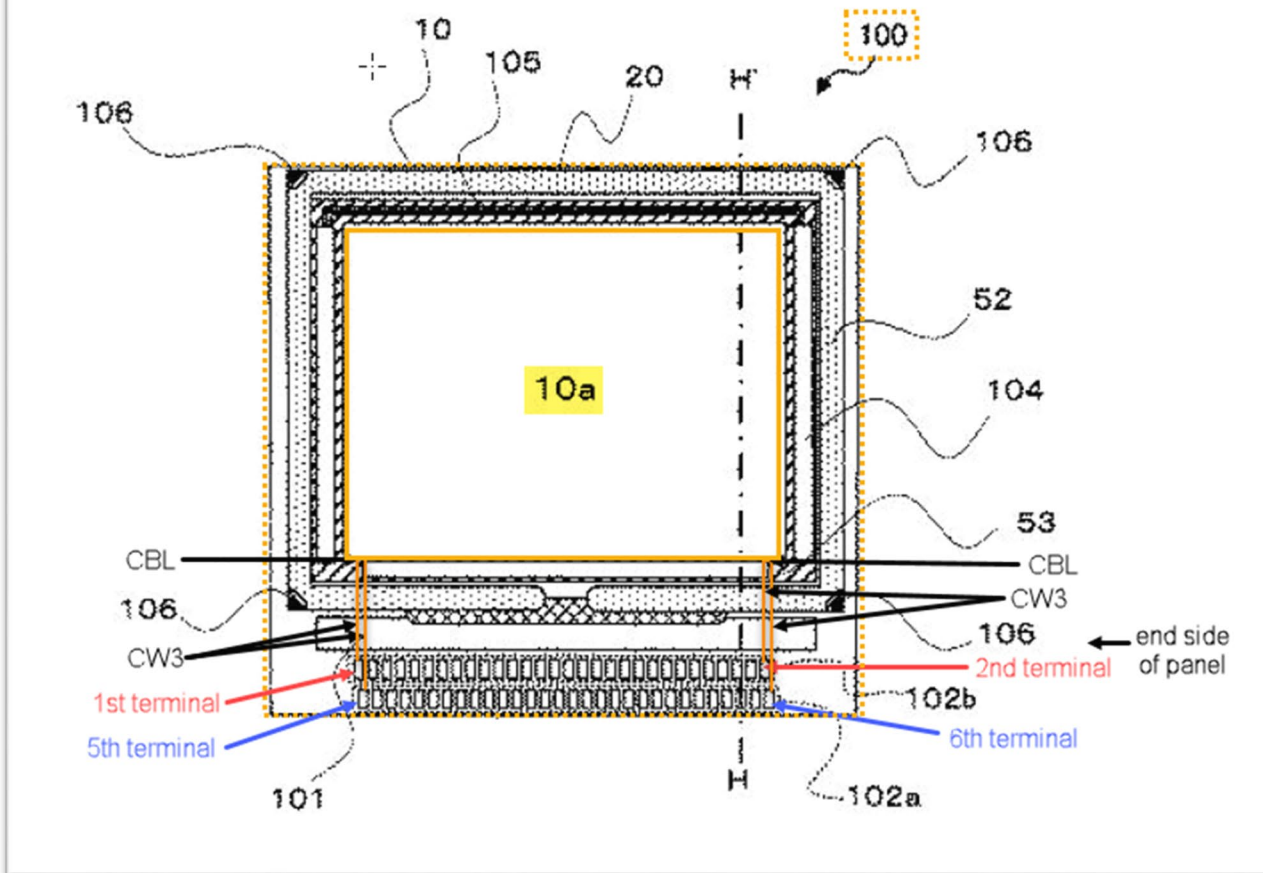
Claim [8i] is substantially similar to Claim [1i], discussed in Section VIII.A.1. (Murphy ¶165.) The only differences, here, are that Claim [1i]'s third and fourth external terminals are relabeled as Claim [8i]'s fifth and sixth external terminals, respectively. (*Compare* Claim [8i] *with* Claim [1i]; Murphy ¶165.) Thus, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [8i]. (Murphy ¶165.)

9. Dependent Claim 9

[9] The electro-optical device according to claim 8, wherein the fifth connection wiring and the sixth connection wiring are provided at an end side of the electro-optical panel rather than the display region.

As shown in Figure 1 below, the fifth and sixth connection wiring are provided at an end side of the LCD panel rather than the display region (10a):

[FIG. 1]



(Ito at Fig. 1 (annotated); Murphy ¶166.) A POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [9]. (Murphy ¶166.)

10. Dependent Claim 10

[10a] The electro-optical device according to claim 8, wherein: each of the first and third group of terminals configures a terminal group arranged in a predetermined direction, and

Claim [10a] is substantially similar to Claim [3a], discussed in Section VIII.A.3. (*Compare* Claim [10a] *with* Claim [3a]; Murphy ¶167.) Thus, a POSITA

reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [10a]. (Murphy ¶167.)

[10b] the first terminal and the second terminal, and the fifth terminal and the sixth terminal are provided at both end sides of the predetermined direction of the terminal group.

Claim [10b] is substantially similar to Claim [3b], discussed in Section VIII.A.3. (*Compare* Claim [10b] *with* Claim [3b]; Murphy ¶168.) Thus, a POSITA reading Takenaka and Ito would understand that Takenaka and Ito teach Claim [10b]. (Murphy ¶168.)

C. Ground 3: Claims 1-7 and 13 are Obvious over Takemura

Claims 1-7 and 13 would have been obvious in view of Takemura to a person of ordinary skill at the time of the '020 Patent's filing. (Murphy ¶169.) *Game & Tech*, 926 F.3d at 1381; *SIBIA*, 225 F.3d at 1356. Specifically, and as explained in greater detail below, claims 1-7 and 13 recite LCD devices and LCD panels having various configurations of connection wirings, and it would have been obvious for a POSITA to arrive at the claimed configurations in view of Takemura.

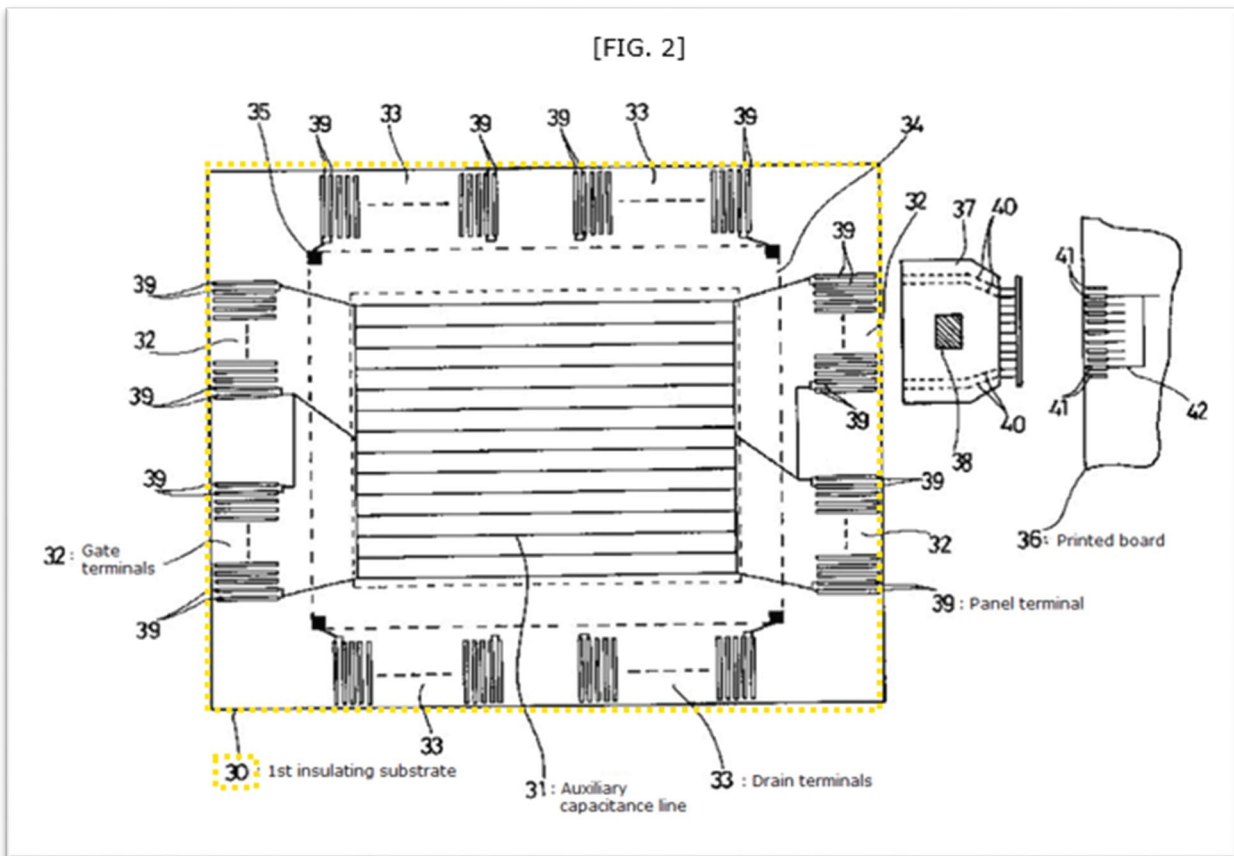
1. Independent Claim 1

[1pre] "An electro-optical device comprising:"

To the extent the preamble is limiting, it is taught by Takemura. Takemura discloses a "*liquid crystal display device*." (Takemura at [0001]; Murphy ¶170.)

[1a] "an electro-optical panel including:"

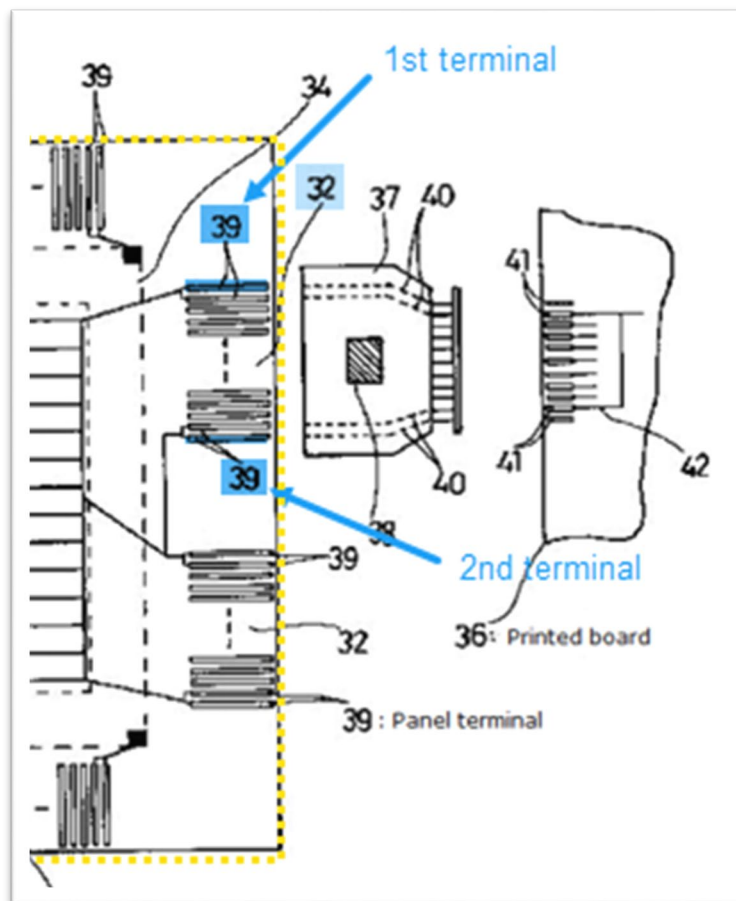
Takemura discloses a liquid crystal display device configured with a “*liquid crystal panel*.” (Takemura at [0001]; Murphy ¶171.) As shown in Figure 2 below, the LCD panel “is composed of a transparent first insulating substrate (30) and a transparent opposing substrate facing each other, with liquid crystals injected between them.”:



(Takemura at [0021], Fig. 2 (annotated); Murphy ¶171.) A POSITA reading Takemura would understand that Takemura teaches Claim [1a]. (Murphy ¶171.)

[1b] “a first terminal portion having a first group of terminals, the first group of terminals including: a first terminal; and a second terminal separated from the first terminal; and”

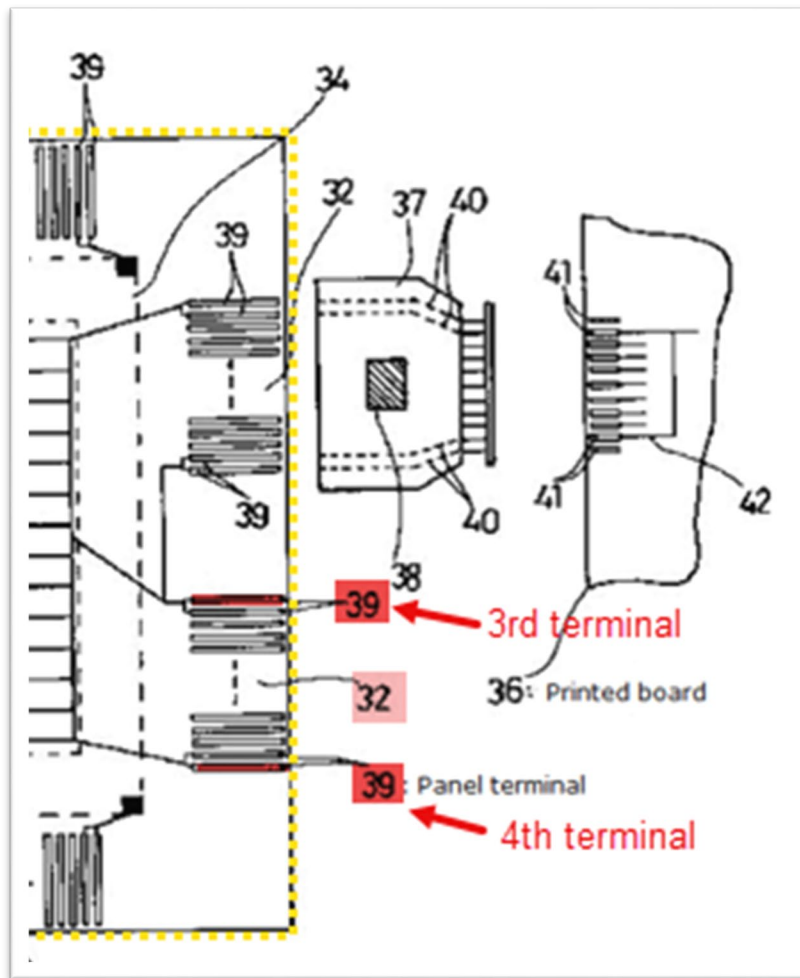
As shown in Figure 2 below, Takemura discloses that a first portion of the LCD panel has “*panel terminals (39) [] provided at both ends of a gate terminal group (32)*”:



(Takemura at [0029], Fig. 2 (annotated); Murphy ¶172.) A POSITA reading Takemura would understand that Takemura teaches Claim [1b]. (Murphy ¶172.)

[1c] “a second terminal portion arranged adjacent to the first terminal portion and having a second group of terminals, the having second group of terminals including: a third terminal; and a fourth terminal separated from the third terminal”

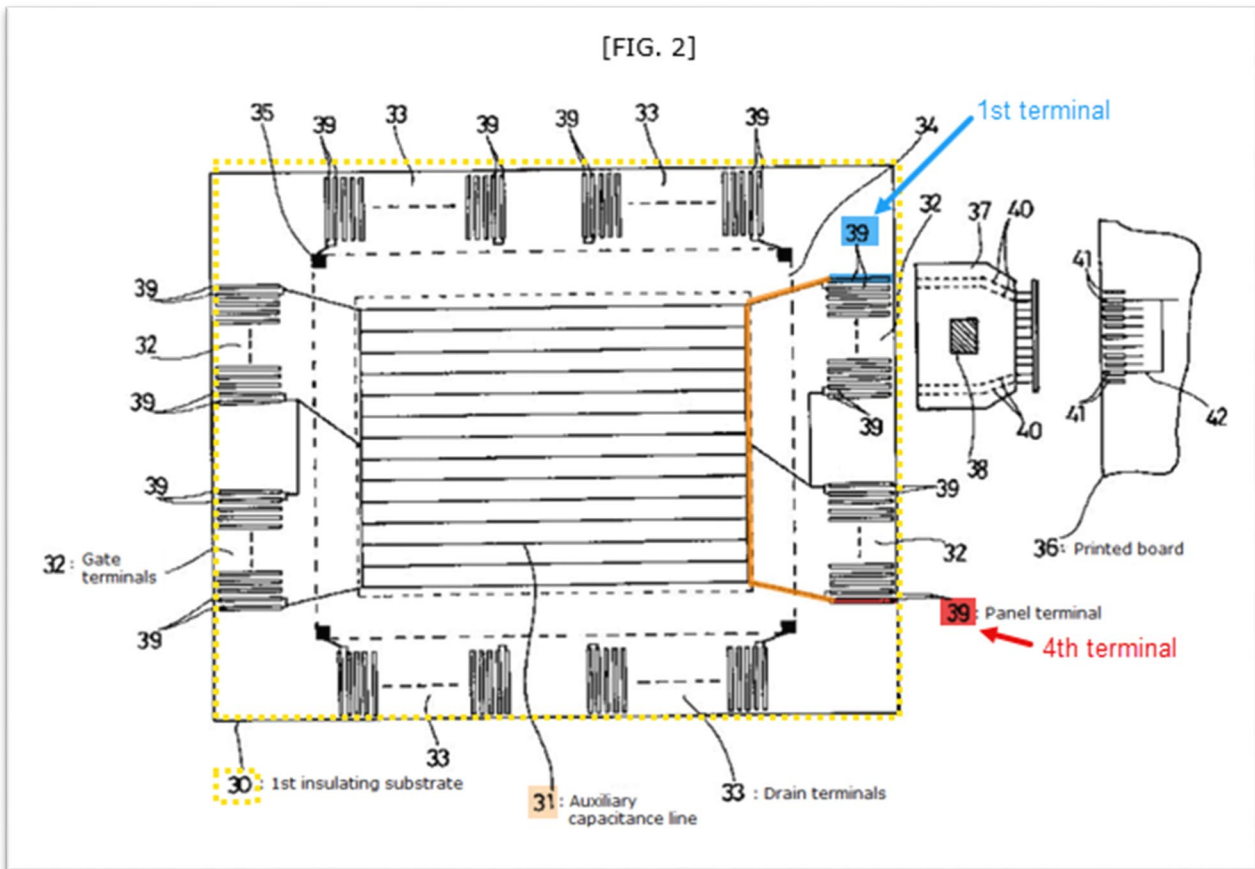
As shown in Figure 2 below, Takemura discloses that a second portion of the LCD panel, adjacent to the first portion, has “*panel terminals (39) [] provided at both ends of a gate terminal group (32)*”:



(Takemura at [0029], Fig. 2 (annotated); Murphy ¶173.) A POSITA reading Takemura would understand that Takemura teaches Claim [1c]. (Murphy ¶173.)

[1d] “the first terminal and the fourth terminal being electrically connected through a first connection wiring provided on the electro-optical panel,”

Takemura discloses that the panel terminals may be used to supply a stable voltage to the LCD panel. (Takemura at [0031] (“The second aspect of the present invention uses the panel terminals as terminals for auxiliary capacitance[.]”), [0033]; Murphy ¶174.) As shown in Figure 2 below, this is accomplished by “contact[ing]” the panel terminals (39), such as the first and fourth terminals to auxiliary capacitance lines (31) on the insulating substrate (30):

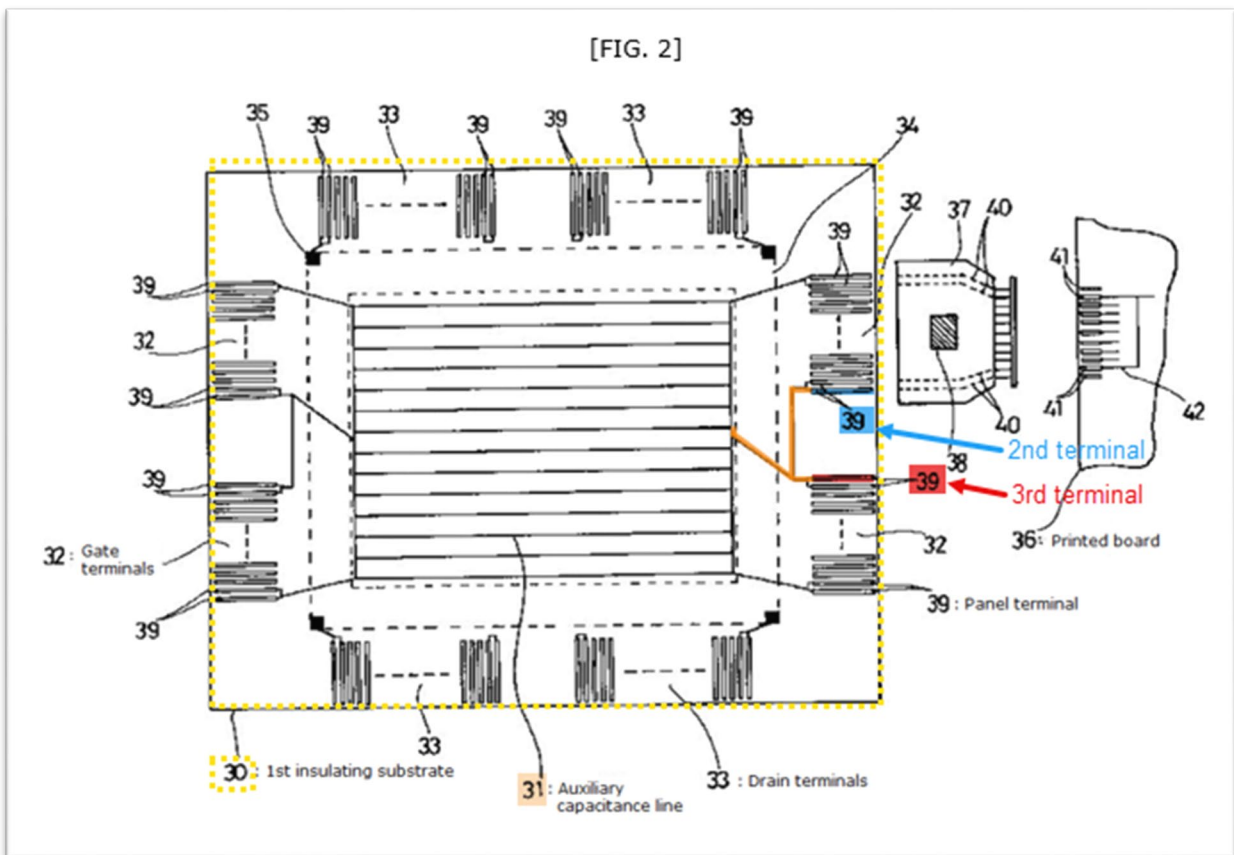


(Takemura at [0030] (“[T]he panel terminal on the gate terminal side is in contact with an auxiliary capacitance line[.]”), Fig. 2 (annotated); Murphy ¶174.) A POSITA would understand that the contact with the auxiliary capacitance line is an electrical

connection because an auxiliary capacitance signal is supplied. (Takemura at [0029] – [0031], [0033], Fig. 2; Murphy ¶174.) A POSITA reading Takemura would understand that Takemura teaches Claim [1d]. (Murphy ¶174.)

[1e] “the second terminal and the third terminal being electrically connected through a second connection wiring provided on the electro-optical panel;”

As shown in Figure 2 below, second and third panel terminals (39) “contact” auxiliary capacitance lines (31) on the insulating substrate (30):

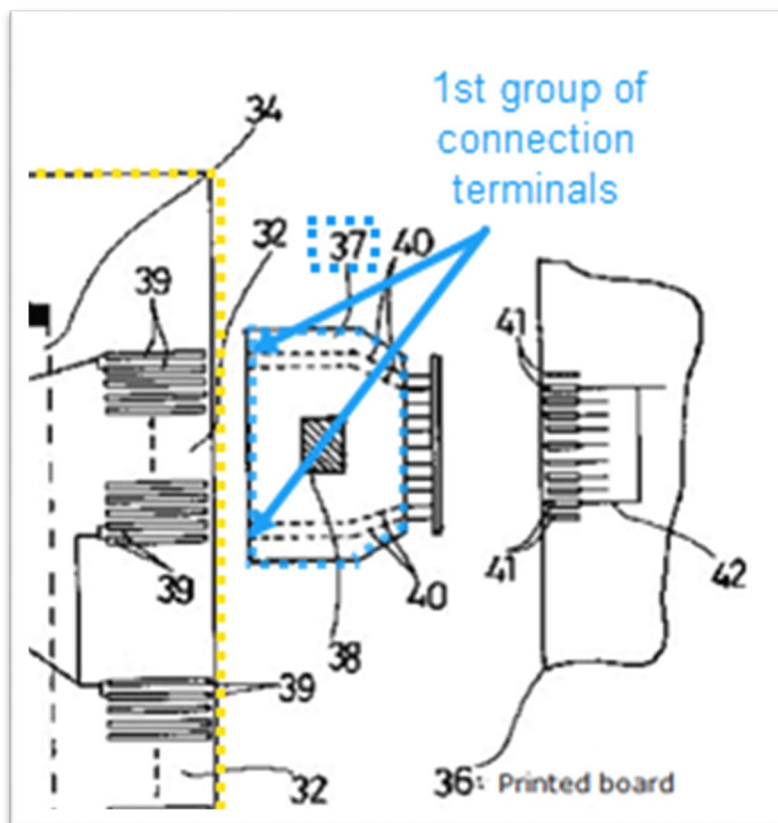


(Takemura at [0030], Fig. 2 (annotated); Murphy ¶175.) A POSITA would understand that the contact with the auxiliary capacitance line is an electrical

connection because an auxiliary capacitance signal is supplied. (Takemura at [0029] – [0031], [0033], Fig. 2; Murphy ¶175.) A POSITA reading Takemura would understand that Takemura teaches Claim [1e]. (Murphy ¶175.)

[1f] “a first circuit substrate including: a first connection terminal portion having a first group of connection terminals to be electrically connected to the first terminal portion;”

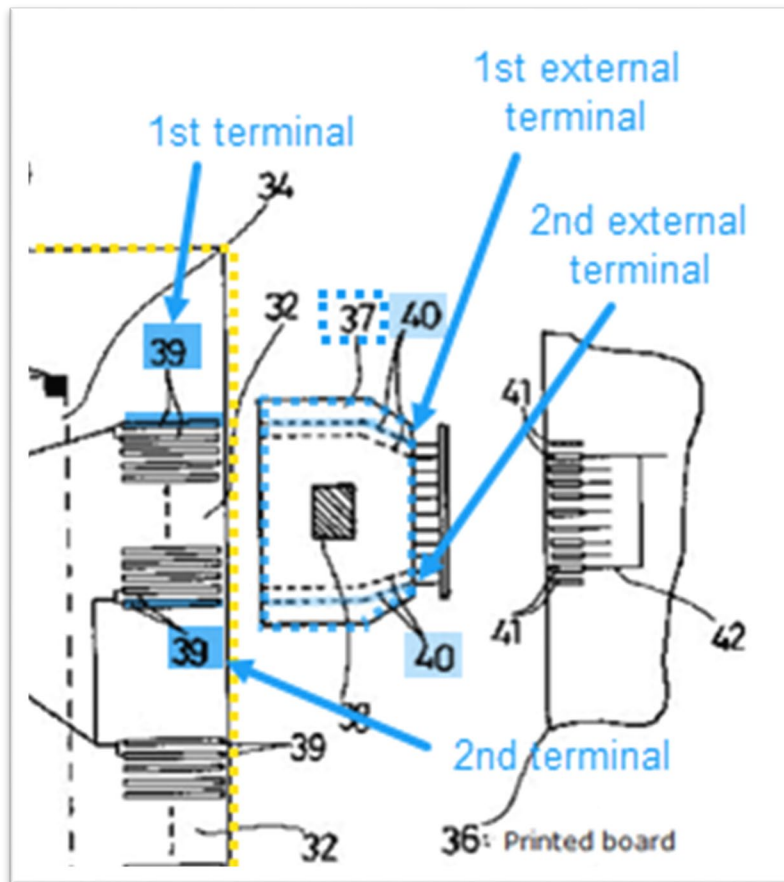
As shown in Figure 2 below, Takemura discloses that tape automated bonding (“TAB”) (37) is a flexible substrate between the LCD panel and printed circuit board (36):



(Takemura at [0013] (“The connecting means is a *flexible substrate*, generally TAB[.]”), [Reference Numbers], Fig. 2 (annotated); Murphy ¶176.) Takemura further discloses that a group of “terminals (or wiring serving as terminals) are provided on the left . . . side[] of the TAB” and that “panel terminals [(39)] are connected to wiring via left-side terminals of the TAB[.]” (Takemura at [0013], [0015], [0017], [0029], [0030]; Murphy ¶176.) In other words, the left side terminals of TAB (37) are a first group of connection terminals in a first connection terminal portion to be electrically connected to the first terminal portion of the LCD panel. (Murphy ¶176.) A POSITA reading Takemura would understand that Takemura teaches Claim [1f]. (Murphy ¶176.)

[1g] “a first external terminal connected to the first terminal through the first connection terminal portion; and a second external terminal connected to the second terminal through the first connection terminal portion; and”

As shown in Figure 2 below, Takemura discloses that “terminals (or wiring serving as terminals) are [also] provided on the . . . right side[] of the TAB” and that “panel terminals [(39)] are connected to wiring via left-side terminals of the TAB [(37)], and the right ends of the wiring extend to the right edge of the TAB and are connected to the [right-side] terminals” of TAB (37):



(Takemura at [0013], [0015], [0017], [0029], [0030], Fig. 2 (annotated); Murphy ¶177.) A POSITA would understand that wiring (40) between the left and right-side terminals of TAB (37) may comprise a metal film such as copper. (Murphy ¶177.) In other words, the right-side terminals of the TAB include first and second external terminals which are connected to the first and second panel terminals, respectively, through the first connection terminal portion. (Murphy ¶177.) A POSITA reading Takemura would understand that Takemura teaches Claim [1g]. (Murphy ¶177.)

[1h] “a second circuit substrate including: a second connection terminal portion having a second group of

connection terminals to be electrically connected to the second terminal portion;”

Takemura discloses that “**two TABs (37)** like the one shown in FIG. 2 **may be provided on each side edge**” of the LCD panel (Takemura at [0028]; Murphy ¶178.)

Thus, a POSITA would understand that the second TAB is structured similarly to the first TAB such that a second circuit substrate includes a second connection terminal portion having a second group of connection terminals to be electrically connected to the second terminal portion. (Murphy ¶178. *See also* Claim [1f], *supra*.) A POSITA reading Takemura would understand that Takemura teaches Claim [1h]. (Murphy ¶178.)

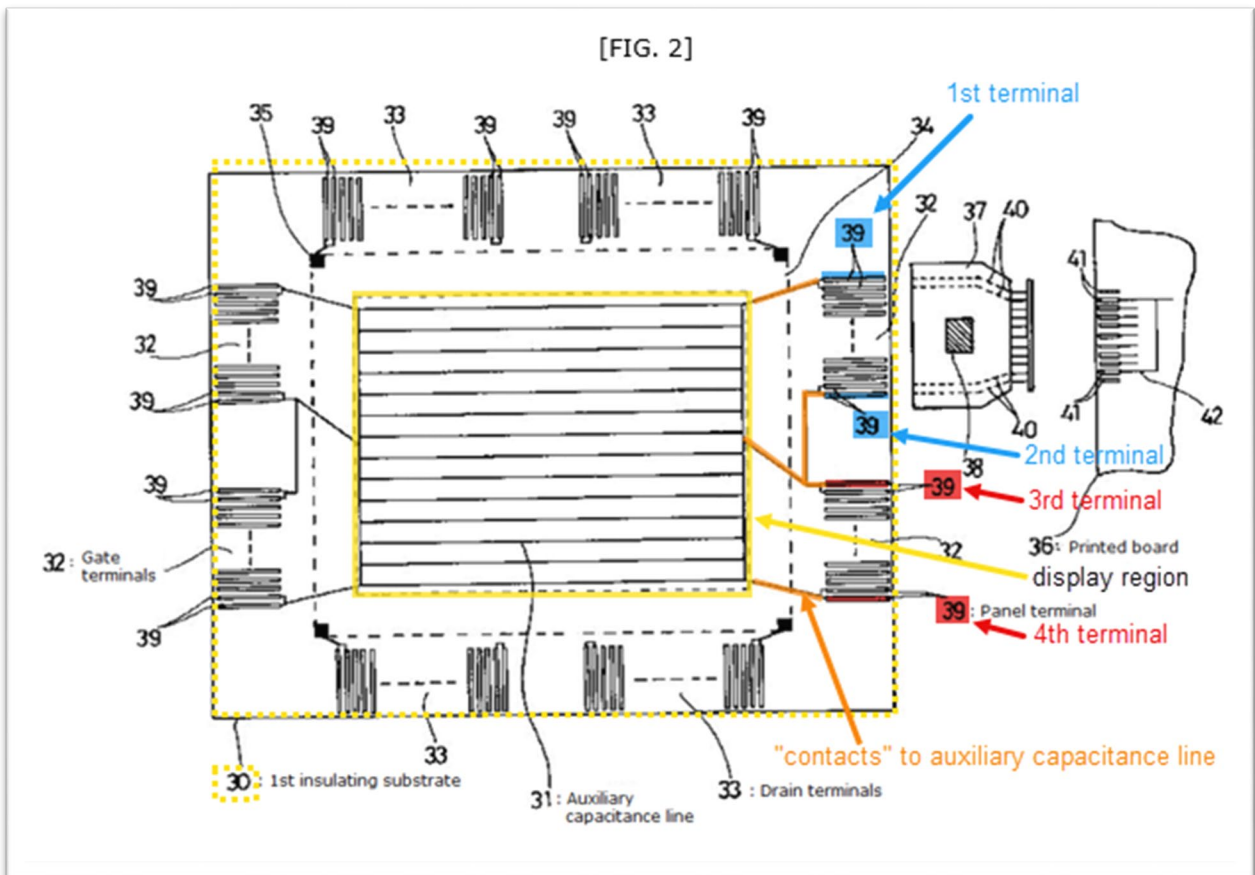
[1i] “a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion.”

Takemura discloses that the LCD panel is connected to two TABs. (Takemura at [0028]; Murphy ¶179.) Thus, a POSITA would understand that the second TAB is structured similarly to the first TAB such that the second circuit substrate includes a third external terminal electrically connected to the third terminal through the second connection terminal portion; and a fourth external terminal electrically connected to the fourth terminal through the second connection terminal portion. (Murphy ¶179. *See also* Claim [1g], *supra*.) A POSITA reading Takemura would understand that Takemura teaches Claim [1i]. (Murphy ¶179.)

2. Dependent Claim 2

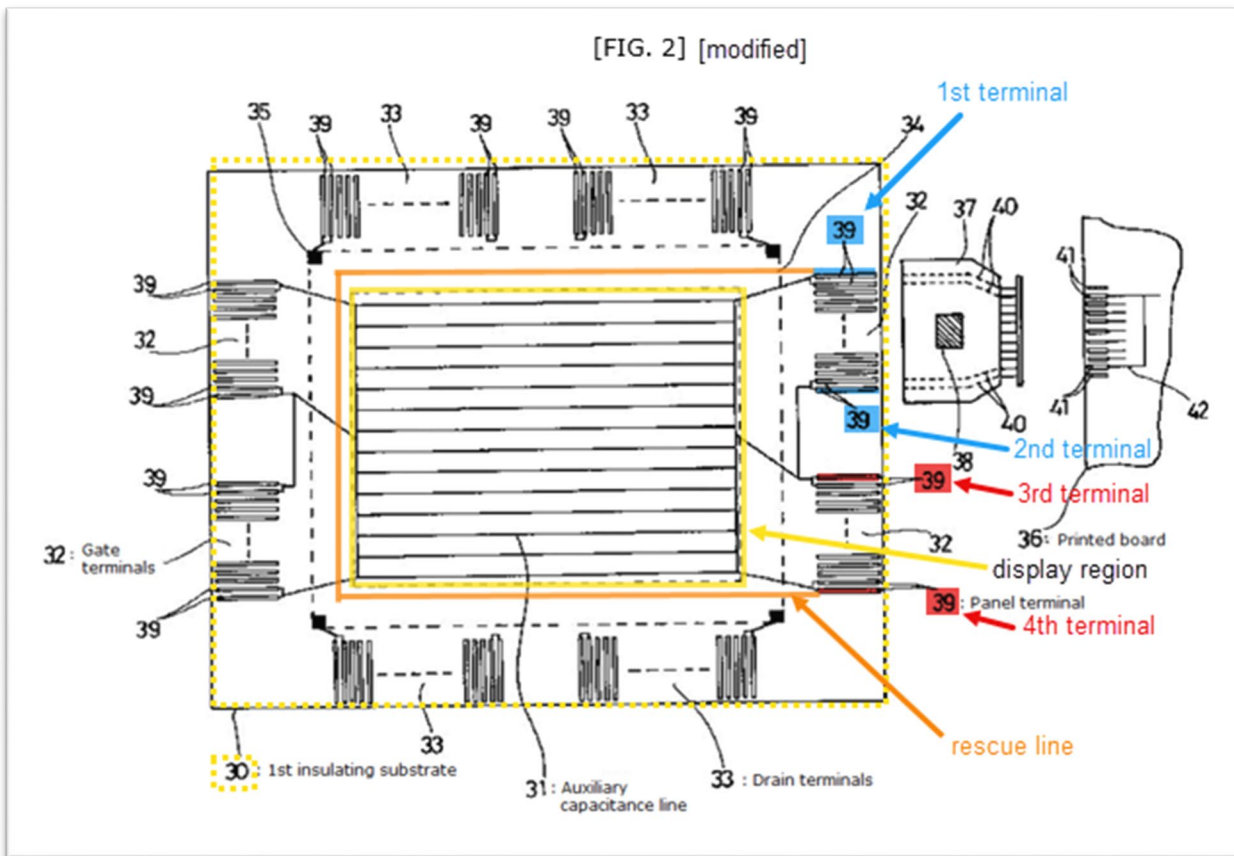
The electro-optical device according to claim 1, wherein some of the first connection wiring and the second connection wiring is arranged so as to be extended around the circumference of a display region.

As shown in Figure 2 below, Takemura discloses that a portion of the panel terminals' (39) "contacts" to auxiliary capacitance line (31) extends around the circumference of the display region:



(Takemura at [0014], [0029] – [0031], [0033], Fig. 2 (annotated); Murphy ¶180. See also Claim 1[e], *supra*.)

Alternatively, Takemura discloses that the panel terminals may be used as rescue terminals that are “in contact with *a rescue line extending around the display region.*” (Takemura at [0033]; Murphy ¶181.) In this case, the rescue line takes the place of the “contacts” to auxiliary capacitance line (31), as shown in modified Figure 2 below:



(Takemura at [0033], Fig. 2 (modified) (annotated); Murphy ¶181.) Thus, a POSITA reading Takemura would understand that Takemura teaches Claim [2]. (Murphy ¶181.)

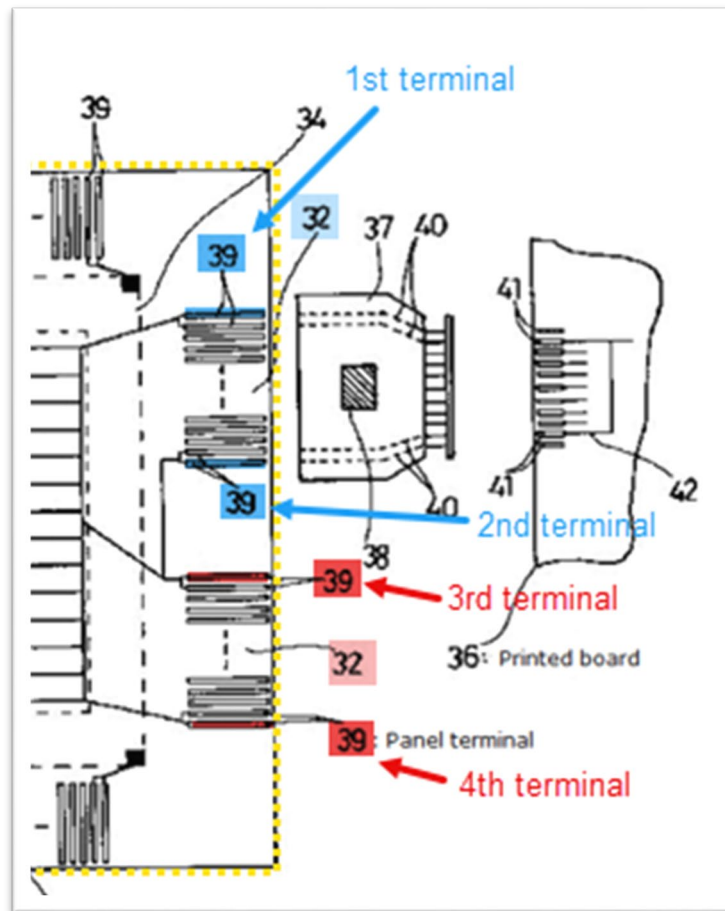
3. Dependent Claim 3

[3a] The electro-optical device according to claim 1, wherein: each of the first and second group of terminals configures a terminal group arranged in a predetermined direction, and

Takemura discloses that the first and second groups of terminals are fixed on the LCD panel. (Takemura at [0028], Fig. 2; Murphy ¶182. *See also* Claims [1b], [1c].) As such, the order of the terminals does not change, e.g., the first terminal is always above the second terminal. (Murphy ¶182.) Accordingly, a POSITA reading Takemura would understand that Takemura teaches Claim [3a]. (Murphy ¶182.)

[3b] the first terminal and the second terminal, and the third terminal and the fourth terminal are provided at both end sides of the predetermined direction of the terminal group.

As shown in Figure 2 below, Takemura discloses that the “***panel terminals (39) are provided at both ends of a gate terminal group (32)***”:

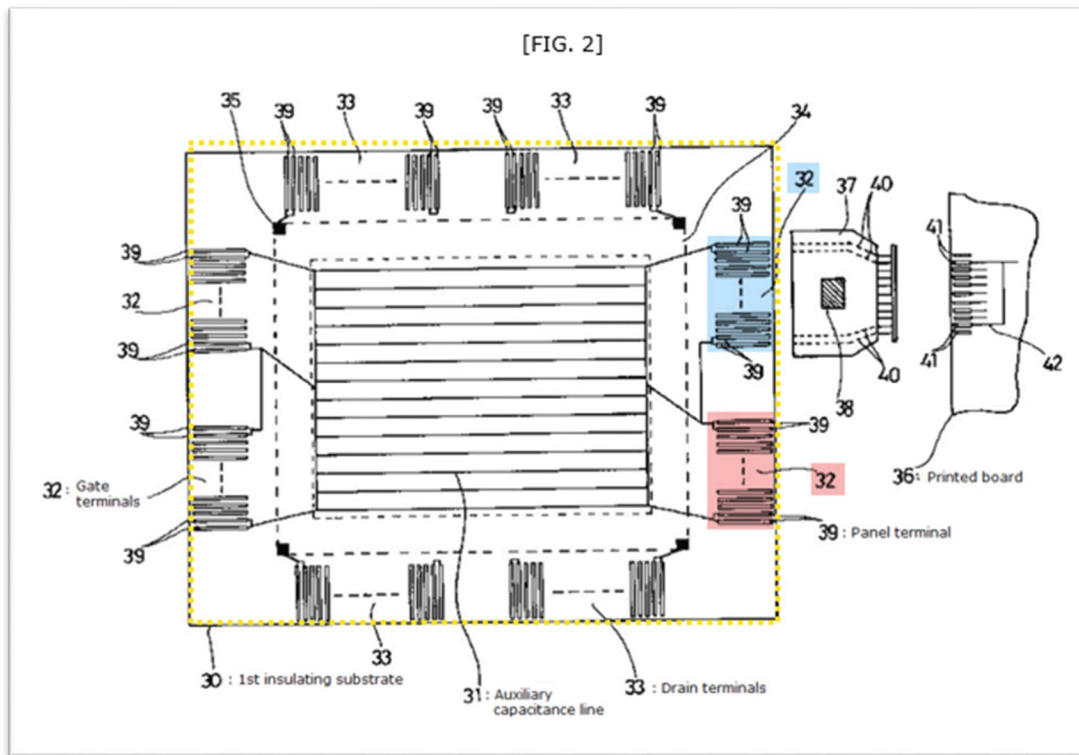


(Takemura at [0029], Fig. 2 (annotated); Murphy ¶183.) Thus, a POSITA reading Takemura would understand that Takemura teaches Claim [3b]. (Murphy ¶183.)

4. Dependent Claim 4

[4] The electro-optical device according to claim 1, wherein the first terminal portion and the second terminal portion are provided on at least one of a first side of the electro-optical panel and a second side of a direction crossing the first side.

As shown in Figure 2 below, Takemura discloses that the first and second terminal portions, indicated by the first and second terminal groups, respectively, are provided along the right side of the LCD panel:

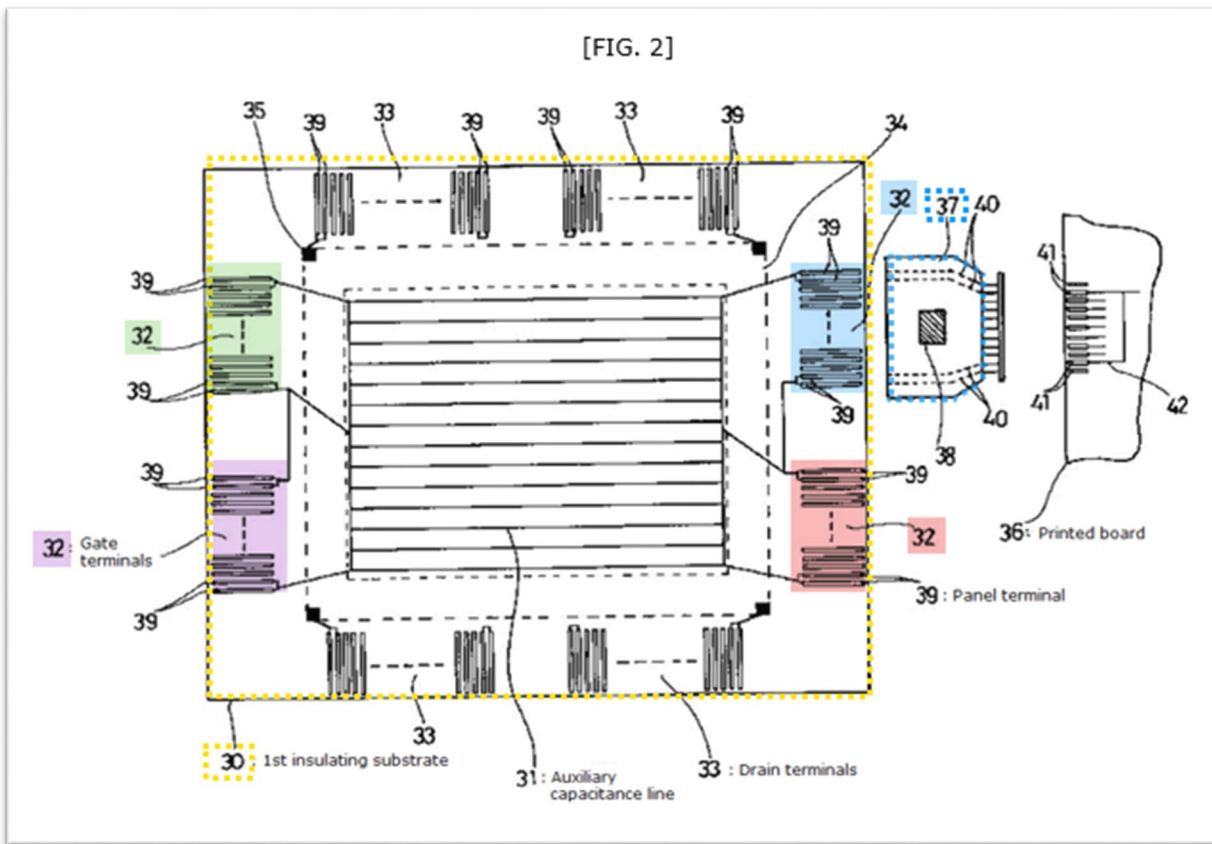


(Takemura at Fig. 2 (annotated); Murphy ¶184.) The left side of the panel is a second side of a direction crossing the right side of the panel. (Murphy ¶184.) Thus, a POSITA reading Takemura would understand that Takemura teaches Claim [4]. (Murphy ¶184.)

5. Dependent Claim 5

[5a] The electro-optical device according to claim 1, wherein: the electro-optical panel includes a third terminal portion having a third group of terminals, a fourth terminal portion having a fourth group of terminals arranged so as to be adjacent to the third terminal portion,

As shown in Figure 2, Takemura discloses four portions of the LCD panel, each with a terminal group (32):



(Takemura at [0014], [0021], Fig. 2 (annotated); Murphy ¶185.) The third and fourth terminal portions with third and fourth groups of terminals, respectively, are adjacent to each other on the left side of the LCD panel. (Murphy ¶185.) A POSITA reading Takemura would understand that Takemura teaches Claim [5a]. (Murphy ¶185.)

[5b] a third circuit substrate on which a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion is provided, and a fourth circuit substrate on which a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion is provided,

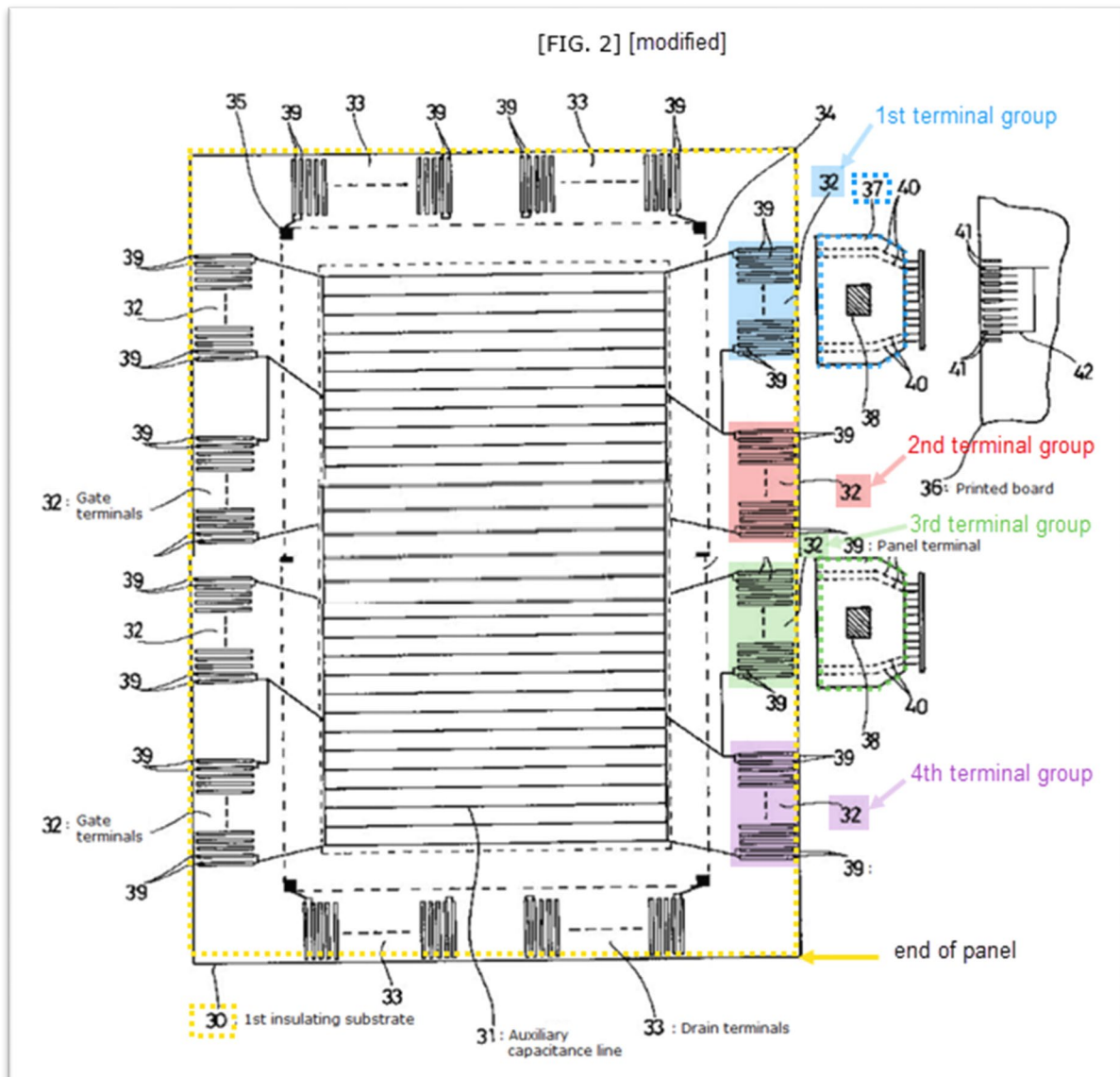
Takemura discloses that “**two TABs (37)** like the one shown in FIG. 2 **may be provided on each side edge.**” (Takemura at [0028]; Murphy ¶186.) There are no differences between the TABs structurally or how they are electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0028]; Murphy ¶186. *See also* Claim [1f], [1h], *supra*.) Thus, Takemura discloses third and fourth flexible substrates, provided on the left side of the LCD panel, the third substrate including a third connection terminal portion having a third group of connection terminals to be electrically connected to the third terminal portion, and the fourth substrate including a fourth connection terminal portion having a fourth group of connection terminals to be electrically connected to the fourth terminal portion. (Murphy ¶186.) A POSITA reading Takemura would understand that Takemura teaches Claim [5b]. (Murphy ¶186.)

[5c] the third terminal portion is provided between a position where the first terminal portion is provided and an end of the electro-optical panel, and the fourth terminal portion is provided between a position where the second terminal portion is provided and an end of the electro-optical panel,

Takemura discloses that the number of TABs provided on any side of the LCD panel “is not limited, and one [TAB] may be provided on each side edge, **or three or more may be provided on each side edge.**” (Takemura at [0028]; Murphy ¶187.) In the case where four TABs are provided on the right side of the LCD panel, a

POSITA would understand that there are also four corresponding terminal portions and groups of terminals that are electrically connected to the TABs because the TABs' purpose is to connect the LCD panel to a printed circuit board. (Takemura at [0029], [0030]; Murphy ¶187.)

For example, Takemura's LCD panel with four TABs (two shown), four terminal portions and four groups of terminals along the right side of the LCD panel would be arranged as shown in modified Figure 2 below:

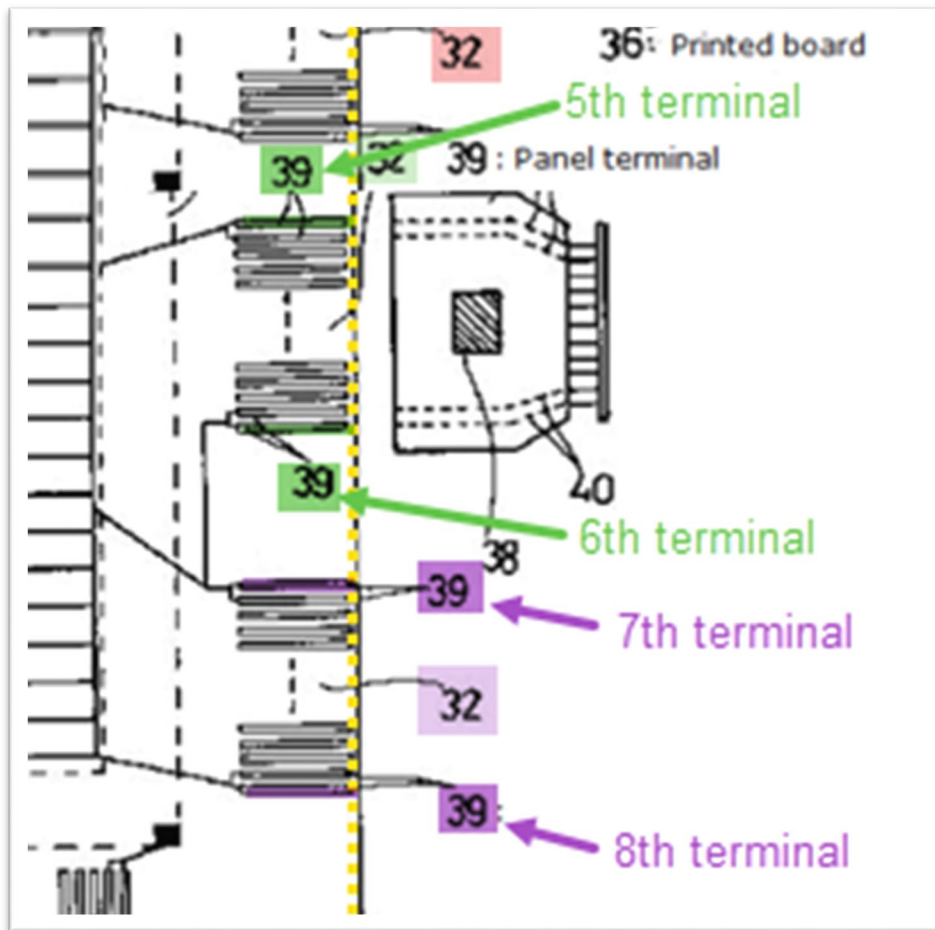


(Takemura at Fig. 2 (modified) (annotated); Murphy ¶188.) The third and fourth terminal portions and third and fourth groups of terminals remain adjacent to each. (Murphy ¶188.) Moreover, there are no differences between the TABs structurally or how they are electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0028]; Murphy ¶188.) Thus, a POSITA would understand that, in this arrangement, the third terminal portion is provided between

the first terminal portion and an end of the LCD panel, and the fourth terminal portion is provided between the second terminal portion and an end of the electro-optical panel. (Murphy ¶188.) A POSITA reading Takemura would understand that Takemura teaches Claim [5c]. (Murphy ¶188.)

[5d] the third group of terminals has fifth and sixth terminals separated from each other, the fourth group of terminals has seventh and eighth terminals separated from each other, and

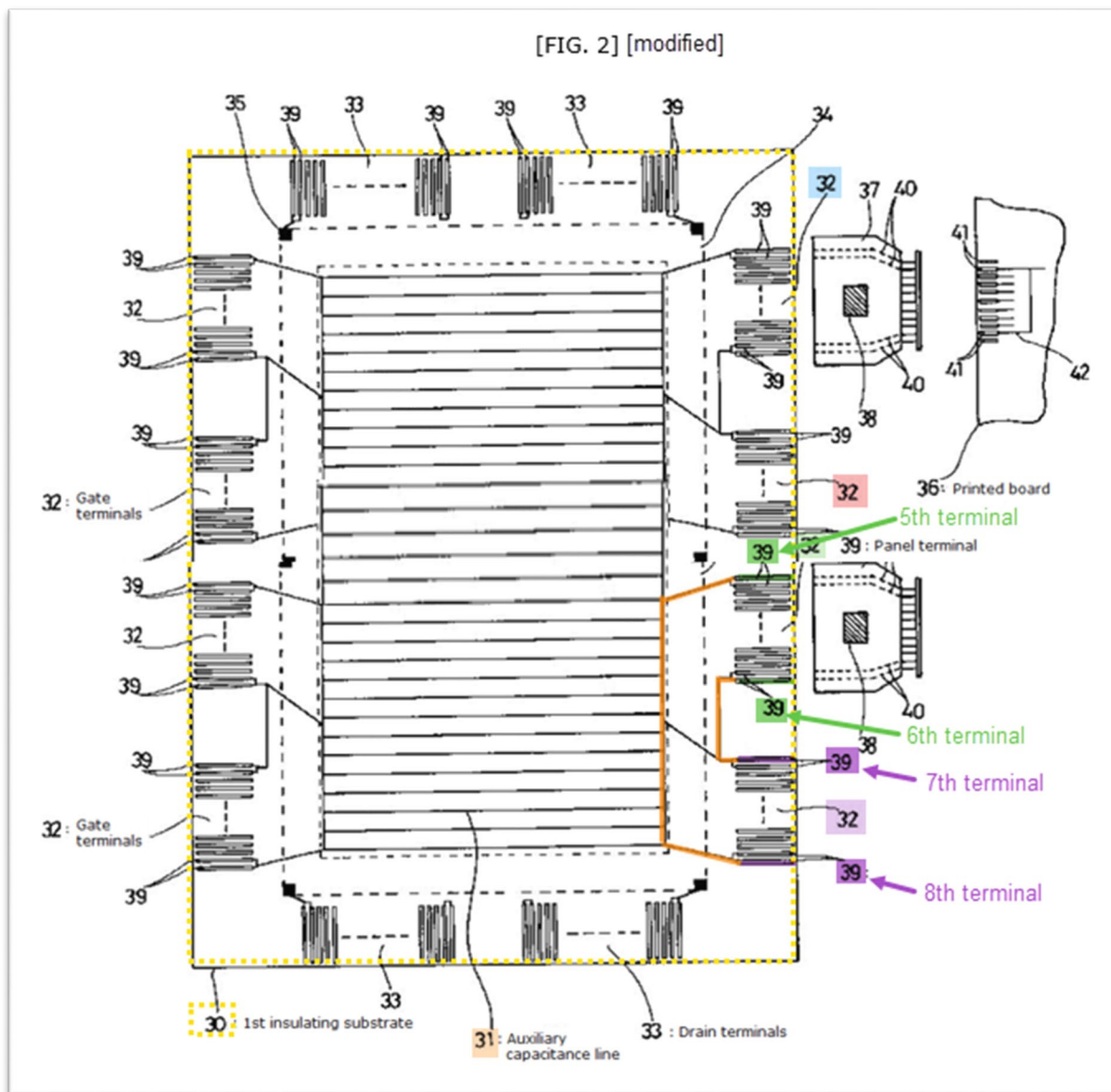
There are no structural differences between each of the terminal groups. (Takemura at [0014], [0021], [0029], Fig. 2; Murphy ¶189. *See also* Claim 1[b], 1[c], [5a], *supra*.) Thus, Takenaka discloses that the third group of terminals has fifth and sixth terminals separated from each other, and the fourth group of terminals has seventh and eighth terminals separated from each other, as shown in modified Figure 2 below:



(Takemura at [0029], Fig. 2 (modified) (annotated); Murphy ¶189.) A POSITA reading Takemura would understand that Takemura teaches Claim [5d]. (Murphy ¶189.)

[5e] the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively,

There are no differences between the first and second, and third and fourth terminal groups, or how their respective panel terminals “contact” the auxiliary capacitance lines on the LCD panel, as shown in modified Figure 2 below:

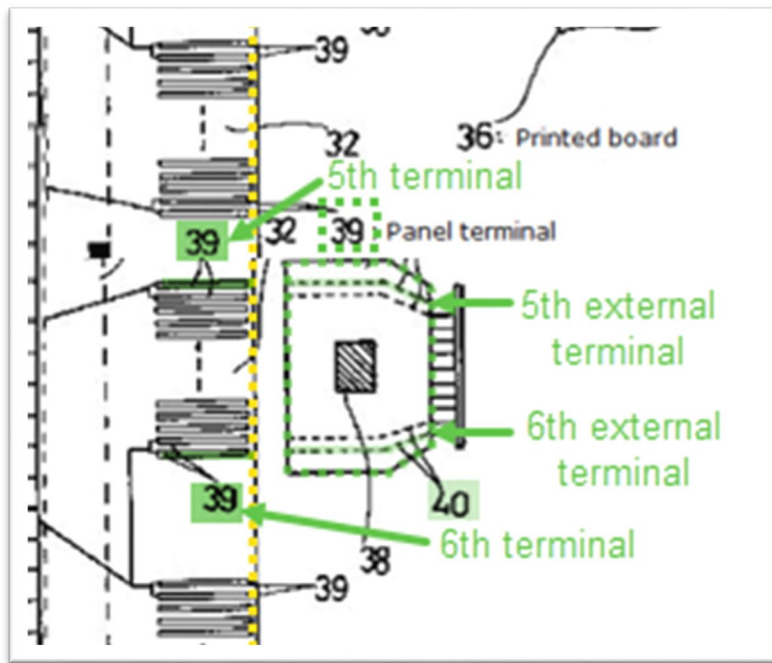


(Takemura at [0014], [0021], [0029]–[0031], [0033], Fig. 2 (modified) (annotated);
Murphy ¶190. *See also* Claim [1d], [1e], *supra*.) Accordingly, a POSITA would

understand that the fifth terminal and the eighth terminal, and the sixth terminal and the seventh terminal are electrically connected through a third connection wiring and a fourth connection wiring provided on the electro-optical panel, respectively. (Murphy ¶190.) A POSITA reading Takemura would understand that Takemura teaches Claim [5e]. (Murphy ¶190.)

[5f] the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, and

There are no differences between the TABs structurally or how they are electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0013], [0015], [0017], [0028]-[0030]; Murphy ¶191. *See also* Claims [1g], [1i], [5b], [5d], *supra*.) Thus, Takemura discloses that the third circuit substrate has a fifth external terminal electrically connected to the fifth terminal through the third connection terminal portion and a sixth external terminal electrically connected to the sixth terminal, as shown in modified Figure 2 below:



(Takemura at Figure 2 (modified) (annotated); Murphy ¶191.) A POSITA reading Takemura would understand that Takemura teaches Claim [5f]. (Murphy ¶191.)

[5g] the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external terminal electrically connected to the eighth terminal.

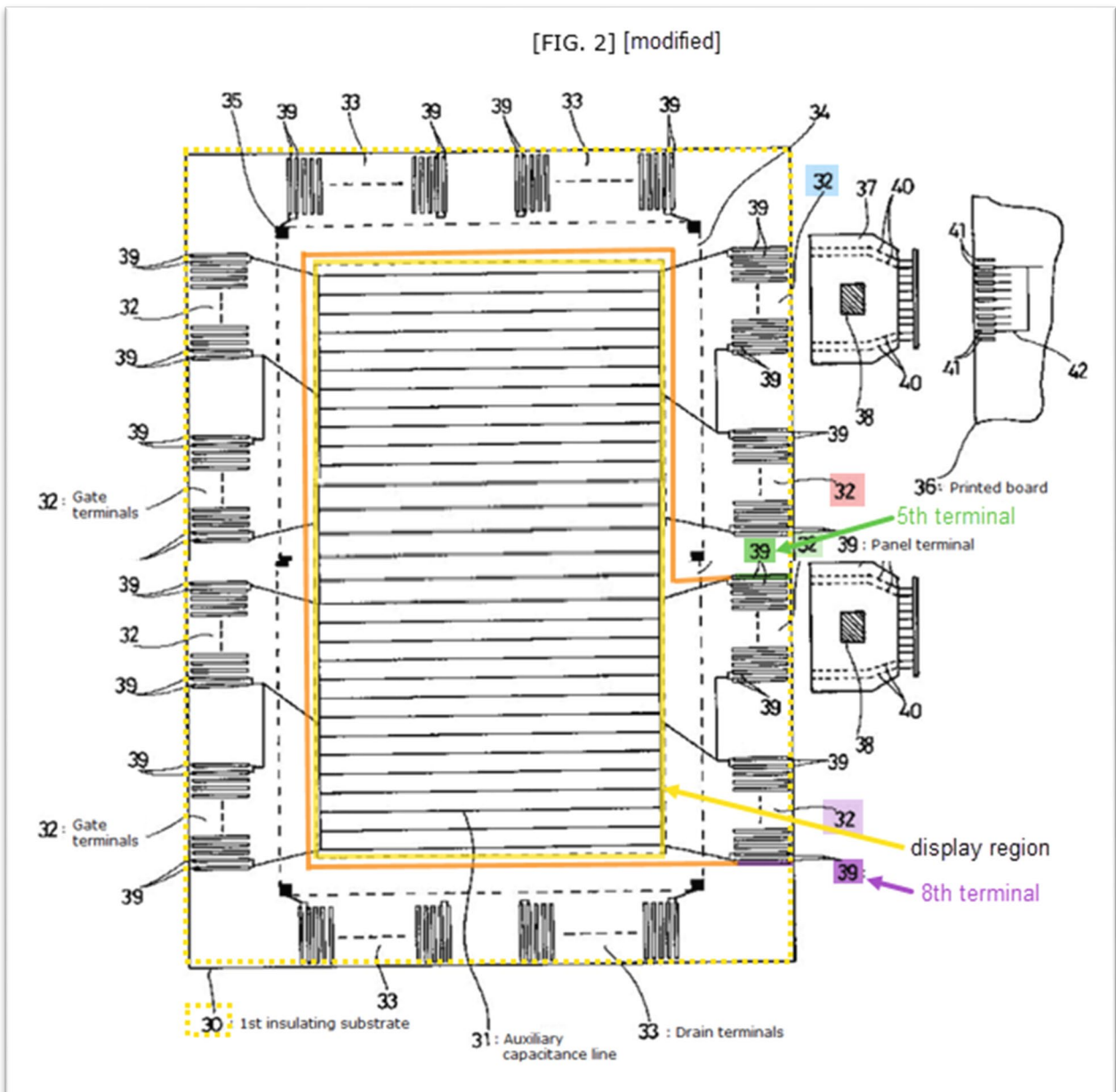
There are no differences between the TABs structurally or how they are electrically connected to their respective terminal portions and groups of terminals. (Takemura at [0013], [0015], [0017], [0028]-[0030]; Murphy ¶192. *See also* Claims [1g], [1i], [5b], [5d], *supra*.) Thus, Takemura discloses that the fourth circuit substrate has a seventh external terminal electrically connected to the seventh terminal through the fourth connection terminal portion and an eighth external

terminal electrically connected to the eighth terminal. (Murphy ¶192.) A POSITA reading Takemura would understand that Takemura teaches Claim [5g]. (Murphy ¶192.)

6. Dependent Claim 6

[6] The electro-optical device according to claim 5, wherein the third connection wiring is extended around the circumference of the display region.

Takemura discloses that panel terminals may be used as “rescue terminals,” as an alternative to being used to supply signals to the auxiliary capacitance line. (Takemura at [0033]; Murphy ¶193.) In this case, Takemura discloses that “rescue terminals will be in contact with a *rescue line extending around the display region.*” (Takemura at [0033]; Murphy ¶193.) Accordingly, a POSITA would understand that the third connection wiring electrically connecting the fifth and eighth terminals may comprise a rescue line extended around the circumference of the display region, as shown in modified Figure 2 below:



(Takemura at [0033], Fig. 2 (modified) (annotated); Murphy ¶193.) A POSITA reading Takemura would understand that Takemura teaches Claim [6]. (Murphy ¶193.)

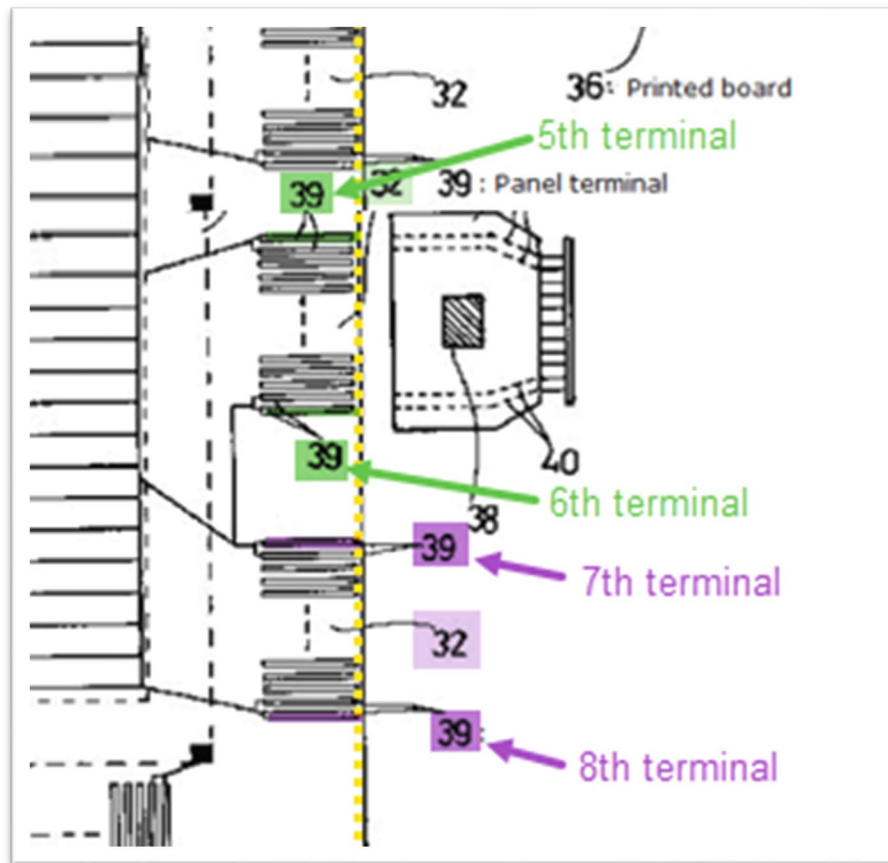
7. Dependent Claim 7

[7a] The electro-optical device according to claim 5, wherein: each of the third and fourth group of terminals configures a terminal group arranged in a predetermined direction, and

Similarly to the first and second groups of terminals, Takemura discloses that the third and fourth groups of terminals are fixed on the LCD panel. (Takemura at [0028]; Murphy ¶194. *See also* Claims [1b], [1c], [3a], *supra*.) As such, the order of the terminals does not change, e.g., the fifth and seventh terminals are always above the sixth and eighth terminals, respectively. (Murphy ¶194.) Accordingly, a POSITA would understand that the terminal groups are arranged in a predetermined direction. (Murphy ¶194.) A POSITA reading Takemura would understand that Takemura teaches Claim [7a]. (Murphy ¶194.)

[7b] the fifth terminal and the sixth terminal, and the seventh terminal and the eighth terminal are provided at both end sides of the predetermined direction of the terminal group.

As shown in modified Figure 2 below, similarly to the first through fourth terminals, Takemura discloses that the fifth and sixth, and seventh and eighth “***panel terminals (39) are provided at both ends of a gate terminal group (32)***”:



(Takemura at [0029], Fig. 2 (modified) (annotated); Murphy ¶195.) A POSITA reading Takemura would understand that Takemura teaches Claim [7b]. (Murphy ¶195.)

13. Dependent Claim 13

[13] *An electronic apparatus comprising the electro-optical device according to claim 1.*

Takemura discloses that the LCD device of Claim 1 may be incorporated into an LCD projector. (Takemura at [0027] (“[P]rinted circuit board (36) is hollow in the center for use in an LCD projector.”); Murphy ¶196.) A POSITA reading Takemura would understand that Takemura teaches Claim [13]. (Murphy ¶196.)

IX. CONCLUSION

For the reasons above, claims 1-13 are obvious.

Dated: September 5, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(D)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 13,497, excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: September 5, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of this **PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,391,020** and its supporting materials have been served by FedEx delivery service on Patent Owner at the correspondence address for the attorney of record for the '020 Patent shown in USPTO records:

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