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【54】發明名稱：路徑切換裝置以及測試焊墊之減少方法

A SWITCHING CIRCUIT AND A METHOD FOR REDUCING TEST PAD

【21】申請案號：095147504

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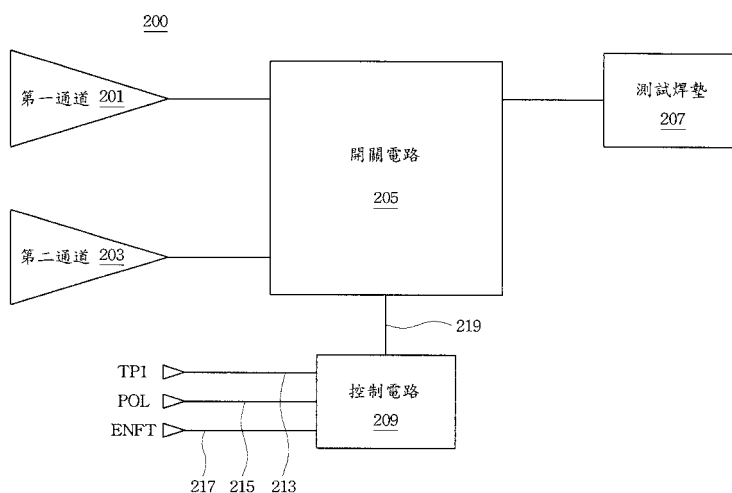
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【57】發明摘要

測試焊墊之減少方法以及其所使用的路徑切換裝置，係用以在一晶片之最終測試階段，切換晶片之輸出路徑，其中晶片具有一第一通道以及一第二通道，路徑切換裝置則包括測試焊墊以及開關電路，其中開關電路係用以選擇地將第一通道或第二通道連接至測試焊墊，當最終測試致能信號具有第一邏輯位準或第二邏輯位準時，開關電路則藉由第一通道或第二通道，分別將其上的第一驅動電壓或第二驅動電壓傳送至測試焊墊。



200：路徑切換裝置
201：第一通道
203：第二通道
205：開關電路
207：測試焊墊
209：控制電路
213：脈衝信號
215：極性信號
217：最終測試致能信號
219：控制信號

代表圖式

發明專利說明書

(本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

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一、發明名稱：(中文/英文)

路徑切換裝置以及測試焊墊之減少方法

A SWITCHING CIRCUIT AND A METHOD FOR REDUCING TEST
PAD

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中華民國 / R.O.C.

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3.卜令楷 / BU, LINKAI

國 籍：(中文/英文)

1.中華民國 / R.O.C.

2.中華民國 / R.O.C.

3.中華民國 / R.O.C.

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☐ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☐ 有主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼 順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要

路徑切換裝置以及測試焊墊之減少方法

測試焊墊之減少方法以及其所使用的路徑切換裝置，係用以在一晶片之最終測試階段，切換晶片之輸出路徑，其中晶片具有一第一通道以及一第二通道，路徑切換裝置則包括測試焊墊以及開關電路，其中開關電路係用以選擇地將第一通道或第二通道連接至測試焊墊，當最終測試致能信號具有第一邏輯位準或第二邏輯位準時，開關電路則藉由第一通道或第二通道，分別將其上的第一驅動電壓或第二驅動電壓傳送至測試焊墊。

六、英文發明摘要

A switching circuit and a method for reducing test pad

A switching device and a method for reducing test pad which switch the output driving voltage of the source driver during the final test period. The source driver has a first channel and a second channel, and the switch device includes a test pad and a switch circuit. The switch circuit is used to select one of the first channel and second channel to connect to the test pad. The switch circuit delivers either the first driving voltage or the second driving voltage to the test pad through the first channel and the second channel according to the logic level of an Enable Final Test signal.

七、指定代表圖：

(一)、本案指定代表圖為：第(2)圖

(二)、本案代表圖之元件符號簡單說明：

200：路徑切換裝置

201：第一通道

203：第二通道

205：開關電路

207：測試焊墊

209：控制電路

213：脈衝信號

215：極性信號

217：最終測試致能信號

219：控制信號

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

九、發明說明：

【發明所屬之技術領域】

本發明是有關於一種液晶顯示器閘極驅動電路之測試裝置及方法，且特別是有關於一種閘極驅動電路在最終測試階段的測試裝置及方法。

【先前技術】

近年來，由於薄膜覆晶（Chip On Film Process，COF）製程能夠提供小體積的顯示器，以迎合消費者大眾對於顯示器輕薄短小的要求，因此驅動 IC 之封裝方式由自動捲帶式晶粒接合製程（Tape Automatic Bonding Process，TAB Process）演進到薄膜覆晶製程。

薄膜覆晶製程是一種（Flip Chip Bonding）將電子元件與可撓性電路板（Flexible or Film Printed Circuit board，FPC）接合的技術，可以將顯示器的源極驅動晶片及其電子零件直接安裝於薄膜（Film）上，省去傳統的印刷電路板，達到輕薄短小的目的。

請參照第 1 圖，其係繪示一源極驅動晶片在最終測試階段的測試裝置，包括樹脂層 101、薄膜 103、測試焊墊 105、金屬走線 107、外引腳 109 以及鉾阻 111，其中，樹脂層 101 係用以包覆一源極驅動晶片（未顯示於圖中），金屬走線 107 則用以與樹脂層 101 內之源極驅動晶片耦接。源極驅動晶片、樹脂層 101、測試焊墊 105、金屬走線 107 以及外引腳 109 係安置於薄膜 103 之上。

在這樣的測試裝置之中，每一個源極驅動電壓的輸出

都需要有一個測試焊墊與之耦接，才能使得測試探針能夠透過這些測試焊墊來測試每一源極驅動電壓。然而，由於源極驅動電壓的數目眾多，因此測試焊墊的數目也必須隨之增加，大幅增加了測試裝置之體積以及製造成本。

因此需要一個新的測試裝置以及方法，來減少測試焊電的數量，降低測試裝置的體積以及成本。

【發明內容】

因此本發明之一方面就是在提供一種路徑切換裝置，減少一源極驅動晶片在最終測試階段所需要的測試焊墊之數目。

依照本發明之一實施例，路徑切換裝置係用以在一覆晶薄膜晶片之最終測試階段中，切換晶片之輸出路徑，其中，覆晶薄膜晶片具有一第一通道以及一第二通道，路徑切換則裝置包括一測試焊墊以及一開關電路。開關電路係用以選擇地將第一通道或第二通道連接至測試焊墊。

本發明另一方面在提供一種測試焊墊之減少方法，用以在一最終測試階段當中，減少一源極驅動晶片所需要的測試焊墊之數目。

依照本發明之另一實施例，測試焊墊之減少方法，係使用於一源極驅動晶片之最後測試階段，該方法係當一最終測試致能信號具有一第一邏輯位準時輸出一第一驅動電壓至測試焊墊，當最終測試致能信號具有一第二邏輯位準時輸出一第二驅動電壓至測試焊墊。

根據本發明之上述實施例，路徑切換裝置以及測試焊

墊之減少方法，能夠在終測試階段中減少源極驅動晶片所需要的測試焊墊之數量。

【實施方式】

請參照第 2 圖，其繪示依照本發明一實施例的路徑切換裝置，路徑切換裝置 200 包括第一通道 201、第二通道 203、開關電路 205、控制電路 209 以及測試焊墊 207，其中，第一通道 201、第二通道 203、開關電路 205 以及控制電路 209 係位於一源極驅動晶片之上，測試焊墊 207 則安置於薄膜之上。

控制電路 209 係依據脈衝信號(TP1)213、極性信號(POL)215 以及最終測試致能信號(ENFT)217 來產生控制信號 219 以控制開關電路 205。當每一脈衝信號(TP1)213 產生時，源極驅動晶片會經由第一通道 201 以及第二通道 203，將用來驅動液晶面板上第一資料線的第一驅動電壓，或是用來驅動第二資料線的第二驅動電壓傳遞至開關電路 205，然後再由開關電路 205 根據控制信號 219，選擇將第一驅動電壓或是第二驅動電壓輸出至測試焊墊 207。

請參照第 3 圖，其係繪示面板控制信號之時序以及測試焊墊之輸出波形，包括脈衝信號(TP1)213、極性信號(POL)215、最終測試致能信號(ENFT)217 以及測試焊墊之輸出波形 309。在最終測試階段，最終測試致能信號 217 會在脈衝信號 213 的每兩個脈衝之間進行一次邏輯位準之切換，以選擇輸出第一驅動電壓或是第二驅動電壓，極性信號 215 則賦予第一驅動電壓或是第二驅動電壓極性。

舉例來說，當最終測試致能信號(ENFT)217 具有一第一邏輯位準，也就是第 3 圖中的區間 301，控制電路 209 會依據最終測試致能信號 217 以及極性信號(POL)215 產生相應的控制信號 219，使開關電路 205 將具有第一極性的第一驅動電壓輸出至測試焊墊 207。再舉區間 303 來做說明，當最終測試致能信號 217 具有一第二邏輯位準時，控制信號 219 會控制開關電路 205，將具有第二極性第二驅動電壓輸出至測試焊墊 207。

請參照第 4 圖，其係繪示開關電路 205 之內部電路，包括第一電晶體 401、第二電晶體 403、第三電晶體 405、第四電晶體 407、以及第五電晶體 409。第二電晶體 403 以及第三電晶體 405 之第一源汲極係電性連接至第一通道 201，第四電晶體 407 以及第五電晶體 409 之第一源汲極則電性連接至第二通道 203。

第二電晶體 403 以及第四電晶體 407 之第二源汲極電性連接測試焊墊 207 以及第一電晶體 401 之第一源及極，第三電晶體 405 以及第五電晶體 409 之第二源汲極則電性連接第一電晶體 401 之第二源汲極。第一控制信號 411、第二控制信號 413、第三控制信號 415、第四控制信號 417 以及第五控制信號 419 則分別電性連接至第一電晶體 401、第二電晶體 403、第三電晶體 405、第四電晶體 407、以及第五電晶體 409 之閘極。

請參照第 5 圖，其係表列最終測試致能信號、脈衝信號以及極性信號與第一、第二、第三、第四、第五控制信號之關係以及測試焊墊之相應輸出結果。

當脈衝信號 213 產生之時，最終測試致能信號 217、極性信號 215 將使第一控制信號 411、第二控制信號 413、第三控制信號 415、第四控制信號 417 以及第五控制信號 419 具有應有的邏輯位準以關閉第一電晶體 401、第二電晶體 403、第三電晶體 405、第四電晶體 407、以及第五電晶體 409，使得該第一通道 201 以及該第二通道 203 與測試焊墊 207 隔離，測試焊墊上的輸出呈現一高阻抗狀態。

當脈衝信號 213 結束，且最終測試致能信號 217 具有第二邏輯位準時，第一控制信號 411 導通第一電晶體 401，並由第三控制信號 415 導通第三電晶體 405 以輸出具有第一極性之第二驅動電壓；或是由第五控制信號 419 導通第五電晶體 409 以輸出具有第二極性之第二驅動電壓。

當脈衝信號 213 結束，且最終測試致能信號 217 具有第一邏輯位準時，第一控制信號 411 關閉第一電晶體 401，並由第二控制信號 413 導通第二電晶體 403 以輸出具有第一極性之第一驅動電壓；或是由第四控制信號 417 導通第四電晶體 407 以輸出具有第二極性之第一驅動電壓。

綜上所述，路徑切換裝置與其上的控制信號，能夠在脈衝信號 TP1 之每兩個脈衝之間，輸出第一驅動電壓以及第二驅動電壓至同一測試焊墊，使得測試探針能夠在一個脈衝信號週期內，由同一測試焊墊量測到第一驅動電壓以及第二驅動電壓，測試焊墊的數目因而可以減少一半。

雖然本發明已以實施例揭露如上，然其並非用以限定本發明，任何在本發明所屬技術領域中，具有通常知識者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤

飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者為準。

【圖式簡單說明】

為讓本發明之上述和其他目的、特徵、優點與實施例能更明顯易懂，所附圖式之詳細說明如下：

第 1 圖係繪示傳統驅動晶片在最終測試階段的測試裝置。

第 2 圖係繪示依照本發明一實施例的一種路徑切換裝置。

第 3 圖係繪示依照本發明一實施例的面板控制信號之時序以及測試焊墊之輸出波形。

第 4 圖係繪示開關電路之內部電路。

第 5 圖係表列最終測試致能信號、脈衝信號以及極性信號與第一、第二、第三、第四、第五控制信號之關係以及測試焊墊之相應輸出結果。

【主要元件符號說明】

101：樹脂層	103：薄膜
105：測試焊墊	107：金屬走線
109：外引腳	111：鉾阻
200：路徑切換裝置	201：第一通道
203：第二通道	205：開關電路
207：測試焊墊	209：控制電路
213：脈衝信號	215：極性信號

217：最終測試致能信號	219：控制信號
301：區間	303：區間
309：測試焊墊之輸出波形	
401：第一電晶體	403：第二電晶體
405：第三電晶體	407：第四電晶體
409：第五電晶體	411：第一控制信號
413：第二控制信號	415：第三控制信號
417：第四控制信號	
419：第五控制信號	

十、申請專利範圍：

1.一種路徑切換裝置，用以在一晶片進行最終測試時切換該晶片之輸出路徑，其中該晶片具有一第一通道以及一第二通道，該路徑切換裝置包含：

一測試焊墊；以及

一開關電路，用以選擇地將該第一通道或該第二通道連接至該測試焊墊。

2.如申請專利範圍第 1 項所述之路徑切換裝置，其中該晶片在一脈衝信號之每一脈衝產生時，經由該第一通道以及該第二通道平行輸出一第一驅動電壓以及一第二驅動電壓，該開關電路則在一最終測試致能信號具有一第一邏輯位準以及一第二邏輯位準時，分別將該第一驅動電壓以及該第二驅動電壓輸出至該測試焊墊，且該最終測試致能信號係在該脈衝信號之每兩個脈衝之間進行一次該第一邏輯位準以及該第二邏輯位準之切換。

3.如申請專利範圍第 2 項所述之路徑切換裝置，其中該第一驅動電壓以及該第二驅動電壓係分別用以驅動一液晶面板上之一第一資料線以及一第二資料線。

4.如申請專利範圍第 2 項所述之路徑切換裝置，其中該晶片在一極性信號具有該第一邏輯位準時使該第一驅動電壓以及該第二驅動電壓分別具有一第一極性以及一第二極

性，而在該極性信號具有該第二邏輯位準時使該第一驅動電壓以及該第二驅動電壓分別具有該第二極性以及該第一極性。

5.如申請專利範圍第4項所述之路徑切換裝置，其中該開關電路包含：

一第一電晶體，其第一源汲極電性連接於該測試焊墊，其閘極電性連接於一第一控制信號；

一第二電晶體，其第一源汲極電性連接於該第一通道，其第二源汲極電性連接於該第一電晶體之第一源汲極，其閘極電性連接於一第二控制信號；

一第三電晶體，其第一源汲極電性連接於該第一通道，其第二源汲極電性連接於該第一電晶體之第二源汲極，其閘極電性連接於一第三控制信號；

一第四電晶體，其第一源汲極電性連接於該第二通道，其第二源汲極電性連接於該第一電晶體之第一源汲極，其閘極電性連接於一第四控制信號；以及

一第五電晶體，其第一源汲極電性連接於該第二通道，其第二源汲極電性連接於該第一電晶體之第二源汲極，其閘極電性連接於一第五控制信號。

6.如申請專利範圍第5項所述之路徑切換裝置，更包含一控制電路，電性連接於該開關電路，該控制電路係根據該脈衝信號、該最終測試致能信號以及該極性信號分別輸出該第一邏輯位準或該第二邏輯位準至該些控制信號以控

制該些電晶體之導通。

7.如申請專利範圍第 5 項所述之路徑切換裝置，其中當該脈衝信號產生時，該控制電路輸出該第一邏輯位準以及該第二邏輯位準至該些控制信號以關閉該些電晶體，使得該第一通道以及該第二通道與該測試焊墊隔離。

8.如申請專利範圍第 5 項所述之路徑切換裝置，其中當該最終測試致能信號具有該第二邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至該第一控制信號以導通該第一電晶體，藉以使該第二驅動電壓輸出至該測試焊墊。

9.如申請專利範圍第 8 項所述之路徑切換裝置，其中當該極性信號具有該第二邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至第三控制信號以導通該第三電晶體，藉以使具有該第一極性之該第二驅動電壓經由該第一通道輸出至該測試焊墊。

10.如申請專利範圍第 8 項所述之路徑切換裝置，其中當該極性信號具有該第一邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至該第五控制信號以導通該第五電晶體，藉以使具有該第二極性之該第二驅動電壓經由該第二通道輸出至該測試焊墊。

11.如申請專利範圍第 5 項所述之路徑切換裝置，其中當該最終測試致能信號具有該第一邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至該第一控制信號以關閉該第一電晶體，藉以使該第一驅動電壓輸出至該測試焊墊。

12.如申請專利範圍第 11 項所述之路徑切換裝置，其中當該極性信號具有該第二邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至第四控制信號以導通該第四電晶體，使得具有該第二極性之該第一驅動電壓經由該第二通道輸出至該測試焊墊。

13.如申請專利範圍第 12 項所述之路徑切換裝置，其中當該極性信號具有該第一邏輯位準時，該控制電路輸出該第一邏輯位準或該第二邏輯位準至第二控制信號以導通該第二電晶體，藉以使具有該第一極性之該第一驅動電壓經由該第一通道輸出至該測試焊墊。

14.如申請專利範圍第 1 項所述之路徑切換裝置，其中當該晶片使用覆晶薄膜技術貼附於一薄膜上時，該開關電路係內建於該晶片中，且該測試焊墊係配置於該薄膜上。

15.如申請專利範圍第 1 項所述之路徑切換裝置，其中當該晶片之最終測試完成後，該開關電路分別將該第一輸出通道以及該第二輸出通道連接至該晶片之一第一輸出端

以及一第二輸出端。

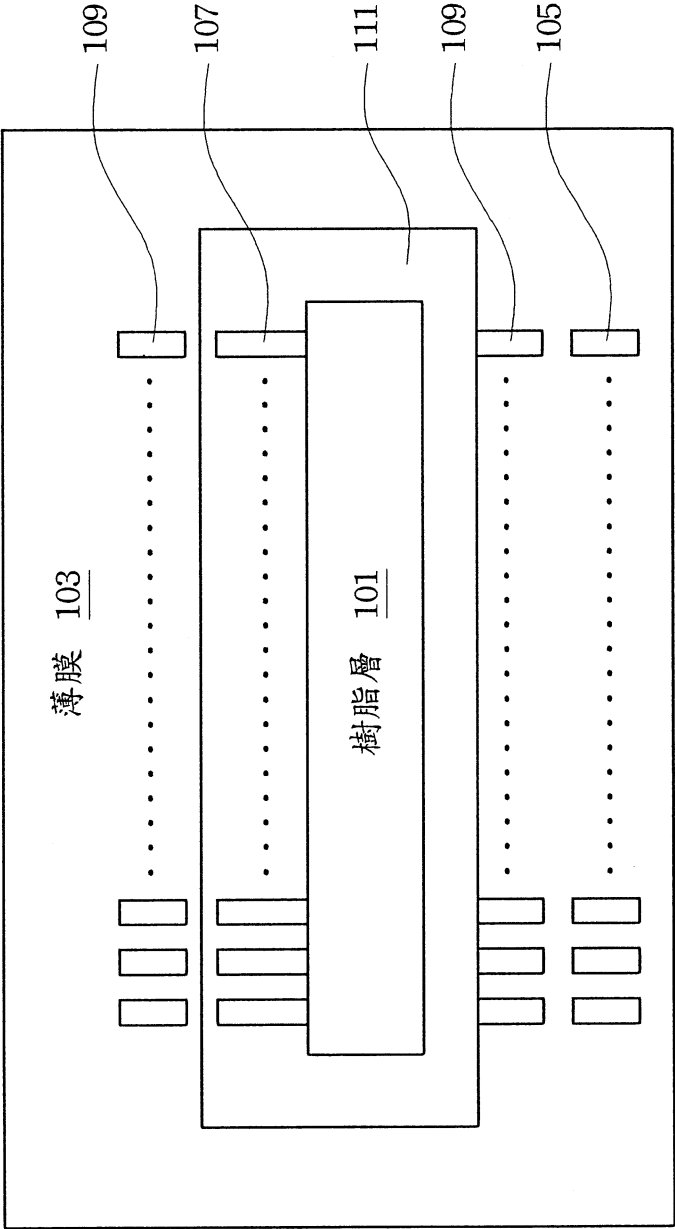
16.一種測試焊墊之減少方法，係使用於一晶片之最後測試階段，該方法包含：

當一最終測試致能信號具有一第一邏輯位準時輸出一第一驅動電壓至該測試焊墊，當該最終測試致能信號具有一第二邏輯位準時輸出一第二驅動電壓至該測試焊墊。

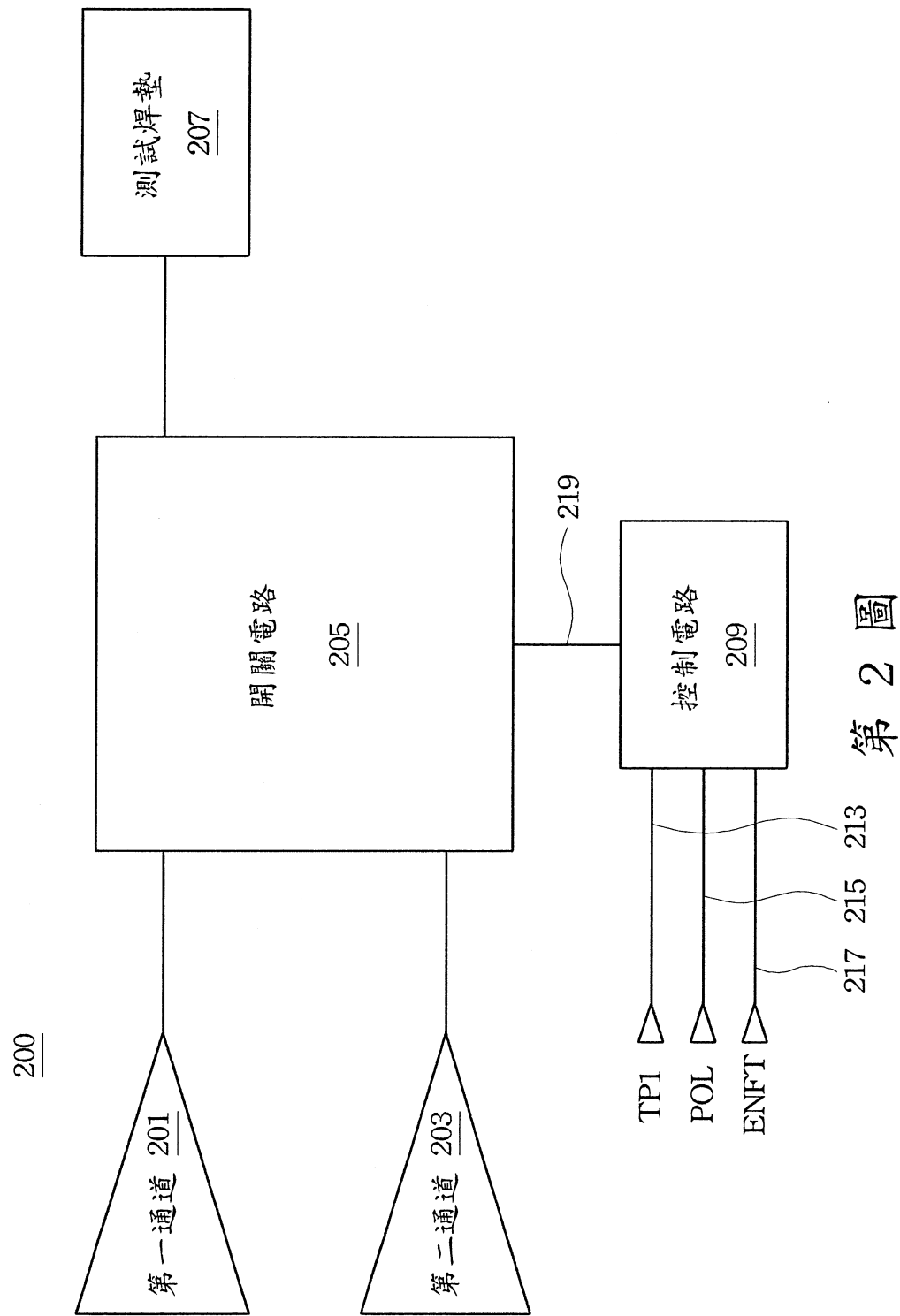
17.如申請專利範圍第 16 項所述之方法，其中該最終測試致能信號係在一脈衝信號之每兩個脈衝之間進行一次該第一邏輯位準以及該第二邏輯位準之切換。

18.如申請專利範圍第 16 項所述之方法，其中該第一驅動電壓以及該第二驅動電壓在一極性信號具有該第一邏輯位準時分別具有一第一極性以及一第二極性，而在該極性信號具有該第二邏輯位準時該第一驅動電壓以及該第二驅動電壓分別具有該第二極性以及該第一極性。

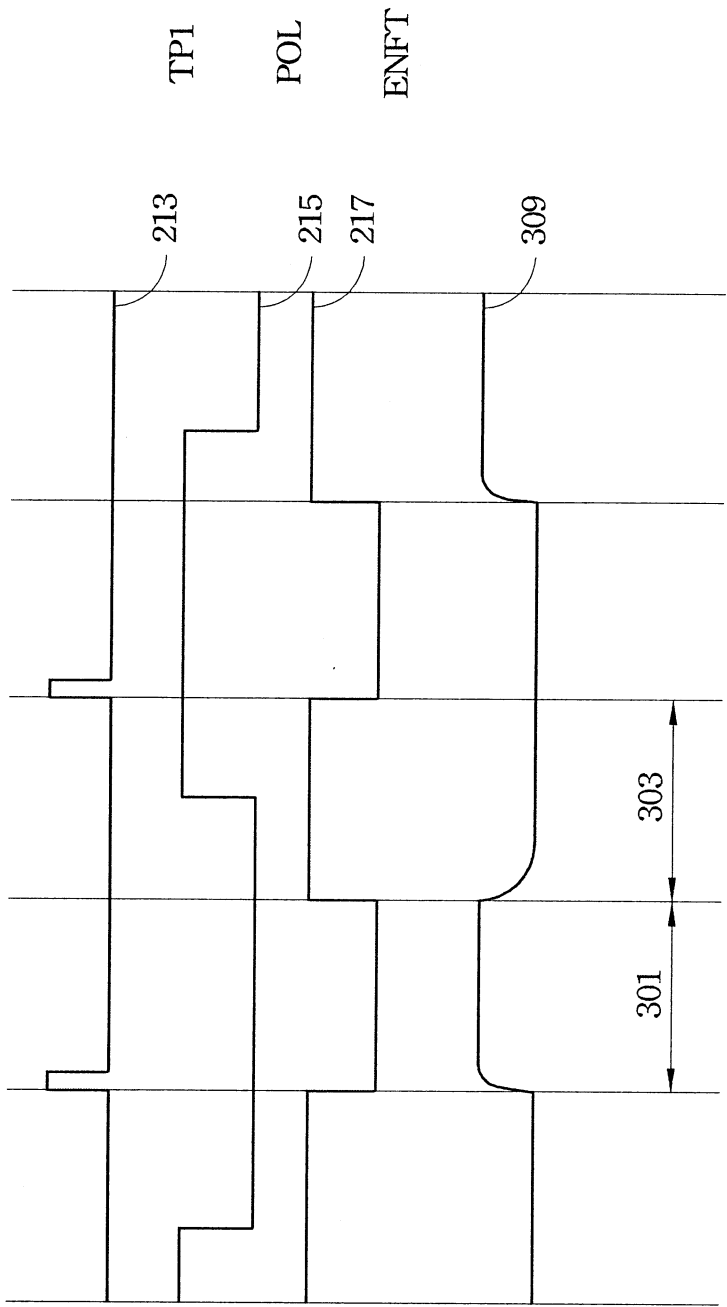
19.如申請專利範圍第 16 項所述之方法，其中該第一驅動電壓以及該第二驅動電壓係分別用以驅動一液晶面板上之一第一資料線以及一第二資料線。



第 1 圖



第 2 圖



第 3 圖

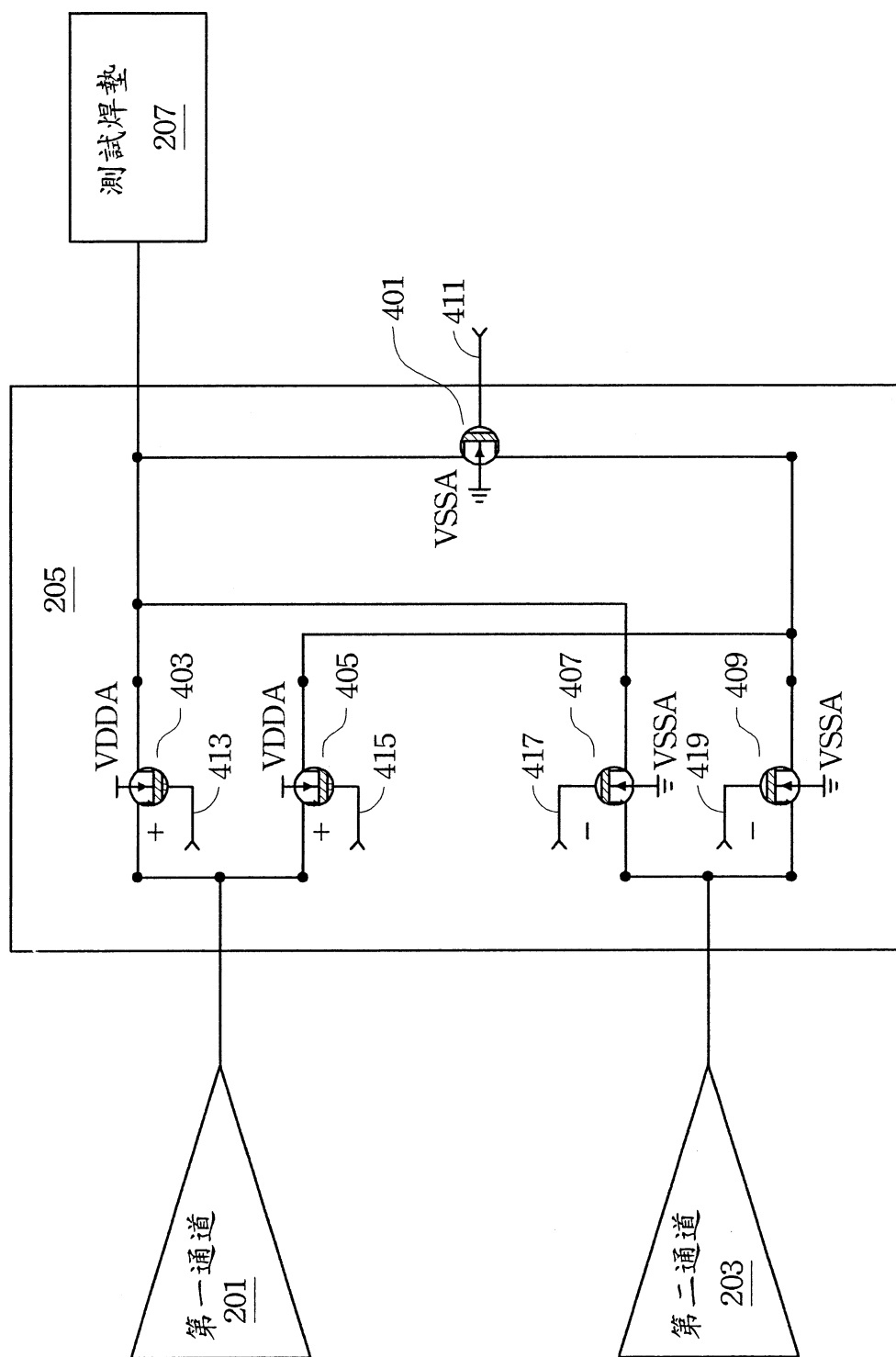


圖
4
策

217 (ENFT)	213 (TP1)	215 (POL)	411	413	415	417	419	測試焊墊207之輸出
0	0	0	0	0	1	0	1	第一極性之第一驅動電壓
0	1	0	0	1	1	0	0	高阻抗狀態
1	0	0	1	1	1	0	1	第二極性之第二驅動電壓
0	0	1	0	1	0	1	0	第二極性之第一驅動電壓
0	1	1	0	1	1	0	0	高阻抗狀態
1	0	1	1	1	0	0	0	第一極性之第二驅動電壓

第 5 圖

[19] Republic of China [12] Invention Publication Gazette (A)

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[54] Title of the Invention: A SWITCHING CIRCUIT AND A METHOD FOR REDUCING TEST PAD

[21] Application Number: 095147504

[22] Filing Date: December 18, 2006

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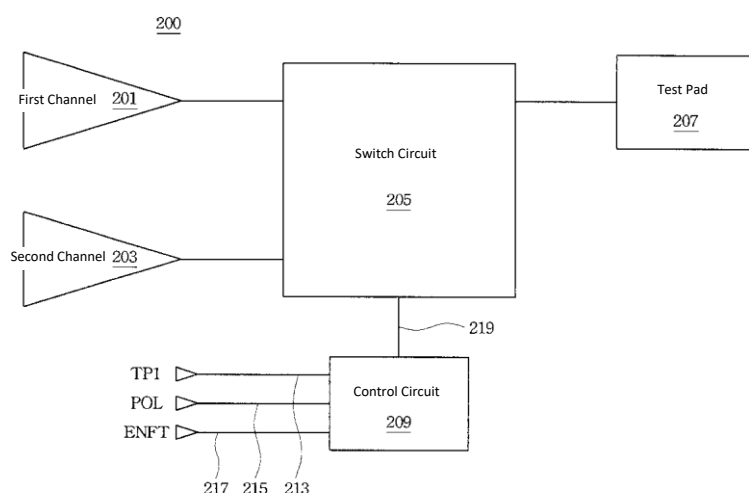
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[57] Abstract of the Invention

A method for reducing test pads and a path switching device used therefor are configured to switch the output path of a chip during the final testing phase of the chip. The chip has a first channel and a second channel, and the path switching device includes a test pad and a switch circuit. The switch circuit is used to selectively connect the first channel or the second channel to the test pad. When the final test enable signal has a first logic level or a second logic level, the switch circuit transmits the first driving voltage or the second driving voltage thereon to the test pad through the first channel or the second channel, respectively.



200: Path Switching Device
201: First Channel
203: Second Channel
205: Switch Circuit
207: Test Pad
209: Control Circuit
213: Pulse Signal
215: Polarity Signal
217: Final Test Enable Signal
219: Control Signal

Representative Drawing

Invention Patent Specification

(The format, sequence, and bolded text in this specification must not be altered arbitrarily. Do not fill in the parts marked with ※)

※ **Application No.:** 95147504

※ **Filing Date:** December 18, 2006

※ **IPC Classification:** H01L 21/66

I. Title of Invention: (Chinese/English)

路徑切換裝置以及測試焊墊之減少方法

**A SWITCHING CIRCUIT AND A METHOD FOR REDUCING TEST
PAD**

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IV. Statements:

☐ The facts prescribed in ☐ Subparagraph 1 or ☐ Subparagraph 2 of Paragraph 2 of Article 22 of the Patent Act are claimed, and the occurrence date of such facts is:

Year Month Day .

☐ Prior to this application, the patent has been filed in the following countries (regions):

[Please note the information in the following order: Receiving Country (Region), Filing Date, Application Number]

☐ Claiming the international priority under Paragraph 1 of Article 27 of the Patent Act:

1.

2.

☐ Not claiming the international priority under Paragraph 1 of Article 27 of the Patent Act:

☐ Claiming the domestic priority under Paragraph 1 of Article 29 of the Patent Act:

[Please note the information in the following order: Filing Date, Application Number]

☐ Claiming biological materials under Article 30 of the Patent Act:

☐ Biological materials that need to be deposited:

Domestic biological materials [Please note the information in the following order: Depository institution, Date, Number]

Foreign biological materials [Please note the information in the following order: Depositing country, Institution, Date, Number]

☐ Biological materials that do not need to be deposited:

Deposition is not required if the biological materials are easily obtainable by a person of ordinary skill in the relevant technical field.

V. Chinese Abstract**路徑切換裝置以及測試焊墊之減少方法**

測試焊墊之減少方法以及其所使用的路徑切換裝置，係用以在一晶片之最終測試階段，切換晶片之輸出路徑，其中晶片具有一第一通道以及一第二通道，路徑切換裝置則包括測試焊墊以及開關電路，其中開關電路係用以選擇地將第一通道或第二通道連接至測試焊墊，當最終測試致能信號具有第一邏輯位準或第二邏輯位準時，開關電路則藉由第一通道或第二通道，分別將其上的第一驅動電壓或第二驅動電壓傳送至測試焊墊。

VI. English Abstract**A switching circuit and a method for reducing test pad**

A switching device and a method for reducing test pad which switch the output driving voltage of the source driver during the final test period. The source driver has a first channel and a second channel, and the switch device includes a test pad and a switch circuit. The switch circuit is used to select one of the first channel and second channel to connect to the test pad. The switch circuit delivers either the first driving voltage or the second driving voltage to the test pad through the first channel and the second channel according to the logic level of an Enable Final Test signal.

VII. Designated Representative Figure:

- (1) The designated representative figure for this case is: FIG. (2)
- (2) Brief description of reference numerals in the representative figure for this case:
 - 200: Path switching device
 - 201: First channel
 - 203: Second channel
 - 205: Switching circuit
 - 207: Test pad
 - 209: Control circuit
 - 213: Pulse signal
 - 215: Polarity signal
 - 217: Enable final test signal
 - 219: Control signal

VIII. If chemical formulas are involved in this case, the chemical formula(s) that best reflect the inventive feature shall be disclosed:

IX. Description**[Technical Field]**

The present invention relates to a testing device and method for a gate driver circuit of a liquid crystal display, and particularly to a testing device and method for a gate driver circuit in a final test stage.

[Related Art]

In recent years, a Chip On Film (COF) process can provide small-sized displays to meet general consumers' demands for light, thin, short, and small displays, and therefore, a packaging method of driver ICs has evolved from the Tape Automatic Bonding (TAB) process to the COF process.

The COF process is a type of Flip Chip Bonding technology that bonds electronic elements to a Flexible or Film Printed Circuit board (FPC) which allows a source driver chip of a display and its electronic elements to be directly mounted on a film, eliminating the need for a traditional printed circuit board and achieving the objective of making the display light, thin, short, and small.

Referring to FIG. 1, a testing device for a source driver chip in a final test stage is illustrated, including a resin layer 101, a film 103, a test pad 105, a metal wire 107, an external pin 109, and a solder mask 111. The resin layer 101 is used to wrap a source driver chip (not shown in the figure), and the metal wire 107 is used to be coupled to the source driver chip inside the resin layer 101. The source driver chip, the resin layer 101, the test pad 105, the metal wire 107, and the external pin 109 are arranged on the film 103.

In such a testing device, an output of each source drive voltage needs to have a test pad coupled to it so that a test probe can test each source drive voltage through each of these test pads. However, due to the large number of source drive voltages, the number of test pads must also increase accordingly, which significantly increases the volume and manufacturing cost of the testing device.

Therefore, a new testing device and method are required to reduce the number of test pads, thereby reducing the volume and cost of the testing device.

[Summary of Invention]

Therefore, one aspect of the present invention is to provide a path switching device that reduces the number of test pads required for a source driver chip in a final test stage.

According to an embodiment of the present invention, the path switching device is configured to switch an output path of a Chip On Film (COF) chip in a final test stage of the chip. The COF chip has a first channel and a second channel. The path switching device includes a test pad and a switching circuit. The switching circuit is configured to selectively connect the first channel and the second channel to the test pad.

Another aspect of the present invention is to provide a method for reducing a test pad, which is used for reducing the number of test pads required for a source driver chip in a final test stage.

According to another embodiment of the present invention, the method for reducing a test pad is used in a final test stage of a source driver chip. The method

outputs a first drive voltage to the test pad when an enable final test signal has a first logic level and outputs a second drive voltage to the test pad when the enable final test signal has a second logic level.

According to the above embodiments, the path switching device and the method for reducing a test pad can reduce the number of test pads required for the source driver chip in the final test stage.

[Detailed Description]

Referring to FIG. 2, a path switching device according to an embodiment of the present invention is illustrated. The path switching device 200 includes a first channel 201, a second channel 203, a switching circuit 205, a control circuit 209, and a test pad 207. The first channel 201, the second channel 203, the switching circuit 205, and the control circuit 209 are located on a source driver chip. The test pad 207 is arranged on a film.

The control circuit 209 generates a control signal 219 based on a pulse signal (TP1) 213, a polarity signal (POL) 215, and an enable final test signal (ENFT) 217 to control the switching circuit 205. When each pulse signal (TP1) 213 is generated, the source driver chip may transmit, through the first channel 201 and the second channel 203, a first drive voltage for driving a first data line or a second drive voltage for driving a second data line on a liquid crystal display panel to the switching circuit 205. Then, the switching circuit 205 selects, based on the control signal 219, to output the first drive voltage or the second drive voltage to the test pad 207.

Referring to FIG. 3, a timing of a panel control signal and an output waveform of a test pad are illustrated, including the pulse signal (TP1) 213, the polarity signal (POL) 215, the enable final test signal (ENFT) 217, and an output waveform 309 of the test pad. In the final test stage, the enable final test signal 217 may perform a logic level switching every two pulses of the pulse signal 213, so as to select to output the first drive voltage or the second drive voltage, and the polarity signal 215 imparts a polarity to the first drive voltage or the second drive voltage.

For example, when the enable final test signal (ENFT) 217 has a first logic level, that is, an interval 301 in FIG. 3, the control circuit 209 may generate a corresponding control signal 219 based on the enable final test signal 217 and the polarity signal (POL) 215, causing the switching circuit 205 to output the first drive voltage with a first polarity to the test pad 207. By taking an interval 303 for further illustration, when the enable final test signal 217 has a second logic level, the control signal 219 may control the switching circuit 205 to output a second drive voltage with a second polarity to the test pad 207.

Referring to FIG. 4, an internal circuit of the switching circuit 205 is illustrated, including a first transistor 401, a second transistor 403, a third transistor 405, a fourth transistor 407, and a fifth transistor 409. First source-drains of the second transistor 403 and the third transistor 405 are electrically connected to the first channel 201. First source-drains of the fourth transistor 407 and the fifth transistor 409 are electrically connected to the second channel 203.

Second source-drains of the second transistor 403 and the fourth transistor 407 are

electrically connected to the test pad 207 and the first source-drain of the first transistor 401, and second source-drains of the third transistor 405 and the fifth transistor 409 are electrically connected to the second source-drain of the first transistor 401. A first control signal 411, a second control signal 413, a third control signal 415, a fourth control signal 417, and a fifth control signal 419 are respectively electrically connected to gates of the first transistor 401, the second transistor 403, the third transistor 405, the fourth transistor 407, and the fifth transistor 409.

Referring to FIG. 5, a table of relationships between the enable final test signal, the pulse signal, the polarity signal, and the first, second, third, fourth, and fifth control signals, as well as corresponding output results of the test pad are shown.

When the pulse signal 213 is generated, the enable final test signal 217 and the polarity signal 215 may cause the first control signal 411, the second control signal 413, the third control signal 415, the fourth control signal 417, and the fifth control signal 419 to have respective due logic levels to turn off the first transistor 401, the second transistor 403, the third transistor 405, the fourth transistor 407, and the fifth transistor 409, so that the first channel 201 and the second channel 203 are isolated from the test pad 207, and an output on the test pad presents a high-impedance state.

When the pulse signal 213 ends and the enable final test signal 217 has the second logic level, the first control signal 411 turns on the first transistor 401, and the third control signal 415 turns on the third transistor 405 to output a second drive voltage with the first polarity. Alternatively, the fifth control signal 419 turns on the fifth transistor 409 to output a second drive voltage with the second polarity.

When the pulse signal 213 ends and the enable final test signal 217 has the first logic level, the first control signal 411 turns off the first transistor 401, and the second control signal 413 turns on the second transistor 403 to output a first drive voltage with the first polarity. Alternatively, the fourth control signal 417 turns on the fourth transistor 407 to output a first drive voltage with the second polarity.

In view of the above, the path switching device and the control signals thereon can output, between every two pulses of the pulse signal TP1, the first drive voltage and the second drive voltage to the same test pad, allowing a test probe to measure the first drive voltage and the second drive voltage from the same test pad within one pulse signal cycle. As a result, the number of test pads can be reduced by half.

Although the present invention has been disclosed above through embodiments, they are not intended to limit the present invention. Any person with ordinary skill in the art to which the present invention belongs can make various modifications and refinements without departing from the spirit and scope of the present invention. Therefore, the protection scope of the present invention shall be defined by the appended claims.

[Brief Description of the Drawings]

In order to make the above and other objectives, features, advantages, and embodiments of the present invention more obvious and understandable, detailed explanation of accompanying drawings is described as follows:

FIG. 1 illustrates a traditional testing device for a driver chip in a final test stage.

FIG. 2 illustrates a path switching device according to an embodiment of the present invention.

FIG. 3 illustrates a timing of a panel control signal and an output waveform of a test pad according to an embodiment of the present invention.

FIG. 4 illustrates an internal circuit of a switching circuit.

FIG. 5 is a table of relationships between an enable final test signal, a pulse signal, a polarity signal, and first, second, third, fourth, and fifth control signals, as well as corresponding output results of a test pad.

[Description of Main Reference Numerals]

101: Resin layer	103: Film
105: Test pad	107: Metal wire
109: External pin	111: Solder mask
200: Path switching device	201: First channel
203: Second channel	205: Switching circuit
207: Test pad	209: Control circuit
213: Pulse signal	215: Polarity signal
217: Enable final test signal	219: Control signal
301: Interval	303: Interval
309: Output waveform of the test pad	
401: First transistor	403: Second transistor
405: Third transistor	407: Fourth transistor
409: Fifth transistor	411: First control signal
413: Second control signal	415: Third control signal
417: Fourth control signal	419: Fifth control signal

X. Claims

1. A path switching device configured to switch an output path of a chip during a final test of the chip, wherein the chip has a first channel and a second channel, the path switching device comprising:

a test pad; and

a switching circuit configured to selectively connect the first channel or the second channel to the test pad.

2. The path switching device of claim 1, wherein the chip outputs a first drive voltage and a second drive voltage in parallel through the first channel and the second channel when each pulse of a pulse signal is generated, the switching circuit outputs the first drive voltage and the second drive voltage to the test pad respectively when an enable final test signal has a first logic level and a second logic level, and the enable final test signal switches between the first logic level and the second logic level once every two pulses of the pulse signal.

3. The path switching device of claim 2, wherein the first drive voltage and the second drive voltage are respectively used to drive a first data line and a second data line on a liquid crystal display panel.

4. The path switching device of claim 2, wherein the chip causes the first drive voltage and the second drive voltage to have a first polarity and a second polarity, respectively, when a polarity signal has the first logic level, and causes the first drive voltage and the second drive voltage to have the second polarity and the first polarity, respectively, when the polarity signal has the second logic level.

5. The path switching device of claim 4, wherein the switching circuit comprises:

a first transistor with its first source-drain electrically connected to the test pad and its gate electrically connected to a first control signal;

a second transistor with its first source-drain electrically connected to the first channel, its second source-drain electrically connected to the first source-drain of the first transistor, and its gate electrically connected to a second control signal:

a third transistor with its first source-drain electrically connected to the first channel, its second source-drain electrically connected to a second source-drain of the first transistor, and its gate electrically connected to a third control signal;

a fourth transistor with its first source-drain electrically connected to the second channel, its second source-drain electrically connected to the first source-drain of the first transistor, and its gate electrically connected to a fourth control signal; and

a fifth transistor with its first source-drain electrically connected to the second channel, its second source-drain electrically connected to the second source-drain of the first transistor, and its gate electrically connected to a fifth control signal.

6. The path switching device according to claim 5, further comprising a control circuit electrically connected to the switching circuit, wherein the control circuit outputs the first logic level or the second logic level respectively to the control signals based on the pulse signal, the enable final test signal, and the polarity signal, to control the transistors to be turned on.

7. The path switching device of claim 5, wherein when the pulse signal is generated,

the control circuit outputs the first logic level and the second logic level to the control signals to turn off the transistors, so that the first channel and the second channel are isolated from the test pad.

8. The path switching device of claim 5, wherein when the enable final test signal has the second logic level, the control circuit outputs the first logic level or the second logic level to the first control signal to turn on the first transistor, so that the second drive voltage is output to the test pad.

9. The path switching device of claim 8, wherein when the polarity signal has the second logic level, the control circuit outputs the first logic level or the second logic level to the third control signal to turn on the third transistor, so that the second drive voltage with the first polarity is output to the test pad through the first channel.

10. The path switching device of claim 8, wherein when the polarity signal has the first logic level, the control circuit outputs the first logic level or the second logic level to the fifth control signal to turn on the fifth transistor, so that the second drive voltage with the second polarity is output to the test pad through the second channel.

11. The path switching device of claim 5, wherein when the enable final test signal has the first logic level, the control circuit outputs the first logic level or the second logic level to the first control signal to turn off the first transistor, so that the first drive voltage is output to the test pad.

12. The path switching device of claim 11, wherein when the polarity signal has the second logic level, the control circuit outputs the first logic level or the second logic level to the fourth control signal to turn on the fourth transistor, so that the first drive voltage with the second polarity is output to the test pad through the second channel.

13. The path switching device of claim 12, wherein the polarity signal has the first logic level, the control circuit outputs the first logic level or the second logic level to the second control signal to turn on the second transistor, so that the first drive voltage with the first polarity is output to the test pad through the first channel.

14. The path switching device of claim 1, wherein when the chip is attached to a film using a Chip On Film process, the switching circuit is built in the chip, and the test pad system is arranged on the film.

15. The path switching device of claim 1, wherein after the final test of the chip is completed, the switching circuit connects the first output channel and the second output channel to a first output terminal and a second output terminal of the chip, respectively.

16. A method for reducing a test pad, used in a final test stage of a chip, the method comprising:

outputting a first drive voltage to the test pad when an enable final test signal has a first logic level, and outputting a second drive voltage to the test pad when the enable final test signal has a second logic level.

17. The method of claim 16, wherein the enable final test signal switches between the first logic level and the second logic level once every two pulses of a pulse signal.

18. The method of claim 16, wherein the first drive voltage and the second drive voltage have a first polarity and a second polarity, respectively, when a polarity signal has the first logic level, and the first drive voltage and the second drive voltage have the second polarity and the first polarity, respectively, when the polarity signal has the

second logic level.

19. The method of claim 16, wherein the first drive voltage and the second drive voltage are respectively used to drive a first data line and a second data line on a liquid crystal display panel.

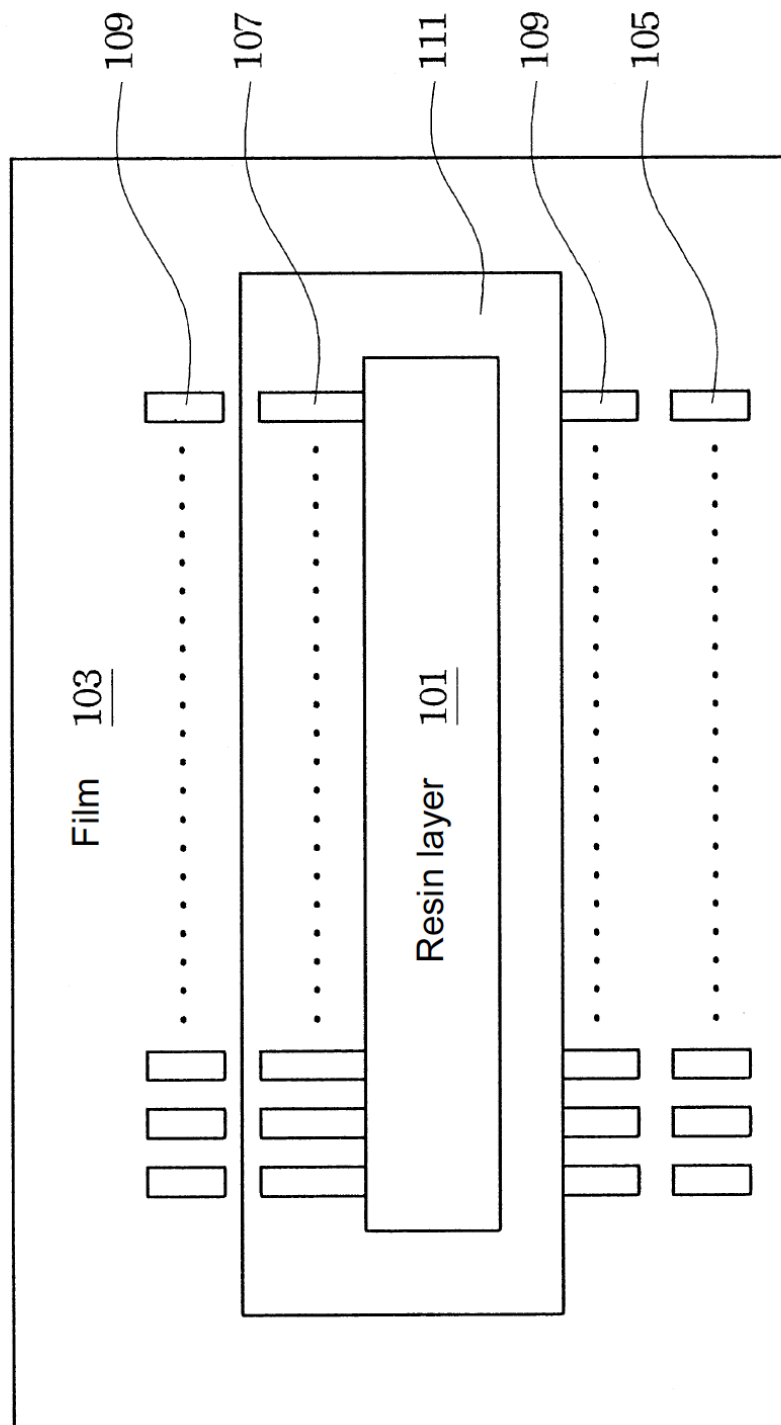


FIG. 1

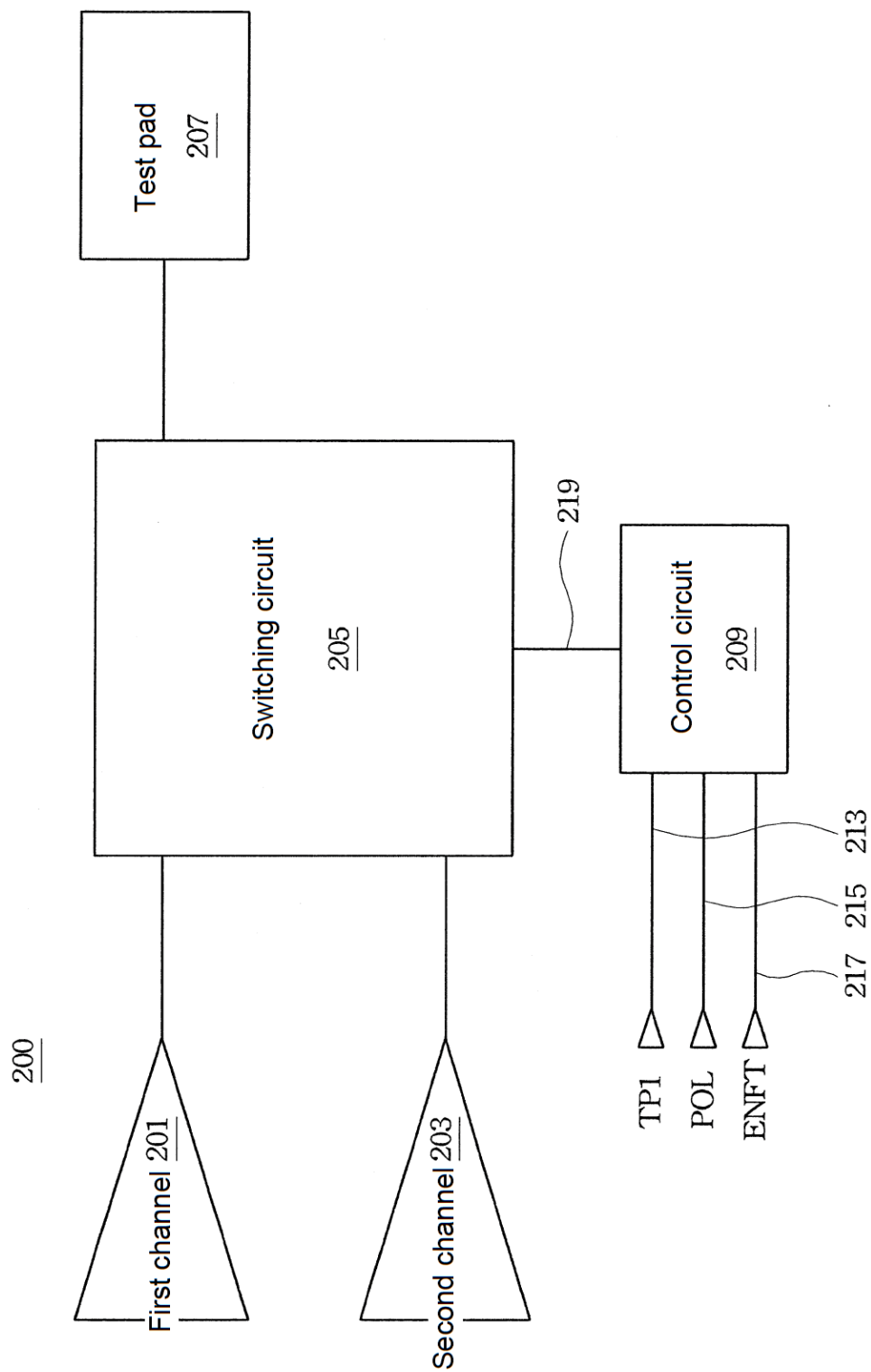


FIG. 2

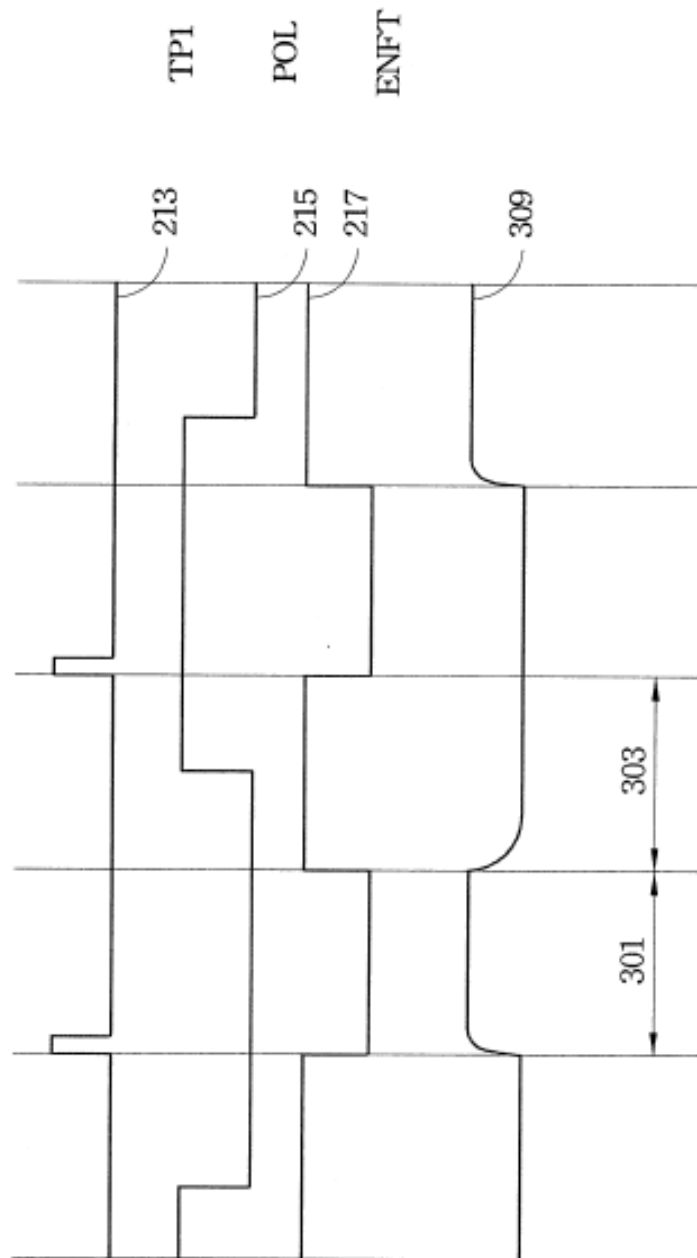


FIG. 3

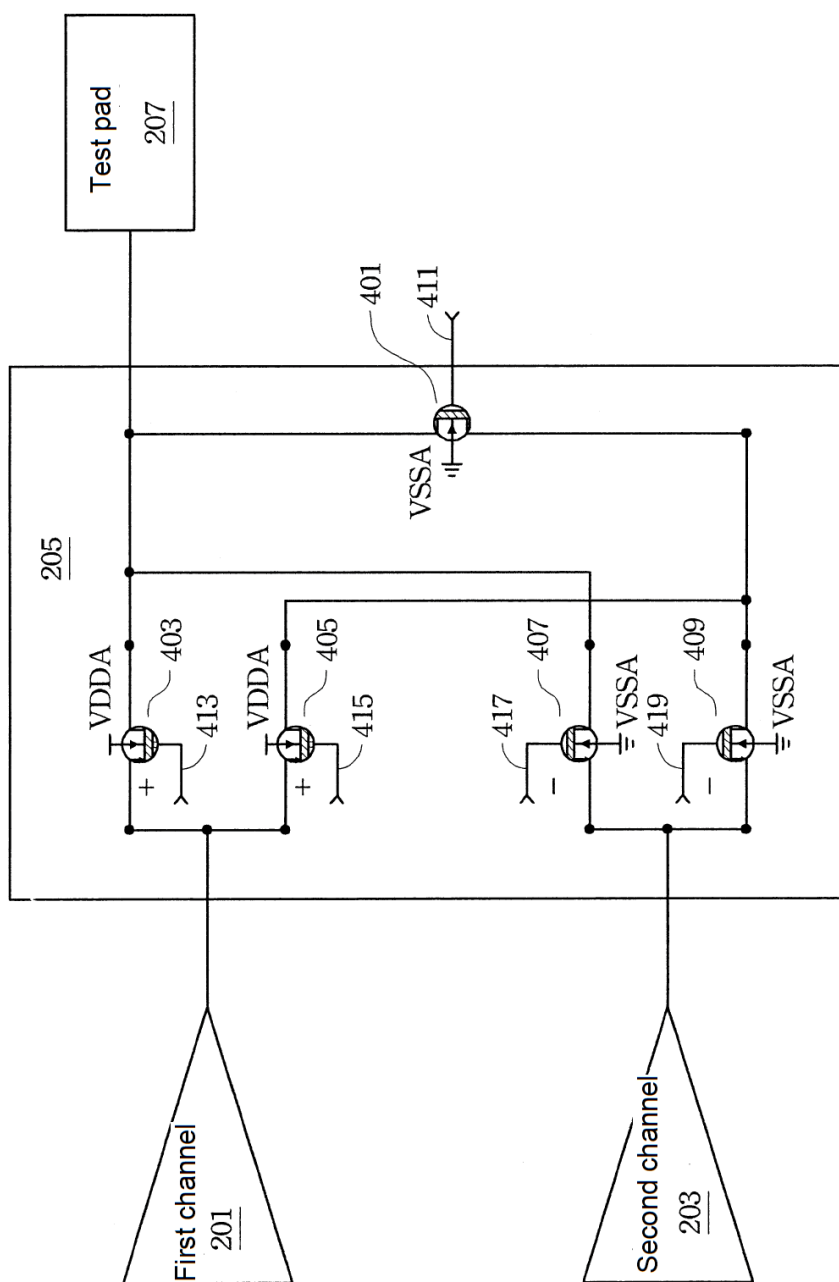


FIG. 4

217 (ENFT)	213 (TPI)	215 (POL)	411	413	415	417	419	Output of the test pad 207
0	0	0	0	0	1	0	1	First drive voltage with first polarity
0	1	0	0	1	1	0	0	High-impedance state
1	0	0	1	1	1	0	1	Second drive voltage with second polarity
0	0	1	0	1	0	1	0	First drive voltage with second polarity
0	1	1	0	1	1	0	0	High-impedance state
1	0	1	1	1	0	0	0	Second drive voltage with first polarity

FIG. 5

TRANSLATION CERTIFICATION

Date: August 26, 2025

To whom it may concern:

This is to certify that the attached translation is an accurate representation of the documents received by this office. The translation was completed from:

- Chinese (Taiwan)

To:

- English (USA)

The documents are designated as:

- D1 - TW200828476A

Emily Paras, Project Manager in this company, attests to the following:

"To the best of my knowledge, the aforementioned documents are a true, full and accurate translation of the specified documents."



Signature of Emily Paras

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