

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.

Petitioner

v.

138 EAST LCD ADVANCEMENTS LIMITED,

Patent Owner.

PTAB Case No. IPR 2025-01413

U.S. Patent No. 8,319,512

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,319,512
CHALLENGING CLAIMS 1-12**

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EXHIBIT LIST

Exhibit No.	Document
Ex. 1001	U.S. Patent No. 8,319,512 (“’512 patent”)
Ex. 1002	Declaration and Curriculum Vitae of Dr. Manos M. Tentzeris
Ex. 1003	File History of the ’512 patent
Ex. 1004	U.S. Patent No. 6,300,997 (“Saito”)
Ex. 1005	U.S. Patent Application Publication No. 2002/0139567 (“Kim”)
Ex. 1006	U.S. Patent Application Publication No. 2004/0183985 (“Taguchi”)
Ex. 1007	U.S. Patent Application Publication No. 2004/0183563 (“Her”)
Ex. 1008	U.S. Patent No. 5,592,199 (“Kawaguchi”)
Ex. 1009	U.S. Patent Application Publication No. 2003/0095227 (“Kohtaka”)
Ex. 1010	U.S. Patent Application Publication No. 2003/0155908 (“Ohazama”)
Ex. 1011	Japanese Application Publication No. JP2000131393 (“Sugano”)
Ex. 1012	U.S. Patent No. 5,644,331 (“Hazama”)
Ex. 1013	U.S. Patent Application Publication No. 2007/0226569 (“Her- 569”)
Ex. 1014	Taiwan Patent Application Publication No. 200828476 (“Chen”)

Petitioner BOE Technology Group Co., Ltd. (“BOE” or “Petitioner”) respectfully requests *inter partes* review (“IPR”) of claims 1-12 of U.S. Patent No. 8,319,512.

I. INTRODUCTION

The Supreme Court has instructed that, when evaluating obviousness, “a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). For the claims of the ’512 patent, the answer to this question is a resounding no. All claims of the ’512 patent represent predictable combinations of prior art elements that had been taught in patents and printed publications published several years prior to the earliest priority date—nearly all of which stem from competitors in the same field as the original patent owner—thus demonstrating that any purported invention contained in the ’512 claims was “well within the grasp of a person of ordinary skill in the relevant art.” *Id.* at 427. Therefore, Petitioner asks the Board to cancel all challenged claims.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner BOE is the sole real party-in-interest for this Petition.

B. Related Matters

Patent Owner 138 East LCD Advancements Limited with its exclusive licensee Longitude Licensing Limited (collectively “Patent Owner” or “138 East LCD”) has alleged, in two separate cases, that BOE infringes the ’512 patent: *Longitude Licensing v. BOE, et al.*, No. 2:25-cv-440 (E.D. Tex.) (filed April 25, 2025) and *Longitude Licensing v. BOE, et al.*, No. 2:25-cv-358 (E.D. Tex.) (filed April 8, 2025). In Case No. 2:25-cv-440, 138 East LCD has also sued LG Electronics, Inc., which allegedly sells TVs incorporating BOE LCD panels. In Case No. 2:25-cv-358, 138 East LCD has also sued Hisense Group Holdings Co. Ltd. *et al.* (“Hisense”), which allegedly sells TVs incorporating BOE LCD panels.

Finally, Petitioner is also filing petitions for *inter partes* review challenging two other patents also asserted in the above-listed litigations, U.S. Patent No. 7,636,146 (IPR 2025-01396) and U.S. Patent No. 8,391,020 (IPR 2025-01412).

C. Counsel and Service Information

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Petitioner consents to electronic service. All services and communications to the attorneys listed above may be sent to BOEIPRService@hklaw.com. A Power of Attorney is concurrently filed with this Petition.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '512 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the '512 patent on the grounds presented here. This Petition is filed less than one year after BOE was served with a complaint alleging infringement.

B. Overview of Challenges and Requested Relief

Pursuant to Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner requests cancellation of claims 1-12 of the '512 patent under pre-AIA 35 U.S.C. § 103.

1. Identification of Prior Art

In this Petition, Petitioner relies on the patents and printed publications listed in the Table of the Exhibits, including:

Exhibit No.	Prior Art Basis
Exhibit 1004: U.S. Patent No. 6,300,997 ("Saito")	Saito issued on October 9, 2001, and is prior art at least under (pre-AIA) §102(b).

Exhibit No.	Prior Art Basis
Exhibit 1005: U.S. Patent Application Publication No. 2002/0139567 (“Kim”)	Kim published on October 3, 2002, and is prior art at least under (pre-AIA) §102(b).
Exhibit 1006: U.S. Patent Application Publication No. 2004/0183985 (“Taguchi”)	Taguchi published on September 23, 2004, and is prior art at least under (pre-AIA) §102(b).
Exhibit 1007: U.S. Patent Application Publication No. 2004/0183563 (“Her”)	Her published on September 23, 2004, and is prior art at least under (pre-AIA) §102(b).

The Examiner did not cite or discuss any of the prior art cited as Grounds (or cited as Background) in this Petition during the ’512 prosecution.

2. Grounds for Challenge

Saito Grounds		
Ground 1	Claims 1-4, 6 and 8-11	Obvious over Saito and Her
Ground 2	Claim 5	Obvious over Saito and Her, in further view of Taguchi
Ground 3	Claims 2, 7 and 12	Obvious over Saito and Her, in further view of Kim

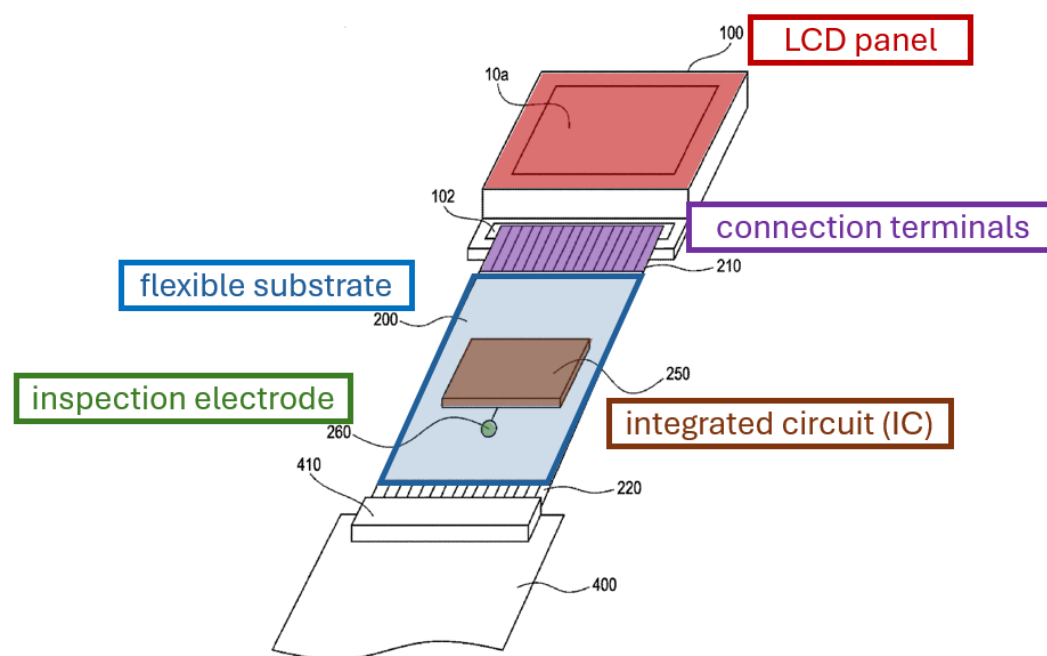
Taguchi Grounds		
Ground 4	Claims 1-6 and 8	Obvious over Taguchi and Her
Ground 5	Claims 9-11	Obvious over Taguchi and Her, in further view of Saito
Ground 6	Claims 2, 7 and 12	Obvious over Taguchi and Her, in further view of Saito and Kim

Dr. Manos M. Tentzeris's declaration ("Tentzeris") supports this Petition and demonstrates a reasonable likelihood that Petitioner will prevail with respect to the cancellation of at least one challenged claim. *See* 35 U.S.C. § 314(a). Dr. Tentzeris's declaration and CV are attached as Exhibit 1002.

IV. OVERVIEW OF THE '512 PATENT

A. The Alleged Invention

The '512 patent describes using an integrated circuit mounted on a flexible substrate to drive a connected liquid-crystal panel. (Ex.1001, 1:22-24.) The '512 further describes forming a test pad, or "inspection electrode," on the substrate that can be used to monitor one or more electrical signals. (*Id.*, 1:43-56.) The inspection electrode is "exposed to the outside of the flexible substrate" to facilitate access by a "reading probe or the like." (*Id.*, 2:12-25.) This is depicted in Figure 4:



B. The Prosecution History

The '512 patent claims priority to a Japanese application filed on March 23, 2009. (Ex.1001, Cover.) Only one office action issued during prosecution rejecting most claims but indicating that dependent claims 3 and 4 “would be allowable if rewritten in independent form.” (Ex.1003 at 101.) In rejecting claim 1, the Examiner concluded that “the term ‘inspection electrode’ is a broad term and it does not contribute any significant meaning to the scope of the instant claim.” (*Id.* at 100.)

The Applicant overcame the rejection by amending claim 1 to incorporate claim 3 and added additional claims. (*Id.* at 129-133.) The Applicant did not traverse the Examiner’s interpretation of “inspection electrode.” (*Id.*) Following this, twelve claims were allowed. (*Id.* at 146.)

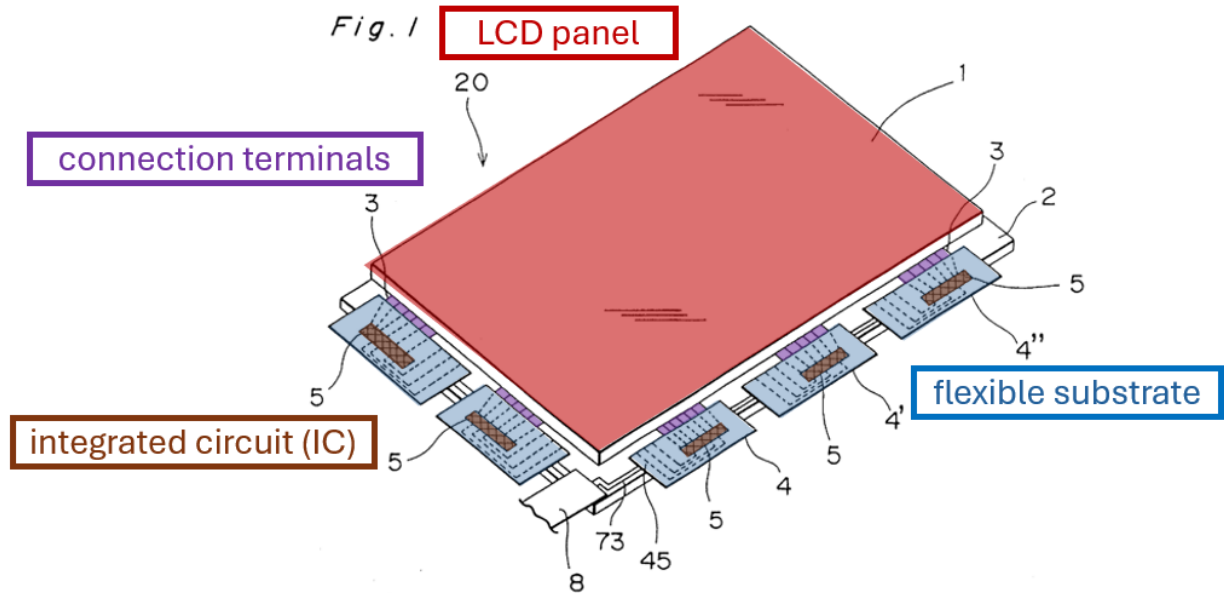
C. The Alleged Priority Date

For this Petition only, Petitioner assumes the priority date is March 23, 2009. The U.S. filing date for purposes of (pre-AIA) §102(b) is March 12, 2010.

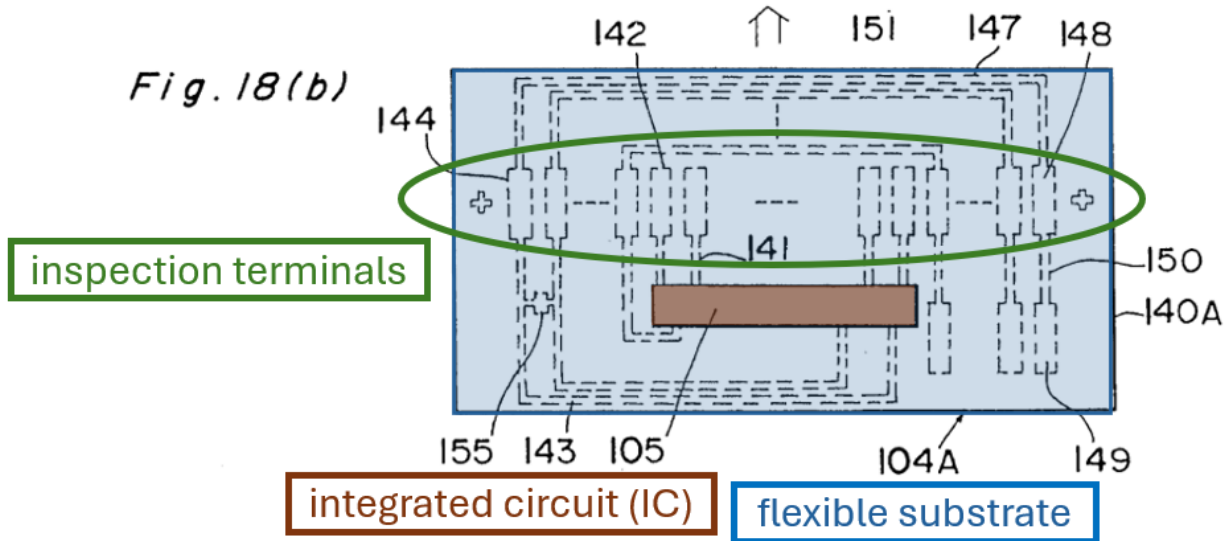
D. State of the Art

The '512 patent discloses only conventional features that were well known in the industry. The '512 patent originally was assigned to Seiko Epson based in Japan. Myriad other Asia-based companies practiced everything in the '512 patent long before its March 2009 priority date.

By January 1994, Sharp (also in Japan) disclosed “a flexible wiring board on which a drive IC for driving [an LCD] panel is mounted [that] is electrically connected to the electrode terminals of the panel” (Ex.1008, 2:34-37):



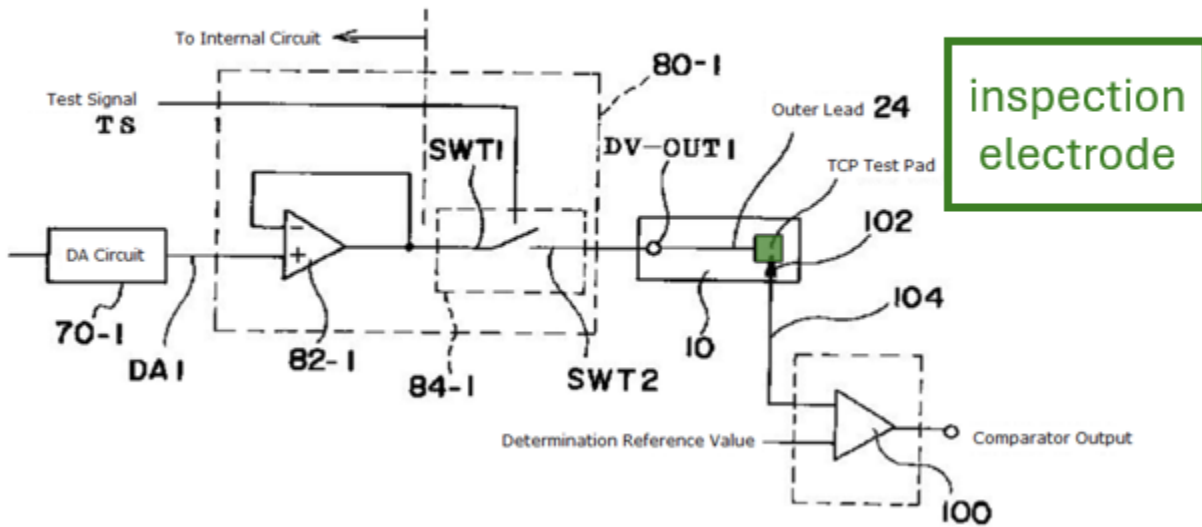
Sharp also disclosed using external probes to test electrical contacts patterned on the flexible substrate, namely, “a prober terminal for performance tests can be put in contact with the terminals.” (*Id.*, 6:59-63). As seen below, “with the flexible wiring board 104 connected to the peripheral portion of the liquid crystal panel 120, a prober terminal for performance tests can be thrown in contact with the input terminal 144, output terminals 142, or third junction terminal 148 of the flexible wiring board 104” (*id.*, 22:55-61):



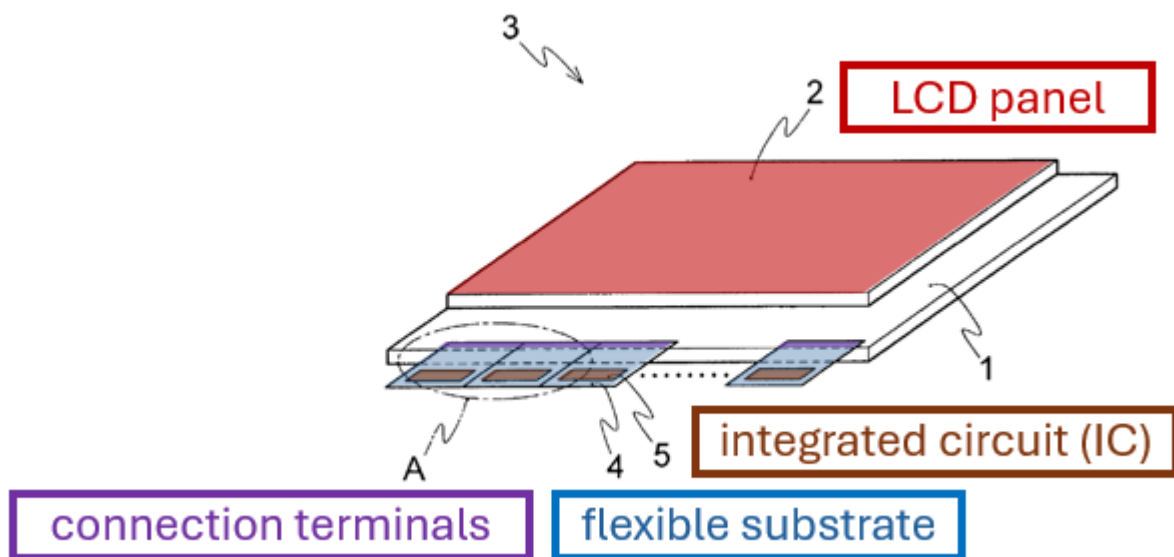
Indeed, Japanese electronics heavyweight Sony remarked that by 1994, such “inspection-use output terminals” for testing LCD driver ICs had become “the conventional method of inspection.” (Ex.1012, 1:50-53.)

In 1998, Oki Electric in Japan similarly disclosed using “a liquid crystal display driver IC” that is “mounted” on a flexible substrate called a “TCP” and “connected to a liquid crystal panel at the lead terminals.” (Ex.1011, [0017]; [0025-28].) The substrate also employed a variety of “test pads” patterned on the substrate. (*Id.*) Oki Electric also taught using an internal switch controlled by a “test signal” (TS) to turn on and off the signal output to the “test pad”:

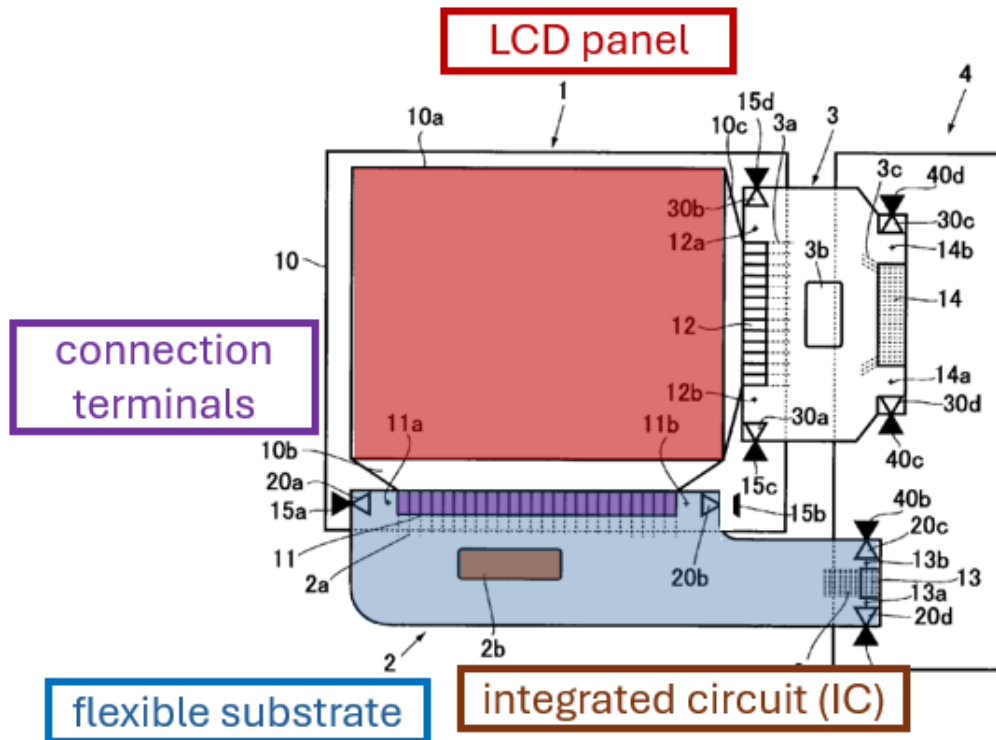
[FIG. 3]



Many other well-known Japanese companies, including Advanced Display and Pioneer, likewise were using ICs mounted on flexible substrates to drive LCD panels years before the '512 priority date:



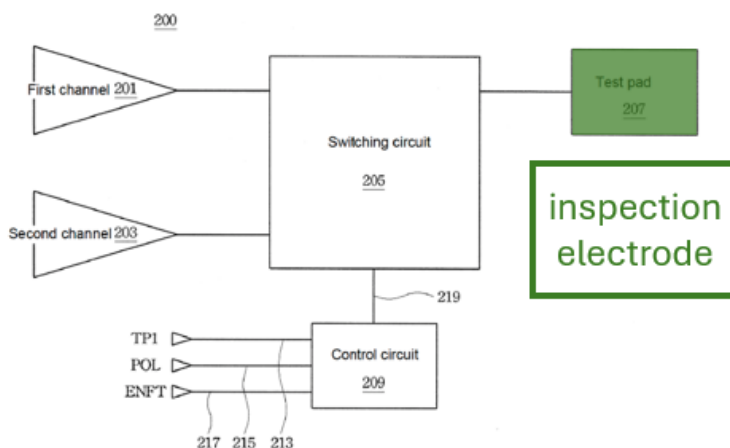
(Ex.1009, Figure 1; [0029].)



(Ex.1010, Figure 1; [0040-42].)

This pre-existing technology was not limited to Japan. By 2006, Korean display giant Samsung was using chips mounted on flexible substrates “such as a chip-on-film (COF)” to “transmit[] a signal generated by a display driver to a display panel.” (Ex.1013, [0005].) By that date, Samsung considered the use of “test pads” patterned on the flexible substrate to be part of “a conventional film-type semiconductor package.” (*Id.*, [0007-09]; Figures 1 and 4.) Samsung also was using switches for turning on/off the signal output to a given “test pad,” and further using switches to send two signal types to a single test pad. (*Id.*, [0067-68]; Figure 8A.)

Himac Technologies in Taiwan likewise described using the “Chip On Film (COF)” methodology to allow “a source driver chip of a [liquid crystal] display and its electronic elements to be directly mounted” on a “Flexible” film where the “output of each source drive voltage needs to have a test pad coupled to it so that a test probe can test each source drive voltage through each of these test pads.” (Ex.1014 at 28.) Himac also disclosed a “switching circuit 205” to select the type of signal output from “the test pad 207” and thereby “reduce the number of test pads required for the source drive chip” (*id.* at 29; Figure 2):



Against this backdrop, Seiko-Epson filed for patent in March 2010 (claiming Japan priority) seeking coverage for this commonplace arrangement of a “flexible substrate” with “an integrated circuit that is arranged on the substrate body . . . and an inspection electrode that is arranged on the substrate body and electrically connected to the integrated circuit and capable of outputting a signal processed in the integrated circuit.” (Ex.1001, Abstract.)

V. CLAIM CONSTRUCTION

At this time, Petitioner does not believe construction of any term is necessary to resolve the patentability challenges set forth in this Petition. *See Vivid 10 Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Petitioner reserves the right to construe terms in the litigation or to respond to any constructions that Patent Owner presents in this proceeding.

VI. LEVEL OF ORDINARY SKILL

As of the alleged March 23, 2009 priority date, a POSITA is a person having at least a bachelor-level degree in electrical or mechanical engineering, or a related subject, and two or more years of experience working in the field of semiconductor substrates and related circuitry. Additional education may substitute for professional experience, and significant work experience may substitute for formal education. (Ex.1002, ¶¶26-27.)

VII. DESCRIPTION OF THE CITED PRIOR ART

A. Saito

Saito relates to LCD devices having a panel connected to an IC chip mounted on a flexible film wiring board. (Ex.1004, 1:14–16; 6:22-26.) Saito teaches that as the number of these substrate-mounted IC chips, or “IC modules” increases, so does the required process time, and the physical width of the film wiring boards limits compact integration. (Ex.1004, 1:30–40.)

Saito proposes making the contact terminal region of the LCD panel shorter than the overall panel width and optimizing wiring layout. (Ex.1004, 2:21–25.) A semiconductor chip is mounted on a central portion of a film wiring board, with output lead wires extending from the chip to terminals arranged at different locations along the panel edge. (Ex.1004, 4:8–16, 1:63–2:7; 2A–2B; Ex.1002, ¶¶44–47.)

FIG.2A

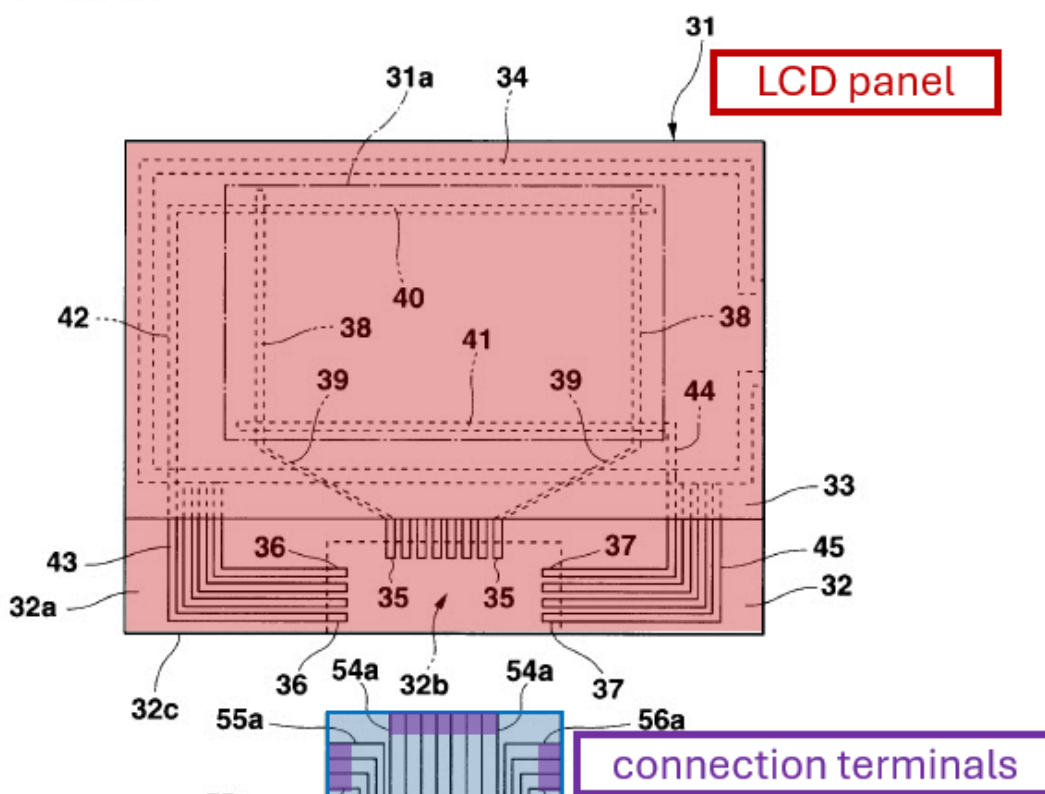
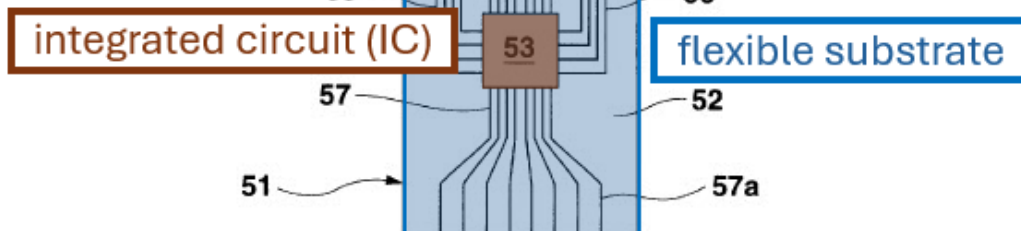


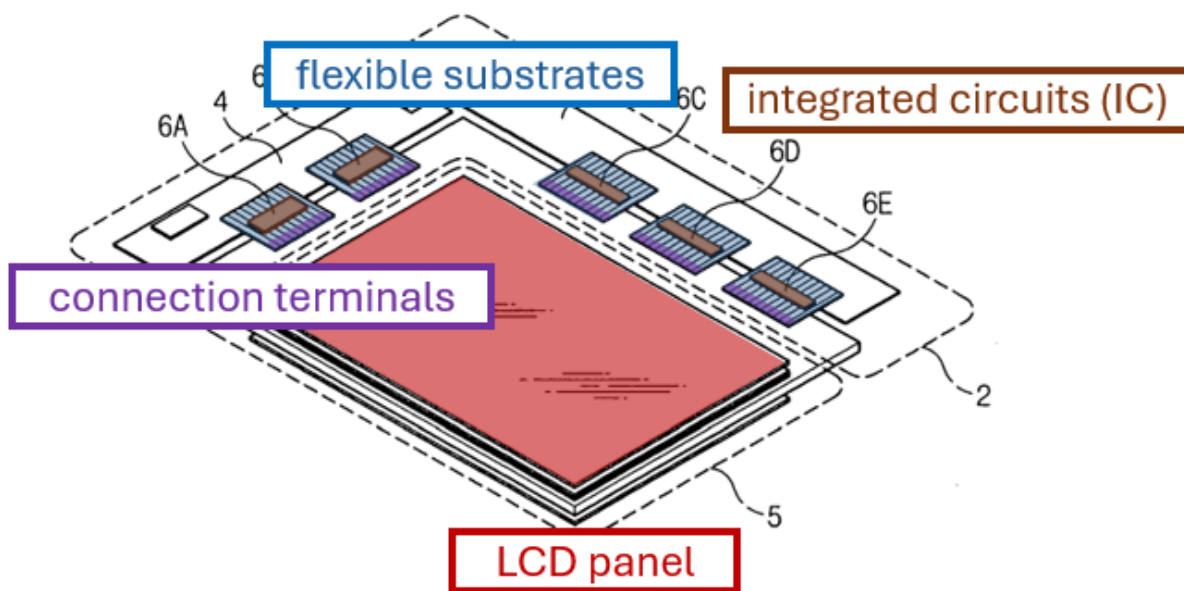
FIG.2B



Saito also discloses test pads formed on intermediate portions of the output wires. These test pads permit electrical continuity checks using test pins. (Ex.1004, 5:23–33.) By integrating test pads into the layout, Saito reduces space requirements while enabling chip-level testing, thereby improving manufacturing yield and reliability. (*Id.*, 5:46–59; Ex.1002, ¶¶44-47.)

B. Her

Her is directed to “an LCD panel 5” (Ex.1007, ¶[0003]) and “a plurality of gate driver ICs 6A-6C and source driving ICs 6C-6E for driving a panel 5” (*id.*, ¶[0004]), as seen in Figure 1:

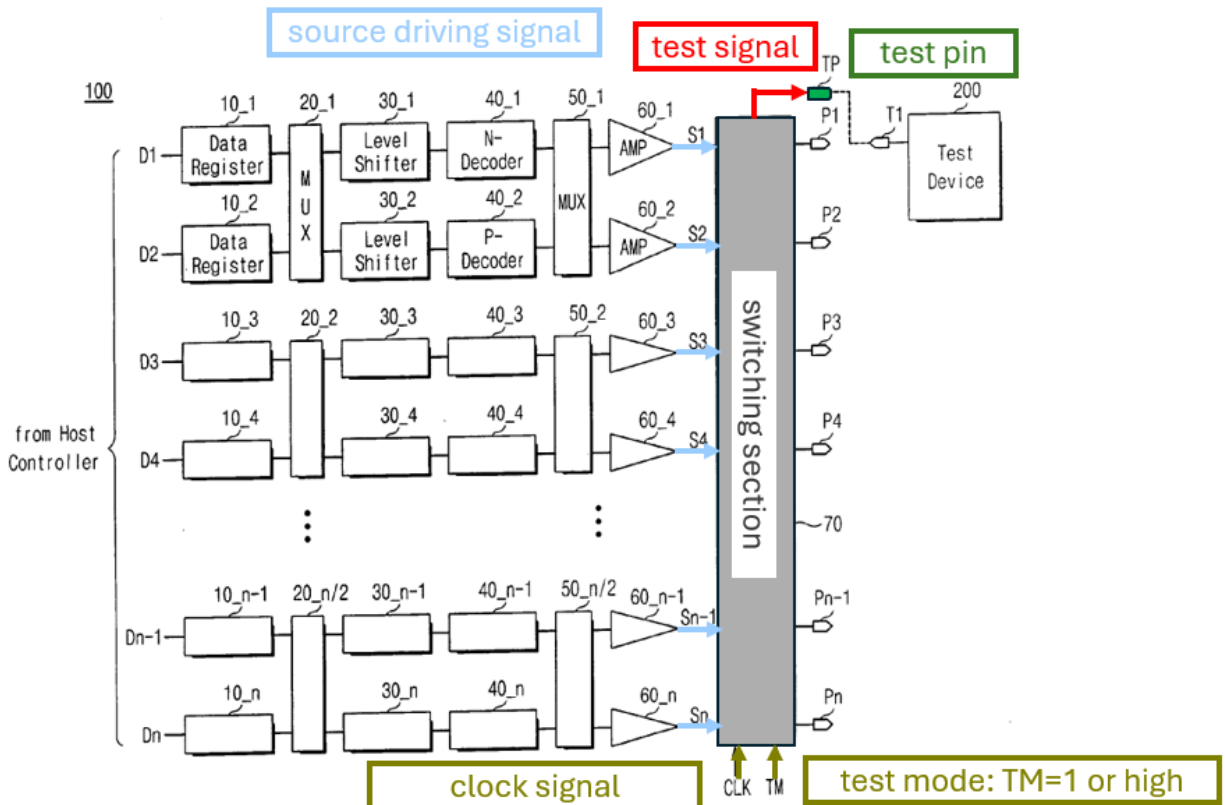


Her explains that a test device conventionally must have test pins equal to the number of data output pins of the IC under test. As high-resolution displays require

ICs with increasing pin counts, this one-to-one correspondence becomes inefficient and costly. (Ex.1007, ¶¶[0001]–[0007].)

Her discloses an integrated circuit having a test mode in which the output signals—normally output through separate data output pins—are combined into a new composite signal and then sequentially output through a single dedicated test pin. (Ex.1007, at ¶¶[0008]–[0009], [0021]–[0036].) In normal mode, the IC drives the display using source driving signals output through output pins. In test mode, however, the circuit uses switching logic to turn off the output pins and creates a new composite signal that is sent to a test pin, reducing the number of pins and equipment needed for testing. (Ex.1007, ¶¶ [0021]–[0036].)

Figure 2 illustrates Her’s IC including a designated “test pin TP” intended for connection to an external “test device 200” (*id.*, ¶[0034]). This includes “channel shifter 70” that acts as a switching section and controls the operation of “test pin TP.” (*Id.*, [0028].) “The channel shifter 70 operates in response to a test mode signal TM” (*id.*, [0029]):



“The test mode signal TM has a low level (i.e., logic “0”) in a normal mode and has a high level (i.e., logic “1”) in a test mode.” (*Id.*, ¶[0029]; Figure 3.) The switching section of channel shifter 70 “determines whether the test mode signal TM indicates a test mode.” (*Id.*, ¶[0030]). If the TM signal “indicates a test mode (i.e., high level),” the channel shifter 70 switches the test pin TP “on” and “sequentially outputs the source driving signals S1~Sn” in a composite “signal” to the test pin TP “in response to a clock signal CLK.” (*Id.*, [0032]; Figure 3.) In contrast, “[w]hen the test mode signal TM indicates the normal mode, not the test mode” (*id.*, ¶[0030-31]) the channel shifter switches the test pin TP “off,” and “the source driving signals S1-Sn . . . are provided to the LCD panel through the data output pins P1-Pn” (*id.*, ¶[0028]).

This structure reduces the number of required test pins, eliminates the need for parallel signal detection, and simplifies test equipment, making it well-suited for testing high-pin-count integrated circuits used in LCD displays. (Ex.1007, ¶¶[0008]–[0010], [0022-0034]; Ex.1002, ¶¶48-53.)

C. Taguchi

Taguchi discloses an LCD apparatus that includes an insulation film substrate connected to a panel, and addresses testing drive signal lines without relying on conventional substrates. (Ex.1006, ¶¶[0003], [0025].)

In conventional LCD apparatuses, drive signals are supplied to thin film transistors (TFTs) on a liquid crystal panel using patterned wires on an insulation film substrate. (Ex.1006, ¶ [0005]–[0007].) These patterned wires often have extremely narrow widths, making it difficult to establish reliable electrical contact for testing. (Ex.1006, ¶¶ [0011], [0023].)

Taguchi discloses providing test pads on the substrate itself. (Ex.1006, ¶¶[0026]–[0028].) These test pads are patterned as widened portions of the wire, often circular in shape, providing sufficient area to enable easy and reliable contact with test probes. (Ex.1006, ¶¶ [0057]–[0059], Figs. 7, 8; *also* Figure 2.)

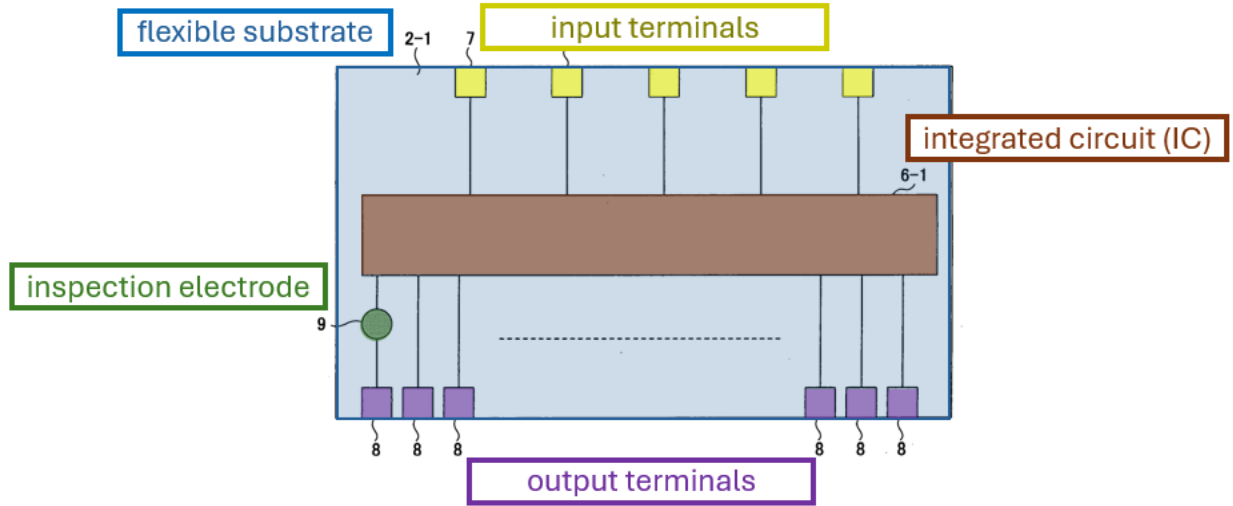


FIG. 7

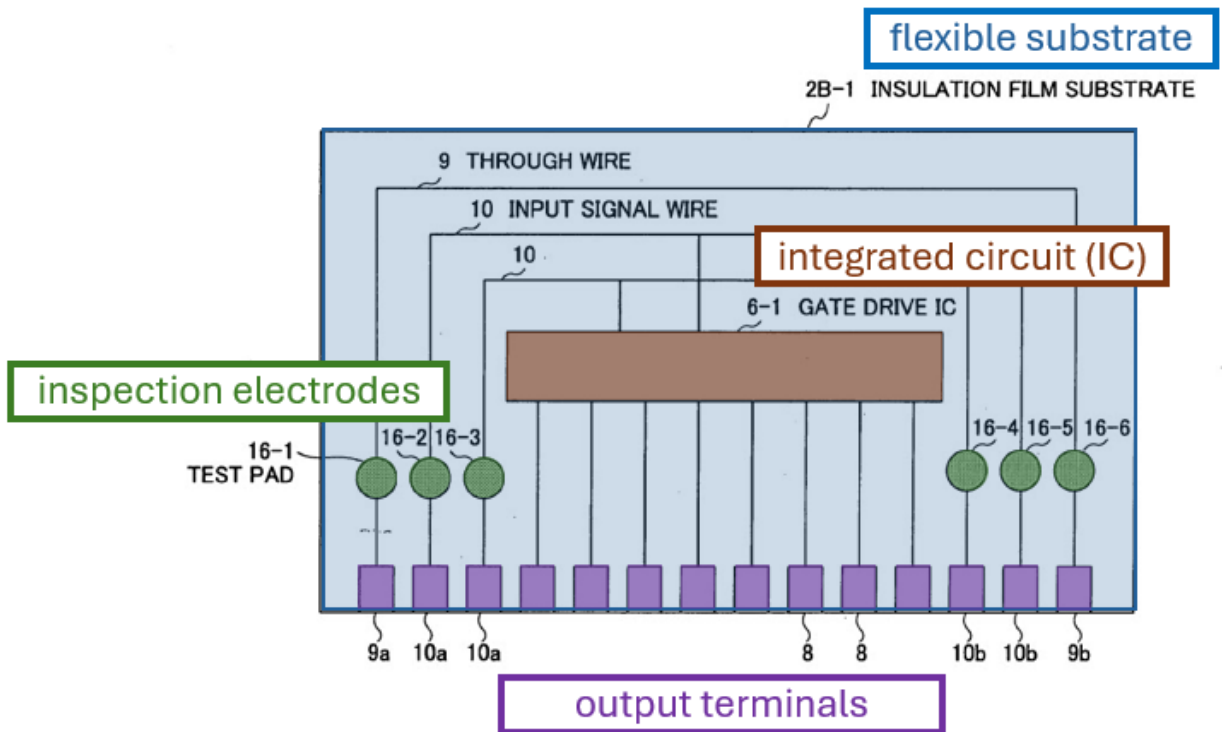
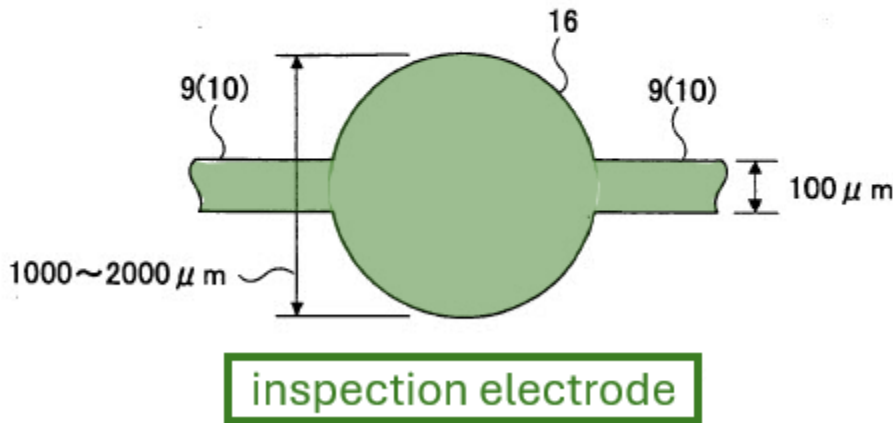


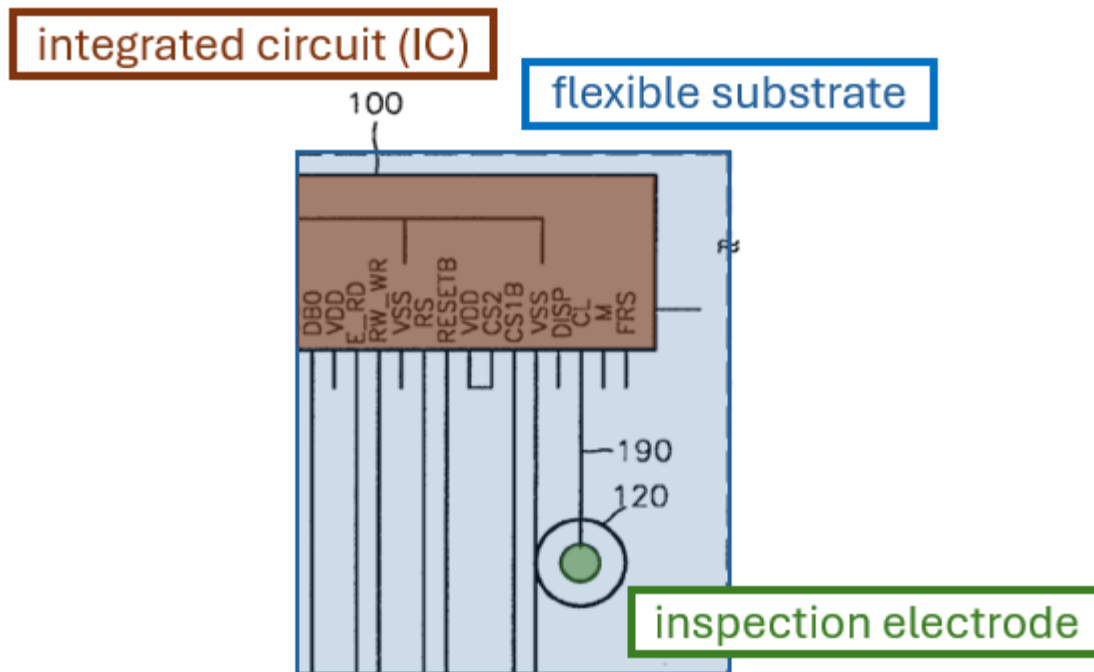
FIG.8



Taguchi also explains that test pads can be formed across different signal lines allowing detection of abnormal signal waveforms, resistance anomalies, or misalignment-related failures. (Ex.1006, ¶¶ [0022], [0065], [0066], [0068]; Ex.1002, ¶57.)

D. Kim

Kim describes “integrated circuit (IC) packages for LCDs” (Ex.1005, ¶[0005]) each “mounted on a base film” substrate (*id.*, ¶[0011]). The preferred “base film” disclosed in Kim is a particular “polyimide tape” that provides “more flexibility.” (*Id.*, ¶[0007].) Kim teaches an enlarged “test pad 120” that is “formed on a base film for the terminals requiring an electrical function test.” (*Id.*, ¶[0040].) This “test pad 120” is connected to the “LCD driver chip 100” via “patterned signal lines” on the “polyimide base film” (*id.*, ¶[0020]) as seen in Figure 1:



Kim teaches “employing a liquid crystal device (LCD) . . . in various electronic devices such as laptop computers (notebook computers), mobile phones, watches, and measuring instruments and apparatuses.” (*Id.*, [0005]-[0006]; Ex.1002, ¶61.)

VIII. GROUNDS FOR CHALLENGE

A. Ground 1: Claims 1-4, 6 and 8-11 Are Obvious Over Saito and Her

1. Motivation To Combine Saito and Her

A person of ordinary skill in the art (“POSITA”) would have been motivated to combine the teachings of Saito with those of Her to arrive at the claimed invention. (Ex.1002, ¶64.)

Saito describes a liquid crystal display device having a flexible wiring board (e.g., “film wiring board 52”) mounted with an IC (“semiconductor chip 53”) that is

tested via test pads (e.g., “test pads” 62, 63, 64, and 66) formed along signal paths on the flexible substrate. (Ex.1004, 5:23-42; Figure 3.) These pads are used to inspect the connectivity and function of signals processed by the IC. (Ex.1004, 5:43-50.) Saito’s test structure lacks a mechanism for selectively enabling or disabling the output of such signals to the test pads, which could be beneficial during certain modes of operation. (Ex.1002, ¶65.)

Her provides that mechanism. Her discloses an IC that includes a test output circuit with a channel shifter that selectively outputs signals processed in the IC only when a test mode is activated. (Ex. 1007, ¶¶ [0028]-[0034].) This switching allows inspection outputs to be selectively enabled or disabled, thereby improving control over test procedures and reducing the potential for signal conflicts or leakage during device operation or inspection. (Ex.1002, ¶66.)

Both references—Saito and Her—are directed to testing signals processed in an integrated circuit formed on a flexible substrate. Both references solve similar problems, namely, optimizing inspection and minimizing substrate area, and are thus from analogous fields. (*Compare* Ex.1004, 5:23-59 *with* Ex. 1007, ¶¶[0002]-[0006].) A POSITA would recognize that Her’s inspection-signal switching solution could be readily incorporated into Saito’s flexible wiring architecture using conventional circuit integration techniques without altering the fundamental structure of Saito’s device. (Ex.1002, ¶67.) A POSITA would have been motivated to combine Her’s

switching functionality with Saito's flexible substrate in order to improve inspection and testing efficiency. (Ex.1002, ¶68.)

Accordingly, a POSITA would have found it obvious to incorporate Her's switching functionality into the circuitry of Saito to provide selective control over signals output from the inspection electrodes. (Ex.1002, ¶68.) Doing so would have yielded predictable results using known techniques and would not have required undue experimentation. (*Id.*)

2. Independent Claim 1

1[pre] "A flexible substrate comprising:"

To the extent the preamble is limiting, it is taught by Saito. (Ex.1002, ¶¶69-73.) Saito explains that "[t]his method of face-down bonding the semiconductor chip 53 to the film wiring board 52 is generally called COF (Chip On Film)." (Ex.1004, 4:27-29.) Saito teaches that "[i]n the above embodiments, the IC module called COF is used. However, a TCP (tape carrier package) may be used instead." (Ex.1004, 6:22-24.) A POSITA would understand that both TCP and COF technologies involve the use of flexible film substrates, such as polyimide, which are widely used in semiconductor packaging for their mechanical flexibility and thin profile. (Ex.1002, ¶70.) These film wiring boards support conductive traces and are designed to flex, making them ideal for compact or foldable electronic assemblies. (Ex.1002, ¶70.)

Saito emphasizes that "the width of the film wiring board 52 can be small and the cost can be reduced. In addition, since the mounting area is small, the degree of

freedom of mounting is increased. And since the area which receives external force is reduced, reliability of interconnection can be considerably improved.” (Ex.1004, 6:28-34.) These are direct benefits that flow from using a flexible substrate. (Ex.1002, ¶72.)

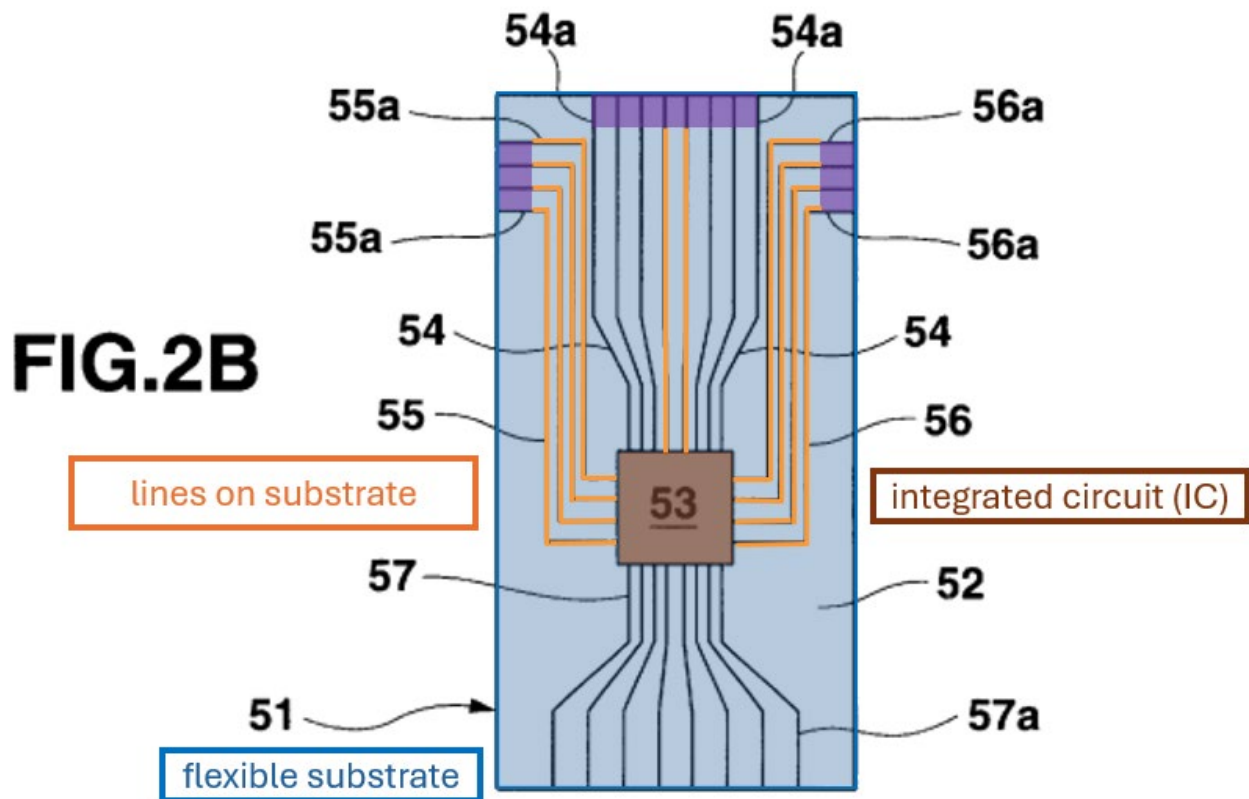
1[a] “a substrate body;”

Saito discloses “a substrate body” in the form of a film wiring board 52, which constitutes a flexible base on which the integrated circuit is mounted: “[t]he film wiring board 52 has a carrier tape having a thickness of, for example, 25 to 50 μm.” (Ex.1004, 4:17-21.) A POSITA would understand that Saito’s film wiring board constitutes a structural base that provides mechanical support and electrical interconnect functionality that corresponds to the “substrate body.” (Ex.1002, ¶¶74-75.) This is consistent with the ’512 patent itself, which illustrates and describes the substrate body as a foundational platform on which multiple components are arranged. (Ex.1001, 8:6-26; Figures 4 and 6; Ex.1002, ¶¶74-75.) As such, the ’512 patent confirms that the “substrate body” functions as a structural and electrical foundation, just as the flexible film wiring board in Saito.

1[b] “a plurality of lines that are arranged on the substrate body;”

Saito discloses “a plurality of lines that are arranged on the substrate body.” Saito describes: “[a] plurality of output lead wires 54 for the segment terminals and output lead wires 55 and 56 for the common terminals are formed in a central portion

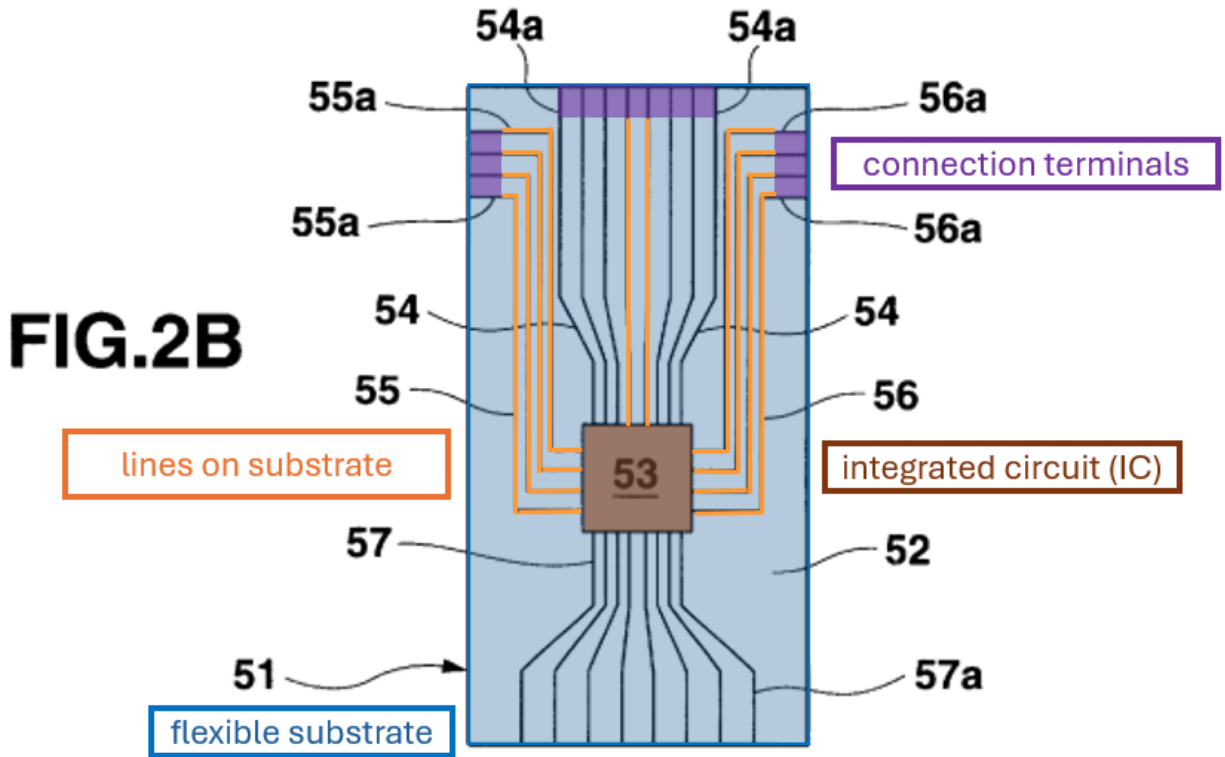
of an upper side of the upper surface of the film wiring board 52.” (Ex.1004, 4:17-21.) Saito further explains that: “the lead wires 54, 55 and 56 are directly formed on the carrier tape.” (Ex.1004, 4:32-33.) As depicted in Fig. 2B of Saito below, a series of these lead wires 54, 55 and 56 are patterned onto the film wiring board 52 and radiate outward from the chip 53 and extend toward the edge of the film wiring board 52. These lead wires provided electrical pathways between chip 53 and the terminal portions located at the periphery of the board. (Ex.1004, Figs. 2A, 2B; Ex.1002, ¶77.)



A POSITA would understand that these lead wires are electrical lines arranged on the substrate body used for transmitting signals. (Ex.1002, ¶¶76-78.) Therefore, Saito discloses limitation 1[b]. (*Id.*)

1[c] “a plurality of connection terminals that are arranged on an end portion of the substrate body and electrically connected to the respective lines;”

Saito discloses “a plurality of connection terminals that are arranged on an end portion of the substrate body and electrically connected to the respective lines.” Saito teaches: “[s]econd ends of the lead wires 54, 55 and 56, whose first ends are connected to the semiconductor chip 53, are extended to an upper side end portion of the upper surface of the film wiring board 52, and constitute output lead terminal portions 54a, 55a and 56a.” (Ex.1004, 4:37-47.) This is shown in FIG. 2B below, depicting lead wires 54, 55, and 56 extending outward from the centrally mounted semiconductor chip (53) and terminating at the edge of the film wiring board (52) in terminal portions labeled 54a, 55a, and 56a. These terminal portions (54a, 55a, 56a) are arranged on the end portion of the substrate body (52). (Ex.1004, Figs. 2A, 2B; Ex.1002, ¶80.)



Saito confirms that these output lead terminal portions 54a, 55a, 56a are **electrically connected** to the respective lines 54, 55, and 56. Saito explains that the “first ends” of the lead wires 54, 55, and 56 are bonded to the bump electrodes of the semiconductor chip 53, and that the “second ends” of those same lead wires form the output lead terminal portions 54a, 55a, and 56a. (Ex.1004, 4:24-27; 4:37-47.) A POSITA would understand that these output lead terminal portions 54a, 55a, and 56a are the end portions of continuous conductive paths (*i.e.*, the lead wires), and therefore are electrically connected to those lead wires 54, 55, and 56. These output lead terminals serve as external connection terminals that transfer signals from the

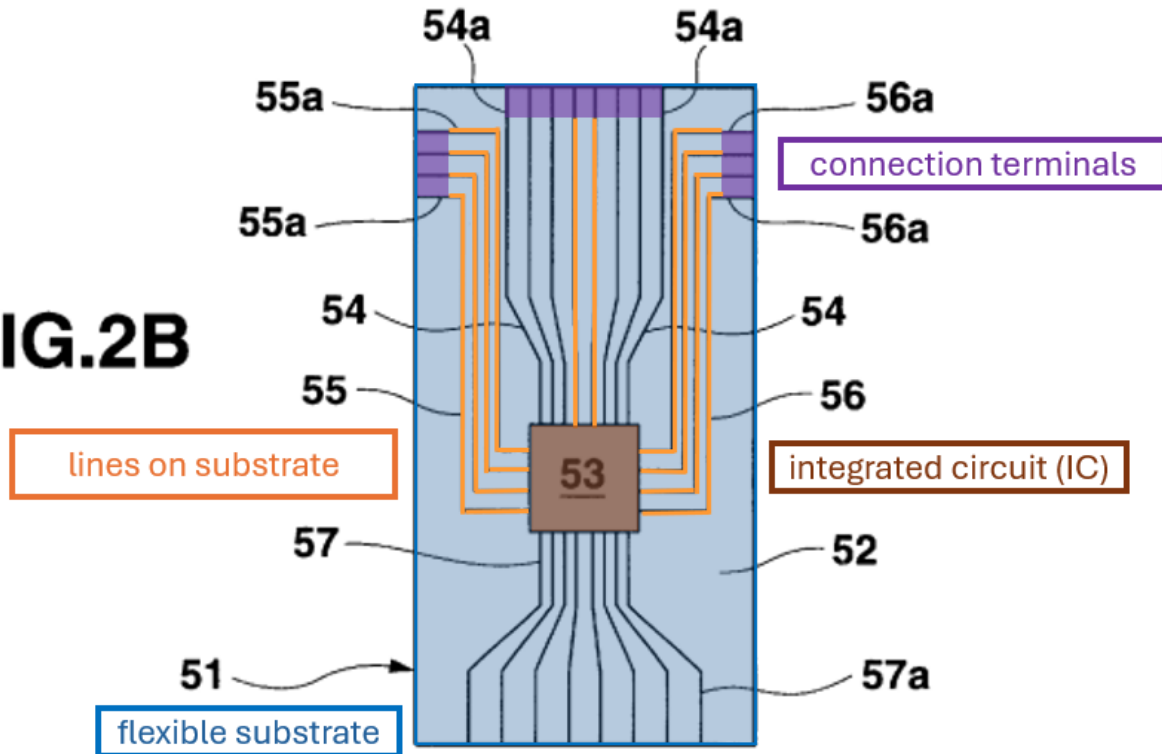
IC chip through the lead wires to external components. (Ex.1002, ¶81.) Accordingly, Saito discloses limitation 1[c]. (*Id.*, ¶79-81.)

1[d] “an integrated circuit that is arranged on the substrate body and electrically connected to at least one of the lines;”

Saito discloses “an integrated circuit that is arranged on the substrate body and electrically connected to at least one of the lines.” Saito teaches “[t]he chip 53 is mounted on a central portion of the upper surface of the film wiring board 52.” (Ex.1004, 4:15-16.) Thus, the integrated circuit (chip 53) is “arranged on” the film wiring board 52, which corresponds to the claimed “substrate body.”

Saito also discloses that this IC is **electrically connected** to lines formed on the substrate body. “Bump electrodes (not shown) of the semiconductor chip, made of gold, are respectively bonded to first ends of the lead wires 54, 55 and 56.” (Ex.1004, 4:24-27.) Lead wires 54, 55, and 56 are formed directly on the upper surface of the substrate 52 and serve as conductive paths from the chip to external terminals. (*Id.*; Ex.1002, ¶83.) This structure is illustrated in FIG. 2B of Saito:

- Semiconductor chip 53 mounted centrally on the substrate (film wiring board 52); and
 - Lead wires 54, 55, and 56 radiating outward from the edges of chip 53.
- (Ex.1004, Fig. 2B; Ex.1002, ¶84.)



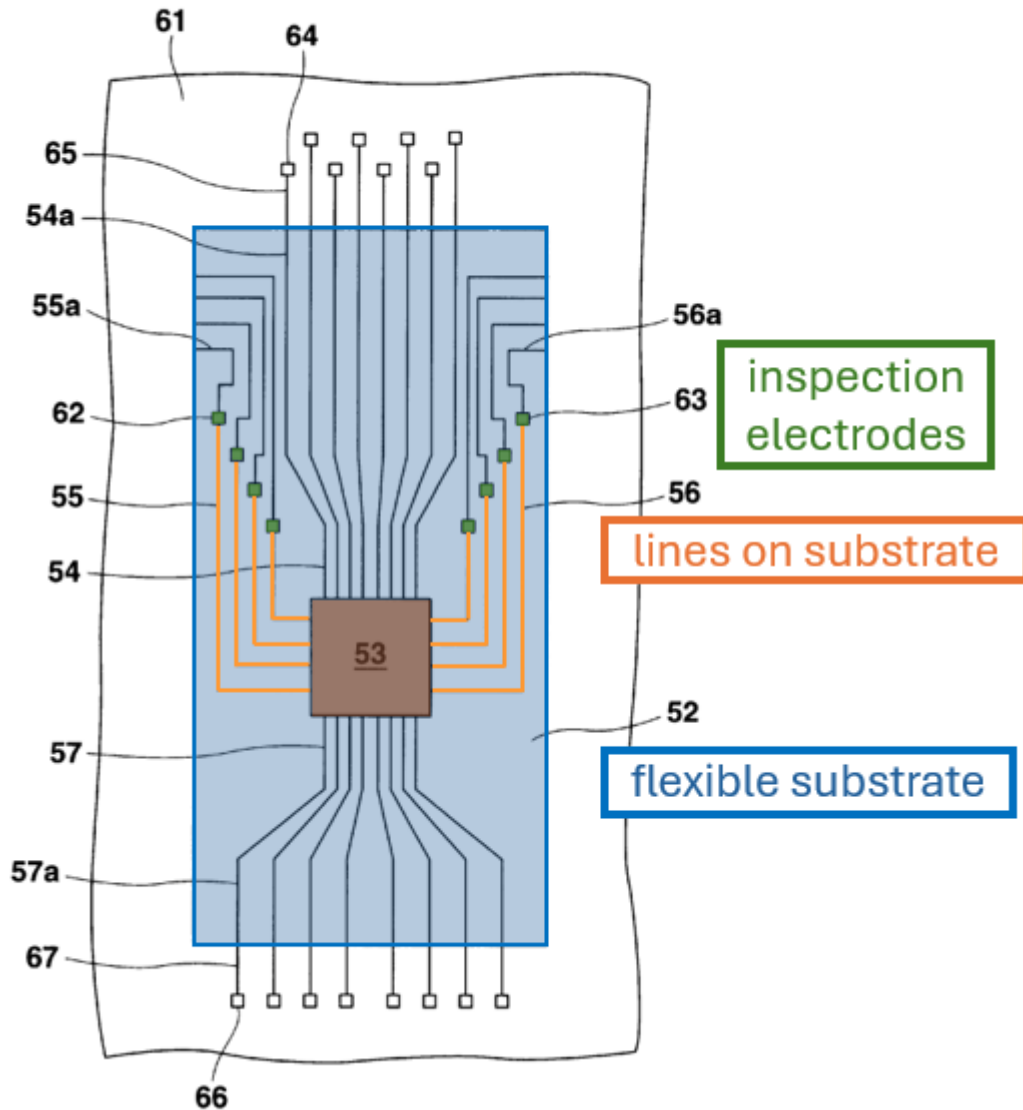
Accordingly, Saito discloses an integrated circuit (chip 53) that is (1) arranged on the substrate body (film wiring board 52), and (2) electrically connected to lead wires 54, 55, and 56 formed on that substrate. These lead wires constitute the claimed

“lines.” (Ex.1002, ¶86.) Therefore, Saito discloses limitation 1[d]. (Ex.1002, ¶¶82-86.)

1[e] “an inspection electrode that is arranged on the substrate body and electrically connected to the integrated circuit and capable of outputting a signal processed in the integrated circuit; and”

Saito discloses the “inspection electrode...” of element 1[e]. First, Saito expressly teaches that “[t]est pads 62 and 63 are formed in middle portions of output lead wires 55 and 56 on the upper surface of the film wiring board 52.” (Ex.1004, 5:31-33.) A POSITA would understand these “test pads” correspond to the claimed “inspection electrodes” and provide external access to signals associated with the IC chip for testing and diagnostic purposes. (Ex.1002, ¶¶87-88.) It is well known that “test pads” serve as inspection points electrically connected to internal circuitry and are functionally interchangeable with what claim 1 of the ’512 patent refers to as “inspection electrodes.” (*Id.*, ¶88.) Accordingly, a POSITA would equate these test pads with the claimed inspection electrodes. (*Id.*) Saito’s FIG. 3 visually confirms this arrangement, showing test pads (62, 63) physically located on the surface of the substrate. (Ex.1004, Fig. 3; Ex.1002, ¶88.)

FIG.3



Therefore, Saito discloses inspection electrodes (“test pads 62 and 63”) that are formed directly on the substrate body, satisfying the first part of limitation 1[e].

Second, Saito further explains that “bump electrodes (not shown) of the semiconductor chip [53] are respectively bonded to first ends of the lead wires 54, 55, and 56.” (Ex.1004, 4:24–27.) The test pads 62 and 63 are formed in the middle

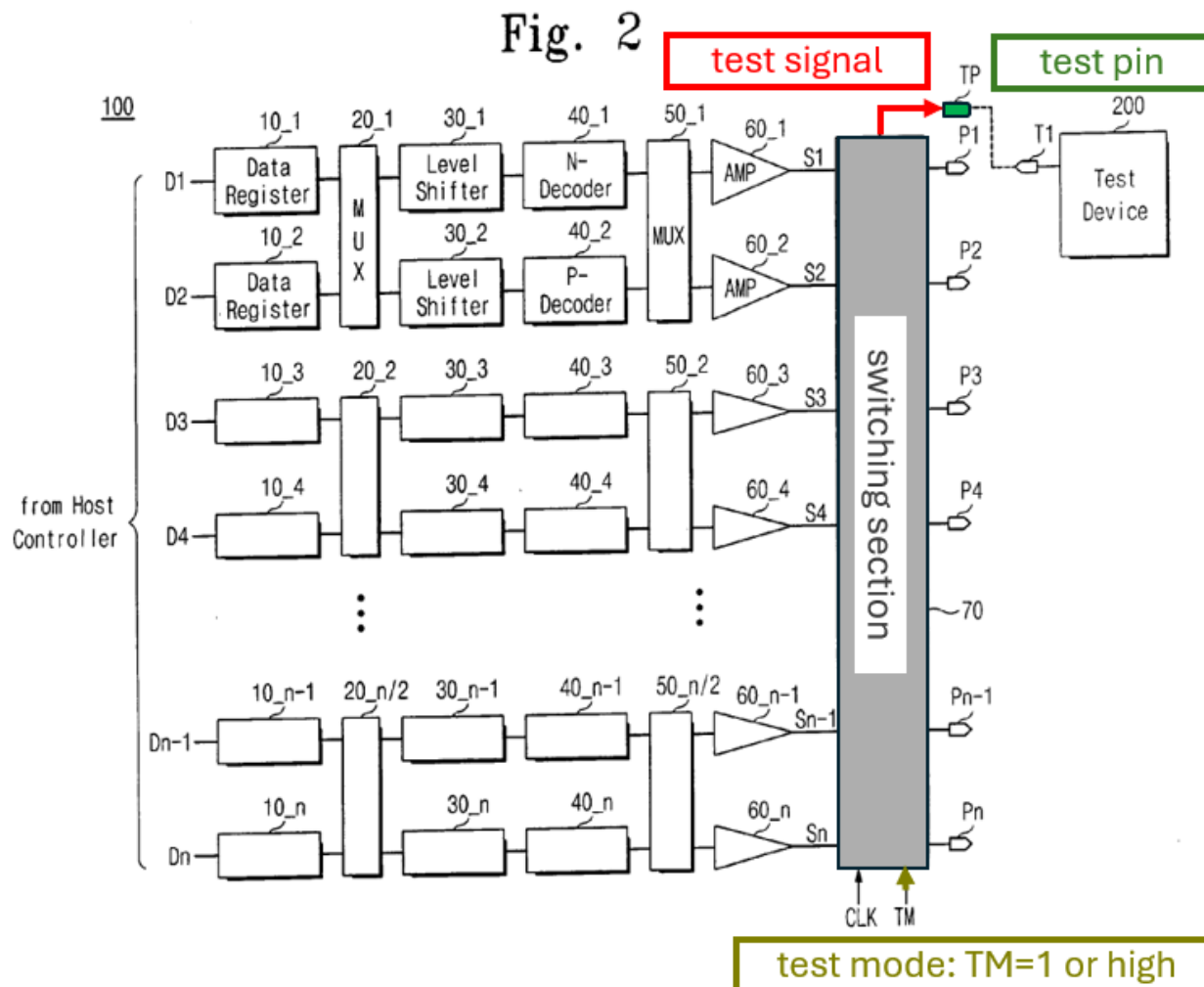
portions of lead wires 55 and 56, which are the same wires connected to the IC. (Ex.1004, 5:31–33.) Accordingly, a POSITA would understand that the test pads are electrically connected to the IC (semiconductor chip 53) via these continuous conductive paths (lead wires 55, 56). (Ex.1002, ¶¶89-91.) This connection is visually confirmed in Figure 3 of Saito, which depicts the test pads 62 and 63 positioned along the continuous conductive traces (output lead wires 55 and 56) that extend from the semiconductor chip 53 to the output lead terminals. This figure shows that the test pads are disposed between the chip and the output lead terminals, affirming that they are part of the same electrical network directly linked to the integrated circuit. This is further supported by standard industry practice, in which intermediate contact points along signal paths (like test pads) are commonly used for probing signals from an IC. (Ex.1002, ¶¶89-92.) Because the signal present at the test pad must have come from the IC through the connected lead wire, a POSITA would understand that the test pad is inherently and electrically connected to the IC. (Ex.1002, ¶¶89-90.) Therefore, Saito discloses the second part of limitation 1[e].

Third, Saito teaches that these test pads are used to verify connectivity between the lead wires and the IC chip: “Test pins (not shown) are brought into contact with the test pads 62, 63, 64 and 66, to inspect whether the semiconductor chip 53 is satisfactorily connected to lead wires 54, 55, 56 and 57.” (Ex.1004, 5:43–46.) To perform such inspection, signals processed or relayed through the IC chip

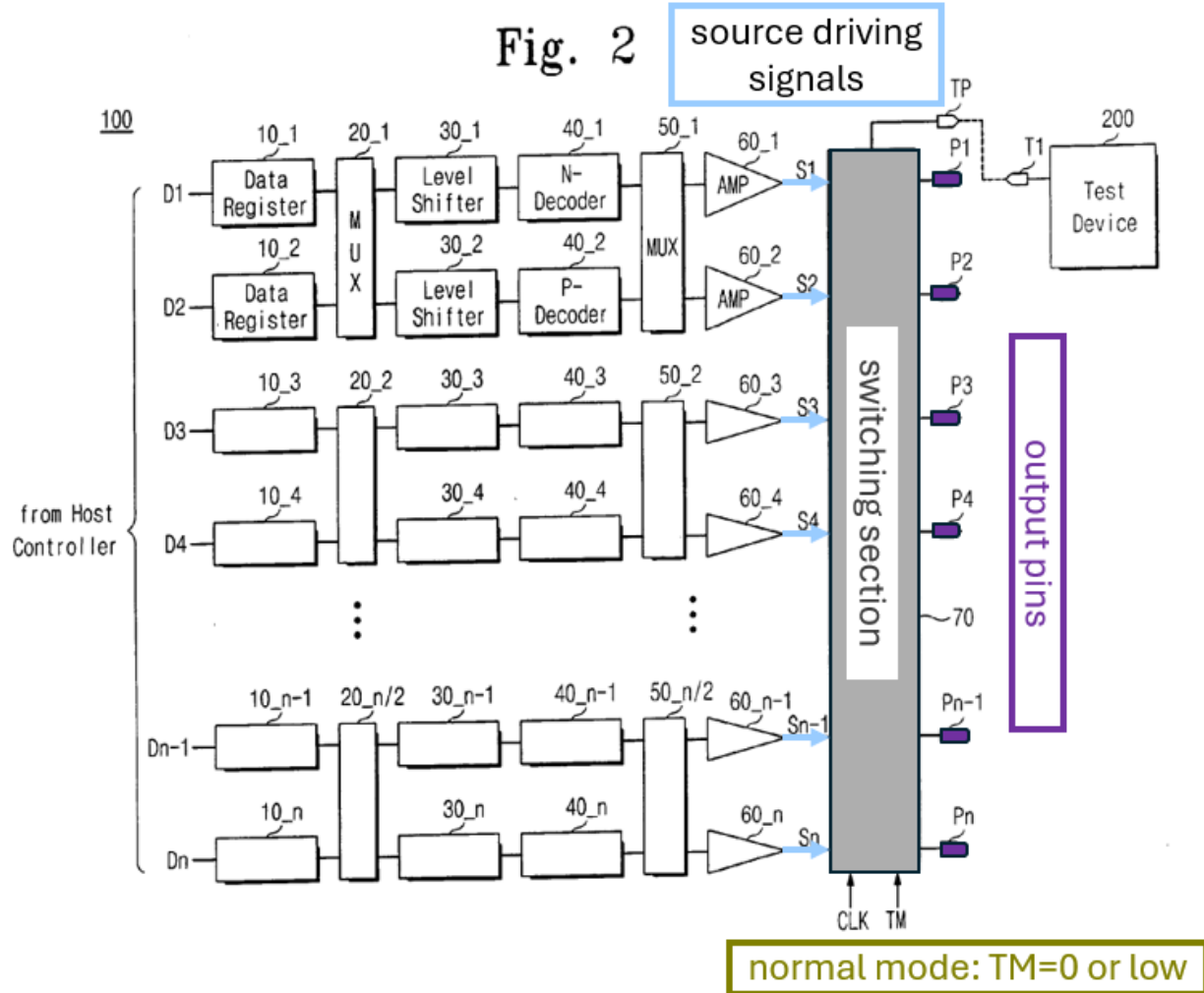
must reach the test pads and be output from the chip via the lead wires. (Ex.1002, ¶¶91-92.) A POSITA would understand that for these signals to be tested externally, the test pads must be capable of outputting signals originating from the IC. (*Id.*) This is consistent with standard industry practice, where test pads connected to IC outputs are probed during electrical testing to verify chip operation and signal integrity. (*Id.*) Thus, Saito's test pads (62, 63) are used for outputting signals processed or driven by the IC, and therefore disclose the third part of limitation 1[e]. (*Id.*, ¶¶87-93.)

1[f] “a switching section that switches an operation of the inspection electrode on/off to cause the inspection electrode to output or not to output the signal processed in the integrated circuit.”

Although Saito does not disclose the “switching section...” recited in 1[f], Her does. Her discloses a “channel shifter 70” (see Fig. 2) that determines whether the test pin (TP) is active (*i.e.*, “on”) or inactive (“off”) based on the test mode signal TM. In the test mode (TM=high), Her states that “the channel shifter 70 sequentially outputs the source driving signals S1~Sn outputted from the amplifier 60_1~60_n in response to a clock signal CLK” to the test pin TP. (Ex.1007, ¶¶[0030]-[0032].)



In the normal mode (TM=low), Her states that “the channel shifter 70 outputs the source driving signals S1~Sn outputted from the amplifiers 60₁~60_n to the output pins P1~Pn.” (*Id.*)



In other words, Her's switching section is controlled by a test mode signal TM, which acts as a binary control input to the channel shifter. When TM is low, the test pin is switched "off" and the IC operates in normal mode where the output signals are delivered to the regular output pins P1–Pn. When TM is high (*i.e.*, logic "1") indicating test mode, the test pin is "on" and the channel shifter 70 switches the routing path, sequentially outputting a newly created composite signal consisting of the processed signals to the test pin (TP). (Ex.1007, ¶¶[0029]–[0032]; Figs. 2-3.)

Fig. 3

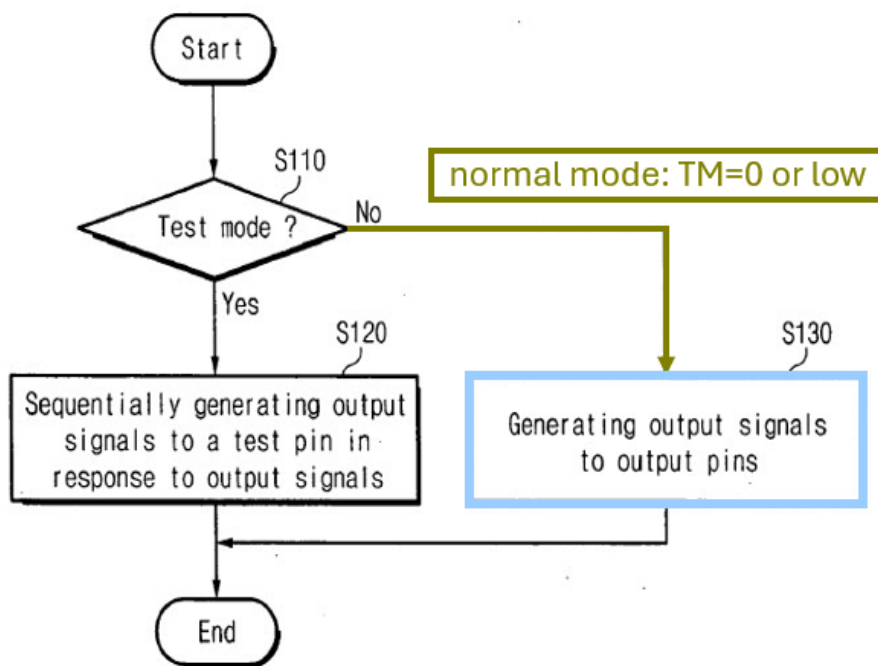
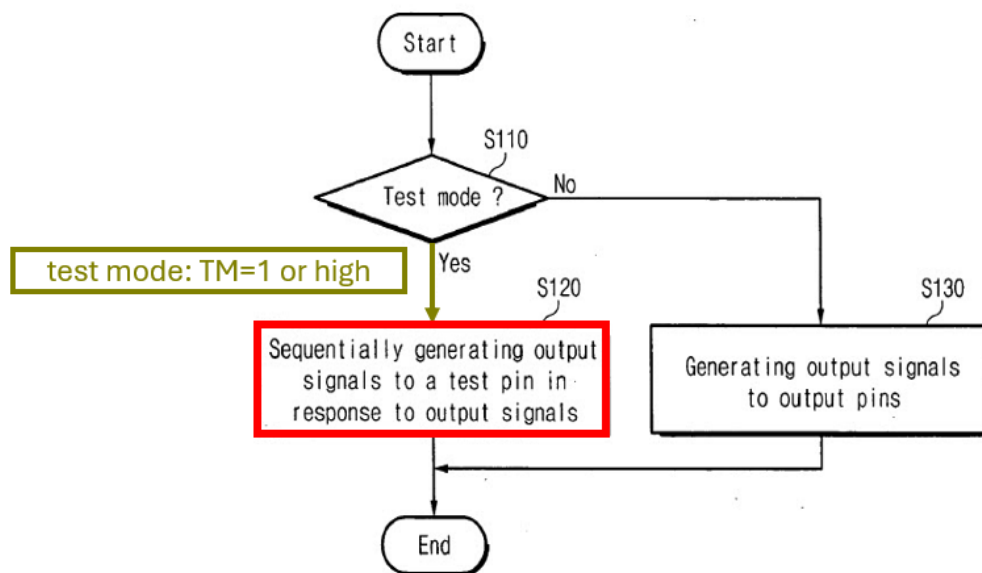
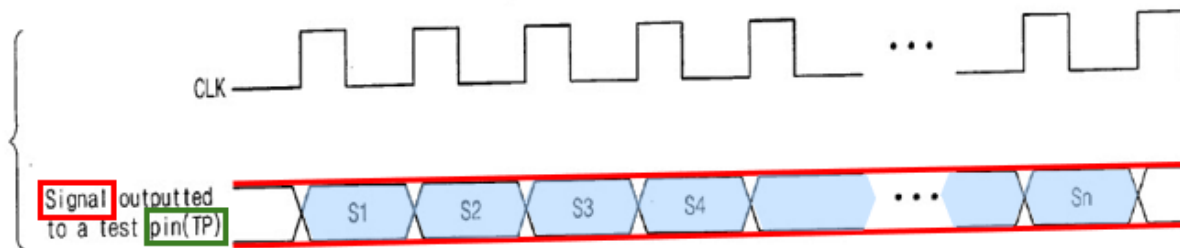


Fig. 3



This switching mechanism is further illustrated in FIG. 4, a timing diagram that shows the test pin TP receiving a composite signal consisting of the signals S1–Sn sent in sequence at successive rising edges of the clock signal. (Ex. 1007, Fig. 4; [0033].)

Fig. 4



It would be obvious to a POSITA to connect a patterned wire with a test electrode as taught in Saito to a “test pin TP” as taught in Her for easier reading of the composite test signal by an external test probe. When so connected, the switching mechanism of “channel shifter 70” turns the inspection electrode on the substrate on/off in response to whether the test mode signal TM indicates the “test mode” (i.e., “high level,” or “1”) or the “normal mode” (i.e., “low level,” or “0”). (Ex.1002, ¶¶94-97, 189.)

In addition, a POSITA would understand that a test pad that is always “on” could introduce several drawbacks. For instance, such a test electrode that

continually outputs a test signal may add unwanted parasitic capacitance or act as an antenna, potentially degrading signal integrity or increasing susceptibility to noise on proximate lines. Moreover, a test pad that is always active may draw unnecessary current or interact with other circuitry, impacting power efficiency. (Ex.1002, ¶¶98-99.) Thus, a POSITA would be motivated to add the on/off switching mechanism taught in Her to selectively enable or disable the connection between the test pad and the driver IC, and would have a reasonable expectation of success in doing so, to help eliminate parasitic effects, prevent unintended signal coupling or leakage, and conserve power. (*Id.*) Further, a POSITA would know that by isolating the test pad when it is not needed, the risk of electro-static discharge, current leakage, or other negative environmental factors affecting the IC also is minimized. (*Id.*)

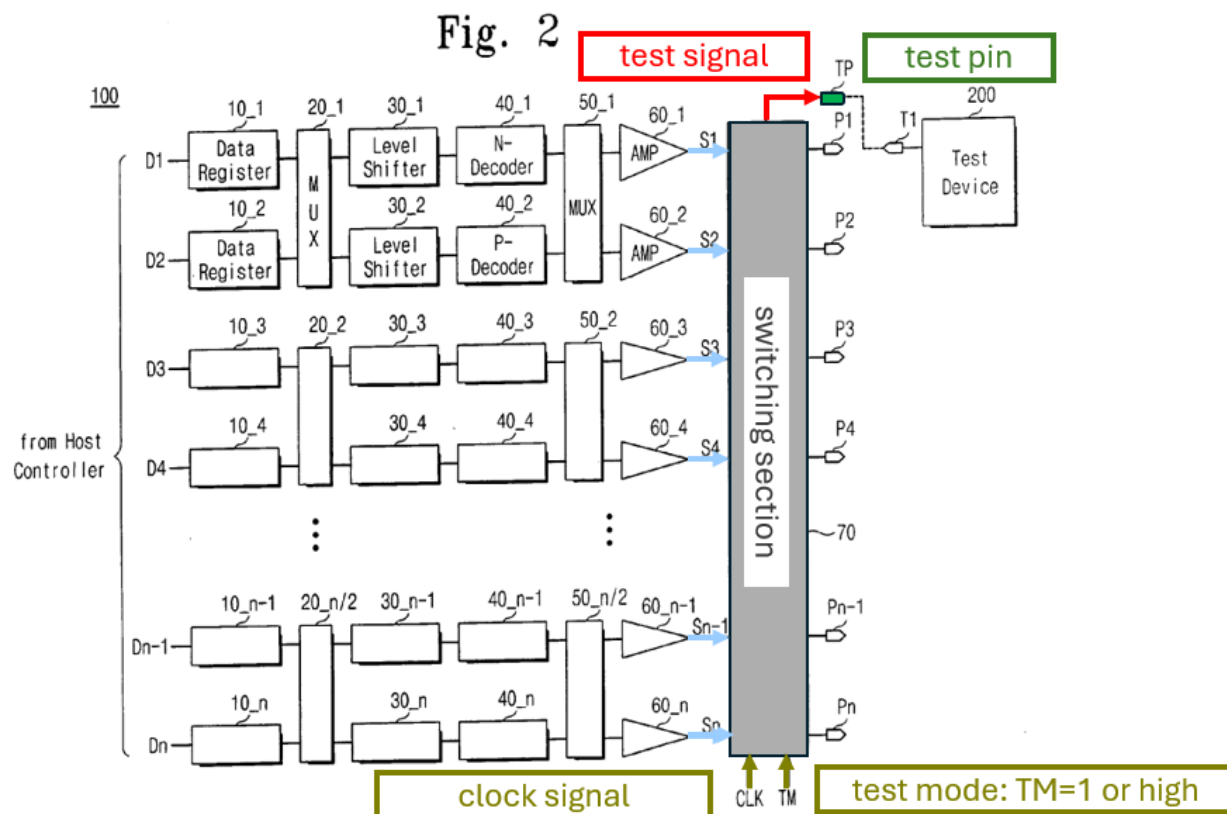
In sum, the combination of Saito and Her renders independent claim 1 of the '512 patent obvious. (Ex.1002, ¶¶69-99.)

3. Dependent Claim 2

The flexible substrate according to claim 1, wherein the inspection electrode outputs a signal that is not input to or output from the integrated circuit through the plurality of connection terminals.

As discussed above, the combination of Saito and Her renders claim 1 obvious. The combination of Saito and Her also discloses the additional limitation of claim 2. Her discloses a “channel shifter” that, when in “test mode,” combines the incoming “source driving signals S1~Sn” into a new “signal outputted to a test

pin TP.” (Ex.1007, ¶[0033]; Figures 2-4.) This new composite “signal” is created internally by the driver IC and is only monitored directly on the substrate by an external “test device 200” and not output to the LCD panel. (Ex.1007, ¶[0032-34]; Figures 2-4).



The signal is not intended to drive the LCD panel and, during test mode, is not routed through the normal source output terminals (*i.e.*, the “connection terminals” in claim 2) that connect the IC to the LCD panel. (Ex.1002, ¶102.) Instead, the channel shifter directs the signal exclusively to the test pin TP, bypassing the panel-driving connection terminals entirely. (*Id.*) Thus, as described in claim 2, Her’s composite test signal is neither input nor output “from the integrated circuit

through the plurality of connection terminals.” (*Id.*) Therefore, the combination of Her’s test signal with Saito’s test electrode arrangement also renders claim 2 obvious. (Ex.1002, ¶¶100-103.)

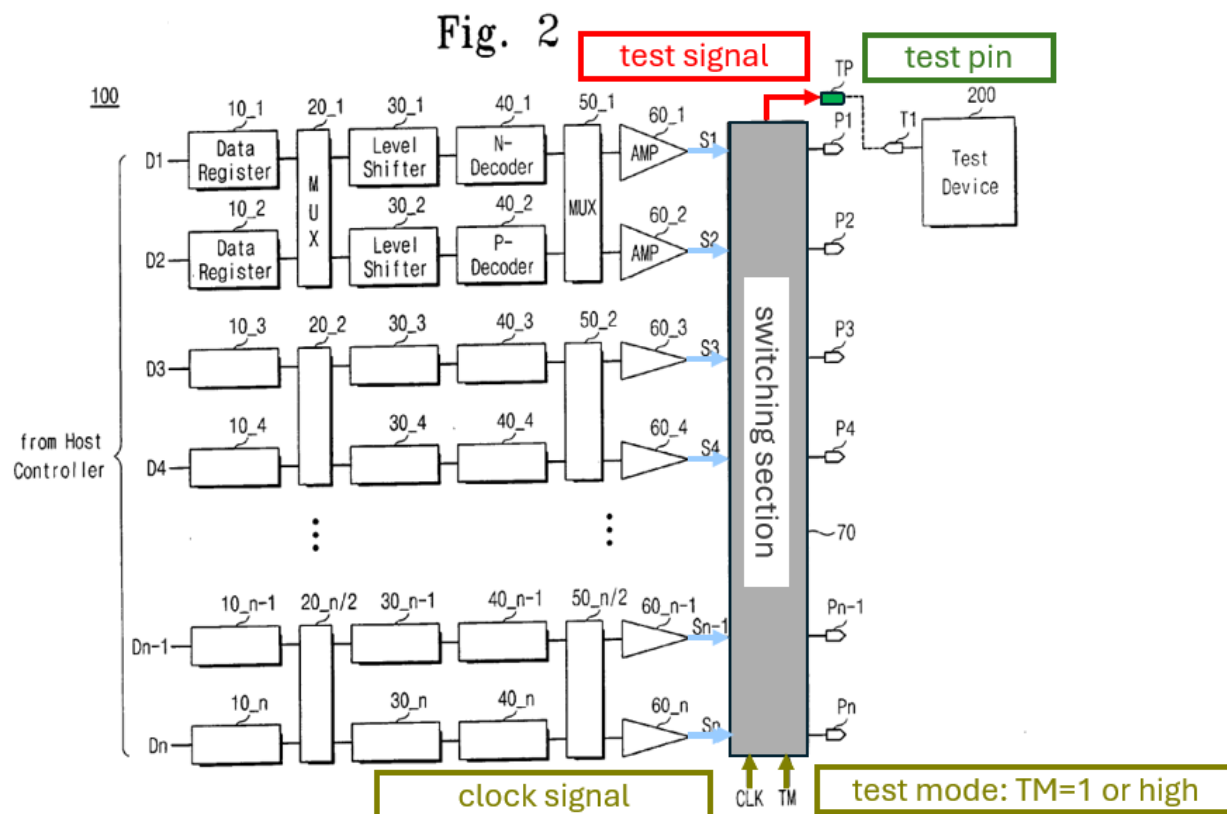
4. Dependent Claim 3

The flexible substrate according to claim 1, wherein the switching section that switches the types of signals that are to be output from the inspection electrode.

As discussed previously, the combination of Saito and Her renders claim 1 obvious. The “switching section” of the channel shifter IC disclosed in Her also “switches the types of signals that are to be output from the inspection electrode.” As explained in the ’512 patent, using a switching section results in “signals of different types can be output from the inspection electrode even when the number of inspection electrodes . . . is only one. Thus, many signals can be inspected regardless of the number of inspection electrodes.” (Ex.1001, 3:13-19.)

Her teaches (per Figure 4) that, when the test signal TM puts the “channel shifter” into the “test mode” and thereby switches on the operation of the test pin TP, “the channel shifter 70 outputs, at a first rising edge of the clock signal CLK, the **source driving signal S1** . . . to the test pin TP,” “[a]t a second rising edge of the clock signal CLK, the channel shifter 70 outputs the **source driving signal S2** outputted . . . to the test pin TP,” and so forth for all the signal types S1 through Sn. (Ex.1007, ¶ [0033]; *also id.* (“In this manner, the channel shifter 70 sequentially outputs the source d[r]iving signals S[3]~Sn . . . to the test pin TP in response to

from third to nth rising edges of the clock signal CLK”).) By so doing, the “channel shifter 70” of Her switches the types of signals that are to be output from the inspection electrode (as required by claim 3) at each successive rising edge of the input clock signal CLK. (Ex.1002, ¶¶104-105, 197.)



A POSITA would understand that each of these source driving signals—S1 through Sn—originates from a different amplifier (60_1 through 60_n) and corresponds to a different output channel. (Ex.1007, ¶[0028]; Ex.1002, ¶106.) Thus, the channel shifter is not simply outputting multiple values of the same signal, but rather **dynamically switching between different types of signals**, each representing a distinct output channel. (Ex.1002, ¶¶106, 197.) Accordingly, a

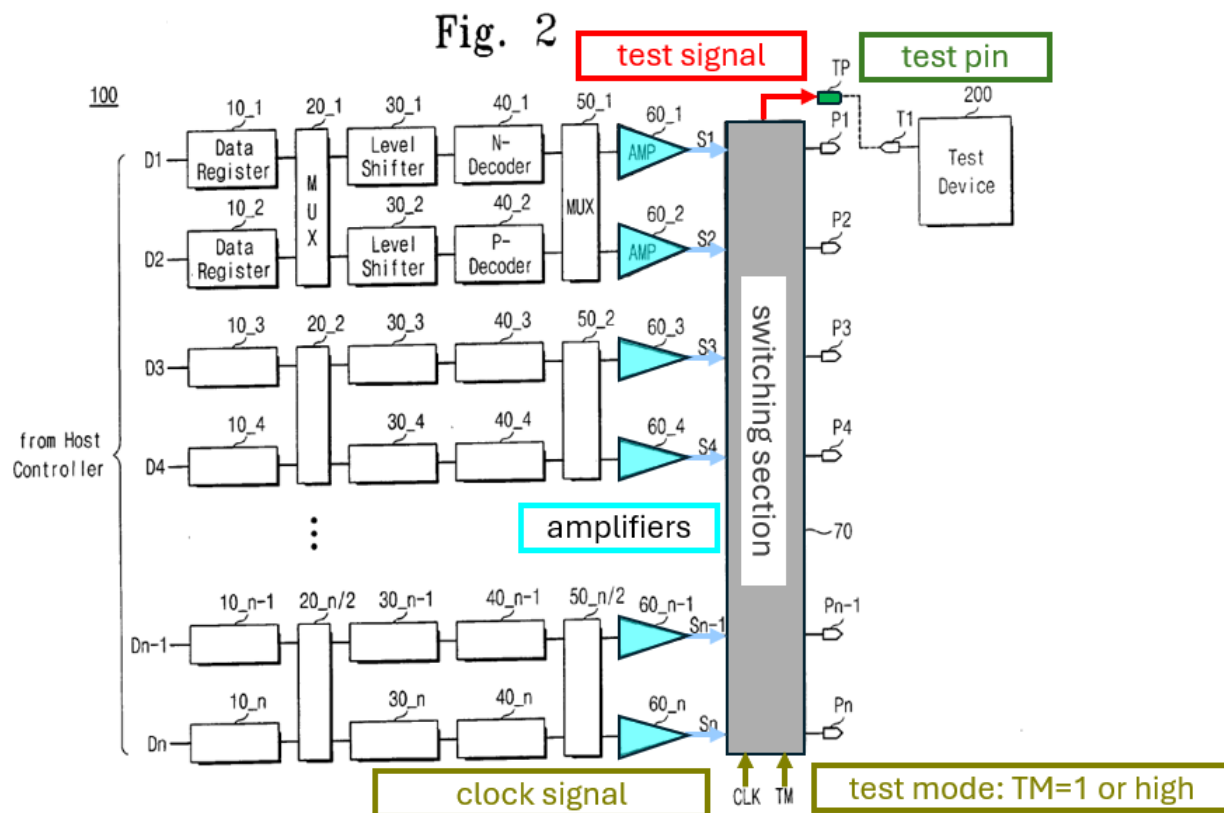
POSITA would understand that Her discloses a switching section (*i.e.*, the channel shifter 70) that “switches the types of signals that are to be output from the inspection electrode” as recited in claim 3. (*Id.*)

Therefore, claim 3 is rendered obvious by the combination Saito and Her. (*Id.*, ¶¶104-107.)

5. Dependent Claim 4

The flexible substrate according to claim 1 further comprising: an amplifier that amplifies a signal that is to be output to the inspection electrode.

As discussed previously, the combination of Her and Saito renders claim 1 obvious. Her also discloses the additional “an amplifier...” limitation of dependent claim 4. Her expressly discloses the use of **amplifiers (60_1 through 60_n)** in the signal path between the data processing circuitry and the output stages, including the inspection electrode (via the test pin TP). As depicted in Figure 2 of Her below, Her teaches that, when in test mode, the “source driving signals S_1~Sn **outputted from the amplifiers 60_1~60_n** are sequentially outputted to a test pin TP at each rising edge of a clock signal” (Ex.1007, ¶[0033]; Ex.1002, ¶108):



A POSITA would understand that the fundamental purpose of the amplifiers shown in Her, as suggested by the name “amplifier” itself, is to *amplify* an incoming signal and make the signal more reliable for later detection. (Ex.1002, ¶109.) The multiple amplifiers taught in Her each serves to amplify a constituent signal sent to the “channel shifter” in Her, and thereby amplifies the composite test signal sent by the channel shifter to the “test pin” (and ultimately sent to the test electrode taught in Saito). (Ex.1002, ¶110.) Therefore, claim 4 is rendered obvious by the combination of Saito and Her. (Ex.1002, ¶¶108-111.)

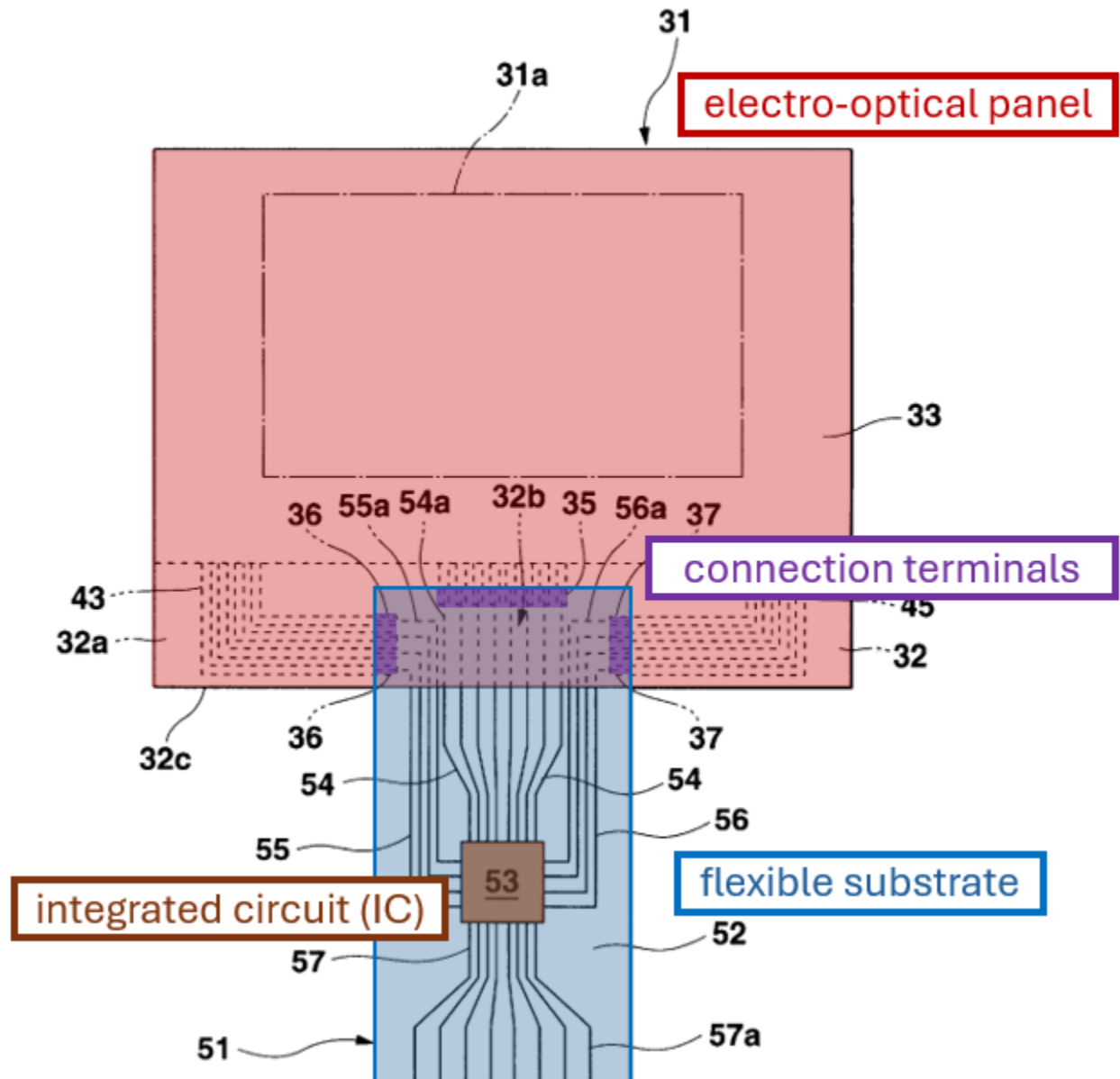
6. Dependent Claim 6

An electro-optical device comprising: the flexible substrate according to any of claims 1, 2, or 3-5 and; an electro-optical panel that is electrically connected to the flexible substrate through the connection terminals.

As discussed previously, the combination of Saito and Her renders claims 1-4 obvious. Saito also discloses an “electro-optical device comprising . . . an electro-optical panel that is electrically connected to the flexible substrate through the connection terminals.”

Saito is directed to a “liquid crystal display device” that includes a “panel connected to an IC chip mounted on a narrow film wiring board.” (Ex.1004, 1:13–15.) This is shown in Saito’s Fig. 1, which shows the overall configuration of the LCD device. (Ex.1004, Fig. 1; Ex.1002, ¶112.)

FIG.1



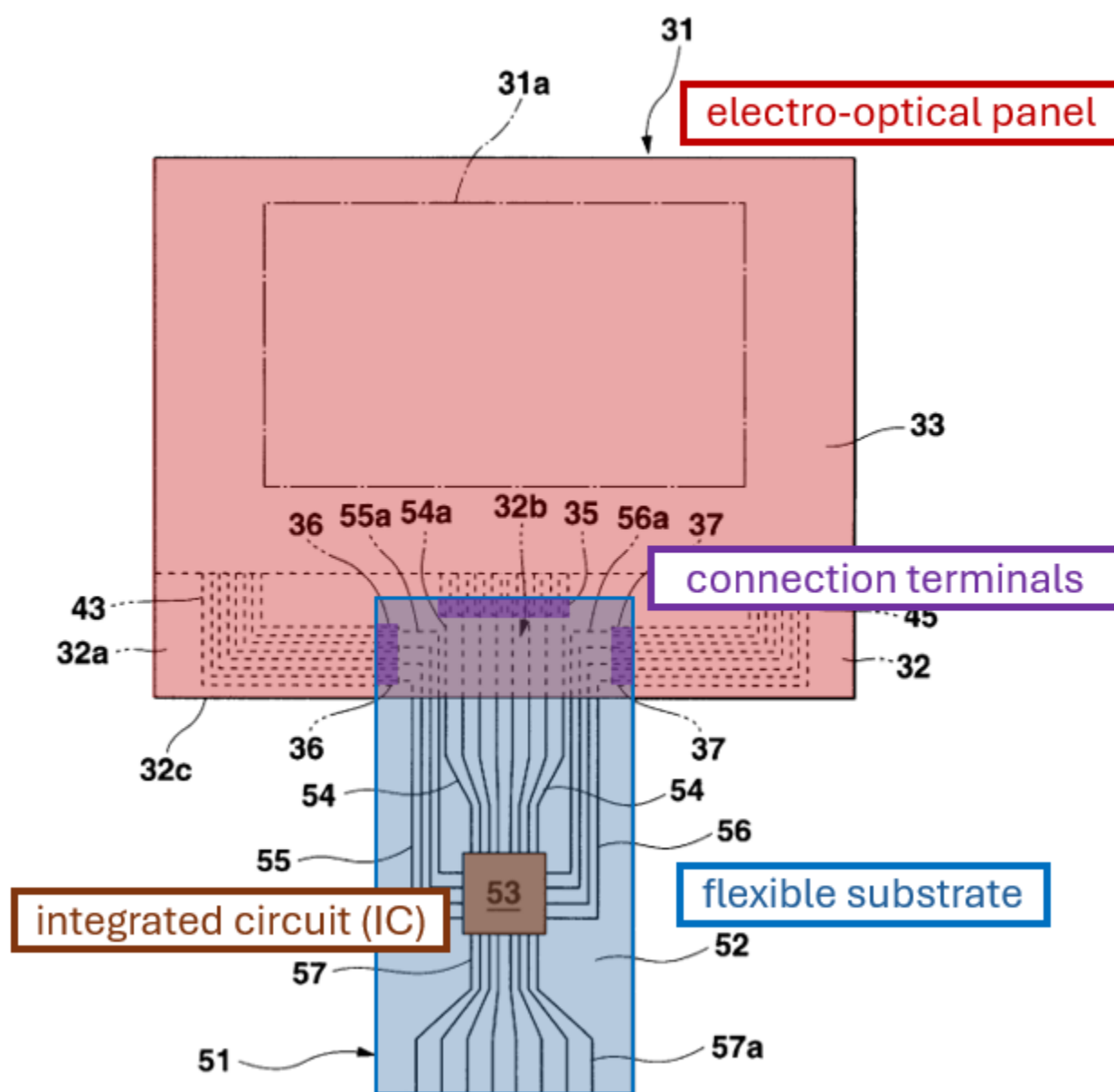
A POSITA would understand Saito's LCD device to be a well-known type of "electro-optical device," as it electrically controls the optical characteristics of a liquid crystal panel. (Ex.1002, ¶¶113-115.) Saito describes a **liquid crystal display panel 31** that includes a segment substrate 32 and common substrate 33 sealed

together to define a display region, with multiple segment terminals 35 and common terminals 36, 37 formed on the segment substrate 32. (Ex.1004, Fig. 1; 3:60–67.) In the display technology field, the term “electro-optical panel” is commonly understood to include LCD panels, which use electrical signals to control light and produce images. (Ex.1002, ¶¶113-115.) Accordingly, a POSITA would recognize Saito’s LCD panel as an electro-optical panel within the meaning of claim 6. (*Id.*)

Saito also discloses that this liquid crystal display panel 31 is **electrically connected to a film wiring board 52** (*i.e.*, a flexible substrate), through output lead terminal portions 54a, 55a, and 56a formed on the edge of the film wiring board. (Ex.1002, ¶116.) These output lead terminals are joined to the segment terminals 35 and the common terminals 36 and 37 of the liquid crystal display panel using anisotropic conductive adhesive. (Ex.1004, 4:58–63.) This adhesive provides electrical conductivity, enabling electrical signals from the semiconductor chip 53—transmitted along the lead wires 54, 55, and 56—to flow through the output lead terminal portions into the segment and common terminals of the display panel. (Ex.1002, ¶116.) Thus, this structure creates an electrical pathway from the IC chip, through the lead wires and terminal portions on the flexible substrate, and into the electrodes of the display panel, enabling the IC to drive the display panel. (Ex.1002, ¶117.)

This physical and electrical connection between the display panel and the flexible substrate is confirmed in FIG. 1, which depicts the film wiring board 52 joined to the lower portion of the liquid crystal display panel 31. (Ex.1004, Fig. 1; Ex.1002, ¶118.)

FIG.1



Thus, a POSITA would understand that Saito discloses an **electro-optical panel** (i.e., the liquid crystal display panel 31) that is **electrically connected to a flexible substrate** (i.e., the film wiring board 52) **through the connection terminals** (i.e., the output lead terminal portions 54a, 55a, 56a), and thus constitutes the “electro-optical device” recited in claim 6, rendering claim 6 obvious. (Ex.1002, ¶¶112-119.)

7. Independent Claim 8

8[pre] “*A flexible substrate comprising:*”

See Claim 1[pre], supra.

8[a] “*a substrate body;*”

See Claim 1[a], supra.

8[b] “*a plurality of lines that are arranged on the substrate body;*”

See Claim 1[b], supra.

8[c] “*a plurality of connection terminals that are arranged on an end portion of the substrate body and electrically connected to the respective lines;*”

See Claim 1[c], supra.

8[d] “*an integrated circuit that is arranged on the substrate body and electrically connected to at least one of the lines;*”

See Claim 1[d], supra.

8[e] “*an inspection electrode that is arranged on the substrate body and electrically connected to the integrated*

circuit and capable of outputting a signal processed in the integrated circuit; and”

See Claim 1[e], supra.

8[f] “a switching section that switches the types of signals that are to be output from the inspection electrode.”

See Claim 3[a], supra.

Therefore, Saito and Her render claim 8 obvious (Ex.1002, ¶¶120-127.)

8. Independent Claim 9

9[pre] “A flexible substrate comprising:”

See Claim 1[pre], supra.

9[a] “a substrate body;”

See Claim 1[a], supra.

9[b] “a plurality of wirings that are arranged on the substrate body;”

See Claim 1[b], supra. Saito discloses that “[l]ead wires 24, 25 and 26 are formed on the upper surface of the film wiring board 22” (Ex.1004, 1:63–64), and that “[t]he lead wires 54, 55 and 56... are formed by, for example, depositing copper directly on the carrier tape and plating the copper with tin” (Ex.1004, 4:21–24). These “lead wires” are conductive paths arranged on the surface of the flexible substrate and function as electrical interconnects. (Ex.1002, ¶130.) A POSITA would understand that the term “wirings” in claim 9 refers to such conductive paths—also commonly referred to as “lines” or “traces”—that are arranged on a

substrate body to route electrical signals. (*Id.*) Accordingly, Saito discloses “a plurality of wirings that are arranged on the substrate body.” (*Id.*)

9[c] “a plurality of connection terminals that electrically connects a device and at least one of the plurality of wirings;”

See Claim 1[c], *supra*. Again, a POSITA would also understand that the terms “wirings” and “lines” are interchangeable in this context and as used in the ’512 patent, and both represent electrical interconnects patterned on the claimed “substrate body.” (Ex.1002, ¶¶81, 131.)

9[d] “an inspection electrode that is arranged on the substrate body, the inspection electrode electrically connecting to an integrated circuit, the inspection electrode being capable of outputting a signal processed by the integrated circuit; and”

See Claim 1[e], *supra*.

9[e] “a switching section that switches types of signals, are to be outputted from the inspection electrode,”

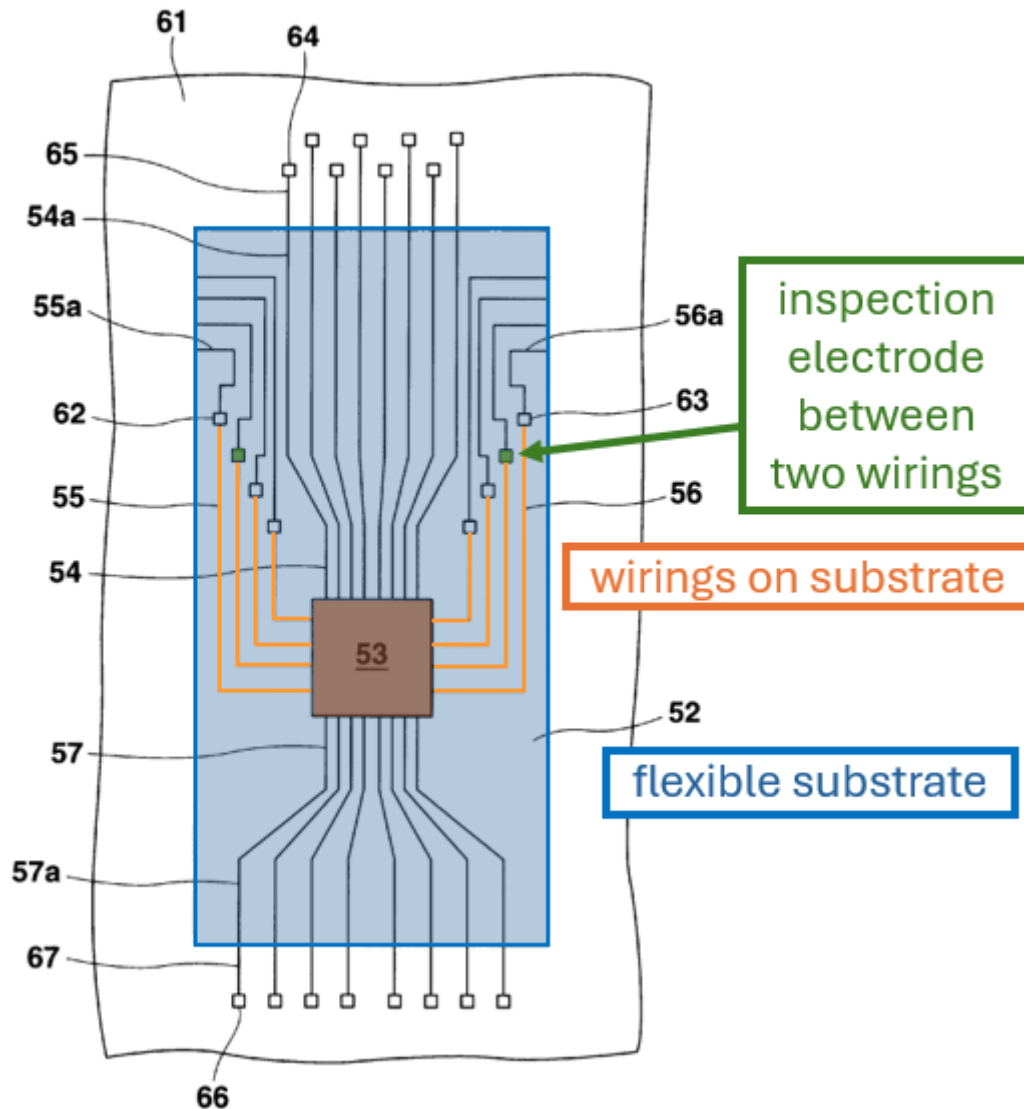
See Claim 3[a], *supra*.

9[f] “the inspection electrode being disposed between one of the plurality of wirings and another one of the plurality of wirings, wherein the integrated circuit is electrically connected to at least one of the plurality of wirings.”

Saito discloses “the inspection electrode being disposed between one of the plurality of wirings and another one of the plurality of wirings” limitation of element 9[f]. A POSITA would understand from FIG. 3 below that the test pads (shown in

green) are each interposed between adjacent wirings (shown in orange). (Ex.1002, ¶134.)

FIG.3



It is well known in the field of flexible printed circuits and display technology that test pads are commonly arranged between pairs of signal lines or wirings. (Ex.1002, ¶134.) This placement helps make the circuit layout simpler, saves space, and makes it easier to test individual signals during inspection, especially when

many wires are packed closely together. (*Id.*) By placing a test pad between two adjacent wires, each wire can be independently tested without causing interference or accidentally connecting the wires during inspection. (*Id.*)

As for the remainder of element [9f] “wherein the integrated circuit is electrically connected to at least one of the plurality of wirings,” Saito discloses this limitation as discussed in Claim 1[d], *supra*.

Therefore, Saito and Her render claim 9 obvious. (Ex.1002, ¶128-135.)

9. Independent Claim 10

10[pre] “*A flexible substrate comprising:*”

See Claim 9[pre], *supra*.

10[a] “*a substrate body;*”

See Claim 9[a], *supra*.

10[b] “*a plurality of wirings...;*”

See Claim 9[b], *supra*.

10[c] “*a plurality of connection terminals...;*”

See Claim 9[c], *supra*.

10[d] “*an inspection electrode... ”*

See Claim 9[d], *supra*.

10[e] “*the inspection electrode being disposed... ”*

See Claim 9[f], *supra*.

Therefore, claim 10 is obvious over the combination of Saito and Her.
(Ex.1002, ¶¶136-141.)

10. Dependent Claim 11

An electro-optical device comprising: the flexible substrate according to claim 10; and an electro-optical panel that is electrically connected to the flexible substrate via at least one of the plurality of connection terminals.

As discussed previously, the combination of Saito and Her renders claim 10 obvious. Regarding the additional substance of Claim 11, see the discussion of Dependent Claim 6, *supra*. Thus, Saito and Her render claim 11 obvious. (Ex.1002, ¶¶142-144.)

B. Ground 2: Claim 5 Is Obvious Over Saito and Her, in Further View of Taguchi

1. Motivation To Combine Saito, Her, and Taguchi

A POSITA would have been motivated to combine Saito, Her, and Taguchi for practical and well-understood engineering reasons. (Ex.1002, ¶145.)

Saito and Her both disclose flexible substrates with inspection electrodes. While Saito at least suggests in Figure 3 that the test pads are visually larger than the adjacent lines, Saito does not discuss the specific dimensional relationship between the test pads and the wires. Taguchi expressly discloses that “the test pad 9 is formed to have a width greater than that of the patterned wire,” explaining that this design “facilitates easier contact with a test probe.” (Ex.1006, ¶[0011].)

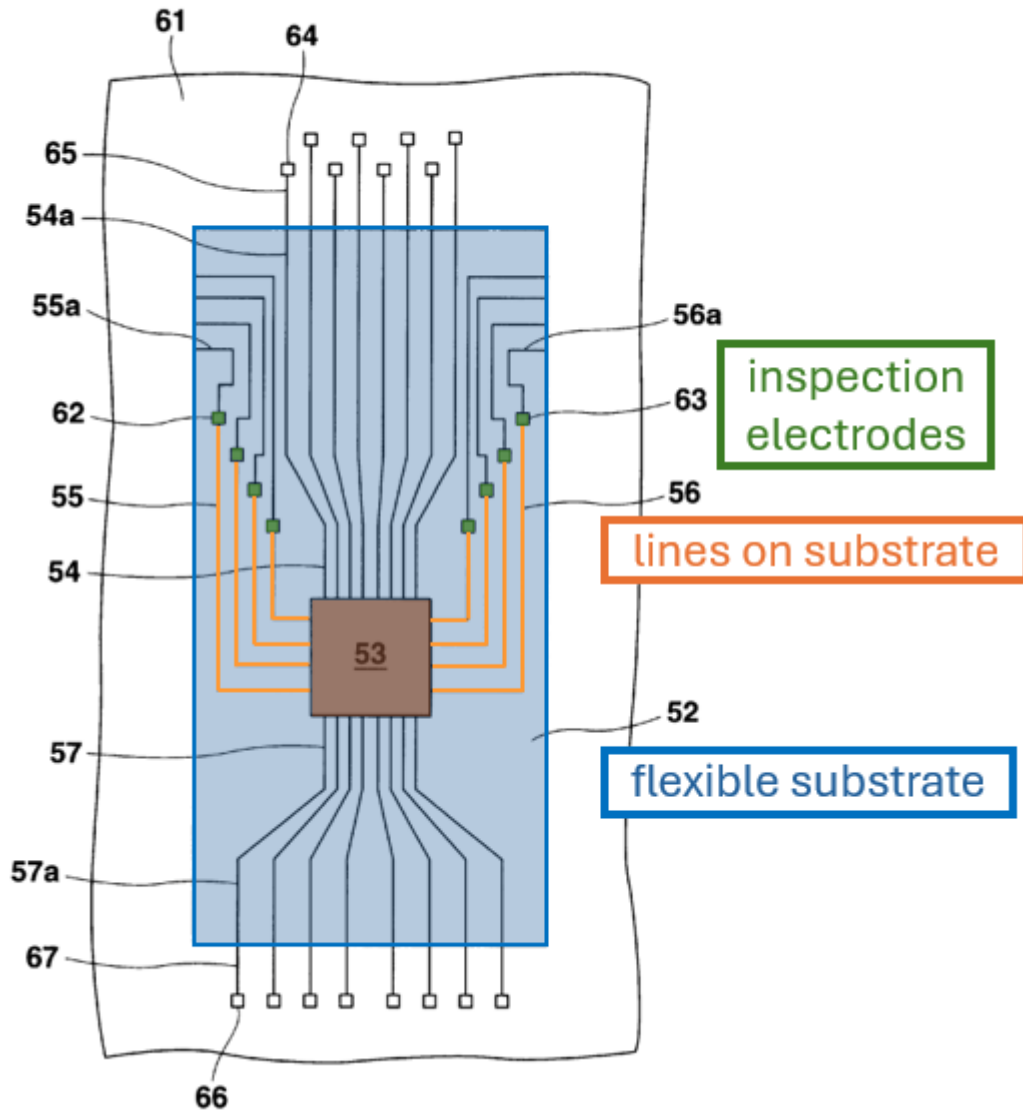
A POSITA would have found it obvious to adopt Taguchi's teaching of a widened inspection electrode for the test electrode disclosed in Saito in order to improve probe contact reliability. (Ex.1002, ¶¶146-147.) It is well known in the industry that making test pads wider than adjacent signal lines reduces alignment sensitivity and improves test accuracy, especially in high-density layouts where lines are closely spaced. (*Id.*) The combination would thus be driven by the goal of improving inspection efficiency and reliability. (*Id.*) Accordingly, adopting Taguchi's dimensional relationship into the combination of Saito and Her would have been a predictable design choice for a POSITA. (*Id.*, ¶¶145-148.)

2. Dependent Claim 5

The flexible substrate according to claim 1, wherein the inspection electrode has a width larger than the widths of the lines.

Saito discloses this limitation. As shown in FIG. 3 of Saito, the test pads (62, 63) are significantly wider than the adjacent signal lines (output lead wires 55, 56). (Ex.1002, ¶¶149-150.) A POSITA would recognize from this visual disclosure that the test pads must have a greater width to ensure reliable electrical contact during probe inspection, especially in densely routed circuits where the signal lines are extremely narrow. (*Id.*)

FIG.3



In this field, it is well known that test pads are intentionally made larger than the signal lines to facilitate accurate and repeatable probing. Given the narrow width and dense arrangement of signal lines on flexible substrates, direct contact with a probe is often unreliable and may result in misalignment, shorting, or damage. A wider inspection electrode provides a more accessible and stable contact point for

the test probe, thereby ensuring accurate signal monitoring without risk to the surrounding circuitry. Accordingly, a POSITA would understand that the width of the inspection electrode is intentionally made larger than that of the signal lines for these well-known engineering reasons. (Ex.1002, ¶151.)

To the extent Patent Owner argues that Saito does not disclose that the test pads are “larger in width,” this limitation is expressly taught in Taguchi. Taguchi states: “a test pad 9 having a width greater than that of the patterned wire is provided.” (Ex.1006, ¶[0010].) Taguchi further explains: “the test pad 9 is formed to have a width greater than that of the patterned wire so as to realize easier contact with a test probe.” (Ex.1006, ¶[0011].) This is consistent with standard industry practice and reinforces what a POSITA would already understand from Saito’s Figure 3. (Ex.1002, ¶152.)

Thus, claim 5 is rendered obvious by the combination of Saito and Her, in further view of Taguchi. (Ex.1002, ¶¶149-153.)

C. Ground 3: Claims 2, 7 and 12 Are Obvious Over Saito and Her, in further view of Kim

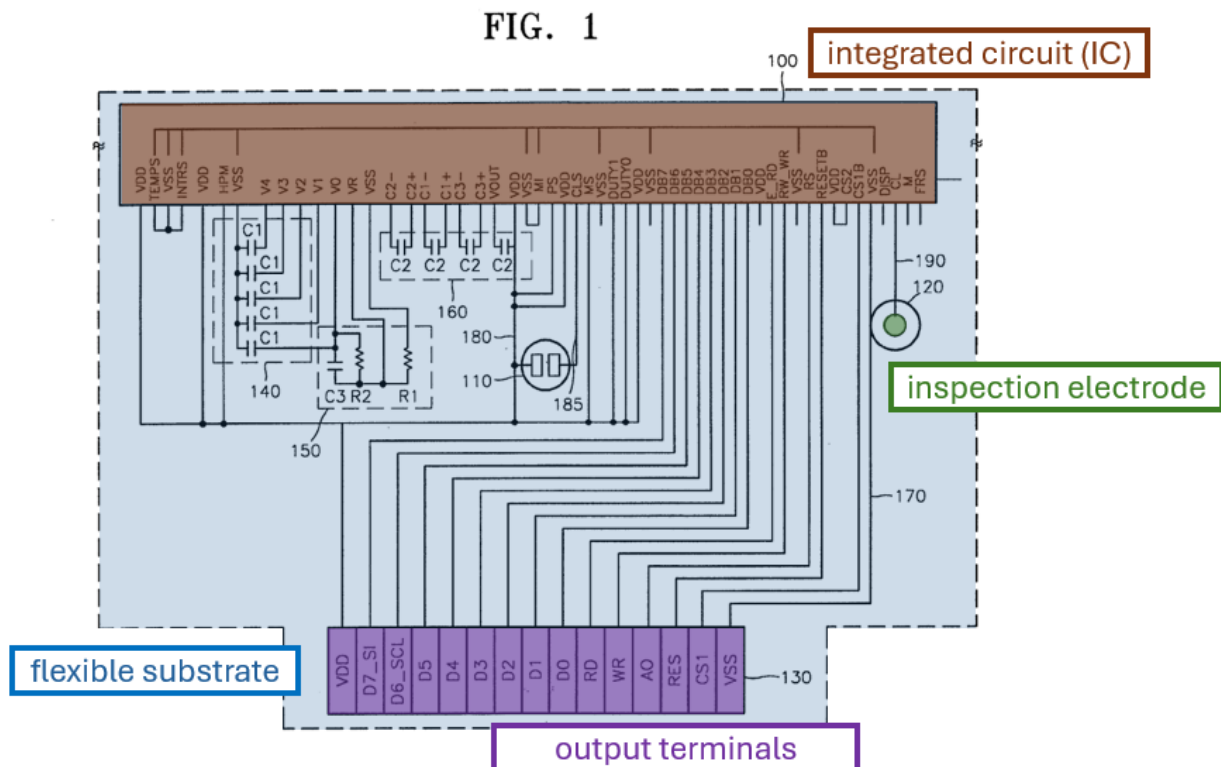
1. Dependent Claim 2

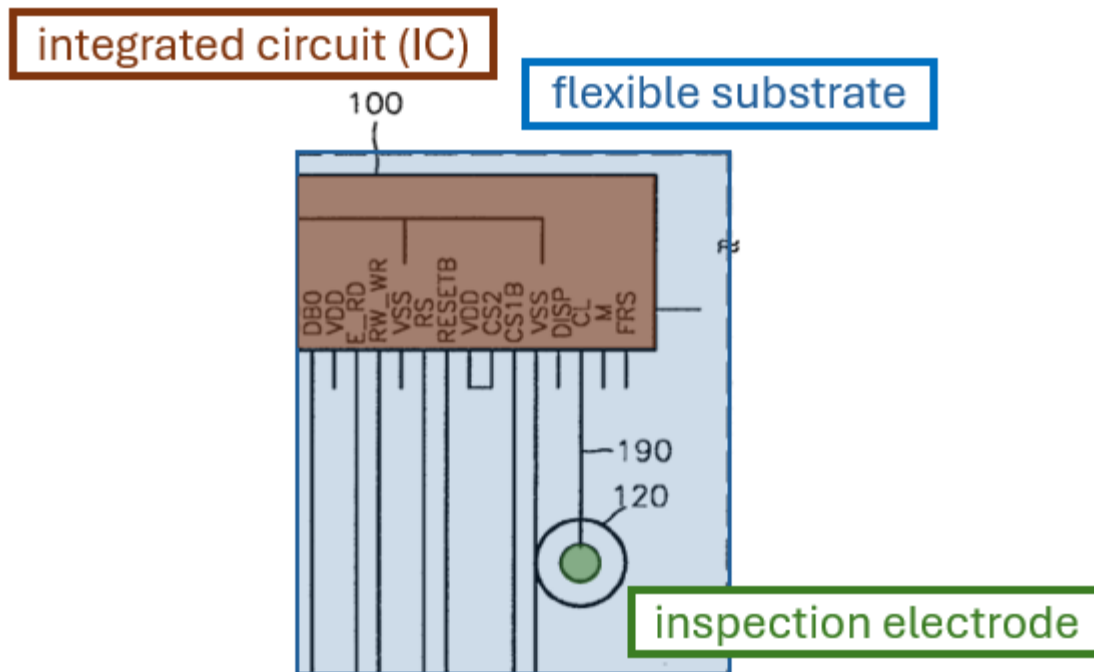
The flexible substrate according to claim 1, wherein the inspection electrode outputs a signal that is not input to or output from the integrated circuit through the plurality of connection terminals.

As discussed previously, the combination of Saito and Her renders claims 1 and 2 obvious. To the extent Patent Owner argues that this combination does not

teach an inspection electrode that outputs a signal that is not output “through the plurality of connection terminals” as recited in claim 2, Kim teaches this limitation.

Kim discloses a detailed example of an integrated circuit mounted on a flexible substrate that includes an enlarged “test pad 120” that is nearly identical to the test electrode taught in Taguchi. (Ex.1005, ¶[0040].) Kim expressly teaches inclusion of a test electrode on the substrate that “do[es] not lead to the outside of the COF package 10” (*id.*, ¶[0031]) and thereby is able to “test the electrical functions of terminals of the chip package which do not lead to the outside of the chip package” (*id.*, ¶[0033]) as seen below from Figure 1:





Specifically, test pad 120 outputs a CL signal connected through CL signal line 190 to the CL terminal. Unlike other terminals on the IC (*e.g.*, D0–D5), the CL signal is not first supplied to the IC from an input connection terminal. Thus, test pad 120 outputs a signal (CL signal) that is not previously input to the integrated circuit (chip 100) through the connection terminals (signal input portion 130). (Ex.1002, ¶¶154-56.)

In sum, Kim expressly teaches using a substrate-mounted driver IC with an enlarged test electrode (such as disclosed in Saito) to output a signal that is not input to or output from the IC through any external connection terminal (such as the test signal from Her). (Ex.1002, ¶¶154-157; *also* Ex.1005, Figures 1 and 2.)

A POSITA would understand that as ICs become more complex, ensuring the functional integrity of internal nodes and signal paths (such as the composite “test signal” taught in Her) is critical for both yield and long-term reliability. A POSITA thus would be motivated to employ a substrate-only electrode like that disclosed in Kim on the substrate of Saito in order to detect test signals originating in the IC and not sent to the LCD panel, such as the composite signal taught in Her. By providing a substrate-only test electrode connected for such a signal, it becomes possible to directly monitor, stimulate, or measure these signals during wafer-level or final testing. Moreover, a POSITA would understand that substrate-only test electrodes allow for more comprehensive test coverage, including the ability to isolate and diagnose faults within specific blocks or signal paths. Therefore, it would have been obvious to a POSITA to combine the approach taught in Kim with Saito and Her, namely, modifying one or more test pad structures taught in Saito to terminate on the substrate to monitor test signals created internally by the IC (such as the composite test signal from Her) that are not sent to the LCD panel. (Ex. 1002, ¶¶154-158.)

Therefore, claim 2 also is obvious over Saito and Her, in further view of Kim. (Ex.1002, ¶¶154-159.)

2. Dependent Claims 7 and 12

*An electronic device comprising the electro-optical device
according to claim 6 / 11*

As discussed previously, the combination of Saito and Her renders claims 6 and 11 obvious. *See* Section VIII.A, *supra*. That combination, in further view of Kim, also renders dependent claims 7 and 12 obvious.

Saito discloses an electronic device. Saito describes a liquid crystal display device that includes (i) a liquid crystal display panel (i.e., the electro-optical panel), (ii) a semiconductor chip for driving the panel, and (iii) a film wiring board (i.e., the flexible substrate), all electrically interconnected to form a functional unit. (Ex.1004, 3:25-28; 4:9-11.) A POSITA would understand that the term “**electronic device**” in claims 7 and 12 is broader than “electro-optical device” and encompasses a display module that includes active circuitry for driving and interfacing with the panel. Saito’s liquid crystal display device meets this understanding, as it integrates a display panel, IC driver, and flexible wiring substrate into a single unit for electronic display functionality. Saito consistently refers to this integrated assembly as a “**liquid crystal display device,**” which a POSITA would recognize as a type of electronic device widely used in consumer electronics, computers, automotive displays, and other commercial applications. Thus, Saito discloses “an electronic device,” as recited in claims 7 and 12. (Ex.1002, ¶¶160-166.)

To the extent Patent Owner argues that Saito does not disclose an “electronic device,” this limitation is taught in Kim. Like Saito, Kim describes “integrated circuit (IC) packages for LCDs” (Ex.1005, ¶[0005]) each “mounted on a base film”

substrate (*id.*, ¶[0011]). Kim simply makes explicit what is manifest to a POSITA (and even a lay person), namely, “employing a liquid crystal display panel” such as disclosed in Saito “**in various electronic devices** such as laptop computers (notebook computers), mobile phones, watches, and measuring instruments and apparatuses.” (*Id.*, [0006]; Ex.1002, ¶160-166.) Therefore, claims 7 and 12 are obvious over Saito and Her, in further view of Kim. (*Id.*)

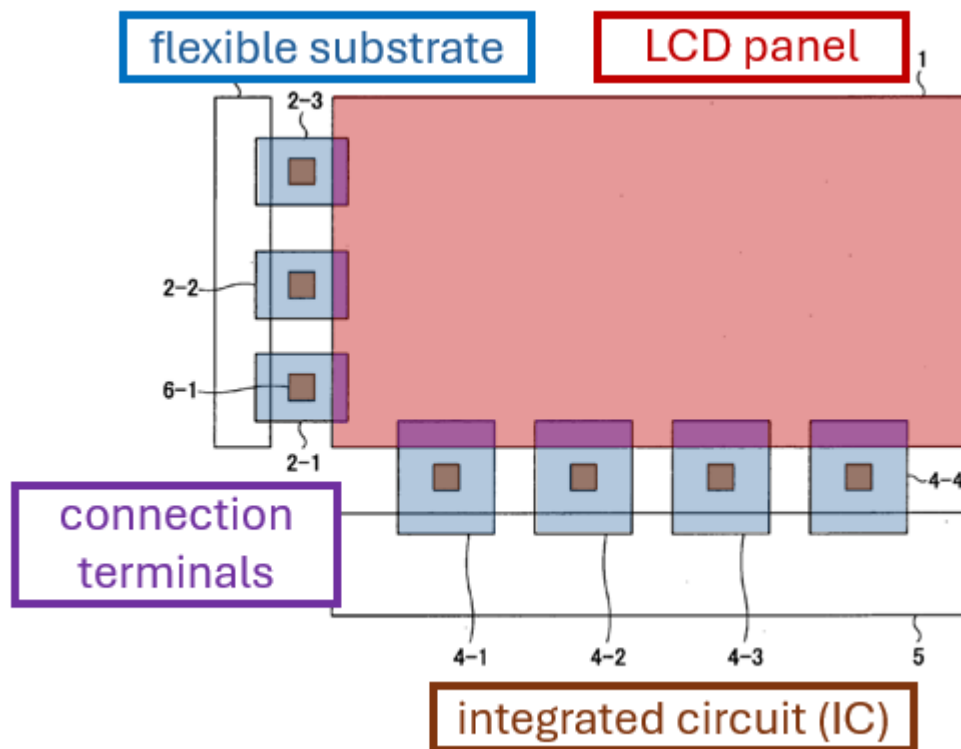
D. Ground 4: Claims 1-6 and 8 Are Obvious Over Taguchi and Her

1. Motivation To Combine Taguchi with Her

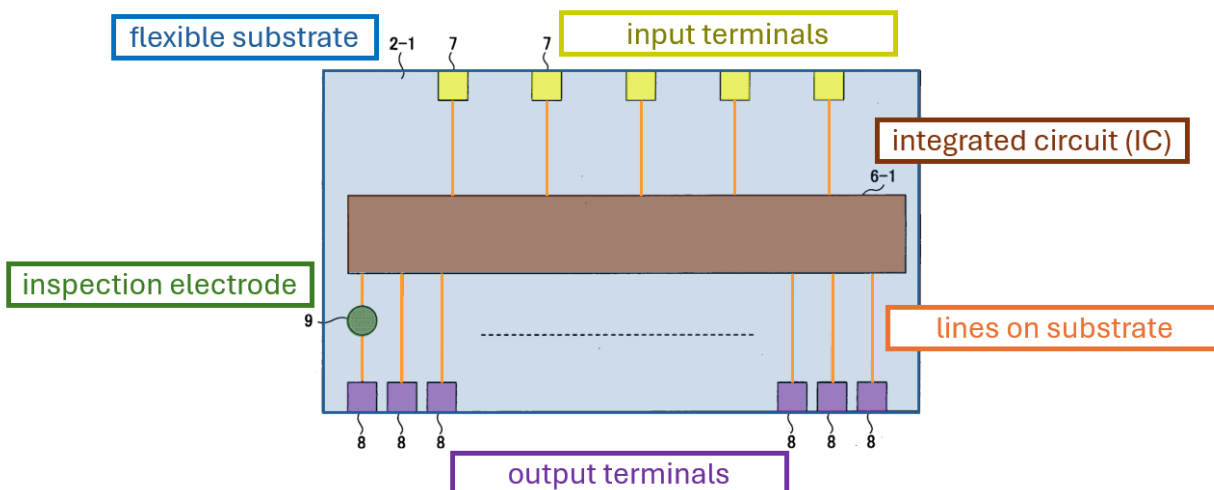
A POSITA would have been motivated to combine the teachings of Taguchi and Her. Both references are in the same field of semiconductor integrated circuits mounted on substrates and used as drivers for connected LCD panels. Further, both references teach checking whether a substrate-mounted driver IC is functioning properly through use of either a dedicated test pin or test pad connected to the IC. Thus, a POSITA would look to both references to design a source driver IC for an LCD panel that can be externally tested. A POSITA also would have had a reasonable expectation of success combining the teachings from the references, because both teach compatible methods and systems for using substrate-mounted ICs to drive LCD panels, and for testing the same. (Ex.1002, ¶¶167-168.)

Taguchi discloses a conventional arrangement of a “plurality of insulation film substrates 2-1 through 2-3 and 4-1 through 4-4 [that] are coupled to X and Y

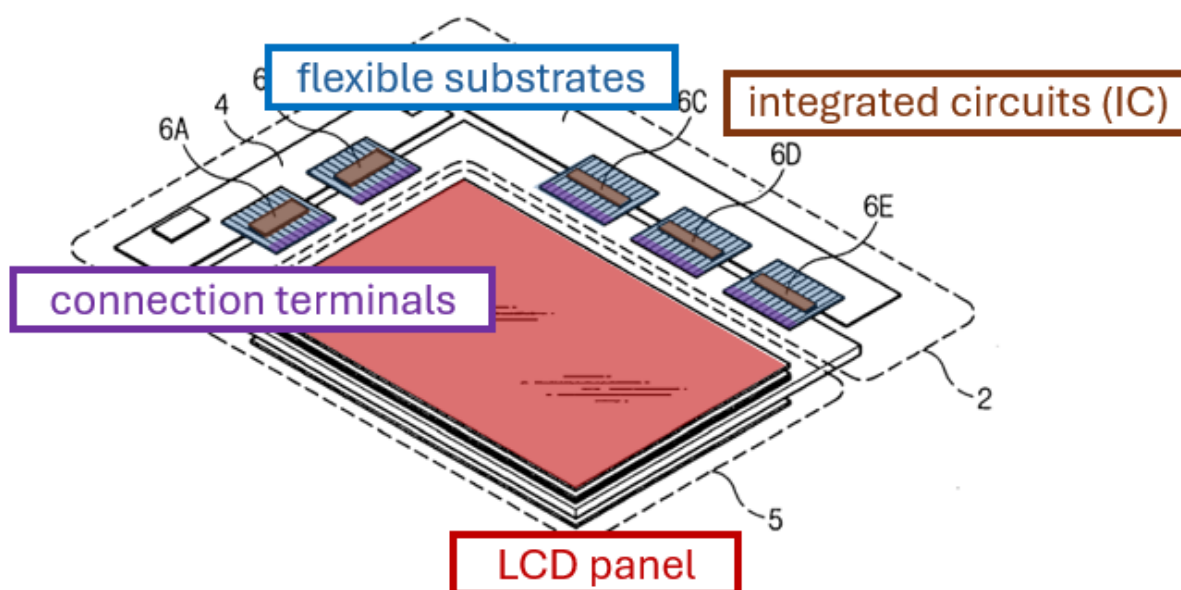
directional edges of a liquid crystal panel 1” (Ex.1006, ¶[0007]) and for “each of these insulation film substrates, a drive IC, which is collectively illustrated in FIG. 1 as the reference numeral 6-1, is connected to convert an input signal into a liquid crystal drive signal and supply the liquid crystal drive signal to the liquid crystal panel 1” (*id.*):



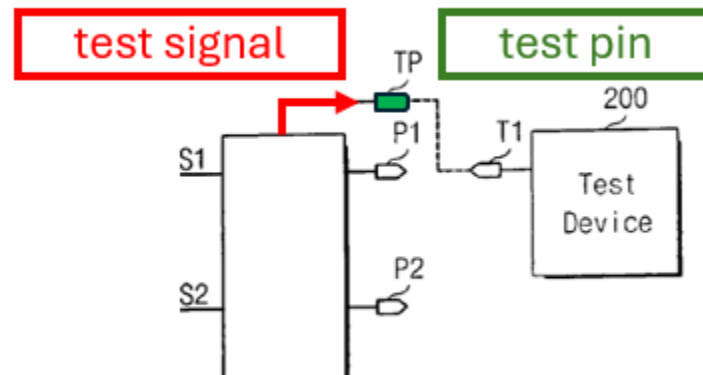
Taguchi further teaches using “wires patterned on the insulation film substrate” that are connected to the pins of the mounted driver IC 6-1, including “[o]n one of the patterned wires . . . a test pad 9 having a width greater than that of the patterned wire is provided” which facilitates “easier contact” with an external “test probe” (Ex.1006, ¶[0010-11]), as seen in Figure 2:



On its part, Her discloses a nearly identical arrangement of “an LCD panel 5” (Ex.1007, ¶[003]) and “a plurality of gate driver ICs 6A-6C and source driving ICs 6C-6E for driving a panel 5” (*id.*, ¶[004]) as seen in Figure 1:



Her further describes the “schematic block diagram of a circuit” within each disclosed “driving integrated circuit (IC)” (Ex.1007, ¶[0017]), including a designated “test pin TP” intended to be connected to an external “test device 200” (*id.*, ¶[0034]), as seen in the below excerpt from Figure 2:



Given these express teachings, a POSITA would be motivated to combine, with a reasonable expectation of success, Taguchi’s patterned substrate wire and enlarged test electrode with the dedicated IC “test pin” and corresponding testing circuit disclosed in Her. In particular, a POSITA would be motivated to combine the testing approach of Her with the “easier” means of reading a test signal taught in Taguchi, namely, employing a LCD-driver on the flexible substrate with a dedicated test pin as disclosed in Her and connecting that “test pin” to an enlarged test electrode for improved reading by an external test probe as taught in Taguchi. (Ex.1002, ¶¶167-173.)

Her also teaches that “a semiconductor integrated circuit” such as disclosed in both references conventionally was “tested by assigning test pins of a test device to all input/output pins in a one-on-one relationship.” (Ex.1007, ¶[0006].) At the time of Taguchi and Her,¹ however, “the number of pins installed at driving ICs [was] increasing and a pitch between pins [was] decreasing,” resulting in “difficulty in increasing the number of pins of a test device as pins of the semiconductor integrated circuit increase in number.” (*Id.*, ¶[0007].) Implementing Her’s integrated circuit—including the test-mode switching and the “channel shifter” that creates a new composite test signal to be sent to a dedicated “test pin”—addresses this industry-wide problem by dramatically simplifying the testing of the substrate-mounted ICs disclosed in Taguchi. Thus, a POSITA would have been further motivated, with a reasonable expectation of success, to adopt key aspects of the test circuit taught in Her to simplify testing of the driver ICs taught in Taguchi. (Ex.1002, ¶¶167-175.)

2. Independent Claim 1

1[pre] “A flexible substrate comprising:”

To the extent the preamble is limiting, Taguchi discloses a “flexible substrate.” Figure 1 of Taguchi depicts a “plurality of insulation film substrates 2-1 through 2-3 and 4-1 through 4-4 [that] are coupled to X and Y directional edges of

¹ Both Taguchi and Her were filed and published on the exact same days.

a liquid crystal panel 1” (Ex.1006, ¶[0007]). Taguchi teaches that the “insulation film substrates” are composed of a flexible material “such as a polyimide film.” (*Id.*, ¶[0060]; Ex.1002, ¶¶176-177.)²

1[a] “a substrate body;”

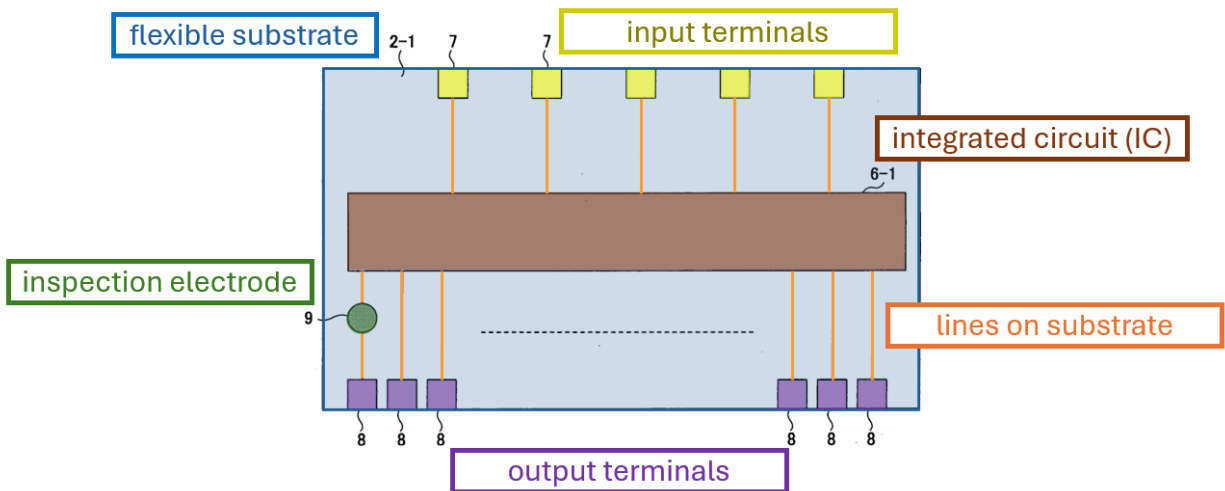
As discussed in Claim 1[pre], *supra*, Taguchi discloses “a substrate body.” Figure 1 of Taguchi discloses seven discrete substrate bodies (2-1 through 2-3; 4-1 through 4-4) (Ex.1006, ¶[0008]), and Figure 2 of Taguchi provides a more detailed view of one such substrate body, namely, “insulation film substrate 2-1” (*id.*, ¶[0010]; Ex.1002, ¶178).

² Although not part of this ground, background references confirm that polyimide-film substrates like the one used in Taguchi are “flexible substrates.” For instance, Kim provides two specific examples of known “polyimide film” options for such substrates: (i) “tape automated bonding (TAB)” which provides “improved flexibility” by employing a “polyimide tape” (Ex.1005, ¶¶[0006-07]); and (ii) a “chip on film (COF)” which uses a substantially reduced “thickness of a polyimide tape,” and thus provides “more flexibility” for the substrate (*id.*, ¶[0007]). As set forth in Section IV.D, *supra*, “flexible circuit boards [] made of a film or the like” were ubiquitous in this industry as of the priority date of the ’512 patent. (*E.g.*, Ex.1009, ¶[0028]; Ex.1002, ¶177)

1[b] “a plurality of lines that are arranged on the substrate body;”

Taguchi discloses “a plurality of lines that are arranged on the substrate body.”

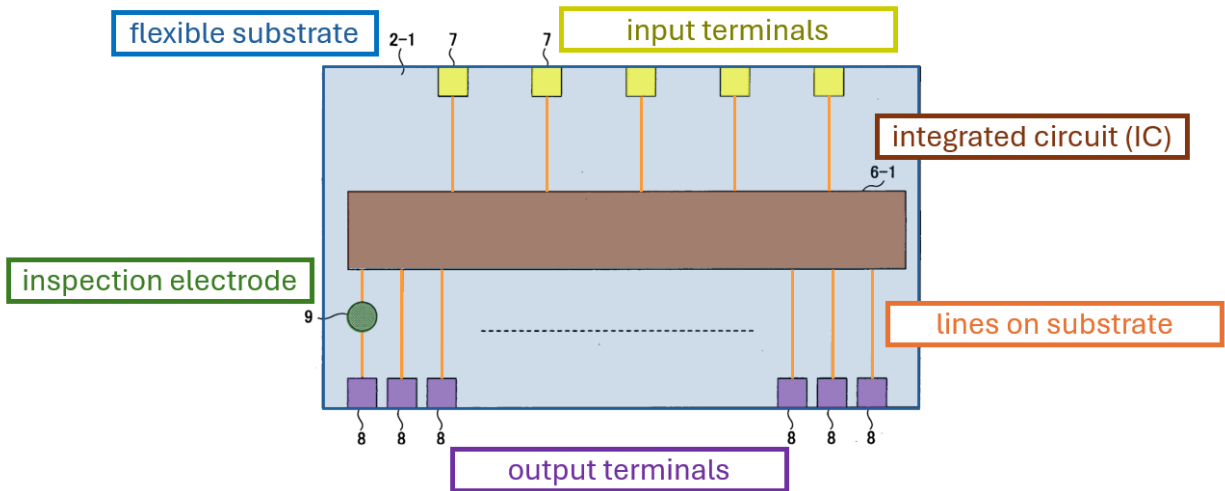
For example, Figure 2 of Taguchi depicts multiple lines arranged on the substrate 2-1 (in orange below):



Taguchi teaches that “[t]he gate drive IC 6-1 is connected to input signal terminals 7 and output signal terminals 8 via **wires patterned on the insulation film substrate 2-1.**” (Ex.1006, ¶[0010].) A POSITA would understand that the terms “wire” and “line” are interchangeable in this context. (Ex.1002, ¶179.)

1[c] “a plurality of connection terminals that are arranged on an end portion of the substrate body and electrically connected to the respective lines;”

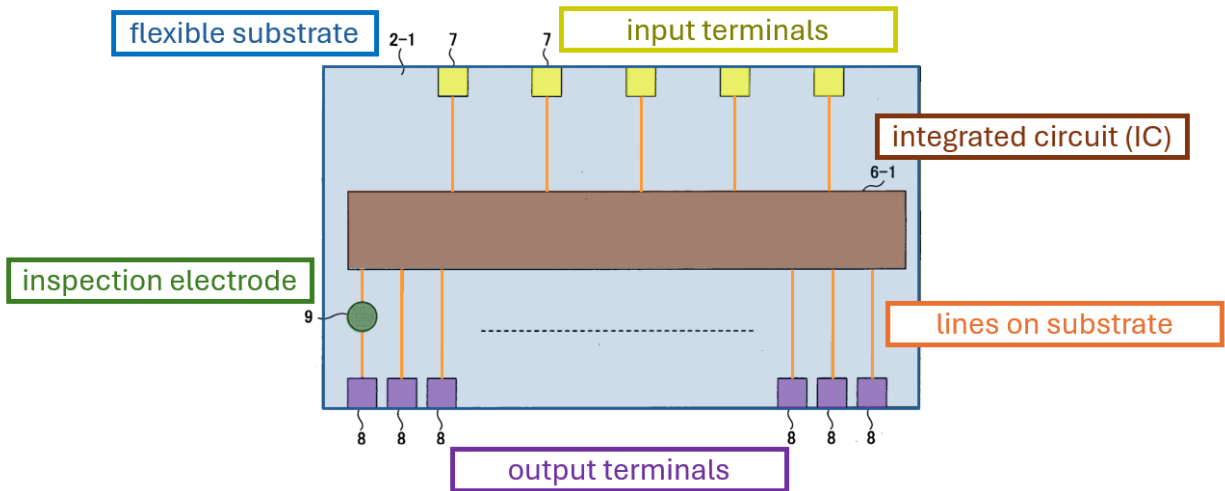
Taguchi discloses “a plurality of connection terminals that are arranged on an end portion of the substrate body and electrically connected to the respective lines” as depicted, for example, in Figure 2 (in purple below):



Specifically, Taguchi teaches “**patterned wires connecting between the output signal terminals 8 and the gate drive IC 6-1**” (Ex.1006, ¶[0010]; Ex.1002, ¶180.)

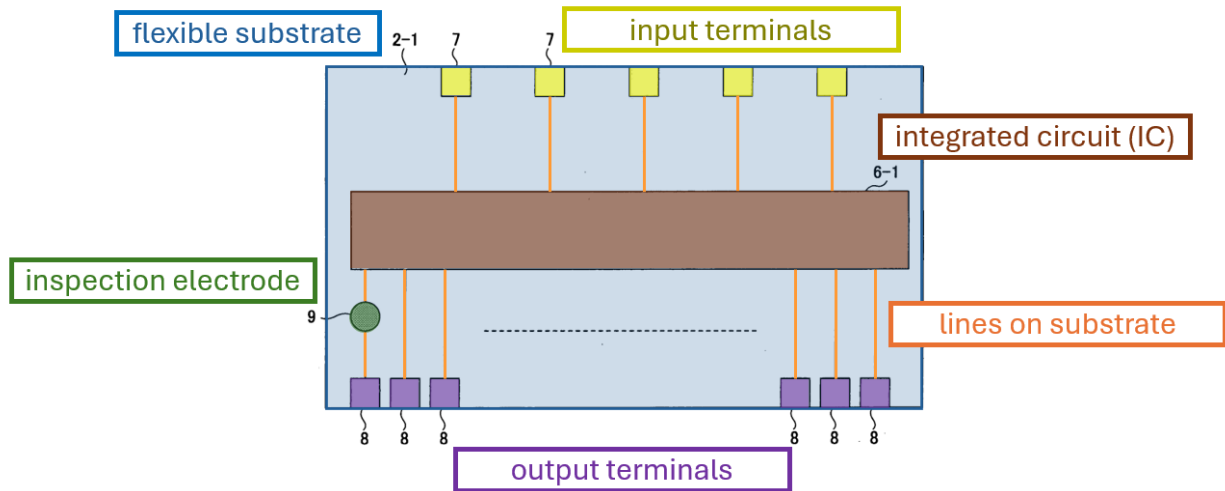
1[d] “an integrated circuit that is arranged on the substrate body and electrically connected to at least one of the lines;”

Taguchi discloses “an integrated circuit that is arranged on the substrate body and electrically connected to at least one of the lines.” Specifically, Taguchi teaches “**patterned wires connecting between the output signal terminals 8 and the gate drive IC 6-1**” (Ex.1006, ¶[0010]; Ex.1002, ¶181) as seen, for example, in Figure 2:



1[e] “an inspection electrode that is arranged on the substrate body and electrically connected to the integrated circuit and capable of outputting a signal processed in the integrated circuit, and”

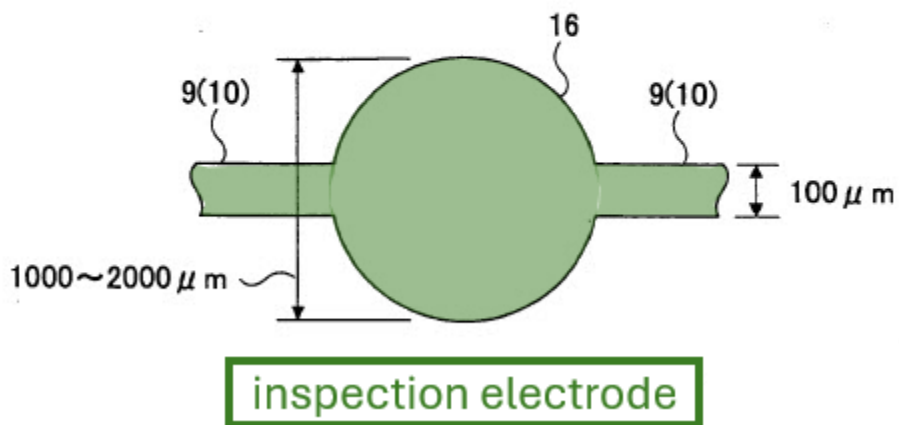
Taguchi discloses “an inspection electrode...” As discussed in Claim 1 [b]-[d], *supra*, Taguchi teaches using “wires patterned on the insulation film substrate” that are electrically connected to the driver IC. As seen in Figure 2 of Taguchi, this includes “[o]n one of the patterned wires . . . a test pad 9 having a width greater than that of the patterned wire is provided” which facilitates “easier contact” with an external “test probe” (Ex.1006, ¶¶[0010-11]):



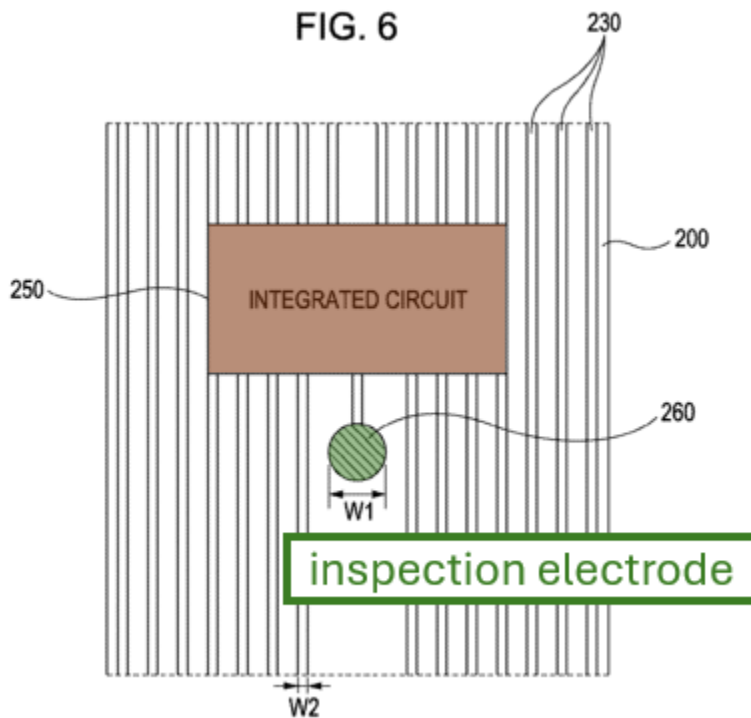
Using this test pad 9, “it can be checked whether the gate drive IC 6-1 is normally operating,” including as illustrated in Figure 2 “the output side signal [from the IC] can be detected through contact of the test pad 9 with the test probe.” (*Id.*, ¶[0012].)

Taguchi further provides a specific example of a test electrode with dimensions in Figure 8, showing a patterned signal wire connected where “a relatively large circle is patterned as a portion corresponding to the test pad 16” (*Id.*, ¶[0057].)

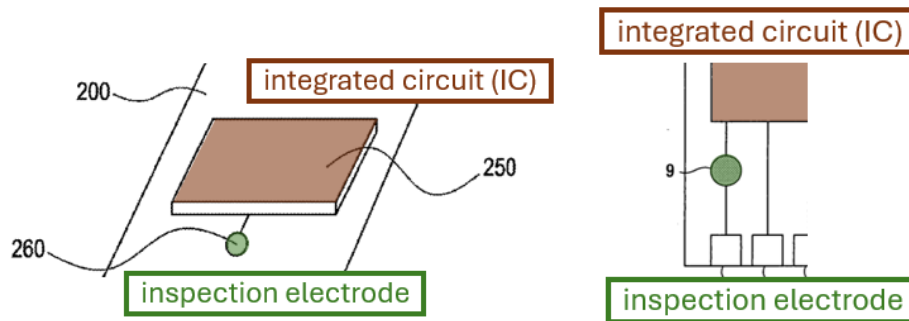
FIG. 8



Notably, the above figures from Taguchi disclose a structure that is largely identical to the “test electrode 260” shown in Figure 6 of the ’512 patent:



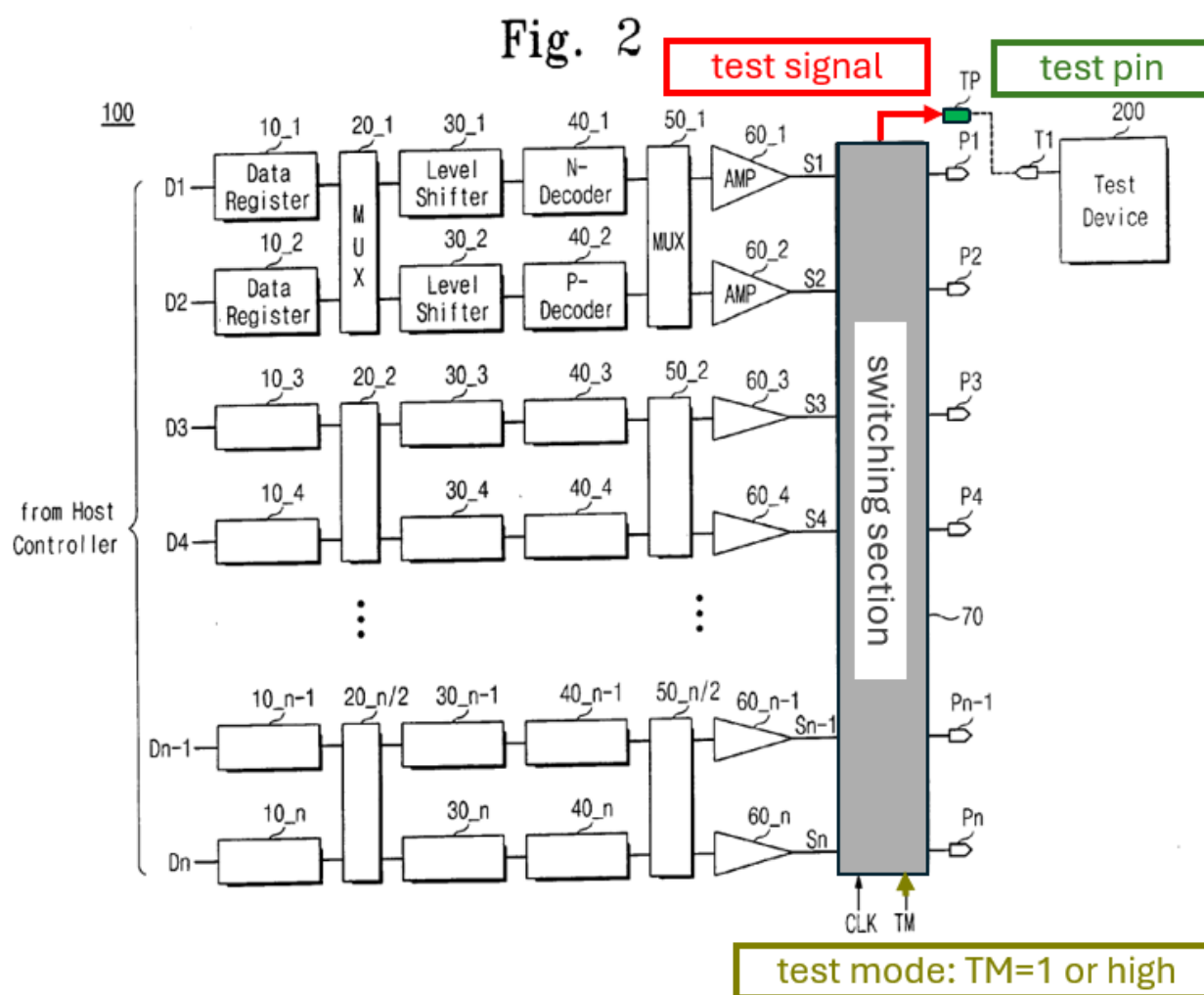
A POSITA would understand that a “test pad” like the one shown in Figure 2 (and Figure 8) of Taguchi is synonymous with the claimed “inspection electrode” of claim 1. As seen above, both are patterned and arranged on the substrate. Both are connected to the integrated circuit on the substrate. And both operate as electrical contacts capable of outputting signals processed in the IC for testing and diagnostic purposes. In the field of semiconductor substrates and display modules, it is well known that “test pads” serve as inspection points electrically connected to internal circuitry and are functionally interchangeable with what claim 1 of the ’512 patent calls an “inspection electrode.” This is manifest from inspection-electrode depictions in the respective Figures of the ’512 patent and Taguchi:



Accordingly, based on their placement, structure, and function in Taguchi, a POSITA would equate each “test pad” disclosed in Taguchi with the claimed “inspection electrode.” (Ex.1002, ¶¶182-186.)

1[f] “a switching section that switches an operation of the inspection electrode on/off to cause the inspection electrode to output or not to output the signal processed in the integrated circuit.”

Although Taguchi does not expressly disclose the “switching section...” described in Claim 1[f], Her discloses this limitation. Her discloses the “schematic block diagram of a circuit” to use for a “driving integrated circuit (IC)” (Ex.1007, ¶[0017]) like the ones disclosed in Taguchi, including a designated “test pin TP” (*id.*, ¶[0034]). Figure 2 of Her further discloses “a channel shifter 70” that acts as a switching section that controls the operation of the “test pin TP.” (*Id.*, [0028].) “The channel shifter 70 operates in response to a test mode signal TM” (*id.*, [0029]) as seen in Figure 2:



“The test mode signal TM has a low level (i.e., logic ‘0’) in a normal mode and has a high level (i.e., logic ‘1’) in a test mode.” (*Id.*, ¶[0029]; Figure 3.) The switching section of channel shifter 70 “determines whether the test mode signal TM indicates a test mode.” (*Id.*, ¶[0030]). If the TM signal “indicates a test mode (i.e., high level),” the channel shifter 70 switches the test pin TP “on” and “sequentially outputs the source driving signals S1~Sn” in a composite signal to the test pin TP “in response to a clock signal CLK.” (*Id.*, ¶[0032]; Figure 3.) In contrast, “[w]hen the test mode signal TM indicates the normal mode, not the test mode” (*id.*, ¶¶ [0030-31]), the channel shifter switches the test pin TP “off” and “the source driving signals S1-Sn” instead “are provided to the LCD panel through the data output pins P1-Pn” (*id.*, ¶[0028]).

It would be obvious to a POSITA in view of Taguchi to connect a patterned wire with an enlarged test electrode to the “test pin TP” of Her for “easier reading” by an external test probe. When so connected, the switching mechanism of “channel shifter 70” turns the inspection electrode on the substrate on/off in response to whether the test mode signal TM indicates the “test mode” (*i.e.*, “high level,” or “1”) or the “normal mode” (*i.e.*, “low level,” or “0”). (Ex.1002, ¶¶187-189.)

In addition, a POSITA would understand that a test pad that is always “on” could introduce several drawbacks. Such a test electrode that continually outputs a test signal may add unwanted parasitic capacitance or act as an antenna, potentially

degrading signal integrity or increasing susceptibility to noise on proximate lines. Moreover, a test pad that is always active may draw unnecessary current or interact with other circuitry, impacting power efficiency. Thus, a POSITA would be motivated to add the on/off switching mechanism taught in Her to the test-pad arrangement of Taguchi to selectively enable or disable the connection between the test pad and the driver IC, and would have a reasonable expectation of success in doing so, to help eliminate parasitic effects, prevent unintended signal coupling or leakage, and conserve power. Further, a POSITA would know that by isolating the test pad when it is not needed, the risk of electro-static discharge, current leakage, or other negative environmental factors affecting the IC also is minimized. (Ex.1002, ¶¶190-191.)

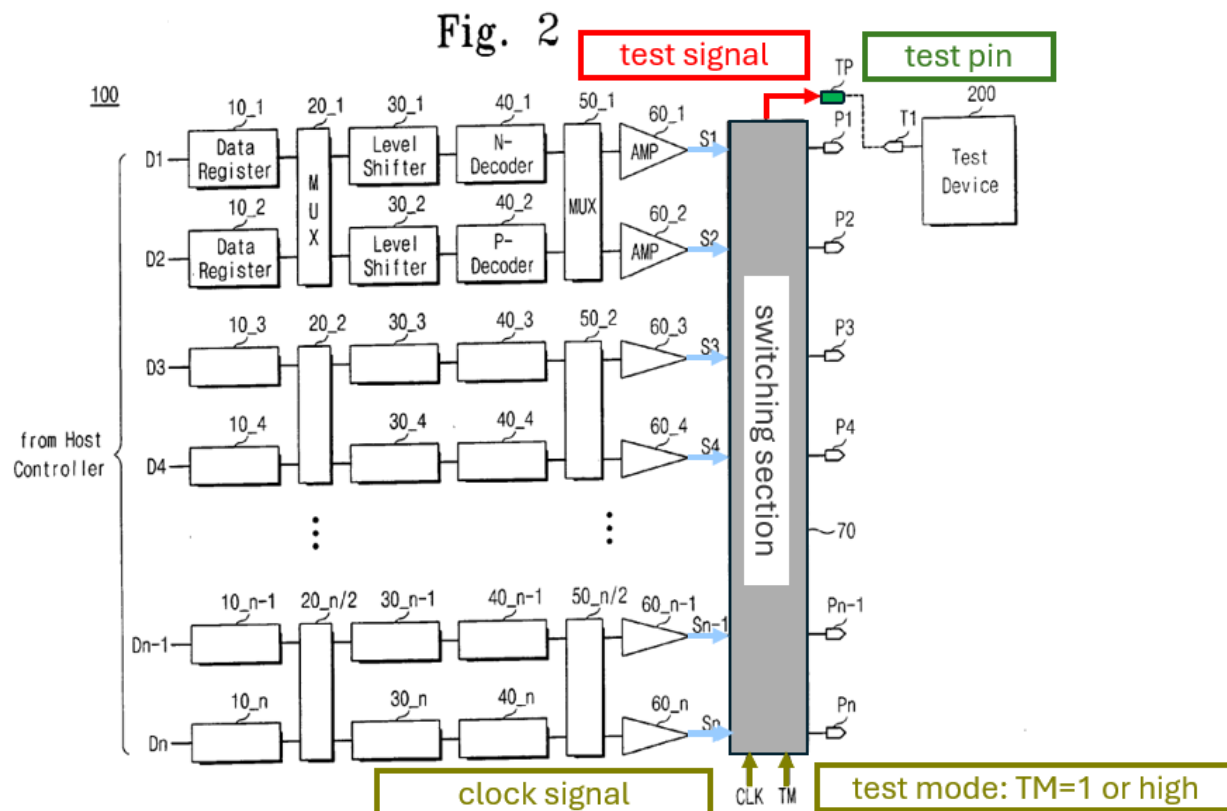
Therefore, it also would have been obvious to a POSITA to integrate a switching section and test pin taught in Her to control a test electrode on the semiconductor substrate as disclosed in Taguchi to address operational requirements for signal integrity and reliability. (*Id.*)

In sum, the combination of Taguchi and Her renders independent claim 1 of the '512 patent obvious. (Ex.1002, ¶¶176-192.)

3. Dependent Claim 2

The flexible substrate according to claim 1, wherein the inspection electrode outputs a signal that is not input to or output from the integrated circuit through the plurality of connection terminals.

As discussed above, the combination of Taguchi and Her renders claim 1 obvious. Her also discloses the “wherein the inspection electrode...” limitation of claim 2. A POSITA would recognize that implementing the testing arrangement of Her’s integrated circuit would advantageously simplify the testing of the IC drivers disclosed in Taguchi. Her accomplishes this using a “channel shifter” that, when in “test mode,” amalgamates the incoming “source driving signals S1~Sn” into a new composite “signal outputted to a test pin TP.” (Ex.1007, ¶[0033]; Figures 2-4.) This composite “signal” is created internally by the driver IC and is only monitored directly on the substrate by an external “test device 200” and not output to the LCD panel. (Ex.1007, ¶[0032-34]; Figures 2-4). Thus, as described in claim 2, Her’s composite test signal is neither input nor output “through the plurality of connection terminals.” (Ex.1002, ¶¶193-194.)



Therefore, claim 2 also is obvious over Taguchi and Her. (*Id.*)

4. Dependent Claim 3

The flexible substrate according to claim 1, wherein the switching section [] switches the types of signals that are to be output from the inspection electrode.

As discussed, the combination of Taguchi and Her renders claim 1 obvious.

Her also discloses the “wherein the switching section...” limitation of claim 3.

As discussed in Claim 1[f] *supra*, it would be obvious (and a POSITA would be motivated) to implement the switching mechanism of the “channel shifter” IC and dedicated test pin arrangement taught in Her with the IC driver and test-electrode approach of Taguchi. Her further teaches (per Figure 4) that, when the test signal

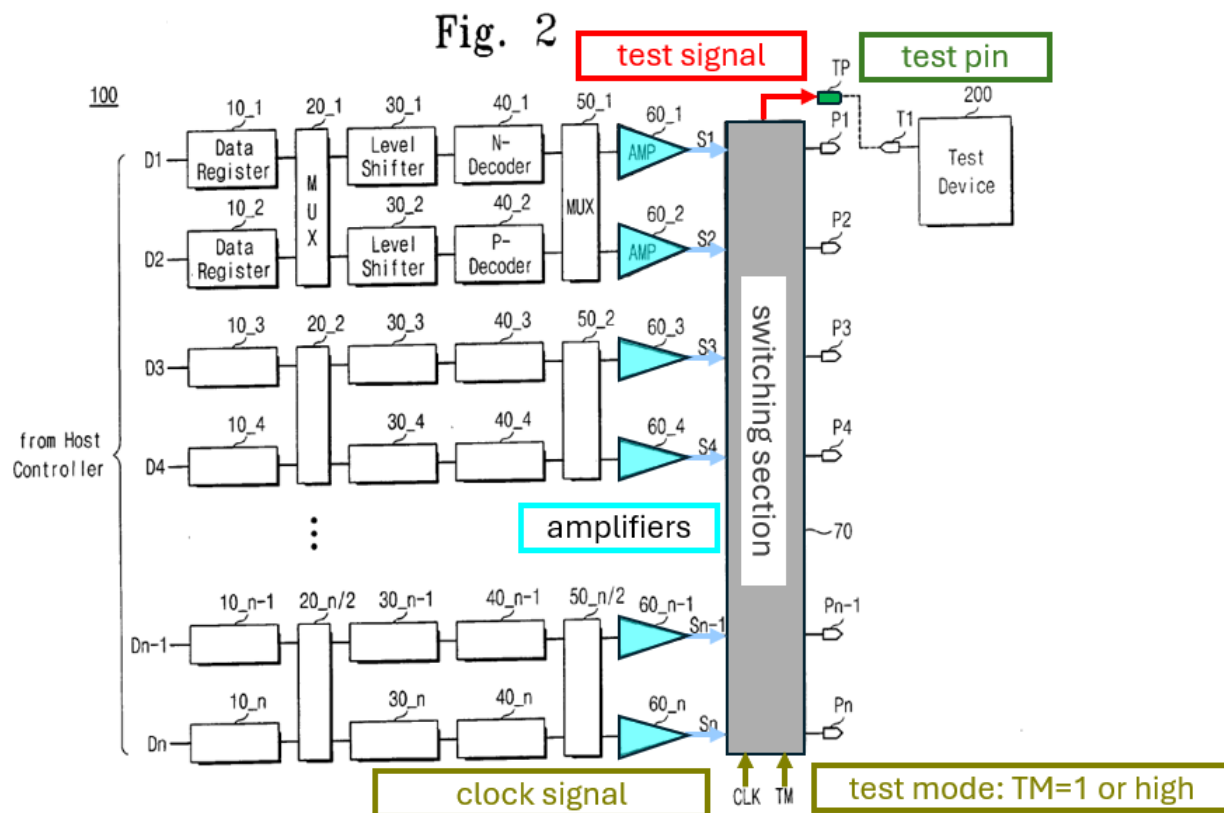
TM puts the “channel shifter” into the “test mode” and thereby switches on the operation of the test pin TP, “the channel shifter 70 outputs, at a first rising edge of the clock signal CLK, the **source driving signal S1** . . . to the test pin TP,” “[a]t a second rising edge of the clock signal CLK, the channel shifter 70 outputs the **source driving signal S2** outputted . . . to the test pin TP,” and so forth for all the signal types S1 through Sn. (Ex.1007, ¶[0033]; *also id.* (“In this manner, the channel shifter 70 sequentially outputs the source d[r]iving signals S[3]~Sn . . . to the test pin TP in response to from third to nth rising edges of the clock signal CLK”).) By so doing, the “channel shifter 70” of Her switches the types of signals that are to be output from the inspection electrode (as required by claim 3) at each successive rising edge of the input clock signal CLK. Therefore, claim 3 also is rendered obvious by the combination Taguchi and Her. (Ex.1002, ¶195-198.)

5. Dependent Claim 4

The flexible substrate according to claim 1 further comprising: an amplifier that amplifies a signal that is to be output to the inspection electrode.

As discussed previously, the combination of Taguchi and Her renders claim 1 obvious. Her also discloses the additional “an amplifier...” limitation of dependent claim 4.

As depicted in Figure 2, Her teaches that, when in test mode, the “source driving signals S₁~Sn **outputted from the amplifiers 60₁~60_n** are sequentially outputted to a test pin TP at each rising edge of a clock signal” (Ex.1007, ¶[0033]):



A POSITA would understand that the fundamental purpose of the amplifiers shown in Her, as suggested by the name “amplifier” itself, is to *amplify* an incoming signal and make the signal more reliable for later detection. The multiple amplifiers taught in Her each serves to amplify a constituent signal sent to the “channel shifter” in Her, and thereby amplifies the composite test signal sent by the channel shifter to the “test pin” (and ultimately sent to the test electrode taught in Taguchi). Therefore, claim 4 also is rendered obvious by the combination of Taguchi and Her. (Ex.1002, ¶¶199-202.)

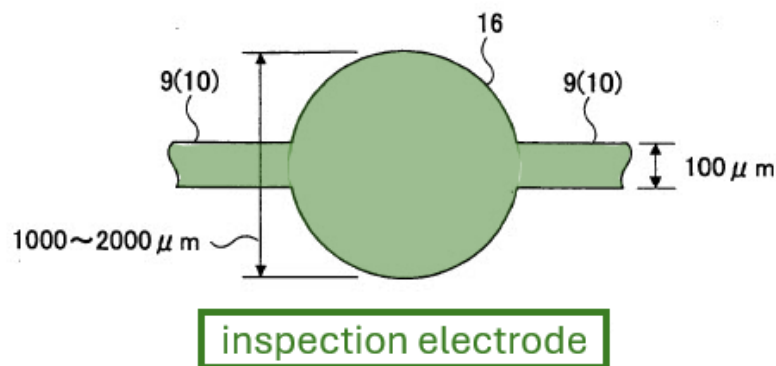
6. Dependent Claim 5

The flexible substrate according to claim 1, wherein the inspection electrode has a width larger than the widths of the lines.

As discussed previously, the combination of Taguchi and Her renders claim 1 obvious. Taguchi also discloses the additional “wherein the inspection electrode...” limitation of dependent claim 5.

As depicted in Figure 2, Taguchi teaches that “[o]n one of the patterned wires . . . a test pad 9 having a **width greater than that of the patterned wire is provided.**” (Ex.1006, ¶[0010].) Taguchi further explains that “[s]ince each patterned wire on the insulation film substrate has an extremely small width, the test pad 9 is formed to have a width greater than that of the patterned wire so as to realize easier contact with a test probe.” (*Id.*, ¶[0011].) Taguchi provides a specific example with dimensions in Figure 8 where “a relatively large circle is patterned as a portion corresponding to the test pad 16.” (*Id.*, ¶[0057].)

FIG.8



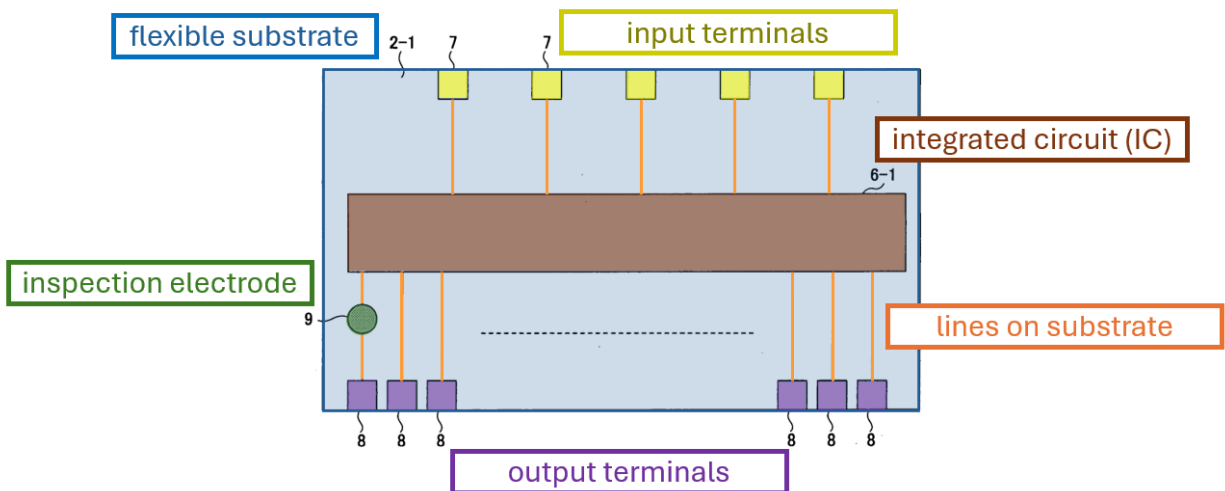
Therefore, claim 5 also is rendered obvious by the combination of Taguchi and Her.
(Ex.1002, ¶¶203-206.)

7. Dependent Claim 6

An electro-optical device comprising: the flexible substrate according to any of claims 1, 2, or 3-5 and; an electro-optical panel that is electrically connected to the flexible substrate through the connection terminals.

As discussed previously, the combination of Taguchi and Her renders claims 1-5 obvious. Taguchi also discloses the remaining substance of claim 6.

Figure 2 of Taguchi teaches that LCD-driver integrated circuits are electrically connected to input and output connection terminals on the substrate body (yellow and purple below):



Specifically, Taguchi teaches “[t]he gate drive IC 6-1 is connected to input signal terminals 7 and **output signal terminals 8** via wires patterned on the insulation film substrate 2-1.” (Ex.1006, ¶[0010].) Taguchi further teaches that each flexible

“insulation film substrate is connected to a liquid crystal panel” via the output signal terminals. (*Id.*, ¶[0021].) A POSITA would understand such an arrangement (as depicted in Figure 1) constitutes an “electro-optical device.” (Ex.1002, ¶¶207-211.)

Therefore, claim 6 also is rendered obvious by the combination of Taguchi and Her. (*Id.*)

8. Independent Claim 8

8[pre] “A flexible substrate comprising:”

To the extent the preamble is limiting, it is taught by Taguchi and Her. *See* Claim 1[pre], *supra*.

8[a] “a substrate body;”

See Claim 1[pre]/8[pre] and Claim 1[a], *supra*.

8[b] “a plurality of lines...;”

See Claim 1[b], *supra*.

8[c] “a plurality of connection terminals...;”

See Claim 1[c], *supra*.

8[d] “an integrated circuit...;”

See Claim 1[d], *supra*.

8[e] “an inspection electrode...”

See Claim 1[e], *supra*.

8[f] “a switching section....

See Dependent Claim 3, *supra*.

In sum, the combination of Taguchi and Her renders independent claim 8 of the '512 patent obvious. (Ex.1002, ¶¶212-219.)

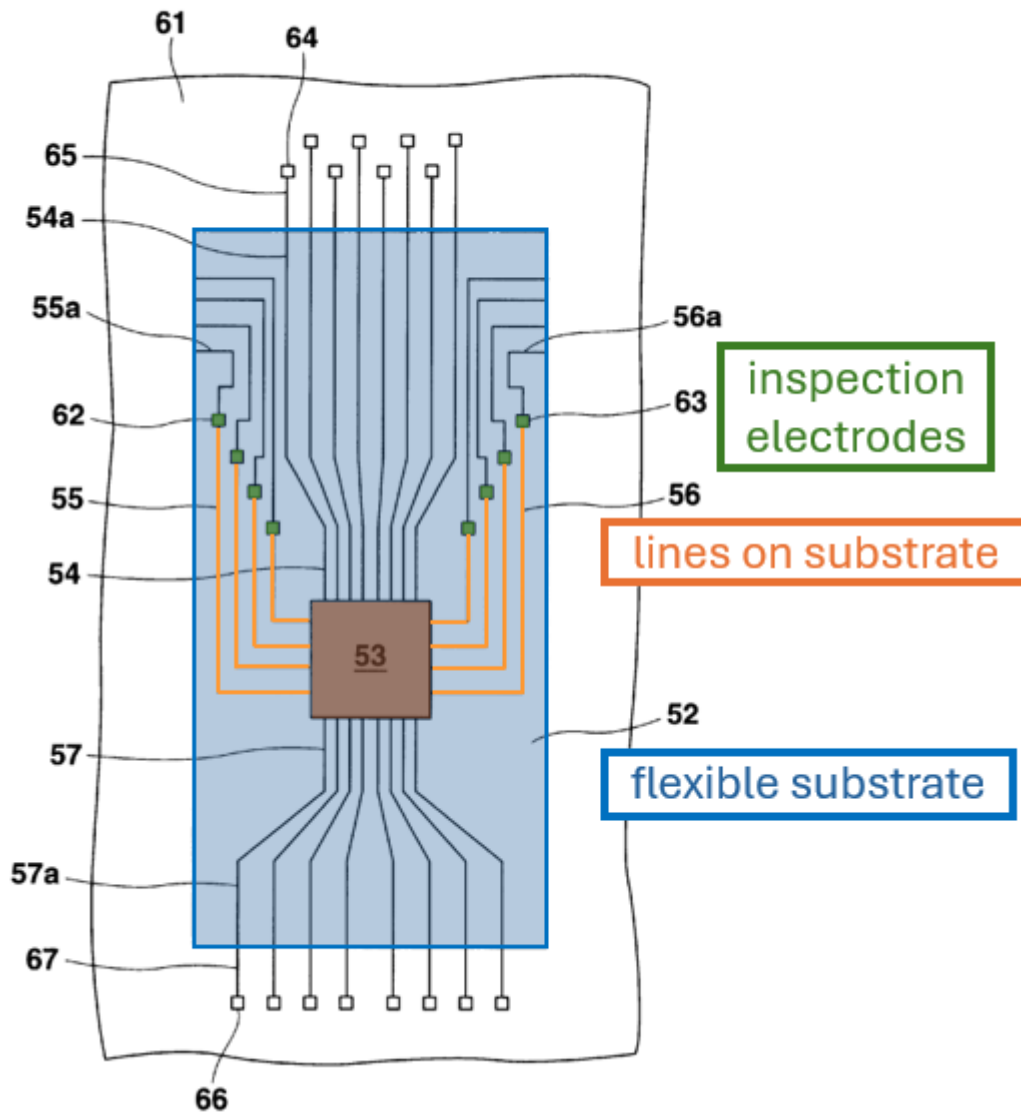
E. Ground 5: Claims 9-11 Are Obvious over Taguchi and Her, in further view of Saito

1. Motivation To Combine Taguchi and Her with Saito

For the reasons discussed in Section VIII.D, *supra*, a POSITA would have been motivated to combine the teachings of Taguchi and Her. Like those references, Saito also discloses “a liquid crystal display device having a panel connected to an IC chip mounted on a narrow film wiring board.” (Ex.1004, 1:13-15.) Saito gives two examples of flexible-substrate modules that can be used, namely, “TCP (Tape Carrier Package)” and “COF.” (*Id.*, 6:22-26; Ex.1002, ¶¶220-221.)

Like Taguchi, Saito discloses “[t]est pads 62 and 63 [that] are formed in middle portions of output lead wires 55 and 56 on the upper surface” of the flexible substrate 52, as seen in Figure 3 below:

FIG.3



A POSITA would combine the teachings of Saito with Taguchi and Her, and have had a reasonable expectation of success in doing so, because, *inter alia*, all the references teach compatible methods and systems for using substrate-mounted ICs to drive LCD panels, and for testing the same. (Ex.1002, ¶¶220-223.)

2. Independent Claim 9

9[pre] *“A flexible substrate comprising:”*

To the extent the preamble is limiting, it is taught by Taguchi. *See* Section VIII.D.2 (Claim 1[pre]), *supra*.

9[a] *“a substrate body;”*

As discussed in Claim 9[pre], *supra*, Taguchi discloses this limitation. *See* Section VIII.D.2 (Claim 1[a]), *supra*.

9[b] *“a plurality of wirings that are arranged on the substrate body;”*

Taguchi discloses this “a plurality of wirings...” limitation. *See* Section VIII.D.2 (Claim 1[b]), *supra*. Again, a POSITA would understand that the terms “wirings” and “lines” are interchangeable in this context and as used in the ’512 patent, and both represent electrical interconnects patterned on the claimed “substrate body.” (Ex.1002, ¶226.)

9[c] *“a plurality of connection terminals that electrically connects a device and at least one of the plurality of wirings;”*

Taguchi discloses “a plurality of connection terminals that electrically connects a device and at least one of the plurality of wirings.” *See* Section VIII.D.7 (Dependent Claim 6), *supra*.

9[d] *“an inspection electrode...;”*

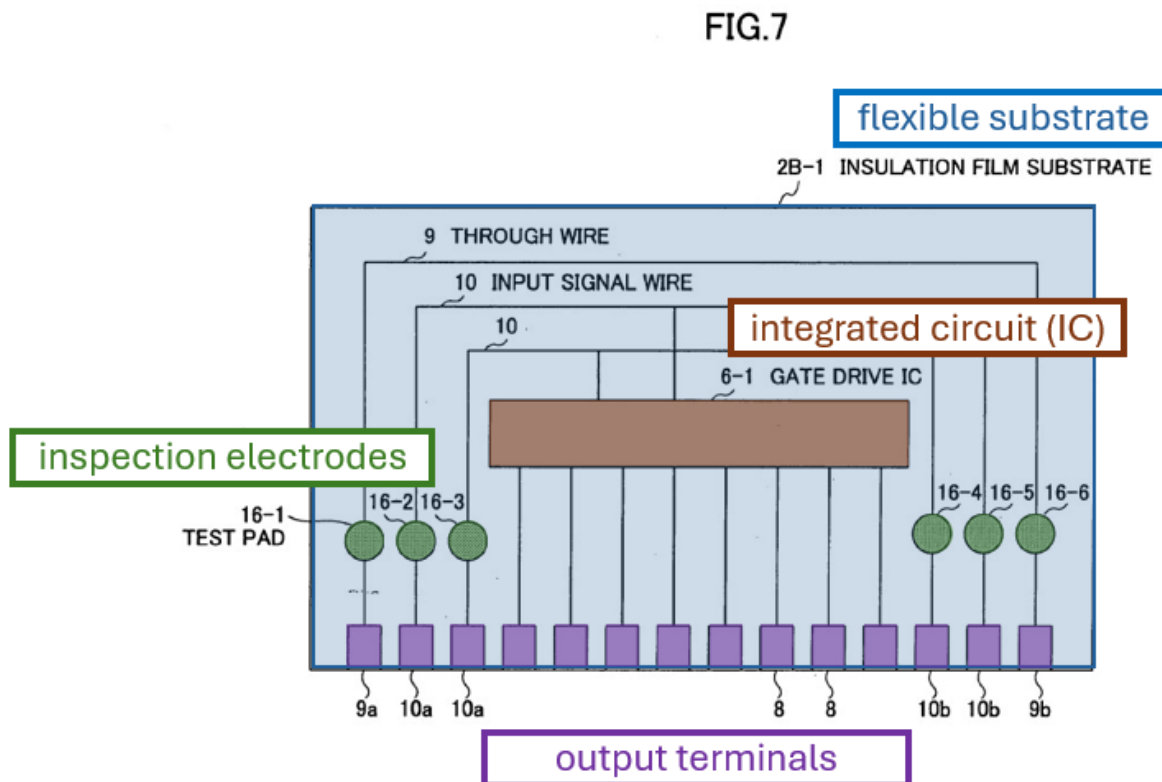
See Section VIII.D.2 (Claim 1[d] and 1[e]), *supra*.

9[e] “a switching section that switches [the] types of the signal [that] are to be outputted from the inspection electrode”

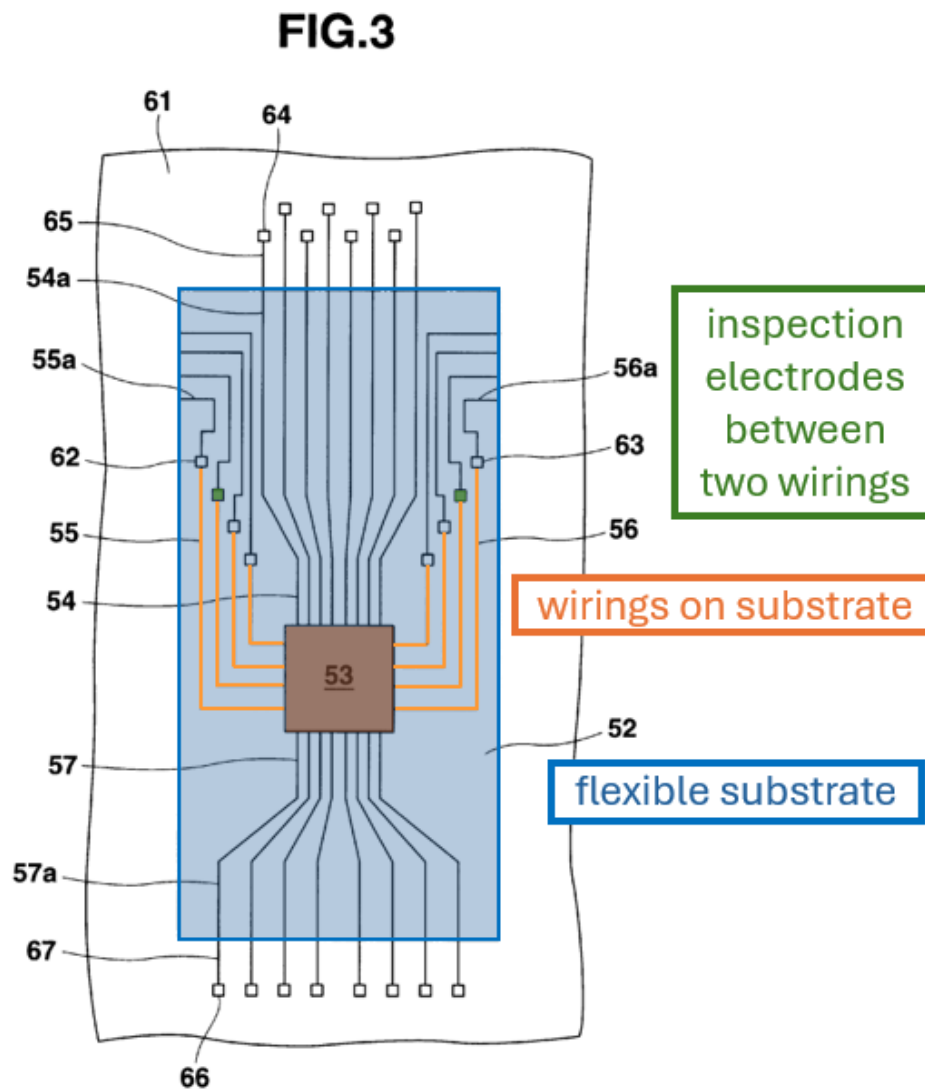
See Section VII.D.4 (Dependent Claim 3), *supra*.

9[f] “the inspection electrode being disposed between one of the plurality of wirings and another one of the plurality of wirings, wherein the integrated circuit is electrically connected to at least one of the plurality of wirings.”

Taguchi discloses (or at least suggests) the recited “inspection electrode disposed between one of the plurality of wirings and another one of the plurality of wirings...” as seen with “test pad 16-2” in Figure 7 which is shown below to be disposed between two different wirings, one of which is electrically connected to the integrated circuit 6-1 (*also* Ex.1006, ¶[0055]; Ex.1001, ¶[230]):



In the event Patent Owner argues that Taguchi does not disclose this element, Saito also teaches “the inspection electrode being disposed between one of the plurality of wirings and another one of the plurality of wirings.” As shown in FIG. 3 below, Saito teaches that “[t]est pads 62 and 63 are formed in middle portions of output lead wires 55 and 56 on the upper surface of the film wiring board 52 . . . the test pads 62 and 63 are respectively arranged at regular intervals on the same lines” including between adjacent “output lead wires.” (Ex.1004, 5:31-35.)



Arranging test electrodes between pairs of signal lines or wirings as shown in Figure 3 of Saito above was a well-known practice in the field of flexible printed circuits as of the priority date of the '512 patent.

A POSITA would know that, as source driver ICs for high-resolution display panels continue to increase in complexity and pin count, efficient layout and testing methodologies become critical. In particular, edge real estate on a substrate is limited, especially in high-pin-count devices where the periphery is densely populated with I/O pads. By placing the test electrode between internal signal wires as taught in Saito (and at least suggested in Taguchi), valuable edge space can be reserved for essential I/O functions, enabling more compact and efficient substrate designs. Moreover, locating the test electrode closer to the internal circuitry by placing it between wires can minimize the length of the signal path from the IC under test to the test pad. This reduction in path length can decrease parasitic capacitance and inductance, improving signal fidelity during high-speed testing and reducing the risk of signal degradation or crosstalk. A POSITA would also understand that internal placement of the test electrode allows for greater flexibility in routing and pad assignment, which is particularly advantageous as pin pitch decreases and the number of required connections increases. This can simplify the overall layout and facilitate the integration of additional test features. (Ex.1002, ¶¶231-235.)

In sum, a POSITA would be motivated to place a test electrode between wires on a substrate (as taught by Taguchi and Saito), rather than at the edge, because doing so enables more efficient use of substrate area, improves signal integrity, and enhances layout flexibility, all of which are increasingly important in high-density, high-performance semiconductor devices. (*Id.*)

Regarding the integrated circuit being “electrically connected to at least one of the plurality of wirings,” Taguchi and Saito each discloses this limitation. *See* Section VIII.D.2 (Claim 1[d]), *supra*.

Therefore, Taguchi and Her, in view of Saito, render independent claim 9 of the ’512 patent obvious. (Ex.1002, ¶¶224-235.)

3. Independent Claim 10

10[pre] “A flexible substrate comprising:”

See Claim 9[pre], *supra*.

10[a] “a substrate body;”

See Claim 9[a], *supra*.

10[b] “a plurality of wirings...;”

See Claim 9[b], *supra*.

10[c] “a plurality of connection terminals...;”

See Claim 9[c], *supra*.

10[d] “an inspection electrode...;”

See Claim 9[d], *supra*.

10[e] “the inspection electrode being disposed....”

See Claim 9[f], supra.

In sum, Taguchi and Her, in view of Saito, render independent claim 10 of the '512 patent obvious. (Ex.1002, ¶¶236-242.)

4. Dependent Claim 11

An electro-optical device comprising: the flexible substrate according to claim 10; and an electro-optical panel that is electrically connected to the flexible substrate via at least one of the plurality of connection terminals.

As discussed previously, the combination of Taguchi and Her renders claim 10 obvious. Regarding the additional limitation of Claim 11 that “an electro-optical panel that is electrically connected to the flexible substrate via at least one of the plurality of connection terminals,” Taguchi discloses this limitation. (See Section VIII.D.7 (Dependent Claim 6), *supra*; Ex.1002, ¶¶243-247.)

F. Ground 6: Claims 2, 7 and 12 Are Obvious over Taguchi and Her, in further view of Saito and Kim

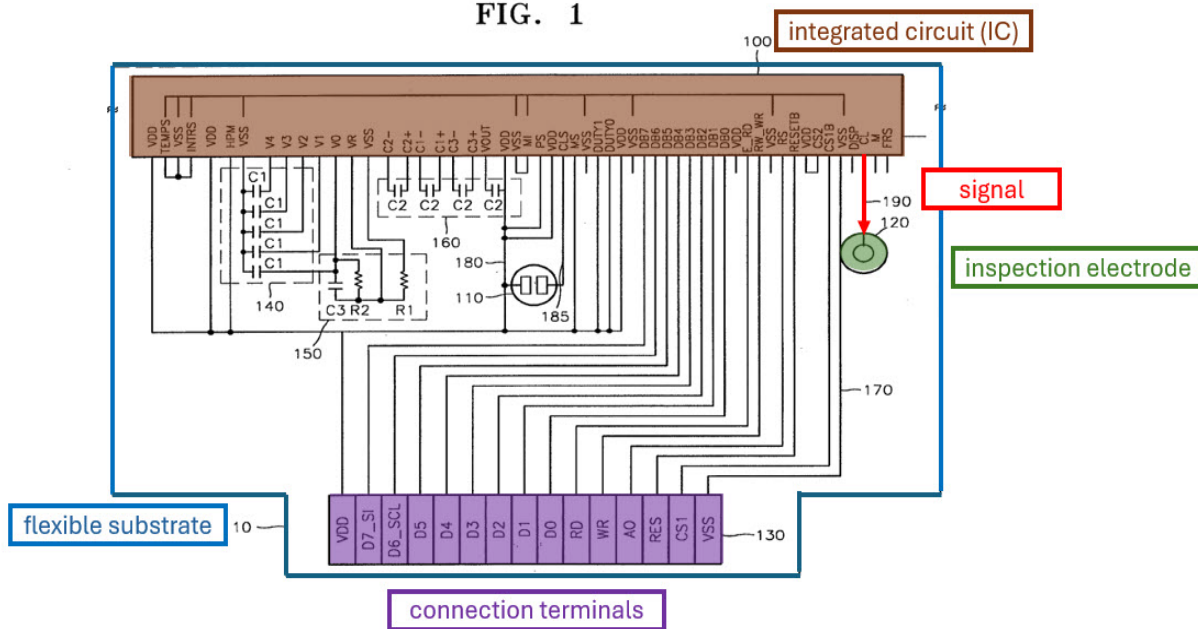
1. Dependent Claim 2

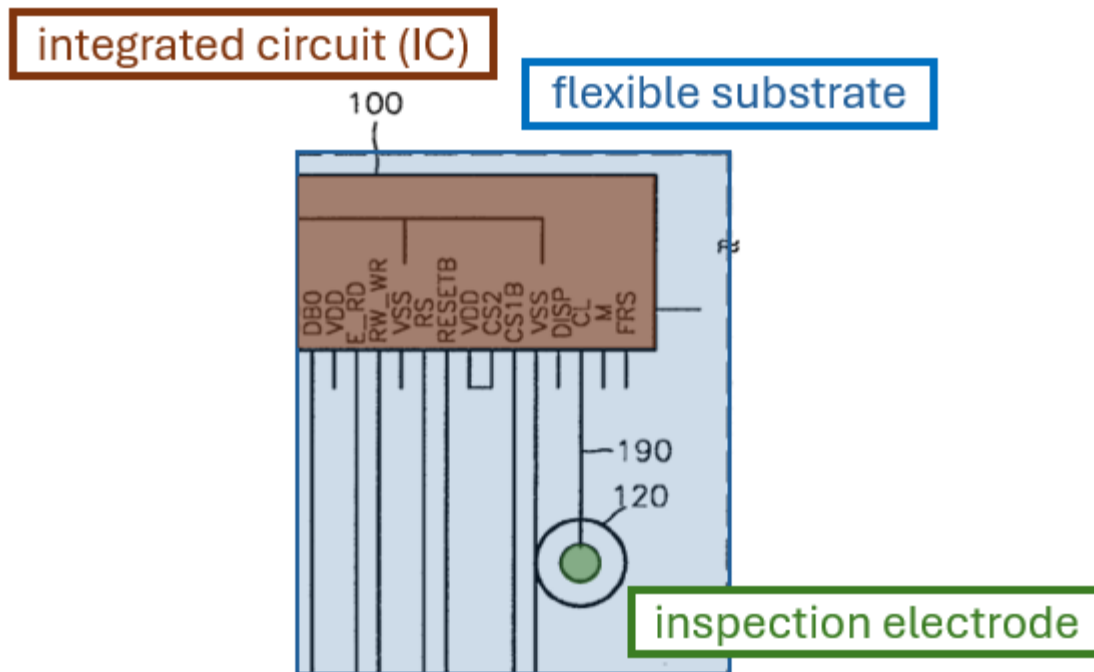
The flexible substrate according to claim 1, wherein the inspection electrode outputs a signal that is not input to or output from the integrated circuit through the plurality of connection terminals.

As discussed previously, the combination of Taguchi and Her renders claims 1 and 2 obvious. To the extent Patent Owner argues that this combination does not teach an inspection electrode that outputs a signal that is not output “through the plurality of connection terminals” as recited in claim 2, Kim teaches this limitation.

Kim discloses a detailed example of an integrated circuit mounted on a flexible substrate that includes an enlarged “test pad 120” that is nearly identical to the test electrode taught in Taguchi. (Ex.1005, ¶[0040].) Kim expressly teaches inclusion of a test electrode on the substrate that “do[es] not lead to the outside of the COF package 10” (*id.*, ¶[0031]) and thereby is able to “test the electrical functions of terminals of the chip package which do not lead to the outside of the chip package” (*id.*, ¶[0033]) as seen below from Figure 1:

FIG. 1





Specifically, test pad 120 outputs a CL signal connected through CL signal line 190 to the CL terminal. Unlike other terminals on the IC (*e.g.*, D0–D5), the CL signal is not first supplied to the IC from an input connection terminal. Thus, test pad 120 outputs a signal (CL signal) that is not previously input to the integrated circuit (chip 100) through the connection terminals (signal input portion 130). (Ex.1002, ¶¶248-253.)

In sum, Kim expressly teaches using a substrate-mounted driver IC with an enlarged test electrode (such as disclosed in Taguchi) to output a signal that is not input to or output from the IC through any external connection terminal (such as the test signal from Her). (Ex.1002, ¶¶248-251; *also* Ex.1005, Figures 1 and 2.)

A POSITA would understand that as ICs become more complex, ensuring the functional integrity of internal nodes and signal paths such as the composite “test signal” taught in Her is critical for both yield and long-term reliability. A POSITA thus would be motivated to employ a substrate-only electrode like that disclosed in Kim on the substrate of Taguchi in order to detect test signals originating in the IC and not sent to the LCD panel, such as the composite signal taught in Her. By providing a substrate-only test electrode connected for such a signal, it becomes possible to directly monitor, stimulate, or measure these signals during wafer-level or final testing. Moreover, a POSITA would understand that substrate-only test electrodes allow for more comprehensive test coverage, including the ability to isolate and diagnose faults within specific blocks or signal paths. Therefore, it would have been obvious to a POSITA to combine the approach taught in Kim with Taguchi and Her, namely, modifying one or more test pad structures taught in Taguchi to terminate on the substrate to monitor test signals created internally by the IC (such as the composite test signal from Her) that are not sent to the LCD panel. (Ex.1002, ¶252.)

Therefore, claim 2 also is obvious over Taguchi and Her, in further view of Kim. (Ex.1002, ¶¶248-253.)

2. Dependent Claims 7 and 12

*An electronic device comprising the electro-optical device
according to claim 6 / 11*

As discussed previously, the combination of Taguchi and Her renders claim 6 obvious. *See* Section VIII.D, *supra*. And the combination of Taguchi and Her, in view of Saito, renders claim 11 obvious. *See* Section VIII.E, *supra*. Those combinations, in view of Kim, also respectively render dependent claims 7 and 12 obvious.

It would be obvious to a POSITA to use the electro-optical device of claims 6 and 11 in an electronic device. Like Taguchi (and Her and Saito), Kim describes “integrated circuit (IC) packages for LCDs” (Ex.1005, ¶[0005]) each “mounted on a base film” substrate (*id.*, ¶[0011]). Kim simply makes explicit what is implicit in Taguchi, namely, “employing a liquid crystal device (LCD)” such as disclosed in Taguchi “**in various electronic devices** such as laptop computers (notebook computers), mobile phones, watches, and measuring instruments and apparatuses.” (*Id.*, [0006].) Indeed, the electro-optical device of claims 6 and 11 would serve little purpose if not ultimately employed in an electronic device.

Therefore, claims 7 and 12 also are rendered obvious by the combination of Taguchi and Her (and Saito), in view of Kim. (Ex.1002, ¶¶254-258.)

IX. SECONDARY CONSIDERATIONS

Petitioner is not aware of any secondary considerations that would overcome the strong showing of obviousness provided by the Petition. (Ex.1002, ¶259).

Further, any attempt by Patent Owner to rely on alleged secondary considerations cannot overcome the showing of obviousness detailed above. *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1370 (Fed. Cir. 2011).

X. CONCLUSION

For the above reasons, claims 1-12 of the '512 are unpatentable and should be canceled.

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Respectfully submitted,

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(D)

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this *Petition for Inter Partes Review* totals 13,908, excluding the parts exempted by 37 C.F.R. §42.24(a).

The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: August 30, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of this **PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,319,512** and supporting materials have been served by FedEx® delivery service on Patent Owner at the correspondence address for the attorney of record for the '512 Patent shown in USPTO records:

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