UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, *vs*. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.; AVNET, INC., Defendants.	Case No. 2:25-cv-557-JRG **JURY TRIAL DEMANDED** (Lead Case)
NETLIST, INC., Plaintiff, *vs*. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC; AVNET, INC., Defendants.	Case No. 2:25-cv-558-JRG **JURY TRIAL DEMANDED** (Member case)

SAMSUNG DEFENDANTS' P.R. 3-3 INVALIDITY CONTENTIONS

Netlist EX2016
Samsung v. Netlist
IPR2025-01431

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Pursuant to the Docket Control Order (Dkt. No. 29) and Local Patent Rule 3-3, Defendants Samsung Electronics Co., Ltd., ("SEC"), Samsung Electronics America, Inc., ("SEA"), Samsung Semiconductor, Inc., ("SSI") (collectively, "Defendants") hereby provide their Invalidity Contentions, which include the accompanying claim charts concerning U.S. Patent Nos. 12,308,087 (the "'087 Patent") and 10,025,731 (the "'731 Patent") (collectively, the "Asserted Patents") to Plaintiff Netlist, Inc., ("Netlist" or "Plaintiff").

The citation of prior art herein and the accompanying exhibits are not intended to reflect Defendants' claim construction contentions, which will be disclosed in due course in accordance with the Docket Control Order and may instead reflect Plaintiff's apparent (and potentially erroneous) claim constructions based on its Infringement Contentions.

1. Introduction

As disclosed in its P.R. 3-1 Infringement Contentions served on Defendants, Plaintiffs assert the following patents and claims:

	Claims
'087 Patent	1–28 (Independent claims 1, 9, 13, 20, 23, 24)
'731 Patent	1–18 (Independent claim 1)

The claims identified above are referred to as "the Asserted Claims" unless reference is made specifically with respect to particularly identified one or more of the Asserted Claims.

As further detailed in and supported by these Invalidity Contentions, Defendants contend that each of the Asserted Claims is invalid at least under 35 U.S.C. §§ 101, 102, 103, 112, and/or

115.[1] Defendants reserve the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures pursuant to P.R. 3-3.

2. Amendment / Supplementation

Defendants' Invalidity Contentions pertain to the Asserted Claims as identified in Plaintiff's Infringement Contentions. To the extent the Court later allows Plaintiff to amend its infringement contentions and/or assert one or more claims other than the Asserted Claims, Defendants reserve the right to modify, amend, or supplement these Invalidity Contentions accordingly to, for example, show the invalidity of any such newly Asserted Claims.

These Invalidity Contentions are based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. A *Markman* Order in this case has not yet been issued, and these Invalidity Contentions shall not be understood as any admission or acquiescence by Defendants as to the proper scope of the Asserted Claims and/or proper claim constructions of terms and phrases recited in those claims. By identifying prior art that anticipates and/or renders obvious the Asserted Claims, Defendants do not admit that the claim limitations are capable of construction, does not admit that any claim limitations are supported with an appropriate written description and enabling disclosure in the applicable patent specifications, and does not adopt Plaintiff's apparent claim constructions or admit the accuracy of any particular claim

[1] References to Title 35 of the United States Code are to statutes before amendment under the America Invents Act ("AIA"), as the Asserted Patents claim effective filing dates before the applicable AIA effective date.

construction.[2] Defendants reserve all rights to later challenge or oppose any claim constructions advanced by Plaintiff and to present their own claim construction positions.

Defendants further reserve the right to revise these Invalidity Contentions in view of the Court's construction of terms and phrases recited in one or more of the Asserted Claims, additional information obtained during discovery, additional infringement theories put forth by Plaintiff during fact and/or expert discovery, any findings as to the priority date(s) of the Asserted Claims, and/or positions that Plaintiff, its fact witnesses, or its expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Defendants further reserve the right to supplement these Invalidity Contentions and the accompanying P.R. 3-4(b) document production should Defendants later discover additional prior art documents, information, testimony, prior art products and related documentation, and/or software or hardware code, including information provided by third parties after the date of service of these Invalidity Contentions.

Defendants may further rely on inventor admissions concerning the scope or state of the prior art relevant to the Asserted Claims, the patent prosecution histories of the Asserted Patents, related patents and/or patent applications, any deposition or trial testimony of the named inventors on the Asserted Patents, and the papers filed and any evidence produced or submitted by Plaintiff in connection with these cases or other related litigation.

[2] Defendants does not concede that Plaintiff's apparent interpretation of the claims is correct, but rather relies on the well-established principle that whatever infringes a claim if later in time anticipates if earlier in time. *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). Thus, where Plaintiff for purposes of its infringement case alleges that a feature of an accused product meets a particular limitation recited in one or more of the Asserted Claims, then that feature, should it be found in the prior art, would also cause that limitation to be met for invalidity purposes. *See also 01 Communique Lab., Inc. v. Citrix Sys., Inc.*, 889 F.3d 735, 742 (Fed. Cir. 2018).

Prior art not included in these Invalidity Contentions, whether known or not known to Defendants, may become relevant. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified in these Invalidity Contentions. Accordingly, Defendants reserve the right to identify other references that would disclose the allegedly missing limitation(s) of the claimed method, device, or system.

The references identified in these Invalidity Contentions, which include the attached claim charts, may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. References identified in these Invalidity Contentions, as well as the "References Cited" on the face of the Asserted Patents and the patents cited within the body of the Asserted Patents, may be used to illustrate, but not limit the scope of, the state of the art to which the Asserted Patents pertains (i.e., at a time prior to the date of alleged inventions and/or the alleged filing date of the Asserted Patents). Moreover, Defendants reserve the ability to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

Because discovery has just recently begun, Defendants anticipate that additional prior art and invalidity bases may be found. Defendants' investigation and analysis of the prior art is continuing, and thus Defendants reserve the right to supplement, amend, and/or revise the information provided herein as Defendants conduct further investigation and/or analysis, including identifying, charting, and relying on additional references.

Additionally, in view of likely third-party discovery that will be taken, Defendants reserve the right to present additional items of prior art under 35 U.S.C. § 102 and/or § 103 located during

discovery or further investigation. For example, Defendants expect to issue subpoenas to third parties believed to have knowledge, documents, and/or other evidence concerning invalidity of one or more of the Asserted Claims.

In addition to the positions and prior art identified in these Invalidity Contentions (including the accompanying invalidity claim charts), Defendants also incorporate by reference all Invalidity Contentions, prior art,[3] and invalidity claim charts (including, without limitation, all anticipation positions, obviousness positions (including all prior art combinations and motivations to combine), indefiniteness positions, written description positions, and non-enablement positions) concerning the Asserted Patents, and corresponding limitations from related patents, as disclosed at any time. This includes without limitation disclosures in previous or related litigation, in United States Patent & Trademark Office ("USPTO") proceedings, by the Plaintiff, or by the named inventors or any individuals associated with the prosecution, *ex parte* reexaminations, *inter partes* review, and/or post-grant review of the Asserted Patents.

Specifically, for example, Defendants identify, as prior art upon which they may rely to show the invalidity of the Asserted Claims, the prior art references disclosed by parties in any other litigation involving the Asserted Patents, any patent related to any of the Asserted Patents, and/or any other patent allegedly assigned to Plaintiff claiming priority to the Asserted Patents (collectively, "Other Netlist Proceedings"). To the extent that any Defendant has stipulated or stipulates in the future that it will not pursue certain invalidity grounds in these actions concerning patent claims subject to post grant review or *inter partes* review proceedings, the relevant Defendant(s) will abide by those stipulation(s), and nothing in these contentions should be read as

[3] Prior art appearing in the file histories of the Asserted Patents is not required to be separately produced by Defendants under P.R. 3-4(b).

suggesting otherwise. Rather, these contentions are intended to put Plaintiff on notice of the grounds of invalidity, within the scope of P.R. 3-3, that one or more Defendants may assert in these actions, including because the conditions of any relevant stipulation are not met (e.g., if the corresponding *inter partes* review is not instituted) or because the grounds fall outside the scope of such stipulations.

Likewise, while Defendants will abide by any orders or guidance provided by the Court regarding the extent to which any stipulations preclude certain references or combinations of references, Defendants note that the law regarding whether "Admitted Prior Art" and JEDEC-related references may be used in an inter partes review is subject to cases pending before the Federal Circuit and the Patent Trial and Appeal Board. See Br. of Appellant Qualcomm Incorporated at 13, *Qualcomm Inc. v. Apple Inc.*, No. 23-1208 (Fed. Cir. March 20, 2023) ("Did the Board err in interpreting Section 311(b) to permit Apple's Ground 2, which consists of so-called applicant admitted prior art (AAPA) in view one or more prior art patents or printed publications?"); Transcript of Record of Oral Hearing at 19-32, IPR2022-00062, IPR2022-00064 (P.T.A.B. March 8, 2023) (discussing whether certain JEDEC-related references constitute "printed publications"). Further developments regarding the law may impact the Court's prior orders and guidance regarding Defendants' stipulations.

Plaintiff has a duty to produce to Defendants all relevant documents from the Other Netlist Proceedings including but not limited to all prior art, Invalidity Contentions, and expert reports on invalidity (among other relevant items).

Defendants reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any relevant discovery provided by third parties, Plaintiff, opening or rebuttal expert reports, fact or expert depositions, or in response to any claim construction ruling(s)

issued by this Court (regardless of how and when such ruling is made). Defendants also reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any rebuttal evidence disclosed by Plaintiff or as otherwise may be necessary or appropriate under the circumstances.

3. Priority Date

Defendants' disclosure of prior art is premised on the alleged priority dates of the Asserted Patents as identified in Plaintiff's Infringement Contentions. Defendants contend Plaintiff is not entitled to the alleged priority dates and reserve the right to modify, amend, or supplement their invalidity contentions with additional prior art references if any Asserted Claim is shown to not be entitled to the respective alleged priority date or if Plaintiff alleges any other priority date for any of the Asserted Claims. Notwithstanding that reservation of rights, Defendants also reserve the right to argue that they have been unduly prejudiced should Plaintiff allege a different priority date for any of the Asserted Claims, and that accordingly Plaintiff should not be allowed to do so.

3.1. '087 Patent

Plaintiff alleges that the Asserted Claims of the '087 Patent are entitled to a priority date of at least November 2, 2010 based on a domestic priority claim to U.S. Provisional Application No. 61/409,893 (the "'893 Provisional"). Despite facially claiming priority to the '893 Provisional, "[f]or a patent to claim priority from the filing date of its provisional application, it must satisfy 35 U.S.C. § 119(e)(1)." *Dynamic Drinkware, LLC v. Nat. Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). That is, "the specification of the *provisional* must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶ 1, to enable an ordinarily skilled artisan to practice the invention *claimed* in the *non-provisional* application." *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294 (Fed. Cir. 2002) (emphasis in original). As discussed below, none of the

claims of the ’087 patent have written description support in any previous application, much less the ’893 Provisional, and thus the ’087 Patent is not entitled to its claimed November 2, 2010 priority date.

The ’893 Provisional includes just 14 paragraphs and 3 figures, a small fraction of the disclosure in non-provisional Application No. 13/288,850 (the “’850 Application”), which was filed on November 3, 2011 and includes 13 paragraphs and 8 figures. The ’893 Provisional does not include the following written description and figures of the ’087 patent:

- Figures 1-5
- 1:5-3:41, 3:65-17:63, 20:18-22:42, portions of 17:65-20:17

Non-exhaustive examples of claim limitations that lack written description support in the ’893 Provisional include limitations reciting: (1) die interconnects (including through-silicon vias or TSVs), (2) signal conduits, including data conduits, command conduits, and address conduits, (3) selective communication of die interconnects or conduits, (4) directionality of die interconnects or conduits, (5) absence of or prohibition on chip select signals, (6) absence of or prohibition on emulation logics, and (6) stacking of more than 8 DRAM dies.

Because the ’893 Provisional Plaintiff relies on for its alleged priority date for the Asserted Claims of the ’087 patent lacks support for many claim limitations, Plaintiff is not entitled to its alleged November 3, 2010 priority date.

The ’087 Patent is also not entitled to the priority date of the earliest Non-Provisional application in this family No. 13/288,850 (now U.S. Patent No. 8,787,060). For example, as explained below, the ’060 Patent lacks written description support for at least the following claim limitations: separate data and control terminals, receiving “signals associated with” memory read operations via “unidirectional interconnects,” sets of C/A interconnects in electrical

communication with less than all dies in the stack, and C/A signals lacking "any chip select signal." Notably: because the '087 Patent is not entitled to allege priority to the '060 Patent, and the '060 Patent issued more than one year before the '087 Patent was filed, the '060 Patent is 102(b) prior art to the '087 Patent and renders obvious the Asserted Claims in combination with the knowledge of one of ordinary skill in the art and/or the references identified in Appendix A.

3.2. '731 Patent

Plaintiff alleges that the Asserted Claims of the '731 Patent are entitled to a priority date of April 14, 2008 based on a domestic priority claims to U.S. Provisional Application Nos. 61/044,839, 61/044,825, and 61/044,801.

4. P.R. 3-3(a) – Identification of Prior Art

Pursuant to P.R. 3-3(a), and subject to Defendants' reservation of rights, Defendants identify the prior art references below.

4.1. '087 Patent

Invalidity claim charts identifying disclosures in the references identified in Tables 1-A and 2-A as to the Asserted Claims of the '087 Patent are provided in attached Exhibits A-1 through A-22 and A-OO.

Table 1-A: Prior Art Patents and Printed Publications for the '087 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-1	'087 Patent's Admitted Prior Art ('087 APA)		
A-2	U.S. Patent No. 9,123,552 (Keeth '552)	Sept. 1, 2015	Mar. 30, 2010
A-3	U.S. Patent No. 9,665,507 (Shaeffer '507)	May 30, 2017	May 11, 2011
A-4	U.S. Patent App. Pub. No. 2010/0195364 (Riho '364)	Aug. 5, 2010	Feb. 1, 2010
A-5	U.S. Patent App. Pub. No. 2011/0103156 (Kim '156)	May 5, 2011	Dec. 29, 2009
A-6	U.S. Patent No. 8,041,881 (Rajan '881)	Oct. 18, 2011	June 12, 2007

Table 1-A: Prior Art Patents and Printed Publications for the '087 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-7	U.S. Patent No. 8,471,362 (Lee '362)	June 25, 2013	April 5, 2011
A-8	U.S. Patent No. 7,969,192 (Wyman '192)	June 28, 2011	Mar. 26, 2010
A-9	U.S. Patent App. Pub. No. 2008/0025137 (Rajan '137)	Jan. 31, 2008	July 31, 2006
A-10	U.S. Patent No. 9,142,262 (Ware '262)	Sept. 22, 2015	Sept. 24, 2010
A-11	U.S. Patent App. Pub. No. 2010/0091537 (Best '537)	Apr. 15, 2010	Dec. 13, 2007
A-12	U.S. Patent No. 8,258,619 (Foster '619)	Sept. 4, 2012	Nov. 12, 2009
A-13	U.S. Patent App. Pub. No. 2010/0110745 (Jeddeloh '745)	May 6, 2010	Oct. 30, 2008
A-14	U.S. Patent App. Pub. No. 2011/0208906 (Gillingham '906)	Aug. 25, 2011	Dec. 14, 2010
A-15	U.S. Patent No. 8,120,958 (Bilger '958)	Feb. 21, 2012	Dec. 24, 2007
A-16	U.S. Patent No. 9,160,349 (Ma '349)	Oct. 13, 2015	Aug. 27, 2009
A-17	U.S. Patent No. 7,796,446 (Ruckerbauer '446)	Sept. 14, 2010	Sept. 19, 2008
A-18	Gabriel H. Loh, 3D-Stacked Memory Architectures for Multi-Core Processors, Georgia Institute of Technology, International Symposium on Computer Architecture (2008) (Loh2008)	June 2008	
A-19	U.S. Patent No. 7,830,692 (Chung '692)	Nov. 9, 2010	Sept. 26, 2008
A-20	U.S. Patent No. 8,582,373 (Hollis '373)	Nov. 12, 2013	Aug. 31, 2010
A-OO	Admitted prior art ("APA") described in '087 Patent		
A-OO	U.S. Patent No. 7,830,692 (Chung '692)	Nov. 9, 2010	Sept. 26, 2008
A-OO	U.S. Patent App. Pub. No. 2009/0103374 (Han '374)	Apr. 23, 2009	Dec. 8, 2008
A-OO	U.S. Patent No. 7,796,446 (Ruckerbauer '446)	Sept. 14, 2010	Sep.19, 2008
A-OO	U.S. Patent No. 7,698,470 (Ruckerbauer '470)	Apr. 13, 2010	Aug. 6, 2007
A-OO	U.S. Patent No. 7,397,684 (Ruckerbauer '684)	July 8, 2008	Sept.15, 2005
A-OO	U.S. Patent No. 8,031,539 (Gregorius '539)	Oct. 4, 2011	Oct. 9, 2008
A-OO	U.S. Patent No. 8,120,958 (Bilger '958)	Feb. 21, 2012	Dec. 24, 2007

Table 1-A: Prior Art Patents and Printed Publications for the '087 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-OO	U.S. Patent App. Pub. No. 2011/0103156 (Kim '156)	May 5, 2011	Dec. 29, 2009
A-OO	U.S. Patent No. 7,817,491 (Kwak '491)	Oct. 19, 2010	Jun. 30, 2008
A-OO	U.S. Patent No. 8,031,505 (Kang '505)	Oct. 4, 2011	May 12, 2009
A-OO	U.S. Patent No. 8,743,582 (Kang '582)	June 3, 2014	May 25, 2011
A-OO	U.S. Patent No. 8,659,136 (Youn '136)	Feb. 25, 2014	Feb. 25, 2010
A-OO	U.S. Patent No. 9,502,345 (Youn '345)	Nov. 22, 2016	Feb. 15, 2010
A-OO	U.S. Patent App. Pub. No.2009/0180257 (Park '257)	July 16, 2009	Jan. 13, 2009
A-OO	U.S. Patent No. 8,030,208 (Leung '208)	Oct. 4, 2011	June 2, 2008
A-OO	U.S. Patent No. 7,409,491 (Doblar '491)	Aug. 5, 2008	Dec. 14, 2005
A-OO	U.S. Patent No. 8,582,373 (Hollis '373)	Nov. 12, 2013	Aug. 31, 2010
A-OO	U.S. Patent No. 8,779,849 (Hollis '849)	July 15, 2014	Jan. 27, 2012
A-OO	U.S. Patent No. 9,116,828 (Hollis '828)	Aug. 25, 2015	June 11, 2008
A-OO	U.S. Patent No. 7,623,365 (Jeddeloh '365)	Nov. 24, 2009	Aug. 29, 2007
A-OO	U.S. Patent No. 8,977,809 (Johnson '809)	Mar. 10, 2015	Nov. 26, 2008
A-OO	U.S. Patent No. 7,855,931 (LaBerge '931)	Dec. 21, 2010	July 21, 2008
A-OO	U.S. Patent No. 7,763,496 (Ikeda '496)	July 27, 2010	Feb. 21, 2007
A-OO	U.S. Patent No. 8,084,854 (Pratt '854)	Dec. 27, 2011	Dec. 28, 2007
A-OO	U.S. Patent No. 6,292,877 (Ryan '877)	Sept. 18, 2001	Nov. 5, 1999
A-OO	U.S. Patent No. 8,675,420 (Tanzawa '420)	Mar. 18, 2014	May 26, 2011
A-OO	U.S. Patent No. 8,127,204 (Hargan '204)	Feb. 28, 2012	Aug. 15, 2008
A-OO	U.S. Patent No. 8,996,836 (Ito '836)	Mar. 31, 2015	Dec. 18, 2009
A-OO	U.S. Patent No. 9,123,552 (Keeth '552)	Sept. 1, 2015	Mar. 30, 2010
A-OO	U.S. Patent App. Pub. No. 2007/0028027 (Janzen '027)	Feb. 1, 2007	July 26, 2005
A-OO	U.S. Patent No. 8,432,027 (Foster '027)	Apr. 30, 2013	Nov. 11, 2009
A-OO	U.S. Patent App. Pub. No. 2009/0150636 (Gower '636)	June 11, 2009	Feb. 11, 2009
A-OO	U.S. Patent No. 7,441,060 (Gower '060)	Oct. 29, 2004	Oct. 29, 2004
A-OO	U.S. Patent No. 7,899,983 (Gower '983)	Mar. 1, 2011	Aug. 31, 2007

Table 1-A: Prior Art Patents and Printed Publications for the '087 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-OO	U.S. Patent No. 7,717,752 (Loughner '752)	May 18, 2010	July 1, 2008
A-OO	U.S. Patent No. 7,305,574 (Ferraiolo '574)	Dec. 4, 2007	Oct. 29, 2004
A-OO	U.S. Patent App. Pub. No. 2010/0121994 (Kim '994)	May 13, 2010	Nov. 10, 2008
A-OO	U.S. Patent No. 7,356,737 (Cowell '737)	Apr. 8, 2008	Oct. 29, 2004
A-OO	Korean Patent Pub. No. KR 2010-0066849 (Chung '849)	June 18, 2010	Dec. 10, 2007
A-OO	U.S. Patent No. 8,112,680 (Chung '680)	Feb. 7, 2012	Mar. 7, 2008
A-OO	U.S. Patent No. 8,384,417 (Laisne '417)	Feb. 26, 2013	Jun. 9, 2009
A-OO	U.S. Patent App. Pub. No. 2003/0090879 (Doblar '879)	May 15, 2003	June 14, 2002
A-OO	U.S. Patent No. 8,310,855 (Riho '855)	Nov. 13, 2012	July 16, 2010
A-OO	U.S. Patent App. Pub. No. 2011/0317495 (Ishikawa '495)	Dec. 29, 2011	June 8, 2011
A-OO	U.S. Patent App. Pub. No. 2012/0069685 (Ide '685)	Mar. 22, 2012	Sept. 16, 2011
A-OO	U.S. Patent No. 8,400,781 (Gillingham '781)	Mar. 19, 2013	Apr. 9, 2010
A-OO	U.S. Patent No. 8,866,303 (Kim '303)	Oct. 21, 2014	Apr. 9, 2010
A-OO	U.S. Patent App. Pub. No. 2010/0295600 (Kim '600)	Nov. 25, 2010	May 20, 2009
A-OO	U.S. Patent App. Pub. No. 2008/0183959 (Pelley '959)	July 31, 2008	Jan. 29, 2007
A-OO	U.S. Patent App. Pub. No. 2005/0166026 (Ware '026)	July 28, 2005	July 13, 2004
A-OO	U.S. Patent No. 7,404,032 (Ware '032)	July 22, 2008	July 13, 2004
A-OO	U.S. Patent No. 7,484,064 (Ware '064)	Jan. 27, 2009	Oct. 22, 2001
A-OO	U.S. Patent No. 9,287,239 (Ware '239)	Mar. 15, 2016	Apr. 13, 2011
A-OO	U.S. Patent No. 9,195,602 (Hampel '602)	Nov. 24, 2015	Mar. 19, 2008
A-OO	U.S. Patent App. Pub. No. 2007/0150667 (Bains '667)	June 28, 2007	June 28, 2007
A-OO	U.S. Patent App. Pub. No. 2011/0047318 (Dmitroca '318)	Feb. 24, 2011	Aug. 19, 2009

Table 1-A: Prior Art Patents and Printed Publications for the '087 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-OO	"Design Techniques to Facilitate Processor Power Delivery in 3-D Processor-DRAM Integrated Systems," by Qi Wu et al., IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 9, September 2011, published July 2010 (Wu 2010)	July 2010	
A-OO	"Impacts of though-DRAM vias in 3D processor-DRAM integrated systems," by Qi Wu et al., 2009 IEEE International Conference on 3D System Integration, Sep. 28-30, 2009 (Wu 2009)	Sept. 28-30, 2009	
A-OO	"Exploring a Low-Cost Inter-layer Communication Scheme for 3D Networks-on-Chip," by Amir-Mohammad Rahmani et al., 2010 15th CSI International Symposium on Computer Architecture and Digital Systems, Sep. 23-24, 2010 (Rahmani 2010)	Sept. 23-24, 2010	
A-OO	"Physical design for performance and thermal and power-supply reliability in modern 2d and 3d microarchitectures" Michael B. Healy Dissertation, Dec. 2010 (Healy 2010)	Dec. 2010	
A-OO	"Distributed TSV Topology for 3-D Power-Supply Networks," by Michael B. Healy et al., IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 20, Issue: 11), Oct. 13 2011 (Healy2011)	Oct. 13, 2011	
A-OO	"Low-Power Clock Tree Design for Pre-Bond Testing of 3-D Stacked ICs," by Xin Zhao et al., IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 30, No. 5, May 2011 (Zhao 2011)	May 2011	
A-OO	"Evolution, challenge, and outlook of TSV, 3D IC integration and 3d silicon integration," (Lau 2011)	2011	
A-OO	U.S. Patent No. 3,044,909, filed Oct. 23, 1958 ("Shokley '909")	July 17, 1962	Oct. 23, 1958

Table 2-A: Prior Art Systems and Inventions for the '087 Patent

No.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
A-21	JEDEC Proposals regarding High Bandwidth Memory (HBM) and Low Power Memories (JEDEC HBM and Low Power Proposals)	2008-2011
A-22	Micron LRDIMM System	Sept. 27, 2011

For each of the prior art devices identified above, Defendants have listed and produced one or more documents as evidence of the relevant features and functionality. Defendants have obtained or is in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (e.g., user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Discovery is ongoing, and Defendants may serve third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to the subject matter claimed in the '087 Patent. Defendants are producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendants reserve the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103 (including as evidence of motivation to combine or reasonable expectation of success), as background references

demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Netlist may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendants reserve the right to revise these contentions and to rely on these references to prove the invalidity of the '087 Patent in a manner consistent with this Court's guidance.

- U.S. Patent No. 7,024,518 (Halbert '518)
- U.S. Patent No. 7,286,436 (Bhakta '436)
- U.S. Patent No. 7,289,386 (Bhakta '386)
- U.S. Patent No. 7,532,537 (Solomon '537)
- U.S. Patent No. 7,545,663 (Ikeda '663)
- U.S. Patent No. 7,619,912 (Bhakta '912)
- U.S. Patent No. 7,664,216 (Schnarr '216)
- U.S. Patent No. 7,890,811 (Rothman '811)
- U.S. Patent No. 8,243,486 (Riho '486)
- U.S. Patent No. 8,244,971 (Rajan '971)
- U.S. Patent No. 8,593,899 (Ide '899)
- U.S. Patent Application Publication No. 2006/0259678 (Gervasi '678)
- U.S. Patent Application Publication No. 2006/0277355 (Ellsberry '355)
- U.S. Patent Application Publication No. 2010/0110748 (Best '748)
- U.S. Patent Application Publication No. 2011/0026293 (Riho '293)
- U.S. Patent Application Publication No. 2011/0193226 (Kirby '226)
- JEDEC JESD79 Standard for Double Data Rate (DDR) SDRAM (June 2000)
- JEDEC Graphics Double Data (GDDR3) Specific SGRAM Functions (May 2005)
- JEDEC Graphics Double Data (GDDR4) SGRAM Specification (Nov. 2005)

- JEDEC DDR3 SDRAM Standard, JESD79-3C (Nov. 2008)
- JEDEC MO-207, Square & Rectangular Die-Size, Ball Grid Array Family (Dec. 2010)
- GDDR5 SGRAM 1Gb (32Mx32) datasheet (Nov. 2009)
- JEDEC Ballot for 3D Stacked DDR3 SDRAM Addressing, Item No. 1655.10 (Sept. 2010)
- Harold S. Stone, Microcomputer Interfacing (1982) (Stone)
- Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
- Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
- Stephen Brown et al., *Fundamentals of Digital Logic* (2d ed. 2008)
- U. Kang *et al.*, *8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology*, IEEE Journal of Solid-State Circuits (Jan. 2010)

Each of these references show that the TSV/multi-die stack concepts claimed in the ’087 patent are not novel and were well-known for many years before the alleged priority date of the ’087 Patent. In light of the references discussed herein, the Asserted Claims of the ’087 Patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserves the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants’ reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the ’087 Patent. Defendants’ investigation of such prior art systems is still ongoing, and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may

reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third-party prior art systems anticipate and/or render obvious the Asserted Claims of the ’087 Patent. As such, Defendants reserve all rights to supplement its Invalidity Contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the ’087 Patent. Defendants have obtained, and are in the process of obtaining, additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be subject to third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants’ possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

4.2. ’731 Patent

Invalidity claim charts identifying disclosures in the references identified in Tables 1-B and 2-B as to the Asserted Claims of the ’731 Patent are provided in attached Exhibits B-1 through B-23.

Table 1-B: Prior Art Patents and Printed Publications for the '731 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
B-1	U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry '355)	Dec. 7, 2006	June 1, 2005
B-2	U.S. Patent No. 7,020,818 (Dour '818)	Mar. 28, 2006	Mar. 8, 2004
B-3	U.S. Patent App. Pub. No. 2008/0218290 (Abadeer '290)	Sep. 11, 2008	Feb. 27, 2007
B-4	U.S. Patent App. Pub. No. 2004/0222834 (Frans '834)	Nov. 11, 2004	May 9, 2003
B-5	U.S. Patent App. Pub. No. 2008/0089155 (Bae '155)	Apr. 17, 2008	Oct. 11, 2007
B-6	U.S. Patent App. Pub. No. 2007/0139071 (Nguyen '071)	Jan. 21, 2007	Dec. 19, 2005
B-7	U.S. Patent App. Pub. No. 2004/0228196 (Kwak '196)	Nov. 18, 2004	Mar. 3, 2004
B-8	U.S. Patent App. Pub. No. 2006/0106951 (Bains '951)	May 18, 2006	Nov. 18, 2004
B-9	U.S. Patent No. 7,646,213 (Kao '213)	Jan. 12, 2010	May 16, 2007
B-10	U.S. Patent No. 6,356,106 (Greeff '106)	Mar. 12, 2002	Mar. 12, 2002
B-11	U.S. Patent App. Pub. No. 2005/0135519 (Lee '519)	Jun. 23, 2005	Dec. 22, 2004
B-12	U.S. Patent App. Pub. No. 2005/0040845 (Park '845)	Feb. 24, 2005	Aug. 5, 2004
B-13	U.S. Patent App. Pub. No. 2009/0237109 (Haig '109)	Sep. 24, 2009	Mar. 24, 2008
B-14	U.S. Patent App. Pub. No. 2004/0100837 (Lee '837)	May 27, 2004	Nov. 18, 2003
B-15	U.S. Patent App. Pub. No. 2005/0225353 (Kwon '353)	Oct. 13, 2005	Dec. 9, 2003
B-16	U.S. Patent App. Pub. No. 2006/0158214 (Janzen '214)	Jul. 20, 2006	Jun. 20, 2005
B-17	U.S. Patent App. Pub. No. 2007/0279084 (Oh '084)	Dec. 6, 2007	Jun 2, 2006
B-18	U.S. Patent App. Pub. No. 2004/0098528 (Janzen '528)	May 20, 2004	Mar. 7, 2003

Table 1-B: Prior Art Patents and Printed Publications for the '731 Patent

No.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
B-19	U.S. Patent App. Pub. No. 2003/0039151 (Matsui '151)	Aug. 23, 2002	Feb. 27, 2003
B-20	U.S. Patent App. Pub. No. 2003/0126338 (Dodd '338)	Jul. 3, 2003	Dec. 31, 2001
B-21	U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320)	Jan. 8, 2009	Jul. 2, 2007
B-22	U.S. Patent App. Pub. No. 2007/012646 (Vergis '464)	Jun. 7, 2007	Dec. 7, 2005
B-23	U.S. Patent No. 8,391,347 (Kim '347)	Mar. 5, 2013	Oct. 30, 2008
B-24	U.S. Patent No. 7,253,655 ("Kwon '655") U.S. Patent No. 7,624,244 ("Yung '244") U.S. Patent No. 6,493,250 ("Halbert '250") U.S. Patent No. 6,658,509 ("Bonella '509") U.S. Patent No. 8,924,680 ("Perego '680") U.S. Patent No. 7,363,422 ("Perego '422") U.S. Patent No. 6,947,304 ("Yen '304") U.S. Patent No. 6,529,422 ("Mazumder '422")	Aug. 7, 2007 Nov. 24, 2009 Dec. 10, 2002 Dec. 2, 2003 Dec. 30, 2014 Apr. 22, 2008 Sep. 20, 2005 Mar. 4, 2003	Sep. 1, 2005 Jun. 22, 2007 Dec. 28, 2000 Oct. 3, 2000 Apr. 11, 2008 Jan. 28, 2004 May 12, 2003 Aug. 30, 2001
B-27	U.S. Patent No. 7,227,376 ("Ahmad '376")	Jun. 5, 2007	Nov. 5, 2004

Table 2-B: Prior Art Systems and Inventions for the '731 Patent

No.	Name of System or Invention	Date of Sale / Offer for Sale / Public Use
B-25	JESD79-2 DDR2 SDRAM Specification Micron TN-49-01 RLDRAM 2 Design Guide	Sep. 2003 2004
B-26	Samsung DDR2 Fully Buffered DIMM Samsung 512Mb E-die DDR2 SDRAM Specification JESD79-2 DDR2 SDRAM Specification JESD82-20 FBDIMM Advanced Memory Buffer Specification	Jan. 2008 Jul. 2007 Sep. 2003 Mar. 2007

For each of the prior art devices identified above, Defendants have listed and produced one or more documents as evidence of the relevant features and functionality. Defendants have

obtained or is in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (e.g., user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Discovery is ongoing, and Defendants may serve third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to the subject matter claimed in the '731 Patent. Defendants are producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendants reserve the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103 (including as evidence of motivation to combine or reasonable expectation of success), as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Netlist may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendants reserve the right to revise these contentions and to rely on these references to prove the invalidity of the '731 Patent in a manner consistent with this Court's guidance.

- U.S. Patent No. 4,739,283 (Metz '283)

- U.S. Patent No. 5,513,135 (Dell ’135)
- U.S. Patent No. 5,630,096 (Zuravleff ’096)
- U.S. Patent No. 5,774,505 (Baugh ’505)
- U.S. Patent No. 5,784,705 (Leung ’705)
- U.S. Patent No. 5,831,467 (Leung ’467)
- U.S. Patent No. 5,905,401 (Sher ’401)
- U.S. Patent No. 6,011,710 (Wiggers ’710)
- U.S. Patent No. 6,070,217 (Connolly ’217)
- U.S. Patent No. 6,157,688 (Tamura ’688)
- U.S. Patent No. 6,209,074 (Dell ’074)
- U.S. Patent No. 6,308,232 (Gasbarro ’232)
- U.S. Patent No. 6,356,105 (Volk ’105)
- U.S. Patent No. 6,377,637 (Berdugo ’637)
- U.S. Patent No. 6,442,644 (Gustavson ’644)
- U.S. Patent No. 6,493,394 (Tamura ’394)
- U.S. Patent No. 6,538,951 (Janzen ’951)
- U.S. Patent No. 6,587,912 (Leddige ’912)
- U.S. Patent No. 6,683,372 (Wong ’372)
- U.S. Patent No. 6,704,910 (Hong ’910)
- U.S. Patent No. 6,721,860 (Klein ’860)
- U.S. Patent No. 6,781,405 (Rajan ’405)
- U.S. Patent No. 6,834,014 (Yoo ’014)
- U.S. Patent No. 6,856,169 (Frans ’169)
- U.S. Patent No. 6,885,959 (Salmon ’959)

- U.S. Patent No. 6,894,691 (Juenger ’691)
- U.S. Patent No. 6,924,660 (Nguyen ’660)
- U.S. Patent No. 6,965,529 (Zumkehr ’529)
- U.S. Patent No. 6,977,655 (Ryan ’655)
- U.S. Patent No. 7,024,518 (Halbert ’518)
- U.S. Patent No. 7,079,446 (Murtagh ’446)
- U.S. Patent No. 7,068,064 (Yen ’064)
- U.S. Patent No. 7,120,727 (Lee ’727)
- U.S. Patent No. 7,142,461 (Janzen ’461)
- U.S. Patent No. 7,148,721 (Park ’721)
- U.S. Patent No. 7,155,627 (Matsui ’627)
- U.S. Patent No. 7,191,302 (Usami ’302)
- U.S. Patent No. 7,196,567 (Nguyen ’567)
- U.S. Patent No. 7,196,966 (Jin ’966)
- U.S. Patent No. 7,240,145 (Holman ’145)
- U.S. Patent No. 7,280,590 (Boecker ’590)
- U.S. Patent No. 7,286,436 (Bhakta ’436)
- U.S. Patent No. 7,289,386 (Bhakta ’386)
- U.S. Patent No. 7,334,150 (Ruckerbauer ’150)
- U.S. Patent No. 7,356,639 (Perego ’639)
- U.S. Patent No. 7,408,378 (Best ’378)
- U.S. Patent No. 7,432,731 (Bains ’731)
- U.S. Patent No. 7,450,535 (Best ’535)
- U.S. Patent No. 7,486,104 (Oh ’104)

- U.S. Patent No. 7,487,428 (Co ’428)
- U.S. Patent No. 7,508,235 (Singor ’235)
- U.S. Patent No. 7,532,537 (Solomon ’537)
- U.S. Patent No. 7,583,768 (Lee ’768)
- U.S. Patent No. 7,584,336 (Tremaine ’336)
- U.S. Patent No. 7,636,274 (Solomon ’274)
- U.S. Patent No. 7,646,215 (Haig ’215)
- U.S. Patent No. 7,701,257 (Bae ’257)
- U.S. Patent No. 7,702,293 (Ruha ’293)
- U.S. Patent No. 7,782,082 (Oh ’082)
- U.S. Patent No. 7,881,150 (Solomon ’150)
- U.S. Patent No. 7,864,604 (David ’604)
- U.S. Patent No. 7,945,793 (Wilcox ’793)
- U.S. Patent No. 7,977,968 (Kim ’968)
- U.S. Patent No. 7,991,573 (Homer ’573)
- U.S. Patent No. 7,996,590 (Lee ’590)
- U.S. Patent No. 8,041,865 (Bruennert ’865)
- U.S. Patent No. 8,081,536 (Solomon ’536)
- U.S. Patent No. 8,130,560 (Rajan ’560)
- U.S. Patent No. 8,250,295 (Amidi ’295)
- U.S. Patent No. 8,266,372 (Gillingham ’372)
- U.S. Patent No. 8,391,347 (Kim ’347)
- U.S. Patent No. 8,406,356 (Hollis ’356)
- U.S. Patent No. 8,417,870 (Lee ’870)

- U.S. Patent No. 8,756,364 (Bhakta ’364)
- U.S. Patent No. 9,570,129 (Shaeffer ’129)
- U.S. Patent Application Publication No. 2001/0008006 (Klein ’006)
- U.S. Patent Application Publication No. 2002/0112119 (Halbert ’119)
- U.S. Patent Application Publication No. 2002/0144166 (Chang ’166)
- U.S. Patent Application Publication No. 2003/0043681 (Janzen ’681)
- U.S. Patent Application Publication No. 2003/0043683 (Funaba ’683)
- U.S. Patent Application Publication No. 2003/0070052 (Lai ’052)
- U.S. Patent Application Publication No. 2003/0234664 (Yamagata ’664)
- U.S. Patent Application Publication No. 2004/0090239 (Ikeoku ’239)
- U.S. Patent Application Publication No. 2005/0044305 (Jakobs ’305)
- U.S. Patent Application Publication No. 2005/0052200 (Nguyen ’200)
- U.S. Patent Application Publication No. 2005/0212551 (So ’551)
- U.S. Patent Application Publication No. 2005/0226080 (Lee ’080)
- U.S. Patent Application Publication No. 2005/0242833 (Park ’833)
- U.S. Patent Application Publication No. 2006/0071683 (Best ’683)
- U.S. Patent Application Publication No. 2006/0091900 (Kang ’900)
- U.S. Patent Application Publication No. 2006/0117152 (Amidi ’152)
- U.S. Patent Application Publication No. 2006/0146627 (Park ’627)
- U.S. Patent Application Publication No. 2006/0262586 (Solomon ’586)
- U.S. Patent Application Publication No. 2007/0007992 (Bains ’992)
- U.S. Patent Application Publication No. 2007/0035326 (Braun ’326)
- U.S. Patent Application Publication No. 2007/0070669 (Tsern ’669)
- U.S. Patent Application Publication No. 2007/0070717 (Kim ’717)

- U.S. Patent Application Publication No. 2007/0159228 (Nguyen ’228)
- U.S. Patent Application Publication No. 2007/0247185 (Oie ’185)
- U.S. Patent Application Publication No. 2007/0276976 (Gower ’976)
- U.S. Patent Application Publication No. 2009/0119451 (Haywood ’451)
- U.S. Patent Application Publication No. 2009/0177853 (Mazzola ’853)
- U.S. Patent Application Publication No. 2009/0248969 (Wu ’969)
- U.S. Patent Application Publication No. 2010/0027356 (Shaeffer ’356)
- WIPO Patent Application Publication No. 1998/004041 (Kaplinsky ’041)
- WIPO Patent Application Publication No. 1999/000734 (Nakagome ’734)
- WIPO Patent Application Publication No. 2000/041300 (Taylor ’300)
- WIPO Patent Application Publication No. 2004/061690 (Kurts ’690)
- WIPO Patent Application Publication No. 2006/055497 (Bains ’497)
- Japanese Patent Application Publication No. 2002-184176 (Masashi ’176)
- JEDEC Standard DDR SDRAM Specification, JESD79 (June 2000)
- JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
- JEDEC Standard DDR2 SDRAM Specification, JESD79-2 (September 2003)
- JEDEC Standard DDR2 SDRAM Specification, JESD79-2A (January 2004)
- JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005)
- JEDEC Standard FBDIMM Advanced Memory Buffer (AMB), JESD82-20 (March 2007)
- JEDEC Standard DDR2 SDRAM Specification, JESD79-3A (September 2007)
- Intel 6400/6402 Advanced Memory Buffer Datasheet (October 2006)
- Intel 7300 Chipset Memory Controller Hub (MCH) Datasheet (September 2007)
- Micron TN-47-02 DDR2 Offers New Features/Functionality, Rev. A 6/06 EN (2005)
- Samsung Electronics DDR2 SDRAM Device Operating & Timing Diagram

- Samsung Electronics 512Mb E-die DDR2 SDRAM Specification, 60FBGA & 84 FBGA with Pb-Free, K4T51043QE, K4T51083QE, K4T51063QE, Rev. 1.8 (July 2007)]
- Samsung Electronics DDR2 Fully Buffered DIMM 250pin FBDIMMS based on 512Mb E-die, Rev. 1.51 (January 2008)
- G. Moore, *Cramming more components onto integrated circuits*, Electronics, Vol. 38, No. 8, April 19, 1965
- Harold S. Stone, Microcomputer Interfacing (1982)
- Peter Gillingham and Bill Vogley, *SLDRAM: High-Performance, Open-Standard Memory*, IEEE Micro (November/December 1997)
- Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
- Young-Soo Sohn et al., *A 512Mbit, 3.2Gbps/pin Packet-Based DRAM with Cost-Efficient Clock Generation and Distribution Scheme*, IEEE 2004 Symposium On VLSI Circuit Digest of Technical Papers (2004)
- Seung-Jun Bae et al., *A 3Gb/s 8b Single-Ended Transceiver for 4-Drop DRAM Interface with Digital Calibration of Equalization Skew and Offset Coefficients*, ISSCC 2005, Session 28, Clocking and I/O / 28.6 (Feb. 9, 2005)
- Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (Jacob)

Each of these references show that the concept of using dynamically controlled resistive circuits to lessen the effects of impedance mismatches on high-speed signal transmission lines between circuits on a memory module is not novel and was well-known for many years before the alleged priority date of the ’731 Patent. As discussed in the prior art references listed above and charted in Exhibits B-1 through B-23, the integration of a dynamically controlled resistive circuit in either a discrete buffer circuit for a memory device or the memory device itself was well-known. In light of the references discussed herein, the Asserted Claims of the ’731 Patent cannot be valid.

Defendants’ reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the

systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the ’731 Patent. Defendants’ investigation of such prior art systems is still ongoing, and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third-party prior art systems anticipate and/or render obvious the Asserted Claims of the ’731 Patent. As such, Defendants reserve all rights to supplement its Invalidity Contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the ’731 Patent. Defendants have obtained, and are in the process of obtaining, additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be subject to third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants’ possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

5. P.R. 3-3(b) – Invalidity Grounds Under 35 U.S.C. §§ 102 and 103

Pursuant to P.R. 3-3(b), Defendants contend that certain prior art references below anticipate one or more Asserted Claims and that to the extent the identified prior art references do not anticipate the Asserted Claims, those claims are invalid as obvious under 35 U.S.C. § 103.[4] Each anticipatory prior art reference, either alone or in combination with other prior art, also renders the Asserted Claims invalid as obvious. In particular, each anticipatory prior art reference may be combined with (1) information generally known to persons skilled in the art at the time of the alleged invention, and/or (2) any of the other anticipatory prior art references. To the extent that Plaintiff contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants contend that any difference between the reference and the corresponding patent claims would have been obvious to one of ordinary skill in the art. Thus, all anticipation charts should be interpreted as both reflecting anticipation by the reference as well as invalidity due to single-reference obviousness, to the extent that Plaintiff contends that any limitation is missing.

Defendants further identify and hereby incorporates by reference as if set forth fully herein the prior art references and Invalidity Contentions as described in any Other Netlist Proceedings wherein Invalidity Contentions have been, or will be, provided regarding the Asserted Patents, their foreign counterparts, or any parent or child patent of the Asserted Patents. Defendants reserve the right to use all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these proceedings to demonstrate and/or

[4] As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or future.

evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

5.1. ’087 Patent

In view of the apparent scope of the Asserted Claims of the ’731 Patent as advanced in Plaintiff’s Infringement Contentions, the limitations of the Asserted Claims would have been at least obvious, if not anticipated, by the prior art references identified below and discussed herein and in Exhibits A1–A22 and AOO. *See, e.g., 01 Communique Lab., Inc. v. Citrix Sys., Inc.*, 889 F.3d 735, 742 (Fed. Cir. 2018).

5.1.1. Anticipation

Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate the ’087 patent’s Asserted Claims in the Exhibit A claim charts, which are hereby incorporated by reference as if fully set forth herein. Exhibit A’s claim charts provide an explanation showing how these prior art references teach or suggest each and every element of the ’087 patent’s asserted claims.

5.1.2. Obviousness

In addition to certain claims being anticipated at least under Plaintiff’s apparent claim constructions as indicated above, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation. Further, the Asserted Claims are obvious over various combinations of the references shown in the claim charts accompanying or incorporated by reference in this disclosure. No Asserted Claim goes beyond combining known elements to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Thus, to the extent that an Asserted Claim is not anticipated, it is nevertheless invalid as obvious. Specifically, Defendants assert that any charted or incorporated reference in combination with one or more other charted or incorporated references renders the Asserted Claims obvious.

5.1.2.1. Level of Ordinary Skill in the Art

To assess the level of ordinary skill of a person of ordinary skill, the following factors can be considered: (i) the type of problems encountered in the art; (ii) the prior solutions to those problems; (iii) the rapidity at which innovations are made; (iv) the sophistication of the technology; and (v) the level of education of active workers in the relevant field.

Based on the foregoing, Defendants contends that a person of ordinary skill for the '087 patent would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

5.1.2.2. Identification of Obviousness Contentions

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Exhibits A-1 through A-22 and A-OO the prior art references that render obvious the Asserted Claims of the '087 Patent and include below exemplary and non-exhaustive combinations showing the obviousness of the Asserted Claims in view of the prior art. Defendants reserve the right to rely on any combination of the references reflected in their charts or incorporated herein by reference. The combinations of prior

art listed below render obvious the Asserted Claims under the proper construction of the claims and/or under Plaintiff's apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Exhibits A-1 through A-22 and A-OO, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the '087 Patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Exhibits A-1 through A-22 and A-OO, such reference may be combined with any other references listed in Exhibits A-1 through A-22 and A-OO for such element, thereby rendering the claim invalid for obviousness.

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Exhibits A-1 through A-22 and A-OO, along with the knowledge of one of ordinary skill in the art, to meet the limitations of the Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

In addition, a person of ordinary skill in the art would have been motivated to combine the prior art references because the elements found in the Asserted Claims of the '087 patent are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the '087 patent. *See, e.g.*, Ex. A-1 ('087 APA).

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent claim was known by a person of ordinary skill in the art at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

For at least the reasons described below, it would have been obvious to a person of ordinary skill in the art to combine each prior art reference listed in Appendix A with any other reference or references listed in Appendix A along with the knowledge of one of ordinary skill in the art to arrive at the claimed inventions in the ’087 patent. For example, and without limitation, the Asserted Claims of the ’087 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor / Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
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As mentioned above, Defendants have not yet completed its search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants inclusion of exemplary combinations does not preclude it from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

5.1.2.3. Obviousness Rationales

Motivations to combine, as well as the general state of the art, may be found in a variety of places including in the references defined above, and the specification of the '087 Patent. For

example, each piece of prior art relates to the design and/or structure and/or function of optoelectronic devices. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there was a motivation in the art to make such a combination.

Motivations to combine various prior art references are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the '087 Patent. Further reasons to combine the references identified in these charts include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of optoelectronic devices that such combinations would have yielded predictable results, and the fact that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007); see also id. at 401 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id*.

at 427. The Supreme Court held that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id*. at 401.

Moreover, the Supreme Court recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id*. at 402 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 402-03.

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 417. If a person of ordinary skill can implement a predictable variation, U.S.C. § 103 bars its patentability. *Id*. The rationale to combine or modify prior art references is significantly stronger when references seek to solve similar problems, come from the same field, and correspond well with one another. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them.

Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination.

These disclosures are provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any Invalidity Contentions. Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Plaintiff may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Defendants reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the '087 Patent.

One or more combinations of the prior art references identified in Exhibits A-1 through A-22 and A-OO would have been obvious because these references would have been combined using a simple substitution of one known, equivalent element for another to obtain predictable results and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Exhibits A-1 through A-22 and A-OO would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

All the Asserted Claims are directed to a DRAM package or a method of operating the same. Such technology was widely known before the alleged priority date of the '087 Patent. *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '619), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), A-OO (Additional References).

The prior art references provide motivations to combine because they describe the field of the '087 Patent, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '619), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), A-OO (Additional References).

Additionally, the prior art also provides sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill in the art to try with a reasonable expectation of success. For example, it would have been obvious to one of skill in the art at the time of the '087 patent that the disclosures relating to memory devices and circuitry could be readily integrated into memory modules.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill in the art within the field of the '087 Patent to yield predictable results. The substitution of one element could have been predictably achieved by one

of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’087 Patent.

5.1.2.3.1 Independent Claim 1

1[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have a “dynamic random access memory (DRAM) package.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[b][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[b][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports

and the DRAM memory cells." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[c][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals." *See, e.g.*, A-1 ('087 APA), Exs. A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[c][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger

’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[d][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[d][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[d][3]. It was well known to one of skill in the art before the time of the '087 Patent to have "each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[e][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "1[e][1] a control die coupled between the terminals and the stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[e][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "the control die including conduits, the conduits including C/A conduits and data conduits." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger

’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[e][3]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[e][4]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[f]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a first C/A interconnect of the first C/A interconnects is in electrical communication with

corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[g]. It was well known to one of skill in the art before the time of the '087 Patent to have "a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[h][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12

(Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[h][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[h][3]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[i]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[j]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[k][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer

’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[k][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the one or more C/A signals do not include any chip select signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[l]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[m]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[n]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[o]. It was well known to one of skill in the art before the time of the ’087 Patent to have “1[o] wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6

(Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[p][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

1[p][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 1.

- Claim 1 is obvious in view of any one of Exhibits A-1–A22.
- Claim 1 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.1 Dependent Claim 2

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the stacked DRAM dies include at least 8 stacked DRAM dies.” *See, e.g.*, Exs. A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-8 (Wyman ’192), A-9 (Rajan ’137), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 2.

- Claim 2 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 2 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.2 Dependent Claim 3

It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the stacked DRAM dies include 16 stacked DRAM dies." *See, e.g.*, Exs. A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-8 (Wyman '192), A-9 (Rajan '137), A-14 (Gillingham '906), A-15 (Bilger '958), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 3.

- Claim 3 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 3 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.3 Dependent Claim 4

4[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

4[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the second driver size is different from the first driver size.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 4.

- Claim 4 is obvious in view of any one of Exhibits A-1–A-2, A4–A19, and A-21–A-22.
- Claim 4 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.4 Dependent Claim 5

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 5.

- Claim 5 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 5 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 5 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 5 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 5 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 5 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.5 Dependent Claim 6

6[a]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

6[b]. It was well known to one of skill in the art before the time of the '087 Patent to have "the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

6[c]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '619), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 6.

- Claim 6 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 6 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 6 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.6 Dependent Claim 7

It was well known to one of skill in the art before the time of the ’087 Patent to have "wherein the control die is further configured to control timing of command/address signals driven

to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 7.

- Claim 7 is obvious in view of any one of Exhibits A1–A18 and A20–A22.
- Claim 7 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 7 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.1.7 Dependent Claim 8

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not

electrically connected to any data port on the at least one DRAM die." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 8.

- Claim 8 is obvious in view of any one of Exhibits A-1–A22.
- Claim 8 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.2 Independent Claim 9

9[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have "9[a] A method, comprising:." *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18

(Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[b][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[b][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[b][3]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the DRAM package further including die interconnects, each of the die interconnects including one or more–silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[b][4]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[c]. It was well known to one of skill in the art before the time of the ’087 Patent to have “receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first

set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[d][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[d][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13

(Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[e][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[e][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[f][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[f][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[f][3]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least

one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[g]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[h]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349),

A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[i]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[j][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[j][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer

’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[k]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

9[l]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 9.

- Claim 9 is obvious in view of any one of Exhibits A-1–A22.
- Claim 9 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.2.1 Dependent Claim 10

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the stacked DRAM dies include at least 8 stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 10.

- Claim 10 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 10 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 10 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 10 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 10 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 10 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.2.2 Dependent Claim 11

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 11.

- Claim 11 is obvious in view of any one of Exhibits A-1–A22.
- Claim 11 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.2.3 Dependent Claim 12

12[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:.” *See, e.g.*, Exs. A-3 (Shaeffer ’507), A-15 (Bilger ’958), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

12[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

12[c]. It was well known to one of skill in the art before the time of the ’087 Patent to have “enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan

’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

12[d]. It was well known to one of skill in the art before the time of the ’087 Patent to have “maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

12[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of Claim 12.

- Claim 12 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 12 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 12 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3 Independent Claim 13

13[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have “[a] dynamic random access memory (DRAM) package.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional

data port." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[c]. It was well known to one of skill in the art before the time of the '087 Patent to have "an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[d]. It was well known to one of skill in the art before the time of the '087 Patent to have "die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[f]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein: the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[g]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee

’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[h][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[h][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[i]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[j]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[k]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein a second C/A interconnect of the second C/A interconnects is in electrical

communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[l]. It was well known to one of skill in the art before the time of the '087 Patent to have "the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[m]. It was well known to one of skill in the art before the time of the '087 Patent to have "the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho

’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[n]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[o]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer

’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[p]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[q]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[r]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die is configurable to drive the one or more second signals to the second DRAM die

ene or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[s]. It was well known to one of skill in the art before the time of the '087 Patent to have "each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[t]. It was well known to one of skill in the art before the time of the '087 Patent to have "a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth

’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

13[u]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 13.

- Claim 13 is obvious in view of any one of Exhibits A-1–A22.
- Claim 13 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 13 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 13 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 13 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 13 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.1 Dependent Claim 14

It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies." *See, e.g.*, Exs. A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-8 (Wyman '192), A-9 (Rajan '137), A-14 (Gillingham '906), A-15 (Bilger '958), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 14.

- Claim 14 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 14 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.2 Dependent Claim 15

It was well known to one of skill in the art before the time of the ’087 Patent to have "wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies." *See, e.g.*, Exs. A-

2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-8 (Wyman ’192), A-9 (Rajan ’137), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 15.

- Claim 15 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 15 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.3 Dependent Claim 16

It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger

’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 16.

- Claim 16 is obvious in view of any one of Exhibits A-1–A22.
- Claim 16 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.4 Dependent Claim 17

17[a][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18

(Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

17[a][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface.” *See, e.g.*, Exs. A-3 (Shaeffer ’507), A-15 (Bilger ’958), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

17[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

17[c]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh

2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

17[d]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the first data conduits are placed in a non-driving state after driving the first data signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

17[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the second data conduits are placed in a non-driving state after driving the second data signals; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

17[f]. It was well known to one of skill in the art before the time of the ’087 Patent to have “data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18

(Loh 2008), A-19 (Chung '692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 17.

- Claim 17 is obvious in view of any one of Exhibits A-3, A-15, and A19.
- Claim 17 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.5 Dependent Claim 18

18[a][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349),

A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

18[a][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 18.

- Claim 18 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 18 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 18 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 18 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 18 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 18 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 18 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.3.6 Dependent Claim 19

It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 19.

- Claim 19 is obvious in view of any one of Exhibits A-1–A22.
- Claim 19 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 19 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 19 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 19 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 19 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 19 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 19 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.4 Independent Claim 20

20[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have “[a] dynamic random access memory (DRAM) package.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “20[b] stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[c][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma

’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[c][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[d][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[d][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the data interconnects including a first set of data interconnects configured to conduct the

first n-bit-wide data signal and the second n-bit-wide data signal." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[d][3]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies–the one or more TSVs; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[e][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "a control die coupled between the terminals and the stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[e][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "the control die including conduits coupled to respective ones of the die interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[f][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[f][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan

’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[g]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[h][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[h][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the one or more C/A signals do not include any chip select signal." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[i]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[j]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer

’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[k]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[l][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[l][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA),

A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

20[m]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 20.

- Claim 20 is obvious in view of any one of Exhibits A-1–A22.
- Claim 20 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 20 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 20 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 20 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 20 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 20 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.4.1 Dependent Claim 21

It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the stacked DRAM dies include at least 8 stacked DRAM dies." *See, e.g.*, Exs. A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-8 (Wyman '192), A-9 (Rajan '137), A-14 (Gillingham '906), A-15 (Bilger '958), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 21.

- Claim 21 is obvious in view of any one of Exhibits A-1–A22.
- Claim 21 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 21 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 21 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.4.2 Dependent Claim 22

22[a]. It was well known to one of skill in the art before the time of the ’087 Patent to have "wherein: the first set of C/A signals include one or more signals to select one DRAM die among

the first plurality of DRAM dies to output the first n-bit-wide data; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

22[b]. It was well known to one of skill in the art before the time of the '087 Patent to have "the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 22.

- Claim 22 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 22 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 22 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 22 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 22 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 22 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 22 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.5 Independent Claim 23

23[a]. It was well known to one of skill in the art before the time of the '087 Patent to have "[a] dynamic random access memory (DRAM) package." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[b]. It was well known to one of skill in the art before the time of the '087 Patent to have "stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[c][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in

response to the (C/A) signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[c][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[d][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh

2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[d][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[d][3]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[e][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a control die coupled between the terminals and the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11

(Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[e][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die including conduits coupled to respective ones of the die interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[f][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[f][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[g]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[h][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552),

A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[h][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the one or more C/A signals do not include any chip select signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[i]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[j]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die is configured to receive signals from the first unidirectional interconnects

and to drive signals to the second unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[k]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[l][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[l][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[m][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[m][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4

(Riho ’364), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

23[n]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’619), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 23.

- Claim 23 is obvious in view of any one of Exhibits A-1–A22.
- Claim 23 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 23 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 23 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 23 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 23 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 23 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.6 Independent Claim 24

24[a]. It was well known to one of skill in the art before the time of the '087 Patent to have "[a] dynamic random access memory (DRAM) package." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[b]. It was well known to one of skill in the art before the time of the '087 Patent to have "stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[c]. It was well known to one of skill in the art before the time of the '087 Patent to have "an interface via which the DRAM package receives C/A signals and receives or outputs data signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364),

A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[d][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a control die coupled between the interface and the stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[d][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the control die including signal conduits and logic configured to control at least some of the signal conduits; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “die interconnects, each die interconnect of the die interconnects coupled between at least one

corresponding conduit in the control die and one corresponding signal port in each of a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[f]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein: the signal conduits include first conduits, second conduits, third conduits and fourth conduits." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[g]. **I**t was well known to one of skill in the art before the time of the '087 Patent to have "the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14

(Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[h]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[i]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[j]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each of the third conduits being a unidirectional conduit configurable to drive a signal received

from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[k]. It was well known to one of skill in the art before the time of the '087 Patent to have "each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect." *See, e.g.*, Exs. A-1 ('087 APA), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[l]. It was well known to one of skill in the art before the time of the '087 Patent to have "the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham

’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[m][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[m][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[n][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[n][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[o][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset

of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[o][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[p][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3

(Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[p][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[q]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[r]. It was well known to one of skill in the art before the time of the ’087 Patent to have “each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects.” *See, e.g.*, Exs. A-1 (’087 APA), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[s][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[s][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17

(Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[s][3]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

24[s][4]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 24.

- Claim 24 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 24 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 24 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 24 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 24 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 24 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 24 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.6.1 Dependent Claim 25

25[a][1]. It was well known to one of skill in the art before the time of the ’087 Patent to have “[t]he DRAM package of claim 24, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of a first subset of DRAM dies and not in electrical communication with any signal port of any of the second subset of DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[a][2]. It was well known to one of skill in the art before the time of the ’087 Patent to have “wherein each of the second subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of the second subset of DRAM dies and not in electrical communication with any signal port of any of the first subset of DRAM dies, and wherein:.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262),

A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[b]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[c]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[d]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals.” *See, e.g.*, Exs.

A-1 (’087 APA), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[f]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung

’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

25[g]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 25.

- Claim 25 is obvious in view of any one of Exhibits A-1–A-22.
- Claim 25 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 25 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 25 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 25 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 25 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.
- Claim 25 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 25 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.6.2 Dependent Claim 26

26[a][1]. It was well known to one of skill in the art before the time of the '087 Patent to have "[t]he DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals." *See, e.g.*, Exs. A-3 (Shaeffer '507), A-15 (Bilger '958), A-19 (Chung '692), A-20 (Hollis '373),and A-OO (Additional References).

26[a][2]. It was well known to one of skill in the art before the time of the '087 Patent to have "wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

26[b]. It was well known to one of skill in the art before the time of the '087 Patent to have "the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3 (Shaeffer '507), A-4 (Riho '364), A-5 (Kim '156), A-6 (Rajan '881), A-7 (Lee '362), A-8 (Wyman '192), A-9 (Rajan '137), A-10 (Ware '262), A-11 (Best '537), A-12 (Foster '169), A-13 (Jeddeloh '745), A-14 (Gillingham '906), A-15 (Bilger '958), A-16 (Ma '349), A-17 (Ruckerbauer '446), A-18 (Loh 2008), A-19 (Chung '692), A-20 (Hollis '373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

26[c]. It was well known to one of skill in the art before the time of the '087 Patent to have "the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and." *See, e.g.*, Exs. A-1 ('087 APA), A-2 (Keeth '552), A-3

(Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

26[d]. It was well known to one of skill in the art before the time of the ’087 Patent to have “the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

26[e]. It was well known to one of skill in the art before the time of the ’087 Patent to have “a conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-3 (Shaeffer ’507), A-4 (Riho ’364), A-5 (Kim ’156), A-6 (Rajan ’881), A-7 (Lee ’362), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-12 (Foster ’169), A-13 (Jeddeloh ’745), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-16 (Ma ’349), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-21 (Micron LRDIMM), A-22 (JEDEC HBM), and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 26.

- Claim 26 is obvious in view of any one of Exhibits A-1–A22.

- Claim 26 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 26 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.6.3 Dependent Claim 27

It was well known to one of skill in the art before the time of the ’087 Patent to have “[t]he DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 27.

- Claim 27 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 27 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 27 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.6.4 Dependent Claim 28

It was well known to one of skill in the art before the time of the ’087 Patent to have “[t]he DRAM package of claim 27, wherein the stacked DRAM dies include 16 stacked DRAM dies.” *See, e.g.*, Exs. A-1 (’087 APA), A-2 (Keeth ’552), A-4 (Riho ’364), A-5 (Kim ’156), A-8 (Wyman ’192), A-9 (Rajan ’137), A-10 (Ware ’262), A-11 (Best ’537), A-14 (Gillingham ’906), A-15 (Bilger ’958), A-17 (Ruckerbauer ’446), A-18 (Loh 2008), A-19 (Chung ’692), A-20 (Hollis ’373),and A-OO (Additional References).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 28.

- Claim 28 is obvious in view of any one of Exhibits A-1–A-22.

- Claim 28 is obvious in view of Exhibit A-1 in view of at least one of Exhibits A-2–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-2 in view of at least one of Exhibits A-1, A-3–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-3 in view of at least one of Exhibits A-1, A-2, A-4,–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-4 in view of at least one of Exhibits A-1, A-2, A-3, A-5–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-5 in view of at least one of Exhibits A-1–A-4, A-6–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-6 in view of at least one of Exhibits A-1–A-5, A-7–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-7 in view of at least one of Exhibits A-1–A-6, A-8–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-8 in view of at least one of Exhibits A-1–A-7, A-9–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-9 in view of at least one of Exhibits A-1–A-8, A-10–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-10 in view of at least one of Exhibits A-1–A-9, A-11–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-11 in view of at least one of Exhibits A-1–A-10, A-12–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-12 in view of at least one of Exhibits A-1–A-11, A-13–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-13 in view of at least one of Exhibits A-1–A-12, A-14–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-14 in view of at least one of Exhibits A-1–A-13, A-15–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-15 in view of at least one of Exhibits A-1–A-14, A-16–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-16 in view of at least one of Exhibits A-1–A-15, A-17–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-17 in view of at least one of Exhibits A-1–A-16, A-18–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-18 in view of at least one of Exhibits A-1–A-17, A-19–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-19 in view of at least one of Exhibits A-1–A-18, A-20–A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-20 in view of at least one of Exhibits A-1–A-19, A-21, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-21 in view of at least one of Exhibits A-1–A-20, A-22, A-OO, and the knowledge of a person of ordinary skill in the art.

- Claim 28 is obvious in view of Exhibit A-22 in view of at least one of Exhibits A-1–A-21, A-OO, and the knowledge of a person of ordinary skill in the art.

5.1.2.3.7 Specific Combinations

Additional motivations to combine specific references are discussed below.

5.1.2.3.7.1 Keeth ’552 (A-2) & Shaeffer ’507 (A-3)

A person of ordinary skill in the art would have been motivated to combine Keeth ’552 with Shaeffer ’507. Keeth ’552 and Shaeffer ’507 are analogous art to the ’087 Patent. For example, each is reasonably pertinent to the problem of improving memory operations in the stack, including speed, signal timing, and/or bandwidth. *See, e.g.*, ’087 Patent, 1:33-34, 8:1-4, 21:26-28; Keeth ’552, 1:55-60, 5:63-67, 10:66-11:7; Shaeffer ’507, 1:15-20, 2:23-26, 11:12-18.

A person of ordinary skill in the art would have been motivated to use the advantageous signaling techniques taught by Shaeffer ’507 in the memory stacks disclosed in Keeth ’552. Keeth ’552 discloses a stack of memory dice (202) and an interface die (210) with multiple “vaults” and respective vault control circuits (212) to control memory “partitions” in the stack. *See, e.g.*, Keeth ’552, 3:44-4:16, Fig. 2. Keeth ’552’s “control circuits 212 … enable communication and control with the corresponding memory partition 204 … via communicative paths 208.” Keeth ’552, 3:44-54. These communicative paths “may communicate (e.g., transfer) information such as data, address, control, ID information, [and] other information.” Keeth ’552, 3:5-8. Keeth ’552 teaches that, by using vaults and interleaving connections that it discloses, “a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth,” Keeth ’552, 4:4-16, and that this may “increase the operational speed of elements in the stack(s),” Keeth ’552, 10:66-11:7. Keeth ’552 further teaches that, “with input/output circuitry connected to the interface die via interleaving conductive paths and command and/or address circuitry of the dice connected to the interface die via interleaving

conductive paths, each vault may be independently controlled." Keeth '552, 6:19-24. Accordingly, a person of ordinary skill would have been motivated to use Keeth '552's independently controlled vaults and interleaving connections alongside other stacked memory architectures to maintain these advantages. However, Keeth '552 does not provide details of the signaling protocol to use. Therefore, persons of ordinary skill would have been motivated to search for signaling protocols that could be advantageously used in Keeth '552's memory vaults and interleaving connections.

Shaeffer '507 teaches an "apparatus and protocol for high speed signaling between a memory device and a memory controller" where the "memory controller … may be stacked with one or more memory devices … in a through-silicon via (TSV) stack." Shaeffer '507, 11:10-18, 11:19-24. Accordingly, Shaeffer '507, like Keeth '552, uses a TSV stack where the memory controller is stacked with the controlled memory dice. Therefore, a person of ordinary skill would have been motivated to implement the advantageous aspects of Shaeffer '507's high speed signaling functionality in Keeth '552's memory stack. For example, Shaeffer '507 teaches that high speed signaling can be achieved using connections for command/address signals (C/A 114) separate from connections for data signals (120/128). Shaeffer '507, Fig. 1A. A person of ordinary skill would have recognized that, by using separate C/A and data connections, the bandwidth of the data transfer can be increased, because C/A connections can be used to schedule further data transfer while the previous data transfers are still being communicated on the data connections. For example, Shaeffer '507's Fig. 4B depicts that the data transfer (Q[A0] and Q[A1]) on data lines DQ[63:0] cam be carried out for previous read commands (RD[A0] and RD[A1]) while new read commands (RD[A2] and RD[3]) are being received for subsequent read operations. *See, e.g.*, Shaeffer '507, Fig. 4B.

Additionally, Keeth ’552 teaches that stacked memory devices can be similar to DDR3 SDRAM devices. *See, e.g.*, Keeth ’552, 2:37-41. The corresponding JEDEC standards require separate C/A and data lines for DDR3 SDRAM. *See, e.g.*, JESD79-3C, 12, Fig. 3. Shaeffer ’507 also likewise teaches that its memory devices can be “graphics double data rate (GDDR, GDDR2, GDDR3, GDDR4, GDDR5, and future generations) and double data rate (DDR2, DDR3 and future memory types).” Shaeffer ’507, 8:60-64. GDDR3 memory devices, like DDR memories, also use separate command, address, and data (DQ) lines. *See, e.g.*, JESD21-C 3.11.5.7, 9. A person of ordinary skill would have recognized that memory devices using separate lines for address, command, and data signals was a well-known technique. *See, e.g.*, Schnarr ’216, Fig. 5; Ide ’899, Fig. 4.

A person of ordinary skill would have also understood that separate C/A and data connections can be used in a stack to communicate with memory dice using such separate C/A and data connections. Notably, stacks of memory dice that used separate C/A and data lines (implemented by TSVs) would have been well known to a person of ordinary skill at the time of the ’087 Patent. *See, e.g.*, U.S. Patent No. Ide ’899, Fig. 4.

Therefore, a person of ordinary skill would have been motivated to use Keeth ’552’s stack of memory devices using its interleaving connections for C/A signals separate from interleaving connections for data signals. A person of ordinary skill would have recognized that such an arrangement would have allowed for accessing the odd and even dies in the stack independently and concurrently which would allow for increased bandwidth. *See, e.g.*, Keeth ’552, 5:63-6:10. For example, Keeth ’552 discloses that, in addition to the conductive paths for data, “the command circuits and/or address circuits of each dice 520 through 523 may be connected to and utilize the

interleaving conductive paths … which may perhaps increase bandwidth and reduce queuing of signals." Keeth '552, 5:63-6:10.

Shaeffer '507 additionally teaches that timing updates may be necessary during memory operations in order to compensate for noise or drift in the temperature supply voltage. *See, e.g.*, Shaeffer '507, 2:10-22. For example, Shaeffer '507 discloses that such timing updates can be achieved using a timing reference signal (TRS) output by the memory device in response to a read command. Shaeffer '507, 2:23-49. "The TRS, in an embodiment, is conveyed from the memory device, to the memory controller via a signaling resource (i.e., signal traces, pins etc.,) that is also used to transfer error detection and correction information (EDC)." Shaeffer '507, 2:64-3:4, Fig. 4B.

Accordingly, a person of ordinary skill would have been further motivated to implement Shaeffer '507's signaling protocol, including EDC and TRS transmissions from the memory devices, into the memory stack disclosed by Keeth '552 to provide error detection and correction as well as timing updates in order to compensate for noise or drift in temperature or supply voltage.

Additionally, Shaeffer '507 discloses that using a data clock or a data strobe (122) to assist the memory device in capturing write data from the memory controller. *See, e.g.*, Shaeffer '507, 9:1-9, Fig. 1A. As Shaeffer '507 Figure 1A depicts, the data clock/strobe 122 is a unidirectional signal from the control die to the memory die and is used for capturing write data. *See, e.g.*, Shaeffer '507, Fig. 1A. Shaeffer '507 discloses that its control die advantageously captures the read data with proper, rank-specific timing using an edge tracking circuit 108 and a rank tracking circuit 132. *See, e.g.*, Shaeffer '507, 3:62-4:6. Shaeffer '507 further teaches that its techniques for high speed signaling can be used in a TSV stack. *See, e.g.*, Shaeffer '507, 1:15-19, 11:4-15. For example, a person of ordinary skill would have recognized that unidirectional strobe signals for

write operations (WDQS) was a standard, well-understood technique at the time of the ’087 Patent for high-speed write operations. *See, e.g.*, Schnarr ’216, 9:19-34, Fig. 5. Additionally, a person of ordinary skill would have understood that a strobe signal would use less power than a continuous clock signal. Accordingly, a person of ordinary skill would have been motivated to use Shaeffer ’507’s write data strobe functionality and its read data capturing functionality in the memory stack disclosed in Keeth ’552.

Accordingly, using certain aspects of Shaeffer ’507’s signaling protocols, e.g., C/A lines being separate from data lines, the use of timing reference and error detection signaling lines, as well as write strobe signal lines, to communicate with memory dice in a stack in the memory stack disclosed in Keeth ’552 would have been well within the level of skill at the time and a person of ordinary skill would have had a reasonable expectation of success in making this combination. For example, Keeth ’552 discloses that its interleaving paths can be used for control, address and data signals and Shaeffer ’507 discloses specific tools which could have been used to implement its teaching about signaling protocol. *See, e.g.*, Keeth ’552, 3:5-8; Shaeffer ’507, 12:28-29.

5.1.2.3.7.2 Keeth ’552 (A-2) & Shaeffer ’507 (A-3) & Riho ’364 (A-4)

A person of ordinary skill in the art would have been motivated to combine Keeth ’552 with Shaeffer ’507 and with Riho ’364. It would have been obvious to a person of ordinary skill to combine Keeth ’552 with Shaeffer ’507 for the reasons discussed above. It would further have been obvious to combine Keeth ’552 with Shaeffer ’507 and with Riho ’364. Riho ’364 is analogous art to the ’087 Patent, as well as to Keeth ’552 and Shaeffer ’507. As discussed above, both Keeth ’552 and Shaeffer ’507 are analogous art to the ’087 Patent, because each is reasonably pertinent to the problem of improving memory operations in the stack, including speed, signal timing, and/or bandwidth. Riho ’364 is likewise directed to stacked memory devices and is reasonably pertinent to the same problems. For example, Riho ’364 teaches “stacking a plurality

of chip dies," such as DRAM chips. Riho '364, [0003]. Riho '364 teaches that "the fabrication of DRAM chips operating at high frequency will impose difficulties in terms of various product specification values (e.g., timing specification), deteriorating the yield of the product. Furthermore, it will make it difficult to ensure stable operation of the memory module during communication with a memory controller. These problems are attributable to the fac[t] that as the number of stacked chips is increased, the high frequency operation (at high data transfer rate) is affected more by total parasitic resistance or total parasitic capacitance of the through silicon vias and via-to-via connections proportional to the thickness of the stacked chips. The present invention [of Riho '364] seeks to solve one or more of the above problems, or to improve upon those problems at least in part." Riho '364, [0010]-[0011]; *see also* Riho '364, [0148] ("according to this invention, the data transfer speed of the memory module as a whole can be increased").

As another example, Riho '364 also teaches that "optimizing the output drive capacity of output buffers provided in the interface circuit 30, according to a change in the time constant caused by parasitic capacitance and parasitic resistance." Riho '364, [0097]; *see also* Riho '364, Fig. 7A. In Riho '364's Figure 7A, "[e]ach of the output buffers X1 to X4 are formed by an inverter, and NAND, NOR, and CMOS transistors. They have the same circuit configuration, but their transistors are of mutually different sizes" and "trimming signals TOUT generated by the third ROM are … controlling the number of output buffers to be activated." Riho '364, [0097]-[0098]. Accordingly, Riho '364 discloses that selecting the number of transistors and/or the size of the transistors that are included in the buffer which drives a signal, similar to the '087 Patent. *See* '087 Patent, 17:26-28 ("size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver").

A person of ordinary skill would have recognized that the changes in the time constant are also present in the combination of Keeth ’552 as modified by Shaeffer ’507. Specifically, the signals that are driven from the control die to the memory dies through conductive paths in the Keeth ’552-Shaeffer ’507 combination stack. These conductive paths include TSVs and joints and can couple to I/O circuits, and a person of ordinary skill would have recognized that the load to be driven is determined by the parasitic capacitance and resistance on the interleaving conductive paths, including the load of the TSVs, joints, and the I/O circuits coupled to these interleaving paths. *See, e.g.*, Keeth ’552, Fig. 7. For example, Keeth ’552 teaches that “conductive paths 704, 705, 706, 707, and 708 of the first dice stack 702 include joints 709 and TSVs 712, at least some of which extend entirely through the dice stack 702 and some of which connect with circuitry.” Keeth ’552, 7:37-45. Keeth ’552 further teaches that the conductive paths “may entirely pass through or partially pass through the dice stack.” Keeth ’552, 5:34-38.

A person of ordinary skill would have also understood from Keeth ’552’s teachings that, for example, the conductive path 706 can end in die 722 without passing through dies 722 and 723, and does not require a TSV in, nor a joint between, dies 722 and 723, because the last I/O circuit that the conductive path 706 is connected to is I/O circuit 732 in die 722. Keeth ’552, Fig. 7. In contrast, conductive path 705 has to pass through die 722, since it is coupled to I/O circuit 733 in die 723 above. Thus, in implementations where Keeth ’552’s conductive paths only “partially pass through” the stack, different conductive paths may have different length. Accordingly, a person of ordinary skill would have recognized that the he load and the corresponding time constant of the conductive paths would typically be different depending on their length, e.g., because they “extend entirely through” or “partially pass through” the stack.

Additionally, Riho ’364 teaches that “it is necessary to take into consideration that the parasitic capacitance and parasitic resistance of data transfer through electrodes formed in the vias (which depend on the thicknesses of the chip dies themselves (i.e., the thickness of the silicon substrates)) and the parasitic capacitance and parasitic resistance caused by bumps connecting between the chip dies (between the through electrodes) differ from one another, and hence the time constants defined by the total parasitic capacitance and total parasitic resistance also differ from one another.” Riho ’364, [0096]. A person of ordinary skill would have understood that such varying parasitic capacitance and resistance is inherent in the manufacturing process. *See, e.g.*, Riho ’364, [0056]. A person of ordinary skill would have likewise also understood that “the SDRAM chip located closer to the …[control die] has a smaller penetrating through resistance while the SDRAM chip located farther from the …[control die] has a larger penetrating through resistance. Further, these penetrating through resistances slightly have variations due to the difference in manufacturing process.” Riho ’364, [0061]. Therefore, a person of ordinary skill would have recognized that that the loads (and the corresponding delays) of the different conductive paths can vary due to manufacturing variations of the joints and TSVs and due to the different locations of the coupled I/O circuits from the control die.

Accordingly, a person of ordinary skill would have been motivated to look for methods addressing these timing problems and would implement a known solution, such as Riho ’364’s driver-size optimization techniques. A person of ordinary skill would have been motivated to implement Riho ’364’s techniques because it would advantageously improve and stabilize high frequency memory operations despite the time-constant variations in the stack of the Keeth ’552-Shaeffer ’507 combination. *See, e.g.*, Riho ’364, [0010]-[0011]. A person of ordinary skill would have likewise recognized that the Riho ’364’s driver-size optimization techniques can save power,

thereby providing further motivation to use them in the Keeth ’552-Shaeffer ’507 combination. *See, e.g.*, Wyman ’192, 1:22-24.

Additionally, Riho ’364 teaches that “[i]n practice, it has been found that various problems such as increased power consumption and deteriorated yield would occur when the data transfer speed from the DRAM chips is increased.” Riho ’364, [0008]. Therefore, to solve the problem of increased power consumption, Riho ’364 teaches that “data signals are transmitted and received through the 256 data transfer through electrodes formed in the 256 vias. In this case, each data transfer through electrode only need be capable of transmitting and receiving data signals at a data transfer rate of 400 Mbps (102.4 Gbit/256).… This enables the memory module to stably communicate with the memory controller at a low power consumption, and provides a memory module having a data transfer speed of 12.8 Gbytes/sec.” Riho ’364, [0052]. In addition to reducing power (and current), Riuho2 also teaches that operating the memory chips at a lower frequency can also increase yield. *See, e.g.*, Riho ’364, [0148].

Accordingly, a person of ordinary skill would have been motivated by Riho ’364’s disclosure to operate Keeth ’552’s communication paths inside the stack at a rate that is lower than the “appropriate data transfer rates” with an external processor, which advantageously results in lower power consumption. Operating the memory chips at a lower rate than the rate for communicating with a processor would have been well within a person of ordinary skill’s skill at the time of the ’087 Patent. *See, e.g.*, Jacob, 19. For example, Keeth ’552 teaches that its interface die includes “circuitry, e.g., buffers, and I/O drivers, to accommodate the transfer of information at appropriate data transfer rates.” Keeth ’552, 3:63-67. A person of ordinary skill would have known how to implement “circuitry … to accommodate … appropriate data rates,” including parallel-to-serial and serial-to-parallel conversion circuits. *See, e.g.*, Riho ’364, [0053].

Implementing Riho ’364’s techniques in the Keeth ’552-Shaeffer ’507 combination was well within a person of ordinary skill’s ordinary skill, and a person of ordinary skill would have had a reasonable expectation of success in doing so. For example, Riho ’364 teaches specific implementations for the buffer circuit using different number of transistors and/or transistors of different sizes to achieve a range of available drive capacities. *See, e.g.*, Riho ’364, [0097]-[0098], Fig. 7A. A person of ordinary skill would have also understood that this range of available drive capacities can be selected, for example, by using computer-aided design tools for a specific design, such as the Keeth ’552-Shaeffer ’507 combination. *See, e.g.*, Shaeffer ’507, 12:28-29. A person of ordinary skill would have also understood that the selection of Riho ’364’s buffer transistors can be implemented not just by ROMs but also by other known techniques, such as anti-fuses or breaking connections. *See, e.g.*, Riho ’364, [0041]; Wyman ’192, 5:34-44.

5.1.2.4. Secondary Considerations

Defendants are not aware of any secondary-considerations evidence demonstrating non-obviousness of the Asserted Claims of the ’087 Patent. Indeed, Plaintiff has not identified any such secondary considerations, let alone demonstrated a nexus between any such considerations and the alleged inventions of the Asserted Claims.

As discussed in Appendix A, the prior art references confirm that the Asserted Claims of the ’087 Patent would have been obvious to a person of ordinary skill before the earliest possible priority date. Defendants reserve the right to supplement or modify these contentions to address any evidence or arguments later identified by Plaintiff.

5.2. ’731 Patent

In view of the apparent scope of the Asserted Claims of the ’731 Patent as advanced in Plaintiff’s Infringement Contentions, the limitations of the Asserted Claims would have been at least obvious, if not anticipated, by the prior art references identified below and discussed herein

and in Exhibits B-1 through B-23. *See, e.g., 01 Communique Lab., Inc. v. Citrix Sys., Inc.*, 889 F.3d 735, 742 (Fed. Cir. 2018).

5.2.1. Anticipation

The Asserted Claims are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the Asserted Claims of the '731 Patent in the invalidity claim charts of Exhibits B-1 through B-23 (collectively "Appendix B") which are hereby incorporated by reference as if fully set forth herein. The invalidity claim charts of Appendix B provide an explanation showing how these prior art references teach or suggest each and every element of the Asserted Claims of the '731 Patent.

5.2.2. Obviousness

In addition to certain claims being anticipated at least under Plaintiff's apparent claim constructions as indicated above, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation. Further, the Asserted Claims are obvious over various combinations of the references shown in the claim charts accompanying or incorporated by reference in this disclosure. No Asserted Claim goes beyond combining known elements to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Thus, to the extent that an Asserted Claim is not anticipated, it is nevertheless invalid as obvious. Specifically, Defendants assert that any charted or incorporated reference in combination with one or more other charted or incorporated references renders the Asserted Claims obvious.

5.2.2.1. Level of Ordinary Skill in the Art

To assess the level of ordinary skill of a person of ordinary skill, the following factors can be considered: (i) the type of problems encountered in the art; (ii) the prior solutions to those

problems; (iii) the rapidity at which innovations are made; (iv) the sophistication of the technology; and (v) the level of education of active workers in the relevant field.

Based on the foregoing, Defendants contend that a person of ordinary skill for the ’731 patent would have had an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. Such a person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. A person of ordinary skill would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs, and more low-level circuits such as tri-state buffers. Examples of JEDEC standards that a person of ordinary skill would have been familiar with include: JESD79 for DDR1 memory (2000); JESD79-2 for DDR2 memory (2004/2005); JESD79-3 for DDR3 memory (2007); and JEDEC 21-C for memory modules (2002).

5.2.2.2. Identification of Obviousness Contentions

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Exhibits B-1 through B-23 the prior art references that render obvious the Asserted Claims of the ’731 Patent and include below exemplary and non-exhaustive combinations showing the obviousness of the Asserted Claims in view of the prior art. Defendants reserve the right to rely on any combination of the references reflected in their charts or incorporated herein by reference. The combinations of prior art listed below render obvious the Asserted Claims under the proper construction of the claims and/or under Plaintiff’s apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Exhibits B-1 through B-23, the limitation would

have been obvious in light of the disclosures within the reference and the knowledge of one of skill in the art at the time of the ’731 Patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Exhibits B-1 through B-23, such reference may be combined with any other references listed in Exhibits B-1 through B-23 for such element, thereby rendering the claim invalid for obviousness.

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Exhibits B-1 through B-23, along with the knowledge of one of ordinary skill in the art, to meet the limitations of the Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants’ inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

In addition, a person of ordinary skill in the art would have been motivated to combine the prior art references because the elements found in the Asserted Claims of the ’731 patent are well known in the art.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent claim was known by a person of ordinary skill in the art at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the

combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided below, Defendants reserve the right to rely on the disclosure of the references listed in Appendix B for additional motivation to combine. The below-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the below-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

For at least the reasons described below, it would have been obvious to a person of ordinary skill in the art to combine each prior art reference listed in Appendix B with any other reference or references listed in Appendix B along with the knowledge of one of ordinary skill in the art to arrive at the claimed inventions in the '731 patent. For example, and without limitation, the Asserted Claims of the '731 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor / Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
U.S. Patent App. Pub. No. 2006/0277355 (Ellsberry '355) (B-1)	• U.S. Patent No. 7,020,818 (Dour '818) (B-2) • U.S. Patent App. Pub. No. 2008/0218290 (Abadeer '290) (B-3) • U.S. Patent App. Pub. No. 2004/0222834 (Frans '834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae '155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen '071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak '196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains '951) (B-8)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2009/0237109 (Haig '109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee '837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon '353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen '214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh '084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen '528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui '151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd '338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis '464) (B-22) • U.S. Patent No. 8,391,347 (Kim '347) (B-23) •
U.S. Patent App. Pub. No. 2006/0106951 (Bains '951) (B-8)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans '834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae '155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen '071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak '196) (B-7) • U.S. Patent No. 7,646,213 (Kao '213) (B-9) • U.S. Patent No. 6,356,106 (Greeff '106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee '519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park '845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig '109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee '837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon '353) (B-15)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent No. 7,646,213 (Kao ’213) (B-9)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
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U.S. Patent No. 6,356,106 (Greeff ’106) (B-10)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
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U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent App. Pub. No. 2003/0126338 (Dodd ’338) (B-20)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh ’084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen ’528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui ’151) (B-19) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis ’320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22) • U.S. Patent No. 8,391,347 (Kim ’347) (B-23)
U.S. Patent App. Pub. No. 2007/012646 (Vergis ’464) (B-22)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans ’834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae ’155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen ’071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak ’196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains ’951) (B-8) • U.S. Patent No. 7,646,213 (Kao ’213) (B-9) • U.S. Patent No. 6,356,106 (Greeff ’106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee ’519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park ’845) (B-12) • U.S. Patent App. Pub. No. 2009/0237109 (Haig ’109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee ’837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon ’353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen ’214) (B-16)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2007/0279084 (Oh '084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen '528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui '151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd '338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320) (B-21) • U.S. Patent No. 8,391,347 (Kim '347) (B-23)
U.S. Patent No. 7,253,655 ("Kwon '655") (B-24)	• U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,947,304 ("Yen '304") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 7,624,244 ("Yung '244") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,947,304 ("Yen '304") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 6,493,250 ("Halbert '250") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,947,304 ("Yen '304") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 6,658,509 ("Bonella '509") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,947,304 ("Yen '304") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 8,924,680 ("Perego '680") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244")

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U.S. Patent No. 7,363,422 ("Perego '422") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 6,947,304 ("Yen '304") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 6,947,304 ("Yen '304") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,529,422 ("Mazumder '422")
U.S. Patent No. 6,529,422 ("Mazumder '422") (B-24)	• U.S. Patent No. 7,253,655 ("Kwon '655") • U.S. Patent No. 7,624,244 ("Yung '244") • U.S. Patent No. 6,493,250 ("Halbert '250") • U.S. Patent No. 6,658,509 ("Bonella '509") • U.S. Patent No. 8,924,680 ("Perego '680") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,947,304 ("Yen '304")
U.S. Patent No. 7,227,376 ("Ahmad '376") (B-27)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans '834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae '155) (B-5) • U.S. Patent App. Pub. No. 2007/0139071 (Nguyen '071) (B-6) • U.S. Patent App. Pub. No. 2004/0228196 (Kwak '196) (B-7) • U.S. Patent App. Pub. No. 2006/0106951 (Bains '951) (B-8) • U.S. Patent No. 7,646,213 (Kao '213) (B-9) • U.S. Patent No. 6,356,106 (Greeff '106) (B-10) • U.S. Patent App. Pub. No. 2005/0135519 (Lee '519) (B-11) • U.S. Patent App. Pub. No. 2005/0040845 (Park '845) (B-12)

Patent No. or Title (Primary Inventor / Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
	• U.S. Patent App. Pub. No. 2009/0237109 (Haig '109) (B-13) • U.S. Patent App. Pub. No. 2004/0100837 (Lee '837) (B-14) • U.S. Patent App. Pub. No. 2005/0225353 (Kwon '353) (B-15) • U.S. Patent App. Pub. No. 2006/0158214 (Janzen '214) (B-16) • U.S. Patent App. Pub. No. 2007/0279084 (Oh '084) (B-17) • U.S. Patent App. Pub. No. 2004/0098528 (Janzen '528) (B-18) • U.S. Patent App. Pub. No. 2003/0039151 (Matsui '151) (B-19) • U.S. Patent App. Pub. No. 2003/0126338 (Dodd '338) (B-20) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320) (B-21) • U.S. Patent App. Pub. No. 2007/012646 (Vergis '464) (B-22) • U.S. Patent No. 8,391,347 (Kim '347) (B-23)
Micron RLDRAM 2 Design Guide & JESD79-2 DDR2 SDRAM (B-25)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans '834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae '155) (B-5) • U.S. Patent App. Pub. No. 2005/0135519 (Lee '519) (B-11) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320) (B-21)
Samsung DDR2 Fully Buffered DIMM (B-26)	• U.S. Patent App. Pub. No. 2004/0222834 (Frans '834) (B-4) • U.S. Patent App. Pub. No. 2008/0089155 (Bae '155) (B-5) • U.S. Patent App. Pub. No. 2005/0135519 (Lee '519) (B-11) • U.S. Patent App. Pub. No. 2009/0010320 (Hollis '320) (B-21)

As mentioned above, Defendants have not yet completed its search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those

claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude it from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

5.2.2.3. Obviousness Rationales

Motivations to combine, as well as the general state of the art, may be found in a variety of places including in the references defined above, and the specification of the '731 Patent. For example, each piece of prior art relates to the design and/or structure and/or function of optoelectronic devices. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein to practice the Asserted Claims and there was a motivation in the art to make such a combination.

Motivations to combine various prior art references are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the '731 Patent. Further reasons to combine the references identified in these charts include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of optoelectronic devices that such combinations would have yielded predictable results, and the fact that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007); *see also id*. at 401 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id*. at 427. The Supreme Court held that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id*. at 401.

Moreover, the Supreme Court recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id*. at 402 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 402-03.

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 417. If a person of ordinary skill can implement a predictable variation, U.S.C. § 103 bars its patentability. *Id*. The rationale to combine or modify prior art references is significantly stronger when

references seek to solve similar problems, come from the same field, and correspond well with one another. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them. Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination.

These disclosures are provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any Invalidity Contentions. Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Plaintiff may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Defendants reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the ’731 Patent.

One or more combinations of the prior art references identified in Exhibits B-1 through B-23 would have been obvious because these references would have been combined using a simple substitution of one known, equivalent element for another to obtain predictable results and/or a

teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Exhibits B-1 through B-23 would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Exhibits B-1 through B-23, along with the knowledge of one of ordinary skill in the art, to meet the limitations of the Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent claim was known by a person of ordinary skill in the art at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the

combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

As mentioned above, Defendants have not yet completed its search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude it from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

All Asserted Claims are directed to memory modules using a switching circuit to "selectively [and] operatively couple one or more ports" to memory devices, where the ports comprise a "correction circuit which reduces noise in one or more signals transmitted" to the circuit. *See* '731 patent, Abstract, 1:48-50, 4:7-9, Fig. 5. Such technology was widely known before the alleged priority date of the '731 Patent. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-22 (Vergis '464).

Using correction circuits in memory modules was a well-known solution to the problem of reducing noise and signal degradation due to impedance mismatches. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-2 (Dour '818), B-3 (Abadeer '290), B-4 (Frans '834), B-5 (Bae '155), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16

(Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-23 (Kim ’347).

5.2.2.3.1 Independent Claim 1

1[a]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could be operable to communicate data with a system memory controller via a bus in response to address and command signals from the system memory controller. *See, e.g.*, B-1 (Ellsberry ’355), B-2 (Dour ’818), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[b]. It was well known to one of skill in the art before the priority date of the ’731 Patent to have a printed circuit board comprising at least one connector configured to be operatively coupled to the memory bus, the connector including edge connections distributed along the edges of the printed circuit board. *See, e.g.*, B-1 (Ellsberry ’355), B-2 (Dour ’818), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[c]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a plurality of memory devices on a printed circuit board arranged in multiple ranks, where each rank comprises an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.

See, e.g., B-1 (Ellsberry ’355), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[d]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise at least one circuit between the connector and plurality of memory devices that comprises a first set of port connections coupled to the edge connections and a second set of port connections coupled to the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[e][1]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a correction circuit configured to make corrections in one or more signals transmitted between port connections. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-4 (Frans ’834), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego

’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[e][2]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a correction circuit that includes a programmable impedance matching circuit. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-2 (Dour ’818), B-3 (Abadeer ’290), B-4 (Frans ’834), B-5 (Bae ’155), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[f][1]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a control circuit configured to receive address and control signals from the system memory controller and to control the plurality of memory devices in response to the address and control signals. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-2 (Dour ’818), B-3 (Abadeer ’290), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

1[f][2]. It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could have control circuitry configured to dynamically control the

programmable impedance matching circuit based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-2 (Dour '818), B-3 (Abadeer '290), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-22 (Vergis '464), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 1:

- Claim 1 is obvious in view of any one of Exhibits B-1, B-7–B-10, B-17–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-4, B-6, B-8–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-4, B-6, B-7, B-9, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-4, B-6–B-9, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-16, B18–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-17, B19–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509,

Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 1 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.1 Dependent Claim 2

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise an impedance matching circuit that has dynamically programmable impedances whose values may differ depending on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-2 (Dour ’818), B-4 (Frans ’834), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304,

Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 2:

- Claim 2 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2, B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2, B-4, B-6, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 2 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 2 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 2 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in

Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with dynamically programmable impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.2 Dependent Claim 3

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise an impedance matching circuit that includes at least one network of programmable resistors and the network is dynamically controllable. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-2 (Dour ’818), B-4 (Frans ’834), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 3:

- Claim 3 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2, B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2, B-4, B-6, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2, B-4, B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-17, B-18, B-19, B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 3 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 3 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with

dynamically programmable impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.3 Dependent Claim 4

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise a correction circuit that includes one or more self-adjusting damper circuits. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-2 (Dour '818), B-3 (Abadeer '290), B-4 (Frans '834), B-5 (Bae '155), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 4:

- Claim 4 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-14 B-16–B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-6, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-6, B-7, B-9, B-10, B-12–B-14, B-16, B-17, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 4 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-10, B-12–B-14, B-16, B-17, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-12–B-14, B-16, B-17, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-17, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-18, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-19, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-18, B-20, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-18, B-19, B-21–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-6, B-7, B-8, B-9, B-10, B-12–B-14, B-16, B-17, B-18, B-19, B-21, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-25 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-26 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 4 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 4 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and damper circuits integrated into discrete memory

buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.4 Dependent Claim 5

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise a correction circuit that includes one or more dynamically programmable repeater/amplifier elements. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-4 (Frans '834), B-5 (Bae '155), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 5:

- Claim 5 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4, B-5, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4, B-5, B-7, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4, B-5, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 5 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 5 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and programmable amplifier/repeater circuits integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.5 Dependent Claim 6

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a correction circuit that includes a delay circuit that is configured to generate delayed versions of the signals transmitted between the respective port connections. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-4 (Frans ’834), B-5 (Bae ’155), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-11 (Lee ’519), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-16 (Janzen ’214), B-17 (Oh ’084), B-18

(Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-23 (Kim ’347), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 6:

- Claim 6 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4–B-6, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4–B-6, B-7, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-18, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-19, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-20, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-21, B-22, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 6 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 6 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in

Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and programmable amplifier/repeater circuits integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.6 Dependent Claim 7

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise port connections, wherein the number of port connections in the first set of port connections corresponds to a bit width of the memory bus. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-23 (Kim ’347), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 7:

- Claim 1 is obvious in view of any one of Exhibits B-1, B-7–B-10, B-17–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 1 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-4, B-6, B-8–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-4, B-6, B-7, B-9, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-4, B-6–B-9, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-16, B18–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-17, B19–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 1 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 7 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 7 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory

devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.7 Dependent Claim 8

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise a circuit that includes multiple physically separate integrated circuit packages, with circuit package having a data width corresponding to a data width of one of the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-12 (Park '845), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 8:

- Claim 8 is obvious in view of any one of Exhibits B-1, B-7–B-10, B-17–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-4, B-6, B-8–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-4, B-6, B-7, B-9, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 8 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-4, B-6–B-9, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-16, B18–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-17, B19–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 8 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 8 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.8 Dependent Claim 9

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise a circuit that includes multiple physically separate integrated circuit packages, with each package having a data width corresponding to a data width of multiple memory devices of the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21

(Hollis ’320), B-22 (Vergis ’464), B-23 (Kim ’347), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 9:

- Claim 9 is obvious in view of any one of Exhibits B-1, B-7–B-10, B-17–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-4, B-6, B-8–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-4, B-6, B-7, B-9, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-4, B-6–B-9, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-16, B18–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-17, B19–B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 9 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 9 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 9 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications,

including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.9 Dependent Claim 10

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise control circuitry configured to activate signal paths in each circuit in response to address and control signals. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-4 (Frans ’834), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-11 (Lee ’519), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 10:

- Claim 10 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 10 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4, B-6, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4, B-6, B-7, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is are obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 10 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 10 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and control circuitry integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.10 Dependent Claim 11

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise control circuitry, wherein the control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-4 (Frans '834), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-22 (Vergis '464), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 11:

- Claim 11 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4, B-7, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4, B-7, B-8, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 11 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 11 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 11 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and control circuitry integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.11 Dependent Claim 12

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise correction circuits, wherein each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements, and wherein the control circuitry is configured to activate the one or more circuit elements in response to the address and control signal. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-4 (Frans ’834), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10

(Greeff ’106), B-11 (Lee ’519), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 12:

- Claim 12 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4, B-6, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4, B-6, B-7, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is are obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-18, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-19, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-20, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-21, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4, B-6, B-7, B-8, B-9, B-10, B-11–B-14, B-16, B-17, B-18, B-19, B-20, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 12 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 12 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and control circuitry integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.12 Dependent Claim 13

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise circuits, wherein each circuit in the at least one circuit has a data width of 4, 8, or 16 bits. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 13:

- Claim 13 is obvious in view of any one of Exhibits B-1, B-7–B-10, B-17–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-2–B-4, B-6, B-8–B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 31 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-2–B-4, B-6, B-7, B-9, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-2–B-4, B-6–B-8, B-10, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-2–B-4, B-6–B-9, B-12–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-16, B18–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-17, B19–B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-2–B-4, B-6–B-10, B-12–B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 13 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 13 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with

impedance matching resistive networks having specific data widths integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.13 Dependent Claim 14

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise one circuit, wherein the at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-4 (Frans '834), B-5 (Bae '155), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 14:

- Claim 14 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4–B-6, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 14 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4–B-6, B-7, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-25 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-26 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 14 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 14 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory

devices themselves for improved signal integrity, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.14 Dependent Claim 15

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise at least one circuit, wherein the at least one circuit is configured to improve timing of signals transmitted between the at least one connector and the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-4 (Frans '834), B-5 (Bae '155), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 15:

- Claim 15 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4–B-6, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4–B-6, B-7, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 15 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-25 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-26 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 15 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 15 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves for improved signal timing, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.15 Dependent Claim 16

It was well known to one of skill in the art before the priority date of the '731 Patent that a memory module could comprise at least one circuit, wherein the at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices. *See, e.g.*, Exs. B-1 (Ellsberry '355), B-3 (Abadeer '290), B-4 (Frans '834), B-5 (Bae '155), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-21 (Hollis '320), B-22 (Vergis '464), B-23 (Kim '347), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 16:

- Claim 16 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-3–B-6, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-3–B-6, B-7, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.
- Claim 16 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-3–B-6, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-21, B-22 B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-25 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-26 in view of at least one of Exhibits B-4, B-5, B-11, B-21, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 16 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 16 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks integrated into discrete memory buffers or the memory devices themselves for improved power consumption, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.16 Dependent Claim 17

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise at least one circuit, wherein the at least one circuit includes signal

paths, wherein the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals. *See, e.g.*, B-1 (Ellsberry '355), B-4 (Frans '834), B-6 (Nguyen '071), B-7 (Kwak '196), B-8 (Bains '951), B-9 (Kao '213), B-10 (Greeff '106), B-11 (Lee '519), B-12 (Park '845), B-13 (Haig '109), B-14 (Lee '837), B-15 (Kwon '353), B-16 (Janzen '214), B-17 (Oh '084), B-18 (Janzen '528), B-19 (Matsui '151), B-20 (Dodd '338), B-22 (Vergis '464), B-24 (Kwon '655, Yung '244, Halbert '250, Bonella '509, Perego '680, Perego '422, Yen '304, Mazumder '422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad '376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 17:

- Claim 17 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4, B-7, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4, B-7, B-8, B-10, B-11–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-11–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.
- Claim 17 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4, B-7, B-8, B-9, B-10, B-11–B-16, B-17, B-18, B-19, B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 17 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509,

Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 17 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and control circuitry integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

5.2.2.3.1.17 Dependent Claim 18

It was well known to one of skill in the art before the priority date of the ’731 Patent that a memory module could comprise at least one circuit, wherein the at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections that is not in an active signal path. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-4 (Frans ’834), B-5 (Bae ’155), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-22 (Vergis ’464), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509,

Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

Defendants propose at least the following combinations of prior art references that render obvious the limitations of claim 18:

- Claim 18 is obvious in view of Exhibit B-1 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-7 in view of at least one of Exhibits B-4–B-6, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-8 in view of at least one of Exhibits B-4–B-6, B-7, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-9 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-10, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-10 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-12–B-16, B-17, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-17 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-18, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-18 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-19, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-19 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-20, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-20 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-22, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-22 in view of at least one of Exhibits B-4–B-6, B-7, B-8, B-9, B-10, B-12–B-16, B-17, B-18, B-19, B-20, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-27 in view of at least one of Exhibits B-4–B-23, and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Kwon ’655) in view of any one of the other references in Exhibit 24 (Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Yung ’244) in view of any one of the other references in Exhibit 24 (Kwon ’655, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Halbert ’250) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Bonella ’509) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Perego ’680) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’422, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Perego ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Yen ’304, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Yen ’304) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Mazumder ’422), and the knowledge of a person of ordinary skill in the art.

- Claim 18 is obvious in view of Exhibit B-24 (Mazumder ’422) in view of any one of the other references in Exhibit 24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304), and the knowledge of a person of ordinary skill in the art.

The prior art combinations proposed for claim 18 could have made according to methods known to those of ordinary skill in the art within the field of the ’731 Patent to yield predictable results at the time of the alleged invention. As can be seen in the background art disclosed in Section 4.2, one of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to

select appropriate attributes of one reference for inclusion in another reference. One of ordinary skill in the art would have employed known techniques to improve similar prior art devices in the same way as claimed in the ’731 Patent. As seen in the applied references and the background references in Section 4.2, a memory module with multiple ranks of memory devices, with impedance matching resistive networks and control circuitry for providing known static impedances integrated into discrete memory buffers or the memory devices themselves, were well-known to one of ordinary skill in the art before the priority date of the alleged invention.

The prior art references provide motivations to combine because they describe the field of the ’731 Patent, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*, Exs. B-1 (Ellsberry ’355), B-2 (Dour ’818), B-3 (Abadeer ’290), B-4 (Frans ’834), B-5 (Bae ’155), B-6 (Nguyen ’071), B-7 (Kwak ’196), B-8 (Bains ’951), B-9 (Kao ’213), B-10 (Greeff ’106), B-11 (Lee ’519), B-12 (Park ’845), B-13 (Haig ’109), B-14 (Lee ’837), B-15 (Kwon ’353), B-16 (Janzen ’214), B-17 (Oh ’084), B-18 (Janzen ’528), B-19 (Matsui ’151), B-20 (Dodd ’338), B-21 (Hollis ’320), B-22 (Vergis ’464), B-23 (Kim ’347), B-24 (Kwon ’655, Yung ’244, Halbert ’250, Bonella ’509, Perego ’680, Perego ’422, Yen ’304, Mazumder ’422), B-25 (Micron TN-49-01 RLDRAM 2/JESD79-2), B-26 (Samsung DDR2 FBDIMM/JESD79-2/JESD82-20), B-27 (Ahmad ’376).

5.2.2.3.2 Specific Combinations of Prior Art References

Additional motivations to combine specific references are discussed below.

5.2.2.3.2.1 Ellsberry ’355 (B-2) in view of Dour ’818 (B-3)

A person of ordinary skill in the art would have been motivated to combine Ellsberry ’355 with Dour ’818. For example, a person of ordinary skill in the art would have been motivated to use the programmable on die termination functionality of Dour ’818—including the use of a

programmable impedance matching circuit at the switch and dynamically controlling it based on rank selection—in memory module of Ellsberry ’355 in order to “allow[] for faster transfer rates over [data] communication lines by reducing the time needed to recover from signal reflection and similar issues” as well as to achieve further advantages as discussed below. *See, e.g.*, Dour ’818, Abstract.

Ellsberry ’355 and Dour ’818 are analogous art to the ’731 Patent, because each is directed to methods for communicating with memory devices, and each is reasonably pertinent to the problem of improving signaling to allow for increased transmission speed. *See, e.g.*, ’731 Patent, 1:65-2:16, 4:18-55; Ellsberry ’355, [0001], [0031], [0057]; Dour ’818, Abstract, 1:8–11, 1:31–39, 3:11–19.

For example, Ellsberry ’355 discloses a memory module which includes a control unit 204 and memory bank switches 206 and 208 that interface with the memory devices (in Banks 0-3) via address and command (CMD) bus 220 from the control unit, and via data busses (*e.g.*, 234 and 236) from the memory bank switches. *See, e.g.*, Ellsberry ’355, [0030], Fig. 2. The memory devices in the memory module of Ellsberry ’355 do not directly interface with a system memory controller, which is coupled to the DIMM interface. *See, e.g.*, Ellsberry ’355, [0030], Fig. 2. Ellsberry ’355 discloses techniques for intercepting and adjusting signals from the host computer to the memory module to implement rank multiplication. *See, e.g.*, *Samsung Elecs., Co., Ltd. v. Netlist, Inc.*, IPR2022-00615, Paper 96 (P.T.A.B. Apr. 17, 2024), 37-51; Ellsberry ’355, Abstract, [0048]. As depicted in Figures 2, 5 and 6 of Ellsberry, this implementation requires that the controller 510/204 and switch 508/206 intercept communications from the host computer intended for the memory devices 504, 512/212, 214, 216, 218. *See, e.g.*, Ellsberry ’355, Figs. 2, 5, 6. The disclosure of Ellsberry ’355 improves on traditional RDIMMs by further including data buffers between the

RDIMMs' DRAM devices and the memory controller on the host, as well as additional functionality in the register (e.g., the Control ASIC). *See, e.g.*, Ellsberry '355, Figs. 5–6.

A person of ordinary skill in the art would have understood that the controller/switch devices, including the Switch ASICs, can implement functionalities of a controller, including the impedance related programming of the OCD and ODT functions for the interface to the memory devices. For example, Ellsberry '355 discloses a "squelch function [which] allows the memory devices to be configured to operate in conjunction with the controller/switch devices and host system, rather than be directly programmed by the host system." Ellsberry '355, [0044]. *See also* Ellsberry '355, Fig. 9. *Compare* Ellsberry '355, Fig. 9 *with* JESD79-2B, 12, Fig. 9. Using the squelch function of Ellsberry '355, the memory devices' off-chip driver (OCD) and on-die termination (ODT) resistance (Rtt) are not programmed by the host, and any such programming received from the host is "squelched." Ellsberry '355, [0044], Fig. 9. *See also* JESD79-2B, 12, Fig. 9, 14-20. Instead, the memories' OCD and ODT functionalities of Ellsberry '355 are programmed by the controller/switch devices on its module. Ellsberry '355, [0044], Fig. 9. *See also* JESD79-2B, 12, Fig. 9, 14-2.

Ellsberry '355 also teaches that new generations of memory devices are faster. *See, e.g.*, Ellsberry '355, [0046]. A person of ordinary skill in the art accordingly would have understood, for example from the JEDEC standards used in memory applications, and "incorporated [into Ellsberry '355] by reference," that the trend of increasingly faster operation would continue. *See, e.g.*, Ellsberry '355, [0050]; *see also* JESD79-2B, 66; JESD79-3, 147–150. A person of ordinary skill in the art would have also understood that reliable transmission at higher rates requires more accurate signal termination, considering factors such as sampling and slew rates. Accordingly, for this reason, JEDEC introduced the "ODT feature … designed to improve signal integrity of the

memory channel" in DDR2 memories and allowed programming to select from three different termination impedance values (Rtt). JESD79-2B, 12, 16–17, Fig. 15, 50. The ODT functionality in next-generation DDR3 memories in June 2007—*i.e.*, before the claimed priority date of the '731 Patent—allowed five different Rtt termination values for a feature called "Dynamic ODT." *See, e.g.*, JESD79-3, 22-23, 25, Figs. 7–8, 87–91. The JEDEC explained that Dynamic ODT was introduced because "to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command." JESD79-3, 87.

Therefore, a person of ordinary skill in the art would have recognized the importance of proper signal termination as speeds of memory operations increase. *See, e.g.*, Nguyen '200, Abstract. It was well known at the time of the claimed priority date of the '731 Patent that "[b]oth the driver [circuits 120 in die 105] and receiver circuits [125 in die 110] include termination elements [145 and 180, respectively, in Fig. 1 below,] that attempt to match the characteristic impedance of the transmission line … as impedance mismatches degrade signal quality and consequently reduce communication speed and reliability." *See id*., [0001]; *see also id.*, [0016]-[0023], Fig. 1. A person of ordinary skill in the art would have recognized the need for an "ODT control system [130 and 187, in the transmitter and receiver, respectively, each of which] … calibrates and maintains termination resistances and drive currents to produce optimal output swing voltages." *See id*., Abstract.

As discussed above, the controller/switch devices of Ellsberry '355 interface with the memory devices and already include OCD and ODT functionalities, which adjust impedance for proper data transmission to and from the memory devices. *See, e.g.*, Ellsberry '355, [0046]. Accordingly, a person of ordinary skill in the art would have been motivated to search for methods

to implement improved signal termination functionalities in the memory module of Ellsberry '355 in order to provide reliable data transmission at the higher transmission speeds expected in 2008 at the time of the claimed priority date of the '731 Patent.

Dour '818 solves this issue by teaching that "terminating signals with a programmable on die termination circuit to maximize transfer rates." Dour '818, 1:8–11. Dour '818 discloses an "on die termination circuit [that] may be programmed to compensate for environmental conditions and the physical characteristics of the device …[and] allows for faster transfer rates over communication lines by reducing the time needed to recover from signal reflection and similar issues." Dour '818, Abstract. Accordingly, a person of ordinary skill in the art would have been motivated to implement on-die termination functionality of Dour '818 into the Switch ASICs of Ellsberry '355 to terminate properly the data signals received from the memory devices as discussed below. For example, Dour '818 discloses that "a receiving circuit must terminate an incoming or received signal to prevent reflection of the signal and noise on communication line 205. A receiving device such as memory controller 213 may utilize a set of resistors 207 to terminate the incoming signal. Resistor 207 must have a resistance of appropriate size to terminate the signal properly." Dour '818, 3:11–19; *see also id.*, Fig. 2. The data signals from the memory devices in Ellsberry '355 are received by the Switch ASICs (which already implement various interface functionalities of a memory controller). Accordingly, a person of ordinary skill in the art would have been motivated to implement on-die termination functionality of Dour '818 into the "receiving device[s]" of Ellsberry '355 (i.e., the Switch ASICs) in order "to terminate the signal properly." *See* Dour '818, 3:11–19.

A person of ordinary skill in the art would have further recognized that there are advantages in programmable ODT solutions of Dour '818 over other techniques. For example, Dour '818

teaches that the "behavior of known on die termination circuits is undesirable because it does not maintain a constant relationship between current I and voltage V during periods of voltage change 301 to minimize signal reflection and maximize the signaling rate of a communication line." *See* Dour '818, 3:20–36, Fig. 3A. In contrast, Dour '818 discloses a "programmable on die termination…where the on die termination has been calibrated for the conditions of the chip[, a] transition period of the signal 303 exhibits a constant resistance . . . [which] facilitates the termination of the signal as the strength of the signal is fully absorbed by the on die termination circuit. This allows higher communication speeds on the communication line." *See, e.g.*, Dour '818, 3:37–58, Fig. 3B. Accordingly, a person of ordinary skill in the art would have been motivated to use the on-die termination functionality of Dour '818 in the Switch ASICs of Ellsberry '355 to terminate data signals from the memory devices in order to achieve such "higher communication speeds."

Additionally, a person of ordinary skill in the art would have recognized that the teachings of Dour '818 are further advantageous because its on-die termination can be calibrated for conditions "such as the quality and type of manufacture, materials and similar physical characteristics, temperature, voltage and similar device conditions," also referred to as "physical characteristics, voltage levels, and temperatures (PVT)." *See* Dour '818, 3:59–4:20, Fig. 4. For example, a "testing circuit 401" can determine conditions in the device and "encode the conditions in a signal . . . used by compensation circuits to adjust the operation of other blocks in the device to correct for conditions in the device and thereby improve the performance of the device." *Id*., 3:59–4:20. Such a testing circuit "may have a more precise encoding of the conditions," thus it may provide a better signal termination. *Id*., 4:21–35. These advantages would have further

motivated a person of ordinary skill in the art to use the on-die termination functionality of Dour ’818 in the Switch ASICs of Ellsberry ’355.

Moreover, a person of ordinary skill in the art would understand that dynamically adjusting the on-die termination circuit advantageously maintains the proper termination, therefore preventing signal reflections and minimizing noise, even if the PVT conditions change, therefore providing additional motivation to use the on-die termination functionality of Dour ’818 in the Switch ASICs of Ellsberry ’355 to properly terminate the data signals from the memory devices. For example, Dour ’818 discloses an “[o]n die termination circuit 500 [which] may absorb the incoming signal to prevent the reflection of the signal and to minimize noise on the communication line.” *See* Dour ’818, 4:36–44, Fig. 5. Dour ’818 further discloses that the PVT “conditions may change dynamically and driver signal 501 may dynamically alter the resistance of the on die termination circuit 500 accordingly.” *See id*., 5:23–29. Additionally, a person of ordinary skill in the art would understand, based on the disclosure of Dour ’818, that dynamically adjusting the on-die termination circuit advantageously maintains the proper termination and thus prevents signal reflections and minimizes noise, even if the PVT conditions change. Accordingly, a person of ordinary skill in the art would have been further motivated to use the on-die termination functionality of Dour ’818 in the Switch ASICs of Ellsberry ’355 to properly terminate the data signals from the memory devices.

Making the Ellsberry-Dour combination would have been well within a person of ordinary skill in the art’s skill at the time of the claimed priority date of the ’731 Patent as evidenced by the prior arts’ disclosures. As discussed, it was well known, and indeed standardized, to implement impedance matching functionalities, including dynamic ODT, in memory devices. A “control system … to account for process, voltage, and temperature variations that affect the resistance

values of termination elements" was also well known. *See, e.g.*, Nguyen '200, [0023]. Ellsberry '355 discloses impedance adjusting functions in its Switch ASICs and Dour '818 details the implementation of its on-die termination circuit. Additionally, Ellsberry '355 discloses that an application specific integrated circuit (ASIC) can implement the functionalities of both the memory bank switch and control unit "on a single die." *See, e.g.*, Ellsberry '355, [0038]. It was well known at the time of the claimed priority date of the '731 Patent to implement a memory controller's functionalities, including enhanced impedance control, by a buffer device that interfaces with the memories on the module. *See, e.g.*, Murtagh '466, Abstract. Accordingly, a person of ordinary skill in the art would have understood from the teachings of Ellsberry '355 that the functionalities of the memory bank switch of Ellsberry '355 and the on-die termination of Dour '818 can also be implemented on a single ASIC die with a reasonable expectation of success.

5.2.2.3.2.2 Ellsberry '355 (B-2) in view of Dour '818 (B-3), and in further view of Abadeer '290 (B-4)

A person of ordinary skill in the art would have been motivated to combine Ellsberry '355 with Dour '818 and with Abadeer '290. For example, a person of ordinary skill in the art would have been motivated to use Abadeer '290's automatic impedance matching functionality in the memory module of the Elsberry-Dour combination "in order to maximize the power transfer and minimize reflections from the load," "reduce[] or eliminate[] voltage overshoot and undershoot," and avoid "degradation of device reliability and reduction of device reliability margins" when "operating at a very high frequency, especially in the gigahertz (GHz) frequency range," and to achieve additional advantages as discussed below in detail. *See, e.g.*, Abadeer '290, [0002], [0014], [0016].

Ellsberry '355 and Dour '818 are analogous art to the '731 Patent, as discussed above, because each is directed to techniques for communicating with memory devices, and each is

reasonably pertinent to the problem of improving signaling to allow for increased transmission speed. Likewise, Abadeer ’290 is directed to “CMOS technologies operating at a very high frequency,” which a person of ordinary skill in the art would have understood as including memory devices at the time of the claimed priority date of the ’731 Patent. *See, e.g.*, Abadeer ’290, [0002]. *See also* Micron DDR2 SDRAM Datasheet. Abadeer ’290 is also pertinent to the problem of improving signaling for communicating with such memory devices. *See, e.g.*, Abadeer ’290, [0002]. Accordingly, Abadeer ’290 is analogous art, and a person of ordinary skill in the art would have considered Abadeer ’290’s teachings to further improve signal integrity and transmission speed in a module according to the Ellsberry-Dour combination.

For example, Abadeer ’290 discloses that “[a]utomatic impedance matcher … may operate across one or more frequency ranges” to avoid voltage overshoots and undershoots. Abadeer ’290, [0002], [0017]. Accordingly, a person of ordinary skill in the art would have been motivated to implement the functionality of Abadeer ’290’s automatic impedance matcher in a memory module according to the Ellsberry ’355-Dour ’818 combination in order to match the impedances “across one or more frequency ranges” and avoid over and undershooting. A person of ordinary skill in the art would have been motivated to use the functionality of Abadeer ’290’s impedance matcher because it performs frequency-based impedance matching automatically: “Within automatic impedance matcher 104, capacitive matching can be achieved electronically by sensing the frequency of the incoming driver signal … and automatically providing the appropriate matching capacitance.” Abadeer ’290, [0017]. A person of ordinary skill in the art would have understood that the memory module of Ellsberry ’355 can use memory devices capable of operating at a wide range of data rates, including DDR2 SDRAMs capable of operating at 400MHz, 667MHz, and 800MHz, and DDR3 SDRAMs capable of operating at 800MHz, 1066MHz, 1333MHz, and

1600MHz. *See, e.g.*, JESD79-2B, 66; JESD79-3, 147–150. Using its automatic operation, Abadeer '290's impedance matcher can match the impedances without external fine tuning or training even when the memory module according to the Ellsberry-Dour combination operates at different frequencies.

Implementing the functionality of Abadeer '290's automatic impedance matcher in a memory module according to the Ellsberry-Dour combination would have been within a person of ordinary skill in the art's ordinary skill at the time of the claimed priority date of the '731 Patent. Ellsberry '355 teaches that its memory bank switch interfaces with the memory devices and can be implemented in an application specific circuit (ASIC) that can, but does not have, to include control functionalities on a single die. *See, e.g.*, Ellsberry '355, [0038]. Accordingly, a person of ordinary skill in the art would have recognized that the automatic impedance matching functionality of Abadeer '290 can also be implemented in the Switch ASIC of Ellsberry '355, *e.g.*, in the interface with the memory devices to avoid over and undershooting in the data signals. Additionally, Abadeer '290 provides detailed teachings about implementing and operating its automatic impedance matcher. *See, e.g.*, Abadeer '290, Figs. 2, 7. Abadeer '290 further teaches implementations of its automatic impedance matcher that operate in the frequency range of the memory devices at the time. *See, e.g.*, Abadeer '290, [0029]-[0030], Figs. 5, 6. Accordingly, for at least these reasons, it would have been obvious to implement the functionality of the automatic impedance matcher of Abadeer '290 into a memory module according to the Ellsberry-Dour combination.

5.2.2.4. Secondary Considerations

Defendants are not aware of any secondary-considerations evidence demonstrating non-obviousness of the Asserted Claims of the '731 Patent. Indeed, Plaintiff has not identified any such

secondary considerations, let alone demonstrated a nexus between any such considerations and the alleged inventions of the Asserted Claims.

As discussed in Appendix B, the prior art references confirm that the Asserted Claims of the ’731 Patent would have been obvious to a person of ordinary skill before the earliest possible priority date. Defendants reserve the right to supplement or modify these contentions to address any evidence or arguments later identified by Plaintiff.

6. P.R. 3-3(c) – Claim Charts

Pursuant to Patent Rule 3-3(c), Defendants provide invalidity claim charts, which identify disclosures in the references identified in Section IV *supra* as to the Asserted Claims, in the attached Appendix A (’087 Patent) and Appendix B (’731 Patent).

7. P.R. 3-3(d) – Other Grounds for Invalidity

7.1. ’087 Patent

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the ’087 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; and indefiniteness under 35 U.S.C. § 112, second paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff’s purported constructions of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendant’s Invalidity Contentions under 35 U.S.C. § 112 may depend, in part, on the Court’s claim construction, as well as Plaintiff’s alleged scope of the ’087 Patent’s Asserted Claims.

Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which it is presently aware.

7.1.1. Lack of Written Description Under 35 U.S.C. § 112, ¶ 1

The '087 Patent does not provide sufficient written description to establish that the named inventor was in possession of the alleged inventions recited in the Asserted Claims at the time the '087 Patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventor was in possession of the full scope of the claimed apparatus.

As discussed below, the specification of the '087 Patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements in the Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '087 Patent fails to sufficiently describe or enable them as required by 35 U.S.C. 112, ¶ 1.[5]

Term	Claim(s)
Combination of all recited claim elements	1-28
C/A terminals	1-8, 13-23
wherein the one or more C/A signals do not include any chip select signal	1-8, 18, 20-23, 25-28
wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies	6, 20-23

[5] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Claim(s)
wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies	1-8
wherein … the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies	9-12
the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies	13-19
wherein the control die is configured to receive signals from the first unidirectional interconnects … wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects	20-23
each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect	24-28
wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects	1-8
receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects	9-12
the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects	13-19
wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects	20-23
in response to the first set of C/A signals, … a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface	24-28
in response to the first set of C/A signals, … a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface	24-28

Term	Claim(s)
in response to the third set of C/A signals, … a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface	24-28
in response to the third set of C/A signals, … a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface	24-28
in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects	1-8
driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects	9-12
the control die is further configurable to, … in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects	13-19
wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects	20-23
in response to the second set of C/A signals, … the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects	24-28
in response to the second set of C/A signals, … a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect	24-28
in response to the fourth set of C/A signals, … the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects	24-28
in response to the fourth set of C/A signals, … a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect	24-28

7.1.1.1. There is No Written Description for All of the Claim Requirements Together (All Claims)

All the ’087 Patent’s Asserted Claims fail to satisfy the written description requirement for several reasons, as discussed below. First, there is no disclosure of the specific combination of all limitations required by each of the ’087 Patent’s independent claims, and caselaw prohibits patentees from “picking and choosing” among disclosures in the patent to cobble together written description based on hindsight and obviousness. *See, e.g.*, *Fujikawa v. Wattanasin*, 93 F.3d 1559, 1571 (Fed. Cir. 1996); *Regents of the Univ. of Minn. v. Gilead Scis., Inc.*, 61 F.4th 1350, 1357 (Fed. Cir. 2023); *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1349 (Fed. Cir. 2013); *Flash-Control, LLC v. Intel Corp*., 2021 WL 2944592, at *4 (Fed. Cir. July 14, 2021) (“A patent owner cannot show written description support by picking and choosing claim elements from different embodiments that are never linked together in the specification.”). Each independent claim of the ’087 Patent requires an extensive combination of limitations, as illustrated in the table below, that is nowhere described in the ’087 Patent:

Independent Claim	Words in Claim
1	1,005
9	870
13	1,070
20	693
23	797
24	1,075

See ’087 Patent, claims 1, 9, 13, 20, 23, 24. The ’087 Patent nowhere describes the specific combination claimed in the Asserted Claims. For example, Figure 2 of the ’087 Patent does not disclose the structure and signals claimed in the ’087 Patent’s claims. In Figure 2, 242 for command/address (C/A) signals is in electrical communication with all of the array dies 210,

contrary to the claimed structure where limitations 1[f]-1[g] prohibit electrical communication with some dies, and where limitation 1[l] also requires a unidirectional interconnect going down, among numerous other differences discussed below. Instead of disclosing the specific combination required by the '087 Patent's claims, the '087 Patent merely provides a "laundry list" disclosure that the Federal Circuit has repeatedly held does not satisfy the written description requirement. The '087 Patent states over 250 times that certain features "may" or "can" be included in "some" embodiments (without ever identifying any particular embodiment), *see, e.g.*, '087 Patent, 10:48, and then the '087 Patent emphasizes that "such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments," '087 Patent, 23:18-26. The '087 Patent therefore provides no evidence that the named inventor actually possessed the specific combination of limitations now recited in the Asserted Claims—instead the '087 Patent merely discloses a laundry list of possible limitations. Notably, none of the claims even include any limitations about reducing driver "load," even though that is part of the purported invention according to the '087 Patent's title, technical field, and summary of invention. *See, e.g.*, '087 Patent, title, 1:30-35, 2:61-62. It is clear that these claims were impermissibly drafted using hindsight, and not based on any combination of limitations that were actually described in the '087 Patent.

The '087 Patent refers to various possibilities that could be combined in over 100 million different ways. The table below has seven rows for seven different features disclosed in the patent, and each row has multiple options in the patent for that feature, resulting in over 100 million combinations. In contrast, the '087 Patent's claims recite an extraordinarily specific combination of features, as shown by just some of the claim requirements in the right column below, some of which are not disclosed (shown in red text) at all, as explained below.

Possibilities in the '087 Patent	Possible Embodiment(s) Claimed
Types of array dies – at least 6 possibilities: (1) DDR DRAM; (2) SDRAM; (3) flash; (4) SRAM; (5) GDDR SDRAM; or (6) other graphics memory. '087 Patent, 21:51-58.	1[b][1], 9[b][1], 13[b], 20[b], 23[b], 24[b] "DRAM dies"
Types of interconnects – at least 5 possibilities: (1) wire; (2) conducting rod; (3) conducting trace; (4) vias; or (5) through-silicon vias (TSVs) '087 Patent, 8:13-17	1[d][3], 9[b][3], 13[d], 20[d][3], 23[d][3], 24[e] "through silicon vias (TSVs)" or "TSVs"
Subsets of dies – at least 2 possibilities: (1) two subsets (Fig. 2) or six subsets (Fig. 3) '087 Patent, Figs. 2-3, 16:40-55	1[b][1], 9[b][1], 13[g], 20[f][1], 23[f][1] "a first [second] plurality of DRAM dies" or "a first [second] subset of the plurality of stacked DRAM dies"
Interconnect(s) with selective electrical communication to subset of dies – at least $2^6 = 64$ possibilities: The specification lists 6 signals, each of which may (or may not) be conveyed by interconnects in selective electrical communication with a subset of dies, but a list of specific possible combinations is not disclosed: (1) data; (2) command; (3) address; (4) chip select; (5) supply voltage; or (6) ground voltage '087 Patent, 10:32-59	1[f], 1[g], 1[h][1]. 1[i], 9[f][1], 9[g], 9[h], 9[i], 13[g], 13[h][1], 13[j], 13[k] both "data interconnects" and "C/A interconnects" in selective electrical communication (combination not disclosed) 20[f][1], 20[f][2] "data interconnects" in selective electrical communication
Bidirectional/unidirectional interconnects/conduits – at least $3^8 = 6{,}531$ possibilities: The specification discloses that the interconnects/conduits for the following 6 signals may (or may not) be either: (i) "bi-directional" or (ii) unidirectional going up (e.g., from the control die up to the array die(s)): (1) data, (2) command, (3) address, (4) chip select, (5) supply voltage, or (6) ground voltage. '087 Patent, 10:32-59. Additionally, the claims claim at least "first signals" (a 7th category of signals) and	1[d][1] command and/or address (C/A), unidirectional up; 1[c][2], 1[d][2] data, bi-directional; 1[l], 1[n], 1[p][1] "first signals" (not disclosed), unidirectional down (not disclosed); 1[m], 1[o], 1[p][2] "second signals" (not disclosed), unidirectional up; 9[d][1], 9[e][1] command and/or address (C/A), unidirectional up; 9[d][1], 9[e][1] data, bi-directional;

Possibilities in the ’087 Patent	Possible Embodiment(s) Claimed
“second signals” (an 8th category of signals), and further claim that at least the “first signals” are (iii) unidirectional going down (e.g., from the array die down to the control die), even though that is not disclosed in the specification. Therefore, in total, there may be at least 8 different signals through an interconnect/conduit, each of which may (or may not be) either (i) bi-directional, (ii) unidirectional up, or (iii) unidirectional down.	9[d][2], 9[j][1] “one or mor signals” (not disclosed), unidirectional down on “first unidirectional interconnects” (not disclosed) (not disclosed) 9[e][2], 9[j][2] “one or more signals” (not disclosed), unidirectional up on “second unidirectional interconnects”; 13[g], 13[h][1] data, bi-directional; 13[i] command and/or address (C/A, unidirectional up; 13[o], 13[q] “first signals” (not disclosed), unidirectional down (not disclosed); 13[p], 13[r] “second signals” (not disclosed), unidirectional up; 20[c][2], 20[d][2] data, bi-directional; 20[d][1] command and/or address (C/A), unidirectional up; 20[k], 20[l][1] “first signals” (not disclosed), unidirectional down (not disclosed); 20[k], 20[l][2] “second signals” (not disclosed), unidirectional up 23[d][2] data, bi-directional; 23[d][1] command and/or address (C/A), unidirectional up; 23[i]-23[k], 23[l][1], “first signals” (not disclosed), unidirectional down (not disclosed) 23[i]-23[k], 23[l][2] “second signals” (not disclosed), unidirectional up; 23[m][1], 23[m][2] supply, unidirectional up 24[c], 24[i], 24[l] data, bidirectional;

Possibilities in the ’087 Patent	Possible Embodiment(s) Claimed
	24[c], 24[h] command and/or address (C/A), unidirectional up (conduit); 24[j], 24[m][2], 24[o][2] “second” / “sixth” “signals” (not disclosed), unidirectional down (conduit) (not disclosed); 24[k], 24[n][2], 24[p][2] “fourth” / “eighth” “signals” (not disclosed), unidirectional up (conduit)
Whether the “C/A signals” do not include any “chip select signals” – at least 2 possibilities: (1) The specification discloses that “a chip select signal” may be part of a control signal that controls a driver for a data conduit to drive a signal to the array die corresponding to the chip select signal. ’087 Patent, 15:21-51. (2) Alternatively, the claims on the right claim controlling the data conduit with C/A signals that do not include any chip select signal	1[k][1]-1[k][2], 20[h][1]-20[h][2], 23[h][1]-23[h][2] “control respective states of the first data conduit and the second data conduit in response to one or more C/A signals … [that] do not include any chip select signal” (not disclosed)
Whether the “control die” does not include emulation logic – at least 2 possibilities: (1) the specification discloses a “control die” with logic to perform rank multiplication ’731 Patent, 22:19-21 (2) Alternatively, the claims on the right claim a control die that does not include emulation logic	20[m], 23[n] “the control die does not include emulation logic” (not disclosed)

As shown by the left-hand column above, there are at least 6×5×2×64×6561×2×2 = 100,776,960 possible combinations of features of the ’087 Patent. Here, where each claim recites a specific combination drawn from millions of different possibilities, the claims lack written description, as the Federal Circuit has repeatedly held. This alone is sufficient to invalidate all claims.

7.1.1.2. There is Also No Written Description for Specific Claim Limitations

7.1.1.2.1 *Unidirectional Interconnects / Conduits for Conducting Signals Down the Stack* (All Claims)

Each independent claim of the '087 Patent, and therefore all claims, require a unidirectional interconnect/conduit for conducting unspecified signals down the stack (e.g., that "conduct[s] signals from one or more DRAM dies … to the control die") and not for conducting any signals up the stack (e.g., "not configured to conduct any signal from the control die to any of the stacked DRAM dies"). *See* limitations 1[l], 9[d][2], 9[j][1], 13[o], 20[j], 20[k], 23[j], 23[k], 24[j]. The claimed unidirectional interconnect/conduit for conducting signals only down the stack is not disclosed in the specification.

The specification discloses unidirectional interconnects/conduits for transmitting command/address ("C/A" or "CA") and chip-select ("CS") signals up from the control die to the array die as shown by conduits 240 and 250, and die interconnects 242 and 252, in Figure 2. However, the specification lacks any disclosure of transmitting C/A or CS signals in the opposite direction, down the stack.

The specification also discloses that die interconnects "to transfer data" either (i) "may be bi-directional," or alternatively (ii) may be "separate die interconnects and corresponding data conduits … to transfer data to the array dies 210 and data from the array dies 210 to the control die 230" resulting in "double the number of die interconnects and data conduits," '087 patent, 9:7-17, but that does not provide written description for the claim language for at least two reasons.

First, the specification lacks any disclosure of the negative claim limitation requiring that the die interconnect is "not configured to conduct any signal from the control die to any of the stacked DRAM dies" as recited by limitation 1[l] and as similarly required by the other independent claims. *See* '087 Patent, 9[d][2], 9[j][1], 13[o], 20[j], 20[k], 23[j], 23[k]. "Silence is

generally not disclosure. If it were, then every later-added negative limitation would be supported so long as the patent makes no mention of it." *Novartis Pharms. Corp. v. Accord Healthcare, Inc.*, 38 F.4th 1013, 1017 (Fed. Cir. 2022) (citations omitted). Here, other possibilities were known in the prior art, so the silence in the specification cannot provide written description for this negative claim limitation. For example, nothing in the specification excludes a die interconnect from transferring data signals from a DRAM die to the control die during read operations and then transferring non-data signals from the control die to the DRAM die during other operations. Such a shared use of a connection for different functions was known at the time (e.g., GDDR4 SGRAM using RDQS lines for transmitting read data strobes during read operations from the DRAM to the controller and using the same RDQS lines for transmitting Data Bus Inversion signals from the controller to the DRAM during write operations). *See, e.g.*, Stone, 17-21. Moreover, given that bi-directional interconnects/conduits can transfer signals in the same direction as a unidirectional interconnect/conduit, two separate bi-directional interconnects/conduits can also transfer data signals as exactly described in the "alternative embodiments"—i.e., one bi-directional interconnect/conduit is "used to transfer data to the array dies 210" and the other bi-directional interconnect/conduit is "used to transfer data … from the array dies 210 to the control die 230" resulting in "double the number of die interconnects and data conduits." '087 Patent, 9:10-17. Given that either bi-directional or unidirectional interconnects/conduits could be used as described for the "alternative embodiments," the use of unidirectional interconnects/conduits in this disclosure is at most an obvious possibility.

Second, this disclosure about the die interconnects and conduits is expressly limited to interconnects/conduits that "transfer data." '087 Patent, 9:9-17. However, the claimed unidirectional interconnect/conduit going down is claimed separately from the die interconnects

for the "data signals" in limitation 1[d][2] (and related claims)—which the claims permit to be bi-directional. Therefore, the claimed signal conducted down through the unidirectional interconnect/conduit is not a read data signal buy rather is a signal "associated with the memory read operation" and a "set of C/A signals" in limitation 1[p][1] (and related claims). The specification does not disclose such a signal. For example, Netlist asserts that the claimed unidirectional interconnects going down to the control die can be for read "data strobes RDQS_t/RDQS_c," Complaint, 16, 42, 67-68, but that is nowhere disclosed in the '087 Patent (which does not mention strobes or DQS). Moreover, it was well known that signal lines like RDQS did not need to be unidirectional, thus highlighting the lack of written description for such a unidirectional interconnect. *See, e.g.*, Stone, 17-21. As discussed, the law prohibits "picking and choosing" among disclosures in the patent to cobble together written description based on hindsight and obviousness, and here there is no disclosure of unidirectional interconnects conducting any signals associated with a read command down to the control die in addition to the separately claimed interconnects for "data signals" that may be bi-directional. The same is true regarding the patent's discussion of Figure 3, which allows for the possibility that a die interconnect "may not be bi-directional," '087 Patent, 14:40-51, but again, does not disclose unidirectional interconnects conducting any signals associated with a read command down to the control die in addition to the separately claimed interconnects for "data signals" that may be bi-directional.

7.1.1.2.2 *Unidirectional First / Second / Fourth / Sixth / Eighth Signals* (All Claims)

The specification likewise fails to disclose "[first]/[second] signals," "one or more signals," "[second]/[sixth] signals," or "[fourth]/[eighth] signals," all of which are transferred via unidirectional interconnects/conduits (collectively the "Unidirectional Signals"), as required by all independent claims (and thus all claims). *See* claims 1[p][1], 1[p][2], 9[d][2], 9[e][2], 13[n],

20[l][1], 20[l][2], 23[l][1], 23[l][2], 24[m][2], 24[o][2], 24[n][2], 24[p][2]. Indeed, the unidirectional signals are claimed separately from "data signals" and "signals" having "at least 32 signals driven in parallel" (which includes data signals, '087 Patent, 15:12)—which the claims permit to be bi-directional. *See* claims 1[c][1], 9[b][2], 13[c], 20[c][1], 23[c][1], 24[c], 24[s][1]-24[s][4]. The Unidirectional Signals are further claimed separately from any chip-select signal (e.g., "signals to select [one] DRAM die") in 6[a]-6[b], 9[c], 13[l], 22[a]-22[b], 25[b]-25[e]. The claims require that a first set of unidirectional signals associated with a memory read operation are sent down in response to a separately claimed first set of C/A signals, *see* claims 1[p][1]. 9[d][2], 13[n], 20[l][1], 23[l][1], 24[m][2], 24[o][2], and require that a second set of unidirectional signals are sent up in response to separately claimed second set of C/A signals, *see* limitations 1[p][2], 9[e][2], 13[n], 20[l][2], 23[l][2], 24[n][2], 24[p][2]. The specification lacks any disclosure of this. Instead, the specification provides a "laundry list" of signals: "a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few." '087 Patent, 10:48-50. This does not satisfy the written description requirement because it does not disclose the specific claimed combination of signals and does not disclose which signals are bi-directional, unidirectional up, or unidirectional down.

7.1.1.2.3 *Fifth*, *Sixth*, and *Eighth Signals* (Claims 24-28)

The claimed "fifth signals" 24[o][1] are going because they are received by a conduit via the respective interconnect "in response to" 24[o][1] "a third set of C/A signals for a memory read operation" [24.l], but they are also "associated with" 24[o][1] a "second set of C/A signals for a memory write operation" 24[l]. The specification does not disclose any self-conflicting signals, like the "fifth signals," that are associated with a write operation (i.e., going up), but sent down from the array die to the control die, and that contradiction also renders the claims indefinite.

The claimed "sixth signals" 24[o][2] are unidirectional signals (as discussed above) received by the third conduits going down, 24[j], but they are "associated with" 24[o][2] a "second set of C/A signals for a memory write operation" going up 24[l]. The specification fails to disclose such a self-conflicting signal. The "sixth signals" are associated with both read and write operations, which is not disclosed. The claim also requires that the "sixth signals" are received by a "second subset of the third conduits" 24[o][2], "being a unidirectional conduit" 24[j], and driven by a "second subset of the second conduits" 24[s][4] "being a bidirectional conduit" 24[i]. But the specification does not disclose a signal that is received by a unidirectional conduit but driven by a bidirectional conduit, and all of these contradictory requirements render the claims indefinite.

The claimed "eighth signals" are "associated with the second set of C/A signals" 24[p][2], 24[l], and also with "the fourth set of C/A signals" 24[p][2], 24[l], 25[e]. But the specification does not disclose such a signal associated with two different operations, and the contradiction also renders the claim indefinite.

7.1.1.2.4 Multiple Types of Interconnects with Selective Electrical Communication (Claims 1, 9, 13, and 23)

The specification also fails to disclose the combination of at least two different types of interconnects (i.e., "C/A," "data," and "supply voltage"), where each type of interconnect is in selective electrical communication with DRAM dies (or ports on those dies), as required by independent claims 1, 9, 13, and 23 (and their dependents). *See* claims 1[f], 1[g], 1[h]1, 1[i], 9[f][1], 9[g], 9[h], 9[i], 13[g], 13[h][1], 13[j], 13[k], 23[f][1], 23[f][2], 23[m][1], 23[m][2]. Instead, the specification provides a "laundry list" of different interconnects for different signals that may (or may not) be in selective electrical communication: "in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array

die 310, which may be in electrical communication with a different die interconnect 320," '087 Patent, 10:21-26, and the "signal along a corresponding die interconnect 320" "can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few," '087 Patent, 10:35-36, 10:48-50. This does not satisfy the written description requirement, because it requires "picking and choosing" among many possible combinations in the patent to cobble together written description based on hindsight and obviousness. For example, Figure 3 of the patent only shows selective electrical communication for one type of interconnect (i.e., for the signal supplied by the buffer 340). The claims, however, require a specific combination involving selective electrical communication for at least two different types of interconnects (i.e., "C/A," "data," and "supply voltage") which is not disclosed by the '087 Patent. Selective electrical communication can provide the benefit of reducing electrical load, but it also has significant drawbacks, such as increasing chip size and complexity due to additional interconnects, conduits (and drivers), and control signals for them. Accordingly, a person of ordinary skill would not have automatically assumed that just because the '087 Patent discloses selective electrical communication for one type of signal (as suggested in Figure 3), that the named inventor actually invented a package with selective electrical communication for two different types of signals (as required by the claims of the '087 Patent). The specification provides no such disclosure, and in fact Figure 2 discloses the opposite (i.e., DQ data signals on die interconnects 220a and 220b that are in selective electrical communication, and CA signals on die interconnect 242 that are not in selective electrical communication). Moreover, there is no disclosure of the unusual requirement in claims 1 and 9 that there are "first" and "second" "C/A interconnects" in selective electrical communication with ports of the DRAM dies, but both the "first set of C/A signals" and the "second set of C/A signals" are conducted on the "first C/A

interconnects" (while other signals may be on the "second C/A interconnects"). *See* claims 1[d][1], 1[f]-1[g], 9[d][1], 9[e][1], 9[h]-9[i].

7.1.1.2.5 *C/A Signals* that *Do Not Include Any Chip Select Signal* (Claims 1, 18, 20, and 23)

The specification also does not disclose controlling the states of first and second data conduits in response to "C/A signals" that "do not include any chip select signal," as required by independent claims 1, 20, and 23 (and their dependents) and dependent claim 18. *See* claims 1[k][2], 20[h][2], 23[h][2], 18[a][2]. The specification provides affirmative examples of using the chip select signals, not prohibitions against including any chip select signal. '087 Patent, 16:5-12, 15:31-40. "Silence is generally not disclosure" of a negative limitation like this. Novartis, 38 F.4th at 1017.

During prosecution Netlist cited to the discussion of drivers 408a/404a and 408b/404b in Figure 4 as purportedly disclosing the claimed "C/A signals" that "do not include any chip select signal." '087 Patent FH, 721. However, the specification does not indicate whether or not the disclosed "command/address signal" excludes a chip select signal as required by the claims.'087 Patent, 15:32-37. Indeed, a chip-select signal in the fork-in-the-road configuration of Figure 4 is needed during read operations (i.e., going down) because the read drivers (408a and 408b) share the same output terminal (402), meaning only one read driver and one corresponding chip can be selected to drive read data at a time to the output terminal (402). During prosecution Netlist also cited to a separate embodiment where an external register device 812 provides "data path control signals" to "operate the data path control circuits" on the control die. '087 Patent FH, 771. But "picking and choosing" among embodiments does not satisfy the written description requirement. Moreover, according to the specification, the "data path control circuits" manage time slots to avoid data collisions among "multiple memory packages 820" sharing the same "data bus 818." '087 Patent, 21:31-40, Fig. 8. Therefore, the "data path control signals," which operates the "data

path control circuits," do not disclose controlling data drivers/conduits on the control die within a single DRAM package as claimed. Moreover, a person of ordinary skill would be familiar with chip-select signals as a command signal, *see, e.g.*, JESD79-3C, 13, so a person of ordinary skill would have had no reason to assume that chip-select signals would be excluded from the disclosed "command/address signals," '087 Patent, 22:1, as required by the claims.

7.1.1.2.6 *The Control Die Does Not Include Emulation Logic* (Claims 6, 20, and 23)

The specification also fails to disclose a "control die" that "does not include emulation logic" (a term nowhere in the specification) as required by the negative limitations in independent claims 20 and 23 (and their dependents) and dependent claim 6. *See* claims 20[m], 23[n], 6[c]. During prosecution Netlist cited to two different disclosures for two different embodiments to try to provide support for this negative limitation. '087 Patent FH, 772. However, the first disclosure does not mention emulation (or rank multiplication). '087 Patent, 9:52-64. And the second disclosure states, "[I]n some embodiments, the register device 812 may be configured to perform rank multiplication. In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication." '087 Patent, 22:18-21. However, that disclosure concerns the "JEDEC 3DS" embodiment in Figure 8, '087 Patent, 19:46-50, Fig. 8, and not the Figure 2 or 3 embodiment discussed in connection with several of the limitations above. As discussed, that does not satisfy the written description requirement because it requires "picking and choosing" among disparate disclosures in the patent to cobble together written description based on hindsight and obviousness. Furthermore, this disclosure supports including rank multiplication logic in the control die, not excluding emulation logic as required by the negative limitations in these claims. "Silence is generally not disclosure" of a negative limitation like this. Novartis, 38 F.4th at 1017.

7.1.1.2.7 *Wherein the Die Interconnects Further Include Second Unidirectional Interconnects Configured to Conduct Signals From the Control Die to One or More DRAM Dies of*

the Stacked DRAM Dies and Not Configured Conduct Any Signal from Any of the Stacked DRAM Dies to the Control Die **(Claims 1-8)**

Claims 1-8 of the '087 patent recites "second unidirectional interconnects." The specification does not disclose any unidirectional interconnects that transmit signals from an array die to the control die. Each of the embodiments illustrated in FIGS. 1-3 describe unidirectional interconnects that transmit signals in the opposite direction—*i.e.*, from the control die to the array dies—only.

Further, the specification does not disclose a prohibition on conducting or driving signals to the DRAM or array dies. "Silence is generally not disclosure" of a negative limitation. *Novartis Pharms. Corp. v. Accord Healthcare, Inc.*, 38 F.4th at 1017.

The specification states that data interconnects may be bi-directional or unidirectional. '087 patent at 9:7-17. But this does not provide written description support for the claimed "second unidirectional interconnects" because claim 1-8 also recite "data interconnects," which are separate and distinct from the claimed "second unidirectional interconnects." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) ("Where a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention.").

7.1.1.2.8 ***Wherein … the Second Unidirectional Interconnects are Not Configured to Conduct Any Signals From Any of the Stacked DRAM Dies*** **(Claims 9-12)**

The '087 patent lacks sufficient written description support for the claim limitation "the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies" in claims 9-12 for the same reasons as explained above.

7.1.1.2.9 ***The One or More of the First Unidirectional Interconnects are Configured to Conduct the One or More First Signals from the First DRAM Die to the Control Die***

and Not Configured to Conduct Any Signal From the Control Die to Any of the Plurality of Stacked DRAM Dies **(Claims 13-19)**

The ’087 patent lacks sufficient written description support for the claim limitation “the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies” in claims 13-19 for the same reasons as explained above.

7.1.1.2.10 ***Wherein the Control Die is Configured to Receive Signals From the First Unidirectional Interconnects … Wherein the Control Die is Not Configured to Drive any Signal to Any of The First Unidirectional Interconnects*** **(Claims 20-23)**

The ’087 patent lacks sufficient written description support for the claim limitation “wherein the die interconnects further include first unidirectional interconnects … wherein the control die is configured to receive signals from the first unidirectional interconnects” in claims 20-23 for the same reasons as explained above.

7.1.1.2.11 ***Each of the Third Conduits Being a Unidirectional Conduit Configurable to Drive a Signal Received From a Corresponding Third Die Interconnect to the Interface and Not Configurable to Drive Any Signal to the Corresponding Third Die Interconnect*** **(Claims 24-28)**

The ’087 patent lacks sufficient written description support for the claim limitation “each of the third conduits being a unidirectional conduit configurable to drive a signal received from the a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect” in claims 24-28 for the same reasons as explained above.

7.1.1.2.12 ***Wherein the Control Die is Configured to, in Response to the First Set of C/A Signals, Receive First Signals Associated with the Memory Read Operation From a DRAM***

Die of the Stacked DRAM Dies via the First Unidirectional Interconnects **(Claims 1-8)**

The '087 patent lacks sufficient written description support for the claim limitation "wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects" in claims 1-8. Except for data signals, the specification does not describe any signals that flow from a DRAM die to the control die, especially any signals that are also "associated with" a memory read operation. The specification states that data signals may be bi-directional, but this does not provide written description support for the claimed signal because claims 1-8 also recite "data signals" (including "first data signals"), which are separate and distinct from the claimed "first signals." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010). None of the other signals described in the specifications (*e.g.*, command signals, address signals, chip select signals, voltage signals) satisfy the recited direction of flow.

7.1.1.2.13 ***Receiving from the First DRAM Die One or More Signals Associated with the First Set of C/A Signals via One or More of the First Unidirectional Interconnects*** **(Claims 9-12)**

The '087 patent lacks sufficient written description support for the claim limitation "receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects" in claims 9-12 for the same reasons as explained above.

7.1.1.2.14 ***The Control Die is Further Configurable to, in Response to the First Set of C/A Signals Being for a Memory Read Operation, Receive One or More First Signals Associated with the Memory Read Operation from One or More of the First Unidirectional Interconnects*** **(Claims 13-19)**

The '087 patent lacks sufficient written description support for the claim limitation "the control die is further configurable to, in response to the first set of C/A signals being for a memory

read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects" in claims 13-19 for the same reasons as explained above.

7.1.1.2.15 ***In Response to the First Set of C/A signals, … a First Subset of the Second Conduits is Configured to Receive First Signals Associated with the First Set of C/A Signals via a First Subset of the Second Die Interconnects and to Drive the First Signals to the Interface*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the first set of C/A signals, … a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface" in claims 24-28 for the same reasons as explained above.

7.1.1.2.16 ***In Response to the First Set of C/A Signals, … a First Subset of the Third Conduits is Configured to Receive One or More Second Signals Associated with the First Set of C/A Signals from a First Subset of the Third Die Interconnect and Drive the One or More Second Signals to the Interface*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the first set of C/A signals, … a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface" in claims 24-28 for the same reasons as explained above.

7.1.1.2.17 ***In Response to the Third Set of C/A Signals … a Second Subset of the Second Conduits is Configured to Receive Fifth Signals Associated with the Second Set of C/A Signals via a Second Subset of the Second Die Interconnects and to Drive the Fifth Signals to the Interface*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the third set of C/A signals … a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second

die interconnects and to drive the fifth signals to the interface" in claims 24-28 for the same reasons as explained above. Additionally, the specification does not describe any signal that is associated with a read command/address signal (*e.g.*, "third set of C/A signals") but is received in response to a write command/address signal (*e.g.*, "second set of C/A signals").

7.1.1.2.18 ***In Response to the Third Set of C/A Signals, … a Second Subset of the Third Conduits is Configured to Receive One or More Sixth Signals Associated with the Second Set of C/A Signals from a Second Subset of the Third Die Interconnect and Drive the One or More Sixth Signals to the Interface*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the third set of C/A signals, … a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface" in claims 24-28 for the same reasons as explained above. Additionally, the specification does not describe any signal that is associated with a read command/address signal (*e.g.*, "third set of C/A signals") but is received in response to a write command/address signal (*e.g.*, "second set of C/A signals").

7.1.1.2.19 ***In Response to the Second Set of C/A Signals, Drive Second Signals Associated with the Memory Write Operation to One or More DRAM Dies of the Stacked DRAM Dies via the Second Unidirectional Interconnects*** **(Claims 1-8)**

The '087 patent lacks sufficient written description support for the claim limitation "wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects" in claims 1-8. Except for data, address, and command signals (which also include chip select signals), the specification does not describe any signals that flow from the control die to the DRAM die and are "associated with" a memory write operation. The specification states that data signals may be bi-directional, but this does not provide written

description support for the claimed signal because claims 1-8 also recite "data signals" (including "first data signals"), which are separate and distinct from the claimed "first signals." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010). Similarly, the specification states that command and address signals may flow from the control die to the DRAM die, but this also does not provide written description support for the claimed signal because claims 1-8 also recite "C/A signals." *Id.*

7.1.1.2.20 ***Driving One or More Signals Associated with the Second set of C/A Signals to the First Plurality of DRAM Dies via One or More of the Second Unidirectional Interconnects*** **(Claims 9-12)**

The '087 patent lacks sufficient written description support for the claim limitation "driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects" in claims 9-12 for the same reasons as explained above.

7.1.1.2.21 ***The Control Die is Further Configurable to, … in Response to the Second Set of C/A Signals Being for a Memory Write Operation, Drive One or More Second Signals Associated with the Memory Write Operation to One or More of the Second Unidirectional Interconnects*** **(Claims 20-23)**

The '087 patent lacks sufficient written description support for the claim limitation "the control die is further configurable to, … in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects" in claims 13-19 for the same reasons as explained above.

7.1.1.2.22 ***Wherein, in Response to the Second Set of C/A Signals, the Control Die is Configured to Drive One or More Second Signals Associated with the Memory Write Operation to the One or More DRAM Dies via One or More of the Second Unidirectional Interconnects*** **(Claims 20-23)**

The '087 patent lacks sufficient written description support for the claim limitation "wherein, in response to the second set of C/A signals, the control die is configured to drive one

or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects" in claims 20-23 for the same reasons as explained above.

7.1.1.2.23 ***In Response to the Second Set of C/A signals, … the First Subset of the Second Conduits is Configured to Receive Third Signals Associated with the Second Set of C/A Signals from the Interface and to Drive the Third Signals to the First Subset of the Second Die Interconnects*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the second set of C/A signals, … the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects" in claims 24-28 for the same reasons as explained above.

7.1.1.2.24 ***In Response to the Second Set of C/A Signals, … a First Subset of the Fourth Conduits is Configured to Receive One or More Fourth Signals Associated with the Second Set of C/A Signals from the Interface and to Drive the One or More Fourth Signals to a First Subset of the Fourth Die Interconnect*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the second set of C/A signals, … a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect" in claims 24-28 for the same reasons as explained above.

7.1.1.2.25 ***In Response to the Fourth Set of C/A Signals, … the Second Subset of the Second Conduits is Configured to Receive Seventh Signals Associated with the Fourth Set of C/A Signals from the Interface and to Drive the Seventh Signals to the Second Subset of the Second Die Interconnects*** **(Claims 24-28)**

The '087 patent lacks sufficient written description support for the claim limitation "in response to the fourth set of C/A signals, … the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to

drive the seventh signals to the second subset of the second die interconnects" in claims 24-28 for the same reasons as explained above.

7.1.1.2.26 *In Response to the Fourth Set of C/A Signals, … a Second Subset of the Fourth Conduits is Configured to Receive One or More Eighth Signals Associated with the Second Set of C/A Signals from the Interface and to Drive the One or More Eight Signals to a Second Subset of the Fourth Die Interconnect* (claims 24-28)

The '087 patent lacks sufficient written description support for the claim limitation "in response to the fourth set of C/A signals, … a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect" in claims 24-28 for the same reasons as explained above. Additionally, the specification does not describe any signal that is associated with a write command/address signal (*e.g.*, "second set of C/A signals") but is received in response to a different write command/address signal (*e.g.*, "fourth set of C/A signals").

7.1.1.3. The '893 Provisional Application Also Fails to Disclose Additional Limitations

The '893 provisional application filed November 3, 2010 also fails to provide written description for everything discussed above, as well as additional limitations. The '893 Provisional's disclosure is much shorter than the '087 Patent's, and does not include the following disclosures that were added to the non-provisional application filed on November 3, 2011:

- Figures 1–5 of the '087 Patent
- Columns 1:5-3:41, 3:65-17:63, and 20:18-22:42 of the '087 patent
- Parts of columns 17:65–20:17 of the '087 Patent (with other parts of 17:65–20:17 being similar to [0004]–[0012] in the '893 Provisional)

Therefore, in addition to the lack of written description for everything discussed above, there is also no written description in the '893 Provisional for a "first" and "second" "plurality of DRAM dies" with "interconnects" in "electrical communication" with the "first" plurality but not the

"second" plurality, and vice versa, as required by claims 1[f]-1[i], 9[f][1]-9[i], 13[g]-13[k], 20[f][1]-20[f][2], 23[f][1]-23[f][2], and 25[a][1]-25[a][2] in the '087 Patent (and their dependents). Instead, the '893 Provisional just discloses a single group of "DRAM chips or dies" in each package, with no disclosure of subsets of dies—or electrical communication with only a subset of dies—in a given package.

7.1.2. Lack of Enablement Under 35 U.S.C. § 112, ¶ 1

The specification of the '087 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '087 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '087 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1: [6]

Term	Claim(s)
wherein the one or more C/A signals do not include any chip select signal … wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies	6, 20-23
[first/second/third/fourth] C/A signals include one or more signals selecting a DRAM die in the first/second subset of DRAM dies … wherein the one or more C/A signals do not include any chip select signals	24-28
The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies	2
The DRAM package of claim 9, wherein the stacked DRAM dies include at least 8 stacked DRAM dies	9
The DRAM package of claim 13, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies	14

[6] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Claim(s)
The DRAM package of claim 20, wherein the stacked DRAM dies include at least 8 stacked DRAM dies	21
The DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies	27

7.1.2.1. *Wherein the One or More C/A Signals do Not Include Any Chip Select Signal … Wherein the Control Die does Not Include Emulation Logic that Performs Emulation Causing Two or More DRAM Dies of the Stacked DRAM Dies to Emulate a Single DRAM Die Having a Larger Capacity than Each of the Two or More DRAM dies* **(Claims 6, 20-23)**

Claims 6 and 20-23 of the ’087 patent lack enablement because a person of ordinary skill would not be able to make or use the invention claimed in claim 6 or 20-23 of the ’087 patent without undue experimentation. Each of these claims recites and requires that “the one or more C/A signals do not include any chip select signal.” Because the DRAM package does not receive a chip select signal, it package would need to use the C/A signals to generate the signals that select the DRAM die(s) internally. Consequently, from the outside, the DRAM package would appear as a single DRAM whose capacity is larger than the capacity of each DRAM die within the package. This conflicts with the limitation that the claimed DRAM package “not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.” Because of this conflict, a person of ordinary skill in the art would not be able to make or used the claimed invention of claims 6 and 20-23 without undue experimentation.

7.1.2.2. *[First/Second/Third/Fourth] C/A Signals Include One or More Signals Selecting a DRAM Die in the First/Second Subset of DRAM Dies … Wherein the One or More C/A Signals do not Include Any Chip Select Signals* **(Claims 24-28)**

Claims 24-28 of the ’087 patent lack enablement because a person of ordinary skill would not be able to make or use the invention claimed in claim 24-28 of the ’087 patent without undue experimentation. Each of these claims also recites that these “C/A signals do not include any chip

select signals." This limitation conflicts with a different limitation that recites and requires that the "[first/second/third/fourth] C/A signals include one or more signals selecting a DRAM die in the first/second subset of DRAM dies." Because of this conflict, a person of ordinary skill in the art would not be able to make or used the claimed invention of claims 24-28 without undue experimentation.

7.1.2.3. *Wherein the [Plurality of] Stacked DRAM Dies Include at Least 8 Stacked DRAM Dies* (Claims 2, 9, 14, 21, 27)

Claims 2, 9, 14, 21, and 27 of the '087 patent lack enablement because a person of ordinary skill in the art would not be able to make or use the full scope of the claimed invention without undue experimentation. *Amgen Inc. v.* Sanofi, 143 S. Ct. 1243, 1254 (2023). These claims do not impose an upper limit on the number of DRAM dies that the claimed DRAM package may include. As a result, the DRAM package of claims 2, 9, 14, 21, and 27 may include more than 32, 64, 128, 256, 512, or 1024 DRAM dies. The technology to stack such a large number of—and potentially an infinite number of—DRAM dies in a single DRAM package was not available at the time of the '087 patent.

7.1.3. Invalidity Under 35 U.S.C. § 112, ¶ 2

"[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g. Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alternation omitted). "Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention," the claim is "invalid under § 112, paragraph 2." *Id*. at 1349. Several of the '087 Patent's Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth

in these claims are not what the patentee regarded as his invention. *Id*. These claims are invalid under the "applicant regards" prong of § 112 at least because they contain elements that differ from and/or conflict with the '087 Patent's written description of the invention, or because they omit elements that one of skill in the art would understand as part of the '087 Patent's invention based on the specification.

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '087 Patent's Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '087 Patent's Asserted Claims are indefinite in whole, in part, or in combination:[7]

Term	**Claim(s)**
wherein the one or more C/A signals do not include any chip select signal … wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies	6, 20-23
logic configur[ed/able] to ...	1-8, 17-18, 20-28
"the control die is configurable to drive the one or more second signals to the second DRAM die ene or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;"	13-19

[7] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Claim(s)
wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies	23
[first/second/third/fourth] C/A signals include one or more signals selecting a DRAM die in the first/second subset of DRAM dies … wherein the one or more C/A signals do not include any chip select signals	24-28
in response to the third set of C/A signals … a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface	24-28
in response to the third set of C/A signals, … a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface	24-28
in response to the fourth set of C/A signals, … a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect	24-28

7.1.3.1. *Wherein the One or More C/A Signals do Not Include Any Chip Select Signal … Wherein the Control Die Does Not Include Emulation Logic that Performs Emulation Causing Two or More DRAM Dies of the Stacked DRAM Dies to Emulate a Single DRAM Die Having a Larger Capacity than Each of the Two or More DRAM Dies* **(Claims 6, 20-23)**

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 6 and 20-23 of the ’087 patent with reasonable certainty because these limitations recite two conflicting requirements as discussed above.

7.1.3.2. *[First/Second/Third/Fourth] C/A Signals Include One or More Signals Selecting a DRAM Die in the First/Second Subset of DRAM Dies … Wherein the One or More C/A Signals do Not Include Any Chip Select Signals* (Claims 24-28)

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 24-28 of the '087 patent with reasonable certainty because these limitations recite two conflicting requirements as discussed above.

7.1.3.3. *The Control Die is Configurable to Drive the One or More Second Signals to the Second DRAM Die Ene or More DRAM Dies of the Plurality of Stacked DRAM Dies-via the One or More of the Second Unidirectional Interconnects and is Not Configurable to Receive Any Signal from Any of the Plurality of Stacked DRAM Dies via Any of the Second Unidirectional Interconnects* (Claims 13-19)

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 13-19 of the '087 patent with reasonable certainty because this limitation contains an apparent typographical error, "ene or more DRAM dies of the plurality of stacked DRAM dies," which renders the term meaningless unless corrected.

7.1.3.4. *In Response to the Third Set of C/A Signals … a Second Subset of the Second Conduits is Configured to Receive Fifth Signals Associated with the Second Set of C/A Signals via a Second Subset of the Second Die Interconnects and to Drive the Fifth Signals to the Interface* (Claims 24-28)

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 24-28 of the '087 patent with reasonable certainty because this limitation also recites conflicting requirements—one requirement that the "fifth signals" be received in response to a read command ("third set of C/A signals") and another requirement that the signals be associated with a write command ("second set of C/A signals").

7.1.3.5. *In Response to the Third Set of C/A Signals, … a Second Subset of the Third Conduits is Configured to Receive One or More Sixth Signals Associated with the Second Set of C/A Signals from a Second Subset of the Third Die Interconnect and Drive the One or More Sixth Signals to the Interface* (Claims 24-28)

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 24-28 of the '087 patent with reasonable certainty because this limitation also recites

conflicting requirements—one requirement that the "sixth signals" be received in response to a read command ("third set of C/A signals") and another requirement that the signals be associated with a write command ("second set of C/A signals").

7.1.3.6. ***In Response to the Fourth Set of C/A Signals, … a Second Subset of the Fourth Conduits is Configured to Receive One or More Eighth Signals Associated with the Second Set of C/A Signals from the Interface and to Drive the One or More Eight Signals to a Second Subset of the Fourth Die Interconnect*** **(Claims 24-28)**

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claims 24-28 of the '087 patent with reasonable certainty because this limitation recites and requires that the "eighth signals" be received in response to a later write command ("fourth set of C/A signals") but the "eighth signals" are associated with a different, earlier write command ("second set of C/A signals").

7.1.3.7. ***Wherein the Power Supply Interconnects Include a First Supply Voltage Interconnect and a Second Supply Voltage Interconnect, Wherein the First Supply Voltage Interconnect is Configured to Conduct a Supply Voltage Received at a Power Supply Terminal to Each of the First Plurality of DRAM Dies and Not to Any of the Second Plurality of DRAM Dies, and Wherein the Second Supply Voltage Interconnect is Configured to Conduct the Supply Voltage Received at the Power Supply Terminal to Each of the Second Plurality of DRAM Dies and Not to Any of the First Plurality of DRAM Dies*** **(Claim 23)**

A person of ordinary skill in the art would not be able to ascertain the scope and meaning of claim 23 of the '087 patent with reasonable certainty because this term lacks antecedent basis.

7.2. '731 Patent

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '731 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; and indefiniteness under 35 U.S.C. § 112, second paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-

infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported constructions of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendant's Invalidity Contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '731 Patent's Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which it is presently aware.

7.2.1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '731 Patent does not provide sufficient written description to establish that the named inventors were in possession of the alleged inventions recited in the Asserted Claims at the time the '731 Patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus.

The specification of the '731 Patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements in the Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '731 Patent fails to sufficiently describe or enable them as required by 35 U.S.C. 112, ¶ 1:[8]

[8] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Relevant Claim(s)	Term
1[d]	"at least one circuit coupled between the at least one connector and the plurality of memory devices, the at least one circuit comprising a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices"
1[e][1]	"each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections"
1[e][2]	"each correction circuit of the set of correction circuits including at least one programmable impedance matching circuit"
1[f][2]	"the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals."
2	"at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit has dynamically programmable impedances whose values may differ depending on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals"
3	"at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit comprises at least one network of programmable resistors that is dynamically controllable"
4	"each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises one or more self-adjusting damper circuits"
5	"each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises first one or more dynamically programmable repeater/amplifier elements"

Relevant Claim(s)	Term
6	"each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further includes a delay circuit that is configured to generate delayed versions of the signals transmitted between the respective port connection of the first set of port connections and the corresponding port connection in the second set of port connections"
7	"the number of port connections in the first set of port connections corresponds to a bit width of the memory bus"
8	"at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of one of the plurality of memory devices"
9	"at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of multiple memory devices of the plurality of memory devices"
10	"the control circuitry is configured to activate signal paths in the each circuit of the at least one circuit in response to the address and control signals"
11	"the control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals"
12	"each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements"
13	"each circuit in the at least one circuit has a data width of 4, 8 or 16 bits"
14	"at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices"
15	"at least one circuit is configured to improve timing of signals transmitted between the at least one connector and the plurality of memory devices"
16	"at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices"

Relevant Claim(s)	Term
17	"at least one circuit includes signal paths, wherein the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals"
18	"at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections that is not in an active signal path"

As discussed in more detail below, the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, since the Plaintiff's Infringement Contentions allege that the claimed "at least one circuit further comprising a set of correction circuits" of claim 1 is realized in the memory devices themselves, and not in a discrete package separate and apart from the memory devices as disclosed in the '731 Patent specification. As discussed in detail below, the '731 Patent specification lacks any disclosure regarding implementation of "at least one circuit further comprising a set of correction circuits" within the memory device itself, *i.e.*, the integrated circuit package.

7.2.1.1. Claim Limitation 1[d]

As one example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, for the "at least one circuit coupled between the at least one connector and the plurality of memory devices" limitation of claim 1 (limitation 1[d]), in view of Plaintiff's application of this limitation to the Accused Products, the '731 Patent specification has no written description that supports the inclusion of a circuit with a first port and a second port within the memory device itself. The '731 Patent specification consistently depicts this specific circuit with the first and second ports as an element separate and apart from the memory devices.

See, e.g., ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Furthermore, the ’731 Patent specification fails to show or describe any circuitry in the memory devices and only discusses general memory design. *See, e.g.*, ’731 Patent at 6:57–7:9. For example, the ’731 Patent specification states that, in certain embodiments, “the circuit 112 may be disposed on a memory board that is populated with sets of memory devices 203, 204.” *See, e.g.*, ’731 Patent at 13:39-41; *see also id*. at 9:30-41 (“Various alternative configurations for the physical organization of the circuit 112 are possible, however. In certain other embodiments, the circuit 112 comprises multiple, physically separate components. For example, in one embodiment, the circuit 112 comprises one physically separate component per memory device 111 (e.g., integrate circuit packages mounted on the memory module 100). In another embodiment, the circuit 112 comprises one physically separate component per memory rank. In some embodiments, the circuit 112 comprises one physically separate component corresponding to multiple memory devices 111.”); *id*. at 14:65-15:7 (“In an example configuration, the plurality of subsystems 310 include a plurality of memory devices 311 (e.g., DRAM devices) mounted on a memory module and the first set of interfaces 330 comprise interfaces between the circuit 112 and the plurality of memory devices 311. For example, each of the first set of ports 122 may correspond to a memory signal (e.g., a data, address, and/or control signal) and each of the first set of interfaces 330 is operatively coupled to a corresponding memory signal port of a corresponding memory device 311.”).

None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. All memory devices are depicted as simple boxes, and there is no information or suggestion in the ’731 Patent specification that such a circuit would be included

within the memory device. Such a suggestion would be contrary to the prosecution history of the '731 Patent, which includes at least one prior art reference that depicts a memory system with memory devices that include the port circuit as this limitation is applied by Netlist. *See, e.g.*, WO 2006/055497 (included in IDS submitted by Netlist on January 16, 2015 in the parent application of the '731 Patent).

7.2.1.2. Claim Limitation 1[e][1]

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, for the "each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted" limitation of claim 1 (limitation 1[e][1]), in view of Plaintiff's application of this limitation to the Accused Products, the '731 Patent specification lacks any written description that supports the inclusion of a circuit with correction circuit configured to make corrections between first and second sets of port connections within the memory device itself. Furthermore, the '731 Patent specification fails to show or describe any circuitry in the memory devices and only discusses general memory design. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitation 1[d] *supra*.

Instead, the '731 Patent specification discloses that the correction circuits are part of the "the circuit 112, which the '731 Patent specification consistently states is not part of, nor integrated into, the memory devices. *See, e.g.*, '731 Patent at 5:22-46; 9:10-13; 12:65-13:4; 13:48-63; 14:20-54; 15:55-64; Figs. 4, 8, 9. In addition, the '731 Patent specification does not disclose using a crossbar arrangement (switching sub-circuit 140) as shown in Figure 9 inside a memory device. *See, e.g., id*. at 14:48-51.

As noted in the previous limitation, the ’731 Patent specification is devoid of any discussion or suggestion that a correction circuit is implemented within the memory devices themselves. As noted elsewhere in this Invalidity Contentions (*see, e.g.*, Section 5.2), signal correction circuits internal to memory devices were notoriously well-known prior to the effective filing date of the ’731 Patent. *See, e.g.*, TN-47-05, Power Solutions for DDR2 Notebook PCs (2004); U.S. Patent No. 7,196,966. Also, as noted above, the prosecution history of the ’731 Patent identifies WO 2006/055497 as prior art (IDS submitted by Netlist on January 16, 2015 in the parent application of the ’731 Patent), and the WO ’497 publication discloses memory devices with correction circuits on the memory device itself. Netlist certainly had the opportunity to include such memory devices with integrated first and second port circuitry that included correction circuits, but appears to have purposefully excluded such memory devices from the ’731 Patent specification.

7.2.1.3. Claim Limitation 1[e][2]

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, for the “each correction circuit of the set of correction circuits including at least one programmable impedance matching circuit” limitation of claim 1 (limitation 1[e][2]), in view of Plaintiff’s application of this limitation to the Accused Products, the ’731 Patent specification has no written description that supports the inclusion of a circuit with correction circuit configured to make impedance matching corrections between first and second sets of port connections within the memory device itself. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d] and 1[e][1] *supra*.

In addition, the ’731 Patent specification does not disclose an impedance matching element that would perform impedance matching in a manner recognized by one of ordinary skill in the art. For example, the ’731 Patent specification identifies Figure 5 as depicting an impedance matching element 152, which is an adjustable resistor. At best, the ’731 Patent specification discloses a resistive matching element, and not an impedance matching element that matches the resistive and reactive components of the conductive pathway connected to the “circuit 112.”

7.2.1.4. Claim Limitation 1[f][2]

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, for the “the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit” limitation of claim 1 (limitation 1[f][2]), in view of Plaintiff’s application of this limitation to the Accused Products, the ’731 Patent specification has no written description that discloses control circuitry integrated into the memory devices themselves that dynamically controls an impedance matching circuit in response to address and control signals. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], and 1[e][2] *supra*.

In addition, the ’731 Patent specification does not disclose how the purported impedance matching circuit would operate within a memory device on internal signal paths, since the memory device does not have the type of “transmission lines” that would typically be found on a memory module. Impedance matching implies resistive and reactive components, and the reactive components are not discussed anywhere in the ’731 Patent specification.

In addition, the ’731 Patent specification does not disclose that the memory devices themselves have multiple ranks within the respective devices. As noted above, the ’731 Patent specification discloses this limitation, and the ’731 Patent specification is devoid of any description regarding the internal circuit structure of the memory devices that would demonstrate how the device is internally decimated into ranks.

Finally, the claim limitation requires that the “control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit....” The ’731 Patent specification does not disclose how the selection of a rank from multiple ranks dynamically controls the purported impedance matching circuit 160 with its programmable resistor 162. The ’731 Patent specification only states is “[t]he resistance of the programmable resistor 162 may be controllable by a control signal 164.” *See* ’731 Patent at 10:50–52. There is no further description of how the control signal 162 is generated, or how the control signal is related to the transmission lines in the system. *See, e.g.*, *id*. at 19:66–11:6.

7.2.1.5. Claim 2

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit has dynamically programmable impedances whose values may differ depending on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals” language of claim 2. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses control circuitry integrated into the memory devices themselves that controls an impedance matching circuit and dynamically programs different

impedance values in response to address and control signals. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

In addition, the claim requires that the “at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit has dynamically programmable impedances whose values may differ depending on which of the multiple ranks is selected . . . .” The ’731 Patent specification does not disclose how the selection of a rank from multiple ranks dynamically controls the purported impedance matching circuit 160 with its programmable resistor 162. The ’731 Patent specification only states is “[t]he resistance of the programmable resistor 162 may be controllable by a control signal 164.” *See* ’731 Patent at 10:50–52. There is no further description of how the control signal 164 is generated or managed, or how the control signal 164 is related to the transmission lines in the system. *See, e.g.*, *id*. at 19:66–11:6.

7.2.1.6. Claim 3

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit comprises at least one network of programmable resistors that is dynamically controllable” language of claim 3. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses control circuitry integrated into the memory devices themselves that controls an

impedance matching circuit in the correction circuit and dynamically programs different impedance values, wherein the impedance matching circuit uses resistor networks. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

In addition, the claim requires that the "at least one network of programmable resistors that is dynamically controllable . . . ." The '731 Patent specification does not disclose how the purported impedance matching circuit 160 with its programmable resistor 162 is dynamically controllable, much less how a network of resistors is dynamically controllable and the parameters related to such control. The '731 Patent specification only states is "[t]he resistance of the programmable resistor 162 may be controllable by a control signal 164." *See* '731 Patent at 10:50–52. There is no further description of how the control signal 164 is generated or managed, or how the control signal 164 is related to the transmission lines in the system. *See, e.g.*, *id*. at 19:66–11:6.

7.2.1.7. Claim 4

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises one or more self-adjusting damper circuits" language of claim 4. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses correction circuitry integrated into the memory devices themselves that comprises at least one-self adjusting damper circuit. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3,

elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

Figure 6 of the '731 Patent depicts what is purported to be a damper circuit, but the '731 Patent specification lacks any detail about the structure of the purported damper circuit that would be useful to one of ordinary skill in the art. For example, Figure 6 shown a "first sub-circuit 184 adapted to generate a first signal 187 responsive to at least a portion of the noise component." *See, e.g.*, '731 Patent at 11:51–53, Fig. 6. The '731 Patent specification further discloses that "the first sub-circuit 184 may generate the first signal 187 in response to the portion of the noise component not reduced by the coarse correction element 152 . . . ." *Id*. at 11:53–55. There is no disclosure in the '731 Patent specification on the constitution of the "first sub-circuit 184," how it generates the "first signal 187 in response to the portion of the noise component," or the type of information included in the "first signal 187," *e.g*., phase information, voltage levels, etc. Furthermore, Figure 6 shows a "second sub-circuit 188" that is "adapted to generate a second signal 190 corresponding to a delayed version of at least a portion of the input signal." *See, e.g.*, *id.* at 11:57–59, Fig. 6. There is no disclosure in the '731 Patent specification on the constitution of the "second sub-circuit 188," how it generates the "second signal 190," or the type of information included in the "second signal 190," *e.g*., phase information, voltage levels, etc. In addition, the '731 Patent specification characterizes the "first subcircuit 184" as comprising "one or more current sources 185, 186" that can be controlled current sources, *e.g.*, a voltage-controlled current source. *See id*. at 12:1–5. The '731 Patent specification refers to U.S. Provisional Application No. 61/044,825 and U.S. Patent Application No. 12/422,912, but there is no language in the '731 Patent specification showing how the provisional application relates to the claimed damper circuit, and the utility patent application

is unpublished. Finally, the ’731 Patent specification states that the “self-adjusting damper circuit 170” includes an unseen enable control input to enable the damper circuit, (*see id*. at 12:8–11) but the ’731 Patent specification lacks any further disclosure of the “enable control input” with respect to its generation, and how it controls the damper circuit. The provisional application was similarly unavailing.

7.2.1.8. Claim 5

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises first one or more dynamically programmable repeater/amplifier elements” language of claim 5. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses correction circuitry integrated into the memory devices themselves that comprises at least dynamically programmable repeater/amplifier device. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff alleges that this claimed element does more than simply turning on/off, the ’731 Patent specification does not disclose how the disclosed repeater/amplifier element 158 is dynamically programmed. For control purposes, the ’731 Patent specification states the “repeater/amplifier element 158 includes an output enable control input 159 for controlling the bi-directional signal path.” *See* ’731 Patent at 12:37–39. There is no further description of how the output enable control input 159 is generated, what circuitry manages the output enable control

input 159, or even how the or how the repeater/amplifier element 158 is "dynamically" programmed.

The '731 Patent specification does not disclose a DFE filter, which is a specialized digital filter for signal equalization. The only filters disclosed are low pass, high pass, band pass, and notch filters. *See, e.g.*, '731 Patent at 12:18–28. For those filter types, however, the '731 Patent specification does not provide any information regarding the constitution of those filters.

Plaintiff alleges that the Decision Feedback Equalizer (DFE) filter in the Accused Products meets this limitation. To the extent that Plaintiff alleges that the '731 Patent specification is inclusive of DFE filters, the '731 Patent specification fails to enable key aspects of a DFE filter implementation, as the specification lacks any information about the number of taps, tap weights, and delay times between the taps. All this information is required for a DFE filter design.

7.2.1.9. Claim 6

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further includes a delay circuit that is configured to generate delayed versions of the signals transmitted between the respective port connection of the first set of port connections and the corresponding port connection in the second set of port connections" language of claim 6. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is configured with a delay circuit that to generate delayed versions of the signals transmitted between the respective port connections. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See,*

e.g., ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

In addition, the claim recites “the at least one circuit further includes a delay circuit that is configured to generate delayed versions of the signals transmitted” and Plaintiff alleges that the Decision Feedback Equalizer (DFE) filter in the Accused Products meets this limitation. The ’731 Patent specification only discloses low pass, high pass, band pass, and notch filters (*see, e.g.*, ’731 Patent at 12:18–28) while failing to provide any information regarding the constitution of those specific filters. To the extent that Plaintiff alleges that the ’731 Patent specification is inclusive of DFE filters (which is a specialized digital filter), the ’731 Patent specification fails to enable key aspects of a DFE filter implementation, as the specification lacks any information about the number of taps, tap weights, and delay times between the taps. To the extent that Plaintiff alleges that any other filter type is present in the Accused Products, there is no enabling disclosure in the ’731 Patent specification.

7.2.1.10. Claim 7

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “number of port connections in the first set of port connections corresponds to a bit width of the memory bus” language of claim 7. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses “at least one circuit” with “a set of correction circuits” integrated into the memory devices themselves that has a number of port connections in the first set of port connections corresponding to bit width of the memory bus. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See,*

e.g., ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices of the Accused Products include “at least one circuit” with “a set of correction circuits” wherein the number of port connections in the first set of port connections corresponds to a bit width of the memory bus, the ’731 Patent specification does not enable this claim. As discussed *supra*, the ’731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.11. Claim 8

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of one of the plurality of memory devices” language of claim 8. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) that comprises multiple integrated circuits integrated into the memory devices themselves. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves of the Accused Products include an “at least one circuit [that] comprises multiple physically separate integrated

circuit packages each having a data width corresponding to a data width of one of the plurality of memory devices," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.12. Claim 9

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of multiple memory devices of the plurality of memory devices" language of claim 9. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) that comprises multiple integrated circuits integrated into the memory devices themselves. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices of the Accused Products include at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of multiple memory devices of the plurality of memory devices, the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit. As discussed *supra*, the '731 Patent

specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.13. Claim 10

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “control circuitry is configured to activate signal paths in the each circuit of the at least one circuit in response to the address and control signals” language of claim 10. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is activated by a control circuit in response to address and control signals. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves of the Accused Products include “control circuitry [that] is configured to activate signal paths in the each circuit of the at least one circuit in response to the address and control signals,” the ’731 Patent specification does not enable this claim. As discussed *supra*, the ’731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.14. Claim 11

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in

its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals” language of claim 11. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is activated by a control circuit in response to address and control signals. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves of the Accused Products include control circuitry configured to receive the address and control signals from the system memory controller, and “wherein the control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals,” the ’731 Patent specification does not enable this claim. As discussed *supra*, the ’731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.15. Claim 12

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements” language of claim 12. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that

discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that has the claimed bit width. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves of the Accused Products include correction circuits, “wherein the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements, and wherein the control circuitry is configured to activate the one or more circuit elements in response to the address and control signals,” the ’731 Patent specification does not enable this claim. As discussed *supra*, the ’731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.16. Claim 13

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “each circuit in the at least one circuit has a data width of 4, 8 or 16 bits” language of claim 13. In view of Plaintiff’s application of this claim to the Accused Products, the ’731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that has the claimed bit width. None of the memory devices depicted in the ’731 Patent specification shows any circuitry at all. *See, e.g.*, ’731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310,

311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices of the Accused Products include correction circuits, "wherein each circuit in the at least one circuit has a data width of 4, 8 or 16 bits," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.17. Claim 14

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices" language of claim 14. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is configured to improve signal integrity. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves in the Accused Products include correction circuits, "wherein the at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices," the '731 Patent specification does not enable this claim. As discussed *supra*,

the ’731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

With respect to “signal integrity,” the ’731 Patent specification states “[t]he circuits 112 may be configured so as to improve the interconnection (e.g., timing, power consumption, and/or signal integrity) between each of the plurality of circuits 112 and a plurality of corresponding memory devices 111 of memory module 100. For example, the data width of each of the plurality of circuits 112 may be selected to optimize the interconnection (e.g., timing, power consumption, and/or signal integrity)” without any further explanation. *See, e.g.*, ’731 Patent at 7:57–63; *see also id*. at 8:14–19.

The claim recites “configured to improve signal integrity in signals transmitted” and Plaintiff alleges that the Decision Feedback Equalizer (DFE) filter in the Accused Products meets this limitation. The ’731 Patent specification only discloses low pass, high pass, band pass, and notch filters (*see, e.g.*, ’731 Patent at 12:18–28) while failing to provide any information regarding the constitution of those specific filters. To the extent that Plaintiff alleges that the ’731 Patent specification is inclusive of DFE filters (which is a specialized digital filter), the ’731 Patent specification fails to enable key aspects of a DFE filter implementation, as the specification lacks any information about the number of taps, tap weights, and delay times between the taps. To the extent that Plaintiff alleges that any other filter type is present in the Accused Products, there is no enabling disclosure in the ’731 Patent specification.

7.2.1.18. Claim 15

As another example of how the ’731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the ’731 Patent specification lacks any disclosure for the “at least one circuit is configured to improve timing of signals transmitted between the at least one

connector and the plurality of memory devices" language of claim 15. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is configured to improve the timing of signals. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices themselves in the Accused Products include correction circuits, wherein "the at least one circuit is configured to improve timing of signals transmitted between the at least one connector and the plurality of memory devices," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

With respect to "timing," the '731 Patent specification states "[t]he circuits 112 may be configured so as to improve the interconnection (e.g., timing, power consumption, and/or signal integrity) between each of the plurality of circuits 112 and a plurality of corresponding memory devices 111 of memory module 100. For example, the data width of each of the plurality of circuits 112 may be selected to optimize the interconnection (e.g., timing, power consumption, and/or signal integrity)" without any further explanation. *See, e.g.*, '731 Patent at 7:57–63; *see also id*. at 8:14–19. The '731 Patent does not disclose any circuitry that improves timing, and there is no disclosure that places any circuitry for improving "timing of signals generated" in the memory devices.

The claim recites that the circuit is "configured to improve timing of signals transmitted" and Plaintiff alleges that the Decision Feedback Equalizer (DFE) filter in the Accused Products meets this limitation. The '731 Patent specification only discloses low pass, high pass, band pass, and notch filters (*see, e.g.*, '731 Patent at 12:18–28) while failing to provide any information regarding the constitution of those specific filters. To the extent that Plaintiff alleges that the '731 Patent specification is inclusive of DFE filters (which is a specialized digital filter), the '731 Patent specification fails to enable key aspects of a DFE filter implementation, as the specification lacks any information about the number of taps, tap weights, and delay times between the taps. To the extent that Plaintiff alleges that any other filter type is present in the Accused Products, there is no enabling disclosure in the '731 Patent specification.

7.2.1.19. Claim 16

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices" language of claim 16. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves that is configured to improve the power consumption of transmitted signals. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices in the Accused Products include correction circuits, wherein "the at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

Plaintiff argues that this claim is met by the DDR5 requirement of an operating voltage of 1.1V. However, that operating voltage is a requirement of the standard. The '731 Patent specification does not show how to reduce power consumption within the memory devices themselves or is any actual gate level circuitry disclosed within the specification that would enable a person of ordinary skill in the art to reduce power consumption in a memory device.

7.2.1.20. Claim 17

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "at least one circuit includes signal paths, wherein the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals" language of claim 17. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices themselves with signal paths activated by a control circuit in response to address and control signals. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices in the Accused Products include correction circuits, wherein the at least one circuit includes signal paths, wherein "the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

7.2.1.21. Claim 18

As another example of how the '731 Patent specification fails to enable, or show that the inventors had possession of, the full scope of the claimed subject matter as asserted by Plaintiff in its Infringement Contentions, the '731 Patent specification lacks any disclosure for the "at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections that is not in an active signal path" language of claim 18. In view of Plaintiff's application of this claim to the Accused Products, the '731 Patent specification has no written description that discloses a circuit (including a correction circuit with impedance matching) integrated into the memory devices that has first and second port connections, with a "known static value" being provided to an unselected signal path. None of the memory devices depicted in the '731 Patent specification shows any circuitry at all. *See, e.g.*, '731 Patent at 6:57–7:9; Fig. 3, elements 110, 111; Fig. 8, elements 203, 204; Fig. 9, elements 310, 311, 320, 321. Defendants incorporate by reference in its entirety the analysis for claim limitations 1[d], 1[e][1], 1[e][2], and 1[f][2] *supra*.

To the extent that Plaintiff argues that the memory devices in the Accused Products include correction circuits, wherein "the at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections that is not in an active signal path," the '731 Patent specification does not enable this claim. As discussed *supra*, the '731 Patent

specification does not disclose or depict any memory device with internal circuitry that is inclusive of an impedance-based correction circuit.

The claim requires that the "[t]he at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections . . . ." The '731 Patent specification does not disclose how the selection of a rank from multiple ranks dynamically controls the purported impedance matching circuit 160 with its programmable resistor 162. The '731 Patent specification only states is "[t]he resistance of the programmable resistor 162 may be controllable by a control signal 164." *See* '731 Patent at 10:50–52. There is no further description of how the control signal 164 is generated, how the control signal 164 is managed, or how the control signal 164 is related to the transmission lines in the system. *See, e.g.*, *id*. at 19:66–11:6.

7.2.2. Invalidity Under 35 U.S.C. § 112, ¶ 2

"[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g. Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alternation omitted). "Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention," the claim is "invalid under § 112, paragraph 2." *Id*. at 1349. Several of the '731 Patent's Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id*. These claims are invalid under the "applicant regards" prong of § 112 at least because they contain elements that differ from and/or conflict with the '731 Patent's written description of the invention, or because they omit elements that one of skill in the art would understand as part of the '731 Patent's invention based on the specification: claims 1–18.

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '731 Patent's Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '731 Patent's Asserted Claims are indefinite in whole, in part, or in combination:[9]

Relevant Claim(s)	Term
1[e][1]	"each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections"
14	"at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices"
15	"at least one circuit is configured to improve timing of signals transmitted between the at least one connector and the plurality of memory devices"
16	"at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices"

7.2.2.1. Claim 1[e][1]

As just one example of how the claims fail to inform those skilled in the art about the scope of the invention, the '731 Patent specification and prosecution history disclose generalities for

[9] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

signal correction ("For example, the data width of each of the plurality of circuits 112 may be selected to optimize the interconnection (e.g., timing, power consumption, and/or signal integrity)."). The claim requires that "each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted…" But fails to delineate any indication of what level of correction to the transmitted signals is necessary to meet the claim.

7.2.2.2. Claim 14

As another example of how the claims fail to inform those skilled in the art about the scope of the invention, claim 14 recites that the circuit is "configured to improve signal integrity in signals transmitted." The '731 Patent specification and prosecution history fail to disclose, however, exactly how any improvement in "signal integrity" is determined. The '731 Patent specification is silent with respect to possible "signal integrity" improvements, such as signal eye, bit rate, noise, or VSWR. A POSA has no way to determine whether an improvement in "signal integrity" has been achieved.

7.2.2.3. Claim 15

As another example of how the claims fail to inform those skilled in the art about the scope of the invention, claim 15 recites that the circuit is "configured to improve timing of signals transmitted." The '731 Patent specification and prosecution history fail to disclose, however, exactly how any improvement in "timing" is determined or the where in the circuit are the timing improvements located. The '731 Patent specification is silent with respect to possible "timing" improvements – is a 0.01% increase in signal processing speed an improvement, or does the improvement need to be greater (e.g., 10% speed increase)? A POSA has no way to determine whether an improvement in "timing" has been achieved.

7.2.2.4. Claim 16

As another example of how the claims fail to inform those skilled in the art about the scope of the invention, claim 16 recites that the circuit is "configured to improve power consumption by signals transmitted" The '731 Patent specification and prosecution history fail to disclose, however, exactly how any improvement in "power consumption" is determined or the where in the circuit are the power consumption improvements located. The '731 Patent specification is silent with respect to possible "power consumption" improvements – is a 1% decrease in power consumption an improvement, or does the improvement need to be greater (e.g., 10% reduction)? A POSA has no way to determine whether an improvement in "power consumption" has been achieved.

8. P.R. 3-4 Document Production

In connection with these Invalidity Contentions, and pursuant to P.R. 3-4(a), Defendants are producing technical documentation relevant to the operation of the accused functionalities of the accused products identified by Plaintiff in its P.R. 3-1(c) charts. Some technical documentation is subject to export control restrictions imposed by the Republic of Korea's Ministry of Trade, Industry and Energy ("MOTIE"). Defendants have applied to MOTIE for export approval of such documentation, but MOTIE has not yet provided approval. Defendants' production does not include documentation subject to MOTIE restrictions. As set forth in Defendants' pending motion to amend in part the docket control order (Dkt. 76), Defendants have requested that the deadline to complete Defendants' P.R. 3-4(a) production be extended to 10 days after the date that MOTIE provides approval.

Pursuant to P.R. 3-4(b), Defendants also produce a copy of each item of prior art identified herein that does not appear in the file history of the '087 or '731 patent. These prior art references are discussed in the invalidity claim charts in Appendices A and B. Defendants will also make

available for inspection any prior art products upon request to the extent Defendants have them in its possession, custody, or control. References that were cited during prosecution of the Asserted Patents may not be contained in Defendants' production as they are not required to be under the local patent rules. Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art products is ongoing. Accordingly, Defendants reserve the right to supplement its production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

Defendants hereby incorporate by reference in their entirety the P.R. 3-3 Invalidity Contentions served contemporaneously on this date by Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC in *Netlist, Inc. v. Micron Technology Inc. et al*., C.A. No. 2:25-cv-00558-JRG (E.D. Tex.), including all appendices, exhibits, claim charts, patents, publications, products, prior art, and other documents produced alongside and/or cited therein.

Defendants reserve its right to supplement its P.R. 3-4 document production pursuant to the Patent Local Rules and the orders of the Court.

* * *

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Respectfully submitted,

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1[a] A dynamic random access memory (DRAM) package, comprising:

1[b][1] stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies,

1[b][2] each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

1[c][1] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,

1[c][2] wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

1[d][1] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,

1[d][2] the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals,

1[d][3] each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

1[e][1] a control die coupled between the terminals and the stacked DRAM dies,

1[e][2] the control die including conduits, the conduits including C/A conduits and data conduits,

1[e][3] the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects,

1[e][4] the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

1[f] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not

in electrical communication with any C/A port on any of the second plurality of DRAM dies;

1[g] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

1[h][1] wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies,

1[h][2] each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies,

1[h][3] wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

1[i] wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

1[j] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

1[k][1] wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals,

1[k][2] wherein the one or more C/A signals do not include any chip select signal;

1[l] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

1[m] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

1[n] wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

1[o] wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

1[p][1] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and

1[p][2] in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

2. The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

3. The DRAM package of claim 2, wherein the stacked DRAM dies include 16 stacked DRAM dies.

4[a] The DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and

4[b] the second driver size is different from the first driver size.

5. The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.

6[a] The DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and

6[b] the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;

6[c] wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

7. The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.

8. The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.

9[a] A method, comprising:

9[b][1] at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports,

9[b][2] the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals,

9[b][3] the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies,

9[b][4] the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects including first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects,

9[c] receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;

9[d][1] in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and

9[d][2] receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;

9[e][1] in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving

second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and

9[e][2] driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;

9[f][1] wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies,

9[f][2] each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies,

9[f][3] wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

9[g] wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

9[h] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

9[i] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

9[j][1] wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and

9[j][2] the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies;

9[k] wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and

9[l] wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.

10. The method of claim 9, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

11. The method of claim 9, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.

12[a] The method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:

12[b] enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;

12[c] enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and

12[d] maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;

12[e] wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.

13[a] A dynamic random access memory (DRAM) package, comprising:

13[b] a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;

13[c] an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals;

13[d] die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and

13[e] a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;

13[f] wherein: the die interconnects include a first set of C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;

13[g] each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;

13[h][1] each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies,

13[h][2] each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;

13[i] the control die is configurable to drive a first set of C/A signals received by the DRAM package via the interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects;

13[j] a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the second subset of the plurality of stacked DRAM dies;

13[k] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;

13[l] the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;

13[m] the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data interconnects and the interface;

13[n] the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;

13[o] the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;

13[p] the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;

13[q] the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;

13[r] the control die is configurable to drive the one or more second signals to the second DRAM die ene or more DRAM dies of the plurality of stacked DRAM dies-via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of the second unidirectional interconnects;

13[s] each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;

13[t] a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and

13[u] each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.

14. The DRAM package of claim 13, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.

15. The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.

16. The DRAM package of claim 13, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.

17[a][1] The DRAM package of claim 13, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects,

17[a][2] wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

17[b] the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;

17[c] the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;

17[d] each of the first data conduits are placed in a non-driving state after driving the first data signals;

17[e] each of the second data conduits are placed in a non-driving state after driving the second data signals; and

17[f] data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.

18[a][1] The DRAM package of claim 13, wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits,

18[a][2] wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.

19. The DRAM package of claim 13, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the second data interconnects in parallel.

20[a] A dynamic random access memory (DRAM) package, comprising:

20[b] stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

20[c][1] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals,

20[c][2] wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

20[d][1] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,

20[d][2] the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,

20[d][3] wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

20[e][1] a control die coupled between the terminals and the stacked DRAM dies,

20[e][2] the control die including conduits coupled to respective ones of the die interconnects;

20[f][1] wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,

20[f][2] the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

20[g] wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

20[h][1] wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,

20[h][2] wherein the one or more C/A signals do not include any chip select signal;

20[i] wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

20[j] wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;

20[k] wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and

20[l][1] wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and

20[l][2] wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;

20[m] wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

21. The DRAM package of claim 20, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

22[a] The DRAM package of claim 20, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first n-bit-wide data; and

22[b] the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second n-bit-wide data.

23[a] A dynamic random access memory (DRAM) package, comprising:

23[b] stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

23[c][1] terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,

23[c][2] wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;

23[d][1] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,

23[d][2] the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,

23[d][3] wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and

23[e][1] a control die coupled between the terminals and the stacked DRAM dies,

23[e][2] the control die including conduits coupled to respective ones of the die interconnects;

23[f][1] wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,

23[f][2] the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;

23[g] wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;

23[h][1] wherein the control die further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,

23[h][2] wherein the one or more C/A signals do not include any chip select signal;

23[i] wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;

23[j] wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;

23[k] wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects;

23[l][1] wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and

23[l][2] wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;

23[m][1] wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and

23[m][2] wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and

23[n] wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.

24[a] A dynamic random access memory (DRAM) package, comprising:

24[b] stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;

24[c] an interface via which the DRAM package receives C/A signals and receives or outputs data signals;

24[d][1] a control die coupled between the interface and the stacked DRAM dies,

24[d][2] the control die including signal conduits and logic configured to control at least some of the signal conduits; and

24[e] die interconnects, each die interconnect of the die interconnects coupled between at least one corresponding conduit in the control die and one corresponding signal port in each of a subset of the stacked DRAM dies, the each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;

24[f] wherein: the signal conduits include first conduits, second conduits, third conduits and fourth conduits;

24[g] the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;

24[h] each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;

24[i] each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;

24[j] each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;

24[k] each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not configurable to receive any signal from the corresponding fourth die interconnect;

24[l] the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;

24[m][1] in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and

24[m][2] a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;

24[n][1] in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and

24[n][2] a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;

24[o][1] in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the second set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and

24[o][2] a second subset of the third conduits is configured to receive one or more sixth signals associated with the second set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;

24[p][1] in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and

24[p][2] a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the second set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect;

24[q] each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;

24[r] each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;

24[s][1] the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;

24[s][2] the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;

24[s][3] the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and

24[s][4] the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.

25[a][1] The DRAM package of claim 24, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of a first subset of DRAM dies and not in electrical communication with any signal port of any of the second subset of DRAM dies,

25[a][2] wherein each of the second subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of the second subset of DRAM dies and not in electrical communication with any signal port of any of the first subset of DRAM dies, and wherein:

25[b] the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;

25[c] the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;

25[d] the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals;

25[e] the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals;

25[f] the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and

25[g] the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.

26[a][1] The DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals,

26[a][2] wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:

26[b] the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;

26[c] the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and

26[d] the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;

26[e] a conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.

27. The DRAM package of claim 25, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.

28. The DRAM package of claim 27, wherein the stacked DRAM dies include 16 stacked DRAM dies.

ADDENDUM B – U.S. PATENT NO. 10,025,731

1[a] A memory module operable to communicate data with a system memory controller via a memory bus in response to address and control signals from the system memory controller, comprising:

1[b] a printed circuit board comprising at least one connector configured to be operatively coupled to the memory bus, the at least one connector including a plurality of edge connections distributed along one or more edges of the printed circuit board;

1[c] a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus;

1[d] at least one circuit coupled between the at least one connector and the plurality of memory devices, the at least one circuit comprising a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices,

1[e][1] each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections,

1[e][2] the each correction circuit of the set of correction circuits including at least one programmable impedance matching circuit; and

1[f][1] control circuitry configured to receive the address and control signals from the system memory controller and to control the plurality of memory devices in response to the address and control signals,

1[f][2] wherein the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals.

2. The memory module of claim 1, wherein the at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit has dynamically programmable impedances whose values may differ depending on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals.

3. The memory module of claim 1, wherein the at least one impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit comprises at least one network of programmable resistors that is dynamically controllable.

4. The memory module of claim 1, wherein the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises one or more self-adjusting damper circuits.

5. The memory module of claim 1, wherein the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further comprises first one or more dynamically programmable repeater/amplifier elements.

6. The memory module of claim 1, wherein the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further includes a delay circuit that is configured to generate delayed versions of the signals transmitted between the respective port connection of the first set of port connections and the corresponding port connection in the second set of port connections.

7. The memory module of claim 1, wherein the number of port connections in the first set of port connections corresponds to a bit width of the memory bus.

8. The memory module of claim 1, wherein the at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of one of the plurality of memory devices.

9. The memory module of claim 1, wherein the at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of multiple memory devices of the plurality of memory devices.

10. The memory module of claim 1, wherein the control circuitry is configured to activate signal paths in the each circuit of the at least one circuit in response to the address and control signals.

11. The memory module of claim 1, wherein the control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals.

12. The memory module of claim 1, wherein the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements, and wherein the control circuitry is configured to activate the one or more circuit elements in response to the address and control signals.

13. The memory module of claim 1, wherein each circuit in the at least one circuit has a data width of 4, 8 or 16 bits.

14. The memory module of claim 1, wherein the at least one circuit is configured to improve signal integrity in signals transmitted between the at least one connector and the plurality of memory devices.

15. The memory module of claim 1, wherein the at least one circuit is configured to improve timing of signals transmitted between the at least one connector and the plurality of memory devices.

16. The memory module of claim 1, the at least one circuit is configured to improve power consumption by signals transmitted between the at least one connector and the plurality of memory devices.

17. The memory module of claim 1, wherein the at least one circuit includes signal paths, wherein the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals.

18. The memory module of claim 17, wherein the at least one circuit is further configured to provide a known static value to each port connection in the second set of port connections that is not in an active signal path.